공학박사학위논문

Silicide Induced Crystallization Phenomenon and Its Application for Low Temperature Polycrystalline Silicon Thin Film Transistors

실리사이드 유도 결정화 현상과 저온 다결정 실리콘 박막 트랜지스터의 적용에 관한 연구

2014 년 8 월

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Silicide Induced Crystallization Phenomenon and Its Application for Low Temperature Polycrystalline Silicon Thin Film Transistors

by

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ABSTRACT

Silicide Induced Crystallization Phenomenon and Its Application for Low Temperature Polycrystalline Silicon Thin Film Transistors

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After cathode ray tube (CRT) display in 1990s, the liquid crystal display (LCD) using thin film transistors (TFTs) with plasma display panel (PDP) using plasma led the display industry instead of CRT display as a result of the amorphous silicon (a-Si) TFTs have been integrated into the cheap glass substrate. Afterward the TFTs come to essential and fundamental electronic components in virtual all consumer and professional display products, from smart phones to large diagonal flat panel televisions. But recently, the active matrix light emitting diode (AMOLED) display worked by current receives attention from industry and academic. In order to meet the specific needs of AMOLED active material, a new active material having high field effect mobility became urgent requirement instead of a-Si which was used to active material on LCD panel because the a-Si exhibits low field-effect mobility and poor reliability. Many researchers concentrated on polycrystalline silicon (poly-Si), oxide type semiconductors, and organics to find new material. Among the new materials,

the poly-Si has been being focused by many researchers due to its high field-effect mobility and good reliability instead of oxide type compounds and organics having complicated processes, low field-effect mobility, and poor reliability. In industry, the excimer laser crystallization is used for crystallization of a-Si thin film. But its high cost and long time for process act as obstacles to realize the large area and the high resolution AMOLED.

In this study, the metal induced lateral crystallization (MILC), the unique alternate technology to supersede the laser crystallization, was advanced to a novel crystallization method – named silicide induced crystallization (SIC). The developed method could solve the problems of MILC technology such as low field-effect mobility and high leakage current. Particularly, we have concentrated on analyzing the mechanisms of leakage current through classification into two kinds of causes – trap assisted thermionic emission and pure tunneling due to lateral electric field.

In order to obtain a low leakage current with decreasing Ni contamination in the channel of the MILC poly-Si TFTs, the Ni silicide was used for crystallization instead of Ni thin film, and was confirmed the applicability of the low temperature poly-Si TFTs. The Ni silicide used in this study was formed by removal of Ni thin film right after sputtering deposition at room temperature. The Ni silicide density on the a-Si surface was increased with increasing sputtering temperature. Therefore, the net area of grain boundary was increased due to decreased grain size. It was experimentally demonstrated that the increased grain boundary degraded the electrical properties of the SIC poly-Si TFTs.

The silicide induced lateral crystallization (SILC) poly-Si TFTs was also fabricated by using room temperature silicidation demonstrated by SIC. The advantage of room temperature silicidation realized the high performance SILC poly-Si TFTs. Moreover,

the self-aligned structured MILC poly-Si TFTs, having bad electrical properties due to defect at MIC/MILC boundary, were developed by SILC technology.

It is well known that the MILC/MILC boundary (MMB) in the channel greatly affects the electrical properties of MILC poly-Si TFT. In this study, the asymmetrically formed silicide induced lateral crystallization method was also developed in order to eject the SILC/SILC boundary (SSB), formed by same mechanism of MILC growth, from the channel. Both a low off-state leakage current and a free short channel effect (kink effect) were observed in high electric-field conditions. Furthermore, it can be observed that the field-effect mobility and drain current noise were drastically improved by ejecting the SILC boundary in the source direction, when the trapped Ni silicide as scattering source was removed from the channel.

After crystallization using the MIC or SIC, Ni silicide residues remained on the poly-Si surface and they degrade the electrical properties of devices. To remove the remained Ni silicide residues after crystallization, the gettering process was applied in this study. It has noticed that not only the leakage current but also the driving characteristics such as the on-state current, the field-effect mobility, the threshold voltage, and the subthreshold slope were considerably improved by the gettering of Ni silicide in the poly-Si channel. Moreover, the reduced trap state density, main cause of improved electrical performance of gettered SIC poly-Si TFTs, was systemically analyzed through Levinson-Proano plot.

From analysis of second leakage current mechanism – pure tunneling emission at high lateral electric field, the lightly doped drain (LDD) structure was applied to SILC poly-Si TFTs. To form the LDD structure, gate insulator doping mask technique was

used. As a result, the LDD structure effectively suppressed the leakage current at high reverse bias region.

From the SILC method, the applications were expanded to previous studies on MILC poly-Si TFTS for better electrical performance. The first one is a channel splitting. The SILC poly-Si TFT having the split channel exhibits the improved driving characteristics because the Ni silicides at front of crystallites was filtered during lateral growth. Furthermore, the effective channel width was enlarged by channel splitting. The results were systemically analyzed by capacitance measurement and various electrical analyses. The second one is an electrical stress. The electrical stress enhanced not only leakage current but also driving characteristics. The electrical stress mechanism was modeled through experimental measurement at various electrical condition and computer simulation.

Since the developed processes in this study is not complicated technique, it can be easily applicable to potential future flat panel display applications.

Keywords: active matrix organic light remitting diode (AMOLED), low temperature polycrystalline silicon (LTPS), metal-induced lateral crystallization (MILC), thin film transistor (TFT), silicide, gettering, electrical stress, leakage current, field effect mobility

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Figure B.2 MILC dependency on doped area. B_2H_6 and PH_3 were doped after the deposition of Ni thin films and they were annealed at 550 °C 4 times.

Figure B.3 Optical microscope images of crystallized Si in case of (a) doped Si and (b) undoped Si.

Figure B.4 MILC dependency on doping time. B_2H_6 and PH_3 were doped 2 times interval after the Ni thin film deposition.

CHAPTER 1

Introduction

1.1 Thin Film Transistors for Display

THIN FILM TRANSISTORs (TFTs) have been intensively researched for possible electronic and display applications in the last two decade, and become the main stream of the electronic flat panel display industry, just as Si chips were earlier called the rice or staple of the computer revolution. Tens of giants factories today produce millions of displays each year, with each display incorporating several million thin film transistors.

How we got to this point is an interesting tale of technology evolution and development that stretches over nearly 70 years, going back to the earliest days of semiconductor physics. It was at that time that materials were first being classified according to their electronic structure so that semiconductors were understood not just as materials with conductivity intermediate between that of metals and insulator, but as crystalline materials with small number of mobile charges per unit cell and a distinguishing temperature dependence of conductivity. Looking back, we can see that the concept of the thin-film transistor and its potential utility significantly predated the

device that gave rice to the term "transistor". Indeed, for many years it was overshadowed by the astounding developments associated with the original bipolar transistor and its technological cousin, the metal oxide semiconductor field-effect transistor (MOSFET) [1.1].

In this chapter we will systematically introduce, how the TFT has evolved in materials and structure to the forms most widely used today.

1.1.1 History of Thin-Film Transistors

It is mostly cited in papers that field-effect device was firstly invented by Lilienfeld in his patent in 1934 - Figure 1.1(a) [1.2], but as argued by Brody [1.3]. Heil has a more solid claim to the inventorship of TFT in his patent in 1935 - Figure 1.1(b) [1.4] in which Heil showed the knowledge and understanding of semiconductors and showed a correct device structure. However, these two patents seem to be concept patents only without any indication of practice or experimental.

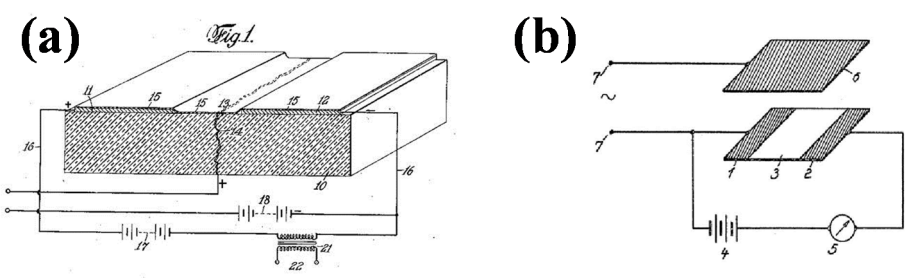


Figure 1.1 Schematic diagrams of (a) Lilinenfeld's patent and (b) Heil's patent about field effect device [1.2, 1.4].

Based on understanding of the Schottky diode, i.e., a metal-semiconductor contact, Shockley represented the invention of the metal-semiconductor field-effect transistor (MESFET) in 1939. In his first idea of a triode where a grid embedded in semiconductor material could be used to deplete a zone between the cathode and anode, cutting off the flow of current. After realizing such a structure might be difficult to make, he adapted to applying an electric field to a semiconductor film by making use of an insulator and a gate electrode. He made a thin-film field-effect device with a germanium film. However, the device performance was disappointing as the change in the conductivity observed was far smaller than that of theoretically expected based on the gate capacitance because of the lower carrier mobility of the induced charges and the existence of a large number of surface states.

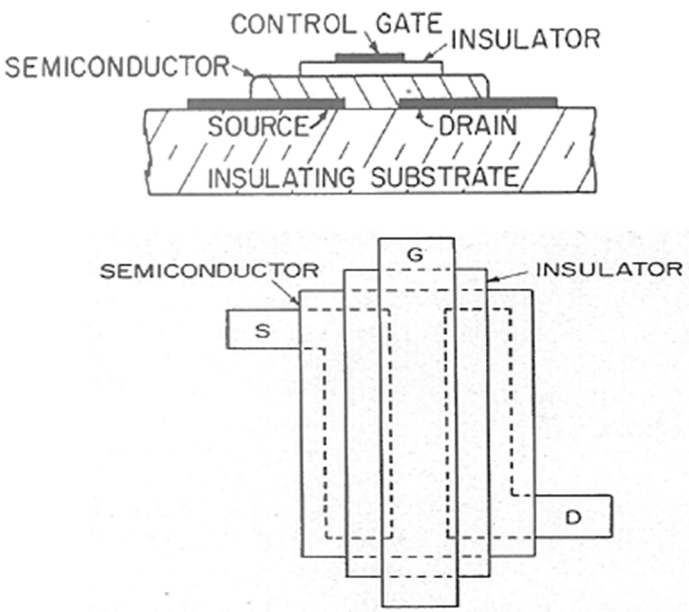


Figure 1.2 Schematic cross sectional (top) and plan (bottom) views of Weimer's top-gate CdS TFT structure [1.5].

The history of the TFT really began with the work of P. K. Weimer at RCA laboratories in 1962 [1.5]. He used a thin-film of polycrystalline cadmium sulfide (CdS), together with insulating films such as Si monoxide in a staggered structure, with the source and drain contacts on the opposite side of the film from the gate - Figure 1.2. Weimer achieved a transconductance of 25000 μA/V for a gate capacitance value of about 50 pF and oscillation frequency close to 20 MHz. Shortly after Weimer's report, F. V. Shallcross [1.6] reported very similar results for TFTs made with cadmium selenide (CdSe). In 1964 Weimer reported *p*-channel TFTs with tellurium as the active material [1.7].

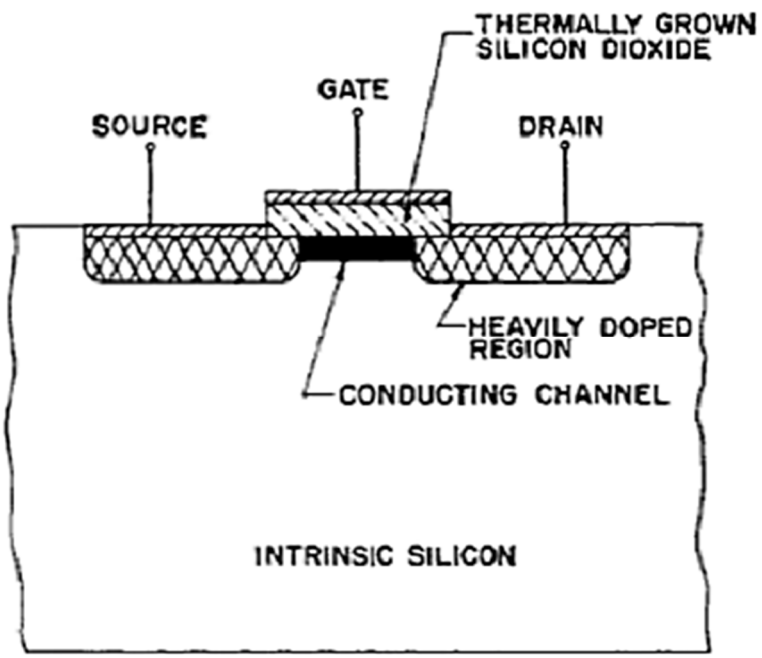


Figure 1.3 Schematic cross sectional of an insulated-gate field-effect transistor (IGFET) in crystalline Si [1.8].

With the appearance of insulated-gate field-effect transistor (IGFET) – Figure 1.3 [1.8], now known as MOSFET, in 1962 and the probability of more dense integrated circuit chips, the expectation of cost saving with TFT technology is difficult to sustain. This led to a decline in TFT development activity by the end of the 1960s. The golden opportunity for TFTs appeared again when people noticed that low cost is inseparable from small chip size for crystalline Si and at the same time large arrays of low-cost electronics are required for some applications, such as liquid crystal displays. By 1973 T. P. Brody and his group had demonstrated a liquid crystal display with CdSe TFTs [1.9]. However, such kinds of TFTs suffer from poor DC stability [1.10].

After it had been discovered that hydrogenated amorphous Si (a-Si:H), in contrast to pure amorphous Si (a-Si), could be doped with donors or acceptors to induce *n*- or *p*-type conductivity [1.11], TFTs using a-Si as the active material was introduced in 1979 [1.12]. Up to the end of 1980s, many companies had mastered the art of making a-Si TFTs having considerably good electrical performances such as low off current (<1 pA), good on/off ratio (>10^7), reasonable mobility (0.5-1.0 cm^2/Vs) and good stability. Low temperature polycrystalline silicon (LTPS) TFTs were fabricated by Morozumi *et al.* [1.13] with a low off current (<0.1 pA) and a high on/off ratio (>10^7), but the mobility is low (~2-3 cm^2/Vs). High performance polycrystalline silicon (poly-Si) TFTs were fabricated by recrystallization of a-Si to poly-Si as active layer at a high temperature [1.14]. LTPS TFTs with characteristics as good as that of high temperature poly-Si TFTs were reported by Little *et al* [1.15] in 1991. In 1990 a new class of TFT based on organic semiconductor active layer material was reported [1.16] and afterwards investigated intensively for the fabrication of displays on flexible substrates.

1.1.2 Flat Panel Displays (FPDs)

Electronic displays, including cathode-ray tube (CRT), plasma display panel (PDP), light-emitting diode (LED) display, organic light-emitting diode (OLED) display, liquid crystal display (LCD), etc., are widely used in our personal and professional lives. They are of different structures, advantages, and operation principles.

The CRT is the oldest while still an important electronic display technology. It is widely has been used for televisions (TVs) and personal computer (PC) monitors. It has the advantages including mature manufacturing, high display quality in brightness contrast ratio, resolution, color rendering, response and view angle, and at the same time, intrinsic disadvantages including large volume, heavy weight, high power consumption and large heat generation.

Owing to its obvious advantages, such as thin, light, small volume, low power dissipation, which just remedy the drawbacks of CRT, flat-panel display (FPD) is becoming a more and more important branch of electronic displays. This technology develops fast and occupies a larger display market. LCD is the most important FPD technology and takes up to 75% f the FPD market [1.17].

Addressable LCDs can be separated into two types, passive-matrix (PM) and active-matrix (AM) LCDs.

Passive-Matrix-Liquid Crystal Display (PMLCD)

The schematic structure of an PMLCD is shown in Figure 1.4(a). The PM LCDs use a simple grid to supply the voltage to a particular pixel on the display. Such grids are created starting with two glass layers called substrates. One substrate is given columns. The other is given rows. The rows or columns are connected to integrated

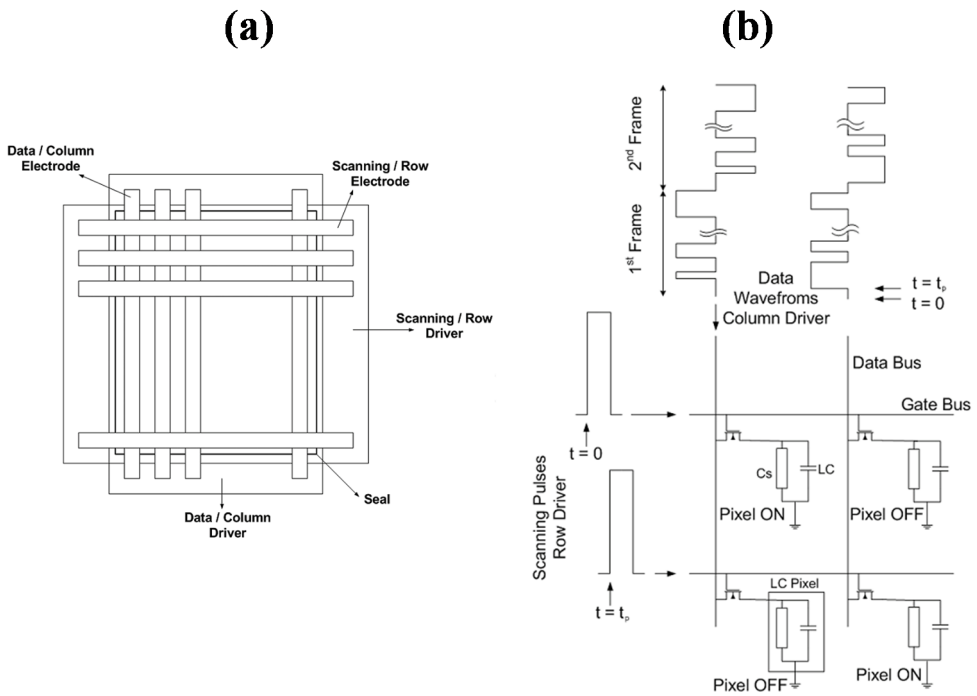


Figure 1.4 Schematic structure of an (a) PMLCD and (b) AMLCD.

circuits that control the time when a voltage is sent down a particular column or row. The liquid crystal material is sandwiched between these two glass substrates. To turn on a pixel, the integrated circuit sends a voltage down the correct column of one substrate and a ground activated on the correct row of the other. The row and column intersect at the designated pixel, and that delivers the voltage to control the liquid crystals at that pixel. The drawbacks of PM include slow response time and imprecise voltage control, which will result in "ghost" and fuzzy images or images lacking in contrast, respectively.

The PM is typically restricted to small display sizes due to issues with image quality that arise as the size and resolution of the display increase. Improvements on

the liquid crystal material and the associated addressing schemes have extended the applicability range of PM addressed panels beyond the limits predicted by conventional technologies. Despite such improvements, however, the intrinsic limitations of PM technology have restricted the application range of PM panels and positioned AM addressing as the technology of choice for high-end display applications.

Active-Matrix-Liquid Crystal Display (AMLCD)

The schematic structure of an AMLCD and the schematic pixel circuit are shown in Figure 1.4(b) and Figure 1.5(a), respectively. AM addressing uses independent electronic switches to individually control the state of each pixel. In this manner, the display performance is free of the shortcomings of PM addressing schemes. AM essentially consists of TFTs, storage capacitor and peripheral driver circuits. The peripheral driver circuits could be either implemented in the form of Si chips which are then mounted onto the substrate or directly fabricated on the substrate when the TFT arrays are fabricated.

The schematic structure of an AMLCD and the schematic pixel circuit are shown in Figure 1.4 and Figure 1.5a, respectively. TFTs are needed to charge pixel capacitors, each consisting of a liquid crystal capacitor (C_{lc}) and a storage capacitor (C_s). When the TFTs in one row are turned on, data writing will be performed in the pixels of this row with C_{lc} and C_s charged up, the pixels in other rows will not be affected. When the TFTs are turned off, charge stored in the storage capacitors will be held for a limited period of time until the next refresh cycle. The hold voltage signal is used to control the state of the liquid crystal molecule and determine the optical state of the pixel.

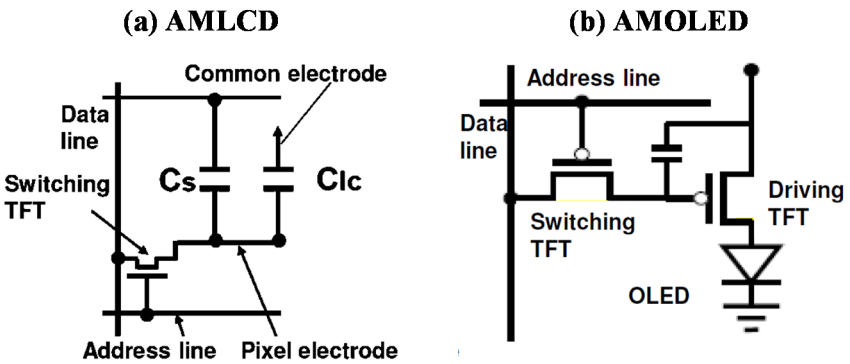


Figure 1.5 Schematic pixel circuit of a pixel in a (a) AMLCD and (b) AMOLED.

Table 1.1 Comparison between (a) AMLCD and (b) AMOLED.

	AMLCD	AMOLED
Active Materials	a-Si	Poly-Si
Mobility	Low mobility (0.5~1 cm^2/Vs) Low current Low definition (TFT size)	High mobility (20~250cm^2/Vs) High definition
Driving	Voltage Driving	Current Driving
Problem	Only N-type Driving Ohmic contact problem between silicon and TCO	Crystallization Process
Flexible	Bad - Cell-gap change - Back light unit	Good
Transparent	Bad - Color Filter, Back Light Unit	Good
3-D	Good	Bad

Active-Matrix Organic Light-Emitting Diode (AMOLED)

OLED display is another important branch of FPDs, which shows great potential to replace LCD due to its superior characteristics, such as self-emission, video rate response, wide view-angle and thin form factor. Unlike the optical state of a pixel in a

LCD that can be voltage-switched using a single TFT, current-controlled emission of an OLED pixel requires at least two TFTs, one as a switch and the other as a current supplier as shown in Figure 1.5(b). Sometimes, four or more TFTs are used to compensate for the dispersed threshold voltages and drain currents of the driving TFTs to improve the display uniformity. The switch TFT's function is similar to that in AMLCD to control the transferring of the data signals. When the switch TFT is turned on, the data signals are transferred to the gate of the driving TFT and a corresponding driving current will be supplied to the OLED. The storage capacitor will be charged up at the same time. The data signals maintained by C_s allow the driving TFT to continue supplying current to the OLED when the switch TFT is turned off. The comparison between AMLCD and AMOLED is briefly shown in Table 1.1.

1.2 Material Issues in TFTs

1.2.1 Amorphous Silicon (a-Si)

The a-Si:H was first used as an active channel material to fabricate TFTs for switches of LCD. Also a-Si is widely used as low cost solar cell material. The advantage of a-Si is the low temperature process (below 300 °C), good uniformity and low cost. However, the disadvantage of a-Si is its poor stability and low field-effect mobility due to the large amount of dangling bonds which acts as recombination states of electrons and holes. The devices show considerable threshold voltage shift during

operation. The low field-effect mobility of a-Si TFT (~1 cm^2/Vs) constraints future application for OLED or high performance circuits.

1.2.2 Oxide Type Semiconductors

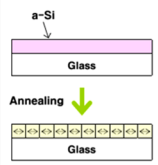
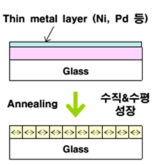
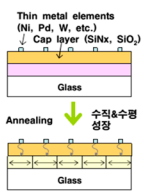
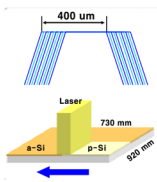
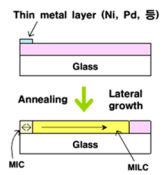
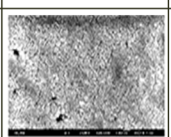
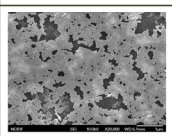
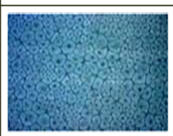
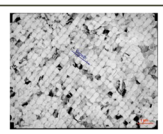
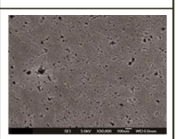
Transparent conductive oxides (TCOs) are unique materials because they are both electrically conductive and visually transparent. Initially, they are widely used as simple passive electrical or optical coatings, such as in antistatic coatings, touch display panels, solar cells, flat panel displays, and optical coatings. The TCOs such as indium-tin oxide (ITO) and zinc oxide (ZnO) have found applications as electrical interconnections and as window electrodes in FPDs and solar cells. Recently ZnO has attracted lots interest in the application as channel material for TFTs with aluminum zinc oxide (AZO). Single-crystal $InGaZnO_4$ TFT with the field-effect mobility of 80 cm^2/Vs and amorphous $InGaZnO_4$ TFT with the field-effect mobility of 20 cm^2/Vs have been reported. The advantages of ZnO based TFTs are higher mobility than a-Si and better uniformity than poly-Si. However, the lower mobility of ZnO TFTs than poly-Si limits its further application for high performance integrated circuits (ICs), such as radio frequency (RF) circuits, logic circuits, analog amplifies, and AMOLED. Particularly, The low field-effect mobility cause result of low definition of panel. Therefore, the oxide type semiconductor for AMOLED actually give up in industry.

1.2.3 Low Temperature Polycrystalline Silicon

The motivation of using poly-Si as channel material for TFTs is the higher field-effect mobility (50~300 cm^2/Vs) than that of a-Si or oxide type semiconductors, which means that for the same on-current, the size of the poly-Si TFT is much smaller than that of a-Si. This results in higher aperture ratio and higher resolution for displays. Also the driver circuits can be integrated peripherally on displays due to the increased mobility of poly-Si TFTs. Poly-Si TFTs also show better stability than that of a-Si TFTs and they have no threshold voltage shift under electrical stress. The high mobility and high electrical stability of poly-Si TFTs are very suitable for AMOLED switches which require TFTs with high drive current and good electrical reliability. However, for small grain (<1μm) poly-Si TFT, the disadvantage is the low mobility (<100 cm^2/Vs) due to dense grain boundaries inside and between grains in the channel region. The grain boundaries act as trap states which decrease the field effect mobility of electrons and holes. For large grain (>1 μm) poly-Si TFT, the disadvantage is the poor uniformity of the motilities due to the fact that location of the large grain size is random. Although there are several technologies to control the location of the large grains, the orientations of the large grains are still random. In order to deposit high quality poly-Si, several technologies are proposed: direct deposition by chemical vapor deposition (CVD); solid phase crystallization (SPC) of a-Si by high temperature thermal annealing (>600 °C) or metal induced lateral crystallization (MILC); liquid phase crystallization by laser crystallization such as zone melting regrowth (ZMR), and excimer laser annealing (ELA). Laser crystallization of a-Si film can produce high performance poly-Si. However, if the laser energy is below complete melt of the a-Si film, the grains are small (<1 μm) and the mobility is low (<100 cm^2/Vs). If the laser

energy is above CM, large grains (>1 μm) are formed and the mobility can up to 300 cm^2/Vs. However, the large grains are randomly located and the orientations of the grains are random which result in a high variation of the field effect mobilities. The crystallization methods are summarized in Table 1.2.

Table 1.2 The major crystallization methods.

Method	Solid Phase Crystallization (SPC)	Metal Induced Crystallization (MIC)	Super Grained Silicon (SGS)	Excimer Laser Annealing (ELA)	Metal Induced Lateral Crystallization (MILC)
Process					
Micro-Structure					
Remarks	-Simple Process -High Temperature (600°C~750°C) -Substrate Shrinkage	-Ni Silicide Catalyst -Low Temperature (<550°C) -Small Grain -Metal Contamination (Leakage current Low Mobility)	-Good Crystallinity -Low Contamination -Large Grain -Complex Process (Dep.-Etch-Dep.) -Leakage Current	-Good Crystallinity -Surface Roughness -Direction Dependence -Expensive Process -Large Area Limit	-Good Crystallinity -Low Contamination -Add. Mask -Leakage Current

1.3 Objective of the Dissertation

A LTPS TFT fabrication process is necessary for the realization of display panels in cheap display-grade glass substrates to avoid glass shrinkage and pattern distortion. The maximum fabrication temperature is commonly constrained to less than 600-650 °C.

a-Si:H TFT is widely used in AMLCDs because of the simple and low temperature TFT fabrication process, capability of large-area and uniform a-Si film preparation. But there are a large number of localized band sate distributing throughout the bandgap of a-Si:H even with the passivation of most of the dangling bonds with hydrogen atoms. In a-Si:H TFTs, carriers have to fill up the localized states and Fermi level has to move through energy levels of deep and shallow trap states before conduction begins. This increases the threshold voltage and reduces the field-effect mobility. Field-effect mobility of 0.4 ~ 1.5 cm^2/Vs for electrons and much lower field-effect mobility of $2 \times 10^{-4} \sim 7 \times 10^{-4}$ cm^2/Vs for holes [1.18-1.23] limit the application of a-Si:H TFTs to pixel switches. In addition, because of the low field-effect mobility, large channel width, usually in the order of 100 μm, with a channel length of 8-10 μm is required to provide an adequate drive current. The large device size reduces the aperture ratio, resolution and brightness of the display. a-Si:H TFT also suffers from long time performance degradation.

Poly-Si TFTs have many advantages over a-Si:H TFTs as pixel active elements. Poly-Si consists of locally ordered grains with grain boundaries in between, so the field-effect mobility of poly-Si TFTs is usually much higher than that of a-Si TFTs. As to the higher field-effect mobility, the size of the poly-Si TFT can be reduced which will increase the aperture ratio, brightness and consequently reduce the power consumption of the display. Low-temperature poly-Si could be obtained using a variety of techniques, such as SPC, ELA and MILC.

Usually, as-deposited poly-Si film consists of grains in the order of hundreds of nanometer, SPC poly-Si with larger grains could be achieved by recrystallization of a-Si with Si implantation [1.24] or crystallization of precursor a-Si at a temperature around 600°C for a long time of tens of hours [1.25]. The crystallized grain grows

from spontaneous nucleation, so both the orientations of crystallized grains and the grain boundaries are random. The grain size of the poly-Si is affected by the microstructure of the precursor a-Si, grain size up to 2~5 μm has been reported [1.24, 1.25]. The SPC process is simple while it requires relatively high process temperature and long crystallization time which are big problems for commonly used glass substrates.

Laser crystallization has been widely used as a low-temperature technology to prepare high quality poly-Si films with few defects. The a-Si film is heated to melt with laser irradiation in a short time and cools down after the irradiation, through which the molten a-Si solidifies and transforms into poly-Si. The damage to the commonly used glass substrate can be minimized by choosing a short-wavelength and short-pulse laser. Both excimer laser [1.26] and continuous-wave laser [1.27] have been reported to be used to fabricate high quality poly-Si and high performance poly-Si TFTs. The drawbacks of this technique are the high equipment cost, complex processing, inherent energy variant, and sensitivity of poly-Si quality to the laser energy density.

Low-temperature crystallization of a-Si is also possible by using some metals as crystallization catalyst to reduce the phase-change energy from a-Si to poly-Si. The metals can be classified into two groups, one includes eutectic-forming metals such as Ag, Au, Al, Sb, and In, and the other includes silicide-forming metals such as Pd, Ti, Ni, and Cu. Atoms of the former kind of metals dissolved in a-Si films may weaken Si bonds and enhance nucleation of crystalline Si [1.28]. Among the latter kind of metals, Ni is the mostly used crystallization catalyst as Ni silicide has the same crystalline structure as Si with only 0.4% lattice constant difference [1.29]. During the

crystallization process, a-Si is continuously transformed to poly-Si such that the poly-Si film consists of longitudinal grains and continuous grain boundaries [1.30].

Initially, TFTs with bilaterally crystallized poly-Si channel and self-aligned metal induced crystallized (MIC) poly-Si source/drain were proposed [1.31], but the highly defective MIC region at the drain junction leads to early drain breakdown and high leakage current [1.32]. New methods of introducing Ni to crystallize a-Si have been reported to either simplify the crystallization process [1.34] or fabricate high quality poly-Si [1.35]. Further improvement of the MILC poly-Si quality by a combination of MILC and post-crystallization, such as high temperature annealing [1.36] and laser annealing [1.37], has also been reported.

1.4 Organization of the Dissertation

New technologies, aiming at fabricating low temperature poly-Si TFTs having low leakage current and excellent driving characteristics, were proposed and successfully demonstrated in this research. This dissertation is consist of six chapters and organized as follows:

Chapter 2 Background and Previous Works. In order to understand this dissertation, basic theories and physical models are needed. Therefore this chapter gives an overview of the crystallization method of :SPC, ELA, and MILC etc. and simple physical models using mathematical formulations of TFT driving. Moreover, the determinations of device key parameters used in this dissertation are presented.

Chapter 3 Experimental Procedures describes the experimental procedures, including the preparation of samples and the development of fabrication processes to

make high performance MILC poly-Si TFTs having low leakage current. First, the conventional fabrication process of MILC poly-Si TFTs is introduced. Next, the direction of experimental is categorized according to 1) crystallization using minimum Ni catalyst, 2) removal of trapped Ni silicide residues using gettering and asymmetrically deposited Ni on the source and drain, and 3) lightly doped drain structure for suppression leakage current at high reverse gate bias region.

Chapter 4 Reduction of the Leakage Current will describes the leakage current mechanism in poly-Si TFTs and to achieve the low leakage current poly-Si TFTs, three kinds of fabrication method was developed. First *silicide induced crystallization* (SIC) using minimum Ni catalyst to decrease minimum leakage current at low reverse gate bias. Second is a novel process named "thin film gettering" to remove Ni silicide residues on the surface of active layer. The last is *lightly doped drain* (LDD) structure for suppression leakage current at high reverse gate bias region.

Chapter 5 Enhancement of Driving Characteristics will introduce three kinds of process development for high performance poly-Si TFTs. First is "*split channel structure*" to improve driving characteristics, subthreshold slope, on-state current, and field-effect mobility, of poly-Si TFTs. The second is "*electrical stress*". In order to investigate device stability, electrical stress was frequently used by many researchers. But in this study, the electrical stress was used the method for electrical performance improvement.

Chapter 6 Conclusion and Future Work will concludes the dissertation with a summary and suggestions for future research.

CHAPTER 2

Background and Previous Works

2.1 Low Temperature Polycrystalline Silicon (LTPS)

POLY-SI exhibits advantages over a-Si technology on the achievable size vs. resolution limits for the display, as well as the opportunity to monolithically integrate additional functionality on the panel. The advantages of poly-Si are the significant performance gains of poly-Si TFTs over a-Si TFTs and its compatibility with complementary metal-oxide semiconductor (CMOS) fabrication. CMOS technology enables monolithic integration of peripheral drivers on panel, as well as opportunities for the addition of other value-added components on the display [2.1, 2.2].

In addition, many researches are concentrated on the AMOLED [2.3, 2.4] because of its low cost, low power consumption, wide viewing angle, and the possibility to be made on flexible substrates. For the pixel element of OLED, poly-Si TFTs are better than a-Si:H TFTs, because OLED is current-driving type and needs more current, while LCD is voltage-driving type.

Unlike MOSFET devices, the TFT active layer needs to be formed on such amorphous host material and that the temperature of all associated processing has to be constrained within the allowable rage prescribed by the materials characteristics of the substrate. For current display-glass substrates, the maximum processing temperature needs to be kept below ~650 °C. To form poly-Si TFTs on the commercial glass substrates, a number of researches have been carried on some methods.

Poly-Si thin films can directly be deposited on glass over 600 °C by PECVD but their electrical properties are inadequate for TFTs [2.5]. Therefore most of research groups have focused on the methods to crystallized a-Si thin films below 650 °C. The most direct method of obtaining poly-Si films from a-Si films is via SPC. However, it needs long time annealing during over 20 h at 600 °C and quality of poly-Si is not enough to make high performance poly-Si TFTs [2.6].

ELA uses excimer laser as a type of gas laser from an inert atom and halide atom. a-Si films are melted by laser irradiation during very short period, ~220 ns, and they are crystallized simultaneously with the solidification [2.7]. This method is also allowable to flexible substrate and can make high mobility poly-Si TFTs, but there are some problems on the productivity, surface roughness, non-uniformity of poly-Si.

Recently, many researches are concentrated on the MILC and MIC. They will be commented at following chapter.

2.2 Metal-Induced Lateral Crystallization (MILC)

The crystallization temperature of a-Si can be lowered by the addition of some metals into a-Si and it is called as MIC. The MIC is induced by some metals such as Au [2.8], Al [2.9], Sb [2.10], and In [2.11], which form eutectics with Si, or metals such as Pd, Ti, and Ni [2.12, 2.13], which form silicides with Si. These metals have been added to a-Si to enhance the nucleation rate. Some of these cases were reported to be successful in lowering the crystallization temperature down to 500 °C. The MIC process, however, has a serious drawback of undesirable incorporation of metal impurities into Si, so that it has not been applicable to the fabrication of TFTs. For example, the crystallization temperature of Al-Si is reported to be as low as 170 °C, but Al is an acceptor-type dopant within Si [2.14].

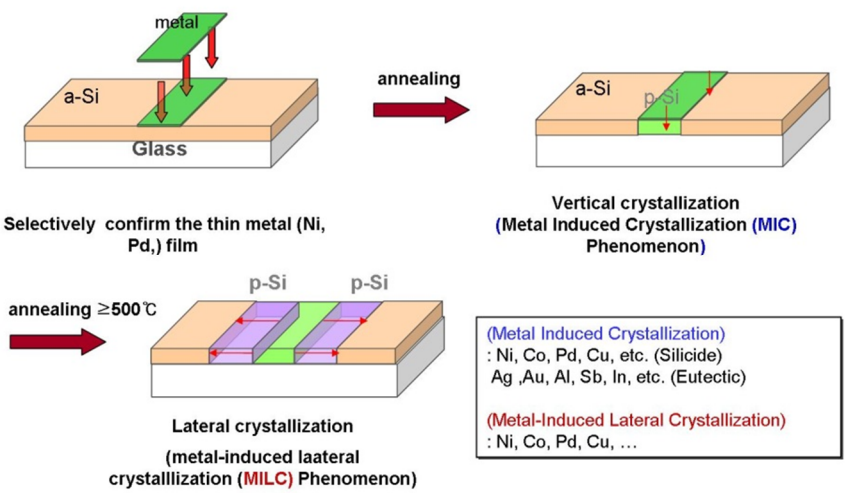


Figure 2.1 The metal-induced lateral crystallization (MILC) process flows.

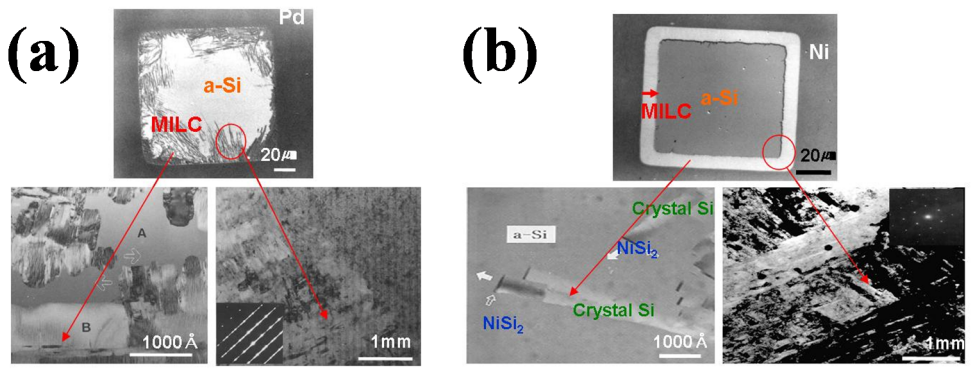


Figure 2.2 The microstructure of (a) Pd-induced lateral crystallization (b) Ni-induced lateral crystallization.

Hence, it is of great significance to minimize the amount of metal incorporation into Si while a lower crystallization temperature is preferable. Liu and Fonash firstly showed that MIC can be applied to the fabrication of poly-Si TFTs, where they tried to minimize the metal contamination by depositing an ultra-thin Pd layer under a-Si films. Though they were able to reduce the crystallization annealing time, the crystallization temperature was still kept at 600 °C.

More recently, a different crystallization phenomenon has been reported, where MIC could be extended laterally into the metal-free areas over 100 μm and this MILC has been known to take place for Pd, Ni, at temperatures lower than 500 °C [2.15, 2.16]. The MILC can provide large grained poly-Si films as well as low temperature crystallization. Figure 2.1 briefly shows the MILC process. Also Figure 2.2 indicates the microstructures of Pd-induced lateral crystallization and Ni-induced lateral crystallization respectively. The a-Si region contact with metal layer is crystallized by MIC and poly-Si grains laterally grow toward a-Si region where does not contact with

metal layer. Thus MILC poly-Si region has lower metal contamination than MIC region [2.17~2.19].

According to MILC reaction model [2.20], MILC phenomenon is caused by strain-stress among a-Si, metal silicide, and c-Si layers. At the tip of the lateral crystallization, there is a silicide of less than 50 Å in thickness, which moves into the a-Si leaving the poly-Si behind, as shown in Figure 2.2. The schematic drawing for this reaction is illustrated in Figure 2.3. For the catalytic phase transformation to occur, three different atomic fluxes are required in the system. Firstly, the bond breaking of a-Si atoms and migration of each atom towards the interface between a-Si and the silicide designated as /1/ in Figure 2.3 (F1). Migrated Si atoms are to be adsorbed at the silicide surface to create the metal vacancies. Secondly, the hopping of the above-mentioned created metal vacancies inside the silicide to reach the interface between the silicide and poly-Si designated as /2/ (F2). Hopping of the metal vacancies should be coupled with the metal ions in the silicide. Finally, the rearrangement of the dissociated Si atoms at /2/ to be attached to the dangling bonds of the poly crystal (F3). Phase transformation of one atomic layer can be completed by the rearrangement of dissociated Si atoms at /2/. In a steady state, F1 should be equal to F2 and F3.

Since there is a volume expansion at /1/ and shrinkage at /2/, corresponding tensile and compressive stresses would be created. For Pd-MILC the volume is calculated to expand by two times at /2/ and to contract in half at /1/. Therefore the tensile stress drives the bond breaking of a-Si and the migration of Si atoms for adsorption at the silicide surface of /1/, while compressive stress built at /2/ would facilitate the atomic rearrangement. For Ni-MILC, the respective volumes occupied by one Si atom in crystalline, Ni silicide and a-Si are calculated to be 20.0, 19.9, and 20.3%. This

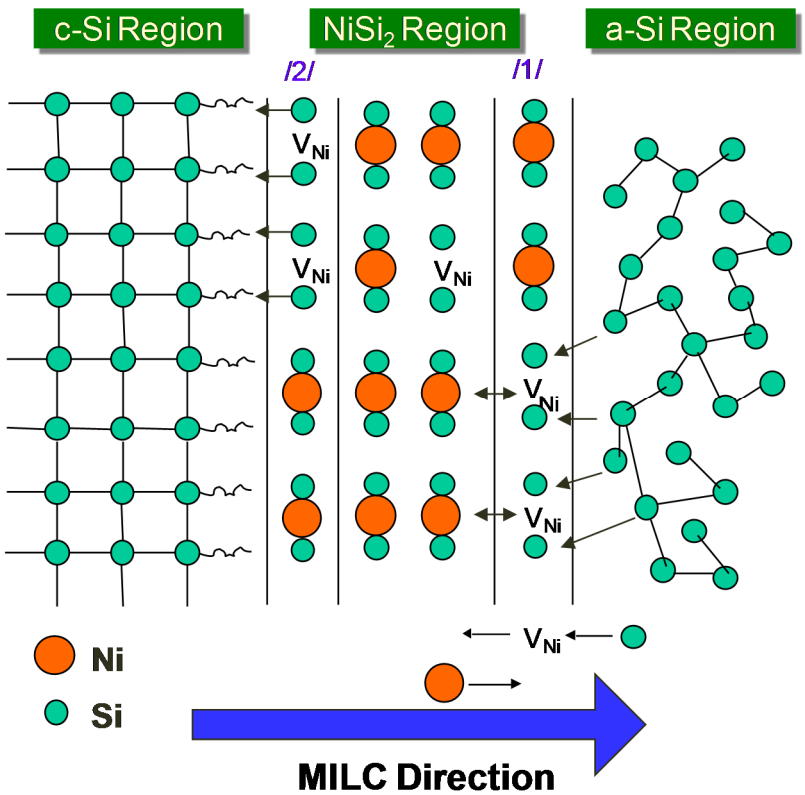


Figure 2.3 Schematic illustrations of the MILC reaction model. 1st step: Si bond breaking and coherent adsorption to the interface /1/ (Ni vacancy formation), 2nd step: Ni ion and Ni vacancy hopping, and 3rd step: Si atom coherent rearrangement.

means that almost no volume change occurs at either interface /1/ of /2/ for Ni-MILC. This fact is related to the MILC growth rate and the adjacent metal effect.

Vacancy motion inside the silicide, which has to be coupled with the metal ions in the reverse direction, can be driven by the thermodynamic equilibrium potential difference between /1/ and /2/. It is known that a-Si can accommodate more metal elements than poly-Si, thermodynamically, so that the charged metal ions have to move toward /1/ [2.16]. Also, MILC reaction model will be analyzed in detail.

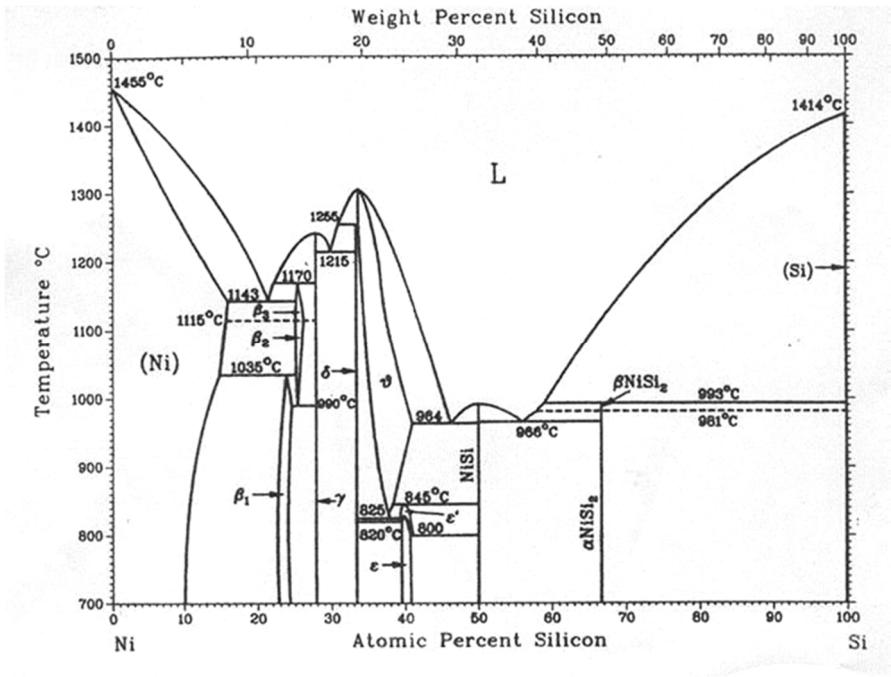


Figure 2.4 Ni-Si phase diagram. β1 : Ni_4Si, β_2 & β_3 : Ni_3Si, Γ : $Ni_{31}Si_{12}$, θ & δ : Ni_2Si, ε : Ni_3Si_2 .

A. Silicide formation

When a thick Ni film (> 100 Å) is deposited on a c-Si substrate and annealed, Ni rich phase of orthorhombic Ni_2Si with the $PbCl_2$ structure is formed by a diffusion controlled process at temperatures as low as ~ 200 °C. Annealing at temperatures in the range 350 ~ 750 °C leads to a diffusion-controlled transformation of Ni_2Si into the monosilicide of NiSi, which is also orthorhombic with the MnP structure [2.21]. Ni has been found to be the dominant diffusing species in the formation of Ni_2Si [2.22, 2.23] and NiSi [2.24, 2.25]. The transport of Si through NiSi has also been studied, although rather poor epitaxial layers of c-Si were observed [2.26]. At temperatures in the range 450 ~ 750 °C, the NiSi transforms into the thermodynamically favored end

phase, $NiSi_2$ [2.27, 2.28]. The high transformation temperature has been attributed to nucleation-controlled kinetics, and Ni has again been observed to be the fast diffusing species [2.29]. The disilicide $NiSi_2$ is cubic with the CaF structure and has a very close lattice parameter match to c-Si (~0.4%). Therefore, $NiSi_2$ coherently confirmed on the c-Si layer.

B. Nucleation of c-Si

The phase transformation of a-Si to c-Si is mediated by $NiSi_2$ precipitates. Crystalline Si nucleates on one or more of the eight {111} faces of the octahedral $NiSi_2$. The $NiSi_2$ is metallic with a very low resistivity of 35 μΩcm and an extremely good lattice match with c-Si. The phenomenon of metal-induced crystallization is thought to be due to an interaction of the free electrons of the metal with the covalent Si bonds at a growing interface [2.30]. The small misfit (0.4%) between $NiSi_2$ and Si facilitates the formation of epitaxial c-Si on the {111} faces of the $NiSi_2$ precipitates. Localized networks of c-Si trails were often single crystal, despite the observation of $NiSi_2$ precipitates at the leading edge of each trail. Migration of $NiSi_2$ led to epitaxial growth of Si constrained to <111> directions. Impingement of migrating silicide precipitates with stationary precipitates promoted further epitaxial growth on variants of the (111) face.

C. Growth of MILC epitaxial c-Si

Following nucleation of c-Si on the $NiSi_2$ precipitates, growth always proceeded with a $NiSi_2$ precipitate at the planar advancing growth front. Many reports confirmed that the growth rate for each individual needle was dependent upon the $NiSi_2$ thickness in the growth direction. Many $NiSi_2$ fanned out, decreased in thickness, and

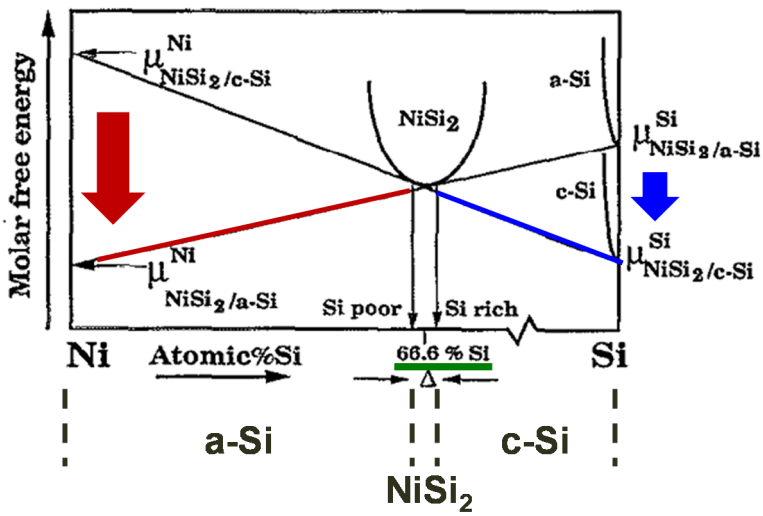


Figure 2.5 Schematic equilibrium molar free-energy diagram for NiSi2 in contact with a-Si and c-Si.

were observed to migrate more rapidly. In general, the trails of c-Si developed a needlelike morphology because lateral growth of the a-Si/c-Si interface via conventional solid phase epitaxial growth occurred much more slowly. The c-Si needles were frequently seen to fan out, with a consequent reduction in the $NiSi_2$ thickness. At the same time, the growth velocity increased with decreasing $NiSi_2$ thickness.

The driving force for the phase transformation is the reduction in free energy associated with the transformation of meta-stable a-Si to stable c-Si [2.31]. Figure 2.5 shows the schematic equilibrium molar free-energy diagram for $NiSi_2$ in contact with a-Si and c-Si. The chemical potential of the Ni atoms is lower at the NiSi/a-Si interface, whereas the chemical potential of the Si atoms is lower at the $NiSi_2$/c-Si interface. For a migrating $NiSi_2$ precipitate consuming a-Si at the leading interface and

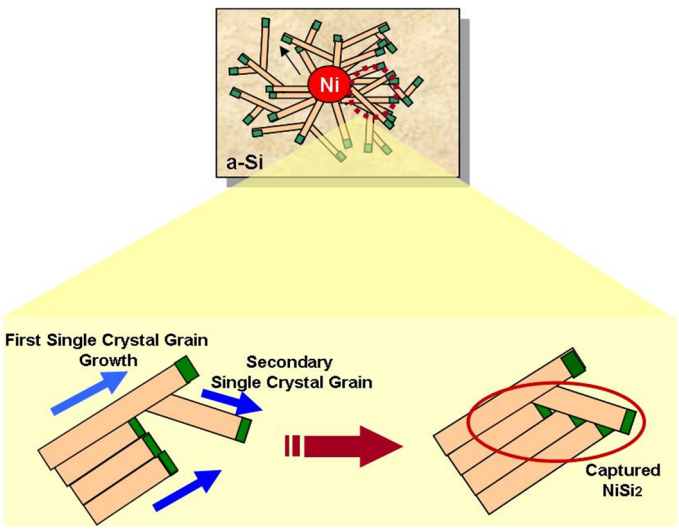


Figure 2.6 The phenomenon of caused grain-boundary defects during MILC process.

forming a trail of epitaxial c-Si, there is a driving force for the forward diffusion of Ni atoms through the $NiSi_2$ and a driving force for the diffusion of Si atoms in the reverse direction through the $NiSi_2$.

The MILC has many advantages such as large grains without defects [2.32], low temperature processes, smooth surface, high crystalline uniformity and low process cost, etc. Thus, MILC poly-Si TFTs were fabricated by some groups and they showed excellent properties [2.16, 2.19, 2.32, 2.33]. Their performance is better than that by SPC [2.16].

However, it has been reported that the leakage current of poly-Si TFTs using MILC is higher than those of poly-Si TFTs prepared by laser annealing process [2.34]. The MILC method uses metals, such as Ni and Pd [2.35, 2.36]. The crystallization occurs through lateral phase transformation from the MIC region and this lateral crystallization is mediated by silicides which are formed in the MIC regions. In

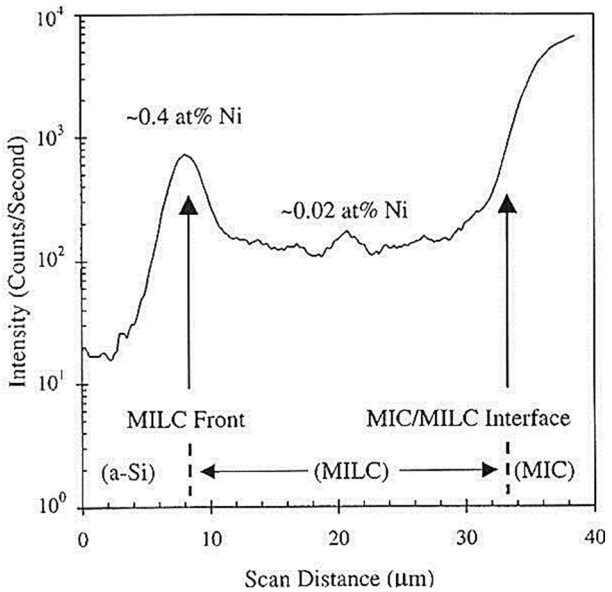


Figure 2.7 Distribution of Ni across the MIC, the MILC, and the a-Si regions obtained by secondary ion mass spectroscopy (SIMS).

general, needle-shaped crystal Si grains grow toward the a-Si region with the migration of the silicide [2.37] and the individual crystallites form crystallized networks during the MILC process. If the silicide layer at the front of crystal Si grain meets other crystal grains which have already been crystallized by the MILC process, the silicide layer cannot migrate through the crystal Si grains anymore because there is no difference in chemical potential-driving force for the phase transformation between the facing the two crystal Si grains [2.31]. Therefore, the captured silicides can increase the silicide contamination in the MILC region. Figure 2.6 and 2.7 show these phenomenons. The presence of the captured silicides and/or poly-Si grain boundary defects in the channel region of TFTs degrades the electrical performance, resulting to the high leakage current of MILC poly-Si TFTs.

2.3 Poly-Si TFT Device Theories

2.3.1 Seto's Model

Seto's paper concerning the electrical behavior of polycrystalline is a very important work in the field. [2.38] On the basis of initial experimental results reported by T. I. Kamins [2.39] and by M. E. Cowher & T. O. Sedgwick [2.40], J. Y. Seto was the first to give an original and credible interpretation of the specific conduction in polycrystalline materials. The main result concerned a high temperature process on boron doped poly-Si films and were well described in his paper.

The Seto's model is based on the following assumptions:

a. Poly-Si film has small grain size,
b. The single crystalline Si energy band structure is assumed to be applicable inside the crystallites,
c. Doping concentration in poly-Si is uniform,
d. All the doping atoms are ionized,
e. All the grains have the same size,
f. The representation is mono-dimensional,
g. The grain boundaries have no thickness
h. The defects are carrier traps that are located in grain boundaries. The trap concentration is defined per surface unit.
i. The traps are acceptors in the n-type and donors in the p-type semiconductor.
j. The trap energy level is unique and located more or less in the middle of the forbidden band.

The device characteristics of poly-Si TFTs are strongly influenced by the grain structure in poly-Si film. Even though the inversion channel region is also induced by the gate voltages as in MOSFETs, the existence of grain structure in channel layer bring huge differences in carrier transport phenomenon. Many researchers studying the electrical properties and the carrier transport in poly-Si TFTs have been reported. A simple grain boundary trapping model has been described by many authors in detail [2.41-2.49]. In this model, it is assumed that the poly-Si material is composed of a linear chain of identical crystallite having a grain size L_g and the grain boundary trap density N_t. The charge trapped at grain boundaries is compensated by opposite charged depletion regions surrounding the grain boundaries. From Poisson's equation, the charge in the depletion regions causes curvature in the energy bands, leading to potential barriers that impede the movement of any remaining free carriers from one grain to another. When the dopants/carrier density n is small, the poly-Si grains will be fully depleted. The width of the grain boundary depletion region x_d extends to be $L_g/2$ on each side of the boundary, and the barrier height V_B can be expressed as

$$V_B = \frac{qn}{2\varepsilon_s} x_d^2 = \frac{qnL_g^2}{8\varepsilon_s} \tag{2-1}$$

As the dopant/carrier concentration is increased, more carriers are trapped at the grain boundary. The curvature of the energy band and the height of potential barrier increase, which making carrier transport from one grain to another more difficult. When the dopant/carrier density increases to exceed a critical value $N^* = N_t / L_g$, the poly-Si grains turn to be partially depleted and excess free carriers start to spear inside the grain region. The depletion width and the barrier height can be expressed as

$$x_d = \frac{N_t}{2n} \tag{2-2}$$

$$V_B = \frac{qn}{2\varepsilon_s}\left(\frac{N_t}{2n}\right)^2 = \frac{qN_t^2}{8\varepsilon_s n} \tag{2-3}$$

The depletion width and the barrier height turn to decrease with increasing dopant/carrier density, leading to improved conductivity in carrier transport. The carrier transport in partially-depleted poly-Si film can be described by the thermion emission over the barrier. Its current density can be written as [2.50]

$$J = qnv_c \exp\left[-\frac{q}{KT}(V_B - V)\right] \tag{2.4}$$

Where n is the free-carrier density, v_c is the collection velocity ($v_c = \sqrt{KT/2\pi n^*}$), V_B is the barrier height without applied bias, and V_G is the applied bias across the grain boundary region. For small applied biases, the applied voltage divided approximately uniformly between the two sides of a grain boundary. Therefore, the barrier in the forward-bias direction decrease by an amount of $V_G/2$. In the reverse-bias direction, the barrier increases by the same amount. The current density in these two directions then can be expressed as

$$J = qnv_c \exp\left[-\frac{q}{KT}\left(V_B - \frac{1}{2}V_G\right)\right] \tag{2-5}$$

$$J = qnv_c \exp[-\frac{q}{KT}\left(V_B + \frac{1}{2}V_G\right)] \quad (2\text{-}6)$$

the net current density is then given by

$$J = 2qnv_c \exp\left(-\frac{qV_B}{KT}\right)\sinh\left(\frac{qV_G}{2KT}\right) \quad (2\text{-}7)$$

at low applied voltages, the voltage drop across a grain boundary is small compared to the thermal voltage *KT/q*, from the Taylor expression:

$$\sinh(x) = \sum_{n=0}^{\infty} \frac{1}{(2n+1)!} x^{2n+1}$$

Equation (2.7) then can be simplified as

$$J = 2qnv_c \exp\left(-\frac{qV_B}{KT}\right)\frac{qV_G}{2KT} = \frac{q^2 nv_c V_G}{KT}\left[\exp\left(-\frac{qV_B}{KT}\right)\right] \quad (2\text{-}8)$$

the average conductivity $\sigma = J/E = J \times (L_G/V_G)$ and the effective mobility $\mu_{eff} = \sigma/qn$, then can be obtained

$$\sigma = \frac{q^2 nv_c L_G}{KT}\exp(-\frac{qV_b}{KT}) \quad (2\text{-}9)$$

$$\mu_{eff} = \frac{qnv_c L_G}{KT} \exp(-\frac{qV_b}{KT}) \equiv \mu_0 \exp(-\frac{qV_b}{KT}) \qquad (2\text{-}10)$$

where μ_0 represents the carrier mobility inside grain regions. It is found that the conduction in poly-Si is an activated process with activation energy of approximately qV_B, which depends on the dopant/carrier concentration and the grain boundary trap density. In poly-Si TFTs, the carrier density n induced by the gate voltage can be expressed as

$$n = \frac{C_{ox}(V_G - V_{TH})}{qt_{ch}} \qquad (2\text{-}11)$$

where t_{ch} is the thickness of the inversion layer. Therefore, by replacing equation (2-10) and (2-11) into (2-8), the drain current $I_D = J \times W \times t_{ch}$ of poly-Si TFT then can be given by

$$I_D = \mu_0 C_{ox} \frac{W}{L} (V_G - V_{TH}) V_D (\frac{qV_G}{KT}) \qquad (2\text{-}12)$$

where drain voltage $V_D = V_G \times n_G = V_G \times L/L_G$. Obviously, this *I-V* characteristics is very similar to that in MOSFETs, except that the mobility is activated.

In comparison with single-crystalline silicon (c-Si), grain boundary defects and in-grain defects existing in poly-Si film are important factor to affect significantly the electrical characteristics of poly-Si TFTs. TFTs with more defects in the channel region require larger gate voltage to induce more carriers in order to fill the greater

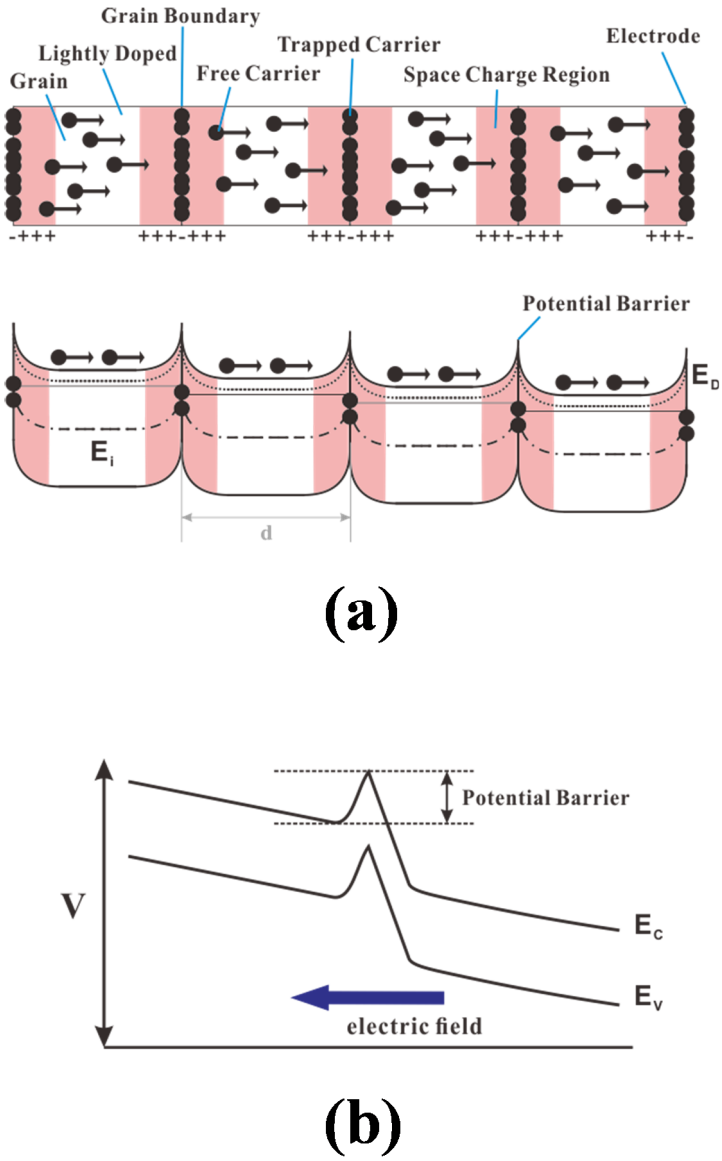


Figure 2.8 Cross-sectional view of a poly-Si TFT and the potential distribution around the grain boundary.

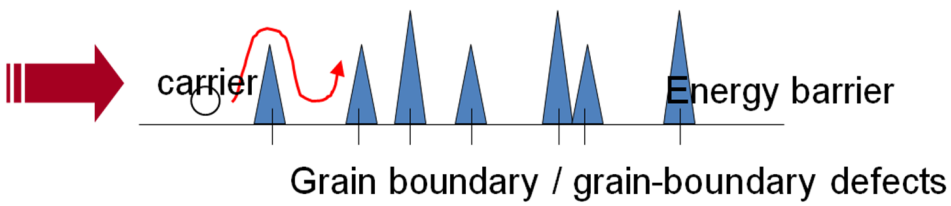


Figure 2.9 Simple sketch of carrier movement in the poly-Si. The oppositely charged grain boundary defect leads the potential barriers that impede the movement of carriers.

number of traps, and then the TFT can turn on. Figure 2.8 show a cross sectional view of the poly-Si TFT with the columnar grain structure and the potential distribution around grain boundary. The grain boundary potential barrier (Φ_B) increase when traps at the grain boundary are filled with majority carriers, and then the grain boundary potential barrier (Φ_B) decrease as the gate voltage kept increasing as shown in Figure 2.8(a). When the drain voltage is increased, the potential barrier (Φ_B) is also lowered, which is called drain induced grain barrier lowering (DIGBL) effect which is shown in Figure 2.8(b) [2.41].

Besides, the carriers trapped at the trap states were compensated by oppositely charged depletion regions, and cause curvature in the energy bands, leading to potential barriers that impede the movement of free carriers [2.49]. A very simple sketch gives an idea of the phenomenon, as shown in Figure 2.9. Thus, the typical characteristics such as threshold voltage (V_{TH}), on state current (I_{ON}), field-effect mobility (μ_{FE}), subthreshold slope (SS), and transconductance (g_m) of TFTs are inferior to those of devices fabricated on single crystal Si film – MOSFET.

An anomalous high leakage current, which is strongly bias and temperature dependent, is also an undesired problem in poly-Si TFTs, and results from electrons

field emission (for *p*-channel TFTs) via grain boundary traps in the surface depletion region at the drain. The holes also can be excited from the trap states to the valence band by three basic mechanisms as shown in Figure 2.10:

a. **Thermion emission**, which is due to thermal excitation of trapped holes into the valence band.
b. **Thermionic field emission**, which caused by field-enhanced thermal excitation of trapped holes into valence band.
c. **Pure tunneling**, which carried by field ionization of trapped holes tunneling through the potential barrier into valence band.

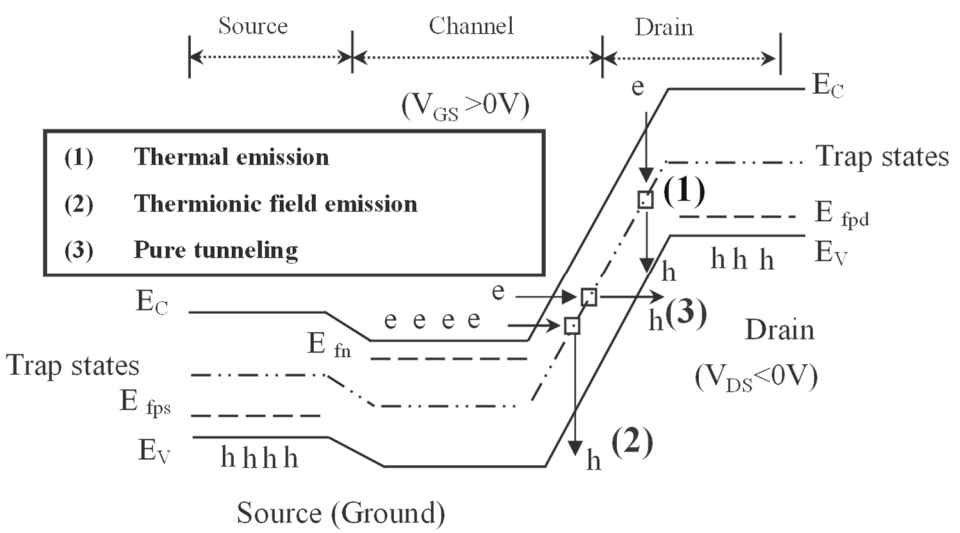


Figure 2.10 Anomalous leakage current mechanism (1) thermal emission, (2) thermionic emission, and (3) pure tunneling.

As mentioned above, the location and amount of defect traps have a significant influence on electrical characteristics of poly-Si TFTs. The most effective approach to improve the performance of poly-Si TFTs is to reduce the defect traps by improving the quality of poly-Si thin films. The other important work is to reduce the undesired bias-depended effects and temperature-depended effects of poly-Si TFTs, by modifying the architecture of poly-Si TFTs.

2.4 Electrical Properties Characterization

2.4.1 The I_D-V_G Transfer Characterization

The I_D-V_G transfer characteristics represent the dependence of the drain current (I_D) on the gate voltage (V_G) as a function of drain voltages (V_D) as shown in Figure 2.11. When a TFT is biased with positive or negative voltages, basically three cases exist at the semiconductor surface. As discussed in the following in the *p*-channel, when a positive gate voltage ($V_G > 0$) is applied to the gate metal, the carrier do not have energy to overcome the barrier, so no current flows in the channel. This is the off-state or accumulation case. When a small negative voltage ($V_G < 0$) is applied, the majority carriers are depleted in the channel, but the electron still does not have enough energy to overcome the barrier. This is the depletion case. When a larger negative voltage is applied, the number of holes at the surface is larger than that of the electrons, so holes have enough energy to overcome the barrier. This is the on-state or inversion case. Similar results can be obtained for *n*-channel TFT. The polarity of the voltage, however, should be changed for *n*-channel TFT.

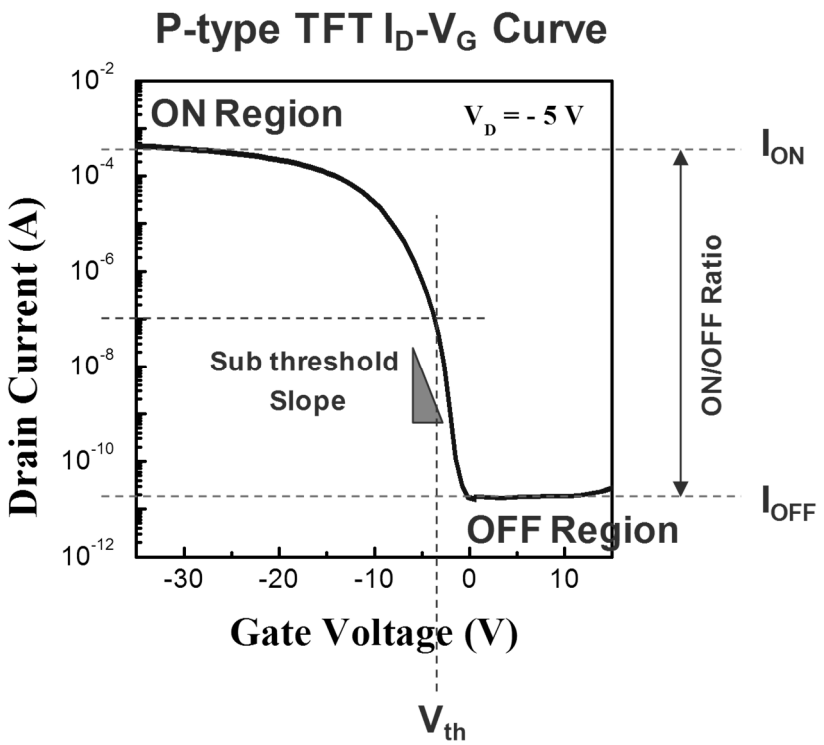


Figure 2.11 Typical I_D-V_G transfer characteristics curve. The key parameters such as on-state current, off-state current, subthreshold slope, threshold voltage, and on/off current ratio are represented in the figure. The field-effect mobility was determined from the transconductance at low drain voltage by mathematical calculation.

Moreover, the threshold voltage (V_{TH}) often has been extrapolated from I_D-V_G curves [2.51, 2.52]. However, this voltage, which occurs at the knee of the log(I_D)-V_G characteristics, is more properly labeled as the on voltage, V_{ON}. The V_{TH} is better defined at the much lower current level where the I_D dependence ceases to be exponential. Many key parameters such as field-effect mobility, subthreshold slope and so on, could be determined in the this curve and be discussed in the next paragraphs. Consequently, it will be helpful to understand this dissertation.

2.4.1.1 Determination of the Threshold Voltages (V_{TH})

Plenty ways are used to determinate the threshold voltage which is the most important parameter of semiconductor devices. The method to determinate the threshold voltage is some paper or dissertation is the constant drain current method that the voltage at a normalized drain current (N-I_D) is taken as the threshold voltage. This technique is adopted in most studies of TFTs. It can give a threshold voltage close to that obtained by the complex linear extrapolation method. Typically, the threshold current N-I_D=$I(L_{eff} / W_{eff})$ is specified at 10 nA for V_D = 0.1 V and 100 nA for V_D = 10 V in this dissertation to extract the threshold voltage of TFTs.

2.4.1.2 Determination of the Field-Effect Mobility (μ_{FE})

The field-effect mobility (μ_{FE}) is determined from the transconductance (g_m) at low drain voltage (V_D = 0.1 V). The transfer characteristics of poly-Si TFTs are similar to those of conventional MOSFETs, so the first order I-V relation in the bulk Si MOSFETs can be applied to the poly-Si TFTs, which can be express as

$$I_D = \mu_{FE} C_{ox} \frac{W}{L} [(V_G - V_{TH})V_D - \frac{1}{2} V_D^2] \qquad (2\text{-}13)$$

where C_{ox} is the gate insulator capacitance per unit area, W and L are the width and the length of the channel, V_{TH} is the threshold voltage.

If V_D is much smaller than V_G-V_{TH} (i.e. $V_D << V_G$-V_{TH}) and $V_G > V_{TH}$, the drain current can be approximated as:

$$I_D = \mu_{FE} C_{ox} \frac{W}{L} [(V_G - V_{TH}) V_D] \tag{2-14}$$

The transconductance is defined as

$$g_m = \left. \frac{\partial I_D}{\partial V_G} \right|_{V_D = const} \tag{2-15}$$

Therefore, the field-effect mobility can be obtained by

$$\mu_{FE} = \frac{L}{C_{ox} W V_D} g_m \tag{2-16}$$

2.4.1.3 Determination of the ON/OFF Current Ratio ($I_{ON/OFF}$)

The ON/OFF current ratio is another important parameter of TFTs. High ON/OFF current ratio represents not only large turn-on current but also small off-state current (leakage current). It affects mechanism in poly-Si TFTs is much different from conventional MOSFETs since the channel layer of poly-Si TFTs is composed of polycrystalline. A large amount of trap densities in grain structure serve as lots of defect states in energy band gap to enhance tunneling effect. Therefore, the leakage

current due to trap-assisted tunneling effect is much larger in poly-Si TFTs than in the single crystal MOSFETs. There are many methods to specify the on and off state currents. The easiest one is to define the maximum current as on-state current and the minimum leakage current as off state current while drain voltage of 5 V. This simple method to define ON/OFF current ratio is used in this dissertation.

2.4.1.4 Determination of the Subthreshold Slope (*SS*)

Subthreshold slope SS (V/dec) is a typical parameter to describe the control ability of gate toward channel. It is defined as the amount of gate voltage required to increase/decrease drain current by one order of magnitude. The subthreshold slope should be independent of drain voltage and gate voltage. However, in reality, the subthreshold slope might increase with drain voltage due to short-channel effects such as charge sharing, avalanche multiplication, and punch through-like effect. The subthreshold slope is also related to gate voltage due to undesirable factors such as series resistance and interface state. In this dissertation, the subthreshold slope is defined as the gate voltage required increasing the drain current by a factor of 10. The threshold current is specified to be the drain current when the gate voltage is equal to the threshold voltage. In the LCD, the subthreshold slope is most important parameter due to it reflects the response ability of liquid crystal.

2.4.1.5 Determination of the Trap State Density (N_t)

The grain boundary potential barrier height is related to the carrier concentrations inside the grain and the trapping states located at grain boundaries. Based on this consideration, the amount of trap state density (N_t) can be extracted from the current-voltage characteristics of poly-Si TFTs. As proposed by Levinson *et al.* [2.42], the *I-V* characteristics including the trap density can be obtained by

$$I_D = \mu_0 C_{ox} \frac{W}{L} (V_G - V_{TH}) V_D \exp\left(-\frac{q^3 N_t^2 t_{ch}}{8kT\varepsilon_s C_{ox}(V_G - V_{TH})}\right) \quad (2\text{-}17)$$

This equation had been further corrected by Proano *et al.* by considering the mobility under low gate bias [2.53]. It is found that the behavior of carrier mobility under low gate bias can be expressed more correctly by using the flat-band voltage V_{FB} instead of the threshold voltage V_{TH}. Moreover, a better approximation for channel thickness t_{ch} in an undoped material is given by defining the channel thickness as the thickness at which 80% of the total charge resides. Therefore, by solving the Poisson's equation, the channel thickness is given by

$$t_{ch} = \frac{8kT\sqrt{\varepsilon_s \varepsilon_{ox}}}{qC_{ox}(V_G - V_{FB})} \quad (2\text{-}18)$$

The drain current of poly-Si TFTs then should be expressed as

$$I_D = \mu_0 C_{ox} \frac{W}{L}(V_G - V_{FB})V_D exp\left(-\frac{q^2 N_t^2 \sqrt{\frac{\varepsilon_{ox}}{\varepsilon_S}}}{C_{ox}^2 (V_G - V_{FB})^2}\right) \quad (2\text{-}19)$$

where *W*, *L*, and *t* are the channel width, length, and semiconductor thickness, respectively. the grain boundary trap state density then can be obtained from the slope of the curve ln[I_D/(V_G-V_{FB})] versus (V_G-V_{FB})$^{-2}$, where the flat-band voltage (V_{FB}) is defined as the gate voltage that yields the minimum drain current from the transfer characteristic with linear region. Finally, the grain boundary trap state density can be determined from the square root of the slope:

$$\mathrm{N_{trap}} = \frac{\mathrm{C_{ox}}}{\mathrm{q}}\sqrt{|\mathrm{slope}|} \quad (2\text{-}20)$$

2.4.2 The I_D-V_D Transfer Characterization

The other important *I-V* characteristics is I_D-V_D output curve. They present the dependence of the drain current (I_D) on the drain voltage(V_D) at different gate voltages (V_G). The drain current increases linearly at low drain voltages (linear regime) and saturates at high drain voltages (saturation regime). The saturation values of drain current depend on the applied gate voltage. When low gate voltage applied, the thickness of the induced channel is small and the current saturates at low values of drain current. On the other hand, thicker channel in induced at high gate voltages and

the saturation current is higher. Well separated output characteristics are an indication of good ohmic drain and source contacts. The transistor enters in saturation regime when $V_D > V_{SAT}$, where $V_{SAT} = V_G - V_{TH}$. The successive line of corresponding to $V_D > V_{SAT}$ are described by the following equation:

$$I_D = \frac{W}{L}\mu_{eff}C_{ox}(V_G - V_{TH})^2 \quad (2\text{-}21)$$

where W and L are the width and the length of the TFT channel, μ_{eff} is the field-effect mobility and C_{ox} is the gate insulator capacitance. The threshold voltage and the field effect mobility can be determined from measurements of the saturation current, plotting the square root of the measured I_D vs. V_G in saturation (at $V_D \geq V_G - V_{TH}$).

2.4.2.1 Kink Effect

Most of the applied voltage drops across the grain boundaries since they have much larger resistances than the grain. The lateral electric field in the grain boundaries will, therefore, be much higher than in the grains, and at large drain voltage, impact ionization may occur. In contrast, the field in the neutral regions of the grains will not be high enough to cause impact ionization. Electrons are collected at the drain electrode, while holes are injected into the film, flowing toward the source and finally lowering the source junction potential. As consequence, the turn-on voltage decreases and the channel current is increased at drain voltage well above the knee voltage. This so-called kink effect is larger in poly-Si TFTs than in crystalline devices because of the large potential drops at the grain boundaries [2.54].

CHAPTER 3

Experimental Procedures

3.1 Device Fabrication

3.1.1 Fabrication of Conventional MILC Poly-Si TFTs

FABRICATION process for conventional MILC poly-Si TFTs is shown in Figure 3.1. A 3000 Å-thick SiO_2 buffer layer was deposited on the glass substrate (Corning 1737) by plasma enhanced chemical vapor deposition (PECVD). A 1000 Å-thick a-Si film was then deposited by low pressure chemical vapor deposition (LPCVD) using SiH_4. The deposition pressure and temperature for the a-Si were 200 mTorr and 500 °C, respectively. Then, the active layer was patterned by photolithography and etched by reactive ion etching (RIE) system, using SF_6. After defining the active layer, photo resistor (PR) was pattern to prevent the metal contamination at a-Si region which will be MILC. Native oxide was eliminated with buffered-HF solution. Then, 50 Å-thick Ni film was deposited by sputtering system and PR was removed with PRS 2000 remover at 70 °C. Thin Ni layer was also eliminated simultaneously during PR strip. It was called as lift-off method. The

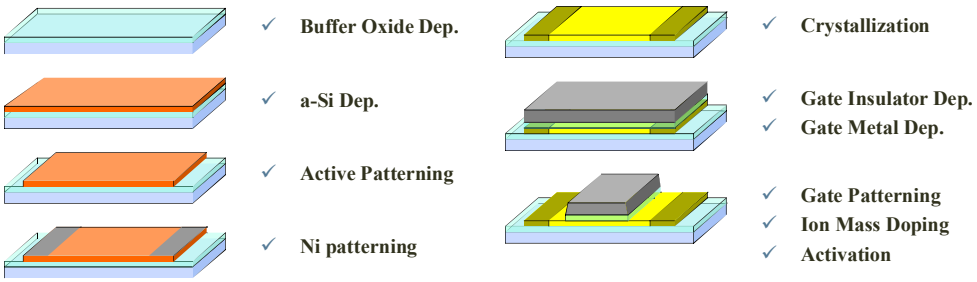


Figure 3.1 Schematic diagrams of fabrication process for conventional MILC poly-Si TFT.

Table 3.1 Detailed conditions of fabrication processes for MILC poly-Si TFT

Step	Equip.	Conditions	Materials
Buffer Layer	PECVD	350 °C 20 W	SiNx 1500 Å
Active Layer	LPCVD	500 °C	a-Si 1000 Å
Catalyst Layer	Sputter	R.T.	Ni 50 Å
Ni removal	Wet Station	80 °C	H_2SO_4
Crystallization	Furnace	550 °C 2 h	H_2
Gate Insulator	PECVD	350 °C	SiNx 1000 Å
Gate Metal	Sputter	300 °C	MoW 2000 Å
Doping	IMD	150 W 17 kV	B_2H_6, PH_3
Activation	Furnace	550 °C 2 hr	H_2

samples were annealed in hydrogen ambient at a temperature of 550°C for 2 h for the crystallization of the a-Si. Then, a 1000 Å-thick of SiN_x gate insulator was prepared by PECVD using SiH_4 and NH_3 at 350 °C. Subsequently, the MoW layer was formed by sputtering for gate metal and etched by H_3PO_4+CH_3COOH+HNO_3+H_2O etchant. The gate oxide was etched by RIE, using SF_6, CHF_3 and Ar. After PR removing, the source/drain region was doped with B_2H_6 (*p*-channel) or PH_3 (*n*-channel) by ion mass

doping (IMD) system. The process condition of IMD is summarized at Table 3.1. The samples were annealed at 550 °C for 2 h in H_2 ambient for dopant activation. Thickness of thin films was measured by alpha-step and resistivity of thin films could be got from 4-point probe. The MILC phenomenon was observed by optical microscopy with Normaski Filter. The MILC poly-Si has different optical properties from that of a-Si, and then, it can be observed with optical microscopy.

3.1.2 Minimization of Ni Contamination

3.1.2.1 Silicide Induced Crystallization

a. Characterization of SIC Poly-Si Thin Film

Poly-Si thin films were made by SIC and their material properties were characterized using various analysis method. a-Si films (1000-Å-thick) were deposited on buffered-layered (3000 Å thickness SiO_2) glass (Corning eagle XG, substrate size: 106 mm × 106 mm) substrates by LPCVD using SiH_4 at a temperature of 500 °C. After dipping in 1% diluted HF for 1 min to remove native SiO_2, 50-Å-thick Ni films were deposited by direct-current (DC) magnetron sputtering at room temperature (RT), 100 °C, 200 °C, and 300 °C. The conditions of Ni sputtering were 15 mTorr working pressure, 800 V DC voltage, and 0.6 A DC current. Then the samples were dipped into 70 °C H_2SO_4 for 30 min to remove unreacted Ni. For crystallization, the samples were annealed at 500 °C for 1 h. Figure 3.2(a) shows the process sequence for fabricating the SIC poly-Si thin films. For the purpose of comparison, conventional MIC poly-Si thin films were also prepared.

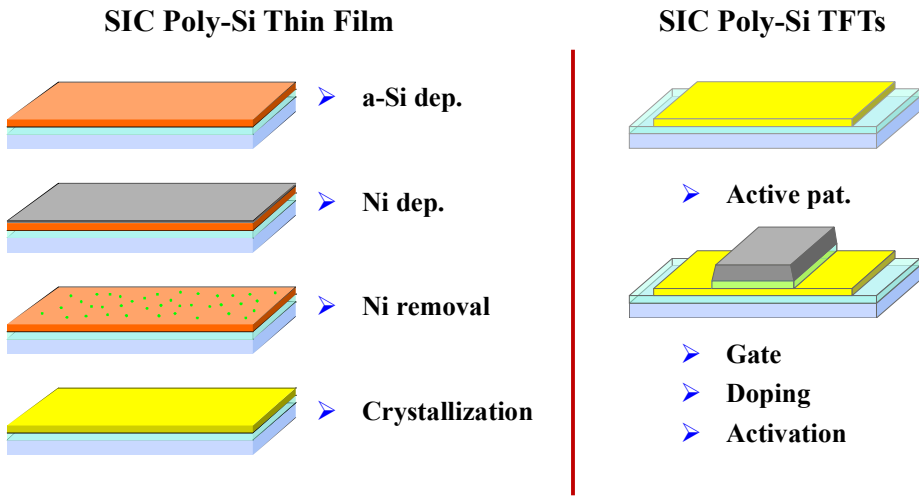


Figure 3.2 Schematic diagram of fabrication processes for SIC poly-Si thin film and its application for TFT.

The preparation process of MIC poly-Si thin films was almost the same as that of SIC poly-Si thin films; the major difference was that the surfaces of MIC poly-Si thin films needed to undergo an additional step to remove unreacted Ni using H_2SO_4 after crystallization annealing. X-ray photoelectron spectroscopy (XPS), scanning electron microscopy (SEM), Auger electron spectroscopy (AES), atomic force microscopy (AFM) and micro-Raman scattering spectroscopy were used to characterize SIC poly-Si thin films.

b. Electrical Performance Characterization of SIC Poly-Si TFTs

To investigate the electrical properties, *p*-channel SIC poly-Si TFTs with self-aligned coplanar structures were fabricated on glass as shown in Figure 1b. Previously made SIC poly-Si thin films were used as the active layer. After active layer patterning by lithography and subsequent RIE processes, a 1000-Å-thick SiO_2 film as

a gate dielectric layer was deposited by PECVD using SiH_4 and N_2O gas at 300 °C, and a 2000-Å-thick MoW film as a gate-metal layer was formed by sputtering. The gate metal was defined by conventional lithography and etched by H_3PO_4 + CH_3COOH + HNO_3 + H_2O etchants. The gate dielectric was etched by RIE using SF_6, Ar and CHF_3 gases. To define the source/drain junction, the samples were doped by IMD using B_2H_6 as the source gas. The accelerating voltage and the radio frequency (RF) power were 17 keV and 150 W, respectively. After the source/drain doping, interlayer dielectrics were deposited. Then, the dopants were activated by furnace annealing at a temperature of 550 °C for 2 h in hydrogen under ambient conditions. After opening contact holes, metallization was carried out. The 6000 Å-thick MoW was used for metallization. For comparison, *p*-channel MIC and MILC poly-Si TFTs with top gate self-aligned coplanar structures were also fabricated on glass. The I_D-V_G transfer curves were measured with a Keithley 2636 System SourceMeter. The entire fabrication process was carried out in a 1000-class clean room.

3.1.2.2 Silicide Induced Lateral Crystallization

a. Fabrication of Off-Set SILC Poly-Si TFT

In this study, *p*-channel MILC and SILC poly-Si TFTs with self-aligned coplanar structures were fabricated on glass, as shown in Figure 3.3(a). In brief, a 3000 Å-thick SiO_2 buffer layer and 1000 Å-thick a-Si layer were consequently deposited on glass substrates (Corning eagle XG, substrate size: 106 mm × 106 mm) by PECVD and LPCVD using SiH_4 at a temperature of 500 °C, respectively. Dehydrogenation was carried out for 2 h at 450 °C in a vacuum. In order to define the active patterns,

conventional photolithography and RIE using SF_6 gas were utilized. Ni was deposited on the source and drain areas after photolithography with an island pattern mask. Ni was sputtered at DC 700 V for 15 sec. The initial pressure was 2×10^{-6} Torr . The working pressure was 30 mTorr with an Ar flow of 30 sccm and a throttle valve was used to keep the pressure constant. The current was measured to be 0.5 mA and the thickness was estimated to be about 5 nm by extrapolating the straight line in a plot of thickness vs. sputtering time. The lift-off method was used for the Ni island pattern. For the SILC process, the Ni was removed right before the sample was put into a furnace for crystallization annealing while for the MILC process, Ni was removed after crystallization annealing, as shown in Figure 3.3 (Top).

We call the process SILC because only seeds are left on the source and drain regions before annealing. After crystallization annealing in hydrogen ambient at a temperature of 550 °C for 2 h, 1000 Å thick gate oxide was deposited by PECVD using SiH_4 and N_2O gas at 350 °C, and a 2000 Å thick MoW gate metal was subsequently formed by sputtering. The gate metal was etched by H_3PO_4 + CH_3COOH + HNO_3 + H_2O etchant and the gate oxide was etched by RIE using SF_6, Ar, and CHF_3 gases. To define the source/drain junction, the samples were doped by an IMD system using B_2H_6 source gas diluted with 80% hydrogen. The accelerating voltage and RF power were 17 kV and 150 W, respectively. After the source/drain doping, 600 nm-thick interlayer dielectrics were deposited. Then, the dopants were activated by furnace annealing in hydrogen ambient at a temperature of 550 °C for 2 h. After opening contact holes by RIE, metallization and alloying at 400 °C for 30 min were performed. The 6000 Å-thick MoW was used for metallization. The I_D-V_G transfer curves were measured with a Keithley 2636 System SourceMeter.

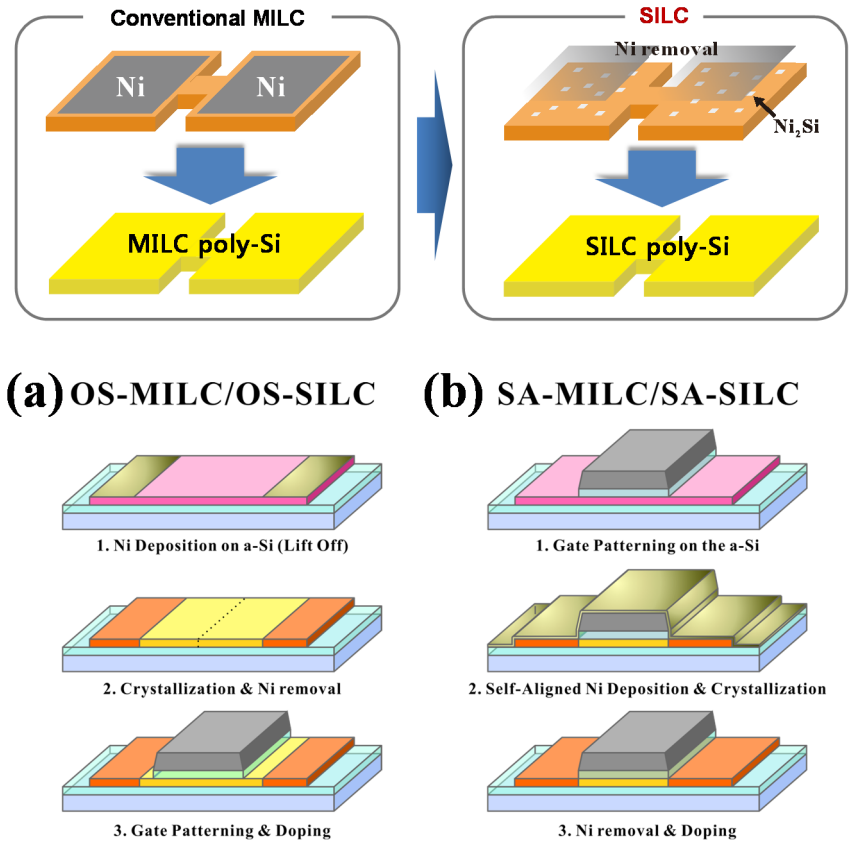


Figure 3.3 Schematic diagram of fabrication processes for SILC poly-Si thin film compared with conventional MILC poly-Si thin film (Top). Schematic diagrams for explain of Off-set SILC (OS-SILC) Poly-Si TFT and (b) Self-aligned SILC (SA-SILC) Poly-Si TFT. In order to comparison, The Off-set and Self-aligned MILC poly-Si TFTs fabrication processed are included in the figure.

b. Fabrication of Self-Aligned SILC Poly-Si TFT

The *p*-channel poly-Si TFTs with self-aligned coplanar structures were fabricated on glass. Figure 3.1(b) shows the fabrication of procedures of self-aligned MILC and self-aligned SILC (herein after SA-MILC and SA-SILC) poly-Si TFTs. In brief, a 3000 Å-thick SiO_2 buffer layer and 1000 Å -thick a-Si layer were deposited on glass substrates (Corning eagle XG, substrate size: 106 mm × 106 mm) by PECVD and

LPCVD, respectively. In order to define the active patterns, photolithography and RIE using SF_6 gas were utilized. 1000-Å-thick gate oxide was deposited by PECVD using SiH_4 and N_2O gas at 350 °C, and a 2000-Å-thick MoW gate metal was subsequently formed by PECVD and sputtering. The gate metal was etched by $H_3PO_4 + CH_3COOH + HNO_3 + H_2O$ etchant, and the gate oxide was etched by RIE using SF_6, Ar, and CHF_3 gases. 50-Å-thick Ni was deposited after HF treatment to remove native oxide. Ni was sputtered at DC 700 V for 15 sec. The initial pressure was 2×10^{-6} Torr. The working pressure was 30 mTorr with an Ar flow of 30 sccm, and a throttle valve was used to keep the pressure constant. The current was measured to be 0.5 mA, and the thickness was estimated to be about 5 nm by extrapolating the straight line in a plot of thickness vs. sputtering time. For SA-SILC, the Ni was removed right before the sample was put into a furnace for crystallization annealing, while for the MILC process, Ni was removed after crystallization annealing. After crystallization annealing in hydrogen ambient at a temperature of 550°C for 2 h, The source and drain junction was defined by an IMD system using B_2H_6 source gas diluted with 80% hydrogen. The accelerating voltage and RF power were 17 kV and 150 W, respectively. After the source/drain doping, the dopants were activated by furnace annealing in hydrogen ambient at a temperature of 550 °C for 2 h. After the dopant activation, 600 nm-thick interlayer dielectrics were deposited. Then, the dopants were activated by furnace annealing in hydrogen ambient at a temperature of 550 °C for 2 h. After opening contact holes by RIE, metallization and alloying at 400 °C for 30 min were performed. The 6000 Å-thick MoW was used for metallization. In order to comparison, the conventional off-set MILC and off-set SILC (here-in-after OS-MILC and OS-SILC) were also fabricated and compared.

3.1.3 Gettering

3.1.3.1 Gettering on the MIC and SIC Poly-Si TFTs

In this study, we categorize the two sets of experiments - conventional poly-Si TFTs and gettered poly-Si TFTs as summarized in Table 3.2. In each case, the poly-Si was crystallized by the following two ways. - (1) MIC, (2) SIC, In case of MIC methods, Ni was sputtered on a-Si thin film and a heat treatment was carried out for crystallization and Ni was removed after the crystallization. In the SIC methods, Ni was removed prior to a heat treatment for crystallization.

Table 3.2 Designations of different crystallization methods

	Conventional Poly-Si	Gettered Poly-Si
MIC group	MIC	GMIC
SIC group	SIC	GSIC

Previously explained crystallization method and gettering process were applied to *p*-channel coplanar structures TFTs. The common glass substrate (Eagle XG; SAMSUNG Corning Inc.; size, 105 × 105 mm^2) was cleaned using piranha solution (H_2SO_4 : H_2O_2 = 3 : 2) for 30 min at 70 °C. The glass was thoroughly rinsed with deionized (DI) water and dried with a spin dryer. A 3000-Å-thick SiO_2 buffer layer was first deposited on a glass substrate by PECVD. Then, a 1000-Å-thick a-Si thin film was deposited by LPCVD at 500 °C using SiH_4 as the precursor and an active pattern was defined by the conventional photolithography and RIE. A 50-Å-thick Ni film was deposited by a DC magnetron sputtering (room temperature, 15 mTorr working pressure, DC 800 V, and 0.6 A) after dipping in 1% HF for 1 min to remove

native SiO_2. In case of SIC group, Ni was removed by dipping into H_2SO_4 at 70 °C for 10 min prior to crystallization annealing. Crystallization was carried out in a tube furnace at 550 °C for 2 h in H_2 ambient. After crystallization annealing, un-reacted Ni of MIC group was removed by dipping into H_2SO_4 at 70 °C for 30 min and 1% HF cleaning was done in order to remove the oxide. In case of GMIC and GSIC, a 1000-Å-thick a-Si layer was deposited by PECVD at 300 °C as the gettering layer, followed by gettering annealing in a tube furnace at 550 °C for 2 h. The gettering Si layer was removed using KOH. The active layer was defined by conventional photolithography and RIE, followed by deposition of a 1000-Å-thick SiO_2 gate-dielectric layer by PECVD using SiH_4 and N_2O gas at 300 °C, and sputtering of a 2000-Å-thick MoW gate-metal layer. The gate metal was defined by conventional lithography and etched by $H_3PO_4 + CH_3COOH + HNO_3 + H_2O$. The gate dielectric was etched by RIE using SF_6, Ar, and CHF_3 gases. To define the source/drain junction, the samples were doped by IMD B_2H_6 as the source gas (accelerating voltage, 17 kV; RF power, 150 W). After the source/drain doping, the dopants were activated by furnace annealing at 550 °C for 1 h under hydrogen ambient.

3.1.3.2 Gettering Process using Etch Stopper

In this experiments, top gate *p*-channel G-SIC poly-Si TFTs were fabricated on glass, as shown in Figure. 3.4. First, a conventional SIC poly-Si film was fabricated. All of conditions from buffer layer deposition to crystallization are same with the described in above paragraph. After crystallization, the active layer was defined by photolithography and etching. The obtained active layer was dipped into H_2SO_4 at

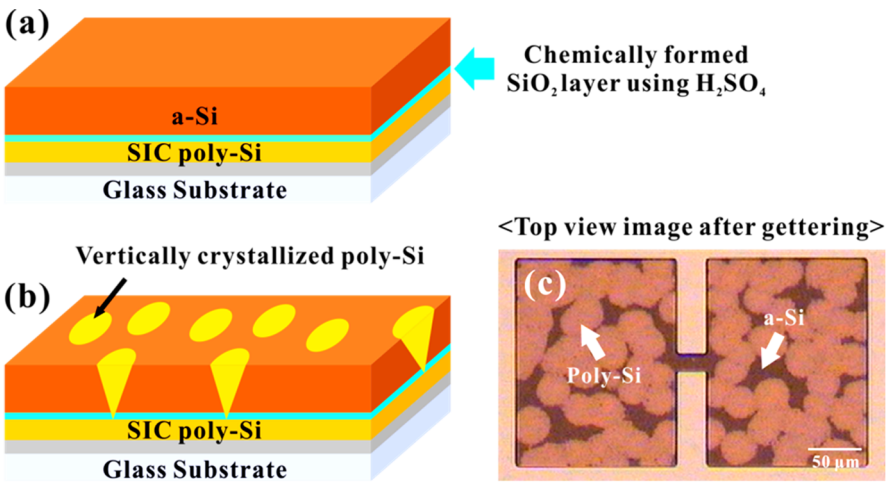


Figure 3.4 Schematic diagrams and optical microscopy image of key processes for gettered SIC poly-Si TFT, including (a) chemical SiO_2 and gettering layer formation after active layer crystallization, (b) after annealing for gettering, and (c) microscopy top view image of gettering layer after gettering annealing at 550 °C for 2 h.

100 °C for 1 h to form a chemical SiO_2 layer that acts as an etch stopper. Y. Uchida *et al*. investigated that the chemical oxide layer is formed about 50 Å at the condition [3.1]. Then, a 3000-Å-thick gettering a-Si layer was deposited by LPCVD at 500 °C as shown in Figure. 3.4(a), followed by gettering annealing at 550 °C for 6 h. As shown in Figure 3.4(b) and (c), the gettering layer was partially crystallized by the Ni silicide that diffused through the chemically deposited SiO_2. The partially crystallized gettering Si layer was removed by dipping into KOH solution. The chemically formed oxide layer was not etched by KOH during gettering Si layer removal (Selectivity in KOH; poly-Si : SiO_2 = 88 : 1). Therefore, chemically formed oxide layer was removed by 1% HF solution. We confirmed that Ni diffusion into the gettering layer led to a drastic reduction in the Ni concentration from 5.04×10^{12} to 6.77×10^{10} atoms/cm^2, as measured by total reflection X-ray fluorescence.

In order to fabricate top gate TFT, gate formation and doping processes were carried out. A 1000-Å-thick SiO_2 was deposited by PECVD using SiH_4 and N_2O gas at 350 °C, and a 2000-Å-thick MoW gate metal was subsequently formed by sputtering. The gate metal was etched by $H_3PO_4 + CH_3COOH + HNO_3 + H_2O$ etchant and the gate oxide was etched by RIE using SF_6, Ar, and CHF_3 gases. To define the source/drain junction, the samples were doped by an IMD system using B_2H_6 source gas diluted with 80% hydrogen. The accelerating voltage and RF power were 17 kV and 150 W, respectively. After the source/drain doping, 6000 Å-thick interlayer dielectrics were deposited. Then, the dopants were activated by furnace annealing in hydrogen ambient at a temperature of 550 °C for 2 h. After opening contact holes by RIE, metallization and alloying at 400 °C for 30 min were performed. The 6000 Å-thick MoW was used for metallization.

3.1.4 SILC/SILC Boundary Ejection

In this experiment, two kinds of top-gate *p*-channel poly-Si TFTs were fabricated by a modified SILC method to study the relationship between the SILC/SILC boundary (SSB) and the electrical properties. Figure 3.4(a) shows the conventional SILC poly-Si TFT (symmetrical SSB) with an SSB at center of the channel, and Figure 3.4(b) and (c) show the SILC poly-Si TFTs with an SSB ejected from the channel in the directions of the drain (drain-SSB) and source (source-SSB), respectively. All TFTs were fabricated on the same substrate. The electrical properties of the drain-SSB and source-SSB were measured on the same TFT with different source/drain directions, so the distances from the channel edge to the SSB of the

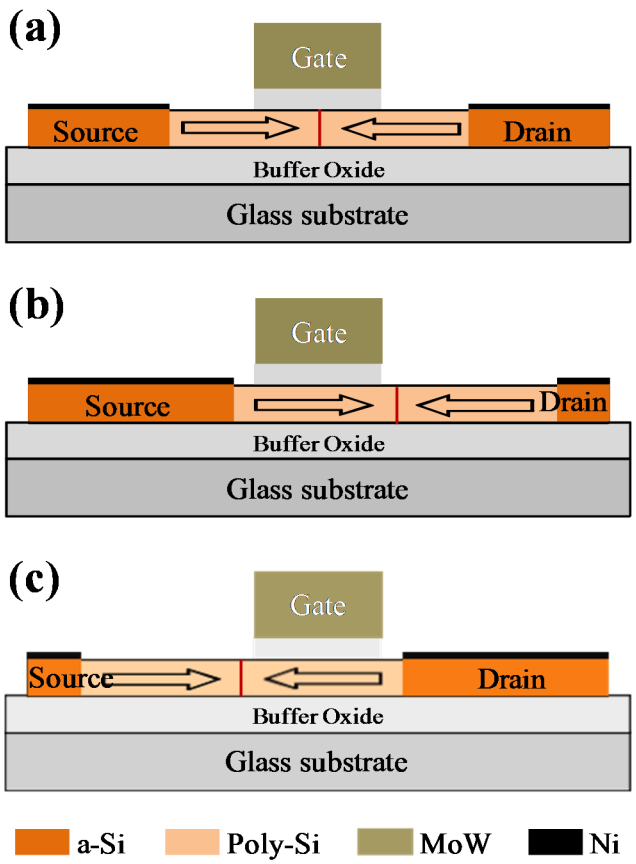


Figure. 3.5 Schematic diagrams of fabrication processes for (a) conventional SILC, (b) drain-SSB, and (c) source-SSB poly-Si TFTs

source-SSB and drain-SSB are the same. In order to fabricate poly-Si TFTs, a-Si films (1000-Å-thick) were deposited on buffered-layered glass substrates (Eagle XG, 300-nm-thick SiO_2, 105 × 105 mm^2; SAMSUNG Corning Inc.) by low-pressure chemical vapor deposition (LPCVD) using SiH_4 gas at a temperature of 500 °C. After dipping into 1% dilute HF for 1 min to remove native oxide, 50-Å-thick Ni films were asymmetrically deposited by direct-current magnetron sputtering at room temperature,

as shown in Figure 3.4(b) and (c). The conditions of Ni sputtering were a working pressure of 15 mTorr, 800-V DC voltage, and a 0.6-A DC current. Then, the samples were dipped into 70 °C H_2SO_4 for 30 min to remove un-reacted Ni. For crystallization, the samples were annealed at 550 °C for 2 h. After active layer patterning by lithography and subsequent reactive ion etching (RIE), a 1000-Å-thick SiN_x film was deposited as a gate-insulator layer by PECVD using SiH_4 and NH_3 gases at 350 °C, and a 2000-Å-thick MoW film was formed as a gate-metal layer by sputtering. The gate metal was defined by conventional lithography and etched by H_3PO_4 + CH_3COOH + HNO_3 + H_2O etchants. The gate dielectric was etched by RIE using SF_6, Ar, and CHF_3 gases. To define the source/drain junction, the samples were doped by ion mass doping (IMD) using B_2H_6 as the source gas. The accelerating voltage and the radio frequency power were 17 kV and 150 W, respectively. After the source/drain doping, interlayer dielectrics were deposited. Then, the dopants were activated by furnace annealing at a temperature of 550 °C for 2 h in hydrogen atmosphere.

3.1.5 Lightly Doped Drain Structure

3000 Å buffer oxide was deposited by PECVD on Corning Eagle Glass and then, 1000 Å of a-Si was deposited by LPCVD. Active area was patterned and MILC was carried out at the temperature of 550 °C for 2 h at hydrogen ambient. SiN_x or SiO_2 was used as a gate insulator. After deposition of a gate insulator, a MoW as gate metal, was deposited and wet etched with a gate mask. The gate length was fixed to 10 µm. After etching of the gate metal, PR was striped and an LDD mask was used to etch the gate insulator. Various gate lengths were patterned in an LDD mask. Since the LDD

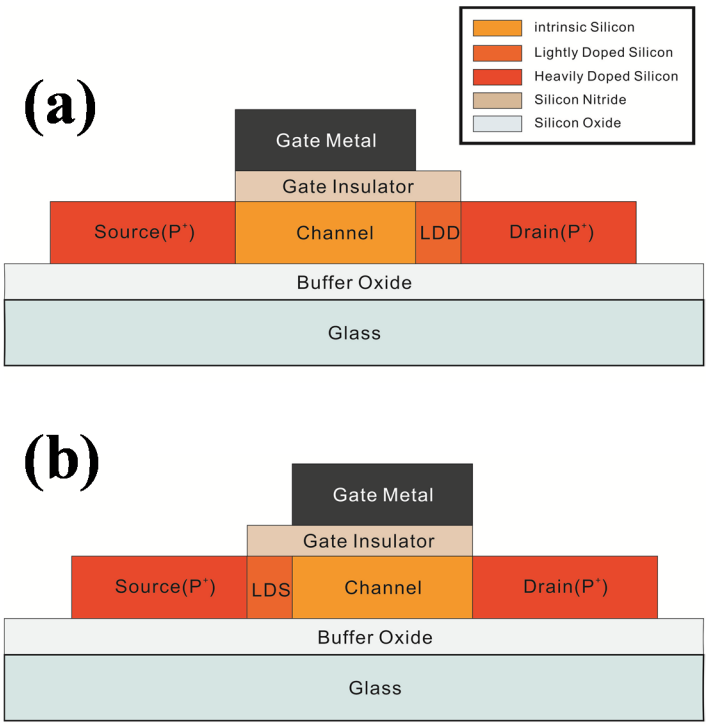


Figure 3.6 Schematic drawings for two structures with lightly doped region in the channel. (a) The lightly doped drain and (b) lightly doped source structures.

length has to be defined relatively to the gate length, + sign in a designation stands for deduction of the length from both ends of the source and drain. Therefore, +3 means the gate length in the LDD mask would be 4 μm, +2, 6 μm, +1, 8μm, and 0, 10 μm. And -1 is for the gate length in the LDD mask to be 12μm and -2, 14 μm, respectively. After the lithography, the gate insulator was dry etched and The PR was striped. IMD for formation of the source and drain was carried out, followed by electrical activation at 550 °C for 2 h in a hydrogen ambient. The final structure after formation of LDD is shown in Figure 3.5. It should be noticed that even in case of "0", where the LDD mask length is same to the gate metal length, we should have LDD or lightly doped

source (LDS) structure in reality due to inevitable misalignment in a lithography. If the difference in length between the gate length in the LDD mask and the gate length in the gate mask is larger than the margin in misalignment in a lithography, than we are supposed to have a TFT structure either with lightly doped regions or without at both of the source and drain. Since the electrical properties of LDD and LDS are very much different, we can determine the misalignment by measuring twice along opposite directions. We have not done any further process after electrical activation of the source and drain.

3.2 Analytical Methods for Thin Film Characterization

3.2.1 Auger Electron Spectroscopy (AES)

Auger electron spectroscopy (AES) is an analysis method which uses a primary electron beam to probe the surface of materials as seen in Figure 3.7. Secondary electrons which are emitted via the Auger process are analyzed. Also their energy is determined. The identity and quantity of the elements in the sample are determined by kinetic energy and intensity of Auger electrons. Auger electrons can escape from depth of only 5~50 Å of solid surface at their characteristics energy. This is possible to make AES an extremely surface sensitive analysis method. A finely focused electron beam can be scanned to make secondary electron and Auger images. Also, it can be positioned to analyze at specific sample features. The Auger process (effect) is name for Pierre Auger who found the radiation-less relaxation of excited ions in a cloud chamber in 1920s. Auger electrons are emitted at discrete energy level, allowing the

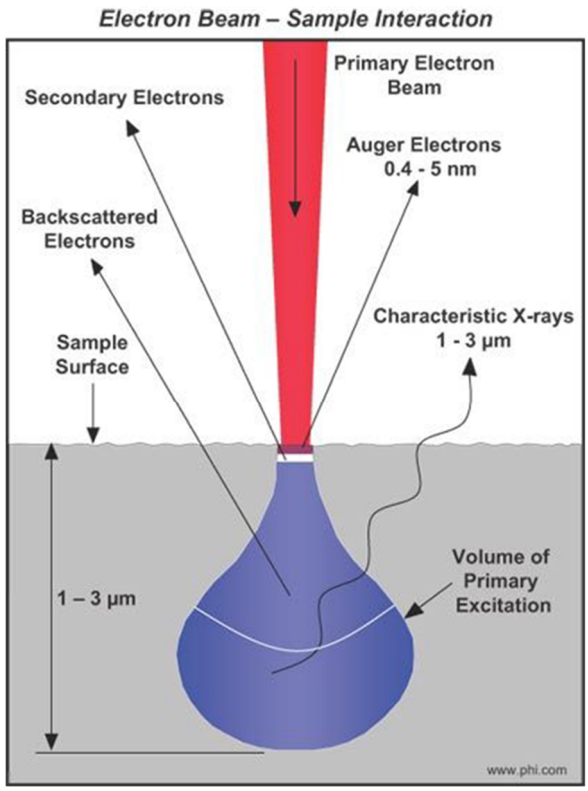


Figure 3.7 Signals produced by electron bombardment on the sample.

atom of origin to be identified [3.2]. The Auger process consists of three steps as shown in Figure 3.8:

(1) Excitation of the atom causing the electron emission

(2) An electrons drops down to fill the vacancy created in step 2

(3) The energy released in step 2 causes the Auger electron emission

Figure 3.9 shows Auger electron spectroscopy (phi 680 scanning Auger nanoprobe) made by Phi Co. with 10 keV of primary beam source. The Auger electron detector was cylindrical mirror analyzer (CMA). The chemical concentration in AES analysis was calculated by using following equation:

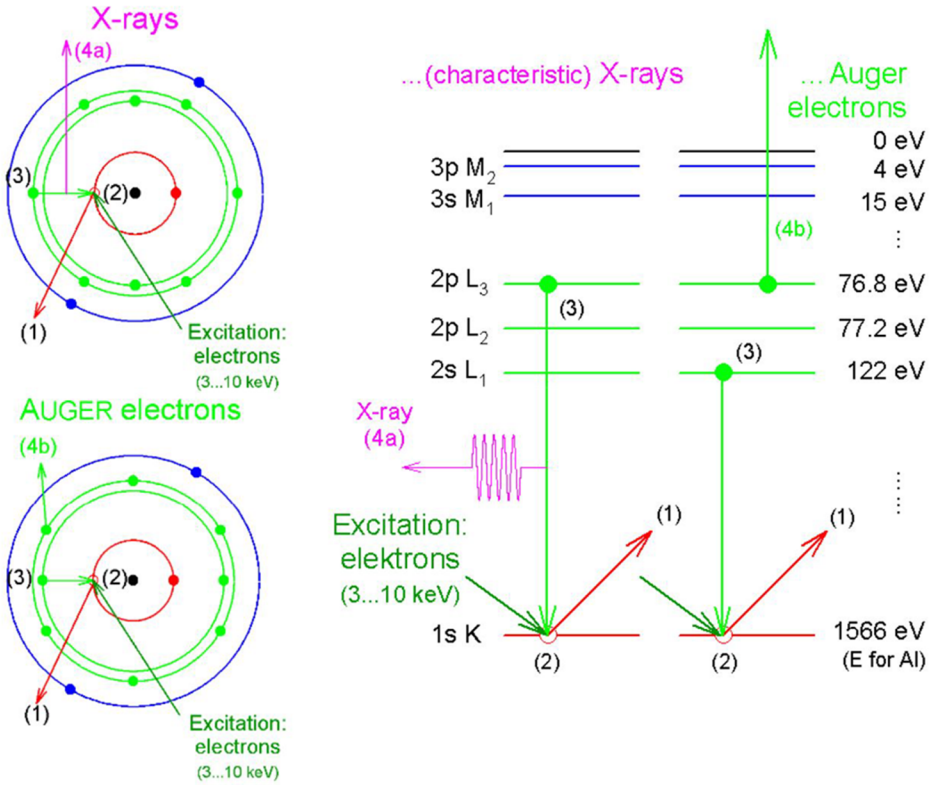


Figure 3.8 The Auger process for emission of auger electron. The inner shell of an atom is ionized (1), mainly due to electron bombardment. The vacancy (2) is filled by an electron form an outer shell. The released energy is emitted as X-ray (4a) or is transferred by electromagnetic interaction to a 3rd electron. If it gets sufficient energy it can leave the atom as Auger electron (4b).

$$X_A = \frac{(P_A/S_A)}{\Sigma(P_i/S_i)} \times 100 \qquad (3\text{-}1)$$

X_A : atomic percentage of element A

P_i : Auger peak-to-peak height of element i

S_i : elative sensitivity factor of element i

Figure 3.9 Auger electron spectroscopy fabricated by Phi cooperation, and model name is *phi 680* scanning Auger nanoprobe - Hanyang University, Korea.

The calculated atomic percent is relative values mainly due to the fact that the relative sensitivity factor did not be defined [3.3].

3.2.2 X-ray Photoelectron Spectroscopy (XPS)

X-ray photoelectron spectroscopy (XPS) in the Figure 3.10 is a quantitative spectroscopic method which can measure the elemental composition, chemical state and electronic states of elements in the material. The XPS spectra are obtained by irradiating a sample using X-ray beam. Then, the kinetic energy and number of

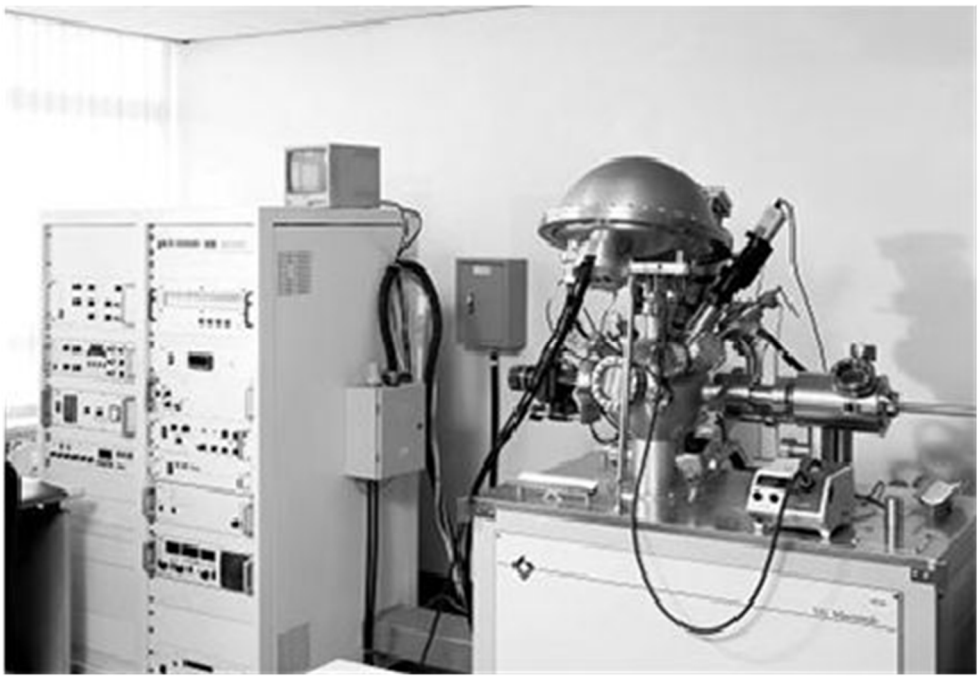


Figure 3.10 X-ray photoelectron spectroscopy fabricated by Thermo Scientific VG, and model name is *VG ESCA 220 I* - Hanyang University, Korea.

electrons which escaped from 1 nm to 10 nm of material were analyzed. XPS requires ultra-high vacuum (UHV) due to surface sensitive technique. XPS utilizes either monochromatic Al Kα or non-monochromatic Mg Kα X-ray beams to eject a photoelectron from an atom of the sample's surface. Then, an electron at a high energy level falls down to fill the hole left behind. As a result, the emitted radiation energy is used to eject an Auger electron. Therefore, XPS emits both photoelectron and Auger electrons that can be observed in the spectrum. The ejected electrons are analyzed in the XPS detector by measuring the kinetic energy of electrons, and it can provide the information to determine the kind of elements included in the sample. Figure 3.11 describes the schematic of the X-ray photoelectron process [3.4].

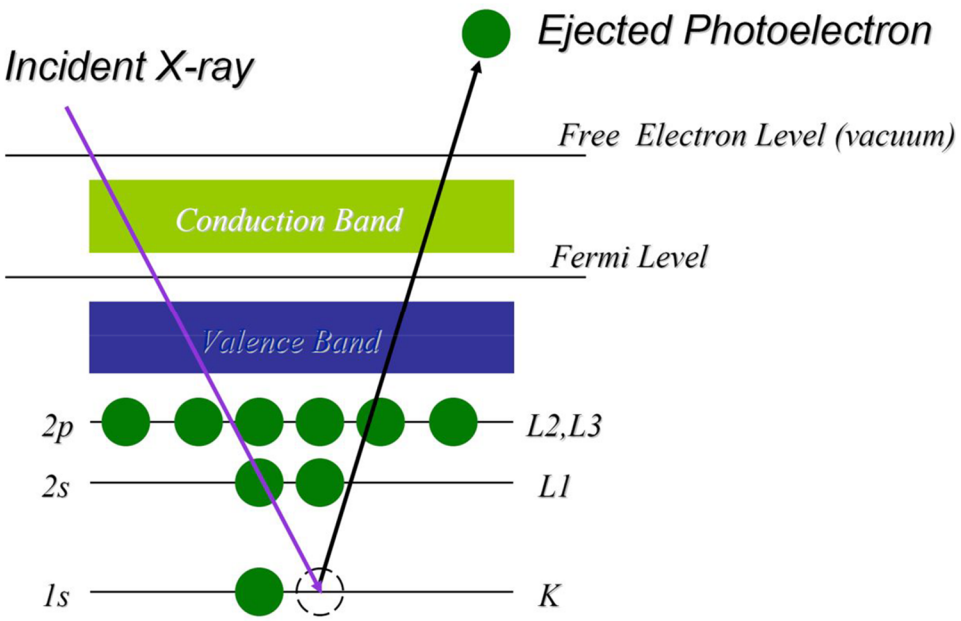


Figure 3.11 Photoelectron process by interaction between incident X-ray and inner shell electron.

The kinetic energy of the emitted electrons is named E_k, and this is determined by the following equation

$$E_k = h\nu - E_b - \Phi \tag{3-2}$$

The binding energy of an electron is represented by E_b, and the photon energy is given by hν where h represents the plank's constant and ν is the frequency of a photon. The work function is represented by Φ which is the minimum energy needed to eject an electron from sample. Figure 3.12 shows graphically the equation $E_K = h\nu - E_B - \Phi$ [3.5].

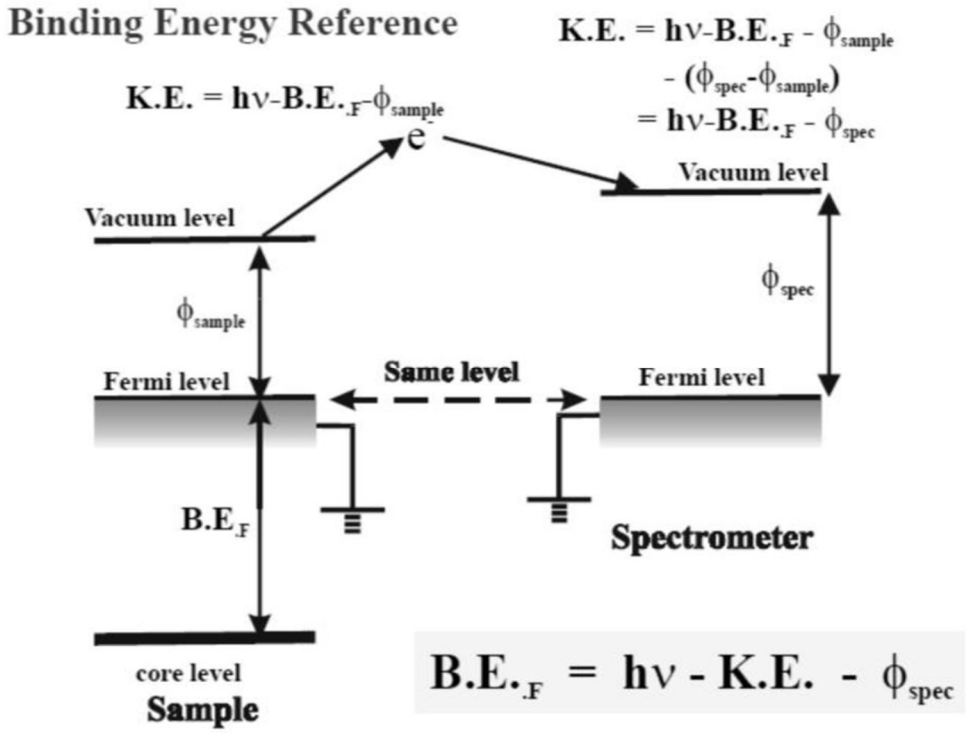


Figure 3.12 Graphically representation of the equation $E_K=h\nu-E_B-\Phi$.

3.2.3 Raman Spectroscopy

When photons are incident upon a medium, they get scattered either elastically (Rayleigh scattering) or inelastically (Raman scattering). In Rayleigh scattering, the energy of the emitted photon is the same as the incident photon. On the other hand, in Raman scattering, the energies of the scattered and incident photons are different. The change is depicted in Figure 3.13, where an incoming photon either creates a phonon and is remitted at a lower energy (anti-Stoke scatting) or annihilates a phonon and is remitted at a higher energy (Stoke scattering). The inelastically scattered light can be

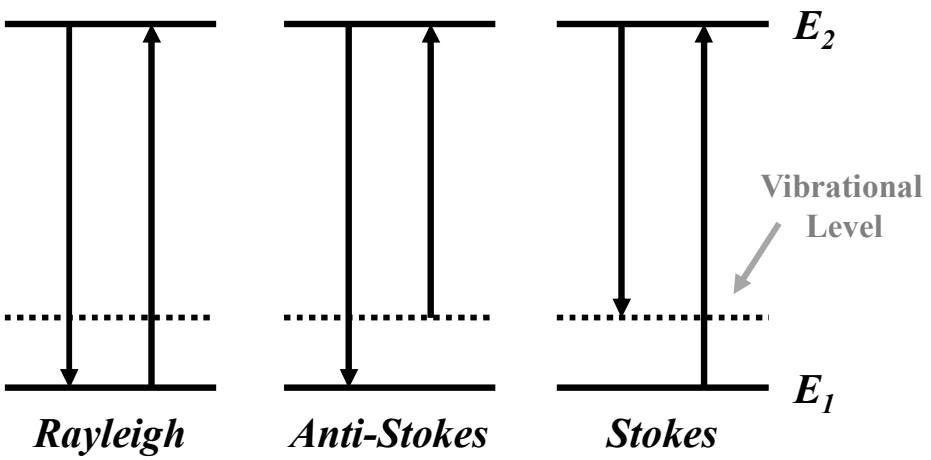


Figure 3.13 Schematic deposition of various scattering processes within a medium. The incident photon energies are marked by the right-hand-side arrows.

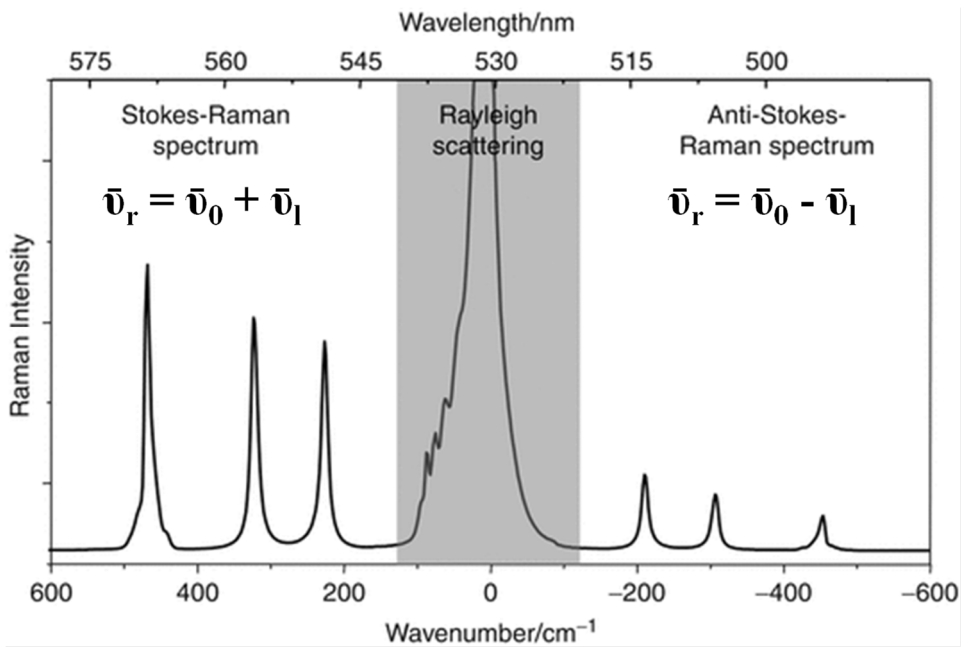


Figure 3.14 An examples of a Raman spectrum representing Rayleigh, Stokes, and anti-Stokes Raman peaks.

collected, and information about the energy levels within the medium can be deduced from the energy change in the light.

A monochromatic light source, usually an argon ion laser, is used to excite the sample and a spectrometer/PMT set is used to detect the scattered light. An example of a Raman spectrum is schematically shown in Figure 3.14.

3.2.4 X-ray Diffraction

X-ray diffraction (XRD) is a rapid analytical method which primarily used for phase identification of a crystalline material. And XRD can provide the information on unit cell dimensions. XRD is most widely used for the identification of unknown crystalline materials. The constrictive interaction of the incident X-ray with the material produces the constrictive interference (diffraction) when the condition is satisfied with Bragg's law ($n\lambda = 2d\sin\theta$) as shown in Figure 3.15. This law follows the wavelength of electromagnetic radiation to the diffraction angle and the lattice space in the crystalline material. Then, these diffracted X-rays are detected, counted, and processed. All possible diffraction directions of the lattice were attained by scanning the sample via a range of 2θ angles. XRD consists of three basic elements such as an X-ray tube, a sample holder, and an X-ray detector. The X-ray is generated in a cathode ray tube by heating a filament to emit electrons, accelerating the electrons toward a target by electric field, and bombarding the target with electrons. When the electrons have enough energy to dislodge the electrons of inner shell of target material, characteristics X-ray spectra are produced. These spectra consist of several components such as $K\alpha$ and $K\beta$. Filtering by foil or monochromatic is required to

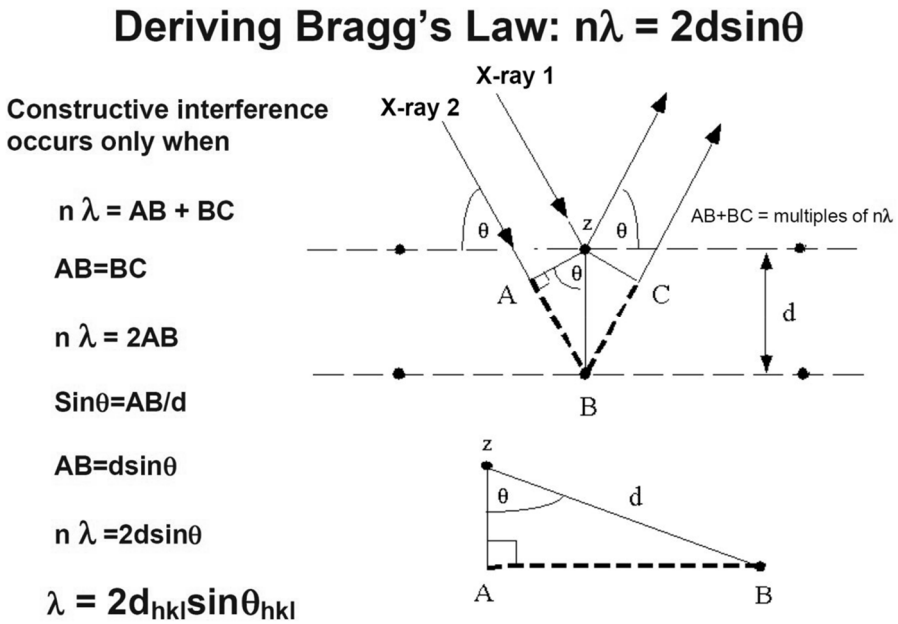


Figure 3.15 Bragg condition for X-ray diffraction.

produce monochromatic X-ray required foil diffraction. Cu is the most common target material for diffraction with Cu Kα radiation = 1.5418 Å. These X-ray is collimated and directed onto the sample. As the detector and sample are rotated, the intensities of the diffracted X-ray are recorded. When the geometry of the incident X-ray irradiated on the sample satisfied the Bragg condition, constructive interference occurs and a peak in intensity appears. A detector records this X-ray signal and converts this signal to a count rate that is output to a device such as computer monitor. The geometry of an X-ray diffraction is that the sample rotates in the path of the collimated X-ray beam at angle θ while the X-ray detector rotates at an angle 2θ. This instrument used to maintain the angle and rotate the sample is termed a goniometer. Typically, the spectra are collected at 2θ from ~5° to 70°, angles that are preset in the X-ray scan [3.6, 3.7].

3.2.5 Scanning Electron Microscopy (SEM)

A scanning electron microscopy (SEM) is probably the most widely used semiconductor characterization instrument. A schematic of a typical SEM system is shown in Figure 3.15. Electrons are emitted from a tungsten cathode either thermionically or via field emission and are focused by two successive condenser lenses into a very narrow beam. Two pairs of coils deflect the beam over a rectangular area of the specimen surface. Upon impinging on the specimen, the primary electrons transfer their energy inelastically to other atomic electrons and to the lattice. Through many random scattering processes, some electrons manage to leave the surface to be collected by a detector facing the specimen. Usually these are the secondary electrons, originated from a depth of no larger than several angstroms, that are collected by the detector. A photomultiplier tube (PMT) amplifier is used to amplify the signal and output serves to modulate the intensity of a cathode ray tube (CRT). Research quality SEMs are generally able to produce image with a resolution of ~50Å.

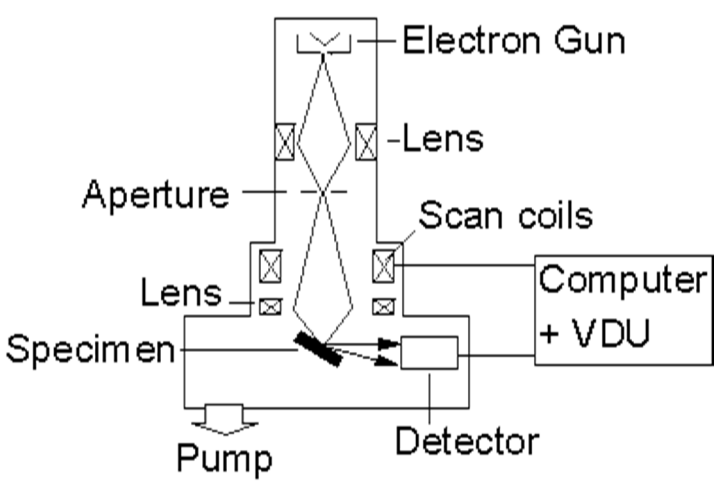


Figure 3.16 Schematic of a scanning electron microscopy.

SEM not only can provide images of the surface but also by rotating the sample, one can obtain information about the thickness of various layers in the structure (cross-sectional SEM).

3.2.6 Scanning Probe Microscopy (SPM)

Scanning Probe Microscopy (SPM) is a useful method for the study of the surface morphology. This method employs the concept of scanning an extremely sharp tip (3~50 nm radius of curvature) across the object surface. The tip is mounted on a flexible cantilever, allowing the tip to follow the surface profile (Figure 3.17). When the tip moves in the proximity of the object under investigation, forces of interaction between the tip and the surface influence the movement of the cantilever. These movements are detected by selective sensors.

There are three major types of SPM:

- Atomic Force Microscopy (AFM) measures the interaction force between the tip and the surface. The tip may be dragged across the surface, or may vibrate as it moves. The interaction force will depend on the nature of the sample, the probe tip and the distance between them.
- Scanning Tunneling Microscopy (STM) measures a weak electrical current flowing between tip and sample as they are held a very short distance apart.
- Near-Field Scanning Optical Microscopy (NSOM) scans a very small light source very close to the sample. Detection of this light energy forms the image. NSOM can provide resolution below that of the conventional loght microscope.

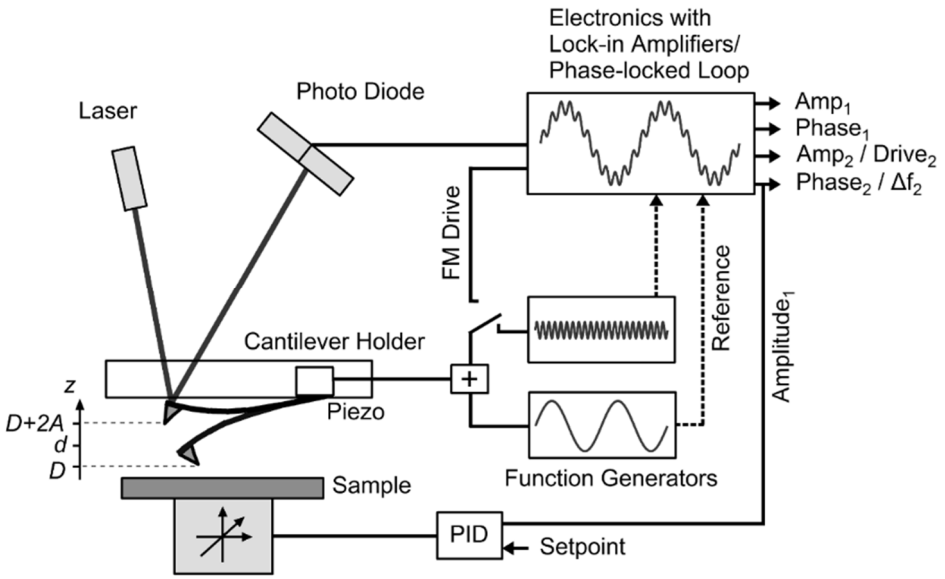


Figure 3.17 Schematic of an atomic force microscopy (AFM) tip scanning over the surface of a sample.

Essential to the system is a piezoelectric tube as shown in Figure 3.18. It consists of a piezo-material inserted inside a hollow tube. Pair of electrodes on the inner and outer walls are placed on either side of the tube. When suitable voltage differences are applied to these electrodes, one of the tube expands and the other side contracts. This results in a bending of the tube, hence if one end is fixed the other end moves, resulting in the scanning motion. Two sets of electrodes, 90 degrees apart, allow motion in the *x*-*y* plane. A further pair of electrodes extending around the entire circumference of the tube cause an entire section of the tube to expand or contract, resulting in the free end of the tube moving parallel to the tube axis (the *z*-axis). The combination of all three sets of electrodes allows movement of the free end of the tube to be controlled very precisely in all three axes. For surface mapping applications, the feedback provided by the probe and detector is used to keep the probe at a constant

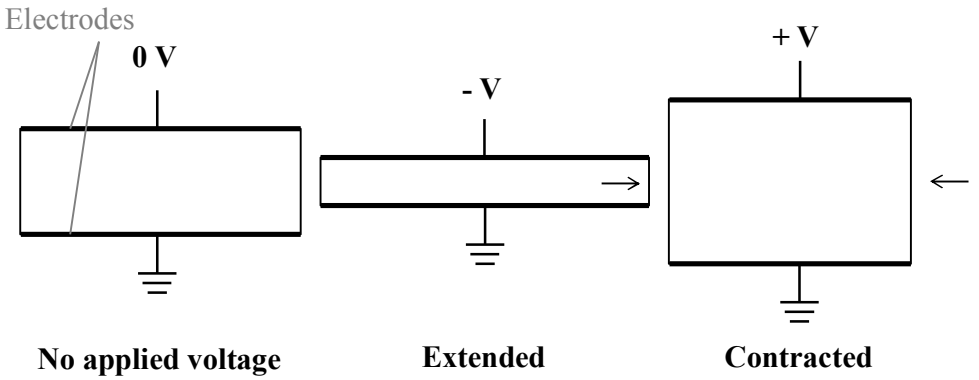


Figure 3.18 Reaction of a piezo-material to applied bias.

distance from the surface (*z*-direction) while it is free to move across the surface (*x*- and *y*- direction). This is accomplished by applying a voltage to the piezoelectric tube. This voltage is proportional to the probe's movement in *z*-direction which is then used to generate the surface topology.

In this research, AFM fabricated by Park Systems and named *XE-100* was used.

3.3 Electrical Properties Measurement

The electrical properties of the TFTs were measured using HP4140B. The threshold voltage was defined at a normalized drain current ($I_{DS} \times W/L$) of 0.1 μm at V_D = 1 V. The subthreshold swing, SS, defined as the voltage required to increase the drain current by a factor of 10, is given by

$$S = \frac{dV_G}{d(\log I_D)} \tag{3-3}$$

From the straight line in the transfer curve, S is given by the maximum slope. The field-effect mobility was derived from the transconductance (g_m) in the linear region at V_D = 0.1V, given by

$$g_m = \left.\frac{\partial I_D}{\partial V_G}\right|_{V_D=const.} = \frac{W}{L} C_i \mu_h V_D \quad (V_D < V_{Dsat}) \tag{3-4}$$

$$\mu_h = \frac{L}{WC_i V_D} g_m = \frac{L}{WC_i V_D} \left.\frac{\partial I_D}{\partial V_G}\right|_{V_D=const.} \quad (V_D < V_{Dsat}) \tag{3-5}$$

Where, W and L are width and length of channel, C_i is capacitance of insulator. We calculated the field-effect mobility of MILC poly-Si TFTs by equation (3-5) at every points of gate voltage and we calculated the mobility for maximum values. The maximum on/off ratio was defined at V_D = 10.1 V and V_G = -30 to 15 V.

CHAPTER 4

Reduction of the Leakage Current

4.1 Leakage Current Mechanism in LTPS TFTs

LEAKAGE CURRENT of poly-Si TFTs is much greater than that of single-crystal Si transistors, primarily because of carrier generation at the grain boundary and in-grain defects. The leakage current arises primarily within the space charge region between the channel and the drain. The dominant generation mechanism is thermionic field emission assisted by the high density of trap state within the poly-Si energy bandgap [4.1]. Besides, thermal emission and pure tunneling is also thought as main leakage current mechanism. The detailed explanation is mentioned next paragraph.

The three dominant mechanisms of the leakage current in poly-Si TFTs have been reported, as shown in Chapter 2.3 [4.1, 4.2]. The first (M1) is thermal emission due to thermal excitation of the trapped carrier. The second mechanism (M2) is thermionic field emission due to field-enhanced thermal excitation of the trapped carrier. The third mechanism (M3) is pure tunneling due to field ionization of trapped carrier tunneling through the potential barrier. In MILC TFTs, the M2 and M3 mechanisms

are believed to be dominant as opposed to other poly-Si TFTs. There are two scenarios for these processed. The first is the formation of many trap states within the band gap in poly-Si. In the MILC fabrication process, Ni-silicides are captured in the TFT channel regions [4.3, 4.4]. The incorporation of metallic elements into Si forms trap states [4.5]. Some impurities, such as Cu, Au or Ni, give rise to multiple levels. Therefore, it is believed that M2 and M3 become dominant in MILC poly-Si TFTs because these captured Ni silicides make multiple trap states between the band gap leading to a large dependence of the leakage current on the gate and drain voltages. The second scenario is the formation of an abrupt drain junction due to the low activation annealing temperature [4.6]. MILC TFTs undergo thermal annealing for activation at 550~600 ˚C. At these temperatures, lateral diffusion is negligible and the i/p^+ drain junctions will be effectively abrupt. Field relief is impossible in these abrupt drain junctions, indicating that M2 and M3 are dominant in MILC TFTs.

Therefore, the leakage current of poly-Si TFTs can be reduced by decreasing the density of defect states and by reducing the electric field at the drain depletion region. Because the leakage current depends strongly on drain voltage, it can be greatly reduced by placing two gates in series, so that only a portion of the drain voltage appears across each of the two drain depletion region [4.7].

4.2 Minimization of Ni Contamination

As mentioned above, the defects in the poly-Si generate the leakage current because, they act as trap state in the forbidden band gap. The main drawback of the conventional MILC poly-Si TFTs is the high leakage current due to Ni, which used as

catalyst for crystallization of a-Si thin film, contamination in channel. In this chapter, newly developed crystallization methods, the SIC and SILC, are presented.

4.2.1 Silicide Induced Crystallization

LTPS TFTs are attractive for use in various fields, such as AM-FPDs, because they exhibit good electrical properties and can be integrated in peripheral circuits on inexpensive glass substrates [4.8]. In addition, flexible substrates can be used when low temperature crystallization of a-Si is realized. Therefore, intensive studies have been made on lowering the crystallization temperature of a-Si. Among the crystallization methods, the most popular method is MIC using Ni [4.9]. The MIC method has many merits, much more than other approaches, such as ELA, or SPC, because it requires a relatively low thermal budget, is a simple process, with low cost, etc. However, the major problem to be addressed for MIC poly-Si is Ni contamination, such as Ni silicide, since Ni contamination degrades the electrical performance of the device.

Several crystallization methods have been utilized to reduce the unwanted Ni precipitates, such as MILC [4.10-4.12], MIC through capping-layer (SiN_x, SiO_2) [4.13], and the gettering of Ni within the MILC [4.14]. However, these methods are complicated and require high process temperatures, and very long times which can damage the poly-Si active layer. To reduce Ni contamination and to fabricate high performance poly-Si TFTs, we have studied SIC using *in-situ* silicidation during Ni deposition, where the Ni was deposited by sputtering at room temperature. According

to our previous reports, dot shaped Ni silicide are formed by Ni sputtering at room temperature, and they can act as nuclei during crystallization [4.15-4.17].

In this small chapter, we propose a novel process, called SIC, which uses Ni silicide for crystallization of a-Si to reduce Ni precipitates. Therefore the trap states were minimized and high performance characteristics of the poly-Si TFT are obtained by SIC method. Moreover, the effect of Ni silicide density on the SIC poly-Si TFTs was also investigated by *in-situ* silicidation at room temperature, 100 ℃, 200 ℃, and 300 ℃, and we studied the behavior and distribution of the trap-states formed by Ni silicides, which strongly affect the performance of SIC poly-Si TFTs.

4.2.1.1 Silicide Density Effect on SIC Poly-Si TFTs

In order to investigate the Ni silicide density effect on crystallization phenomenon, The Ni was deposited at various temperature to form *in-situ* Ni silicide on the a-Si thin film. The partially crystallized Ni silicide seeds were observed through a short time annealing process, at 550 ℃ for 30 min, as shown in Figure 4.1. It can be seen that the density of partially crystallized Ni silicide seeds (white color) are increased with Ni deposition temperature. It is already explained that the increasing of Ni deposition temperature changes the phase of Ni silicide seeds on the a-Si from Ni rich silicide phase (Ni_2Si) to Si rich silicide phase ($NiSi_2$). Then the $NiSi_2$ acts as nuclei to crystallization, by the lattice mismatch between the crystallized Si and Ni silicide [4.18]. From these nuclei, lateral crystallization proceeds with increasing annealing time and temperature. The needle-like crystalline Si grains grow toward the a-Si region with the migration of $NiSi_2$, and the individual crystallites grow from

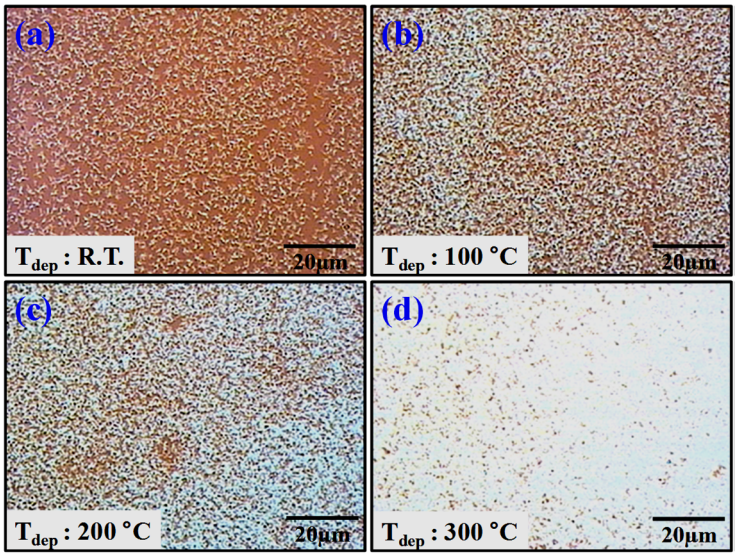


Figure 4.1 Optical microscope images of Ni silicide seed deposited at various in-situ silicidation temperatures, for which short time annealing was carried out at 550 °C for 30 min.

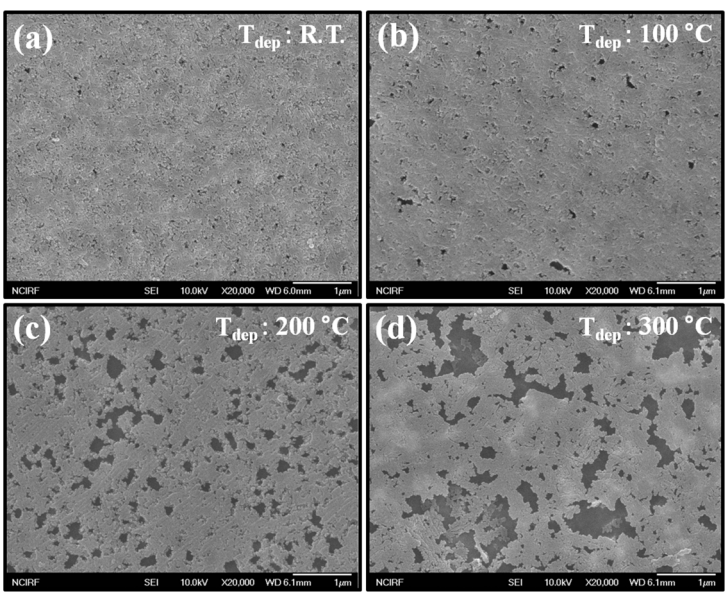


Figure 4.2 FESEM images of fully crystallized SIC poly-Si thin-films after Secco etchant treatment.

crystallized networks during lateral crystallization [4.3, 4.11, 4.12, 4.18-4.23]. If the $NiSi_2$ at the front of a crystalline Si grain meets others, which have already been crystallized by the $NiSi_2$ induced crystallization, the $NiSi_2$ cannot migrate through the crystal Si grains because there is no chemical potential-driving force for the phase transformation between the two crystal grains [4.3, 4.23]. Therefore, $NiSi_2$ located at the front of a crystal is captured at the boundary between two crystal grains, grain boundary, and the captured Ni silicide will act as a defect, which is a major cause of electrical performance degradation of the SIC poly-Si TFTs.

The captured Ni silicides (Ni_2Si, NiSi, and $NiSi_2$) were observed by field emission SEM (FESEM) after full crystallization at 550 °C for 2 h followed by Secco etching ($Fe_2Cr_2O_7$ + HF + H_2O) as shown in Figure 4.2. Note that the holes (dark color) are piled up with increasing Ni deposition temperature. This means that the Ni silicide seeds are more excessively formed and captured at higher Ni deposition temperature.

The I_D-V_G transfer characteristics of SIC poly-Si TFTs fabricated by *in-situ* silicidation at various Ni deposition temperatures is shown in Figure 4.3. The curves reveal that firstly, the on-state current at gate voltage of -30 V and the field-effect mobility at maximum trans-conductance are significantly decreased, from 2.0×10^{-4} A to 4.2×10^{-6} A and from 40.24 cm2/Vs to 3.75 cm2/Vs respectively, with the increasing *in-situ* silicidation temperature, from room temperature to 300 °C. These results show that the poor electrical properties of the SIC poly-Si TFTs occur with the increase of *in-situ* Ni silicidation temperature. This can be understood, because the captured Ni silicide density is low at a lower *in-situ* silicidation temperature: the captured Ni silicide between crystallites traps charge carriers and builds up potential barriers to the flow of carriers [4.24]. Secondly, in the case of leakage current, the off-state leakage current at positively biased gate voltage is drastically increased with

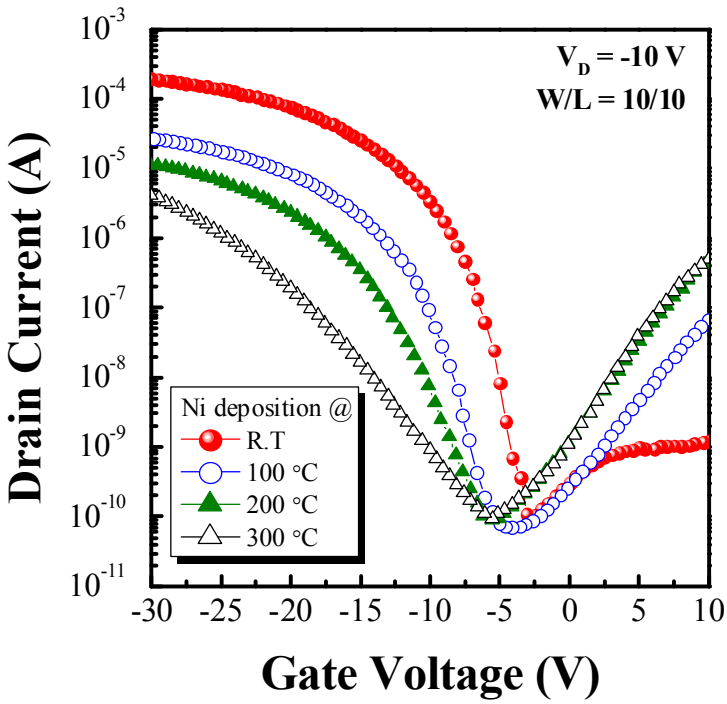


Figure 4.3 Comparison of I_D-V_G transfer characteristics of SIC poly-Si TFTs fabricated at various Ni deposition temperatures.

in-situ silicidation temperature. Moreover, the gate voltage of the minimum leakage current is shifted towards the negative direction, while the quantity of minimum leakage current stands almost the same, which means that the threshold voltage is shifted by captured Ni silicides. It is generally known that the captured Ni precipitates, such as Ni and Ni silicides, strongly affect leakage current and threshold voltage shift, because Ni precipitates form charged trap-states in the band gap of poly-Si [4.6, 4.25-4.27]. Lastly, the subthreshold slope is anomalously increased from 0.75 V/dec (room temperature) to 2.95 V/dec (300 °C). The subthreshold slope should be strongly related to grain boundary trap-state density (N_t) and interface trap-state density (N_{it}).

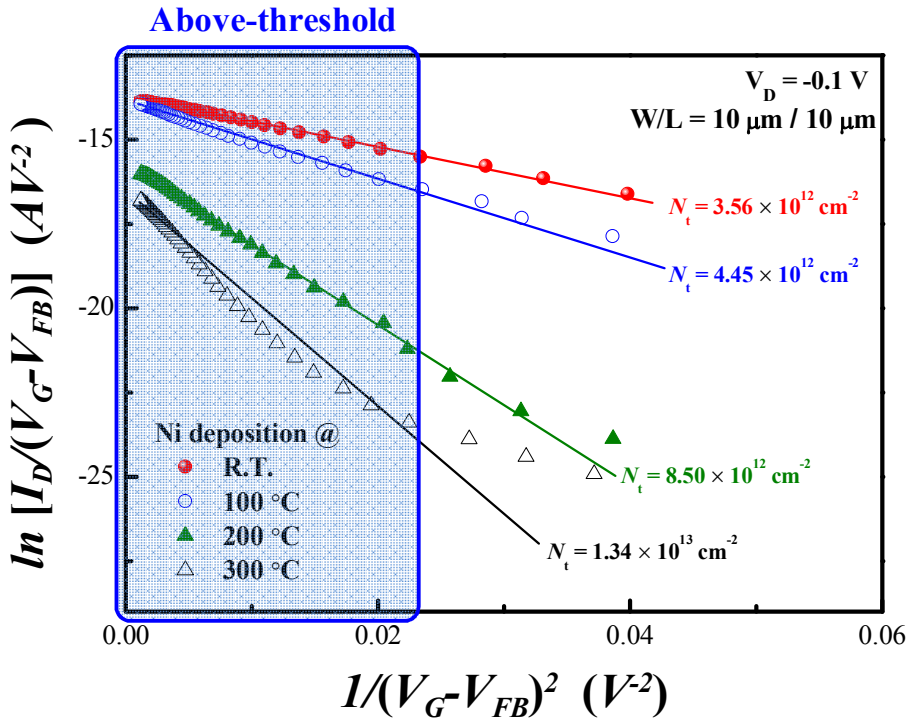


Figure 4.4 Levinson and Proano plots and grain boundary trap-state densities of SIC poly-Si TFTs fabricated by in-situ Ni silicidation at various temperatures.

Grain boundaries and interface trap-states act as recombination sites, which are obstacles to channel inversion during gate biasing in the band gap, because the charge carriers such as electrons and holes are captured into the trap-states.

In Figure 4.4, the grain boundary trap-state density, as well as the dominant threshold slope degradation source and result from captured Ni silicide in the channel region, was determined using the method of Levinson [4.28] and Proano [4.29], which can estimate the grain boundary trap-state density from the slope of the linear region of the curve $\ln[I_D/(V_G-V_{FB})]$ versus $(V_G-V_{FB})^{-2}$ at low drain voltage and high gate voltage. The plots were given by equation (2-19).

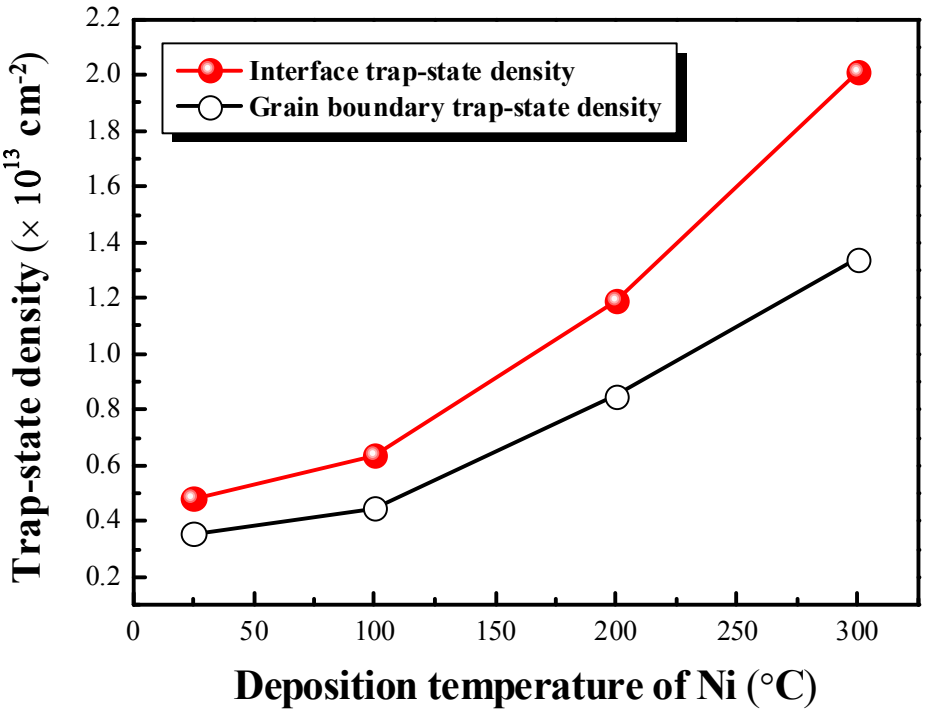


Figure 4.5 Interface and grain boundary trap-state density changes of the SIC poly-Si TFTs as a function of Ni deposition temperature.

The lower slope corresponds to the lower trap density. From Figure 4.4, it was observed that the slope gradually increases with *in-situ* silicidation temperature, this is due to increase of grain boundary trap-state density.

The interface between the SIC poly-Si and SiO_2 trap-state density was determined from the subthreshold slope by using the Dimitriadis model [4.30] as follows:

$$SS = \left(\frac{qN_{it}}{C_{ox}} + 1\right)\frac{kT}{q} ln\, 10 \qquad (4\text{-}1)$$

where q is the electron charge, k the Boltzmann constant and C_{ox} the gate insulator capacitance. The result of the extraction is shown in Figure 4.5. With increased *in-situ* silicidation temperature, a greater number of interface trap-state densities are generated. Note that the interface trap-state should not change according to the Ni silicide density of the active layer, supposing that the SiO_2 of the gate insulator layer is deposited after crystallization of the active layer. [4.31] However from the experimental, the interface trap-state density was increased with grain boundary trap-state density, with the increase of *in-situ* Ni silicidation temperature. So far, it was thought that the Ni silicide residues forming the grain boundary trap-state anomalously generate the charged trap-states in the interface, by reaction of Ni silicides and N_2O gas, which is used as a source gas during gate insulator deposition, at grain boundaries. The relative area of grain boundary was increased along with the *in-situ* silicidation temperature. Therefore, the enlarged relative grain boundary area was affected, to form a much higher quantity of charged trap-states in the interface.

4.2.1.2 SIC Thin Film Analysis

The changes of the Si and Ni XPS before and after Ni removal on the a-Si are shown in Figure 4.6. From Figure 4.6(a), the Si peaks had a binding energy of 99.5 eV before and after Ni removal, whilst the broad oxidized Si peaks appeared differently. The oxidized Si peak before Ni removal was lower than that after the Ni removal, indicating that the exposed Si surface was chemically oxidized during the Ni removal in H_2SO_4 [4.32]. The Oxidized Ni (mixture of NiO, NiO_2, and elemental Ni) and deposited Ni on the a-Si were removed by dipping in 70 °C H_2SO_4 for 30 min, as

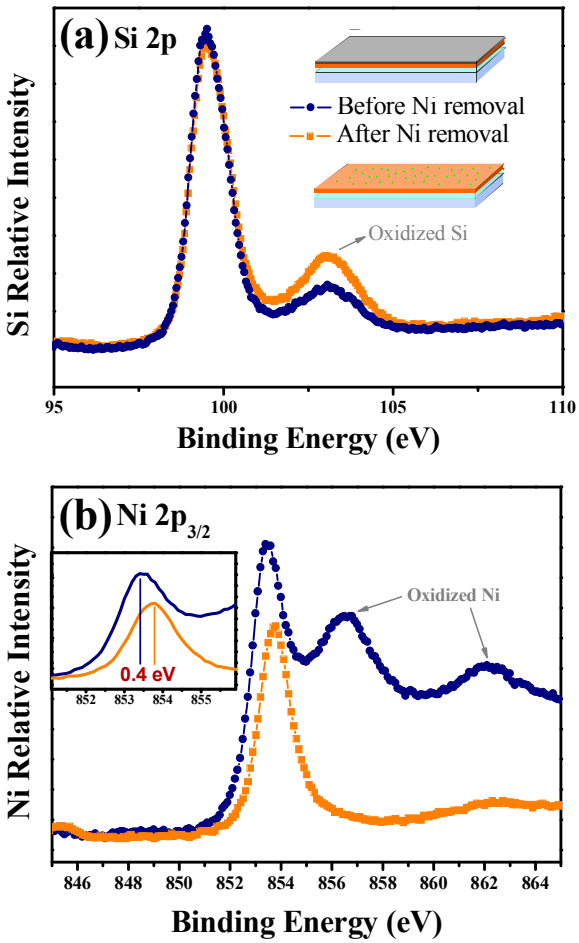


Figure 4.6 XPS spectra before and after Ni removal on the a-Si films before crystallization. Comparison of (a) Si relative intensity (binding energy around 99 eV) and (b) Ni relative intensity (binding energy around 855 eV).

shown in Figure 4.6(b). After removing Ni and oxidized Ni, only the Ni silicide phase remained, which appeared at the binding energy of 853.6 eV [4.18, 4.33, 4.34]. It can be found that the binding energy of Ni2*p* was shifted. This change in the binding energy reflect the charge transfer from Ni to Si upon Ni-Si bond formation [4.34].

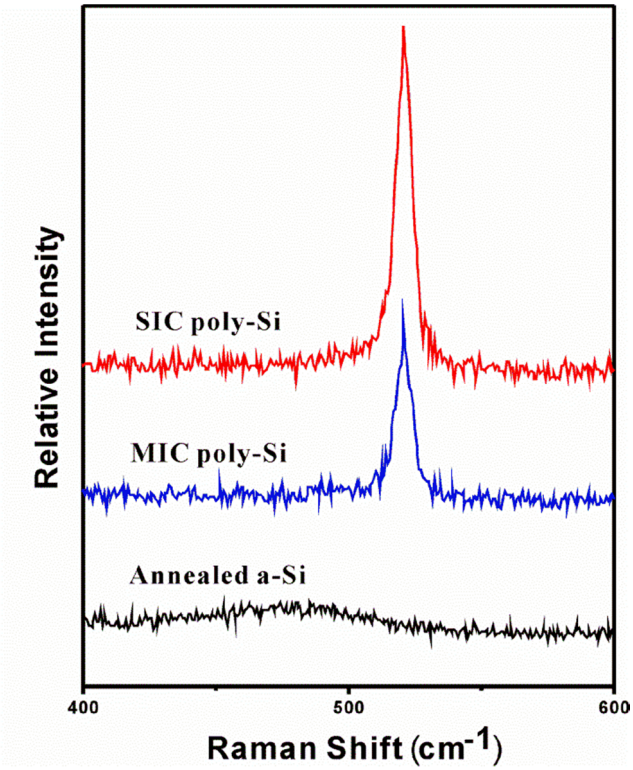


Figure 4.7 Raman spectra of annealed a-Si, MIC and SIC poly-Si thin films.

Therefore, the presence of Ni-Si bond as silicide seeds formed nuclei for crystallization during the annealing process.

Raman spectra of the three samples are shown in Figure 4.7. Annealed a-Si without Ni layer (annealed a-Si), with Ni layer (MIC poly-Si), and the film that underwent Ni removal after deposition (SIC poly-Si) were measured. The a-Si films were 1000 Å thick and were annealed at 500 °C for 1 h. The spectrum of the a-Si showed a broad structure near 480 cm^{-1}, with a full-width-at-half-maximum (FWHM) of about 60 cm^{-1}. This transverse optical spectrum is typically associated with a-Si. The spectrum of the MIC poly-Si thin film had a peak centered at 520 cm^{-1} with FWHM of 7.2 cm^{-1}, which was larger than the value of 6.0 cm^{-1} obtained for the SIC poly-Si thin film. The

intensity of MIC poly-Si was lower than that of the SIC poly-Si, indicating that the crystallinity of MIC poly-Si thin film was lower than that of the SIC poly-Si thin film. The absence of the broad peak centered at 480 cm^{-1}, indicated that MIC and SIC had occurred and the a-Si thin film was fully crystallized after annealing at 500 °C for 1 h. In addition, the maximum Raman peak of SIC poly-Si film appears at 520.86 cm^{-1}, indicating that the poly-Si film is under less tensile stress than the conventional excimer laser crystallized poly-Si thin film showing the peak at 517.12 cm^{-1} [4.35].

In order to investigate the Ni contamination in MIC and SIC poly-Si thin films after crystallization, Auger electron spectroscopy (AES) spectra were analyzed. Figure 4.8 shows the AES spectra of the surface of the MIC and SIC poly-Si thin films crystallized at 500 °C for 1 h. The Si and oxygen peaks were present in both MIC and SIC poly-Si; however, the Ni peak at kinetic energy of 801 eV was only present in the SIC poly-Si. These results indicate that the Ni contamination of SIC poly-Si was lower than that of MIC poly-Si.

The relative atomic percentages of each element on the surface of MIC and SIC poly-Si are listed in Table 4.1. Relative Ni atomic percentage of SIC poly-Si was 1.79%, which was lower than that of MIC poly-Si (16.26%). The atomic percentage of Ni (16.26%) was higher than that of Si(4.22%) in the surface of MIC poly-Si.

However, opposite result was shown in SIC poly-Si (1.79% Ni, 5.63% Si). This indicates that the MIC poly-Si consists of a Ni-rich silicide phase. However, in case of SIC poly-Si, a values that indicates the Ni is in a more Si-rich environment than that of MIC. Both poly-Si films had a high percentage of oxygen due to the presence of oxidized Ni and Si on the surfaces.

To observe the surfaces of MIC and SIC poly-Si using optical microscopy and SEM, the samples were Secco etched. Secco etchant can selectively etch a-Si and Ni

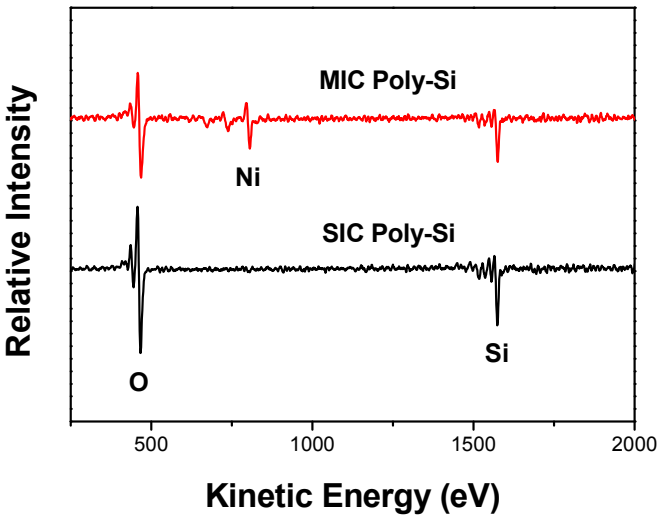


Figure 4.8 AES spectra of SIC poly-Si and MIC poly-Si thin films (area 50 μm × 50 μm) at 500 °C after 1 h of crystallization heat treatment.

Table 4.1 The relative atomic percentages of each element on the surface of MIC and SIC poly-Si thin films

[%]	MIC poly-Si	SIC poly-Si
O	60.90	84.77
Si	4.22	5.63
Ni	16.26	1.79

silicide from crystalline Si. Figures 4.9(a) and (b) show the optical microscope images of SIC and MIC poly-Si, respectively. As shown in Figure 4.9(a), the a-Si was crystallized by grain growth using Ni silicide seeds as nuclei, while the MIC poly-Si- Figure 4.9(b) showed a very porous structure and the grains were not well defined due to the whole crystallized region being etched. Many Ni silicides were on the surface as Ni atoms were supplied from the Ni metal film, and excessive Ni atoms were injected to the MIC film [3.36]. This result indicates that the grain size of the low

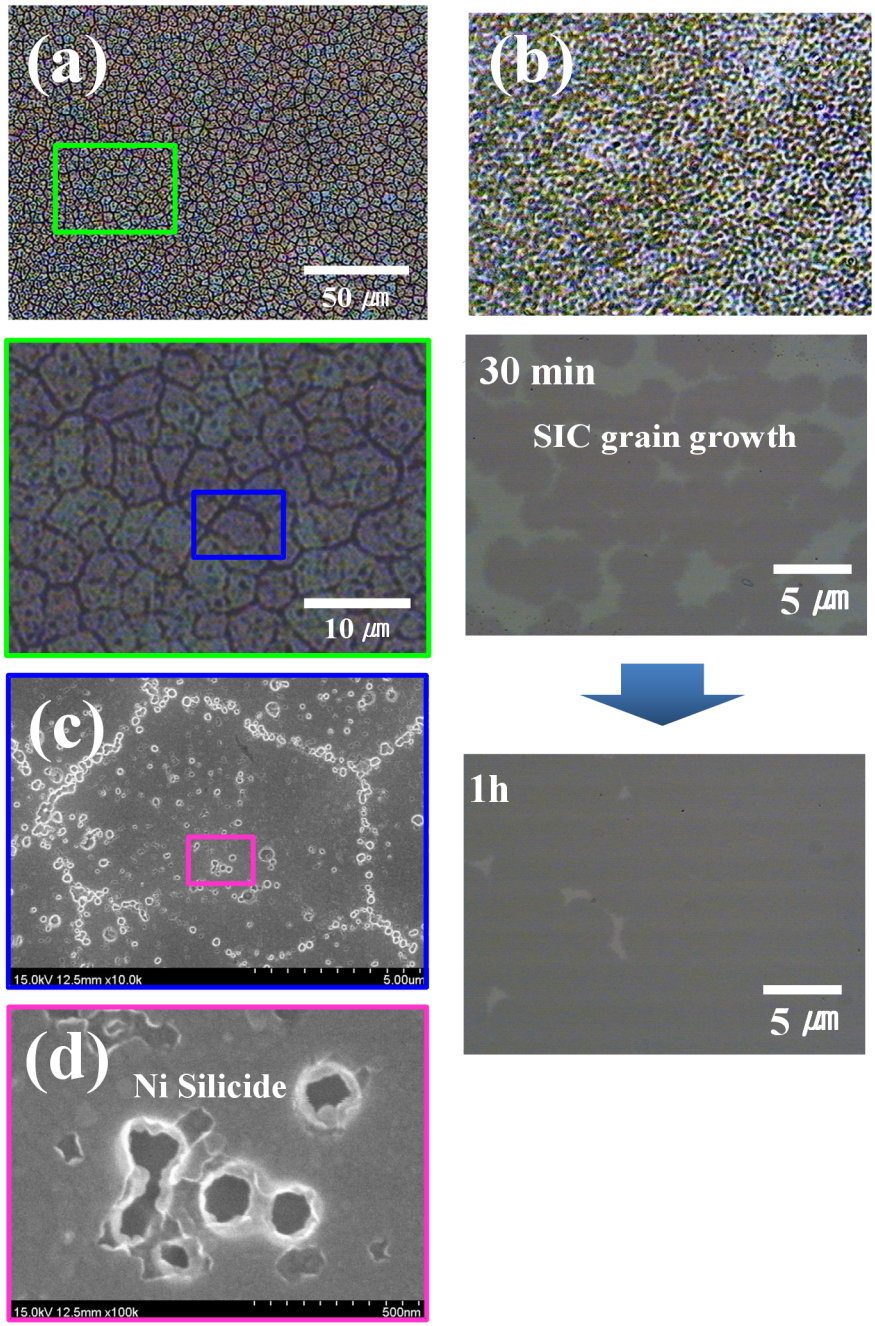


Figure 4.9 Optical micrographs and SEM images of poly-Si films crystallized by (a) MIC, (b) SIC. (c) and (d) Magnified box areas in (a) and (c) respectively.

Ni concentrated poly-Si film was larger than that of the high Ni concentrated poly-Si film. During crystallization annealing, Ni silicides migrated laterally and densely aggregated at the grain boundaries, and some captured Ni silicides remained inside the laterally grown region - see magnified SEM images shown in Figures 4.9(c) and (d).

In MILC, it is well known that some captured Ni silicides exist in the MILC region. Needlelike c-Si grows toward the c-Si region with the migration of $NiSi_2$ and the individual crystallites form networks. When the $NiSi_2$ layer at the front of c-Si grain meets other c-Si grains that have already been crystallized by the MILC process, the $NiSi_2$ layer cannot migrate through the c-Si grains anymore because there is no difference in chemical potential between the two c-Si regions, and thus these captured silicides remain in the MILC region. From the point of view of the MILC mechanism, the SIC and MILC poly-Si thin films have very similar characteristics.

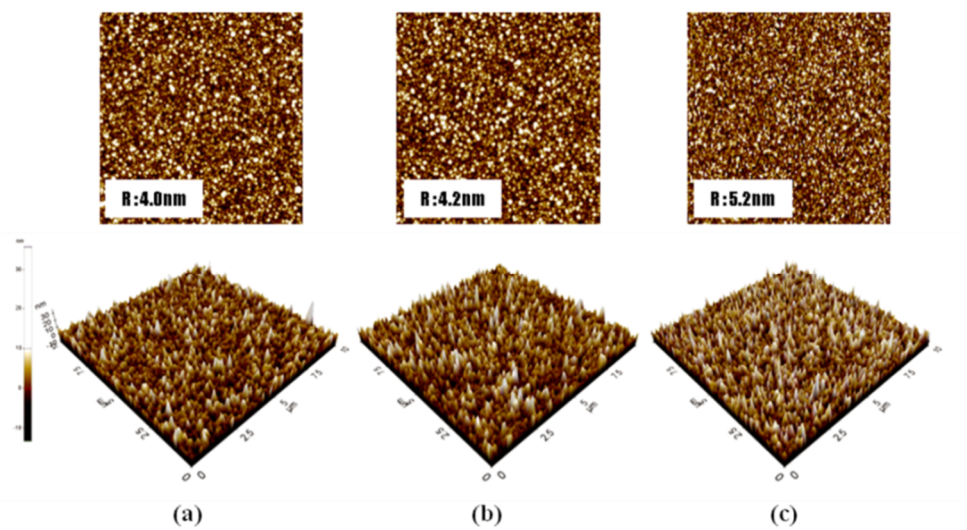


Figure 4.10 AFM topology and three-dimensional images of the three surfaces (a) a-Si, (b) poly-Si after SIC, and (c) poly-Si after MIC, after crystallization annealing and subsequent un-reacted Ni removal at 70 °C for 30 min. R: root mean square (RMS).

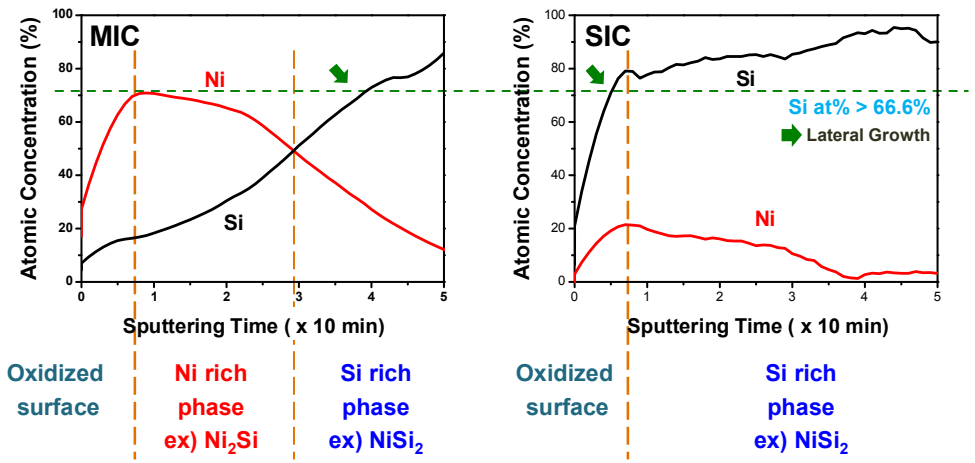


Figure 4.11 AES depth profiles of Si and Ni concentration in (a) MIC and (b) SIC poly-Si thin films.

AFM was used to evaluate the morphology of the surfaces of the a-Si, SIC and MIC poly-Si thin films. Figure 4.10 shows the topological morphologies and three-dimensional images of a-Si, SIC, and MIC poly-Si after crystallization annealing and subsequent unreacted Ni removal. The a-Si was the smoothest amongst the three samples in terms of root mean square (RMS) and the RMS of SIC poly-Si is lower than that of MIC poly-Si, because the concentration of SIC poly-Si was very low compared with poly-Si, crystallized by MIC. The AFM images confirm that SIC forms larger grains than MIC (cf. Figure 4.9).

AES depth profiling was performed on MIC and SIC poly-Si films to further investigate the film characteristics. The concentration variations of selected elements (Si, Ni) across the 1000-Å-thick poly-Si, crystallized by MIC and SIC, are plotted in Figure 4.11. Prior to the measurement, unreacted Ni was removed by H_2SO_4 at 70 °C for 30 min after crystallization annealing. As shown in Figure 4.11(a), Ni

concentration of MIC poly-Si near the surface was 70%, which was higher than that of Si (18%); however, on increasing the depth, the Ni concentration was reduced to 15% and the Si concentration increased to 80%. For SIC poly-Si - Figure 4.11(b), the Ni concentration did not drastically change and was always lower than that of Si with Ar sputtering time. Both the MIC and SIC poly-Si showed very low concentrations of Ni and Si at the surfaces, indicating that Ni on the surface and the poly-Si surface were partly oxidized.

4.2.1.3 SIC Poly-Si TFTs

Figure 4.12 shows the I_D-V_G transfer characteristics of the *p*-channel poly-Si TFTs, which were fabricated using MIC, MILC, and SIC. The measured and extracted parameters are summarized in Table 4.2. 10 transistors (W/L = 10/10 μm) were randomly selected per sample and the key parameters were calculated for average values. The determinations of key parameters are explained in the chapter 2.4.

The electrical properties of SIC-TFTs showed lower leakage current, higher on-state current, higher effective mobility and better subthreshold slopes than those of MIC-TFTs and the electrical properties were similar to those of MILC-TFTs. Comparing SIC and MIC-TFTs, the electrical properties improved by the SIC method especially the off-state leakage current, on-state current and ON/OFF current ratio. Compared with MIC-TFTs, SIC-TFTs showed a 54.4-fold decrease in off-state leakage current and a 2.19-fold increase in on-state current, resulting in an 85.09-fold increase in the ON/OFF current ratio.

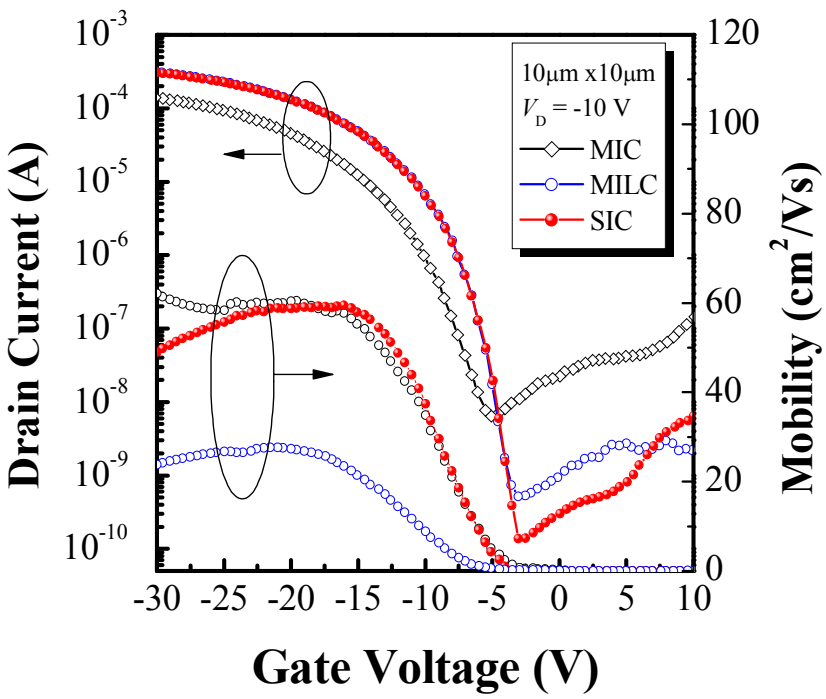


Figure 4.12 Electrical properties of the *p*-channel poly-Si TFTs fabricated by MIC, MILC, and SIC.

Table 4.2 Device key parameters of the MIC, MILC, and SIC poly-Si TFTs

Key Parameters	MIC	MILC	SIC
Field-effect mobility (cm^2/V-s)	29.86 ± 4.0	57.6 ± 3.5	62.08 ± 3.8
Threshold voltage (V)	10.11 ± 1.04	7.52 ± 0.86	7.42 ± 0.98
Subthreshold slope (V/dec)	1.56 ± 0.23	0.9 ± 0.11	0.73 ± 0.08
Minimum leakage current ($\times 10^{-10}$ A)	63.7 ± 3.41	2.76 ± 3.51	1.17 ± 3.55
Maximum on current ($\times 10^{-4}$ A)	1.40 ± 1.12	3.10 ± 1.11	3.07 ± 0.85
Maximum on/off ratio ($\times 10^5$)	0.21	11.23	17.87

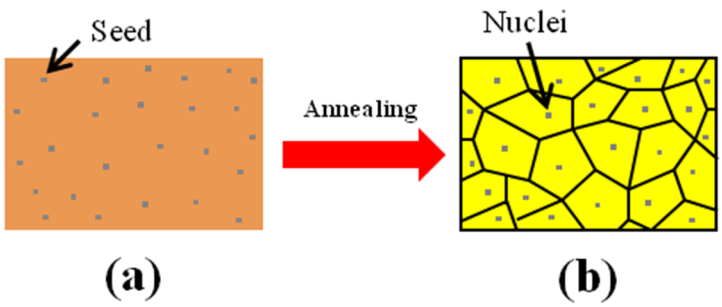


Figure 4.13 Schematic diagram of the grain growth during crystallization annealing (a) seeds on the a-Si film before annealing (b) SIC poly-Si film after annealing

The leakage current improvement was attributed to the reduction of Ni concentration in the poly-Si films. Ni residues in the poly-Si thin films served as deep-level trap states, which promoted thermionic emission that dominated leakage current in the low-gate and drain-voltage region (Figure 4) [4.1-4.7]. With the reduction of the Ni concentration in SIC, the minimum off-state leakage current reduced and therefore the on/off current ratio increased. It is thought that MIC poly-Si has many trap states, compared to SIC poly-Si, in grain boundaries and these states take charge carriers and build up potential barriers allowing the flow of carriers. The presence of the potential barriers and the additional scattering at the grain boundaries lead to field-effect mobility degradation. The high density of the trap states increases the subthreshold slope, the threshold voltage, and the off-state leakage current [4.13].

To explain the improvement of the electrical properties compared to MIC poly-Si TFTs, Figure 4.13 illustrates the effects of the seeds in a-Si on the grain growth after crystallization. It is well known that the grain size affects the electrical properties such as on-state current [4.37]. After dipping in H_2SO_4, the remaining Ni from the silicide form seeds, which act as nuclei, from which grains are laterally grown. These seeds

are advantageous as in the MIC method the Ni silicide covers the whole surface, resulting in small grains of poly-Si. In other words, with the reduction of Ni concentration, the grain size is enlarged, enhancing the electrical properties such that they are close to those of MILC TFTs.

4.2.2 Silicide Induced Lateral Crystallization

LTPS TFTs are attractive for use in various fields, such as AM-FPDs, because they exhibit good electrical properties and can be integrated in peripheral circuits on inexpensive glass [4.8] or flexible substrates [4.38]. In order to lower the crystallization temperature of a-Si films, intensive studies have been performed. SPC and ELA are common methods for crystallizing a-Si. SPC is a well-known process, but the normal crystallization temperature and time, which are around 600 °C and 24 h, respectively, are too high and long to utilize common glass and flexible substrates in the process [4.39]. Besides, SPC poly-Si TFTs have a field-effect mobility of less than about 25 cm^2/Vs, due to the significant reduction of the lateral grain size as the thin film thickness decreases. The ELA methods has been developed in order to achieve the high performance of poly-Si TFTs [4.40], but a couple of problems remain to be solved, such as the non-uniform crystalline quality and high production cost.

It is well known that the crystallization temperature of a-Si can be lowered by adding some metals. This is called MIC. This phenomenon has been reported for various metals and they can be classified into two groups: one is eutectic-forming metals, such as Ag [4.41, 4.42], Au [4.43], Al [4.42, 4.44, 4.45], Sb [4.45], and In

[4.46], and the other is silicide-forming metals, such as Pd [4.47, 4.48], Ti [4.49], Ni [4.10, 4.26, 4.50, 4.51], and Cu [4.52]. However, devices fabricated by the MIC method have poor electrical properties due to contamination with undesirable metal residues in the channel region. In order to overcome these drawbacks, it was reported that a thin layer of Ni or Pd deposited and patterned on a-Si thin films induced lateral crystallization at a temperature of as low as 550 °C [4.10, 4.19, 4.23, 4.53]. This phenomenon is called MILC. In the case of Ni-MILC, it is known that the Ni silicides formed to act as catalysts have low lattice mismatch (about 0.4%) with Si. Ni-induced laterally crystallized poly-Si has fewer micro-defects, scattering and trapping sources, and this is due to the low Ni silicide contamination and micro-twins presence [4.19, 4.53]. Therefore, most studies have concentrated on Ni-MILC TFTs. However, the relatively high leakage current and low field-effect mobility are regarded as problems for employing this technology. Therefore, much research related to overcoming these problems in MILC TFTs has been performed [4.54, 4.55]. It has been known that the main reason for these problems is the trapping of Ni, NiSi, and $NiSi_2$ precipitates in the poly-Si grain boundaries, which increase the leakage current, reduce the field effect mobility, and shift the threshold voltage [4.6, 4.25, 4.26]. Several crystallization methods and the development quality of poly-Si processes have been utilized to reduce the unwanted Ni precipitates, such as Ni off-set MILC [4.12, 4.18], MIC through capping-layers (SiN_x) [4.13], and the gettering of Ni within MILC [4.14]. However, these processes are complicated and require high process temperatures and very long annealing times, which can damage the poly-Si active layer.

In this study, we propose a novel and simple process, called SILC, which uses seeds of silicides to reduce Ni precipitates. There are no additional processes that are not observed in conventional MILC TFT fabrication, such as photolithography, deposition,

and/or etching processes. The interface trap density of MILC-TFTs is minimized by using different sorts of catalysts and high-performance characteristics of the SILC poly-Si TFTs are obtained.

Furthermore, it has been reported that the MIC/MILC boundary which is start point of MILC has many defect as well as trapped Ni silicides [4.18, 4.55]. So the electrical performance of self-aligned MILC poly-Si TFT is worse than off-set MILC TFT. But, the newly developed SILC is different from MILC in terms of SILC has not defect at SIC/SILC boundary due to SIC is also partially lateral crystallization. Then, the self-aligned structure was applied to SILC method in represented research.

4.2.2.1 Off-Set SILC Poly-Si TFTs

In Figure 4.14, optical micrographs after (a) MILC and (b) SILC annealing at 550 °C for 4 h are shown. Ni was removed after crystallization for MILC, while Ni was removed before crystallization for SILC. It can be noticed that, in the case of MILC, the color of the MIC area (Region A) is different from that of the MILC area (Region B); but in the case of SILC, the color of the SIC area (Region C) is the same as that of the SILC (Region D) area. It can be thought that the difference of the optical micrograph color imply the difference of crystalline texture and crystallization mechanism. The color of region A is brighter than those of the other regions. This is because of the difference between the crystallization mechanisms of MIC and MILC due to the different concentrations of Ni silicide in regions A and B. Since there was a Ni layer in region A during annealing, the region should contain a lot of Ni silicide.

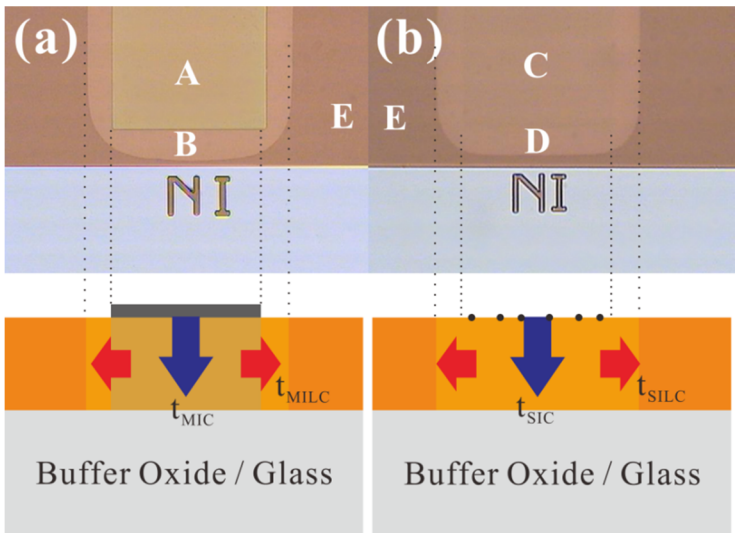


Figure 4.14 Schematic diagram of the grain growth during crystallization annealing (a) dot shape of Ni silicide on the a-Si film before annealing (b) SIC poly-Si film after annealing.

While, it is well known that MILC proceeds by the catalytic reaction of Ni silicide so that, in region B, there exists only a small amount of the Ni silicide trapped at the grain boundaries [4.10]. Region C and D contain almost the same and a lower amount of the Ni silicide, respectively, than that of region A because Ni was removed before annealing. Namely, the crystallization mechanisms of SIC (region C) and SILC (region D) are the same, even though the amount of Ni concentration was not analyzed in this work. The difference in the amount of Ni silicide in region B, C, and D should not be significant based on the similarity of the colors in the images.

The XRD does not reflect any preferred orientation of laterally grown poly-Si since it is needle-like grains and narrow region which cannot be detected by X-ray spot. But, MILC and SILC is extension of MIC and SIC, respectively. Hence, orientation of laterally grown crystals can be analyzed from those of MIC and SIC poly-Si films.

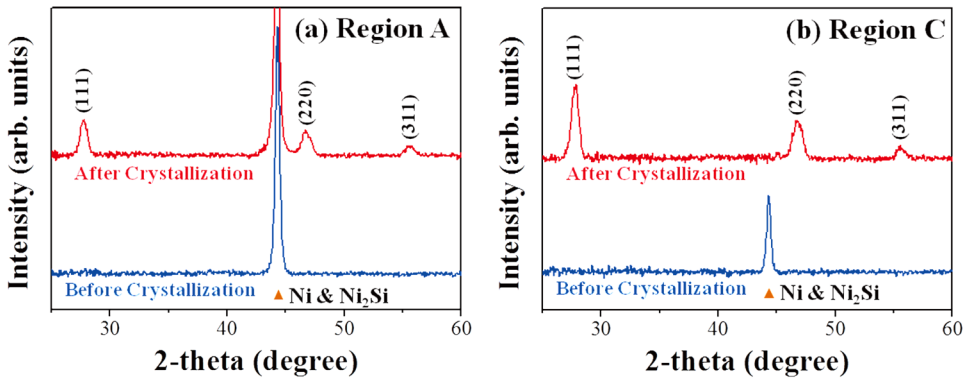


Figure 4.15 XRD spectra of the MIC and SIC poly-Si thin films before and after crystallization annealing at 550 °C for 4 h.

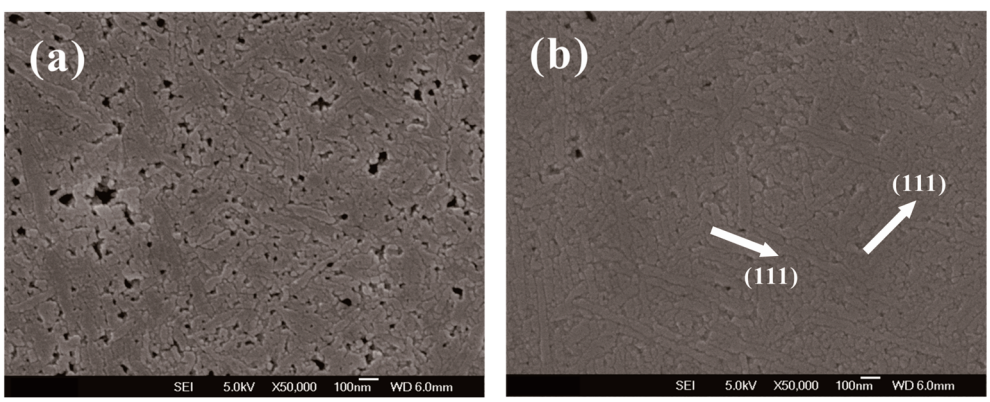


Figure 4.16 FESEM images of the laterally crystallized poly-Si by (a) conventional MILC (region B) and (b) SILC (region D).

Figure 4.15 shows the XRD spectra of the (a) MIC (Region A) and (b) SIC poly-Si (Region C) films before and after crystallization at 550 °C for 4 h. It can be noticed that the same crystalline Si peaks at d = 3.14 Å (111), d = 1.92 Å (220) and 1.64 Å (311) were measured from (a) MIC poly-Si (Region A) and (b) SIC poly-Si (Region B) after crystallization. But, each peaks intensities were increased by SIC method. It means that the texture of SILC poly-Si crystals is more constant than that of MILC

poly-SI crystals. It is confirmed by FESEM in the Figure 4.16. It can also be noticed that the Ni and Ni_2Si combined peak at 44.5° was presented in case of MIC poly-Si before and after crystallization, whilst the peak (at 44.5°) was eliminated after SIC as shown in Figure 4.15(b). It is interesting to note that the Ni silicide seeds were formed at Ni deposition and removal on top of a-Si surface, and then the seeds were acted as nuclei for crystallization.

To observe the surfaces of MILC and SILC poly-Si samples using FESEM, samples were Secco etched after crystallization annealing at 550°C for 4 h. It is known that Secco etchant can remove the a-Si and Ni silicide selectively [4.59]. In Figure 4.16, FESEM images of region B and D in Figure 4.14 are shown. It is obvious noticed that the MILC region contains more Ni silicides than the SILC region and the Ni silicides trapped at the grain boundaries make large holes after the Secco etch. The lateral growth occurs by the catalytic reaction of the Ni silicide, not by diffusion of Ni into the a-Si, so we cannot find Ni silicide inside the poly-Si grain. But lateral growth would stop when the catalyst comes across other poly-Si grain boundaries and the Ni silicide would be trapped at the grain boundaries, because there is no chemical potential difference - driving force for the phase transformation between the two poly-Si grains. [4.3] The presence of trapped Ni silicide in the channel region of the TFTs degrades the leakage current in MILC poly-Si TFTs [4.18, 4.22]. It can also be noticed that SILC exhibits longer grains than MILC because SILC starts with a lower concentration of Ni silicide at the lateral growth front than does MILC. It is well known that, as more short grains are utilized to make grain boundaries, the grain boundaries trap charged carriers and buildup potential barriers to the flow of carriers [4.27]. In light of this previous result, longer grains of SILC compared to those of MILC would yield better electrical performances.

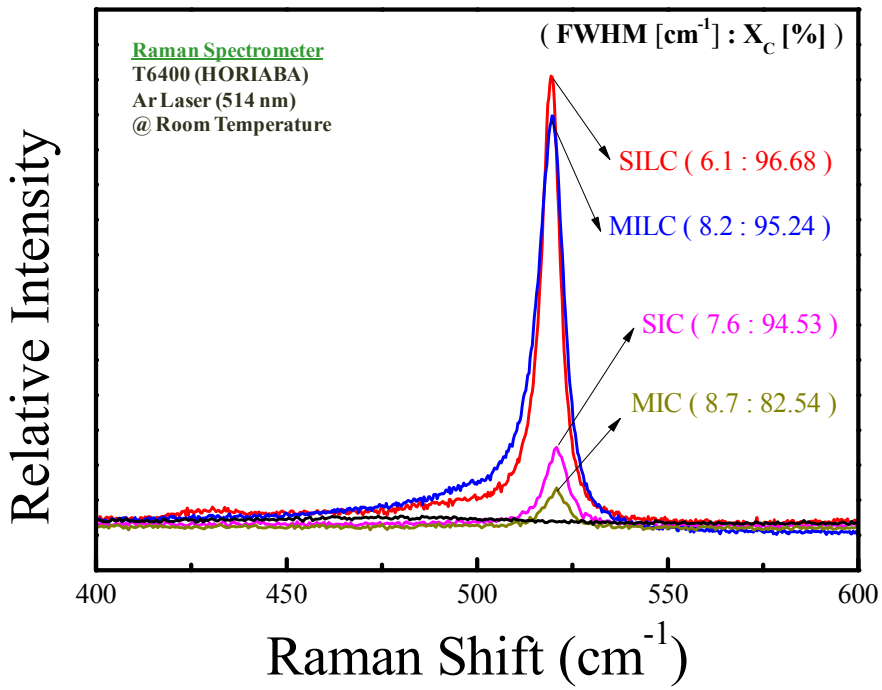


Figure 4.17 Raman spectra of a-Si film and poly-Si films crystallized by MIC (region A), MILC (region B), SIC (region C), SILC (region D) and a-Si (region E).

Figure 4.17 shows the Raman spectra of each regions of Figure 4.14. The spectrum of the a-Si showed a broad structure near 480 cm^{-1}, with a full-width-at-half-maximum (FWHM) of about 60 cm^{-1}. The spectra of the MILC and SILC poly-Si thin films each had a peak centered at 519.67 cm^{-1} and 519.38 cm^{-1} with FWHM values of 8.2 cm^{-1} and 6.1 cm^{-1}, respectively. Also, the MIC poly-Si thin film had a peak centered at 520.86 cm^{-1} with a FWHM value of 8.7 cm^{-1}, which was larger than the value of the peak centered at 520.52 cm^{-1} with a FWHM value of 7.6 cm^{-1} obtained from the SIC poly-Si thin film. The absence of the broad peak centered at 480 cm^{-1} for the MIC, SIC, MILC, and SILC thin films indicated that the a-Si thin film was fully crystallized by those crystallization methods after annealing at 550 °C for 4 h.

In order to better analyze this characteristic in the poly-Si thin films, we calculated the of the Raman spectra, which is defined as crystalline fraction (X_c) from the integral intensities follows [4.60]:

$$X_c = \frac{I_c}{I_c + \gamma I_a} \tag{4.1}$$

In this equation, I_a and I_c are the amorphous and crystalline integral intensities of the Raman spectra, respectively, and to take into account the different Raman scattering cross section of amorphous and crystalline phases, I_a is multiplied by a correction factor γ. In this study, the value 0.8 was utilized for γ [4.61].

$$I_c = I_{520}$$
$$I_a = I_{480}$$
$$\gamma = 0.8$$

As shown in Figure 4.17, the crystalline fraction of SILC (96.69%) is higher than that of MILC (95.24%); while, the SIC and MIC regions exhibit lower percentages of crystalline fraction (94.53% and 82.54, respectively) than those of SILC or MILC. Notably, the MIC region has the lowest crystalline fraction among those regions, which turned out to contain much of the Ni silicides as defects. This result was confirmed from the results of the FWHM comparisons.

A smaller FWHM value means a better poly-Si quality. SILC turns out to be the best among these poly-Si. This might indicate that SILC has the largest grain size with the fewest grain boundaries. This FWHM is also related to the concentration of Ni

silicide trapped at the grain boundaries so that it can be concluded that SILC shows the lowest defect concentration among these poly-Si films [4.62].

Raman spectroscopy is a technique that can be applied in stress characterization. This method is currently recognized as a powerful tool in identifying stress and strain in poly-Si [4.62]. The magnitude of the residual stress was estimated based on the in-plane stress model. In particular, we used the following (3) that was described by Pillard *et al.* [4.63]:

$$\sigma\,[MPa] = -250\Delta\omega\,[cm^{-1}] \tag{4.2}$$

where $\Delta\omega$ is the wave number shift calculated from (ω_s - ω_0), ω_0 is the wave number of stress-free single crystalline Si (520 cm^{-1}), and ω is the wave number of the film under measurement conditions. As we can see in this expression, the magnitude of the wave number shift of Si from the 520 cm^{-1} peak is related to the magnitude of residual stress of the poly-Si thin film.

The residual stresses of the poly-Si thin films crystallized by MIC, SIC, MILC, and SILC were calculated using equation (4.2). The wave number shifts ($\Delta\omega$) of 0.86, 0.52, -0.33, and -0.62 cm^{-1}, when utilized in the equation, lead to stresses of - 447.2, -270.4, 171.6, and 322.4 MPa for MIC, SIC, MILC, and SILC, respectively. This result clearly shows that the laterally crystallized poly-Si thin films, such as MILC and SILC, have tensile stresses, and vertically crystallized poly-Si thin films, such as MIC and SIC, have compressive stresses; this is because, in the tensile stress case of lateral crystallization, the lattice parameters were lowered by reducing the Ni silicide concentration in the poly-Si thin film; while, the compressive stresses of vertical crystallization, as with MIC and SIC, contain relatively high concentrations of Ni

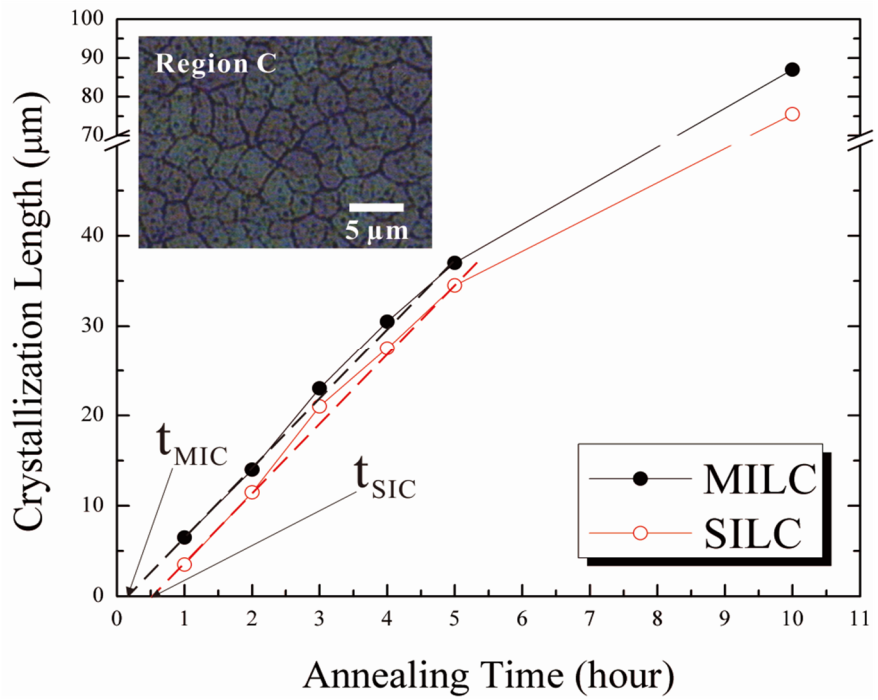


Figure 4.18 Comparison of conventional MILC and SILC growth lengths as a function of annealing time from 1 to 10 h. Crystallization temperature was fixed at 550 °C.

silicide. As a result, an enlargement of the lattice parameter above the standard value of Si (5.43 Å) occurred. For the same reason, we can recognize that the residual stresses of SILC and MIC have higher tensile and compressive stresses than those of MILC and SIC, respectively.

The lateral crystallization rates of MILC and SILC are compared in Figure 4.18. Since there is a continuous Ni film in case of MILC, its rate is only attributed to lateral growth; while, in the case of SILC, the Ni silicide has to propagate along random orientations at the beginning from the silicide seeds. From the extrapolation of the MILC plot, we can obtain an incubation time for lateral growth, t_{MIC}, of about 8 min at 550 °C. This incubation time should include the time needed for the sample to reach

550°C in our tube furnace. t_{SIC} was similarly determined to be about 29 min. By subtracting t_{MIC} from t_{SIC}, we can get the time needed for crystallization at random orientations at the beginning of a phase transformation and it turns out to be about 21 min. The lateral growth rate at this temperature was about 6.5 μm/h, so the spacing between the seeds of the Ni silicide phase in region C in Figure 4.14 can be deduced to be about 4.5 μm, considering the random locations of the seeds on the surface. It turned out that the grain size of the SIC area was observed to be about 5 μm, as shown in Figure 4.18, which is close to the value calculated in this work.

In Figure 4.19, The I_D-V_G transfer curves of MILC and SILC poly-Si TFTs are compared. It is obvious that the SILC TFT shows a lower leakage current than the MILC TFT. It is thought that the lower amount of Ni silicide contained in the channel of the poly-Si TFT fabricated by SILC compared to that of MILC should be responsible for the low leakage current. The shift in the threshold voltage is quite noticeable and it is known that the Ni concentration in the channel is mainly responsible for that shift [4.63]. Important parameters obtained from the I_D-V_G transfer curves of MILC and SILC TFTs are listed in Table 4.3. 20 transistors (W/L = 10 μm /10 μm) were selected per sample to confirm the uniformity and the samples were fabricated 10 times for repeatability. The electrical properties were calculated for average values. The determinations of key parameters are explained in chapter 2.4.

It should be noticed that the electrical properties were improved by the SILC method, especially the off-state leakage current, field effect mobility, and threshold voltage. The minimum leakage current, which was defined as the minimum current along the gate voltage, was drastically decreased from 1.0×10^{-10} to 3.4×10^{-11} A by SILC at V_D = - 5 V, while, the field effect mobility was improved from 54 to 66 cm^2/Vs in the linear regime at V_D = - 0.1 V. However, the on-current was almost the

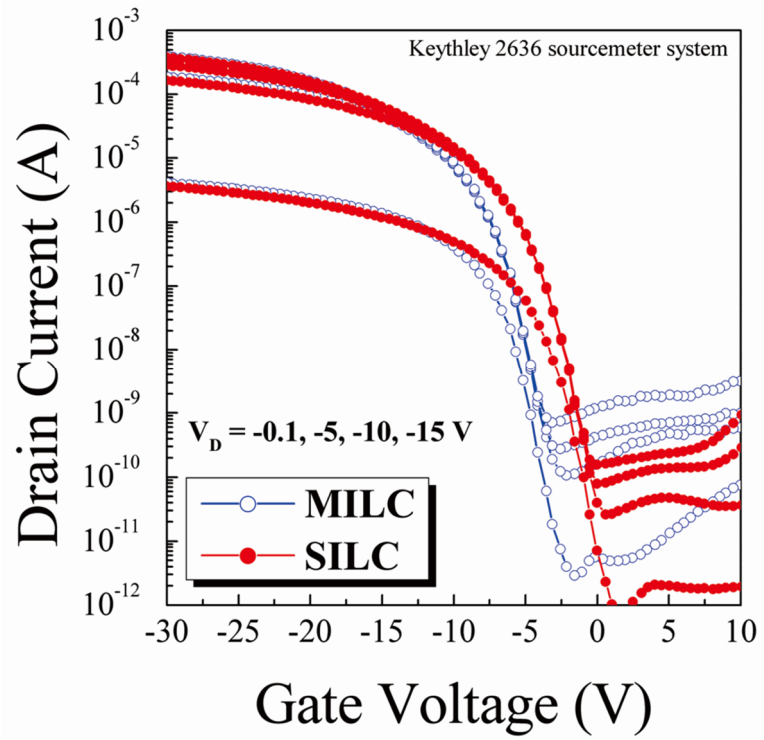


Figure 4.19 I_D-V_G characteristics of the poly-Si TFTs (Width / Length = 10 / 10 μm) fabricated by MILC and SILC. The poly-Si TFTs were measured at V_D = -0.1, -5, -10, -15 V respectively.

Table 4.3 Device key parameters of the MILC and SILC poly-Si TFTs.

Parameter		MILC	SILC
V_{th} (V)		-7.5 ± 0.3	-5.5 ± 0.3
Mobility (cm^2/V-s)		54 ± 3	66 ± 2
Subthreshold Slope (V/dec)		0.9 ± 0.05	0.85 ± 0.05
V_D = -5 V	I_{ON} (× 10^{-4} A)	1.8 ± 0.4	1.7 ± 0.3
	I_{OFF} (× 10^{-11} A)	10 ± 1.8	3.4 ± 1.6
	ON/OFF ratio (× 10^6)	1.8	5.0
V_D = -10 V	I_{ON} (× 10^{-4} A)	3.1 ± 0.4	3.0 ± 0.5
	I_{OFF} (× 10^{-11} A)	27 ± 1.3	7.9 ± 1.2
	ON/OFF ratio (× 10^6)	1.12	3.79

same. Therefore, the on/off ratio of the SILC TFT was larger than that of the MILC TFT. A reduction of the threshold voltage occurred in the SILC TFTs due to the low Ni silicide contamination compared with the MILC TFTs. The leakage current improvement was attributed to the reduction of the Ni concentration in the poly-Si films. Ni residues in the poly-Si thin films served as deep-level trap states, which promoted a thermionic emission that dominated the leakage current in the low gate and high drain voltage regime [4.64]. It is well known that there are three major defects related to the performance of Ni-induced crystallized TFTs: (1) Ni concentration (Ni-related defects), (2) grain boundaries, and (3) channel damage. [4.65]. It is thought that MILC poly-Si has many trap states, as compared to SILC poly-Si; this is because MILC poly-Si has a higher Ni silicide concentration than SILC poly-Si as shown above in Figure 4.16. Grain boundaries and trap states take charged carriers and buildup potential barriers allowing the flow of carriers. The presence of the potential barriers and the additional scattering at the grain boundaries lead to field effect mobility degradation. The high density of the trap states increases the subthreshold slope, the threshold voltage, and the off-state leakage current.

Figure 4.20 shows the dependence of the minimum leakage current and on-current on the V_D. It can be noticed that the leakage current is more sensitive to the drain voltage in the MILC TFT than in the SILC TFT, while there is no significant difference in the on-current behavior between these two TFTs. It is known that the increase of the V_D gives rise to the increase of the leakage current and the sensitivity is related to the trap states, such as trapped Ni silicide in the grain boundaries [4.18]. Hence, this proves the SILC TFT has fewer defects in the channel than the MILC TFT.

The grain boundary trap state density (N_t) was determined using a Levinson plot, which can estimate the N_t from the slope of a linear regime of $\ln(I_D/V_G)$ vs. $1/V_G$ at low

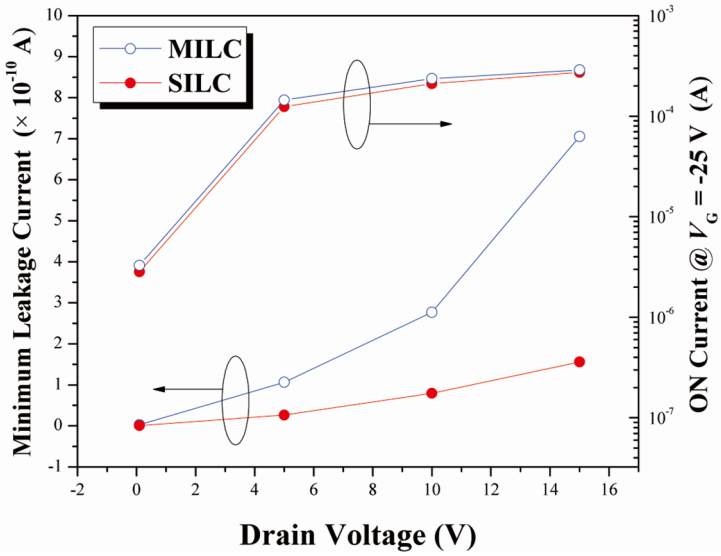


Figure 4.20 Comparison of the minimum leakage current and on state current between MILC and SILC poly-Si TFTs. The drain voltages was varied from -0.1 to 15 V.

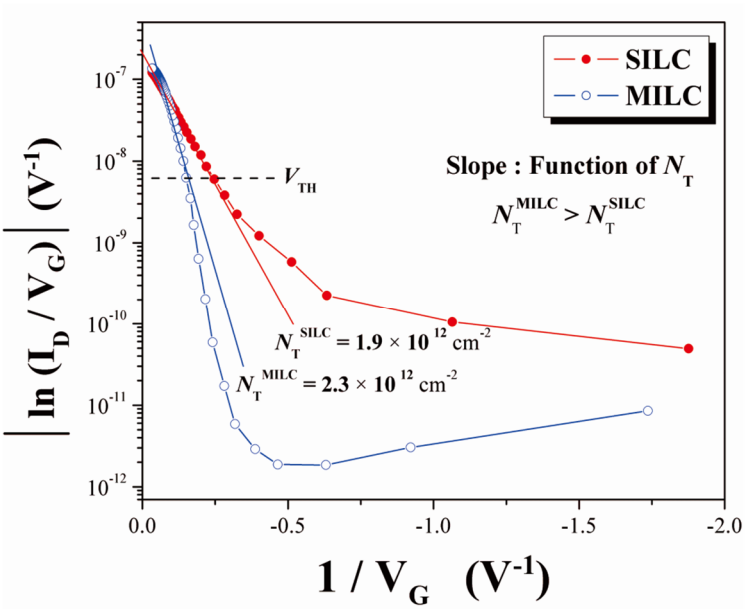


Figure 4.21 Levinson plot of $\ln(I_D/V_G)$ vs. $(1/V_G)$ for MILC and SILC poly-Si TFTs. I_D measured at V_D = -0.1 V.

V_D (= -0.1 V) and high V_G (over threshold voltage) values. The plots were given by Equation (2-17). [4.28]

As shown in Figure 4-21, the *Nt* of the SILC TFT was 1.9×10^{12} cm^{-2}, which was much lower than that of the MILC TFT (2.3×10^{12} cm^{-2}). As we mentioned before, the N_t, which is the dominant leakage source and results from Ni silicide trapped at grain boundaries, is drastically reduced by the SILC process and the comparison of SILC with MILC is consistent with their electrical performances.

4.2.2.2 Self-Aligned SILC Poly-Si TFTs

The I_D-V_G transfer curves of the poly-Si TFTs fabricated by SA-MILC and SA-MILC methods were compared in Figure 4.22, and the measured as well as extracted device parameters are summarized in Table 4.4. The 10 TFTs were measured. The SA-SILC poly-Si TFT was found to show better electrical properties than that of SA-MILC poly-Si TFT. As shown in Table. 4.4, the field-effect mobility of SA-SILC poly-Si TFT is 67 $cm^2/V{\cdot}s$, which is much higher than that of SA-MILC poly-Si TFT. The threshold voltage, subthreshold slope, on-state current, and off-state leakage current were also improved by SA-SILC.

It is well known that when an MIC/MILC boundary that is highly defective, containing both a continuous grain boundary and a high concentration of Ni, coincides with any of the metallurgical junctions, it becomes part of the channel. The high density of the grain boundary trap state effectively raises the local, hence also the overall, threshold voltage and subthreshold slope of the device. Only by removing the

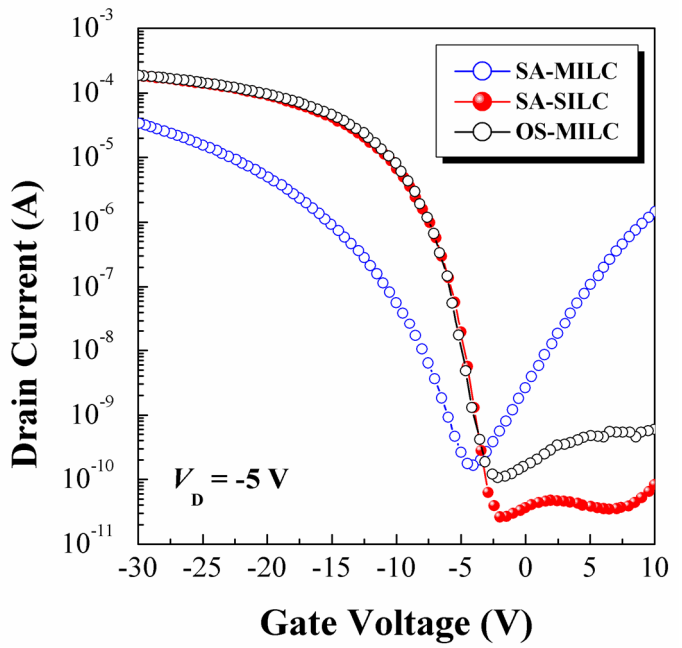


Figure 4.22 I_D-V_G transfer curves of the poly-Si TFTs (width / Length = 10 μm / 10 μm) fabricated by SA-MILC and SA-SILC. Conventional OS-MILC poly-Si TFT was referred.

Table 4.4 Device key parameters of the SA-MILC and SA-SILC poly-Si TFTs

Key Parameters	SA-MILC	SA-SILC	OS-MILC
Field-effect mobility (cm^2/V-s)	17 ± 3.0	67 ± 3.5	66 ± 3.0
Threshold voltage (V)	11 ± 2.1	6 ± 0.8	7.5 ± 1.0
Subthreshold slope (V/dec)	1.6 ± 0.2	0.8 ± 0.2	0.9 ± 0.2
Minimum leakage current ($\times 10^{-11}$ A)	17 ± 3.2	2.6 ± 2.5	10 ± 2.6
Leakage current ($\times 10^{-11}$ A) @ V_G = 5 V	265 ± 34	3.8 ± 1.2	47 ± 5.0
Maximum on current ($\times 10^{-4}$ A)	0.2 ± 0.1	1.8 ± 0.3	1.8 ± 0.3
Maximum on/off ratio ($\times 10^6$)	0.8	7.0	1.8

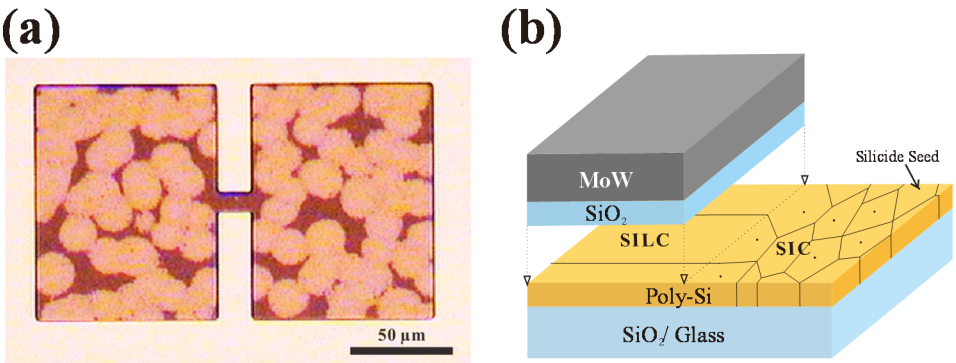


Figure 4.23 Optical microscope image and schematic diagram of SILC (a) Optical microscope image after crystallization annealing at 550 °C for 30 min (b) Schematic diagram for SILC. The gate was lifted to reveal the channel area crystallized by SILC.

MIC/MILC boundary from both junctions can the threshold voltage and subthreshold slope effectively be reduced [4.12, 4.18].

In addition, it presents an interesting result in off-state leakage current. The off-state leakage current at V_G = 5 V and V_D = -5 V was decreased from 4.7 × 10^{-10} A to 3.8 × 10^{-11} A. The reason is that the SILC lowered trap states than continuous Ni film (MILC), as it is known that the major mechanism of the high off-state leakage current is the field emission via trap states due to the high electrical field in the drain depletion region [4.1, 4.2]. Consequently, the leakage current is drastically reduced.

In this study, the MIC/MILC boundary was effectively removed by silicide seed catalyst, as is clearly shown in Figure 4.23. The Figure 4.23(a) shows an optical microscope image after crystallization annealing at 550 °C for 30 min. The a-Si where Ni was deposited and removed was crystallized at first from a dot of silicide seed and grew gradually. Finally, the SIC region was fully crystallized and lateral growth took place. The crystallization proceeds from the dot of silicide seed and, then, eventually meets neighboring crystallites and forms grain boundary. These results show that the

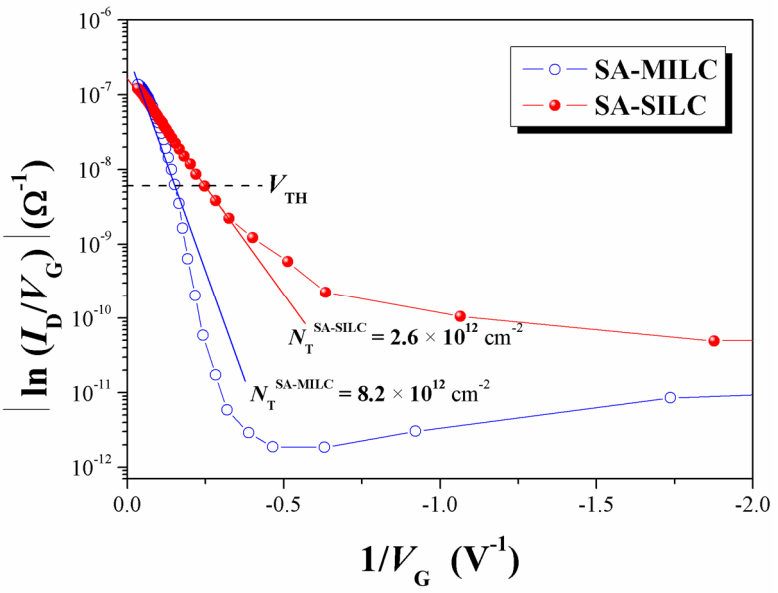


Figure 4.24 Levinson plot of ln (I_D / V_G) vs. (1 / V_G) for MILC and SILC poly-Si TFTs. I_D measured at V_D = -0.1 V.

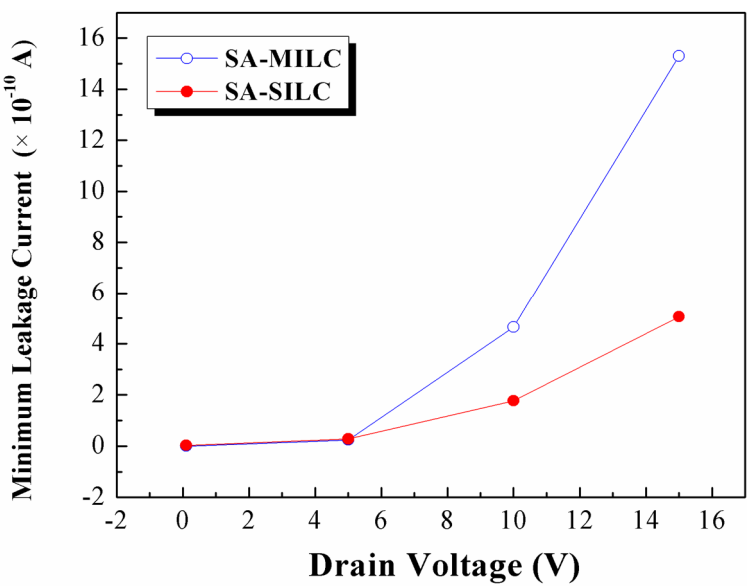


Figure 4.25 Comparison of the minimum leakage current between SA-MILC and SA-SILC poly-Si TFTs. The drain voltages was varied from -0.1 to -15 V.

crystallization that occurred by silicide seed is distinctly different from that by continuous Ni film. Therefore, source and drain depletion regions were located inside of the laterally crystallized poly-Si from silicide seeds, as shown in Figure 4.23(b).

It has been reported that poly-Si has many trap states in grain boundaries and these states take charge carriers and build up potential barriers, allowing the flow of carriers. The presence of the potential barriers and the additional scattering at the grain boundaries lead to field effect mobility degradation. The high density of the trap state increases the threshold voltage, subthreshold slope, and off-state leakage current. The trap state density (N_t) was measured using a Levinson plot, which can estimate the N_t from the slope of the linear regime of ln (I_D/V_G) vs. $1/V_G$ at low $V_{D\,(=0.1\,V)}$ and high V_G. The plots were given by Equation (2-17).

As shown in Figure 4.24, the N_t of SA-MILC poly-Si TFT is 8.2×10^{12} cm^{-2}, which is larger than that of SA-SILC poly-Si TFT. The reduction in the N_t values implies that those defects have been effectively terminated by silicide seed.

In the MILC poly-Si, there are two major kinds of defects related to trap states: (*i*) grain boundary defects and (*ii*) Ni-related defects. These defects degrade electrical performance because they introduce dangling and strain bonds [4.65, 4.66, 4.67]. The SA-SILC method can reduce those defects by less grain boundary and Ni contamination through silicide seed catalyst.

Figure 4.25 shows the variation of the minimum leakage currents with an increase in the drain voltages in SA-MILC and SA-SILC poly-Si TFTs. The minimum leakage current of the SA-MILC poly-Si TFT was as low as that of SA-SILC poly-Si TFT at $|V_D| \leq 5V$, while the minimum leakage current of the SA-MILC poly-Si TFT became higher than that of SA-SILC poly-Si TFT with the increase of drain voltages. Generally, it has been reported that the leakage at high drain voltage is dominated by

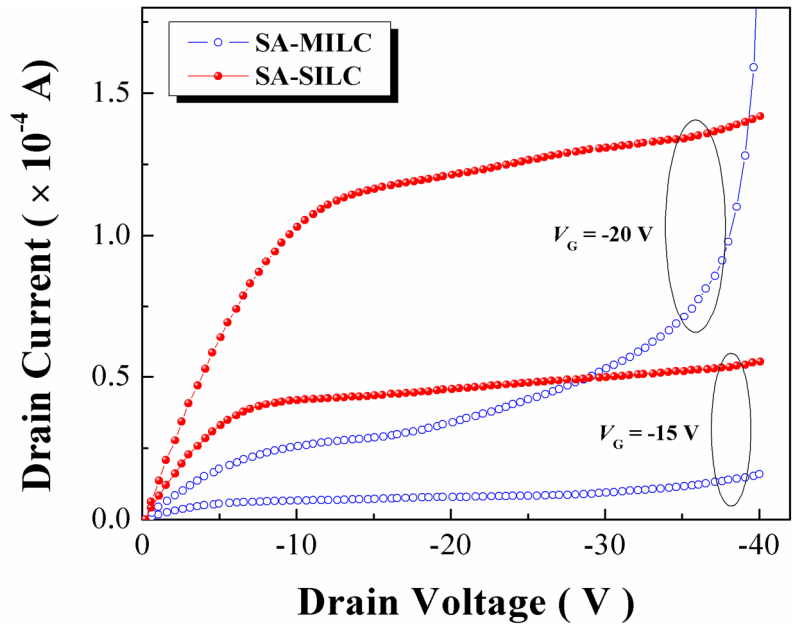


Figure 4.26 Comparison of I_D-V_D output characteristics of SA-MILC and SA-SILC poly-Si TFTs.

trap-assisted field-emission current; the combination of the high electric field in the junction and high trap states density in the overlapping MIC/MILC boundary will result in significantly higher leakage current when compared to the case with the defective MIC/MILC boundary effectively removed from the junctions [4.13].

Figure 4.26 shows the I_D-V_D output characteristics of SA-MILC and SA-SILC poly-Si TFTs. It is important to note that SA-SILC exhibits kink-free I_D-V_D characteristics. This due to the fact that when the MIC/MILC boundary overlaps the drain junction, either the drain electric field or the impact ionization rate is enhanced due to the presence of charged defect states, such as the grain boundary traps or the Ni contaminations, in the MIC/MILC boundary [4.11].

4.2.3 Analysis of Improved Electrical Performance by SILC

The leakage current mechanisms of MILC TFTs is well established in the previous studies [4.1, 4.2]. According to the studies, the leakage current is produced by two mechanisms as shown in Figure 4.27. Two separated leakage current regions are appeared in the off-state region. Region A is first mechanism of leakage current which is thermionic emission due to thermal excitation of trapped carriers at relatively low gate voltages and high drain voltages. This leakage current mechanism is manifested by the "bump" and "minimum leakage current" in the I_D-V_G transfer curves. Region B is second mechanism of leakage current which is field emission due to field ionization of trapped carriers tunneling through the potential barrier and field-enhanced thermal excitation of trapped carriers at high reverse gate voltages. This leakage current mechanism is manifested by the "pinning" in the I_D-V_G transfer curves. The pinning means the increase of drain current that occurs with increasing gate voltage. The "pinning current" is defined as the maximum drain current in the high gate voltage region. The height of the bump and minimum leakage current in region A is related to the defects in the surface of the channel, and the pinning current is related to the amount of defects at the channel and drain junction, where the highest electric field is applied during the measurement. If the defect concentration in the channel and electric field are minimized, then the bump and pinning are eliminated and region A remains flat. [4.21]

Figure 4.28 shows the comparison of the I_D-V_G transfer curves of SIC, SA-SILC and OS-SILC poly-Si TFTs. It was surprising that SIC and SA-SILC did not show much difference in I_D-V_G transfer curves. However, threshold voltage was lower by about 2.5 V in OS-SILC as compared to the other two. The on-state current was

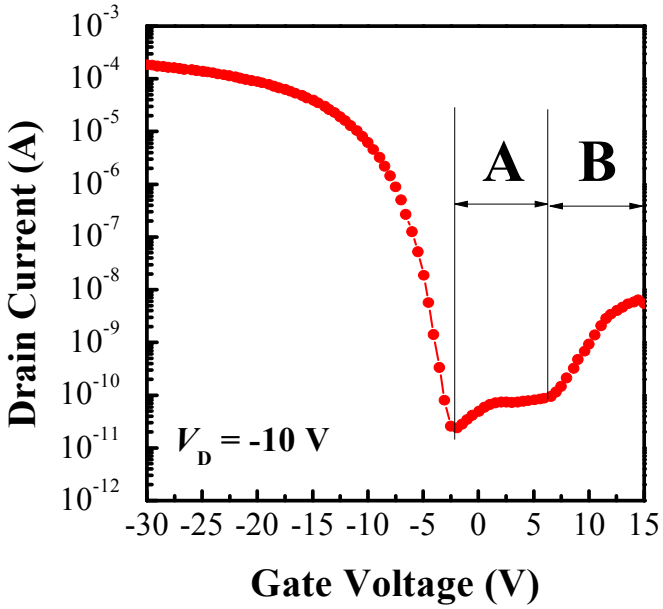


Figure 4.27 Typical I_D-V_G transfer curves of conventional MILC poly-Si TFT.

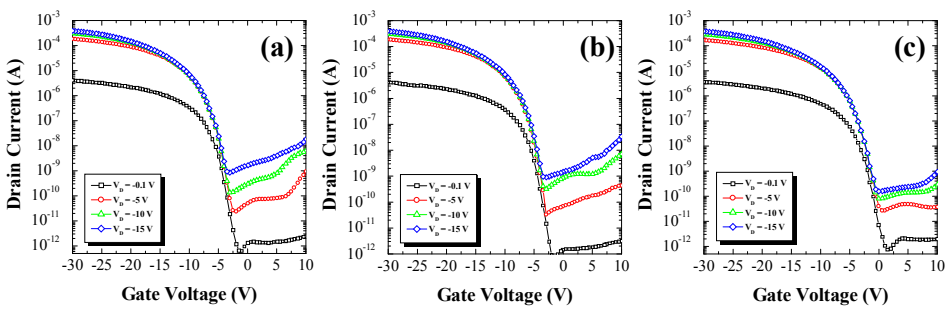


Figure 4.28 Comparison of I_D-V_G transfer curves of (a) SIC, (b) SA-SILC, and (c) OS-SILC.

almost the same for each group. The on-state current is not affected by Ni silicide defect concentration, compared with the leakage current, which is much more dependent on the concentration of Ni silicide defects. As for the behavior of the leakage current, SIC showed a bump and a low pinning current. On the other hand,

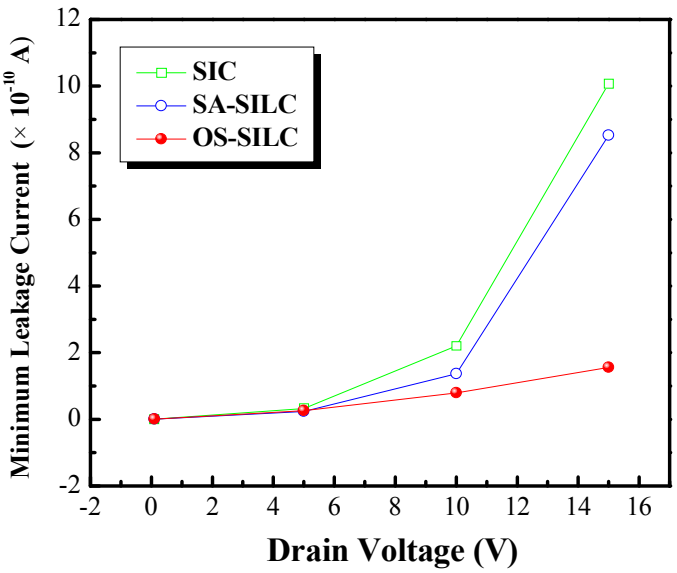


Figure 4.29 Dependence of the minimum leakage current of SIC, SA-SILC and, OS-SILC as increasing of drain voltage.

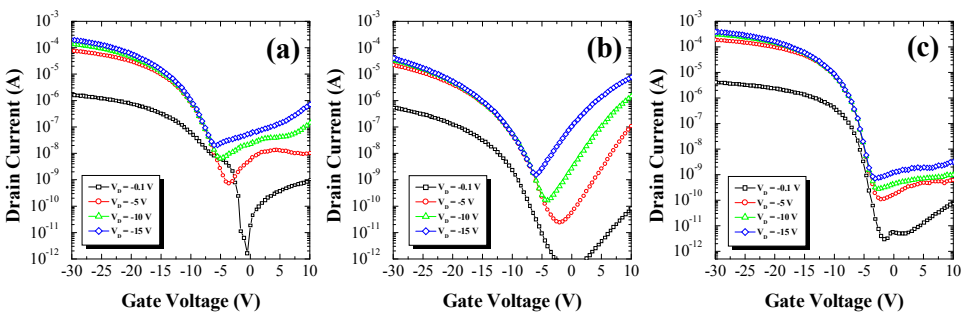


Figure 4.30 Comparison of I_D-V_G transfer curves of (a) MIC, (b) SA-MILC, and (c) OS-MILC.

SA-SILC showed no bump, but the pinning current was relatively high. The minimum leakage current for each was about the same at $V_D < -5$ V; but at $V_D > -5$ V, OS-SILC showed the lowest minimum leakage current. The minimum leakage current increased more rapidly in SA-SILC and SIC than in OS-SILC, as shown in Figure 4.29 It means

that the trapped carriers are minimized by OS-SILC. The OS-SILC showed a flat region A, and no pinning was observed in the Figure 4.28. Similar I_D-V_G characteristics for SIC and SA-SILC indicate that, even for the blanket deposition of Ni, the seed cannot be formed continuously on the surface of a-Si because of which, in practice, the lateral growth occurs during crystallization, even in the case of SIC. However, because there was a bump in region A in the case of SIC, and there was no bump in SA-SILC, there was a slight difference in the amount of trapped Ni silicide between these two groups. Less trapping of Ni silicide at the grain boundaries in the channel was expected in OS-SILC than in SIC or SA-SILC; this was confirmed by the lower threshold voltage observed in this group than in the other two. Since the pinning phenomenon is related to the amount of Ni silicide traps between channel and drain junction, it was not seen in OS-SILC.

Figure 4.30 shows the comparison of the I_D-V_G transfer curves of MIC, SA-MILC and OS-MILC poly-Si TFTs. The on-state current was the lowest in SA-MILC and the highest in OS-MILC, regardless of drain voltage. The leakage current level in MIC was more than two orders of magnitude higher than that of OS-MILC, indicating that there were far too many Ni silicide traps. In case of SA-MILC, the pinning phenomenon was so outstanding that the bump in region A was hidden under the rapid increase of the leakage current with gate voltage. Therefore, we determined that MIC and SA-MILC cannot be applied to AMOLED because the leakage current is too high. On the other hand, for OS-MILC, the on-state current of 10^{-4} A, the subthreshold slope of less than 1 V/dec, the mobility of 20–40 cm^2/Vs, and the on/off ratio of more than 10^6 are all quite acceptable for AMOLED; however, the leakage current near 10^{-10} A could still be a problem. The electrical parameters of MIC and SIC groups calculated from the I_D-V_G transfer curves are listed in Table 4.5.

Table 4.5 Device key parameters of the MIC, SA-MILC, OS-MILC, SIC, SA-SILC, and OS-SILC poly-Si TFTs.

Key Parameters	MIC	SA-MILC	OS-MILC	SIC	SA-SILC	OS-SILC
Field-effect mobility μ_{FE} (cm^2/V-s)	29.8	17.5	66.3	63.3	63.4	63.2
Threshold voltage V_{TH} (V)	10	9	7.5	7.5	7.4	5.5
Subthreshold slope *S. S.* (V/dec)	1.5	1.6	0.9	0.7	0.8	0.8
Drain current @ $V_G = 0$ V I_D ($\times 0^{-10}$ A)	220	26	4.1	8.6	3.0	0.8
Maximum on-current I_{on} ($\times 0^{-4}$ A)	1.4	0.3	2.7	3.0	3.1	2.8
Minimum leakage current I_{Leak} ($\times 0^{-10}$ A)	69	1.6	2.7	1.3	3.2	0.8
Pinning current @ $V_G = 15$ V $I_{Pinning}$ ($\times 0^{-8}$ A)	215	753	0.70	6.89	8.80	0.78

From this, we can see relatively low mobility in the case of MIC and SA-MILC due to high concentration of trapped Ni silicides. Other than these two cases, more than 60 cm^2/V-sec can be obtained for the electrical mobility. As the concentration of Ni silicides got smaller, threshold voltage became lower. It is obvious from this table that MIC contained the highest concentration of trapped Ni silicides at the channel and OS-SILC contained the lowest, as was expected. The on-state current has little influence on the concentration of Ni silicides, and the pinning current can be reduced by offsetting the Ni deposition from the gate edge. It was surprising to notice that SIC poly-Si TFT shows low pinning current without offsetting, which was different from MIC and SA-MILC poly-Si TFTs. This strongly suggests that the seed did not form continuously on a-Si thin film in SIC, and that the lateral growth was the predominant mechanism, even at the area where Ni was once deposited before the heat-treatment. Since the electrical parameters of SIC poly-Si TFT are quite acceptable, if not better than OS-SILC poly-Si TFT, it shows great promise in terms of mass production capabilities. This suggests that no extra mask step is necessary for mass production, which could make a big difference in the industry.

In Figure 4.31, I_D-V_G transfer curves of SA-MILC and SA-SILC poly-Si TFTs are compared. SA-MILC showed higher leakage current and lower on-state current than

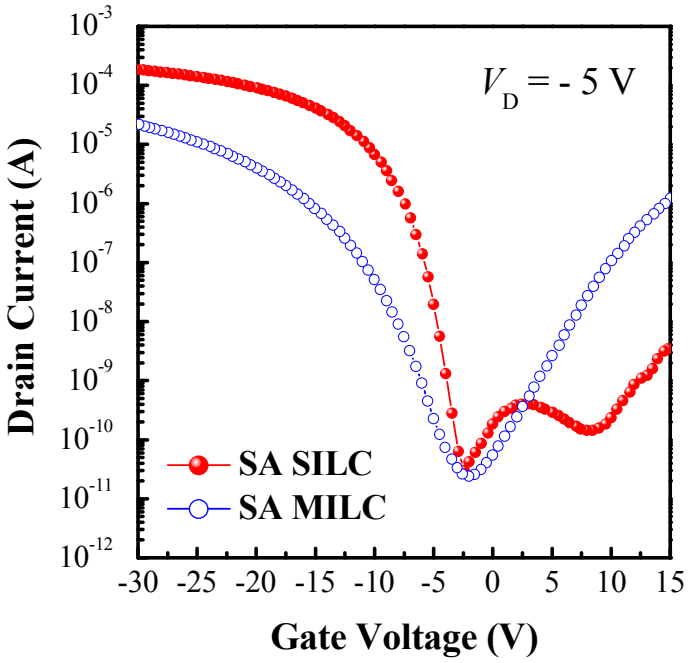


Figure 4.31 I_D-V_G transfer curves of (a) SA-SILC, and (b) SA-MILC at V_D = -5 V.

SA-SILC in the case of self-aligned Ni deposition. The pinning phenomenon was more outstanding in SAMILC due to relatively larger number of Ni silicide traps between channel and drain junction [4.11], and it roles as potential barrier to flow of carriers. the SA-SILC was expected to also contain a large number of Ni silicide traps because it was also a self-aligned process; however, the Ni was removed immediately after the deposition, thus the number of Ni silicide traps between channel and drain junction should be far fewer than SA-MILC. In the case of SA-SILC, we did observe the bump in region A, which is an indication that the Ni silicide traps in the channel were much smaller than SA-MILC. We have not yet identified the nature of the seed that was formed, but we are currently investigating what happened after Ni sputtering on a-Si at room temperature. The slope, which is directly related to the switching

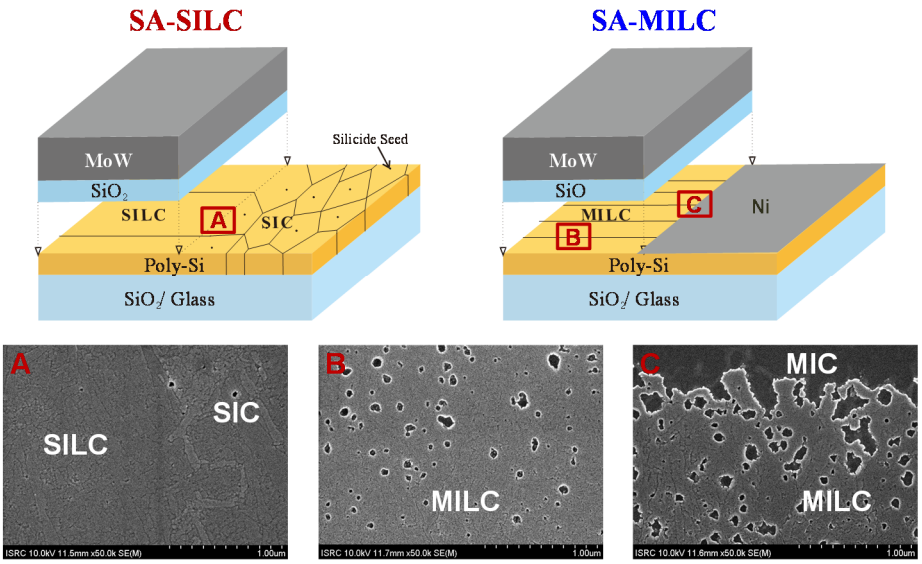


Figure 4.32 Schematic diagrams of crystallization mechanism of (a) SA-SILC and (b) SA-MILC. The gate was lifted to reveal the channel area crystallized by SILC and MILC.

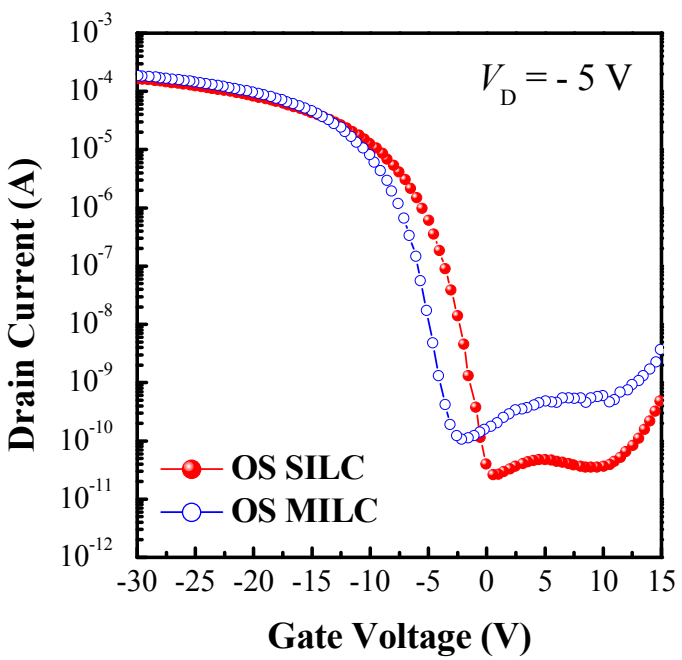


Figure 4.33 I_D-V_G transfer curves of (a) OS-SILC, and (b) OS-MILC at V_D = -5 V.

characteristic of the pixel, was much worse in the case of SA-MILC than in SA-SILC. In this self-align process, since the gate was used as a mask for Ni deposition, Ni silicide must have been intensively trapped at both ends of the channel. If that was the case, SA-MILC should have been much worse than SA-SILC because Ni was not removed before crystallization, and the new Ni silicide fragments could be formed continuously during heat-treatment as shown in Figure 4.32.

For the off-set process, SILC and MILC are compared in Figure 4.33. OS-SILC showed lower leakage current than OS-MILC, but there was no difference in the on-state current. Reduction in threshold voltage by about 2.5 V was observed in OS-SILC as compared with OS-MILC. This could have been due to the difference in the amount of trapped Ni silicides between the two. The pinning current was almost the same, which might indicate that trapping of Ni silicide proceeds to a certain extent even though supply of Ni is stopped during the heat-treatment.

4.3 Gettering

poly-Si TFTs, which afford devices with high field effect mobility, is being extensively studied as a key device to realize FPDs with integrated peripheral circuits. Moreover, the crystallization temperature lowering allows the use of low-cost glass and flexible substrates.

The most popular low-temperature crystallization methods are MIC and MILC [4.9], [4.19]. Compared with other techniques, these methods have many advantages, including a low-cost batch process, smooth device surfaces. Compared with other processes, however, relatively higher leakage current is a drawback due to the metal

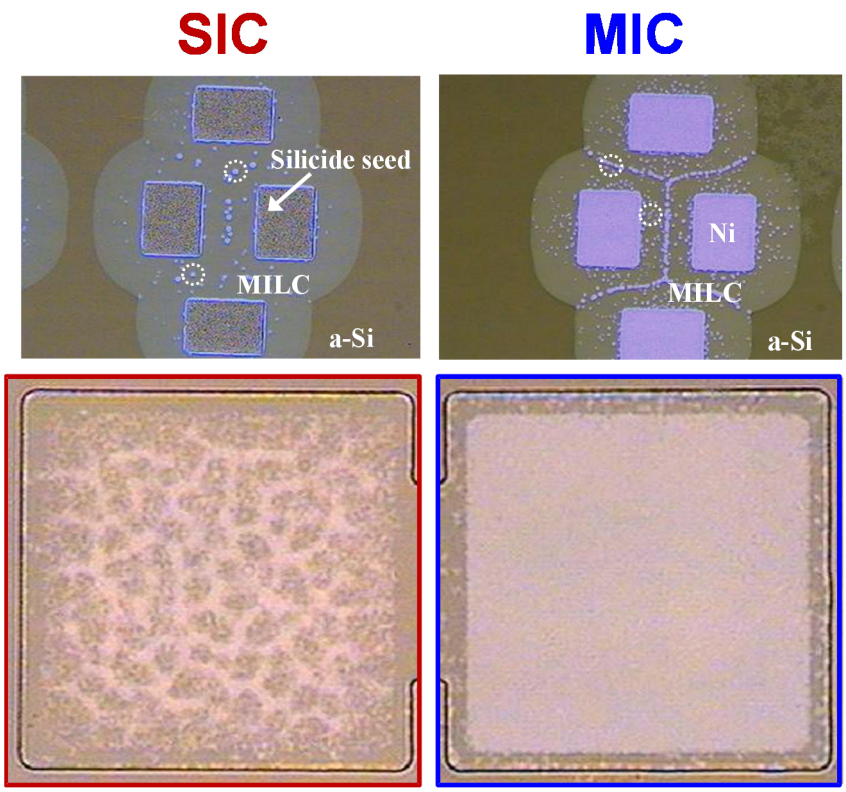


Figure 4.34 Optical microscope images of partially crystallized 2nd Si layer on the (a) metal-induced laterally crystallized and (b) silicide-induced laterally crystallized poly-Si thin films [4.59]. ; Amount of bright dots were concentrated to the MILC region as well as the MILC/MILC boundary. But, only a few bright dots exist only at the SILC/SILC boundary, and few bright dots exist in the SILC region. Therefore, it was revealed that captured Ni silicides could be reduced by silicide seed.

catalyst, which is often Ni: Ni-related centers or complexes within the channel form many levels within the band gap [4.6]. In order to reduce the contamination of Ni catalyst and to enhance the electrical performance, several crystallization methods have been utilized, such as Ni offset MILC [4.11, 4.12], MIC through SiN_x capping layer [4.13], metal-induced unilateral crystallization [4.55], and Ni silicide seed-induced lateral crystallization [4.15-4.17]. However, these processes are complicated

and required high process temperatures and long annealing times, which can damage the poly-Si active layer. In our earlier report, a new crystallization method was presented, that is SIC using Ni-silicide seed which formed by Ni sputtering. But, the leakage current near 10^{-10} A could still be a problem [4.15].

In this work, a new a-Si layer was formed on top of the poly-Si which is already crystallized by MIC and SIC. And then heat treatment was carried out to getter the Ni silicides trapped at the surface of the active layer. The Ni silicides trapped at the surface of the active layer would move toward a new a-Si layer (2^{nd} a-Si) during the heat treatment. Crystallization of the 2^{nd} a-Si layer by catalytic phase transformation of the Ni silicide trapped at the grain boundaries of the active thin film is shown in Figure 4.34. It can be seen that the 2^{nd} a-Si layer only on top of the trapped Ni silicides is crystallized during the deposition of the 2^{nd} a-Si in LPCVD. After the heat treatment, the partially crystallized 2^{nd} Si layer was removed to get the Ni silicide free surface. And then, the electrical properties of thus prepared TFTs were analyzed. Considerable improvement in the electrical performance was observed to prove that the method developed in this work is very effective. The electrical properties of the gettered TFT are suitable for AMOLED display.

4.3.1 Gettered MIC and SIC Poly-Si TFTs

In Figure 4.35, I_D-V_G transfer characteristics of MIC TFT and gettered MIC (GMIC) TFT are compared. It is obvious that the electrical properties of the gettered TFT are much better than non-gettered TFT. The leakage current gets lower. On-state current, however, does not change much with the gettering process. Especially, the

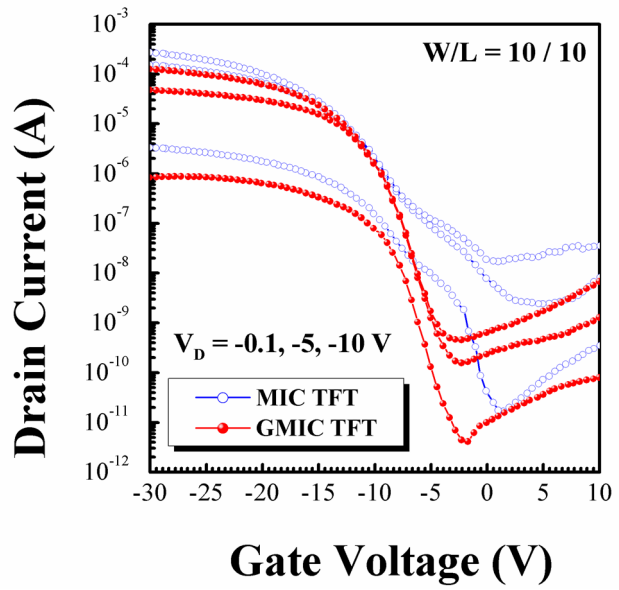


Figure 4.35 Typical I_D-V_G transfer curves of poly-Si TFTs (width / length = 10 μm / 10 μm) fabricated by MIC and GMIC.

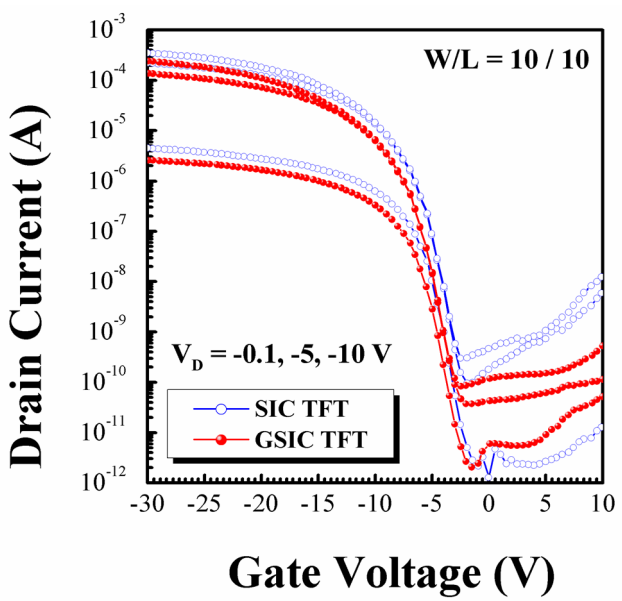


Figure 4.36 Typical I_D-V_G transfer curves of poly-Si TFTs (width / length = 10 μm / 10 μm) fabricated by SIC and GSIC.

Table 4.6 Device key parameters of MIC, GMIC, SIC, and GSIC poly-Si TFTs

Key Parameters	MIC	GMIC	SIC	GSIC
Field-effect mobility (cm^2/Vs)	60	20	74	45
Threshold voltage (V)	9	9.5	6.5	7.5
Subthreshold slope (V/dec)	2.8	1.2	0.8	0.8
Minimum leakage current ($\times 10^{-10}$ A)	170	4.5	3.0	0.8
Maximum on current ($\times 10^{-4}$ A)	2.7	1.5	3.5	2.4
Maximum on/off ratio ($\times 10^6$)	0.15	0.32	1.17	2.8

subthreshold slope is improved considerably. The slope is closely related to defects at the channel surface so that it can be said that the major defect at the channel, which is a Ni silicide, is gettered by the heat treatment after deposition of a-Si on top of the crystallized Si layer. Anyway, the electrical properties of the GMIC TFT turn out to be not good enough for AMOLED pixels.

In Figure 4.36, I_D-V_G transfer characteristics of SIC TFT and gettered SIC (GSIC) TFT are compared. Since Ni thin film was removed before the crystallization in SIC process, the electrical performance of SIC TFT is much better than that of MIC TFT. We expect to have much less Ni silicide defects in the channel of SIC TFT than MIC TFT [4.15]. Gettering of SIC TFT turns out to improve the electrical performance considerably as for the case of MIC, which is shown in Figure 4.36. Especially, it can be noticed the leakage current is much reduced and the pinning phenomenon at the maximum value of the gate voltage disappeared in the gettered SIC TFT [4.17]. Exponential increase of off-state current at relatively high gate voltages has been known to be related to defects at the boundary of the drain and channel. Also, it can be noticed that a bump in off-state current, which appears at relatively low gate voltages

disappeared in the gettered TFT. The bump is found to be related to defects at the channel surface [4.17]. No considerable change with the gettering can be noticed in the subthreshold slope, saturation, V_{TH}. The electrical properties of the GSIC TFT have been summarized in Table 4.6.

4.3.2 Gettering Process using Etch Stopper

The comparison of typical I_D-V_G characteristics of SIC and SIC poly-Si thin film gettered using etch stopper layer (G-SIC) poly-Si TFTs is illustrated in Figure 4.37. The curves revealed that while all the devices showed good transfer characteristics, the on/off ratio was drastically improved—more than doubled—by the gettering. It successfully lowered the I_{Leak} by at least an order of magnitude over the range of interest, although the on-state current was slightly lower than that of the SIC poly-Si TFT due to reduction of crystallinity [4.15]. Moreover, the off-state current was particularly improved by gettering: the curve became flatter at low gate voltage and began to increase at V_G of 8 V higher than 5 V for SIC poly-Si TFT. The measured and calculated key parameters are summarized in Table 4.7.

In Figure 4.38, the trap-state density (N_t), the dominant leakage source and results from trapped Ni-silicide in channel, was determined using Levinson and Proano's method [4.28, 4.29], which can estimate the N_t from the slope of the linear region of the curve $\ln[I_D/(V_G-V_{FB})]$ versus $(V_G-V_{FB})^{-2}$ at low V_D and high V_G. The plots were given by Equation (2-19)

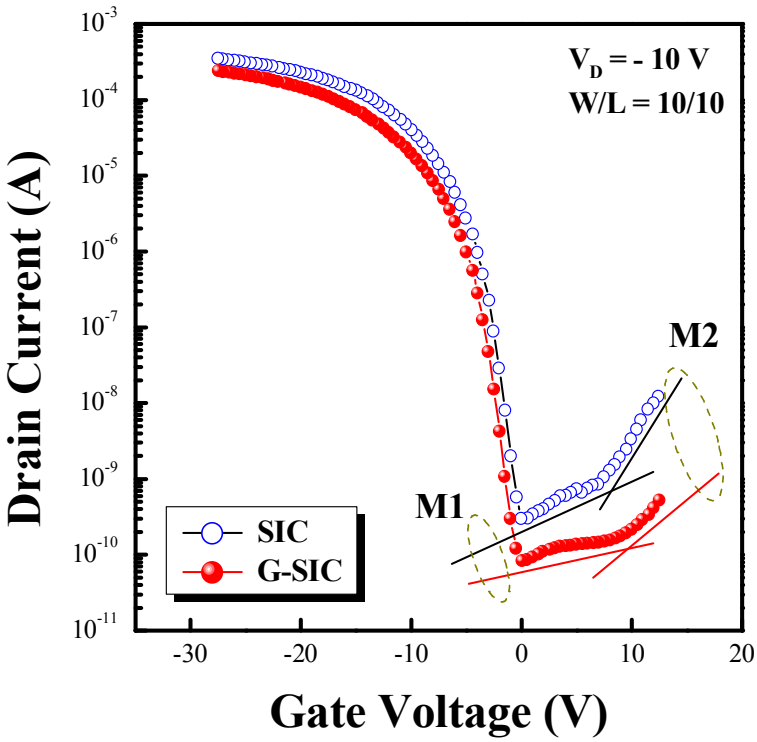


Figure 4.37 Comparison of I_D–V_G characteristics of SIC, and G-SIC

Table 4.7 Device key parameters of the MIC, SIC and G-SIC poly-Si TFTs

W/L = 10/10	SIC	G-SIC
Field-effect mobility μ_{FE} (cm^2/Vs)	62 ± 3	57 ± 4
Threshold voltage V_{TH} (V)	- 6.5 ± 0.3	- 7.5 ± 0.3
Subthreshold slope *S.S* (V/dec)	0.8 ± 0.05	0.8 ± 0.05
Minimum leakage current I_{leak} ($\times 10^{-10}$ A)	3 ± 1	0.8 ± 0.2
Maximum on current I_{on} ($\times 10^{-4}$ A)	3.5 ± 0.4	2.4 ± 0.3
Maximum on/off ratio ($\times 10^6$)	1.1 ± 0.5	2.8 ± 0.2
Trap state density N_t ($\times 10^{12}$ / cm^{-2})	8.4 ± 2.1	2.3 ± 1.8

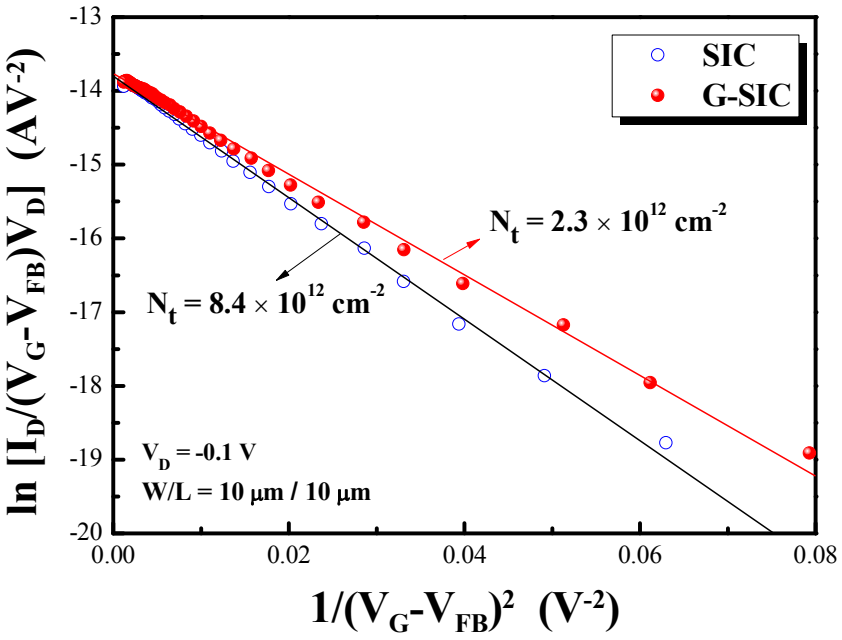


Figure 4.38 Levinson and Proano plots of SIC and G-SIC poly-Si TFTs with different trap densities in the channel region. The lower slope corresponds to the lower trap density.

In this figure, the lower slope corresponds to the lower trap density. As shown in the Figure 4.38, the N_t of the G-SIC was 2.3 × 10^{12} cm^{-2}, which was much lower than that of the SIC (8.4× 10^{12} cm^{-2}).

The I_{Leak} region is well divided in Figure 4.37. It is well known that there are two mechanisms of leakage current [4.2, 4.18]. The first mechanism (M1) is thermal excitation of trapped carriers in the channel at low V_G and high V_D. According to M1, the increased minimum I_{Leak} at V_G = 0 V and high V_D seen in Figure 4.39(a) is the result of a high concentration of trap-states in the channel [4.2]. Furthermore, the Figure 4.39(b) shows that the minimum leakage current is more sensitive to the V_D in the SIC poly-Si TFT than that in the G-SIC poly-Si TFT, because the SIC poly-Si film

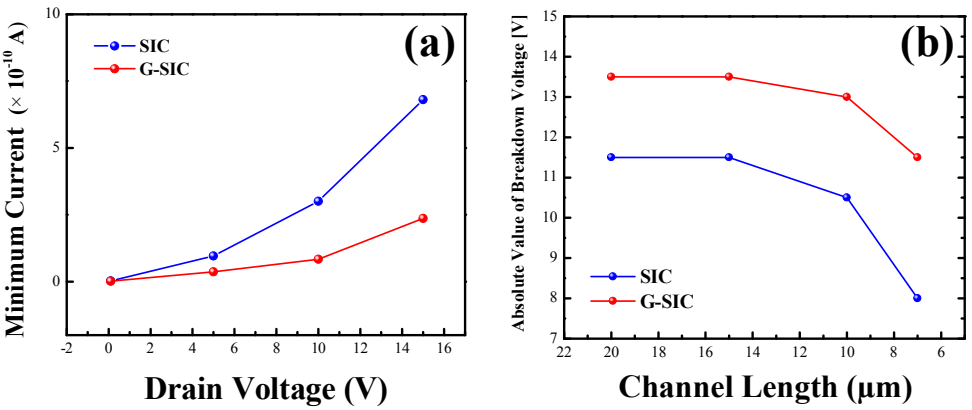


Figure 4.39 (a) Dependences of the minimum leakage current as the increasing of drain voltage and (b) Drain breakdown voltage versus channel length for SIC TFT and G-SIC TFT.

has more trap states caused by Ni precipitates. The second mechanism (M2) is field emission due to field ionization of trapped carrier tunneling through the potential barrier and field-enhanced thermal excitation of the trapped carrier at high reverse V_G [4.2]. It is well known that the field emission is dependent on the channel/drain junction quality and the lateral electric field. This explains why, as shown in Figure 4.37, the off-state current of the G-SIC poly-Si TFTs is flatter than that of SIC poly-Si TFTs at high V_G as well. Furthermore, the off-state current at high reverse V_G of 10 V is lower by almost one order of magnitude, attributed to a low trap-state density due to the lower Ni precipitate concentration at the channel/drain junction. This result is supported by channel junction breakdown voltage (V_{BR}), defined as V_D at I_D = 2 nA and V_G = 0 V, as shown in Figure 4.39(b): the V_{BR} of SIC poly-Si TFTs ($\Delta V = V_{BR}^{20\,\mu m} - V_{BR}^{7\,\mu m}$ = 3.5 V; 43.75%) decreased more drastically than that of G-SIC poly-Si TFT ($\Delta V = V_{BR}^{20\ \mu m} - V_{BR}^{7\ \mu m}$ = 2 V; 17.39%), showing the higher quality of the channel/drain junction in the latter.

4.4 SILC/SILC Boundary Ejection

LTPS TFTs are attractive for use in various fields, such as active-matrix AM-FPDs, because they exhibit good electrical properties, and can be integrated in peripheral circuits on inexpensive glass substrates [4.8]. In addition, flexible substrates will be feasible when the low-temperature crystallization of a-Si can be achieved. Therefore, intensive studies have attempted to lower the crystallization temperature of a-Si. Among the crystallization methods, the most popular method is MIC using Ni [4.9]. The MIC method has many merits compared to other approaches such as ELA or SPC, because it requires a relatively low thermal budget, the process is simple process, and its cost is low. However, the major problem to be addressed for MIC poly-Si is Ni contamination, such as by Ni silicide, which degrades the electrical performance of the device.

Several crystallization methods have been utilized to reduce the unwanted Ni precipitates, such as MILC [4.19], the application of a MIC through capping-layer (SiN_x, SiO_2) [4.13], and the gettering of Ni [4.68, 4.69]. However, these methods are complicated, and require high process temperatures and very long process time, which can damage the poly-Si active layer. In order to fabricate high performance poly-Si TFTs by reducing Ni contaminations, silicide SIC was studied using *in-situ* silicidation during Ni deposition, in which the Ni was deposited by sputtering at room temperature. Ni silicide seed dots were formed by Ni sputtering at room temperature, which can act as nuclei during crystallization [4.15, 4.70]. But, the SIC poly-Si thin film consisted of non-uniform grains, which can result in problems with non-uniform electrical properties in a panel. To improve the electrical performance and uniformity, lateral crystallization was applied. The process is called SILC," because a seed must

be formed right after Ni sputtering in order to produce a lateral crystallization, even when the substrate is kept at room temperature during sputtering. Although the process of lateral crystallization takes somewhat more time than the conventional MILC process, the poly-Si TFTs prepared in this manner showed much better electrical properties than MILC TFTs [4.17, 4.71]. However, the relatively high leakage current and low field-effect mobility are regarded as problems for employing this technology. It has been thought that the main reason for these problems is the crystal boundary formed by laterally grown crystallites in both the source and drain regions (SILC/SILC boundary, SSB hereafter), which are formed in the center of the channel region [4.72]. The SSB contains many defects, such as micro-twins and metal silicide, which act as trap sites for high leakage current. These defects work as a scattering source that reduces the field-effect mobility considerably [4.55].

Recently, Kim *et al*. and Song *et al*. reported that adjacent Pd metal enhanced the crystal growth rate of Ni MILC without additional energy. The electrical properties of poly-Si TFTs could be improved by ejecting the SSB from the channel [4.73, 4.74]. But, the method requires complicated processes, such as Ni and Pd deposition and removal. In the present study, a novel method of SSB ejection from the channel was investigated to achieve a simpler fabrication process and better electrical properties, and the performance of the devices was analyzed in term of breakdown voltage and short channel effects.

4.4.1 Mechanism of SILC/SILC Boundary Formation

Figure 4.40 shows the FESEM images of MIC/MILC and MILC/MILC boundary regions after Secco etching ($Fe_2Cr_2O_7$ + HF + H_2O). The Secco etchant can selectively etch a-Si and Ni silicides from crystalline Si (c-Si). As shown in Figure 4.40(a), more Secco-etched holes exist in the SIC region than in the SILC region, since the SIC region contains more Ni silicides than the SILC region. The contained Ni silicides are segregated at grain boundaries. Figure 4.40(b) shows that apparent crystalline defects of grain boundaries were formed at the channel region of the SILC poly-Si TFTs after completion of the crystallization process, and the crystallinity of the boundary was very poor. The defects contained a high concentration of Ni silicides and inter-grain micro-defects [4.74]. It is well known that the Ni silicides are trapped at the center of the channel region in conventional SILC poly-Si TFTs. This occurs because the needlelike c-Si grows toward the c-Si region with the migration of Ni silicides and the individual crystallites form networks during SILC annealing. When the Ni silicide layer at the front of a c-Si grain meets other c-Si grains that have already been crystallized by the SILC process, the Ni silicides can no longer migrate through the c-Si grains because there is no difference in the chemical potential between the two c-Si regions. Thus, the Ni silicides are segregated and form an SSB at the center of the channel region. These SSB defects in the channel region can possibly degrade the electrical properties of the SILC poly-Si TFTs. It was reported that the major source of leakage current in the SILC poly-Si TFTs in the off-state is the SSB, because the segregated Ni silicides generate localized trap states [4.72]. When mobile carriers encounter the SSB within the channel region, a certain amount of these carriers are

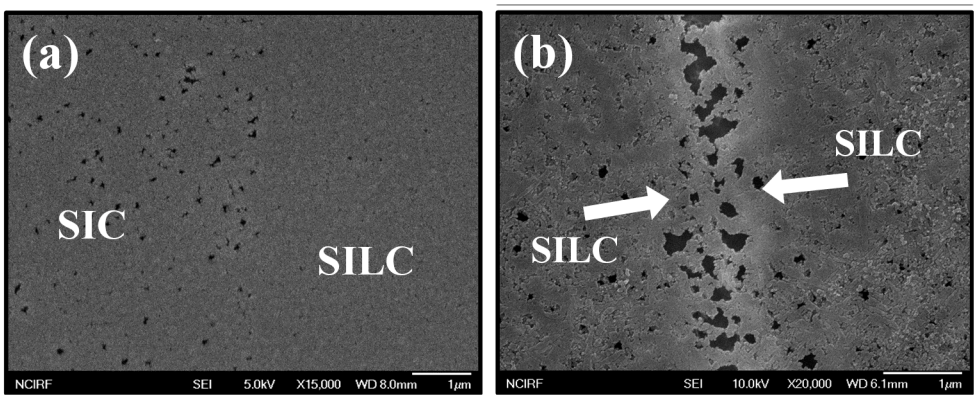


Figure 4.40 FESEM images of SIC, SILC, and SILC boundary regions. The samples were chemically treated by Secco etchant before analysis.

trapped at the SSB, and then the on-current and the field-effect mobility of the TFTs are reduced [4.55].

4.4.2 Electrical Properties of SSB Ejected SILC Poly-Si TFTs

Typical I_D-V_G transfer characteristics of the conventional symmetrical SSB, drain SSB, and source SSB are plotted in Figure 4.41. The key parameters of the devices are listed in Table 4.8. The transfer characteristics reveal that while all the TFTs showed good transfer and inversion characteristics, the off-state leakage current with a high reverse gate bias applied (V_G > 5 V) shows different aspects according to the location of the SSB. The different aspects are intensified at higher drain voltage (V_D = -10 V), as shown in Figure 4.41(b). It is well known that the leakage current region can be categorized according to two mechanisms [4.1, 4.2, 4.18]. The first mechanism is the thermal generation of trapped carriers in the channel at low gate voltage and high

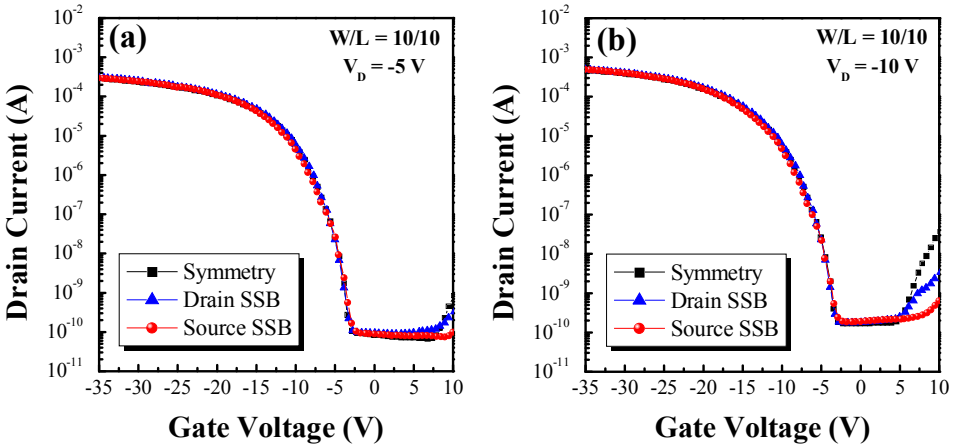


Figure 4.41 Typical I_D-V_G transfer curves of conventional symmetrical, drain-SSB, and source-SSB poly-Si TFTs measured at (a) V_D = -5 V and (b) V_D = -10 V.

Table 4.8 Device key parameters of the conventional MILC, drain MMB, and source MMB poly-Si TFTs.

Key parameters	Symmetrical	Drain-MMB	Source-MMB
Field-effect mobility μ_{FE} (cm^2·/Vs)	88	91	96
Threshold voltage V_{TH} (V)	7.8	7.7	7.8
Subthreshold slope $S.S$ (V·dec^{-1})	0.85	0.83	0.80
Minimum leakage current I_{Leak} ($\times 10^{-10}$ A)	1.79	1.77	1.75
Maximum on current Ion ($\times 10^{-4}$ A)	4.81	4.96	4.92
Maximum on/off ratio ($\times 10^{6}$)	2.83	2.80	2.65

drain voltage. This thermal excitation strongly affects the minimum leakage current at low reverse gate bias. The second mechanism is field emission due to the field ionization of trapped carriers tunneling through the potential barrier, and field-enhanced thermal excitation of the trapped carriers at high reverse gate voltage. In

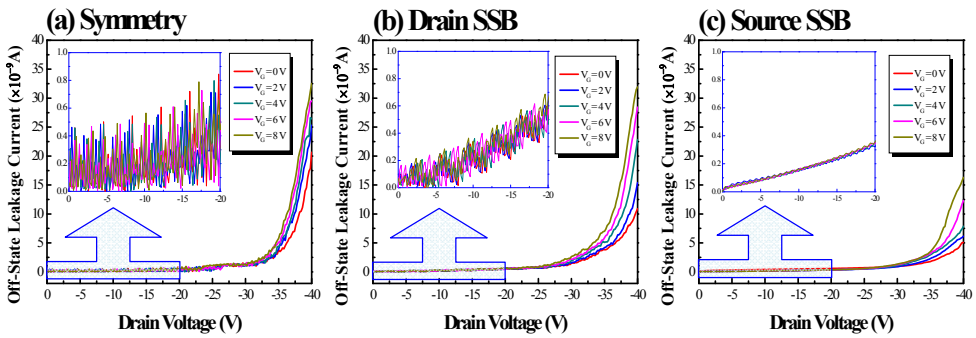


Figure 4.42 Reverse gate bias dependence of leakage current as a function of drain voltage characteristics for (a) symmetrical, (b) drain-SSB, and (c) source-SSB poly-Si TFTs. In each plots, the leakage drain current noise at low drain voltage is shown.

Figure 4.41(b), it can be clearly seen that the leakage current in the high reverse gate bias region is drastically suppressed by ejecting the SSB in the source direction compared with the conventional symmetrical SSB poly-Si TFTs with the SSB at the center of the channel. The leakage current improvement was attributed to the reduction of the trap state in band gap, as well as to the field emissive leakage current source due to the Ni silicides having formed trap states into the band gap of poly-Si. The reduction of the trap state in the depletion region of the reverse junction in the band gap means that the channel/drain junction was improved by ejecting the SSB in the source direction [4.31], which is supported by the channel junction breakdown voltage measurement as shown in Figure 4.42.

In order to investigate the reverse gate bias dependence of the leakage current, the changes in the off-state leakage current as a function of drain voltage for various reverse gate voltages was measured according to the SSB location, as shown in Figure 4.42. It can be clearly observed that the off-state leakage current of the conventional symmetrical SSB poly-Si TFT was most rapidly increased with a higher electric field (high drain and gate voltages), as shown in Figure 4.42(a). Moreover, despite the low

reverse gate voltages, the off-state leakage current was drastically increased with increasing drain voltage. In the case of poly-Si TFTs with an SSB ejected from the channel to the drain-SSB and source-SSB, the off-state leakage current was efficiently suppressed at low reverse gate voltages compared with the conventional symmetrical poly-Si TFT, as shown in Figure 4.42(b). In particular, a greatly suppressed off-state leakage current was observed with the source-SSB poly-Si TFT at high reverse gate voltage and drain voltage, as shown in Figure 4.42(c). From these results, the electric field level applied to the SSB can be compared by comparing the trapped carrier generation, which changes when an electric field is applied to the SSB. First, comparing the conventional symmetrical SSB and the drain-SSB and source-SSB poly-Si TFTs, the gate voltage more strongly affected the off-state leakage current of the conventional symmetrical SSB poly-Si TFT than that of the ejected SSB poly-Si TFTs. This means that SSB ejecting can efficiently suppress the field emission at high drain voltages by the reduction of the trap states in the depletion region in the band gap. Second, comparing the drain SSB and source SSB poly-Si TFTs, the off-state leakage current was more drastically decreased when the SSB was ejected in the source direction than in the drain direction, because the electric field applied to the source SSB was smaller than that applied to the drain SSB due to the source-drain voltage drop. The each magnified off-state leakage current plot at relatively low drain voltages from 0 V to -20 V, which were used to compare the off-state leakage drain current noise also shown in Figure 4.42. Dimitriadis *et al*. reported on the causes of the drain current noise in poly-Si TFTs [4.30]. The drain current noise was related to the carrier number fluctuations due to oxide traps and additional fluctuations of the potential barrier height at the grain boundaries. These reports support the present investigation in terms of the SSB forming a potential barrier that affects the carrier

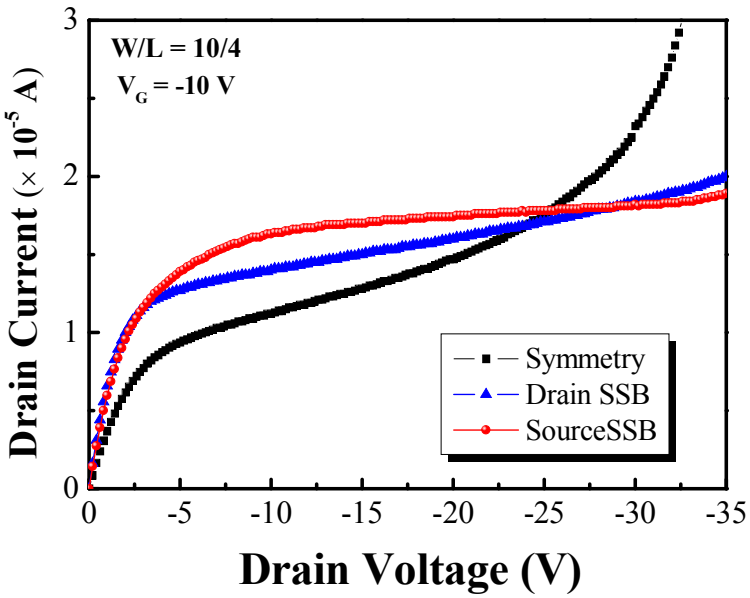


Figure 4.43 Comparison of I_D-V_D output characteristics of (a) symmetrical, (b) drain-SSB, and (c) source-SSB poly-Si TFTs.

transportation. When the SSB is located in the channel (conventional symmetrical poly-Si TFT) or near the channel/drain junction (drain-SSB poly-Si TFT), which strongly affects the electrical properties of the TFTs, it acts as a scattering source for carrier transportation, which induces fluctuation in the carrier number by the potential barrier of the SSB. Ejecting the SSB to the source direction suppressed the off-state leakage drain current noise.

As mentioned above, the SSB acts as a scattering source, which is well known to impede the carrier transportation. Then, the on-state current and field-effect mobility are degraded by the SSB. Figure 4.43 shows a comparison of the I_D-V_D output characteristics of the conventional symmetrical, drain-SSB, and source-SSB poly-Si TFTs. The on-state currents, which are related to the field-effect mobility are also

compared. As shown in Figure 4.43, although the on-state current was improved by ejecting the SSB from the channel, especially in the source direction, can drastically improve the on-state current compared with other configurations. Furthermore, the source-SSB poly-Si TFT exhibits kink-free I_D-V_D output characteristics. This is due to fact that when the SSB is located along the channel or drain junction, either the drain electric field or the impact ionization rate is enhanced due to the presence of charged defect states in the SSB, such as grain boundary traps or Ni contamination [4.75].

4.5 Lightly Doped Drain Structure

The current pinching phenomenon in the offset gate structure can be improved by employing an lightly doped region between the channel and drain, i.e., lightly doping the offset region. The LDD region can be formed by, for example, an additional implantation or ion-doping of impurity atoms with a low dosage. Alternatively, the LDD region can be formed by doping through a thick insulating layer, such as SiO_2 or TaO_x, extending from the gate edge. LDD region can be formed together with doping for the source and drain, since the insulating layer lowers the acceleration voltage and hence the doping concentration.

Since the parasitic resistance effect is inversely proportional to the LDD doping concentration N_{LDD} while the drain field decreases for decreasing the N_{LDD}, the choice of N_{LDD} is determined ion the actual application requirement of the TFT. The LDD structure also lowers the lateral field in the saturation regime, and consequently, decreases the impact ionization rate.

Once of the difficulties in preparing the LDD structure is that the lightly doped implant, in addition to being expensive, is difficult to reproduce. This is because the background doping and the doping efficiency, both closely related to the grain size and defects in the grain boundary and within the grains, vary from run to run and are difficult to control. The other difficulty is the LDD length, which significantly affects the output current and can vary in the wafer. If the offset region is determined by, for example, the sidewall of the passivation layer, the variation will be reduced.

4.5.1 LDD Region on MILC Poly-Si TFTs

Currently, a lot of attention is being drawn to research on poly-Si TFTs for applications in AMOLEDs. Since AMOLED is a current controlled device, TFTs with high field-effect mobility and low leakage current are necessary in AMOLED panels. The poly-Si TFTs have considerably high mobility compared to a-Si TFTs while having relatively high leakage current [4.8]. The core technology for the fabrication of poly-Si TFTs is a crystallization method, within which non-laser and laser technologies can be distinguished [4.61]. The method using a laser is not only very expensive but also disadvantageous for a large substrate since it is a scanning process [4.76, 4.77]. On the other hand, SPC, which is one of the non-laser methods, has to be done at a relatively high temperature and therefore an ordinary glass substrate cannot be used. Furthermore, solid phase crystallization is time consuming process. [4.78, 4.79] MILC technology requires neither a high temperature nor a scanning process, so it places no limitation on the substrate size. [4.19, 4.20] However, it suffers from a relatively high leakage current and off-state leakage current [4.80, 4.81]. It has been

known that the leakage current in poly-Si TFTs arise from the high electric field between channel and drain region, which result in the activation of free carriers that are trapped at the grain boundaries located at the boundaries between the drain and the gate [4.1, 4.75, 4.82, 4.83]. It has also been reported that a LDD or field induced drain (FID) structure is very effective for reducing the leakage current because these structures may reduce the electric field between the channel and drain [4.63, 4.84]. In the this work, we fabricated gate insulator doping mask (GIDM) LDD MILC TFTs and demonstrated that the GIDM LDD structure can effectively suppress off-state leakage current in MILC poly-Si TFTs [4.85, 4.86]. From this result, it was confirmed that GIDM LDD structure is very effective to reduce the electric field at the channel/drain junction in MILC TFTs. However, if the dopant concentration in LDD is too low, the LDD region can act as a resistor in TFTs so that the mobility of the TFT is reduced. On the other hand, if the concentration of LDD region is too high, the LDD structure does not work for reducing the electric field. Therefore an appropriate dopant concentration in LDD region has to be decided. In order to find the dopant concentration of the LDD region without performance degradation, we fabricated and analyzed the electrical properties of without LDD MILC TFT and GIDM MILC TFTs having different LDD dopant concentration. The dopant concentrations in LDD regions of the TFTs were measured by using secondary ion mass spectroscopy (SIMS). From the electrical properties and the SIMS data of the TFTs, we have found the optimum dopant concentration in LDD region for *n*-type MILC TFTs.

4.5.2 Leakage Current Suppression

Figure 4.44 shows the I_D-V_G transfer characteristics of (a) conventional MILC TFT and (b) GIDM LDD MILC poly-Si TFT. In this figure, it is found that the minimum current of LDD TFT is considerably lower than that of conventional MILC TFT. And the GIDM LDD TFTs have the flat region from the gate voltage of minimum leakage current to the gate voltage of 10 V, while conventional MILC TFT shows sharp increase of current in that gate voltage region. It has been reported that the sharp increase of current in negative gate voltage region in *n*-type poly-Si TFT is related to the activation of defects in channel/drain junction, due to the high electric field in the junction [4.1, 4.2, 4.6]. On the basis of this, It has been thought that the reduction of minimum current and the suppression of the off-state leakage current in GIDM LDD TFT arise from the reduction of electric field in the channel/drain junction in the TFTs. From this result, it is confirmed that GIDM LDD structure is very effective to reduce the electric field at the channel/drain junction in MILC TFTs.

Doping profiles for source, drain, and the LDD regions of GIDM LDD TFTs with different gate insulators are compared in Figure 4.45. The LDD dopant concentration of SiN_x GIDM LDD TFT could not be plotted in this figure, because the dopant concentration of the SiN_x GIDM LDD TFT is too low to be plotted in the scale of this figure. As shown in Figure 4.44, the dopant concentration in LDD region is reduced as the thickness of gate insulator increases. And almost undoped LDD region is made when the 1,000 Å of SiN_x is used as a doping mask. From this result it is confirmed that the dopant concentration in LDD region can be controlled by adjusting the gate insulator thickness and the type of gate insulator materials.

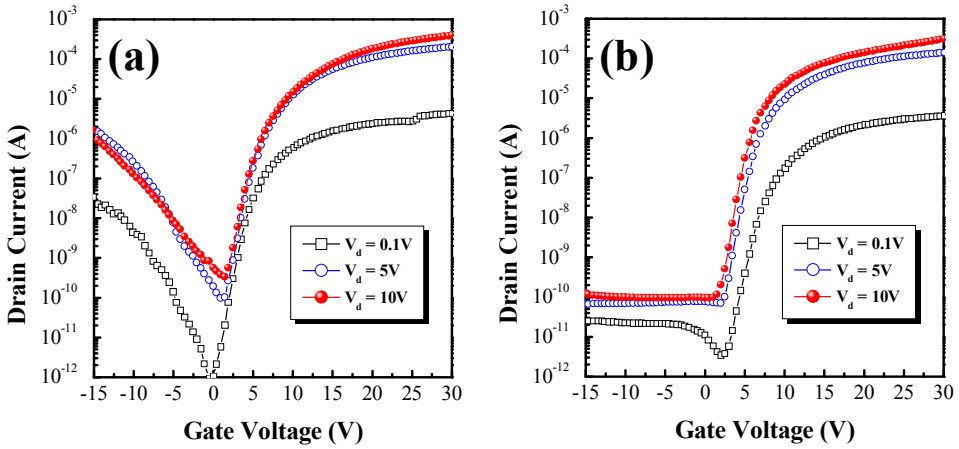


Figure 4.44 I_D-V_G transfer curves of (a) conventional MILC poly-Si TFT and (b) GIDM LDD MILC poly-Si TFT.

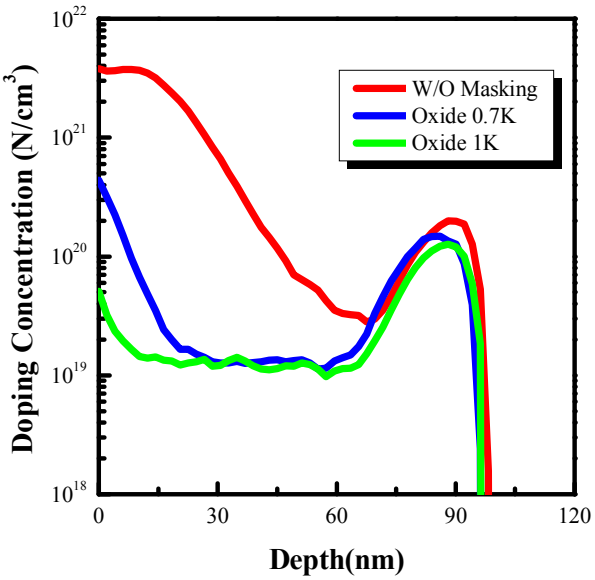


Figure 4.45 Doping profiles for source/drain and the LDD regions of GIDM LDD TFTs with different gate insulator thicknesses.

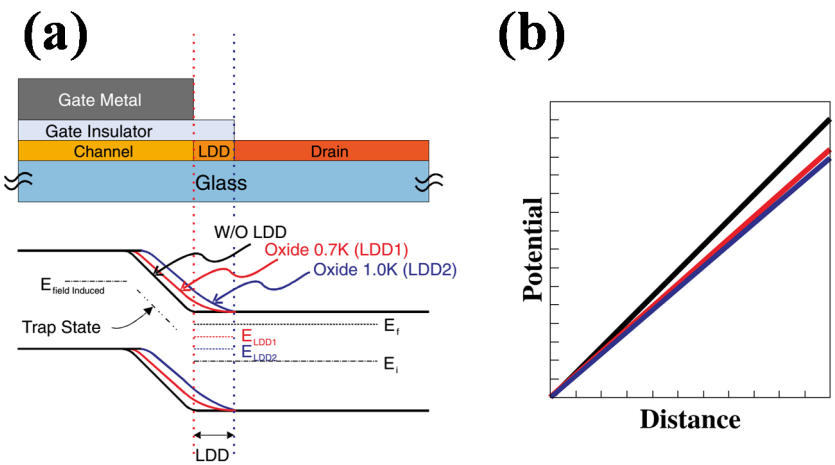


Figure 4.46 (a) Energy-band diagrams of the conventional SILC TFT (Without LDD) and GIDM LDD TFT with different gate insulator thickness. (b) Potential gradients near the drain edge of channel region of the TFTs.

The energy-band diagrams for the without LDD SILC poly-Si TFT and GIDM LDD SILC poly-Si TFTs are sketched in Figure 4.46. The relative positions of Fermi energy in each LDD regions are determined based on the SIMS data. The black, red, and blue lines correspond to the energy-band diagram for conventional TFT, 700 Å SiO_2 GIDM, and 1,000 Å SiO_2 GIDM LDD TFTs respectively. Figure 4.46(b) shows the potential gradient in channel/drain junction. The gradient of black line(W/O LDD TFT) is bigger than those of red and blue line. It is well known that the maximum electric field in a junction is proportional to the potential gradient within space charge region. [4.87, 4.88] Since, the Fermi energy of LDD region is higher than that of channel region, the potential difference between LDD and channel region is lower than that between drain and channel in *n*-Type LDD TFT, the voltage drop at the channel/drain junction takes place not only in channel region but also in the LDD region, the potential gradient at the junction may be additionally lowered. As a result

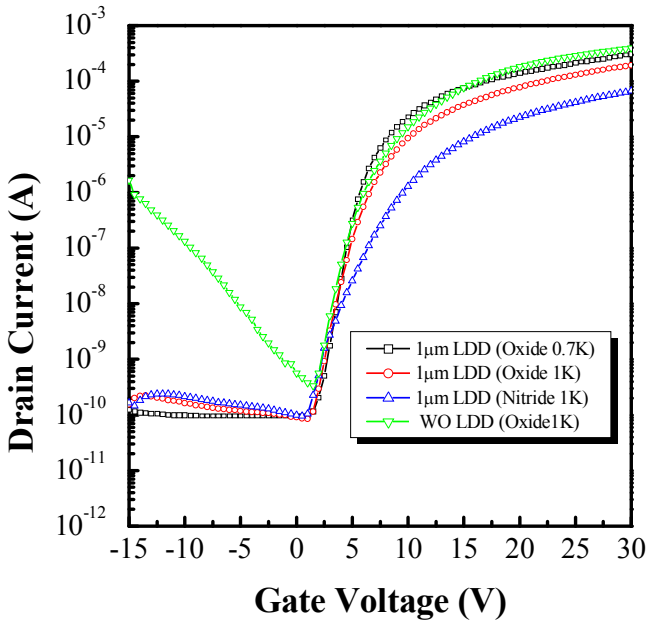


Figure 4.47 I_D-V_G transfer characteristics of conventional SILC TFT and GIDM LDD SILC poly-Si TFTs with different gate insulators.

of these two effects (potential difference reduction and voltage drop region extension), the potential gradient is reduced in LDD TFTs and therefore, the number of activated trap sites can be reduced. Hence, the free carrier generation near the channel/drain junction in the LDD structure is not as significant as it is in the normal structure.

The I_D-V_G transfer characteristics of conventional SILC TFT and GIDM LDD SILC poly-Si TFTs are compared in Figure 4.47. The off-state leakage current are well suppressed in all GIDM LDD SILC poly-Si TFTs, but the on-state current of the TFTs are reduced with the decrease of the dopant concentration in LDD region and the on-state current reduction of the TFT having undoped LDD region is remarkable.

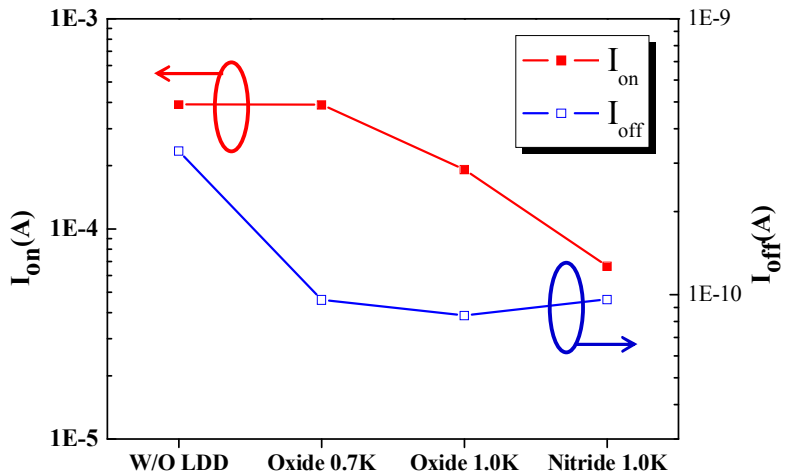


Figure 4.48 ON /OFF current variations as a function of gate insulator thickness.

The abrupt reduction of the on-state current in undoped LDD TFT is thought to be attributed to the increase of series resistance in the undoped LDD region.

The on-state current and the off-state leakage current of the poly-Si TFTs having different structure are plotted in Figure 4.48. From this figure, It can be found that both the on-state current and the off-state leakage current reduction takes place when LDD structure is formed on the SILC poly-Si TFTs, however, the magnitude of on current reduction is negligible in oxide 700 Å GIDM TFT, while the magnitude of off-state leakage current reduction is remarkable in the TFTs. Therefore, the oxide 700 Å GIDM poly-Si TFT shows highest value of on/off current ratio, of which sufficiently high value is necessary for driving OLED devices. It is also found that the field-effect mobility of LDD TFT having 700 Å oxide gate insulator is slightly higher than that of the without (W/O) LDD TFT, even though the 700 Å oxide LDD TFT shows not only almost 1order of magnitude lower off current but also well suppressed off-state leakage current. The higher field-effect mobility of 700 Å oxide LDD TFT

than W/O LDD TFT is thought to be caused by the capacitance increase due to the decrease of gate insulator thickness as well as the decrease of series resistance in LDD region due to the relatively high dopant concentration in the LDD region.

CHAPTER 5

Enhancement of Driving Characteristics

5.1 Factors Influencing the Driving Characteristics

ELECTRICAL performance of the TFT depends on the characteristics of the poly-Si thin film, such as the density of trap-state in the grain and grain boundaries, the conductivity, the interface trap state density between gate insulator and poly-Si active layer, and its device geometry. Table 5.1 summarizes the factors influencing poly-Si TFT performance. Here, the most important factors are the density of trap-state in the poly-Si, the interface state between poly-Si and gate insulator. In order to improve the driving characteristics, such as on-state current, subthreshold slope, and field-effect mobility, the trap-state in the grain and interface should be minimized. Moreover, the electrical stress effect was also investigated. Generally the electrical stress had been used for studying about reliability of device at various stress condition. But in this study, it was used to change of the charge state of interface and active. And then the condition for enhancement of electrical performance was investigated and analyzed.

Table 5.1 Factors influencing poly-Si TFT performance.

TFT Performance	Dominant factor
On-Current	♦ W/L ♦ Drift mobility ♦ Interface trap state (poly-Si/Gate insulator) ♦ Ohmic contact ♦ Trap-state density in poly-Si ♦ Back interface state
Off-current	♦ W/L ♦ Fermi level (poly-Si) ♦ Interface trap state (poly-Si/Gate insulator) ♦ Back surface charge ♦ Band gap
Field-Effect Mobility	♦ Trap-state density in poly-Si ♦ Interface trap state (poly-Si/Gate insulator)
Subthreshold Slope	♦ Trap-state density in poly-Si ♦ Interface trap state (poly-Si/Gate insulator)

5.2 Channel Splitting Effect

Recently, LTPS became a dominant active layer material due to their much higher mobility and drivability instead of a-Si for various applications [5.1, 5.2]. In addition, flexible and cheap glass substrates can be used when the low temperature crystallization of a-Si is realized. Therefore, intensive studies have been made on lowering the crystallization temperature of a-Si. Among the crystallization methods, the most popular methods are MIC and MILC using Ni. [5.3, 5.4] Compared with other techniques, such as SPC and ELA, the MIC and MILC methods have many advantages, including a low-cost batch process and a smooth film surface. However,

the relatively high leakage current due to Ni contamination and low field-effect mobility due to the grain boundary defects of scattering source are disadvantages compared with ELA poly-Si TFTs. It is generally known that, the poly-Si has many grain boundaries resulting in a large number of defects and they produce trap-states in the band gap region [5.5, 5.6]. The defects in the channel create potential barriers that lower the driving current and field-effect mobility, and the trap states in the band gap act as recombination sites that degrade the inversion characteristics such as subthreshold slope and threshold voltage.

In this chapter, split channel TFTs having same processes compared with conventional SILC poly-SI TFTs are introduced. The split channel means that the channel width is divided but the numerical channel size is kept constant. The improvement of the driving current and field-effect mobility were discussed in terms of the effective channel width enlargement and the crystal filtering effect, leading to a vast decrease of trap-states in the grain boundaries and interface between the poly-Si and gate insulator. In addition, variation regarding the series resistance of the active layer is also discussed; the relation between the variation of series resistance and the quantity of field-effect mobility degradation from that of intrinsic is clarified.

5.2.1 Experimental

In the present study, *p*-channel SILC poly-Si TFTs with self-aligned coplanar structures were fabricated on glass. In order to compare the relation between the number of split channels and the electrical performance of the poly-Si TFTs, a series of four different TFTs having a various number of split was fabricated. The channel

Table 5.2 Details of Prepared poly-Si TFTs having various number of split-channel paths.

	SC-1	**SC-2**	**SC-5**	**SC-10**
Number of channel paths	1	2	5	10
Path width W_{path} (μm)	10	5	2	1
Numerical channel width W (μm) (No. Channel × W_{path})	1×10=10	2×5=10	5×2=10	10×1=10
Channel length L (μm)	10	10	10	10
W/L	1	1	1	1

splitting was done by channel width dividing into 1 (SC-1 TFT), 2 (SC-2 TFT), 5 (SC-5 TFT), and 10 (SC-10 TFT) with a fixed channel length (Table 5.2). It is noticed that the numerical channel sizes were constant (width × length: 10 μm × 10 μm) and all TFTs were fabricated on the same substrate, so the only difference in this work is the number of split channels. Figure 5.1 shows the optical microscope images of the poly-Si TFTs having the split channel fabrication process after gate formation.

For devices fabrication, a SiN_x buffer layer of 1500 Å thickness was deposited on glass substrate (Eagle XG; SAMSUNG Corning Inc.; size, 106 mm × 106 mm) by PECVD to prevent inter-diffusion of undesirable species from the glass substrates. Thereafter, a 1000 Å-thick a-Si layer was deposited by LPCVD using SiH_4 gas at a temperature of 500 °C. In order to define the active pattern, photolithography and RIE using SF_6 gas were utilized. Ni film was deposited on source and drain areas after photolithography with a hole pattern mask. The Ni film was sputtered at DC 700 V for 15 sec. The ultimate pressure in the chamber was 2×10^{-6} Torr. The working pressure was 30 mTorr with an Ar flow rate of 30 sccm and a throttle valve was used to keep

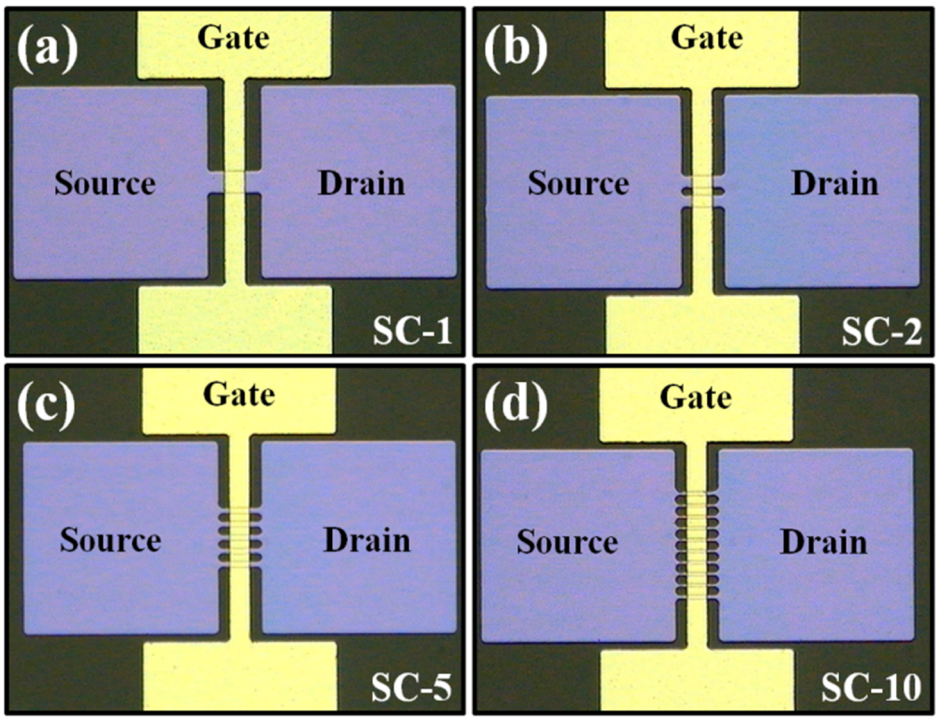


Figure 5.1 Optical microscope top view images of split channel poly-Si TFTs with W/L = (a) 10 μm / 10 μm × 1, (b) 5 μm / 10 μm × 2, (c) 2 μm / 10 μm × 5, and (d) 1 μm / 10 μm × 10.

the pressure constant. The current was measured to be 0.5 mA and the thickness was estimated to be approximately 50 Å by extrapolating the straight line in a plot of thickness versus sputtering time. The lift-off method was used for the Ni island pattern. For the SILC process, the Ni was removed right before the sample was put into a furnace for crystallization annealing. After crystallization in hydrogen ambient at a temperature of 550 °C for 2 h, 1000 Å-thick gate oxide was deposited by PECVD using SiH_4 and N_2O gases at 350 °C, and a 2000 Å-thick MoW gate metal was subsequently deposited by sputtering. The gate metal was etched by H_3PO_4 + CH_3COOH + HNO_3 + H_2O etchant and the gate oxide was etched by RIE using SF_6,

Ar, and CHF_3 gases. In order to define the source/drain junction, the samples were doped by an IMD system using B_2H_6 source gas diluted with 80% of H_2 gas. The accelerating voltage and RF power were 17 keV and 150 W. After the source/drain formation, a 600 nm-thick dielectric interlayer was deposited. Then, the dopants were activated by furnace annealing in hydrogen ambient at a temperature of 550 °C for 2 h. After opening contact holes by RIE, metallization was performed with a 600 nm-thick MoW. The I_D-V_G transfer curves were measured by Agilent System. The entire fabrication process was carried out in a 1000-class clean-room.

5.2.2 Result and Discussion

Figure 5.2 shows the comparison of I_D-V_G transfer characteristics and the field-effect mobilities of poly-Si TFTs having a various number of split channels, the measured and extracted parameters are summarized in Table 5.3. In Figure. 5.2, the curves reveal that, all TFTs demonstrated good transfer characteristics. But, the on-state driving current and field-effect mobility were significantly increased from 5.0×10^{-4} to 1.2×10^{-3} A and from 78 to 231 cm^2/Vs as a function of channel splitting number. The inversion characteristics such as subthreshold slope and threshold voltage were also significantly improved from 0.59 to 0.47 V/dec and from -7 to -4 V. From the point of view of off-state leakage current, it was slightly increased with channel splitting. However, the quantity of leakage current increase was much lower than on-state driving current. Therefore the on/off current ratio was gradually increased from 1.9×10^7 to 4×10^7 with channel splitting to narrower width.

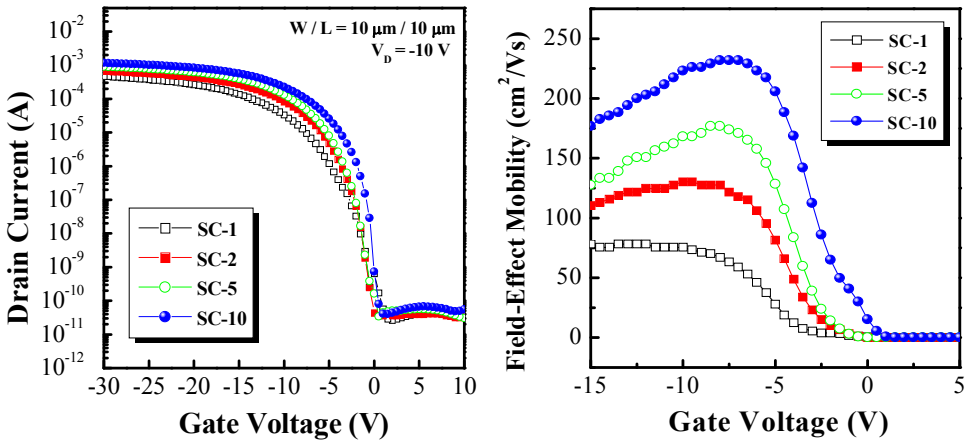


Figure 5.2 Comparison of C_{GSD}-V_G characteristics of SC-TFTs having a various number of split channels. The inset figure shows the measurement circuit.

Table 5.3 Device key parameters of SC-1 (conventional), SC-2, SC-5, and SC-10 poly-Si TFTs.

W/L = 10/10	SC-1	SC-2	SC-5	SC-10
V_{TH} (V)	-7	-5.5	-5	-4
S.S (V/dec)	0.59	0.52	0.50	0.47
Max. I_{on} ($\times 10^{-4}$ A)	5.0	6.9	9.4	12
Min. I_{off} ($\times 10^{-11}$ A)	2.6	3.1	3.4	4.0
on/off ratio ($\times 10^{7}$)	1.9	2.2	2.7	3.0
μ_{FE} (cm^2/Vs)	78	130	176	231
μ'_{FE} (cm^2/Vs)	83	133	178	232
R_s (Ω)	1033	737	372	300
N_t ($\times 10^{12}/cm^2$)	5.25	4.30	3.75	3.04
N_{it} ($\times 10^{12}/cm^2$)	3.69	3.21	3.06	2.86

In previous report in 2006 [5.6], the crystal filter which can improve the driving characteristics on the MILC poly-Si TFTs. But the off-state leakage current also increased with narrower crystal filter width. Therefore, the on/off current ratio was not

enlarged. Because MILC poly-Si layer has much higher Ni related defects density and randomly grown crystallites compared with the SILC poly-Si layer which are applied in present work [5.5]. Furthermore, the present SILC poly-Si TFTs having split channel had simple structures which can be integrated into panel compared with MILC crystal filtered poly-Si TFTs.

It is well known that there are three main causes to affect electrical performance, especially the driving characteristics of poly-Si TFTs such as (1) channel geometry (width and length) of poly-Si TFTs, (2) series resistance, and (3) grain boundary and interface trap-state densities. In this paper, the three main causes were intensively investigated and demonstrated.

a. Geometry – Enlarged Effective Inversion Area

The effective channel width and length are changed by channel geometry while supposing the numerical channel width and length are constant. The drain current and field-effect mobility are proportionately affected by the change of the effective channel geometry. In the linear region, the driving current equation of the poly-Si TFTs can be written as

$$I_D = \frac{W}{L} C_{ox} \mu_{FE} (V_G - V_{TH}) V_D, \tag{5-1}$$

where W, L, C_{ox}, and V_{TH} are the effective channel width, length, gate insulator capacitance, and threshold voltage, respectively. In this study, the effective channel length was kept constant for all TFTs by the same photolithography process of the gate mask, but the effective channel width was altered by channel splitting along the

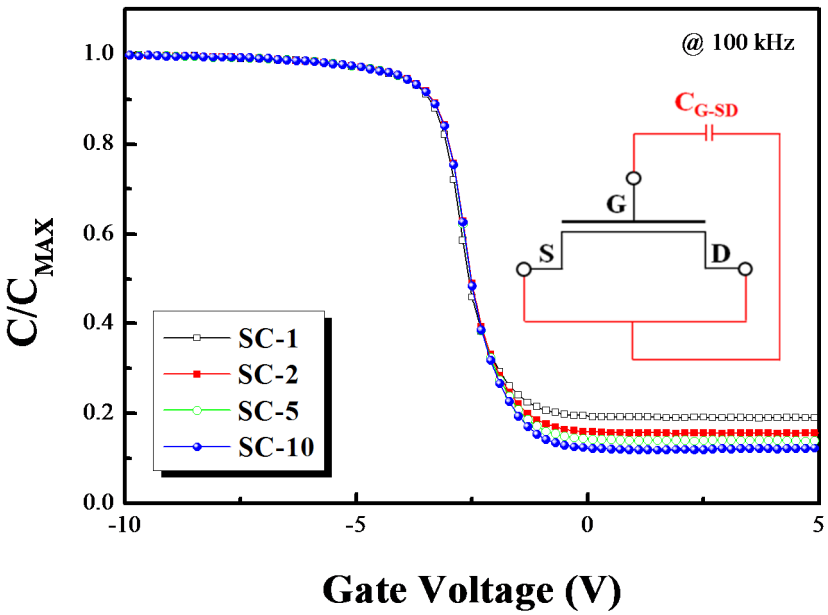


Figure 5.3 Comparison of C_{GSD}-V_G characteristics of SC-TFTs having a various number of split channels. The inset figure shows the measurement circuit.

carrier flow direction. In order to investigate the change of the effective channel width, capacitance-gate voltage was measured as shown in Figure 5.3. The maximum value of capacitance is not changed, but the minimum value of capacitance is significantly increased with the number of split channel paths. This result means that the effective channel length was not changed, but the effective channel width was increased by the channel splitting method. The maximum value of capacitance related to effective channel length due to it was measured in the inversion region of on-state gate voltage (V_G < 0 V) [5.7], and the minimum value of capacitance in the off-state gate voltage region (V_G > 0 V) attributed to the increased overlapped capacitance caused by the enlargement of the inversion area due to the increase of the effective channel width [5.8]. In this study, the conventional photolithography and reactive ion etching (RIE)

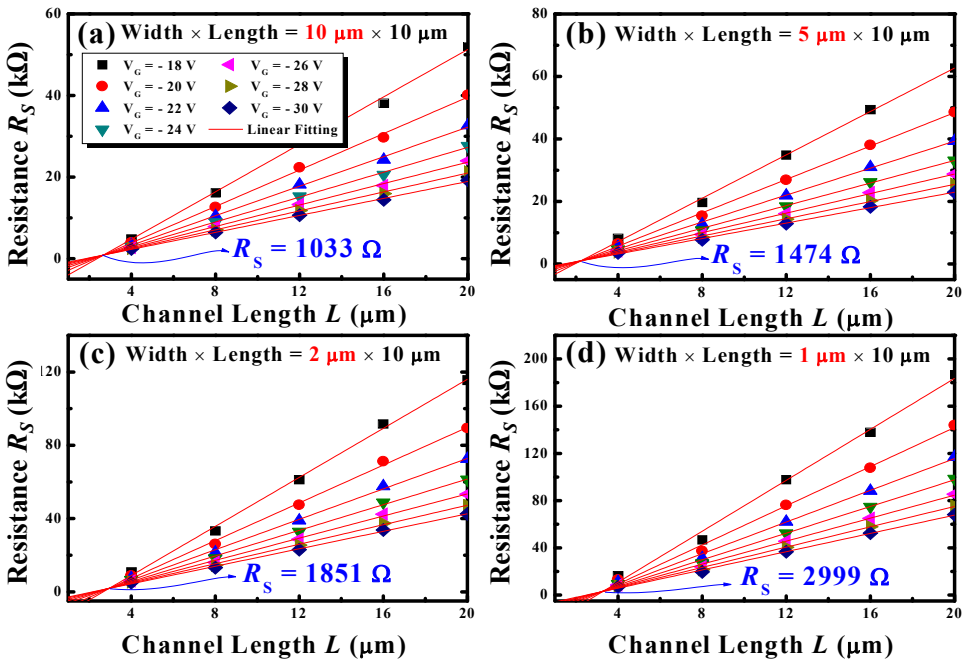


Figure 5.4 Series resistances versus channel length as a function of gate voltage for various channel widths of (a) 10 μm, (b) 5 μm, (c) 2 μm, and (d) 1 μm, respectively.

using SF_6 were utilized to define the active pattern. Therefore, the shape of active corner becomes the trench corner with a sharp edge. This means that the number of trench corner increased with split channel number, and as a result the inversion area as well as the effective channel width was enlarged and driving current, inversion property was improved.

b. Lowered Series Resistance

The effect of series resistance, which greatly lowers driving current and field-effect mobility due to drain voltage drop along the direction of carrier flow, was also investigated in the split channel poly-Si TFTs [5.9]. Figure 5.4 shows the series

resistances extracted from the channel width of (a) 10, (b) 5, (c) 2, and (d) 1 μm, respectively. To prevent the influence regarding the change in the effective channel width during the measurement, the series resistances were extracted for each single path, although the split channel poly-Si TFTs have multi paths from the source to the drain. The extracted series resistances of poly-Si TFTs having various channel widths of 10, 5, 2, and 1 μm are 1033, 1474, 1851, and 2999 Ω, respectively. However, since the multi paths in the split channel poly-Si TFTs were connected in parallel, the parallel computation of series resistance was performed and shown in Table 5.3. The resistance of source and drain regions were ignored due to the source and drain regions being heavily doped by ion mass doping. Consequently, the series resistance was significantly decreased from 1033 Ω to 300 Ω with channel splitting into 10 paths.

In order to investigate the influence of series resistance on field-effect mobility, the modified field-effect mobility's were extracted by (1) taking the series resistance calculated in parallel into account as follows:

$$I_D = \frac{W}{L} C_{ox} \mu_{FE}^{'} (V_G - V_{TH}) V_D^{'} \tag{5-2}$$

$$V_D^{'} = V_D - I_D R_S \tag{5-3}$$

$$\boldsymbol{\mu_{FE}^{'} = \mu_{FE} \frac{V_D}{V_D - I_D R_S}} \tag{5-4}$$

where V_D, I_D and R_S are the total drain voltage, drain current, and series resistance, respectively. The drain voltage drop occurs in the conduction channel of

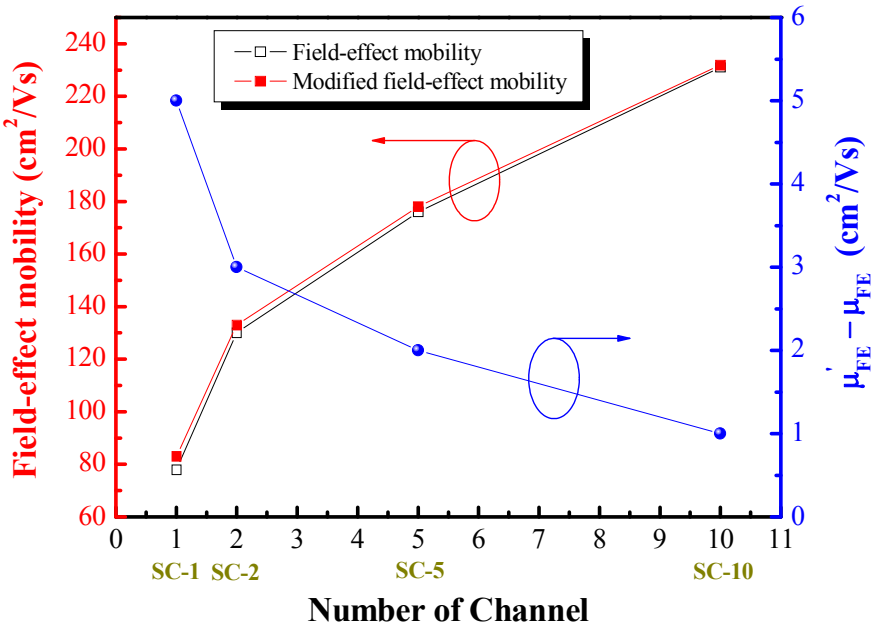


Figure 5.5 The changes of field-effect mobility and modified field-effect mobility as a function of various split channel poly-Si TFTs. The quantity of field-effect mobility degradation is also shown.

poly-Si TFTs due to series resistance. V_D' is thus the real applied voltage across the channel of poly-Si TFTs [5.7, 5.9]. Therefore, the modified field-effect mobility, which is not affected by series resistance, can be extracted as shown in Figure 5.5 (Table 5.3). The field-effect mobility and modified field-effect mobility were plotted as a function of the number of split channels, which is shown in Figure 5.5. The plots reveal that the field-effect mobility is significantly improved by channel splitting, however it can also be noticed that the field-effect mobility's are slightly degraded by series resistance. Moreover, the quantity of degradation (μ_{eff}' - μ_{eff}) is continuously reduced as the split channel becomes narrower. The reduced degradation of field-effect mobility due to series resistance means that the lower drain voltage drop occurred in the conduction channel, while the channel size and applied drain voltage

are the same. The lower drain voltage drop resulted from the qualitative improvement of the poly-Si conduction channel. Consequently, it means that the microstructures of SILC poly-Si thin-film was improved by channel splitting.

c. Trap-State Density – Crystal Filtering Effect

Generally, the microstructure quality of poly-Si thin-films and the electrical performance of poly-Si TFTs are affected by trap-states in the grain boundary and the interface between poly-Si and the gate insulator. It is well known that the Ni silicide acts as nuclei due to the lattice mismatch between the crystallized Si and Ni silicide in Ni mediated crystallization [5.10]. From these nuclei, the lateral crystallization proceeds with increasing the annealing time and temperature. The needle-like crystalline Si grain is grown towards the a-Si region with the migration of Ni silicide, and the individual crystallites from crystallized networks during lateral crystallization [5.4-5.6, 5.10-5.16].

If the Ni silicide at the front of a crystalline Si grain meets others, which have been already crystallized by the Ni silicide induced crystallization, the Ni silicide cannot migrate through the crystalline Si grains because there is no chemical potential-driving force for the phase transformation between the two crystal grains [5.13], [5.14]. Therefore, Ni silicides located at the front of the crystal is captured at grain boundaries. Furthermore, the higher Ni silicide density makes smaller grains due to it acts as the nuclear, as a result the relative grain boundary portion was increased [5.17]. It is well known that the grain boundary buildup potential barriers to the flow of carriers. As a result, electrical properties such as driving current, field-effect mobility, subthreshold slope, and threshold voltage are degraded due to the grain boundary of poly-Si has a lot of dangling bonds which are not passivated and acts as trap-states the band gap

region as well as the recombination sites. The crystal filtering method on the growth of MILC poly-Si crystals improve the electrical properties such as field-effect mobility and subthreshold slope [5.18]. The poly-Si with well-ordered crystallites was prepared by preferred filtration of poly-Si through the narrow neck of the a-Si region, because randomly grown crystallites were captured at the edge of a-Si. The crystallites grown towards the channel migrated continuously, which was previously observed from electron backscatter diffraction (EBSD) by Kim et al. [5.18]. The well-ordered crystal growth was observed as the width of the crystal filter becomes narrower. Furthermore, the field-effect mobility of crystal filtered MILC poly-Si TFTs is drastically improved by the reduction of captured Ni silicides in the channel. In this small chapter, the crystal filter effect was systemically discussed by two kinds of trap-state densities such as grain boundary and interface trap-state densities.

Grain Boundary Trap-State Density

In Figure 5.6, the density of the grain boundary trap-state, as well as the dominant source of electrical performance degradation, which is due to captured Ni silicides in the channel region, was determined using the Levinson [5.19] and Proano [5.20] method. The grain boundary trap-state density can be estimated from the slope of the linear region for the curve $\ln[I_D/(V_G-V_{FB})]$ versus $1/(V_G-V_{FB})^2$ at a low drain voltage of-0.1 V and a high gate voltage above the threshold voltage. These plots were given by equation (2-19).

where ε_{si} and ε_{ox} are the Si and SiO_2 dielectric constants. The flat band voltages (V_{FB}) were defined as the gate voltage that yields the minimum drain current at a drain voltage of -0.1 V. A lower drain voltage is better, because the channel charge is more uniform from the source to the drain. The lower slope corresponds to the lower trap

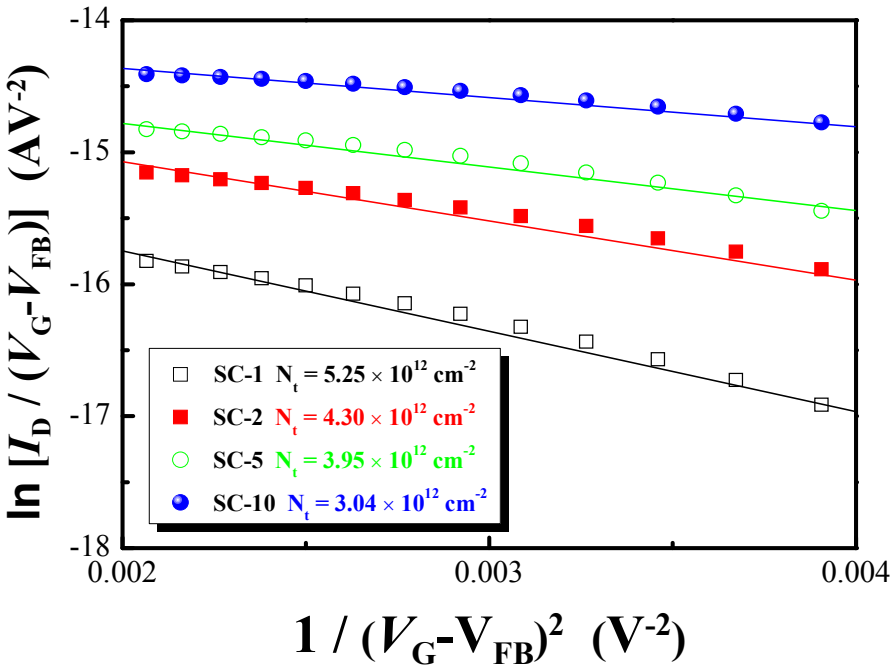


Figure 5.6 The Plots of $\ln[I_D/(V_G-V_{FB})]$ versus $1/(V_G-V_{FB})^2$ of SC-TFTs having a various number of spilt channels. The plots were determined from the Levinson and Proano method at V_D = - 0.1 V and high V_G.

density. From Figure 5.6, it is observed that the slope gradually decreases as the split channel becomes narrower; this is due to a decrease of the grain boundary trap-state density.

Interface Trap-State Density

The interface trap-state density between poly-Si and the gate insulator was determined from the subthreshold slope (S.S.) by using Dimitriadis model as follows [5.21]

$$S.S. = \left(\frac{qN_{it}}{C_{ox}} + 1\right)\frac{kT}{q} ln\, 10, \tag{5-5}$$

where q is the electron charge, k the Boltzmann constant and C_{ox} the gate insulator capacitance. It can be found that, the extracted interface trap-state density is gradually decreased as the split channel becomes narrower, due to the crystal filtering effect as shown in Figure 5.7 and Table 5.3.

The improvement of the split channel poly-Si TFTs driving current during the on-state region was shown in Table 5.3. The driving current is a combination of the drift and diffusion currents [5.22],

$$I_D = \frac{W\mu_{eff}QV_D}{L} - W\mu_{FE}\frac{kT}{q}\frac{dQ}{dx}, \tag{5.6}$$

where Q is the charge density of the mobile channel and x is the distance along the channel. Under the inversion state of p-channel poly-Si TFTs, the interface trap-states are fully positively charged [5.23], and then the mobile channel charge density is decreased with an increase of the positively charged trap-states. Thus, the charge density difference between the conventional single channel poly-Si TFTs (Q_{single}) and split channel poly-Si TFTs (Q_{split}) in the mobile channel can be expressed as

$$\Delta Q = Q_{single} - Q_{split} = -q\Delta N_{it} \tag{5-7}$$

It has been reported that the field-effect mobility is degraded by the Coulomb scattering due to the charged interface trap-states [5.22]. This is in agreement with the

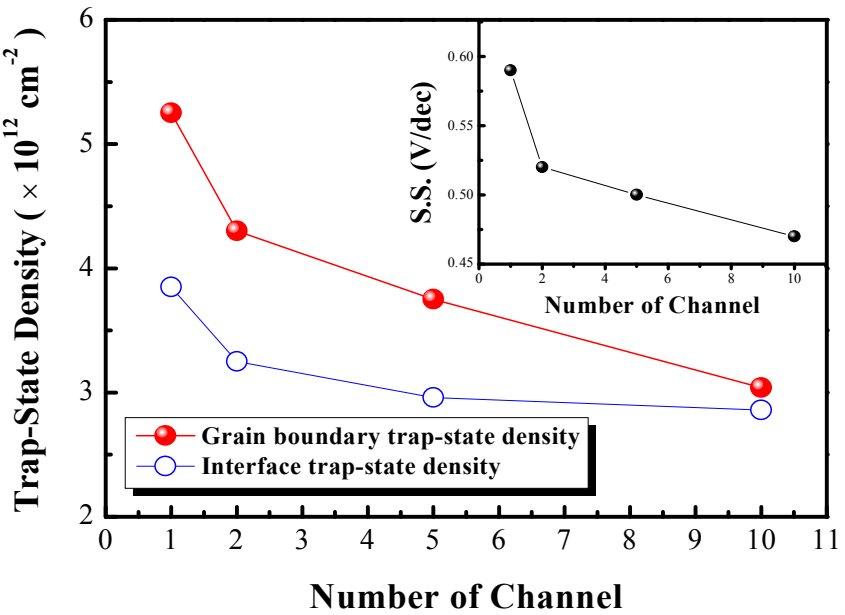


Figure 5.7 The changes of grain boundary trap-state density and interface trap-state density versus four different poly-Si TFTs (SC-1, SC-2, SC-5, and SC-10) having a various number of split channels.

experimental result that the field-effect mobility was improved approximately 3 times in case the poly-Si TFTs split into 10 channel paths, due to decrease of interface trap-states. According to an empirical model including the Coulomb scattering effect by the interface trap-state and the field-effect, mobility improvement can be given by

$$\frac{\mu_{FE-single}}{\mu_{FE-split}} = \frac{1}{1+ \alpha \Delta N_{it}} \tag{5-8}$$

where α is an empirical constant. The interface trap-states are generated regardless of the position in the channel, ΔN_{it} is not a function of x, so ΔQ is also not a function of x ($d\Delta Q/dx = 0$). As a result from the equation 5.6 ~ 5.8, ΔI_D can be

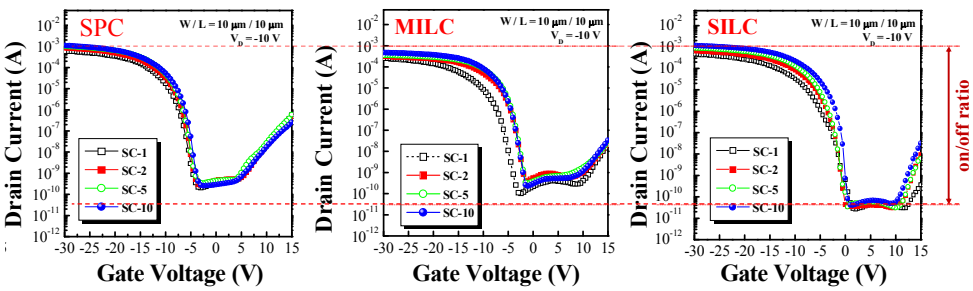


Figure 5.8 The comparison of channel splitting effect on SPC, MILC, SILC poly-Si TFT.

described as a function of ΔN_{it}. The mobile channel charge density and the field-effect mobility were increased due to the reduced interface trap-state density. Consequently, the driving current was also increased by channel splitting.

The interface trap-states act as recombination sites, which are obstacles to channel inversion during gate biasing due to the charge carriers such as electrons and holes being captured within the trap-states in the band gap region. This means that the subthreshold slope is strongly related to interface trap-state density [5.21]. From Figure 5.7, it can be seen that fewer interface trap-states are generated as the channel splitting becomes narrower. Therefore, inversion characteristics such as threshold voltage and subthreshold slope were significantly improved by channel splitting as shown in Table 5.3 and inset of Figure 5.7.

In Figure 5.8, the SPC, MILC, SILC poly-Si TFTs having split channel were compared to know what is the main mechanism of improved driving characteristics on SILC poly-Si TFT. As shown in figure, the SILC poly-Si TFT comes out highest on-state current, lowest leakage current, and best subthreshold slope among the three kind of poly-Si TFTs. The reason was analyzed and explained above chapters. Additionally, the new results can deduce by comparison. The SPC is not lateral growth of

crystallites, then the geometry effect only affect to slightly improved driving characteristics. Otherwise, the MILC and SILC was affected geometry effect and crystal filtering effect due to lateral growth of crystallites. Moreover, the effects such as geometry and crystal filtering are maximized on SILC poly Si TFT due to it has lower Ni contamination than MILC poly-Si TFTs.

5.3 Electrical Stress Effect

The electrical stress is used to investigate the reliability of the device using various stress conditions. The various electrical stress effects and mechanisms are presented in Figure 5.9. The detailed explain of electrical condition will explain in followed Table 5.4. In this chapter, however, the leakage current lowering and driving characteristics by electrical stress were discussed. Moreover, the mechanisms are analyzed using carrier trapping and de-trapping phenomenon, local electric field, and computer simulation.

5.3.1 Experimental

In this study, *p*-channel MILC poly-Si TFTs with self-aligned coplanar structure were fabricated on glass. In brief, a 3000 Å-thick-SiO_2 buffer layer and 1000 Å-thick a-Si layer were consequently deposited on glass substrates (Eagle XG; SAMSUNG Corning Inc.; size, 105 × 105 mm^2) by PECVD at 350 °C and LPCVD using SiH_4 at 500 °C, respectively. Dehydrogenation was carried out for 2 h at 450 °C in a vacuum.

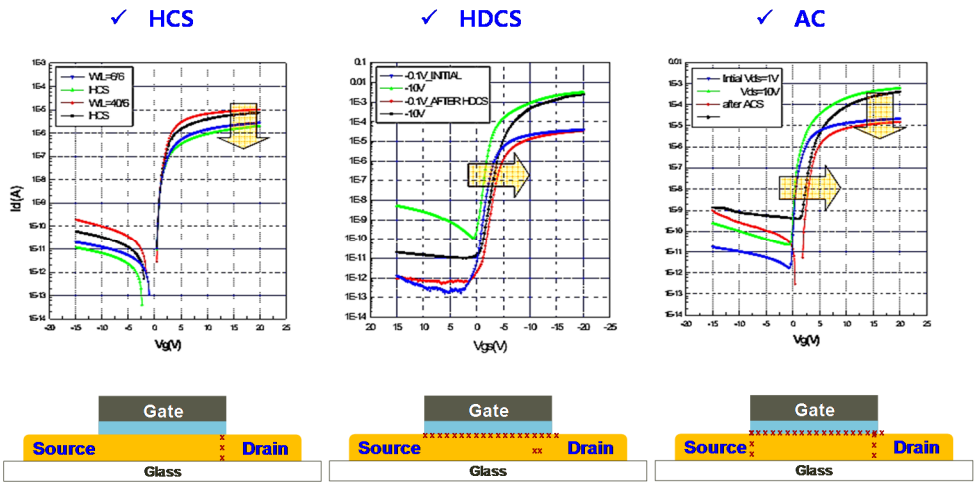


Figure 5.9 Various electrical stress effects and mechanisms. The detailed conditions are summarized in Table 5.4.

Table 5.4 Various electrical stress conditions and effects on poly-Si TFTs.

	Hot Carrier Stress (HCS)	**High Drain Current Stress (HDCS)**	**AC Stress**
Condition	$V_G = V_{TH}$, V_D = high voltage, Time = 60s	V_G = ON (20V), V_D = high voltage, Time = 60s	V_G =pulse, V_D = high voltage
Effect	Drain junction break → Series resistance↑ → μ_{FE}↓	Interface degradation due to high I_D → Charge trap → V_{TH} shift	Junction break → Interface degradation → V_{TH} shift + μ_{FE}↓
Spec	$\Delta\mu/\mu_0$ 〈 20%	V_{TH} shift 〈 1V	V_{TH} shift 〈 1V
Remarks	n-MOS	n-MOS, p-MOS	Affected during real operation

In order to define the active patterns, conventional photolithography and RIE using SF_6 gas were utilized. Ni was deposited on the source and drain areas after photolithography with an island pattern mask. Ni was sputtered at DC 700 V for 15 sec. The initial pressure was 2×10^{-6} Torr. The working pressure was 30 mTorr with

an Ar flow of 30 sccm and a throttle valve was used to keep the pressure constantly. The current was measured to be 0.5 mA and the thickness was estimated to be about 50 Å by extrapolating the straight line in a plot of thickness versus sputtering time. The lift-off method was used for the Ni island pattern. For the low Ni contamination, the Ni was removed right before the sample was put into a furnace for crystallization annealing. After crystallization annealing, the 1000 Å thick SiN_x gate insulator was deposited by PECVD using SiH_4 and NH_3 gases at 350 °C, and a 2000 Å thick MoW gate metal was subsequently formed by sputtering. The gate metal was patterned by $H_3PO_4 + CH_3COOH + HNO_3 + H_2O$ etchant and the gate insulator was etched by RIE using SF_6, Ar, and CHF_3 gases. To define the source/drain junction, the samples were doped by an IMD system using B_2H_6 source gas diluted with 80% hydrogen. The accelerating voltage and RF power were 17 kV and 150 W, respectively. After the source/drain doping, 6000 Å thick interlayer dielectrics were deposited. Then, the dopants were activated by furnace annealing in hydrogen ambient at a temperature of 550 °C for 2 h. After opening contact holes by RIE, metallization and alloying at 400 °C for 30 min were performed. The 6000 Å thick MoW was used for metallization.

Typical DC electrical stress conditions are the following. The source is grounded, the stress gate voltage is 10 V, and the drain voltage is -10 V. This means that the TFT is under off-state condition. In order to prevent the electrical stress effect during measurement, all TFTs was measured at -3 V drain voltage.

5.3.2 Result and Discussion

5.3.2.1 Stress Effect on Leakage Current on SILC Poly-Si TFTs

In *p*-channel poly-Si TFTs, the on-state current is a migration of holes from the source to the drain, collected at the TFT channel, by the electric field between the gate (negatively biased) and the substrate. The off-state leakage current, however, is formed completely differently. It is the same hole movement, but the holes in this case are not from the poly-Si active layer, rather from the positively charged defect centers in the bad gap, like the fixed charges at the interface, the positively charged defects in the gate oxide, and the hole trapping centers in the poly-Si. The fixed charges at the oxide side of the oxide/Si interface are known to be positively charged and naturally formed, balanced by the interface-trapped charges that are formed at the Si side of the oxide/ Si interface and negatively charged [5.24]. Positively charged defects in the gate insulator can generate the holes when an applied potential—typically the gate voltage, to lower the energy barrier for trapping—is high enough to liberate the holes. This reaction is not reversible, so the defects become neutral after the liberation of the holes to be injected into the Si substrate and are not capable of further hole generation at a smaller potential than that under which the holes were first liberated. Hole trapping centers in the Si are formed by capturing the holes that drift into the Si with an electric field between the source and drain. A relatively small potential is needed to generate holes from these traps. Since two mechanisms, the generation of the holes and injection into the Si, are involved in the formation of hole trap centers in Si, the amount of the trapped hole is not large, so the leakage current due to these trap centers is small at the low gate voltages.

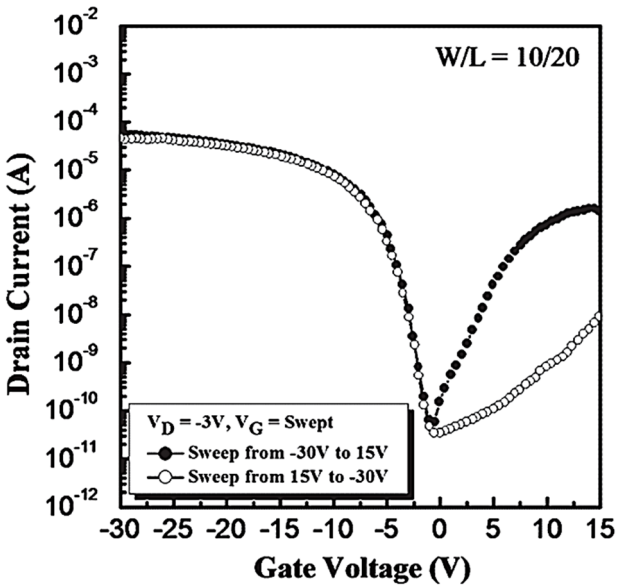


Figure 5.10 Initial I_D-V_G curves of *p*-type SILC TFT. Two different leakage currents are shown depending on the sweeping direction of the gate voltages.

Figure 5.10 shows the initial I_D-V_G curves before any electrical stress. It can be seen that the leakage current increases exponentially with the increase in V_G, but when the V_G decrease from 15 V to 0 V, the first large leakage current drops rapidly and shows a lower leakage current than that with gate voltages in the opposite direction. If positive voltages are applied to the gate, the TFT should be in the off-state and the fixed charges, which are positive and lie at the oxide side of the interface between the gate oxide and the poly-Si, would free holes to be injected into the channel. These holes should drift to the drain under the electric field between the drain, to which a negative voltage is applied, and the source, which is grounded. If a large gate voltage is applied first and decreases, all fixed charges would generate the holes

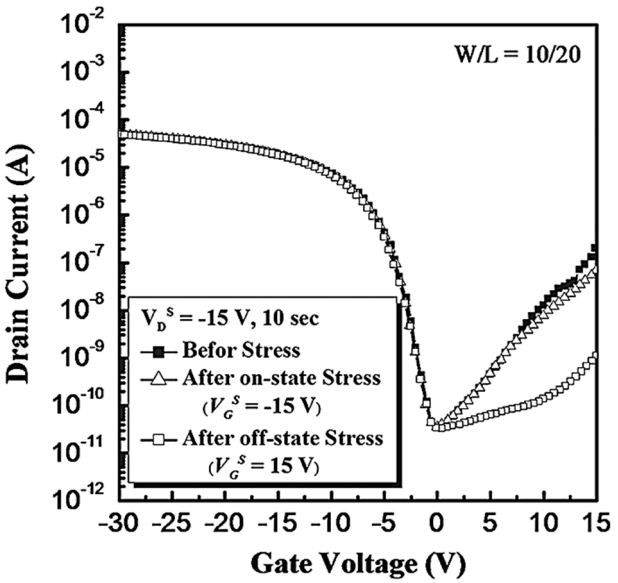


Figure 5.11 Effect of the stress conditions on the leakage current in P-type SILC TFT. The stress conditions are $V_G^S = \pm 15$ V, $V_D^S = -15$ V, for 10 sec.

simultaneously and then the resulting gate voltages, which would be smaller than the first ones, would give rise to almost no free carriers.

As can be seen in Figure 5.11, under the negative gate voltages (on-state), no stress effect is observed. However, the leakage current decreased drastically when positive gate voltages (off-state), leading to a saturated minimum leakage current. The threshold voltage, on-state current and subthreshold swing would be not largely changed by the electrical stress.

Typical electrical stress conditions are shown in Figure 5.12. and the symbols used in this chapter are showing in the Table 5.5. The electric field between the drain and the gate would allow $X+$ liberated holes to be neutral. These holes are injected into the Si and recombined at the drain; this should also happen at the source, but the electric field at the source is smaller than that at the drain, so the concentration of X should be

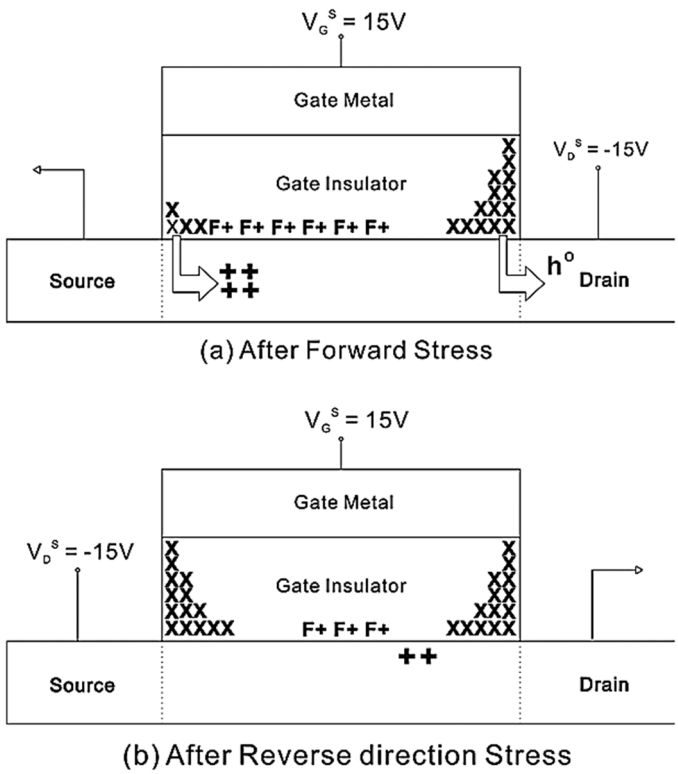


Figure 5.12 Illustration of a charge distribution (a) after the forward electrical stress and (b) the reverse electrical stress.

low at the source, as shown in Figure 5.12. The holes liberated from *X*+ at the source are injected into the Si and then drift towards the drain to form +*s*. Now, the leakage currents after the electrical stress consist of two parts, I_{leak}^{L} and I_{leak}^{H}. Here the I_{leak}^{L} comes from the generation of holes at the +*s* under a positive bias of the gate and recombination at the drain under a negative bias of the drain. I_{leak}^{H} comes from the liberation of holes at *X*+ at gate voltages larger than V_G^S.

In order to investigate effect of V_G^S, stress condition were varied. The leakage currents were measured after different V_G^S and the results are shown in Figure 5.13. It

Table 5.5 Designations for electrical stress model.

Symbol	Quantity
$F+$	The fixed charges
$X+$	Hole containing defect site in the oxide
X	Neutral defect site in the oxide
$+s$	Hole trap centers in the channel
V_D	The drain voltage
V_G	The gate voltage
V_D^S	The drain stress voltage
V_G^S	The gate stress voltage
I_{leak}^L	The leakage current at low gate voltages
I_{leak}^H	The leakage current at high gate voltages
FS	Forward stress - Negative voltage on the drain and the grounded source
FBM	Forward bias measurement - Bias the source and the drain such that holes are flowing from the source to the drain.
RS	Reverse stress - Negative voltage on the source and the grounded drain
RBM	Reverse bias measurement - Bias the source and the drain such that holes are flowing from the drain to the source

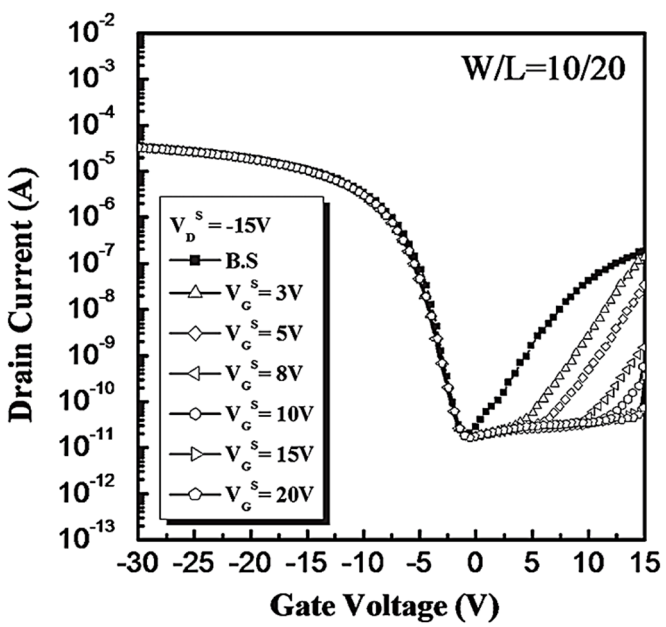


Figure 5.13 Gate stress voltage on the leakage current in P-type MILC TFT. V_D^S was -15 V and the measurement was done at V_D = -3V.

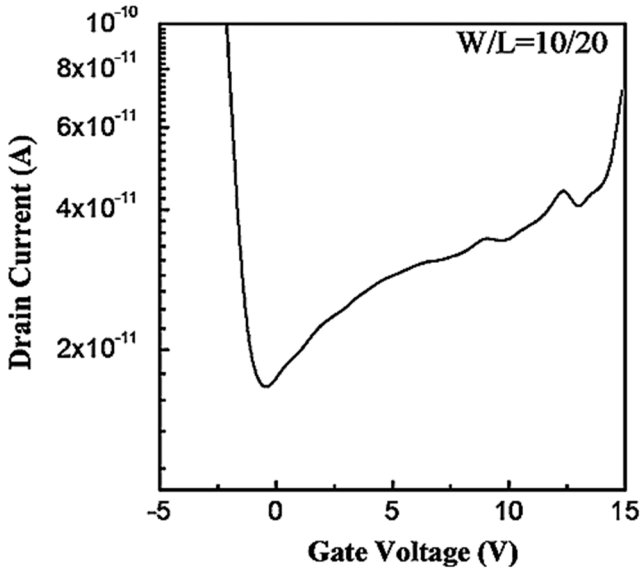


Figure 5.14 The leakage current after the electrical stress of V_D^S = -15 V, V_G^S = 20 V. The measurement was done at V_D = -3 V.

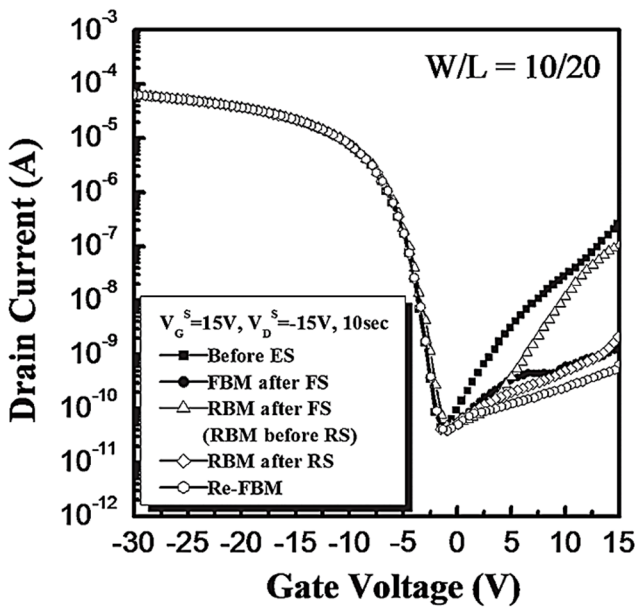


Figure 5.15 Effect of the electrical stress bias on the leakage current behavior in *p*-channel MILC TFT.

turns out gate voltage for the high leakage current, presumably caused by the holes generated at the defects in the oxide (X+) at high electric fields, is exactly the same as V_G^S. This proves that the leakage current at high V_G is due to X+ and it is important to set the V_G^S above the V_G in an operation. At low V_G, the positive trap centers (+) play a key role in determining the leakage current and the magnified version of I_{leak}^L in Figure 5.13 is shown in Figure 5.14. Note that the I_{leak}^L is concave and has a slowly increasing curve, which is in contrast to the I_{leak}^H curve. Even though I_{leak}^L is not high, the value is important because it determines the size of the leakage current in a switching TFTs.

The forward stress (FS) and the forward bias measurement (FBM) have a low leakage current, as shown in Figure 5.15. After the FS and the reverse bias measurement (RBM) show the low I_{leak}^L, it quickly catches up with the initial leakage curve. When reverse bias is applied for I_D-V_G measurements after the FS, then the F+ at the left half of the channel (the source side, which has not been greatly affected by the FS) would contribute to the large leakage current. The leakage current at the beginning is very low due to the lack of fixed charges at the vicinity of the source, as shown in Figure 5.12. The reverse stress (RS) is applied after the FS and then RBM was performed. In this case, the leakage current is quite small. A bump at the I_{leak}^L could not be observed as it could in the FBM after the first stress, because as shown in Figure 5.12 (b), there are no hole trap centers due to recombination at the source during reverse stress (the source is negative biased). Re-FBM showed the lowest leakage current, without any rapid increase of the leakage current at the gate voltage of 15 V.

According to the model suggested in this paper, as we increase the V_G of the electrical stress, the concentration of X at the source and drain increase so that the

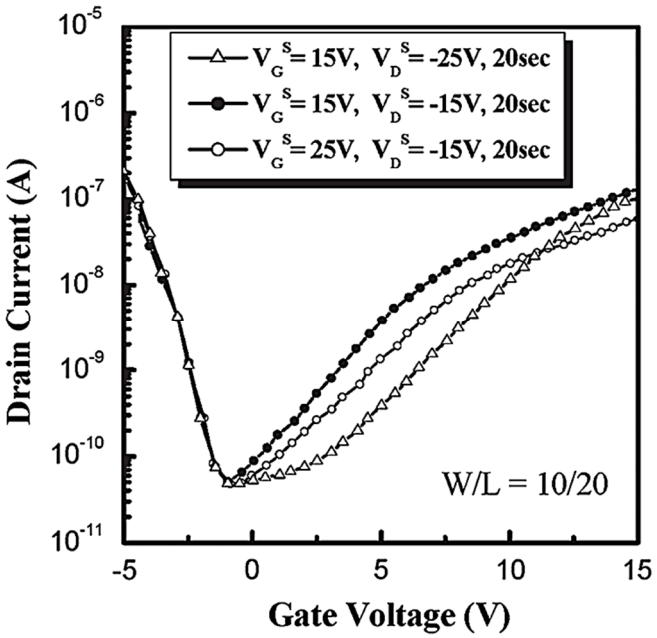


Figure 5.16 The leakage current behavior under the different stress conditions.

I_{leak}^H decreases in the RBM. In case of a large V_D, trap centers increase so that I_{leak}^L increases in the RBM. The experimental results to verify this model are given in Figure 5.16.

The standard stress conditions are V_G^S = 15 V and V_D^S = -15 V and the I_D-V_G curves under RBM are shown in Figure 5.16 (closed circle). The charge distribution after the standard stress is shown in Figure 5.12. When V_G^S was increased to 25 V with V_D^S unchanged (open circle), the leakage current at V_G = 15 volts decreased, compared with that under standard stress conditions, due to the lack of X+ centers to liberate the holes at the source. On the other hand, if V_D^S increased to -25 V with V_G^S unchanged (open triangle), then more holes can be injected into the Si to increase the number of trap centers than at a low electric field between the source and the drain, so I_{leak}^L should increase, as in Figure 5.16. Not much change can be expected at I_{leak}^H because

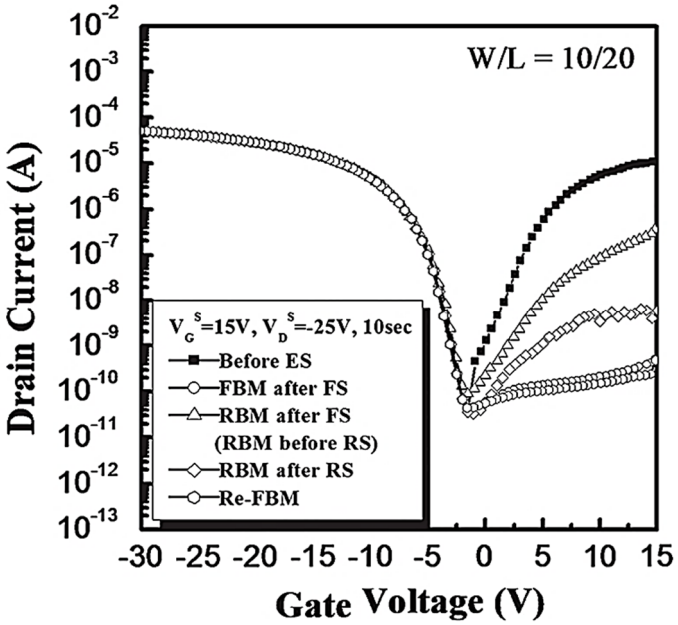


Figure 5.17 The leakage currents at the high drain voltage stress conditions.

the electric field between the source and the gate to produce X was unchanged. When the V_D^S is high, we expect to have more trap centers at the channel. If the RS is carried out after the FS, then the concentration of *X* at both the source and the drain would increase with a large number of trap centers at the center of the channel. Hence, we get a large leakage current at I_{leak}^L (due to trap centers at the channel) in the RBM after the RS and a small leakage current at I_{leak}^H (due to the lack of X+ at both ends). This was observed in the experiment, as shown in Figure 5.17.

In order to maximize the electric field to generate the trap centers in the channel, the source and the gate are connected and 15 V was applied during the electrical stress. In this case, we do not have any *X* at the source and 30 V between the gate and the drain gives rise to a large number of trap centers in the channel. The results are shown in Figure 5.18.

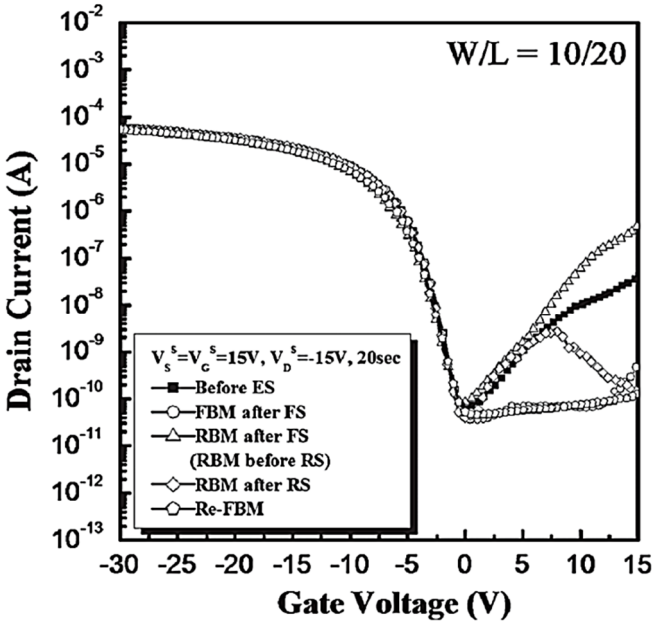


Figure 5.18 The leakage current behavior when the gate and the source are connected.

The FBM would show a low leakage current because 30 V exists between the gate and the drain to produce a large number of X at the drain. A relatively large I_{leak}^{L} can be seen in Figure 5.18 due to the increase of $+s$ in the channel, but not significant effect in the FBM. However, in the RBM after the stress, a large increase of I_{leak}^{H} can be observed due to the large number of $X+$ at the source (since no electric field was applied during the stress between the gate and the source). A large increase in the I_{leak}^{L} can also be observed because the trap centers created during the stress render the holes to make I_{leak}^{L} large. If the RS is followed by the FS, then both ends would contain a large number of X so that a small I_{leak}^{H} can be expected. As can be seen in Figure 5.18, the leakage current of the RBM shows rapid increase in the I_{leak}^{L} (due to $+s$ in the channel) and decreases rapidly afterwards (due to the lack of $X+$ at both ends of the

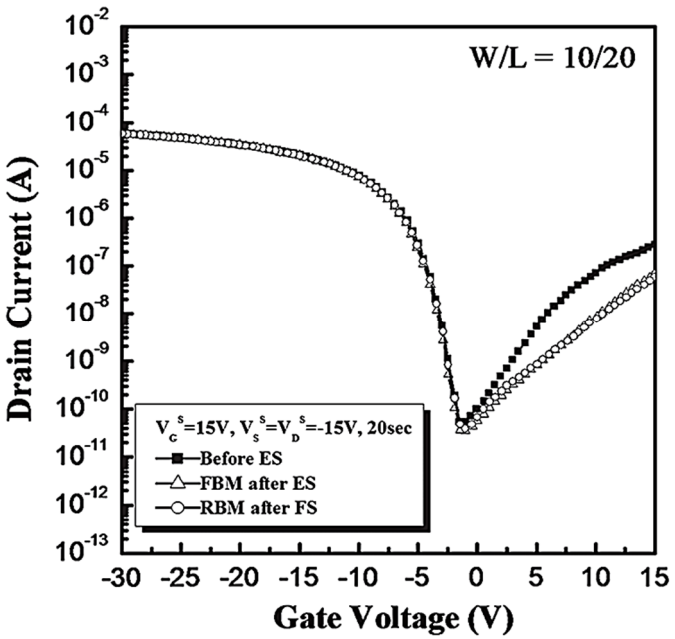


Figure 5.19 The leakage current behavior when the source and the drain are connected.

channel). Since the trap centers in the channel are deprived of the holes during the RBM, Re-FBM shows a low leakage current (see Figure 5.18).

If the source and the drain are connected, a large concentration of *X* at both ends is created due to the high electric field, but there will be no hole to be trapped in the channel due to the absence of an electric field between the source and the drain. The leakage current comes from the fixed charges at the oxide side of the interface, which liberate the holes by the gate voltage and inject them into the Si. The leakage current is not directional and is slightly less than that of the initial measurement, as can be seen in Figure 5.19.

5.3.2.2 Stress Effect on Driving Characteristics on SILC Poly-Si TFTs

Figure 5.20(a) shows the I_D-V_G transfer characteristics before and after electrical stress for various V_D^S. The V_D^S was varied from -1 to -40 V and the V_G^S was fixed at -10 V. The electrical stress time was also fixed for 10 sec. It can be found that the threshold voltage, subthreshold slope, and minimum leakage current were not changed by electrical stress. But, the off-state leakage current in high reverse gate bias was proportionally decreased with increase of V_D^S. The result of unchanged threshold voltage and subthreshold slope indicated that the electrical stress was not affect to gate insulator layer, however, the lowered leakage current means that the poly-Si active layer was affected by electrical stress. These results were already analyzed by previous report of our research group [2.25, 2.26]. Figure 5.20(b) shows the magnified curves of on-state current region. As shown in the Figure 5.20(b), the on-state current was consistently increased with increase of V_D^S.

The exact value of on-state current change is plotted in Figure 5.21 (red circle). The on-state current change versus electrical stress time relationship also presented in the Figure 5.21 (blue square). In order to obtain the Figure 5.20 and 5.21 results, the measurement and electrical stress procedures are the following. First, the initial I_D-V_G transfer characteristic was measured. The 0.7 V/dec of *SS*, 7 V of V_{TH} and the 63 cm^2/Vs of field effect mobility (μ_{FE}), which were determined using an equation for the linear region, were obtained. Next, the DC electrical stress (V_D^S = variation from -1 V to -40 V and V_G^S = 10 V; off-state condition) was applied. During the DC electrical stress, the hot electrons might not be injected from the drain to gate insulator but active poly-Si. The SS and V_{TH} were not altered, while the leakage current and on-state current were changed, which result can support the hypothesis of hot electron

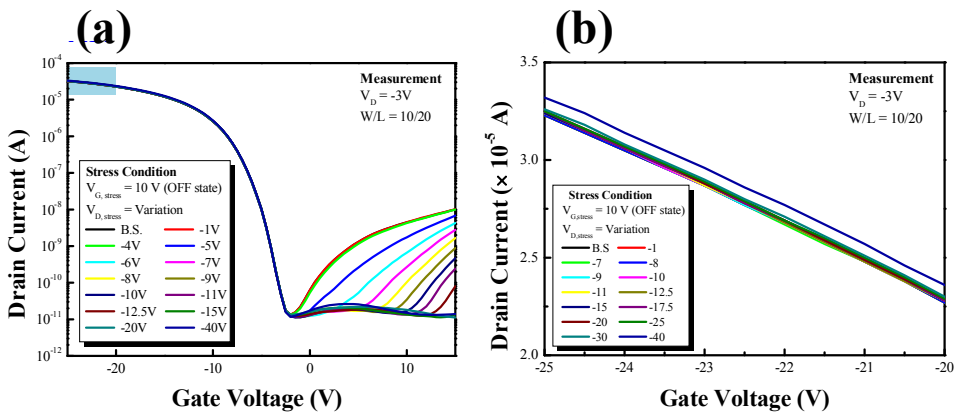


Figure 5.20 Changes of I_D-V_G transfer characteristics before and after electrical stress for various stress drain voltages. The magnified curves of on-state current are shown in (b).

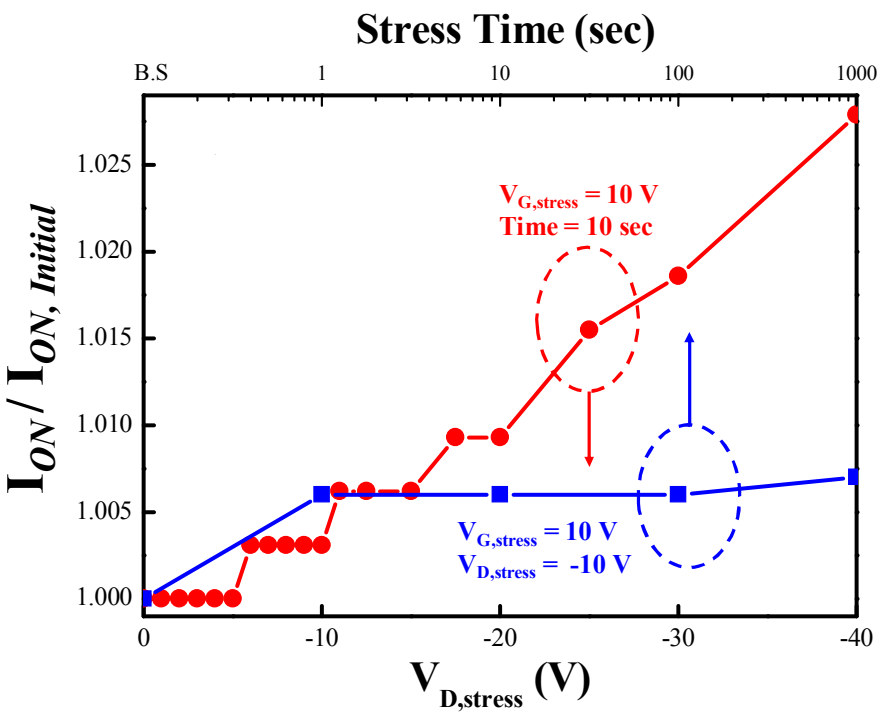


Figure 5.21 The on-state current changes as functions of stress drain voltage (red circle) and time (blue square).

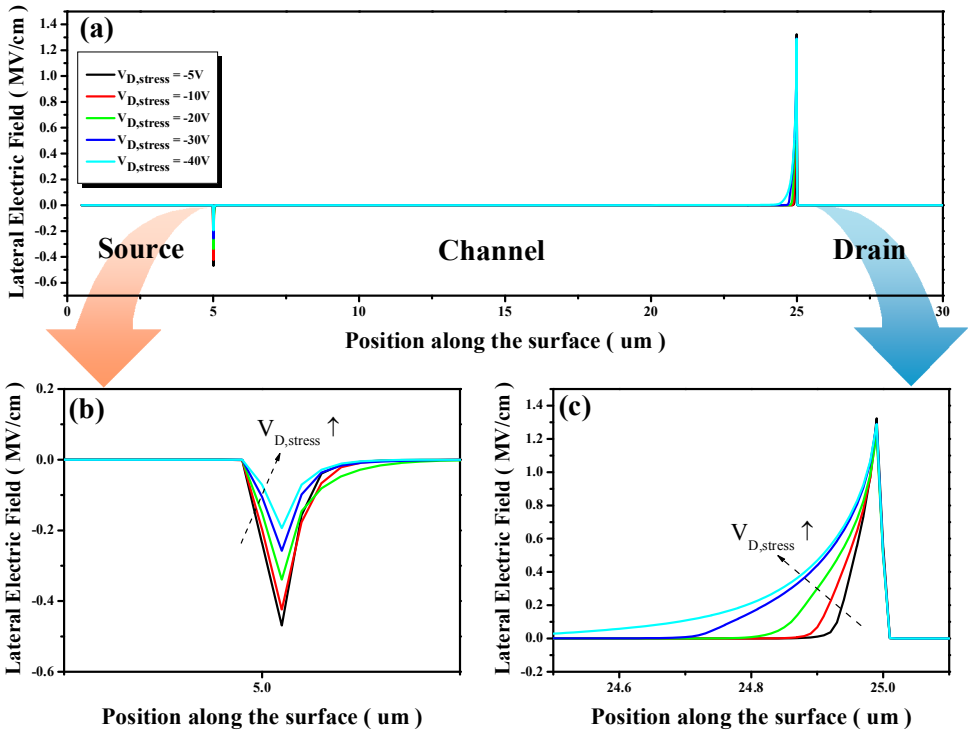


Figure 5.22 Computer simulation (ATLAS) of the electric field distribution along the channel during electrical stress.

injection to active poly-Si. Finally, the changed I_D-V_G transfer characteristic was measured after electrical stress time of 1, 10, 100, and 1000 s. Consequently, the I_D-V_G characteristics and I_D - electrical stress time relationships were obtained. From the Figure 5.21, it can be noticed that the electrical stress effect is rapidly occurred within the 1 s. The phenomena of the off-state leakage current suppression and the on-state improvement were already reported in MOSFETs [5.27]. These results can be explained by a reduction of the effective channel length since hot electrons were trapped in active poly-Si.

In order to explain the experimental results, the mechanism of the improvement was analyzed through a 2-D computer simulation (ATLAS) [5.28]. The Figure 5.22(a) shows the lateral electrical field distributions during various electrical stress conditions. The lateral electric field distributions of source/channel and channel/drain junctions are magnified in Figure 5.22(b) and (c), respectively. From the results, it can be clearly noticed that the absolute value of electric field at source/channel junction is much lower than that of channel/drain junction due to when electrical stress applying, forward bias is applied at source/channel junction while, reverse bias is applied at channel/drain. In addition, the distance of lateral electric field from source to channel was not altered with increase of electrical stress. But, in the channel/drain junction, the distance of lateral electric field was expanded from drain to channel with increase of electrical stress although the intensity of electric field is decreased due to voltage drop. This results means that the hot electron is injected from drain to channel till zero lateral electric field in the channel.

The correlation between hot electron injection and effective channel length shortening mechanism is explained in the Figure 5.23 on the basis of the simulation results. During typical DC electrical stress (V_D^S = -10 V and V_G^S = 10 V; off-state condition for 10 sec), the hot electrons are injected from drain to active poly-Si and the injected hot electrons are trapped in the active poly-Si surface, because positive V_G^S is applied during electrical stress. The evidence covering to support the hypothesis is explained in next paragraph. Then the injected electrons induce the local electric field to accumulate the holes from the active poly-Si. The region accumulated holes near the drain junction act as an extended drain. Then the effective channel length is reduced by extended drain. If electrical stress field increases, the distance of lateral

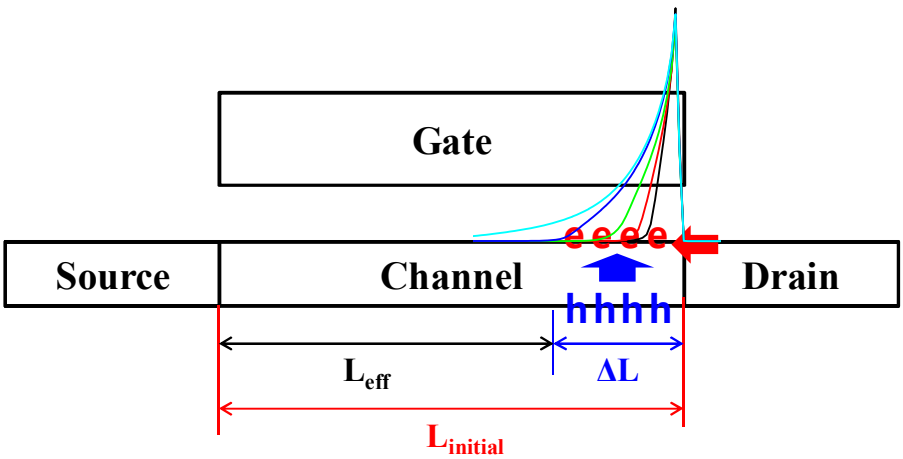


Figure 5.23 Illustration of on-state current increase mechanism which is hot electron induced channel length shortening during the electrical stress.

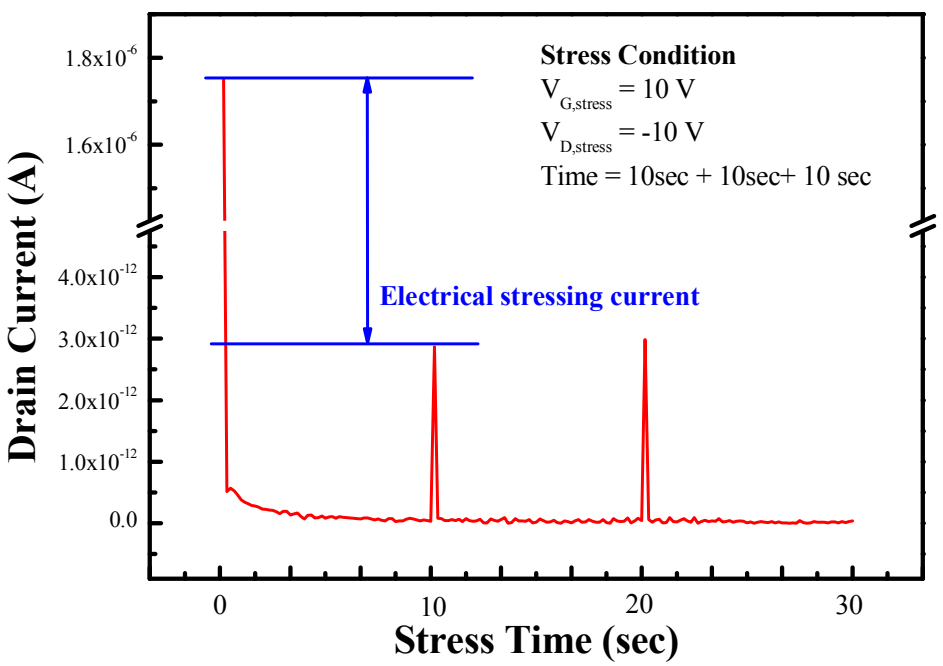


Figure 5.24 Drain current measurement with pulsed electrical stress for three times. Every electrical stress was applied for 10 sec.

electric field extend and drain region also extends, then the effective channel length decreases.

Figure 5.24 shows the drain current during pulsed electrical stress for 10 sec, three times. At the first electrical stress, the drain current was decreased from much higher than that of second within 1 sec. But when the second electrical stress applying, electrical stress drain current was not high as much as first electrical stress.

This result means that the difference of electrical stress drain current between first and second is resulted from hot electron injection from drain to active poly-Si. Additionally, when the third electrical stress was applied, the electrical stress drain current was not different compared with that of second. The result indicates that the injected hot electrons were not depleted but trapped in the active poly-Si.

In order to confirm the lateral electric field decrease, I_D-V_D output characteristics were measured as shown in Figure 5.25 In general, output characteristics of poly-Si TFTs show, at high drain voltage, an anomalous drain current increase, often called the "kink effect" in analogy with SOI devices [5.29]. The kink effect is caused by impact ionization at the junction between channel and drain, due to the large lateral electric field when the device is operating in saturation. From the Figure 5.25, it can be noticed that the kink effect is suppressed after electrical stress compared with before electrical stress. This result means that the electrical stress can lower the lateral electric field.

Figure 5.26 shows the C-V curves before and after stress. The minimum capacitance at V_G > - 5 V exhibited a rather larger capacitance between the gate and the drain (C_{GD}) after electrical stress than before stress. However, the capacitance between the gate and the source (C_{GS}) value was not altered by the application of electrical stress since the charge trapping as well as hot electron injection occurred

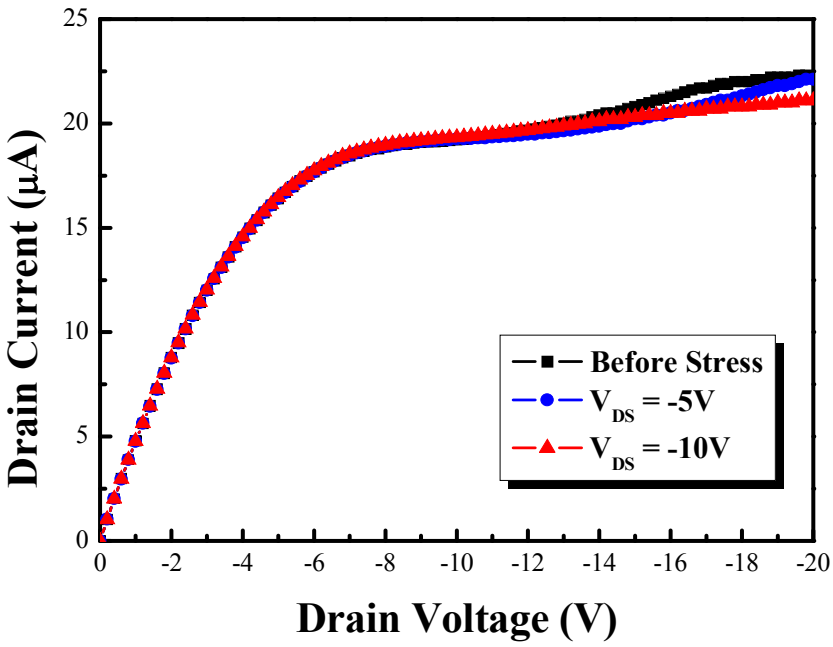


Figure 5.25 I_D-V_G output characteristics of poly-Si TFT before and after electrical stress. The electrical stress was applied at V_G = 10 V and V_D = -5, -10 V respectively.

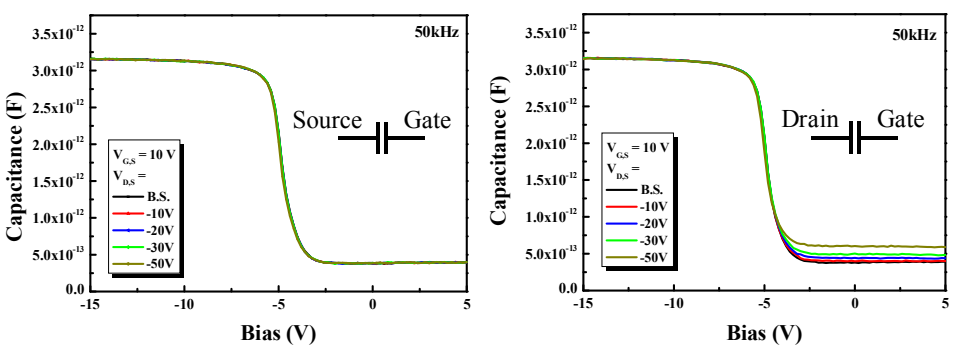


Figure 5.26 *C-V* curves of poly-Si TFT after electrical stress with various V_{DS}. (a) Gate to source capacitance. (b) Gate to drain capacitance.

near the drain junction. The increase in the C_{GD} value with increase of electrical stress field was attributed to the increased overlapped capacitance caused by the hot electron injection and drain region extension. [5.27] In case of p-channel poly-Si TFTs, the activation energy of hole to inject into the channel is about 4.3 eV that is larger than that of electron (3.2 eV). [5.30] This means that the probability of the electron trapping is rather larger than the hole trapping. And the electrical properties changes are occurred only p-channel poly-Si TFTs. In the future, we will report the electrical properties change in n-channel poly-Si TFTs.

CHAPTER 6

Conclusion and Future Work

6.1 Summary of Results

SILC, a new processes, were investigated to reduce the leakage current of MILC poly-Si TFTs by reducing the metal contamination in channel area. Also, the LDD structure was investigated to suppress the leakage current at high reverse bias regime. Moreover, the gettering process was demonstrated to remove the trapped Ni silicide on the channel surface. In order to achieve high performance poly-Si TFT, not only reduction of the leakage current but also improvement of driving characteristics such as the on-state current, the field-effect mobility, the threshold voltage, and the subthreshold slope were investigated through the split channel structure and electrical stress. From the results and discussion given in previous chapter, the following conclusions were made:

The a-Si thin film could be crystallized by SIC whose the catalyst for crystallization is Ni silicide instead of Ni thin film. The Ni silicide was formed by removal of Ni thin film by H_2SO_4 right after Ni sputtering at room temperature. By using the Ni silicide,

the minimum metal (Ni) catalyst was used during crystallization. Therefore, the trap states in the band gap of poly-Si were effectively reduced.

When the a-Si is crystallized by the SIC, good crystallinity and smooth surfaces are achieved. The electrical properties of SIC poly-Si TFTs fabricated with the seed are similar to MILC poly-Si TFTs and compared to the conventional MIC poly-Si TFTs, a vast improvement is seen. From the results, we conclude that the SIC method using silicide reduces the Ni concentration in the surface of the poly-Si thin films, resulting in lower leakage current and higher field-effect mobility, compared to MIC poly-Si TFTs. The Ni silicidation density was increased with *in-situ* silicidation temperature, and the higher silicide density makes smaller grains, and as a result the relative grain boundary portion was increased. The Ni silicides such as Ni, Ni_2Si, NiSi, and $NiSi_2$ were captured at the grain boundaries. The Ni silicides at the grain boundaries formed trap-states in the band gap of poly-Si, and acted as the major cause of degradation of the electrical performance of the SIC poly-Si TFTs. Especially, the on-state current, field effect mobility, leakage current, and subthreshold slope were significantly degraded due to the high trap-state density produced by *in-situ* silicidation at higher temperatures.

When a-Si is crystallized by SILC, the Ni concentration of the lateral crystallized poly-Si region is considerably reduced compared to that of MILC. Due to the lower Ni silicide concentration, the silicide seed-induced laterally crystallized poly-Si has good crystallinity and a higher crystalline fraction. In addition, it can be noticed that the interface trap density of the poly-Si thin film crystallized by SILC is lower than that of the poly-Si thin film crystallized by MILC due to the lower Ni silicide concentration. The electrical properties of SILC poly-Si TFT fabricated with the silicide seeds were effectively improved compared to those of conventional MILC

poly-Si TFT. It can also be noticed that the leakage current is more sensitive to the drain voltage in MILC poly-Si TFT than in SILC poly-Si TFT, while there is no significant difference in the on-current behavior between these two TFTs. These results prove clearly that the SILC poly-Si TFT has a lower interface trap density than that of the MILC poly-Si TFT. The poly-Si TFTs produced by the SILC process do not require additional mask steps and have good electrical characteristics compared with conventional MILC poly-Si TFTs.

The effectiveness of this gettering process has been proved by fabrication of gettered MIC and SIC TFTs, comparing non-gettered TFTs. Especially, the gettered SIC poly-Si TFTs affords a lower leakage current and wider on/off ratio by reducing the trap-state density in the channel and improving the quality of the channel/drain junction.

The Poly-Si TFTs with SSBs ejected from the channel were fabricated. It was discovered that the SSB is responsible for the off-state high leakage current and low field-effect mobility. By ejecting the SSB from the channel, the off-state leakage current and on-state current and field-effect mobility were improved compared with the conventional symmetrical poly-Si TFT with the SSB in the center of the channel. Moreover, the drain current noise was also improved by the removal of SSB from channel, since it acts as a scattering source.

The SILC poly-SI TFT having LDD structure was fabricated by gate insulator doping mask (GIDM) method. By using LDD structure, the lateral electric field at junction between channel and drain was efficiently decreased. Therefore, leakage current at high reverse bias regime was effectively reduced.

The SILC poly-Si TFTs having a split channel along the carrier flow direction were fabricated. It was observed higher driving current and field-effect mobility along with

better inversion characteristics such as threshold voltage and subthreshold slope compared to the conventional single channel poly-Si TFT fabricated by SILC. The enlarged effective channel width, reduced series resistance, lower grain boundary density by crystal filter during crystallization, and lowered interface trap-state density were determined as the causes for the improved electrical performance. Since the proposed poly-Si TFTs having split channels does not require a different process compared with conventional SILC poly-Si TFTs fabrication processes, it can be easily applicable to potential future flat panel display applications.

In order to investigate the electrical stress effect on SILC poly-Si TFT, *p*-channel top-gate SILC poly-Si TFTs was fabricated and various gate, drain, and source bias as electrical stress were applied prior to I_D-V_G measurement. After electrical stress, it was found that the lowered leakage current at high reverse bias, the increased on-state current and field-effect mobility with electrical stress field without the changes of gate insulator interface properties such as threshold voltage and subthreshold slope.

The initial leakage current, which stems from the fixed charges at the interface of the gate oxide and the Si, showed a hysteresis upon the direction of the gate voltage application. A plausible model has been suggested to explain the experimental results. Under the proper bias between the gate and the source or the drain, the defects in the oxide may generate and inject the holes into the drain or the source to become neutral, which can keep the leakage current low at high gate voltages. The electric field between the source and the drain works to create the hole trap centers in the channel, which may deliver the holes to form the leakage current at the low gate voltages. It appears that the stress gate voltage determines the onset of the gate voltage for the high leakage current, so it is important to maintain the stress gate voltage higher than the gate voltage in operation.

The drain avalanche hot electron effect plays a reduction of effective channel length since extension of drain region with local electric field by injected hot electron during electrical stress. This phenomenon is analyzed and confirmed by device simulation based on the model considering the electron trapping. Moreover, the capacitance measurement was carried out to support the effective channel length reduction model.

6.2 Future Works and Suggested Research

In this study, the high performance SILC poly-Si TFTs having lower leakage current and better driving characteristics such as the on-state current, the field-effect mobility, the threshold voltage, and the subthreshold slope than those of conventional MILC poly-Si TFTs. The dot shape Ni silicide instead of Ni thin-film was applied for reducing the Ni contamination in poly-Si thin film.

Compared with conventional MILC method, the process of SILC method was not changed but the sequence of fabrication. Therefore, the research should concentrated on the SIC method which can drop the Ni mask step.

The dot shape Ni silicide was formed by removal by dipping into the H_2SO_4 right after Ni deposition using sputtering, thus control of the silicide density and location were almost impossible. If we can control the location and density of Ni silicide on the a-Si by using another method, such as photolithography and imprinting, we could demonstrate the optimum process architecture of poly-Si TFTs having better uniformity and electrical performance. Furthermore, the non-vacuum process to determine the location of silicide should be realized.

Appendix A

Ni-Si Solid-State Reaction

SILICIDES are compounds of a metal (M) and Si. For microelectronic applications, thin silicide layers are generally produced via solid-state reaction of a thin layer of M, deposited on a Si substrate. Generally, the as deposited combination of these two materials (M and Si) is not in thermodynamical equilibrium (Figure A.1). Heating provides the required energy for the system to overcome the energy barriers for solid-state reaction. Intermediate silicides form, driven by the need of the system to finally achieve a silicide/ Si combination in thermodynamical equilibrium. In thin films, the reaction between M and Si usually results in the sequential formation of various M_xSi_y phases (Figure A.2). Because of the higher mobility of metal (or lower mobility of Si), metal rich phases are usually expected to form first, followed by Si rich phases. Depending on the required silicide properties, the heating conditions to which the M/Si system is subjected, are adapted in order to select the desired silicide compound.

The formation of a new compound is dictated by two mechanisms: its initial nucleation (related to thermodynamics, the driving force for the reaction to occur), and further growth of this compound (which is related to diffusion kinetics). Both effects

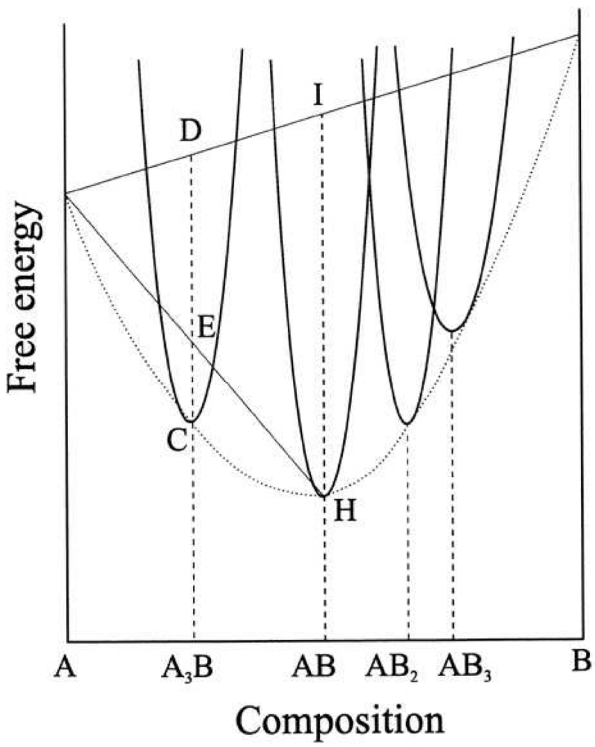


Figure A.1 The parabolic variation of free energy as a function of composition for several phases in an A/B binary system at a temperature T [A.1]. The system A/B is not in thermodynamical equilibrium. Upon heating, the system will form intermediate phases in order to lower its free energy. The presented system is representative for a typical M/Si system.

should be considered when analyzing the compound formation. In general, one of these two mechanisms (thermodynamics, or kinetics) will be the mechanism that limits or *controls* the compound formation, and the reaction is called either *nucleation controlled* or *diffusion controlled*. Generally, diffusion limited reactions are preferred above nucleation controlled reactions, as diffusion of atoms is generally slower and therefore easier to keep under control in a process.

A.1 Diffusion

A.1.1 Diffusion Equation

When discussing atomic diffusion, the first equation that comes to mind is Fick's equation, relating the atomic flux J_A of a species A to an atomic concentration gradient dc_A/dx as

$$J_A \propto D_A\left(-\frac{dc_A}{d_x}\right) \tag{A-1}$$

with c_A [at./m^3] the (local) concentration of species A, and D_A [cm^{2}s^{-1}] the diffusion coefficient. The latter expresses the extent to which a specific species diffuses through a specific phase, and depended strongly on temperature through:

$$D(T) = D_0 \cdot exp\left(\frac{-\Delta G_{kin}}{kT}\right) \tag{A-2}$$

with ΔG_{kin} the activation energy for diffusion, and k the Boltzmann factor.

In case of silicide growth, problems arise with the interpretation of equation A-1. The concentration gradient $\frac{dc_a}{dx}$ is (1) not known, (2) likely extremely small (as silicide are usually strict stoichiometric compounds), and (3) its temperature dependency is not known [A.2].

In general, an atomic flux can be written in the form of

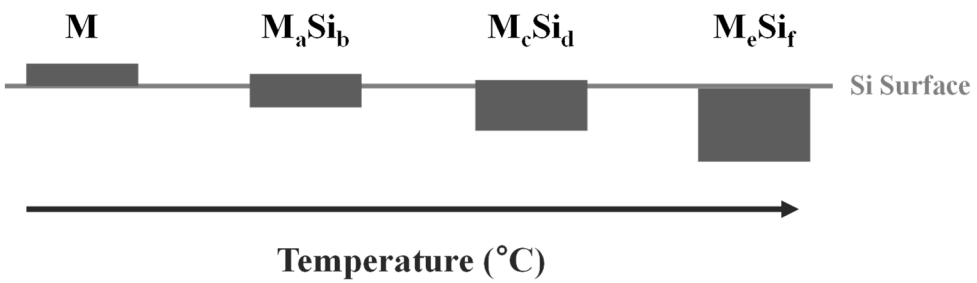


Figure A.2 Simplified representation of the sequential formation of intermediate M_xSi_y silicide phases upon heating of a metal (M) deposited on a Si substrate. Generally, Si is consumed and the sequential silicides are more Si rich.

$$\text{Flux} = (\text{concentration}) \cdot (\text{mobility}) \cdot (\text{driving force}) \qquad \text{(A-3)}$$

Based on this intuitive concept, a better representation of J_A in case of silicide growth, is provided by the Nernst-Einstein equation:

$$J_A = c_A \frac{D_A^{n.e.}}{kT}\left(-\frac{d\mu}{dx}\right) \qquad \text{(A-4)}$$

This equation represents the atomic flux J_a [at.m^{-2}s^{-1}] in relation to the actual driving force that causes atoms to diffuse i.e. a reduction of the chemical potential μ, represented by the gradient dμ/dx [eV/m]. The factor $D_A^{n.e.}/kT$ then represents mobility, with $D_A^{n.e.}$ the Nernst-Einstein diffusion coefficient (in general $D_A^{n.e.} \neq D_A^{f.}$, unless there is no interaction between both A and B species). It can be shown that equation A-4 reduces to equation A-1, in the case that one is dealing with an ideal mixture of species A and B (which implies the assumption of no interaction between

the species). With the assumption that there is no concentration gradient, J_a, $D_A^{n.e.}$, and c_A are then constants; from equation A-4, the chemical potential gradient should then also be constant. By integration over the full layer thickness, J_A can then be written as

$$J_A = -c_A \frac{D_A^{n.e.}}{kT}\left(\frac{\Delta G_A}{l}\right) \tag{A-5}$$

In which l represents the total thickness of the layer that is to be diffused through; ΔG_A represents the gain in free energy per mobile atom A that reacts into the daughter compound (i.e. $\Delta G_A = \Delta G/p$ in case of growth of A_pB_q). The factor c_A represents the total number of A atoms per unit volume in the growing phase (i.e. $c_A = C{\cdot}N$, with C the relative concentration of the A atoms per molecule of the new phase (for instance $\frac{p}{p+q}$ in case of growth of A_pB_q) and N is the total number of atoms per unit volume).

A.1.2 Single Layer Growth

The above equation for the flux in an atomic layer through a thin film can now be used to model the evolution of the thickness of a growing silicide layer. For simplicity we focus on a two-phase system of a film M deposited on a Si substrate. A single daughter phase M_2Si forms through the reaction $2M + Si \rightarrow M_2Si$, driven by a decrease in energy ΔG per mole of formed M_2Si (see Figure A.3). As soon as a lateral layer of this daughter phase has formed, no direct contact between the unreacted M species

and Si substrate exists anymore; for further growth to proceed, one of the reacting species necessarily has to diffuse through the formed M_2Si layer. Depending on which

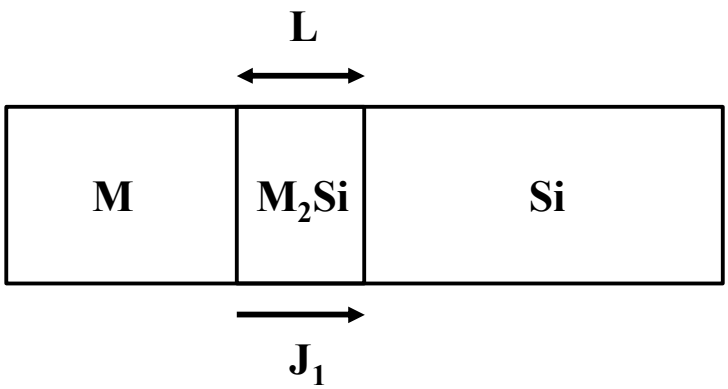


Figure A.3 Representation of diffusion controlled growth of phase M_2Si, by reaction of a metal M and substrate Si. M is the most mobile species and diffuses through the phase (with increasing thickness L) to the M_2Si/Si interface resulting in systematic further growth of M_2Si. J_1 represents the flux of atoms through the layer.

element is most mobile in the M_2Si layer, either M diffuses toward the M_2Si/Si interface, or Si toward the M/M_2Si interface. The diffusion coefficients of M and Si through M_2Si are respectively represented by D_M and D_{Si}.

Generally, one of the species diffuses faster through the phase than the other one. Suppose M is in our case the fastest diffusing species, i.e. $J_M >> J_{Si}$. The growth of the phase with time then directly relates to the flux of M atoms through

$$\frac{dL}{dt} = \Omega J_M \upsilon_M \tag{A-6}$$

in which L represents the M_2Si thickness, and υ_M represents the growing film volume

increase per transferred atom M i.e. $\upsilon_M = 1/c_M$. The geometrical scale factor Ω relates the diffusion coefficient to the thickness of the growing film. Combining equation A-5 and A-6 leads to

$$\frac{dL}{dt} = \Omega \frac{-D_M \Delta G_M}{kT} \frac{1}{L} \tag{A-7}$$

When solving this equation, the film thickness l evolves with time t as

$$L^2 = \Omega K t \qquad \text{with} \qquad K = 2\alpha_M = -2D_M \frac{\Delta G_M}{kT} \tag{A-8}$$

The value of α_M (which is > 0 since ΔG_M < 0) is called the *diffusivity*.

The silicide layer thickness caries as the square root of time. The parabolic law is characteristic of diffusion controlled growth and shows good agreement with experimental observations. It can be understood that according to this theory, mathematically, an infinitely thin layer (such as at the initial stage of formation) implies an infinite increase of the film growth rate (which is physically impossible). This problem can be circumvented with the aid of a mathematical trick; the reader is referred to excellent considerations in literature on this topic [A.2]. Consequently, the initial stage of the silicide growth is believed to occur at a slower rate; diffusion controlled silicide growth is then said to follow *linear-parabolic* kinetics.

A.2 Classical Nucleation Theory

A reaction is nucleation controlled, when the thermodynamically driven reaction itself limits the compound formation. Somewhere in between the phases that are already present in a system, small nuclei of a new phase are formed. This concept is well-known in case of the solidification of a liquid (crystallization).

The main condition for nucleation to be reaction-rate controlling, is that the change in free energy ΔG associated with the reaction (i.e. the driving force for the phase transition) is small. If this change in free energy ΔG is expressed per unit volume, the creation of a nucleus with radius r induces a change in free energy proportional to $ar^3\Delta G$, where a is a geometrical factor that describes the shape of the newly formed nucleus. On the other hand, the formation of a nucleus requires the creation of new interfaces, resulting in an energy cost. The change in interface energy $\Delta\sigma$ is expressed per surface unit; the total cost required for the nucleus formation is given by $br^2\Delta\sigma$ in which b is again a geometrical factor.

The total free energy change associated with the creation of the nucleus is then given by

$$\Delta G_n(r) = -ar^3\Delta G + br^3\Delta\sigma \qquad \text{(A-9)}$$

The sign of both terms explicitly expresses the difference in the respective 'gain' and 'loss' of energy.

Figure A.4 shows a graphical representation of the change in free energy as a function of the radius of the formed nucleus (equation A-9). If the formed nucleus of

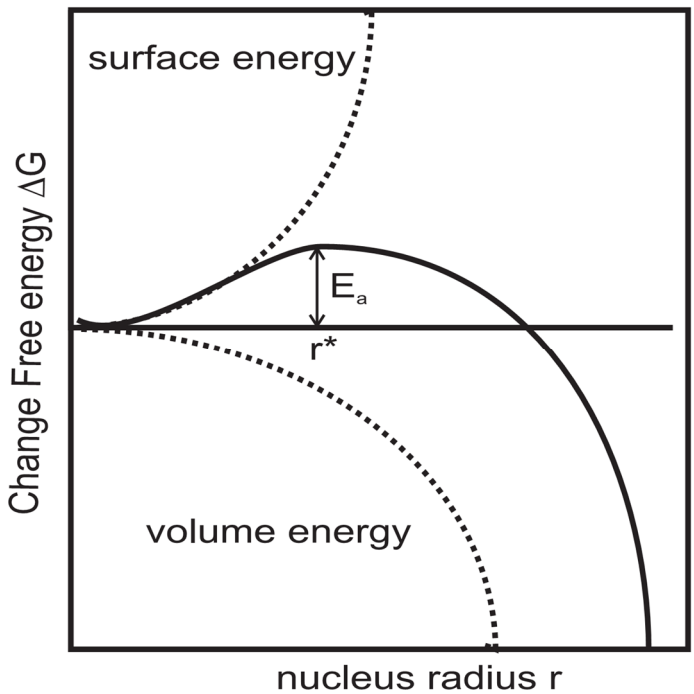


Figure A.4 Graphical representation of the energy balance associated with formation of a nucleus with radius *r*.

the compound is small ($r < r^*$), it is thermodynamically unstable, as the maintenance and further growth of the new phase requires more energy. Such nucleus can only temporarily be formed by a thermal fluctuation of the system. Yet, when the radius of the initially formed nucleus exceeds the critical radius r^*, the system can lower its energy by further increasing the nucleus radius, thus giving rise to the systematic further growth of this new phase. One can calculate this critical radius r^* and the nucleation activation energy ΔG^*, by differentiation of equation A-9:

$$r^* = \frac{2\Delta\sigma}{\Delta G} \tag{A-10}$$

$$\Delta G^* = \frac{16\pi(\Delta\sigma)^3}{3(\Delta G)^2} \propto \frac{(\Delta\sigma)^3}{(\Delta G)^2} \propto \frac{(\Delta\sigma)^3}{(\Delta H - T\Delta S)^2} \quad \text{(A-11)}$$

This last relationship A-11 between the activation energy ΔG^* and the change in free energy ΔG is of high importance for nucleation. ΔG is given by

$$\Delta G = \Delta H - T\Delta S \quad \text{(A-12)}$$

in which ΔH is the standard heat of formation, T is temperature and ΔS the change in entropy associated with the phase transition. In general, the change in entropy is small compared to ΔG in solid-state formation; ΔHi is usually taken as a good measure for ΔG. The rate at which nuclei form and grow is also related to the critical energy to overcome (ΔG^*) through:

$$\rho^* \propto \exp\left(\frac{-\Delta G^*}{kT}\right) \exp\left(\frac{-Q}{kT}\right) \quad \text{(A-13)}$$

The growth rate depends on the number of nuclei reaching the critical size (first factor), and on the local atomic rearrangement needed to form the initial nucleus through Q, the kinetic activation energy for this local rearrangement. The growth rate $\rho*$ strongly depends on temperature. As nucleation typically occurs at higher temperatures (because of the small ΔG, and thus high ΔG^*), equation A-13 explains why nucleation controlled reactions generally occur fast in a very narrow temperature window.

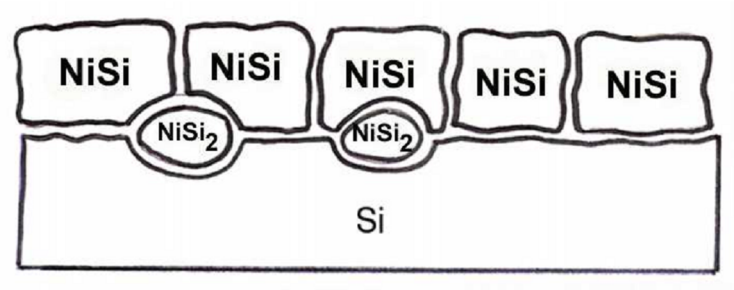


Figure A.5 Nucleation of $NiSi_2$ through NiSi + Si → $NiSi_2$. The figure illustrates both homogeneous (at a double grain boundary site) and heterogeneous nucleation (at a triple grain boundary site).

Thin Films We focus on the specific case of nucleation in a solid planar two-phase system. The total amount of energy to ne overcome for nucleation is given by equation A-11. The system evolves from a two-phase system into a three-phase system. The nucleation principle is illustrated in Figure A.5 for the nucleation controlled transition NiSi + Si → $NiSi_2$, characterized by a change in enthalpy of about -2 kJ/(mol of Ni atoms) [A.3].

The change in surface energy $\Delta\sigma$ associated with the reaction, can be specified in the form of $\Delta\sigma = \sigma_{final} - \sigma_{initial}$ as

$$\Delta G_{homo} = \left(\sigma_{\mathrm{Ni_2Si/NiSi}} + \sigma_{\mathrm{Ni_2Si/Si}}\right) - \sigma_{\mathrm{NiSi/Si}} \qquad \text{(A-14)}$$

In case of homogeneous nucleation (at NiSi/Si interface), or

$$\Delta G_{homo} = \left(\sigma_{\mathrm{Ni_2Si/NiSi}} + \sigma_{\mathrm{Ni_2Si/Si}}\right) - \sigma_{\mathrm{NiSi/Si}} - \sigma_{\mathrm{NiSi/NiSi}} \qquad \text{(A-15)}$$

In case of heterogeneous nucleation (at a triple grain boundary/interface point).

A.3 First Phase Formation

For many year, people have tried to understand the mechanism by which the first phase that forms upon heating of a planar M/Si system, is selected.

The prediction of the first forming phase upon silicidation is a very complex problem in which many aspects of kinetics and thermodynamics are involved. Many years of research did not provide us with a clear way to predict this first phase. It is generally accepted that the first feature occurring upon heating of a M film deposited on a Si substrate, is the formation of a thin amorphous (i.e. without long-range ordering) M-Si mixed layer at the interface. The reaction leading to the formation of this layer is referred to as the Solid-State-Amorphization Reaction (SSAR). Such amorphous interlayer formation was initially observed in metal-alloys; later, it was also detected in respectively metal/a-Si and metal/crystalline-Si systems. Three essential factors were found that permitted the initial formation of an amorphous interlayer [A.4]:

1. the fast diffusion of one component into the other (kinetics),

2. a negative heat of mixing of the amorphous mixture (thermodynamics), And

3. sufficiently low temperatures to suppress either nucleation/growth of the thermodynamically preferred crystalline compounds.

As this amorphous layer precedes first-phase formation, its characteristics are essential for a better insight in the first crystalline phase selection mechanism. The composition

of this layer is found to be heterogeneous, ranging from more Si-rich at the Si interface toward more metal-rich at the metal interface. It has been experimentally observed that this metastable metal-Si amorphous layer is limited in thickness. The layer grows until it reaches a critical thickness. Once this thickness is reached, crystalline phases nucleate [A.5].

Thermodynamics necessarily provides the driving force for compound crystallization in this amorphous mixed layer. However, the concentration gradients within this amorphous layer and the need for diffusion to form a crystalline compound indicate with specific composition, indicate that kinetics will also play an important role in the formation of the first phase. Several theories have been developed in order to understand the mechanism by which the first forming phase is selected. The theories can be roughly divided into two schools of thoughts, with either thermodynamics, or kinetics being the mechanism that controls first-phase selection.

A.3.1 First Phase Selection by Thermodynamics

Initial Work Historically, the first model that tried to explain the first forming phase by means of thermodynamics was postulated by Walser and Bene in 1976 [A.6]. They postulated that during the initial reaction, a glassy membrane forms at the metal/Si interface. This glassy membrane is supposed to be a very thin amorphous region, with a concentration that corresponds to the composition of the lowest-temperature eutectic. The thickness of this glassy interface layer increases, until it reaches a critical (unstable) thickness, after which the first crystalline compound nucleates within this region. The authors supposed that atomic diffusion in the initial stage of nucleus

formation is limited, and that thermodynamics selects the first phase as the one causing the biggest free energy change: *'The first compound nucleated in planar binary reaction couples is the most stable congruently melting compound adjacent to the lowest-temperature eutectic on the bulk equilibrium phase diagram.'*.

The model showed a relative success in predicting the first formed phase: for a total of 84 binary systems, the model could predict the first phase in 67 cases. However, critical reviewers [A.4] stated that the experimental data on the first phase should be treated with care, as the applied techniques suffered from limited sensitivity. Therefore, it is hard to really evaluate the success of the proposed model.

Effective Heat of Formation (EHF) Pretorious *et al.* [A.7, A.8] formulated a model that allows for a quantitative prediction of the first nucleating phase at a metal/ Si growth interface, by using thermodynamic data as the change in enthalpy ΔH^0. As mentioned before, for solid-state reactions, ΔH^0 is typically a good estimation for the change in free energy ΔG associated with the phase formation.

The authors attributed the failure of the model by Walser and Bene to the fact that this model did not take into account the atomic ratio at the interface. The atomic ratio of the species present at the growth interface (further referred to as *effective concentration*) generally does not match to the composition of a binary compound. Hence, one of the species exhibits an effective concentration that is lower than the concentration of any stoichiometric compound, and is thus limiting the formation of that compound. Any deviation of the exact stoichiometric composition proportionally decreases the energy released when the compound is formed i.e. for every compound ΔH^0 can be redefined into a concentration dependent heat of formation $\Delta H'$, named the effective heat of formation (EHF):

$$\Delta H'_{\text{eff}} = \Delta H^0 \frac{\text{effective concentration limiting element}}{\text{compound concentration limiting element}} \qquad \text{(A-16)}$$

with $\Delta H'_{\text{eff}}$ and ΔH^0 expressed in kJ/mol.

Presenting $\Delta H'_{\text{eff}}$ versus the effective concentration results in a typical diagram as given in Figure A.6 for Ni-Si. The congruent phase that has the most favorable EHF at that specific effective concentration is the one expected to form first (The temperature dependency of ΔH (and ΔS) is generally minimal and therefore). neglected.. The excess of atoms not used for initial stoichiometric crystallization is assumed to remain somehow available for formation of following phases. The model generally does not take into account whether phases are able to nucleate or not, it only deals with the driving force for the reaction. In a way to at least partially deal with nucleation barriers, non-congruent phases are not supposed to form readily, due to their typically high nucleation barrier. As in this EHF model, elementary species are supposed to be readily available, the model mainly deals with thermodynamics in predicting the compound formation in an intermixed layer with a given composition.

The problem for predicting the first phase in a real bilayer solid-state reaction, is the fact that it requires knowledge on this *effective concentration* of the intermixed metal-Si layer at the growth interface. This concentration at the interface cannot be calculated theoretically. Some atomic intermixing should occur at the interface, and kinetics should then (at least partially) be considered to determine the effective atomic concentration at the metal/Si interface. Brown & Ashby found that solid-state diffusion correlates with the melting point of the solid. As a consequence, the most effective mixing at the interface is then supposed to be related to the composition of

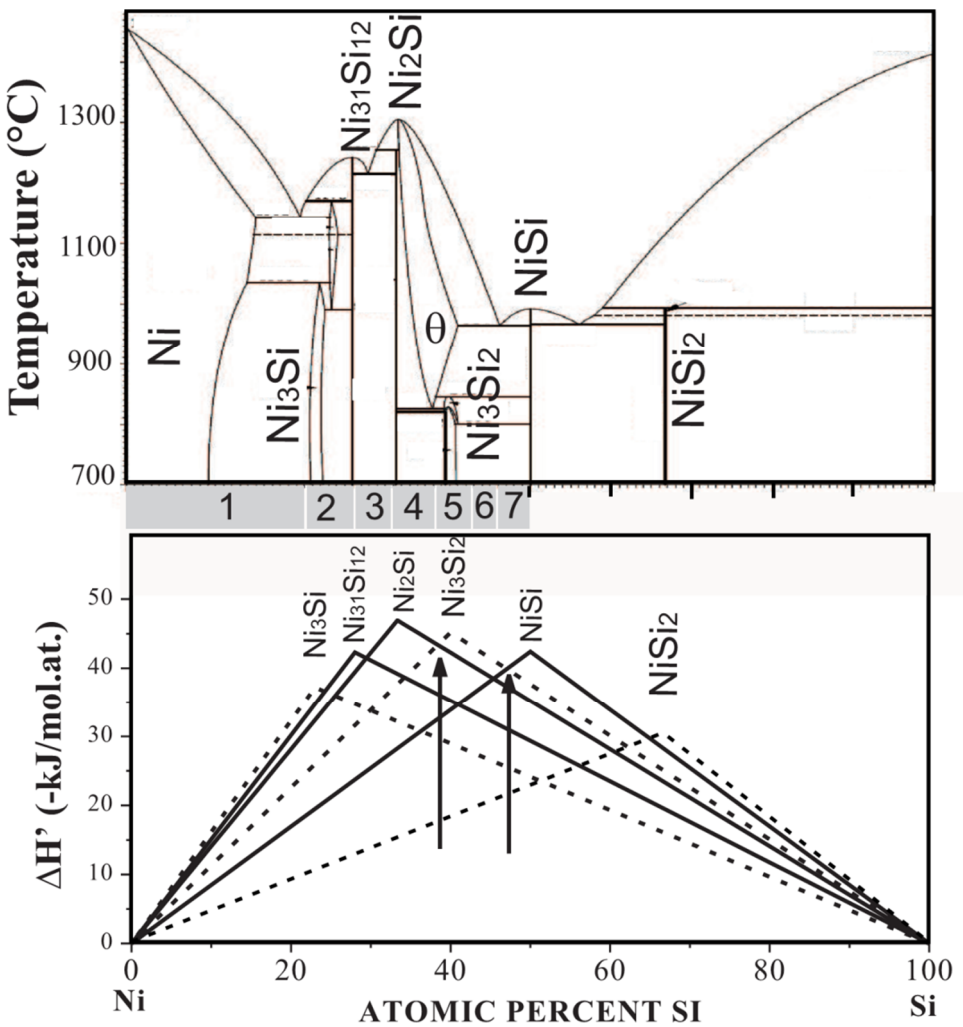


Figure A.6 The ΔH_{eff} diagram and phase diagram for the Ni-Si system. The dashed lines indicate non-congruent phases. Note that the values for $\Delta H'$ of δ-Ni_2Si and NiSi are nearly identical and cannot be distinguished when taking into account typical error bars on thermodynamic data [A.7].

the liquidus minimum of the binary metal-Si system. In agreement, Pretorius *et al.* used the concentration at the liquidus minimum in the phase diagram as a measure for the concentration of the amorphous layer, in order to deal at least partially (as the model does not deal with mass transport) with kinetics that are certainly involved in thin film formation. The following phase rule can then be formulated: Phases will react with each other to form a phase with a composition lying between that of the interacting phases, whose effective heat of formation, calculated at the concentration closest to that of the liquidus minimum within this composition range, is the most minimum.

The EHF model allowed to predict the first forming phase in 68 of a total of 84 investigated systems. In particular, for the Ni/Si system, the EHF for every compound is listed in Table A.1. The EHF theory suggests initial nucleation of NiSi or δ-Ni_2 Si. One should note that uncertainties on the value of ΔH can be as high as 10%.

Table A.1 Ni silicides and their crystal structures, prototype, heat of formation ΔH^0, and effective heat of formation ΔH_{eff}[A.7].

Ni phase	Crystal Structure	Type	ΔH^0 [kJ(mol at.)$^{-1}$]	ΔH_{eff} [kJ(mol at.)$^{-1}$]
Ni	Cubic	Cu		
β1-Ni_3Si	Cubic	$AuCu_3$	-37.2	-26.5
$Ni_{31}Si_{12}$	Trigonal	$Ni_{31}Si_{12}$	-42.3	-31.7
δ-Ni_2Si	Orthorhombic	Co_2Si	-46.9	-37.6
θ-Ni_2Si	Hexagonal	Ni_2In	?	?
Ni_3Si_2	Orthorhombic	Ni3Si2	-45.2	-40.3
NiSi	Orthorhombic	MnP	-42.4	-39.4
$NiSi_2$	Cubic	CaF_2	-29.3	-20.4

A.3.2 First Phase Selection by Kinetics

A very intensive theoretical study on kinetics controlling the first-phase formation in M/Si systems was done by d'Heurle [A.1, A.2, A.9]. The theory excludes nucleation from being the mechanism that controls the first-phase formation, as the change in energy ΔG to form a first phase from its elementary components is normally sufficiently high, and hence not expected to be rate-controlling during the formation of the first phase.

The theory assumes that initial phase nucleation is laterally uniform, and that multiple phases can start to grow simultaneously at different reaction interfaces. Out of all the phases that can initially form simultaneously, the phase that is actually observed as 'first phase', is then the one that grows fastest i.e. the one that has the fastest supply of mobile atoms to the growth interface, so that the growth at this interface proceeds faster than the (possible) consumption at another reaction interface. Other present growing phases that are consumed at a faster rate than grown at the other interface, are likely very thin and possibly below the detection limit. The first (detected) forming phase is then the one that actually wins this kinetic growth competition. This rule of kinetics determining the first phase selection was summarized [A.1] as: *Generally, one gets that which grows*.

The concept of kinetics being responsible for the selection of the first phase, is mainly based on the differences in atomic diffusion coefficients for atoms in different compounds. Atomic diffusion coefficients can differ by several orders of magnitude, especially at the relatively low temperatures where the first growing phase is selected. This is in strong contrast with the typical heats of formation ΔH_0 for the different compounds, for which the relative differences for the compounds are assumed to be

too small (factors of the order of 2 or 3) to fully determine the first phase selection. The physical explanation thereof should be found in the respective dependencies of both quantities on the melting point: whereas the free energy typically scales linearly with the melting point, the diffusion coefficient scales exponentially.

Experimentally, HR-TEM for instance confirmed that multiple phases can co-nucleate within an amorphous layer. This has been observed in the Ti/Si system [A.10], and more recently in the Ni-Si system as well [A.11]. These observations stress the idea that the free energy change to make the initial transition of an amorphous layer into a crystalline phase is probably more or less equal for the potentially forming compounds (see for instance Table 1.1).

A.3.3 Kinetics and Thermodynamics

Based on the number of cases in which the first phase can be successfully predicted, both schools of thought on first-phase selection can claim to have proved their value. However, when it comes to predicting the first phase in a real bilayer system, a direct application of these theories should be treated with care. The truth on the first-phase formation is likely a compromise dealing partially with both theories.

Thermodynamics necessarily provides the driving force for crystallization of an amorphous layer. Yet, it is unlikely that the selection of the first phase should be governed by nucleation, as ΔG, the driving force to form a compound from elementary components, is typically sufficiently high, at least too high for nucleation to be rate-controlling in the initial stage of phase formation. Furthermore, even if thermodynamics would lead to the nucleation of a phase different than the one that

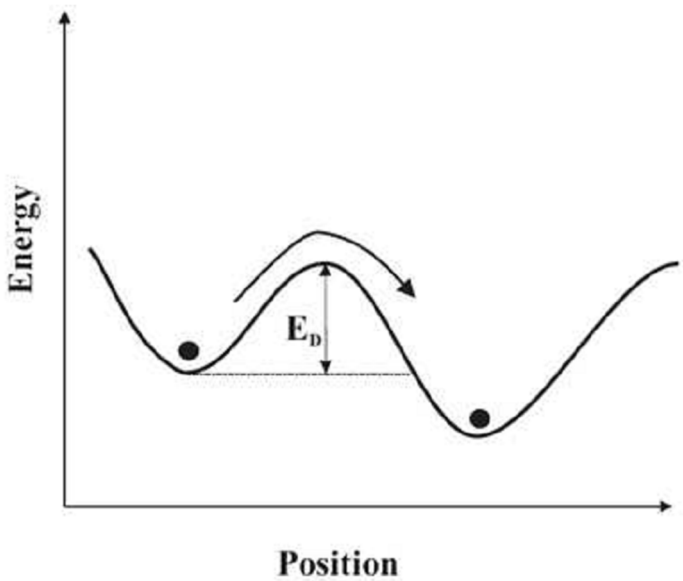


Figure A.7 Illustration of the atomic diffusion process on microscopic scale (figure taken from [A.12]). E_D represents the diffusion activation energy.

grows fastest, this layer would remain extremely thin. It would be unstable (1) from a kinetic point of view, as it will be consumed fast, and (2) from thermodynamic point of view, as the volume free energy (gain) is too small compared to the surface energy (loss) [A.2]. In the real M/Si system, the diffusion controlled growth (i.e. kinetics) thus clearly plays an important role in the selection of the first phase that can grow until it is detected. Unfortunately, the key limit to the direct applicability of the kinetic theory as stated by d'Heurle is likely the fact that it deals with mass transport on a macroscopic scale. The experimentally derived atomic diffusivities, which should according to the theory be used as quantitative measure determining the growth rate, are generally diffusivities derived in bulk materials. On microscopic scale, atomic mass transport is governed by the ability of an atom to move from one vacancy into

another one (Figure A.7). A thin polycrystalline film system typically exhibits a particular microstructure, existing of a single layer of grains. This implies that the concentration of vacancies is mostly found along the film's grain boundaries, which can then act as fast diffusion paths (i.e. fast compared to the lattice mass transport in bulk material). Hence, diffusivities in film compounds can differ significantly from the diffusivities in the bulk counterparts. This idea was experimentally confirmed by Barge *et al.* for diffusion in the Co-Si system [A.13]. The authors found that the diffusion coefficient D is much larger in thin films than in bulk materials, and were able to correlate this with the difference in grain size for both systems. For polycrystalline films, the effective resulting diffusion coefficient D_{eff} could then be written as:

$$D_{\text{eff}} = D_{\text{lattice}} + \frac{\delta}{2a} D_{\text{grainboundary}} \tag{A-17}$$

with a the grain size and δ the grain boundary width. Hence, one should be careful when directly estimating the fastest growing phase in a binary metal/Si couple by the diffusivities derived for bulk material. The difference in atomic diffusivities (and hence the growth rates) for the different phases may then not be so clearly pronounced as in bulk material.

Appendix B

Dopant Effect on MILC Phenomenon

SINCE the escalating use of mobile instruments, display devices are in increasingly high demand. The global call for dynamic random access memory (DRAM) and FPDs in particular has pushed development of those products to the forefront of the high-tech industry. Currently, the LCDs require a process for pixel switching, which is presently achieved with a-Si TFTs and a driving integrated circuit (IC). In fact, the determining quality factor for an LCD is the switching speed of the TFT. Intensive investigation is underway in support of the competition to set the latest trend in high-definition and high-speed mobile devices, including through the determination of the appropriate number of electrons for poly-Si TFTs. In addition to this research, the next generation technology is monitoring the commercial use of OLED displays, and due to this high interest, the use of poly-crystalline thin film transistors will only become a more vital necessity.

There are two different approaches to the manufacturing of poly-Si TFTs: SPC [B.1] and ELA. The poor element properties and high temperature annealing requirement of SPC are drawbacks to this method. On the other hand, the ELA shows excellent

electric properties, but problems like suspect uniformity and high cost make the technique difficult to deploy commercially.

Among the various SPC methods, the MILC, which are developed in 1996, has proven to be more successful than all other methods in terms of lowering the crystallization temperature of a-Si thin film. Annealing after metal deposition such as Pd and Ni an a-Si, catalytic phase transformation is possible when crystallizing under a low temperature of 500 ℃, unlike in the process of MIC, metal contamination rarely occurs, good quality poly-Si is available and highly efficient poly-Si can also be produced [B.1, B.2].

Fabricating an actual device by means of MILC should be done over the doping are. According to previous experiments, it is known that the MILC temperature changes depending on the type of dopant, but the causes of the specific changes in speed and phase are not exactly known. To investigate the causes of these changes in speed and phase, B_2H_6 and PH_3 are doped using IMD in this experimental, yielding several observed changes in the MILC rate. Also, in order to observe and measure more changes in the rate of MILC, a two-minute interval doping pattern was performed on a fixed shape.

B.1 Sample Preparation

On the top of corning 1737 glass, a SiO_2 of 3000 Å was deposited by PECVD using SiH_4 and N_2O precursor, and a 500 Å a-Si was deposited with SiH_4 by LPCVD. Various shapes of a-Si patterns were defined by photolithography and RIE processes. Sputtering was done for 50 Å-thickness-Ni deposition on defined a-Si thin films, the

Table B.1 IMD conditions. For *n*-type and *p*-type, phosphorus and boron were used, respectively.

	***n*-Type**	***p*-Type**
Accelerating Voltage	11 kV	16 kV
RF Power	150 W	
Working Pressure	3 mTorr	
Doping Time	10 min (variation)	
Gas	PH_3 8 sccm	B_2H_6 15 sccm
Sheet Resistance	200 Ω/□	180 Ω/□

lift-off method was carried out for defining of Ni pattern. Also, B_2H_6 15 sccm, PH_3 15 sccm were applied for the doping at a two-minute intervals using the IMD method and, in order to observe the rate of crystallization of the doping areas, IMD was continued for about ten minutes. Annealing was done at a temperature of 550 °C in a vacuum furnace four times at two-hour time intervals. With the degree of vacuum below 1×10^{-6} Torr, the growth phase was observed under an optical microscope.

B.2 Observations and Discussion

In order to investigate the rate of MILC related the doped area, 6 kinds of samples were prepared, and the IMD conditions of each sample are presented in Table B.1.

In this investigate, RF electric power of 150 W, and the inductively coupled plasma (ICP) structure was supplied by fixed plasma and DC acceleration voltages of 17 kV. The hydrogen-diluted source gasses 5%$PH_3$and 3%B_2H_6, as well as highly purified H_2 were used. The photolithography method was used to form patterns, using Ni, on the front surface of the vapor-deposited a-Si thin film sample, and the lift-off method from

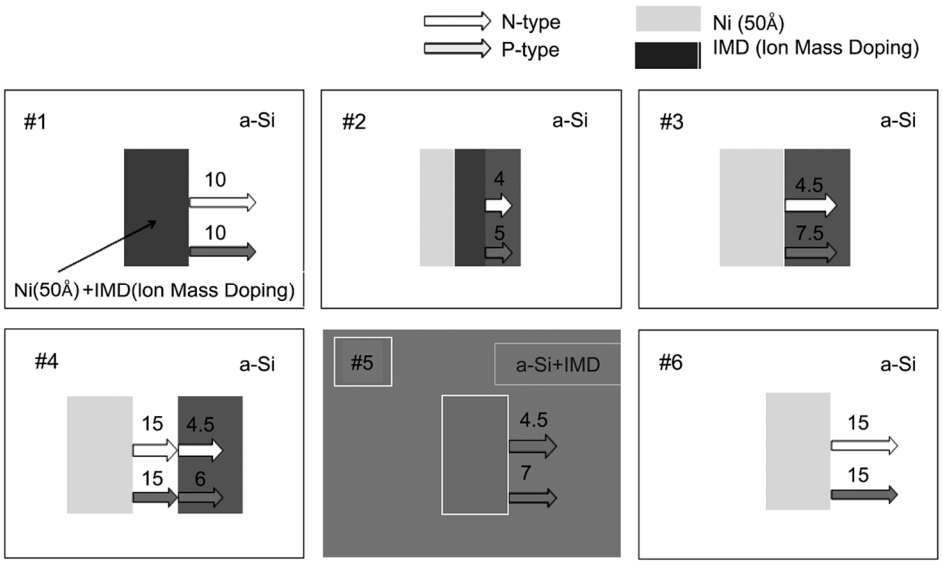


Figure B.1 The rate of MILC annealed at 550 °C for 2h after IMD

PR was used later on. In order to limit the areas being doped, a mask was used during the process of the Ni-pattern formation. After crystallization crystal growth was observed as shown in Figure B.1.

In sample #1, to form the Ni pattern on the top surface of the a-Si thin film, dopants were doped only on same region of Ni thin film, and a speed of crystallization growth of 10 μm/h was observed on both the *p* and *n* type regions. A Ni vapor deposition was produced equally on both samples #2 and #1, where the dopant shifted 50 μm to the right where IMD took effect. As a result, the crystallization rate for *p*-type was 5 μm/h, and the crystallization rate for *n*-type was 4 μm/h. When these two samples are compared with a non-doped sample like #6, as doping is proceeding on sample #1's Ni dopant, we can observe that the rate at which MILC takes place decreases 30%.

When sample #6 is compared to sample #2, the rate of MILC on the doping areas on a-Si is also decreased by 60%. This result is evidenced in sample #3 where the *p*-

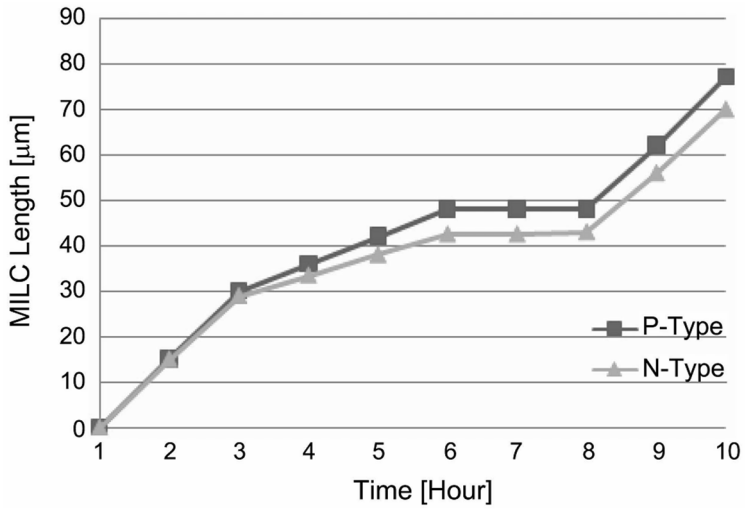


Figure B.2 MILC dependency on doped area. B_2H_6 and PH_3 were doped after the deposition of Ni thin films and they were annealed at 550 °C 4 times.

type MILC rate was 7.5 μm/h, and the *n*-type rate was 4.5 μm/h. Even though the rate of MILC proved to be the same on samples #4 and #6, sample #4 not having dopant doped in the Si area, it can be observed that past the doped areas, in both a rate of *n*-type of 4.5 μm/h and *p*-type of 6 μm/h were shown. It can be also observed that samples #5 and #3 yield similar results, and that despite doping with either PH_3 or B_2H_6, the rate of MILC is certain to decrease.

Nevertheless, we found that sample #4 merited our attention in this experiment. It was observed that the MILC process began in the Ni vapor deposition area, passing the Si and doped Si area, where MILC was seen to be taking effect in the Si area again. The crystallization phase of this sample is shown in the graph below Figure B.2.

The length of MILC continued to grow in Sample #4's Si area, but as soon as it reached the end stages of the doped areas, no growth of MILC could be observed. In order to investigate the aspect of MILC growth, an additional annealing process was

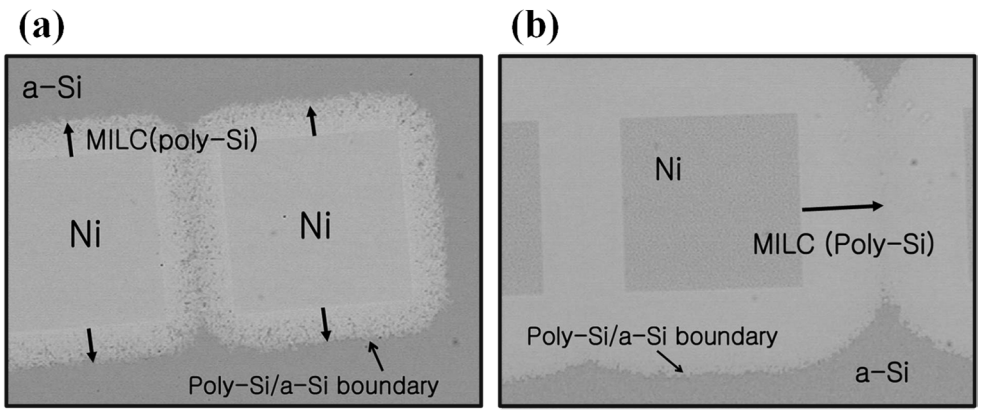


Figure B.3 optical microscope images of crystallized Si in case of (a) doped Si and (b) undoped Si.

done for one time. The result of this process showed us that crystallization took place up to the boundary between the doped Si areas and undoped Si areas. This aspect of crystallization on doped areas can be explained by comparing the MILC on the doped areas in sample #4, and the MILC on the un-doped areas in sample #6. See Figure B.3. It can be observed that from Figure B.3, the poly-Si/a-Si boundary on both undoped and doped areas, that the crystallization took effect more evenly and uniformly on undoped Si areas than on the doped Si areas. Looking at the MILC results from sample #4, passing the undoped Si area, MILC does not start to take effect until it reaches the doped Si area. As shown in Figure B.3(a), in the MILC area, crystallization did not take place and we can observe that the a-Si formed sparsely on the sample. However, after having annealed the sample for two additional time and after crystallization had taken place, MILC began taking effect immediately upon entering the undoped Si areas, passing the end stages in the doped Si area.

In order to investigate the extent of the effect that the doping time had on the rate of MILC, a sample shaped similarly to sample #5 was made, and even though they each

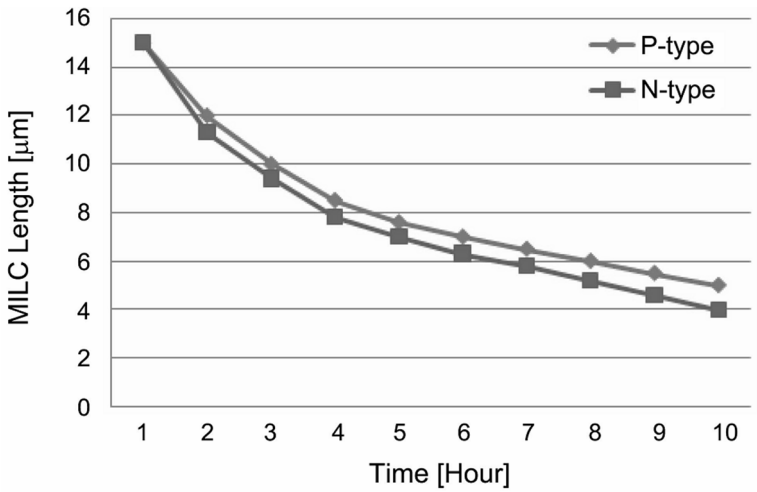


Figure B.4 MILC dependency on doping time. B_2H_6 and PH_3 were doped 2 times interval after the Ni thin film deposition.

had the same doping time, the new sample displayed a change in MILC length. Se Figure B.4. After experimenting with the effect that doping time had on the rate of MILC, it was found as expected that the MILC rate of the n-type was slower than that of the *p*-type.

In 2002, Tianfu Ma *et al.* [B.3] reached a conclusion regarding the effect that dopants have on MILC, stating that when a non-crystalline Si of 1000 Å and B atoms at a high dose of 3×10^{15} /cm^2 is injected at 550 °C, the growth rate will double at that temperature. According to the same study, when a large amount of B atoms were used as a dopant, the formation temperature of $NiSi_2$ starts to decrease and the boron atoms of $NiSi_2$ are capable of lowering the energy formation. However, if we follow what is said in that investigation, a high degree of B atom doping can cause a decrease in the rate of MILC growth. Also, the MILC mechanism through Ni silicide allows Si atoms of a-Si to easily situate themselves in the Si crystalline lattice. Keeping this in mind, it can be assumed that because of the additional annealing process of the Ni silicide, the

formation temperature may have been affected and it is believed that the rate of growth should be followed by the, annealing time which should probably be the same. However, it can be concluded that instead of the actual annealing period and growth rate being intrinsic, it probably depends on a larger condition, and having said that, an inference can perhaps be made that the mechanism might not be as dominant as it is perceived to be. It was found through this experiment that the rate of MILC will show a decrease when using B or P, even when compared to the rate of MILC of undoped a-Si, and the drop in MILC rate can be particularly observed upon the doping of P.

The decrease in the rate of MILC results from disturbance of dopant migration through segregation and the NiSi layer of dopant. Particularly, the rate of MILC was reduced due to the strong bonding between Ni and phosphorous. it is reported that rate of MILC increased by 40% when doped with B [B.4], but in our experiment, the rate of MILC decreased when doped with two dopants because the IMD diluting source gas in Hare contain 3% B_2H_6 and 5% PH_3 is different from ion implantation in separation of source gas by mass. This phenomenon was reported that the rate of crystallization decreased through research of SPE (solid phase epitaxy) [B.5, B.6].

Generally H_2 inside the a-Si have similar types of combinations like Si-H and Si-H. It is reported that both the combination of Si-H_2 around 400 °C and Si-H around 550 ~ 600°C breaks down, hence H_2 escapes from the thin film [B.7, B.8]. This combination of Si atom and H_2 atoms bonding is thought a primary factor that the rate of MILC growth decrease. Nevertheless, Si atoms in a-Si grow through the $NiSi_2$ boundary, this combination breaks down, and that during this process, Si atoms cannot be supplied enough to fill the vacant spaces.

Abbreviation

AES	Auger electron spectroscopy
AFM	atomic force microscopy
AMOLED	active matrix organic light emitting diode
a-Si	amorphous silicon
a-Si:H	hydrogenated amorphous silicon
AZO	aluminum zinc oxide
CdS	cadmium sulfide
CdSe	cadmium selenide
CRT	cathode-ray tube
CVD	chemical vapor deposition
DC	direct current
DRAM	dynamic random access memory
EBSD	electron backscatter diffraction
EHF	effective heat of foemation
ELA	excimer laser annealing
FID	field induced drain
FPDs	flat panel displays
FWHM	full width half maximum
GIDM	gate insulator doping mask
GMIC	gettered metal induced crystallization
GSIC	gettered silicide induced crystallization
G-SIC	SIC pol-Si thin film gettered using etch stopper layer

HCS	hot carrier stress
HDCS	high drain current stress
HRTEM	high resolution transmission electron microscopy
IC	integrated circuit
ICP	inductively coupled plasma
IMD	ion mass doping
ITO	indium tin oxide
LCD	liquid crystal display
LDD	lightly doped drain
LDS	lightly doped source
LED	light emitting diode
LPCVD	low pressure chemical vapor deposition
LTPS	low temperature polycrystalline silicon
MESFET	metal semiconductor field effect transistor
MIC	metal induced crystallization
MILC	metal induced lateral crystallization
MIVC	metal induced vertical crystallization
MOSFET	metal oxide semiconductor field effect transistor
OLED	organic light emitting diode
OS-MILC	off-set metal induced lateral crystallization
OS-SILC	off-set silicide induced lateral crystallization
PC	personal computer
PDP	plasma display panel
PECVD	plasma enhanced chemical vapor deposition
Poly-Si	polycrystalline silicon

PR	photo resistor
RF	radio frequency
RIE	reactive ion etching
RMS	root mean square
SA-MILC	self-aligned metal induced lateral crystallization
SA-SILC	self-aligned silicide induced lateral crystallization
SEM	scanning electron microscopy
SIC	silicide induced crystallization
SILC	silicide induced lateral crystallization
SIMS	secondary ion mass spectroscopy
SOI	silicon on insulator
SPC	solid phase crystallization
SPM	scanning probe microscopy
SSAR	solid-state amorphization reaction
SSB	SILC/SILC boundary
TCOs	transparent conductive oxides
TEM	transmission electron microscopy
TFT	thin film transistor
TVs	televisions
XPS	X-ray photoelectron spectroscopy
XRD	X-ray Diffraction
ZMR	zone melting regrowth
ZnO	zinc oxide

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요약(국문초록)

실리사이드 유도 측면 결정화 현상과 저온 다결정 실리콘 박막 트랜지스터의 적용에 관한 연구

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과거 음극선관 디스플레이 이후 비정질 실리콘을 이용한 박막 트랜지스터의 집적이 가능하게 되었고, 액정표시장치가 플라즈마 디스플레이 패널과 함께 평판 디스플레이 산업을 점유하게 되었다. 결국 박막 트랜지스터는 스마트 폰, 대형 디스플레이, 등 많은 전자기기에 있어서 필수적인 요소가 되었다. 하지만 최근에 능동형 유기 발광 디스플레이가 차세대 디스플레이로 주목을 받기 시작했고, 과거 액정 표시장치에서 활성층으로 사용되었던 비정질 실리콘의 낮은 전계 이동도 및 신뢰성 등의 한계로 인해 새로운 활성층 물질의 요구가 절실해 졌다. 기존의 비정질 실리콘을 대체할 물질로 산화물, 유기물, 다결정 실리콘 등이 주목을 받고 있는데, 유기물 및 산화물을 공정의 어려움과, 신뢰성, 낮은 전계 이동도의 문제로 고해상도 유기발광 디스플레이 제작에 어려움이 있다. 또한 다결정 실리콘의 경우 결정화 방법에 있어서 레이저를 이용한 방법과 비레이저 방식이 있는데, 현재 상용화 된 레이저 방식은 대면적화에 한계가 있어 새로운 결정화 방법이 요구되는 시점이다.

본 연구에서는 레이저 결정화의 차세대 대체 기술로 주목 받고 있는 금속유도 결정화 방법의 문제점들을 보완하여 실리사이드 유도 결정화

기술을 제시하였다. 특히 본 연구는 기존 금속유도 측면 결정화의 누설전류를 다음과 같이 두 가지 원인으로 분류하여 원인을 찾아 해결 방안을 도출 하는데 집중하였으며, 그 결과 다음과 같은 기술 들을 개발 할 수 있었다.

금속 유도 측면 결정화 된 다결정 실리콘 영역 내에 존재하는 실리사이드 오염을 줄이기 위하여 기존에 사용한 니켈 금속 대신 직접 실리사이드를 이용하여 저온 결정화를 진행하였고, 저온 다결정 실리콘 박막 트랜지스터를 제작, 그 응용 가능성을 확인 하였다. 본 연구에서 사용된 실리사이드는 스퍼터링으로 증착된 니켈 박막을 황산에서 제거 함으로써 씨앗 형태로 얻게 된 것으로 상온에서도 비정질 실리콘 표면에 실리사이드가 형성됨을 확인 할 수 있었다. 실리사이드는 니켈의 증착 온도가 높아질수록 실리사이드 씨앗의 밀도가 높아졌고, 결정화 후 결정립 크기가 작아졌으며, 결정립계의 면적이 커져 소자 제작 시 전기적 특성이 열화되는 사실을 실험을 통해 증명 하였다.

상온에서도 실리사이드가 효과적으로 형성된다는 장점을 이용해 실리사이드 유도 측면 결정화에 대해 연구를 수행 하였고, 기존 금속 유도 측면 결정화에 비해 낮은 누설전류를 갖는 저온 다결정 실리콘 박막 트랜지스터를 제작 할 수 있었다. 또한 기존 금속 유도 측면 결정화 기술에서 금속 유도 결정화/금속 유도 측면 결정화 경계 있는 많은 결함으로 인한 한계로 알려졌던 자기정렬 측면 결정화된 다결정 실리콘 박막 트랜지스터 제작을 가능하게 하였다.

금속유도 측면 결정화 된 박막 트랜지스터의 누설전류 원인으로 잘 알려진 측면 성장 결정 경계를 제거할 수 있는 비대칭 실리사이드 형성과 같은 새로운 공정 개발에 관한 연구를 수행하였다. 그 결과 높은 역방향

게이트 바이어스 영역에서 누설전류가 낮아 졌으며, 낮은 전류밀도에서 노이즈 또한 줄어드는 결과를 보였다.

금속유도 결정화 및 실리사이드 유도 결정화 공정후 다결정 실리콘 표면에 남아있는 실리사이드 오염물을 제거하기 위해 게터링 공정을 적용하였고, 다결정 실리콘 내에 함유되어 있던 실리사이드 오염물을 효과적으로 제거하여 누설전류를 줄일 수 있었다. 또한 게터링층을 효과적으로 제거하고, 수월한 공정을 위해 화학적 산화물 형성을 연구하였고, 활성층과 게터링층의 효과적인 분리를 통해 균일한 게터링층 제거를 가능하게 하였다.

다결정 실리콘 박막 트랜지스터의 누설전류의 원인에 관해 분석하고, 이를 해결하기 위해 실리사이드 유도 측면 결정화 기술 외에 저농도 도핑된 드레인 구조를 적용하여 높은 측면 전계에서도 낮은 누설전류를 유지 할 수 있는 소자를 제작하였다.

누설 전류 감소에서 더 나아가 구동전류 및 이동도 등의 구동 특성을 향상시키기 위해 갈라진 채널을 갖는 다결정 실리콘 박막 트랜지스터 및 전기적 스트레스에 관해 추가적으로 연구가 되었다.

본 연구에서 제시된 기술 및 구조는 복잡한 공정 및 기술을 포함하지 않고 있어 즉각적인 생산기술에 적용이 가능하며, 6 장에서 제시된 향후 과제가 수행되면, 현재의 생산 기술 한계를 넘어 대면적 초 고화질 디스플레이를 제작 가능하게 할 것으로 생각된다.

Keywords: 능동형 유기 발광 다이오드, 저온 다결정 실리콘, 금속 유도 측면 결정화, 실리사이드, 박막 다결정 실리콘, 게터링, 전기적 스트레스, 누설전류, 이동도

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Patents

Domestic

1. 실리사이드 씨드 유도 측면 결정화를 이용한 비정질 실리콘 박막의 결정화 방법 및 이를 이용한 다결정 박막 트랜지스터의 제조방법,
   등록번호: 1013337970000
2. 하부 게이트를 갖는 다결정 박막 트랜지스터의 제조방법
   등록번호: 1013337960000
3. LDD 구조를 갖는 박막 트랜지스터의 제조방법
   등록번호: 1013779900000
4. 비정질 실리콘 박막의 결정화 방법 및 이를 이용한 다결정 박막 트랜지스터의 제조방법
   출원번호: 1020120038103(출원)
5. 자기 정렬 금속 실리사이드 유도 측면결정화 방법을 이용한 다결정 박막 트랜지스터의 제조방법
   출원번호: 1020120039068(출원)
6. 다결정 실리콘 박막의 게터링 방법 및 이를 이용한 다결정 실리콘 박막 트랜지스터의 제조방법
   출원번호: 1020120071328(출원)

International

1. Method for Crystallizing Amorphous Silicon Thin Film and Method for Fabricating Poly Crystalline Thin Film Transistor Using the Same
   USA patent (13-630148)

Projects

1. Flexible Display용 CNT를 이용한 투명 전극재료 및 공정개발
   (2008.01.01~2008.12.31) – 삼성전자
2. 금속유도 수직결정화를 이용한 고효율 다결정 박막 실리콘 태양전지 제조기술 개발
   (2008.01.01~2008.12.31) – 삼성전자
3. AMOLED를 위한 고성능 저온 다결정 실리콘 TFT제조에 관한 연구
   (2010.09.01~2013.08.31) – 교육과학기술부
4. 수송엔진 배기가스 촉매용 백금 저감/대체 기술 개발
   (2010.04.01~2014.03.30) – 지식경제부
5. Thin Film Battery 및 차세대 고용량 이차전지 개발
   (2011.05.01~2012.10.30) – ㈜STX 종합기술원