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$Si_{1-x}Ge_x$ crystallization for vertical channel in VNAND

수직 구조 낸드 플래시 메모리 내 수직 채널 적용

목적으로의 $Si_{1-x}Ge_x$ 결정화 연구

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이 상 수

Abstract

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Recently, the three-dimensional vertical NAND (VNAND) flash memory structure is developed to overcome the scaling limit and degree of integration issues of conventional two-dimensional planar NAND flash memory. The solid phase crystallization is used as a crystallization technique for vertical channel in VNAND. However, the solid phase crystallized film has fatal limitations related to the electrical properties when used as a channel material due to the high density of grain boundaries and intra-grain defects in the microstructure. Especially, it is expected that the string current degradation as the number of cell layers is increased for higher bit densities in the next-generation VNAND.

Therefore, having a high quality poly-crystalline channel that is large-grained and less-defective microstructure is very important for next-generation VNAND as well as devices currently in use.

In this study, the $Si_{1-x}Ge_x$/Si bi-layer structure is proposed in order to obtain the high quality poly-crystalline Si channel microstructure. This bi-layer structure is simple, easy and directly applicable to the VNAND process. The bi-layer shows $Si_{1-x}Ge_x$ surface nucleation and induces equiaxial grains that leads to large-grained and less-defective microstructure in the Si channel layer. Furthermore, the $Si_{1-x}Ge_x$ lateral growth method is proposed based on the crystallization behavior of $Si_{1-x}Ge_x$ bi-layer in order to obtain even large grains in the Si channel layer. The Ge/Si bi-layer is introduced to maximize the lateral growth effect. It was confirmed that the Ge layers are crystallized through the lateral growth only without any nucleation. After Si growth, the laterally grown grains are shown through the Ge and Si layers. These results mean that the very large Si grains over film thickness can be obtained after the Ge nucleation layer stripping. Accordingly, using a bi-layer as a channel structure is expected to improve the electrical properties of each cells and to minimize the degradation of string current in VNAND.

Additionally, the poly-crystalline Ge single layer is proposed as a vertical channel structure in VNAND. The secondary grain growth which shows the very larger grains over film thicknesses is applied as a crystallization technique. The grains three or four time larger than adjacent grains and over film thickness are detected after annealing near VNAND thermal budget. Besides, the two-step

annealing was proposed combining different grain growth kinetics in order to enlarge the grain size in a given thermal budget. The two-step annealed films showed greatly increased hole mobility compare to conventional single-step annealing and expected microstructural evolution was also discussed.

Keywords:

Vertical NAND flash memory (VNAND), Solid phase crystallization (SPC), Grain growth, $Si_{1-x}Ge_x$, *In situ* transmission electron microscopy (TEM), Transmission electron microscopy (TEM)

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1 Introduction

1.1 Scaling of NAND flash memory

The scale of NAND flash memory in memory market is rapidly increased due to the high demands for smart phone, table PC and solid state disk drives. The NAND flash memory storage capacity enhancement is continuously required because storage increasing of applications. The storage capacity is determined by the number of devices in a chip called as the degree of integration. To increase the bit density in a given space, the feature size and the distance between cells should be reduced. Based on the ITRS flash roadmap, a half pitch of two-dimensional flash memory is 18 nm in 2013.[1] However, the additional shrinkage of feature size and the distance of cells cause problems related to the physical, electrical and reliability limitations. The physical limitations mean unwanted diffraction and scattering due to the slimmer line width of devices than the laser wavelength during the lithography process. One of the electrical limitations is the electric field crowding due to the small size of floating gate. The others are cell to cell interference, hot carrier distribution and channel boosting potential due to short cell to cell distance. In a very small-sized floating gate, the amount of electrons that can be stored is also very small. Therefore, if electrons loss occurs, the cell information can be changed. Many researchers have investigated both increasing the degree of integration and solutions for scaling limitations. As a solution, the vertical structure is proposed which stacks cells in a vertical array instead of shrinking feature size

used in the two-dimensional planar NAND flash memory technology.

1.2 Emergence of vertical NAND flash memory

The first vertical type NAND flash memory as a chip level is ‘Simple Stack Memory’ fabricated by Samsung Electronics Corporation. It was revealed in International Electron Devices Meeting (IEDM) in 2006.[2] The Figure 1.1 shows the cross-section SEM image of Simple Stack Memory. This memory structure is implemented by layer stacking method repeating same fabrication processes used in the conventional two-dimensional NAND process technology. This memory structure works well, however, the relative bit cost would increase (for example over the 4 layers) due to the repeating process especially for lithography. The cost is one of the most important factors for NAND flash memory development. Therefore, Simple Stack Memory structure cannot be developed continuously and hard to be industrialized.

After one year later, Toshiba Corporation announced innovative memory architecture which names is Bit-Cost Scalable technology (BiCS) at 2007 symposium on Very Large Scale Integration (VLSI) technology.[3] The BiCS is evaluated as a ‘break through concept’ as a vertical NAND (VNAND) memory structure because the whole vertical channels are formed by single process called ‘punch and plug’. The process sequence of `punch and plug` is as follow. As shown

in Figure 1.2, the plates and dielectrics are deposited in the form of multilayer. Then, the dry etching is carried out to form the vertical hole which will be used for vertical channel. This process is called `punch`. After then, the vertical holes are filled with channel material and this is called `plug` process. The lithography cost is dramatically reduced in BiCS due to these processes. BiCS is an ideal vertical memory structure because the relative bit cost decreases as the number of stacked layers increase as shown in Figure 1.3.

After two years later, Toshiba announced Pipe-shaped BiCS (P-BiCS)[4] which is upgraded type of BiCS. The P-BiCS uses U-shape folded channel as shown in Figure 1.4(a) to solve the problems that introduces thermal damage to the select transistors in the BiCS fabrication process. At the same conference and year, Samsung announced their vertical memory architecture which name is Terabit Cell Array Transistor (TCAT)[5] as shown in the schematic image in Figure 1.4(b). It shows reduced cell size compare to BiCS by their own improved process technology. TCAT adopts metal (tungsten) gate structure that leads to fast operation speed and better reliability compare to BiCS. Anyway, the P-BiCS and TCAT adopt `punch and plug` process for vertical channel formation. TCAT went into mass production in 2013.[6] So far (January, 2015), Toshiba produces the two-dimensional NAND flash memory.

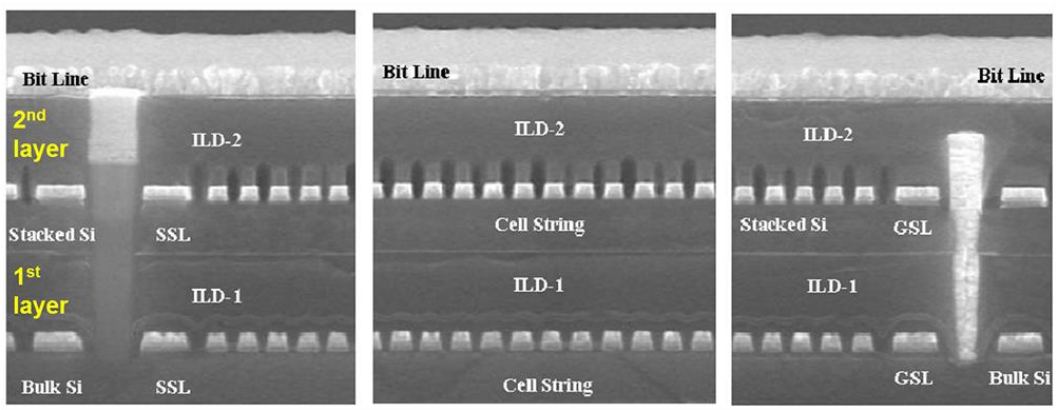


Figure 1.1 The cross-section SEM image of stacked NAND cell string.[2]

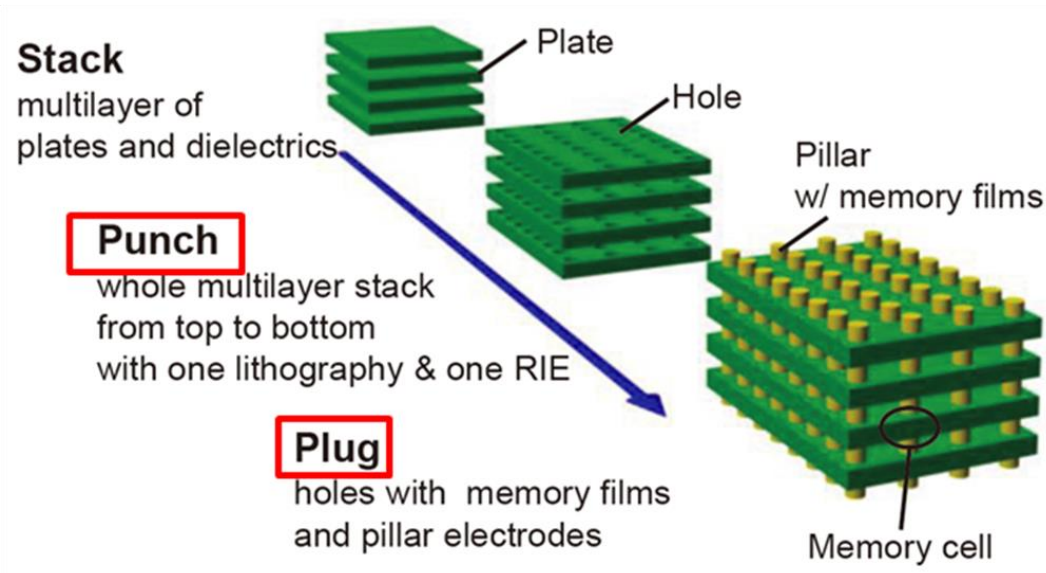


Figure 1.2 Basic concept of BiCS technology using `punch and plug` process.[3]

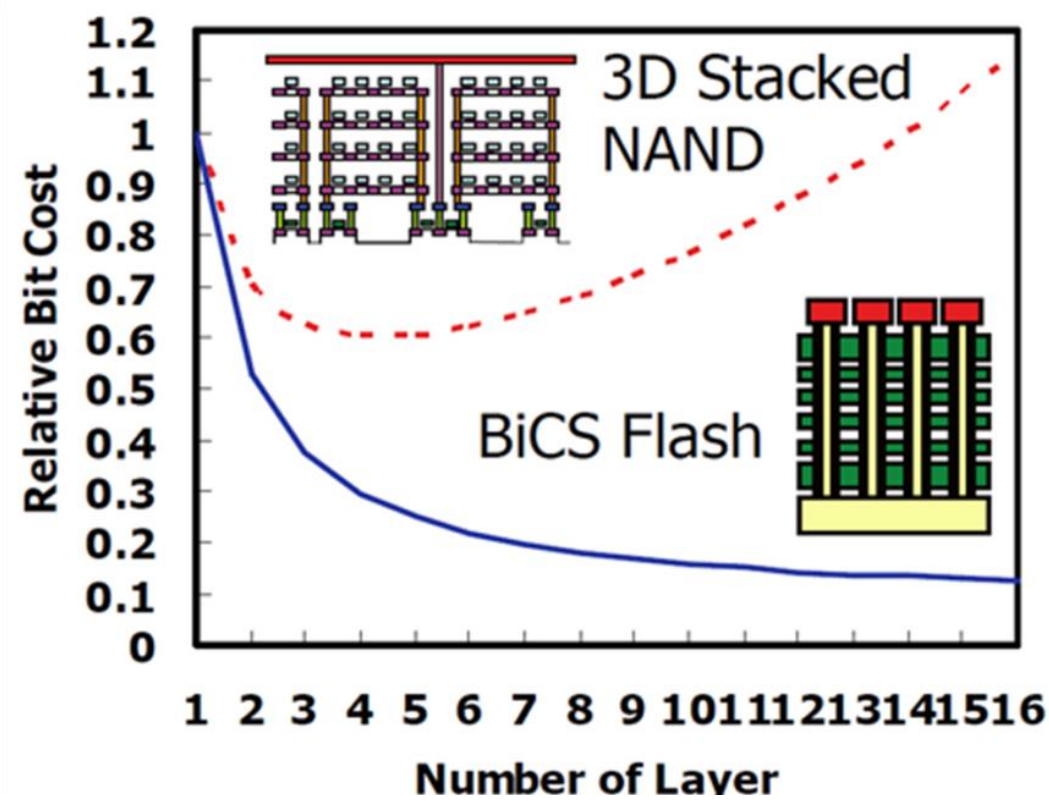


Figure 1.3 Bit Cost scalability of 3D Stacked NAND (Simple stack memory) and BiCS Flash structure.[3]

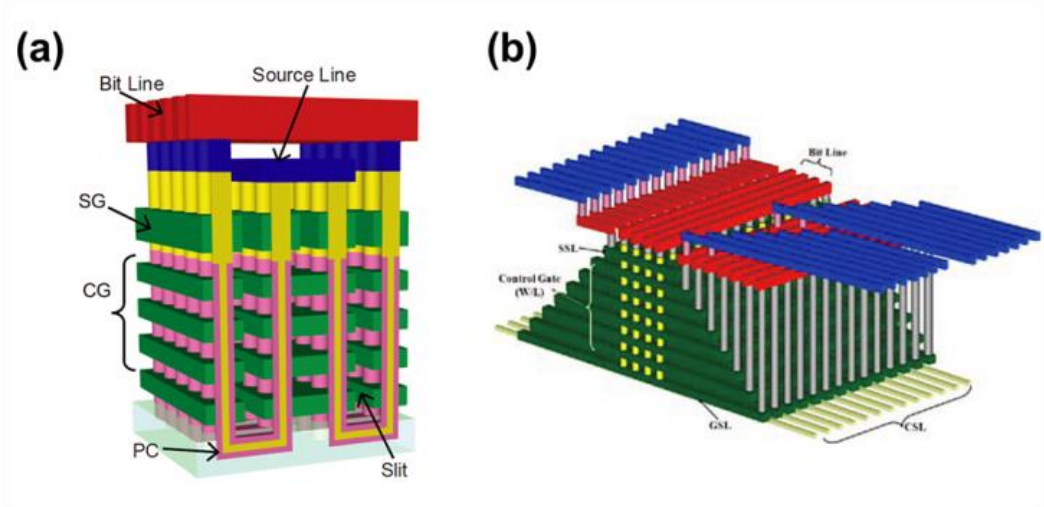


Figure 1.4 The schematics of (a) P-BiCS[4] and TCAT[5] structures.

1.3 **Vertical channel formation in VNAND**

Figure 1.5 shows the schematics of process sequence focused on vertical channel formation especially for TCAT. Firstly, the SiO_2 and Si_3N_4 are deposited in the form of multilayer on Si substrate as shown in Figure 1.5(a). This multilayer is vertically dry etched to form vertical hole as indicated in Figure 1.5(b). These holes are filled with channel material via low pressure chemical vapor deposition system as shown in Figure 1.5(c). The channel material is Si and the crystallinity is an amorphous state. The amorphous Si shows poor electrical properties due to the high density of dangling bonds in a film when used as electrical channel material. To enhance the properties, the crystallization process is carried out to crystallize the amorphous Si.

Numerous Si crystallization techniques have been researched so far. The representative crystallization techniques are metal induced crystallization (MIC)[7-10], excimer laser annealing (ELA)[11-14], selective epitaxial growth (SEG)[15-17] and solid phase crystallization (SPC)[18-21]. The characteristics of those techniques are summarized in Figure 1.6. The MIC uses metal like Ni, Al, Cu as catalyst sources. This technique crystallizes the Si film by forming the silicide that generates nuclei on its interface or though the diffusion itself. One of the advantages of MIC is low temperature process availability. However, it cannot be utilized to the vertical channel formation process due to the metal contamination that generates leakage path in a film. The ELA is solidification process. The lower thermal budget is

induced to the Si film during the ELA process due to its very short melt duration. The lower density of intra-grain defects is presented in the film microstructure after ELA process. The aspect ratio of vertical channel is so high (32 layers stacking → about 1:30). Then, it needs high laser energy density to melt the whole vertical film in the ELA process. This high energy density of laser beam would lead to film agglomeration that means the ELA also cannot be utilized to the vertical channel formation process. The SEG shows excellent crystal quality by epitaxial growth form Si substrate. However, the low throughput is expected though SEG process to form whole vertical channel due to lower growth rate. It is not suitable for mass production. Alternative crystallization technique is required to overcome such limitations. The SPC is the only the alternative method. SPC is crystallization technique that crystallize the amorphous material under the melting temperature via furnace or rapid thermal annealing system. It proceeds by phase transformation from amorphous to crystalline in the solid state. The SPC technique exhibits no problem for adjusting vertical channel formation process unlike other crystallization techniques. In practice, it is known that the memory corporations employ SPC for vertical channel formation in VNAND.

The characteristics of SPC in terms of process and film microstructure are as follows. It is relatively simple and cheap process. The SPC is carried out in a low temperature (for example; the conventional Si SPC has been carried out around 600 ^{o}C). Therefore, the thermal damages to the devices are very small or negligible. The solid phase crystallized film shows relatively large-grained microstructure over

the film thicknesses. Also, it shows uniform microstructure. However, the SPC has a fatal limitation. That is the high density of microstructural defects in the crystallized film as shown in Figure 1.7 which is the plan-view bright field transmission electron microscopy image of solid phase crystallized Si film[21]. The high density of defects are origins that degrading the electrical properties. The effects of microstructural defects for carrier movement and current flow will be treated in the next chapter.

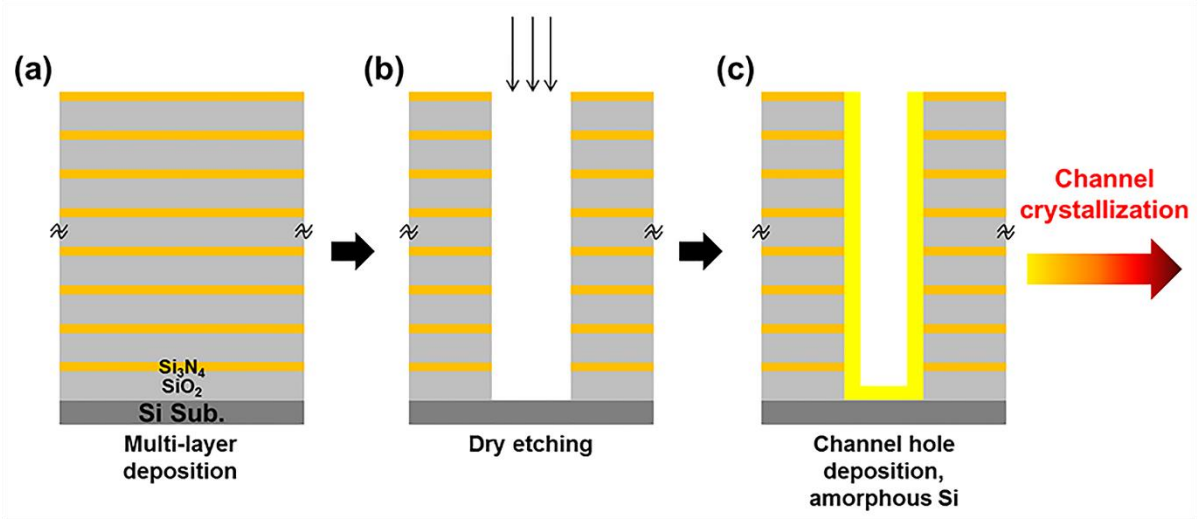


Figure 1.5 The cross-section schematics of vertical channel formation process in TCAT.

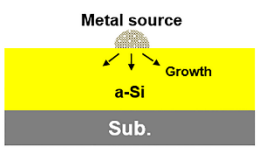
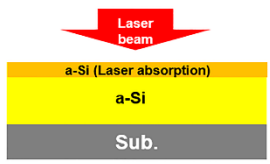
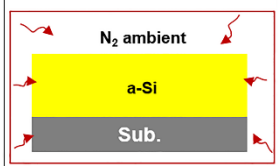
Metal Induced Crystallization (MIC)	Excimer Laser Annealing (ELA)	Selective Epitaxial Growth (SEG)	Solid Phase Crystallization (SPC)
			
-. Metal source as catalyst (Al, Ni, Cu, etc.) -. Low temperature process	-. Solidification -. Lower thermal budget -. Lower density of intra-grain defects	-. Epitaxial growth -. Excellent crystal quality	-. Via furnace/RTA -. Phase transformation from amorphous to crystalline
Metal contamination (x)	Film agglomeration (x)	Low throughput (x)	Applicable to VNAND process (O)

Figure 1.6 The characteristics of various Si crystallization techniques. The solid phase crystallization is the only applicable technique for the vertical channel formation in VNAND process.

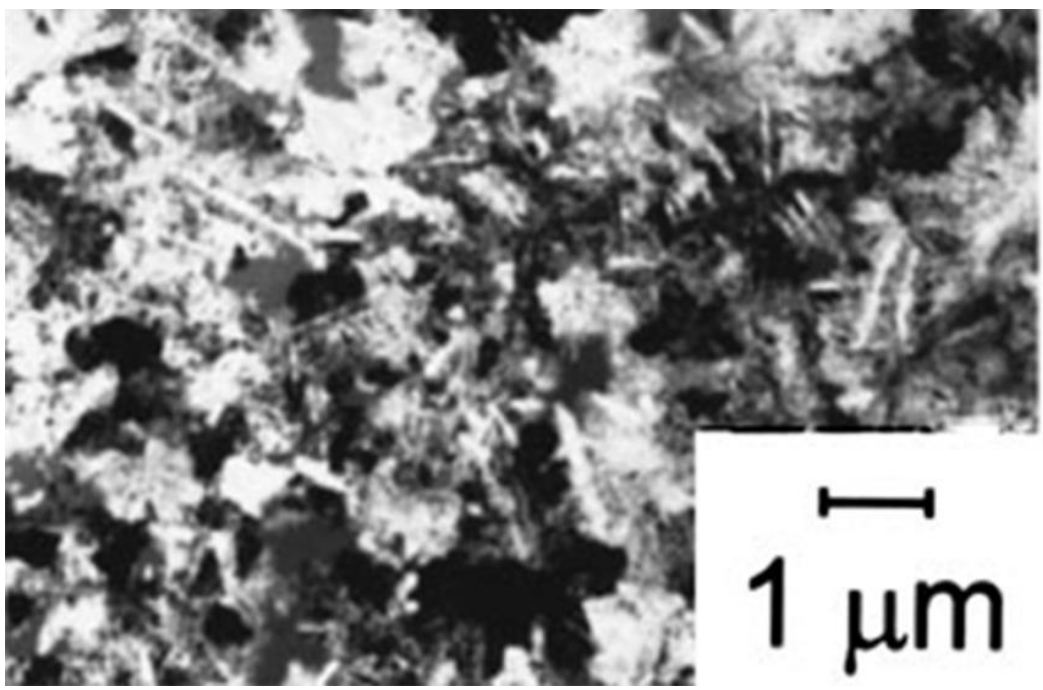


Figure 1.7 The plan-view transmission electron microscopy image of solid phase crystallized Si film.[21]

1.4 **Technical issues for vertical channel in VNAND**

The final microstructure of vertical channel through SPC process is poly-crystalline film. There exist high density of grain boundaries and intra-grain defects such as twin boundaries, stacking faults and dislocations in a film. The Figure 1.8 shows the influences of those microstructural defects in the band structure. The grain boundaries form the localized states.[22] The potential barriers are formed when the carriers are trapped in the localized states as shown in Figure 1.8. It is known that the defects states can be formed near conduction and valance band edge by stacking faults generation.[23, 24] The twin boundaries is known for dislocation sources.[24] The generated dislocations can be charged and then acted as scattering centers.[25] All these microstructural defects affect the carrier movement. The trap density *N* and the drain current I_D has following relationship as shown Equation 1-1 and 1-2 reported by J. Levinson *et al*,.[26]

$$E_b \propto N_2 \quad [1\text{-}1]$$

$$I_D \propto \mu_{gb}\left(\frac{W}{L}\right)\exp\left(\frac{-E_b}{kT}\right) \quad [1\text{-}2]$$

where E_b is the potential barrier height, μ_{gb} is carrier mobility at the grain boundaries, κ is the Boltzmann constant and *T* is the temperature. Therefore, to enhance the current of poly-crystalline film, the large grains and lower density of intra-grain defects is required in the final microstructure.

To increase the memory density, the VNAND are continuously developed in a way of vertical stacking. The length of vertical strings is getting longer as more cells are stacked as shown in Figure 1.9. Then, the density of microstructural defects in a unit string would increase. The string is vertical channel and it is poly-crystalline film. It is expected that resistivity increasing in a whole vertical string as the number of cell layers increasing. Figure 1.10 shows the string current variation depending on the bit densities by the experimental and simulation results.[27] It shows that the string current is gradually decreased as the bit densities increasing. The string current is related to the operation of devices and if the string current drops to a specific level, the device cannot operate properly. Therefore, it is very important to have high quality microstructure that is large-grained and less-defective of vertical channel in VNAND for the next-generation VNAND for high bit densities as well as the devices currently in use.

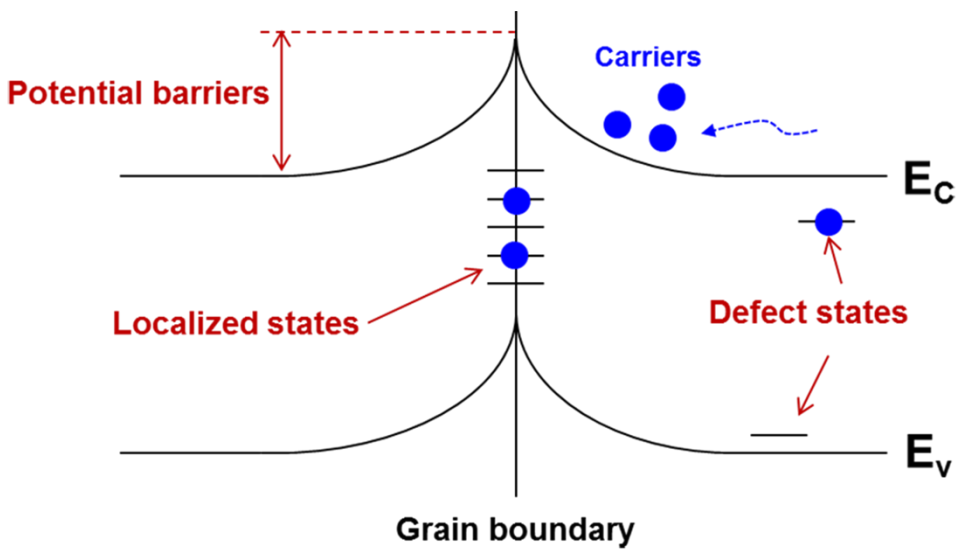


Figure 1.8 The schematic of band diagram of poly-crystalline film containing microstructural defects like grain boundaries, twins and stacking faults.

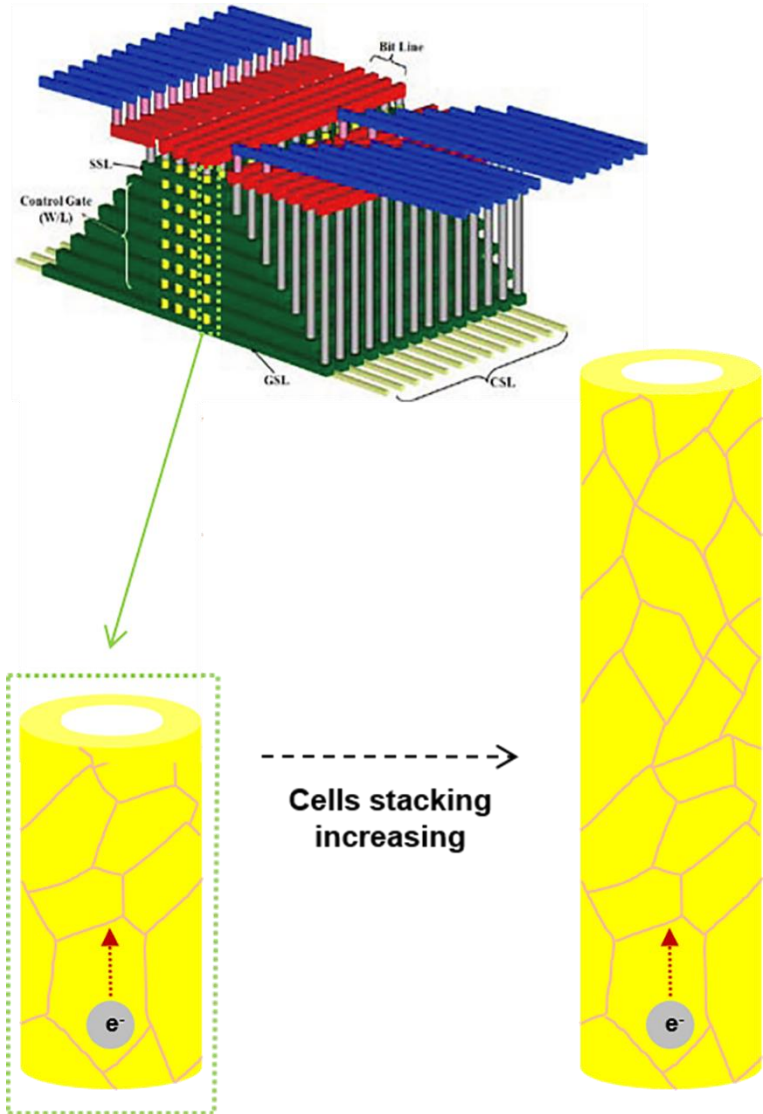


Figure 1.9 The expected microstructural schematics of poly-crystalline vertical channel when the number of cell layers is increased.

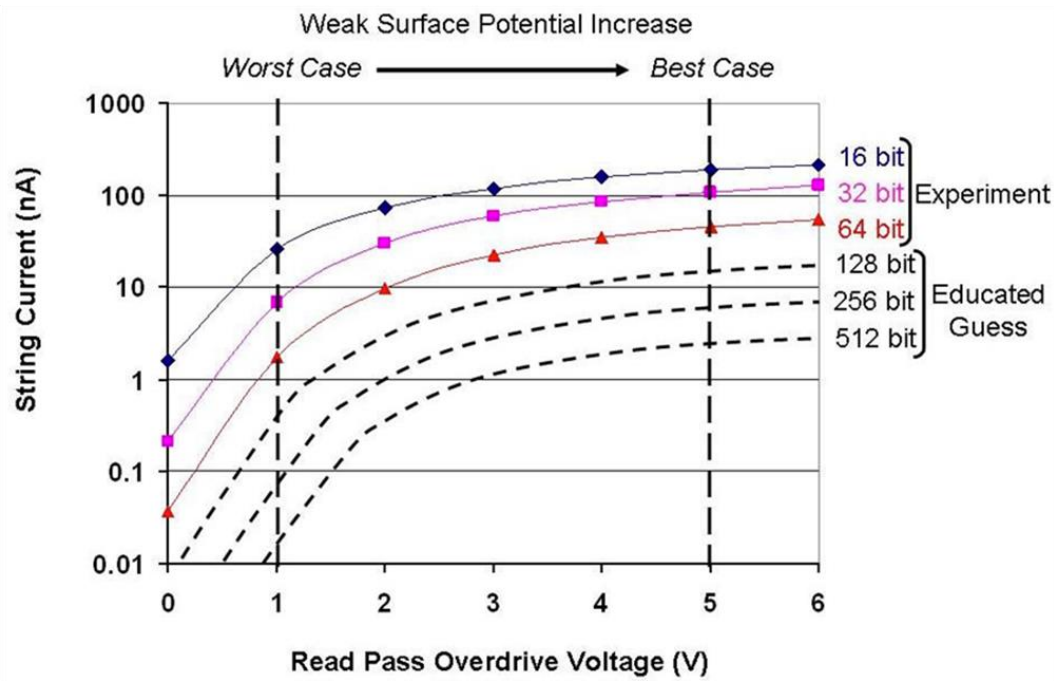


Figure 1.10 The string currents with a polycrystalline channel measured as a function of read pass overdrive voltage for different string lengths.[27]

1.5 **Thesis contents and organization**

This thesis is composed of experimental results and discussions about the research for obtaining the high quality poly-crystalline Si channel microstructure for vertical channel in VNAND based on the observation and characterization of crystallization behavior and the microstructure. It contains two big parts as per subject of research depending on the proposed vertical channel structure and the annealing methods.

I. SPC of $Si_{1-x}Ge_x$/Si bi-layer: I proposed the $Si_{1-x}Ge_x$/Si bi-layer for vertical channel structure to replace the conventional Si single layer structure currently being used. The bi-layer is very simple and easy method and also directly utilized to the current VNAND process. The crystallization behavior and film microstructure were examined in terms of applicability to VNAND process and microstructural quality of channel layer. The crystal quality enhancement of Si channel layer in a bi-layer structure in terms of crystallization mechanism will be mentioned and discussed in detail compare to conventional the Si single layer structure.

II. Grain growth of poly-crystalline Ge: I proposed poly-crystalline Ge single layer as vertical channel structure. The Ge has advantages as a channel material through the crystallization process because it shows lower crystallization temperature and higher carrier mobility than Si. The

as-deposited poly-crystalline Ge is annealed through the rapid thermal annealing system and their crystallization behavior is characterized. The surface-energy-driven secondary grain growth technique for poly-crystalline Ge as an initial microstructure was utilized in this experiment in order to obtain large-grained microstructure over the film thicknesses. Additionally, two-step annealing method was proposed to get the even large-grained microstructure in a given VNAND thermal budget by combining RTA and furnace processes.

2 Crystallization Techniques for Vertical Channel in VNAND

2.1 Solid phase crystallization

2.1.1 Crystallization of amorphous Si

The amorphous Si is in a metastable state. The crystalline Si is a stable than the amorphous Si. There is a driving force in an amorphous Si to be a stable crystalline Si. As shown in Figure 2.1, it requires the thermal and/or strain energies to become crystalline from amorphous Si.

The crystallization of amorphous Si proceeds through the two stages which are nucleation and growth, respectively. The Figure 2.2 is the schematics of amorphous Si crystallization process as time evolves in the thermal annealing process. As shown in Figure 2.2(a), the nucleation occurs in order to lower the total energy of a film when the thermal energy is provided. The continuous annealing induces a growth from the generated nuclei. Also, additional nucleation can occur elsewhere from the growing grains as shown in Figure 2.2(b). Figure 2.2(c) shows the growing grains. Such grains growth continue until the impingement to the adjacent growing grains and when the all the area of film completes such grain impingements as shown in Figure 2.2(d), it can be seen that the film is fully

crystallized.

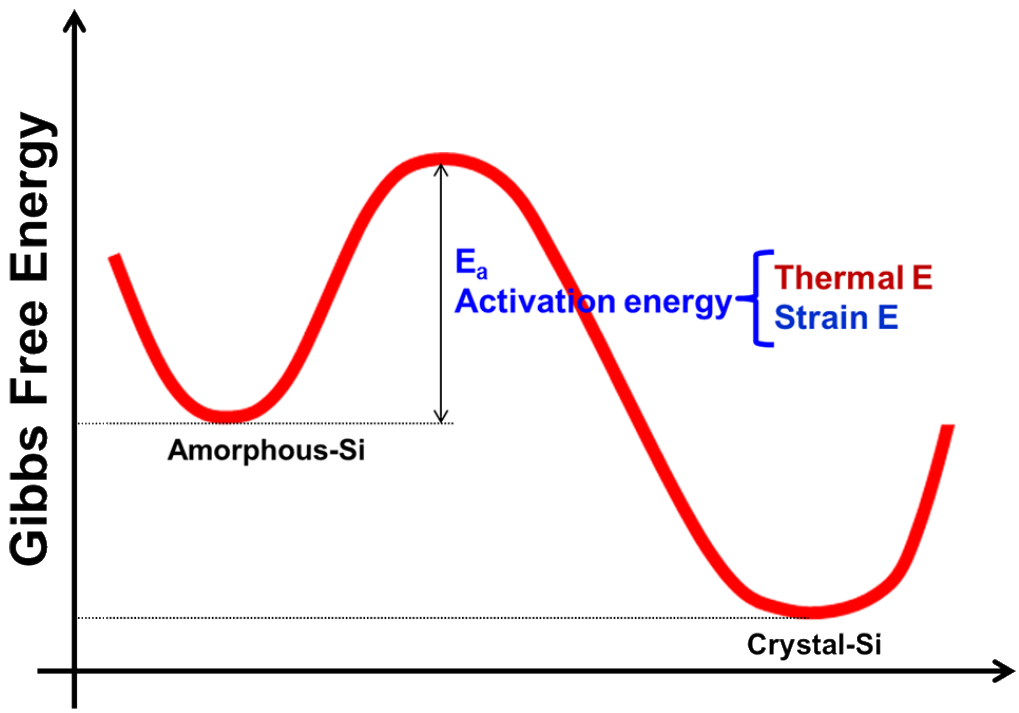


Figure 2.1 The Gibbs free energy of amorphous and crystal Si.

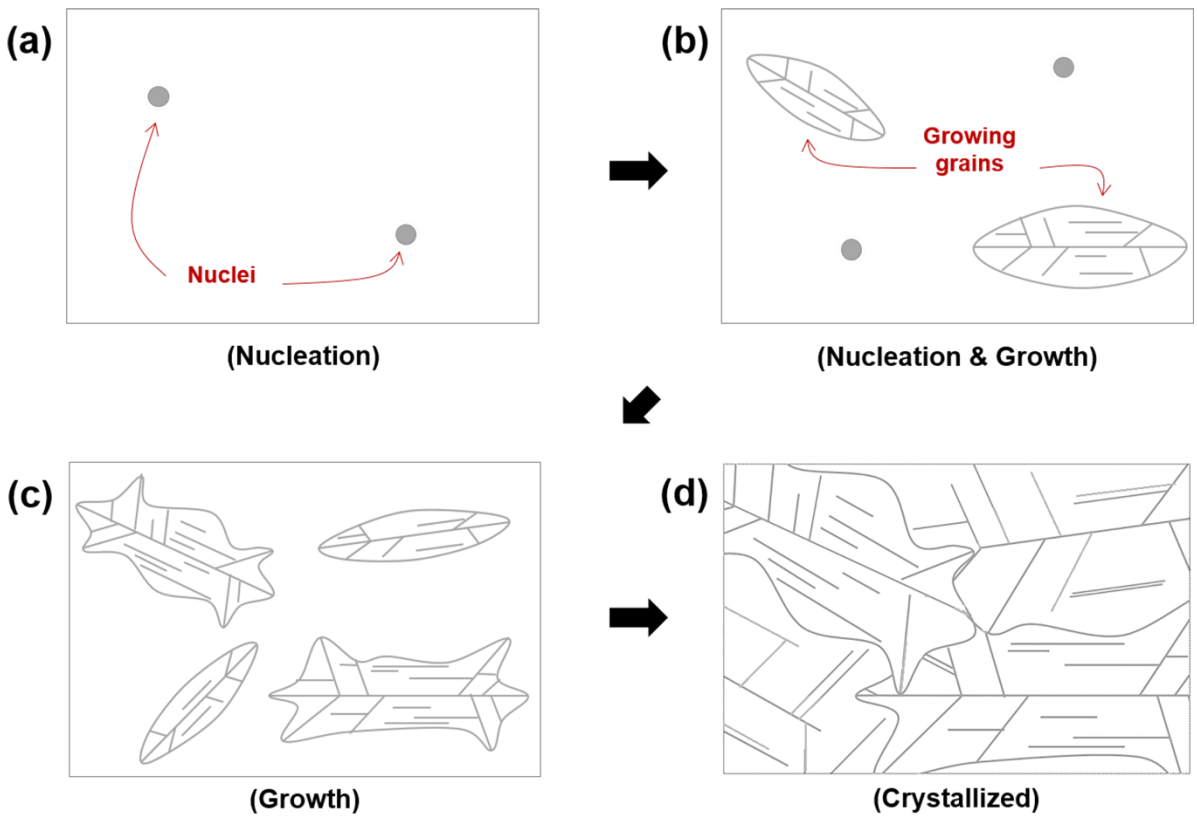


Figure 2.2 The schematics of Si SPC process. When the amorphous Si film is annealed, it crystallized through the nucleation and growth, respectively.

2.1.2 Thermodynamics of Si SPC

Figure 2.3 shows the total free energy change as a function of nuclei radius in a film during (a) solidification and (b) SPC (diffusional transformation in solids) processes. During solidification, total free energy change (ΔG) can be expressed as the following equation below.

$$\Delta G = -V\Delta G_v + A\gamma \quad [2\text{-}1]$$

Where V is the volume of generated nuclei, ΔG_v is volume free energy change, A is the interface of generated nuclei and γ is the interface energy between solid and liquid phases. On the other hand, in the case of SPC, film crystallizes through the diffusional transformation from amorphous to crystal in a solid state. During the phase transformation, most of the transformed volume does not fit perfectly into the film matrix. Therefore, the misfit strain energy per unit volume ($V\Delta G_s$) is generated. This phenomenon adds strain energy change to the total free energy variation as shown in Figure 2.3(b). The ΔG in SPC can be expressed as below.

$$\Delta G = -V\Delta G_v + A\gamma + V\Delta G_s \quad [2\text{-}2]$$

This is the one of the major difference between SPC and solidification process.

The nucleation rate (N) means number of clusters (nuclei) per volume and time. The growth rate (v_g) is represented by the grown distance of grain per time during the growth. In the SPC process, the nucleation and growth rates are as follows.

$$N \propto \left(\frac{1}{T}\right) exp[-(E_d + \Delta G^*)/kT] \quad [2\text{-}3]$$

$$v_g \propto exp[-(E_d + \Delta G/2)/kT] \quad [2\text{-}4]$$

Where T is the annealing temperature, E_d is the energy to break the atomic binding for atomic migration. The ΔG^* is the Gibbs free energy variation value at a critical nuclei size. According to the R. B. Iverson *et al*.,[18] the final grain diameter (d_f) of crystallized film through the SPC has the following relationship.

$$d_f \propto (v_g/N)^{1/3} \quad [2\text{-}5]$$

Based on the Equation 2-5, it requires lower nucleation and/or higher growth rate in order to obtain the large-grained microstructure.

The nucleation and growth rate can be controlled during the SPC by the process factors that configure Equation 2-3 and 2-4. The T can be changed through the annealing temperature control in a furnace or rapid thermal annealing system. The E_d can be varied depending on the deposition conditions such as deposition temperature or pressure and also for the materials for deposition. The ΔG_s can be controlled depending on the film structures.

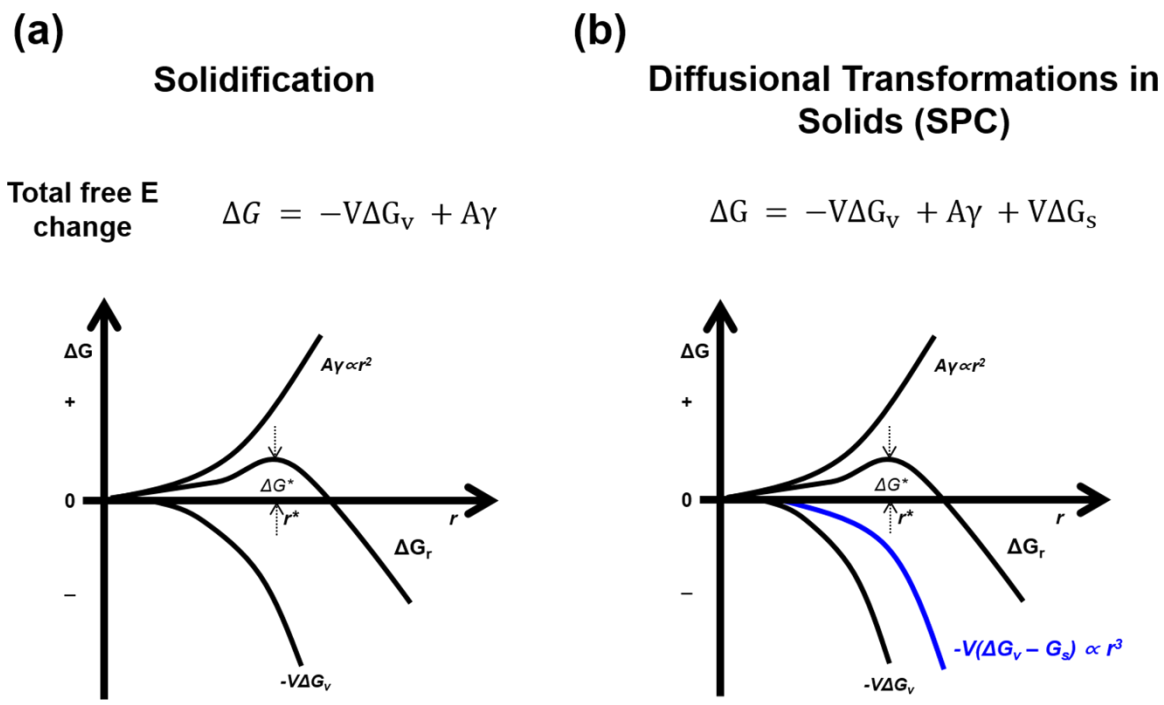


Figure 2.3 The total free energy change as a function of nuclei size during the nucleation for (a) solidification and (b) SPC (diffusional transformation in solids) processes.

2.1.3 Microstructure of solid phase crystallized Si film

The Si SPC has been extensively utilized for poly-TFT fabrication process.[20, 28-30] As mentioned in the previous chapter 2.1.2, the Si SPC should proceeds in the temperature range where possible for both lower nucleation and higher growth rate in order to obtain large-grained microstructure in a film. Moreover, the process temperature is required under glass transition temperature when the Si SPC is applied to the TFT process because it is fabricated on the glass substrate for display applications. When considering those two conditions, it is necessary some optimized temperature for Si SPC and that is around 600 ^{o}C.

Figure 2.4 is the schematics of grains morphology during Si SPC as time evolves in the 600 ^{o}C annealing.[31] The 600 ^{o}C is relatively low temperature when considering Si melting point (T_M of Si – 1413 ^{o}C). The lower thermal energy is provided during the SPC. Due to the insufficient energy for Si crystallization, the growth proceeds by forming the boundaries which has low formation energy especially like {111} twins.[19] This twin boundaries has <111> and <211> to the perpendicular and parallel direction, respectively. In the Si diamond structure, the <111> has the lowest growth rate than any other directions due to the highest density of atoms in a plane. Therefore, when the Si growth proceeds, the grains show elliptical shape after time evolution as shown in Figure 2.4(a). The grains grow continually by generating micro-twins. By the created micro-twins and faster growth rate of <211> than <111>, the Si grains show dendrite shape as shown in

Figure 2.4(b). This is the characteristics of conventional (600 ºC annealing) Si SPC related to the growth mechanisms. By this mechanism, it leads to very high density of twins in the fully crystallized Si film. It is expected that one of the major factors that lowers carrier mobility in the solid phase crystallized film even though their large grain size compare to excimer laser annealed films.[32]

However, that elliptical microstructure can be varied from elliptical to equiaxial shape depending on the process conditions. Figure 2.5 shows the process of (a) the high temperature annealing and (b) the Ge incorporation into the Si film that makes $Si_{1-x}Ge_x$ alloy. The equiaxial microstructure is shown by the high temperature annealing over 850 ºC in Si SPC.[33-35] Making $Si_{1-x}Ge_x$ alloys by Ge incorporation is another method for obtaining the equiaxial microstructure.[31, 36-41] Figure 2.5(c) shows the grain shape as a function of Ge contents in the $Si_{1-x}Ge_x$ alloy.[37] As the Ge contents increasing, the value of long/short axis of grains is getting close to 1.0 which means the grain shape is equiaxial. Figure 2.5(d) and (e) shows the corresponding plan-view TEM images of Figure 2.5(c) that Si and $Si_{0.47}Ge_{0.53}$, respectively. Unlike elliptical microstructure, there is no clear analysis for mechanisms about the formation of equiaxial microstructure yet. According to the presented hypothesis by using $Si_{1-x}Ge_x$ alloy as an example[37], the Ge incorporation lowers melting point of $Si_{1-x}Ge_x$ that introduces relatively higher thermal energy to the film during the crystallization. Finally, it has sufficient thermal energy to the atomic migrations and can grow randomly by generating few twin boundaries. Therefore, the equiaxial microstructure shows relatively lower density of twins in

the grains and it is expected to show higher carrier mobility than the elliptical microstructures which has high density of twins in a grain.[37]

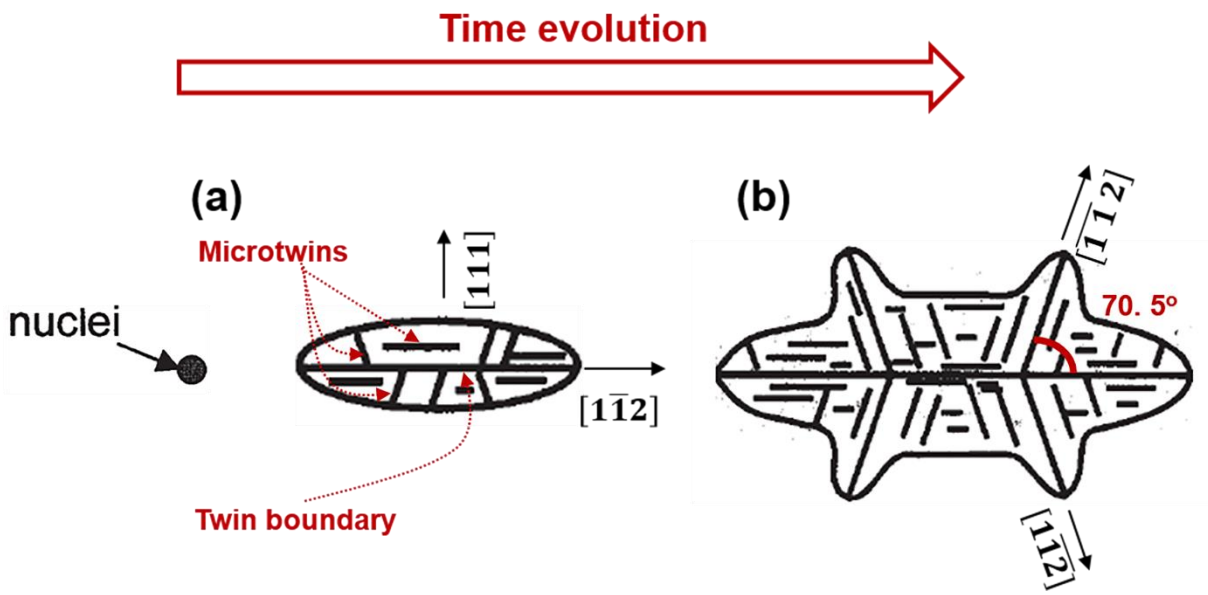


Figure 2.4 The microstructural evolution of Si grain in the conventional SPC process (600 °C annealing).[31]

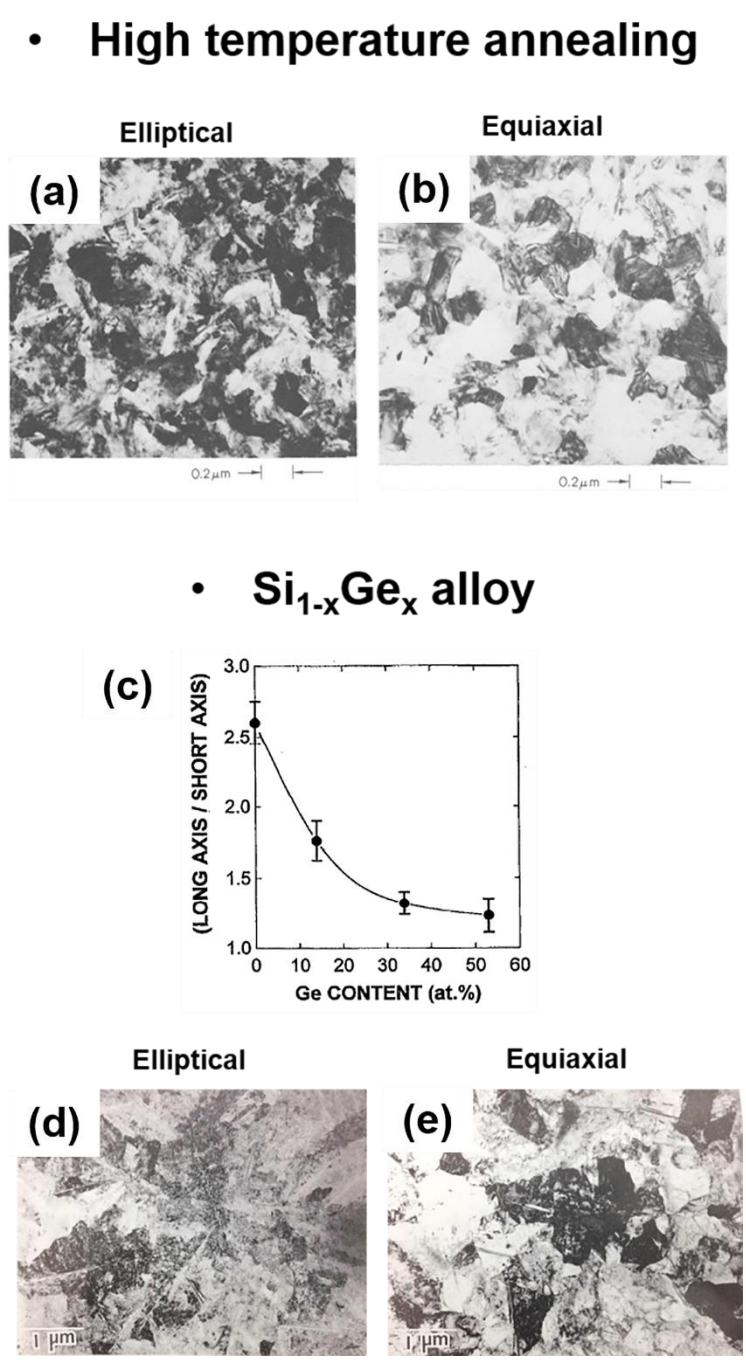


Figure 2.5 The plan-view TEM images of amorphous Si film annealed at (a) 800 and (b) 1200 ^{o}C.[35] The (c) ratio of the long to the short axis length of the grains as a function of Ge content in the $Si_{1-x}Ge_x$ film annealed at 600 ^{o}C and the corresponding plan-view TEM images of (d) Si and (e) $Si_{0.47}Ge_{0.53}$ film.[37]

2.1.4 Limitations of Si SPC techniques for VNAND process

Numerous researches[20, 42-50] have been carried out in order to obtain the high quality poly-crystalline Si film based on the characteristics of SPC and related microstructure which were explained in the previous chapters. The high quality poly-crystalline film means the large-grained and/or less-defective microstructure. So far, various SPC techniques were proposed and those techniques can be achieved by adding an additional processes or modifying the film structures.[20, 46-51] Their microstructure quality is improved compared to conventional Si SPC process. I classified those techniques depending on their mechanisms. Those are selective and surface crystallization techniques.

Figure 2.6 is the schematic images of selective [(a), (b)][20, 46, 47] and surface crystallization [(c), (d)][48-51] techniques. Figure 2.6(a) is the process sequence schematics of selective MIC.[46, 47] The metals are selectively deposited on the film surface through the patterning process which was designed for selected nucleation site. Then the crystallization proceeds via MIC from the metal islands. During crystallization, the nucleation in the other amorphous region is suppressed except metal diffusion. Figure 2.6(b) indicates other selective crystallization technique. The single nuclei are formed by the Si pre-implantation process on a patterned surface of as-deposited poly-crystalline film.[20] The selectively amorphized Si film is crystallized though the growth only without nucleation from the remained nuclei

that acts as seeds. Those techniques control the location of grain boundaries by adopting initial nucleation or growth site and finally obtain the large-grained microstructure.

Figure 2.6(c) and (d) indicates the surface crystallization techniques. The initial nucleation site of conventional LPCVD deposited amorphous Si film on SiO_2 is interface between film and substrate.[19, 51-53] It is due to the some crystallites near the interface that acts as growth site during crystallization. Another cause is the thermal coefficient difference between Si and SiO_2. Due to this differences, the large amount of strains exist near the film interface. The higher stain rate at the interface preferentially induces the nucleation. The surface crystallization techniques are the method that control the initial nucleation site from the film interface to the surface and shows the high quality poly-crystalline microstructure. Figure 2.6(d) shows the cantilever structure.[48] When this structure is annealed the large and less-defective grains are detected on the intentionally formed surface compare to grains formed at the Si and SiO_2 interface. It is explained due to the small amount of strains and free surface effects at the intentionally formed surface that leads to lower nucleation and higher growth rate and stress relief to the surface, respectively during crystallization. Figure 2.6(d) shows film structure contains the high concentration of oxygen at the interface.[51] The oxygen is blown in the initial stage of Si film deposition and gradually decreased to zero. The oxygen is blown to suppress nucleation. After annealing, the nucleation occurs at the surface not the interface in that structure. The grown grains show the relatively large size and

equiaxial shape. This variations are also explained by the lower strain rate at the surface and free surface effects. Table I summarized the Si SPC techniques for process, mechanism and final microstructure of the selective and surface crystallization techniques.

Those SPC techniques are effective for channel layer formation because they show the high quality poly-crystalline film as a final microstructure. It would improve the electrical properties. However, those techniques cannot be applied to the VNAND process by the following reasons. Table II shows the expected issues of those SPC techniques when applying for the VNAND process. When considering `punch and plug` process of VNAND, patterning process cannot be applied. Except patterning process, other additional processes also have problem for applying VNAND process. Eventually, in order to obtain high quality poly-crystalline Si film as a channel microstructure, another SPC techniques or channel structure is required.

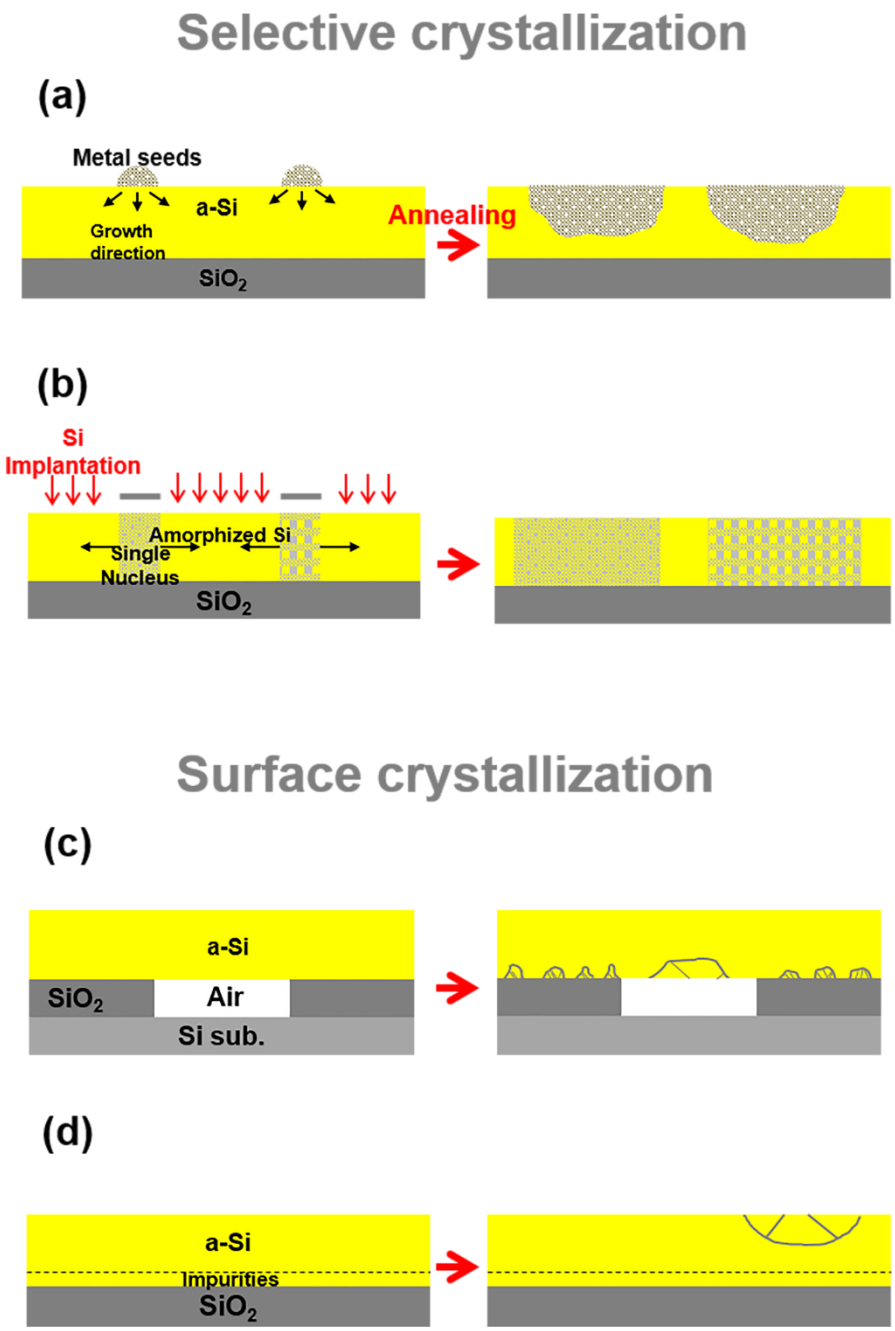


Figure 2.6 The selective and surface crystallization techniques. The (a) metal islands are selectively deposited on the top Si surface.[46, 47] The (b) as-deposited poly-crystalline Si film is selectively amorphized via Si pre-implantation process.[20] The (c) air gap is intentionally formed in the middle of SiO_2 between Si film and substrate.[48] The (d) oxygen was blown at the initial deposition period and the gradually decreased to zero.[51]

Classification	Process	Mechanism	Final microstructure
Selective Crystallization	Metal islands on the top surface	Location control of grain boundaries	Large-grained microstructure
	Self-implantation to poly-crystalline and subsequent SPC		
Surface Crystallization	Underlying air-gap formation	Lower N & higher υ_g, Stress relief to the surface	Larger-grained and less defective or equiaxial microstructure
	Impurity (Oxygen) incorporation		

Table i The process, mechanism and final microstructure of selective and surface crystallization techniques are summarized.[20, 46-51]

Classification	Process	Expected issues for VNAND process
Selective Crystallization	Metal islands on the top surface	Patterning, metal contamination
	Self-implantation to poly-crystalline and subsequent SPC	Patterning, implantation
Surface Crystallization	Underlying air-gap formation	Patterning, complex structure
	Impurity (Oxygen) incorporation	Oxygen impurities near the channel region

Table ii The expected issues of selective and surface crystallization techniques for vertical channel formation process in VNAND.

2.1.5 $Si_{1-x}Ge_x$/Si bi-layer structure for vertical channel in VNAND

As an advanced SPC technique for the vertical channel formation in VNAND, I proposed the bi-layer as a channel structure. Figure 2.7 shows the proposed bi-layer structure. The bi-layer can be fabricated by the sequential deposition of nucleation layer on the Si channel layer through the source gas change in a same chamber of deposition system. Therefore, it is directly applicable to the VNAND process and also very simple and easy method. As a nucleation layer, I proposed $Si_{1-x}Ge_x$ by the following reasons. The $Si_{1-x}Ge_x$ has the same crystal structure to Si. The melting point of $Si_{1-x}Ge_x$ is lower than Si that can induce pre-crystallization in the $Si_{1-x}Ge_x$ prior to Si. The $Si_{1-x}Ge_x$ can be selectively removed via wet etching process.[54] Also, the $Si_{1-x}Ge_x$ can induce the equiaxial microstructure which shows lower density of intra-grain defects especially like twins. The experimental details, results and discussions will be treated in the Chapter 3.

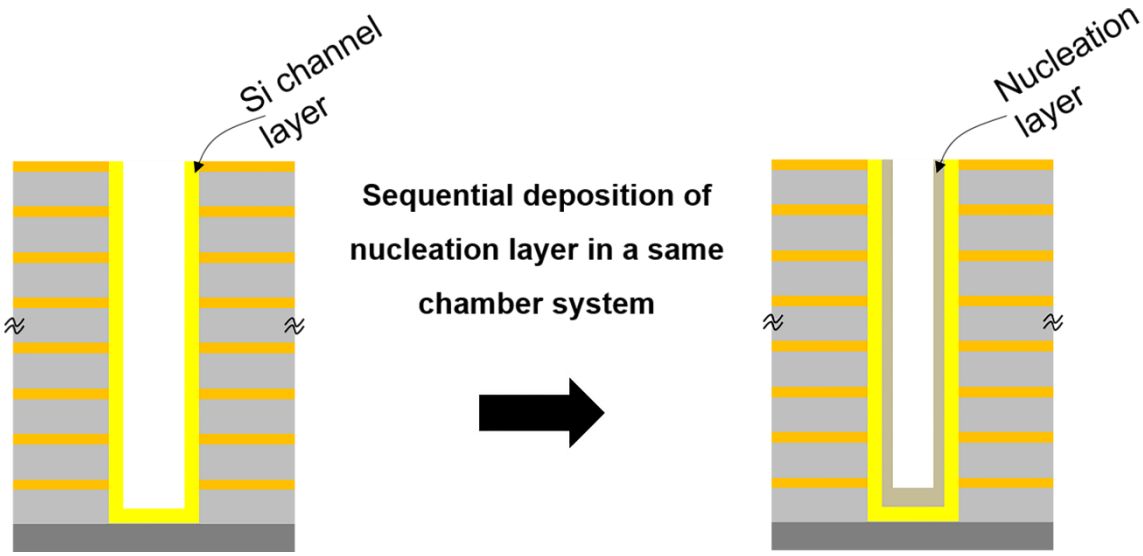


Figure 2.7 The cross-section schematics of proposed bi-layer structure as an advanced Si SPC technique for vertical channel formation in VNAND.

2.2 Grain growth

2.2.1 Poly-crystalline semiconductor film

Semiconductor-on-insulator (SOI) structures can be fabricated by the growth of semiconductor film on insular (sapphire) substrates[55], wafer bonding[56], recrystallization from the melt process[57-60] and the deposition semiconductor film on insulator substrate like glass or quartz by using low pressure chemical vapor deposition (LPCVD) system[61]. Among them, the LPCVD method is widely used due to its advantages that are low cost and large area available with good uniformity. There exists the deposition transition temperature from amorphous to poly-crystalline in the deposition process of LPCVD. The transition temperature can be varied depending on the deposition pressure or type of source gases.[61] When the film is deposited under transition temperature, the deposited film shows amorphous state. On the other hand, when deposited over the transition temperature, the film exhibits poly-crystalline state and its microstructure is composed of fiber-like structure with smaller size of grains than the film thicknesses.

The poly-crystalline film has high density of grain boundaries. When it used as channel material, it shows poor electrical properties due to grain boundaries that forms localized states and potential barriers as explained in the previous chapter

1.4. The method for reducing the density of grain boundaries is the post annealing. When the as-deposited poly-crystalline film is annealed, the grain growth happens through the movement of grain boundaries. There are two kinetics of grain growth that are normal and abnormal (or secondary) grain growth. Figure 2.8 shows the microstructure evolution of (a) normal grain growth until completion and (b) at the early stage of secondary grain growth. The phenomenology and kinetics of them will be explained in the next chapters.

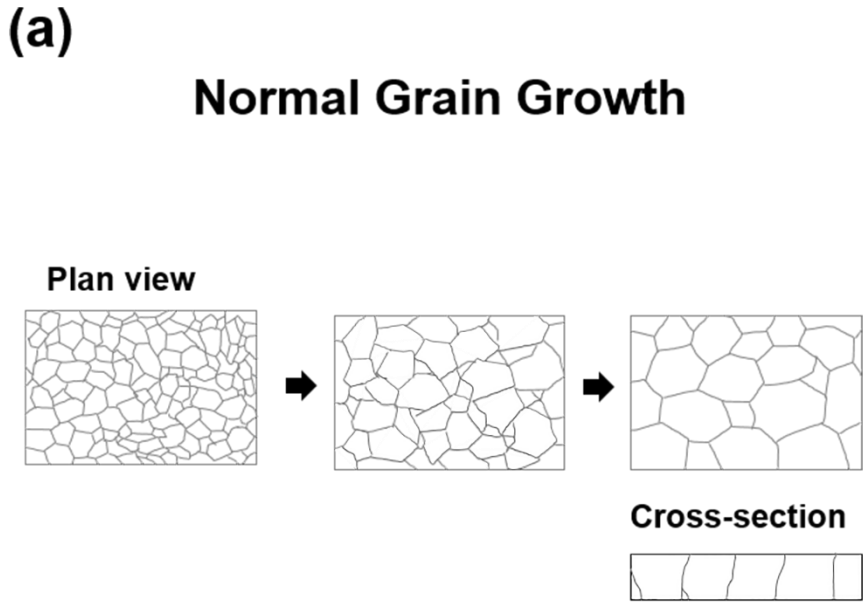


Figure 2.8 The schematics of microstructural evolution of (a) normal grain growth and (b) abnormal (or secondary) grain growth.

2.2.2 Normal grain growth

When the as-deposited poly-crystalline film is annealed, the normal grain growth proceeds. It is continued through the grain boundary energy reducing of film. The normal grain growth rate is expressed as follows.

$$r_n = M\Delta F_n \quad [2\text{-}6]$$

Where r_n is the normal grain growth rate, M is the grain boundary mobility and ΔF_n is the driving force for normal grain growth. The M is expressed as below.

$$M = M_0 e^{(\frac{-Q}{\kappa T})} \quad [2\text{-}7]$$

Where M_0 is weekly temperature-dependent constant, Q is the activation for grain boundary movement, κ is the Boltzmann constant and T is the annealing temperature. Even though several factors exist as driving forces for normal grain growth, when considering the grain boundary energy reduction is the dominant factor, the grain boundary curvature has strong influence. This is called 'capillarity effect'.[62] The normal grain growth rate is rapidly decreased when the average grain size of film is reached to the film thicknesses as shown in Figure 2.8(a) and it is known as 'sample thickness effect'. The origins of that phenomenon are reduced grain boundary curvature, disturbance of grain boundary migration by thermal grooves and local oxidation at the intersection of grain boundaries. The monomodal shape is examined for the number of grains as a function of grain sizes.

It follows log-normal distribution[63] when the normal grain growth is saturated or completed.

2.2.3 Secondary grain growth

The normal grain growth saturated film is consists of columnar grains as shown in the cross-section schematic of Figure 2.8(a). The normal grains have their own surface energy based on their orientations. That is the function of atomic density in a plane. The relative surface energy in the case of diamond structure such as Si and Ge is shown in Figure 2.9.[64] The randomly oriented normal grains are equally distributed in the whole film area. Then, the surface energy anisotropy is generated due to the randomly oriented normal grains. At this stage, when the high temperature or strain is induced to the film, some specific grains grow by consuming adjacent grains. It is expressed as schematics in Figure 2.8(b) and this phenomenon is called as abnormal or secondary grain growth. In the early stage of secondary grain growth, the grain size distribution would show bimodal shape.[63, 64]

Thompson *et al*.[63-69] studied the secondary grain growth by using SOI structures like Si or Ge as an application of channel for electronic devices. Thompson *et al*.[65] suggested that the main driving force for secondary grain growth is the surface energy reduction of film and named it as surface-energy-driven secondary grain growth (SEDSGG). The growth rate of SEDSGG is as follows.[64]

$$r_s = M\Delta F_s \quad [2\text{-}8]$$

Where r_s is the secondary grain growth rate. The ΔF_s is the driving force for secondary grain growth and expressed as follows.

$$\Delta F_s = -\frac{2\Delta\gamma - \gamma_{gb}}{h} \quad [2\text{-}9]$$

Where γ_{gb} is the average grain boundary energy and h is the film thickness. The $\Delta\gamma$ is expressed as follows.

$$\Delta\gamma = \bar{\gamma} - \gamma_{min} \quad [2\text{-}10]$$

Where $\bar{\gamma}$ is the average surface energy of normal grains and γ_{min} is the secondary grains with minimum surface energy growing into the matrix of stagnant normal grains. Based on the Equations from 2-7 to 2-10, the size of secondary grain are influenced by the some factors that affecting the activation energy of grain boundary movement (Q), initial microstructure of film ($\Delta\gamma$), film thickness (h) and annealing temperature (T). In the case of annealing temperature, the SEDSGG was carried out in the temperature range around 1200 ºC and above 900 ºC for Si and Ge, respectively.[63, 65, 67-69] It is relatively very high temperature when considering the melting point of materials.

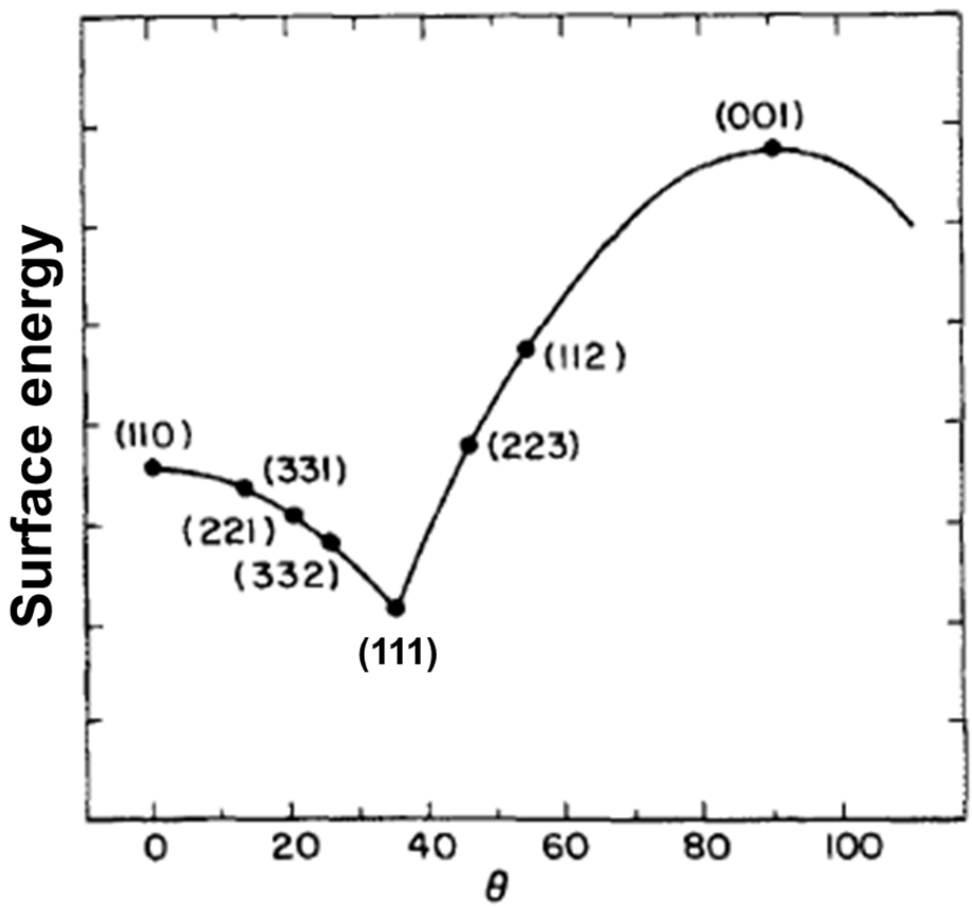


Figure 2.9 The relative surface energy of Si, Ge diamond crystal structures depending on their orientations.[64]

2.2.4 Ge SEDSGG for vertical channel in VNAND

The germanium has same crystal structure to silicon. Germanium shows higher carrier mobility both electrons and holes compare to silicon. Due to the lower melting point of germanium than Si, relatively lower temperature crystallization process is available using Ge as a channel material. As a vertical channel material for VNAND process, the Ge has technical issues related to the process compatibility for conventional process and the instability of germanium oxide. However, in terms of `Plug` process, there is not a big problem for Ge deposition instead of Si as a channel material.

The high temperature annealing is available in VNAND process because it is fabricated on the Si substrate unlike glass substrate fabricated devices like TFT. However, there also exists the device thermal budget of VNAND and it is known that about 850 ^{o}C for 30 minutes which is related to the dopant profile suppression of the select transistors. It would be advantageous for current flow when SEDSGG technique is applied to the vertical channel formation process due to the results of large grains sizes over the film thicknesses. As mentioned in the chapter 2.2.3, the SEDSGG temperature is relatively very high. When considering the device thermal budget of VNAND, the Si SEDSGG cannot be applied to the VNAND process. Whereas, the Ge SEDSGG looks available. In order to increase the current of vertical channel, I proposed poly-crystalline germanium single layer as a vertical channel structure for higher carrier mobility and combining it to the SEDSGG as a

crystallization technique in order to obtain the large grain size over the film thickness. The experimental results and discussions will be treated in the Chapter 4.

3 Solid Phase Crystallization of $Si_{1-x}Ge_x$/Si Bi-Layer

3.1 Crystallization behavior of $Si_{1-x}Ge_x$/Si bi-layer

3.1.1 Introduction

Vertical NAND (VNAND) flash memories like BiCS[3] and TCAT[5] have been considered one of the most promising solutions to the scaling limit issue affecting conventional two-dimensional flash memory. Poly-crystalline Si film formed by a solid phase crystallization (SPC) is used in VNAND as a vertical channel.[70, 71] As the number of vertically stacked cell layers increase for high bit densities, the string current characteristics of the extended vertical channel become degraded due to the existing grain boundaries and intra-grain defects in the solid phase crystallized film.[72] Therefore, the high quality poly-crystalline Si microstructure consists of large grains and low density of intra-grain defects is required for vertical channel of next-generation VNAND.

In the past several decades, many researchers have extensively proposed various SPC methods for macro-electronics such as thin-film transistors and photovoltaics. These enable the formation of large-grained and/or less-defective Si microstructure.[20, 46-48, 51] Selective nucleation and/or grain growth via artificial seed like metal (Ni, Al, etc.)[46, 47] or intentionally formed single nucleus[20] are the most

feasible suggestions to attain the precise location control of grain boundaries. In addition, the equiaxial microstructure via surface nucleation is likely to improve the channel mobility, since it has limited intra-grain defects unlike a conventional solid phase crystallized elliptical microstructure.[48, 51] However, these methods cannot be applied to the VNAND process due to patterning process,[20, 46-48] complicated structure[48] and impurity contamination issue[51].

Thus, I proposed advanced SPC using $Si_{1-x}Ge_x$/Si bi-layer structure especially focused on the TCAT process that can be easily integrated by the sequential deposition of amorphous Si and $Si_{1-x}Ge_x$ in the same chamber of deposition system. During the SPC, the $Si_{1-x}Ge_x$ layer acts as a selective nucleation site. In particular, it is used for surface nucleation[53], which can lead to large-grained and equiaxial microstructures along the total $Si_{1-x}Ge_x$/Si bi-layer. Furthermore, $Si_{1-x}Ge_x$ can be easily removed by a specific etchant without any damages to the underlying Si layer.[54] In this chapter 3.1, the experiment was carried out to observe and to characterize the crystallization behavior of bi-layer structure. The crystallization mechanisms and expected superiority of electrical properties of bi-layer structure in VNAND will be discussed in detail compare to the Si single layer structure being used for conventional vertical channel.

3.1.2 Experimental details

The amorphous $Si_{1-x}Ge_x$/Si bi-layer was sequentially deposited by using Si_3H_8 and

GeH_4 source gases in a low-pressure chemical vapor deposition (LPCVD) system on silicon dioxide on Si substrate at a deposition temperature was 480 ^oC. The deposited Si and $Si_{1-x}Ge_x$ layers were 21 and 20~25 nm thick, respectively. The Ge contents in the $Si_{1-x}Ge_x$ layer varied from 0.37 to 0.55. The bi-layer structures were annealed under nitrogen ambient in a mini furnace (SMF-800, Seoul Electron Inc.) system. The Si crystalline fractions were acquired by measuring the refractive index at 830 nm wavelength via a J. A. Woollam EC-400 spectroscopic ellipsometer. The surface roughness after $Si_{1-x}Ge_x$ wet etching was investigated via Park Systems, XE-100 atomic force microscopy (AFM) system. The transmission electron microscopy (TEM) samples for plan-view measurement were prepared by ion-milling method and cross-section samples were fabricated via focused ion beam system. In the TEM experiment, a JEOL JEM-3011 *in situ* TEM equipped with a double-tilting holder was used at 300 kV. The initial crystallinity of bi-layers were characterized by the cross-section transmission electron microscopy and selective area diffraction pattern (SADP). The cross-section *in situ* TEM measurement with heating was carried out in order to investigate the crystallization behavior of the $Si_{1-x}Ge_x$/Si bi-layer in a real time. Finally, a plan-view TEM measurement was carried out to investigate the film microstructure.

3.1.3 Results and discussions

Figure 3.1 shows the cross-section TEM image of the $Si_{1-x}Ge_x$/Si bi-layer structure. Generally, pre-existing nano-crystallites at the interface in the as-deposited film may act as a nucleation or growth site during SPC and directly affect the film microstructure.[21] Hence, the initial crystallinity of as-deposited films was investigated by the cross-section TEM before annealing. As shown in Figure 3.1, no nano-crystallites were observed in the $Si_{1-x}Ge_x$ and Si layers and the SADP halo pattern in the inset of Figure 3.1 indicates that entire layers are composed of only amorphous phases.

Figure 3.2 shows the crystalline fraction of Si layer as a function of annealing time and Ge contents of $Si_{1-x}Ge_x$ nucleation layer. The samples were wet etched to selectively remove the $Si_{1-x}Ge_x$ nucleation layer after annealing. The crystalline fractions were acquired by using the Temple-Boyer *et al.* method[73] and set as zero percent when the Si layer is amorphous (as-deposited state) and one-hundred percent when it is fully crystallized. In the case of the conventional Si SPC, it has been reported that the incubation time for nucleation takes a few hours at 600 ^{o}C.[18, 37] In this experiment, the incubation time were observed in two hours as shown in Figure 3.2. This is consistent with previous TEM results (Figure 3.1), since the early nucleation or growth should take place without sufficient incubation time if there are any crystallites in the film. The time to begin and completion of Si crystallization were gradually shortened as the Ge contents increased in the $Si_{1-x}Ge_x$ nucleation layer. This agrees with thermodynamics in that $Si_{1-x}Ge_x$ film with higher Ge contents would be crystallized earlier in a same annealing temperature. It

also implies that the $Si_{1-x}Ge_x$ layer can act as a nucleation site.

The cross-section *in situ* TEM measurement was performed to observe the crystallization behavior of the $Si_{1-x}Ge_x$/Si bi-layer structure. Figure 3.3 shows the cross-section *in situ* TEM images and SADPs in the identical position of bi-layer structure annealed at 600 ºC in a TEM chamber. As shown in Figure 3(a), the nucleation selectively took place on the $Si_{0.45}Ge_{0.55}$ surface in 19 minutes. The $Si_{0.45}Ge_{0.55}$ grain growth from the nuclei proceeded down to the underlying amorphous Si layer. After 28 minutes, this crystallized $Si_{0.45}Ge_{0.55}$ acted as a seed for the subsequent crystallization of the underlying amorphous Si, which can be seen in Figure 3.3(b). This selective Si surface crystallization led to perpendicular growth until the impingement to the bottom SiO_2 and then some Si grains laterally grew as shown in Figures 3.3(c) and (d), respectively.

As identified in the *in situ* TEM results, when the bi-layer is annealed, the initial nucleation begins at the $Si_{0.45}Ge_{0.55}$ surface. The nuclei may have random orientations because they were generated on the amorphous native oxide (the native oxide of the SiGe surface was composed of mixed phase of SiO_x and GeO_x by X-ray photoelectron spectroscopy characterization). Therefore, when a bi-layer is continuously annealed, it causes impingements and occlusions among the neighboring $Si_{0.45}Ge_{0.55}$ grains due to the anisotropic growth rate of randomly oriented nuclei. Consequently, competitive growth[19, 74] take place along the vertical direction. Figure 3.4 shows (a) the bright and (b) the dark field cross-section TEM images of partially crystallized $Si_{0.45}Ge_{0.55}$/Si bi-layer in the identical position

annealed in an *in situ* TEM chamber at 600 ºC. Figure 3.4(a) indicates that the $Si_{0.45}Ge_{0.55}$ layer is crystallized and the Si layer is partially crystallized. The $Si_{0.45}Ge_{0.55}$ grains grow over $Si_{0.45}Ge_{0.55}$/Si interface as shown in Figure 3.4(b). The grain sizes were getting larger away from the initial nucleation site ($Si_{0.45}Ge_{0.55}$ surface) through the vertical direction. Such texture formation is believed due to the competitive growth effect by the grain impingement between neighboring grains with difference orientation during the initial growth.

For the underlying amorphous Si channel layer, the crystallization occurs via the epitaxy-like growth from the pre-crystallized $Si_{0.45}Ge_{0.55}$ layer as identified in Figure 3.3(b). When the growth proceeds to the bottom amorphous Si layer as shown in Figures 3.3(c) and (d), this epitaxy-like growth seems to suppress the nucleation in a Si layer during crystallization. Thus, the large-grained Si microstructure can be obtained near Si/bottom SiO_2 interface without any nucleation. This may be an advantageous for channel structure when applied to the VNAND process because channel region of each cell is located away from the $Si_{1-x}Ge_x$ nucleation layer.[5] Figure 3.5 shows the schematic cross-section images of (a) a conventional Si single layer structure and (b) a $Si_{1-x}Ge_x$/Si bi-layer structure of each cell transistor in TCAT structure. As shown in Figure 3.5(b), the large-grained Si microstructure region corresponds to the channel area of each cell transistors by the competitive and epitaxy-like growth. Meanwhile, the small grains may be obtained near Si channel/bottom SiO_2 interface for the conventional Si single layer channel structure as shown in Figure 3.5(a). This is because the nucleation would

begin at the interface between film and SiO_2 in a Si single layer structure.[52] Eventually, surface nucleation via the $Si_{1-x}Ge_x$ nucleation layer should be geometrically beneficial to the current flow in the vertical channel as well as each cell transistors of TCAT.

Figure 3.6 shows the plan-view TEM images of (a) a partially crystallized Si film of single layer structure, (b) a partially crystallized $Si_{0.45}Ge_{0.55}$ film and (c) a fully crystallized Si film of the $Si_{0.45}Ge_{0.55}$/Si bi-layer structure. As shown in Figure 3.6(a) the Si grains showed elliptical shape. However, the $Si_{0.45}Ge_{0.55}$ microstructure showed a completely different grain morphology that was equiaxial shape as shown in Figure 3.5(b). Such microstructural differences can be explained by growth mode variations due to the relatively lower melting point of the $Si_{0.45}Ge_{0.55}$ compared to the Si[37] and/or the ledge-assisted growth of the $Si_{1-x}Ge_x$ film[40]. In addition, Ryu *et al*.[51] obtained equiaxial grains when the initial nucleation site was intentionally changed from the film interface to the surface, even with Si SPC. Considering previous reports, the equiaxial grains in the $Si_{0.45}Ge_{0.55}$ layer are believed to be caused by both low melting point of $Si_{0.45}Ge_{0.55}$ and surface nucleation effect. Additionally, it has been reported that equiaxial grains via surface nucleation have relatively lower density of intra-grain defects such as twins and stacking faults, when compared to the elliptical grains.[37, 48] Elliptical grains have many intra-grain defects which are considered to be one of the main reasons for low carrier mobility.[19] Therefore, the equiaxial microstructure can be advantageous in increasing carrier mobility of films. The plan-view TEM

observation was carried out after etching the $Si_{0.45}Ge_{0.55}$ nucleation layer to investigate the underlying Si layer microstructure, which is the actual channel area in VNAND. As shown in Figure 3.6(c), the equiaxial microstructure as like partially crystallized $Si_{0.45}Ge_{0.55}$ layer was obtained in the Si layer. When considering the *in situ* TEM results [Figure 3.3(b)] where the Si crystallization was initiated from the pre-crystallized $Si_{0.45}Ge_{0.55}$ seeds, the underlying Si layer is thought to follow the microstructure of the $Si_{0.45}Ge_{0.55}$ layer by epitaxy-like growth. It may result the equiaxial microstructure of the underlying Si layer. It means that less-defective microstructure can be attained in the channel region of VNAND by using $Si_{1-x}Ge_x$ as a nucleation layer.

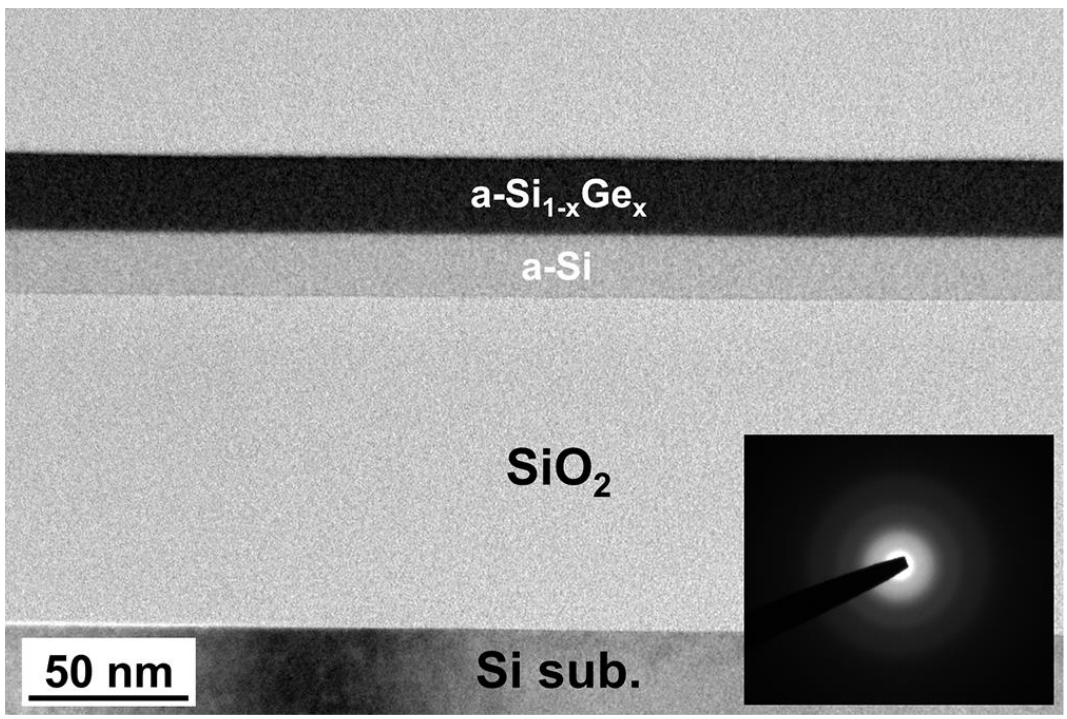


Figure 3.1 The cross-section bright field TEM image and SADP of the proposed $Si_{1-x}Ge_x$/Si bi-layer structure.

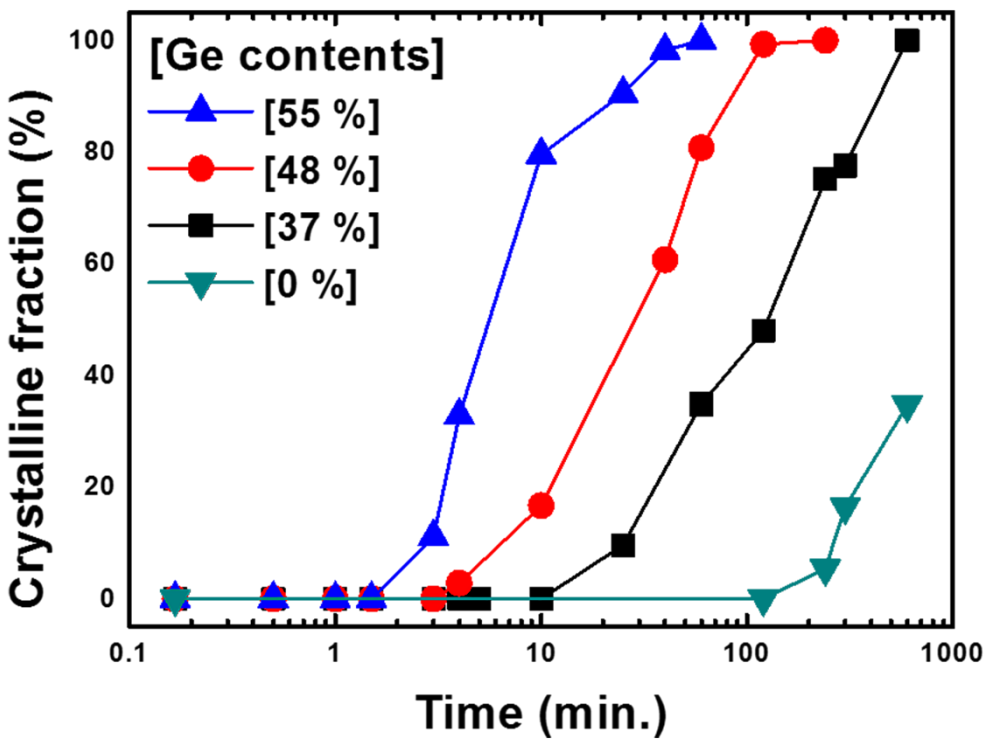


Figure 3.2 The crystalline fraction of Si layer as a function of Ge content and annealing time after $Si_{1-x}Ge_x$ layer removal in a bi-layer via wet etching process. The samples are annealed at 600 ^{o}C in the furnace system.

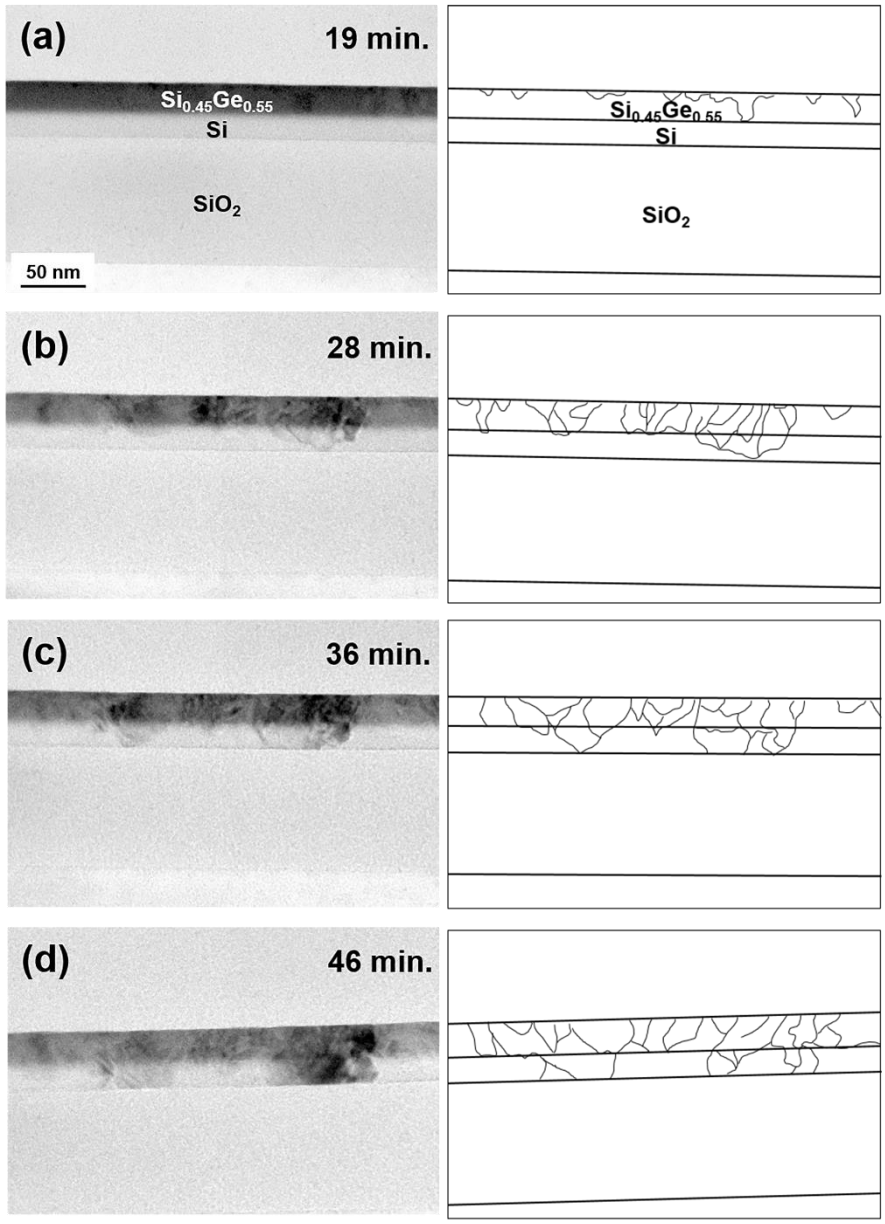


Figure 3.3 The *in situ* cross-section bright field TEM images and microstructure schematics of $Si_{0.45}Ge_{0.55}$/Si bi-layer in a TEM chamber annealed at 600 ºC. The images respectively show after the annealing time of (a) 19 min. – $Si_{0.45}Ge_{0.55}$ surface nucleation, (b) 28 min. – Si crystallization from the pre-crystallized $Si_{0.45}Ge_{0.55}$, (c) 36 min. and (d) 46 min. – Si grain growth and impingement to the bottom SiO_2.

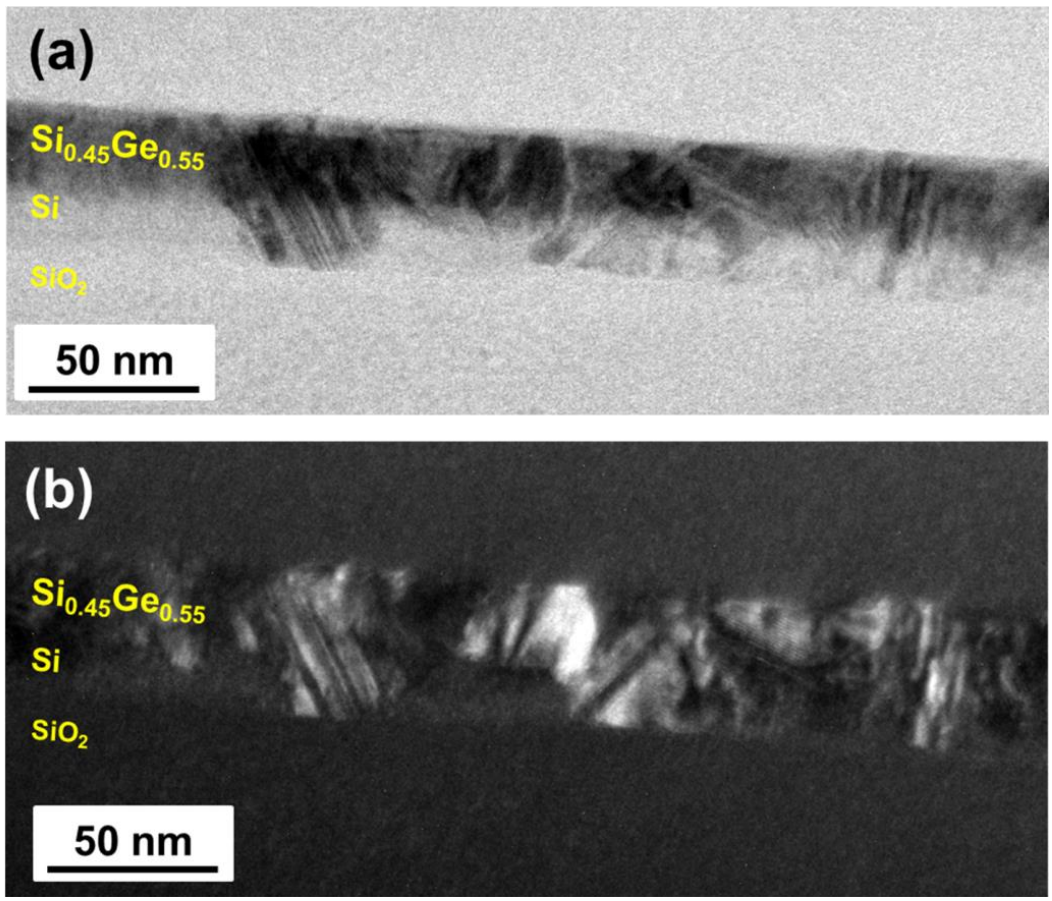


Figure 3.4 The cross-section (a) bright and (b) dark field TEM images of same position of partially crystallized $Si_{0.45}Ge_{0.55}$/Si bi-layer annealed in an *in situ* TEM chamber at 600 ^{o}C for 46 minutes.

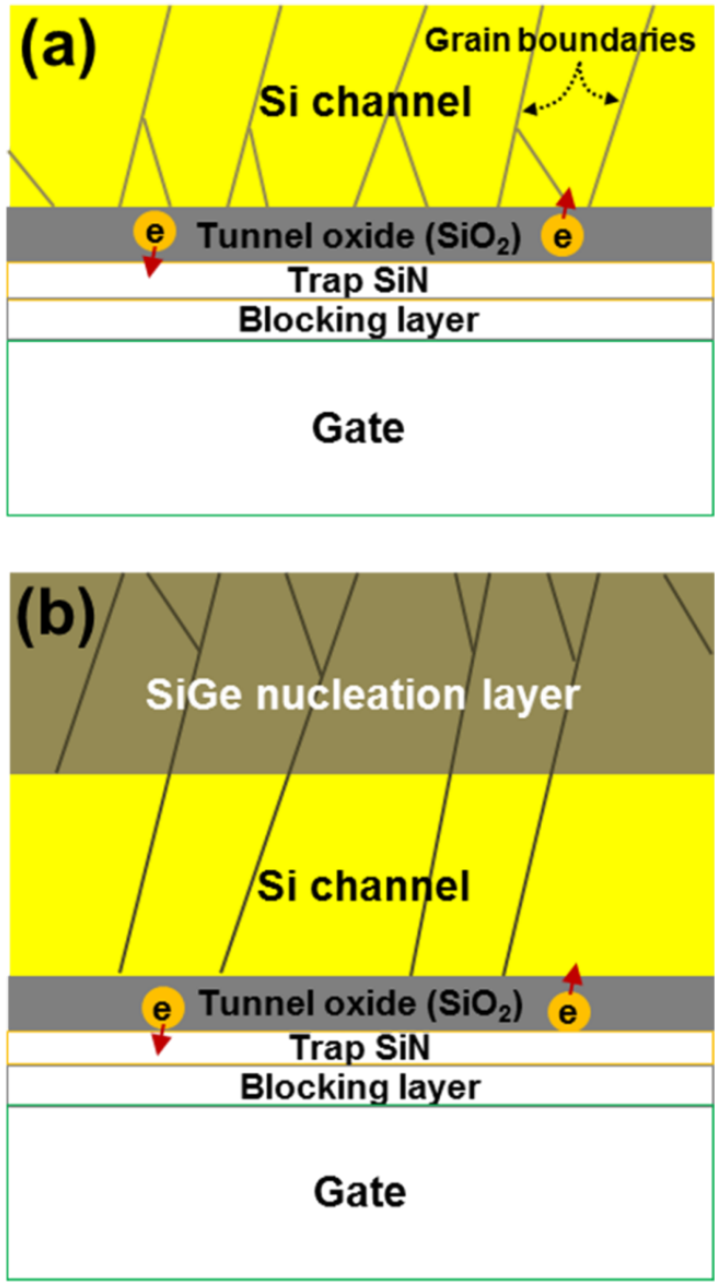


Figure 3.5 The schematic cross-section images of VNAND cell transistors for the vertical channel formation process as (a) a Si single layer and (b) a $Si_{1-x}Ge_x$/Si bi-layer structures.

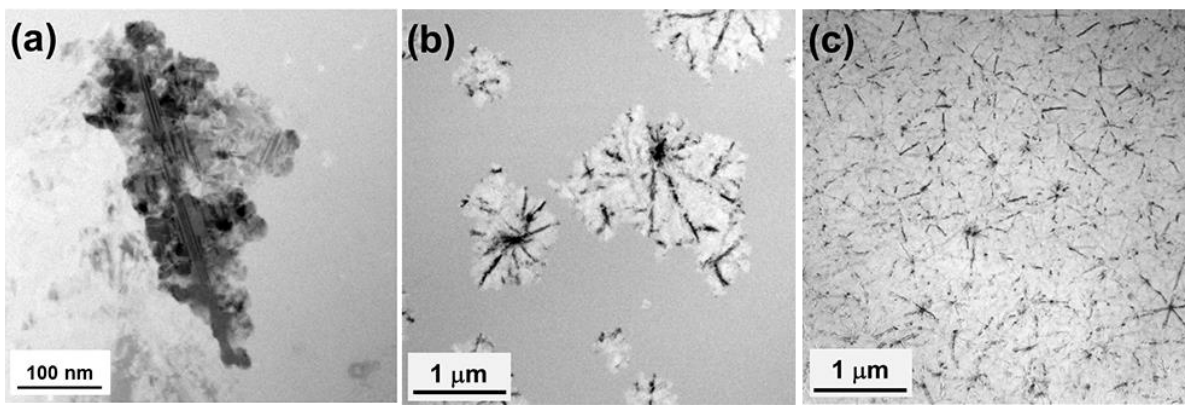


Figure 3.6 The plan-view bright field TEM images of (a) a partially crystallized Si film of Si single layer structure, (b) a partially crystallized $Si_{0.45}Ge_{0.55}$ film and (c) a fully crystallized Si film of $Si_{0.45}Ge_{0.55}$/Si bi-layer structure. [The convergent black lines in the (b) and (c) are bending contours.].

3.1.4 Summary

In this experiment, the $Si_{1-x}Ge_x$/Si bi-layer was proposed as an advanced SPC method to obtain the large-grained and equiaxial Si channel microstructure. The surface nucleation of $Si_{1-x}Ge_x$/Si bi-layer was verified through the *in situ* TEM measurement. It was also identified that the orientation filtering at the $Si_{1-x}Ge_x$ surface via competitive growth during the $Si_{1-x}Ge_x$ grain growth expected due to the growth rate anisotropy of randomly oriented nuclei. The equiaxial $Si_{1-x}Ge_x$ microstructure obtained by surface nucleation and stress relief effect was propagated downward into the underlying Si channel layer by epitaxy-like growth without further nucleation. Based on these experimental results, it is expected that the simple replacement from the conventional Si single layer to $Si_{1-x}Ge_x$/Si bi-layer would solve the problem associated with electrical property degradations with the increase of the number of cell layers in VNAND.

3.2 Lateral growth for large-grained Si channel layer

3.2.1 Introduction

In a $Si_{1-x}Ge_x$/Si bi-layer, the Si layer is crystallized following the pre-crystallized $Si_{1-x}Ge_x$ as a seed. The Si solid phase epitaxy (SPE) proceeds in the Si layer. The ultimate goal of this research is obtaining high quality poly-crystalline Si microstructure. During the Si SPE, the Si microstructure is affected by the $Si_{1-x}Ge_x$ microstructure. The details of Si microstructure dependence on the $Si_{1-x}Ge_x$ layer are as follows. If the $Si_{1-x}Ge_x$ layer is single-crystalline film, the threading dislocations will be generated in the Si layer due to the lattice mismatch between $Si_{1-x}Ge_x$ and Si. However, the $Si_{1-x}Ge_x$ layer is poly-crystalline film in this experiment. It is expected the dislocations as well as the intra-grain defects and grain boundaries in the Si layer by propagation from the $Si_{1-x}Ge_x$ layer. Therefore, the microstructural quality of Si layer depends on the quality of $Si_{1-x}Ge_x$ layer. In this chapter 3.2, I induce the large-grained $Si_{1-x}Ge_x$ film during the bi-layer annealing. If the large $Si_{1-x}Ge_x$ grains are obtained, the Si microstructure also shows large grains through the SPE behavior.

In order to obtain the large $Si_{1-x}Ge_x$ grains, the lateral growth method is introduced. Figure 3.7 shows the process sequence schematics of lateral growth. The bi-layer annealing proceeds at a low temperature where only $Si_{1-x}Ge_x$ crystallize as shown in Figure 3.7(a). The $Si_{1-x}Ge_x$ surface nucleation will occur (as

shown in the chapter 3.1) and the grain growth follows. As shown in Figure 3.7(b), if the bi-layer is continuously annealed in a low temperature, the perpendicularly growing $Si_{1-x}Ge_x$ grains may impinge to the $Si_{1-x}Ge_x$/Si interface. At this time, the Si growth would not happen because the low temperature annealing is not sufficient to provide thermal energy to the rearrangement of Si atoms. When this low temperature annealing continues, the bi-layer would become to crystallize further. In accordance with Figure 3.7(c), the $Si_{1-x}Ge_x$ lateral growth would be naturally induced. If this crystallization behavior continues, the large $Si_{1-x}Ge_x$ grains at the $Si_{1-x}Ge_x$/Si interface will be shown after fully crystallization of $Si_{1-x}Ge_x$ as shown in Figure 3.7(d). Then, the high temperature annealing where Si can be crystallized would carry out. The Si SPE proceeds following the large $Si_{1-x}Ge_x$ grains as shown in Figure 3.7(e). Finally, the large-grained Si microstructure will be attained in the underlying Si channel layer.

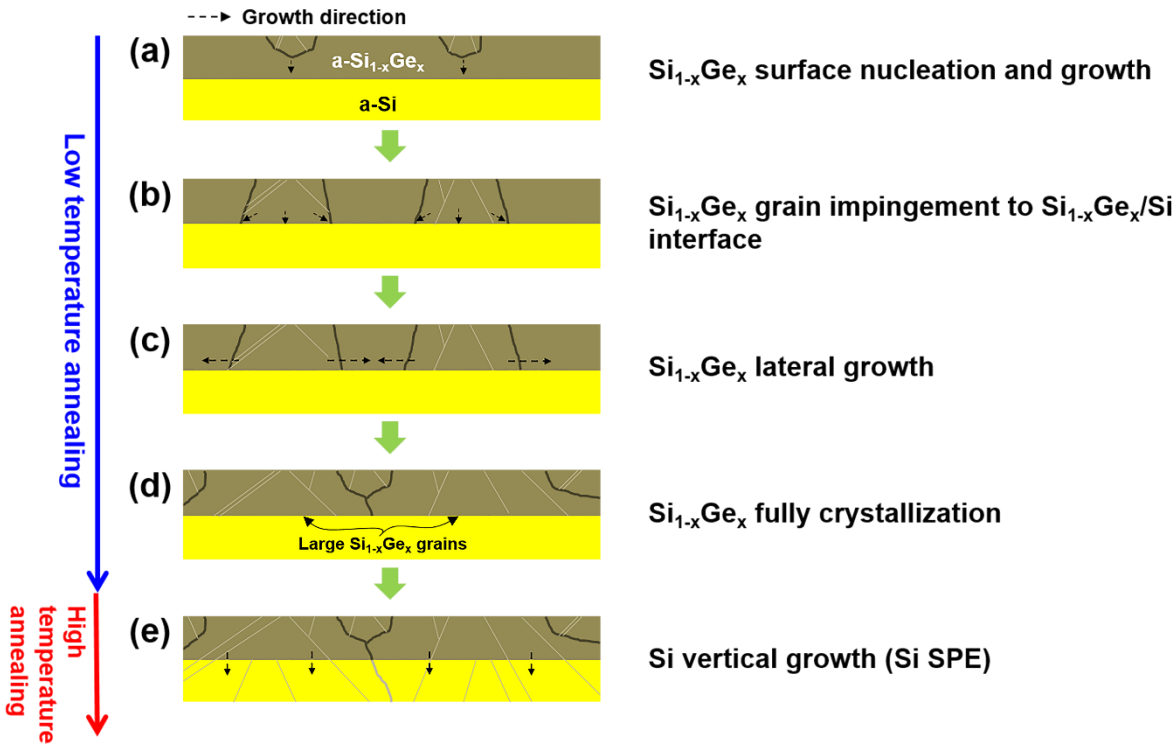


Figure 3.7 The process sequence of the $Si_{1-x}Ge_x$ lateral growth.

3.2.2 Experimental details

Two channel structures that are $Si_{1-x}Ge_x$/Si and Ge/Si bi-layer with different thicknesses are fabricated in this experiment. The $Si_{1-x}Ge_x$/Si structure is same as investigated in the chapter 3.1. The Ge/Si bi-layer was sequentially deposited by using Si_3H_8 and GeH_4 source gases in a low-pressure chemical vapor deposition (LPCVD) system on silicon dioxide on Si substrate. The deposited Si and Ge layers were 4 and 30 nm thick, respectively. The bi-layer structures were annealed under nitrogen ambient in a mini furnace (SMF-800, Seoul Electron Inc.) system. The Ge crystalline fractions were acquired by measuring the refractive index at 830 nm wavelength via a J. A. Woollam EC-400 spectroscopic ellipsometer. The transmission electron microscopy (TEM) samples for cross-section measurements were fabricated via focused ion beam system. In the TEM experiment, a JEOL JEM-3011 *in situ* TEM equipped with a double-tilting holder was used at 300 kV. The initial crystallinity of bi-layers were characterized by the cross-section transmission electron microscopy and selective area diffraction pattern (SADP). The cross-section *in situ* TEM measurement with heating was carried out in order to investigate the crystallization behavior of the Ge/Si bi-layer in a real time. The cross-section TEM measurement was carried out to investigate the degree of crystallinity and film microstructure.

3.2.3 Results and discussions

The $Si_{0.45}Ge_{0.55}$/Si bi-layer structures were annealed only to induce $Si_{0.45}Ge_{0.55}$ lateral growth at 450, 475 and 500 ^{o}C, respectively for 24 hours via furnace system. The degree of crystallinity of $Si_{0.45}Ge_{0.55}$ and Si layers were characterized by the cross-section TEM. Figure 3.8 shows the cross-section TEM and fast Fourier transform (FFT) results of bi-layers. The $Si_{0.45}Ge_{0.55}$ and Si layers were fully crystallized at 500 ^{o}C annealing as shown in Figure 3.8(a). The 475 ^{o}C annealed bi-layer showed partially crystallized $Si_{0.45}Ge_{0.55}$ and Si layer as presented in Figure 3.8(b). Both layers were remained as an amorphous state as shown in Figure 3.8(c) at 450 ^{o}C annealing. Based on these results, the low temperature annealing should be carried out in the temperature range between 450 and 475 ^{o}C to induce the $Si_{0.45}Ge_{0.55}$ lateral growth in a $Si_{0.45}Ge_{0.55}$/Si bi-layer structure. Depending on the Ge contents in the $Si_{1-x}Ge_x$ nucleation layer, the temperature to induce $Si_{1-x}Ge_x$ lateral growth should set differently. If the Ge contents increase, the melting point difference between $Si_{1-x}Ge_x$ and Si is getting increase and it would be easy to induce lateral growth only at a relatively low temperature. I try to observe the $Si_{1-x}Ge_x$ lateral growth behavior by using 100 % Ge as a nucleation layer in a bi-layer structure.

The crystallinity of as-deposited film of Ge/Si bi-layer structure was characterized by cross-section TEM and shown in Figure 3.9. Some pre-existing nano-crystallites (NC) in the Ge film were observed. The existence of NCs in the Ge film is

supposed that some Ge atoms were actively migrated at the amorphous Si surface at the initial stage of film deposition. There are some report those NCs in the amorphous film deposited by LPCVD system.[35, 61, 75] C. H. Hong *et al*.[61] mentioned that the NCs could be existed when the film was deposited near the transition temperature from amorphous to poly-crystalline and their density in a film is proportional to the deposition temperature.

The crystallization behavior of Ge nucleation layer is observed. The annealing was carried out in the temperature range from 350 to 450 ^{o}C. Figure 3.10 shows the crystalline fraction of Ge film as a function of annealing temperature and time. The y-axis of the graph indicates the initial state of the as-deposited film. When the film is begun to crystallized, the value change occurs in the y-axis. The fully crystallized film shows 100 % in the y-axis. As shown in Figure 3.9, the time to beginning of crystalline fraction change and completion of crystallization is gradually shortened as the annealing temperature increase.

When the amorphous film is annealed, it is crystallized through the nucleation and the growth as shown Figure 2.2. The cross-section schematic of available nucleation and growth site in a Ge/Si bi-layer when this structure is annealed is shown in Figure 3.11. The nucleation site may the interface of native oxide (germanium oxide)/amorphous Ge and amorphous Ge/amorphous Si. The NC/amorphous Ge interface may act as a growth site. The crystallization of Ge layer can be achieved through the only growth or both nucleation and growth,

because the activation energy of nucleation is higher than growth.[18] The occurrence of nucleation will be determined whether the density and distribution of NCs in a film or the annealing temperature. When nucleation occurred during annealing, the density of grain boundaries increases due to the generation of grains. Therefore, nucleation should be suppressed as much as possible or should not occurred in order to obtain the large-grained Ge microstructure.

The *in situ* TEM measurement was carried out to examine the crystallization behavior of Ge/Si bi-layer in a real time. Figure 3.12 shows the cross-section *in situ* TEM results of Ge/Si bi-layer annealed in a TEM chamber at 425 ^{o}C. Figure 3.12(a) shows the amorphous Ge film with pre-existing NC. When this structure was annealed, the growth from the NC was observed after a period of time as shown in Figure 3.12(b). The grain grew laterally. This lateral growth continued over time like Figure 3.12(c) and (d). This growth behavior extended until the grain impingement to the laterally growing grains from adjacent NCs as shown in Figure 3.12(e) and (g). Figure 3.12(f) shows wider area containing the position of Figure 3.12(d). The FFT results show the crystallized region by lateral growth and amorphous region without lateral growth in a Ge film. As like FFT results, the amorphous region remained without nucleation until crystallized through the lateral growth. That is, the Ge film is crystallized by the lateral growth only without nucleation.

The vertical growth of the Si should be suppressed during Ge lateral growth to

prevent grain boundaries formation in the Si layer. The microstructure of Ge/Si bi-layer interface was investigated after completion of Ge crystallization via cross-section TEM as shown in Figure 3.13(a) the cross-section TEM image of Ge/Si bi-layer and (b) magnified image of Ge/Si interface annealed at 425 ºC for two hours in furnace system. The amorphous Si remained without being crystallized. This is thought that the 425 ºC is too low temperature to provide sufficient thermal energy for Si atomic rearrangement for growth by breaking their bonding during annealing.

The high temperature annealing was carried out to induce Si growth at 700 ºC. Figure 3.14 shows the cross-section TEM images of Ge/Si bi-layer structure annealed at 700 ºC for one hour after 425 ºC annealing for two hours via furnace system. As shown in Figure 3.14(a), the Si layer showed epitaxial growth behavior following the atomic arrangement of crystallized Ge layer. Figure 3.14(b) is the dark field TEM image of identical position with Figure 3.14(a). The laterally grown grain was observed through the Ge and Si layers. Figure 3.15 shows the expected microstructural schematics of Ge/Si bi-layer (a) after 425 ºC annealing for Ge lateral growth, (b) additional 700 ºC annealing for Si growth and (c) after Ge layer stripping via wet etching process. Based on the crystallization behavior results of Ge/Si bi-layer, it is thought that that Ge grain is laterally grown at 425 ºC as shown in Figure 3.15(a). Then, Si growth occurs via SPE during 700 ºC annealing as described in the Figure 3.15(b). After fully crystallization of Ge/Si bi-layer, the Ge layer can be selectively wet etched and only Si layer remains as a channel for VNAND. The remaining Si single layer shows very large grains

compare to its film thickness as shown in Figure 3.15(c). As a channel layer, such large grains are very advantageous to improve the electrical properties such as sting current and carrier flow in each cell transistor in VNAND.

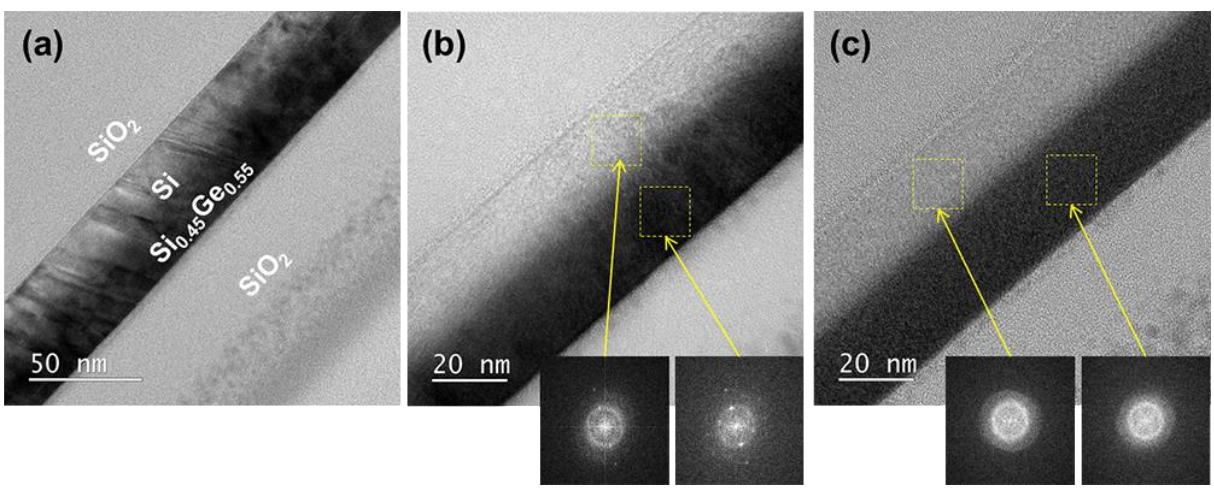


Figure 3.8 The cross-section bright field TEM images and FFT results of $Si_{0.45}Ge_{0.55}$/Si bi-layer structure annealed in the furnace system for 24 hours at (a) 500, (b) 475 and (c) 450 ^{o}C, respectively.

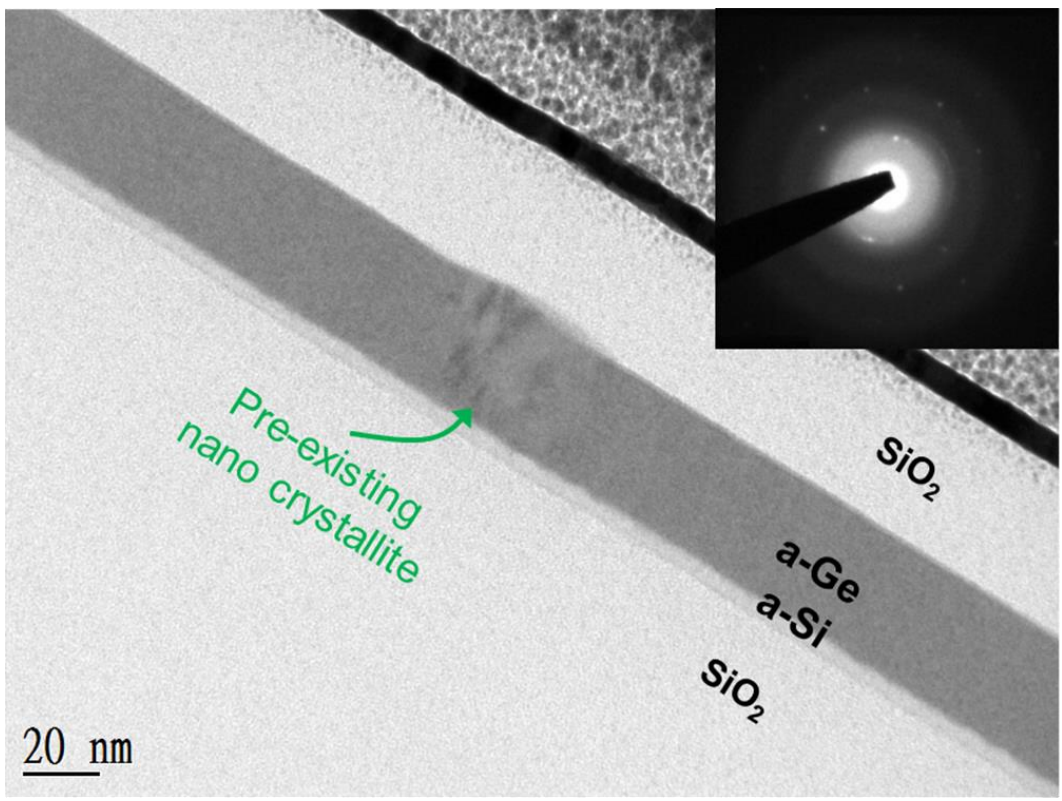


Figure 3.9 The cross-section bright field TEM image and SADP of as-deposited Ge/Si bi-layer structure.

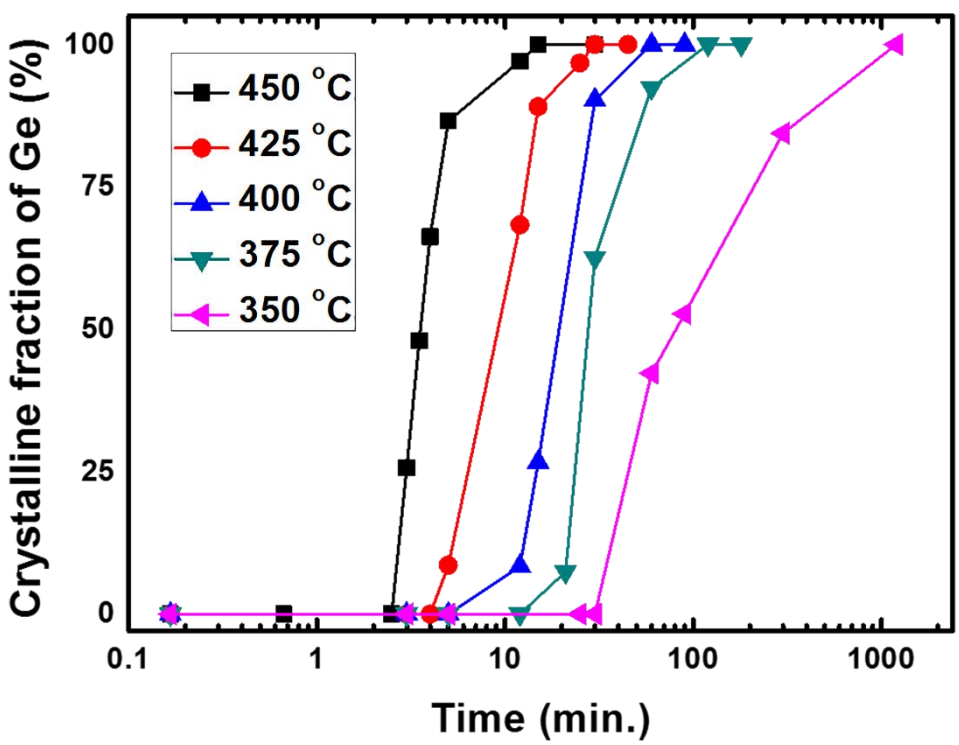


Figure 3.10 The crystalline fraction of Ge in a Ge/Si bi-layer structure as a function of annealing time. The samples are annealed in a furnace system.

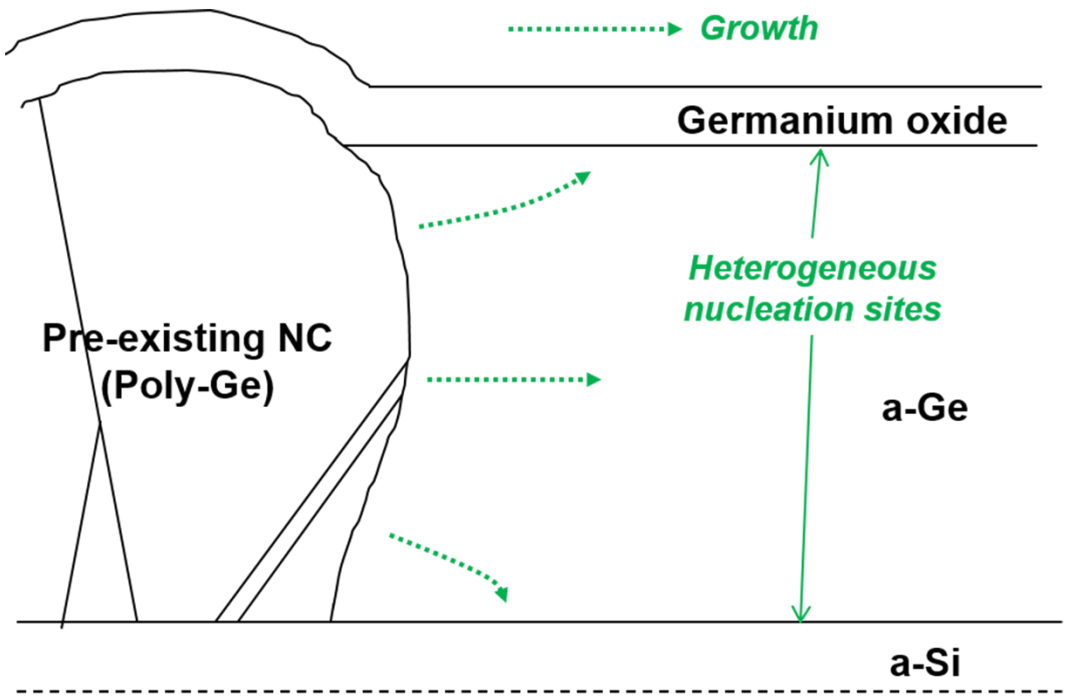


Figure 3.11 The cross-section schematic of available nucleation and growth site of Ge/Si bi-layer structure when the bi-layer begin to crystallize via the annealing process.

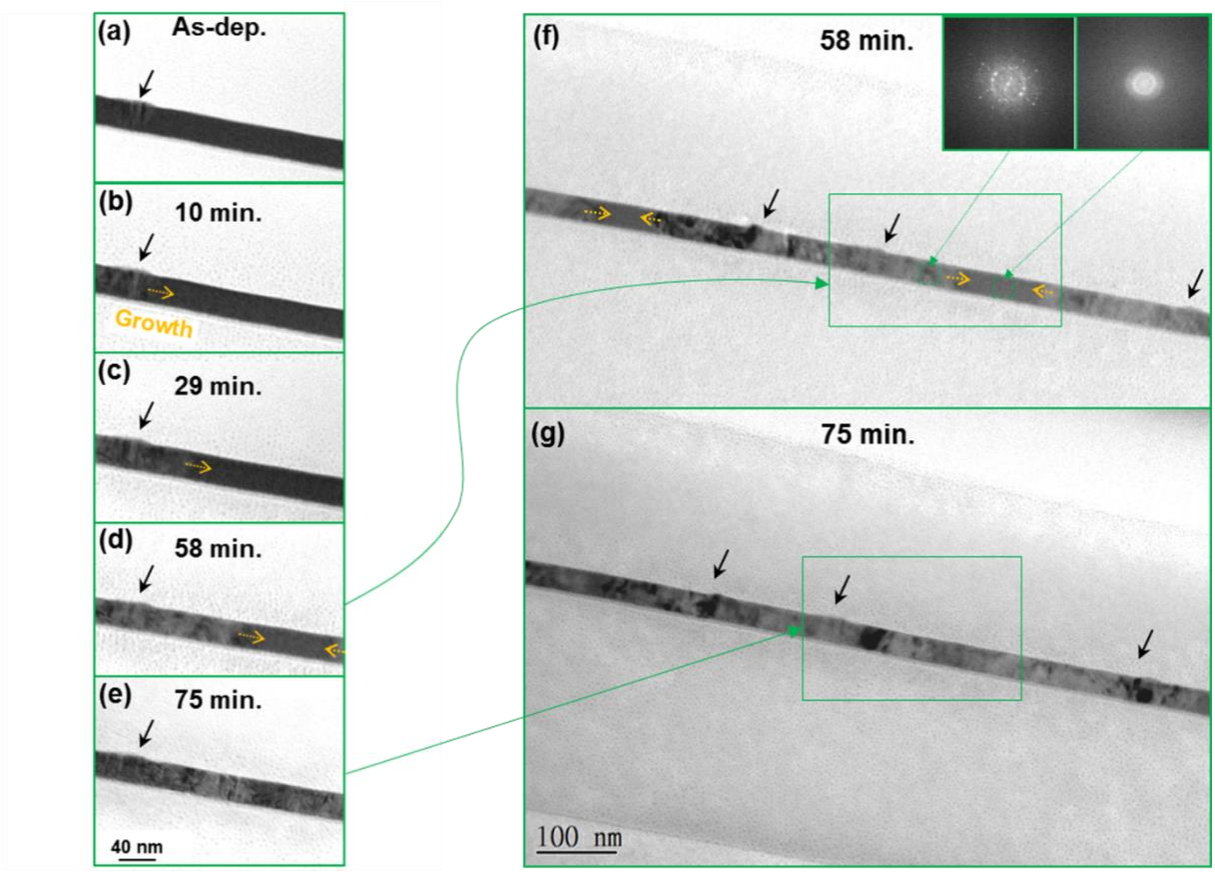


Figure 3.12 The cross-section bright field *in situ* TEM images and FFT results of Ge films in a Ge/Si bi-layer structure annealed at 425 ºC in a TEM chamber.

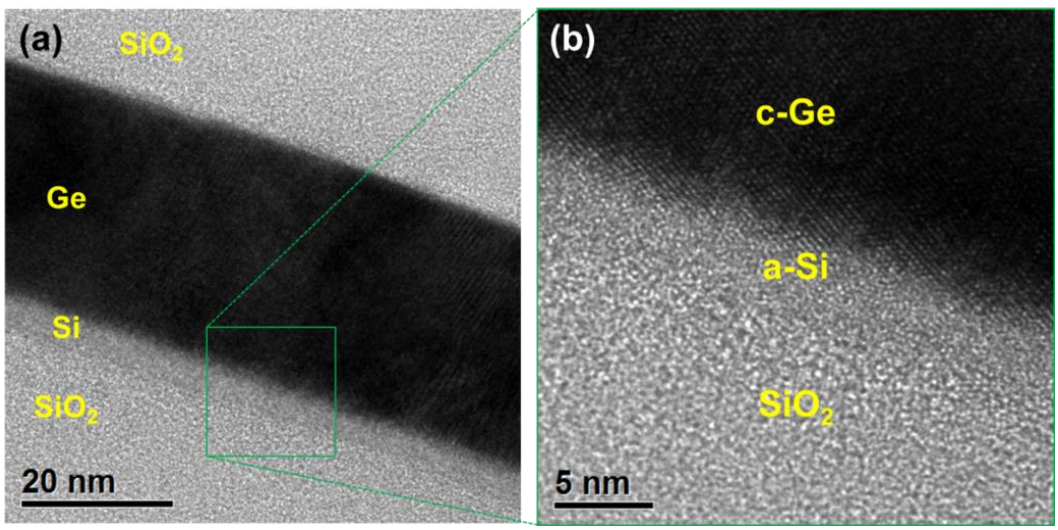


Figure 3.13 The cross-section TEM images of Ge/Si bi-layer structure annealed at 425 °C for two hours via furnace system.

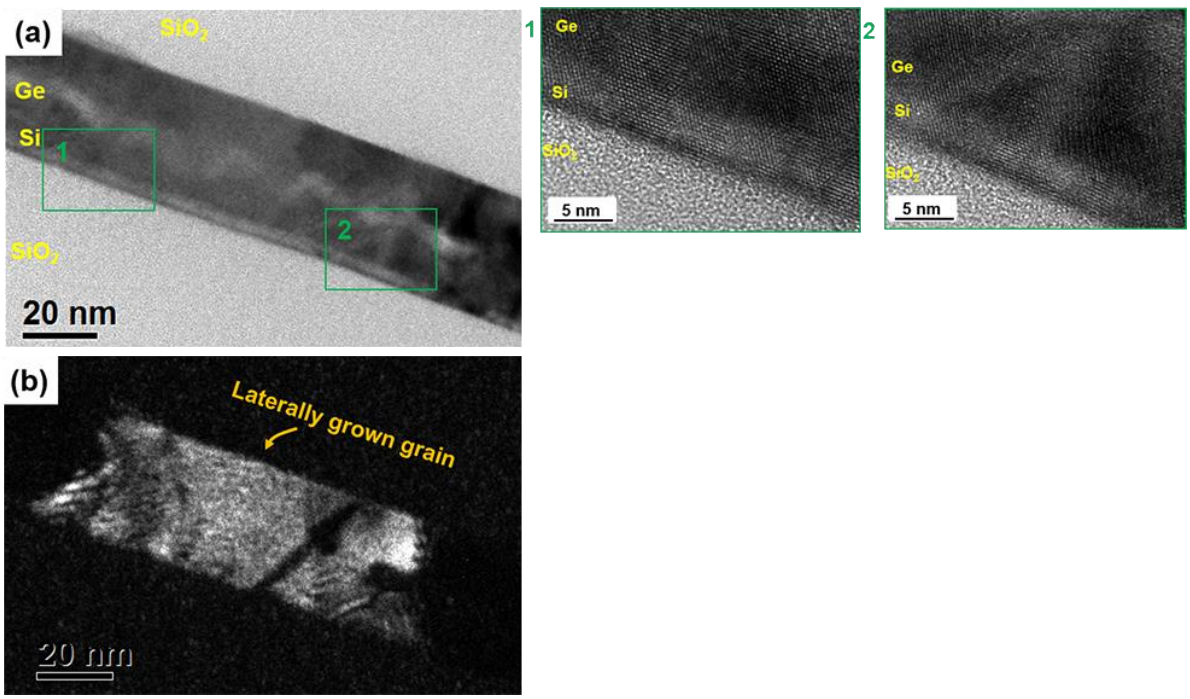


Figure 3.14 The cross-section (a) bright field TEM image with high resolution of Ge/Si interface and the (b) dark field TEM image with same position of (a). The Ge/Si bi-layer structure is annealed at 700 ^{o}C for one hour after 425 ^{o}C annealing for two hours via furnace system.

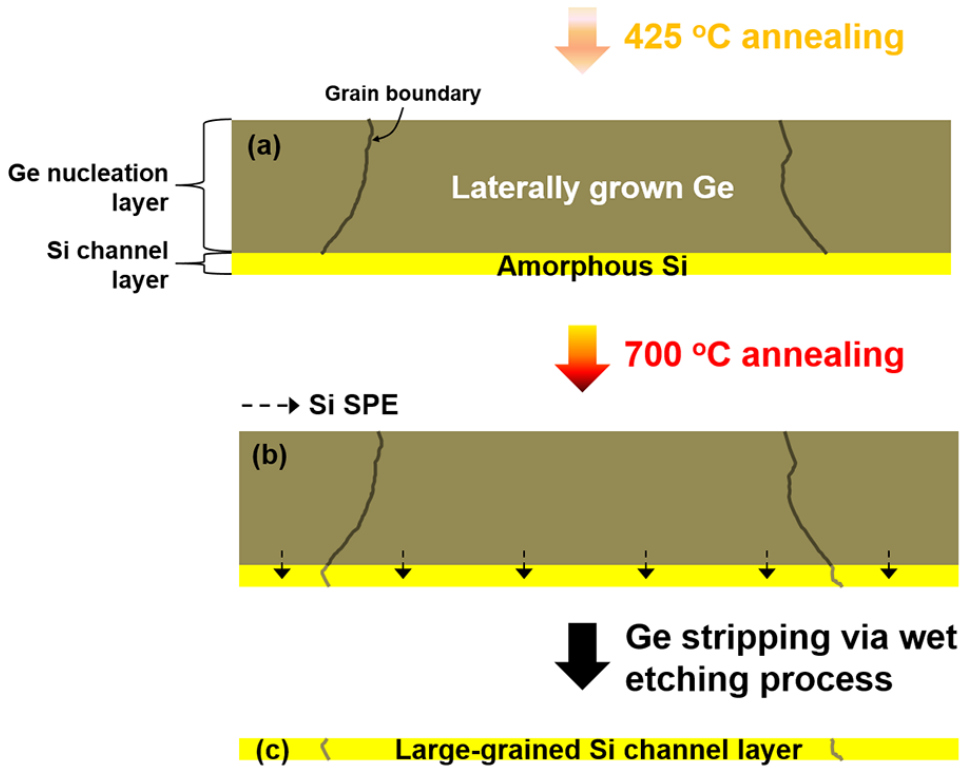


Figure 3.15 The expected microstructural schematics of Ge/Si bi-layer (a) after 425 °C annealing for Ge lateral growth, (b) additional 700 °C annealing for Si growth and (c) after Ge layer stripping process. [The grain boundaries are sketched based on the TEM image of Figure 3.14(b)].

3.2.4 Summary

In order to obtain even large-grained Si channel microstructure, the $Si_{1-x}Ge_x$ lateral growth method is proposed. In the case of Ge/Si bi-layer using pure Ge as a nucleation layer, the Ge layers are crystallized only by lateral growth without any nucleation. After high temperature annealing for Si growth, the grains is obtained in the Si layer following the laterally grown Ge grain boundaries through the SPE behavior. Lateral growth method shows the very large grains in the Si layer over the film thickness. Based on the proposed structure and annealing method, it would be advantageous to improve the electrical properties of each cell transistors and minimize the degrading of string current in the vertical channel.

3.3 Technical issues and future work

3.3.1 Si, Ge intermixing

In the chapter 3.1 and 3.2, the temperature for Si growth is 600 and 700 ºC for several hours, respectively. It is relatively high temperature where Si and Ge intermixing can occur. If intermixing happen, the Ge atoms in the Si channel layer would change the structural and electrical properties of channel layer and it should be avoided. The detailed researched like depth profiling characterization after bi-layer crystallization is needed to examine the atom distributions in a Si channel layer depending on the crystallization temperature. To suppress Si diffusion, the crystallization should be carried out in a relatively lower temperature. As shown in Figure 3.8, the Si growth is observed at 475 ºC. It is lower temperature compare to bi-layer annealing and expected to suppress Ge diffusion to the Si layer during the bi-layer crystallization.

3.3.2 Surface roughness of Si channel layer after $Si_{1-x}Ge_x$ layer stripping

As previously mentioned, the $Si_{1-x}Ge_x$ nucleation layer is stripped via wet etching process after crystallization of bi-layer. The remained Si layer acts as a channel of

each cell transistors in VNAND. The AFM characterization was carried out to investigate the surface roughness both $Si_{1-x}Ge_x$/Si bi-layer and remained Si layer after $Si_{1-x}Ge_x$ stripping. The root mean square values are 0.3 and 2.5 for bi-layer and remained Si layer, respectively. The surface roughness affects the carrier mobility. It is thought that the electrical property characterization is required related to the surface roughness of Si channel layer.

3.3.3 Surface nucleation in a $Si_{1-x}Ge_x$/Si bi-layer

In the chapter 3.1, the one of main idea for the research is the $Si_{1-x}Ge_x$ surface nucleation. As previously mentioned, the initial nucleation of amorphous Si on SiO_2 structure is the film interface. However, the primary cause of surface nucleation is not exactly clarified. Figure 3.16 is the schematics that indicating the nucleation stage of bi-layer during crystallization. The major factors that affect nucleation are the small crystallite and/or strains in a film. However, not any crystallites are detected in the cross-section TEM and SADP characterization (see Figure 3.1). The strains is expected that higher at the $Si_{1-x}Ge_x$ surface than the interface. The interface and surface are acts as heterogeneous nucleation site when nucleation occurs in a bi-layer. Those two nucleation sites are consisted of difference materials that amorphous Si and native oxide composed mixed phase of silicon and germanium oxides. The atomic migration would be more activated at

the interface than the surface due to the lower binding energies of amorphous Si than the native oxide. So far, it is suggested that some differences at those two heterogeneous nucleation sites related to the material, leads to surface nucleation in a bi-layer. Further and detailed research will be needed to understand the exact nucleation behavior mechanisms in a bi-layer.

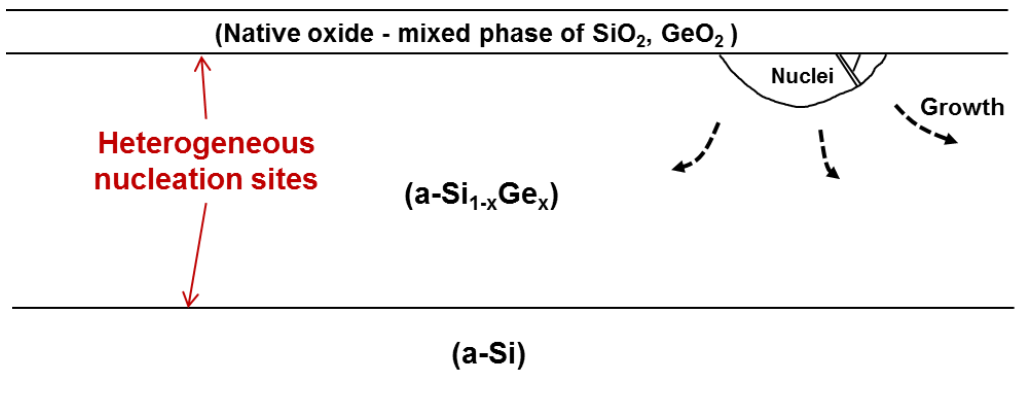


Figure 3.16 The schematic of $Si_{1-x}Ge_x$/Si bi-layer at the initial stage of crystallization through the surface nucleation.

4 Grain Growth of Poly-Crystalline Ge

4.1 Introduction

Poly-crystalline Ge film has been substantially studied as the channel material in the next-generation TFT technologies due to its lower crystallization temperature and higher carrier mobility compared to conventional poly-crystalline Si films.[76-80] However, the existence of grain boundaries in channel area forms localized states causes potential barriers in the band structure, resulting in the degradation of the currents of the poly-crystalline TFTs.[22] In addition, the orientation of each grain has a strong effect on the uniformity of device performances. Therefore, it is necessary not only to make the grain size of poly-channel materials as large as possible, but also to get the textured orientation with particular crystallographic direction to increase the device uniformity as well as performance.

Various researches for large-grained poly-crystalline Ge microstructure have been pursued in a plenty of ways such as excimer laser annealing (ELA)[81], solid phase crystallization (SPC)[82], radio-frequency (RF) sputter deposition followed by SPC[83], surface-energy-driven secondary grain growth (SEDSGG)[63, 66], and so on. Among these techniques, the SEDSGG seems to be one of the representative solid-state transformation techniques for abnormally large-grained and textured microstructure over the film thicknesses. It is known that SEDSGG is taken place over some

specific transition temperature,[63, 65] where seems the dominant kinetics is altered from normal to secondary grain growth.[84] To complete SEDSGG, it requires a very high thermal energy such as several hours of annealing near melting temperature.

The objective of this paper is to present Ge SEDSGG in a various way to apply vertical channel in VNAND. In a given thermal budget of VNAND, the annealing temperature and time were varied to verify SEDSGG effects via microstructure characterization of films. Also, the two-step annealing is proposed to enlarge the grain size in a limited thermal budget. Proposed two-step annealing is utilized the transition of grain growth kinetics dominated by the annealing temperature. A first-step low temperature annealing was carried out to induce normal grain growth followed by a subsequent second-step high temperature annealing for SEDSGG. This separation of annealing steps was planned to employ individual grain growth kinetics depending on the annealing temperature. Also, the initial microstructure dependence in a two-step annealing was analyzed and explained based on the experimental results.

4.2 **Experimental details**

The un-doped poly-crystalline Ge films were deposited on 500 nm thick SiO_2 on Si substrate by using lower pressure chemical vapor deposition system. In order to exclude the thickness effects on the grain growth, Ge thin films with 60 and 500

nm thickness were selected. Similarly to conventional SEDSGG, the whole films were encapsulated by 200 nm thick SiO_2 layers to avoid the film agglomeration. For the SiO_2 deposition, a 310PC plasma-enhanced chemical vapor deposition system (Surface technology system) was used. Some Ge films were boron doped to verify the secondary grain growth rate change and it was carried out by E220 medium current ion implant (Varian) system. For identifying the temperature dependence, the KVR-3006T rapid thermal annealing (RTA) system (Korea vacuum technology) was used. In the RTA reactor, the films were isochronally annealed with varying temperature in the range from 700 to 900 ^{o}C. After reaching the peak temperature, it drastically goes down to the room temperature. The temperature profile as a function of time was shown in Figure 4.1 for the 900 ^{o}C annealing case. For a long time annealing, a SMF-800 mini furnace (Seoul electron incorporation) system was used. Sample structures were isothermally annealed in a furnace. All the samples in the RTA and furnace system were annealed under nitrogen ambient.

The Raman spectroscopy was performed to characterize the film crystallinity. Raman measurements were made in a backscattering geometry with a JY LabRam HR equipped with a liquid-nitrogen cooled CCD detector. The spectra were collected under ambient conditions using the 514.5 nm line of an argon-ion laser with the excitation source at 0.5 ~ 1.0 mW. The laser spot diameter was about 1 μm and the penetration depth in Ge was about 20 nm. All the Raman spectra obtained in the experiments were fitted by Lorentizian function. Ge bare wafer was also

measured as a reference for the Raman analysis of the samples. FWHM of as-deposited 60, 500 nm thick films and the Ge bare wafer were 6.8, 7.0 and 2.7 cm^{-1}, respectively. The microstructure of the films was investigated via a JEOL JEM-3000F transmission electron microscopy (TEM) at 300 kV in the bright-field mode. Plan-view and cross-section TEM samples were prepared via ion-milling and FIB system, respectively. The Oxford energy dispersive spectroscopy (EDS) was used for examining the segregations of impurity atoms at the grain boundaries. Finally, Hall measurements were performed to investigate the carrier mobility by using the Van der Pauw method via Accent HL5500PC.

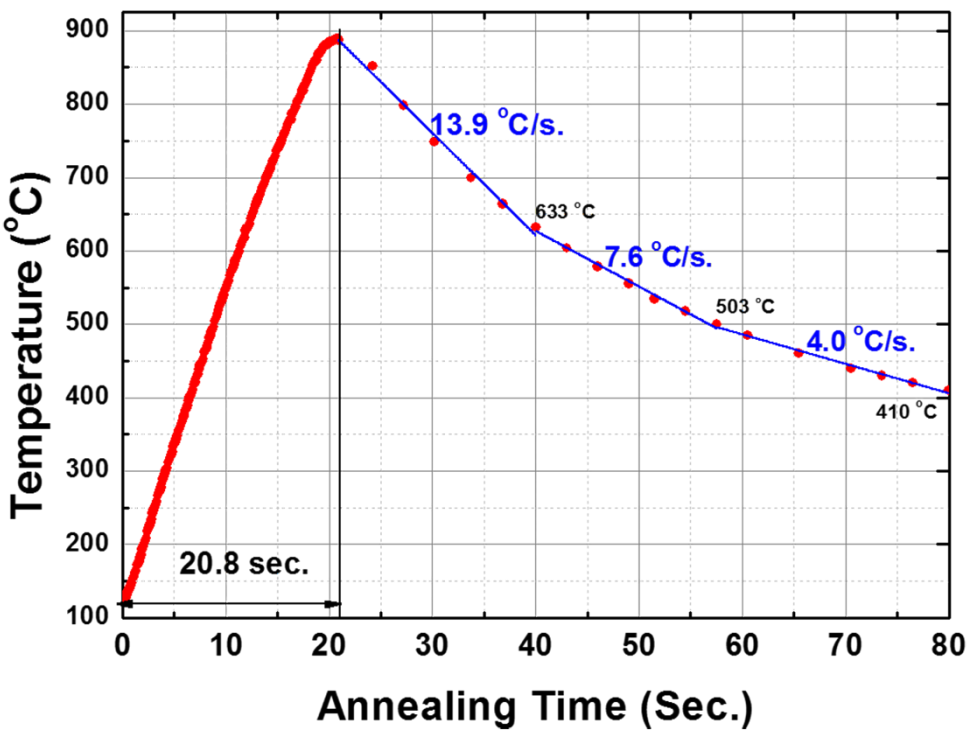


Figure 4.1 The temperature profile via RTA process at 900 °C.

4.3 Results and discussions

4.3.1 High temperature annealing of poly-crystalline Ge

The purpose of research in this chapter 4.1 is explained chapter 2.4.4. The Ge SEDSGG temperature is relatively very high when considering the melting point of Ge. Firstly, I tried the high temperature annealing over 700 ^{o}C to induce secondary grains in a Ge film. To characterize the crystallinity of poly-crystalline Ge as a function of annealing temperature, Raman analysis was carried out. Figure 4.2 shows the Raman spectrum results of (a) 500 nm thick as-deposited Ge, (b) 500 and (c) 60 nm thick Ge films depending on the annealing temperature. It showed a main peak at 300 and a broad peak at 290 cm^{-1} in as-deposited Ge film as shown in Figure 4.2(a). In the Ge bare wafer measurement, the peak at 300 cm^{-1} was obtained. (Not shown here) Therefore, I speculate the main peak of as-deposited sample is originated from Ge-Ge vibrations. Kartopu *et al*.[85] reported that the peak at 290 cm^{-1} indicated the existence of very small sized grains (~3-4 nm). This peak is gradually vanished from the Raman spectrum of the annealed Ge film as shown in Figure 4.2(b) and (c). It implies the disappearance of the small grains after the annealing. The main peak positions of the annealed films were observed to vary in the range between 299 and 300 cm^{-1} most likely due to strain in the films shown in Figure 2(b) and (c). Figure 4.3 shows the normalized Raman FWHM of Ge-Ge

vibration of 60 and 500 nm thick Ge films at various annealing temperatures. The normalized Raman FWHM is obtained from the value of annealed film divided by that of as-deposited. As shown in Figure 4.3, the normalized Raman FWHM decreases as the annealing temperature increases. Typically, the density of grain boundaries in the poly-crystalline Ge film affects Ge-Ge vibrations (i.e., grain boundaries broaden the width of peak).[86] Therefore, this result can be supposed that the grain sizes of poly-crystalline Ge are getting larger as the annealing temperature increase. In Figure 4.3, the deflection point at 800 ^{o}C is clearly observed that normalized FWHM abruptly decreases for both thickness. This might be caused by any mechanism transition in grain growth depending on annealing temperature. To specifically investigate such a transition behavior, TEM measurement was carried out to evaluate the microstructure of poly-crystalline Ge.

Figure 4.4 shows plan-view TEM images of 500 nm thick Ge films of (a) as-deposited, annealed at (b) 800 ^{o}C, (c) 850 ^{o}C and (d) 900 ^{o}C. Figure 4.4 (e) and (f) is the different area of same films of (c) and (d), respectively. In the TEM analysis, the grain size was determined by measuring the largest dimension in a grain and the largest perpendicular dimension to the first measurement and then averaging those following Thompson *et al*. used method.[65] As annealing temperature increased, average grain size of poly-crystalline Ge increased. Over 850 ^{o}C, the extensive grain growth is examined as shown in Figure 4.4(c) and (d). It is expected that the reduced grain boundaries by extensive growth may one of the main reason that affecting the Raman FWHM transition behavior shown in Figure

4.3. On the other hand, as shown in the microstructure of 850 and 900 ^{o}C annealed films [Figure 4.4(e) and (f)], it contains a few larger grains over the film thickness. The average size of these larger grains was about three times larger than adjacent grains. Based on their size and over the film thickness, I suppose that those larger grains can be secondary grains in the initial stage of secondary grain growth. In the 60 nm thick films (not shown here), same microstructural analysis reveals that the large grains than adjacent grains and over film thickness took place at 850 and 900 ^{o}C.

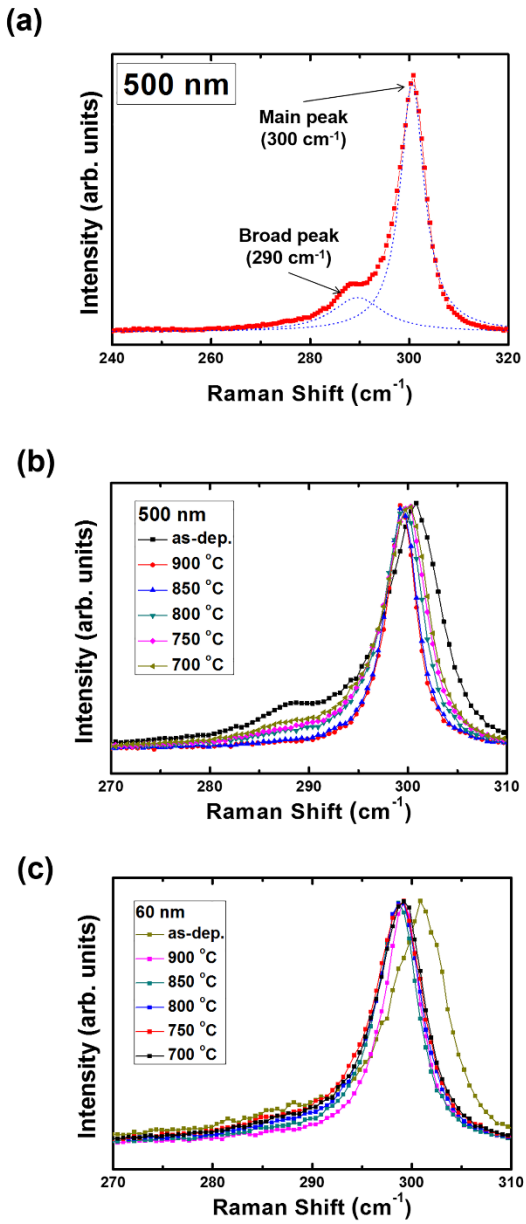


Figure 4.2 The Raman results of poly-crystalline Ge films. The (a) Raman spectra of as-deposited 500 nm thick film and the two fitted curve indicates broad (290 cm^{-1}) and main (300 cm^{-1}) peaks, respectively. The Raman spectrum of as-deposited and annealed (b) 500 and (c) 60 nm thick films.

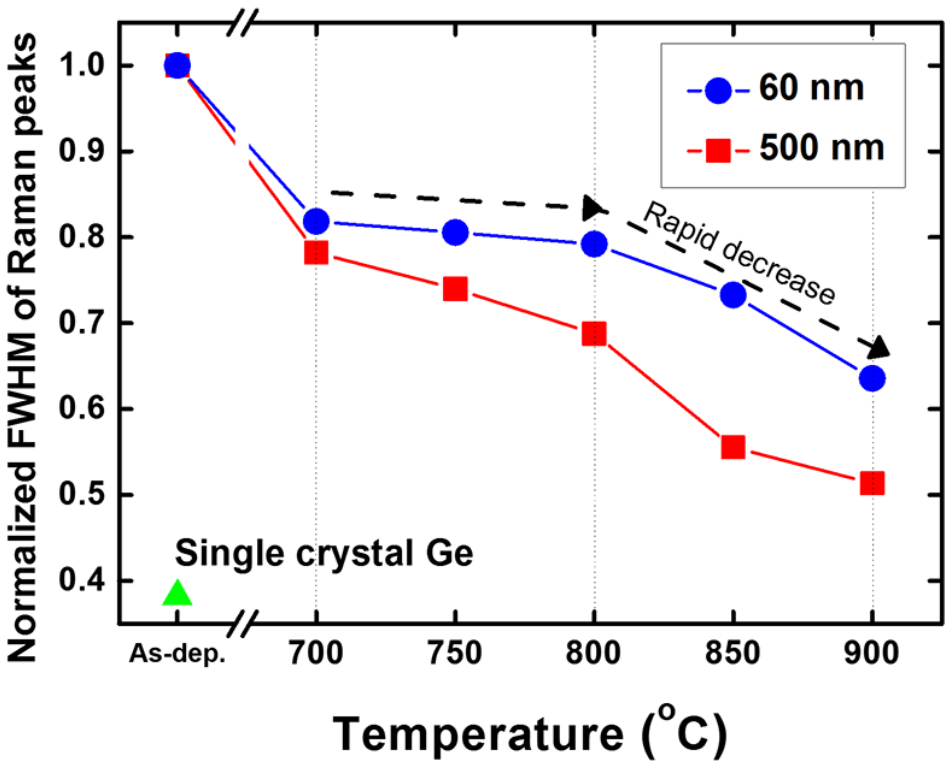


Figure 4.3 The normalized Raman FWHM of Ge main peaks as a function of annealing temperature via RTA system for both thicknesses. The value of single crystal Ge is inserted as a reference.

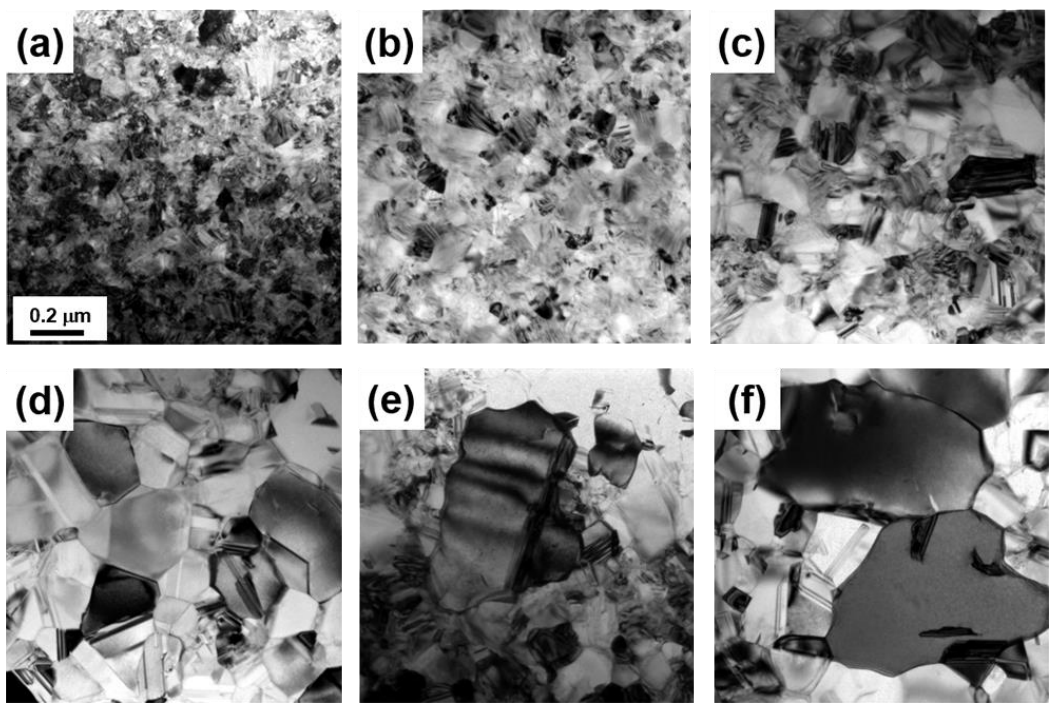


Figure 4.4 The plan-view bright filed TEM images of 500 nm thick poly-crystalline Ge films annealed via RTA system. The images indicate (a) as-deposited, (b) annealed at 800, (c) 850 and (d) 900 ºC, respectively. The (e) and (f) are different position of same sample of (c) and (d) respectively where the large grain is observed.

4.3.2 Annealing near VNAND thermal budget

Based on the previous results of chapter 4.3.1, I obtained the some large grains in a Ge film via high temperature annealing. It is desired to enhance their grain size and/or increase the density of them in a film in order to increase the carrier mobility. Therefore, I tried the long time annealing to maximize the grain growth effect in a given device thermal budget of VNAND. Before annealing, the device thermal budget should be considered. Figure 4.5 indicates the available annealing time as a function of annealing temperature based on the known thermal budget of VNAND (see chapter 2.4.4). The largest grains are detected at the highest temperature annealing where 900 ^{o}C. The available thermal budget in 900 ^{o}C annealing, is about 130 sec. The annealing was performed at 900 ^{o}C for 2 minutes in a furnace system and Figure 4.6 shows the plan-view TEM images of (a) 60 and (b) 500 nm thick Ge films after annealing. Some larger grains than adjacent grains and over film thicknesses were observed for both thickness films (indicated as green arrows). The size of those large grains are about 260 and 1600 nm for 60 and 500 nm thick Ge film, respectively. The size and distribution of those large grains is uniform in the whole film area.

J. E. Palmer[63] *et al*. researched Ge SEDSGG. Their experimental conditions are as follows. The un-doped 30 nm thick poly-crystalline is deposited by LPCVD system and annealed at 900 ^{o}C for 6 hours. They shows the secondary grains which size is about 700 nm. There certainly exists the microstructural difference between them

and my experiment related to the deposition condition. However, when considering the same conditions such as deposition system, doping condition and annealing temperature, the main reason for small size grains in my results, is thought that not a sufficient time for secondary grain growth compare to them. On the other hand, S. M. Garrison *et al.*[68] obtained the secondary grains over 14 times larger than the film thickness by using heavily phosphorus doped Si films even though very short annealing time less than 10 seconds. They annealed films over temperature range of ~1100 to 1225 ^{o}C via RTA system. To check the doping effect to the secondary grain growth rate in this experiment, some Ge films were heavily boron doped and annealed at 900 ^{o}C for 2 minutes (not shown here). However, there was not a big microstructural difference compare to the un-doped films. It is known that the impurities like oxygen retard the grain growth rate by the segregation at the grain boundaries. However, in the EDS characterization no impurity segregations are observed in the grain boundaries as shown in Figure 4.7. It is also known that the dopants in a film affect the grain growth kinetics by changing electron concentration in a film. Kim *et al*.[69] research SEDSGG by using LPCVD deposited Si film depending on the type of dopants like phosphorus, arsenic and boron related to their concentration. They mentioned that the secondary grain growth rate is increased through the grain boundary mobility increasing by the enlarged total vacancy concentrations. However, they mentioned that the boron doped films shows no SEDSGG even heavy doping and/or high temperature annealing which is related to the compensation effect of grain growth. There is no report related to the

SEDSGG with doping by Ge films, however, the effects what they mentioned should be considered to control the SEDSGG growth rate of my experiment.

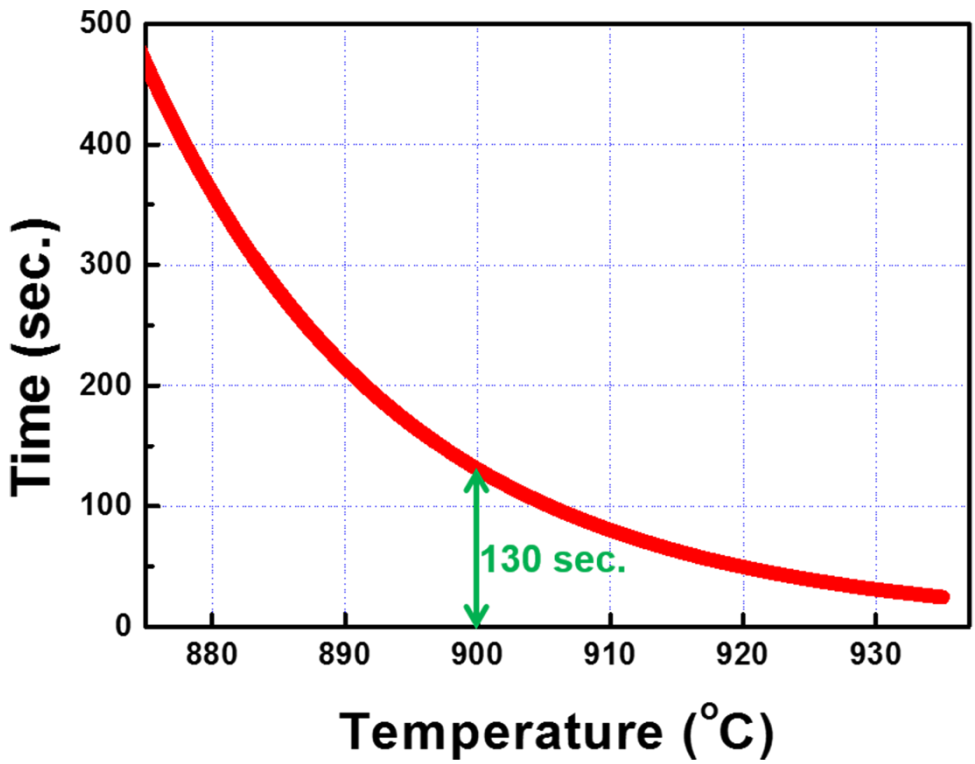


Figure 4.5 The available annealing time as a function of annealing temperature based on the thermal budget of VNAND. (At 900 ºC, about 130 seconds annealing is permitted.)

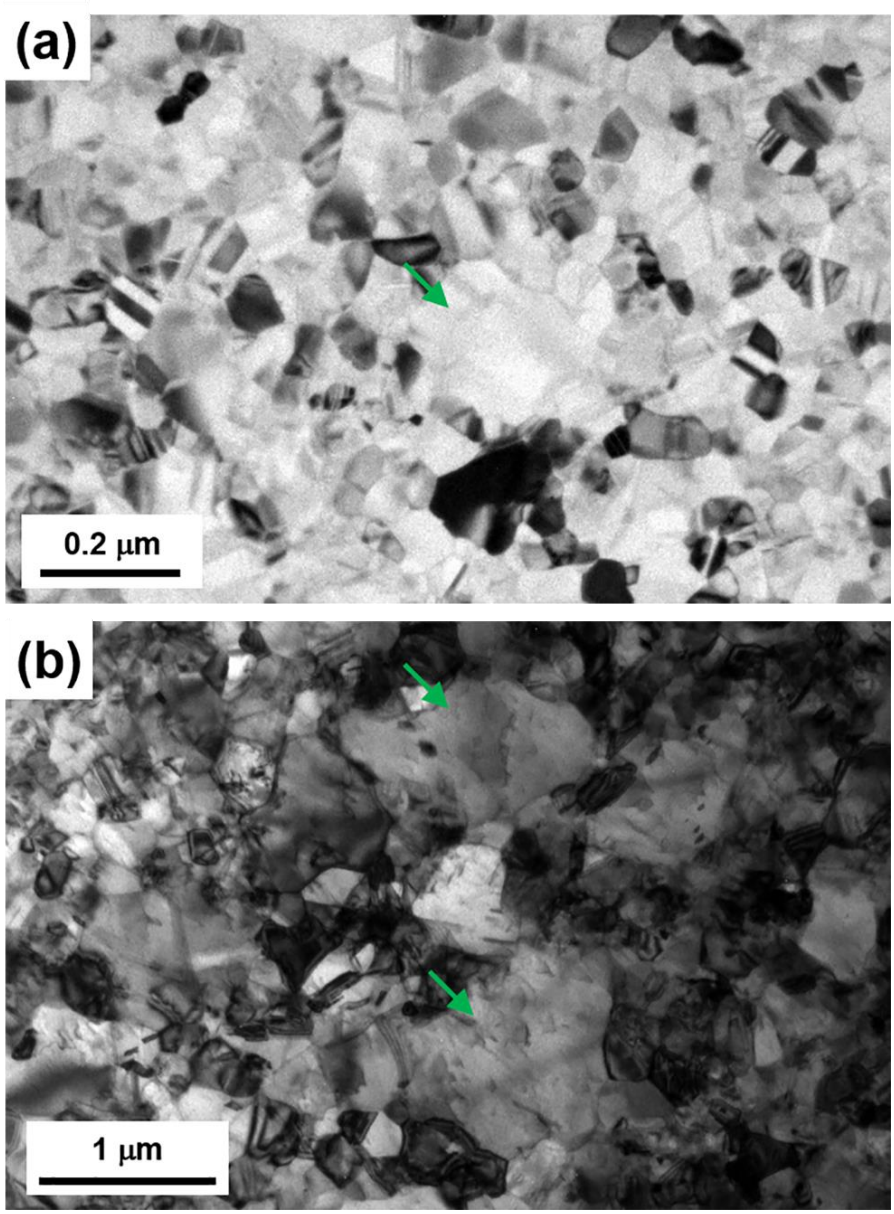


Figure 4.6 The plan-view TEM images of (a) 60 and (b) 500 nm thick poly-crystalline Ge films annealed at 900 ºC for 2 minutes via furnace system.

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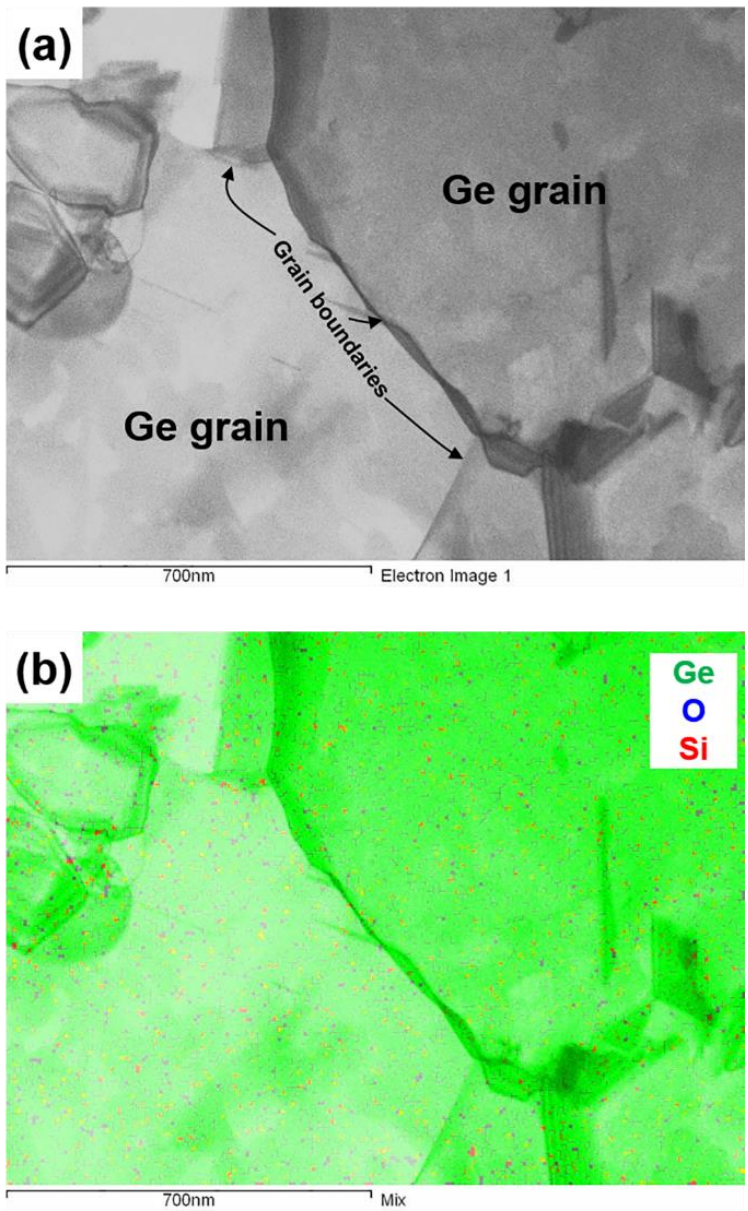

Figure 4.7 The (a) STEM image and corresponding (b) EDS mapping results of 500 nm thick Ge film annealed at 900 ºC for 2 minutes via furnace system.

4.3.3 Two-step annealing

In the chapter 4.3.1 and 4.3.2, the Ge grains over three or four times larger than adjacent grains and over film thicknesses were obtained. It seems there is not a clear definition for secondary grains because it is classified through their relative size compare to the film thicknesses and also their orientations. In this chapter, I suppose that the grains over film thickness can be secondary grains at the initial stage of secondary grain growth. Those secondary grains show various planes following the preferred orientations of poly-crystalline Ge in the SADP characterization.

The development of secondary grains for large size is advantageous in electrical channel materials. Therefore, it is strongly desired to induce secondary grain growth as much as possible in the grain matrix, even though higher temperature and/or longer annealing time can be essential for further development. Hence, I hereby propose the two-step annealing to maximize the grain size in a given VNAND thermal budget. Based on the SEDSGG theory[64], the main driving force for secondary grain growth is the surface energy anisotropy of normal grains. The as-deposited poly-crystalline film shows fiber-like structure[87] and it is identified through the cross-section microstructure characterization via TEM as shown in Figure 4.8. When this as-deposited poly-crystalline film is annealed at a high temperature like experimental results in the chapter 4.3.1, the normal grain growth might take place first from the fiber-like grains. These developed normal grains

have random orientations which provide surface energy anisotropy. When this structure continues to be annealed, the secondary grains would be sparsely evolved from some normal grains which have lower surface energy than their adjacent grains to reduce the entire energy of film system. However, the size of these secondary grains in the final microstructure would be relatively small, because the induced annealing time is too short for enough enlargements of normal grains. On the other hand, when the as-deposited film is already composed of normal grains, the SEDSGG can be directly take place from the normal grains which already have the surface energy anisotropy via the subsequent high temperature annealing. Therefore, I induce the normal grain growth first to the as-deposited poly-crystalline film and high temperature annealing follows to induce even larger grains. The expected microstructural evolution of proposed two-step annealing compare to direct high temperature annealing is shown as schematics in Figure 4.9.

For the normal grain growth, the as-deposited poly-crystalline Ge films were annealed in a furnace at 800 ^{o}C for 30 minutes and Figure 4.10 shows the corresponding (a) plan-view and (b) cross-section TEM images. The film microstructure was composed of normal grains. The size of those normal grains almost reach to the film thickness. Subsequently, this film is underwent the RTA process at 900 ^{o}C. After annealing, the microstructure was composed of enlarged normal grains and some larger grains about two or three times larger than the adjacent grains. Figure 4.11 shows those larger grains of (a) 500 and (b) 60 nm thick films. The size of such a large grains after two-step annealing are compared

to direct high temperature annealing (named single-step annealing) as shown in Figure 4.11(c) and (d) for 500 and 60 nm thick films, respectively. The large grains supposed as secondary grains are enlarged in the two-step annealing compare to single-step annealing. It is expected that due to the direct evolution from already enlarged normal grains compare to evolution from small normal grains from fiber-like grains as expected in Figure 4.9.

The two-step annealing results indicate that the final microstructure seem to be strongly dependent on the microstructure before 900 ^{o}C annealing. I performed the new two-step annealing (named hybrid annealing) which combines SPC and SEDSGG. There is no report yet using solid phase crystallized film as an initial microstructure for SEDSGG. The expected advantage of hybrid annealing is obtaining even large grains in a final microstructure. This is due to already enlarged large grains at the film surface of solid phase crystallized films through the competitive growth.[19] As an initial film structure, I used amorphous Ge on amorphous Si bi-layer structure and its deposition conditions and initial microstructure are treated in the chapter 3.2.2. The SPC was carried out at 350 ^{o}C for 20 hours and Figure 4.12(a) shows the plan-view TEM image of Ge film after SPC. The Ge films were fully crystallized through the lateral growth as explained in the previous chapter (see 3.2.3). The grain size of solid phase crystallized Ge film is about 240 nm which is eight times larger than the film thickness. This structure is annealed at 900 ^{o}C via RTA. The microstructure is characterized via plan-view TEM and shown in Figure 4.12(b). The hybrid annealed film shows

similar grain morphology with solid phase crystallized film. The abrupt microstructure evolution is not observed such as grain size enlargement.

It is believed that characteristics of initial microstructure. When the film structure is post annealed, different crystallization mechanisms are applied depending on the initial microstructure between as-deposited amorphous and poly-crystalline film. The amorphous and poly-crystallized film is crystallized though the SPC and grain growth, respectively. That led to texture and microstructure differences. In terms of film microstructure, the film after grain growth shows the normal grains as shown in Figure 4.10 through normal grain growth from fiber-like grains. On the other hand, the solid phase crystallized film shows not normal grains but the elliptical or equiaxial microstructure through defect-assisted or random growth mode[51] as shown in Figure 4.12(a). As previously mentioned, the main driving force for secondary grain growth is the surface energy anisotropy of randomly oriented normal grains. It is expected that the different microstructure of solid phase crystallized films may act as obstacles for secondary grain growth. However, C. V. Thompson *et al*.[65] reported the secondary grain growth by using LPCVD deposited amorphous Si films as an initial microstructure through 1200 ^{o}C annealing for 20 minutes. Even though they did not show the exact microevolution during high temperature annealing, such phenomenon is expected that different crystallization mechanisms may be applied for amorphous Si crystallization due to the relatively high annealing temperature (~1200 ^{o}C) compare to conventional Si SPC temperature (~600 ^{o}C) that can lead to secondary grain growth.

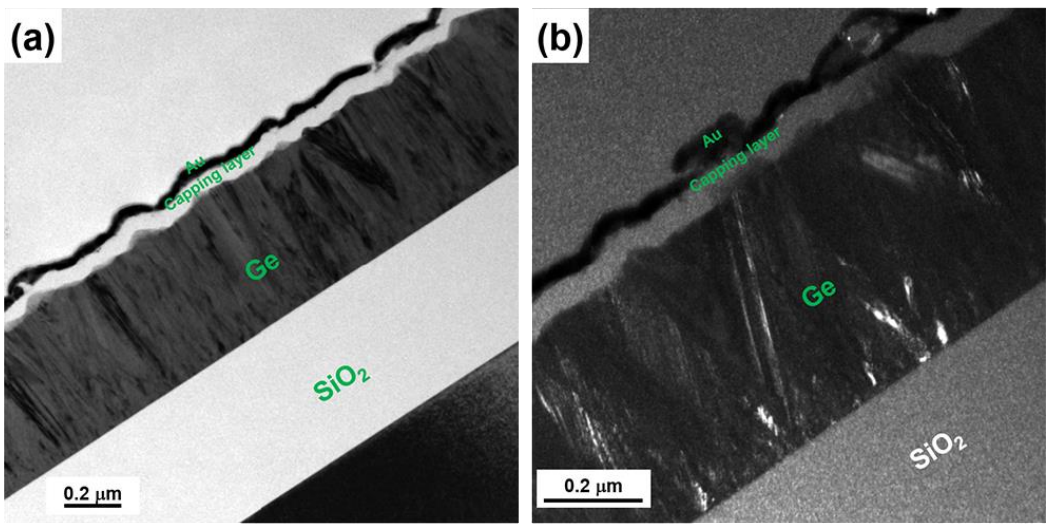

Figure 4.8 The cross-section TEM images of 500 nm thick as-deposited poly-crystalline Ge film through (a) bright and (b) dark field mode.

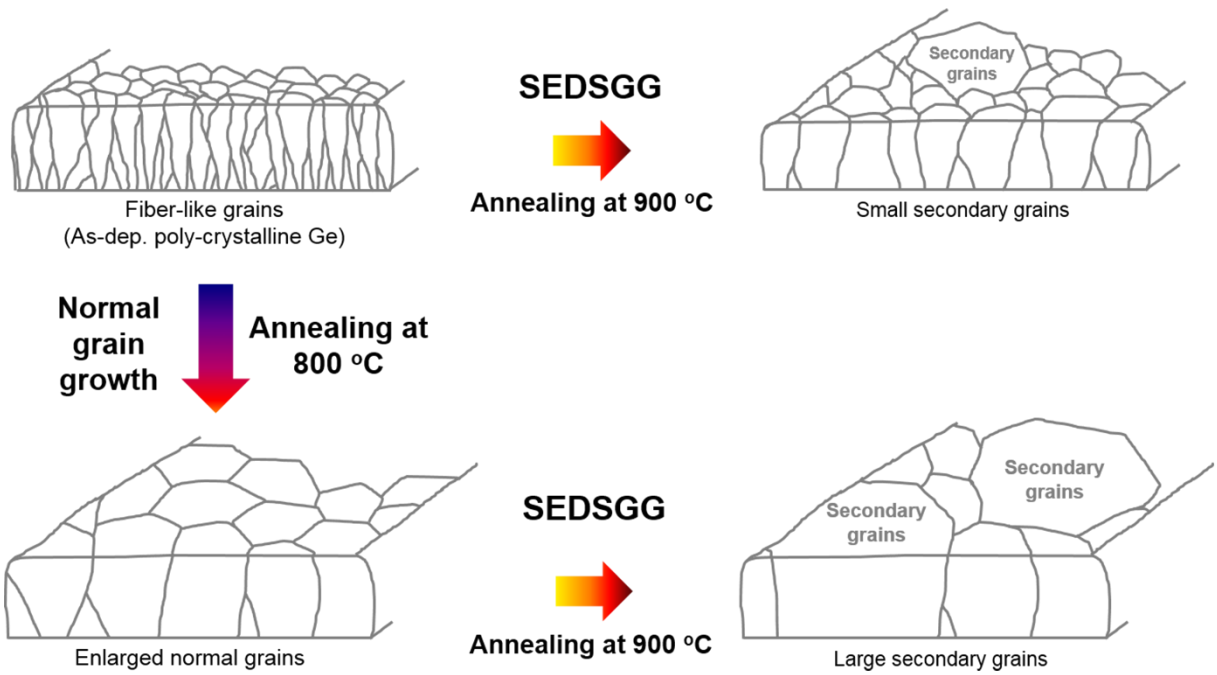

Figure 4.9 The expected microstructural evolution of as-deposited poly-crystalline Ge film depending on the annealing temperature and number of steps.

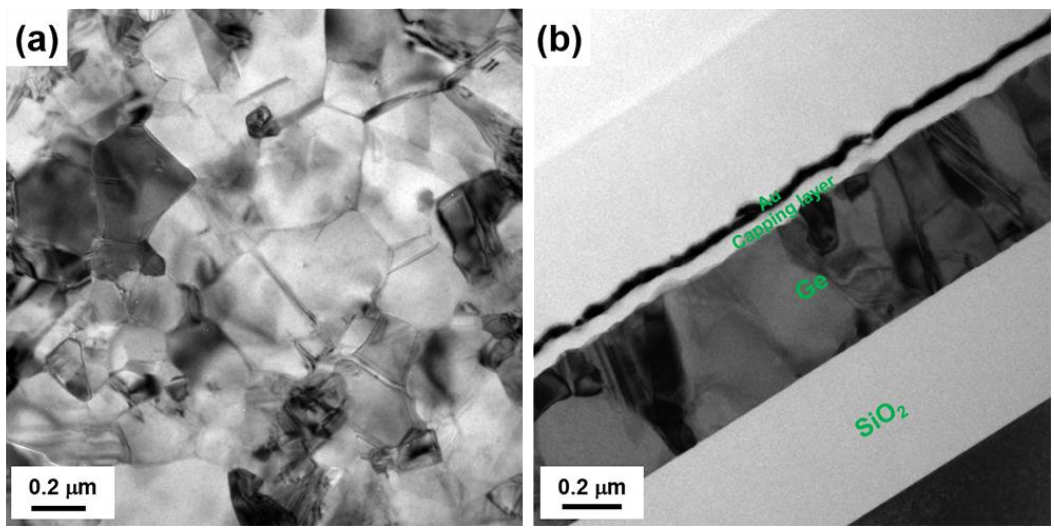

Figure 4.10 The (a) plan-view and (b) cross-section bright field TEM images of 500 nm thick Ge film annealed at 800 ºC for 30 minutes via furnace system.

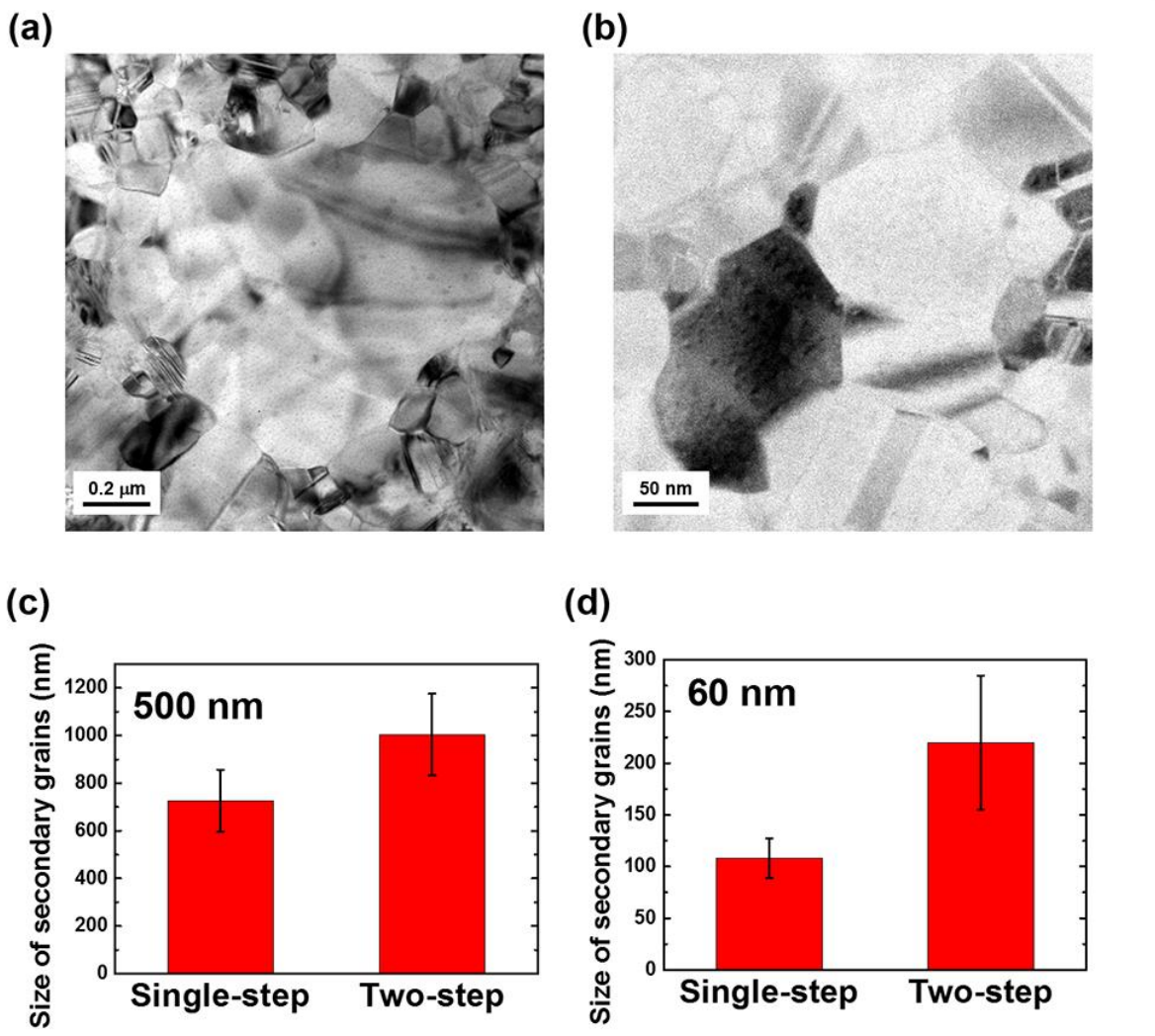

Figure 4.11 The plan-view bright field TEM images of (a) 500 and (b) 60 nm thick Ge films after two-step annealing. The (c) and (d) indicates the size of secondary grains after two-step annealing for 500 and 60 nm thick films, respectively.

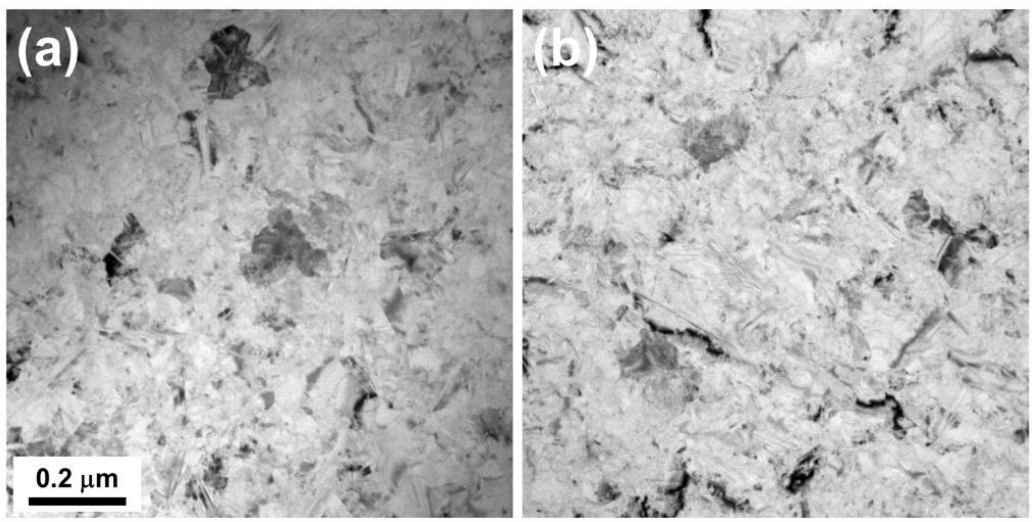

Figure 4.12 The plan-view bright field TEM images after (a) SPC and (b) hybrid annealing. The SPC was carried out at 350 ºC for 20 hours via furnace system. The hybrid annealing was carried out after SPC with subsequent 900 ºC annealing via RTA system.

4.3.4 Carrier mobility of poly-crystalline Ge films

In order to investigate the carrier mobility of poly-crystalline Ge films, Hall measurement was carried out depending on the annealing temperature and steps. Figure 4.13 shows Hall mobility as a function of the annealing temperature for both thicknesses. All poly-crystalline Ge films showed p-type conductivity. As shown in Figure 4.13, the hole mobility gradually increases as the annealing temperature increases. Especially, it rapidly increases at temperatures over 850 ^{o}C where the larger grains are observed as shown in the Figure 4.4. It was also shown that the two-step annealed films at 900 ^{o}C shows much higher hole mobility than the single-step annealed one. It is believed that such a remarkable increase originated from the enlarged grain size both normal and secondary grains of two-step annealed films compared to single-step as explained in the chapter 4.3.3.

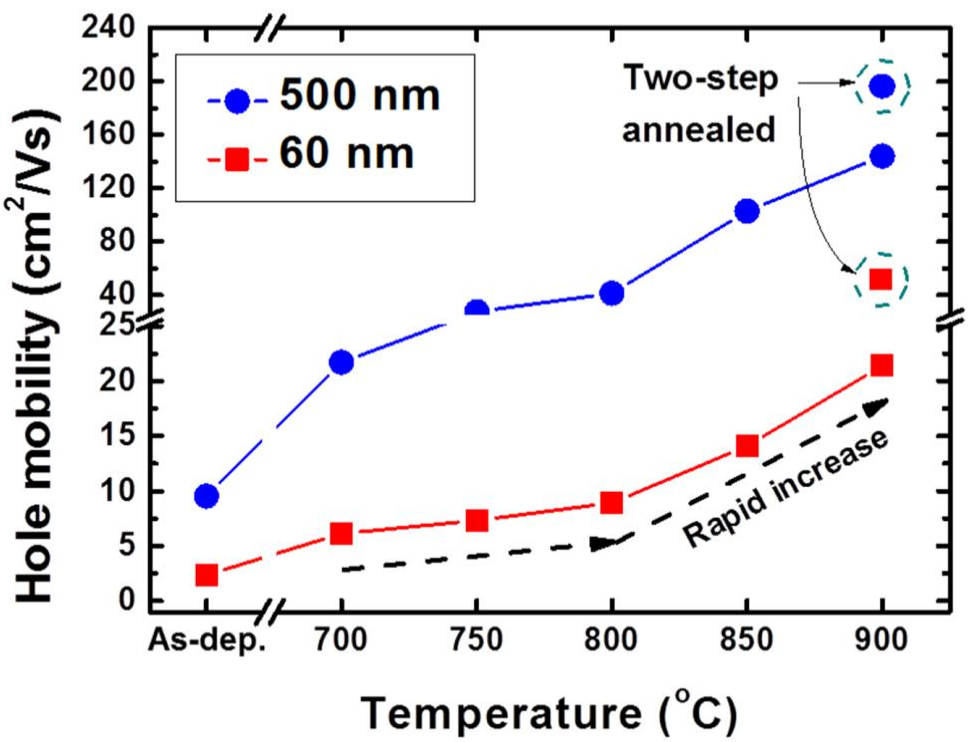

Figure 4.13 The hole mobility of poly-crystalline Ge depending on the annealing temperature and process steps for both thicknesses.

4.4 **Summary**

In this chapter, I proposed Ge SEDSGG for vertical channel in VNAND. It is adopted due to the advantages both higher carrier mobility characteristic of Ge and very large grains over film thicknesses via SEDSGG. In the experiment, I obtained the grains three or four time larger than adjacent grains and over film thicknesses. Also, the two-step annealing is proposed for grain enlargement in a given thermal budget of VNAND and shows great increasing of carrier mobility compare to the conventional single-step annealing. However, the sizes of secondary grains are relatively small compare to previous report for SEDSGG. It is expected due to the limited annealing conditions related to the VNAND thermal budget process. Further research is necessary for secondary grain growth rate increasing via process condition and/or initial microstructure control.

5 Conclusions

The $Si_{1-x}Ge_x$/Si bi-layer and poly-crystalline Ge single layer structures were proposed for vertical channel in VNAND. These structures were suggested in order to improve the microstructural quality by nucleation and/or growth engineering. The solid phase crystallization and grain growth were applied for each structure, respectively as crystallization techniques. Based on the crystallization behavior and the microstructure of films, the advantages for electrical properties as a channel layer were expected.

Firstly, the bi-layer structure which using $Si_{1-x}Ge_x$ as a nucleation layer on a Si channel layer was proposed as a vertical channel structure. Bi-layer structure exhibited the $Si_{1-x}Ge_x$ surface nucleation and the equiaxial microstructure during the crystallization. Based on that, it was expected that the large-grained and less-defective microstructure in the Si channel layer compared to Si single layer structure which was conventionally being used. Based on the crystallization behavior of bi-layer, the $Si_{1-x}Ge_x$ lateral growth method was additionally proposed in order to obtain the even large-grained Si channel microstructure. To maximize the lateral growth effect, it was desired the high contents of Ge in the $Si_{1-x}Ge_x$ nucleation layer and the Ge/Si bi-layer which has pre-existing nano-crystallites in the Ge layer was fabricated. This Ge layer was crystallized through the lateral growth only without any nucleation. After high temperature annealing for Si crystallization, it was examined that the very large grains over film thickness in the

Si layer which grown following the grain boundaries of laterally grown Ge grains. Those microstructural improvement by using a bi-layer is expected to solve the problem associated with electrical property degradations with the increase of the number of cell layers in VNAND.

Secondly, the poly-crystalline Ge single layer was proposed as a vertical channel structure. The SEDSGG technique which shows very large grains over the film thicknesses was combined with Ge. The large grains expected as the secondary grains were observed over 850 ºC annealing. In order to increase the size of secondary grains, the structure was annealed for a long time near device thermal budget. However, the great size enlargement of secondary grains was not observed and it was estimated due to low mobility of grain boundaries of poly-crystalline Ge film. Additionally, two-step annealing method was proposed to enlarge the grain size in a given thermal budget and the expected microstructural evolution was explained. In the Hall measurement, two-step annealed film shows significantly enhanced hole mobility than the film annealed via conventional single-step annealing process.

Acknowledgements

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국 문 초 록

낸드 플래시 메모리는 기존 2차원 평면 구조의 스케일링 한계를 극복하고자 수직방향으로 셀을 적층 하는 3차원 수직 구조가 최근에 개발되었고, 현재는 양산되고 있다. 수직 구조 낸드 플래시 메모리는 소자 구조 및 제조 공정상의 호환성 때문에 고상 결정화 기술을 채널 형성공정으로 사용하고 있다. 하지만 고상 결정화 된 박막이 채널로 사용 될 경우, 그레인간 경계나 그레인 내부의 높은 밀도의 결함들이 소자의 전류를 감소시킨다는 치명적인 단점이 있다. 특히, 차세대 수직 구조 낸드 플래시 메모리에서 용량을 늘리고자 셀을 추가로 수직 적층 할 경우 수직 채널의 길이가 길어짐에 따라, 단위 채널 당 결함 밀도 증가로 인해 스트링 전류 감소가 예상된다. 즉, 고품질 채널 미세구조 형성은 현재 수준의 소자뿐만 아니라 차세대 수직 구조 낸드 플래시 메모리 공정에서 필수적이라 할 수 있다.

따라서 본 연구에서는 수직 구조 낸드 플래시 메모리의 수직 채널 미세구조 특성 향상을 위해 기존의 채널 형성공정에 사용되는 Si 단일 층 채널 구조 대신 $Si_{1-x}Ge_x$/Si 이중 층 구조를 제시하여, 고 품질의 Si 채널 미세구조를 얻고자 하였다. 실험 결과, 제안 된 이중 층 구조는 Si 단일 층 구조와 달리 표면 핵 생성과 등방형 미세구조를 형성함을 확인

하였고, 더 큰 그레인과 낮은 결함밀도를 가진 채널 미세구조를 가질 수 있을 것으로 예상 되었다. 뿐만 아니라 이중 층 구조는 공정이 쉽고 간단하며 수직 구조 낸드 플래시 메모리의 양산 공정에 바로 적용 가능한 방법으로서, 향후 차세대 메모리의 용량증대를 위한 셀 적층 시에 스트링 전류 감소 문제를 해결하는데 직접적인 도움이 될 방법으로 기대된다. 이중 층 구조의 결정화 거동에 기반하여 더 큰 크기의 그레인을 가진 Si 채널 미세구조를 얻고자 측면 성장 방법도 제안 및 연구 되었다. 측면 성장 거동은 $Si_{1-x}Ge_x$의 층의 Ge 함유량에 영향을 받는데, Ge 농도가 높을수록 낮은 온도 열처리가 가능함에 따라 측면 성장 거동에 유리하다. 따라서, 순수 Ge을 핵 생성 층으로 사용하는 Ge/Si 이중 층 구조를 새로 제시하였고, 결정화 거동을 관찰하였다. Ge/Si 이중 층 구조에서 Ge은 핵 생성 없이 측면 성장을 통해서만 결정화 됨을 확인할 수 있었다. 이후 추가 고온 열처리를 통해 Si 층을 결정화 하였고, Si 층은 측면 성장을 통해 이미 크게 형성 된 Ge 그레인 경계를 따라 그대로 성장함이 관찰 되었다. 이는 Ge 층을 제거하면, Si층내 두께에 비해 매우 큰 크기의 그레인을 얻을 수 있는 방법으로서 수직 구조 낸드 플래시 메모리의 채널로 적용 시 각 셀에서의 캐리어 흐름에 도움이 될 뿐만 아니라 스트링 전류 감소 문제도 해결할 수 있을 것으로 기대된다.

추가로 Si 보다 캐리어 이동도가 좋고, 결정화 온도가 낮은 Ge을 수

직 채널 구조 물질로 제시하였다. 실험에 사용 된 채널 구조는 다결정 Ge박막으로 구성 된 단일 층 구조 이다. 더불어 박막 두께를 띄어 넘는 큰 크기의 그레인을 얻을 수 있는 표면 에너지 구동 이차 그레인 성장 방법을 적용하였다. 온도에 따른 결정화 거동 분석을 통해 박막 두께를 띄어 넘고 주변부의 그레인들보다 크기가 큰 그레인을 발견할 수 있었다. 이 큰 그레인들을 성장 초기의 이차 그레인이라고 가정하고, 박막 내 크기 확대를 위해 제한된 수직 구조 낸드 플래시 메모리의 thermal budget 내에서 장시간 열처리 및 미세구조에 대해 분석 하였다. 또한, 같은 thermal budget 내에서 박막 내 그레인의 크기를 더 키울 수 있는 2단계 열처리 방법 제시와 예상 미세구조 변화에 대해 설명하였다. 2단계 열처리 방법은 단일 단계 열처리 방법에 비해 더 큰 그레인들을 보임으로서, 박막의 캐리어 이동도 값을 매우 크게 높였다.

주요어:

수직 구조 낸드 플래시 메모리, 고상 결정화, 그레인 성장, $Si_{1-x}Ge_x$,
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연 구 실 적

I. Publications

1. **Sangsoo Lee**, Yongjo Park, Yong-Hoon Son, Kihyun Hwang, Yoo Gyun Shin and Euijoon Yoon, *"Lateral growth induced bi-layer for large-grained vertical channel in VNAND"*, (in preparation).

2. **Sangsoo Lee**, Yong-Hoon Son, Yongjo Park, Kihyun Hwang, Yoo Gyun Shin and Euijoon Yoon, *"Ge surface-energy-driven secondary grain growth via two-step annealing"*, Thin Solid Films, **571**, 108 (2014).

3. **Sangsoo Lee**, Yong-Hoon Son, Kihyun Hwang, Yoo Gyun Shin and Euijoon Yoon, *"Advanced Si solid phase crystallization for vertical channel in vertical NANDs"*, APL Materials, **2**, 076106 (2014).

4. Yong-Hoon Son, **Sangsoo Lee**, Kihyun Hwang, Seung Jae Baik, and Euijoon Yoon, *"Laser-induced epitaxial growth technology for monolithic three dimensional integrated circuits"*, ECS Journal of Solid State Science and Technology, **2**, 230 (2013).

5. **Sangsoo Lee**, Yong-Hoon Son, and Euijoon Yoon, *"Ge Surface-Energy-*

Driven Secondary Grain Growth for Vertical Channel in 3D NAND Flash Memories", ECS Transactions, **50**, 991 (2012).

6. Changjae Yang, **Sangsoo Lee**, Keun-Wook Shin, Sewoung Oh, Daeyoung Moon, Sung-Dae Kim, Young-Woon Kim, Chang-Zoo Kim, Won-kyu Park, Won Jun Choi, Jinsub Park, and Euijoon Yoon, *"Characterization of deep levels in GaInP on Ge and Ge-on-Si substrates by photoluminescence and cathodoluminescence"*, Journal of Crystal Growth, **370**, 168 (2013).

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8. Keun Wook Shin, Hyun-Woo Kim, Jungsub Kim, Changjae Yang, **Sangsoo Lee** and Euijoon Yoon, *"The effects of low temperature buffer layer on the growth of pure Ge on Si(001)"*, Thin Solid Films, **518**, 6496 (2010).

II. Presentations

International conference:

1. **Sangsoo Lee**, Yong-Hoon Son, Yongjo Park, Kihyun Hwang, Yoo Gyun Shin and Euijoon Yoon, *"Crystallization behavior of $Si_{1-x}Ge_x$ in $Si_{1-x}Ge_x$ /Si bi-layer structure for vertical channel in VNAND"*, The 17th ISPSA, 2014, Jeju, Korea.
2. **Sangsoo Lee**, Yong-Hoon Son, Kihyun Hwang, Yoo Gyun Shin and Euijoon Yoon, *"Surface Nucleation and Grain Growth of SiGe/Si bi-layer for Vertical Channel in VNANDs"*, spring E-MRS meeting, 2014, Lille, France.
3. **Sangsoo Lee**, Yong-Hoon Son, and Euijoon Yoon, *"Ge Surface-Energy-Driven Secondary Grain Growth for Vertical Channel in 3D NAND Flash Memories"*, 222nd ECS meeting, 2012, Honolulu, USA.
4. **Sangsoo Lee**, Yong-Hoon Son, and Euijoon Yoon, *"Ultra Large-Grained Ge Channels for 3D Vertical NAND Flash Memories"*, IUMRS-ICA 2012, 2012, Busan, Korea.
5. Changjae Yang, **Sangsoo Lee**, Keun Wook Shin, Daeyoung Moon, Sewoug Oh, Gun-Do Lee, Chang-Zoo Kim, Won-Kyu Park, Won Jun

Choi and Euijoon Yoon, *"Study of the optical properties of GaInP on Ge and Ge-on-Si substrates by photoluminescence and cathodeluminescence"*. 16th ICMOVPE, 2012, Busan, Korea.

6. Changjae Yang, Keun Wook Shin, **Sangsoo Lee**, Sewoung Oh, Chang-Zoo Kim, Won-Kyu Park, and Euijoon Yoon, *"Investigation of III-V layers grown on the Ge-on-Si substrate for the solar cell operation"*, MRS Fall Meeting, 2011, Boston, USA.

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International workshop:

1. **Sangsoo Lee**, Yong-Hoon Son, and Euijoon Yoon, *"Surface-energy-driven Secondary Grain Growth (SEDSGG) in Ge films"*, 8th SUN-Ritsumeikan Univ. Workshop, 2011, Seoul, Korea.

Domestic conference:

1. **Sangsoo Lee**, Yong-Hoon Son, Yongjo Park, Kihyun Hwang, Yoo Gyun Shin, Euijoon Yoon, *"Lateral growth induced SiGe/Si bi-layer for vertical channel in VNAND"*, 추계 재료학회, 2014, 대전.

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III. Award Event

1. **Sangsoo Lee**, *"Crystallization behavior of $Si_{1-x}Ge_x$/Si bi-layer structure for vertical channel in VNAND"*, Gold award in Physical Devices & Science at the 21st Samsung HumanTech paper award.