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공학박사 학위논문

A study on the low temperature buffer layer for III-nitride electronic device

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Abstract

A study on the low temperature buffer layer for III-nitride electronic device

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The group III-nitride semiconductors with their wide applications in electronic devices such as high electron mobility transistor (HEMT) have attracted much research interest in the past two decades. A major drawback of III-nitride is that native substrates are not yet available in large quantities, so heteroepitaxy using foreign substrates such as Si and sapphire have been widely used. Unfortunately, although both materials have been chosen as substrates for GaN epitaxial growth, the substrates are badly matched to GaN with respect to their lattice constant and thermal expansion coefficient. In addition, when atoms such as Ga are deposited on the substrate, the atoms are very mobile on the plain substrate, so homogeneously wetting on the substrate is difficult. To solve the problems, buffer layer was developed in the growth of GaN layer, resulting in rapid progress in III-nitride growth.

Accordingly, the buffer techniques have become critical key issue and determine the properties of III-nitride. However, several problems such as leakage current, wafer bowing and metal-organic chemical vapor deposition (MOCVD) chamber condition still exist, resulting in the degraded properties of electronic device. To overcome these problems, new low temperature buffer layers for each substrate were proposed in this study.

The problems in epitaxial growth of GaN on Si substrate, first of all, were investigated when AlN buffer layer, conventional buffer layer for GaN on Si, was grown by same MOCVD system for the GaN growth. We confirmed MOCVD reactor circumstance related with previous GaN growth run, Ga memory effect, is significant for properties of GaN/AlN/Si structure. The small amount of Ga from the Ga memory effect affected the final stress and crystal quality of GaN on Si as well as the surface of AlN buffer layer. To solve the Ga memory effect, we proposed a AlN buffer layer deposited by DC magnetron sputtering at room temperature. The ex-situ buffer layer could be effective solution to avoid growth circumstance problem in MOCVD reactor since the system does not include Ga. Moreover low growth temperature could prevent interdiffusion between Si-Al, leading to leakage path. For epitaxial growth of AlN on Si substrate by DC magnetron sputtering at room temperature, the pre-deposited Al process, deposition of thin Al layer before main AlN deposition, was developed. It was expected that the activation energy for epitaxial growth of AlN on Al interlayer became lower than it on Si substrate, resulting from smaller lattice mismatch between AlN and Al (6~8%) than between AlN and Si (19%). Moreover, the sufficient kinetic energy from the high DC power helped epitaxial growth of AlN even at the room temperature. Also, single crystalline GaN was successfully grown by

MOCVD on the AlN buffer layer, which shows the new room temperature AlN buffer layer could be substituted for conventional AlN buffer layer grown at high temperature by MOCVD system.

Additionally, new low temperature (LT) GaN buffer layer for GaN on sapphire substrate was proposed to solve problems of the GaN on sapphire which are low resistivity and convex wafer bowing. The LT GaN buffer layer was fabricated as introduction of tri-methylgallium (TMGa) into the reactor together with ammonia during the temperature ramp-up after the growth of a LT GaN buffer layer. We confirmed nano-columnar structure of the buffer layer with high carbon concentration and investigated the growth mechanism. The GaN layer on sapphire with new LT GaN buffer layer revealed the high-resistivity characteristic and reduction of wafer bowing. A HEMT device made on the layer showed a good pinch-off characteristic and high off-state breakdown voltage over 800 V at a gate voltage of -4 V, implying the new LT buffer layer is effective to grow GaN on sapphire for electronic device.

Key Words:
Buffer layer, GaN, AlN, Metalorganic chemical vapor deposition (MOCVD), DC magnetron sputtering, High electron mobility transistor (HEMT), Si substrate, Sapphire substrate, Memory effect, Semi-insulating GaN, wafer bowing, room temperature growth

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Contents

List of Tables ..... **viii**

List of Figures ..... **ix**

Chapter 1. Introduction **1**

1.1. III-nitride based devices 1

1.1.1 General properties of III-nitride materials 1

1.1.2 The principal of formation of two-dimensional electron gas in III-nitride semiconductor 3

1.2. Growth of III-nitride film 10

1.2.1 Epitaxial growth of III-nitride 10

1.2.2 The intrinsic stress evolution at the grain boundary in the film 11

1.3. Substrate for III-nitride 18

1.3.1 Si substrate 18

1.3.2 Sapphire substrate 19

1.4. Buffer layer in III-nitride 24

1.4.1 Buffer layer for Si substrate 24

1.4.2 Buffer layer for sapphire substrate 26

1.5. The problems of the buffer layer for HEMT device 32

1.5.1 Electrical problem 32

1.5.2 Stress problem..... 34

1.5.3 Dislocation problem 35

1.6. Thesis contents and organization 41

1.7. Bibliography 43

Chapter 2. The problem of GaN on Si grown by MOCVD – Investigation of Ga memory effect 51

2.1. Introduction..... 51

2.2. Experimental procedure..... 53

2.3. The effect of AlN run sequence for GaN on Si substrate..... 56

2.4. Ga memory effect for AlN buffer layer on Si 68

2.5. Summary..... 76

2.6. Bibliography 77

Chapter 3. Growth of AlN buffer layer on Si substrate by DC magnetron sputtering at room temperature 81

3.1. Growth of AlN buffer layer with same alignment of out-of-plane 81

3.1.1 Introduction..... 81
3.1.2 Experimental procedure..... 83
3.1.3 Results and discussion..... 85
3.1.4 Summary..... 96

3.2. Epitaxial growth of single crystalline AlN buffer layer on Si (111) 97

3.2.1 Introduction..... 97
3.2.2 Experimental procedure..... 99
3.2.3 Results and discussion..... 102
3.2.4 Summary..... 121

3.3. Further study of AlN buffer layer grown by DC magnetron sputtering at room temperature..... 122

3.3.1 Annealing process for AlN buffer layer..... 122
3.3.2 Further study on the pre-deposition process 129

3.4. Bibliography..... 134

Chapter 4. The development of low temperature buffer layer for GaN on sapphire..... 139

4.1. Introduction 139

4.2. Experimental procedure 142

4.3. Results and discussion 145

4.3.1 Semi-insulating characteristics 145

4.3.2 Characteristic of less bowed GaN and crystal qualities..... 156

4.4. Investigation of growth mechanism and evaluation of HEMT device..... 165

4.4.1 Investigation of growth mechanism and new low temperature buffer layer …….. 165

4.4.2 Evaluation of HEMT device 174

4.5. Summary 177

4.6. Bibliography 178

Chapter 5. Conclusion 183

국 문 초 록..... 186

Publication list 190

List of Tables

Table 1.1 Physical properties of Si, 4H-SiC and GaN. 5

Table 1.2 Physical properties of GaN, AlN, Si(111) and Sapphire.[4] 22

Table 2.1 The experimental growth sequences of samples. 55

Table 2.2 Summary of results in annealed Si substrate. 73

Table 3.1 The sputtering parameters in the experiment. 84

Table 3.2 The (0002) AlN peak results according to the Ar : N_2 ratio. 91

Table 3.3 Detailed deposition parameters of the samples. 101

List of Figures

Figure 1.1 Crystal structure of hexagonal GaN along (a) [0001] and (b) [1010] [14] and (c) unit cell of wurtzite GaN[8]. 6

Figure 1.2 Atomic arrangement in Ga-face and N-face GaN. 7

Figure 1.3 Band diagram of the heterostructure formed by lightly n-doped narrow bandgap semiconductor and heavily n-doped wide bandgap semiconductor before and after the contact.[10] 8

Figure 1.4 Polarization induced sheet charge density and directions of the spontaneous and piezoelectric polarization in Ga-face of (a) AlGaN with tensile stress on GaN structure, (b) relaxed AlGaN on GaN structure and (c) GaN with compressive stress on AlGaN structure. 9

Figure 1.5 Schematic illustrations of (a) homoepitaxial structure and (b) strained and (c) relaxed heteroepitaxial structure. 15

Figure 1.6 (a) Polycrystalline thin film before and after the point of crystallite coalescence. (b) Crystallite coalescence process, showing the elastic displacements and stresses associated with forming a continuous film.[17] 16

Figure 1.7 Growth of polycrystalline film after the point of crystallite coalescence. The film grows in a strained state (a) for the case of low adatom mobility, but (b) for the case of high adatom mobility, surface diffusion to the grain boundaries allows the stresses to be relaxed during subsequent film growth.[17] 17

Figure 1.8 (a) Perspective view of Si along various directions of [001], [011] and [111].[31] (b) atomic arrangement of GaN on Si (111).[27] 21

Figure 1.9 (a) The hexagonal unit cell of sapphire (green line shows the rhombohedral unit cell). (b) Atomic arrangement of GaN on sapphire (green balls represent GaN lattices rotated with respect to the substrate by 30°). 23

Figure 1.10 SEM image of GaN film grown without GaN buffer layer.[38] . 28

Figure 1.11 (a) Conventional structure of GaN on Si structure with HT AlN buffer layer and the picture of GaN on 6-inch Si substrate. (b) Conventional structure of GaN on sapphire structure with LT GaN buffer layer and the picture of GaN on 2-inch sapphire substrate..... 29

Figure 1.12 SEM image of GaN on Si after meltback etching has occurred. The GaN layer shows a rough surface and deep hollows in the Si substrate caused by the etching reaction visible.[34] 30

Figure 1.13 Schematic diagram of the growth process of GaN on the AlN buffer layer as the cross sectional view.[37] 31

Figure 1.14 The possible leakage current path through (a) buffer layer and (b) interface between buffer layer and substrate in HEMT structure.. 37

Figure 1.15 The AES atomic depth profiles of AlN grown on Si substrate at 1040 ^{o}C by MOCVD. 38

Figure 1.16 (a) Topography and (b) current image taken under bias (-3 V) and (c) current image taken under forward bias (+2.5 V) at the same position from scanning current-voltage microscopy.[47] 39

Figure 1.17 In-situ curvature measurement of two identically thick GaN on Si samples containing a high- or a low-temperature AlN interlayer.[58] 40

Figure 2.1 The radius of curvature (left axis) and tensile stress (right axis) in the GaN on samples. 60

Figure 2.2 Plan-view SEM images of (a) sample A, (b) sample B, (c) sample C and (d) sample D. Inset: cross-sectional TEM images of the (a) sample A and (d) sample D..... 61

Figure 2.3 5 x 5 μm^2 topological AFM images of (a) sample A, (b) sample B, (c) sample C and (d) sample D. The RMS roughness of the samples are 4.61 (sample A), 3.93 (sample B), 3.39 (sample C) and 2.06 (sample D) nm, respectively. 62

Figure 2.4 Plan-view SEM images of 15 s and 30 s GaN on (a) sample A, (b) sample B, (c) sample C and (d) sample D..... 63

Figure 2.5 Cross-sectional SEM images of 15 s and 30 s GaN on (a) sample A, (b) sample B, (c) sample C and (d) sample D. 64

Figure 2.6 Cross-sectional scanning TEM images of (a) 15 s GaN and (b) 30 s GaN on sample A and (c) 15 s GaN and (d) 30 s GaN on sample D. The red arrows indicate pits of AlN layer..... 65

Figure 2.7 Schematic diagram showing the initial growth behavior of GaN on (a) sample A and (b) sample D. The dotted arrows indicate the grain boundaries formed when GaN islands are coalesced. i.e. the site generating tensile stress..... 66

Figure 2.8 XRD FWHM values of (0002) and (1012) reflection of GaN on samples..... 67

Figure 2.9 Ga concentration in the samples. 71

Figure 2.10 Cross-sectional high-resolution TEM images showing interface between AlN and Si of (a) sample A and (b) sample D. Inset: Fast Fourier transform images corresponding to the HRTEM..... 72

Figure 2.11 5 x 5 μm^2 topological AFM images of annealed Si (111)

substrate of (a) sample I, (b) sample II and (c) sample III. 74
Figure 2.12 Si-Ga Phase diagram.[34] 75

Figure 3.1 XRD θ-2θ patterns of sputtered AlN layer and the GaN layer grown by MOCVD system on the sputtered AlN layer. 89
Figure 3.2 XRD θ-2θ patterns of the AlN films sputtered under varying pressures of 1-5 mTorr, at a constant DC power of 400 W, room temperature and flow rate of Ar (10 sccm) and N_2 (10 sccm) gas. 90
Figure 3.3 XRD θ-2θ patterns of the AlN films sputtered under various DC power, at a constant pressure of 1 mTorr, room temperature and flow rate of Ar (10 sccm) and N_2 (10 sccm) gas. 92
Figure 3.4 (a) XRD θ-2θ patterns, (b) XRD ϕ-scans for the $(1012)_{GaN}$ and (c) plan-view SEM image of the GaN grown on AlN layer sputtered under DC power of 600 W, pressure of 1 mTorr, room temperature and flow rate of Ar (10 sccm) and N_2 (10 sccm) gas. 93
Figure 3.5 (a) XRD θ-2θ patterns and (b) XRD ϕ-scans for the $(1013)_{AlN}$ of the AlN layer sputtered under DC power of 600 W, pressure of 1 mTorr, room temperature and flow rate of Ar (10 sccm) and N_2 (10 sccm) gas. 94
Figure 3.6 Schematic diagrams showing the alignment direction of the each columns in (a) poly-crystalline sputtered AlN and (b) single-crystalline sputtered AlN. 95
Figure 3.7 XRD θ-2θ scan pofiles of (a) sample A, (b) sample B, (c) sample C and (d) sample D. XRD ϕ-scan profiles for the $(1013)_{AlN}$ plane of (e) sample A, (f) sample B, (g) sample C and (h) sample D.. 111

Figure 3.8 (a) Cross sectional TEM image, (b) HR TEM image of the AlN layer and (c) the corresponding FFT pattern of sample A. (d), (e) and (f) the data of sample B. 112

Figure 3.9 XRD asymmetric ϕ-scan profiles for AlN (1011) and Si (220) plane. 113

Figure 3.10 XRD θ-2θ scan profile of 100-nm-Al layer on Si substrate by sputtering system. 114

Figure 3.11 (a) HR TEM image of sample A at the interface between AlN and Si substrate and (b) the corresponding FFT pattern. (c) HR TEM image of sample B at the interface between AlN and Si (inset: the corresponding FFT pattern). 115

Figure 3.12 Schematic model showing the interface between Al (100) and AlN (0002). 116

Figure 3.13 (a) HR TEM image of sample A at the interface between AlN and Si substrate with Al (111) interlayer and (b) the corresponding FFT pattern. (c) Schematic model showing the interface between Al (111) and AlN (0002). 117

Figure 3.14 Free energy path demonstrating the AlN sputtering on Si (left) and on Al/Si (right). 118

Figure 3.15 Pictures of 2 inch template of GaN on (a) sample A and (b) sample B. 119

Figure 3.16 (a) plan-view SEM image (inset: cross-sectional SEM image), (b) XRD θ-2θ pattern and (c) XRD ϕ-scan profiles for the $(10\bar{1}2)_{GaN}$ plane of GaN on sample A. (d), (e) and (f) the data of GaN on sample B (The data is same with Fig. 3.4). 120

Figure 3.17 Sheet resistance map of (a) sputtered AlN (sample A in chap. 3.2) and (b) annealed sample A under ammonia and nitrogen ambient during 10 min by MOCVD. The average sheet resistance is 41.58 and 33,351 Ω/sq, respectively. The schematic in the circle shows ammonia annealing process of sample A..... 125

Figure 3.18 Al_{2p} XPS spectra at the interface between AlN and Si of (a) sample A and (b) annealed sample A. The binding energy of Al-Al is 73.5 eV and Al-Al is 72.4 eV. 126

Figure 3.19 HR TEM image at the interface between AlN and Si of (a) sample A and (b) annealed sample A. 127

Figure 3.20 SIMS depth profiles of Al (red), N (blue) and Si (green) for sample A (deep colors) and annealed sample A (pale colors). 128

Figure 3.21 XRD θ-2θ scan profiles of the 100-nm-thickness Al layers on Si (111) substrate. The table lists the sputtering conditions for each sample. 131

Figure 3.22 XRD θ-2θ scan profiles of (a) 15-nm-thickness Ti layer on Si (111) substrate and (b) 100-nm-thickness Al layers on Si (111) substrate with 5-nm-thickness Ti interalyer (black) and withouth Ti interlayer (red).. 132

Figure 3.23 XRD ϕ-scan profiles for the (1013) plane of sputtered AlN layer with pre-deposited Ti and Al (black) and sputtered AlN layer with only pre-deposited Al (red). The structures of samples are 100-nm-thickness AlN/2-nm-thickness Al/5-nm-thickenss Ti/Si (111) substrate and 100-nm-thickness AlN/5-nm-thickenss Al/Si (111) substrate (in Fig. 3.7(e)), respectively. 133

Figure 4.1 Schematic growth procedure of sample A and B. 144
Figure 4.2 Carrier concentration depth profiles determined by C-V analysis for HEMT structures (15-nm-thick $Al_{0.25}Ga_{0.75}N$ layer) on sample A (red dots) and sample B (black squares)..... 150
Figure 4.3 (a) a schematic diagram of the samples for the TLM measurement. IV characteristics from TLM method of (b) sample A and (c) sample B. 151
Figure 4.4 Plots of total contact to contact resistance as a function of contact separation in TLM measurement for sample A (red dots) and sample B (black squares). The slopes of the lines in sample A and sample B are 1.02 x 10^6 and 3.95 Ω/μm, respectively. The inset illustrates a schematic diagram of the samples for the TLM measurement. 152
Figure 4.5 Buffer breakdown characteristics of the HEMT on sample A. The distance between contacts is 40 μm. The inset shows the enlarged view of the same data in logarithm scale..... 153
Figure 4.6 SIMS depth profiles of carbon (C), oxygen (O) and hydrogen (H) impurities for (a) sample A and (b) sample B. 154
Figure 4.7 Formation energies of C_I , C_N, and C_{Ga} as a function of Fermi-level position in the GaN band gap calculated by density-functional theory for the wurtzite structure. Null growth conditions (neither N nor Ga rich) were simulated here.[31] 155
Figure 4.8 Scan profiles of sample A (red line) and sample B (black line). The extent of wafer bowing was 15 μm (red line) and 34 μm (black line). 160

Figure 4.9 (a) The extent of wafer bowing (left, black) and XRD FWHM (right, blue) at various LT GaN thicknesses under the same TMGa flow rate during the temperature ramp-up process. (b) The extent of wafer bowing (left, black) and XRD FWHM (right, blue) at various TMGa flow rates during the temperature ramp-up at a fixed LT GaN thickness of 60 nm. 161

Figure 4.10 10K PL spectra of GaN layer with various TMGa flow rate during the temperature ramp-up (the samples are same with Fig, 5.9(b))..... 162

Figure 4.11 Crosse sectional TEM images of (a) sample A and (b) sample B. 163

Figure 4.12 8 x 8 μm^2 Plan-view CL images of (a) sample A and (b) sample B. 2 x 2 μm^2 topological AFM images of (c) sample A and (d) sample B..... 164

Figure 4.13 (a) Plan-view SEM image, (b) cross-sectional SEM image, (c) cross-sectional TEM image and (d) XRD ϕ-scan profiles for the $(10\bar{1}2)_{GaN}$ plane of the LT GaN buffer layer grown at 570 ^{o}C on a sapphire substrate..... 169

Figure 4.14 Plan-view SEM images of annealed LT GaN layers from 570 ^{o}C to 1040 ^{o}C: (a) sample I obtained with 3.5 $mmolsec^{-1}$ TMGa flow during temperature ramp-up and (b) sample II obtained without TMGa flow during the temperature ramp-up..... 170

Figure 4.15 Cross-sectional TEM images of annealed LT GaN layers form 570 ^{o}C to 1040 ^{o}C: (a) sample I and (b) sample II. Inset: cross-sectional TEM image of the upper part of sample I (red line). (c) XRD

ϕ-scan of sample I. 171
Figure 4.16 Cross sectional TEM image of HT GaN layer grown on (a) sample I and (b) sample II. 172
Figure 4.17 Schematic diagram showing the two growth mechanisms with and without TMGa flow during temperature ramp-up. 173
Figure 4.18 Schematic diagram showing the HEMT device fabricated with sample A. 175
Figure 4.19 (a) DC I_{DS}-V_{DS} and (b) transfer characteristics of HEMT device on sample A. 176

Chapter 1. Introduction

1.1. III-nitride based devices

1.1.1 General properties of III-nitride materials

The group-III nitride semiconductors including GaN, InN, AlN and their ternary and also quarternary alloys form continuous and direct band-gap energy from 6.2 eV (AlN) to 0.7 eV (AlN). Therefore, III-nitride could be possible to fabricate solid state lightning or light emitting diode (LED) covering whole spectral range from infra-red to ultra-violet region by alloying.[1,2] Beside their superior optical properties, the group-III nitrides show good thermal stability at high temperature, large thermal conductivity, good chemical stability, high electron saturation velocity, and good mechanical strength. The III-nitride alloys are also suitable for electronic devices. Electrical properties of GaN in comparison to other materials for electronic devices are listed in Table 1.1. GaN based devices are idle for both high power and high frequency electronics because of their high saturation velocity, high current rating, low specific on resistance, high breakdown fields, fast switching time and the ability to form two-dimensional electorn gas (2DEG) by using AlGaN/GaN structure.[3,4]

The common crystal structure of group III-nitrides is hexagonal wurtzite since the wurtzite, $P6_3mc$, is thermodynamically stable structure in ambient environment.[5] When the III-nitride is grown with c-plane, which is most common case, the III-nitride has polarization charges located at each of the two surfaces of a layer. The atoms are arranged in bilayers consisting of two

closely spaced hexagonal layers, one with cations and the other with anions, as shown in Fig. 1.1. Due to the displacement of electron charge clouds towards anions, a net positive charge is present on one face and a net negative charge is on the other face. Therefore, internal electric fields occur due to the polarity, and we call it spontaneous polarization (P_{SP}). Figure 1.2 shows two types of polarization of c-plane GaN. The III-nitrides lead an inversion plane perpendicular to the c-axis, so crystal surface have either a group III element (Ga, Al or In) polarity or a N-polarity as shown in Fig. 1.2.[6] In general, GaN grown by metal-organic chemical vapor deposition (MOCVD) on sapphire or Si substrate results in crystals with Ga-face.[7]

There is strain-induced or piezolecetric polarization charges (P_{PE}) as well as the spontaneous polarization. The nature of P_{PE} is attributed to the strain caused by pseudomorphical growth between two lattice mismatched layers while P_{SP} is an inherent characteristic associated with crystal structure.[8] The strain in the epitaxial layer can be compressive or tensile. In the compressive strain case, the epitaxial layer of interest is laterally compressed. For example, thin InGaN (not relaxed) is compressively strained when grown on a thick relaxed GaN layer. In the tensile-strain case, the epitaxial layer of interest is expanded along the lateral direction. For example, thin AlGaN is under tensile strain when grown on a thick relaxed GaN buffer layer.[9] The direction of P_{PE} is determined by the sign of the strain.

1.1.2 The principal of formation of two-dimensional electron gas in III-nitride semiconductor

The heterostructure with different band-gap energy in III-nitride enables to form 2DEG, which is the origin of high electron mobility transistor (HEMT). A heterostructure in the chapter means growth of material with different band gap energy grown on the other. Figure 1.3 shows the heterostructure system before and after the connection with both semiconductors. When two semiconductors are put into contact together, that is thermodynamical equilibrium, the Fermi-level energy (E_F) of the both semiconductors must be in the line what cause the discontinuity in the conduction (E_C) and valence (E_V) band and the band bending.[10] Therefore, triangular quantum well is formed between these two semiconductors. In the quantum well, electrons can move freely paralle to the heterojunction and 2DEG is formed as shown in Figure 1.3, resulting in high mobility.[11] In case of III-nitride structure, the bandgap energy of AlGaN is larger than it of GaN layer; thus, the heterostructure of AlGaN on GaN induces the 2DEG channel.

The accumulation of the charge in the quantum well in AlGaN/GaN heterostructure is caused by P_{SP} and P_{PE} in the structure unlike other III-V semiconductor which needs doped layer. When AlGaN is grown over a relaxed GaN layer, the AlGaN layer will experience tensile strain filed because of the different lattice constant, so the P_{PZ} is negative, meaning that for polarization is pointing toward the substrate, in Ga-face structure as shown in Figure 1.4(a). The P_{SP} for GaN and AlGaN is also negative in Ga-face structure, as mentioned in previous chapter (Figure 1.2). As a consequence, the alignment of the P_{PE} and P_{SP} is parallel in the case of the

tensile strain, and the polarization field will add up in the same direction. In case of compressive stress, the each polarization would be compensated as shown in Figure 1.4(c).[12] The polarization makes high electron density at the interface, that is 2DEG channel. At the interface between AlGaN and GaN, the disparity of the polarization field produces net charges given by

$$\pm\sigma = P_{Total}^{AlGaN} - P_{Total}^{GaN} = (P_{SP}^{AlGaN} + P_{PZ}^{AlGaN}) - (P_{SP}^{GaN} + P_{PZ}^{GaN}) = P_{SP}^{AlGaN} + P_{PZ}^{AlGaN} - P_{SP}^{GaN} \quad [1\text{-}1]$$

That's because relaxed GaN is zero of P_{PZ}. The value is calculated as the order of 10^{13} cm^{-2}. Accordingly, the charge density is describe by

$$n_s = \frac{\sigma}{e} \quad [1\text{-}2]$$

When AlGaN was grown on GaN structure with Ga-face, the total polarization of AlGaN is greater than that of GaN buffer, resulting in positive sheet charge. The value of sheet charge is in the order of 10^{13} cm^{-2}.[13] The AlGaN/GaN heterostructure makes high sheet carrier density with high mobility in 2DEG channel due to the polarization without intentionally doping, so is very attractive for electronic device.

Table 1.1 Physical properties of Si, 4H-SiC and GaN.

Properties	Si	4H-SiC	GaN
Energy bandgap, E_g (eV)	1.1	3.26	**3.4 (direct bandgap)**
Maximum operating temperature (°C)	150	300~	**300~**
Critical electric field, E_c (10^5 V/m)	0.3	3.3	**3.5**
Electron mobility, μ_e (cm^2/V-s)	1450	700	**900 / 2000(HEMT)**
Saturation electron velocity, v_{sat} (10^7 cm/s)	1	2.0	**2.5**
Thermal conductivity (W/cm-K)	1.5	3.5	**1.7**

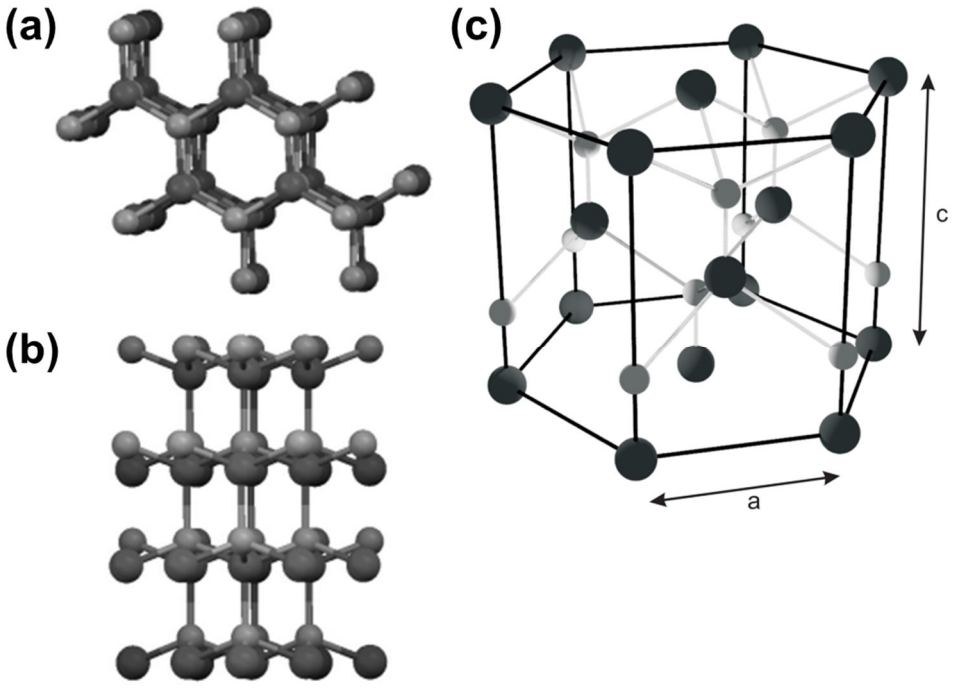

Figure 1.1 Crystal structure of hexagonal GaN along (a) [0001] and (b) [10$\bar{1}$0] [14] and (c) unit cell of wurtzite GaN[8].

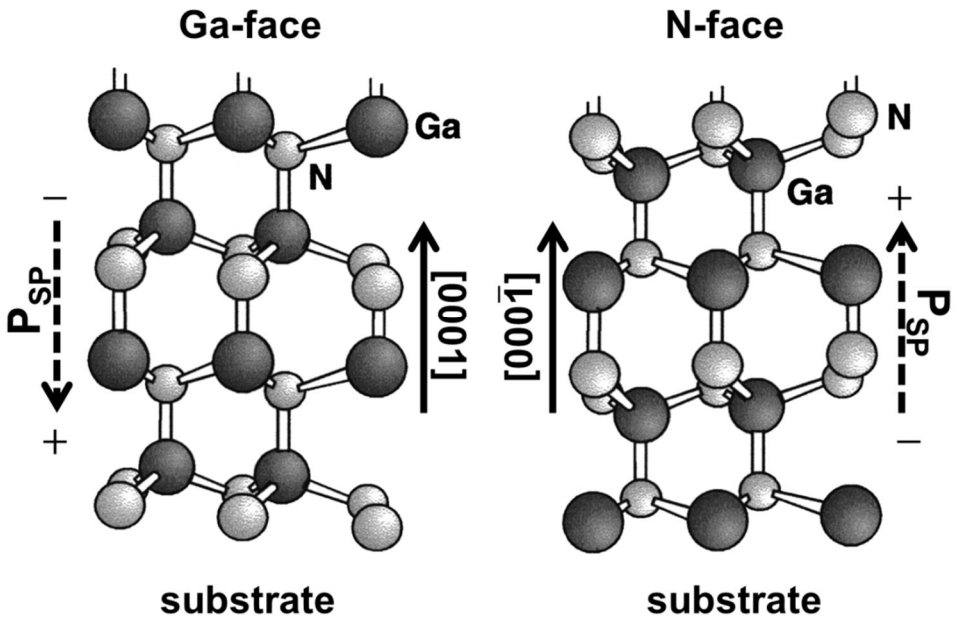

Figure 1.2 Atomic arrangement in Ga-face and N-face GaN.

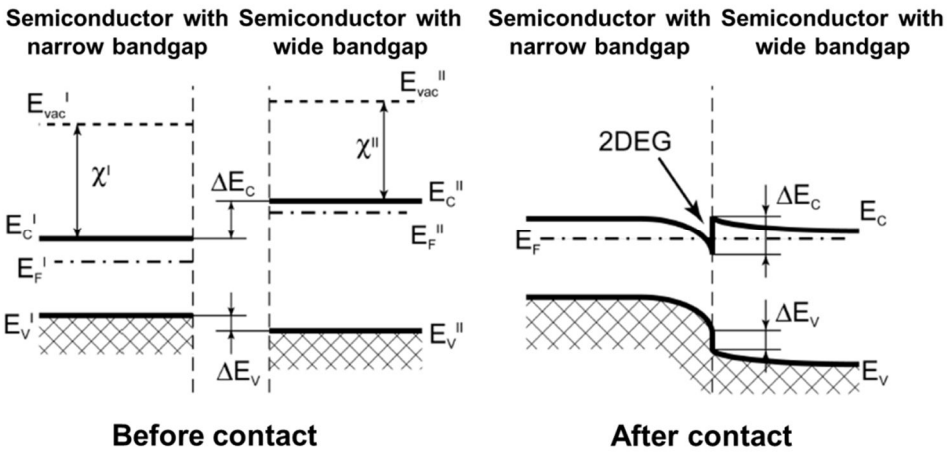

Figure 1.3 Band diagram of the heterostructure formed by lightly n-doped narrow bandgap semiconductor and heavily n-doped wide bandgap semiconductor before and after the contact.[10]

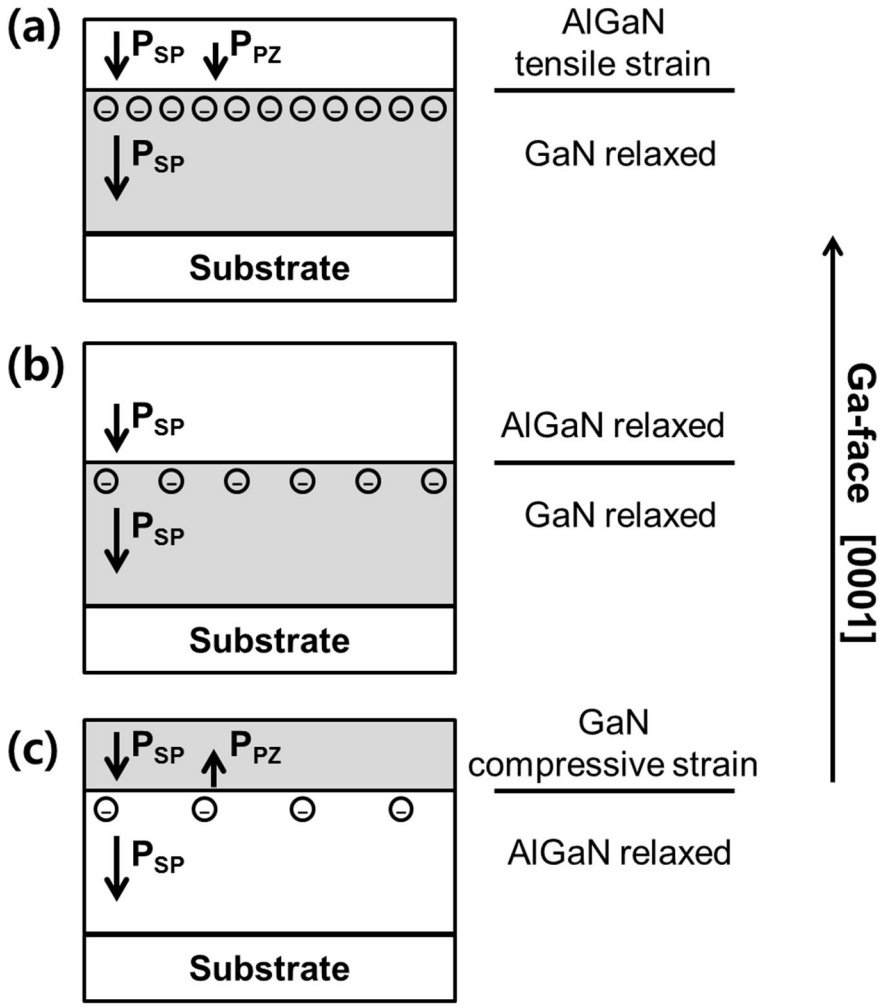

Figure 1.4 Polarization induced sheet charge density and directions of the spontaneous and piezoelectric polarization in Ga-face of (a) AlGaN with tensile stress on GaN structure, (b) relaxed AlGaN on GaN structure and (c) GaN with compressive stress on AlGaN structure.

1.2. Growth of III-nitride film

1.2.1 Epitaxial growth of III-nitride

The term of epitaxy refers to the growth of a crystalline layer on (epi) the surface of a crystalline substrate surface imposing a crystalline order (taxis) onto the thin film. For most thin film applications, especially semiconductor technology, the epitaxial growth is crucial since the crystal structure of material is determined by the epitaxial growth. Properties of the materials such as physical, electrical, optical and so on are affected by crystal structure of the material. In the scientific and technological implications, there are two types of epitaxy; these are homoepitaxy and heteroepitaxy. The homoepitaxy refers to the growth of one element on a crystal surface of its own, e.g. GaN film on GaN substrate. The layers grown homoepitaxially are purer than the substrate and can be doped independently of it. Figure 1.5(a) shows the schematic of homoeptaxy, implying the merit of the homoepitaxy. Because the substrate and film have identical lattice parameters, the film can be nearly stress-free and dislocation-free. The homoepitaxy is widely used in Si or GaAs semiconductor due to easy manufacturing of the substrate, relatively. Unfortunately, in growth of III-nitride, homoepitaxial growth is hardly used because of difficulties in fabrication of nitride substrate. The equilibrium vapor pressure and the melting point of nitride material is very high, and the growth speed of nitride material is even very slow.[15] Accordingly, fabrication of nitride substrate using Czochralski method is almost impossible and the HVPE method is not widely used due to the poor quality of the substrate until now. For these reasons, nitride materials are commonly grown by

heteroepitaxy. The heteroepitaxy refers to the growth of the element on different substrate with the element, e.g. GaN film on Si substrate. For nitride film growth, heteroepitaxy is commonly used due to the lack of its nitride substrate. However the heteroeptiaxy has several problems as shown in Fig. 1.5 due to the lattice mismatch. For many applications nearly matched lattice parameter is desired to minimize defects. As the mismatch gets larger, the film may be strained to accommodate the lattice mismatch from the substrate. The case is arisen during the early stage of film growth as shown in Fig. 1.5(b). When the strain is accumulated until critical point, the dislocation defects at the interface is generated leading to relaxed epilayer and the film returns to its original lattice parameter above the interface like Fig. 1.5(c). Therefore, lattice mismatch is important parameter in heteroepitaxy. The lattice mismatch is defined as:

$$\boldsymbol{mismatch\ \varphi} = \frac{[\boldsymbol{a_0(s)} - \boldsymbol{a_0(f)}]}{\boldsymbol{a_0(s)}} \qquad [1\text{-}3]$$

where, $a_0(s)$ and $a_0(f)$ are lattice constant of the substrate and film, respectively. We have to take an attention to the lattice mismatch when the heteroepitaxial growth is conducted.

1.2.2 The intrinsic stress evolution at the grain boundary in the film

There are many factors to generate stress in film during the film growth. One of the factors is the lattice mismatch mentioned in previous chapter. The mismatch of thermal coefficient expansion between film and substrate causes

stress in the film, which will introduce in Chap.1.5. These result from the heteroeptiaxy. In this chapter, the intrinsic stress from the grain boundaries of crystallites would be introduced. In the island growth mode, the earliest stage of film growth is nucleation and growth of individual crystallites at favorable sites. As the crystallites grow, they begin impingement on each other, eventually forming a continuous film. The development of tensile stresses in the early stages of polycrystalline film deposition has been observed and studied experimentally by many investigations.[16-19] Moreover, in III-nitride film, similar results, tensile stress is generated at initial growth stage, have been reported.[20-23] W. D. Nix et al.[17] explained the occurrence of tensile stress at initial stage by using the coalescence of the island and zipping process and the Nix's model will be introduced here. At coalescence of the individual grains, in brief, the overall energy of the system is lowered by reducing surface area, i.e. surface energy, at the expense of elastic energy of the film-substrate system, hence tensile stress is generated in the film.[24] Although the model were developed from polycrystalline thin films and do not consider epitaxial effects, the energy related arguments used in the model is universally applicable, hence the intrinsic stress in III-nitride have been explained by using the model. Tensile stresses are generated during grain coalescence when boundaries separated by a distance Δ snap together. Consider perfectly regular array of hexagonal crystallites, as shown in Fig. 1.6(a)., with height h and size L = 2a and, before coalescence, are separated by a gap of size Δ.[17] Before coalescence the free energy per unit film area of such an array is expressed as

$$\boldsymbol{E_1 = E_0 + \frac{2h\gamma_{sv}}{a}} \qquad [1\text{-}4]$$

where E_0 is the free energy per unit film area associated with both the top surface of the film and the film/substrate and the second term represents the free energy of the side faces of the crystallites, per unit film area. The surface free energy is represented as γ_{sv}. When the spaces between the crystallites are closed by elastic displacements of the side surfaces, grain boundary by elastic displacements of the side surfaces, grain boundaries are formed in the film, and each of the crystals is subjected to a biaxial strain, $\varepsilon_{elastic} = \Delta/2a$. Accordingly, the free energy after coalescence becomes

$$\boldsymbol{E_2 = E_0 + \frac{h\gamma_{gb}}{a} + \frac{E}{1-\nu} h(\frac{\Delta}{2a})^2} \quad [1\text{-}5]$$

where the second term is the grain boundary free energy and the third term is the strain energy per unit film area. The crystallites are assumed to be elastically isotropic with Yong's modulus E and Poisson's ratio, ν. γ_{gb} is grain boundary interfacial energy. Crystallite would be coalesced spontaneously, until $E_2 - E_1 = 0$, at maximum gap size, Δ_{max}.

$$\boldsymbol{\Delta_{max} = [\frac{4a(2\gamma_{sv} - \gamma_{gb})}{a} \frac{1-\nu}{E}]^{1/2}} \quad [1\text{-}6]$$

and maximum tensile stress generated is therefore,

$$\boldsymbol{\sigma_{max} = [\frac{(2\gamma_{sv} - \gamma_{gb})}{a} \frac{E}{1-\nu}]^{1/2}} \quad [1\text{-}7]$$

The process is illustrated in Fig. 1.6(b).[17] As grow the film, the tendency of stress could be different mode as shown in Fig. 1.7.[17] If arrived adatoms have high mobile, stress created in the film by the coalescence could be relaxed during subsequent film growth. When arriving adatom diffuses to the

grain boundaries due to the high mobility, the additional atoms at the grain boundary will naturally relax the tensile stress in the film, as shown in Fig. 1.7(b). On the other hand, in Fig. 1.7(a), maintained grain boundaries during the subsequent film growth due to low mobility of adatoms could not relax the tensile stress. Therefore, the condition during the film growth has an effect on the intrinsic stress.

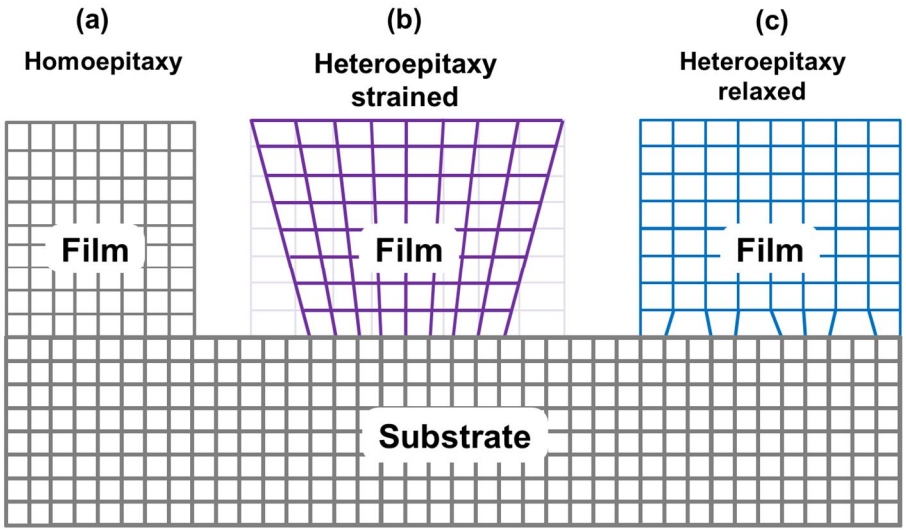

Figure 1.5 Schematic illustrations of (a) homoepitaxial structure and (b) strained and (c) relaxed heteroepitaxial structure.

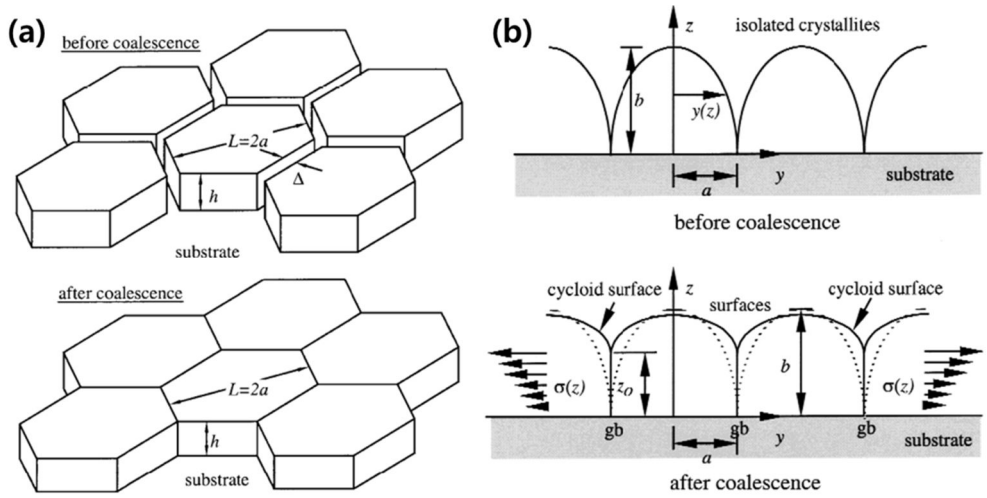

Figure 1.6 (a) Polycrystalline thin film before and after the point of crystallite coalescence. (b) Crystallite coalescence process, showing the elastic displacements and stresses associated with forming a continuous film.[17]

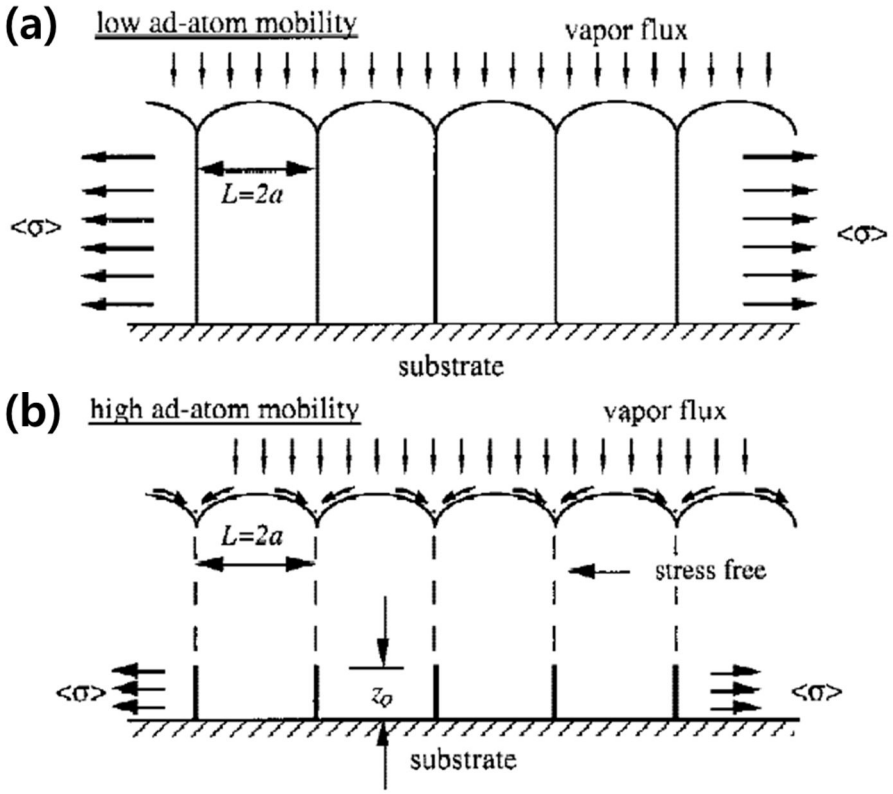

Figure 1.7 Growth of polycrystalline film after the point of crystallite coalescence. The film grows in a strained state (a) for the case of low adatom mobility, but (b) for the case of high adatom mobility, surface diffusion to the grain boundaries allows the stresses to be relaxed during subsequent film growth.[17]

1.3. Substrate for III-nitride

A major drawback of III-nitride is that native substrates are not yet available in large quantities. Accordingly, heteroepitaxy is essential for III-nitride device. It is necessary to choose the suitable foreign substrates for the characteristics of the films. Most commonly, the lattice constant and the structure of crystal material are main criteria for choosing the substrate.[14] Also, the chemical, thermodynamic and electric properties of the subsrate are important elements for the performance of device based on the film. In the structural properties of III-nitride in Fig. 1.1, suitable foreign substrate has to be hexagonal structure with small lattice mismatch with the III-nitride film. Moreover, the thermal stability of the substrate is demanded because III-nitride films are commonly grown at high temperature. The potential substrates which contain the properties mentioned above have been known and investigated. Silicon (Si) and sapphire substrate among the potential substrates have received attention due to the advantages of each substrate. The properties of each substrate are as follows.

1.3.1 Si substrate

Si is most perfected and least expensive substrate that is available in sizes up to 450 mm. Also, Si has good thermal stability under conditions used for GaN growth.[25] This also offers the advantages of compatibility with standard Si processing equipment.[26] The Si has a diamond-lattice structure with the space group of $Fd\bar{3}m$ and each atom in the lattice is surrounded by

four equidistant nearest neighbors that lie at the corners of a tetrahedron.[25] Figure 1.8(a) shows the perspective view along the [001], [011] and [111]. For the growth of wurtzite nitrides, Si (111) is commonly used due to the three-fold surface symmetry, as shown in Fig. 1.8(a). The symmetry gives a good rotational matching for III-nitride. A GaN layer is grown with an in-plane orientations of GaN<10$\bar{1}$0>||Si<$\bar{1}$12> and GaN<$\bar{1}\bar{1}$20>||Si<$\bar{1}$10> and an out-of-plane orientation of GaN<0002>||Si<111>. (Figure 1.8(b)) For the alignment lattice mismatch is 16.9 % to GaN and 19 % to AlN as listed in Table 1.2. The growth of GaN on Si substrate has been extensively investigated, which has been motivated by the huge commercial attraction forming the big market in both power electronics and solid state lightning.

1.3.2 Sapphire substrate

Sapphire has become the dominant substrate for III-nitride epitaxy, owing to tis relatively low cost, availability in large area and continual improvement in its quality.[25] Also, the sapphire is stable at high temperature which is over growth temperature of III-nitrite. The transparent properties and the physical properties make an attention in the use of optoelectronics. Meanwhile, sapphire substrate may still be also attractive in low power HEMT applications in despite of low thermal conductivity.[28] Moreover, other applications using HEMT on sapphire are expected such as transparent conductors[29] or monolithically integrated LED/HEMT layer.[30] Sapphire has the space group of R$\bar{3}c$ and is represented by hexagonal unit cell which is displayed in Fig. 1.9(a). The hexagonal symmetry gives a rotational matching

for III-nitride. The calculated lattice mismatch between the GaN and sapphire is about 49%. However, the actual lattice mismatch of nitride layers with sapphire is reduced by the rotation of the nitride lattice with respect to the substrate unit cell by 30° like figure 1.9(b).[25] Therefore, the lattice mismatch is reduced to ~13 % to AlN and ~16% to GaN. An epitaxial GaN layer is grown with an in-plane orientation of GaN<$01\bar{1}0$>||Sapphire<$\bar{2}110$> and an out-of-plane orientation of GaN<0002>||Sapphire<0006>.

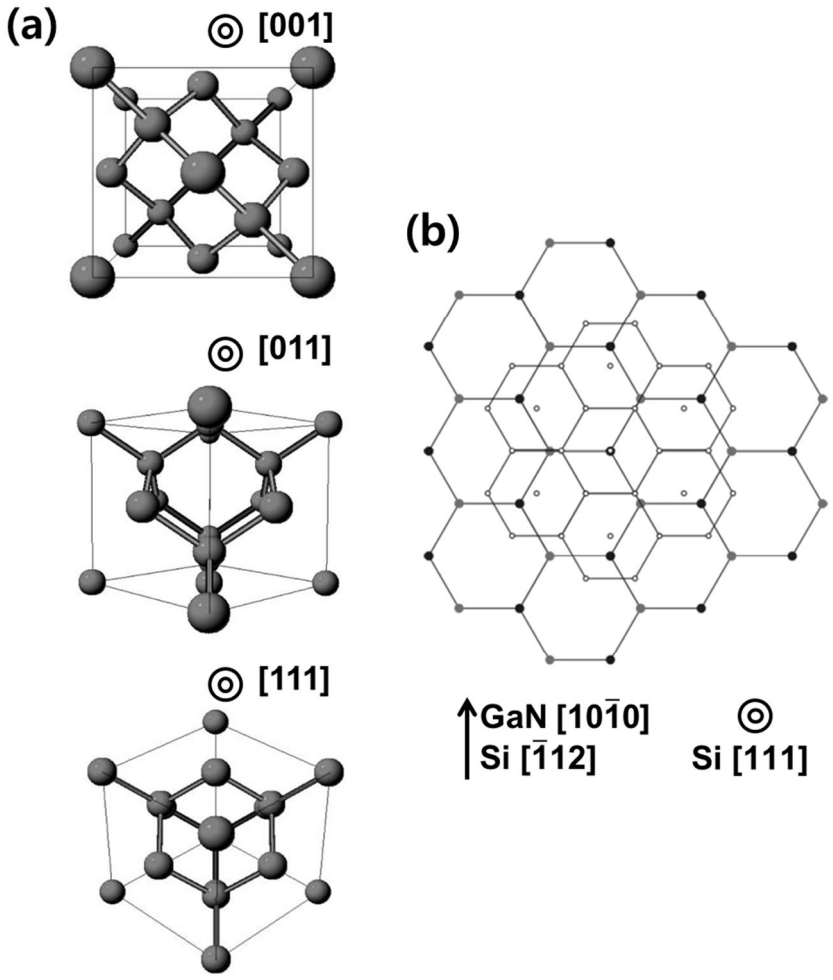

Figure 1.8 (a) Perspective view of Si along various directions of [001], [011] and [111].[31] (b) atomic arrangement of GaN on Si (111).[27]

Table 1.2 Physical properties of GaN, AlN, Si(111) and Sapphire.[4]

Material	GaN	AlN	Si (111)	Sapphire
Lattice constant (Å)	**a = 3.189** c = 5.185	**a = 3.112** c = 4.982	**a = 3.840**	**a = 4.759** c = 12.991
Thermal expansion coefficient ($10^{-6}K^{-1}$)	**a = 5.59** c = 3.17	**a = 5.27** c = 4.15	**a = 2.6**	**a = 7.3** c = 8.5
Thermal conductivity ($Wcm^{1}K^{-1}$)	**4.1**	**5.9**	**1.3**	**0.41**
Melting point (K)	**2791**	**3487**	**1690**	**2303**

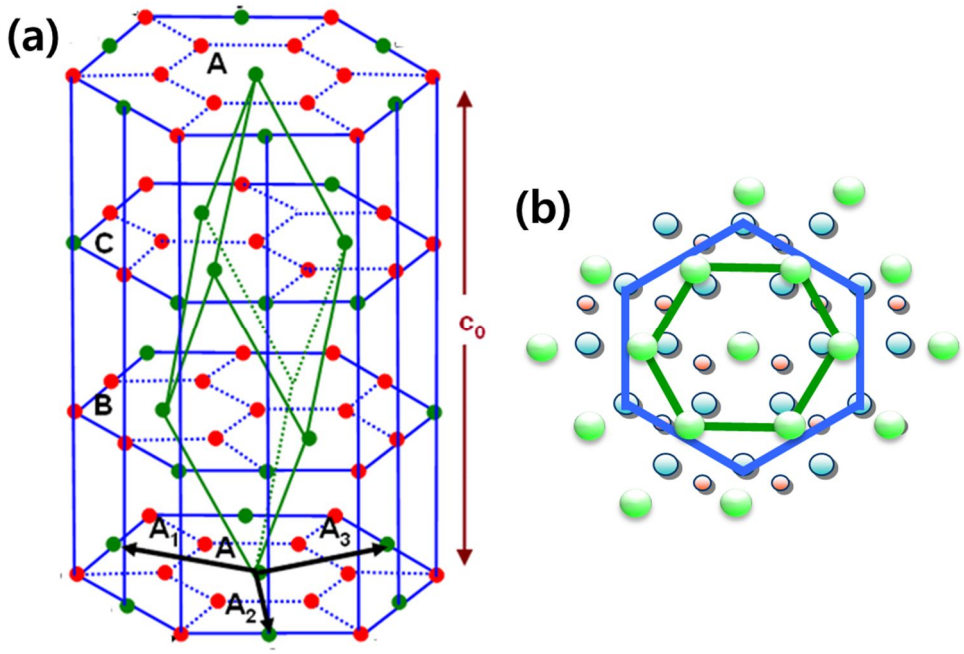

Figure 1.9 (a) The hexagonal unit cell of sapphire (green line shows the rhombohedral unit cell). (b) Atomic arrangement of GaN on sapphire (green balls represent GaN lattices rotated with respect to the substrate by 30°).

1.4. Buffer layer in III-nitride

As we mentioned in previous chapter, GaN is commonly deposited on the foreign substrates such as Si and sapphire due to the difficulty of the bulk growth of GaN. Unfortunately, although both materials have been chosen as substrates for GaN epitaxial growth, the substrates are badly matched to GaN with respect to their lattice constant and thermal expansion coefficient. In addition, when atoms such as Ga are deposited on the substrate, the atoms are very mobile on the plain substrate, so homogeneously wetting on the substrate is difficult. Therefore, GaN layers directly grown on the substrates, normally, exhibit 3 dimensional layer, that is not flat surface, like Fig. 1.10 with low crystal quality. To solve the problems, buffer layer was developed in the growth of GaN layer, resulting in rapid progress in III-nitride growth. Accordingly, the buffer techniques have become critical key issue and determined the properties of III-nitride. High temperature (HT) AlN buffer layer (Fig. 1.11(a)) and low temperature (LT) GaN buffer layer (Fig. 1.11(b)) have been wildly used for Si and sapphire substrates, respectively. We will introduce the conventional buffer layers in each substrate.

1.4.1 Buffer layer for Si substrate

When GaN is grown on a Si substrate, Ga adatoms are mobile, resulting in the poor wetting on the substrate. In addition, several problems exist in the GaN on Si without buffer layer. First, at normal growth condition for GaN, Ga reacts with Si to form a Ga-Si eutectic alloy. It causes a strong and fast

etching reaction, usually refer to as a 'meltback etching'.[4,32] The meltback etching disturbs the 2 dimensional GaN growth as shown in Fig. 1.12. Another problem is the stress problem. As listed in the Table 1.2, there are the mismatches of lattice constant and thermal expansion coefficient between GaN and Si. When GaN film is grown on the Si substrate directly, the film would be in tension during temperature cooling process from the growth temperature, resulting in the cracking problem. The cracking will degrade the device performance such as a non-uniform illumination pattern, current leakage and short lifetime, etc.[4] Therefore, a buffer layer for GaN on Si substrate is desirable not only to give nucleation site for GaN but also to prevent the reaction between Ga and Si and reduce the tensile stress in the structure. Several materials such as hafnium nitride[4], boron monophosphide (BP)[33], Al_2O_3[34] and so on were considered for the buffer layer. Among the several candidates for buffer layer, HT AlN layer is widely used for buffer layer of GaN on Si, due to the relatively easy growth in same MOCVD system. Because of no reaction between Al and Si, the HT AlN layer can be barrier for the diffusion of Ga into the Si substrate. Accordingly, the buffer layer prevents to the meltback etching problem. Moreover, a GaN grown on AlN layer can be under compression due to the larger in-plane lattice parameter of GaN than that of AlN, resulting in compensation for tensile stress in GaN on Si.[32] Therefore, HT-AlN is grown before the GaN growth on Si substrate. However the buffer layer could not solve all problems of GaN on Si, so many studies have been investigated until now.

1.4.2 Buffer layer for sapphire substrate

In the early study on the GaN growth, sapphire, which has similar crystal symmetry with GaN and is thermally and chemically stable, was used as a substrate.[35] However, different lattice constant and thermal expansion coefficients between GaN and sapphire made it difficult to grow high-quality GaN film with a flat surface free from pits and cracks. After many years with the experiments, Akasaki and Amano, who were awarded the 2014 Nobel Prize in Physics, discovered that the growth of thin low-temperature AlN buffer layer prior to high-temperature growth of GaN allowed to grow GaN film with optically flat surface.[36] The flat GaN growth mechanism using LT AlN buffer layer was proposed as shown in Fig. 1.13.[37] According to the mechanism, the AlN columnar structure was formed when LT AlN was annealed to the growth temperature of main-GaN layer. Each GaN nuclei would be generated on top of each columnar structure after the starting of GaN growth. Therefore, high-density nucleation of GaN occurs due to the high density of the AlN columns, as shown in Fig. 1.13, compared to the nucleation density of GaN grown directly on the sapphire substrate. As the GaN gradually grows, only GaN islands preferentially grow up to become larger trapezoid crystals, and lateral growth and coalescence of the islands occur, resulting in the smooth GaN layer.[37] The key point of flat GaN surface is to offer high density nucleation site for GaN. In 1992, Nakamura, who is another 2014 Nobel Prize in Physics winner, invented low temperature GaN buffer layer. The low temperature GaN buffer layer also gives many nucleation sites for GaN, resulting in flat GaN layer.[38] The buffer layer have been widely used until now because the buffer growth method is much

simpler and suitable for mass production as there is no need to change material during the growth process. The buffer technics improved the quality of GaN layer remarkably and made the breakthrough of III-nitride device, but subsidiary problems in GaN growth exist until now.

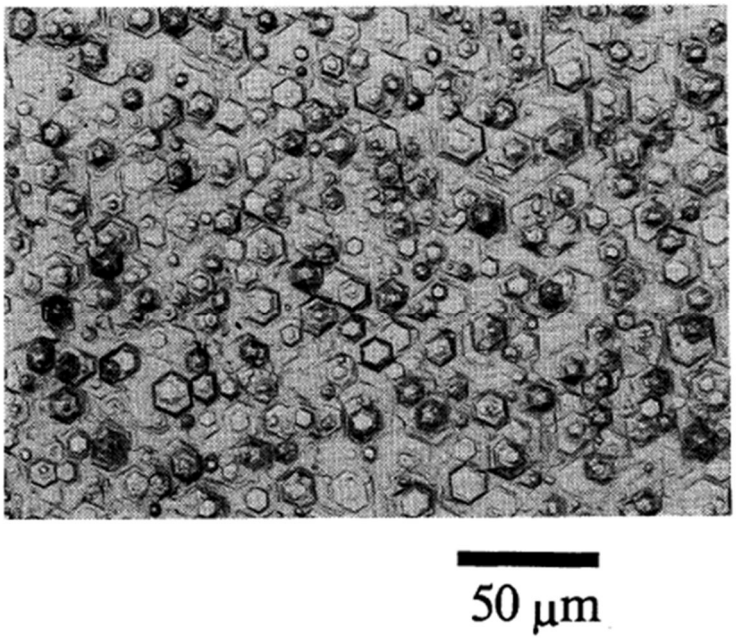

Figure 1.10 SEM image of GaN film grown without GaN buffer layer.[38]

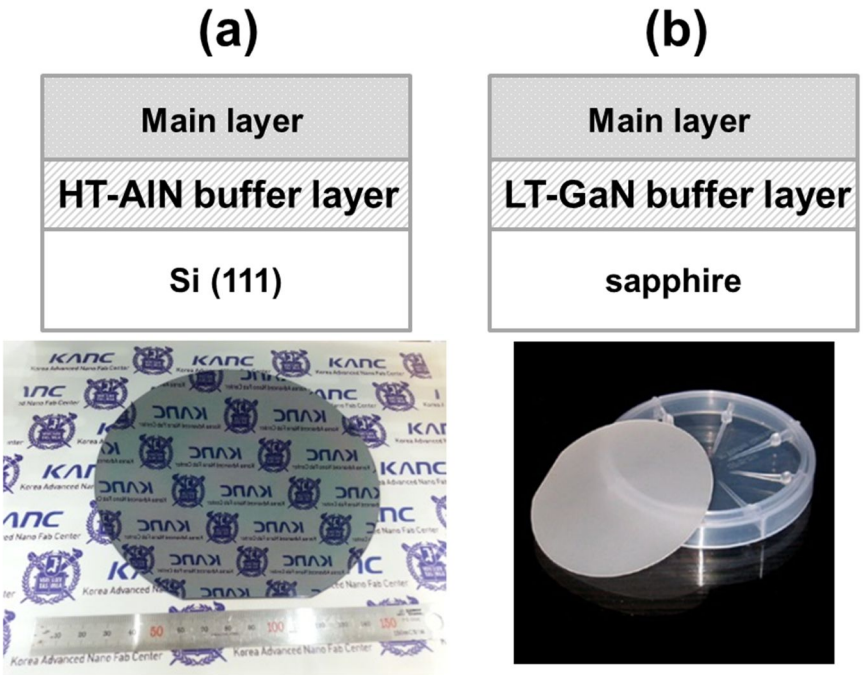

Figure 1.11 (a) Conventional structure of GaN on Si structure with HT AlN buffer layer and the picture of GaN on 6-inch Si substrate. (b) Conventional structure of GaN on sapphire structure with LT GaN buffer layer and the picture of GaN on 2-inch sapphire substrate.

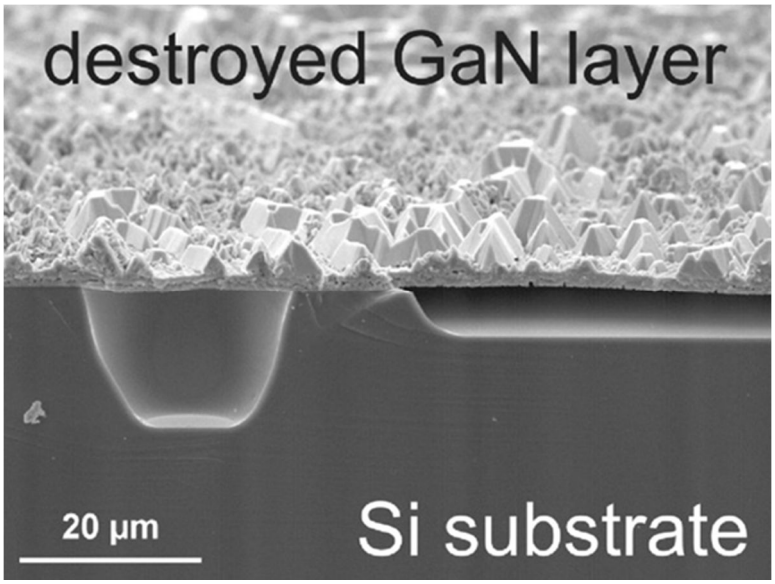

Figure 1.12 SEM image of GaN on Si after meltback etching has occurred. The GaN layer shows a rough surface and deep hollows in the Si substrate caused by the etching reaction visible.[34]

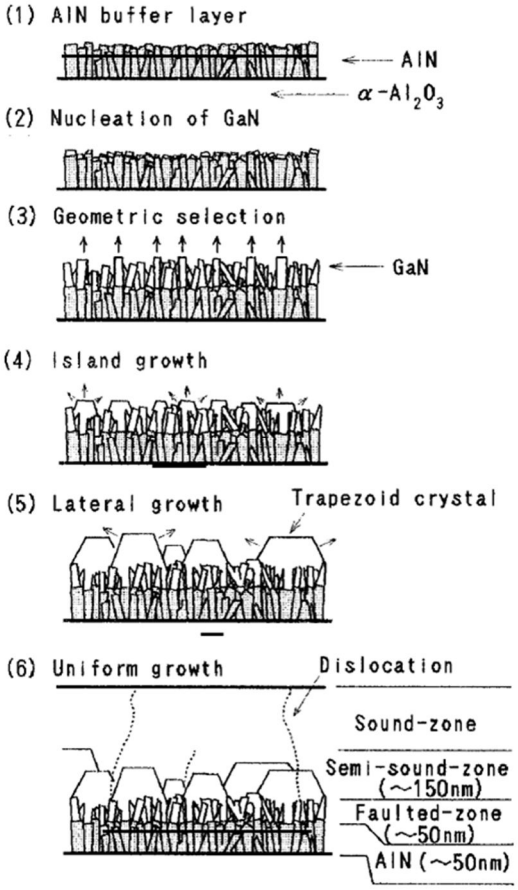

Figure 1.13 Schematic diagram of the growth process of GaN on the AlN buffer layer as the cross sectional view.[37]

1.5. The problems of the buffer layer for HEMT device

The epitaxial growth of wide-gap AlGaN semiconductors on a GaN buffer layer leads to a heterostructure with 2DEG at the interface. Therefore, the epitaxy techniques of buffer layer for growing III-nitride are very important in power electronic device such as HEMT. The issues about epitaxial growth of III-nitride for electronic device will be introduced.

1.5.1 Electrical problem

In the electronic device market, the breakdown voltage (or leakage current) is one of most important issue. The desirable scenario is that current from the source to drain during on-state flows in only 2DEG channel without any leakage current. However, there are several possible leakage paths related with buffer layer as shown in Figure 1.14.[39] First of all, the semi-insulating GaN buffer layer is mandatory to prevent the leakage path like Fig. 1.14(a). If the buffer layer is conductive due to undesirable background donor impurities,[40] the current can be partially flowed in the GaN buffer layer instead of 2DEG channel.[41] It result in a serious drawback in HEMT device. Various approaches have been investigated to obtain semi-insulating GaN layer by doping or generation of edge-type dislocation.

Figure 1.14(b) shows the vertical breakdown through the buffer, resulting from the interface between buffer layers and substrate. In case of HEMT device using Si substrate, AlN buffer layer is widely used as mentioned in previous chapter. Interestingly, it has recently been reported

that the AlN/Si interface is likely responsible for a strong decrease in the device breakdown voltage.[42] During growth of AlN buffer layers on Si substrate, the AlN is usually grown by MOCVD at high temperature, the Si atoms out-diffuse from the substrate into the growing layer, and Al atoms may diffuse into the Si substrate as well. Figure 1.15 shows the Auger electron spectroscopy (AES) atomic depth profiles of AlN grown on Si substrate at 1040 ^{o}C by MOCVD. The inter-diffusion of Al and Si are observed at the interface. The diffused Al into Si substrate would have role of p-type acceptor, resulting in leakage path as shown in Fig. 1.14(b).[43,44] Meanwhile, it is recently reported that sharp interface between AlN and Si is critical regardless of the interdiffusion.[45]

In case of HEMT device using sapphire substrate, LT GaN buffer layer is widely used as mentioned in previous chapter. It has been known that a thin degenerate layer responsible for serous n-type conductivity exists at the LT-GaN buffer/sapphire interface.[46] Figure 1.16 shows topography and current image taken under bias (-3 V) and current image taken under forward bias (+2.5 V) at the same position from scanning current-voltage microscopy from ref. 47. In the images, bright regions mean conducting region, i.e., with measurable current. Under reverse bias, the interfacial region is conductive, and under forward bias, the bulk film becomes conducting while the interfacial region remains slightly more conducting.[47] That's because, during the GaN growth on sapphire substrate, the substrate itself becomes a source of oxygen (O) through diffusion, resulting in a highly conducting channel at the LT-GaN buffer layer region.[48] The conducting LT buffer layer becomes the leakage path in the HEMT device as shown in Fig. 1.14(b). We could notice that the interfaces between AlN buffer layer and Si substrate and

between LT GaN buffer layer and sapphire substrate are important in the applications of electrical device.

1.5.2 Stress problem

The III-nitride has inherent problems associated with heteroepitaxy since free standing GaN substrate is not economically available, but the GaN layers grown on Si and sapphire substrates are highly strained because of the differences in lattice constants and thermal expansion coefficient as listed in Table 1.2.[49-52] Owing to the large difference between GaN or AlN growth temperatures of approximately 1000 ^{o}C by MOCVD and room temperature (RT), strong strain is applied to the III-nitride, which causes significant wafer bowing. In case of Si substrate, less thermal expansion coefficient of Si than III-nitride causes tensile stress to the III-nitride films during the temperature ramp down, resulting in serious crack problem. The III-nitride films on sapphire substrate are in compression after the growth process. In addition to the stress from thermal expansion coefficient, growth or intrinsic stresses are also present in the layer deposited on all hetero-substrate.[53-54] In recent years, owing to the rapid expansion of III-nitride industry, demands for cost reduction through enhancement of growth/fabrication techniques and manufacturing efficiency by scale-up of wafer size have been rapidly rising.[54-55] However, scale-up of the wafer size is expected to further increase wafer bowing.[56] This wafer bowing problem, leads to non-uniform wafer temperature distribution that deteriorates the uniformity of device properties. Furthermore, excessive bowing results in difficulties with subsequent device

processing, especially in regards to achieving an adequate yield.[57]

To solve the problems, many studies have been investigated until now. In case of Si substrate, AlGaN intermediate layers, LT AlN or AlGaN/GaN superlattices have been used to introduce sufficient compressive stress into the epilayer during the growth.[58] Figure 1.17 shows the LT AlN interlayer gives a compressive stress, resulting in the unstrained full layer. The method requires no complex external preparation steps, but it is not sufficient to solve the stress problems due to the lots of variables and unstable properties of Si substrate. In case of sapphire substrate, there are no methods to use III-nitride like GaN on Si substrate due to nonexistence of suitable layer to give tensile stress to compensate for the compressive stress in GaN on sapphire. Therefore, many different methods such as inserting a void structure have been investigated, but the methods require complex external preparation steps.[59-60]

1.5.3 Dislocation problem

Due to the lattice mismatch between III-nitride and substrate, high density of dislocation is generated. To fabricate high-efficiency LEDs, achieving of low threading dislocation density (TDD) is needed. However, for the fabrication of AlGaN/GaN HEMTs, it is still an open question as to whether low/ultralow TDD GaN layer are desirable.[45] In the application, it is important to reduce the leakage current as much as possible, so low conductivity is desirable. The some dislocation acts as an acceptor and scattering centers, resulting in lower buffer conductivity.[61] The 2DEG

mobility values of 2000 cm^2/VS, which are close to the theoretical limit, have been reported with a sheet carrier concentration of approximately $1x10^{13}$ cm^{-2}, in despite of a high TDD ranging from 10^9 to 10^{10} cm^{-2}.[45,62-63] Low TDD, of course, would be important for improvement of performance, reproducibility and reliability, but the growth of high resistive nitride buffer layer have to be focused prior to the obtaining of low TDD in case of electronic device.

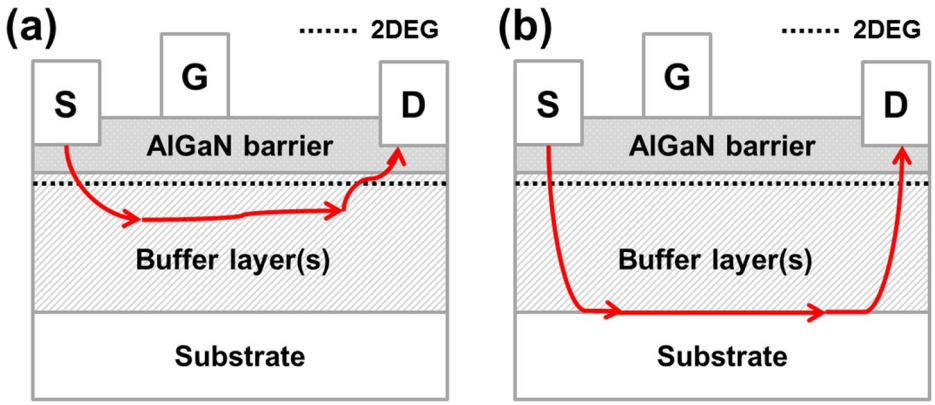

Figure 1.14 The possible leakage current path through (a) buffer layer and (b) interface between buffer layer and substrate in HEMT structure

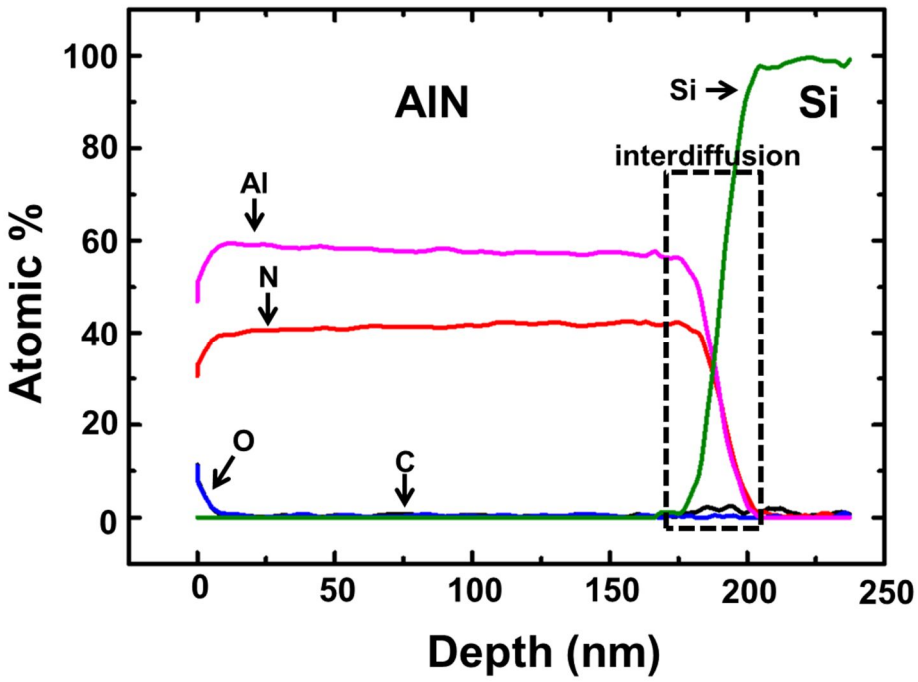

Figure 1.15 The AES atomic depth profiles of AlN grown on Si substrate at 1040 ^{o}C by MOCVD.

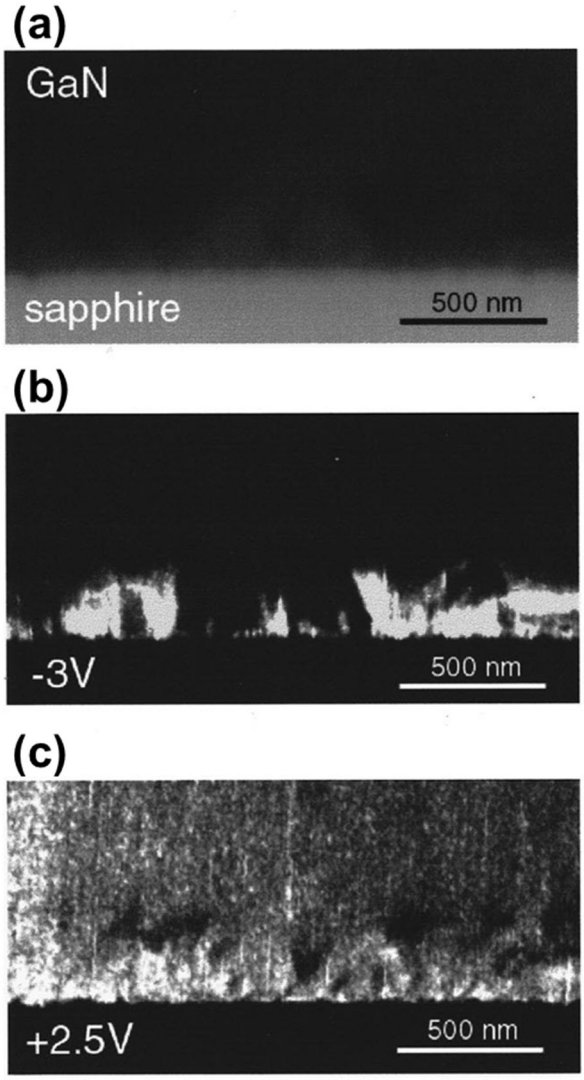

Figure 1.16 (a) Topography and (b) current image taken under bias (-3 V) and (c) current image taken under forward bias (+2.5 V) at the same position from scanning current-voltage microscopy.[47]

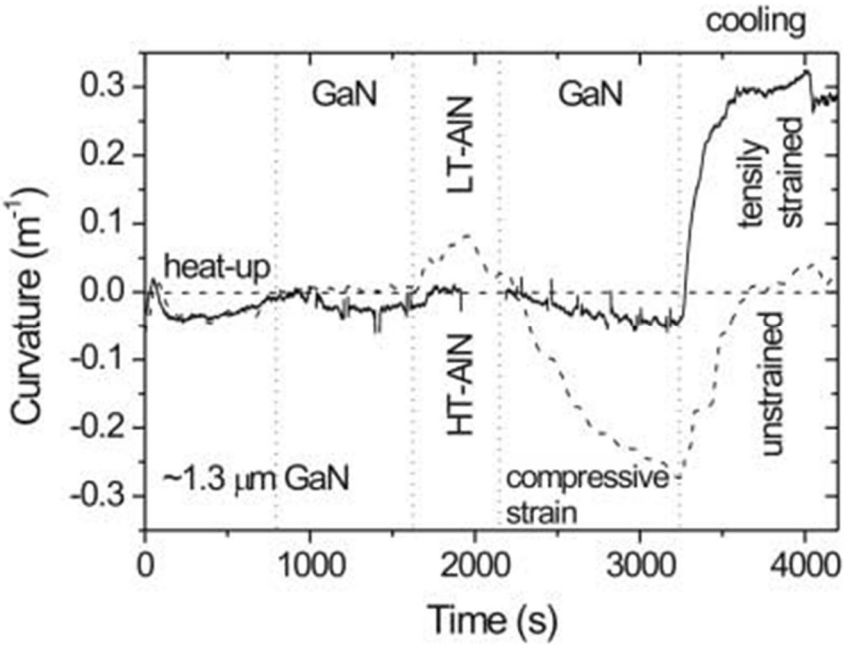

Figure 1.17 In-situ curvature measurement of two identically thick GaN on Si samples containing a high- or a low-temperature AlN interlayer.[58]

1.6. Thesis contents and organization

This thesis is composed of experimental results and discussions about the research for buffer layer of GaN on Si and GaN on sapphire. As we discussed above, buffer layer is critical for the properties of GaN layer. However, several problems such as leakage current, wafer bowing and MOCVD chamber condition still exist, resulting in the degraded properties of electronic device. To overcome these problems, new LT buffer layers for each substrate were proposed in this study. It contains two big parts as per subjects of research about new buffer layers for the Si and sapphire substrate for using III-nitride device, in parallel.

1. In case of GaN on Si, first of all, we investigated the problems of GaN on Si substrates when GaN was grown by MOCVD system. We confirmed that the AlN buffer layer on Si have been affected by Ga memory effect. The Ga effect determines the final stress, electrical properties and crystal quality of GaN on Si. To solve the Ga memory effect for AlN buffer layer, we proposed new AlN buffer layer, room temperature AlN layer by DC magnetron sputtering, for GaN on Si structure. The ex-situ buffer layer grown by the sputtering system could be effective solution to avoid growth circumstance problem which is Ga memory effect. Moreover low growth temperature could reduce the interdiffusion problem between AlN and Si substrate. The room temperature AlN buffer layer would be reported in this thesis.

2. There are several problems about GaN on sapphire as electronic

device. The GaN grown on sapphire shows n-type conductivity due to the degenerate layer near the conventional LT GaN buffer layer. Also, compressive stress is applied to the GaN on sapphire substrate, resulting in wafer bowing. To solve these problems, we developed new buffer layer, nano-columnar LT buffer layer, for GaN on sapphire substrate. We confirmed the buffer layer induced tensile stress with elimination of degenerate layer. Also, HEMT device was fabricated with the new buffer layer. The LT GaN buffer layer would be explained in this thesis.

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Chapter 2. The problem of GaN on Si grown by MOCVD – Investigation of Ga memory effect

2.1. Introduction

III-nitride semiconductors have attracted much research interest due to their wide applications in light emitting devices and power devices.[1,2] For the growth of III-nitride, various substrates such as Si, sapphire, and silicon carbide have been used. In recent years, owing to the rapid expansion of the III-nitride industry, demands for cost reduction through enhancement of growth techniques and manufacturing efficiency by scale-up of wafer size have been rapidly rising. Si substrates have been investigated for a long time due to strong advantages of low cost, availability of large wafer size and applicability of well-established processes for Si electronics.[3-5] However, the large mismatch of thermal expansion coefficient (TEC) (56%) and the lattice parameter (17 %) mismatches between GaN and Si, leading to a formation of cracks and high dislocation density, have hindered the direct growth of GaN on Si substrate.[6] Also, the strong chemical reaction between Gallium (Ga) and Si, called a meltback etching, occurs at a high temperature, resulting in the deterioration of the GaN and Si substrate.[7] In order to solve these problems, AlN layer has been widely used as a buffer layer prior to the growth of GaN.[8] A good coverage of AlN on Si substrate can not only serve as an good nucleation site for the growth of GaN layer, but also prevent an interdiffusion of Ga and Si.[9] Moreover, GaN grown on the AlN layer could be under compressive stress due to the larger in-plane lattice parameter of

GaN than that of AlN, resulting in the reduction of tensile stress in the film from the mismatch of TEC between GaN and Si substrate. [10]

The AlN buffer layer for GaN on Si is commonly grown in the same MOCVD system, which is normally used deposition method for III-nitride, for the GaN growth. I-H Lee et al. reported that when the MOCVD reactor wall is coated with the GaN after the growth of GaN/AlN/Si, the harmful Ga-containing droplets were formed on the AlN buffer layer for the subsequent growth, leading to deteriorated surface morphology of the films.[11] This implies that the reactor circumstance of MOCVD could affect the growth of nitrides and resultantly their characteristics, but little has been known for this issue. In this chapter, we have investigated specially the effect of Ga remaining in the MOCVD reactor, which we call a Ga memory effect, on the growth of GaN on Si substrates and its crystal quality.

2.2. Experimental procedure

AlN layers of 200 nm thickness were grown on a 2-inch Si (111) substrate by a Thomas Swan 6x2" close-coupled showerhead MOCVD reactor. Trimethylgallium (TMGa), trimethylaluminuam (TMAl) and ammonia were used as precursors for Ga, aluminum (Al) and nitrogen, respectively. After a native oxide layer on Si was removed by thermal annealing at 1100 ^{o}C for 5 min under a hydrogen (H_2) gas flow, an Al pre-seeding process was conducted at 1040 ^{o}C for 10 prior to the AlN growth. For the AlN growth, the temperature and the reactor pressure were 1040 ^{o}C and 38 torr, respectively. All the AlN samples were grown under the same conditions but at different run sequences after the previous GaN growth. Four batches of the AlN growth on Si were carried out and they were identified as sample A to D from the first run to the last one, as shown in Table 2.1. The baking is a thermal annealing process under a H_2 gas for 90 min to clean the chamber.

Four AlN/Si samples, one from each batch run, were loaded into the MOCVD chamber at the same time, and 700 nm thickness GaN layers were grown on them. The GaN growth temperature was 1040 ^{o}C and the reactor pressure was 76 Torr. These GaN/AlN/Si samples were identified as GaN on sample A to D. The GaN surfaces were mirror-smooth without peculiar features such as pits.

The structural characteristics of the samples were investigated using a Hitachi S-4800 field emission scanning electron microscope (SEM) and a JEOL JEM-2100F transmission electron microscope (TEM). The cross-sectional TEM samples were prepared by focused ion beam (FIB) using a

FEI Quanta 3D FIB machine with carbon coating. The magnitude of wafer bowing was estimated by an optical method using a Frontier Semiconductor FSM 500 TC. The crystalline quality of the GaN layers was analyzed by X-ray diffraction (XRD) using a PANalytical X'pert Pro X-ray diffractometer. The surface morphologies were measured using a Park Systems XE-100 atomic force microscopy (AFM). The quantitative analysis of elements in the samples was conducted using X-ray fluorescence (XRF) spectrometer (shimadzu XRF-1700).

Table 2.1 The experimental growth sequences of samples.

Run order	**1**	**2**	**3**	**4**	**5**
Growth procedure	GaN growth	Baking	AlN growth **(Sample A)**	Baking	AlN growth **(Sample B)**

Run order	**6**	**7**	**8**	**9**
Growth procedure	Baking	AlN growth **(Sample C)**	Baking	AlN growth **(Sample D)**

2.3. The effect of AlN run sequence for GaN on Si substrate

All the samples A to D showed a similar radius of curvature in the range from 18 to 19 m in a concave type, indicating they were under tensile stress. This implies that the wafer bow of the samples was independent of the run sequence of the AlN growth. On the other hands, the GaN layers grown on the AlN/Si samples, GaN on sample A to D, exhibited a remarkable difference of the radius of curvature (left, square) and the corresponding stress in the GaN layer (right, dot), as shown in Fig. 2.1. Using the radius of curvature, the stresses within the layer were estimated by the Stony's equation[12] with the reported elastic constants.[13] It was found that the radius of curvature increased from 6.7 for GaN on sample A to 11.1 m for GaN on sample D. Thus, the tensile stress decreased from 1260 for GaN on sample A to 759 MPa for GaN on sample D. Considering all the AlN/Si samples have the similar stress and the GaN layers were of the same thickness, we speculate that the stress in the GaN layers was reduced when they were grown on AlN/Si samples deposited at the latter run sequence.

Figure 2.2 shows plan view SEM images of the samples A to D. Pits were observed on the AlN surface for all the samples and they were revealed in a V-shape, as shown in the inset of Fig. 2.2(a), a cross-sectional TEM image. It was clear that the pit density was reduced from sample A to D. indicating its strong dependence on the run sequence of the AlN growth. Also, in AFM measurement, the root mean square (RMS) values, as shown in Fig. 2.3, show the improved surface roughness as the AlN is grown latter from the previous GaN growth run. Since the GaN layers were grown on the AlN/Si samples in a same batch, we expect that the different pit density could affect

the stress in the GaN layers.

To investigate the GaN growth mechanism on the AlN surface at the initial stage, GaN lyaers were grown during 15 s and 30 s on the sample A, which was expected to reveal the initial stage of the GaN growth. Figure 2.4(a)-(d) show plan-view SEM images of the GaN surface grown on the sample A to D, respectively. We confirmed that initial growth behaviors of GaN were quite different with the morphology of AlN samples as shown in Fig. 2.4. The tendency of rapid lateral growth behavior was observed in case of AlN layer with lots of pits, but slow coalescence of GaN was found in AlN layer with few pits in despite of same growth time of GaN as shown in Fig. 2.5, the cross sectional SEM images of GaN on sample A to D for 15 s and 30 s.

Figure 2.6 shows the cross-sectional scanning TEM images of the GaN film grown for 15 s and 30 s on the sample A and D. The particle-like objects on the GaN layer was a compound of GaN and carbon coating layer formed during the sample preparation by FIB. The GaN layer and the AlN layer could be distinguished in the images by contrast difference. It is shown that in Fig. 2.6(a), GaN was nucleated inside the pits, indicated by the red arrows, but not on the AlN flat surface. For the sample grown for 30 s on the sample A, the GaN was observed to fill up the pits and form a continuous film on the AlN surface, shown in Fig. 2.6(b). In case of sample D, GaN was also nucleated inside the pits preferentially (Fig. 2.6(c)), and then the GaN was grwon laterally having started at the center of the pit, but not continuous film (Fig. 2.6(d)) This could indicate that during the initial stage of the growth GaN nucleated at the pits of the AlN surface preferentially and after filling up them, GaN layer grew laterally on the AlN flat surface.

Based on our observations, a schematic diagram for the initial growth behaviors of GaN on sample A and D is derived in Fig. 2.7. The sample A, which contains lots of pits, has many nucleation sites for GaN nuclei. Therefore, at initial GaN growth, sample A would consist of many GaN nuclei at each pit. As GaN growth time is increased, the GaN nuclei become large size and would be coalesced with each GaN islands. The coalescence of GaN islands would be completed in a short time due to high density of GaN nuclei in sample A. On the other hand, the number of nucleation site for GaN in sample D, contains few pits, is limited compared to the other samples. Therefore few GaN nuclei would become large size, so would be taken a long time to complete the coalescence in sample D.

It has been reported that when crystal islands are coalesced, a significant biaxial tensile stress is generated at grain boundaries[14,15] and several papers showed experimentally that tensile stress was built up in the GaN film due to the coalescence of the islands.[16,17] The detailed explanation was introduced in Chap. 1.2.2. According to these reports, in case of lots of islands with small size, high density of coalesced island (i.e. high density of grain boundaries of islands) is formed, resulting in strong tensile stress in the film.[18] When GaN islands are coalesced on the sample A, high density of coalesced island would generate strong tensile stress. On the other hands, relatively small tensile stress would be generated in sample D due to low density of coalesced island, resulting from few GaN islands, shown in Fig. 2.7.

In fact, the stresses in the GaN on samples caused by mismatch of lattice constant and thermal expansion coefficient would be same, since all samples have same structure and thickness. Therefore, it could explain the result of Fig. 2.1 that the tensile stress was reduced from the sample A, including more

grain boundary due to higher pit density, to the sample D, including less grain boundary due to smaller pit density. Combining the previous results, we speculate that the difference in the stress in GaN on samples A to D, shown in Fig. 2.1, could be attributed to the different pit density on the AlN surface, shown in Fig. 2.2.

XRD measurement was carried out for the GaN layers on AlN/Si substrates, and their full widths at half maximum (FWHM) were plotted in Fig. 2.8. It is also observed that XRD FWHM values of GaN (0002) and $(10\bar{1}2)$ reflection decreased with the number of AlN, for overgrowth of GaN layer, growth run, which is same with the tendency of stress of GaN on samples in Fig. 2.1. The differences in the XRD results could be attributed partially to the existence of grain boundary.[19,20] According to our observation, GaN island density at initial growth is varied with samples due to the different AlN pit densities, so the FWHM results of GaN on samples could be partially influenced by it. Thus, decrease of XRD FWHM values of GaN (0002) and $(10\bar{1}2)$ reflection is also observed from GaN on sample A to GaN on sample D. The results demonstrate the order of run sequence of AlN growth affects not only stress of GaN on Si substrate but crystal quality of the GaN.

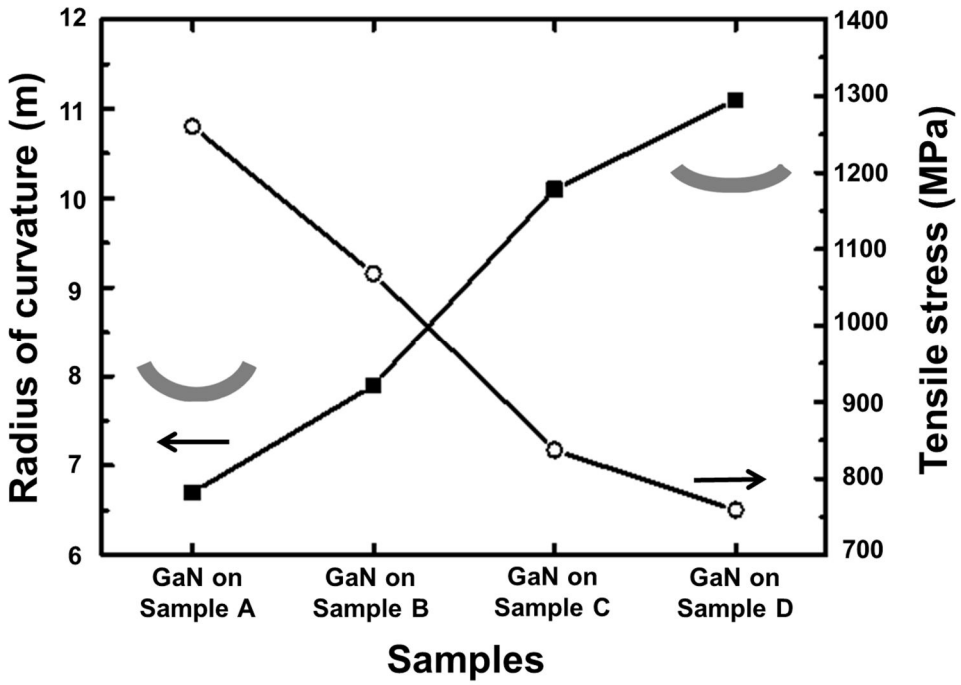

Figure 2.1 The radius of curvature (left axis) and tensile stress (right axis) in the GaN on samples.

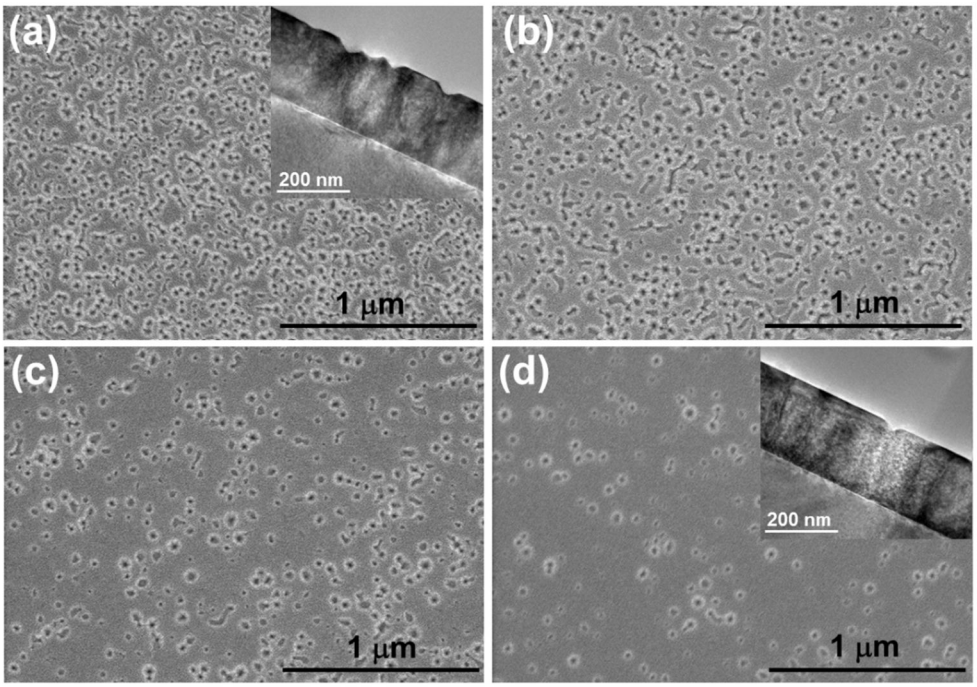

Figure 2.2 Plan-view SEM images of (a) sample A, (b) sample B, (c) sample C and (d) sample D. Inset: cross-sectional TEM images of the (a) sample A and (d) sample D.

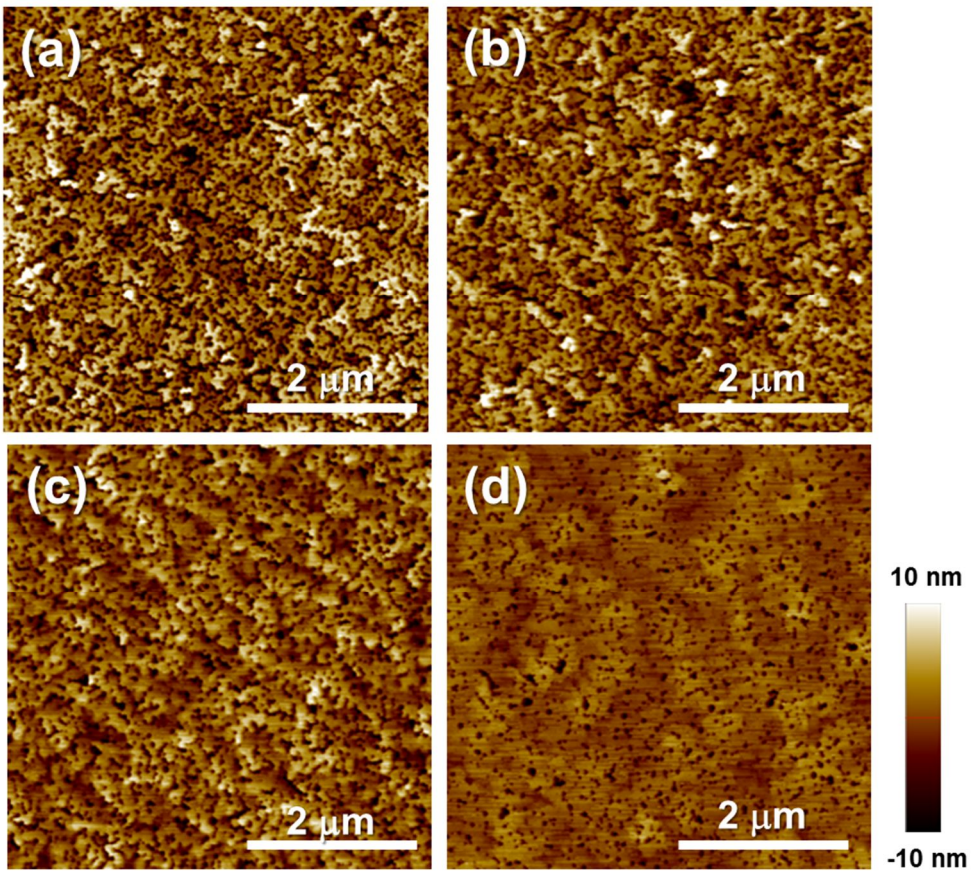

Figure 2.3 5 x 5 μm^2 topological AFM images of (a) sample A, (b) sample B, (c) sample C and (d) sample D. The RMS roughness of the samples are 4.61 (sample A), 3.93 (sample B), 3.39 (sample C) and 2.06 (sample D) nm, respectively.

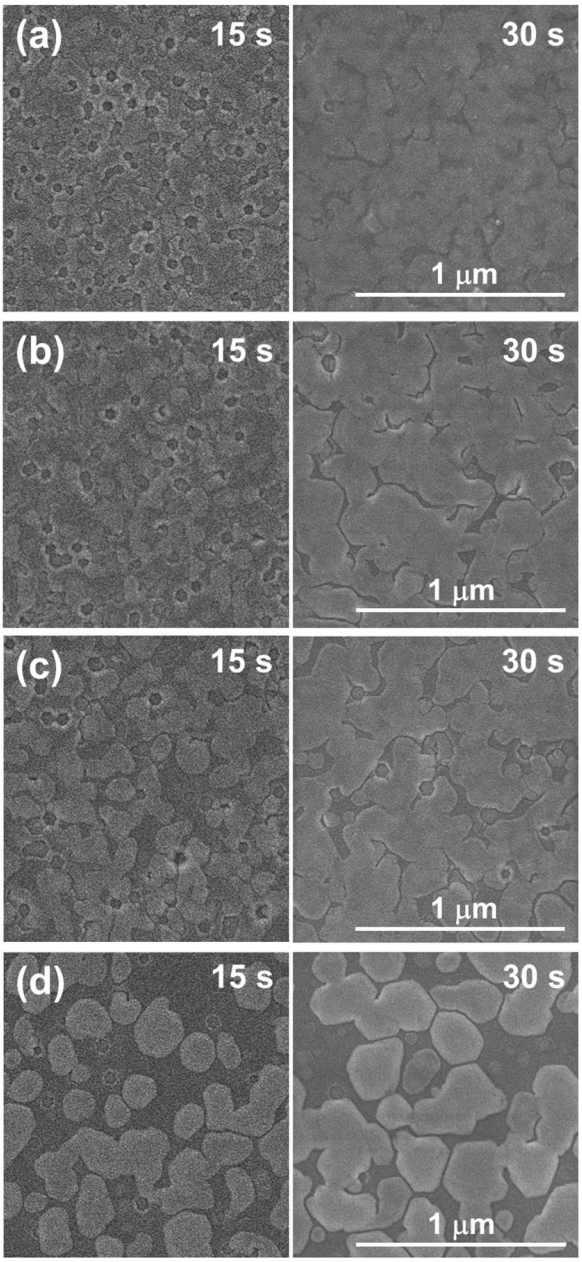

Figure 2.4 Plan-view SEM images of 15 s and 30 s GaN on (a) sample A, (b) sample B, (c) sample C and (d) sample D.

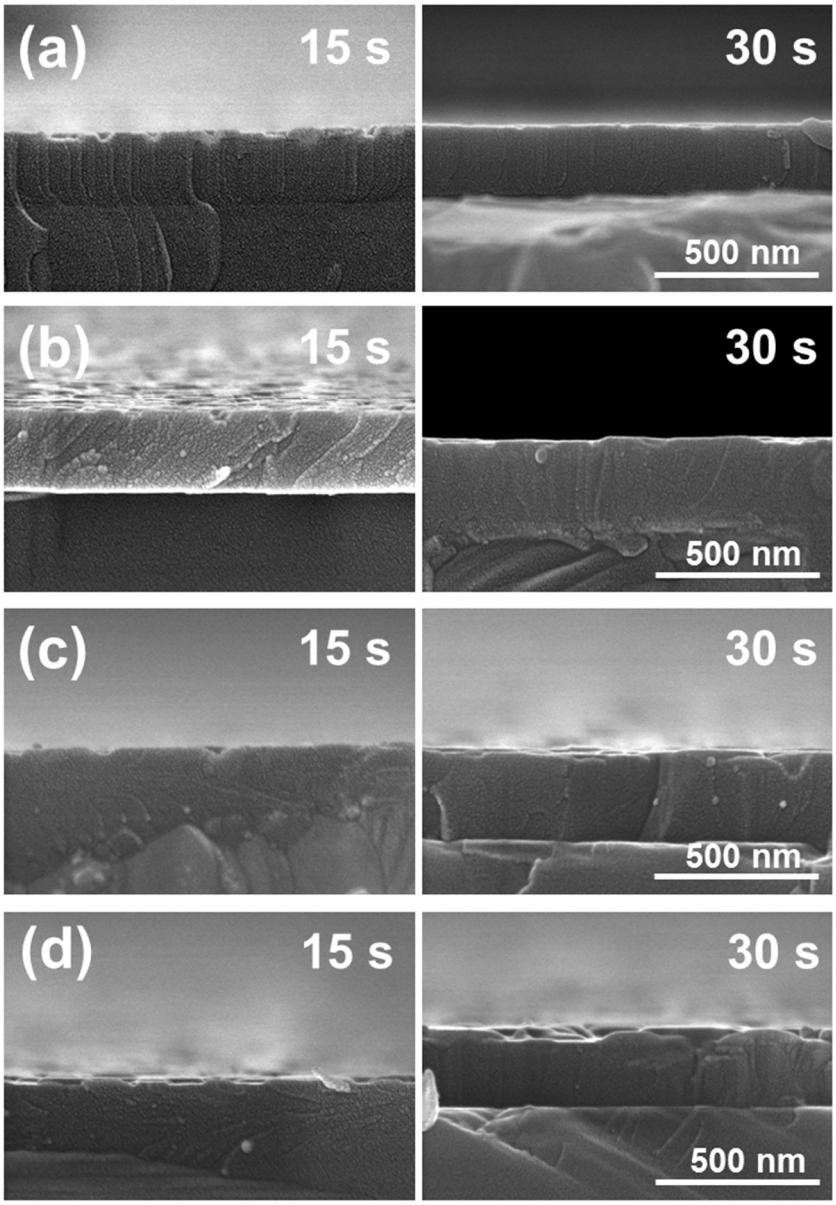

Figure 2.5 Cross-sectional SEM images of 15 s and 30 s GaN on (a) sample A, (b) sample B, (c) sample C and (d) sample D.

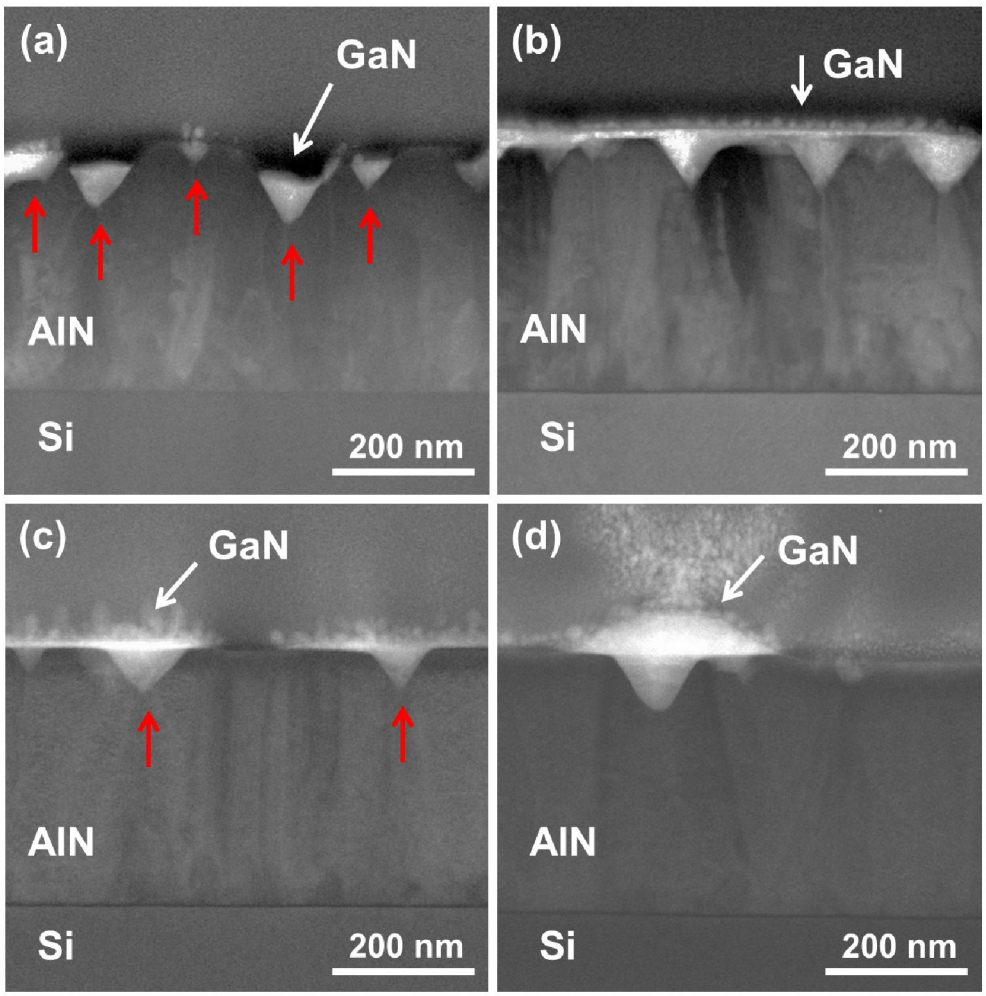

Figure 2.6 Cross-sectional scanning TEM images of (a) 15 s GaN and (b) 30 s GaN on sample A and (c) 15 s GaN and (d) 30 s GaN on sample D. The red arrows indicate pits of AlN layer.

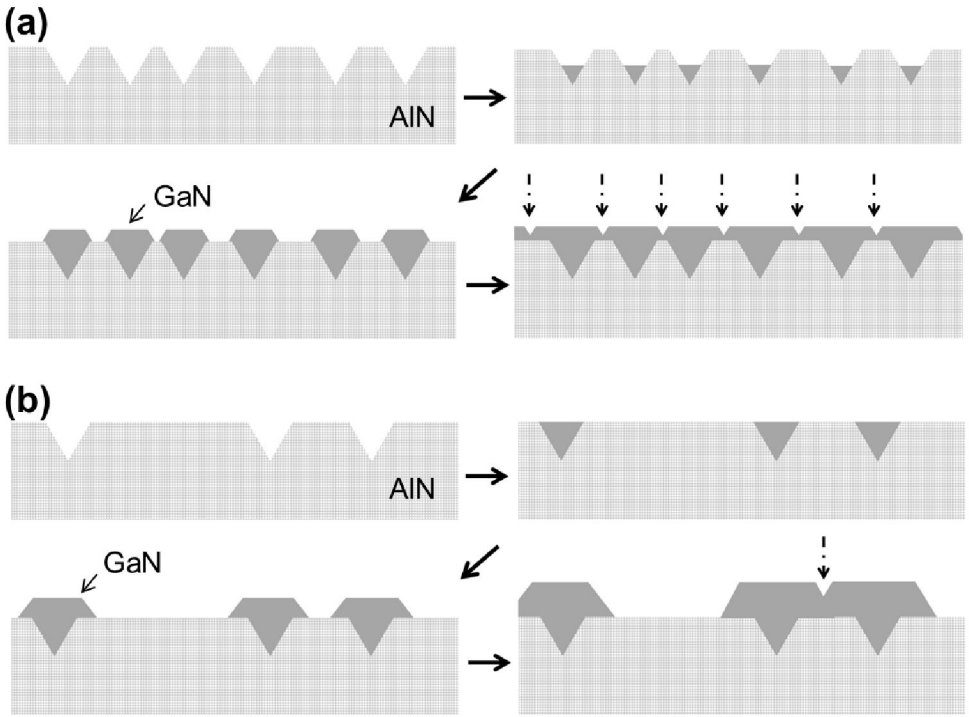

Figure 2.7 Schematic diagram showing the initial growth behavior of GaN on (a) sample A and (b) sample D. The dotted arrows indicate the grain boundaries formed when GaN islands are coalesced. i.e. the site generating tensile stress.

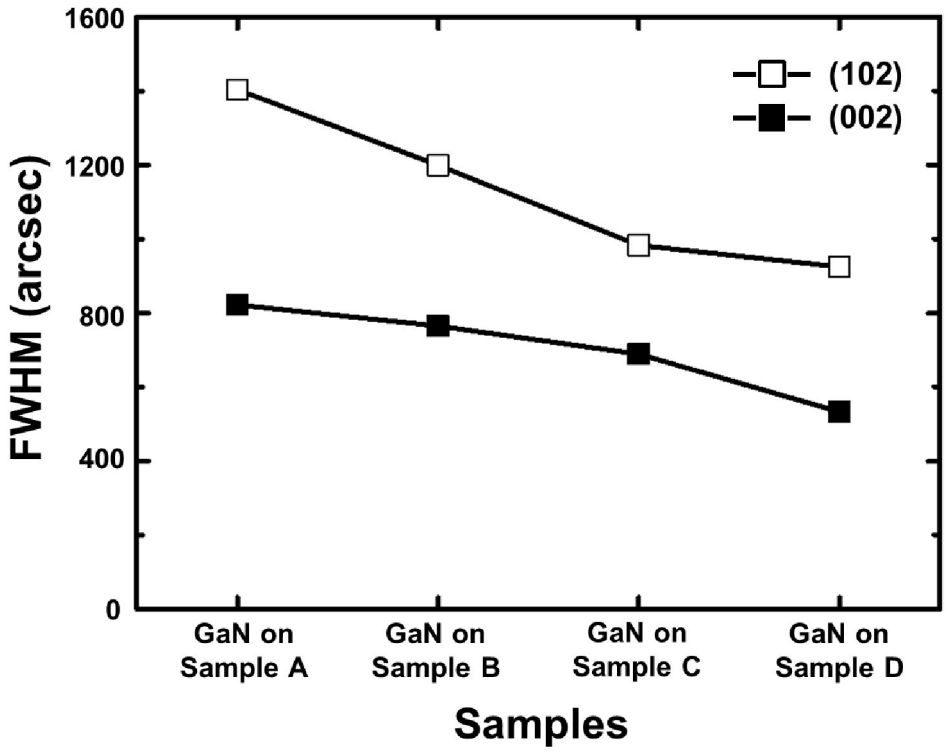

Figure 2.8 XRD FWHM values of (0002) and $(10\bar{1}2)$ reflection of GaN on samples.

2.4. Ga memory effect for AlN buffer layer on Si

According to our experiment the difference of samples is the run sequence following the previous GaN growth. We expect that in our system the reactor circumstance such as quartz liner or susceptor, coated by GaN in the previous run, could be a source for Ga incorporating into the films. In order to detect the Ga concentration in the AlN/Si samples A to D, XRF measurement, which is widely used for a quantitative analysis of elements in the detection range of few ppm, was conducted. They are shown in Fig. 2.9. Figure 2.9 showed that the Ga concentration decreased in the order of the run sequence of AlN growth from sample A to D. Moreover the Ga concentration in the AlN sample was reduced by about 50 % through the successive four runs of AlN growth. This implies that each baking and AlN growth run reduced the amount of remaining Ga in the reactor circumstance. However, small amount of Ga was still incorporated during AlN growth run, in despite of several runs, which showed Ga memory effect exists in the system. Considering the remaining Ga concentration is extremely small in the AlN film, we expect the Ga on the Si surface had significant impact on the formation of pits on the AlN surface.

To confirm the effect of the Ga incorporation on the growth of AlN layer on Si substrate, cross sectional structure of the samples A and D was analyzed by high resolution TEM (HR-TEM). In the TEM images of the AlN film, no noticeable difference in the lattice image and the diffraction pattern was detected for both samples. On the other hand, we confirmed that the interface between AlN and Si substrate was somewhat different for both samples. Figure 2.10 is bright field HR-TEM images showing an ambiguous

layer at the interface between AlN and Si. The presence of the ambiguous layer has been reported in several papers indicating it as SiN_x or the intermixing layer of Si, Al, N and C, but it's clear feature has not been understood until now.[21-24] It is worth noting that the thickness of the ambiguous layer for sample A is 2.5 nm but it is only a few monolayer for the sample D. This difference in the thickness of the ambiguous phase could be attributed to the different amount of the remaining Ga on Si surface.

In order to study the effect of the Ga incorporation on Si (111) surface, three samples (sample I, II and III) were prepared by thermal annealing under a H_2 gas flow at 1100 ^oC. The thermal annealing is a routine process preceded before the AlN growth to remove a native oxide on Si substrate. The sample I, II and III were annealed after twice, four times and ten times growth of AlN layer following the previous GaN growth, respectively. Therefore, we expect different amount of Ga on Si surface for the three samples. The result of XRF measurement, Table 2.2, revealed that the samples I and II included Ga concentration of 5 ppm and 3 ppm, respectively and no noticeable amount of Ga on the sample III. Figure 2.11 is AFM images showing the surface morphologies of the sample I, II and III. The sample III exhibited a well-defined surface steps, but the other two samples revealed degraded rough surfaces, worse one for the sample I including more amount of Ga on the surface. The RMS roughness values, as listed in Table 2.2, also show tendency the higher Ga concentration is incorporated in Si, the rougher surface morphology of the Si is observed.

According to the Ga-Si phase diagram as shown in Fig. 2.12, Ga forms an eutectic with Si even at extremely small amount of 5×10^{-8} at. % at 29.8 ^oC and exists as a mixed liquid in a broad range of temperature and

composition.[10,25-27] Therefore, in spite of the small amount of Ga on the Si surface, shown in Table 2.2, the Ga could form an eutectic with Si. The Ga-Si liquid at annealing temperature attributes to the formation of rough surface, as shown in Fig. 2.11(a) and (b), and we expect that the higher Ga concentration was responsible for the rougher surface morphology of the sample I.

Combining the results of Fig. 2.2 and 2.11, we could consider that rougher Si surface was responsible for higher density of the pits on the AlN surface. In fact, A.M. Sánchez et al. has reported the screw dislocations and the corresponding pits on the AlN surface strongly depends on surface step of Si substrate.[21,28] However, the formation mechanism of pits on the rough Si surface is unclear at present time. More work is under way to understand fundamentally how AlN is deposited on the rough Si surface, forming the pits. In conclusion, the incorporated Ga with the Si substrate during thermal annealing process determines the surface morphology of the substrate, resulting in the different pit densities on AlN layer.

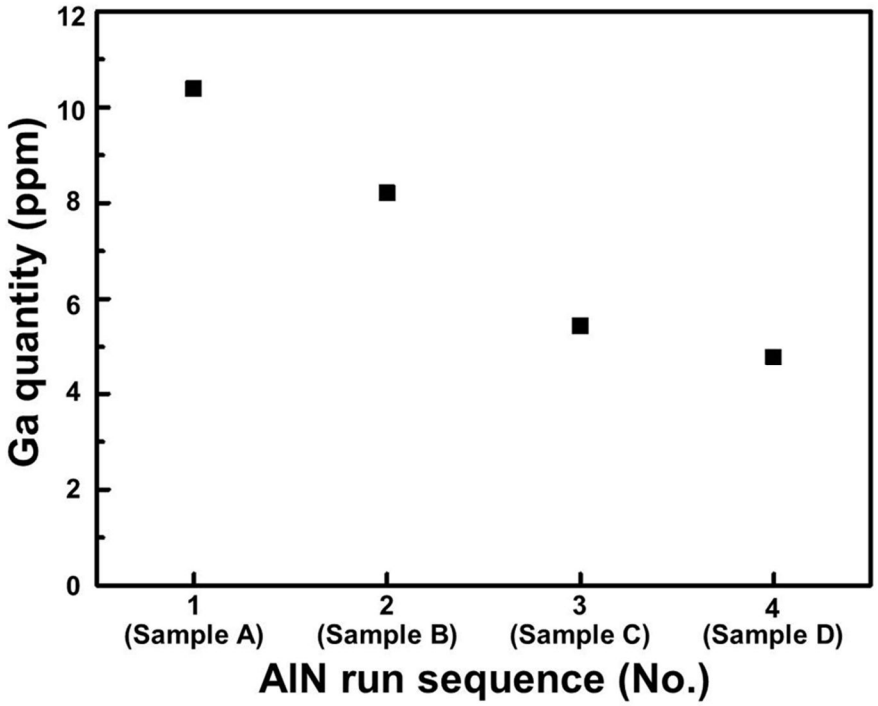

Figure 2.9 Ga concentration in the samples.

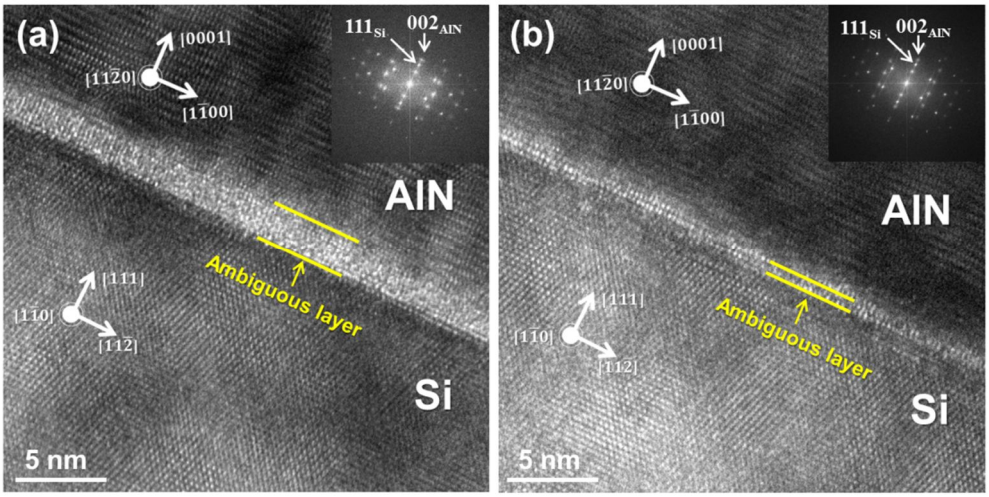

Figure 2.10 Cross-sectional high-resolution TEM images showing interface between AlN and Si of (a) sample A and (b) sample D. Inset: Fast Fourier transform images corresponding to the HRTEM.

Table 2.2 Summary of results in annealed Si substrate.

Sample	**XRF**	**AFM**
	Ga concentration (ppm)	RMS (nm)
I	5	1.105
II	3	0.825
III	0	0.333

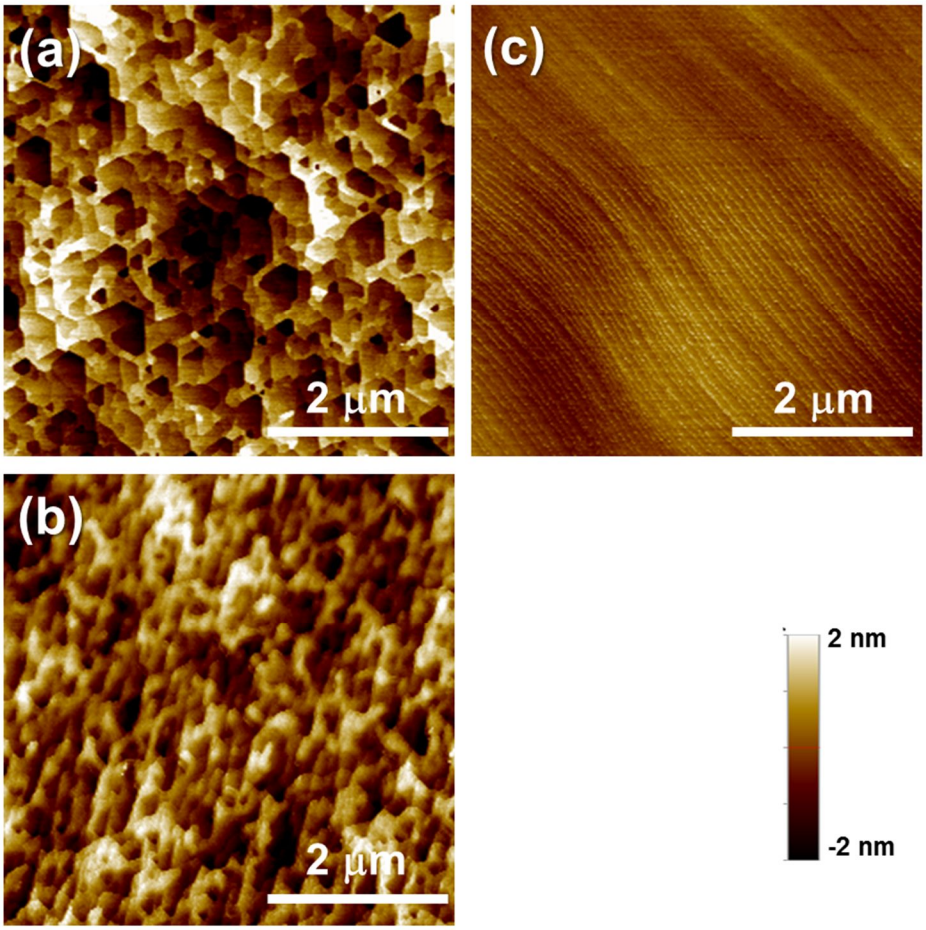

Figure 2.11 5 x 5 μm^2 topological AFM images of annealed Si (111) substrate of (a) sample I, (b) sample II and (c) sample III.

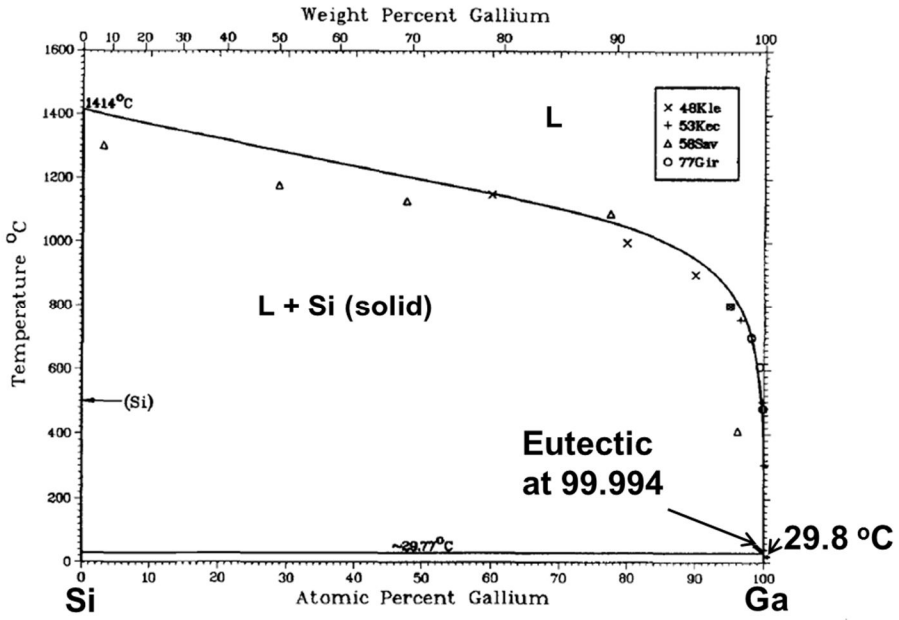

Figure 2.12 Si-Ga Phase diagram.[34]

2.5. Summary

In this chapter, we investigated Ga memory effect in GaN on Si substrate and verified remained Ga from previous GaN run affects properties of GaN on Si substrate. Our observations in the experiment are as follows. During thermal annealing process of Si substrate, small amount of Ga, from the MOCVD reactor, was incorporated in the Si substrate, resulting in rough surface. When AlN layer was grown, as a next step, on the Si substrate, the layer contained various densities of pits following the degree of rough surface in the Si substrate. Initial GaN nuclei densities were determined by the pit densities in AlN, because the pit in AlN layer had a role of nucleation site for GaN. Accordingly, the final stress and crystal quality of GaN was affected by densities of the pit in AlN buffer layer. In conclusion, small amount of Ga from the Ga memory effect affected the final stress and crystal quality of GaN on Si. Our results showed the GaN layer on Si was considerably sensitive to growth circumstance, so attention of the growth circumstance is needed. This observation may enable the improvement of crystal quality of GaN on Si and would provide the understanding of the growth mechanism in GaN on Si. Also, we conclude that the alternative of conventional buffer layer is needed to solve the problem.

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Chapter 3. Growth of AlN buffer layer on Si substrate by DC magnetron sputtering at room temperature

3.1. Growth of AlN buffer layer with same alignment of out-of-plane

3.1.1 Introduction

AlN has received much attention due to the wide direct band gap (6.2 eV), high thermal conductivity (~300 $WK^{-1}m^{-1}$) and high melting temperature (2200 ^{o}C).[1,2] Therefore, AlN have been investigated for applications in insulating ceramics, microelectronics and optoelectronics.[3,4] Especially, AlN is widely used as a buffer or intermediate layer for GaN on Si substrate.[5,6] A good coverage of AlN on Si substrate can not only serve as an good nucleation site for GaN layer, but also prevent an interdiffusion of Ga and Si, which causes meltback etching problem.[7] However epitaxial growth of AlN on Si is not easy due to the large lattice mismatch between AlN and Si (~19%).[8,9] The AlN epitaxial films on Si substrate have been grown by various techniques, such as MOCVD and molecular beam epitaxy (MBE). The techniques require the high temperature and cost[10,11] Especially when AlN is deposited by MOCVD, it was known that the quality of the AlN layer was degraded due to the incorporation of the remaining Ga in the reactor, as reported in chapter 2, which is particularly important for manufactures of nitride based devices due to the frequency of MOCVD maintenance and cycle time.[12]

On the other hands the magnetron sputtering system for AlN growth has attracted much research interest due to the simple and cost effective technique.[13,14] Moreover, growth temperature could be lowered even to room temperature by using the system**.** The magnetron sputtering system of the low growth temperature could be an alternative of conventional high temperature growth by MOCVD or MBE system due to prevention of interdiffusion between Si-Al.[15,16] Also, when the AlN layer grown by the sputtering system was used as a buffer layer for GaN on Si substrate, the ex-situ buffer layer could be effective solution to avoid growth circumstance problem in MOCVD reactor since the system does not include Ga. In the chapter, we investigate to grow AlN layer by DC magnetron sputtering system for buffer layer of GaN on Si substrate.

3.1.2 Experimental procedure

AlN thin films were deposited on a 2-inch Si (111) substrate using a DC magnetron sputtering system (KVT-T8896) with an Al target of 99.999% purity. The sputtering and reactive gases were high-purity Ar and N_2, respectively. Before loading Si (111) substrate into the sputter chamber, the native oxide on the Si wafer was removed by etching in a buffered oxide etchant (BOE) solution. The base pressure of the sputtering system was stabilized at 10^{-7} Torr before introducing the gas mixture. The target was pre-sputtered for 30 min to equilibrate and clean the target surface with the shutter closed. After the pre-sputtering, the 100-nm-thickness AlN thin film was deposited at room temperature. The sputtering variables were sputtering pressure, Ar/N_2 ratio and DC power. The detailed deposition parameters are listed in Table 3.1. The crystal structure and crystallinity were analyzed by XRD using a PANalytical X'pert Pro X-ray diffractometer. The structure characteristics of the samples were analyzed using a Hitachi S-4800 field emission SEM.

Table 3.1 The sputtering parameters in the experiment.

Target	Aluminum
Temperature	Room temperature
DC power	200 ~ 600 W
Pressure	1 ~ 5 mTorr
Ar : N_2	15 : 5 ~ 8 : 12 (sccm)
AlN thickness	~ 100 nm
Substrate	Si (111)

3.1.3 Results and discussion

Prior to the growth of AlN layer by sputtering, we had to confirm the problems of sputtered AlN layer for buffer layer of GaN on Si substrate. Figure 3.1 shows the XRD θ-2θ patterns of sputtered AlN layer and the GaN layer grown by MOCVD system on the sputtered AlN layer. The diffraction peaks at 28°, 36.1^{o}, and 37.9^{o} corresponding to Si (111), AlN (0002) and AlN ($10\bar{1}1$), respectively, were observed in sputtered AlN layer. Interestingly, GaN (0002), GaN ($10\bar{1}1$) and GaN ($10\bar{1}2$) peaks, which is corresponding with each AlN plane, were also observed in XRD θ-2θ patterns of the GaN layer. The results indicate that the orientation of growth planes of GaN is determined by the orientation of planes of AlN underlayer. In other word, only (0002) AlN layer is indispensable to grow (0002) GaN layer. Accordingly, the sputtering conditions related with preferred orientation were investigated. Figure 3.2 shows θ-2θ XRD patterns of the AlN films sputtered under varying pressures of 1-5 mTorr, at a constant DC power of 400 W, room temperature and flow rate of Ar (10 sccm) and N_2 (10 sccm) gas. The result showed the preferred orientation of the AlN films parallel to the plane of the substrate changed with the sputtering pressure. At 3 and 5 mTorr, only AlN ($10\bar{1}0$) plane was observed in Fig. 3.2., but AlN (0002) peaks did not appear in the XRD patterns. In the sputtering system, the sputtered materials are deposited and etched simultaneously, because the materials are exposed to the bombardment of atoms. It has been known that preferential orientation of sputtered AlN is related with the energy of arriving adatoms to the growing surface.[23,24] According to the periodic bond chain theory, in the wurtzite structure such as AlN, the ($10\bar{1}0$), (0001) and ($10\bar{1}1$) are stable

planes.[19] Under a sputtering condition of high energy arriving atoms, the crystals with loosely packed planes would suffer a higher etch rate than the crystals with closed-packed ones.[13] Therefore, as the bombardment becomes more energetic, microcrystals in the film tend to grow with the (0001) plane, the most close-packed plane among the stable planes, along the surface normal.[26]

From basic kinetic gas theory, the mean free path of the atoms in the gas phase could be expressed by pressure P as given by

$$\boldsymbol{\lambda_{mfp}} = \frac{\mathbf{5}\,[\boldsymbol{mTorr\ cm}]}{\boldsymbol{P}\,[\boldsymbol{mTorr}]} \qquad [3\text{-}1]$$

From eq. [3-1], as the sputtering pressure is decreased, the mean free path of the sputtered atoms is increased, so the energy loss of atoms by collisions in the gas phase before arriving at the growing surface become reduced. Hence, the arriving atoms under 1 mTorr become energetic to align with (0002) out-of-plane, as shown in Fig. 3.2. On the other hand only AlN $(10\bar{1}0)$ peak without AlN (0002) peak were observed under 3 and 5 mTorr due to reduced energy of the arriving atoms.

We varied the Ar/N_2 ratio, as listed in Table 3.2., under 3 and 1 mTorr, room temperature and a constant DC power of 400 W. However it was confirmed that Ar/N_2 ratio was not related with alignment of AlN crystal to (0002) out-of-plane. The results show Ar/N_2 ratio could not give high energy to arriving atoms, but only sputtering pressure is key factor to supply the high energy for adatoms.

The AlN films were sputtered under various DC power, at a constant pressure of 1 mTorr, room temperature and flow rate of Ar (10 sccm) and N_2

(10 sccm) gas. The θ-2θ XRD patterns of the AlN films were plotted in Fig. 3.3. All samples exhibits only (0002) peaks located at 36.1°, resulting from the sputtering pressure of 1 mTorr. The results showed sputtering pressure would be a major factor for the alignment of AlN crystal to (0002) out-of-plane. Although all samples exhibit AlN (0002) peak, the different intensities of the peaks are observed for each sample. The different intensities suggested that, in addition to the sputtering pressure, DC power were important to improve (0002) orientation of sputtered AlN.

The GaN layer was grown on the AlN layer sputtered under DC power of 600 W, pressure of 1 mTorr, room temperature and flow rate of Ar (10 sccm) and N_2 (10 sccm) gas. The GaN was grown at 1040 °C and 38 Torr using TMGa and ammonia by MOCVD. During the temperature ramping-up to growth temperature, ammonia gas was flowed in order to prevent the decomposition of the AlN layer. Figure 3.4(a) shows the θ-2θ XRD patterns of the GaN sample. Only GaN (0002) and AlN (0002) peaks were observed thanks to the preferred orientation of the sputtered AlN layer. On the other hands, 2 dimensional GaN was not observed in the sample as shown in Fig. 3.4(c). At some of the coalescence boundaries, differently oriented GaN crystallites are visible with random angles. Because of the randomly oriented GaN islands, any peaks were not obtained in XRD ϕ-scan data (Fig. 3.4(b)), though GaN (0002) peak was observed in Fig. 3.4(a).

To verify the reason why GaN was grown with 3 dimensional islands, XRD ϕ-scan was measured for the AlN layer. Figure 3.5 shows XRD θ-2θ and ϕ patterns of the AlN layer. No peaks were observed in XRD ϕ-scan data, though the clear AlN (0002) peak was observed. The result shows that, in case of the AlN layer, each AlN columns is aligned to the (0002) orientation

along the surface normal, but the columns are aligned randomly to the in-plane orientation as shown in Fig. 3.6(a). That means the sputtered AlN is poly-crystalline, not single crystalline structure. Because the growth of GaN is determined by the orientaion of AlN underlayer, the GaN exhibits poly-crystalline properties, too. Therefore, to use the sputtered AlN for buffer layer of GaN on Si substrate, obtaining of single crystalline sputtered AlN layer, that is same out-of-plane and in-plane alignment, is important like the schematic diagram in Fig. 3.6(b).

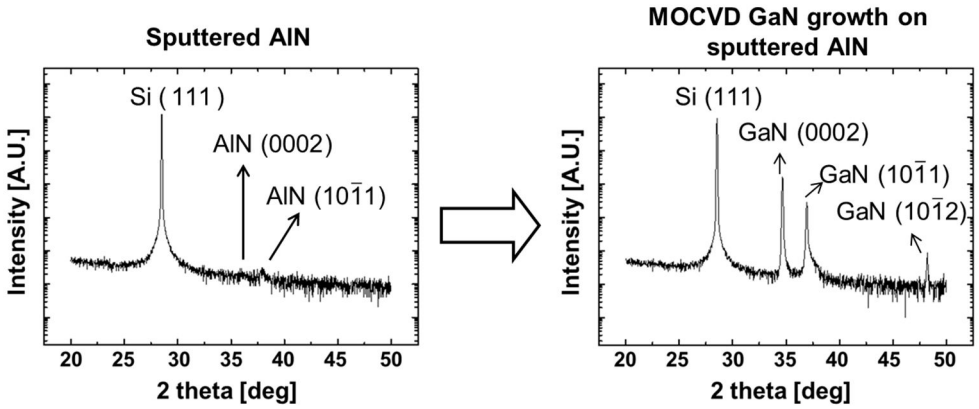


Figure 3.1 XRD θ-2θ patterns of sputtered AlN layer and the GaN layer grown by MOCVD system on the sputtered AlN layer.

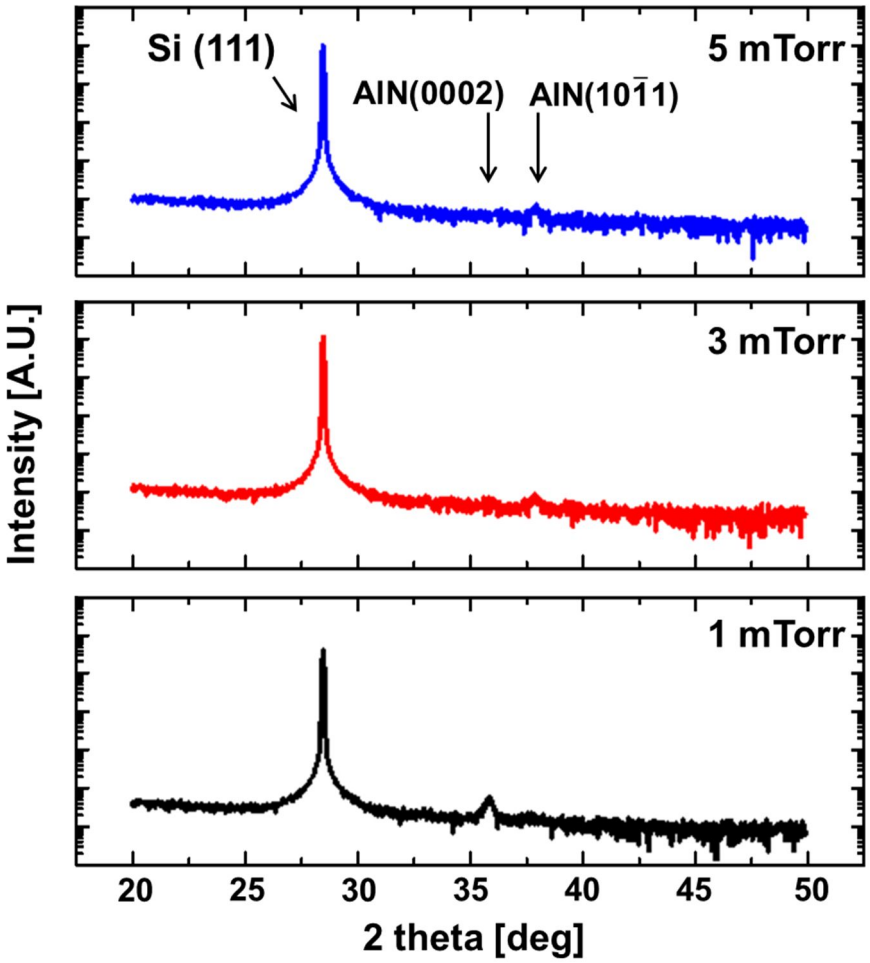


Figure 3.2 XRD θ-2θ patterns of the AlN films sputtered under varying pressures of 1-5 mTorr, at a constant DC power of 400 W, room temperature and flow rate of Ar (10 sccm) and N_2 (10 sccm) gas.

Table 3.2 The (0002) AlN peak results according to the Ar : N_2 ratio.

Ar : N2 (sccm)	Pressure (mTorr)	DC power	(0002) AlN peak
10 : 10	3	400 W	**X**
12 : 8	3	400 W	**X**
8: 12	3	400 W	**X**
10 : 10	1	400 W	**O**
15 : 5	1	400 W	**O**

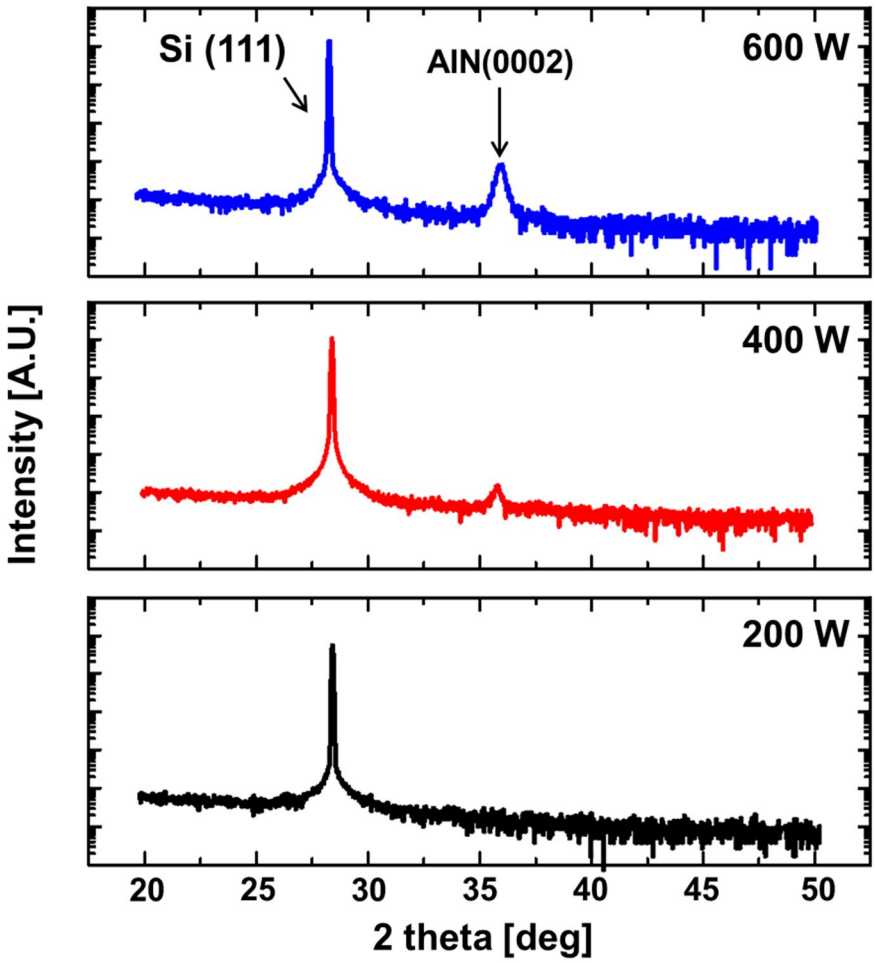


Figure 3.3 XRD θ-2θ patterns of the AlN films sputtered under various DC power, at a constant pressure of 1 mTorr, room temperature and flow rate of Ar (10 sccm) and N_2 (10 sccm) gas.

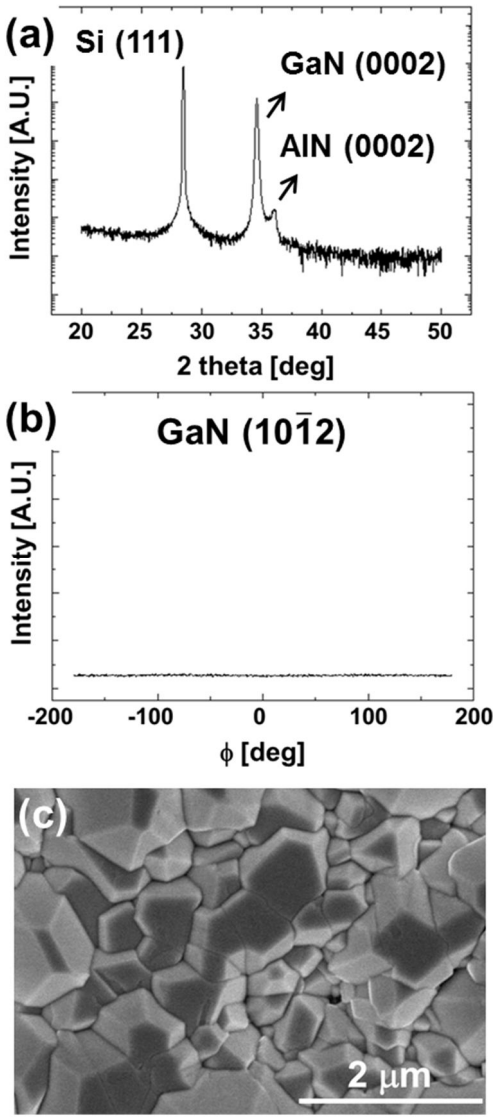


Figure 3.4 (a) XRD θ-2θ patterns, (b) XRD ϕ-scans for the $(10\bar{1}2)_{GaN}$ and (c) plan-view SEM image of the GaN grown on AlN layer sputtered under DC power of 600 W, pressure of 1 mTorr, room temperature and flow rate of Ar (10 sccm) and N_2 (10 sccm) gas.

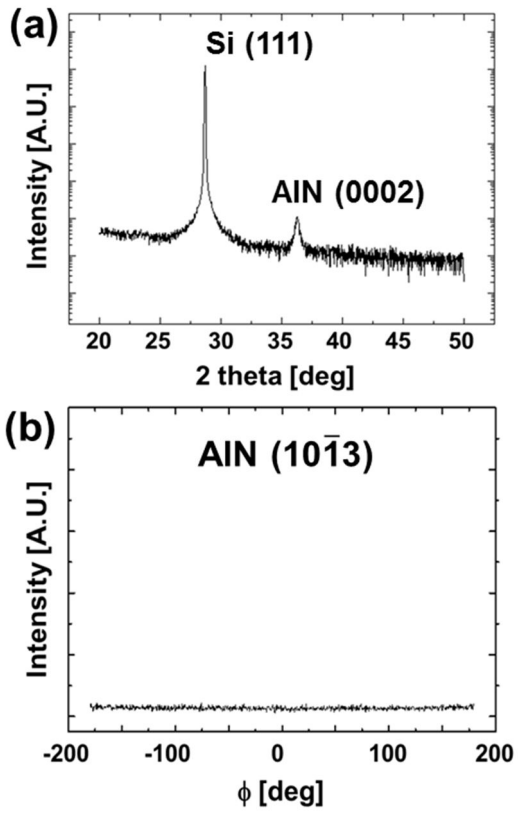


Figure 3.5 (a) XRD θ-2θ patterns and (b) XRD ϕ-scans for the $(10\bar{1}3)_{AlN}$ of the AlN layer sputtered under DC power of 600 W, pressure of 1 mTorr, room temperature and flow rate of Ar (10 sccm) and N_2 (10 sccm) gas.

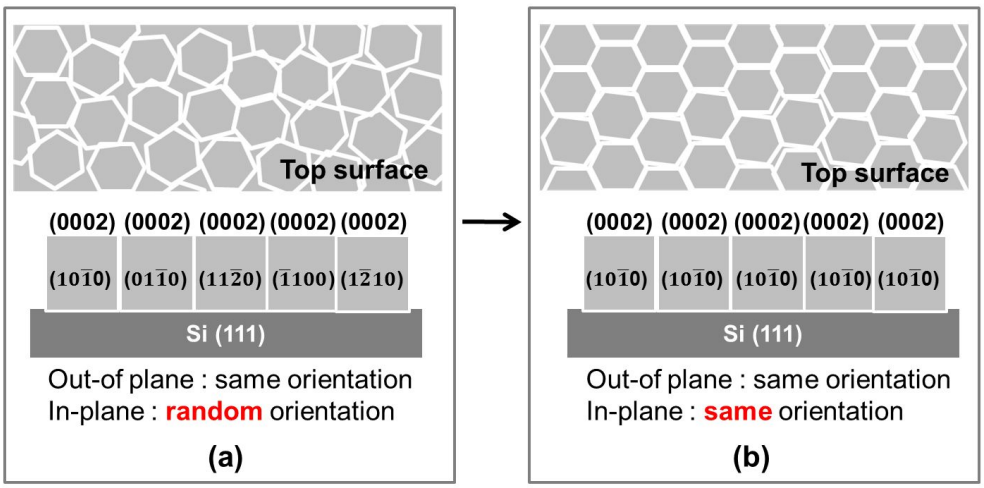


Figure 3.6 Schematic diagrams showing the alignment direction of the each columns in (a) poly-crystalline sputtered AlN and (b) single-crystalline sputtered AlN.

3.1.4 Summary

The AlN layer was sputtered on the Si (111) substrate by DC magnetron sputtering system at room temperature. To align the AlN layer to (0002) plane normal to the Si substrate, the sputtering condition such as pressure, DC power and Ar/N_2 flow rate was investigated. We confirmed that the preferred orientation of sputtered AlN layer was related with the energy of arriving adatoms. Especially, the sputtering pressure was key factor to supply the high energy for adatoms. We succeed the obtaining of (0002) AlN layer using the particular sputtering condition. However, in the growth GaN on the sputtered AlN, we confirmed that the alignment of (0002) orientation does not mean single crystal because alignment in out-of plane was not related with in-plane orientation alignment. Therefore, to use the sputtered AlN for buffer layer of GaN on Si subsrate, obtaining of single crystalline sputtered AlN layer, that is same out-of-plane and in-plane alignment, is needed.

3.2. Epitaxial growth of single crystalline AlN buffer layer on Si (111)

3.2.1 Introduction

For GaN on Si substrate, AlN buffer layer have been widely used. The AlN buffer layer for GaN on Si is commonly grown in the same MOCVD system, which is normally used deposition method for III-nitride, for the GaN growth. The AlN layer is affected by Ga memory effect, as mentioned in chapter 2. Also high growth temperature of AlN buffer layer causes the interdiffusion between Si-Al, resulting in leakage path in electronic device.[15,16] Therefore, other growth systems for AlN buffer layer are necessary. We tried to grow AlN buffer layer by DC magnetron sputtering in previous chapter. In the chapter 3.1, it was confirmed that in-plane alignment of sputtered AlN is needed to use the layer as a buffer layer for GaN on Si. Accordingly, epitaxial growth of AlN on Si by the sputtering system is necessary.

However, to grow AlN on the Si substrate epitaxially, many researchers have used magnetron sputtering at high temperature[21,22] or different sputtering system supplying extreme high power such as pulsed sputtering deposition (PSD) and high power impulse magnetron sputtering (HiPIMS).[23-25] That is because high energy of adatoms (Al or N atoms) was needed to obtain epitaxial layer. However these sputtering conditions offset the advantages of magnetron sputtering system. Recently, single crystalline AlN layer sputtered at 350 ^{o}C was reported by using Al pre-deposition in DC magnetron sputtering system. It was still done at a high temperature and little

has been known about the mechanism. To my knowledge, the epitaxial growth of AlN on Si substrate at room temperature by magnetron sputtering has not been reported. In this chapter, we report successful epitaxial growth of the sputtered AlN at room temperature by DC magnetron sputtering system.

3.2.2 Experimental procedure

AlN thin films were deposited on a 2-inch Si (111) substrate using a DC magnetron sputtering system (KVT-T8896) with an Al target of 99.999% purity. The sputtering and reactive gases were high-purity Ar and N_2, respectively. Before loading Si (111) substrate into the sputter chamber, the native oxide on the Si wafer was removed by etching in a BOE solution. The base pressure of the sputtering system was stabilized at 10^{-7} Torr before introducing the gas mixture. The target was pre-sputtered for 30 min to equilibrate and clean the target surface with the shutter closed. After the pre-sputtering, the 100-nm-thickness AlN thin film was deposited at room temperature. The sputtering pressure of 1 mTorr and Ar/N_2 ratio of 1:1 were fixed for all the samples. In order to study the effect of DC power and Al pre-deposition on the quality of AlN layer, the sputtering conditions were selected as shown in Table 3.3. The process of Al pre-deposition means deposition of 5-nm-thickness thin Al layer by switching off the N_2 gas, before main AlN deposition.

The GaN layer was grown on sample A and B by a Thomas Swan 6x2" close-coupled showerhead MOCVD reactor at 1040 ^{o}C and 38 Torr. Standard precursors such as TMGa and ammonia were used as Ga and nitrogen sources, respectively.

The crystal structure and crystallinity were analyzed byXRD using a PANalytical X'pert Pro X-ray diffractometer. The structural characteristics of the AlN samples were investigated using a JEOL JEM-2100F TEM. The cross-sectional TEM (XTEM) samples were prepared by FIB using a FEI Quanta 3D FIB machine with Pt coating. The structure characteristics of the

GaN layer were analyzed using a Hitachi S-4800 field emission SEM.

Table 3.3 Detailed deposition parameters of the samples.

Sample	Al pre-deposition	DC power	Pressure	Ar/N_2 ratio
A	O	600 W	1 mTorr	1 : 1
B	X	600 W	1 mTorr	1 : 1
C	O	400 W	1 mTorr	1 : 1
D	X	400 W	1 mTorr	1 : 1

3.2.3 Results and discussion

The crystalline structure and preferred orientation of the samples were investigated by XRD. Figure 3.7(a)-(d) shows the XRD θ-2θ patterns of the AlN samples. The diffraction peaks at 28° and 36.1° corresponding to the Si (111) and hexagonal AlN (0002), respectively, were observed for the samples. This indicates that basal plane (0002) of the AlN is parallel to the plane of the substrate, that is $(0002)_{AlN} \| (111)_{Si}$. As we mentioned in chapter 3.1, 1 mTorr adopted in the experiment, the arriving atoms become energetic to align with (0002) out-of-plane, as shown in Fig. 3.7(a) to (d). Although all the samples exhibited AlN (0002) peak under 1 mTorr, the different intensities of the peaks were observed for each sample. The intensities indicate degrees of the alignment to (0002) orientation of the AlN crystallites. Accordingly, sample A was well aligned to the (0002) orientation but sample D was not done. The different intensities suggested that, in addition to the sputtering pressure, other conditions such as a DC power and pre-deposited Al process were also important to improve alignment to (0002) orientation of sputtered AlN. Nevertheless, the alignment of (0002) orientation does not mean single crystal because alignment of out-of plane is not related with in-plane orientation alignment.

To confirm the in-plane orientation of the samples, ϕ-scan from the asymmetric $(10\bar{1}3)_{AlN}$ was measured for the samples, as shown in Fig. 3.7(e)-(h). A six-fold symmetry with an interval of 60° was observed for only sample A (Fig. 3.7(e)), which indicates sample A was single crystalline structure. On the other hand, no peaks were observed for sample B-D, implying random in-plane orientation. It was known that sufficient energy to

cause surface and bulk diffusion for epitaxial growth is necessary to grow single crystalline film on a single crystalline substrate.[26,27] In comparison of sample A with sample B and C, the samples were deposited under same parameters except Al pre-deposition and DC power, respectively. It could be understood that the adatoms with high kinetic energy from high DC power for sample A would contribute to the enhancement of surface migration, resulting in epitaxial growth.[28-30] Interestingly, under same DC power, no ϕ-peaks were observed in sample B in comparison with sample A. The outstanding appearance of the six-fold symmetry for sample A suggested that the AlN could be grown epitaxially with pre-deposited Al process as well as high DC power.

Figure 3.8 shows results of cross-sectional TEM observations of samples A and B, shows the effect of Al pre-deposition for the sputtering of AlN layer, along the zone axis of Si [1$\bar{1}$0] direction. The 100-nm-thickness AlN layers were observed for both samples in Fig. 3.8(a) and (d). The figure 3.8(b) and (c) are HRTEM image and the corresponding fast-Fourier-transformed (FFT) pattern of the AlN layer in sample A. The AlN lattices of sample A are well aligned with the growth direction along [0001] without tilting. The FFT image displays the diffraction spots of wurtzite AlN along the [11$\bar{2}$0] zone axis with revealing the AlN was grown as a single crystalline structure. Especially, the all spots related with in-plane direction were displayed clearly.

On the other hands, HR TEM image (Fig. 3.8(e)) and the corresponding FFT pattern (Fig. 3.8(f)) of the AlN layer in sample B showed different results from that for the sample A. The crystalline AlN lattices were observed in Fig. 3.8(e), but the lattices were slightly tilted with respect to the growth direction, in Fig. 3.8(e). Accordingly, the spot of $(0002)_{AlN}$ was observed as

an arc broadening with 30° in Fig. 3.8(f). The weaker peak intensity of AlN (0002) in sample B than sample A, as shown in Fig. 3.7(a) and (b), could be explained as the alignment behavior of AlN lattices along to the $[0002]_{AlN}$ direction. Moreover, in Fig. 3.8(f), the spots related with in-plane direction were displayed with nearly ring pattern, which means that each AlN column is aligned with various in-plane orientations. The TEM results indicate again that sample A was deposited as a single crystal, but sample B was deposited as a poly-crystalline structure, which are consistent with the XRD results in Fig. 3.7.

To investigate the epitaxial relationship between the AlN layer and Si (111) substrate in sample A, further analysis of ϕ-scan was employed. Figure 3.9 shows the ϕ-scan of sample A from the asymmetric $(10\bar{1}1)$ plane of AlN layer, which again confirms single-crystalline AlN film, and (220) plane of Si substrate, which exhibits three-fold peaks with an interval of 120°. Furthermore, the six diffraction peaks of AlN $(10\bar{1}1)$ and three diffraction peaks of Si (220) are exactly overlapped without any rotation. Therefore, the in-plane epitaxial relationship is determined to be $AlN[11\bar{2}0]\|Si[1\bar{1}0]$.

Pre-deposited Al process proceeded before the main deposition of AlN. Accordingly, the Al layer on the Si (111) substrate was investigated. 100-nm-thickness Al layer was sputtered on the Si substrate at room temperature, 1 mTorr and 650 W. Figure 3.10 shows XRD θ-2θ pattern of the Al sample. In the pattern, Al (111) and Al (200) peaks were observed. It is known that Al (100) is deposited on Si (111) when Al is sputtered at room temperature on Si (111) substrate.[31] The inter-plane spacing of Al (100), Al (111) and Si (111) was known as 2.02 Å, 2.48 Å and 3.135 Å, respectively. Under low thermal energy circumstance, Al (100) could be grown at the steps in the Si (111)

surface preferentially, because the difference in step height between two of Al (100) and one of Si (111) is smaller than that between two of Al (111) and one of Si (111).[31,32] Nevertheless, it was observed that epitaxial growth of Al (111) on Si (111) could be accomplished on the terraces due to the same threefold symmetry under sufficient thermal energy.[33,34] Therefore, it is expected that the pre-deposited Al in the sample A would be grown epitaxially with (100) and (111) out-of-plane.

The difference between sample A and B caused by pre-deposited Al process would be observed at the interface between AlN and Si substrate. The HRTEM images of the AlN/Si interface of sample A and B were shown in Fig. 3.11. In case of sample A, the 5-nm-thickness Al film was observed between AlN and Si substrate, resulting from pre-deposited Al process. The FFT pattern at the interface between AlN and Si of sample A (Fig. 3.11(b)) represented single crystalline Al with face centered cubic (FCC) structure spots. According to the FFT pattern, the AlN, Al and Si substrate had orientation relationship of out-of-plane with AlN[0001]||Al[100]||Si[111]. The result of Al is accordance with the result of Fig. 3.10. Moreover, in the FFT pattern, in-plane orientation relationship among AlN and Al to the Si substrate could be determined to be AlN$[1\bar{1}00]$||Al$[0\bar{1}1]$||Si$[11\bar{2}]$ and AlN$[11\bar{2}0]$||Al[011]||Si$[1\bar{1}0]$. The results indicate that AlN and Al layers in the sample A were grown on the Si substrate epitaxially.

Figure 3.11(c), a HRTEM image of sample B, shows a sharp AlN/Si interface with no interdiffusion of Al and Si due to the low sputtering temperature. Also, no SiN_x layer was observed between AlN and Si substrate. Nevertheless, sample B does not reveal the epitaxial relationship between AlN and Si substrate. Figure 3.11(c) and the inset, the corresponding FFT

pattern at the region, show that the lattice of AlN is not followed to the lattice of Si substrate to in-plane orientation. Based on the above results, we confirmed that the existence of Al interlayer between AlN and Si enables sputtered AlN to be grown epitaxially on Si (111) substrate.

Based on the XRD and TEM analyses, atomic arrangement model of interface between AlN (0002) and Al (100) was derived as shown in Fig. 3.12. The theoretical lattice parameters of a-axis in AlN of wurtzite structure is 3.11 Å and a-axis in Al of FCC structure is 4.048 Å.[31,35] Figure 3.12 shows Al (100) top surface with FCC structure and AlN (0002) lattice with wurtzite structure. According to the in-plane alignment of AlN[$1\bar{1}00$]||Al[$0\bar{1}1$] and AlN[$22\bar{4}0$]||Al[011], in our observations shown in FFT pattern and XRD result, the coincident positions between AlN and Al lattices having the different crystal structures could be marked as shown in the schematic model. Using the theoretical lattice constants of Al and AlN, the lattice mismatch between AlN and Al is calculated to be 6% (AlN[$1\bar{1}00$]||Al[$0\bar{1}1$]) and 8.5% (AlN[$22\bar{4}0$]||Al[011]), respectively.

Meanwhile, the Al (111) region in the sample A was also observed. Figure 3.13(a) and (b) show the HRTEM image of AlN/Al(111)/Si substrate and the corresponding FFT pattern of the region. The epitaxial relationship with sample A and Si substrate was also determined as a AlN[0001]||Al[111]||Si[111] and AlN[$1\bar{1}00$]||Si[$11\bar{2}$]. The results indicate that AlN could be grown on Si (111) substrate at room temperature through Al (111) layer as well as Al (100) layer. The atomic arrangement model of interface between AlN (0002) and Al (111) could be derived as shown in Fig. 3.13(c). The coincident positions between AlN and Al lattices could be marked as shown in the Fig. 3.13(c) thank to the same hexagonal symmetry.

The theoretical lattice parameter of a-axis in AlN with Wurtzite structure is 3.11 Å and a-axis in Al (111) plane with FCC structure is 2.86 Å. Thus, lattice mismatch between AlN and Al (111) is calculated to be 8.5%. Considering the lattice mismatches between AlN and Al (100) and Al (111) are much lower than that between AlN and Si substrate (19%), we speculated that the epitaxial growth of AlN is attributed to the small lattice mismatch between AlN and Al in such selected planes.

For the growth of single crystalline AlN, sufficient energy to migrate to the substrate lattice, that is demanded energy (or activation energy) for epitaxial growth, is necessary to arriving atoms. The total energy delivered to the film during the sputtering (E_T) could be expressed as follows.[36]

$$\boldsymbol{E_T = E_S + E_P + E_{mt} + E_{ch} + E_{rad}} \quad [3\text{-}2]$$

where E_S is heat from substrate, E_P is kinetic energy of bombarding and condensing particles incident on the film surface and forming the film, E_{mt} is heat radiated form sputtered magnetron target, E_{ch} is the heat evolved in formation of the compound (energy from exothermic chemical reactions), and E_{rad} is the heat radiation from plasma. In our case, all the AlN samples were sputtered under same condition except the DC power and Al pre-deposition. Thus, E_S, E_{mt}, E_{ch}, and E_{ch} are identical for all the AlN samples. Moreover temperature of sputtering was room temperature. Therefore the AlN film was deposited away from thermodynamic equilibrium but by kinetic energy. The E_P can be expressed by the following formula:[36]

$$\boldsymbol{E_P \approx (U_s i_s) exp(-L/\lambda_i)/a_D} \quad [3\text{-}3]$$

where $U_s i_s$ is the term related with DC power, L is the distance between target and substrate, λ_i is the mean free path, and a_D is the deposition rate. Under the same sputtering pressure, DC power determines the total energy delivered to the film. Accordingly, the relative magnitude of total energy between sample A (E_{TA}), B (E_{TB}), C (E_{TC}), and D (E_{TD}) could be expressed by following

$$\boldsymbol{E_{TA} = E_{TB} > E_{TC} = E_{TD}} \quad [3\text{-}4]$$

To be grown epitaxially, the sufficient energy would be needed because the adatom have to move to suitable lattice site, whereas the demanded energy for poly-AlN growth is small relatively compared with the energy for epitaxy growth. Figure 3.14 shows the energy profile diagram demonstrating the AlN sputtering. Because the free energy of epitaxial AlN is more stable than that of poly-crystalline AlN and demanded (or activation) energy for epitaxial growth of AlN on Si ($E_{a,s}$) is larger than the energy for poly-crystalline AlN($E_{a,p}$), the energy paths are expressed as shown in Fig. 3.14.

In our result, the sample B and D was grown as a poly-crystal, but not single crystal. Therefore the kinetic energy of atoms during the sputtering in sample B and D was lower than the activation energy for epitaxial growth of AlN on Si (111) substrate ($E_{a,s}$). On the other hands, it was expected that the activation energy for epitaxial growth of AlN deposition on Al interlayer ($E_{a\prime,s}$) became lower than that on Si substrate ($E_{a,s}$), resulting from small lattice mismatch with AlN and Al comparing with AlN and Si. Therefore, sample A could be grown epitaxially on Si substrate thanks to pre-deposited Al, in despite of same kinetic energy with sample B. In case of sample C, it could be explained that the kinetic energy of sputtered adatoms under 400 W

was smaller than the lowered activation energy for single crystalline AlN deposition due to the Al interlayer. Therefore we could conclude the energy relationship as follows;

$$\boldsymbol{E_{a,s} > E_{TA} = E_{TB} > E_{a',s} > E_{TC} = E_{TD} > E_{a,p}} \qquad [3\text{-}5]$$

The energy relationship in equation [3-5] is expressed in Fig. 3.14. In our experiment, different from other methods such as supplying high thermal[21,22] or kinetic energy[23-25], the reduced activation energy for single crystalline AlN, resulting from the pre-deposited Al layer, enabled to grow epitaxial AlN layer.

GaN layer was grown on the sample A and B by MOCVD, in the same batch at 1040 ^{o}C and 38 Torr. Figure 3.15 shows the pictures of 2 inch GaN on sample A and B. Mirror-smooth film was observed in GaN on sample A, as shown in Fig. 3.15(a), which means GaN was grown with single crystalline characteristics. On the other hands, the GaN layer grown on the sample B was not observed as mirror-smooth by naked eyes, as shown in Fig. 3.15(b).

In SEM images, 2-dimensional and flat GaN on sample A was observed as shown in Fig. 3.16(a). Also, strong GaN (0002) peak and 6-fold symmetry of GaN was observed in Fig. 3.16(b) and (c). The result shows that we succeeded in the growth of single crystalline GaN layer using AlN buffer layer sputtered at room temperature. On the other hand, the GaN layer grown on the sample B exhibited 3 dimensional GaN, differently oriented GaN crystallites with random angles, as shown in Fig. 3.16(d). Because of the randomly oriented GaN islands, any peaks were not obtained in XRD ϕ-scan data (Fig. 3.16(f)), though GaN (0002) peak was observed in XRD θ-2θ scan

profile (Fig. 3.16(e)). The tendency of XRD result corresponds to the result of sample B, which means the GaN layer is significantly affected by sputtered AlN layer. Therefore, the AlN layer grown epitaxially at room temperature by sputtering system can be buffer layer for GaN growth on Si substrate. It is expected the sample A would be substituted for AlN layer grown by MOCVD at high temperature for GaN on Si growth.

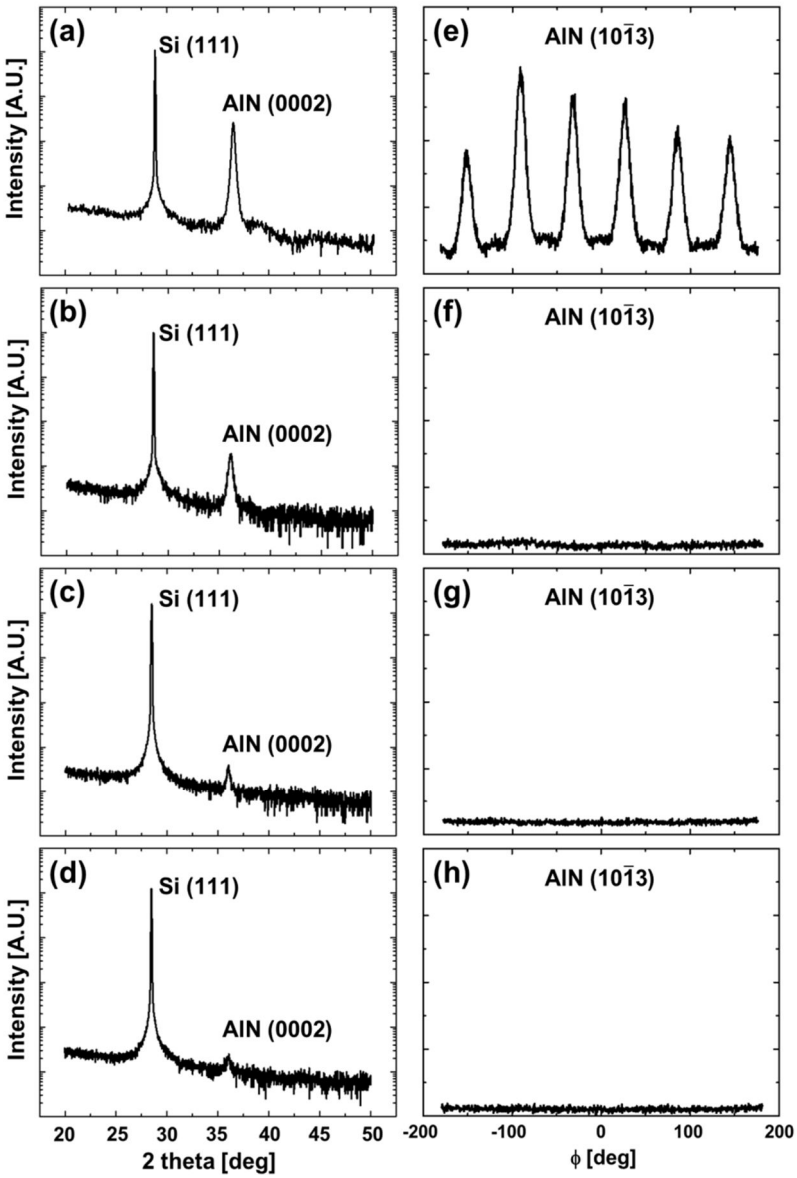


Figure 3.7 XRD θ-2θ scan profiles of (a) sample A, (b) sample B, (c) sample C and (d) sample D. XRD ϕ-scan profiles for the $(10\bar{1}3)_{AlN}$ plane of (e) sample A, (f) sample B, (g) sample C and (h) sample D.

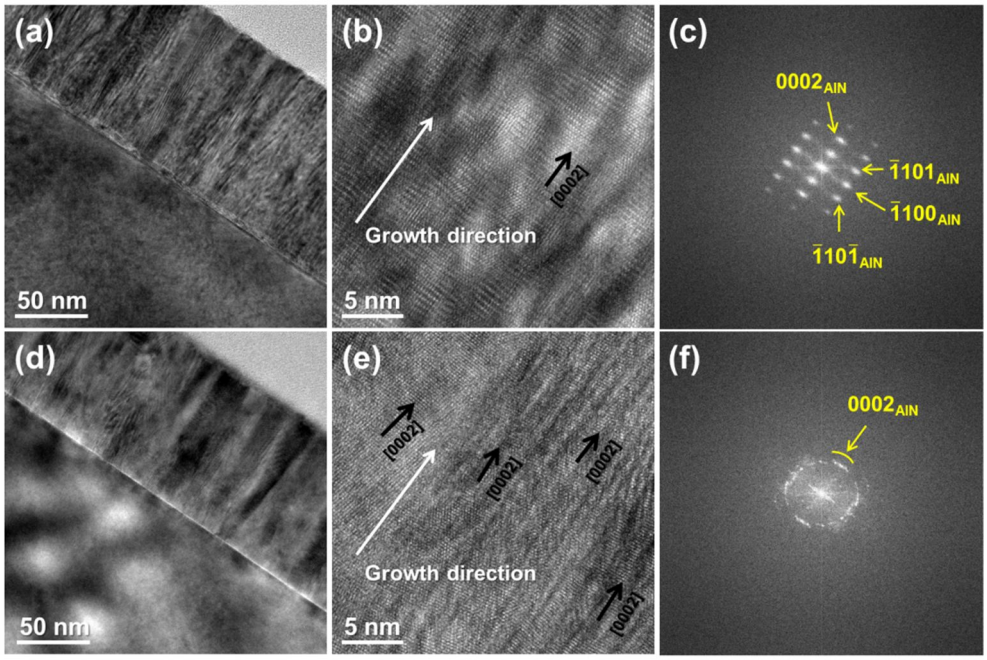


Figure 3.8 (a) Cross sectional TEM image, (b) HR TEM image of the AlN layer and (c) the corresponding FFT pattern of sample A. (d), (e) and (f) the data of sample B.

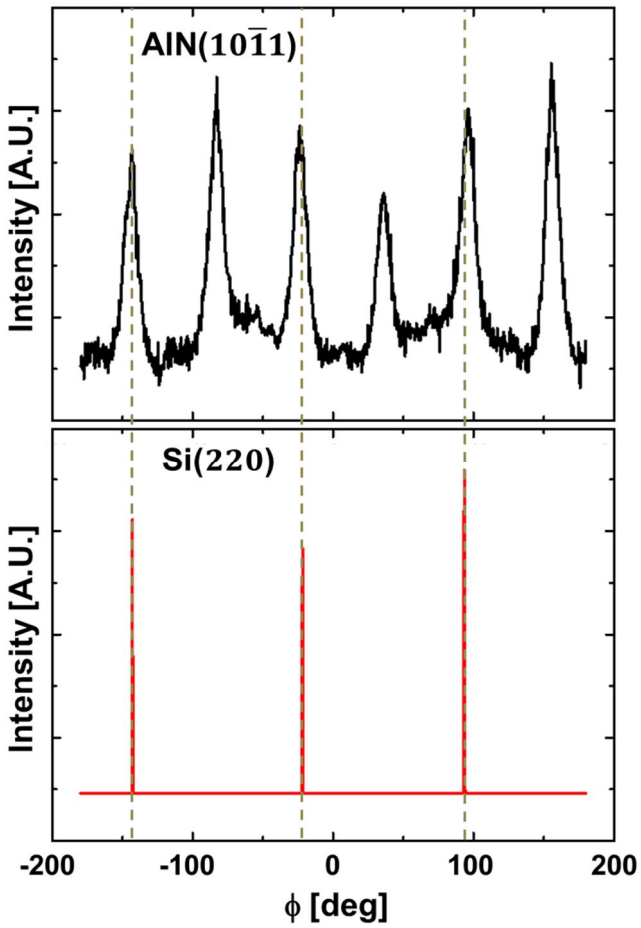


Figure 3.9 XRD asymmetric ϕ-scan profiles for AlN (10$\bar{1}$1) and Si (220) plane.

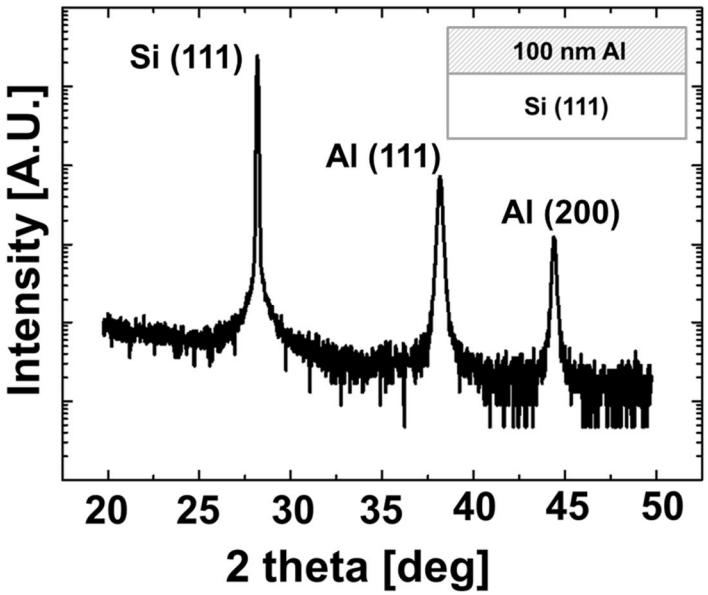


Figure 3.10 XRD θ-2θ scan profile of 100-nm-Al layer on Si substrate by sputtering system.

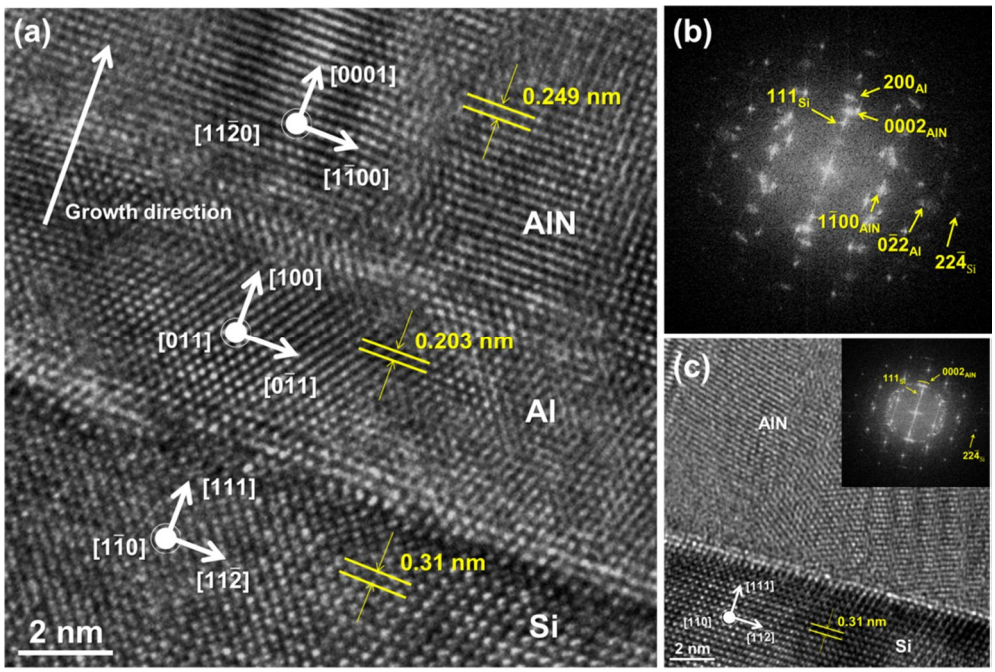


Figure 3.11 (a) HR TEM image of sample A at the interface between AlN and Si substrate and (b) the corresponding FFT pattern. (c) HR TEM image of sample B at the interface between AlN and Si (inset: the corresponding FFT pattern).

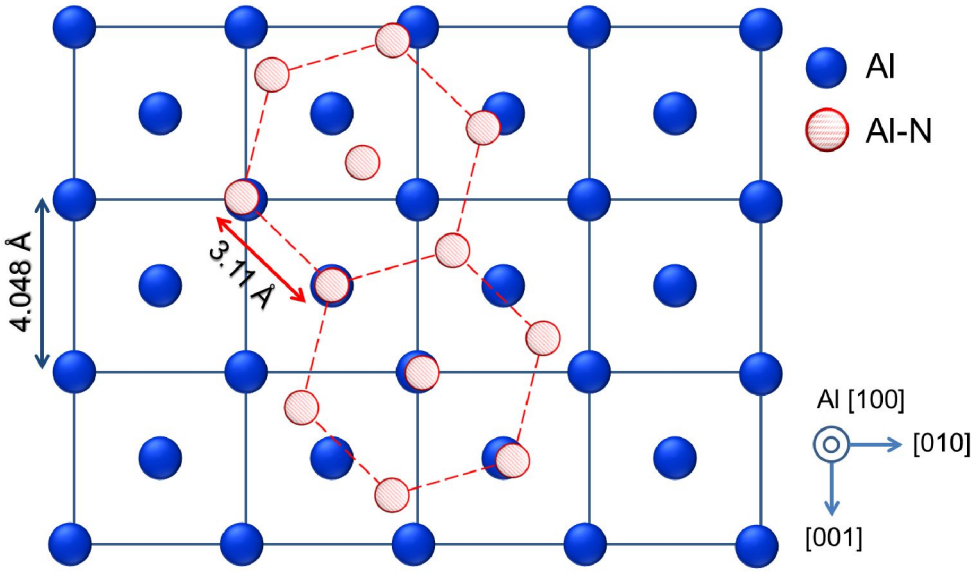


Figure 3.12 Schematic model showing the interface between Al (100) and AlN (0002).

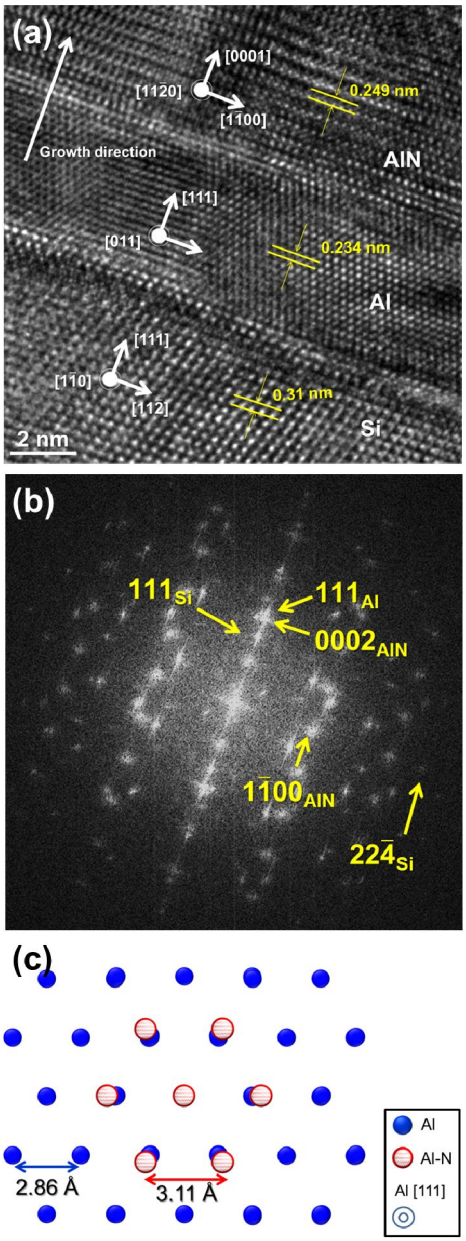


Figure 3.13 (a) HR TEM image of sample A at the interface between AlN and Si substrate with Al (111) interlayer and (b) the corresponding FFT pattern. (c) Schematic model showing the interface between Al (111) and AlN (0002).

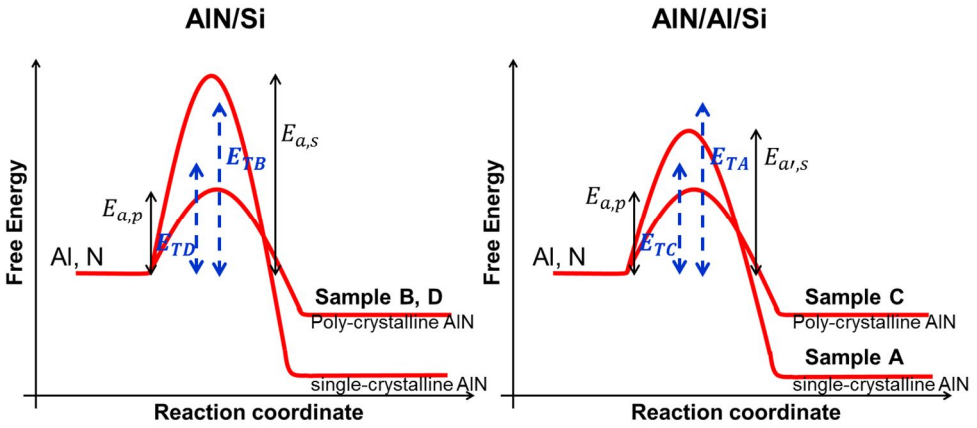


Figure 3.14 Free energy path demonstrating the AlN sputtering on Si (left) and on Al/Si (right).

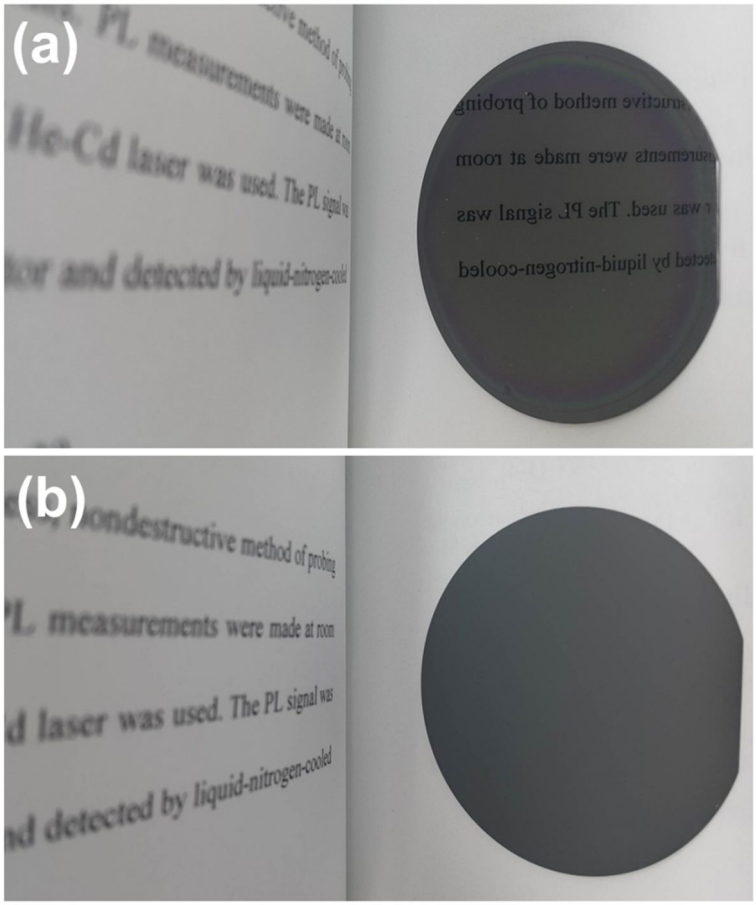


Figure 3.15 Pictures of 2 inch template of GaN on (a) sample A and (b) sample B.

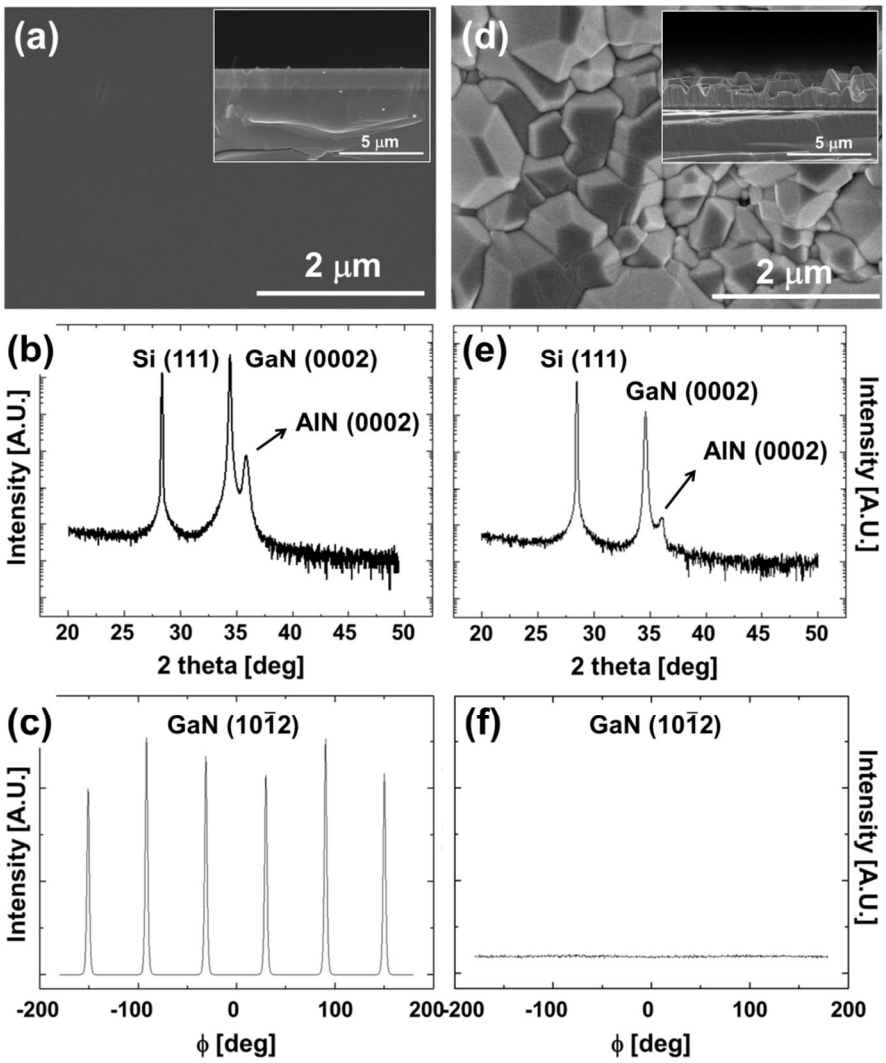


Figure 3.16 (a) plan-view SEM image (inset: cross-sectional SEM image), (b) XRD θ-2θ pattern and (c) XRD ϕ-scan profiles for the $(10\bar{1}2)_{GaN}$ plane of GaN on sample A. (d), (e) and (f) the data of GaN on sample B (The data is same with Fig. 3.4).

3.2.4 Summary

The epitaxial growth of AlN layer by DC sputtering at room temperature was investigated. We verified the single crystalline AlN could be deposited with pre-deposited Al and high DC power. It is expected that the activation energy for epitaxial growth of AlN on Al interlayer became lower than that on Si substrate, resulting from small lattice mismatch with AlN and Al (6~8%) comparing with AlN and Si (19%). The method to grow epitaxial AlN layer is different from other methods such as supplying extremely high thermal or kinetic energy. Moreover, the sufficient kinetic energy from the high DC power helps to grow single crystalline AlN even at room temperature. Finally, single crystalline GaN was grown by MOCVD on the sputtered AlN, which shows epitaxial AlN layer grown at room temperature by sputtering system could be substituted for AlN layer grown at high temperature by MOCVD.

3.3. Further study of AlN buffer layer grown by DC magnetron sputtering at room temperature

3.3.1 Annealing process for AlN buffer layer

The growth technique of single crystalline AlN layer by DC sputtering at room temperature was developed as using pre-deposited Al process. To use the layer for electrical device, semi-insulating characteristic is necessary. Unfortunately, the AlN layer would be very conductive due to thin Al layer between Si substrate and AlN. The sheet resistance of 2 inch wafer was measured with a Lehighton Lei 1510B, which gives sheet resistance mapping of the total layer including the substrate. Figure 3.17(a) shows the result of sheet resistance of 2 inch full wafer of the sputtered AlN (sample A in Chap. 3.2). The average sheet resistance is 41.58 Ω/sq. It is assumed conducing Al interlayer makes current path because Si substrate and AlN are semi-insulting. The low resistivity is not suitable for electronic device. To solve the problem, the sample A was annealed at 1040 ^{o}C during 10 min under ammonia and N_2 ambient by MOCVD system (the process is identified as ammonia annealing). The ammonia gas was started to flow from 200 ^{o}C (where is starting point of temperature ramp-up). Figure 3.17(b) shows the sheet resistance map of sample A after ammonia annealing**.** The average sheet resistance was measured as a 33,351 Ω/sq, which is comparable or little bit higher value than it of conventional AlN layer grown by MOCVD system. It is expected the Al layer was eliminated by ammonia annealing process.

To confirm the behavior of Al interlayer before and after the ammonia annealing, Al_{2p} X-ray photoelectron spectroscopy (XPS) spectra was

measured using AXIS-His for sample A and annealed sample A as shown in Figure 3.18. The Al_{2p} XPS peaks were measure at the interface between AlN and Si, which was conducted by the XPS depth profiling. In the sample A, Al_{2P} peak consists of Al-N bond, which have binding energy of 73.5 eV, and Al-Al bond, which have binding energy of 72.4 eV. It is expected that the Al-Al bond represents the Al interlayer, which is shown in Fig. 3.11(a), resulting from pre-deposited Al process. On the other hand, after ammonia annealing, Al-Al bond was not observed, but strong and sharp Al-N peak was only observed. The result shows Al interlayer was eliminated during ammonia annealing, and the Al would be changed to AlN due to the introduction of N source from ammonia gas.

Figure 3.19 shows the HR TEM images of sample A and annealed sample A. It is also observed the Al interlayer was eliminated after ammonia annealing. The ambiguous layer was observed, but the further study of the layer is under way.

There are two possibilities in behavior of Al interlayer during ammonia annealing; one is diffusion into the Si substrate and another is formation of AlN due to ammonia source. To confirm the behavior of Al interlayer, SIMS depth profiling was conducted as shown in Fig. 3.20. In the image, the profile with deep color and pale color represent sample A and annealed sample A, respectively. In case of profile of sample A, decreased intensity toward surface is due to the charging effect. Focused on the circle in Fig. 3.20, we verified that Al was present in high concentration at the interface between Si and AlN, but the intensity of N is already decreased at the point in sample A, which indicates Al interlayer. On the other hands, in profile of annealed sample A, N was diffused to the Al interlayer, but no diffusion of Al into the

Si substrate was observed. We concluded that introduction of ammonia gas from starting point of temperature ramp-up supplied nitrogen source, and the nitrogen diffused to the Al interlayer before diffusion of Al into the Si substrate, resulting in formation of AlN layer. Accordingly, high-resistive AlN layer on Si could be obtained through the ammonia annealing process. It is expected that the epitaxial AlN grown at room temperature by sputtering system could be used for nitride-based electronic devices.

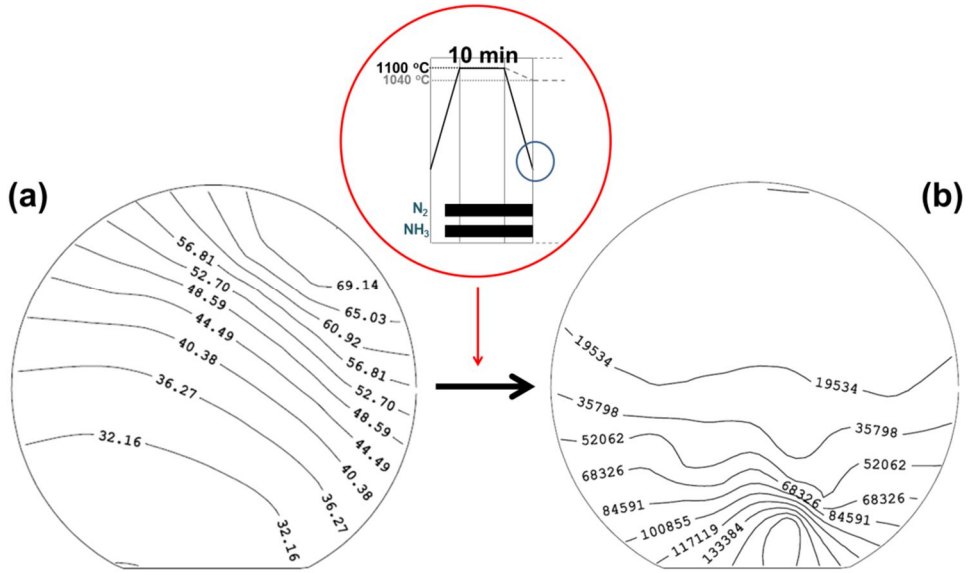


Figure 3.17 Sheet resistance map of (a) sputtered AlN (sample A in chap. 3.2) and (b) annealed sample A under ammonia and nitrogen ambient during 10 min by MOCVD. The average sheet resistance is 41.58 and 33,351 Ω/sq, respectively. The schematic in the circle shows ammonia annealing process of sample A.

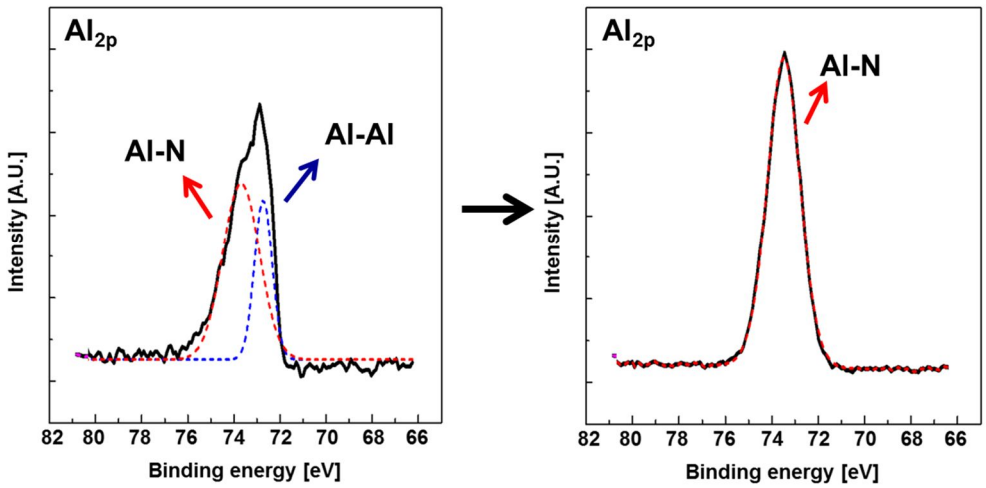


Figure 3.18 Al_{2p} XPS spectra at the interface between AlN and Si of (a) sample A and (b) annealed sample A. The binding energy of Al-Al is 73.5 eV and Al-Al is 72.4 eV.

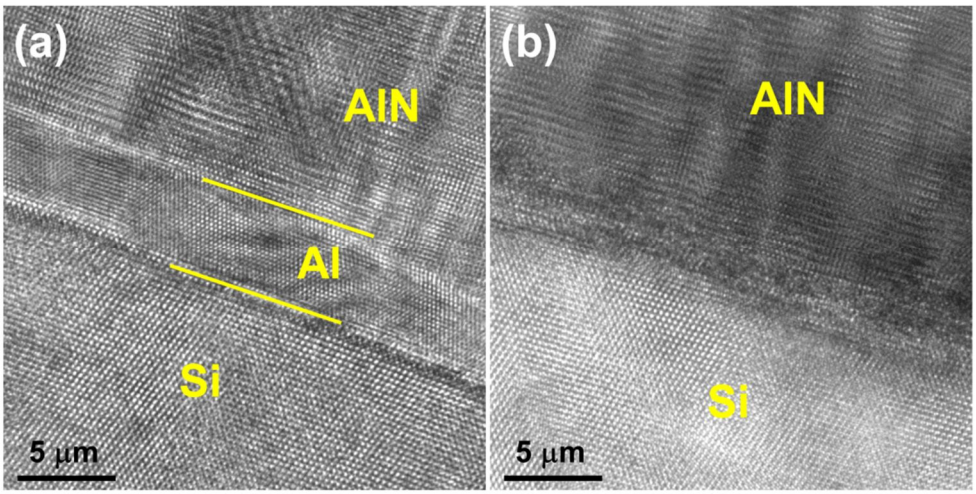


Figure 3.19 HR TEM image at the interface between AlN and Si of (a) sample A and (b) annealed sample A.

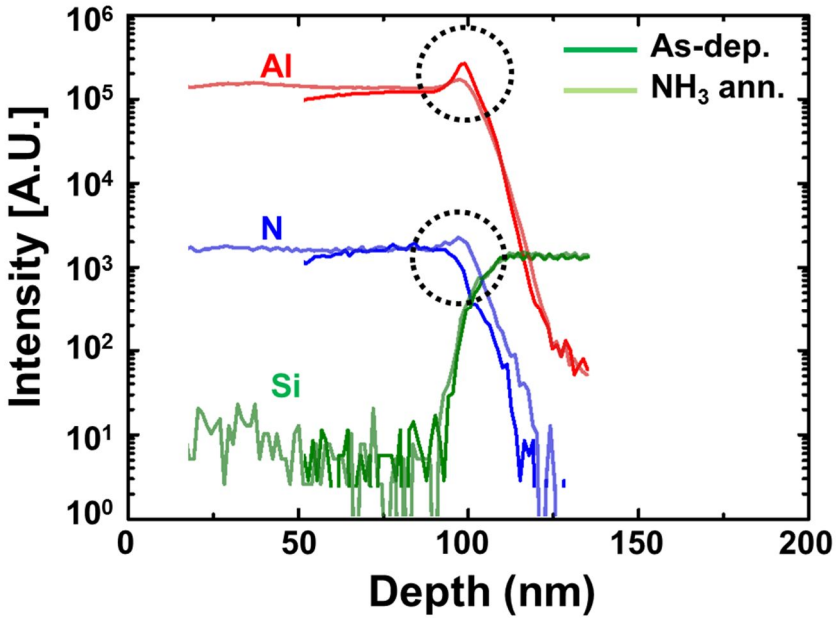


Figure 3.20 SIMS depth profiles of Al (red), N (blue) and Si (green) for sample A (deep colors) and annealed sample A (pale colors).

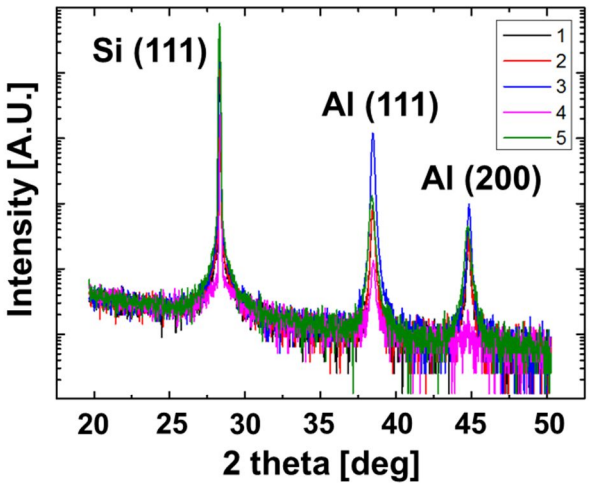
3.3.2 Further study on the pre-deposition process

In the chap. 3.2, pre-deposited Al process was important to obtain single crystalline AlN layer. However, we confirmed that the pre-deposited Al on Si (111) substrate at room temperature was deposited with (111) and (100) orientation, simultaneously, as shown in Fig. 3.10, 3.11 and 3.13. It means that Al interlayer between AlN and Si substrate would have poly grains with (111) and (100) orientations. We expect that the Al layer would have negative effect for AlN layer, because the each AlN layers grown on Al (111) and Al (100) would have different crystalline properties. Therefore, we tried to obtain uniform Al layer with one preferential orientation. The 100-nm-thickness Al layers were deposited on the Si (111) by sputtering system at room temperature with various pressure and DC power. Figure 3.21 shows θ-2θ XRD pattern of the samples with the sputtering conditions of each sample. Al (111) and Al (100) peaks are always observed, simultaneously, under various conditions. It is known that Al (111) on Si (111) could be grown with sufficient thermal energy.[33,34] Therefore, it is hard to obtain only Al (111) peak at room temperature.

We developed introduction of Ti interlayer to get only Al (111) layer. It is known that Ti is easily aligned in the (0002) orientation, since the facet has the lowest total energy.[37,38] To confirm the preferential crystalline orientation of sputtered Ti, 15-nm-thicnkess Ti was deposited on Si (111) substrate by DC magnetron sputtering under 1 mTorr, 500 W and room temperature. The only Ti (0002) peak was observed in XRD θ-2θ pattern in Figure 3.22(a). Accordingly, the 100-nm-thickness Al was deposited on the 5 nm-thickness Ti on Si (111) substrate. Figure 3.22(b) shows the XRD θ-2θ pattern of Al on

Si (111) with and without Ti interlayer. The data of Al on Si with Ti interlayer reveals, surprisingly, only Al (111) peak, though both of Al (111) peak and Al (100) peak are revealed in case of Al on Si (111) without Ti interlayer. The preferential orientation of Ti would help that Al layer could be grown with one preferential orientation. That's because the crystal structure of Ti (0002) is same with Al (111) and also the lattice mismatch between two metal layers is small (3%).

AlN layer was deposited under same sputtering condition with sample A in chap. 3.2., but 5-nm-thickness Ti and 2-nm-thickness Al were pre-deposited prior to main AlN deposition. Figure 3.23 shows the comparison with ϕ-scan from the asymmetric $(10\bar{1}3)_{AlN}$ for the AlN layer with only pre-deposited Al (black) and AlN layer with pre-deposited Ti and Al (red) process. The scan profile of AlN with pre-deposited Al is the data of Fig. 3.7(e). The strong intensity and sharp peaks were observed in case of AlN layer with pre-deposited Ti and Al, which means the sample exhibits excellent alignment to in-plane orientation. We assume that the only one preferential orientation of Al layer would help to obtain the improved crystalline AlN layer. The results show that there are potentials of improvement in the crystal quality for sputtered AlN layer by using various pre-deposited metal process.



Sample	Pressure	DC power
1	3 mTorr	500 W
2	5 mTorr	500 W
3	1 mTorr	600 W
4	1 mTorr	400 W
5	1 mTorr	200 W

Figure 3.21 XRD θ-2θ scan profiles of the 100-nm-thickness Al layers on Si (111) substrate. The table lists the sputtering conditions for each sample.

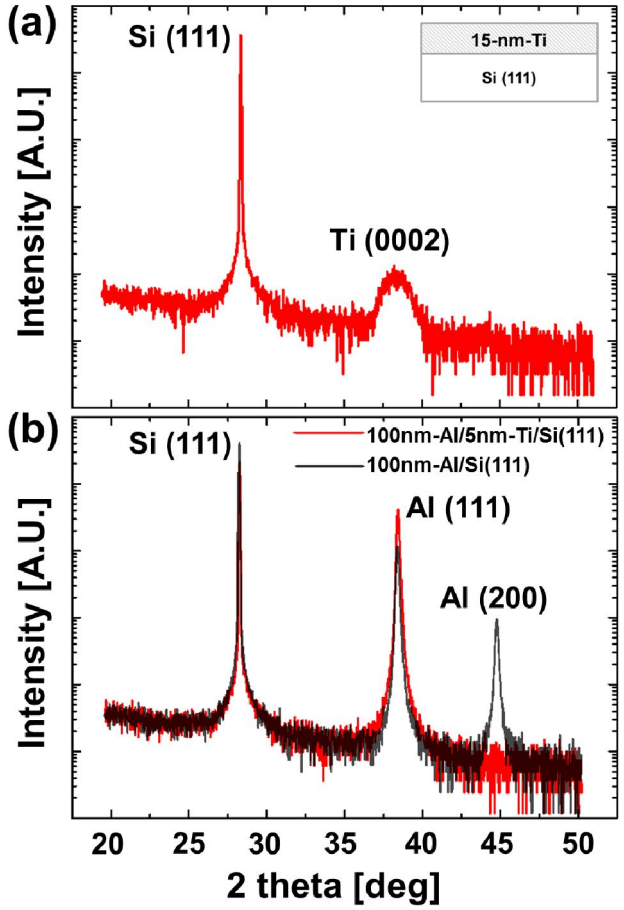


Figure 3.22 XRD θ-2θ scan profiles of (a) 15-nm-thickness Ti layer on Si (111) substrate and (b) 100-nm-thickness Al layers on Si (111) substrate with 5-nm-thickness Ti interlayer (black) and without Ti interlayer (red).

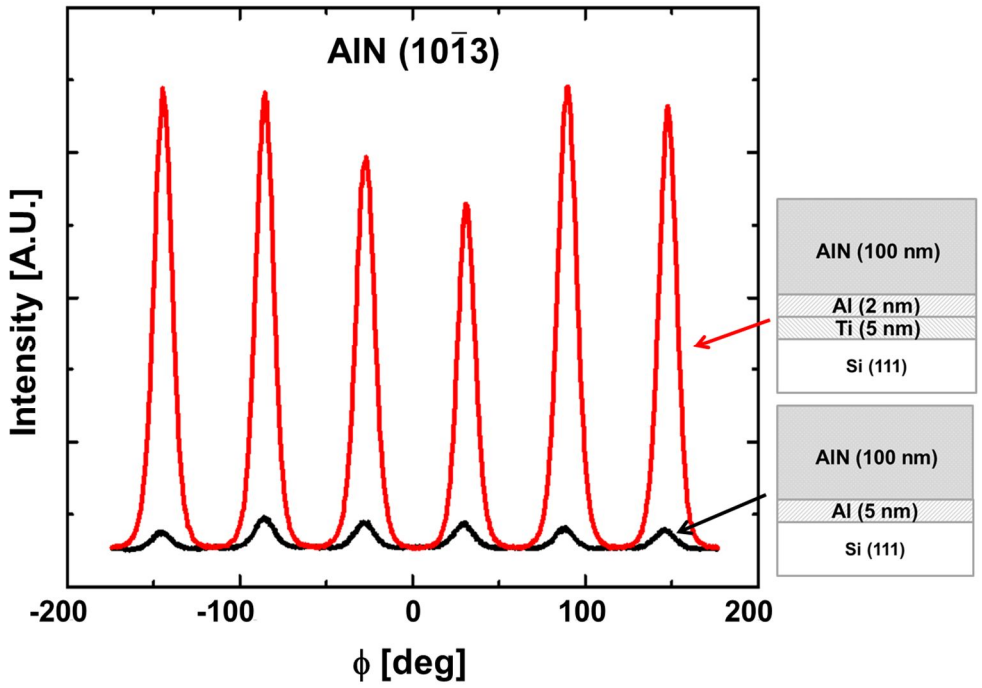


Figure 3.23 XRD ϕ-scan profiles for the (10$\bar{1}$3) plane of sputtered AlN layer with pre-deposited Ti and Al (black) and sputtered AlN layer with only pre-deposited Al (red). The structures of samples are 100-nm-thickness AlN/2-nm-thickness Al/5-nm-thickenss Ti/Si (111) substrate and 100-nm-thickness AlN/5-nm-thickenss Al/Si (111) substrate (in Fig. 3.7(e)), respectively.

3.4. Bibliography

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Chapter 4. The development of low temperature buffer layer for GaN on sapphire

4.1. Introduction

For growth of AlGaN/GaN based HEMT structures, various substrates such as sapphire, silicon, and silicon carbide have been used. In particular, for power device, Si and SiC substrates have been investigated due to high thermal conductivity. The SiC substrate, however, is so expensive that it hinders the application of GaN materials,[1] and the GaN layer grown on Si substrate still have many problems like high dislocation density and strain control.[2] On the other hand, sapphire substrates may still be attractive for low power HEMT applications because of low cost and high crystal quality of GaN grown on sapphire. Moreover, other applications using HEMT on sapphire are expected such as transparent conductors[3] or monolithically integrated LED/HEMT layer.[4]

However, it is well known that normally undoped GaN grown on sapphire shows n-type conductivity due to undesirable background donor impurities.[5] The conductivity becomes a serious drawback in HEMT structure because the current can be partially flowed in the GaN layer instead of 2DEG channel.[6] Therefore, growth of a semi-insulating GaN layer is important for electronic devices to enable a complete channel pinch-off, low loss at high frequency, and high off-state breakdown voltage.[6] Various approaches have been investigated to obtain a high quality semi-insulating GaN layer. One approach is to compensate donor impurities by doping with

deep acceptors such as iron[7], zinc[8], beryllium[9], chrome[10] or carbon[11]. However, these methods have undesired side-effects such as reactor contamination leading to strong memory effects.[7] Another method to induce deep acceptor levels is to generate edge-type dislocations in GaN layer.[12] This approach seems also to be problematic because the high density of dislocations affects the electrical performances associated with carrier trapping and carrier lifetime.[13] It has been suggested that a thin degenerate layer responsible for serous n-type conductivity in undoped GaN layer exists at the GaN/sapphire interface.[14] During the GaN growth on sapphire substrate, the substrate itself becomes a source of oxygen through diffusion, resulting in a highly conducting channel near the GaN/sapphire interface.[15] It was reported that the vast majority of the measured conductivity in a nominally undoped GaN layer originated in the near-interface region, with material far from the interface being insulating.[16]

Meanwhile, a large compressive stress is applied to the GaN layer because of the difference in the thermal expansion coefficients, which results in significant wafer bowing after the growth.[17,18] In the case of a 2-μm-thick GaN layer on 2 inch diameter sapphire wafer, wafer bowing larger than 30 μm is often observed after cooling to room temperature.[19] Moreover, scale-up of the wafer size is expected to further increase wafer bowing.[20] This wafer bowing problem leads to non-uniform wafer temperature distribution that deteriorates the uniformity of device properties. Furthermore, excessive bowing results in difficulties with subsequent device processing, especially in regards to achieving an adequate yield.[21] In recent years, demands for cost reduction through improved growth/fabrication techniques and manufacturing efficiency by the scale-up of wafer size have been rapidly

rising, which is largely due to the rapid expansion of the nitride semiconductor industry.[22] Therefore, understanding of the stress evolution associated with GaN growth and endeavor for potential wafer bowing reduction will be indispensable. Many previous studies have attempted to reduce stress and wafer bowing in GaN layer. Recently, Ryu et al.[23] and Huang et al.[24] achieved a reduction in wafer bowing by using a patterning process. Also, Aida et al.[20] used an internally focused laser process to treat the substrate and Sakai et al.[25] inserted superlattice interlayers to reduce the stress. However, these structures required many complicated processes, which were not efficient in reducing wafer bowing.

The goal in our experiment is growth of semi-insulating GaN layer for HEMT structure with less wafer bow which are main problems of GaN on sapphire. We will propose growth method by using new low temperature (LT) buffer layer for GaN on sapphire in this chapter.

4.2. Experimental procedure

GaN layers were grown on 430-μm-thick c-plane sapphire substrates by a MOCVD system (Thomas Swan 6x2 inch close-coupled showerhead reactor) using TMGa, TMAl and ammonia as precursors for Ga, Al and N, respectively. Prior to the GaN growth, two inch sapphire substrates were thermally cleaned in hydrogen ambient at 1100 °C for 10 min. Subsequently, the reactor temperature was decreased to 570 °C to grow a LT GaN layer under 200 Torr. After the growth of the 30-nm-thick LT GaN, the reactor temperature was ramped up to 1040 °C under 300 Torr through two different procedures. For sample A, during the temperature ramp-up process, TMGa source of a 3.5 μmol/s, which is the TMGa flow rate for the growth of the LT GaN layer, were flowed into the reactor together with ammonia gas. On the other hand, for sample B only ammonia gas was flowed without TMGa source; this is the conventional temperature ramp-up process for the GaN growth on sapphire. The temperature ramp-up and the stabilization times were kept constant at 300 s and 210 s, respectively, for all the growth experiments. Then, high temperature (HT) GaN layers were grown at 1040 °C under 300 Torr for both samples. The growth sequence is shown in Fig. 4.1. The total thickness of both samples is 1.5 μm. For investigation of the effect the growth method, TMGa flow rates during the temperature ramp-up and the thickness of LT GaN were varied to investigate their effects on wafer bowing reduction.

HEMT structures of a 15-nm-thick $Al_{0.25}Ga_{0.75}N$ layer were grown on both samples, and 2 nm GaN cap layer was sequentially grown. The Ohmic

contacts were made by evaporating Ti/Al/Ni/Au (15/120/40/50 nm) and annealing in nitrogen ambient at 850 ^{o}C for 30 s. Ni/Au (30/80 nm) were evaporated for the Schottky contacts. Hall measurement was made to determine the sheet carrier concentration and electron mobility of the 2DEG. C-V measurement for depth profiles of carrier concentration was made. Then, HEMT devices using sample A were fabricated with a 2-μm x 100-μm gate. The DC performance and off-state breakdown voltage were measured by using a microcontact technique with an HP4156C parameter analyzer and a STI curve tracer 5000E.

The surface morphology of the GaN layers was investigated using a Park Systems XE-100 AFM. To explore the concentration of impurities in the samples, a CAMECA IMS-6f Magnetic Sector secondary ion mass spectrometry (SIMS) was used. The structural characteristics of the GaN layers were investigated using a Hitachi S-4800 field emission SEM and a JEOL JEM-2100F TEM. The cross-sectional TEM samples were prepared by FIB using a FEI Quanta 3D FIB machine with double Pt coating. The magnitude of wafer bowing was estimated by an optical method using a Frontier Semiconductor FSM 500 TC before and after GaN growth. The crystalline quality of the epitaxial layers was analyzed by XRD using a PANalytical X'pert Pro X-ray diffractometer and by cathodoluminescence (CL) measurement using a Gatan MonoCL4. The residual stress was evaluated by photoluminescence (PL) measurement (Dongwoo Optron micro-PL) at low temperature using a 325 nm He-Cd laser.

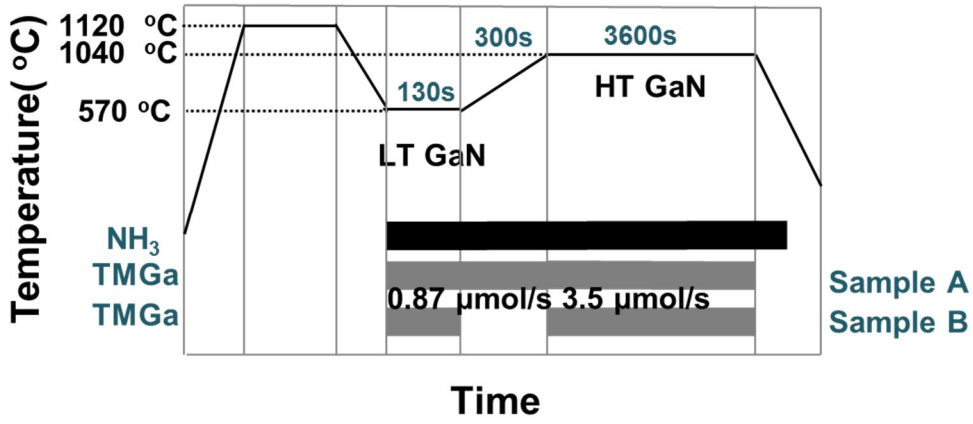

Figure 4.1 Schematic growth procedure of sample A and B.

4.3. Results and discussion

4.3.1 Semi-insulating characteristics

CV measurement was conducted to confirm the carrier concentration with the depth of the samples. The Ohmic and Schottky contact was evaporated on the HEMT structure of sample A and B. The carrier depth profiles could be calculated with the result of CV measurement as follows.

$$N_D = -\frac{C^3}{q\varepsilon_s\varepsilon_0 A^2 \frac{dC}{dV}} = \frac{2}{q\varepsilon_s\varepsilon_0 A^2 \frac{d\frac{1}{C^2}}{dV}} \quad [4\text{-}1]$$

$$C = \frac{\varepsilon_s\varepsilon_0 A}{W} \leftrightarrow W = \frac{\varepsilon_s\varepsilon_0 A}{C} \quad [4\text{-}2]$$

Figure 4.2 shows the depth profiles of carrier concentration in the HEMT structures. The samples reveal a 2DEG at the AlGaN/GaN interface but different profiles at the GaN/sapphire interface. Sample B shows an increase of the carrier concentration at the interface, indicating that a buried charge layer, a degenerate layer, exists at the interface.[14] The degenerate layer is expected to deteriorate the characteristics of HEMT device such as pinch-off and leakage current. Therefore, sample B, or the conventionally grown GaN layer, does not seem to be suitable for HEMT devices. On the other hand, sample A, grown by the new scheme, does not reveal an increase of the carrier concentration at the interface, implying that no degenerate layer exists in sample A.

The sheet resistance of the samples was measured using a dark current-voltage (I-V) transmission line model (TLM) technique. The TLM patterns

consisted of a set of 350 x 1000 μm^2 pads with spaces in 15 to 60-μm range. For the measurement, a thin $Al_{0.25}Ga_{0.75}N$ layer was grown on the samples, which induces the 2DEG insuring Ohmic contact.[7] After the Ohmic metallization and annealing, the AlGaN layer between the contacts was etched off using reactive-ion etching. The metal contacts act as masks, preserving the AlGaN layer under the contacts, allowing for improved Ohmic contacts to the semi-insulating GaN layer.[26] The sample scheme is shown in Fig. 4.3(a). The linear I-V curve was measured for both samples, as shown in Fig. 4.3(b) and (c), showing good Ohmic contact. The sheet resistances were obtained from the slope in the resistance-contact separation graphs (Fig. 4.4). The sheet resistance of sample A was calculated to be 1.02 x 10^9 Ωsq^{-1}. On the other hand, sample B exhibited a low sheet resistance of 3.9 x 10^3 Ωsq^{-1}, resulting from the leaky degenerate layer near the interface.[16] The buffer breakdown voltage was measured to confirm the leakage level of the samples with an ohmic contact spacing of 40 μm spacing. As shown in Fig. 4.5, the buffer breakdown voltage for sample A was 1390 V, which is promising for nitride HEMT device. Also, the leakage current of sample A was found to be as low as about 10^{-8} A at 100 V. On the other hand, the buffer breakdown voltage could not be measured for sample B due to the leaky property of the layer. These results imply that the new scheme to eliminate the degenerate layer is effective to obtain a semi-insulating GaN layer.

Figure 4.6 shows the SIMS profiles of oxygen, carbon, and hydrogen. In the profiles, the Ga intensity is observed to keep a constant value for the entire sputtering depth. Oxygen is present in high concentration at the interfacial region between GaN and sapphire substrate. Its profile, including the thickness and the concentration, is similar for both samples, regardless of

different growth procedures. It implies the high oxygen concentrations at the interfacial region were caused by thermal etching and/or diffusion from the sapphire substrate.[6] It is well known that when oxygen is incorporated in GaN layer, oxygen in N-site (O_N), a source of shallow donors with activation energy of 33.2 meV in GaN, is stable.[27] O_N is difficult to be formed in other regions of the film away from the interface because of limited diffusion, resulting in the limited thickness of the high oxygen concentration, generating a highly conducting channel near the sapphire substrate. Carbon also exists in high concentration at the interfacial region for both samples as shown in Fig. 4.6. It is generally known that carbon in GaN originates from TMGa .[28]

$$\boldsymbol{Ga(CH_3)_3 \rightarrow (3-x)CH_3 + Ga(CH_3)_x} \quad [4\text{-}3]$$

$$\boldsymbol{Ga(CH_3)_x \rightarrow (Ga-CH_y) + H_z} \quad [4\text{-}4]$$

$$\boldsymbol{(Ga-CH_y) + H_k \rightarrow Ga + CH_4} \quad [4\text{-}5]$$

During the GaN growth at low temperature, the TMGa molecule may be partially dissociated into dimethylgallium or monomethylgallium in the boundary layer above the growth surface like eq. [4-3].[29] If they do not desorb immediately, hydrogen is decomposed from the methyl group by breaking the C-H bond, inducing the incorporation of carbon into GaN surface as Ga-C bonds like eq. [4-4].[28] The carbon atoms could be desorbed from the GaN layer as methane (CH_4) formed by hydrogenation process in which hydrogen generated from ammonia reacts with carbon in the surface, reducing carbon concentration in the layer like eq. [4-5].[30] Therefore, the

carbon concentration is sensitive to the temperature and the ammonia flow rate, and GaN layer grown at low temperature is expected to contain high concentration of carbon.

Whereas the oxygen concentration profiles are similar for both samples, the carbon concentration profiles at interfacial region are found somewhat different. The carbon concentration in sample A (3 x 10^{19} cm^{-3}) is five times higher than that of sample B (6 x 10^{18} cm^{-3}). Also, the thickness of high carbon concentration in sample A, which is about 150 nm from the sapphire substrate, is 100 nm thicker than that of sample B. When carbon is incorporated into GaN, it can substitute for a gallium site (C_{Ga}), a nitrogen site (C_N), or various interstitial sites (C_I).[31] It was found that C_N behaves as an acceptor in GaN with an ionization energy of approximately 0.2 eV [32] or 0.9 eV [33] above the valence band maximum, and C_{Ga} acts as a deep donor. Several theoretical studies reported a role of carbon in GaN in view of the relationship between the formation energy of C_N, C_{Ga} and C_I and the Fermi level of GaN. In GaN where the Fermi level is in the upper half of the band gap, carbon substitutes for N, acting as an acceptor.(see Fig. 4.7) Moreover, as the Fermi level shifts toward the middle of the band gap, GaN becomes semi-insulating due to self-compensation, *i.e.*, the carbon occupation of both N and Ga substitutional lattice sites.[31,33] We suppose that in the degenerate layer, carbon substitutes for N site, and the resultant deep acceptors, C_N, compensate the shallow donors, O_N. Therefore, the higher carbon concentration and the thicker layer with high carbon concentration could be responsible for the high resistivity characteristic at the interfacial region in sample A, as shown in Fig. 4.4. On the other hand, the increase of carrier concentration at the interfacial region for sample B could be attributed to the

insufficient compensation due to the less carbon concentration and/or the thinner layer of high concentration compared to those of sample A.

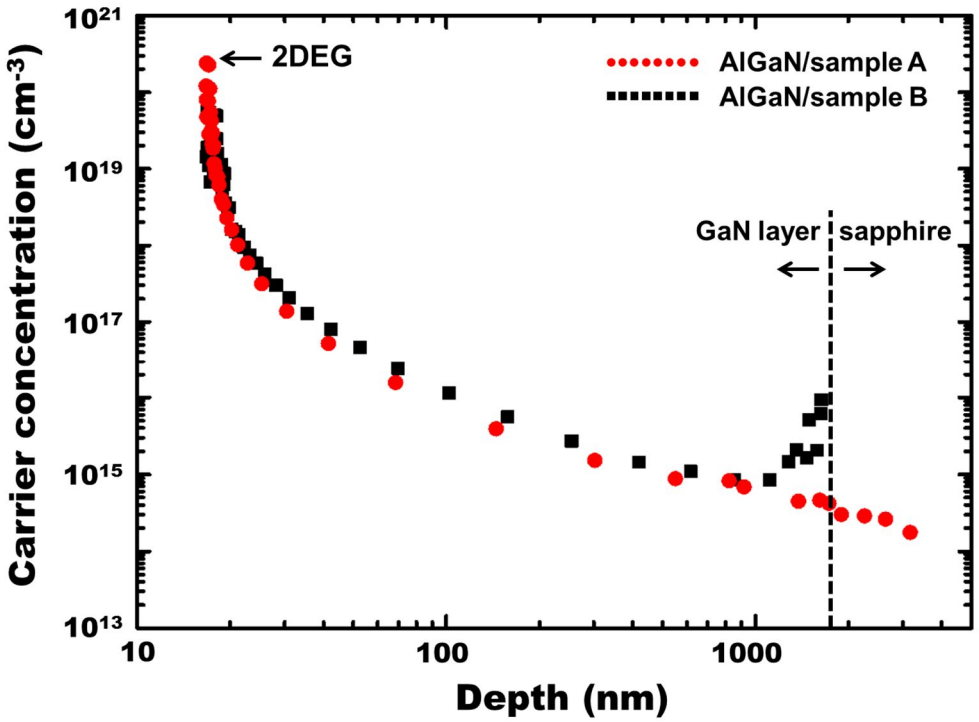

Figure 4.2 Carrier concentration depth profiles determined by C-V analysis for HEMT structures (15-nm-thick $Al_{0.25}Ga_{0.75}N$ layer) on sample A (red dots) and sample B (black squares).

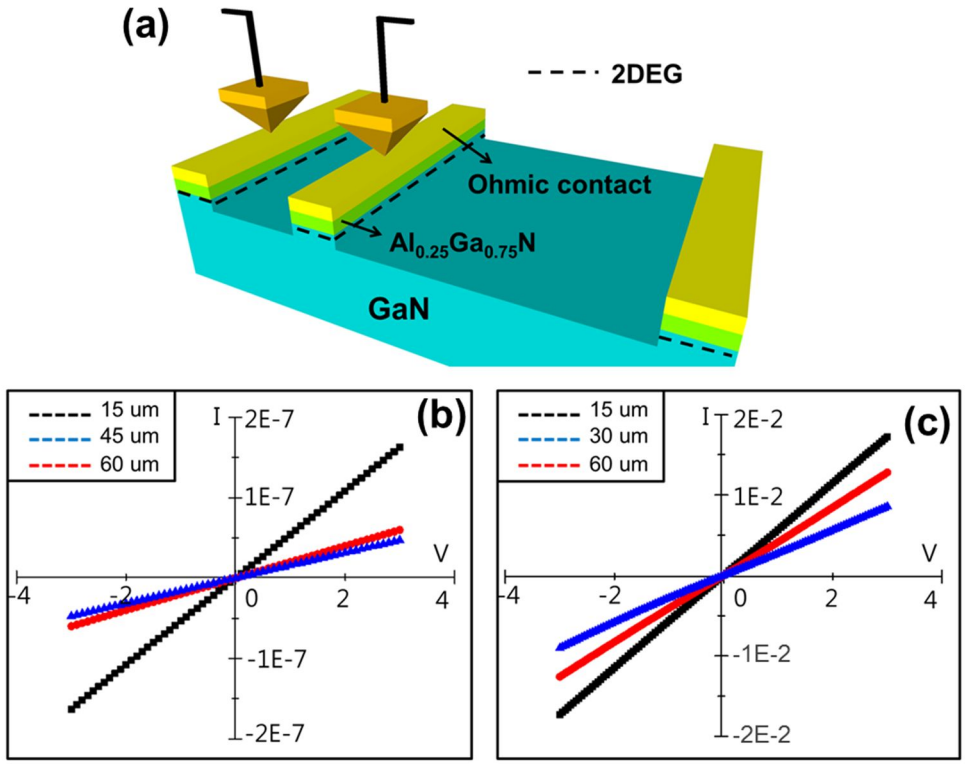

Figure 4.3 (a) a schematic diagram of the samples for the TLM measurement. IV characteristics from TLM method of (b) sample A and (c) sample B.

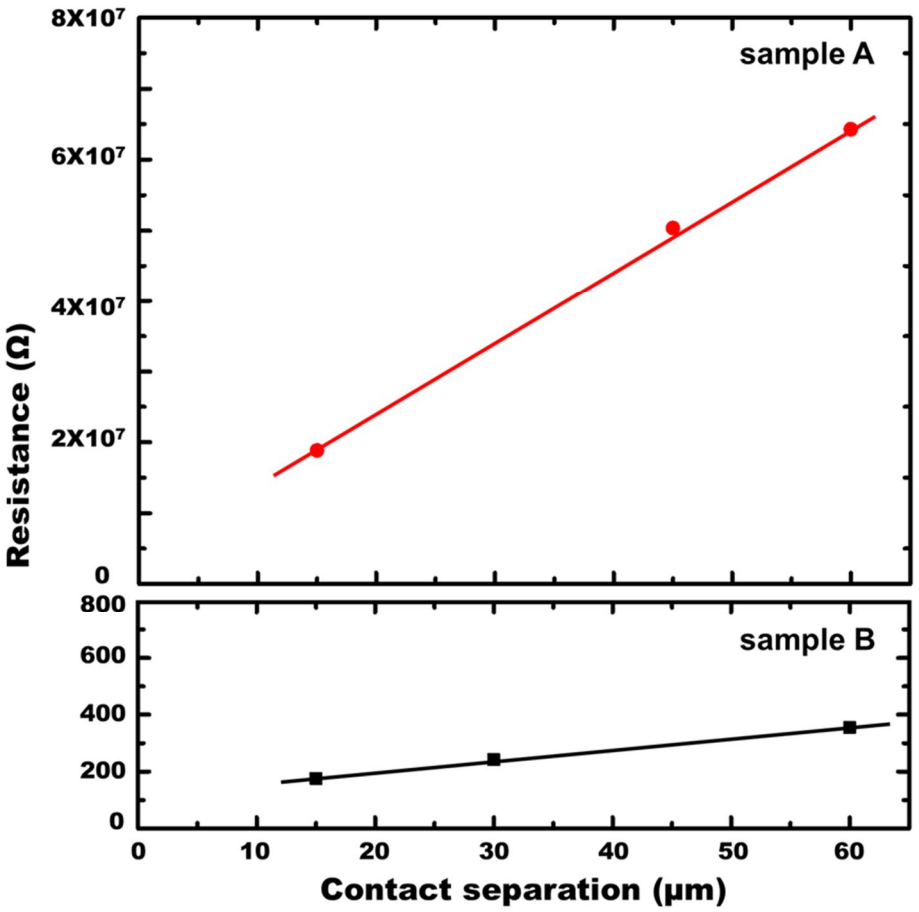

Figure 4.4 Plots of total contact to contact resistance as a function of contact separation in TLM measurement for sample A (red dots) and sample B (black squares). The slopes of the lines in sample A and sample B are 1.02 x 10^6 and 3.95 Ω/μm, respectively. The inset illustrates a schematic diagram of the samples for the TLM measurement.

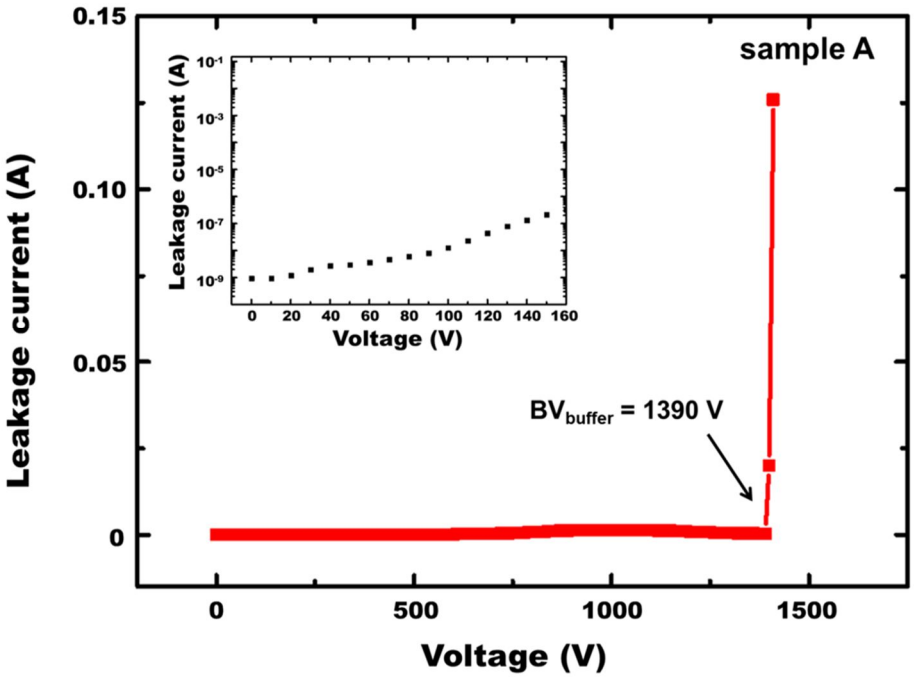

Figure 4.5 Buffer breakdown characteristics of the HEMT on sample A. The distance between contacts is 40 μm. The inset shows the enlarged view of the same data in logarithm scale.

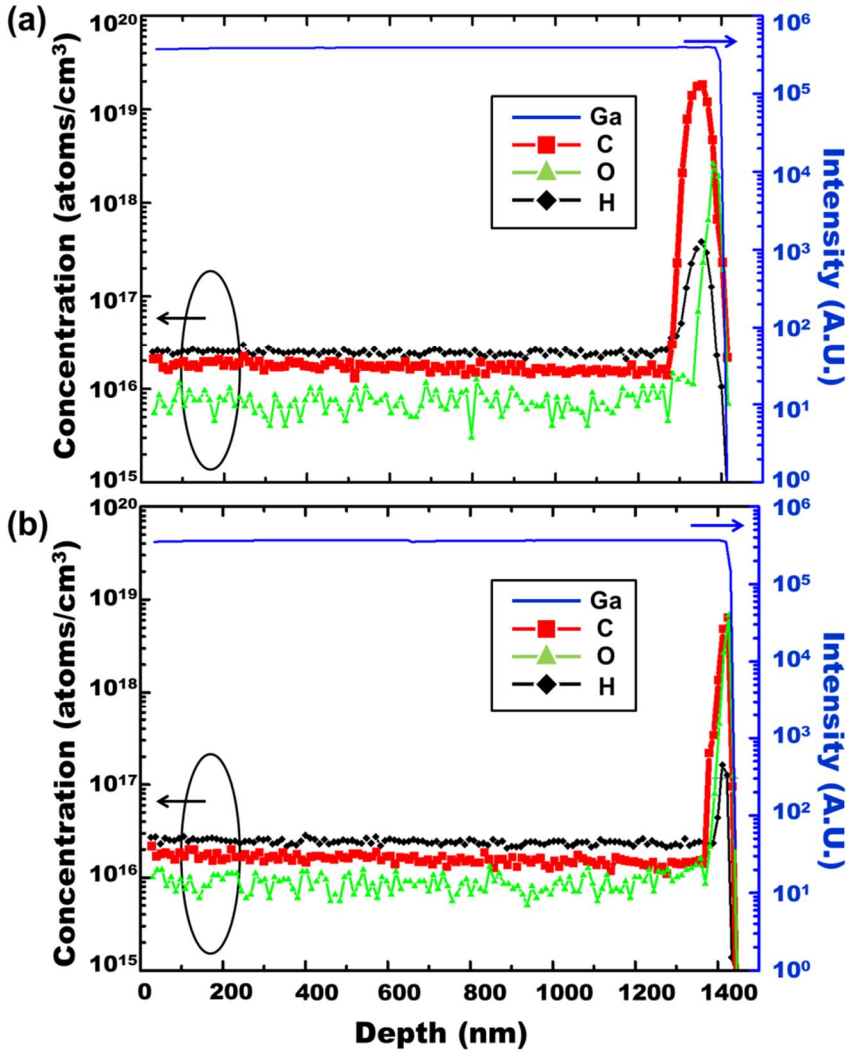

Figure 4.6 SIMS depth profiles of carbon (C), oxygen (O) and hydrogen (H) impurities for (a) sample A and (b) sample B.

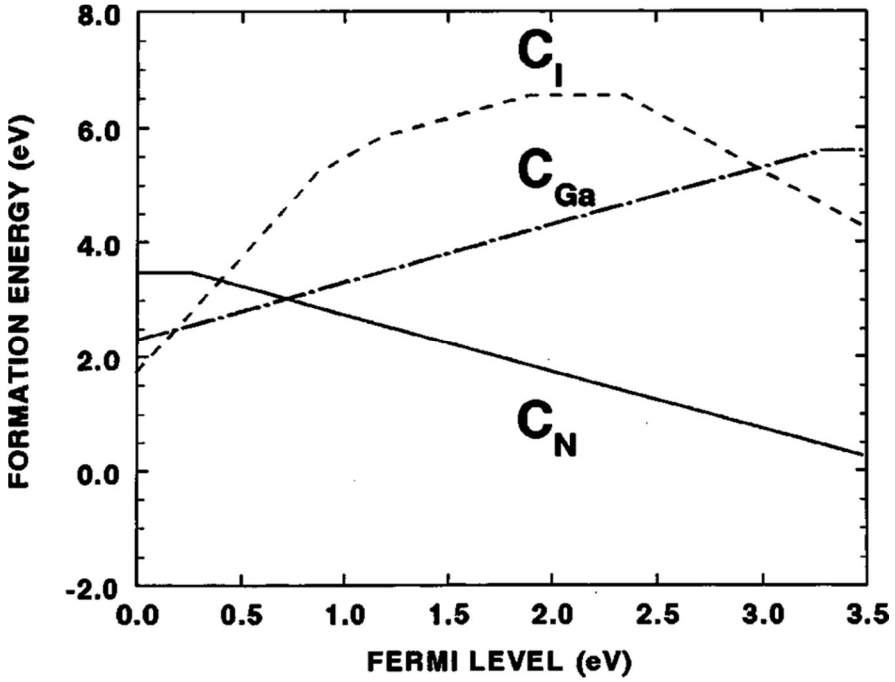

Figure 4.7 Formation energies of C_I , C_N, and C_{Ga} as a function of Fermi-level position in the GaN band gap calculated by density-functional theory for the wurtzite structure. Null growth conditions (neither N nor Ga rich) were simulated here.[31]

4.3.2 Characteristic of less bowed GaN and crystal qualities

The actual wafer bowing of samples were measured by the laser scanning technique. The degree of wafer bowing in both samples was measured before and after GaN growth. The wafer bowing was 34 μm for sample B and 15 μm for sample A, resulting in over 50 % reduction in wafer bowing when new low temperature buffer layer was used in GaN on sapphire, as shown in Fig. 4.8. We speculated the reduction of stress, including different carbon concentration, is related to the different growth procedures, that is different low temperature buffer layer. To investigate the effect of buffer layer more specific, we varied the thickness of the LT GaN layer from 0 to 400 nm under the same condition (0.9 μmol/s TMGa flow rate during ramp-up and subsequent 1.4-μm-thick HT GaN growth – the method of sample A) and studied its effect on wafer bowing and crystal quality. The extent of wafer bowing reduction was found to not be sensitive to the thickness of the LT GaN layer, as shown in Fig. 4.9 (a). The XRD FWHMs are also not sensitive to that. Since the formation and the quality of seed GaN deposited during the temperature ramp-up process can affect the crystal quality of HT GaN as well as the extent of wafer bowing, we varied the TMGa flow rate from 0.2 to 3.5 μmol/s. The thicknesses of LT (60 nm) and HT (1.4 μm) GaN was kept the same for all samples. Figure 4.9 (b) shows the extent of wafer bowing and XRD full widths at half maximum (FWHM) of (0002) and $(10\bar{1}2)$ reflection of the samples. The extent of wafer bowing was found to be related to the TMGa flow rate during the temperature ramp-up process. XRD FWHM of (0002) and $(10\bar{1}2)$ reflections varied from 344 to 592 and from 683 to 2010 arcsec with TMGa flow rate, indicating that the

crystal qualities of the less bowed GaN layer were poorer than the conventional GaN layer with 330 and 450 arcsec for (0002) and ($10\bar{1}2$) reflection, respectively. As shown in the 10K-PL spectra of Fig. 4.10, red shift of GaN band edge peak position was observed according to the TMGa flow during temperature ramp-up process. The PL result also shows our growth method reduce the intrinsic compressive stress in the GaN on sapphire. According to the results, we speculate our growth method using new LT buffer layer is effective to reduce wafer bowing, and important factor in new LT buffer layer is the TMGa flow rate during temperature ramping up.

The structural observation was investigated by cross-sectional TEM image as shown in Fig. 4.11. In the TEM image, different microstructures are observed in sample A and B. The different structure is the part of LT buffer layer located at the interfacial region between sapphire and HT GaN. In sample A, nano-columnar buffer layer was observed at this region. The nano-columnar buffer layer is expected as a preserved columnar LT buffer GaN and the part of additional layer made during temperature ramp (More details will be explained in chapter 4.4.1. The thickness of nano-columnar buffer layer is about 150 nm, which is same with the thickness of region where high carbon concentration is detected in Fig. 4.6. Accordingly, we speculate the nano-columnar buffer layer contains lots of carbon, resulting in eliminating of the degenerate layer. In stress problem, it is thought that the preservation of nano-columnar microstructure in GaN layer was responsible for the reduction of wafer bowing. Many papers have reported that the a biaxial tensile stress is pronounced at grain boundaries of islands.[34,35] In the GaN layer with nano-columnar structure, the tensile stress developed at grain boundaries between nano-columnar structures[34] compensates for the

compressive stress developed in the HT GaN layer, resulting in reduced wafer bowing. In conclusion, less stressed semi-insulating GaN could be obtained due to the nano-columnar LT buffer layer. On the other hand, the nano-columnar buffer layer was not observed in sample B, GaN with conventional LT buffer layer. Accordingly, sample B does not reveal not only semi-insulating characteristic but also reduction of wafer bowing. The mechanism of our growth method and the formation of nano-columnar buffer layer, including carbon incorporation in the buffer layer, would be investigated in next chapter.

The surface morphology of the GaN layer is important for HEMT structure because the 2DEG channel is formed on top of the surface when AlGaN is grown on the GaN layer. To good channel property, degradation of GaN surface property has to be avoided. Plan-view CL images measured at 77K were investigated in order to compare the density of threading dislocation as shown in Fig. 4.12(a) and (b). Although, unfortunately, each sample had different XRD FWHM values in Fig. 4.9, the threading dislocation densities in CL images were observed to be similar at ~low 10^8 cm^{-2}. In the non-contact AFM measurement as shown in Fig. 4.12(c) and (d), the samples show a similar surface morphology. Also, the threading dislocation density obtained from the number of dark spots in the AFM images was kept as low as $5x10^8$ cm^{-2}, and the root mean square (RMS) roughness was measured to be in the range of 0.3~0.4 nm. Further analysis of the crystal quality of these layers are currently under way; however, we hypothesize that the poor XRD FWHM was due to the poor crystal quality of the nano-columnar microstructure and the crystal quality of HT GaN itself with a nano-columnar microstructure (sample A) was similar to that of the

conventional GaN layer (sample B). Therefore, the new LT buffer layer for GaN on sapphire does not degrade the crystal quality of HT GaN and produce an acceptable semi-insulating GaN layer with less bowing.

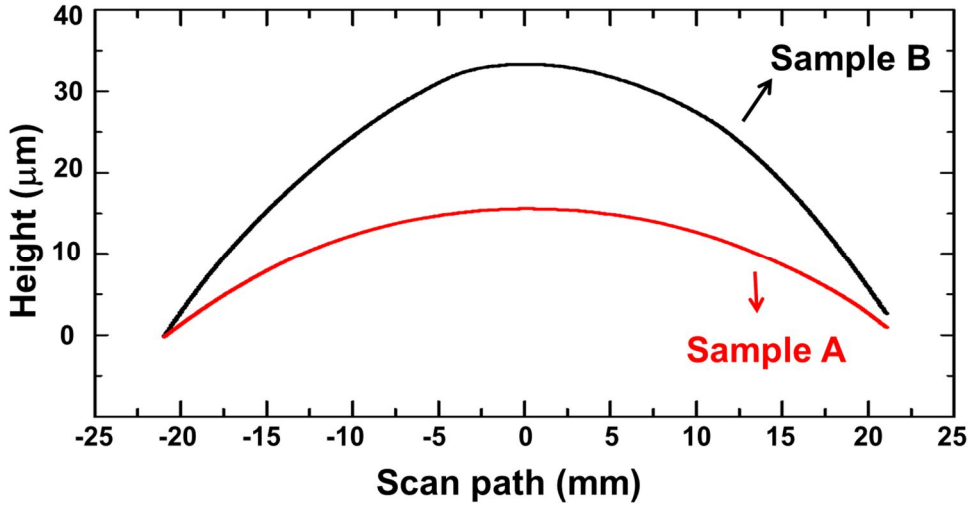

Figure 4.8 Scan profiles of sample A (red line) and sample B (black line). The extent of wafer bowing was 15 μm (red line) and 34 μm (black line).

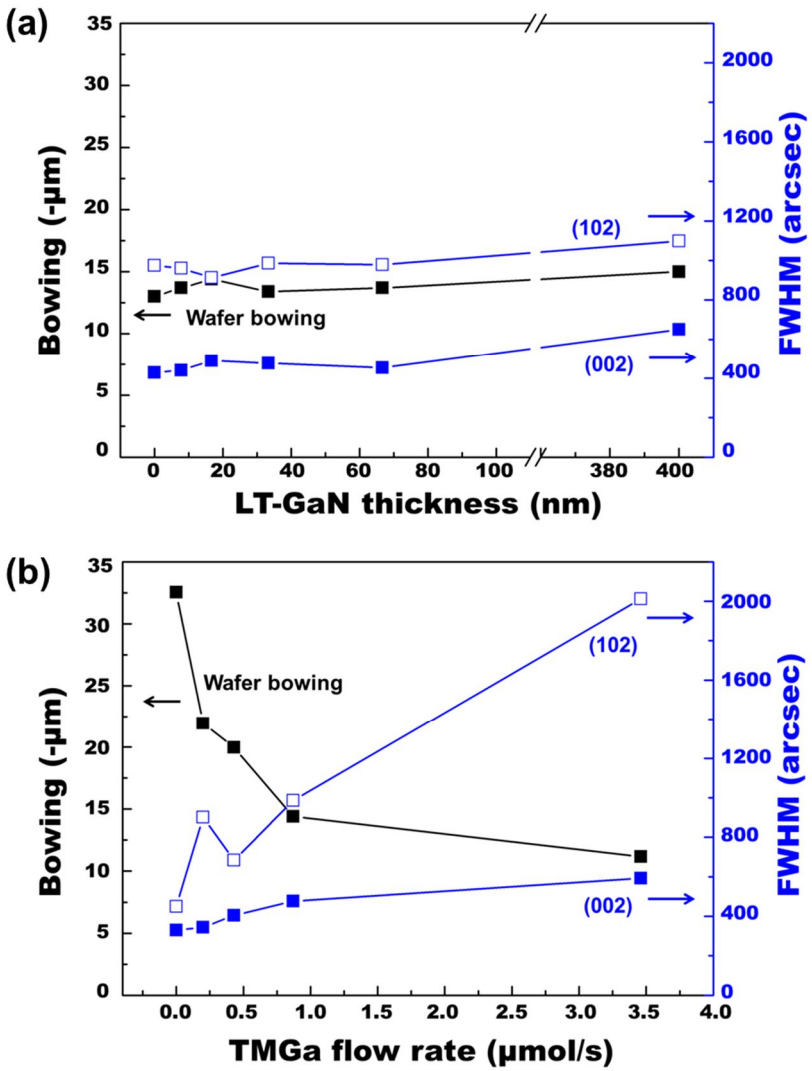

Figure 4.9 (a) The extent of wafer bowing (left, black) and XRD FWHM (right, blue) at various LT GaN thicknesses under the same TMGa flow rate during the temperature ramp-up process. (b) The extent of wafer bowing (left, black) and XRD FWHM (right, blue) at various TMGa flow rates during the temperature ramp-up at a fixed LT GaN thickness of 60 nm.

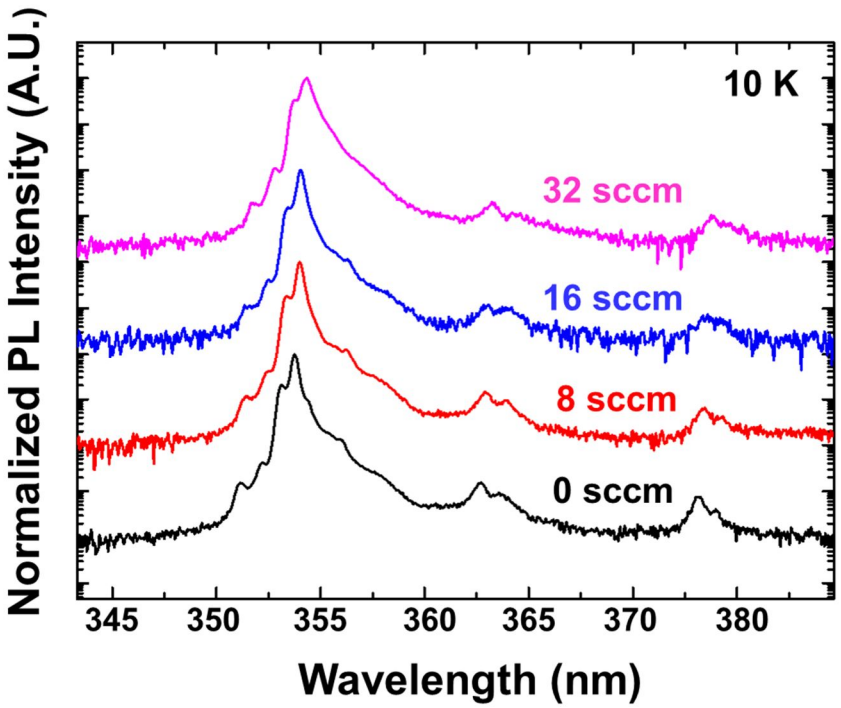

Figure 4.10 10K PL spectra of GaN layer with various TMGa flow rate during the temperature ramp-up (the samples are same with Fig, 5.9(b)).

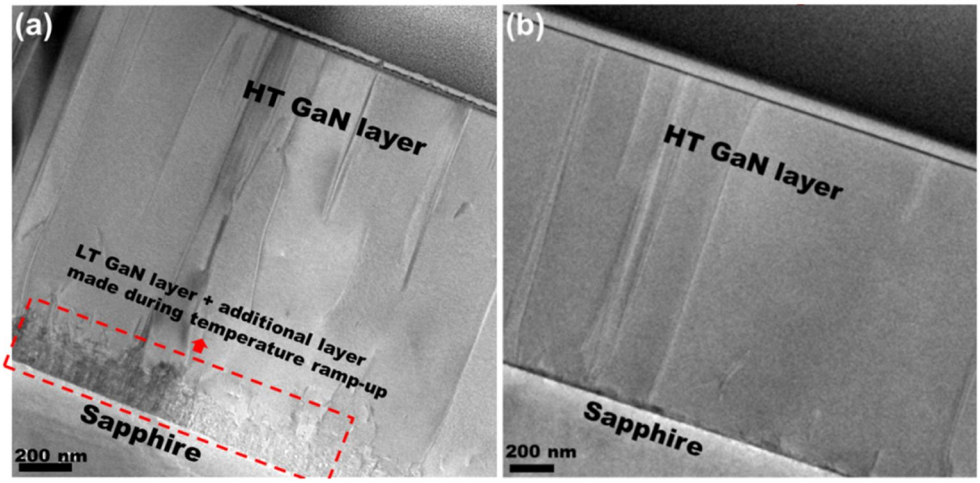

Figure 4.11 Crosse sectional TEM images of (a) sample A and (b) sample B.

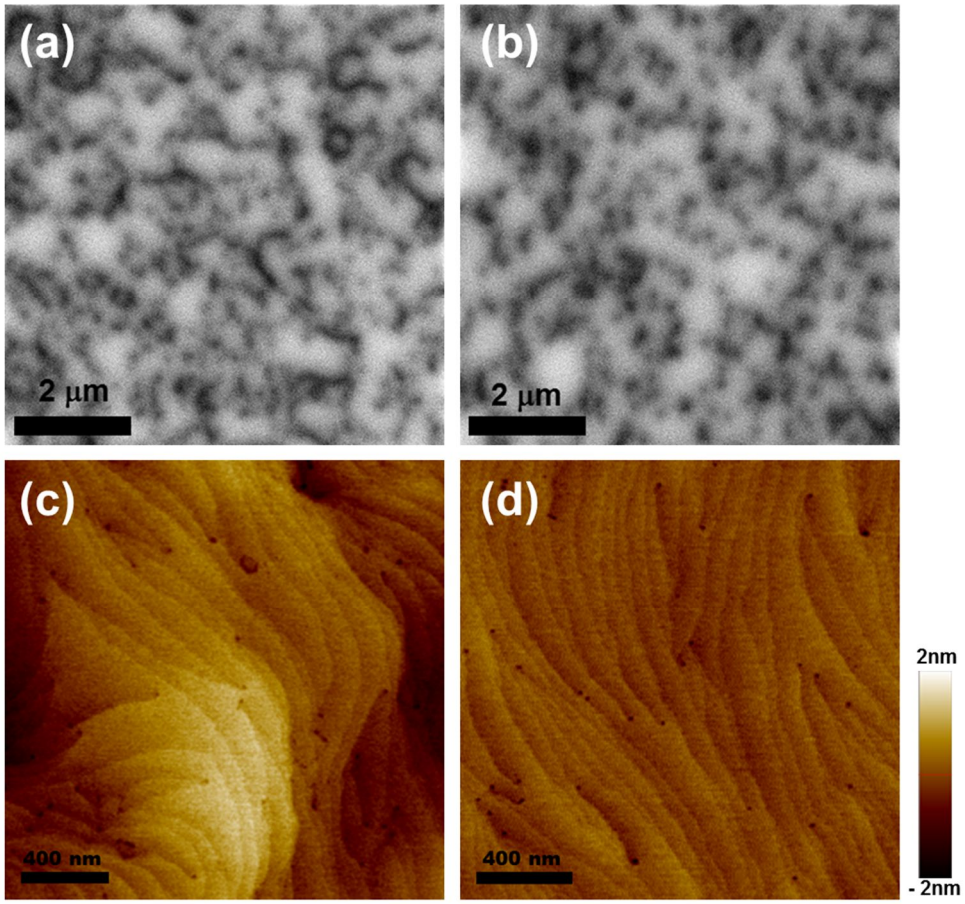

Figure 4.12 8 x 8 μm^2 Plan-view CL images of (a) sample A and (b) sample B. 2 x 2 μm^2 topological AFM images of (c) sample A and (d) sample B.

4.4. Investigation of growth mechanism and evaluation of HEMT device

4.4.1 Investigation of growth mechanism and new low temperature buffer layer

To investigate the growth mechanism of the experiment, the 800-nm-thick LT GaN layer was grown on a sapphire substrate at 570 ^{o}C for an hour. When the layer was examined by SEM, a nano-columnar microstructure was clearly observed, as shown in Fig. 4.13(a) and (b). At low temperatures, the density of GaN nuclei is very large and the adatom surface diffusion is very limited, resulting in a nano-columnar microstructure with numerous misoriented grains.[36] The nano-columnar microstructure was examined by cross sectional TEM as in Fig. 4.13(c). Note that the saw-toothed surface feature was clearly visible, suggesting that the average nano-columnar diameter was ~60 nm. However, the nano-columns were found to be highly defective and the boundaries between nano-columns were poorly defined. The thin white layer above the nano-columns was coated with Pt for cross sectional TEM sample preparation by FIB. XRD ϕ-scan was carried out to determine the in-plane orientation of the nano-columnar microstructure. However, six-fold peaks were not observed from the LT GaN layer, suggesting that LT GaN was not single crystal as shown in Fig 4.13(d).

After the growth of the LT GaN layer, the temperature was ramped up to HT around 1040 ^{o}C for GaN growth under an NH_3 atmosphere. During the temperature ramp-up from 570 ^{o}C to 1040 ^{o}C for 300 s, 3.5 μmol/s flow of

TMGa was used for sample I, and the TMGa source was switched off for sample II. The two samples were cooled to room temperature and analyzed by SEM, cross sectional TEM and XRD. Plan-view SEM images of Fig. 4.14(a) and (b) show that the surface morphologies of the two samples were quite different. GaN nano-columnar structures were observed in both samples even after heat treatment at 1040 ^{o}C. However, in Sample I, the nano-columns became partially coalesced. On the other hand, in sample II, some nano-columns were covered by large facetted islands. TEM images of Fig. 4.15(a) and (b) more clearly show the structural difference in both samples. For Sample I, the decomposition of nano-columnar GaN was suppressed since TMGa was introduced during the temperature ramp-up. Instead, the growth of an additional 220 nm GaN was made on top of the nano-columnar LT GaN. A close-up view of Fig. 4.15(a) shows that grain size increased through recrystallization. The thickness of the recrystallized GaN was around 110 nm. These results indicate that considerable grain growth occurred during the temperature ramp-up from 570 to 1040 ^{o}C. On the other hand, in sample II, some parts of the LT nano-columnar GaN were decomposed, forming facetted, inverted pyramidal etch pits. It is worth noting that highly perfect GaN pyramids (both truncated and untruncated) were formed on top of the LT nano-columnar GaN adjacent to etch pits. The decomposition of GaN provided a local Ga flux to adjacent nucleation sites for the growth of highly perfect GaN seed crystals. Meanwhile, the XRD ϕ-scan shows clear six-fold peaks as shown in Fig. 4.15(c), suggesting that significant recrystallization occurred during the temperature ramp-up process in Sample I, and the layer would be able to play a role of the buffer layer for GaN epi-layer.

It is clear that the microstructure of the two samples produced a very different microstructure when HT GaN was grown on both samples. 1.4-μm-thick HT GaN layers were grown at 1040 ^{o}C, and the microstructures of both samples were examined by cross sectional TEM. Interestingly, the 800 nm nano-columnar LT GaN completely disappeared for Sample II, as shown in Fig. 4.16(b). It was hypothesized that a significant gas-phase and/or solid-phase mass transport process occurred during the HT GaN growth, which would have led to complete disappearance of the nano-columnar LT GaN. The insufficient supply of GaN towards the etch pits during HT GaN growth lead to the formation of inverted triangular cavities, as shown in Fig. 4.16(b). On the other hand, the nano-columnar LT GaN buffer layer was preserved in Sample I, as shown in Fig. 4.16(a). It is believed that the 110 nm thick recrystallized GaN shown in the inset of Fig. 4.15(a) provided the template for HT GaN growth. A schematic diagram for the two different growth mechanisms is shown in Fig. 4.17. By introducing TMGa during the ramp-up from LT to HT, the nano-columnar microstructure was preserved throughout the growth process, resulting in tensile stress. The TMGa flow rate during the temperature ramp-up would determine the degree of preserving the nano-columnar structure of LT GaN, resulting in Fig. 4.9 in chapter 4.3.2. According to the mechanism, wafer bowing reduction was observed in Sample A thanks to the preserved nano-columnar structure.

In the point of view of semi-insulating characteristic, the incorporation of carbon could be well explained. The difference between sample A and B is the different growth procedures, and we already confirmed that the carbon concentration is related with nano-columnar LT buffer layer in chapter 4.3.2. For sample B, during the temperature ramp-up process, only ammonia gas

flows and a part of the LT GaN layer was decomposed and re-deposited due to the high thermal energy and the supply of hydrogen and nitrogen from ammonia as shown in above paragraph. It seems that the incorporated carbon in the LT GaN was partially desorbed during the process, resulting in the less carbon concentration at the GaN/sapphire interfacial region in sample B. On the other hand, for sample A, the decomposition and re-deposition of LT GaN was suppressed during the temperature ramp-up since TMGa was introduced and instead, the additional GaN layer was grown as shown in above paragraph. Therefore, the incorporated carbon into the LT GaN layer could be maintained during the process. In addition, the GaN layer grown in the beginning of the temperature ramp-up, when the temperature is low, contains high carbon concentration as well, leading to the thicker GaN layer of the high carbon concentration. The sufficient incorporation of the carbon eliminated degenerate layer at the interfacial region, resulting in semi-insulating characteristic of sample A.

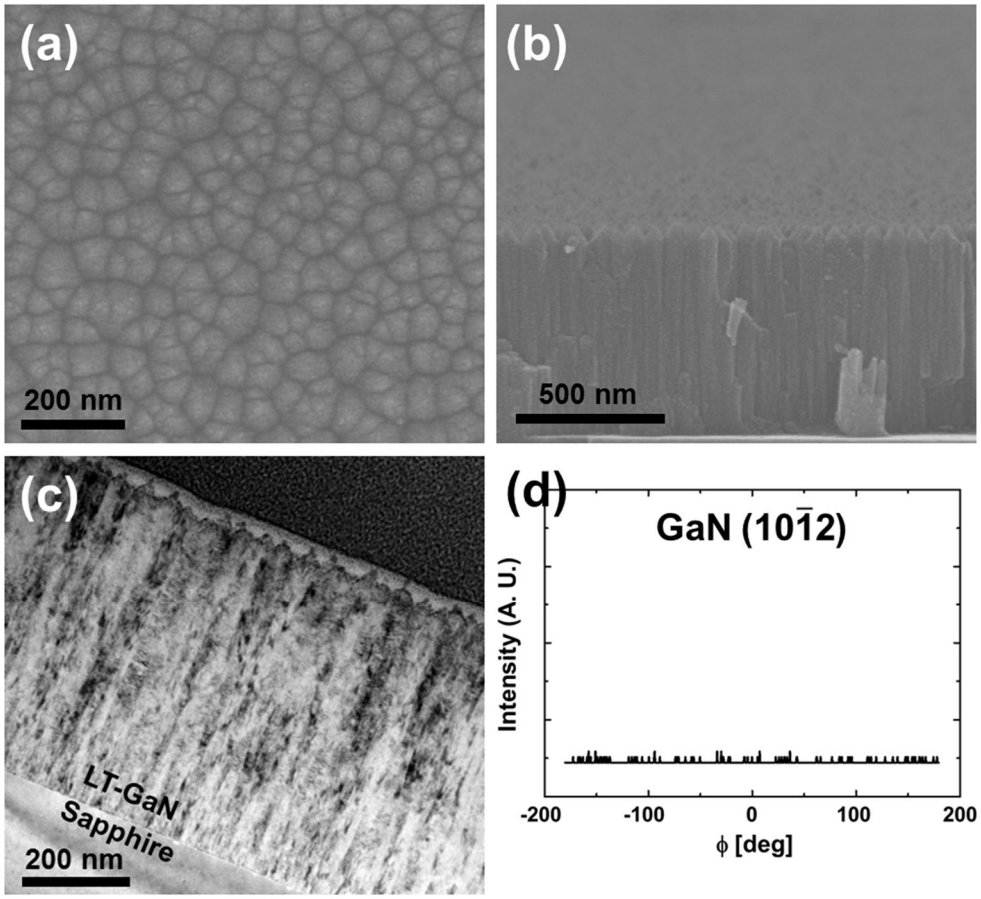

Figure 4.13 (a) Plan-view SEM image, (b) cross-sectional SEM image, (c) cross-sectional TEM image and (d) XRD ϕ-scan profiles for the $(10\bar{1}2)_{GaN}$ plane of the LT GaN buffer layer grown at 570 ^{o}C on a sapphire substrate.

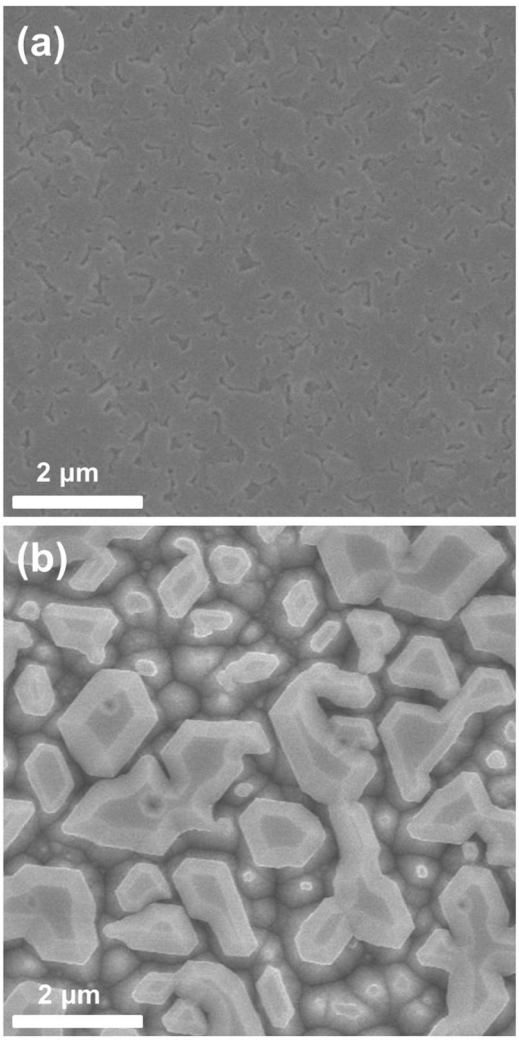

Figure 4.14 Plan-view SEM images of annealed LT GaN layers from 570 ^{o}C to 1040 ^{o}C: (a) sample I obtained with 3.5 mmolsec^{-1} TMGa flow during temperature ramp-up and (b) sample II obtained without TMGa flow during the temperature ramp-up.

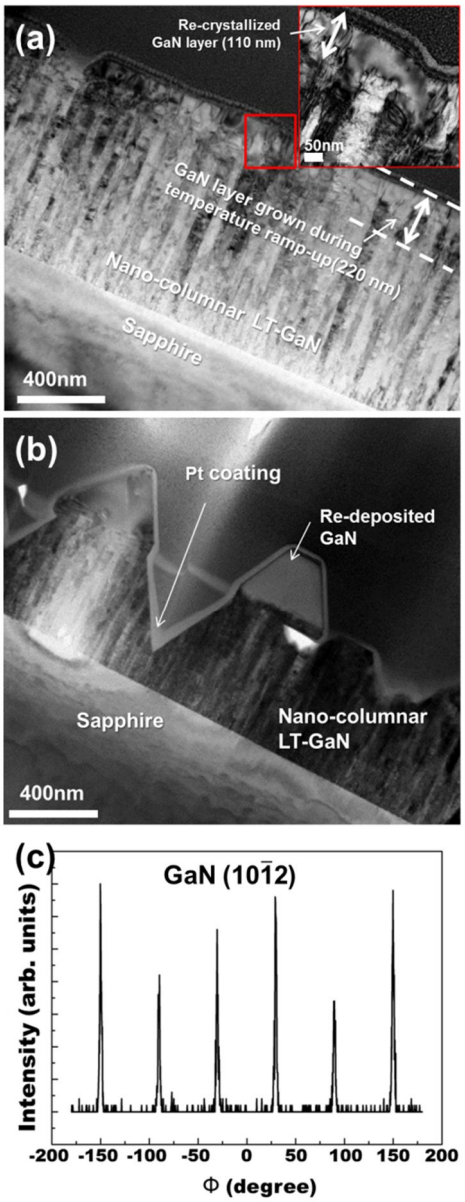

Figure 4.15 Cross-sectional TEM images of annealed LT GaN layers form 570 ^{o}C to 1040 ^{o}C: (a) sample I and (b) sample II. Inset: cross-sectional TEM image of the upper part of sample I (red line). (c) XRD ϕ-scan of sample I.

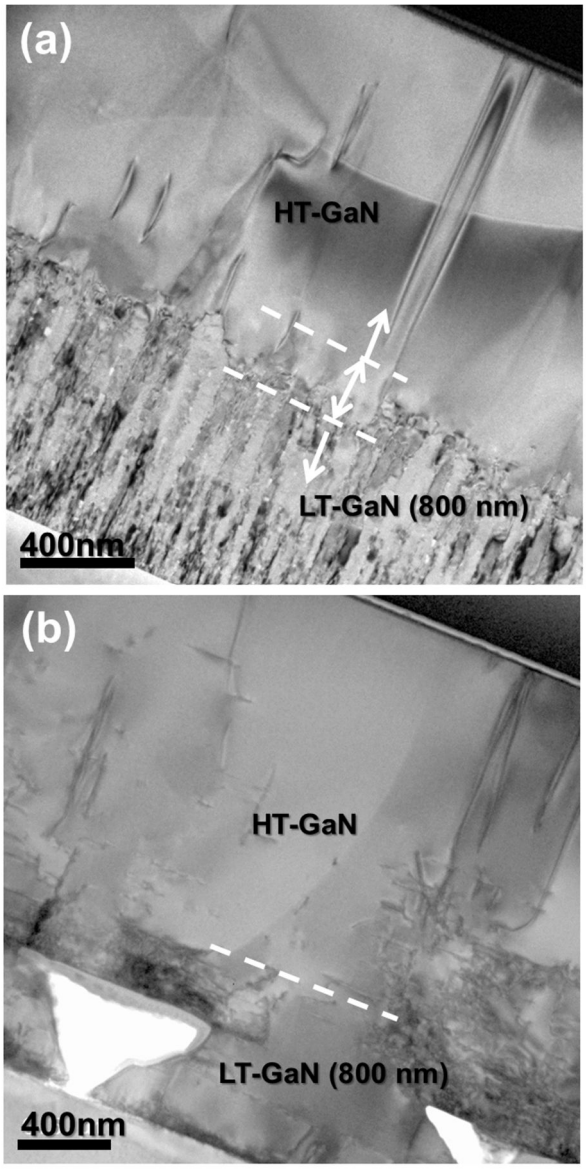

Figure 4.16 Cross sectional TEM image of HT GaN layer grown on (a) sample I and (b) sample II.

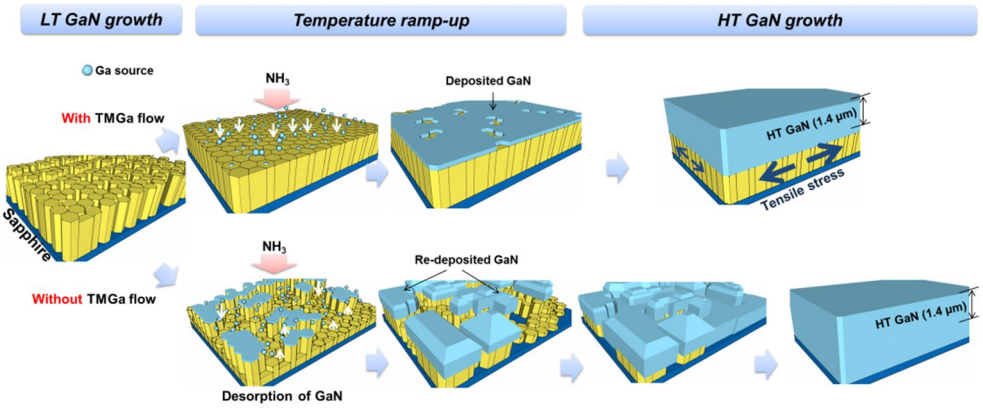

Figure 4.17 Schematic diagram showing the two growth mechanisms with and without TMGa flow during temperature ramp-up.

4.4.2 Evaluation of HEMT device

A HEMT structure of $Al_{0.25}Ga_{0.75}N$ was grown on sample A. The 2DEG electron concentration and mobility were measured to be 0.92 x 10^{13} cm^{-2} and 1300 cm^2/Vs, respectively, by Hall measurement. Then, the HEMT device was fabricated with a GaN cap layer, SiN_x passivation layer and Ohmic and Schottky contacts. Figure 4.18 shows the device schematic diagram with a 2-μm x 100-μm gate and a 20-μm source-drain spacing. Figure 4.19 shows the I_{DS}-V_{DS} characteristics of the device. The maximum gate voltage was 0 V and the gate voltage step was -0.5 V. Figure 4.19(a) and (b) shows the device had good pinch-off characteristics and I_{max} was 450 mA/mm at V_{GS} = 0 V with the the maximum transconductance of 150 $mSmm^{-1}$. Also, the breakdown voltage was found to be over 800 V, which is the compliance limit of the measurement system, under a gate voltage of -4 V. This result indicates that high quality semi-insulating GaN layer for high performance HEMT device could be obtained by the new growth scheme, leading high carbon incorporation eliminating the degenerate layer at the interfacial region.

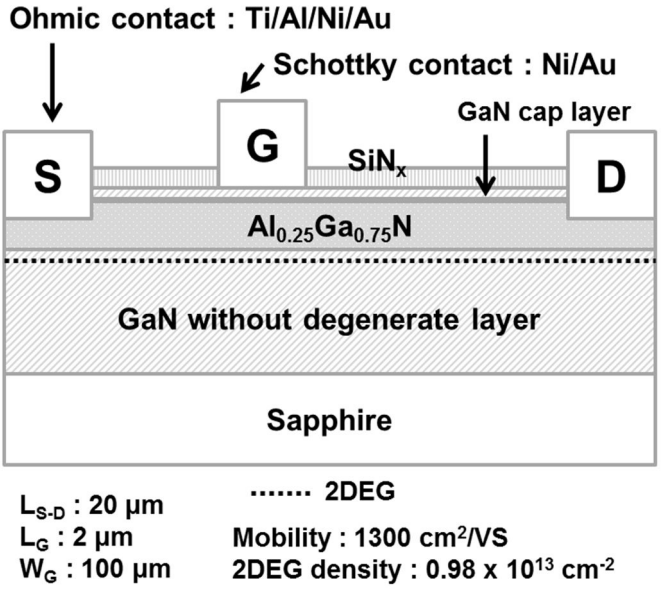

Figure 4.18 Schematic diagram showing the HEMT device fabricated with sample A.

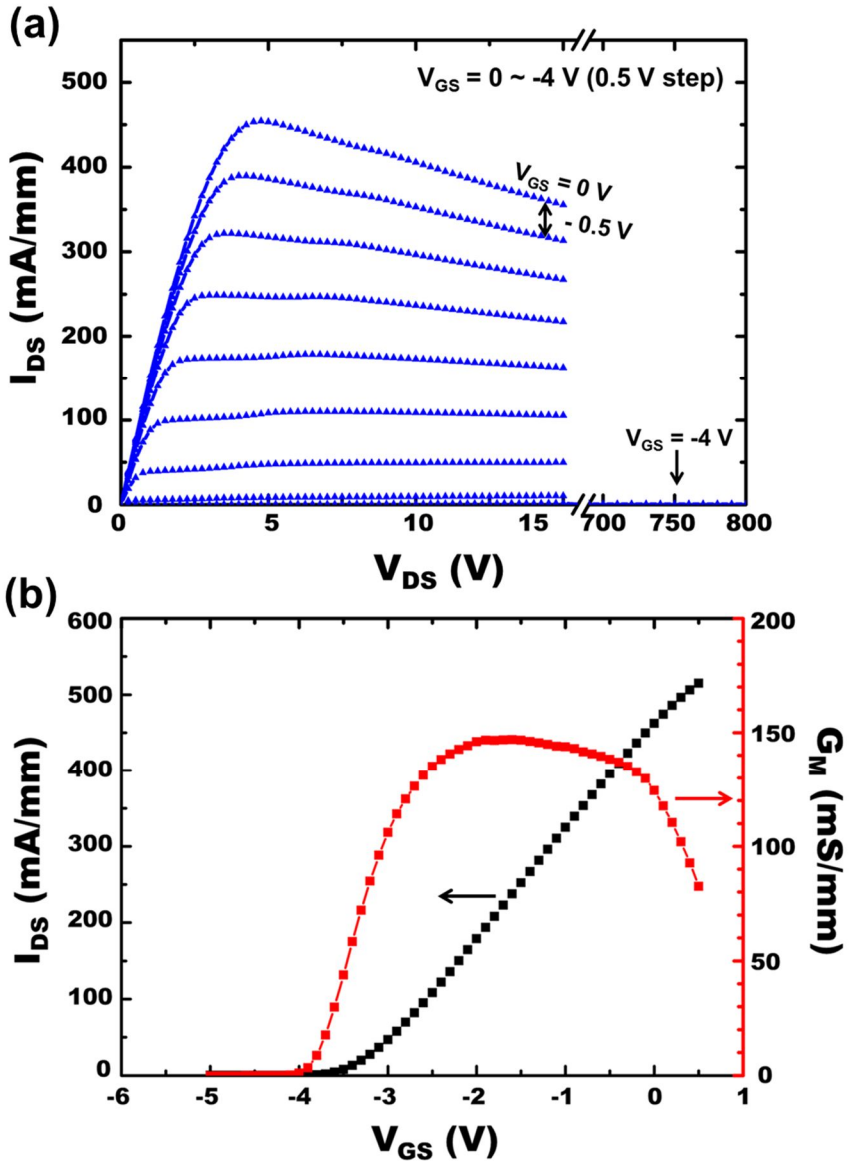

Figure 4.19 (a) DC I_{DS}-V_{DS} and (b) transfer characteristics of HEMT device on sample A.

4.5. Summary

A new LT buffer layer, nano-columnar LT buffer layer, for GaN on sapphire was developed to eliminate a degenerate layer at the GaN and sapphire substrate and reduce wafer bowing of the GaN on sapphire. We demonstrated that the introduction of TMGa during the temperature ramp-up from LT GaN to HT GaN preserved nano-columnar microstructure inducing tensile stress and high carbon concentration at the interfacial region. As a result, the induced tensile stress in nano-columnar LT buffer layer compensated the compressive stress in the GaN layer grown on the sapphire substrate, resulting in less wafer bowing. Also, the incorporated carbon in nano-columnar LT buffer layer formed C_N in the degenerate layer and compensated shallow donors such as O_N, resulting in the elimination of the degenerate layer, resulting in semi-insulating characteristic. It was confirmed that no noticeable degradation was detected as a result of the new scheme. Moreover, a HEMT device made on the sample grown by the new LT buffer showed good pinch-off characteristics and high off-state breakdown voltage over 800V at a gate voltage of -4 V, implying the new LT buffer layer is effective to grow GaN on sapphire substrate for HEMT device.

4.6. Bibliography

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Chapter 5. Conclusion

The new LT buffer layers for each substrate, Si and sapphire, were proposed to solve several problems such as leakage current, wafer bowing and MOCVD chamber condition leading to degraded properties of nitride electronic device.

Firstly, the problems in epitaxial growth of GaN on Si substrate were investigated when conventional AlN buffer layer was grown by same MOCVD system for the GaN growth. We confirmed MOCVD reactor circumstance related with previous GaN growth run, Ga memory effect, was significant for properties of GaN/AlN/Si structure. During thermal annealing process of Si substrate, small amount of Ga, from the MOCVD reactor, was incorporated in the Si substrate, resulting in rough surface. When AlN layer was grown, as a next step, on the Si substrate, the layer contained various densities of pits following the degree of rough surface in the Si substrate. Initial GaN nuclei densities were determined by the pit density in AlN, because the pit in AlN layer had a role of nucleation site for GaN. Accordingly, the final stress and crystal quality of GaN was affected by densities of the pit in AlN buffer layer. We concluded the conventional AlN buffer layer and GaN layer on Si was considerably sensitive to growth circumstance, so the alternative of the buffer layer was needed.

Accordingly, we proposed new AlN buffer layer deposited by DC magnetron sputtering at room temperature for GaN on Si substrate. The ex-situ buffer layer could be effective solution to avoid growth circumstance

problem in MOCVD reactor since the system does not include Ga. Moreover low growth temperature could prevent interdiffusion between Si-Al leading to leakage path. To align the AlN layer to (0002) plane normal to the Si substrate, the sputtering condition such as pressure, DC power and Ar/N_2 flow rate was investigated. We confirmed that the preferred orientation of sputtered AlN layer was related with the energy of arriving adatoms. Especially, the sputtering pressure was key factor to supply the high energy for adatoms. We succeed the obtaining of (0002) AlN layer by using the particular sputtering condition. However we confirmed that the alignment of (0002) orientation does not mean single crystal because alignment in out-of plane was not related with in-plane orientation alignment. For epitaxial growth of AlN, single crystalline AlN, on Si substrate by DC magnetron sputtering at room temperature, the pre-deposited Al process, deposition of thin Al layer before main AlN deposition, was developed. It was expected that the activation energy for epitaxial growth of AlN on Al interlayer became lower than it on Si substrate, resulting from smaller lattice mismatch between AlN and Al (6~8%) than between AlN and Si (19%). Moreover, the sufficient kinetic energy from the high DC power helped epitaxial growth of AlN even at the room temperature. Also, single crystalline GaN was successfully grown by MOCVD on the AlN buffer layer, which shows the new room temperature AlN buffer layer could be substituted for conventional AlN buffer layer grown at high temperature by MOCVD system.

Additionally, new LT buffer layer for sapphire substrate was proposed to solve problems of the GaN on sapphire which are low resistivity from the degenerate layer between GaN and sapphire substrate and convex wafer

bowing from the TEC difference between GaN and sapphire substrate. The LT buffer layer was fabricated as introduction of TMGa into the reactor together with ammonia during the temperature ramp-up after the growth of a LT GaN buffer layer. We demonstrated that the introduction of TMGa during the temperature ramp-up from LT GaN to HT GaN preserved nano-columnar microstructure inducing tensile stress and high carbon concentration at the interfacial region. As a result, the induced tensile stress in nano-columnar LT buffer layer compensated the compressive stress in the GaN layer grown on the sapphire substrate, resulting in less wafer bowing. Also, the incorporated carbon in nano-columnar LT buffer layer formed C_N in the degenerate layer and compensated shallow donors such as O_N, resulting in semi-insulating characteristic with elimination of the degenerate layer. It was confirmed that no noticeable degradation was detected as a result of the new scheme. Moreover, a HEMT device made on the sample with the new LT buffer showed good pinch-off characteristics and high off-state breakdown voltage over 800V at a gate voltage of -4 V, implying the new LT buffer layer was effective to grow GaN on sapphire substrate for HEMT device.

국 문 초 록

3 족 질화물 반도체는 HEMT 와 같은 전자소자의 응용가능성으로 인해 많은 연구가 진행되어 오고 있다. 3 족 질화물 반도체는 동종 기판 사용의 한계로 인하여 일반적으로 실리콘 기판이나 사파이어 기판과 같은 이종기판을 사용하여 에피텍셜 성장이 이루어 진다. 하지만 갈륨 (Ga) 원자 등의 3 족 원소들은 이종기판 위에서 안정적으로 붙어 있기 어렵기 때문에 균일한 박막을 얻는데 한계가 있었다. 버퍼층 (buffer layer)의 개발은 3 족 질화물 반도체와 기판 사이의 물리적 특성 차이로 발생하는 위와 같은 문제점들을 해결 해주었고 이로 인해 3 족 질화물 반도체에서 꼭 필요한 핵심 기술로 널리 이용 되고 있다. 하지만 여전히 누설전류 (leakage current), 기판 휨 (wafer bowing) 그리고 성장 환경의 영향과 같이 3 족 질화물 반도체의 특성을 저하 시키는 문제점들이 존재 하고 있다. 본 연구에서는 각 기판 위에 질화물 반도체를 성장함에 따라 발생하는 문제점들을 확인 하고, 이를 버퍼층을 이용해 해결 하고자 하였다.

우선 실리콘 기판 위 GaN 층 성장에서 일반적으로 사용 되는 AlN 버퍼층의 문제점에 대한 연구를 진행하였다. 대개 AlN 버퍼층과 GaN 층은 같은 유기금속화학기상증착 (MOCVD) 장비 내에서 성장 되기 때문에 남아 있는 갈륨이 AlN 버퍼층에 영향을

미치게 된다. 본 연구를 통해 유기금속화학기상증착 장비 내 에 남아 있는 극소량의 갈륨이 AlN 버퍼층의 표면상태에 영향을 끼치고, 이로 인해 그 위에 성장 되는 GaN 층의 결정성 및 응력에 부정적인 영향을 미치는 것을 확인 하였다. 이는 Si 기판 위 GaN 를 성장 할 때 마다 다른 결과가 나오는 등의 신뢰성 문제를 야기 시키며, 갈륨의 영향을 최소화 하려면 장비의 유지 보수 등에 많은 비용과 시간이 요구 되기 때문에 해결책이 필요 하다.

위 문제를 해결하고자 DC 마그테트론 스퍼터링 (magnetron sputtering) 장비를 이용하여 상온에서 증착 한 AlN 버퍼층을 개발 하였다. 이 새로운 AlN 버퍼층은 유기금속화학기상증착 장비로 성장 되는 것이 아니므로 갈륨 의 영향이 없을 뿐만 아니라, 상온에서 성장되기 때문에 알루미늄 (Al)-실리콘의 상호 확산으로 인한 누설전류 문제를 해결 할 수 있을 것으로 기대된다. DC 마그네트론 스퍼터링을 이용한 상온 AlN 층이 버퍼층으로서 역할 할 수 있도록, 우리는 실리콘 기판과 AlN 층 사이에 알루미늄 층을 넣어 AlN 의 에피텍셜 성장이 되도록 만들었다. 알루미늄 과 AlN 의 격자상수 차이 (6~8%)가 실리콘 과 AlN 의 격자상수 차이 (19%) 보다 작기 때문에, 알루미늄 층의 도입이 AlN 가 에피텍셜 성장이 되기 위한 활성화 에너지를 낮추는 효과를 만들어냈다. 더불어 높은 DC power 를 통해 충분한 운동에너지를 공급 함으로써 실리콘 기판 위 AlN 층의 에피텍셜 성장을 상온에서 성공 하였다.

유기금속화학기상증착 장비를 사용하여 위 AlN 층 위에 GaN 층을 성장 한 결과, 단결정의 GaN 층이 성장 하는 것을 확인 하였고, 이는 본 연구에서 개발한 DC 마그네트론 스퍼터링을 이용한 AlN 버퍼층이 현재 여러 문제점을 가지고 있는 기존의 AlN 버퍼층을 대체 할 수 있음을 보여준다. 추가적인 연구를 통해 이 버퍼층의 품질 향상을 위한 본 기술의 가능성을 보았다.

추가적으로 사파이어 기판 위 GaN 층이 갖고 있는 누설전류 문제 및 기판 휨 현상을 해결하기 위한 새로운 저온 버퍼층을 개발 하였다. 일반적으로 사파이어 기판 위 저온 GaN 버퍼층은 저온에서 GaN 버퍼층을 성장 한 후 주 GaN 층을 성장 하기 위해 고온으로 올리는 동안 암모니아 가스만 흘려준다. 반면 본 연구에서는 GaN 버퍼층을 저온에서 성장 한 후에 고온으로 승온 하는 동안 암모니아 가스와 함께 TMGa 소스도 함께 흘려주었다. 이와 같은 방법으로 성장된 GaN 버퍼층은 나노 컬럼나 (nano-columanr) 구조를 유지하면서 많은 양의 탄소를 포함 하고 있는 것을 확인 하였으며, 그에 대한 성장 메커니즘을 규명 하였다. 결과적으로 새로운 GaN 버퍼층을 적용 함으로써 사파이어 기판 위 GaN 층의 기판 휨 현상이 완화 되었으며, 고저항 특성을 나타내었다. 이 버퍼층을 적용하여 HEMT 소자를 제작한 결과 -4 V 의 게이트 전압 하에서 800 V 이상의 off-state 항복전압 (breakdown voltage) 특성을 보였으며

이러한 결과는 본 연구의 새로운 저온 GaN 버퍼층이 사파이어 기판 위 GaN 전자소자에 적합함을 보여준다.

주요어:

버퍼층, GaN, AlN, 유기금속화학기상증착법, DC 마그네트론 스퍼터링, 고전자이동도 트랜지스터, 실리콘 기판, 사파이어 기판, 메모리 효과, 고저항 GaN, 기판 휨 현상, 상온 성장

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