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Design and Fabrication of Gate Driver Circuits Employing Depletion-Mode Oxide TFTs for AMLCD and AMOLED

능동 구동 액정 디스플레이 및 유기 발광 다이오드를 위한 공핍형 산화물 박막트랜지스터를 이용한 게이트 드라이버 회로 설계 및 제작

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ABSTRACT
Design and Fabrication of Gate Driver Circuits Employing
Depletion-Mode Oxide TFTs for AMLCD and AMOLED

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Recently, the high-end flat panel display (FPD) requires ultrahigh-resolution (≥4Kx2K) and high-frame-rate (≥240Hz). However, it is well known that the electrical characteristics of the widely used a-Si:H TFT could not meet the requirements. The amorphous oxide-based thin-film transistors (TFTs) have attracted considerable attention due to high mobility and good uniformity over large area substrates. Most oxide-based TFTs are inherently a depletion-mode device rather than the widely used enhancement-mode device due to large electron concentrations. In addition, it is well known that a severe negative shift in the threshold voltage of oxide-based TFTs occurs during negative bias illumination stress or only light illumination. Therefore, the driving circuit which can be operated in depletion-mode would be indispensable for an oxide TFT-based display.

In this study, novel level shifters and shift registers employing depletion-mode a-IGZO TFTs were investigated. The level shifter employing two clock signals with 180° out of phase and one discharging TFT has been swung fully from VDD to VSS. Although the level shifter employed only n-
type depletion-mode a-IGZO TFTs, it had a wide swing output without any additional power sources and input signals.

The shift register (I) has been designed by employing two low-voltage-level power signals with which a negative voltage can be applied to the Vgs of depletion-mode a-IGZO TFTs. Especially, the shift register (II) has been designed by employing only one low-voltage-level power signal, which has been usually used in a circuit employing a conventional enhancement-mode device, without an additional signal. The shift registers successfully exhibited a high-voltage output pulse without any distortion. For the narrow-bezel display, the shift register (III) employing node-shared structure, where Q-node and Qb-node of adjacent two stages are shared, respectively, required 14 TFTs, 3 clock lines, and 3 power source lines for two output pulses, whereas the previous shift registers consisted of more than 22 TFTs, 4 clock lines, and 6 power source lines.

For the applications of the driving circuits in displays, such as AMLCD and AMOLED, the depletion-mode a-IGZO TFT shift registers embedded with a full-swing level shifter were investigated. The start signal and the clock input signals of $-10 \sim 5$ V have been level shifted to the output signals of $-10 \sim 20$ V. The depletion-mode a-IGZO TFT shift register embedded with a full-swing level shifter has successfully exhibited a high-voltage output pulse without any distortion. Also, the shift register embedded with the level shifter successfully exhibited a high-voltage output pulse without distortion at a clock frequency of 100 kHz, which is enough to drive a high-frequency FPD with a frame rate of $\sim 360$ Hz and a resolution of FHD. The SPICE simulation results have shown that the shift register embedded with the level shifter would work without any problem, although the threshold
voltages of the TFTs degraded by gate bias stress in the level shifter and the shift register would be largely shifted to $-9.3$ and $+15.2$ V, respectively. The measured output waveform of the shift register embedded with the level shifter has not been distorted after 240-h driving under 450-nm illumination with an intensity of 1 mW/cm$^2$ at 60°C.

Keywords : amorphous oxide-based thin-film transistors (TFTs), a-IGZO, Depletion-mode, illumination, level shifter, shift register.

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Chapter 1 Introduction

The oxide-based TFTs have attracted considerable attentions as promising alternatives for pixel elements of AMLCD and AMOLED. The electrical characteristics and stability of the oxide-based TFTs are not only superior to those of the a-Si:H TFTs, but also the uniformity is much better than the poly-Si TFTs. Most of the oxide-based TFTs are inherently a depletion-mode device rather than the widely used enhancement-mode device. It is well known that a design of driving circuits which employ a depletion-mode device is rather difficult and troublesome. Therefore, the design of driving circuits employing the oxide-based TFTs may be a very important issue in practical application in order to commercialize the oxide-based TFTs.
1.1 Background

Flat panel displays (FPDs) have been grown rapidly for last decade [1]. FPDs include various displays such as active-matrix liquid crystal display (AMLCD) [2], active-matrix organic light-emitting diode (AMOLED) [3], plasma display panel (PDP) [4], and so on. Among FPDs candidates, AMLCD is widely used as a main display because it is thin, light-weight, low power, and cost-effective. It could be produced as very many kinds of sizes such as less than 1 inch to larger than 100 inch due to low-temperature process on glass substrates. Therefore, AMLCD is used at various applications such as smart-phone, digital camera, tablet PC, notebook PC, computer monitor, TV and so on.

Although AMLCD technology has very matured, the residual image problem at fast moving picture in AMLCD have been issued. It is because that the liquid crystal material has inherent drawback such as slow response time. One of the approaches to suppress the residual image problem is to employ the high operation frequency driving such as 120 and 240 Hz [5], [6]. Also, AMLCD is employing to the advanced technologies such as ultrahigh-definition (UD) and 3-dimension (3D). Therefore, the electrical characteristics of thin-film transistors (TFTs) have to be improved for ultrahigh-resolution and high-frame-rate display.

Nowadays, AMOLED has attracted a considerable attention due to wider viewing-angle, faster response-time, more vivid color, lighter weight, and lower power-consumption in comparison with AMLCD. The market of AMOLED is growing very rapidly at mainly smart-phone and mobile device applications. This success in the small-sized AMOLED displays is leading
some display manufacturers to develop the large-sized AMOLED TVs.

The luminescence of OLED is controlled by current amount of TFTs. The image quality of AMOLED is very sensitive to the characteristics of TFTs. Although a pixel circuit in AMOLED could be operated with only 2 transistors and 1 capacitance in principle, it requires more transistors and capacitances in order to compensate of drawback of TFTs such as non-uniformity and poor electrical stability [7]-[12].

AMLCD and AMOLED employ dominantly hydrogenated amorphous-silicon (a-Si:H) TFTs and low temperature polycrystalline-silicon (LTPS) TFTs.

a-Si:H TFTs are very suitable for large area applications due to its low-cost, low temperature processing, and better uniformity over large area substrates. They are widely used as a switching device of pixel elements in AMLCD. They have been well proven for large area commercial applications. It could be produced with below 400°C process which is compatible to low price glass substrate [13]-[15]. Drastic improvement of the driving technology and the electrical performance of a-Si:H TFTs make it possible not only to switch pixels but to integrate the gate driver [16]-[25]. However, a-Si:H TFTs have drawbacks such as low field-effect mobility (<1 cm²/V·s) and well-known instabilities with respect to bias stressing [26] and light exposure [27]. The growth of the high-end commercial market with ultrahigh-resolution (UD), high-frame-rate (>240 Hz), and sizes larger than 70 inches requires a higher electrical performance of TFTs. At least 3 cm²/V·s of field-effect mobility is required to satisfy such demands [28], which is not so easy to achieve by modifying the conventional amorphous silicon material. Also, the threshold voltage of a-Si:H TFTs is easily increased or decreased when the
gate bias is applied. The charge trapping and defect state creation are considered as main mechanisms of instabilities of a-Si:H TFTs [26], [27], [29]-[31]. It is well known that the SiNx, which is widely used as a gate insulator, has a high density of trap sites. When the gate bias was applied at the a-Si:H TFTs, the electron charges are trapped at the SiNx gate insulator or SiNx/a-Si:H interface [32]. When the positive bias is applied at a-Si:H TFTs, the defect states could be generated at a-Si:H layer or at SiNx/a-Si:H interface [33]. Almost all extra electron carriers generated by gate bias in channel region are accumulated in tail state of conduction band which has weak Si-Si bonds.

On the other hand, LTPS TFTs are widely used to drive AMOLED because it exhibits a more sufficient and stable current supply into the OLED than the a-Si TFTs. Since the poly-Si TFTs could be made as both NMOS and PMOS TFTs, the CMOS circuit could be designed [34]-[36]. As a result the peripheral driver circuits of flat panel display could be integrated at glass substrate without additional integrated chip. The poly-Si TFTs can exhibit electron mobility in excess of 50 cm²/V·s, and the stability is very excellent than that of the a-Si TFTs. However, large area application has been proven to be difficult, and the relatively high thermal budget makes poly-Si unsuitable for flexible substrates. It is suffered from current non-uniformity at large area caused by inherent fluctuation of laser energy density. Because the each laser pulse generated during crystallization of amorphous silicon has different energy density and the spot size of laser is very small, the electrical characteristics of the poly-Si are not uniform. The many compensation circuits in AMOLED have been reported in order to compensate the current non-uniformity of the poly-Si TFTs [7]-[12]. The
production cost of the poly-Si TFTs is relatively high due to expensive laser equipment.

Recently, the oxide-based TFTs, such as ZnO, InGaZnO (IGZO), HfInZnO (HIZO), ZnSnO (ZTO), ZnInO (ZIO), and ZnInSnO (ZITO), have attracted considerable attentions as promising alternatives for pixel elements of FPD [37]-[54]. The electrical characteristics and stability of the oxide-based TFTs are superior to those of the a-Si:H TFTs, and at the same time, the uniformity is much better than the poly-Si TFTs. The field-effect mobility of the oxide-base TFTs is about $10 \text{ cm}^2/\text{V} \cdot \text{s}$, which is not too small to drive AMLCD with ultrahigh-resolution and high-frame-rate or AMOLED. In addition, oxide semiconductor materials have an amorphous phase in general, which shows uniform electrical properties even with a large-area substrate and is strongly advantageous for the display applications. The production process of the oxide-based TFTs are compatible to that of the a-Si:H TFTs.

Transparent electronics is today one of the most advanced topics for a wide range of device applications. The key components are wide bandgap semiconductors, where oxides of different origins play an important role, not only as passive component but also as active component, similar to what is observed in conventional semiconductors like silicon. Transparent electronics has gained special attention during the last few years and is today established as one of the most promising technologies for leading the next generation of FPD due to its excellent electrical performance. The transparent display is applicable to automobile displays so that people can get information from the transparent display as well as a real environment, such as in traffic situations while driving a car. Also, the transparent display
may involve a see-through mobile phone that would allow users to access both sides of the display as independent touch screens and thereby to provide resourceful user interfaces.

However, the stability of the oxide-based TFTs especially under light illumination [55]-[61] should be improved in order to apply at practical application of FPD as shown in Figure 1.1.

In this study, the driving circuits employing amorphous IGZO (a-IGZO) TFTs are designed. Most of a-IGZO TFTs are inherently a depletion-mode device rather than the widely used enhancement-mode device [62]-[69]. In addition, it is well known that a severe negative shift in the threshold voltage of oxide TFTs occurs during negative bias illumination stress or only light illumination [57], [70], [71]. Therefore, the driving circuit which can be operated in depletion-mode would be indispensable for an oxide TFT display. Several level shifters and shift registers are proposed and fabricated. Also, the shift register embedded with a level shifter are designed, and the reliability of the circuits are verified for display applications.
Figure 1.1 Next-generation displays.
1.2 Outline of This Thesis

This study focuses on the design of driving circuits employing depletion-mode a-IGZO TFTs. Most of a-IGZO TFTs are inherently a depletion-mode device rather than the widely used enhancement-mode device. It is well known that a design of driving circuits such as a shift register and a level shifter which employ a depletion-mode device is rather difficult and troublesome. In this thesis, the driving circuits, such as level shifter and shift register, employing depletion-mode a-IGZO TFTs are proposed and fabricated.

In Chapter 2, the electrical characteristics and reliability of oxide-based TFTs are reviewed. Also, it gives brief introduction to inverter, level shifter, and shift register employing n-type TFTs.

In Chapter 3, the driving circuits employing depletion-mode a-IGZO TFTs are introduced. Two level shifters and three shift registers are proposed and fabricated. a-IGZO TFTs with an etch-stopper structure are fabricated by six-mask process compatible to conventional a-Si:H TFTs fabrication process. It is very difficult to turn off the depletion-mode a-IGZO TFTs due to considerable leakage current. Therefore, in the two level shifters and three shift registers, the concepts which can apply the negative voltage to Vgs of the depletion-mode a-IGZO TFTs are employed. Furthermore, the level shifter and the shift register which can be operated in depletion-mode without any additional power sources and input signals are proposed. The experimental results have shown that the level shifters and the shift registers have been designed to easily turn off the depletion-mode a-IGZO TFTs.

In Chapter 4, the depletion-mode a-IGZO TFT shift register embedded
with a full-swing level shifter is introduced and discussed. The shift register embedded with the level shifter has been designed by employing two clock signals with $180^\circ$ out of phase and one start signal for the level shifter and two low-voltage-level signals for the shift register, respectively. The depletion-mode a-IGZO TFT shift register embedded with a full-swing level shifter has successfully exhibited a high-voltage output pulse without any distortion.

Also, the shift register embedded with the level shifter without any additional signals is introduced. In addition, the reliability of driving circuits under light illumination is discussed. The shift register embedded with the level shifter successfully exhibits a high-voltage output pulse without distortion at a clock frequency of 100 kHz, which is enough to drive a high-frequency FPD with a frame rate of $\sim360$ Hz and a resolution of full high definition. The experimentally measured output waveform of the shift register embedded with the level shifter has not been distorted after 240-h driving under 450-nm illumination with an intensity of 1 mW/cm$^2$ at 60 $^\circ$C.
Chapter 2 Review of oxide-based TFT and NMOS driving circuit technology

Novel oxide-based channel materials such as IGZO, ZTO, ZITO, etc., exhibit several advantages over a-Si:H TFTs, such as mobility in the range of $\sim 5$ to 50 cm$^2$/V·s, low temperature processing, and transparency. The potential application for the oxide-based TFTs is a backplane for high-performance AMLCD, especially for large-area displays. Another target application for these new materials is using them for the emerging AMOLED display technology. For the first two applications, TFTs need to remain stable while operating under continuous exposure to illumination.

On the other hand, most of the oxide-based semiconductor materials are n-type due to the existence of intrinsic donors. Therefore, all driving circuits with the oxide-based TFTs should be designed by employing only n-type TFTs.
2.1 Overview

In 2003, several groups reported on the oxide-based TFTs based on ZnO, which is a wide-bandgap semiconductor [72], [73]. These original devices generated excitement not only because they were transparent but also because they exhibited electron mobilities (μ) of 0.3–2.5 cm$^2$/V·s and I$_{ON}$/I$_{OFF}$ ratio of $\sim 10^7$. Many novel materials have been used to make TFTs, including In$_2$O$_3$, SnO$_2$, IGZO, ZTO, ZIO, IGO, and ZITO. Although ZnO, In$_2$O$_3$, and SnO$_2$ are typically poly-crystalline in thin-film form, crystallization is frustrated in multi-component materials such as IGZO, ZTO, ZIO, IGO, TGZO, and ZITO. These latter materials are referred to as amorphous oxide semiconductors.

These materials have several advantages for TFT applications as follows:
1) an amorphous crystal structure which can aid in achieving good uniformity and easy manufacturing
2) low-temperature processing which is suitable for flexible substrates
3) electron mobility in the range of 5 to $> 50$ cm$^2$/V·s, which is about ten times greater than a-Si:H
4) transparency in visible region

While most of the research work was being devoted to binary oxides such as ZnO, In$_2$O$_3$ or SnO$_2$, Nomura et al. suggested to use a complex InGaO$_3$(ZnO)$_5$ (or IGZO) single-crystalline semiconductor layer in a TFT [73]. Also, Nomura’s work opened the door for an impressively growing number of publications regarding the application of amorphous multi-component oxides as channel layers in TFTs. Several combinations of cations with (n-1)d$^{10}$ns$^0$ ($n \geq 4$) electronic configuration started to be used for this end, being ZTO [74], [75], IZO [76], [77], and IGZO [78]-[80] the most widely explored ones. With
the continuous improvements verified on these devices, it is now common to obtain remarkable electrical properties, such as mobilities above 10 cm²/V·s, \( I_{ON}/I_{OFF} \) ratio exceeding \( 10^7 \) and sub-threshold swing of 0.20 V/dec, with the indium-based semiconductors. In particular, a-IGZO is the most widely used semiconductor oxide materials [41].

Most of the oxide-based semiconductor materials are n-type due to the existence of intrinsic donors. Therefore, all driving circuits with the oxide-based TFTs should be designed by employing only n-type TFTs.
2.2 Oxide-based TFT

2.2.1 Electrical characteristics of oxide-based TFT

The carrier transport of oxide semiconductors is closely related with the s-orbital overlapping of transition metal atoms and ordering because they have strong iconicity [81]. Amorphous oxide semiconductors exhibit hall-effect mobilities similar to those of the corresponding crystalline phase, even if they are formed at room temperature. These carrier transport properties are unique to oxide semiconductors, and are not seen in covalent amorphous semiconductors such as a-Si:H as shown in Figure 2.1 [41]. The oxide semiconductor materials are divided into three main categories, such as ZnO, IGZO and others including ZTO, ITO, IZO, IZTO, IGO and IHZO. After 2009, it is observed an increase concerning solution-processed TFTs.

The effect of IGZO composition on the TFTs electrical properties was been reported by Iwasaki et al. [80] and by Barquinha et al. [82]. While Iwasaki used a combinatorial co-sputtering study with 3 oxide targets (ZnO, Ga$_2$O$_3$ and In$_2$O$_3$), Barquinha et al. used specific IGZO target compositions. The semiconductor layers were produced with an oxygen percentage of 0.4 %, being the final devices annealed at $T_A = 150$ °C. Transfer characteristics are presented in Figure 2.2 for ternary/quaternary compounds, being the trends of $\mu_{FE}$ and $V_{ON}$ with composition shown in Figure 2.3. For In$_2$O$_3$ films, very large $\mu_{FE}$ is achieved due to high carrier concentration ($N \approx 10^{18}$ cm$^{-3}$). However, the devices are not usable as TFTs, since they cannot be switched off. On the other hand, Ga$_2$O$_3$ films have very large resistivity ($\rho > 10^8$ Ω cm) due to a very low N and large density of empty traps. This results in very poor device performance, with $V_{ON} > 20$ V, $\mu_{FE} \approx 0.02$ cm$^2$/V · s and large $\Delta V_{ON}$,
above 6 V. ZnO seems to be the best binary compound for oxide TFT application, at least considering the range of deposition conditions used herein. In fact, close to $0 \ V_{\text{ON}}$, on/off exceeding $10^6$ and $\Delta V_{\text{ON}} \approx 1 \ V$ are achieved on these ZnO TFTs. Given the stronger bonds of gallium with oxygen, $N$ decreases as gallium content in IGZO increases, resulting in a considerable shift of $V_{\text{ON}}$ toward more positive values. This is naturally advantageous for large $\text{In}/(\text{In}+\text{Zn})$, since it permits the production of TFTs that clearly switch between off- and on-states. However, for smaller $\text{In}/(\text{In}+\text{Zn})$, gallium incorporation can also lead to devices with considerably lower $\mu_{\text{FE}}$ and higher $V_{\text{ON}}$ and $\Delta V_{\text{ON}}$.

Most of the oxide-based TFTs are inherently a depletion-mode device rather than the widely used enhancement-mode device due to large electron concentrations [83]–[88]. An enhancement-mode oxide-based TFT could be fabricated by controlling some fabrication parameters. As the oxygen partial pressure increases, the threshold voltage of the oxide-based TFTs is shifted to positive voltage direction [89]. For non-passivated IGZO TFTs with different $\%O_2$, 0.4 and 10.0 %, the films with $\%O_2=10.0$ % have a lower density of oxygen vacancies, which are known to be the main source of free carriers in oxide semiconductors. Also, a threshold voltage is shifted to positive voltage direction as the active layer thickness decreases [90]. However, the stability of an enhancement-mode oxide-based TFT fabricated by controlling those parameters is worse than that of a depletion-mode oxide TFT.
Figure 2.1 Schematic orbital drawings for the carrier transport paths in crystalline and amorphous semiconductors: (a) Covalent semiconductors, (b) Amorphous oxide semiconductors [41].
Figure 2.2 Effect of oxide semiconductor target composition on the transfer characteristics of TFTs annealed at 150 °C: ternary and quaternary compounds. The effect of decreasing $d_s$ from 40 to 10 nm for IZO 2:1 is also shown [82].
Figure 2.3 (a) $\mu_{\text{FE}}$ and (b) $V_{\text{ON}}$ obtained for TFTs with different oxide semiconductor compositions, in the indium-gallium-zinc oxide system. Devices annealed at 150 °C, with%O$_2$ = 0.4% [82].
2.2.2 Stability of oxide-based TFT

Based on the understanding that has been developed for a-Si:H TFTs [26], [27], it can be expected that light illumination and bias stressing may cause instabilities such as charge trapping and defect creation in the amorphous oxide-based TFTs, in the gate dielectric, or at the oxide semiconductors/dielectric interface. Positive bias stressing has usually been tested for AMOLED applications, because TFT must supply a stable current for the entire operating time. In general, oxide semiconductors have n-type characteristics, so applying negative voltage at the gate is required for turning off the device. The total duration of the negative gate bias applied on the switching transistor is larger than that of the positive gate bias by more than 500 times in the case of AMLCD. Severe negative shift in threshold voltage of oxide-based TFT has been reported during negative bias illumination stress or only light illumination [57], [70], [91].

Figure 2.4 shows the transfer characteristics of ZTO TFT with various intensities and wavelengths [57]. A further increase of the off current with higher intensities could be seen. Also, the threshold voltage decreased as the wavelength was short. Figure 2.5 shows the evolution of the transfer curve under bias temperature stress (BTS) and bias illumination temperature stress (BITS), respectively [71]. For the positive bias stress, there was little difference between under BTS and BITS. However, the transfer curve moved to the negative direction largely under BITS, whereas no remarkable change was observable under BTS for negative bias stress.

Jeong et al. reported the environmental effects such as oxygen and water molecules on the oxide-based TFTs [61]. As shown in Figure 2.6, a suitable passivation layer is essential to improve the long-term reliability of oxide
TFTs.

On the other hand, as aforementioned, an enhancement-mode oxide-based TFTs could be fabricated by controlling some fabrication parameters such as oxygen partial pressure or the thickness of the film [89], [90]. However, the stability of an enhancement-mode oxide-based TFTs fabricated by controlling fabrication parameters such as oxygen partial pressure or the thickness of the film is worse than that of a depletion-mode oxide-based TFTs. P. Barquinha et al. reported that a threshold voltage was shifted to positive direction as the oxygen partial pressure increased. However, as an oxygen partial pressure increased, the threshold voltage shift got considerably larger as shown in Figure 2.7 [89]. They reported that higher oxygen partial pressure generated more defects, both in IGZO’s bulk and at its interface with SiO$_2$, by energetic ions, which led to highly unstable devices. C.-S. Hwang et al. reported that the ZnO TFTs with thicker active layer were more stable as shown in Figure 2.8, because total induced charges per unit area in the channel under operation current were same but the density of induced charges increased according to the thinning of active layer [90].
Figure 2.4 Transfer characteristics of TFT with ZTO channel deposited at 450 °C. (a) For different intensities at $\lambda=470$ nm. (b) For different wavelengths at $I=1$ mW/cm$^2$ [57].
Figure 2.5 Changes in the $I_D$-$V_G$ characteristics of ZnO TFTs (W/L =40 μm/20 μm) under 10 V gate bias stress with (a) $P_{ill}$ of 0 mW/cm$^2$ and (b) 1.0 mW/cm$^2$ and under -10 V gate bias stress with (c) $P_{ill}$ of 0 mW/cm$^2$ and (d) 1.0 mW/cm$^2$. $V_D$ is 15 V during the $V_G$ sweep [71].
Figure 2.6 Dependence of the $V_{th}$ shift on the gate bias stresses. For comparison, the effect of the gate bias stress on the unpassivated oxide transistor was also included [61].
Figure 2.7 Constant $I_D$ stress measurements of non-passivated IGZO TFTs with different $\%O_2$ used to deposit the IGZO layer, 0.4 and 10.0%, and $T_A=150$ °C: (a) transfer characteristics; (b) $\Delta V_T$ vs stress/recovery time [89].
Figure 2.8 (a) Transfer characteristics of ZnO TFTs according to the thickness of active layer. (b) The shift of operation voltage in constant current stress condition for ZnO TFTs [90].
2.3 NMOS driving circuit

2.3.1 Inverter with n-type TFT

The inverter is a basic building block for driving circuits such as level shifter and shift register. It is well known that the push-pull CMOS inverter is the best among various ones. Its output voltage swings from VDD to ground unlike other logic families that never quite reach the supply levels. The static power dissipation of the CMOS inverter is practically zero and the inverter can be sized to give equal sourcing and sinking capabilities. Also, the logic switching threshold can be set by changing the size of the devices. Other inverter configurations are shown in Figure 2.9 [92]. The inverter shown in Figure 2.9(a) is an NMOS-only inverter, useful in avoiding latch-up. The inverters shown in Figure 2.9(b) and (c) use a PMOS load, which is, in general, most useful in logic gates with a large number of inputs. For the oxide-based display technology, all driving circuits should be designed by employing n-type TFTs due to the absence of good p-type TFTs.

Figure 2.10 shows the modified version of the NMOS inverter [92]. It was used when the output voltage must swing up to VDD. When input to the inverter is a logic high, M1 is on and the output is pulled down to approximately

$$V_{OL} = (V_{DD} - 2V_{TH}) \cdot \frac{R_{n1}}{R_{n1} + R_{n2}}$$

When input transitions from high to low, M4 is used as a capacitor. The idea is to capacitively couple the output pulse to the gate of M2. The result is an increase in the gate potential above VDD, allowing M2 to fully turn on. Without bootstrapping, the gate of the M2 is tied to VDD and the output is
limited to \( V_{DD} - V_{THN} \). If the gate of M2 is bootstrapped, then M2 fully turns on and the output goes to VDD. However, it can not swing down to ground as shown in Figure 2.10. Furthermore, M2 is always turned on, so that the power consumption would be a troublesome problem.
Figure 2.9 Various inverter configurations. (a) CMOS inverter, (b) NMOS-only inverter, (c) and (d) Inverter with a p-channel load [92].
Figure 2.10 (a) Bootstrapped NMOS inverter and (b) its simulation results [92].
2.3.2 Level shifter with n-type TFT

Figure 2.11 shows the level shifter with cascaded bootstrapped n-type a-Si:H TFT inverters [93]. The well-known standard CMOS technologies [94] are not suitable for a-Si:H TFT and oxide-based TFT because of the absence of a good p-type TFT and/or its low mobility. As shown in Figure 2.11, the output voltage of the first inverter depends on the resistance ratio of the transistors $T_1$ to $T_2$, indicating that the output-low is always greater than $V_{SS1}$. When the input voltage becomes a low level, the transistor $T_2$ turns off and then the output voltage rises. During this rise, the gate voltage of load transistor $T_1$ is bootstrapped by the bootstrap capacitor $C_1$ and the parasitic capacitance of $T_1$ [95] because $T_3$ acts as reverse biased diode when the voltage increases. Therefore, the output-high reaches $V_{DD1}$. The cascaded inverter keeps the output phase the same as the input phase.
Figure 2.11 Level shifter of cascaded bootstrapped inverters with 5-pF bootstrap capacitors [93].
2.3.3 Shift register with n-type TFT

Integrating the shift register on the panel is very important in the display technology because it can reduce the cost of external IC chip. Nowadays, integrating the shift register employing a-Si:H TFTs as well as poly-Si TFTs is necessary in AMLCD [16]-[25].

Figure 2.12 shows the schematic and the timing chart of the conventional shift register with only n-type TFTs. The operation mechanism of the conventional shift register is as follows.

**Stage 1**: When T1 is turned on by the output pulse of Vg(n-2) in the previous stage, a Q-node is charged to a high-voltage. At the same time, a Qb-node becomes a low-voltage (V_{GL}) because T5 is turned on by a Q-node of a high-voltage.

**Stage 2**: When CLK(x) of a high-voltage is applied to the drain of T7, a Q-node is bootstrapped by the parasitic capacitances of T7. Therefore, the output pulses [Vg(n)] are generated through T6, which is fully turned on.

**Stage 3**: After the output pulse is generated, a Q-node is discharged to VGL when T2 is turned on by the output pulse of Vg(n+2). T3 is turned on so that the voltage of a Q-node is maintained to a low voltage.
Figure 2.12 (a) Schematic and (b) timing chart of the conventional shift register with only n-type TFTs.
Chapter 3 Design of driving circuit units employing depletion-mode a-IGZO TFTs

Amorphous Indium–Gallium–Zinc–Oxide thin-film transistors (a-IGZO TFTs) have the potential advantages of low-temperature processing and superior electrical properties, such as great field-effect mobility, sharp sub-threshold swing, and high on/off current ratio. In this chapter, novel level shifters and shift registers employing depletion-mode a-IGZO TFTs are introduced.
3.1 Overview

Recently, a-IGZO TFTs have attracted considerable attention for active matrix displays with ultrahigh-resolution and high-frame-rate, such as AMOLED and AMLCD, due to their high mobility and fairly good uniformity at large area. Device structure and fabrication process of a-IGZO TFTs are similar with those of hydrogenated amorphous silicon (a-Si:H) TFTs which are widely used in backplane of TFT-LCDs. Therefore, a-IGZO TFTs may be one of the most promising devices for future display applications.

Most oxide TFTs are inherently a depletion-mode device rather than the widely used enhancement-mode device due to large electron concentrations [83]–[88]. It has been reported that an enhancement-mode oxide TFTs could be fabricated by controlling some fabrication parameters such as oxygen partial pressure or the thickness of the film. However, the stability of enhancement-mode oxide fabricated by controlling those parameters is worse than that of depletion-mode oxide TFTs [89], [90]. In addition, it is well known that a severe negative shift in the threshold voltage of oxide TFTs occurs during negative bias illumination stress or only light illumination [57], [70], [71]. Therefore, the driving circuit which can be operated in depletion-mode would be indispensable for an oxide TFT-based display. It is well known that the design of driving circuits, such as inverters, level shifters, and shift registers employing a depletion-mode device rather than an enhancement-mode device, is quite difficult and troublesome due to a considerable leakage current.

In the following sections, novel level shifters and shift registers
employing depletion-mode a-IGZO TFTs are introduced and discussed. a-IGZO TFTs with an etch-stopper structure are fabricated by six-mask process compatible to conventional a-Si:H TFTs fabrication process.

Firstly, the level shifter (I) has been designed by employing two clock signals with 180° out of phase in order to turn off depletion-mode a-IGZO TFTs. The level shifter (II) swings fully from VDD to VSS. It is possible because the resistance of a load TFT is extremely increased by using one discharging TFT. Although the level shifter (II) employs only n-type depletion-mode a-IGZO TFTs, it has a wide swing output without any additional power sources and input signals.

Secondly, the shift register (I) has been designed by employing two low-voltage-level power signals with which a negative voltage can be applied to the gate–source voltage (Vgs) of depletion-mode a-IGZO TFTs. The shift register (II) with depletion-mode a-IGZO TFTs has been designed by employing only one low-voltage-level power signal, which is usually used in a circuit employing a conventional enhancement-mode device, without an additional signal. Although the shift register (II) employs only low-voltage-level power signal, a negative voltage can be applied to the Vgs of a-IGZO TFTs. It is possible because the charging and discharging TFTs of the shift register are composed of the series-connected two-transistor (STT) structure. The driving circuits employing depletion-mode oxide TFTs require many TFTs in addition to additional power sources and input signals in order to turn off depletion-mode oxide TFTs [64]. It should be pointed out that many TFTs and signal lines would increase the circuit area. Therefore, the shift register (III) has been designed by employing node-shared structure, where Q-node and Qb-node of adjacent two stages are shared, respectively. The
shift register (III) requires 14 TFTs, 3 clock lines, and 3 power source lines for two output pulses, whereas the previous shift registers consisted of more than 22 TFTs, 4 clock lines, and 6 power source lines.
3.2 Level shifter with two clock signals of 180° out of phase

3.2.1 Introduction

Figure 3.1 shows the applied voltage at the electrodes of pixel and circuit TFTs. In general, for pixel TFTs, the low-voltage-level of a gate electrode is less than that of a source (or drain) electrode. Although a threshold voltage of TFT is negative, there is no problem to turn off the pixel TFTs by applying a proper voltage at the gate electrode. On the other hand, the low-voltage-level of a gate electrode is equal to that of a source (or drain) electrode for circuit TFTs. A Gate-Source voltage (Vgs) almost becomes zero when operating at the “OFF” condition. Therefore, it is rather difficult to turn off the depletion-mode a-IGZO TFTs in driving circuits due to considerable drain–source current.

Although Hwang’s level shifter employing a depletion-mode aluminum-doped ZTO has been reported [96], it requires an additional power source and input signals in order to turn off the depletion-mode TFTs.

In this section, a new depletion-mode a-IGZO TFT level shifter without any additional power source and input signals are proposed and discussed. This level shifter employs two clock signals with 180° out of phase in order to turn off the depletion-mode a-IGZO TFTs.
Figure 3.1 Applied voltage conditions at the electrodes of (a) pixel and (b) circuit TFTs.
3.2.2 Fabrication and characteristics of a-IGZO TFTs

The bottom-gate a-IGZO TFTs with an etch-stopper structure by using a six-mask process were fabricated as shown in Figure 3.2. A 200-/50-nm-thick AlNd/Mo dual layer as gate electrode was deposited by direct-current magnetron sputtering on a glass substrate. A 200-nm-thick SiO$_2$ film as a gate insulator was deposited by plasma-enhanced chemical vapor deposition (PECVD) at 350 °C, and a 50-nm-thick a-IGZO (In:Ga:Zn = 1:1:1) layer as an active material was sputtered at room temperature. The active layer was patterned by wet-etching, and a 50-nm-thick SiO$_2$ layer as an etch-stopper was deposited by PECVD at 250 °C. A 200-nm-thick Mo layer was deposited for source/drain electrodes. After patterning source/drain electrodes, a 200-nm-thick SiO$_2$ passivation layer was deposited by PECVD at 250 °C, and a 50-nm-thick indium tin oxide layer was formed for pixel electrodes. Finally, the devices were annealed for 2 h in an air ambient at 300 °C.

Figure 3.3 shows the transfer characteristics of a-IGZO TFTs. The channel width and length of a-IGZO TFT are 30 and 10 μm, respectively. The device exhibits the electrical properties such as a field effect mobility of 12.8 cm$^2$/Vs, a threshold voltage of −2.01 V, and a sub-threshold slope of 0.23 V/dec. It should be pointed out that the IGZO TFT operates in the depletion-mode rather than the enhancement-mode.
Figure 3.2 Cross-sectional schematic of a-IGZO TFT.
Figure 3.3 Transfer characteristics of a-IGZO TFT.
3.2.3 Design of level shifter (I)

Figure 3.4 shows the schematic and timing chart of the conventional level shifter. The conventional level shifter [92], as shown in Fig. 2(a), generates a high-voltage output when the clock (CLK) or Vout_1 of a low-voltage-level is applied to the gate of driver TFTs (T3c and T6c). However, in case of a level shifter employing a depletion-mode device, such as a-IGZO TFTs, the outputs of Vout_1 and Vout_2 would not swing up to VDD1 and VDD2, respectively, because the gate–source voltage (Vgs) of driver TFTs becomes zero so that the considerable current still flows through the driver TFTs. It is rather difficult to turn off the depletion-mode a-IGZO TFTs in driving circuits due to considerable drain–source current. Therefore, the output of the conventional level shifter employing depletion-mode a-IGZO TFTs could not reach VDD.

In order to overcome this problem, a new level shifter (I) which employs two clock signals (CLK and CLKB) with 180° out of phase is proposed as shown in Figure 3.5(a). CLK and CLKB are connected to the gate and source of T3p, respectively. As shown in period [A] of Figure 3.5(b), when CLK and CLKB are low- and high-voltages, respectively, the driver TFT (T3p) is completely turned off although a depletion-mode a-IGZO TFT is used. It is possible because the Vgs of the driver TFT becomes negative by CLK and CLKB. Therefore, the high-voltage-level of the output in the proposed level shifter (I) would be equal to VDD.

\[ V_{gs,\text{driverTFT}} = V_L - V_H, \quad V_L \ll V_H \quad (1) \]

On the contrary, when CLK and CLKB are high- and low-voltage
(period [B]), respectively, the driver TFT is turned on so that the output is maintained to a low-voltage-level.

Figure 3.6 shows the illustration of the operation mechanism of the proposed level shifter (I).
Figure 3.4 (a) Schematic and (b) timing chart of the conventional level shifter.
Figure 3.5 (a) Schematic and (b) timing chart of the proposed level shifter (I).
Figure 3.6 Illustration of the operation mechanism of the proposed level shifter (I).
3.2.4 Simulation and experiment

The Simulation Program with Integrated Circuit Emphasis (SPICE) simulation was performed to verify the conventional level shifter and the proposed one (I). The SPICE model parameters were extracted from the fabricated a-IGZO TFTs. Of the extracted SPICE parameters [97], CGSO (gate–source capacitance) and CGDO (gate–drain capacitance) are 0.54 nF/m. The level shifters are operated with a frequency of 12.5 kHz, and the voltages are 10 (for VDD1), 20 (for VDD and VDD2), and 0-10 V (for CLK and CLKB).

Figure 3.7 shows the simulation result of the conventional level shifter employing depletion-mode a-IGZO TFTs. The high voltages of Vout_1 and Vout_2 in the conventional level shifter don’t reach VDD1 (10 V) and VDD2 (20 V), respectively. It is because the driver TFTs (T3c and T6c) are not turned off at the Vgs of 0 V.

Figure 3.8 shows the simulation result of the proposed level shifter (I). The high-voltage-level output of the proposed level shifter (I) successfully reaches VDD by employing two clock signals (CLK and CLKB) with 180° out of phase. Also, it is confirmed that a negative voltage is successfully applied to the Vgs of T3p by CLK and CLKB so that the depletion-mode a-IGZO TFT is easily turned off.

The proposed level shifter (I) was fabricated by employing a-IGZO TFTs. The channel lengths of all TFTs are 10 μm. The channel widths of TFTs are 20 (for T1p), 100 (for T2p), and 1000 μm (for T3p). The bootstrap capacitor is 1.5 pF. The overlap length of gate–drain in TFTs is 4 μm. Figure 3.9 shows the optical image of the proposed level shifter (I). The depletion-mode a-IGZO TFT level shifter (I) was measured by 0–10 V square wave
inputs. As shown in Figure 3.10, the proposed level shifter (I) successfully exhibits that the high-voltage-level is shifted from 10 to 20 V. The experimental results show that the depletion-mode TFT in the proposed level shifter (I) is easily turned off by employing two clock signals with 180° out of phase.
Figure 3.7 Simulation result of the conventional level shifter employing depletion-mode a-IGZO TFTs.
Figure 3.8 Simulation result of the proposed level shifter (I) employing depletion-mode a-IGZO TFTs.
Figure 3.9 Optical image of the proposed level shifter (I).
Figure 3.10 Measured output waveform of the proposed level shifter (I).
3.2.5 Conclusion

A new depletion-mode a-IGZO TFT level shifter (I) without any additional power sources and input signals was proposed and successfully fabricated. The proposed level shifter (I) employed two clock signals with 180° out of phase in order to apply a negative voltage to the Vgs of TFTs. The experimental results showed that the proposed level shifter (I) was designed to easily turn off the depletion-mode a-IGZO TFTs. The proposed level shifter with a depletion-mode device would be an important building block for an oxide TFT display.
3.3 Level shifter with a full-swing output

3.3.1 Introduction

In the previous section, the depletion-mode a-IGZO TFT level shifter (I) was proposed and discussed. The level shifter was designed to easily turn off the depletion-mode a-IGZO TFTs by employing two clock signals with 180° out of phase. However, the low-voltage-level output of the level shifter (I) is greater than VSS (0V), whereas the high-voltage-level output of the level shifter (I) successfully reaches VDD.

The well-known CMOS technologies [92] are not suitable for an oxide TFT due to the absence of a good p-type TFT. Furthermore, the NMOS level shifter employing widely used a-Si and poly-Si TFTs [93], whose output swings fully from VDD to VSS without additional power sources and input signals, has been scarcely reported.

In this section, a new depletion-mode a-IGZO TFT level shifter (II) which swings fully from VDD to VSS without any additional power source and input signals are proposed and discussed. The level shifter (II) employs two clock signals with 180° out of phase and one discharging TFT in order to turn off the depletion-mode a-IGZO TFTs and increase the channel resistance of a load TFT, respectively.
3.3.2 Fabrication and characteristics of a-IGZO TFTs

The bottom-gate a-IGZO TFTs with an etch-stopper structure by using a six-mask process were fabricated.

Details of the device fabrication have been described in the section 3.2.
3.3.3 Design of level shifter (II)

Figure 3.11 show the schematics of the conventional level shifter and the proposed one (I). As shown in Figure 3.11 (a), when the clock signal of a high-voltage-level is applied to the gate of driver TFTs (T3c and T6c), the outputs (Vout_1 and Vout_2) of a low-voltage-level are generated. The outputs depend on the resistance ratio of the load TFTs (T2c and T5c) to driver TFTs so that the low-voltage-level of the outputs is always greater than VSS. Also, as shown in Figure 3.11 (b), the low-voltage-level of an output in the proposed level shifter (I) is determined by the relationship as follows.

\[
V_{\text{out\_low}} = \left\{ \frac{R_{T3p}}{R_{T2p} + R_{T3p}} \times (V_{DD} - V_{SS}) \right\} + V_{SS} \quad (2)
\]

where \(R_{T2p}\) and \(R_{T3p}\) are the resistances of T2p and T3p, respectively. Therefore, the output of the proposed level shifter (I) could not swing fully from VDD to VSS.

In order to overcome this problem, a new level shifter (II) which employs two clock signals (CLK and CLKB) with 180° out of phase and a discharging TFT (T4p) is proposed as shown in Figure 3.12 (a). Figure 3.13 shows the illustration of the operation mechanism of the proposed level shifter (II).

CLK and CLKB are connected to the gate and source of T3p and T4p, respectively. As shown in Figure 3.12 (b), when CLK and CLKB are low- and high-voltage (period [A]), respectively, the driver TFT (T3p) is completely turned off although a depletion-mode a-IGZO TFT is used. It is
possible because the Vgs of the driver TFT becomes negative by CLK and CLKB. Therefore, a high-voltage-level of the output in the proposed level shifter (II) would be equal to VDD [see Figure 3.13].

On the contrary, when CLK and CLKB are high- and low-voltage (period [B]), respectively, the driver TFT is turned on so that the output is maintained at a low-voltage-level. In the proposed level shifter (II), the gate voltage of T2p can be lowered by employing T4p in order to discharge the node “I.” As R_{T2p} is extremely high, the low-voltage-level of an output could reach VSS [see Figure 3.13].

Therefore, in the proposed level shifter (II), the depletion-mode a-IGZO TFTs would be successfully turned off, and the output swing fully from VDD to VSS. The proposed level shifter (II) does not require any additional signals because an even number of clock signals has been used in most gate drivers [22], [98].
Figure 3.11 Schematics of (a) the conventional level shifter and (b) the proposed one (I).
Figure 3.12 (a) Schematic and (b) timing chart of the proposed level shifter (II).
Figure 3.13 Illustration of the operation mechanism of the proposed level shifter (II).
3.3.4 Simulation and experiment

The SPICE simulation was performed to verify the proposed level shifter (II). Of the extracted SPICE parameters [97], CGSO (gate–source capacitance) and CGDO (gate–drain capacitance) are 0.54 nF/m. The level shifter is operated with a frequency of 12.5 kHz, and the voltages are 20 (for VDD) and 0-10 V (for CLK and CLKB), respectively.

Figure 3.14 shows the simulation results of the proposed level shifter (II). The simulation results show that the input voltage of 0–10 V is shifted to the output voltage of 0–20 V. Also, they show that a negative voltage is successfully applied to the Vgs of T3p and T4p by CLK and CLKB so that these depletion-mode TFTs are easily turned off. The node “I” is maintained to a low voltage at the period of CLK of a high-voltage-level and CLKB of a low-voltage-level. Therefore, the channel resistance of T2p increases greatly so that the low-voltage-level of an output could reach 0 V.

T3p and T4p of the proposed level shifter (II) would be degraded with the operating time due to gate bias stress by the CLK signal as shown in Figure 3.15. When the CLK signal is high, a positive voltage (10V) is applied to the gate of T3p and T4p. On the contrary, when the CLK signal is low, a negative voltage (-10V) is applied to the gate of T3p and T4p. The stability of a-IGZO TFTs under the severe stress conditions, such as high gate bias voltage, high temperature, and light illumination, has been analyzed. Figure 3.16 shows the threshold voltage shift of a-IGZO TFTs with high gate-bias stresses (+/- 30 V) under light illumination (60 °C). A threshold voltage is shifted to negative voltage direction under negative bias stress and to positive voltage direction under positive bias stress. a-IGZO TFTs undergo more severe shifts in threshold voltage during negative-bias
illumination stress rather than positive-bias illumination stress. Therefore, the threshold voltages of T3p and T4p in the proposed level shifter (II) would be shifted negatively with the operation time because T3p and T4p are under positive and negative bias stress alternatively with the same duty ratio.

The SPICE simulation was performed to verify the driving characteristics of the proposed level shifter (II) under the severe bias stress condition. Figure 3.17 shows that the proposed level shifter (II) works without any problem until a threshold voltage is -9.79 V. It is possible because the Vgs of T3p and T4p becomes negative (-10V) by CLK and CLKB so that these depletion-mode TFTs are easily turned off.

The proposed level shifter (II) employing a-IGZO TFTs has been fabricated. Figure 3.18 shows the optical image of the proposed level shifter (II). The channel lengths of all TFTs are 10 μm. The channel widths of TFTs are 20 (for T1p), 100 (for T2p), 1000 (for T3p), and 60 μm (for T4p), respectively. The bootstrap capacitor is 1.5 pF. The overlap length of gate–drain in TFTs is 4 μm. The depletion-mode a-IGZO TFT level shifter (II) was measured by 0–10 V square wave inputs. As shown in Figure 3.19, the proposed level shifter (II) successfully exhibits that the high-voltage-level is shifted from 10 to 20 V, and the low-voltage-level reaches 0 V.

The experimental results show that the depletion-mode TFTs in the proposed level shifter (II) are easily turned off by employing two clock signals with 180° out of phase. In particular, the proposed circuit employing n-type depletion mode IGZO TFTs has a wide swing output without any additional power sources and input signals.
Figure 3.14 Simulation result of the proposed level shifter (II).
Figure 3.15 Gate bias stress condition of T3p and T4p in the proposed level shifter (II).
Figure 3.16 Evolution of the transfer curves as a function of the applied stress time under light illumination; (a) Vgs = -30 V, (b) Vgs = +30 V.
Figure 3.17 Simulation results of the output waveform.

[Threshold voltage: $-2.59\, \text{V (Initial)}$, $-9.79\, \text{V (Degraded)}$]
Figure 3.18 Optical image of the proposed level shifter (II).
Figure 3.19 Measured output waveform of the proposed level shifter (II).
3.3.5 Power consumption of the level shifter (II)

The SPICE simulation has been performed in order to compare the power consumptions of the proposed and the conventional level shifters. As shown in Figure 3.20 and 3.21, the estimated power consumptions of the conventional level shifter, the proposed level shifter (I) and (II) are 1.28, 1.05, and 0.31 mW, respectively. In the conventional level shifter and the proposed level shifter (I), the dissipated current through the load TFTs and the driver ones with large channel width is very great.

Figure 3.20 shows the simulation results of the dissipated currents of the proposed level shifter (I) and (II). In the proposed level shifter (II), the dissipated current through T2p (W= 100 μm) and T3p (W= 1000 μm) path, where channel widths are very large, are considerably reduced due to T4p, although the short circuit current occurs through T1p (W= 20 μm) and T4p (W= 60 μm) path, where channel widths are small. The dissipated current through T2p and T3p path of the proposed level shifter (II) is 8.8 μA, whereas that of the proposed level shifter (I) is 52.6 μA. It is possible because, when the CLK signal is high, the gate voltage of T2p is lowered by T4p.

The measured power consumption of the proposed level shifter (II) is 0.30 mW at a clock frequency of 12.5 kHz, whereas that of Hwang’s level shifter was 0.46 mW at a clock frequency of 10 kHz [96].
Figure 3.20 Simulation results of the dissipated currents of the proposed level shifter (I) and (II).
Figure 3.21 Simulation results of the dissipated currents of the conventional level shifter.
3.3.6 Conclusion

A new depletion-mode a-IGZO level shifter (II), which employs two clock signals with 180° out of phase and a discharging TFT, has been proposed and fabricated. The experimental results have showed that the proposed level shifter (II) has been designed to easily turn off the depletion-mode TFTs. Furthermore, the proposed level shifter (II) has exhibited an output characteristic which swings fully from VDD to VSS without any additional power sources and input signals, although only NMOS devices have been used.

The power consumption is 0.30 mW at a clock frequency of 12.5 kHz.
3.4 Shift register (I) with two low-voltage-level signals

3.4.1 Introduction

Integrating a shift register on the panel is very important in the display technology because it can reduce the cost of external IC chip. Most of a-IGZO TFTs are inherently a depletion-mode device rather than the widely used enhancement-mode device [83]–[88]. In addition, it is well known that a severe negative shift in the threshold voltage of oxide TFTs occurs during negative bias illumination stress or only light illumination [57], [70], [71]. Therefore, the driving circuit which can be operated in depletion mode would be indispensable for an oxide TFT display.

In this section, new shift register (I) employing depletion-mode a-IGZO TFTs are proposed and discussed. The proposed shift register (I) employs only two low-voltage-level power signals in order to apply a negative voltage at the gate–source voltage (Vgs) of depletion-mode a-IGZO TFTs.
3.4.2 Fabrication and characteristics of a-IGZO TFTs

The bottom-gate a-IGZO TFTs with an etch-stopper structure by using a six-mask process were fabricated. A 200-/50-nm-thick AlNd/Mo dual layer as gate electrode was deposited by direct-current magnetron sputtering on a glass substrate. A 300-nm-thick SiO$_2$ film as a gate insulator was deposited by plasma-enhanced chemical vapor deposition (PECVD) at 350 °C, and a 60-nm-thick IGZO (In:Ga:Zn = 1:1:1) layer as an active material was sputtered at room temperature. The active layer was patterned by wet-etching, and a 80-nm-thick SiO$_2$ layer as an etch-stopper was deposited by PECVD at 250 °C. A 300-nm-thick Mo/MoTi dual layer was deposited for source/drain electrodes. After patterning source/drain electrodes, a 300-nm-thick SiO$_2$ passivation layer was deposited by PECVD at 250 °C, and a 50-nm-thick indium tin oxide layer was formed for pixel electrodes. Finally, the devices were annealed for 2 h in an air ambient at 300 °C.

Figure 3.22 shows the transfer characteristics of a-IGZO TFTs. The channel width and length of a-IGZO TFT are 20 and 10 μm, respectively. The device exhibits the electrical properties such as a field effect mobility of 11.9 cm$^2$/V · s, a threshold voltage of −0.6 V, and a sub-threshold slope of 0.25 V/dec. It should be pointed out that the a-IGZO TFT operates in the depletion-mode rather than the enhancement-mode.
Figure 3.22 Transfer characteristics of a-IGZO TFT.
3.4.3 Design of shift register (I)

In the TFTs of the driving circuit, the low-voltage-level applied to a gate electrode is equal to that applied to a source (or drain) electrode [21], [22]. Vgs becomes zero under the “off” condition so that it is extremely difficult to turn off the depletion-mode a-IGZO TFTs in the driving circuit due to considerable drain–source current.

A widely used shift register with an enhancement-mode device is shown in Figure 3.23. It is important that the voltage of a Q-node should be a high level in order to generate an output pulse. However, in the case of the conventional shift register employing depletion-mode a-IGZO TFTs, the voltage of a Q-node could be discharged through T1, T2, and T3 because Vgs of these TFTs becomes zero for the generation period of an output pulse as shown in Figure 3.24. Therefore, the conventional shift register could exhibit a distorted output pulse.

In order to overcome a malfunction of circuits due to a leakage current of depletion-mode TFTs, a new shift register (I) with two low-voltage-level signals (VGL and VGL1) is proposed. Figure 3.25 shows the schematic and timing chart of the proposed shift register (I). As shown in Figure 3.25(a), the output sections of the proposed shift register are divided into two parts. The gates of T1a and T1b are connected to the output node of the (A) part in the previous (n–2) stage, and the output pulse of the (B) part in the previous (n–2) stage is supplied to the drain of T1a. In addition, the output pulse of the (A) part in the present (n) stage is supplied to node “I” by T1c. The gate of T2 is connected to the output node of the (A) part in the next (n+2) stage. During the generation period of an output pulse [period “(2)”], Vg (n–2), Vc(n–2), and Vc(n + 2) are kept to VGL, VGL1, and VGL1, respectively.
The voltage of VGL1 is less than that of VGL. Therefore, the Vgs of T1a, T1b, and T2 becomes negative during an output pulse generation.

The specific operation mechanism of the proposed shift register (I) is as follows [see Figure 3.26-3.29].

**Stage 1:** When T1a and T1b are turned on by the output pulse of Vc(n-2), a Q-node is charged to a high-voltage by the output pulse of Vg(n-2). At the same time, a Qb-node becomes a low-voltage (VGL1) because T5 is turned on by a Q-node of a high-voltage [see Figure 3.26].

**Stage 2:** When CLK(x) of a high-voltage is applied to the drain of T6a and T6b, a Q-node is bootstrapped by the parasitic capacitances of T6a and T6b. Therefore, the output pulses [Vc(n) and Vg(n)] are generated through T6a and T6b, respectively, which is fully turned on [see Figure 3.27].

**Stage 3:** The output pulse of Vc(n) in the present (n)stage is supplied to node “I” by T1c. During the generation period of an output pulse, Vg(n – 2), Vc(n – 2), and Vc(n + 2) are kept to VGL, VGL1, and VGL1, respectively. The Vgs of T1a, T1b, and T2 becomes negative during an output pulse generation [see Figure 3.28].

**Stage 4:** After the output pulse is generated, a Q-node is discharged to VGL when T2 is turned on by the output pulse of Vc(n+2). T3 is turned on periodically by CLK(x-1) so that the voltage of a Q-node is maintained to a low voltage [see Figure 3.29].
Figure 3.23 (a) Schematic and (b) timing chart of the conventional shift register.
Figure 3.24 Illustration of the operation mechanism of the conventional shift register; (a) Schematic and (b) timing chart.
Figure 3.25 (a) Schematic and (b) timing chart of the proposed shift register (I).
Figure 3.26 Illustration of the operation mechanism of the proposed shift register (I)-1; (a) Schematic and (b) timing chart.
Figure 3.27 Illustration of the operation mechanism of the proposed shift register (I)-2; (a) Schematic and (b) timing chart.
Figure 3.28 Illustration of the operation mechanism of the proposed shift register (I)-3.

Q-node:

$\rightarrow V_{GH}$

$V_{gate}$:

$V_{GL1}$

$V_{source}$:

$V_{GL}$ or $V_{GH}$

$V_{gs_T1a,T2} = (V_{GL1} - V_{GL}), V_{GL1} < V_{GL}$

$V_{gs_T1b} = (V_{GL1} - V_{GH}), V_{GL1} << V_{GH}$
Figure 3.29 Illustration of the operation mechanism of the proposed shift register (I)-4; (a) Schematic and (b) timing chart.
3.4.4 Simulation and experiment

The SPICE simulation was performed to analyze the conventional shift register and the proposed shift register (I). Of the extracted SPICE parameters [97], CGSO (gate–source capacitance) and CGDO (gate–drain capacitance) are 0.45 nF/m. The shift register is operated with a clock frequency of 12.5 kHz by using four-phase overlapped clock signals [21], [22]. The voltages are 20, −5, and −10 V for VGH, VGL, and VGL1, respectively.

Figure 3.30 shows the SPICE simulation results of the conventional shift register using a-IGZO TFTs. It is observed that the voltage of a Q-node at the first stage is discharged for an output pulse generation time due to considerable current of TFTs at the Vgs of 0V. Therefore, the conventional shift register does not work because the charges were not delivered any more to the next stage by the output pulse distortion at the first stage.

Figure 3.31 shows the simulation results of the output waveforms of the proposed shift register (I). The output pulse of the last stage is generated without any distortion. It is because the voltage of a Q-node can be maintained to a high level during the generation period of a high-voltage output pulse. The simulation result shows that a negative voltage is successfully applied to Vgs of charging TFTs (T1a and T1b) and the discharging TFT (T2) in the proposed shift register (I) so that these depletion-mode TFTs are easily turned off. On the other hand, T3 has Vgs = 0V for the short output generation period so that the voltage of a Q-node could get lower a bit, as shown in Figure 3.32. Although the voltage of a Q-node gets lower, the proposed shift register (I) works without any problem until a threshold voltage is −4.5 V.
Figure 3.33 shows the optical images of the conventional shift register and the proposed shift register (I) with ten stages employing a-IGZO TFTs. The channel lengths of all TFTs are 10 μm. The channel widths of TFTs in the proposed shift register (I) are 180 μm (T1a and T1b), 10 μm (T1c), 100 μm (T2), 50 μm (T3), 10 μm (T4), 60 μm (T5), 120 μm (T6a), 1200 μm (T6b), 24 μm (T7a), and 240 μm (T7b). The channel widths and lengths of TFTs in the conventional shift register are identical to those of TFTs performing the same function in the proposed one.

As shown in Figure 3.34, the proposed shift register (I) successfully exhibits a high-voltage output pulse without any distortion, whereas the output pulse of the conventional shift register is not generated. The experimental results show that the depletion-mode TFTs in the proposed shift register (I) are successfully turned off. Also, as shown in Figure 3.35, it is confirmed that the charges are carried into the next stages, which successfully generate the shifted output pulse in serial order. Figure 3.36 shows output waveforms as a function of VGL1 in the proposed shift register (I). When the Vgs of depletion-mode TFTs is -5 V, the high-voltage output pulse is generated. However, as the Vgs is -1 V, the output pulse is considerably distorted. When the Vgs reaches 0 V, the output pulse is not generated.

Figure 3.37 shows that the proposed shift register (I) is driven at a maximum clock frequency of 417 kHz, which is quite enough to be integrated as a gate driver for an ultrahigh-resolution and high-frame-rate display [5].
Figure 3.30 Simulation result of the conventional shift register.
Figure 3.31 Simulation results of the proposed shift register (I); (a) Voltage change in various nodes and (b) output waveforms.
Figure 3.32 Simulation results of the output waveforms of the proposed shift register (I) [threshold voltage: –0.6 V (initial) and –4.5 V (shifted)].
Figure 3.33 Optical images of (a) the conventional shift register and (b) the proposed shift register (I).
Figure 3.34 Measured output waveforms of (a) the conventional shift register and (b) the proposed shift register (I).
Figure 3.35 Measured output waveforms in each stage of the proposed shift register (I).
Figure 3.36 Output waveforms as a function of $V_{GL1}$; $V_{GL1} =$ (a) -10, (b) -6, (c) -5V.
Figure 3.37 Measurement results of an output node in the last stages at a high clock frequency of 417 kHz.
3.4.5 Power consumption of shift register (I)

The SPICE simulation was performed for the analysis of the power consumption of the proposed shift register (I). As shown in Figure 3.38, the power of the proposed shift register (I) is mostly dissipated by the clock signal applied to a buffer TFT (T6b). The dissipated current by T6b is more than 70% of the overall dissipated current.

T2, T3, T4 and T5 in the proposed shift register (I) may increase the power consumption. However, the increased power consumption by these TFTs would not be large because the channel widths of these TFTs (T4: 10 μm, T5: 60 μm, T2: 100 μm and T3: 50 μm) are very small and the currents flow through these TFTs during a very short period. Among all TFTs in a shift register, T6b has the considerable channel width (1200 μm). In general, the channel width of the buffer TFT is about ten times larger than that of other TFTs. Therefore, the buffer TFT has very large gate-drain overlap capacitance. For this reason, the power consumption of a shift register is mostly dissipated by a clock signal applied to the buffer TFT periodically.

The power consumption of the proposed shift register with ten stages measured experimentally is 3.8 mW at the clock frequency of 13.2 kHz, which is the display driving condition of the resolution of WXGA, and a frame rate of 60 Hz. The sizes of TFTs and driving voltage (30 V) in the proposed shift register (I) are large enough to be applied to a very high-driving-speed display. The sizes of TFTs and driving voltage could be optimized according to the resolution and frame rate of a display. The overlap length of the gate–drain in our TFTs is 5 μm. The large overlap length of the gate–drain, which is caused by an etch-stopper structure, could be reduced by a fabrication technology. Therefore, the power consumption
would be considerably reduced when the sizes of TFTs, driving voltage, and overlap area of the gate–drain are optimized.
Figure 3.38 Simulation results of the dissipated currents of TFTs in the proposed shift register (I).
3.4.6 Conclusion

A new depletion-mode a-IGZO TFT shift register (I) employing two low-voltage-level signals has been proposed and fabricated. The experimental results have shown that the proposed shift register (I) successfully exhibited a high-voltage output pulse without any distortion and a maximum clock frequency of 417 kHz. A negative voltage is successfully applied to the Vgs of depletion-mode a-IGZO TFTs due to two low-voltage-level signals so that these TFTs are easily turned off. The proposed shift register (I) would be an important building block for a depletion-mode oxide TFT and a high-frame-rate display.
3.5 Shift register (II) with a single low-voltage-level signal

3.5.1 Introduction

Most shift registers have required additional signals such as a low-voltage-level power source and a clock of a complicated waveform, in order to apply a negative voltage to the $V_{gs}$ of the depletion-mode a-IGZO TFTs [64]. In the previous section, the depletion-mode a-IGZO TFT shift register employing two low-voltage-level power signals has been discussed. In the shift register, an additional low-voltage-level power signal ($-10$ V), which is less than the original one ($-5$ V), has been required in order to turn off the depletion-mode a-IGZO TFTs. Therefore, the peak-to-peak voltage of clock signals becomes larger so that the power consumption would increase.

In this section, a new depletion-mode a-IGZO TFT shift register (II) employing only one low-voltage-level power signal without an additional signal are proposed and discussed. In the proposed shift register (II), an additional low-voltage-level power signal is not required, and the peak-to-peak voltage of clock signals becomes smaller than that of the proposed shift register (I). Therefore, the power consumption of the proposed shift register (II) would considerably be decreased.
3.5.2 Fabrication and characteristics of a-IGZO TFTs

The bottom-gate a-IGZO TFTs with an etch-stopper structure by using a six-mask process were fabricated. A 200-/50-nm-thick AlNd/Mo dual layer as gate electrode was deposited by direct-current magnetron sputtering on a glass substrate. A 300-nm-thick SiO₂ film as a gate insulator was deposited by plasma-enhanced chemical vapor deposition (PECVD) at 350 °C, and a 50-nm-thick IGZO (In:Ga:Zn = 1:1:1) layer as an active material was sputtered at room temperature. The active layer was patterned by wet-etching, and a 50-nm-thick SiO₂ layer as an etch-stopper was deposited by PECVD at 250 °C. A 200-nm-thick Mo layer was deposited for source/drain electrodes. After patterning source/drain electrodes, a 200-nm-thick SiO₂ passivation layer was deposited by PECVD at 250 °C, and a 50-nm-thick indium tin oxide layer was formed for pixel electrodes. Finally, the devices were annealed for 2 h in an air ambient at 300 °C.
### 3.5.3 Design of shift register (II)

A new shift register (II) employing only one low-voltage-level power signal without an additional signal is proposed. The proposed shift register (II) employs the series-connected two-transistor (STT) structure for charging and discharging TFTs.

Figure 3.39 shows the schematic of the STT structure. TFT-A and TFT-B are connected in series, and a high voltage from an output node is supplied to the S-node. During high-voltage output pulse generation [period “(2)” in Fig. 1(c)], $V_g(n-2)$ and $V_g(n+2)$ are maintained to a low voltage level (i.e., $V_{GL}$). In addition, the S-node becomes a high voltage level due to a high-voltage output pulse of $V_g(n)$. Therefore, the $V_{gs}$ of TFT-A becomes negative so that the voltage of the Q-node can be maintained to a high voltage level during the generation period of a high-voltage output pulse as follows:

$$V_{gs,A-TFT} \approx (V_{GL} - V_{GH}), \quad V_{GL} \ll V_{GH}$$

In the STT structure, a negative voltage can be applied to the $V_{gs}$ of depletion-mode a-IGZO TFTs, although only one low-voltage-level power signal is employed. As shown in Figure 3.40(a), the STT structure is employed for charging and discharging TFTs in the proposed shift register (II). After the Q-node is charged by the output pulse of the previous $(n-2)$ stage during period “(1),” T1A and T2A are turned off during the generation period of an output pulse by employing the STT structure. Therefore, the proposed a-IGZO TFT shift register (II) would generate successfully an output pulse without distortion.
The specific operation mechanism of the proposed shift register (II) is as follows [see Figure 3.41-3.44].

**Stage 1:** When T1A and T1B are turned on by the output pulse of Vg(n-2), a Q-node is charged to a high-voltage. At the same time, a Qb-node becomes a low-voltage (VGL) because T5 is turned on by a Q-node of a high-voltage [see Figure 3.41].

**Stage 2:** When CLK(x) of a high-voltage is applied to the drain of T6, a Q-node is bootstrapped by the parasitic capacitances of T6. Therefore, the output pulse of Vg(n) is generated through T6 which is fully turned on [see Figure 3.42].

**Stage 3:** The output pulse of Vg(n) in the present (n)stage is supplied to node “S1 and S2” by T1C and T2C. During the generation period of an output pulse, Vg(n-2) and Vg(n+2) are kept to VGL. The Vgs of T1A and T2A becomes negative during an output pulse generation [see Figure 3.43].

**Stage 4:** After the output pulse is generated, a Q-node is discharged to VGL when T2A and T2B are turned on by the output pulse of Vg(n+2). T3 is turned on periodically by CLK(x-1) so that the voltage of a Q-node is maintained to a low voltage [see Figure 3.44].
Figure 3.39 Schematic of the series-connected two-transistor (STT) structure.
Figure 3.40 (a) Schematic and (b) timing chart of the proposed shift register (II).
Figure 3.41 Illustration of the operation mechanism of the proposed shift register (II)-1; (a) Schematic and (b) timing chart.
Figure 3.42 Illustration of the operation mechanism of the proposed shift register (II)-2; (a) Schematic and (b) timing chart.
\[ V_{gs-A-TFT} \approx (V_{GL} - V_{GH}), \quad V_{GL} \ll V_{GH} \]

Figure 3.43 Illustration of the operation mechanism of the proposed shift register (II)-3.
Figure 3.44 Illustration of the operation mechanism of the proposed shift register (II)-4; (a) Schematic and (b) timing chart.
3.5.4 Simulation and experiment

The SPICE simulation was performed to verify the proposed shift register (II). The SPICE model parameters were extracted from the fabricated a-IGZO TFTs. Among extracted SPICE parameters [97], gate–source and gate–drain capacitances are 0.27 nF/m. The shift register (II) is operated with a frequency of 13.9 kHz by using four-phase overlapped clock signals. The voltages are 20 and −5 V for high-voltage-level power signal (VGH) and VGL, respectively.

Figure 3.45 shows the simulation results of S-node voltage in the proposed shift register (II). During the generation period of a high-voltage output pulse, the voltages of S1-node and S2-node are maintained to more than 15 V. Therefore, the Vgs of T1A and T2A becomes less than −20 V. The simulation result shows that a negative voltage is applied successfully to the Vgs of the charging TFT (i.e., T1A) and the discharging TFT (i.e., T2A) so that these depletion-mode TFTs are easily turned off. As shown in Figure 3.46(a), the output pulse of a high voltage is generated without distortion. This is possible because the voltage of the Q-node can be maintained to a high voltage during the generation period of a high-voltage output pulse. Also, as shown in Figure 3.46(b), it can be confirmed that the charges are carried into the next stages so that sequentially generate the shifted output pulses.

The proposed shift register (II) with ten stages employing depletion-mode a-IGZO TFTs was fabricated. The channel lengths of all TFTs are 10 μm. The channel widths of TFTs in the proposed shift register (II) are 180 (for T1A and T1B), 10 (for T1C and T2C), 100 (for T2A and T2B), 50 (for T3), 10 (for T4), 60 (for T5), 1200 (for T6), and 240 μm (for T7). The
overlap length of the gate–drain in TFTs is 3 μm. The width and length of the unit circuit area of the proposed shift register (II) are 300 and 800 μm, respectively.

Figure 3.47 shows the optical image of the fabricated shift register (II). As shown in Figure 3.48, the proposed shift register (II) exhibits successfully a high-voltage output pulse without distortion. It could be expected that the depletion-mode a-IGZO TFTs in the proposed shift register (II) would be turned off successfully.
Figure 3.45 Simulation results of S-node voltage in the proposed shift register (II).
Figure 3.46 Simulation results of the proposed shift register (II). (a) Q-node voltage and output waveforms and (b) output waveforms in several stages.
Figure 3.47 Optical image of the proposed shift register (II).
Figure 3.48 Output waveform of the last (10th) stage in the proposed shift register (II).
3.5.5 Power consumption of shift register (II)

Figure 3.49(a) shows the clock signals of the proposed shift register (II) and the previous shift register (I). The previous shift register (I) required an additional low-voltage-level power signal, which is less than the original one. However, the proposed shift register (II) employs only one low-voltage-level power signal. Therefore, the peak-to-peak voltage of clock signals of the proposed shift register (II) is smaller than that of the previous one. In addition, the overlap length of the gate–drain in TFTs of the proposed shift register (II), which affects greatly the power consumption, is 3 μm, whereas that of the previous one (I) was 5 μm as shown in Figure 3.49(b). The power consumption $P$ is determined by the relationship as follows:

$$P = f \cdot C \cdot V^2$$

where $f$, $C$, and $V$ are the frequency, capacitance, and voltage, respectively. The power consumption of the proposed shift register (II) would be decreased considerably compared with the previous one (I) because the driving voltage and capacitance are decreased.

Figure 3.50 shows the measured power consumption of the proposed shift register (II) as a function of $V_{GH}$. The power consumption of the proposed shift register (II) with ten stages is 1.67 mW at the $V_{GH}$ of 20 V, the $V_{GL}$ of −5 V, and the clock frequency of 13.9 kHz, whereas that of the previous one (I) was 3.8 mW.
Figure 3.49 (a) Schematic of the clock signal waveform and (b) optical image of TFT.
Figure 3.50 Power consumption of the proposed shift register (II) as a function of VGH.
3.5.6 Conclusion

A new depletion-mode a-IGZO TFT shift register (II) employing only one low-voltage-level power signal without an additional signal has been proposed and fabricated. The STT structure in the proposed shift register (II) has enabled the Vgs of depletion-mode a-IGZO TFTs to be negative so that these TFTs have been turned off completely.

The experimental results showed that the proposed shift register (II) exhibited successfully a high-voltage output pulse without distortion. In the proposed shift register (II), the peak-to-peak voltage of clock signals and the overlap length of the gate–drain in TFTs are smaller than those of the previous shift register (I). The power consumption of the proposed shift register (II) with ten stages is 1.67 mW at the VGH of 20 V, the VGL of −5 V, and the clock frequency of 13.9 kHz.
3.6 Shift register (III) with a node-shared structure

3.6.1 Introduction

The driving circuits employing depletion-mode oxide TFTs require many TFTs in addition to additional power sources and input signals in order to turn off depletion-mode oxide TFTs [64]. It should be pointed out that many TFTs and signal lines would increase the circuit area. The large circuit area of oxide-based display may be a critical issue in respect that a display panel with a narrow bezel is the general trend.

In this section, a new shift register (III) employing a node-shared structure, where Q-node and Qb-node of adjacent two stages are shared, respectively is proposed and discussed. The proposed shift register (III) generates two output pulses at only one stage. The node-shared structure has the advantage that signal lines such as input clock and power source, in addition to the number of TFTs, are reduced for the layout of the shift register. The proposed shift register (III) requires 14 TFTs, 3 clock lines, and 3 power source lines for two output pulses, whereas the previous shift registers consisted of more than 22 TFTs, 4 clock lines, and 6 power source lines.
3.6.2 Fabrication and characteristics of a-IGZO TFTs

The bottom-gate a-IGZO TFTs with an etch-stopper structure by using a six-mask process were fabricated. Details of the device fabrication have been described in the section 3.5.
3.6.3 Design of shift register (III)

The conventional shift register has usually one Q-node and one Qb-node in one stage. Several node-control TFTs in a shift register are required in order to charge or discharge Q-node and Qb-node [16]–[25].

Figure 3.51 shows the schematic and timing chart of the proposed shift register (III). In the proposed shift register (III), Q-node and Qb-node of adjacent two stages are shared, respectively. Therefore, the number of node-control TFTs is reduced by half compared with that of the previous shift register. In addition, signal lines such as input clock and power source are reduced. The proposed shift register (III) employs six-phase overlapped clock signals, one positive power source (VGH), and two negative power sources (VGL and VGL1). Only three clock signals among six clock signals are required at one stage, as shown in Figure 3.51(a). The overlapped clock signals are usually used to improve the characteristics of an output pulse in high-frequency driving [17], [22], [99].

However, the characteristics of two output pulses generated at one stage could be different due to a node-shared structure. As shown in Figure 3.52, the voltage of a Q-node is changed during the generation of two output pulses [Vg(n) and Vg(n+1)]. In other words, the voltage of a Q-node is changed at the time when two output pulses are pulled down to low-voltage-level. Both CLK(x) and CLK(x+1) are maintained at a high voltage just before the pull-down period of the first output pulse [Vg(n)], whereas only CLK(x+1) is still maintained at a high voltage just before the pull-down period of the second output pulse [Vg(n+1)].

Therefore, the falling times of two output pulses could be considerably different due to the voltage change of a Q-node. When the falling times of
output pulses are different, the image quality of a display would be deteriorated. In order to overcome this problem, as shown in (III) part of Figure 3.51(a), T10 discharges an output node of Vg(n+1) by using the output pulse of Vc(n+4) so that the falling time of Vg(n+1) is adjusted.

In the first stage, the START pulse instead of the output pulses such as Vc(n−2), Vc(n−1), and Vg(n−2) is supplied. In addition, the last stage uses the output pulses such as Vc(n+4) and Vc(n+5) generated from a dummy stage, which is not connected to a gate line.

The specific operation mechanism of the proposed shift register (III) is as follows [see Figure 3.53-3.56].

**Stage 1:** When T1 is turned on by the output pulse of Vc(n−2) in the previous (n−2) stage, a Q-node is charged to a high voltage of the output pulse of Vg(n−2). At the same time, a Qb-node becomes a low-voltage (VGL1) because T5 is turned on by Q-node of high voltage [see Figure 3.53].

**Stage 2:** When CLK(x) of high voltage is applied to the drain of T6a and T6b, as shown in (I) part of Figure 3.51(a), a Q-node is bootstrapped by the parasitic capacitance values of T6a and T6b. Therefore, the first output pulse [Vg(n)] is generated through T6b, which is fully turned on. Subsequently, the second output pulse [Vg(n+1)] is generated through T8b when CLK(x+1) of high voltage is applied to the drain of T8a and T8b, as shown in (II) part of Figure 3.51(a) [see Figure 3.54].

**Stage 3:** T10 discharges an output-node of Vg(n+1) by using the output pulse of Vc(n+4) so that the falling-time of Vg(n+1) is adjusted [see Figure 3.55].

**Stage 4:** After two output pulses are generated, a Q-node is discharged to VGL when T2 is turned on by the output pulse of Vc(n+5). T3 is periodically
turned on by CLK(x−1) so that a Q-node is maintained to VGL1 [see Figure 3.56].
Figure 3.51 (a) Schematic and (b) timing chart of the proposed shift register (III).
Figure 3.52 Voltage change of a Q-node in the proposed shift register (III).
Figure 3.53 Illustration of the operation mechanism of the proposed shift register (III)-1; (a) Schematic and (b) timing chart.
Figure 3.54 Illustration of the operation mechanism of the proposed shift register (III)-2; (a) Schematic and (b) timing chart.
Figure 3.55 Illustration of the operation mechanism of the proposed shift register (III)-3; (a) Schematic and (b) timing chart.
Figure 3.56 Illustration of the operation mechanism of the proposed shift register (III)-4; (a) Schematic and (b) timing chart.
3.6.4 Simulation and experiment

The SPICE simulation was performed to verify the proposed shift register. Among extracted SPICE parameters [97], gate–source and gate–drain capacitance values are 0.27 nF/m. The shift register is operated with a clock frequency of 16.7 kHz. The voltages are 20, −5, and −10 V for VGH, VGL, and VGL1, respectively. The resistance and capacitance of an output node of the shift register are 4 kΩ and 200 pF, respectively.

Figure 3.57 shows the SPICE simulation results of the proposed shift register (III). As shown in Figure 3.57(a), it is observed that a Q-node is bootstrapped twice by two CLK signals. The two output pulses are generated at one stage without any distortion. Also, as shown in Figure 3.57(b), it can be confirmed that the charges are carried into the next stages so that sequentially generate the shifted output pulses.

As aforementioned, the falling times of two output pulses generated at one stage could be considerably different due to the voltage change of a Q-node. Figure 3.58 shows the timing diagram for a reset of an output node by T10. The reset interval means the time gap between the second output pulse [Vg(n+1)] and the output pulse [Vc(n+4)] applied at a gate electrode of T10. As shown in Figure 3.59, the falling time of Vg(n+1) is changed according to reset intervals, whereas the falling time of Vg(n) is not changed. As reset interval decreases, the difference of the falling time between two output pulses becomes smaller. Therefore, in the proposed shift register (III), the falling time of the second output pulse could be adjusted by T10.

On the other hand, the difference of the rising time between two output pulses is considerably large, as shown in Figure 3.59. However, the difference of the rising time of output pulses may not be a problem if the
rising of the output pulses is finished before the data writing time, as shown in Figure 3.58. It is possible because the proposed shift register (III) employs the overlapped clock signals.

The a-IGZO TFT shift register (III) with ten stages was fabricated. The channel widths of TFTs are 180 μm (for T1), 100 μm (for T2), 50 μm (for T3), 10 μm (for T4), 60 μm (for T5), 120 μm (for T6a and T8a), 1200 μm (for T6b and T8b), 24 μm (for T7a and T9a), 240 μm (for T7b and T9b), and 500 μm (for T10), respectively. The channel lengths of all TFTs are 10 μm.

Figure 3.60(a) and (b) shows the optical images of the proposed shift register (III) and the previous one (I), respectively. The circuit area of the proposed shift register (III) for two output pulses is 334 150 μm² (815 μm × 410 μm), whereas that of the previous one (I) is 471 600 μm² (655 μm × 720 μm). The circuit area of the proposed shift register (III) is reduced by about 30%, as compared with that of the previous one (I).

Figure 3.61 and 3.62 show the output waveforms when the reset intervals are 2 and 0 μs, respectively. The proposed shift register (III) successfully exhibits two output pulses at one stage without any distortion. When the reset interval is 2 μs, the falling times between two output pulses generated at one stage are different [OUT9 fall time: 2.68 μs, OUT10 fall time: 3.23 μs]. However, when the reset interval is 0 μs, the difference of the falling time between two output pulses is negligible [OUT9 fall time: 2.65 μs, OUT10 fall time: 2.73 μs]. Therefore, in the proposed shift register (III), the falling time of the second output pulse can be adjusted by T10 so that the uniform output pulses are generated.
Figure 3.57 Simulation results of the proposed shift register (III); (a) Q-node voltage and output pulses in one stage and (b) output pulses in several stages.
Figure 3.58 Timing diagram for a reset of an output node by T10.
Figure 3.59 Simulation results of output pulses of the proposed shift register (III) with various reset intervals.
Figure 3.60 Optical images of (a) the proposed shift register (III) and (b) the previous shift register (I).
Figure 3.61 Output waveforms with the reset intervals of 2 μs.
Figure 3.62 Output waveforms with the reset intervals of 0 μs.
3.6.5 Conclusion

A depletion-mode a-IGZO TFT shift register (III) employing a node-shared structure has been proposed and fabricated. In the proposed shift register (III), Q-node and Qb-node of adjacent two stages are shared, respectively. The proposed shift register (III) requires 14 TFTs, 3 clock lines, and 3 power source lines for two output pulses, whereas the previous shift registers including the shift register (I) consisted of more than 22 TFTs, 4 clock lines, and 6 power source lines.

The experimental results have shown that the proposed shift register (III) has successfully generated two output pulses at one stage. The circuit area of the proposed shift register (III) is reduced by about 30%, as compared with that of the previous one (I).
Chapter 4 Applications of driving circuits employing depletion-mode a-IGZO TFTs

The driving circuits are an important building block for an advanced display employing a-IGZO TFT. A gate driver integration of oxide-based display may be a critical issue in respect that a display panel with a narrow bezel is the general trend. In this chapter, the depletion-mode a-IGZO TFT shift register embedded with a level shifter is introduced and its reliability is discussed.
4.1 Overview

Recently, it has been reported that the negative-bias instability of a-IGZO TFTs under the illumination has been improved, as compared with that of the early stage [53], [70], [100]. However, the negative-bias instability under the illumination, particularly the UV range, may be more investigated to commercialize a-IGZO TFTs. Therefore, the driving circuits that can be operated in the depletion-mode would be useful for an oxide TFT based display.

Also, integrating the gate driver circuits such as the level shifter and the shift register on the panel is very important in the display technology because it can reduce the cost of external IC chip. The gate driver integration employing a-IGZO TFTs may be a very important issue in practical application in order to commercialize them.

In the following sections, the depletion-mode a-IGZO TFT shift registers embedded with a full-swing level shifter are introduced and discussed. a-IGZO TFTs with an etch-stopper structure are fabricated by six-mask process compatible to conventional a-Si:H TFTs fabrication process.

Firstly, the shift register (I) embedded with the level shifter has been designed by employing two clock signals with 180° out of phase and one start signal for the level shifter and two low-voltage-level signals for the shift register, respectively. The level shifter and the shift register consist of six TFTs and one capacitor, and 11 TFTs, respectively. The experimental results have shown that the level shifter and the shift register have been designed to easily turn off the depletion-mode a-IGZO TFTs. The start signal and the clock input signals of −10 ∼ 5 V have been level shifted to the output signals of −10 ∼ 20 V. The depletion-mode a-IGZO TFT shift register (I)
embedded with a full-swing level shifter has successfully exhibited a high-voltage output pulse without any distortion.

Secondly, the shift register (II) embedded with the level shifter employing the depletion-mode a-IGZO TFT without any additional signal is introduced. In addition, the reliability of driving circuits under light illumination is discussed. The shift register (II) embedded with the level shifter successfully exhibits a high-voltage output pulse without distortion at a clock frequency of 100 kHz, which is enough to drive a high-frequency FPD with a frame rate of \( \sim 360 \) Hz and a resolution of full high definition (FHD). The SPICE results show that the shift register (II) embedded with the level shifter would work without any problem, although the threshold voltages of the TFTs degraded by gate bias stress in the level shifter and the shift register are largely shifted to \(-9.3\) and \(+15.2\) V, respectively. Also, the experimentally measured output waveform of the shift register (II) embedded with the level shifter has not been distorted after 240-h driving under 450-nm illumination with an intensity of 1 mW/cm\(^2\) at 60 °C.
4.2 a-IGZO TFT shift register embedded with a full-swing level shifter

4.2.1 Introduction

In the previous chapter, the driving circuit units, such as the level shifter and shift register, employing the depletion-mode a-IGZO TFT was introduced and discussed. The level shifters were designed to easily turn off the depletion-mode a-IGZO TFTs by employing two clock signals with 180° out of phase. Also, the shift registers employed two low-voltage-level power signals or only low-voltage-level power signal to get the high-voltage output pulse without any distortion.

In this section, the shift register (I) embedded with a full-swing level shifter employing the depletion-mode a-IGZO TFTs is proposed. To embed the level shifter in the shift register, a new design of the level shifter and the shift register is necessary. The shift register (I) embedded with the level shifter has been designed by employing two clock signals with 180° out of phase and one start signal for the level shifter and two low-voltage-level signals for the shift register, respectively. The experimental results have shown that the start signal and the four clock signals of $-10 \sim 5$ V have been level shifted to the output signals of $-10 \sim 20$ V through the level shifter. Also, the shift register embedded with a full-swing level shifter have successfully exhibited a high-voltage output pulse without any distortion.
4.2.2 Fabrication and characteristics of a-IGZO TFTs

The bottom-gate a-IGZO TFTs with an etch-stopper structure by using a six-mask process were fabricated. Details of the device fabrication have been described in the section 3.5.

Figure 4.1 shows the transfer characteristics of a-IGZO TFT. The fabricated device exhibits fairly good electrical properties such as a field-effect mobility of $9.16 \text{ cm}^2/(\text{V} \cdot \text{s})$, a threshold voltage of $-1.0 \text{ V}$, and a sub-threshold slope of $0.33 \text{ V/dec}$. It should be pointed out that a-IGZO TFT operates in the depletion-mode rather than the enhancement-mode.
Figure 4.1 Transfer characteristics of the a-IGZO TFT.
4.2.3 Circuit design

In order to embed the level shifter in the shift register (I), the START and CLK level shifters are improved from the level shifter (II) unit as shown in Figure 4.2. Also, in the shift register (I), the new reset method of a Q-node is employed, as compared with the previous shift register.

Figure 4.3 shows the schematics of the START and CLK level shifters and their timing charts. As shown in Figure 4.3(c), the clock output signals (CLKA \sim CLKD) should be maintained to a low voltage during the high-voltage START-O generation [period 1, see Figure 4.4]. Also, the START-O signal should be maintained to a low voltage during the high-voltage clock signals generation [period 2, see Figure 4.5]. Therefore, T3aS, T4aS, T3aC, and T4aC are added for the START and CLK level shifters, as compared with the level shifter (II) unit.

As shown in Figure 4.3(a), when the start input signal (START-I) of a high voltage (5 V) and CLKa and CLKc of a low voltage (\(-10\) V) are supplied to the START level shifter, T3S, T3aS, T4S, and T4aS are turned off so that the output signal of a high voltage (VGH, 20 V) is generated. When START-I of a low voltage is supplied, T3S, T3aS, T4S, and T4aS are alternatively turned on by CLKa and CLKc of a high voltage so that the output signal is maintained to a low voltage of \(-10\) V. Therefore, START-I of \(-10\sim 5\) V is level shifted to START-O of \(-10\sim 20\) V through the START level shifter.

As shown in Figure 4.3(b), when START-I of a high voltage is supplied to the CLK level shifter [period 1 in Figure 4.3(c)], an output signal is maintained to a low voltage of \(-10\) V because T3aC and T4aC are turned on. When CLKa of a high voltage and CLKc of a low voltage are supplied to
the source and the gate of T3C and T4C in the CLK level shifter, respectively, T3C, T3aC, T4C, and T4aC are turned off so that the CLKA of a high-voltage (VGH, 20 V) output signal is generated. On the contrary, when CLKa of a low voltage and CLKc of a high voltage are supplied to the CLK level shifter, T3C, T3aC, T4C, and T4aC are turned on so that the output signal of CLKA is maintained to a low voltage of $-10 \text{ V}$. Therefore, the CLKa of $-10 \sim 5 \text{ V}$ is level shifted to the CLKA of $-10 \sim 20 \text{ V}$ through the CLK level shifter. Also, in the same way, the other input signals of CLKb, CLKc, and CLKd are level shifted to the output signals of CLKB, CLKC, and CLKD, respectively, through the CLK level shifter.

Figure 4.3(c) shows the input signals supplied to the level shifter and the output signals generated through the level shifter.

In the shift register (I), the reset of a Q-node is changed as compared with the previous shift register. A Q-node of the n stage is discharged by the output of the (n + 3) stage, not the (n + 2) stage, because the shift register (I) employs the clock signals with $180^\circ$ out of phase.

Figure 4.7 shows the block diagram of the shift register (I) embedded with a level shifter. The start signal and the four clock signals of $-10 \sim 5 \text{ V}$ are supplied to the level shifters. Those signals are level-shifted to the output signals of $-10 \sim 20 \text{ V}$ through the level shifters, and then, the level-shifted output signals are supplied to the shift register (I).
Figure 4.2 (a) Schematic and (b) timing chart of the level shifter (II) unit.
Figure 4.3 Schematics of the (a) START and (b) CLK level shifters and (c) their timing charts. The CLK level shifter shows the generation of CLKA.
Figure 4.4 Operation mechanism of the CLK level shifter; (a) Schematic and (b) timing chart.
Figure 4.5 Operation mechanism of the START level shifter; (a) Schematic and (b) timing chart.
Figure 4.6 (a) Schematic and (b) timing chart of the shift register (I) unit
(The voltage of VGL1 is less than that of VGL).
Figure 4.7 Block diagram of the shift register (I) embedded with a level shifter.
4.2.4 Simulation and experiment

The SPICE simulation was performed to analyze the shift register (I) embedded with a level shifter. The shift register (I) embedded with a level shifter is operated with a clock frequency of 12.5 kHz by using four-phase overlapped clock signals. The voltages are 20, −5, and −10 V for VGH, VGL, and VGL1, respectively.

Figure 4.8 shows the simulation results of the level shifter and shift register embedded with the level shifter. The voltages of node I [see Figure 4.3] and output are analyzed to verify the driving characteristics of the level shifter as shown in Figure 4.8(a). The simulation results show that the input voltage of -10 ~ 5 V is level shifted to the output voltage of -10 ~ 20 V. It has been confirmed by the simulation results that a negative voltage is successfully applied to the Vgs of the driver TFT (T3p) by CLK and CLKB with 180° out of phase so that these depletion-mode TFTs are completely turned off. Also, the node “I” is discharged periodically by T4S and T4aS for the generation time of the low-voltage output so that the resistance of the load TFT is highly increased. Therefore, the level shifter can successfully obtain the low-voltage output of VGL1 even if only a NMOS device is used.

The output pulse of the shift register (I) embedded with the level shifter is generated without any distortion as shown in Figure 4.8(b). It is because the voltage of a Q-node can be maintained to a high-level during the generation period of a high-voltage output pulse. Also, the simulation result shows that a negative voltage is successfully applied to Vgs of charging TFTs (T1a, T1b) and discharging TFT (T3) so that these depletion-mode TFTs are completely turned off.
The shift register (I) embedded with the full-swing level shifter employing the depletion-mode IGZO TFTs has been fabricated on the glass substrates.

Figure 4.9 shows the optical images of the level shifter and the shift register (I) with a six-mask etch-stopper structure. The level shifter consists of the START and CLK level shifters, which employ six TFTs and one capacitor. The channel widths of TFTs in the level shifter are 20 (T1S and T1C), 100 (T2S and T2C), 1000 (T3S, T3C, and T3aC), and 60 μm (T4S, T4aS, T4C, and T4aC). The bootstrap capacitor is 1.5 pF. On the other hand, the shift register has 11 TFTs and consists of ten stages. The channel widths of TFTs in the shift register are 125 (T1a and T1b), 10 (T1c), 70 (T2), 35 (T3), 10 (T4), 40 (T5), 100 (T6a), 1000 (T6b), 20 (T7a), and 200 μm (T7b). The channel lengths of all TFTs in the level shifter and the shift register (I) are 10 μm. The overlap length of the gate–drain in TFTs is 3 μm.

Figure 4.10 shows the output waveforms of the level shifter. The level shifter exhibits that START-I and CLKa of −10 ∼ 5 V are level shifted to START-O and CLK A of −10 ∼ 20 V, respectively. Also, as shown in Figure 4.11(a), the shift register (I), which uses the start and clock signals generated through the level shifter, successfully exhibits a high-voltage output pulse without any distortion.

In the shift register (I), T3 has Vgs = 0 V for the short output generation period so that a Q-node voltage could get a bit lower. However, the decrease of a Q-node voltage is not significant. It should be pointed out that the decrease of a Q-node voltage may be considerable at a low clock frequency. As shown in Figure 4.11(b), the shift register (I) embedded with the level
shifter successfully exhibits a high-voltage output pulse without any distortion at a very low clock frequency of 1.67 kHz.

Therefore, the shift register (I) embedded with the level shifter is suitable for display application. The gate driver circuits such as the level shifter and the shift register are required to exhibit the uniform output characteristics. When the output waveforms of the gate driver would not exhibit the uniform characteristics, the display quality may considerably deteriorate. The proposed shift register (I) embedded with the full-swing level shifter would exhibit the uniform output waveforms by using the clock signals that are generated from the level shifter.
Figure 4.8 Simulation results of (a) the level shifter and (b) the shift register (I) embedded with the level shifter.
Figure 4.9 Optical images of (a) the level shifter for the start signal and the clock signals and (b) the shift register.
Figure 4.10 Measurement waveforms of (a) the start signal and (b) the clock signals in the level shifters.
Figure 4.11 Output waveforms of the last (tenth) stage in the shift register at a clock frequency of (a) 12.5 and (b) 1.67 kHz.
4.2.5 Power consumption

Figure 4.12 shows the power consumption of the depletion-mode a-IGZO TFT shift register (I) embedded with the level shifter as a function of VGH. Also, the power consumption was measured at a VGL1 of $-7.5$ and $-10$ V. The power consumption of the ten-stage shift register (I) embedded with the level shifter is 2.13 mW at a VGH of 20 V, a VGL1 of $-10$ V, and a clock frequency of 12.5 kHz. The experimental result shows that the power consumption is considerably reduced by controlling driving voltages. In addition, in the level shifter in Figure 4.2(a), the dissipated currents of T2 and T3 with large channel widths are considerably reduced due to T4, although the short-circuit current through T1 and T4 with small channel widths occurs.
Figure 4.12 Power consumption of the shift register embedded with the level shifter as a function of VGH.
4.2.6 Conclusion

The shift register (I) embedded with the full-swing level shifter employing the depletion-mode a-IGZO TFTs has been proposed and fabricated. The driving circuits have been designed by employing two clock signals with 180° out of phase and one start signal for the level shifter and only two low-voltage-level signals for the shift register (I).

The level shifter and the shift register (I) consist of six TFTs and one capacitor, and 11 TFTs, respectively. The experimental results have shown that the level shifter and the shift register (I) have been designed to easily turn off the depletion-mode a-IGZO TFTs. The start signal and the clock input signals of $-10 \sim 5$ V have been level shifted to the output signals of $-10 \sim 20$ V.

The depletion-mode a-IGZO TFT shift register (I) embedded with the full-swing level shifter has successfully exhibited a high-voltage output pulse without any distortion. Also, the level shifter fully swings from 20 (VGH) to $-10$ V (VGL1) without any additional power sources and input signals, whereas the NMOS level shifter employing widely used a-Si and poly-Si TFTs, the output of which fully swings from VDD to VSS, has been scarcely reported. The power consumption is 2.13 mW at a VGH of 20 V, a VGL1 of $-10$ V, and a clock frequency of 12.5 kHz.

The proposed driving circuits would be an important building block for an advanced display employing a-IGZO TFT.
4.3 Highly reliable a-IGZO TFT gate driver circuits for high-frequency display under light illumination

4.3.1 Introduction

In the previous section, the depletion-mode a-IGZO TFT shift register (I) embedded with the level shifter by employing two low-voltage-level power signals was proposed and discussed.

In this section, the shift register (II) embedded with a level shifter employing the depletion-mode a-IGZO TFT without any additional signal is proposed. The operation characteristics and reliability of driving circuits under light illumination is investigated. The proposed gate driver successfully exhibits a high-voltage output pulse without distortion at a clock frequency of 100 kHz, which is enough to drive a high-frequency FPD with a frame rate of \( \sim 360 \) Hz and a resolution of full high definition (FHD). The proposed gate driver would work without any problem, although the threshold voltages of the TFTs degraded by gate bias stress in the level shifter and the shift register are largely shifted to \(-9.3\) and \(+15.2\) V, respectively. Also, the experimentally measured output waveform of the proposed gate driver has not been distorted after 240-h driving under 450-nm illumination with an intensity of 1 mW/cm\(^2\) at 60 \(^\circ\)C.
4.3.2 Fabrication and characteristics of a-IGZO TFTs

The bottom-gate a-IGZO TFTs with an etch-stopper structure by using a six-mask process were fabricated. Details of the device fabrication have been described in the section 3.5.
4.3.3 Circuit design

Figure 4.13 and 4.14 show the schematics of the level shifter and the shift register (II), respectively. In order to turn off the depletion-mode a-IGZO TFTs completely, the level shifter and the shift register (II) employing two clock signals with $180^\circ$ out of phase and the STT structure, respectively, have been designed. As shown in Figure 4.15, the start signal (ST-in) and the four clock signals (CLK1-in–CLK4-in) are supplied to the level shifter. Those signals are level shifted to the output signals (CLK1-out–CLK4-out) through the level shifter, and then, the level-shifted output signals are supplied to the shift register.
Figure 4.13 Schematics of the (a) START and (b) CLK level shifters and (c) their timing chart.
Figure 4.14 (a) Schematic and (b) timing chart of the shift register (II).
Figure 4.15 Block diagram of the shift register (II) embedded with a level shifter.
4.3.4 Simulation and experiment

The SPICE simulation was performed to analyze the shift register (II) embedded with a level shifter. The shift register (II) embedded with a level shifter is operated with a clock frequency of 12.5 kHz by using four-phase overlapped clock signals. The voltages are 20 and -5 V for VGH and VGL, respectively.

Figure 4.16 shows the simulation results of the level shifter and shift register embedded with the level shifter. The voltages of node I [see Figure 4.13] and output are analyzed to verify the driving characteristics of the level shifter. The simulation results show that the input voltage of -5 ~ 5 V is level shifted to the output voltage of -5 ~ 20 V. The output pulse of the shift register (II) embedded with the level shifter is generated without any distortion as shown in Figure 4.16(b).

The shift register (II) embedded with the full-swing level shifter employing the depletion-mode a-IGZO TFTs has been fabricated on the glass substrates. Figure 4.17(a) and (b) show the optical images of the level shifter and the shift register, respectively. The level shifter consists of the START level shifter and the CLK level shifter, which employ six TFTs and one capacitor. The channel lengths of all TFTs are 10 μm. The channel widths of the TFTs in the level shifter are 20 (T1C), 100 (T2C), 1000 (T3C and T3aC), and 60 μm (T4C and T4aC). The bootstrap capacitor is 1.5 pF. On the other hand, the shift register has 11 TFTs and consists of ten stages. The channel widths of the TFTs in the shift register are 180 (T1A and T1B), 10 (T1C and T2C), 100 (T2A and T2B), 50 (T3), 10 (T4), 60 (T5), 1200 (T6), and 240 μm (T7).
The gate driver is operated with four-phase overlapped clock signals. Figure 4.18 and 4.19 show the output waveforms in the level shifter and the shift register. The level shifter exhibits that ST-in and CLK1-in of −5 ~ 5 V are level shifted to ST-out and CLK1-out of −5 ~ 20 V, respectively. Also, as shown in Figure 4.20, the shift register, which uses the start and clock signals generated through the level shifter, successfully exhibits a high-voltage output pulse without any distortion. In particular, the proposed gate driver successfully generates a high-voltage output pulse at a very fast clock frequency of 100 kHz, which is enough to drive a high-frequency FPD with a frame rate of ∼360 Hz and a resolution of FHD.
Figure 4.16 Simulation results of (a) the level shifter and (b) the shift register (II) embedded with the level shifter.
Figure 4.17 Optical images of (a) the level shifter for the start signal and the clock signals and (b) the shift register.
Figure 4.18 Measurement waveforms of (a) the start signal and (b) the clock signals in the level shifters at the clock frequency of 12.5 kHz.
Figure 4.19 Measurement waveforms of (a) the start signal and (b) the clock signals in the level shifters at the clock frequency of 100 kHz.
Figure 4.20 Output waveforms of the last (tenth) stage in the shift register at the clock frequency of (a) 12.5 and (b) 100 kHz.
4.3.5 Reliability of the gate driver

TFTs in the gate driver may be degraded by various gate bias stresses. As shown in Figure 4.21, T3C and T4C of the level shifter are under positive- (10 V) and negative-gate-bias (−10 V) stresses alternatively with the same duty ratio (BTS A). As shown in Figure 4.22, T3 of the shift register is under positive- (25 V) and zero-gate-bias stresses alternatively with the same duty ratio (BTS B). Also, T7 is under positive-gate-bias (25 V) stress (BTS C).

Figure 4.23 through Figure 4.27 show the threshold voltage shift ($\Delta V_{th}$) of a-IGZO TFTs after a gate bias stress of 10000 s at 60 °C. Under +10 V (DC) gate bias stress, the $\Delta V_{th}$’s of a-IGZO TFT at dark and photo conditions (a wavelength of 450 nm and an intensity of 1 mW/cm$^2$) are ~0.003 and ~0.15 V, respectively. Under -10V (DC) gate bias stress, the $\Delta V_{th}$’s at dark and photo conditions are ~ -0.15 and ~ -1.56V, respectively. Also, under +10 and -10V (AC) gate bias stress alternatively with the same duty ratio (BTS A), the $\Delta V_{th}$’s at dark and photo conditions are ~ -0.05 and ~ -0.13V, respectively. On the other hand, under 25 and 0 V (AC) gate bias stress alternatively with the same duty ratio (BTS B), the $\Delta V_{th}$’s at dark and photo conditions are ~ 0.003 and ~ 0.14V, respectively. Under 25V (DC) gate bias stress (BTS C), the $\Delta V_{th}$’s at dark and photo conditions is ~ 0.03 and ~ 0.20V, respectively.

The $\Delta V_{th}$ of a-IGZO TFT under ac stress is smaller than that under dc stress [101]. The threshold voltages under negative-bias temperature stress (NBTS) and positive-bias temperature stress (PBTS) are shifted negatively and positively, respectively. In addition, $\Delta V_{th}$ is larger under NBTS than under PBTS [102]. These $\Delta V_{th}$ tendencies are in agreement with other reported results [101], [102]. Also, as shown in Figure 4.28, the time
dependence of $\Delta V_{\text{th}}$ for a-IGZO TFTs is well fitted by the stretched-exponential equation as follows:

$$
\Delta V_{\text{th}} = \Delta V_{\text{th}}(0) \left\{ 1 - \exp \left( -\left( \frac{t}{\tau} \right)^{\beta} \right) \right\}
$$

where $\Delta V_{\text{th}}(0)$, $\tau$, and $\beta$ are the $\Delta V_{\text{th}}$ at infinite time, the characteristic time constant, and the stretched-exponential exponent, respectively [102], [103]. The $\Delta V_{\text{th}}$ of the degraded a-IGZO TFTs in the gate driver is so small that it may not affect the operation characteristics of the circuits.

A SPICE simulation was performed to verify the reliability of the proposed gate driver. The SPICE model parameters were extracted from the fabricated a-IGZO TFTs. As shown in Figure 4.29(a) and (b), the gate driver works without any problem, although the threshold voltages of the TFTs degraded by gate bias stress in the level shifter and the shift register are largely shifted to $-9.3$ and $+15.2$ V, respectively. It can be expected from these simulation results that the gate driver would be working properly for a long-time driving.

Figure 4.30(a) and (b) shows the experimentally measured output waveforms of the gate driver before and after 240-h driving, respectively, under 450 nm illumination with an intensity of 1 mW/cm$^2$ at 60 °C. The output waveform has not been distorted for 240-h driving. The experimental and SPICE simulation results showed that the proposed gate driver would be highly reliable with the operation time under light illumination, although the TFTs were degraded by gate bias stresses.
Figure 4.21 (a) Schematic and (b) timing chart of the level shifter.
Figure 4.22 (a) Schematic and (b) timing chart of the shift register (II).
Figure 4.23 Evolution of the transfer curves as a function of the applied stress time under +10 V gate bias stress at 60 ºC: (a) Dark, (b) Photo (450nm, 1mW/cm²).
Figure 4.24 Evolution of the transfer curves as a function of the applied stress time under -10 V gate bias stress at 60 °C: (a) Dark, (b) Photo (450nm, 1mW/cm²).
Figure 4.25 Evolution of the transfer curves as a function of the applied stress time under +10 and -10 V gate bias stress alternatively with the same duty ratio at 60 °C: (a) Dark, (b) Photo (450nm, 1mW/cm²).
Figure 4.26 Evolution of the transfer curves as a function of the applied stress time under 0 and +25 V gate bias stress alternatively with the same duty ratio at 60 °C: (a) Dark, (b) Photo (450nm, 1mW/cm²).
Figure 4.27 Evolution of the transfer curves as a function of the applied stress time under +25 V gate bias stress at 60 °C: (a) Dark, (b) Photo (450nm, 1mW/cm²). 
Figure 4.28 $V_{th}$ shift as a function of stress time: [BTS A] +10 and -10 V (AC) gate bias stress alternatively with the same duty ratio, [BTS B] 25V and zero (AC) gate bias stress alternatively with the same duty ratio, [BTS C] 25V (DC) gate bias stress alternatively with the same duty ratio.
Figure 4.29 Simulation results of the output waveforms of (a) the level shifter and (b) the shift register when the TFTs are degraded by gate bias stress: (a) T3C and T4C are degraded; (b) T3 and T7 are degraded. The clock frequency is 200 kHz. V TO(zero-bias threshold voltage) is the SPICE parameter.
Figure 4.30 Measured output waveforms of the gate driver (a) before and (b) after 240-h driving under 450-nm illumination with an intensity of 1 mW/cm² at 60 °C.
4.3.6 Conclusion

A depletion-mode a-IGZO TFT gate driver without any additional signals has been proposed and fabricated. The proposed gate driver successfully exhibited a high-voltage output pulse without distortion at a clock frequency of 100 kHz, which is enough to drive a high-frequency FPD with a frame rate of $\sim$360 Hz and a resolution of FHD. The output waveform of the proposed gate driver was not distorted after 240-h driving under 450 nm illumination with an intensity of 1 mW/cm$^2$ at 60 $^\circ$C. The proposed gate driver would be an important building block for ultrahigh-resolution and high-frame-rate display.
Chapter 5 Summary

In this study, novel level shifters and shift registers employing depletion-mode a-IGZO TFTs were introduced and discussed. a-IGZO TFTs with an etch-stopper structure were fabricated by six-mask process compatible to conventional a-Si:H TFTs fabrication process.

Firstly, the level shifter (I) has been designed by employing two clock signals with 180° out of phase in order to turn off depletion-mode a-IGZO TFTs. The level shifter (II) employing two clock signals with 180° out of phase and one discharging TFT has been swung fully from VDD to VSS. Although the level shifter (II) employs only n-type depletion-mode a-IGZO TFTs, it had a wide swing output without any additional power sources and input signals.

Secondly, the shift register (I) has been designed by employing two low-voltage-level power signals with which a negative voltage can be applied to the Vgs of depletion-mode a-IGZO TFTs. The shift register (I) successfully exhibited a high-voltage output pulse without any distortion and a maximum

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clock frequency of 417 kHz. The shift register (II) with depletion-mode a-IGZO TFTs has been designed by employing only one low-voltage-level power signal, which has been usually used in a circuit employing a conventional enhancement-mode device, without an additional signal. Although the shift register (II) employs only low-voltage-level power signal, a negative voltage could be applied to the Vgs of a-IGZO TFTs. It was possible because the charging and discharging TFTs of the shift register were composed of the STT structure. The driving circuits employing depletion-mode oxide TFTs require many TFTs in addition to additional power sources and input signals in order to turn off depletion-mode oxide TFTs. It should be pointed out that many TFTs and signal lines would increase the circuit area. Therefore, the shift register (III) has been designed by employing node-shared structure, where Q-node and Qb-node of adjacent two stages are shared, respectively. The shift register (III) required 14 TFTs, 3 clock lines, and 3 power source lines for two output pulses, whereas the previous shift registers consisted of more than 22 TFTs, 4 clock lines, and 6 power source lines.

For the applications of the driving circuits in displays, such as AMOLED and AMLCD, the depletion-mode a-IGZO TFT shift registers embedded with a full-swing level shifter were introduced and discussed.

Firstly, the shift register (I) embedded with the level shifter has been designed by employing two clock signals with 180° out of phase and one start signal for the level shifter and two low-voltage-level signals for the shift register, respectively. The experimental results have shown that the level shifter and the shift register have been designed to easily turn off the depletion-mode a-IGZO TFTs. The start signal and the clock input signals of
−10 ∼ 5 V have been level shifted to the output signals of −10 ∼ 20 V. The depletion-mode a-IGZO TFT shift register (I) embedded with a full-swing level shifter has successfully exhibited a high-voltage output pulse without any distortion.

Secondly, the shift register (II) embedded with the level shifter employing the depletion-mode a-IGZO TFT without any additional signal was introduced. In addition, the reliability of driving circuits under light illumination was discussed. The shift register (II) embedded with the level shifter successfully exhibited a high-voltage output pulse without distortion at a clock frequency of 100 kHz, which is enough to drive a high-frequency FPD with a frame rate of ∼360 Hz and a resolution of FHD. The SPICE results have shown that the shift register (II) embedded with the level shifter would work without any problem, although the threshold voltages of the TFTs degraded by gate bias stress in the level shifter and the shift register would be largely shifted to −9.3 and +15.2 V, respectively. Also, the experimentally measured output waveform of the shift register (II) embedded with the level shifter has not been distorted after 240-h driving under 450-nm illumination with an intensity of 1 mW/cm² at 60 °C.

The proposed driving circuits would be an important building block for a depletion-mode oxide TFT and a high-frame-rate display.
Appendix A SPICE Input File

A.1 a-IGZO TFT Model (I) [see Figure 3.3]

.LIB TFT1510
* Temp= 27
* W= 15.0  L= 10.0
.MODEL TFT1510 NTFT ( LEVEL = 35
+TOX = 2E-7  TNOM = 27  VTO = -1.2
+ALPHASAT= 0.515348  DEFO = 0.6  DELTA = 3.3
+EL = 0.35  EMU = 0.06  EPS = 11.9
+EPSI = 3.9  GAMMA = 0.25  GMIN = 2.23872E22
+IOL = 1.258925E-13  KASAT = 6E-3  KVT = -0.036
+LAMBDA = 0.01  M = 2.29268  MUBAND = 7E-3
+SIGMAO = 1.25893E-14  VO = 0.46  VAA = 2.44653E4
+VDSL = 19.62  VFB = -4.6  VGSL = 4.87
+VMIN = 0.05  RD = 0  RS = 0
+LD = 0  XL = 0  XW = 0
+ACM = 0  CGSO = 0.54n  CGDO = 0.54n)
*
.ENDL TFT1510
A.2 a-IGZO TFT Model (II) [see Figure 3.22]

.LIB TFT2010
* Temp= 27
* W= 20.0 L= 10.0
.MODEL TFT2010 NTFT ( LEVEL = 35
  +TOX = 3E-7  TNOM = 27  VTO = -0.83
  +ALPHASAT = 0.95  DEFO = 0.88  DELTA = 1.5
  +EL = 0.36  EMU = 0.06  EPS = 11.9
  +EPSI = 3.9  GAMMA = 0.428  GMIN = 4.46684E21
  +IOL = 7.94328E-16  KASAT = 6E-3  KVT = -0.036
  +LAMBDA = 0.57  M = 2.96  MUBAND = 5E-4
  +SIGMAO = 6.309573E-15  VO = 0.25814  VAA = 184.984
  +VDSL = 8.42  VFB = -2.75  VGSL = 4.51
  +VMIN = 0.96004  RD = 0  RS = 0
  +LD = 0  XL = 0  XW = 0
  +ACM = 0  CGSO = 0.45n  CGDO = 0.45n)
*
.ENDL TFT2010
A.3 a-IGZO TFT Model (III) [see Figure 4.1]

.LIB TFT1K10
* Temp= 27
* W= 1000.0 L= 10.0
.MODEL TFT1K10 NTFT ( LEVEL = 35
+TOX = 3E-7 TNOM = 27 VTO = -2.75
+ALPHASAT= 0.6725204 DEFO = 0.88 DELTA = 0.040727
+EL = 0.36 EMU = 0.06 EPS = 11.9
+EPSI = 3.9 GAMMA = 0.75 GMIN = 1.007935E20
+IOL = 1.42992E-15 KASAT = 6E-3 KVT = -0.036
+LAMBDA = 1.35699E-3 M = 1 MUBAND = 5.990666E-4
+SIGMAO = 1.45799E-14 VO = 0.0718277 VAA = 8.6888559
+VDSL = 5.22233 VFB = -3.2 VGSL = 2.36099
+VMIN = 2.08846E-3 RD = 0 RS = 0
+LD = 0 XL = 0 XW = 0
+ACM = 0 CGSO = 0.45n CGDO = 0.45n)
*
.ENDL TFT1K10
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초 록

최근에 하이엔드 평판 디스플레이는 초고해상도(≥4Kx2K)와 고속프레임속도(≥240Hz)를 요구한다. 그러나, 널리 사용되고 있는 비정질 실리콘 박막트랜지스터의 전기적 특성은 이러한 요구사항을 만족시킬 수 없다. 비정질 산화물 박막트랜지스터가 대면적 기판에서 높은 이동도와 우수한 균일도 특성 때문에 주목을 받고 있다. 대부분의 산화물 박막트랜지스터는 많은 전자 농도 때문에 널리 사용되고 있는 증가형(enhancement-mode) 보다는 기본적으로 공핍형(depletion-mode) 소자이다. 또한, negative bias illumination stress 또는 light illumination 조건 하에서 산화물 박막트랜지스터의 문턱전압은 음전압 방향으로 크게 이동한다. 따라서, 산화물 박막트랜지스터 기반의 디스플레이에서는 공핍 모드에서 동작할 수 있는 구동회로가 필수적이다.

본 논문에서는 공핍형 비정질 IGZO 박막트랜지스터를 적용한 새로운 레벨 쉬프터와 쉬프트 레지스터에 대해서 연구되었다. 180° 위상이 반전된 두 개의 클럭 신호와 하나의 방전 트랜지스터를 적용한 레벨 쉬프터는 VDD 부터 VSS 까지 스윙한다. 레벨 쉬프터가 오직 n-type 공핍형 비정질 IGZO 박막트랜지스터만을 적용함에도 불구하고, 추가적인 전원 이나 입력 신호없이 넓은 스윙 출력을 보여준다.

쉬프트 레지스터(I)은 공핍형 비정질 IGZO 박막트랜지스터의 게이트-소스 전압이 음전압이 되도록 하기 위하여 두 개의 로 전압 레벨 신호를 적용하여 설계되었다. 특히, 쉬프트 레지스터(II)는 일반적으로 증가형 소자를 이용한 회로에서처럼 추가적인
신호없이 단 하나의 로 전압 신호를 적용하여 설계되었다. 위 두 개의 쉬프트 레지스터들은 왜곡없이 하이 전압 출력을 보여줬다. 네로우 베젤 디스플레이를 위한 것으로, 인접하는 두 단의 Q-node 와 Qb-node 가 각각 공유되는 구조인 노드 공유 구조를 적용한 쉬프트 레지스터(III)은 두 출력 펄스를 위해 14 개의 트랜지스터, 3 개의 클럭 라인 그리고 3 개의 전원 라인이 필요하다. 반면에 이전의 쉬프트 레지스터들은 22 개 이상의 트랜지스터, 4 개 이상의 클럭 라인 그리고 6 개 이상의 전원 라인이 필요하다.

능동 구동 액정 디스플레이 및 유기 발광 다이오드와 같은 디스플레이에서 구동 회로의 응용을 위해 풀 스윙 레벨 쉬프트가 내장된 공핍형 비정질 IGZO 박막트랜지스터 쉬프트 레지스터가 연구되었다. -10~5 V 의 스타트 신호와 클럭 입력 신호들이 -10~20 V 의 출력 신호들로 변환된다. 레벨 쉬프트가 내장된 공핍형 비정질 IGZO 박막트랜지스터 쉬프트 레지스터는 성공적으로 왜곡없이 하이 전압 출력을 보여줬다. 또한, 레벨 쉬프트가 내장된 쉬프트 레지스터는 100 kHz 의 클럭 주파수에서도 왜곡없이 하이 전압 출력 특성을 보여줬다. 주파수 100 kHz 는 FHD 해상도와 ~360 Hz 의 프레임 속도를 갖는 평판 디스플레이를 구동하기에 충분하다. SPICE 시뮬레이션 결과에 의하면, 레벨 쉬프트와 쉬프트 레지스터에서 게이트 바이어스 스트레스에 의해 열화되는 박막트랜지스터의 문턱전압이 각각 -9.3 V 와 +15.2 V 로 이동한다 하더라도 레벨 쉬프트가 내장된 쉬프트 레지스터는 불량없이 동작한다. 또한, 레벨 쉬프트가 내장된 쉬프트 레지스터가 60 °C 온도에서 1 mW/cm² 의 intensity 를
갖는 450-nm 빛에 노출된 상태에서 240 시간 구동된 후의 출력 파형은 전혀 왜곡되지 않았다.

주요어 : 비정질 산화물 박막트랜지스터, IGZO, 공핍형, illumination, 레벨 쉬프터, 쉬프트 레지스터.

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감사의 글

회사 생활을 10여 년 하다가 다시 공부를 시작한다는 설렘과 두려움을 동시에 안고 박사과정에 들어선지 3년 6개월이라는 시간이 너무 빠르게 흐른 것 같습니다. 그 동안 박사과정을 무사히 마칠 수 있도록 기회와 도움을 주셨던 모든 분들께 깊은 감사의 글을 전하고자 합니다.

항상 제자의 입장에서 현명한 방법을 선택할 수 있도록 충고와 조언을 아끼지 않았고, 아버지 같은 친근함과 자상함으로 제자들을 가르치시는 한민구 교수님께 큰 감명을 받고 깊이 감사드립니다. 언제나 연구의 핵심을 짚어주시고 방향을 잡아주셔서 연구를 체계적으로 진행할 수 있었습니. 교수님의 가르침은 학문에 국한되지 않고 앞으로 인생을 살아가는 데에 저의 나침반이 될 것입니다.

아울러 저의 부족한 논문을 심사해 주시고 좋은 논문이 될 수 있도록 아낌없이 많은 조언을 해주신 이병호 교수님, 박남규 교수님, 한국항공대학교 전재홍 교수님 그리고 건국대학교 박기찬 교수님께 깊은 감사를 드립니다. 교수님들의 가르침으로 보다 완성도 높은 논문이 되었다고 생각합니다.

박사과정 동안 많은 도움을 주신 회사 여러분들께도 감사의 말씀을 드리고 싶습니다.

박사과정을 밟을 수 있도록 소중한 기회를 주신 정인재 부사장님께 진심으로 감사 드립니다. 부사장님 덕분에 역량을 한 단계 높일 수 있는 소중한 시간을 가질 수 있었습니다. 또한, 온화한 미소로 후배 사원들을 격려해주시고 연구자로서 본받고 싶은
강인병 전무님, 학위과정의 기회를 주시고 연구수행에 있어 회사 인프라를 이용할 수 있도록 최대한 배려를 해주신 김창동 상무님, 박사과정 처음부터 마찰 때까지 지원을 아끼지 않으셨고 언제나 최선을 다하여 도움을 주시는 윤수영 상무님께도 진심으로 감사드립니다.

논문에 많은 조언을 해주신 LGD 최고 전문가 장용호 연구위원님, 학위과정을 원만히 수행할 수 있도록 많은 배려를 해주신 이부열 수석님과 유준석 수석님께도 감사의 말씀을 드리고 싶습니다. 연구 수행에 있어 적극적으로 도움과 관심을 주신 서현식 수석님, 배중욱 수석님 그리고 박권식 수석님 참으로 감사 드리립니다. 샘플제작 및 측정에 많은 도움을 준 최승찬 선임, 조혁력 선임, 조성학 선임, 유창일 선임, 최우석 주임, 유성빈 주임, 헌광일 연구원께도 고마움을 전하고 싶습니다. 이 분들 덕분에 원활한 연구를 할 수 있었습니다. 그리고, 학위과정으로 제가 회사를 자주 비웠지만 항상 최선을 다해 제 몫까지 일을 해준 박수정 선임, 박재희 선임, 김종무 선임, 박성희 주임, 한준수 연구원, 이새이누리 연구원, 정진현 연구원 모두 감사합니다.

연구실 생활 동안 많은 배려를 해주고 즐겁게 지내온 연구실 선배님, 후배님들께도 많은 고마움을 느낍니다.

명석한 두뇌로 미팅 때마다 날카로운 지적을 하는 현상, 언제나 밝은 미소로 상대방을 편안하게 해주고 배려심 많고 성실한 상근, 같이 연구실 생활을 못해 아쉽고 좋은 논문으로 귀감이 되는 영훈, 절대 평범하지 않고 언제가 큰 일을 할 지용, 연구에 진지하고 하나님의 사랑을 연구실에서도 실천하는 미소천사 선재, 방공연을 제 집 드나들듯이 하며 끝임 없이 연구하는 성실한 성환, 항상
긍정적으로 모든 일을 열심히 하고 여러 가지로 많은 도움을 준 졸업동기 동원과 승희, 멋진 외모만큼이나 인생이 밝아 보이는 영실, 모든 운동을 잘하고 승부욕이 무척 강한 남자다운 정수, 쾌활한 성격으로 주변을 즐겁게 하고 생각이 많은 선범, 참으로 순수하고 열정적으로 최선을 다하는 오균이와 민기, 효율적인 인생을 살 줄 아는 미남 용진, 항상 기대 이상의 일을 하는 연구실 홍일점 수연, 연구실에 처음 들어왔을 때부터 많은 도움을 주고, 모든 걸 챙겨주고 싶은 너무 괜찮은 입학동기 용욱, 만학도지만 연구, 운동 등 모든 방면에서 뛰어난 승환과 영욱, 앞으로 크게 성공할 준비된 회사원 중석, 아주 순진해 보이지만 할 것 다하는 진국 스타일 문규, 활달한 성격으로 새로운 것에 관심이 많은 승민, 연구실 생활을 같이 못해 아쉬운 착한 우진 그리고 학생들이 연구에 몰두할 수 있도록 연구실의 많은 일을 처리해 주시는 정유지 씨와 임지혜 씨 등 연구실 모든 분들의 도움으로 무사히 졸업을 할 수 있어 감사를 드리고, 모두 걱정의 없이 즐겁고 유쾌하게 지낼 수 있었던 연구실 생활을 잊을 수가 없을 것 같습니다.

많은 연세에도 불구하고 자식들의 편안함을 위해 여전히 고생을 마다하시지 않는 부모님께 깊이 감사 드립니다. 항상 부모님의 은혜 잊지 않고 살겠습니다. 또한, 언제나 묵묵히 응원해 주시는 장인, 장모님 그리고 처남 가족들에게도 감사의 말씀을 드립니다. 막내 동생을 따뜻하게 챙겨주시는 형님, 형수님, 누나, 매형들께도 고맙다는 말씀을 전하고 싶습니다. 그리고, 여읜 대학생부터 어린 초등학생까지 한결같이 모두 착한 조카들도 많이 사랑합니다.

때로는 칭찬해주고, 때로는 조언해주고, 항상 저를 위해 큰 불평 없이 최선을 다하는 사랑하는 아내 혜진에게 말할 수 없이 큰
고마움을 느끼고 감사를 드립니다. 아내를 향한 저의 마음을 행동으로 옮기지 못해 참으로 미안합니다. 앞으로 표현하고 실천하는 남편이 되도록 노력하겠습니다. 그리고 세상에서 제일 귀엽고 사랑스러운 우리 귀염둥이 재원이를 많이 사랑합니다. 아빠가 많이 놀아주지 못해도 항상 아빠가 최고라고 생각하는 재원이에게 진짜 최고가 될 수 있도록 노력하겠습니다. 항상 즐겁고 행복하고 서로에게 의지할 수 있는 가정이 되도록 최선을 다하겠습니다.