Ph.D. DISSERTATION

Electrical channel formed by the tunneling electroplating

(터널링 도금을 이용한 전기 채널)

By

Seok-Ha Lee

February 2013

SCHOOL OF ELECTRICAL ENGINEERING AND COMPUTER SCIENCE
COLLEGE OF ENGINEERING
SEOUL NATIONAL UNIVERSITY

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Seok-Ha Lee

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Abstract

Electrical channel formed by the tunneling electroplating

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The extreme miniaturization of semiconductor devices in recent years has exposed the intrinsic limitations of the characteristics of silicon materials in conventional device structures. In light of efforts to circumvent these problems, researchers are trying to utilize single atoms or monolayer film in FET (field-effect transistor) channels in addition to using alternative materials such as III-V semiconductors, CNT (carbon nanotube), or graphene.

In this thesis, a novel metal channel device structure as well as its operation method and fabrication process will be proposed. A process flow is proposed and the test pattern is produced accordingly. It has been developed and demonstrated a new manufacturing method dubbed “tunneling electroplating”, which is used to construct

metal layers of nanometer-order thickness on dielectric materials.

An analysis of a metal-electrolyte-metal (MEM) structure is conducted to create the devised metal channel device efficiently. The analysis result is then combined with information from the reduction potential and target ion energy level in an energy band diagram for a better electrical analysis of the electroplating process. Metal layers of the dielectric material with a thickness on the nanometer order are constructed in the forms of electrolyte-oxide-silicon (EOS) and electrolyte-metal-oxide-silicon (EMOS) structures, demonstrating that the tunneling current through the oxide film via an electrolyte is limited by the electric potential across the oxide film. The radical increase in the tunneling current in repeated electric characterizations of the EOS structures is found to be caused by the reduction of the effective oxide thickness due to hydrogen ions (protons) penetrating into the oxide films. A new oxide layer recovery method which emits protons periodically is also proposed, and it is confirmed that, with this method, metal layers of nanometer-order thickness can be formed on the oxide surface without a breakdown of the dielectric layer.

For an enhancement of the oxide adhesion of metal particles produced in the upper dielectric layer during a tunneling electroplating process, the devices are dipped into APTES (3-aminopropyltriethoxysilane) as a SAM (self-assembled monolayer) treatment.

The electrolyte, source, drain and substrate currents through the test patterns during the tunneling electroplating process are also analyzed and the metal layer

formation and channel completion mechanisms are clarified, including what is termed a self-limitation method that prevents the thickness of the metal layer on the oxide films from increasing.

This ‘tunneling electroplating’ method can realize the room-temperature manufacturing of metal layers for FET channel purposes. Because it is compatible with existing CMOS process, it can be easily applied to mass production through additional integration with current semiconductor chips. The applicability of the devised tunneling electroplating process is quite broad in many applications, such as nanometer-order transistor- or metal-based sensors.

Keywords: Tunneling current, Electroplating, Channel layer, Nano particle, Electrolyte, MOSFET, MOS, EOS, EMOS

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Chapter 1

Introduction

1.1 Motivation

In recent years, there have been many attempts and studies to utilize semiconductor devices in an electrolyte, such as an Ion-Sensitive Field-Effect Transistor (ISFET) or Electrolyte–Oxide-Silicon (EOS).[1-6]

Electrolyte in ISFET or EOS device in biomedical and industrial applications is to correlate the pH variation of target substance, potential variation, and/or presence of a certain gases with the silicon substrate current variation through the electrical field effect.[7-10] On the other hand, in the EOS system, tunneling current through the gate insulator has been considered as an undesirable factor that gives rise to reliability issues such as gate insulator degradation and interface state generation [11-13].

Unlike the leakage current through the oxide defects, tunneling current in EOS

system can be considered as the slow infusion of electrons from the substrate into the oxide-solution surface over the oxide energy barrier, where the electrons' energy is high enough to reduce the ions in the solution. By manipulating these tunneling current characteristics, we can control the speed of the electroplating more effectively than we do with the electroplating by the leakage current, and eventually obtain higher quality metal thin films.

Since the resultant metal nano film can function as electric channel for carrier passage, utilizing electroplating technique for the actual device manufacturing method enhances the compatibility with current CMOS process and realizes in-situ monitoring of channel formation process. In this thesis, quite straightforwardly, I will use the term "metal channel device" for the device that forms electrical channel in the metal, and the term "Tunneling electroplating" for the metal layer formation technique in which the electroplating is done by tunneling current.

1.2 Metal channel device

In this chapter, the concept of electrical effect of nano size metal particles in terms of band diagram introduce the metal channel device will be introduced. Also, this device is compared with conventional MOSET device in various aspects

1.2.1 Basic concept of metal channel device

Metal in bulk form is generally good electrical conductor. This can be explained in energy band diagram as in the leftmost drawing of Fig. 1-1(a), where the band

shows the energy states fully filled with electrons.[14-15] But for metal clusters in smaller dimension, the reduction of the effect due to interaction between atoms or perturbation causes energy level splitting, thus the second drawing of Fig. 1-1(a). [16-22] With further grain size reduction up to atomic levels causes energy gap increase between Highest Occupied Molecular Orbital [HOMO] level and Lowest Unoccupied Molecular Orbital [LUMO] level, as in the third and the fourth drawings of Fig. 1-1(a). With this energy gap bigger than kT, the metal even shows semiconductor-like electrical properties. Notably, Fig. 1-2 (b) shows density of state (DOS) change according to the size reduction of metal, as is well established in current literature. [23]

First, Gold (Au) HOMO to LUMO energy difference between atomic state and 1-shell state is calculated. Density Functional Theory [DFT] based simulation software called “abinit” is used for the calculation tool. The left figure of Fig 1-2 shows that the energy gap of Au single atom case is near 5.2 eV, and the right figure shows that the energy gap reduces to 0.67 eV as the particle size increased to 1-shell structure. Considering the energy band gap of silicon is generally 1.1 eV, it can be concluded that the metal particle size needs to be limited within one to three layer integration if metal device is to show semiconductor-like characteristics.

1.2.2 Common channel for FET device

Fig. 1-3 is the vertical section figure of most general form of conventional MOSFET devices that are applied in DRAM, FLASH, logic circuit, etc. In most

MOSFET devices, source and drain are formed by the doping of opposite type to the silicon substrate, and silicon dioxide layer is formed as necessary insulator above source, drain and substrate. On top of that, gate electrode structure is patterned so that the bias on the gate induces the inversion channel in the substrate, through which electrical carriers flow from source to drain.

Proposed metal channel device is presented in Fig. 1-4. Figure (a) is a 3-terminal device structure using 3 electrodes. SiO_2 insulator is grown on silicon substrate, and source and drain are formed using patterned metal. Nano sized metal layer is located between source and drain to function as the channel for electrical carrier transport. In this kind of 3-terminal device, channel modulation is accomplished by using substrate for back side gate function.

Figure (b) is a 4 terminal device structure using 4 electrodes. In addition to the basic 3-terminal structure in Figure (a), electrolyte as a buffer solution is introduced, and the four terminals are completed with a metal block functioning as a gate to control solution potential or a reference electrode with well-known electrode potential such as Ag/AgCl pair. Effective channel control is expected in this 4 terminal device because it is capable of vertical field termination just like conventional MOSFETs. The thickness of Electrical Double Layer(EDL) originated in electrolyte can also be controlled by electrolyte concentration.[24-25] Furthermore, since the relative permittivity(ε_r) value of water (about 80.1 at 20℃) is about 20 times larger than that of silicon oxide (3.9), the channel control with much lower gate bias is possible. Excessive bias on electrolyte may cause electrolysis of

H_2O in the solution, so application of well optimized bias level is required so that it does not produce hydrogen gas near the surface because the gas causes adverse effects on the device performance.

1.3 Tunneling current and common electroplating

1.3.1 Fowler-Nordheim tunneling and direct tunneling current

In MOS (Metal-Oxide-Silicon) devices, high level bias between gate metal electrode and substrate pushes down the fermi level of the metal electrode. In this situation, electrons tend to move through tunneling from silicon conduction band to the conduction band of oxide triangular potential barrier, and eventually to energy levels of metal. This is called Fowler-Nordheim tunneling. [26] Fig. 1-5 (a) shows the energy band diagram in the case of Fowler-Nordheim tunneling.

Simplified Fowler-Nordheim tunneling current equation with respect to the bias voltage is as follows [27]:

$$J_{FN} = \frac{q^3}{16\pi^2\hbar\psi_b} F_{ox}^2 \exp\left[-\frac{4}{3}\frac{\sqrt{2m_{ox}^*}\psi_b^{\frac{3}{2}}}{q}\frac{1}{F_{ox}}\right] \quad \text{(eq. 1)}$$

where q is the electron charge, $\hbar$ the reduced Planck constant, m*ox the electron effective mass in insulating layer, ψb the conduction band height difference between semiconductor and oxide, and Fox is the electric field across the oxide.

On the other hand, it is possible that electrons experience direct tunneling from oxide conduction band to the conduction band of the gate metal electrode when the oxide thickness thin enough, as in a few nanometer size devices. [28-29] In this direct tunneling condition, the oxide energy barrier that electrons go through shows trapezoidal shape, and the current measurement is possible in low electric field across the oxide layer. (Fig. 1-5 (b))

Simplified direct tunneling current equation with respect to the bias is as follows. [30]

$$J_T = \frac{q^3}{16\pi^2\hbar\psi_b} F_{ox}^2 \exp\{-\frac{4}{3}\frac{\sqrt{2m_{ox}^*}\,\psi_b^{\frac{3}{2}}}{\hbar q F_{ox}}[\,1-\left(1-\frac{qV_{ox}}{\psi_b}\right)^{3/2}]\}\ \text{(eq. 2)}$$

An example of modeling prediction of Fowler-Nordheim current and Direct tunneling current as well as actual measurement result are presented in Fig. 1-6.[31-32]

1.3.2 Electroplating

To construct metal channel in the upper portion of the dielectric layer by electroplating using tunneling current, it is necessary to understand the essence of the EDL (Electrical Double Layer) and standard electrodes.

Charged solid material submerged in electrolyte attracts charged particles on the solid-solution interface. Electron charges of the solid and ion charges of the solution

get to face one another across the solid-solution interface and this formation is called "EDL". [24-25]

There are three models describing EDLs; Helmholtz model, Gouy Chapmann model, and Stern model. I adopted Stern model for the EDL analysis in this thesis work. [33] Fig. 1-7 shows an EDL model including gold ion containing electrolyte. In Stern's EDL model, electrolyte near solid can be divided into two layers; diffuse layer that assumes charges and compact layer that resides in between ion and solid surface. Because the charge carrier density is low in the solution with small ion density, the thickness of the ion charge layer in the solution corresponding to the quantity of the electrode charges gets larger as the solution concentration gets lower. Ion charges are concentrated near solid-electrolyte interface where electrostatic force exceeds thermal process, and their concentration reduces to intrinsic electrolyte value as the distance from the interface increase, due to the increasing disorder by the thermal process of ion motion. In Stern model, this ion charge layer is called "diffuse layer", where gradually decreasing charge quantity approaches equilibrium electrolyte concentration. The range of this diffuse layer is influenced by the ion concentration and the electrode bias that determines the electrode charge quantity. Debye ($1/\kappa$) equation is obtained by solving the Poisson-Boltzmann equation regarding charge quantity of solution-electrode interface. [24-25]

The EDL in Stern model, as shown in Fig. 1-6, can be modeled by two capacitors in series connection, where compact layer of electrode-solution interface and outside diffuse layer are in contact. [34]

Capacitance of the compact layer is not affected by the bias potential or electrolyte concentration. In low concentration electrolyte, thinner diffuse layer makes the diffuse layer capacitance smaller, and the capacitance of the equivalent circuit is keenly influenced by the diffuse layer. On the other hand, in high concentration electrolyte, relatively constant compact layer capacitance value determines equivalent circuit capacitance, regardless of the bias potential.[35] Therefore, according to Stern model, low concentration electrolyte EDL shows capacitance variation due to voltage change in low bias condition, whereas either high concentration electrolyte or high bias potential condition results in thinner diffuse layer, which in turn gives constant capacitance electrical double layer determined by compact layer without much variation due to bias voltage.

EDL capacitance equation according to the Stern model is as follows: [33]

$$\frac{1}{\mathrm{C_d}} = \frac{\mathrm{x_2}}{\epsilon\epsilon_0} + \frac{1}{\left(\frac{2\epsilon\epsilon_0 z^2 e^2 n^0}{kt}\right)^{\frac{1}{2}} \cosh\left(\frac{ze\phi_2}{2kt}\right)} \quad \text{(eq. 3)}$$

When constant bias potential is applied to the electrode submerged in the solution, the solution potential is not equivalent to the bias potential because of the EDL voltage reduction at the electrode-solution interface. Because the EDL length varies according to the bias in very low concentration electrolyte, the solution potential cannot be considered constant independently of the bias. Therefore, to measure the

solution electric potential in EOS system, a reference electrode such as Ag/AgCl needs to be used, where the potential difference between the solution and the electrode is constant regardless of the current level through the solution. Unfortunately, though, the chip's small size of near 5 millimeters in this experiment makes it difficult to adopt the reference electrode method. So, instead of the reference electrode, a bigger size electrode relative to active area are prepared and put deeply in the electrolyte drop so that the contact area between the electrolyte and the electrode is bigger than that between active oxide and electrolyte, which results in relatively high EDL capacitance and eventually reduced upper EDL potential difference. Also, high concentration electrolyte is used so that the capacitance of the EDL formed in the solution is not affected by the bias, and reduced the potential drop in the solution for minimum influence from the environments.

1.4 Outline of the Dissertation

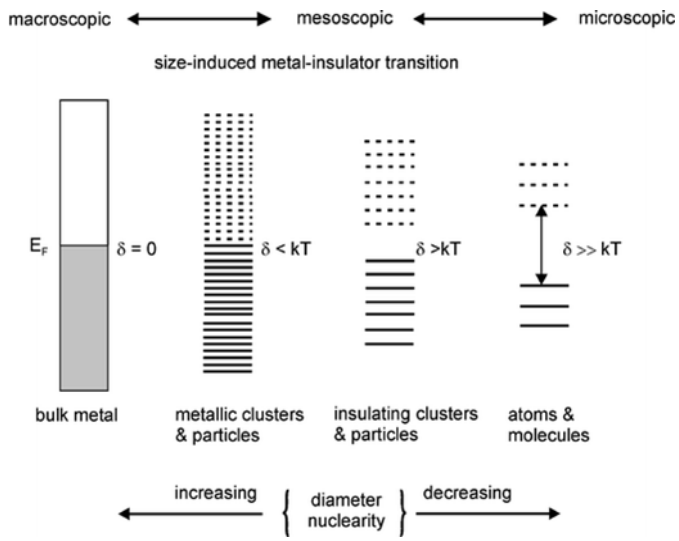
The primary purposes of this dissertation are to establish the optimized fabrication process of metal channel FET device manufacturing, to assess the thus manufactured device, and to clarify the principles of metal channel formation.

In chapter 2, the test pattern manufacturing process for the metal channel device fabrication and the preparation of necessary electrolyte for tunneling electroplating are described. And suggested 4-terminal electroplating process that forms metal channels, self-limitation phenomenon and its measurement method are also given.

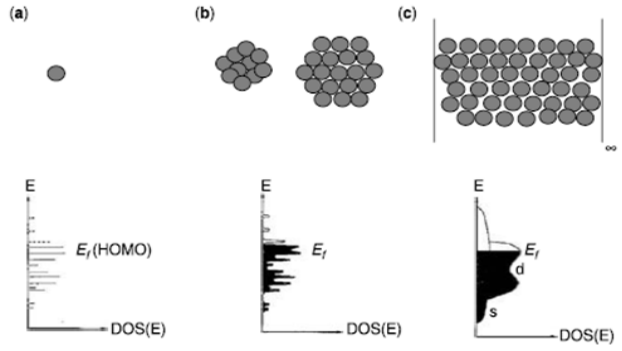
In chapter 3, to understand thin metal film formation process, the ion energy levels in electrolyte are predicted by the faraday current measured in Metal-Electrolyte-Metal (MEM) structure. By comparing the system characteristics of EOS, EMOS, and MOS, phenomena produced by EOS tunneling, their problems, and the improvement possibilities are studied. Also, metal particle formation in upper insulator through the EOS tunneling is studied.

In chapter 4, for actual metal channel FET realization, the electrode electroplating process for channel narrowing and surface treatment is explained. The tunneling current is flowed through the 3-terminal test pattern and the gold electrolyte to form the metal channel. The metal channel formation process is observed in real time, and effective limitation of the metal layer thickness is studied. The electrical characterization of the manufactured device also follows.

In Chapter 5, the summaries of the metal channel device fabrication and the electrical evaluation are provided. Further research possibilities in the thin metal layer characterization methods such as optical metrology and the other applications are also suggested.



(a)



(b)

Fig. 1-1. (a) Quantized energy levels with various metal size and (b) density of states with various metal sizes

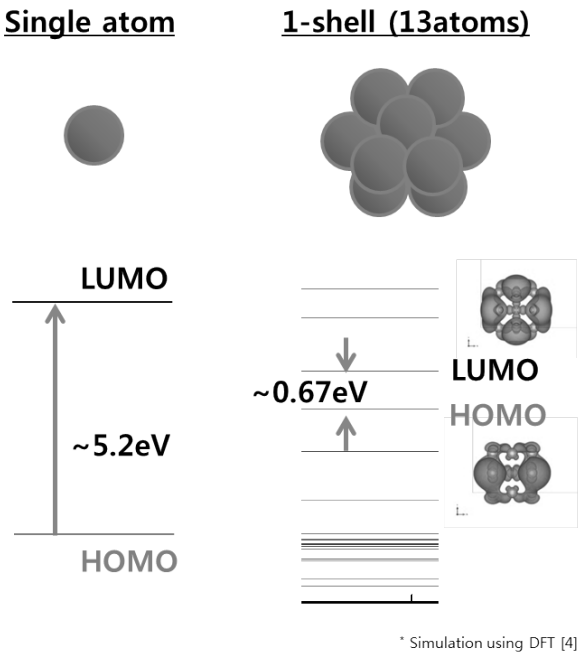


Fig. 1-2. Energy levels of single gold atom and 1-shell gold cluster.

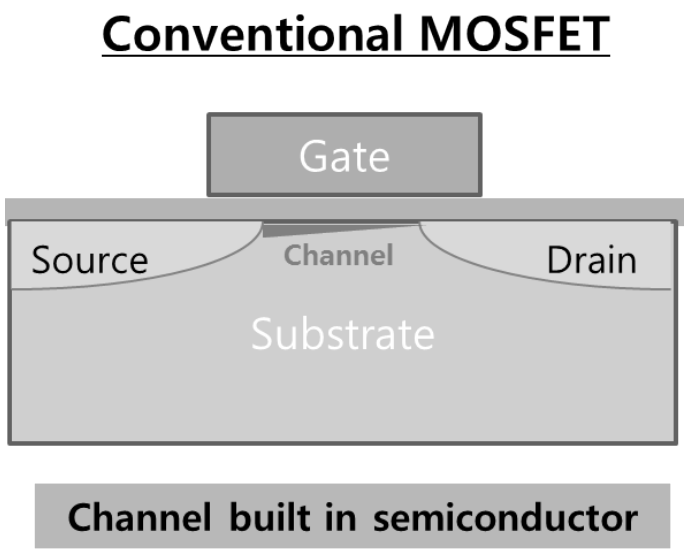


Fig. 1-3. Conventional MOSFET structure

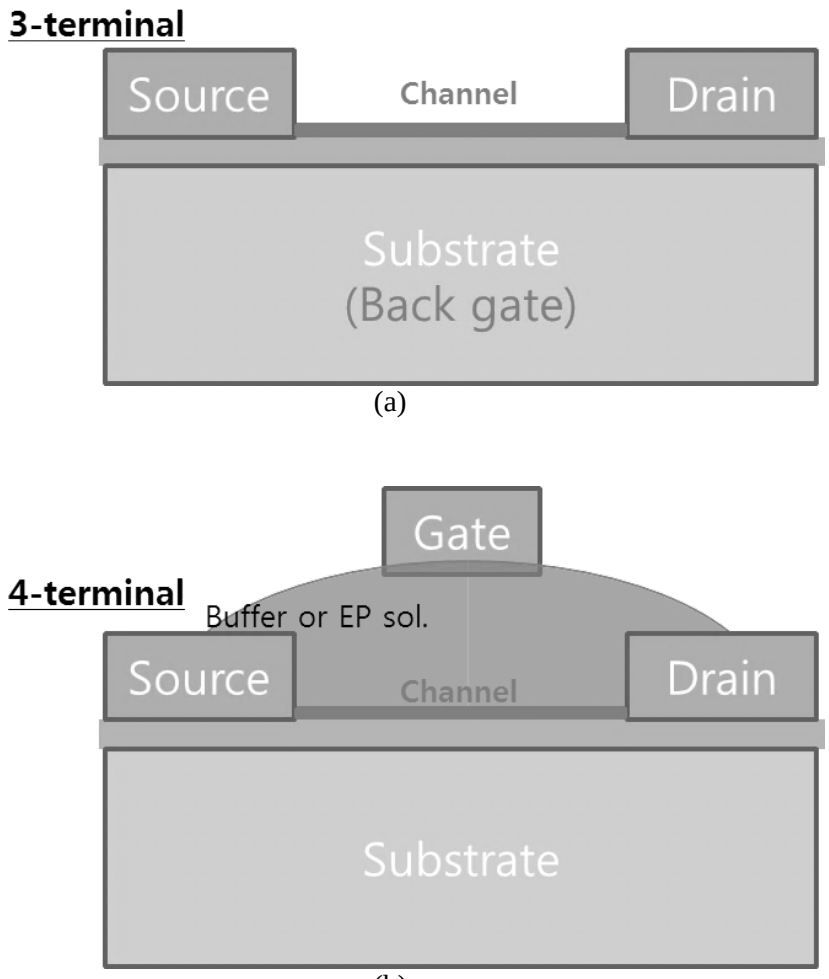
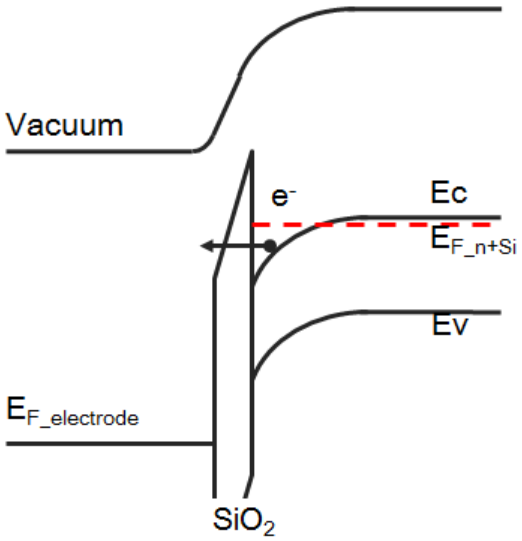
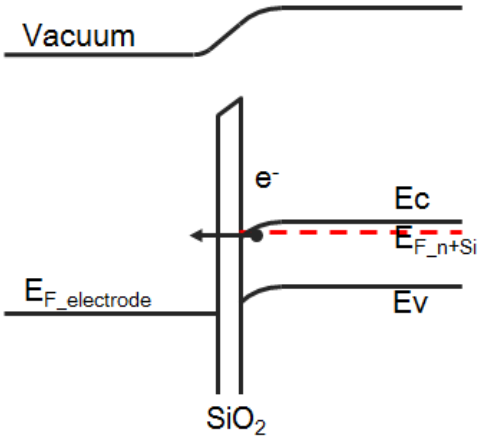


Fig. 1-4. (a) 3-terminal device and (b) 4-terminal device with the metal channel



(a)



(b)

Fig. 1-5. Band diagrams of (a) Fowler-Nordheim tunneling mechanism and (b) direct tunneling mechanism

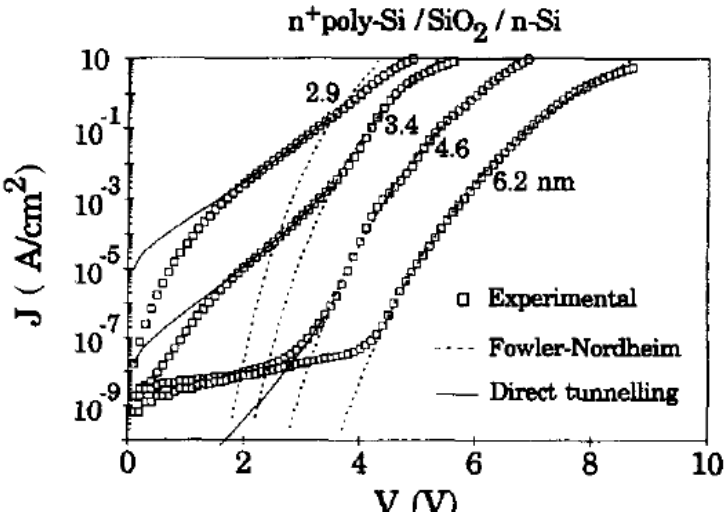


Fig. 1-6. Experimental results of F-N and direct tunneling current [31]

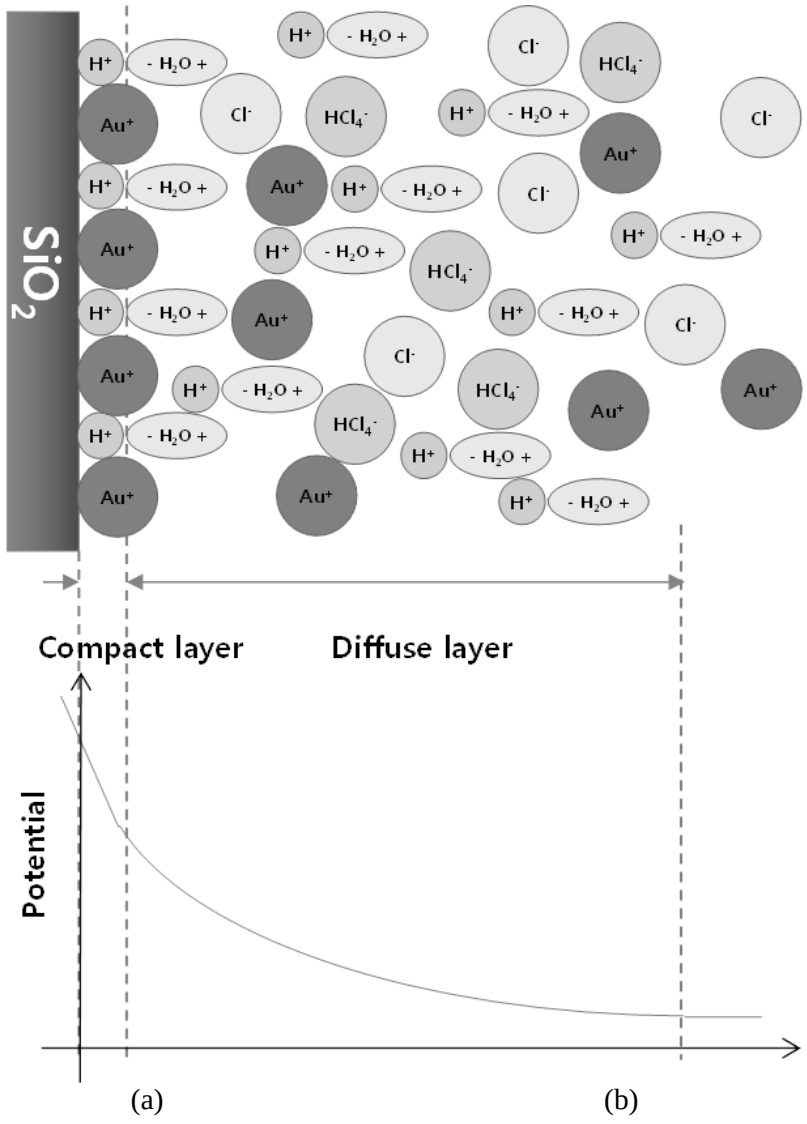


Fig. 1-7. Electrical Double Layer and the potential variation of Stern model

Chapter 2

Device fabrication

The semiconductor device manufacturing processes for the test chip in this thesis work are as follows.

Oxide tunneling current is used to make the metal channel. This kind of the tunneling current shows exponential behavior against the reciprocal of oxide thickness. [36-38] For effective control of the tunneling current, it is important to define the active region that is electrically isolated from other regions. Effective electrical isolation reduces the necessity of electrolyte-device contact area and also solve area reduction problem due to evaporation of the electrolyte during measurements. LOSCOS (LOCal Oxidation of Silicon) and STI (Shallow Trench Isolation) process are widely used silicon isolation techniques.[39] This thesis work excludes STI process because it needs to be guaranteed that tunneling oxide is defect free and STI interface oxide quality is dubious due to surface CMP(Chemical Mechanical Polishing).[40] Less confidence in academic quality STI as opposed to

industrial quality also plays a certain role.

Metal lift-off process follows the isolation process. It is necessary for the source and the drain electrode material to have comparable work function with that of channel metal. Therefore, metal deposition is done by gold evaporation, which is patterned by the lift-off technique simultaneously with the deposition. Finally, tunneling electroplating process is adopted for final metal channel formation in the manufactured test pattern (TEG: Test Element Group).

2.1 Fabrication of basic test pattern

In this section, aforementioned LOCOS process and a series of gate oxide and device electrode forming process are explained.

Substrate silicon wafers, which function as backside gates in 3 terminal devices, have low resistivity of 0.005(Ω•cm); The wafers are N-type [100] silicon treated with high concentration doping. This is because, if the substrate doping level is low, the depletion in the backside gate takes up some portion of the bias potential. The reason N-type wafers are used is to accumulate tunneling electrons in the substrate during the tunneling electroplating for metal channel formation.

Table 2-1 and Fig. 2-1 summarize the total process flow in device manufacturing including LOCOS process. Each wafer is assigned a number by laser marking when the process begins. Wafers for actual device fabrication and wafers for measurements of parameters such as oxide thickness are all included. Possible

organic materials and metal impurities on the wafers are removed by SC-1(Standard Cleaning-1) NH_4OH solution and SC-2(Standard Cleaning-2) HCl solution. Next, to construct LOCOS structure, the nitride layer that prevents oxygen diffusion into silicon surface is formed by LPCVD (Low Pressure Chemical Vapor Deposition) process. 200Å of buffer oxidation is done in furnace machine at this point to protect silicon surface. Active photo process is done, followed by the etching of nitride and oxide layer based on the constructed pattern, which results in the field oxide definition. Then 4000Å oxide layer is grown in the furnace by wet oxidation process. Now silicon surface is cleaned by BHF (Buffered HF) solution to obtain clean active part oxide layer free of remaining nitride. 60Å Gate oxidation growing is carried out by high temperature dry oxidation process in order to make robust films. Metal photo process for source/drain electrodes and metal evaporation process follow, which makes the whole process for test pattern fabrication complete. Electrode metals are Ti 500Å and Au 4000Å, where titanium is an adhesion enhancement metal that helps the gold adhesion on the oxide surface.

Fig. 2-2 (a) shows the shapes and the dimensions of the active and the metal pattern that are used in the test pattern. The active size width is 2~4 um, and the 2 um device channel length is given by metal electrode alignment. In the field shown in the figure, the substrate and the metal electrode are electrically insulated by 4000Å oxide, where the active is 60Å thick and the overlap between the active and the electrode is about a few micrometers.

Fig. 2-2 (b) is the vertical structure of the completed device, which is indicated by

red dotted line in Fig. 2-2 (a). It shows the active overlap shape of the metal electrode and the bird's beak formed during LOCOS process in silicon substrate.

2.2 Preparation of electrolyte

The target metal that is to be reduced is gold (Au) in this case, and for electrolyte, Gold (III) Chloride trihydrate ($HAuCl_4 \cdot 3H_2O$, Sigma Aldrich G4022-1G) 1wt% and Potassium Gold (III) Chloride ($KAuCl_4$, Sigma Aldrich 450235-1G) 1wt% solution are used. $HAuCl_4$ is used when hydrogen ion concentration (pH) is less than 6, specifically pH value of 1.1 and 3 in this experiment, and pH is controlled by hydrochloric acid (HCl). In cases of pH 6, 9 and 11, Buffer solution pH6, Potassium phosphate ($KH_2PO_4 + K_2HPO_4$) is used as a pH control solution, in which hydrogen ions decreases in the solution and hydrogen gas generation is limited. Low pH solution is advantageous in Au electrode spacing narrowing process because of lower surface roughness compared to high pH solution [31], while high pH solution is better suited to metal channel formation process by tunneling electroplating.

2.3 Fabrication process of Metal channel device

Fig. 2-3 (a), (b) are photos of metal channel formation processes. As shown in (a), the test pattern on the silicon substrate undergoes backside scratch with diamond pencil, then it is attached to glass by silver paste to limit leakage current to manipulator. Now electrolyte is dropped in the 2-step well that is made using

Polydimethylsiloxane (PDMS) film manufactured with punch(Fig. 2-2 (b)), which keeps the contact area between the electrolyte and the chip surface constant even under repeated and prolonged experimental condition. The probe station tips used in source, drain, and substrate are gold coated, the tip for Au electrolyte is Au (∅0.5mm) wire, and Pt (∅0.5mm) wire is used for other electrodes.

Fig. 2-3 shows a bias for 4 electrodes and electron movement in an early stage of metal channel formation process. Test pattern substrate potential is 0V, and the source, the drain, and the Au tip that dips electrolyte are at 3 V for tunneling voltage. 0.1 V difference between the source and the drain electrodes is for confirmation of the electrical connection between two electrodes during the channel formation, and the voltage difference between the source (or drain) and the electrolyte electrodes is to prevent the formation of additional metal layers on the electrode surface. The electron migration is indicated by the red line in the figure. Electrons experience MOS tunneling from the substrate to the source and the drain electrodes, and undergo EOS tunneling to electrolyte. The electrons infused into the source and the drain readily escape through the electrodes, but the electrons that enter the electrolyte reduce Au^{+} or Au^{3+} ions in the solution to accumulate solid Au on the surface. Because of the EDL formation between the electrolyte and the oxide surface, the electric potential of the electrolyte itself is a little bit lower than that of Au tip, which may result in Au dissolution of the drain side and its infusion to the electrolyte.

As this phenomenon continues, Au atoms keep accumulating on the active oxide,

and electrons influent to Au atoms now moves into the electrolyte, which generates cluster of gold particles by reduction reaction near the atoms. If this particle gets in contact with the source or the drain electrodes, electrons influent to Au particles go outside through the source or the drain electrodes instead of moving to the electrolyte, which means no Au atom integration on the particles that are in contact with the source or the drain. I call this suppression of Au particle integration 'Self limitation'. Continuing bias on the test chip makes the metal layer area bigger continuously, which results in electrical connection between the source and the drain electrodes and rapidly increasing drain current. This is the metal channel formation.

Detailed metal channel formation mechanics is presented in chapter 4.

.

2.4 Measurement system for analysis

Agilent 4156C semiconductor parameter analyzer was used for current-voltage characteristics measurement in this experiment.

For the investigation of the metal surface of the EMOS system, I used the non-contact mode of an atomic force microscope (AFM) (model XE-150 by Park Systems)

Fluorescence microscope was used to make sure fluorescence treated DNA is properly attached to the surface. The DNA is to confirm that the generated particles on the oxide surface are metals.

Seq-No	Process	Condition
10	Wafer marking	
20	SC-1,2 cleaning	
30	CMOS furnace (Dry oxidation) Buffer oxidation 200 Å	950℃, 720”
40	SC-1,2 cleaning	
50	CMOS LPCVD (Nitride) Oxygen diffusion barrier 1000 Å	785℃, 1320”
60	Active align (MA-6 II) - AZ1512	12”
70	W10D(WS-10, C1-2) development AZ300	60”+
80	P-5000 I SiO/SiN Etch Nitride 1000 Å etching, SiO_2 open	
90	P-5000 I SiO/SiN Etch SiO_2 200 Å etching, SiO_2 open	
100	Tepla300 (PR ashing)	
110	SPM-PR STRIP	
120	SC-1,2 cleaning	
130	CMOS furnace (Wet oxidation) Field oxide 4000 Å	
140	Nitride 1000 Å strip	
150	BHF 7:1 Oxide 200 Å strip	
160	CMOS furnace (Dry oxidation) Gate oxide 60 Å	
170	Metal align (MA-6 II) – AZ5214	Negative 12”
180	W10D(WS-10, C1-2) DEVELOP AZ300	60”+
190	E-gun evaporator Ti 500 Å, Au 4000 Å	
200	Lift off (Sonication)	Acetone

Table 2-1. Process flow table of test pattern fabrication

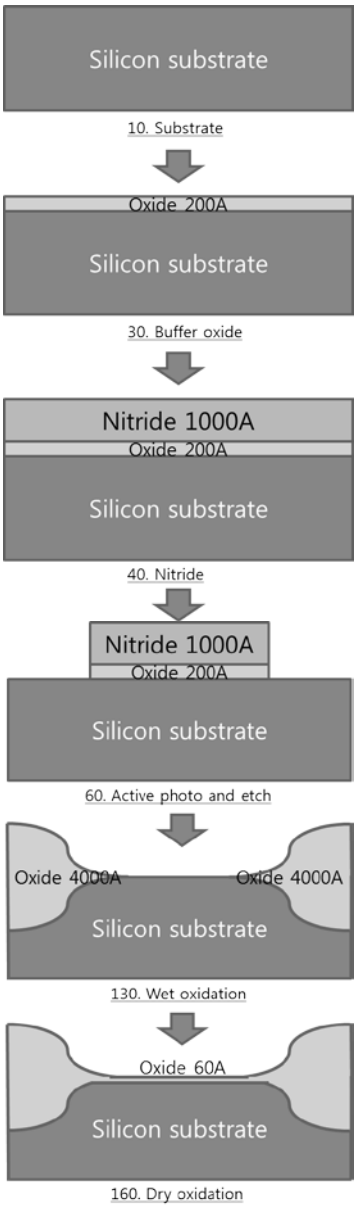
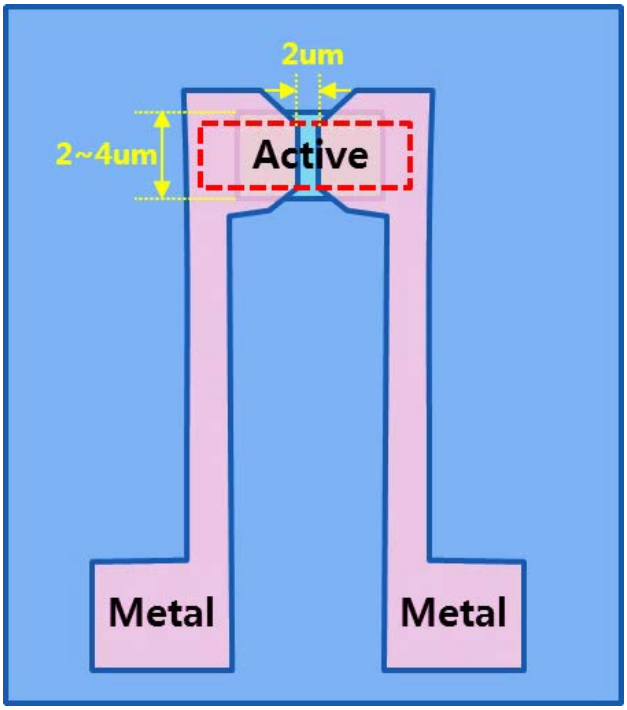
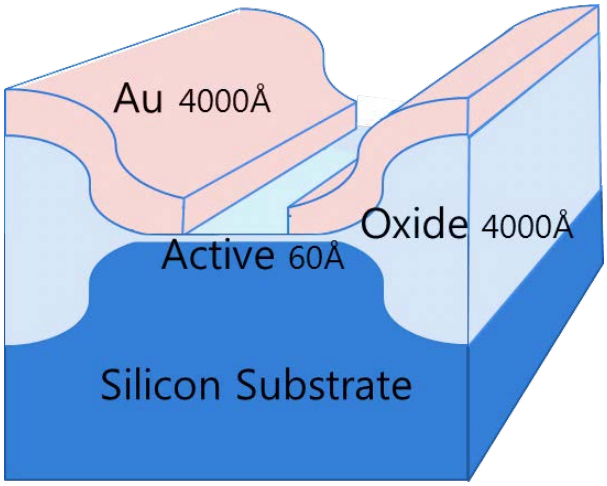


Fig. 2-1. Vertical structure of the each process flow

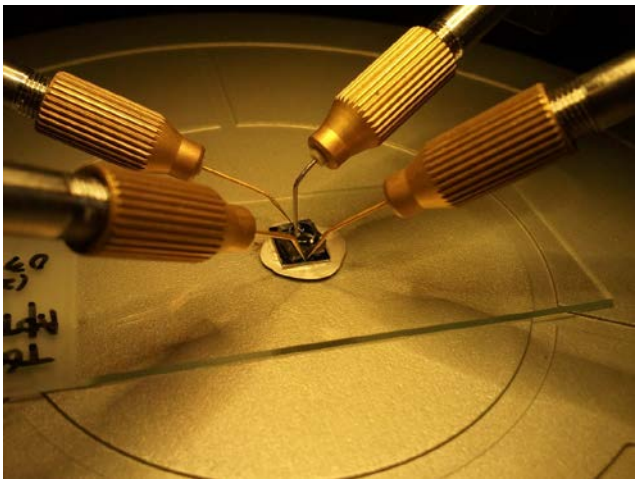


(a)

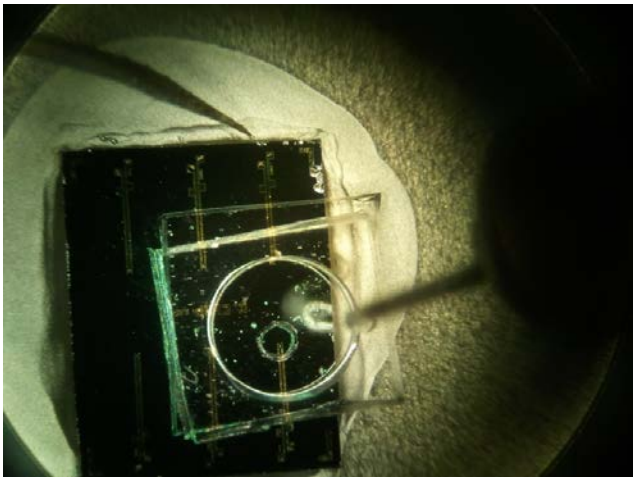


(b)

Fig. 2-2. (a) Test pattern layout and dimension and (b) Vertical structure of final test pattern (Pink: metal, sky blue: oxide, blue: substrate)

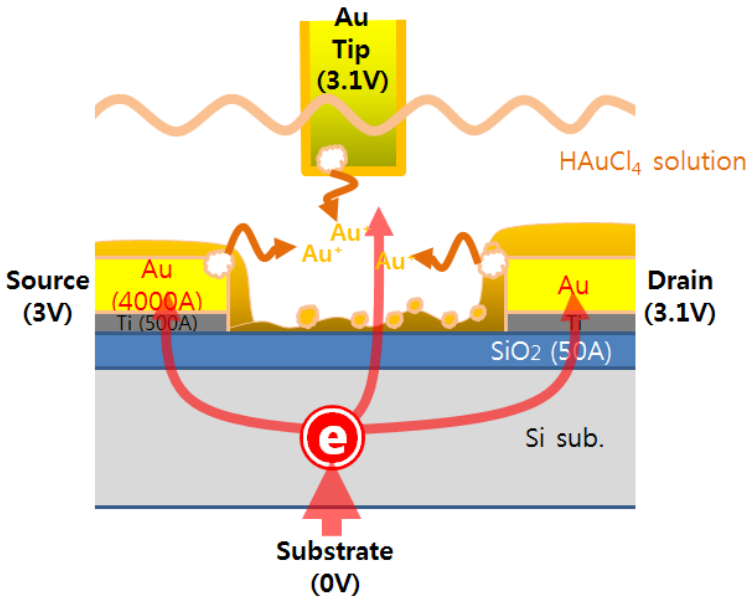


(a)

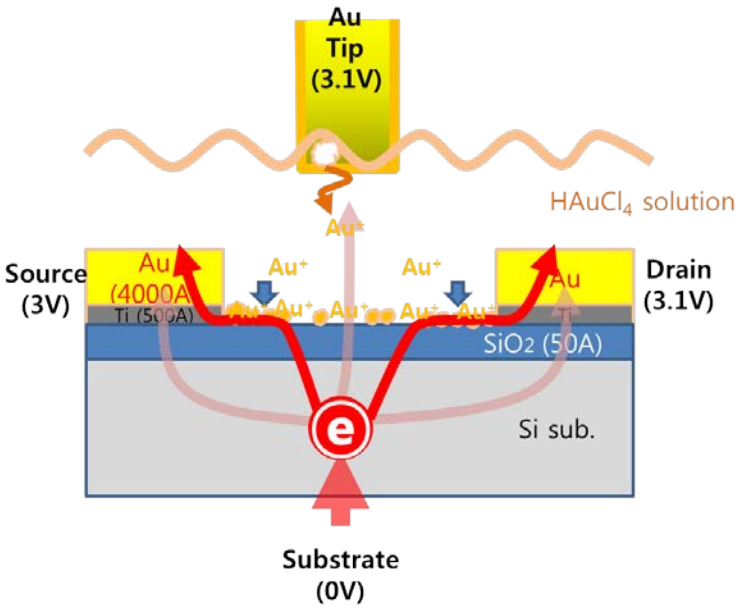


(b)

Fig. 2-3. (a) Picture of the metal channel generation experiment and (b) microscopic view of experiment



(a)



(b)

Fig. 2-4. Schematic diagrams of (a) electron tunneling and (b) self-limitation phenomenon

Chapter 3

Investigation on tunneling electroplating

3.1 Metal-Electrolyte-Metal (MEM) system

Experimental environment for the metal channel fabrication was described in the previous chapter. Now, as the next step in building thin metal layers, analysis and modeling starts with the basic Metal-Electrolyte-Metal (MEM) system where the metal and the electrolyte make direct contact. With lack of physical and chemical complexities unlike EOS system, MEM system is relatively straightforward for the analysis. [41]

3.1.1 Metal-Electrolyte-Metal system

Fig. 3-1(a) shows the schematic diagram of the metal channel formation environment with addition of an equivalent circuit. Au solution is dropped on the test pattern and 3V voltage is applied to the immersed Au tip. The test chip bias

condition is complete with 2.9V at the source, 3.0V at the drain, and 0V at the substrate. We can view this as a combination of two separate systems; one is a MEM system that includes the top side Au tip and all the way down to source or drain through electrolyte, and the other one is a metal-Electrolyte-Oxide-Silicon (mEOS) system that includes the top metal tip and electrolyte-oxide-substrate connection. The latter is usually called Electrolyte-Oxide-Silicon (EOS) system because a reference electrode is often connected to the electrolyte in some applications. [42-44] In this section, a circuit is established through the red line in Fig. 3-1 (a), and it is analyzed using energy band diagram, in the purpose of MEM system electrical analysis.

Fig. 3-1 (b) shows an equivalent circuit of the MEM system. [34] The EDL layer formed along the Au tip submerged in the upper electrolyte area can be expressed as a parallel connection of a capacitor and a resistor. Another resistor is connected in series with this pair, the resistance value of which is determined by the type and the concentration of ions in the electrolyte, which completes the equivalent circuit.

Fig. 3-2 shows the potential distribution along the MEM system, considering the equivalent circuit. A potential drop is caused by the compact layer and the diffuse layer formed along the Au tip and electrolyte interface. [24-25] Smaller potential drop is observed due to electrolyte resistance, and another potential drop happens on the chip surface electrode due to the diffuse layer and the compact layer.

Fig. 3-3 shows a schematic of experimental environments to electrically understand the reduction phenomenon of the MEM system. Thick insulator film of

4000Å on the silicon substrate minimizes the leakage current in the lower part, and lower electrode is completed with 4000Å Au film on that insulator. On top of that, 10uL electrolyte is dropped so that it is smaller than the lower electrode area, and the Au tip is immersed. Two kinds of electrolyte are used; HCl 1% only, and a mixture of this and $HAuCl_4$. Top Au tip is applied with 0 to 5V voltage, and it is used as the counter electrode, while the bottom Au pattern potential is fixed at 0 V and is used as the electron emitting working electrode.

Fig. 3-4 (a) is a faraday current graph of the MEM system with HCl 1% only electrolyte. There are only H^+ positive ions inside the electrolyte, and only hydrogen ion reduction reaction happens near the working electrode. It is shown that the system current increases gradually as the counter electrode voltage increases. Notably, the current increase becomes dramatic beyond 2V bias, when the bubble formation in the electrode is observed with a microscope. The current momentarily decreases as H^+ ions on the working electrode surface are all used up, but it increases again as the reduction reaction increase with the positive ions in the electrolyte moving to the surface. Fig. 3-4 (b) is a log scale presentation of graph (a). Another peak around 1.5 V is related to oxygen gas in the water and will be revisited later on in this thesis.

Fig. 3-5 (a) shows the results of the iterated current density measurements against the increasing counter electrode voltage to investigate Au reduction reaction in $HAuCl_4$ added electrolyte. Unlike Fig. 3-4 (a), this shows current increase near 1V and peaks around 2V voltage. The former is due to the influence of $HAuCl_4$ added to

the electrolyte, and the latter is due to the reduction reaction of Au^{+} ions and Au^{3+} ions added to the solution. This is showed more clearly in Fig. 3-4 (b) log scale graph.

To verify the relationship between the MEM system current and the reduction reaction potential, the result is presented in Fig. 3-6, where H^{+} ion reduction potential is located at 2.2V peak. Reduction reaction possibilities in the electrolyte including $HAuCl_4$ are shown in Table 3-1.

Among these reactions, Au ion is included in the reactions involving 0.93 V, 1.22 V and 1.83 V, in which Au(s) is produced, while Au ion in not involved in the reactions which produce H_2(Gas), $4OH^{-}$, $4Cl^{-}$, and $2H_2O$. Fig. 3-6 graph is essentially rearrangement of the reactions, where high quantity hydrogen gas producing 2.2 V peak is at the center. The red curve represents the virtual potential variation range considering Nernst equation, and this varies according to the changing concentration during the reaction.[40] Au production bias condition predicted in Fig. 3-5 is verified here, and this means that Au particle are produced under counter electrode voltage of 0.4 ~ 1.3 V.

3.1.2 Band diagram of Metal-Electrolyte-Metal system

Based on the result in the previous section, MEM structure energy band diagram is to be investigated here. It is necessary to understand the electrolyte band diagram and the ion energy levels in the electrolyte, to obtain the MEM structure band diagram. Basically, electrolyte is a H_2O based solution. It is well known that H_2O is

a bent structure polar molecule with 104^{o} bonding angle. Although electrons don't have clearly fixed bandgap in the solution with this kind of molecule cluster as opposed to the semiconductor crystal, we can consider this a virtual semiconductor-like material by analogizing Lowest Unoccupied Molecular Orbital (LUMO) level to the conduction band edge and Highest Occupied Molecular Orbital (HOMO) level to valence band edge. It can be argued valid in that LUMO is the lowest energy level electrons can occupy and HOMO is the highest energy level electrons can occupy. [45-46] Fig. 3-7 is the water band gap for the bulk water electronic structure analysis that is obtained by the cluster study which gives information on water bandgap and vacuum level position. [45]

In the figure, the valence band edge is a molecule consisting of two H_2O's, and the conduction band edge is the combination of H_3O (aq) + OH (aq) + e^-. The energy difference between the valence band edge and the conduction band edge is about 6.9 eV, and the energy difference between the conduction band edge and the vacuum level is 0.12 eV.

This calculation can be done from the following reduction reactions;

OH^- (aq) + e^- (cond.) → OH^- (aq) : -6.31eV

$2H_2O$ (l) → OH^- (aq) + H_3O^+ (aq) : +0.58eV

Necessary energy for $2H_2O$ (l) decomposing into OH^- (aq) + H_3O^+ (aq) and then OH^- (aq) + H_3O (aq) converting to H_3O (aq) + OH^- (aq) +e^- (cond.) is 6.89 eV which is the bandgap of the water molecule.

3.1.3 Reduction of metal ion

Now, $HAuCl_4$ containing electrolyte MEM structure band diagram is to be obtained from the H_2O energy band predicted in the previous section.

Fig. 3-8 is the MEM structure band diagram in equilibrium with counter electrode voltage at 0V. By equating relevant Fermi levels, we can see H^+ ion energy level is above the Au metal electrode work function (5.3eV), and those of Au^{3+} (5.96eV) and Au^+ (6.27eV) ions are located below that.

Fig. 3-9 the band diagram under 0.4V bias condition at which Au particles begin to be generated. For the assumption that voltage is divided equally in the both ends, the area between top metal tip and the electrolyte and the area between lower electrode and the electrolyte are kept similar. Under 0.4V condition, H^+ ion energy level is located higher than Au metal energy level, so hydrogen ion reduction doesn't take place, and in the lower part, Au ions can combine to form Au particles.

Fig. 3-10 is the band diagram under 2.3V bias condition where H_2 bubbles start to form. Hydrogen ion energy level is comparable to working electrode energy level or a little bit below, and this shows that reductions of hydrogen ion and Au ion can take place simultaneously.

Understanding electroplating band diagram in the MEM system helps us analyze the production of Au and H_2 in terms of semiconductor modeling, and it can also serve as the basis for the EOS system analysis in the next section.

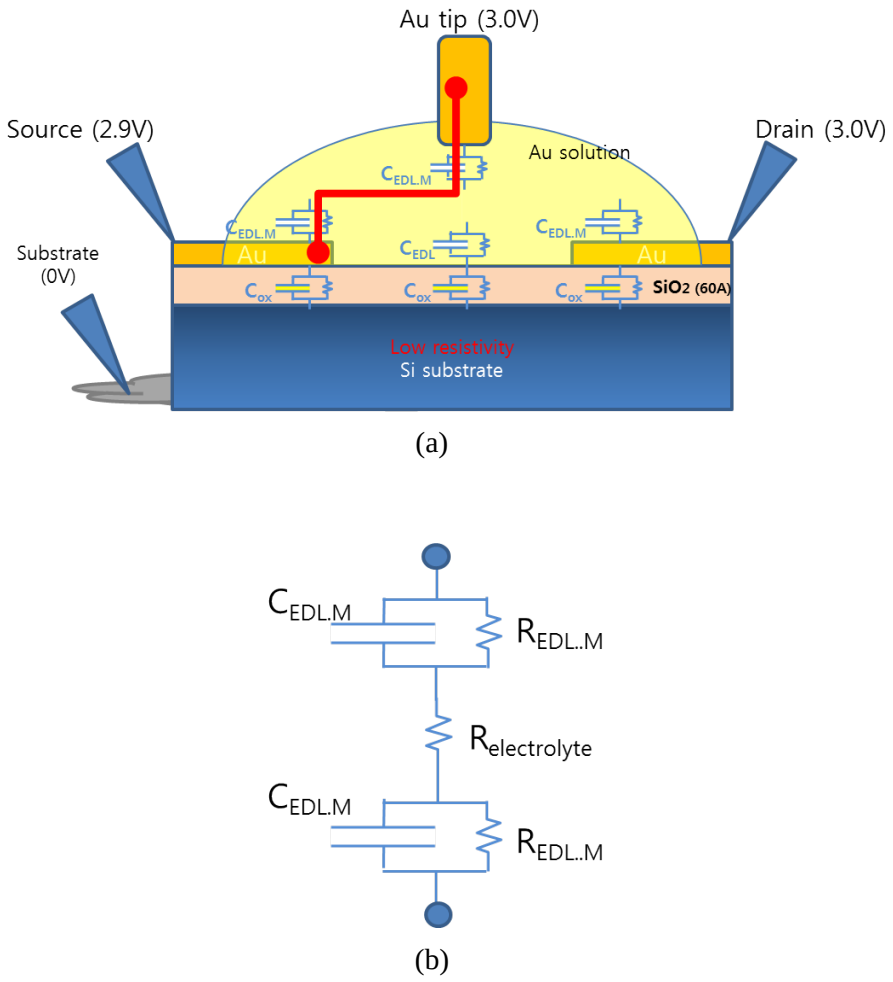


Fig. 3-1. (a) Schematic diagram for the measurement of the electrical characteristics within metal formation (Red line: MEM structure) and (b) equivalent circuit of MEM system

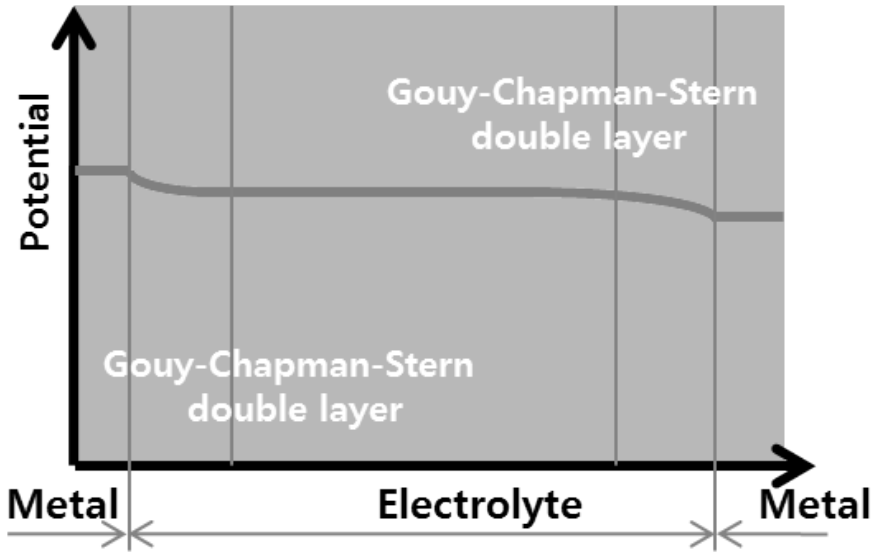


Fig. 3-2. Potential diagram of MEM structure which is contained Gouy-Chapman and Stern model

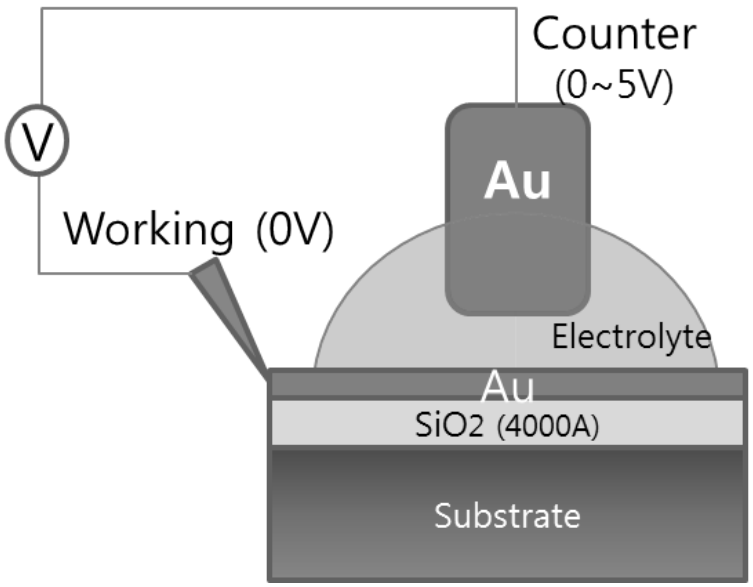
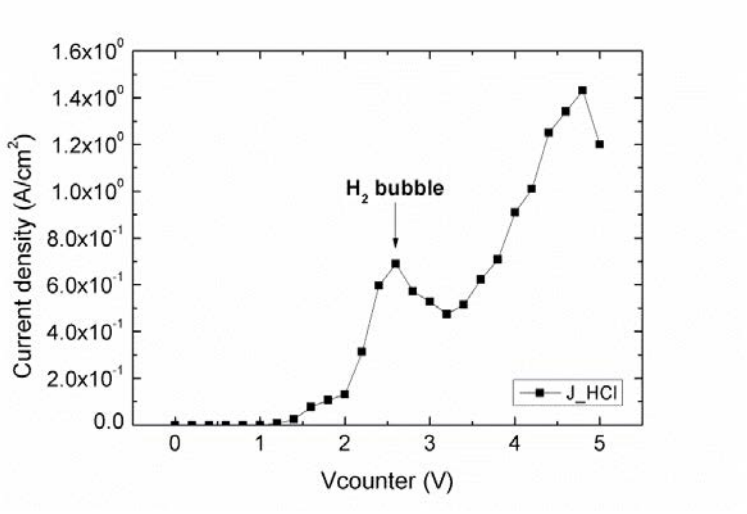
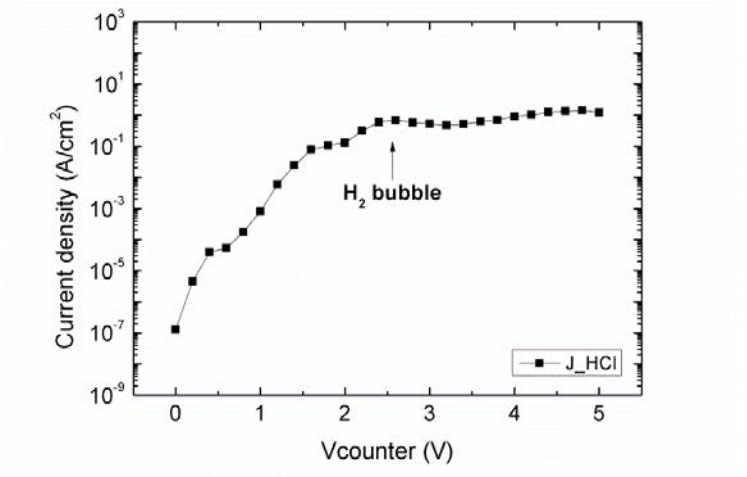


Fig. 3-3. Schematic diagram for the measurement methods which can be used for the MEM structure

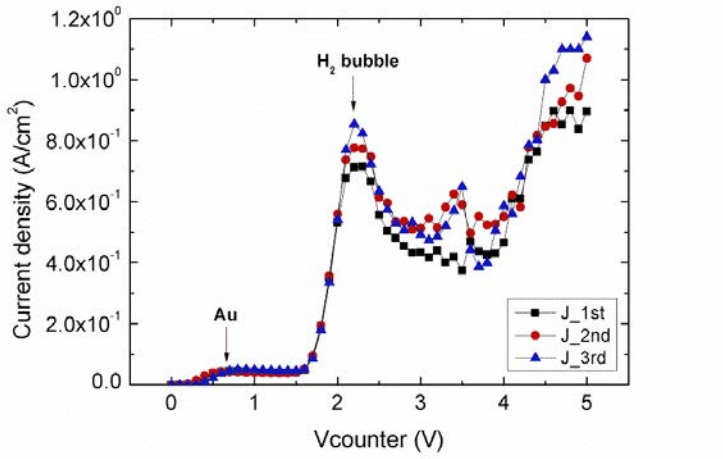


(a)

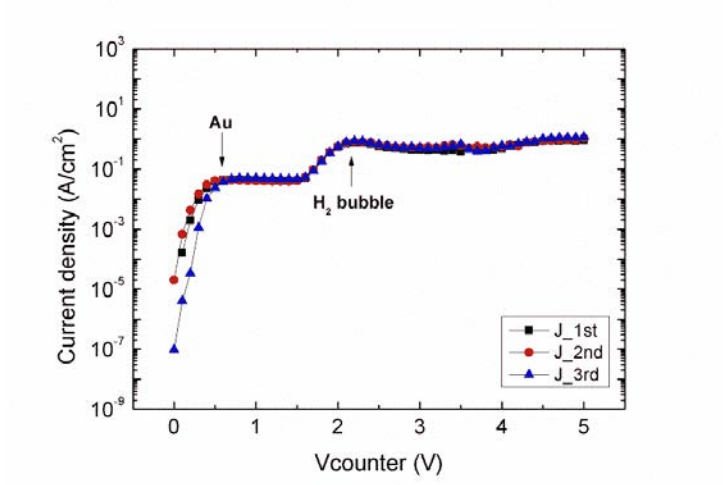


(b)

Fig. 3-4. Reduction reaction current-voltage characteristics of hydrogen ion in MEM system with HCl only (a) linear scale and (b) log scale



(a)



(b)

Fig. 3-5. Reduction reaction current-voltage characteristics of hydrogen ion in MEM system with $HAuCl_4$ and HCl (a) linear scale and (b) log scale

Reaction	Reduction potential [V]
$2H^{+} + 2e^{-} \rightarrow H_2(G)$	0
$O_2(G) + 2H_2O + 4e^{-} \rightarrow 4OH^{-}$	0.41
$[AuCl4]^{-} + 3e^{-} \rightarrow Au(S) + 4Cl^{-}$	0.93
$O_2(G) + 4H^{+} + 4e^{-} \rightarrow 2H_2O$	1.23
$Au^{3+} + 3e^{-} \rightarrow Au(S)$	1.52
$Au^{+} + e^{-} \rightarrow Au(S)$	1.83

Table 3-1. Standard reduction potentials at 25℃ with the electrolyte of $HAuCl_4 + HCl$

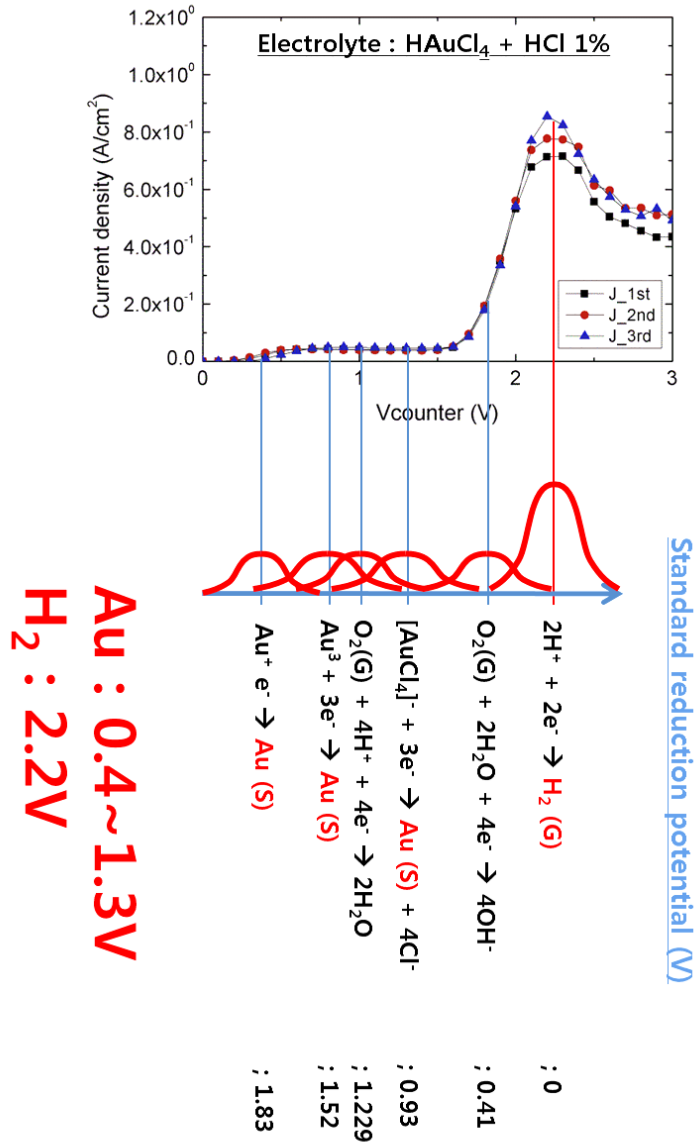


Fig. 3-6. Correlation between current-voltage characteristics and standard reduction potentials in given MEM system

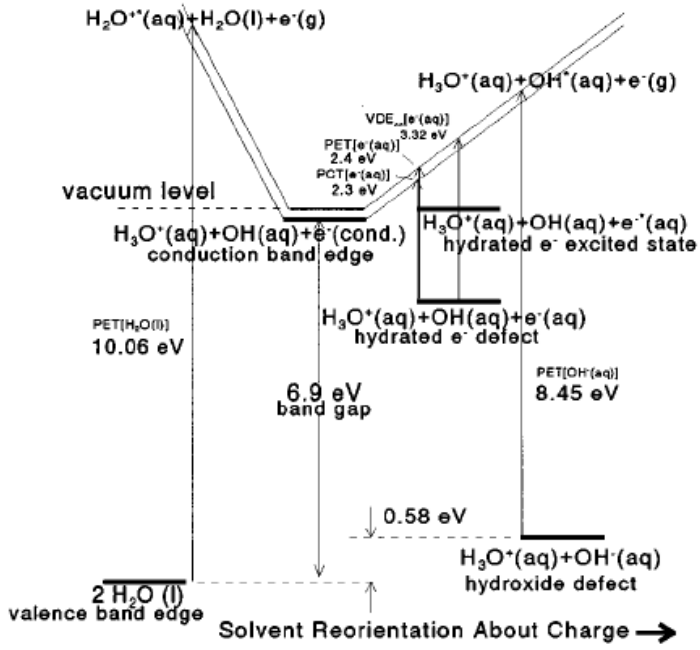


Fig. 3-7. Energy diagram for bulk water which incorporates the effect of reorientation of solvating water molecules about charge [45]

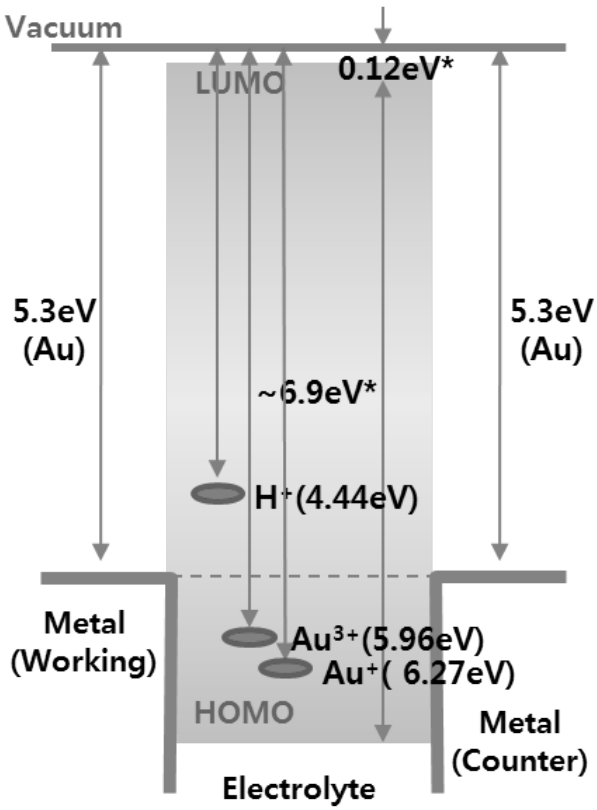


Fig. 3-8. Energy band diagram of given MEM system ($V_{counter}$=0V, $V_{working}$=0V)

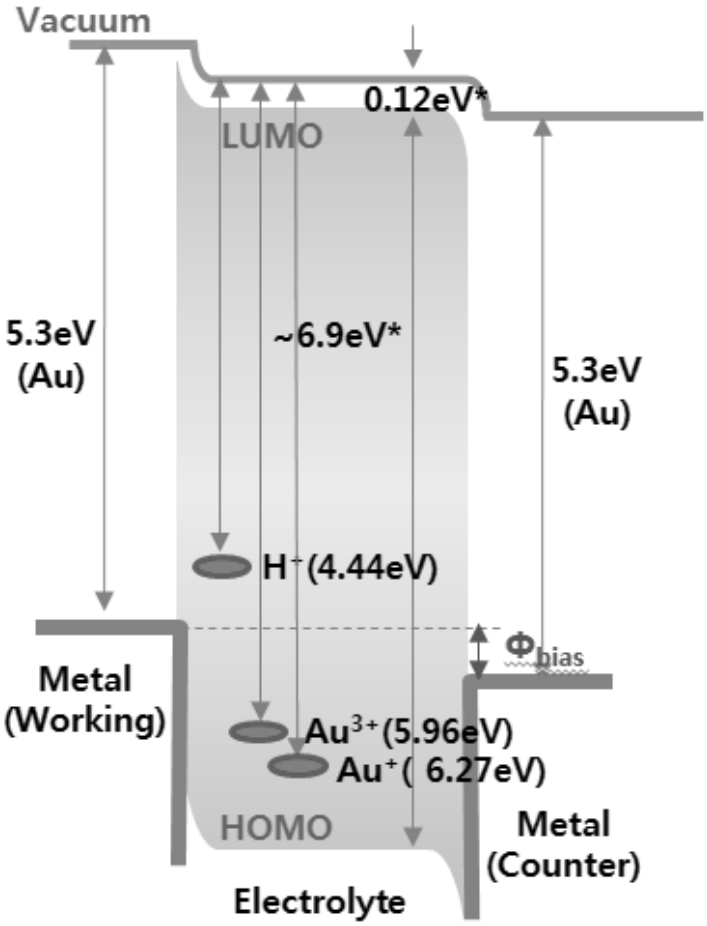


Fig. 3-9. Energy band diagram of given MEM system ($V_{counter}$=0.4V, $V_{working}$=0V)

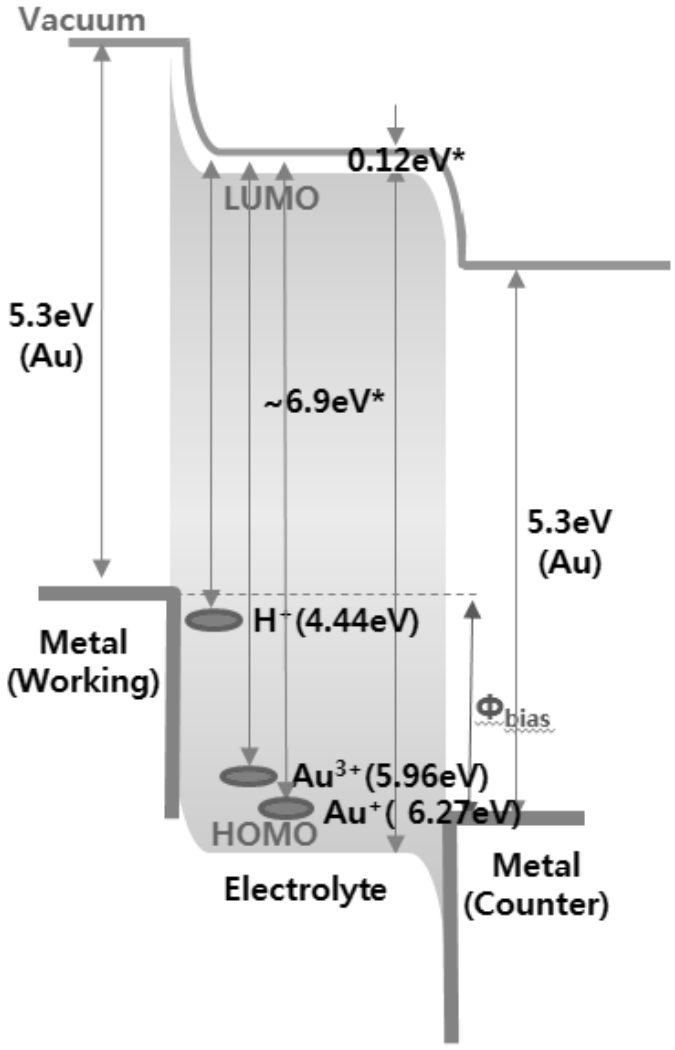


Fig. 3-10. Energy band diagram of given MEM system ($V_{counter}$=2.2V, $V_{working}$=0V)

3.2 Electrolyte-Metal-Oxide-Silicon (EMOS) system

Fig. 3-11 is a schematic diagram of metal channel formation environments with addition of virtual equivalent circuit. With the bias as in the figure, Electrolyte-Oxide-Silicon (EOS) system is formed, consisting of top metal tip, electrolyte, oxide and the substrate. Fig. 3-11(b) is an equivalent circuit along the EOS system. The resistance of EDL layer along immersed Au tip surface and the electrolyte is connected in series. A parallel connection of the resistor and the capacitor of EDL along the oxide surface as well as oxide capacitor completes the equivalent circuit.

Fig. 3-12 is the potential distribution along the EOS system with consideration of the equivalent circuit. [34] A potential drop occurs due to EDL in the left side where Au tip and the electrolyte come in contact, and a minor potential drop occurs again due to the electrolyte resistance control. Another EDL is formed on the chip surface oxide, which causes a potential drop due to diffuse layer and compact layer. [24-25] Also, the potential distribution due to the depletion in oxide and silicon substrate needs to be considered.

The electrical analysis of EOS systems can be complicated in itself by the radical variation of ion density on the oxide surface due to its reduction. Therefore, analysis of mEMOS (metal-Electrolyte-Metal-Oxide-Silicon) system, which is a combination of well-known MOS system and aforementioned MEM system, can be helpful in understanding the experimental environment of EOS system.

3.2.1 Band diagram of Electrolyte-Metal-Oxide-Silicon system

Fig. 3.13 shows EMOS system band diagram using water band model as is done with the MEM structure previously. [45-46] When counter metal electrode and substrate voltage is at 0V, n-type silicon fermi level aligns with metal work function as in the figure. Here, the left side is a MOS system and the right side is a MEM system, and the metal layer in the oxide surface is electrically floating. Au work function energy of 5.3eV is sandwiched between the hydrogen energy level (4.44eV) and the gold ion energy level (5.96eV) in the electrolyte. Higher counter electrode voltage of 3.5V alters the band diagram as in Fig. 3-14. It is assumed that the voltage loss is small because the electrolyte concentration is quite high and the area of the immersed Au tip contact area is relatively large. Most potential is applied to the oxide layer, which has higher resistance ($>10^6 \Omega/cm^2$) than electrolyte and smaller capacitance per area (C_{ox}~1.73uF/cm^2) than the EDL of the electrolyte (C_{EDL}~69.4uF/cm^2). Tunneling electrons through the oxide from the silicon fermi level migrate into the metal on the oxide surface, after which electrons behave as in the low voltage application case of MEM systems and help forming Au atoms on the surface. Hydrogen gas is not supposed to be produced on the surface because the oxide surface metal energy level is lower than that of hydrogen ion, and actual experiment also confirmed that the hydrogen gas bubbles do not form on the metal surface in this condition.

3.2.2 Tunneling current of Electrolyte-Metal-Oxide-Silicon system

In an effort to understand EOS system tunneling current, the current and voltage characteristics of electrically simpler EMOS system is investigated. [32]

Fig. 3-15 (a) is the experiment schematic to study EMOS system. KCl solution is dropped on the MOS test pattern, and a Pt tip is immersed. Potassium ion is not reduced in the process because it has higher energy level than that of hydrogen ion, and platinum metal is not oxidized in the electrolyte and has no effect on the electrolyte composition. 1M, 10mM, and 1mM KCl solutions are prepared so that experiments are split according to the electrolyte resistance. Electrical bias is applied on Pt tip and N-type silicon substrate, and the current through the oxide/electrolyte and the voltage of the metal on the oxide are monitored. Fig. 3-15 (b) is an equivalent circuit of the EMOS system. If the contact area of the immersed Pt tip is relatively large compared to that of the lower metal and the electrolyte, and if the electrolyte resistance is small due to its high concentration, and also if N-type silicon resistivity is relatively very low, then the total potential difference (V_{bias}) on the system is the sum of the potential difference across the oxide (V_{ox}) and the EDL potential difference across the metal (V_{EDL}).

$V_{bias} = V_{ox} + V_{EDL}$ (eq. 4)

If we can say that EMOS system tunneling property is also dependent on the magnitude of the electric field on the oxide, just as in the MOS system, the current density difference between two systems would essentially stem from the electric field magnitude difference on the oxide. For the same oxide thickness and substrate

material, tunneling current density due to V_{ox} is supposed to be same. [32] To verify this statement, I measured the variations of the current density and V_{ox} simultaneously according to the bias voltage. Fig. 3-16 (a) is the comparison of the current densities of EMOS system and MOS system against V_{bias}. EMOS system shows a little bit of difference in current level due to the resistance difference according to the electrolyte concentration, and it is generally lower than that of MOS system. Fig. 3-16 (b) is a plot of this current value vs. V_{ox} which is measured with V_{bias} change. In this figure, the current densities between MOS and EMOS systems vs. V_{ox} are shown to be same, which means the current is driven by the voltage across the oxide in the EMOS system just like the MOS system. [32]

This is applied in EOS system experiment as in Fig. 3-17. Test pattern is basically same with the pattern shown in Fig. 3-15, but metal on the upper oxide is opened so that EOS system current can be monitored. In Fig. 3-18 (a), EOS system and MOS system show different current values against V_{bias}, but if the currents are plotted against the potential difference across the oxide (V_{ox}), which is simultaneously measured with V_{bias}, both systems show the same current characteristics.

This means that tunneling electron transport at the oxide-electrolyte interface of EOS system has the same mechanism with the tunneling electron transport at the oxide-metal interface of MOS system, and the tunneling current magnitude is proportional to the electric field magnitude in the oxide. [32]

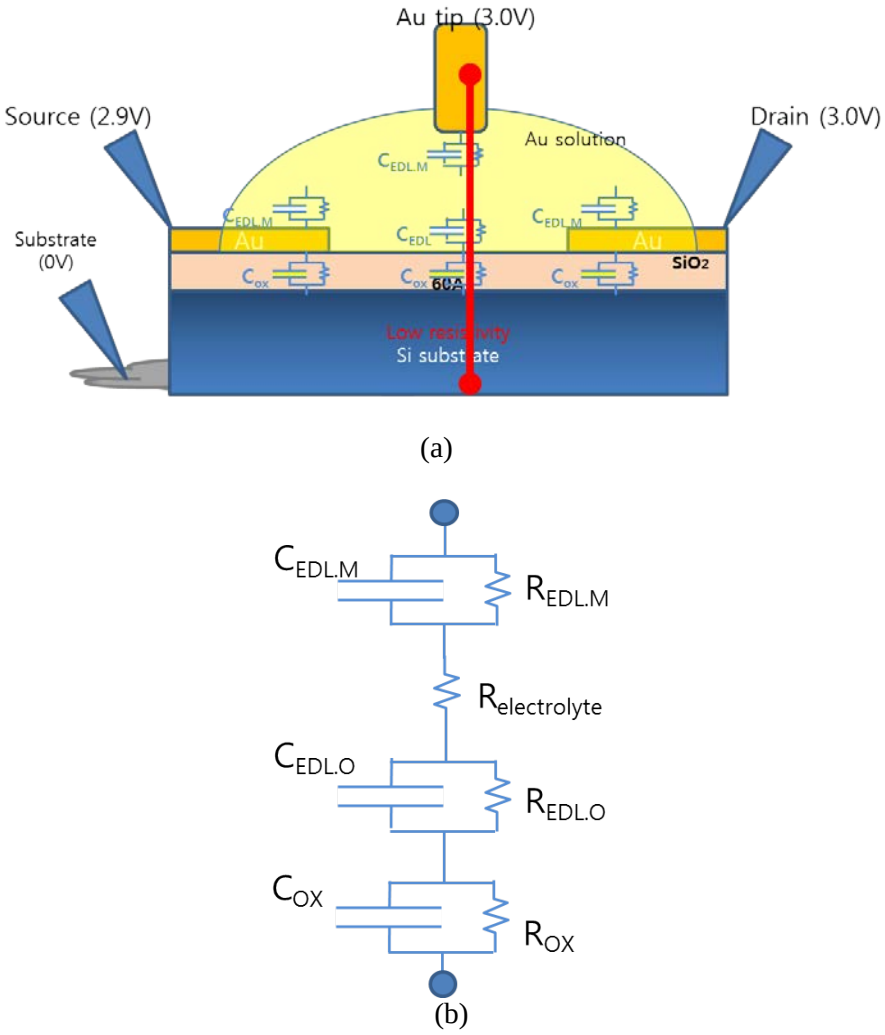


Fig. 3-11. Schematic diagram for the measurement of the electrical characteristics within metal formation (Red line: MEM structure) and (b) equivalent circuit of mEOS system

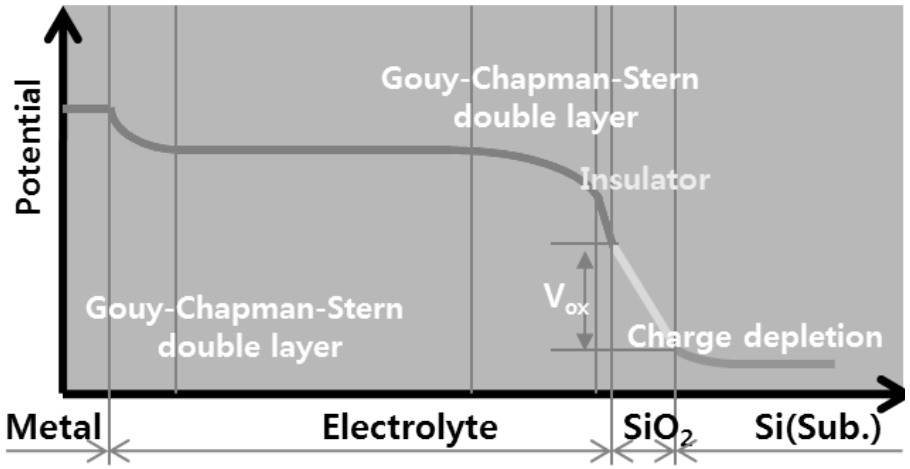


Fig. 3-12. Potential diagram of mEOS structure which is contained Gouy-Chapman and Stern model

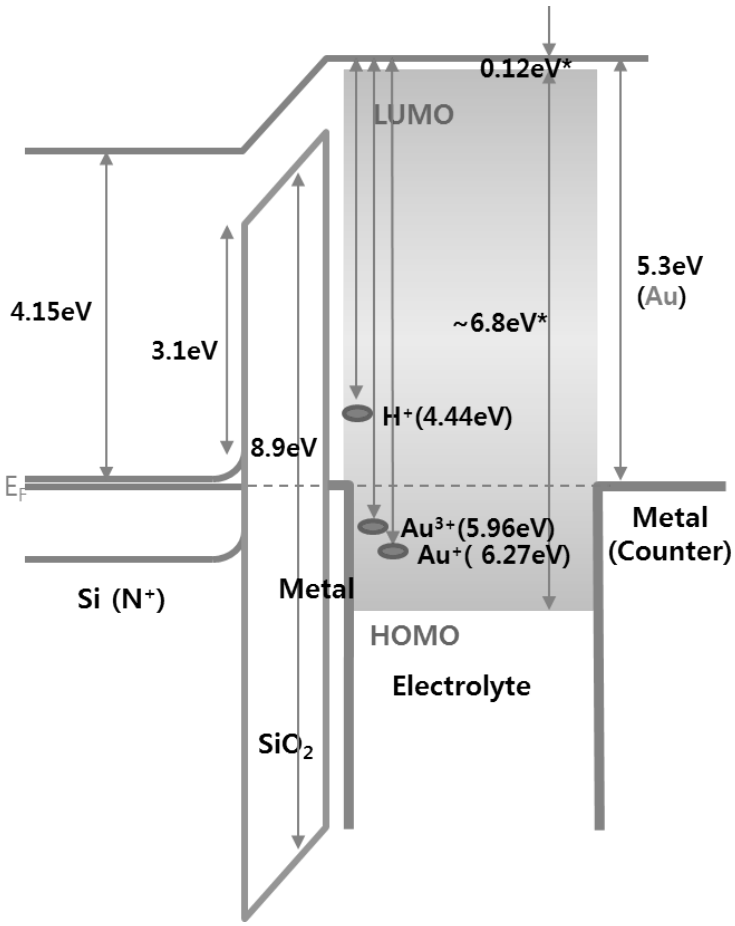


Fig. 3-13. Energy band diagram of given EMOS system ($V_{counter}$=0V, $V_{substrate}$=0V)

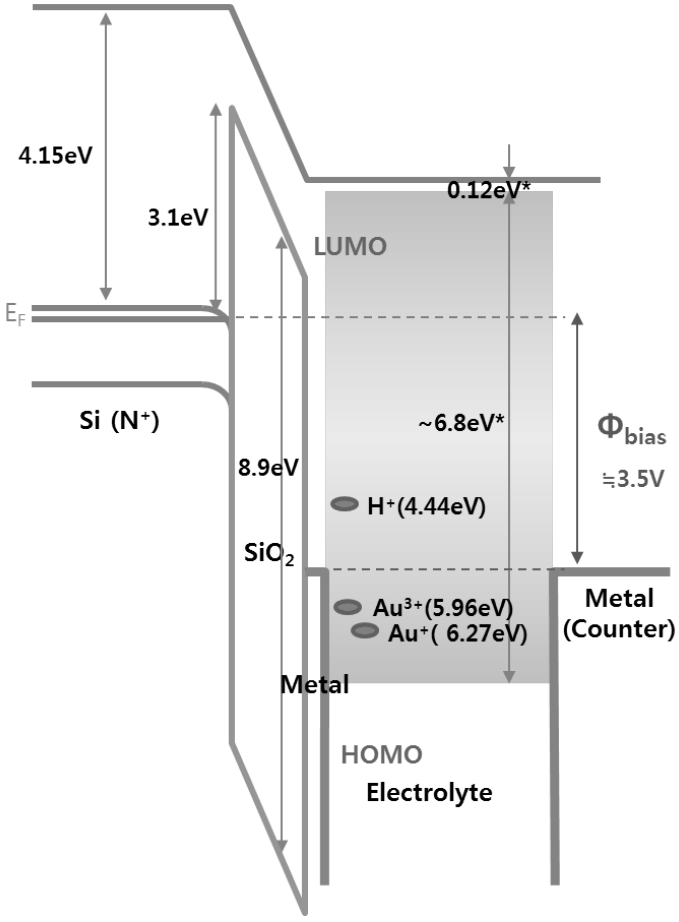
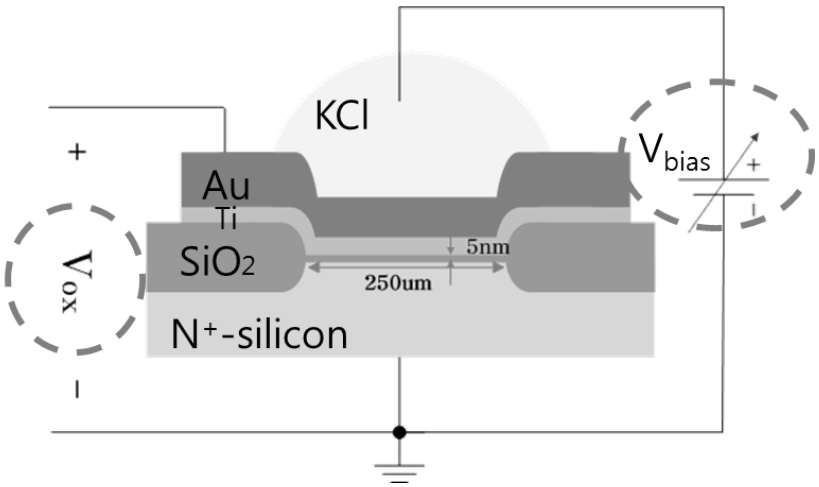
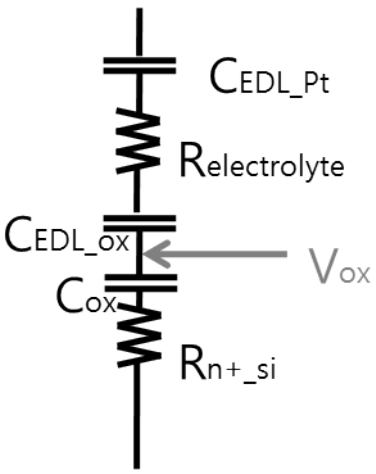


Fig. 3-14. Energy band diagram of given EMOS system ($V_{counter}$=3.5V, $V_{substrate}$=0V)

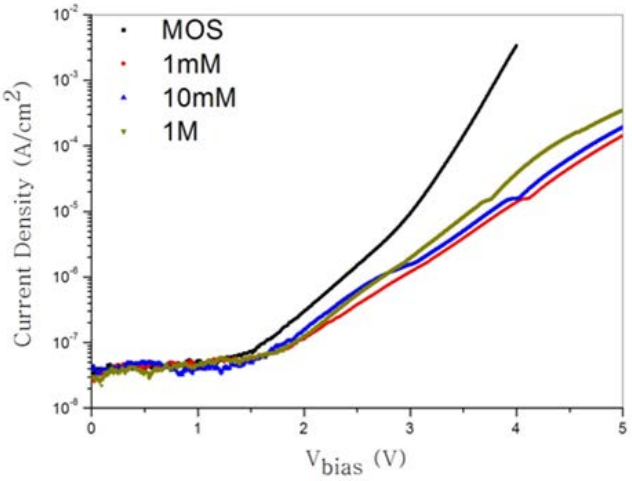


(a)

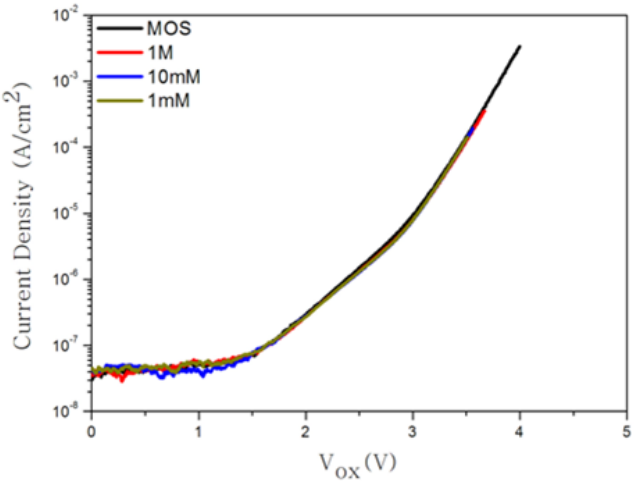


(b)

Fig. 3-15. (a) Schematic diagram of EMOS system using KCl electrolyte and Pt top electrode and (b) equivalent circuit of that (V_{ox} is monitored by Voltage Monitor Unit (VMU) of Agilent 4156C) [32]



(a)



(b)

Fig. 3-16. Current density-Voltage characteristics with (a) V_{bias} and (b) V_{ox} of EMOS system [32]

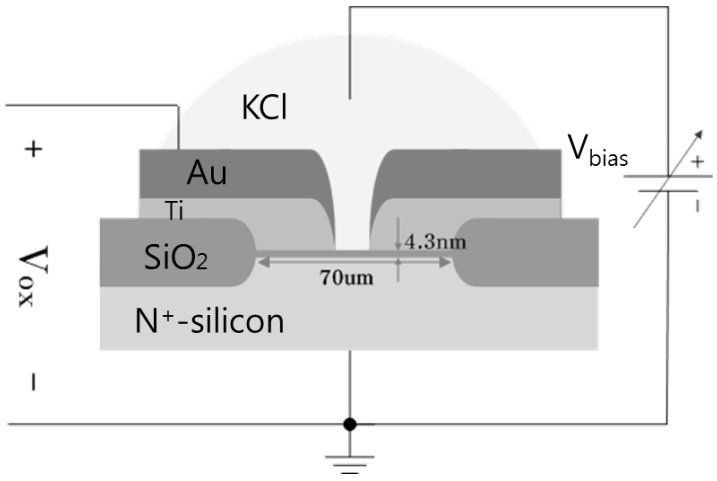
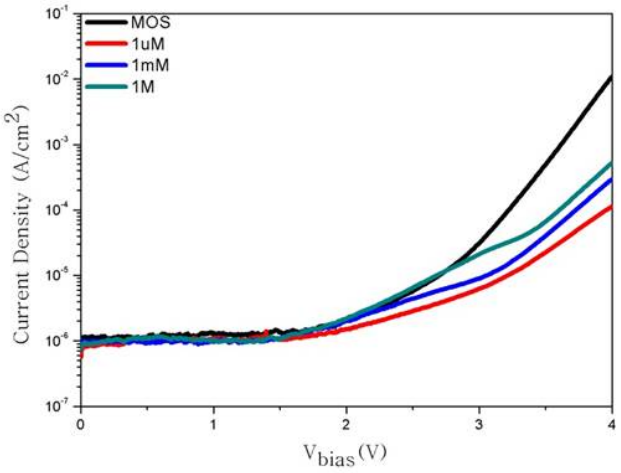
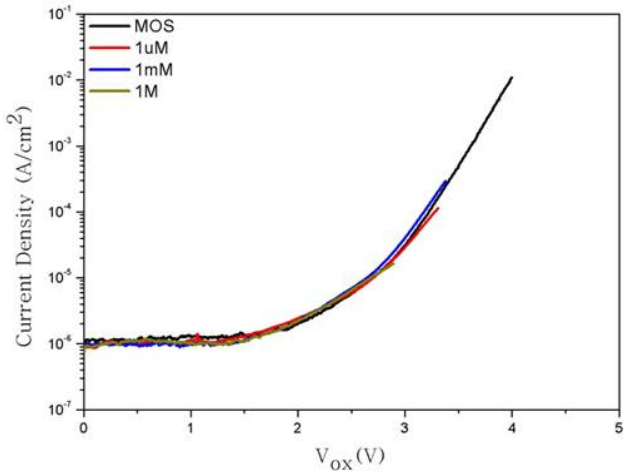


Fig. 3-17. (a) Schematic diagram of mixed EOS and EMOS system using KCl electrolyte and Pt top electrode (V_{ox} is monitored by Voltage Monitor Unit (VMU) of Agilent 4156C) [32]



(a)



(b)

Fig. 3-18. Current density-Voltage characteristics with (a) V_{bias} and (b) V_{ox} of mixed EOS and EMOS system [32]

3.3 Electrolyte-Oxide-Silicon (EOS) system

It is explained earlier that the tunneling current magnitude in EOS system is limited by the voltage across the oxide layer. Now, in the EOS system as the most basic environment for metal channel fabrication, we will look into the mechanism in which the accumulated metal particles on the upper oxide gradually transform the EOS system into the EMOS system.

3.3.1 Tunneling current of Electrolyte-Oxide-Silicon system

Fig. 3-19 is the schematic diagram of the test pattern to investigate the EOS tunneling current. Active area is a mesa type array pattern that has 400 unit cells of 3 $\times 3um^2$ each. 4000Å thick field oxide between actives is made by LOCOS process, and the active is 60Å thick. Small amount of $HAuCl_4$ electrolyte is dropped on the pattern and the Au tip is immersed. Bias voltage is applied to the Au tip as the counter electrode and the substrate as the working electrode.

To determine the current-voltage characteristics of the EOS system, I swept the counter electrode voltage from 0V to 5V for several times and measured the tunneling current through the oxide film, as shown in Fig. 3-20. The experimental results show a considerable difference between the first application of the gate voltage (the first sweep) and the subsequent sweeps after the 1'st sweep. From the second $V_{counter}$ sweep, the tunneling current increased dramatically over entire range of the measurement voltage. After the first sweep, we found with the microscope that H_2 gas bubbles are generated on the active sites. In this case, the electrons tunneling through the oxide from the silicon substrate create hydrogen bubbles by

the reduction of H^+ ions on the SiO_2-electrolyte interface. The H_2 bubbles on the SiO_2 disturb the formation and the adhesion of Au particles to the surface during the metal electroplating process.

Once the current density increases due to the positive voltage, the current-voltage characteristics are maintained for subsequent sweeps. This can be explained as follows: when the positive voltage is applied to the counter electrode, H^+ ions are located at the interface of SiO_2 and the electrolyte enter into the oxide layer. It is known that H^+ ions in the oxide can move freely in oxide via a hopping process [47]. The mobile H^+ ions enhance the electric field of the oxide by the Poisson effect, resulting in further increase in the tunneling current shown in Fig. 3-20.

We speculate that the enhanced oxide tunneling current after the positive electrode sweep generates a massive H_2 bubble at the oxide/electrolyte interface. For this reason, $V_{counter}$ sweep of degraded oxide should be prevented to ensure the quality of the electroplating process.

Another notable point that can be seen in Fig. 3-20 is that the first sweep current is similar to the Fowler-Nordheim tunneling current in Fig. 1-6 and the second weep current is similar to the direct tunneling current in Fig. 1-6. As described in the earlier sections, the tunneling current is the EOS system is proportional to the electric field in the oxide, regardless of the electrolyte chemical composition. That is, when H^+ ions penetrate into the oxide in the first sweep, the electric field in the oxide increases, which in turn reduces the effective oxide thickness, and therefore we can observe the current-voltage relation like direct tunneling current from the

second sweep and beyond, which would normally appear in cases of thinner oxide layers. This phenomenon will be revisited later on in the thesis work in connection with band diagrams.

3.3.2 Hydrogen relaxation

In this section, an electroplating stabilization technique is presented, which achieves quality recovery of the degraded oxide film by extraction of H^+ ions that penetrate into the oxide in large amounts.

To recover the degraded oxide (red circle of Fig. 3-21), I applied 'refresh' voltage with negative bias (a $V_{counter}$ sweep from 0V to -4V) and measured the tunneling current in the counter electrode from 0V to 5V, as shown in Fig. 3-21. The current level after the negative bias of the gate is recovered to the original level (the blue triangle of Fig. 3-21), which infers that the trapped H^+ ions in the oxide are extracted to the electrolyte by the negative voltage in the counter electrode. When the counter electrode voltage is swept from 0V to 5V in succession, the same process of oxide degradation by H^+ penetration occurs (the green inverted triangle of Fig. 3-21).

From the above observation, I propose cycling the positive (stress phase) and negative (refresh phase) biases alternately during the electroplating process to prevent leakage current due to penetrated H^+ ions in the oxide. During the positive bias sweep (the stress phase), Au metal nanoparticles are formed in a reduction reaction with the tunneled electrons at the surface of the SiO_2/electrolyte. During the negative bias sweep (the refresh phase), the H^+ ions are extracted from the oxide

layer into the electrolyte.

3.3.3 Transition to Electrolyte-Metal-Oxide-Silicon system

After more than one hundred repetitions of the voltage cycle like Fig. 3-22 (a), the current-voltage characteristics of the EOS system were obtained, as shown in Fig. 3-22 (b). Unlike the current characteristics of the initial status (the black square in Fig. 3-21), the tunneling current settles down to a smooth curve. This infers that the thin metal layer has been formed successfully during the positive bias on the counter electrode and the reduction reaction of H^+ ion at the SiO_2/electrolyte interface is removed. Once the metal layer is formed at the interface, any additional migration of H^+ into the oxide is effectively blocked. Therefore, the tunneling current of the EOS system after the metal layer is formed shows stabilized characteristics even after subsequent application of positive voltage.

For the sake of comparing the measurement result with the tunneling current of conventional structures, we prepared both a Metal-Oxide-Silicon (MOS) device and an EMOS device, as shown in Fig. 3-23 (a) (b), respectively. Each device has a 200nm-thick metal layer on the oxide fabricated by the e-gun evaporation process. For the EMOS device, the device is immersed in the same solution used to form the tunneling electroplating explained in the previous EOS system. The current-voltage characteristics of the conventional MOS and EMOS devices are also shown Fig. 3-24 (a).

In the MOS device, the gate tunneling current is caused by the direct tunneling

current at a low voltage and by the Fowler Nordheim tunneling current at high bias voltage (see the black square in Fig. 3-24(a)). The EMOS device shows characteristics similar to those of the MOS device (see the red circle in Fig. 3-24 (a)). However, the current-voltage characteristics of the EOS system formed by the tunneling electroplating process show a significant increase in the current, or a shift toward the negative voltage by about 1.5V. This result is similar to the Stress-Induced Leakage Current (SILC) found in the conventional MOS structure in Fig. 3-24 (b).[48-50] Therefore, I conclude that the penetrating H^+ ions are responsible for the oxide degradation during the tunneling electroplating process.

The formation of the metal layer is confirmed by the AFM image shown in Fig. 3-25. Before the tunneling electroplating process, a relatively flat surface can be observed, as shown in Fig. 3-25 (a). After this process, the roughness of the surface increases significantly, as shown in Fig. 3-25 (b), from which it may be concluded that the metal particles layer is successfully fabricated on the oxide surface.

Also, to verify that the layer formed on the surface is indeed a metal layer, the sample is surface-treated with sulfur and fluorescent material attached DNA (Deoxyribonucleic acid), and it is observed with fluorescent microscope, as in Fig. 3-26 (a). Fig. 3-26 (b) and (c) represent the results before and after electroplating, respectively, and the metal adhesion on the surface can be confirmed by appearance of multiple bright spots on the surface after electroplating.

3.3.4 Band diagram of Electrolyte-Oxide-Silicon system

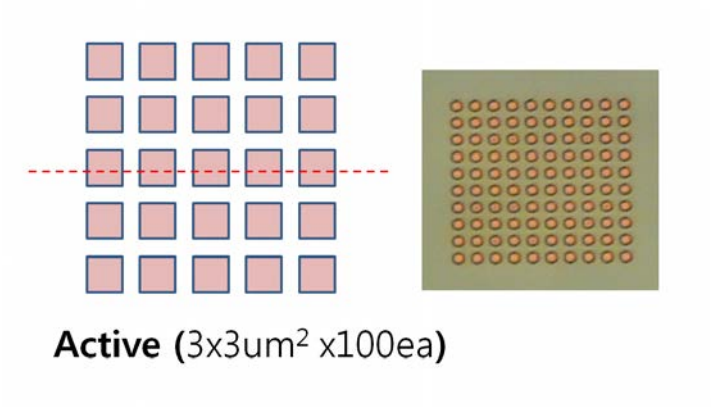
In this section, the band diagram is used for better understanding of the current density increase phenomenon in the EOS electroplating process.

Fig 3-27 shows the change in the current density recovered according to the refresh voltage in the hydrogen relaxation experiment in the section 3.3.2. The current density changes a lot in the bias voltage of 3.6V after the -0.5V negative stress, but if the negative stress voltage is pushed up to –5.0V, the bias voltage necessary to cause noticeable current density change gets gradually larger. This implies that hydrogen ions form trap sites inside the oxide, and that their energy levels are widely distributed. It is due to the variability of bonds between silicon atoms and hydrogen ions penetrating into the oxide. [51]

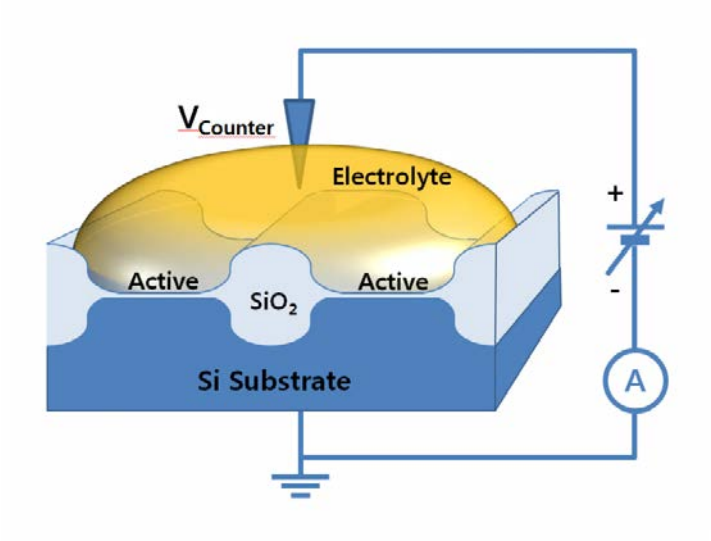
Fig. 3-28 is a band diagram of $HAuCl_4$ electrolyte EOS system at zero voltage difference. This is generally very similar to the EMOS system in Fig. 3-13 except the metal layer between the oxide and the electrolyte. Fig. 3-29 is a band diagram of the EOS system with fresh oxide under the 3.5V voltage bias that is often used in the experiments for the Fowler-Nordheim tunneling. Tunneling electrons from silicon through oxide film are involved in direct reduction reaction with Au^{+}, Au^{3+} ions or H^{+} ions in the electrolyte because most electric field is applied across the oxide. Therefore, hydrogen gas generation in EOS system is inevitable. Only viable measure to reduce the hydrogen gas production is to lower the hydrogen ion concentration in the electrolyte. Solutions with pH higher than 6 are used in the EOS system experiments for low hydrogen concentration.

Now, the band diagram is used for the analysis of the rapid increase of the current density due to repeated measurements and the recovered current density with the help of refresh voltage. Fig. 3-30 (a)~(e) show energy band diagrams with stress induced leakage current models in general MOS systems.[52-57] Considering trap generation by hydrogen ion penetration, it can be said that field enhancement due to trapped positive charges in (a) and trap assisted elastic tunneling in (b) and trap assisted tunneling accompanied by a large energy loss in (d) are all involved in the oxide tunneling current in EOS systems. Fig. 3-31 (a)~(c) are band diagrams corresponding to current density curve of 'fresh', 'after stress' and 'after refresh' in Fig. 3-21, respectively. In (a), hydrogen ions penetrating into wide range energy levels enhance oxide electric field gradually, a large field enhancement due to trapped positive charges oxide modeling.[58-60] Once the enhancement proceeds sufficiently, the oxide thickness as a tunneling barrier gets smaller and smaller (Fig. 3-31 (b)), which results in radical increase in tunneling current. By applying negative bias in this situation, hydrogen ions inside oxide are emitted to electrolyte (Fig. 3-31 (c)), resulting in restoration of the oxide electric field, and the measured current becomes similar to the "after refresh" first measurement value.

With this correct modeling of the EOS system, it now becomes possible to present proper conditions in the metal channel formation experiments such as 'Low counter bias for decrease H_2 generation', 'Maintain stable concentration of H^+ ions in electrolyte', 'Repeat negative stress between electroplating process' and 'Treatment for the adhesion enhancement of Au particles'.



(a)



(b)

Fig. 3-19. (a) Illustration of the active area and a photomicrograph of LOCOS-processed silicon and (b) schematic diagram showing the EOS system when the tunneling electroplating process is used in an electrolytic solution of $HAuCl_4$.

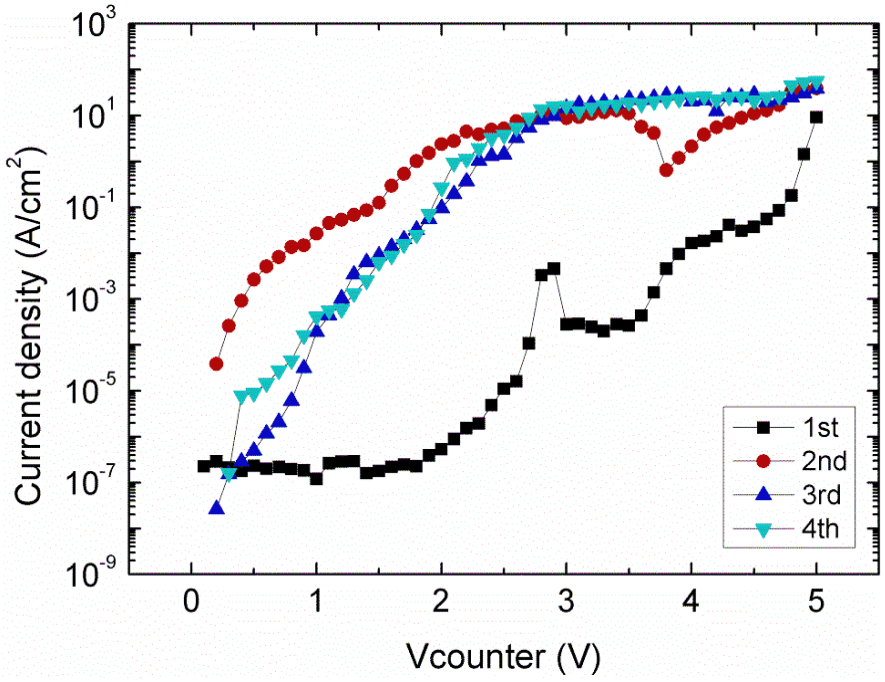


Fig. 3-20. Current density versus the counter electrode voltage measuring tunneling current several times through the oxide film in the EOS system

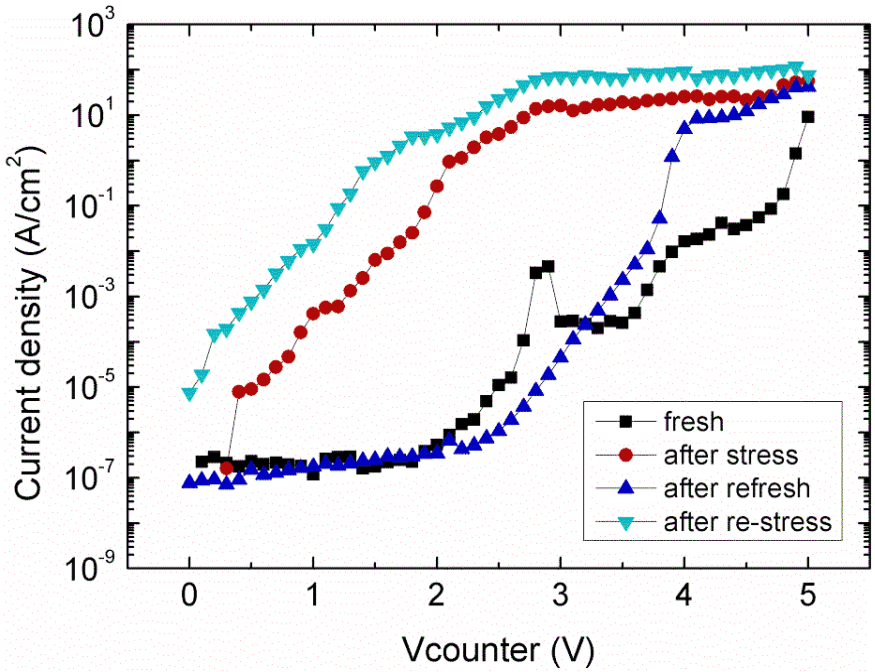
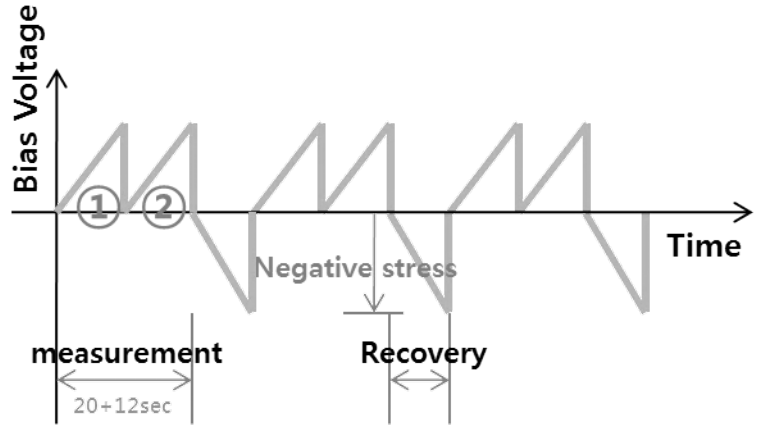
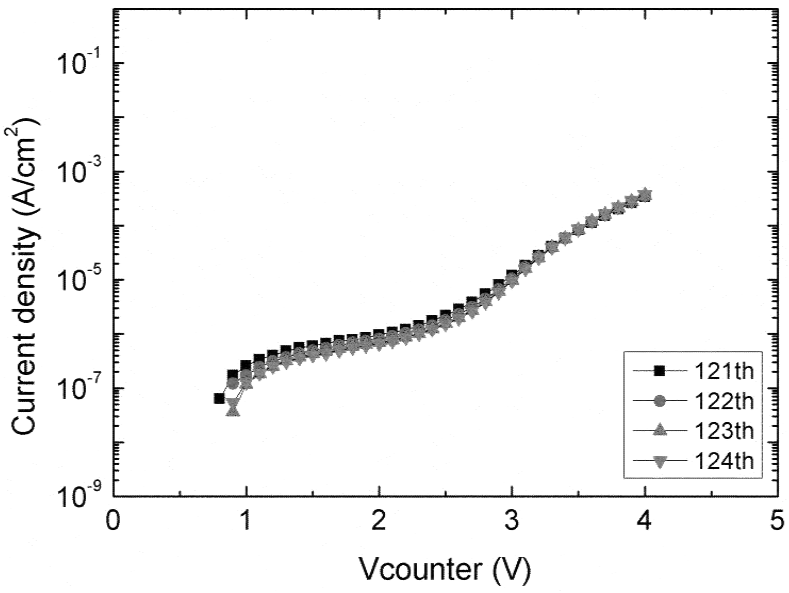


Fig. 3-21. Current density versus the counter electrode voltage measuring the tunneling current after the application stress voltage with a positive bias (red arrow) and refresh voltage with a negative bias (blue arrow).

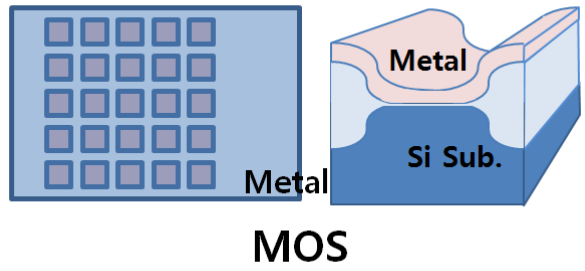


(a)

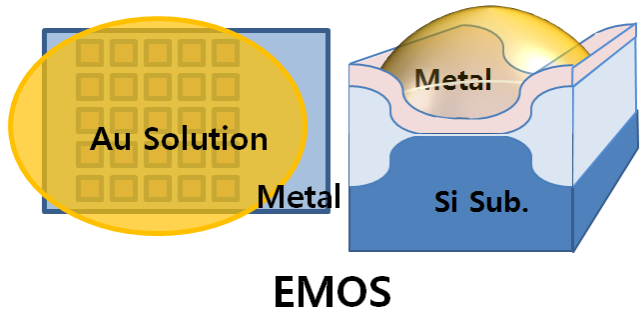


(b)

Fig. 3-22. (a) The voltage cycle diagram for the hydrogen ion relaxation and (b) Current density versus the counter electrode voltage measuring after more than one hundred repetitions of the voltage cycle

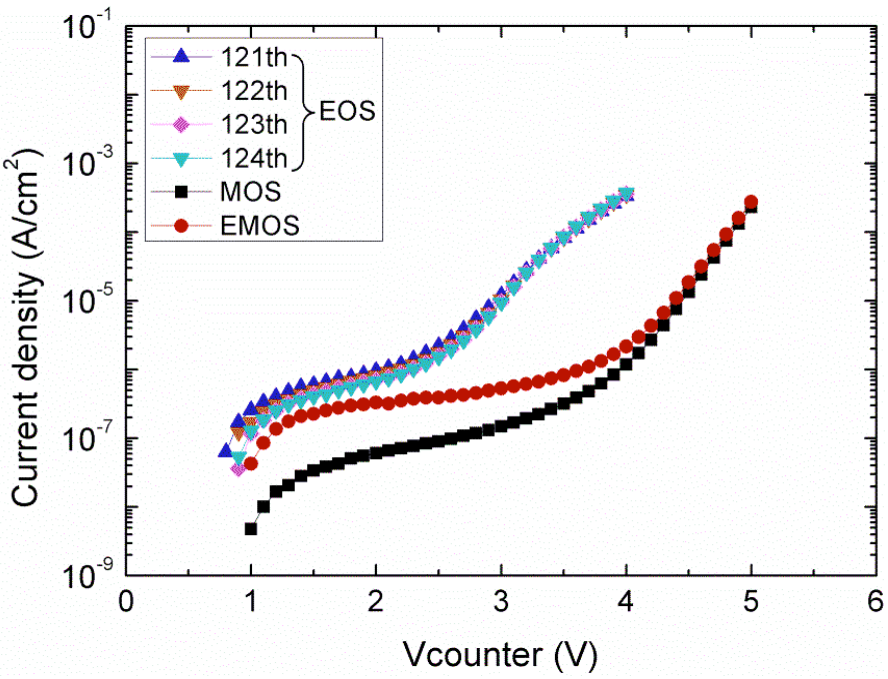


(a)

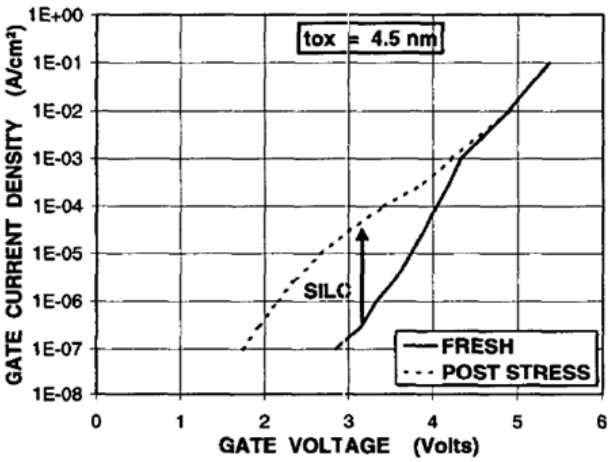


(b)

Fig. 3-23. (a) Schematic showing the MOS and (b) EMOS structure with a thick metal layer processed by e-gun evaporation on the oxide.

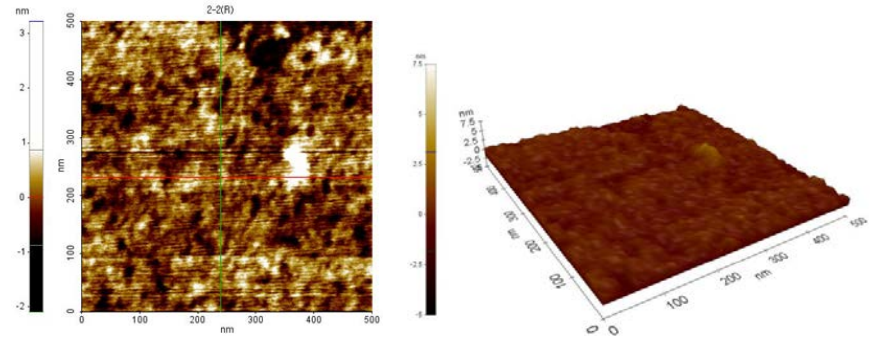


(a)

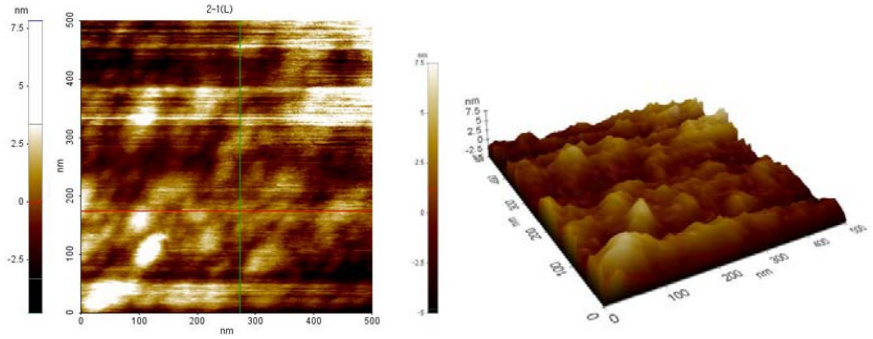


(b)

Fig. 3-24. (a) Current density versus the counter electrode voltage measuring the tunneling current of the EOS system after repetition of the tunneling electroplating cycle (numbers refer to the count of the cycle performed) (b) Stress-Induced Leakage Current (SILC) found in the conventional MOS structure [48]

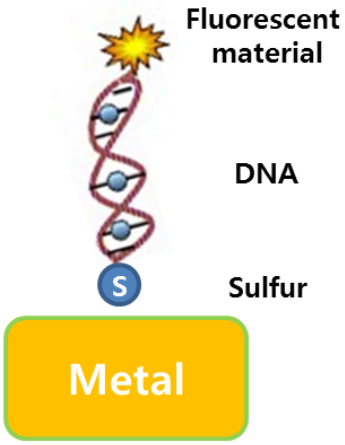


(a)

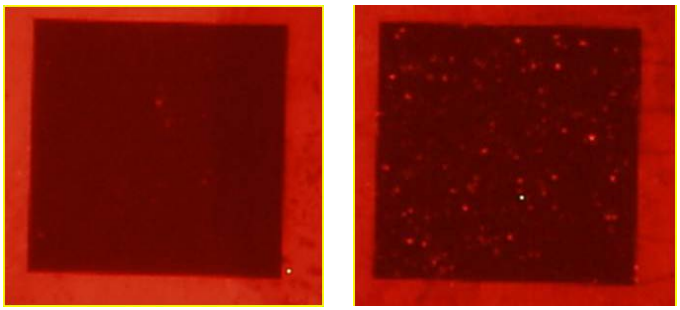


(b)

Fig. 3-25. AFM images of the oxide surface topology in this experiment: (a) before a tunneling electroplating cycle and (b) after a tunneling electroplating cycle



(a)



(b) (c)

Fig. 3-26. (a) Surface treatment by DNA wire with the sulfur and the fluorescent material and the fluorescent microscopic images of the oxide surface in this experiment: (b) before a tunneling electroplating cycle and (c) after a tunneling electroplating cycle

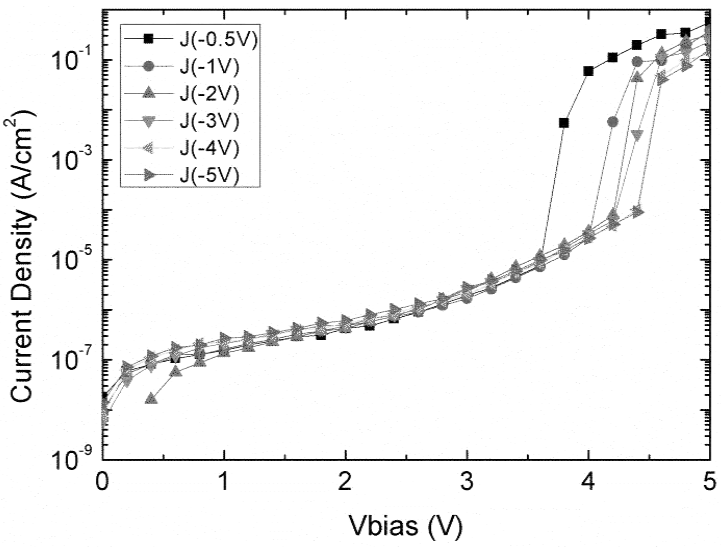


Fig. 3-27. Current density versus the counter electrode voltage measuring the tunneling current of the EOS system with various negative voltages split

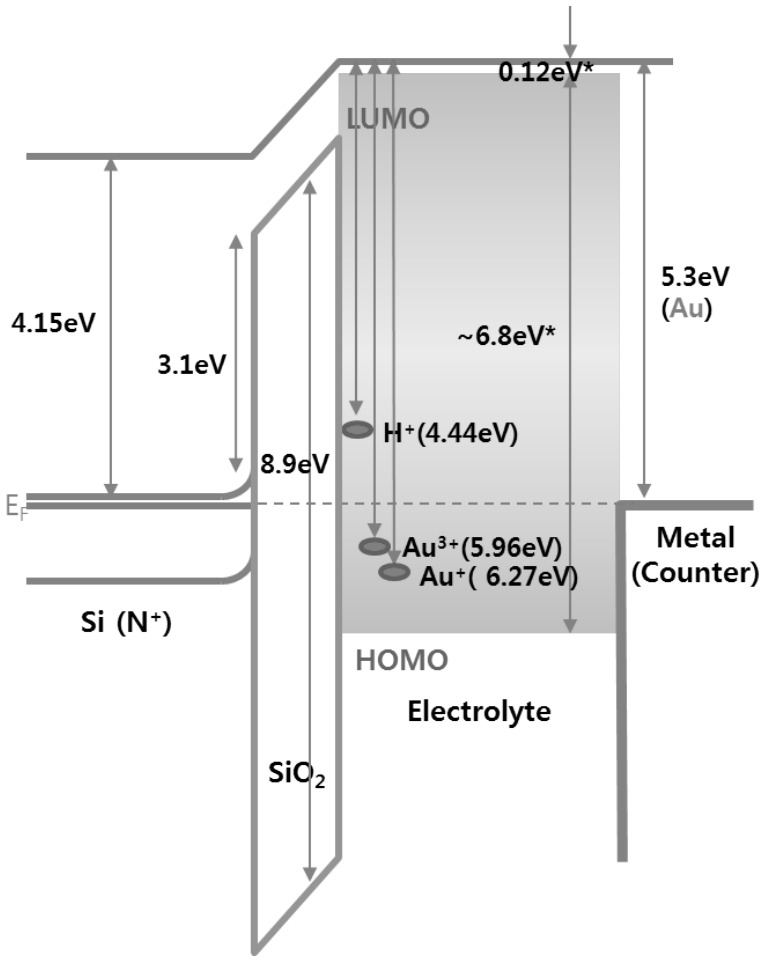


Fig. 3-28. Energy band diagram of given EOS system ($V_{counter}$=0V, $V_{substrate}$=0V)

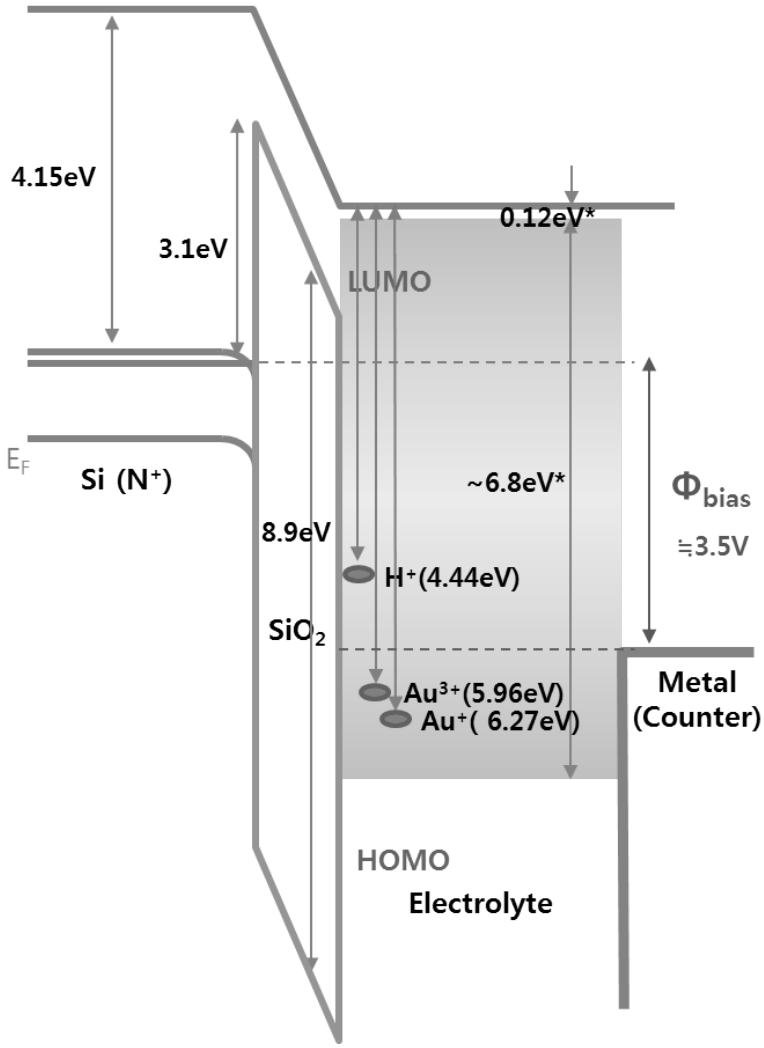


Fig. 3-29. Energy band diagram of given EOS system ($V_{counter}$=0V, $V_{substrate}$=3.5V)

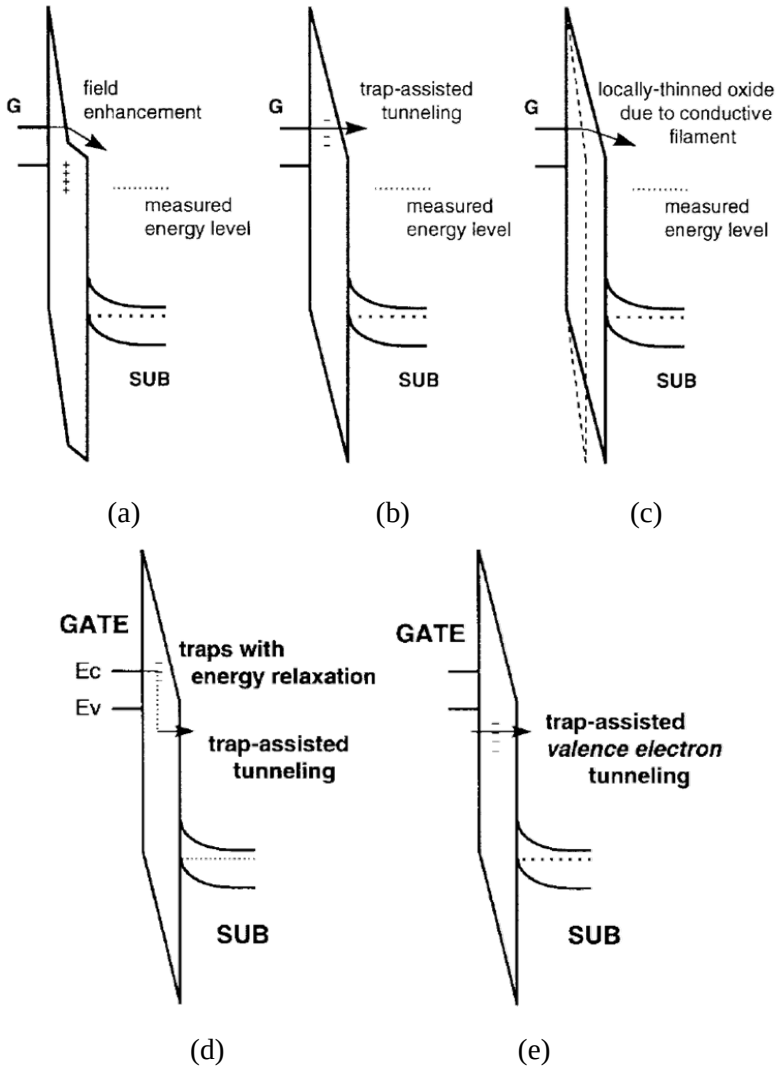
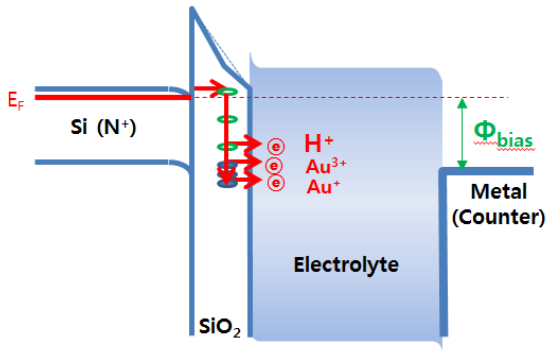
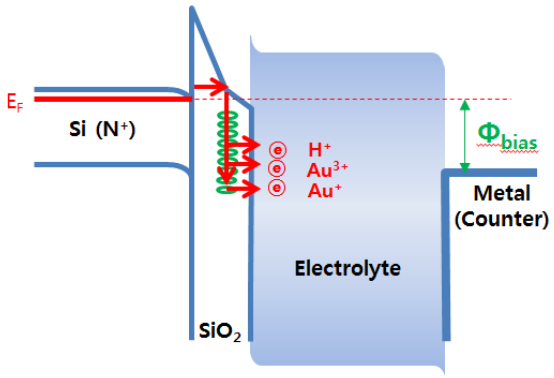


Fig. 3-30. SILC(Stress Induced Leakage Current) modeling (a) Field enhancement due to trapped positive charges (b) Trap-assisted elastic tunneling (c) Local thinning of the gate oxide due to a conductive filament (d) Trap-assisted tunneling accompanied by a large energy loss (e) Trap-assisted tunneling of valence electrons [52]



(a)



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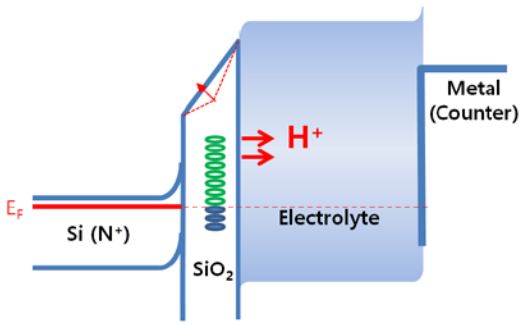


(c)

Fig. 3-31. Energy band diagram of given EOS system of (a) ʹfresh’ condition, (b) ‘after stress’ condition and (c) ‘within refresh’ condition

Chapter 4

Formation of metal channel device

In this chapter, it will be presented an optimized process conditions for the metal particle integration with the oxide and the effective metal channel construction in previously refined EOS systems. Close monitoring result of the electroplating process is also presented, and electrical characterization of the fabricated metal channel devices is provided in efforts to assess possibilities of various device applications.

4.1 Channel narrowing and surface treatment

The test pattern in Fig. 2-2 for the metal channel fabrication has the source and the drain pattern space of at least 2um on the oxide, unlike the EOS system case. In fact, this 2um spacing is quite a long distance in perspective of 1.4Å size gold atom, and the minimization of this distance is in order. In this thesis work, the channel narrowing by source/drain electrode electroplating is for that purpose. As in Fig. 4-1

(a), pH 1.1 $HAuCl_4$ electrolyte is dropped on the test pattern and the Au tip is immersed. Lower pH of the electrolyte renders smaller surface roughness.[32] To suppress hydrogen gas generation, 0V bias is applied to the source, 0.01V to the drain, and less than 0.5V to the Au tip. To prevent the leakage onto the substrate, 0V is applied to the silicon substrate. Fig. 4-1 (b) and (c) show SEM images of before and after channel narrowing. The test pattern with 2um spacing in Fig. 4-1 (b) now gets to have less than 0.5um spacing (in Fig. 4-1 (c)) after the channel narrowing process. This thesis work adopts two measures to minimize opened active area by most effective narrowing process. One is that the narrowing process is terminated just before the source and the drain electrodes are shorted each other, and the other one is that the narrowing is done up to the electrode shortage and then the source and the drain are opened with the fuse effect by electro migration.

Hydrogen gas generated at the surface during the tunneling electroplating hinders gold metal particle adhesion to the surface. On top of that, gold surface energy(~1400ergs/cm^2) is higher than gold/silicon dioxide interphase boundary free energy(390±90 ergs/cm2)[61-66], which makes gold favor atomic cluster form rather than adhesion to the oxide surface.[67-69] Therefore a certain surface treatment is advantageous to attach gold particles on the oxide surface. APTES (3-Aminopropyltriethoxysilane: Fig. 4-2 (a)) is used in this experiment, SiO_3 is attached to the oxide at one end, and amino group (NH_2) is attached to a metal particle at the other, so that it can help adhesion of generated gold particles. [70-71] Fig. 4-2 (b) shows a SEM view of APTES surface treated oxide with 10~100nm size

Au particles adhered. Au nano particles attached to NH_2 gather and make connections of Au atoms generated in reduction reactions during the electroplating process, help the surface adhesion, and contribute to the channel formation.

4.2 Formation of metal channel with self-limitation

Electrode biases are set up as in Fig. 4-3 on the prepared test pattern, and the experiments are carried out accordingly. pH9 electrolyte with $KAuCl_4$ are used to lower hydrogen ion concentration, and the gold wire tip is immersed to maintain original Au ion concentration in the electrolyte.

Recording and analysis of current variation through each electrolyte are very informative because the current during the metal channel formation process transparently reflects the tunneling electroplating mechanism and 'self-limitation' phenomena. Fig. 4-4 is the four electrode current monitoring result during the channel formation by tunneling electroplating. As the tunneling electroplating process duration time exceeds 1050sec, the source and the drain are electrically connected and each current undergoes dramatic change either positive and negative direction, at which point all electrode biases are removed. The graph shows that the currents through the electrolyte and the source gradually decrease, while the drain and the substrate currents reveal no change.

Fig. 4-5 (a) is a vertical and horizontal schematic that describes the current reduction effect through the electrolyte. A lot of gold particles are generated on the oxide surface during the tunneling electroplating process. A portion of produced

metal particles form island clusters on the oxide, and another portion are connected to the source electrode. Electrons that enter the metal islands after the oxide tunneling are again emitted to the electrolyte to expand Au island covered area on the oxide by helping Au^+ ions reduce to solid Au atoms on the island surface. The metal layer connected to the source electrode has obviously the same potential with the source, and tunneling electrons infused from the substrate escape through the source electrode with reduction reaction.(Red line of Fig. 4-5 (a)) The source electrode area keeps growing during the metal channel formation process because of electrical connection to the expanding metal islands with Au particles generated on the oxide through electroplating process, and naturally the total active area keeps shrinking, which facilitates reduction reaction in the electrolyte. Consequently, the electrolyte tunneling current decreases during the metal channel formation due to this area shrinking.

In this process, gold particles generated by reduction reaction do not adhere to the drain periphery (Red line of Fig. 4-5 (b)), which is because the voltages of the tip immersed in the electrolyte and the drain electrode are set equalized. Because of the EDL form on the oxide surface, some potential drop happens by the depletion of electrolyte. Therefore, the oxide surface near the drain electrode assumes smaller potential than that of the drain, causing some oxidation reaction in very small scale. However, total drain current shows almost no change because its contribution on the oxide surface is negligible compared to total drain electrode thickness.

During the electroplating, the source electrode is biased lower by 0.05~0.1V for

source/drain current monitoring purpose, the source current is more negative than the electrolyte current. (Tunneling current value is positive.) The total source current becomes negative because the total exposed electrode area is relatively bigger compared to the active contact area, and also because the tunneling current has lower order of magnitude than faraday current. Unlike the drain, the source electrode attracts metal particles easily due to low electrode potential, and its area becomes larger and larger (Red line of Fig. 4-5 (c)), which causes tunneling current toward the source electrode to increase, and the absolute value of the total source current seem to decrease.

The substrate current value does not change because total tunneling area stays the same (Red line of Fig. 4-5 (d)) even if the metal particles keep accumulating on the channel area during the electroplating. The channel area expands as the electroplating progresses, and the source and the drain current dramatically increase as the generated metal atoms are eventually connected to the drain electrode (Red line of Fig. 4-5 (e)).

Fig. 4-6 is the current change in the condition that the electroplating is let continue even after the source and the drain is connected by the metal channel. Increased current in the previous example upon source/drain connection now reduces rapidly, which is because the percolation style [72] metal channel between the source and the drain sometimes re-opens with the cluster migration and then shorts again with the help of additional generation of metal particles. The devices manufactured this way show quite unstable characteristics, but sometimes it

becomes functional just by washing out surface electrolyte remains.

Fig. 4-7 shows SEM views of the devices with or without metal channel formation. It can be confirmed that a lot of metal particles are congregated on the oxide surface near the source as in (b).

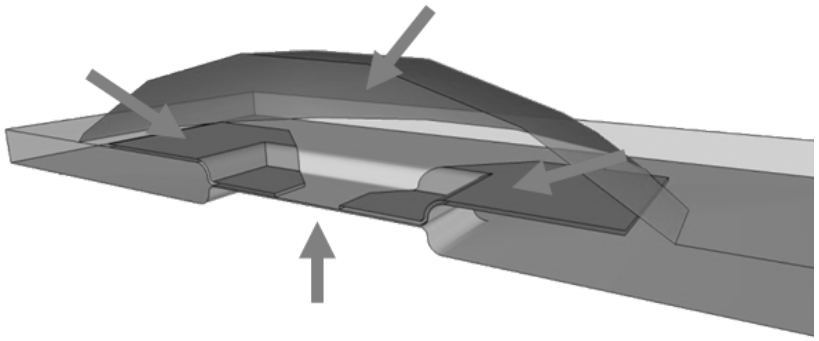
4.3 Characteristics of metal channel device

In this section, electrical characteristics of metal channel devices are to be analyzed. The device has 50Å active oxide, and the biases during the tunneling electroplating are 3V at the electrolyte, 2.71V at the drain, 2.7V at the source and 0V at the substrate. The metal channel is connected in 40 seconds, at which point the tunneling electroplating is terminated. (Fig. 4-8) Fig. 4-9 (a) and (b) are I_D-V_D and I_D-V_G characteristics in the 3-terminal structure as shown in Fig. 1-4 (a). The measurement took place after washing the remaining surface electrolyte upon process completion. In Fig. 4-9 (a), the drain voltage is swept from 0V up to 0.05V, source is fixed at 0V, and the back gate (substrate) voltage is at 1V step from -2V to 2V. In Fig. 4-9 (b), the source and the drain voltages are fixed at 0V and 0.05V, respectively, and back substrate voltage is swept from -1V to 1V. It can be verified that the drain current gradually reduces as the back gate voltage increases, and Fig 1-4 (a) and (b) are well matched in this respect. Rather than widely formed metal channel property, this current reduction seems to be the result of Au particle characteristics, which is connected in percolation form and seems to channel

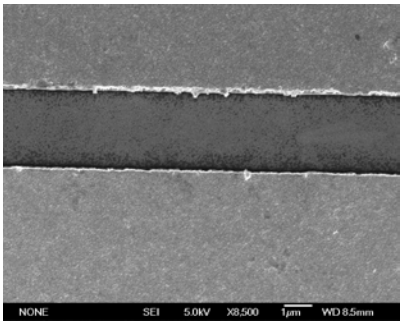
mobility reduction with increasing back gate voltage.

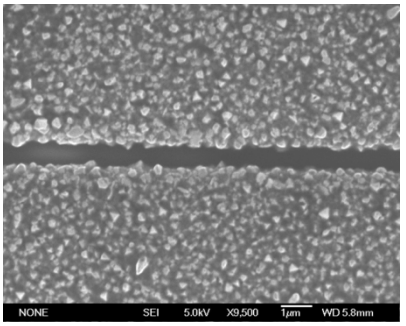
Fig. 4-10 (a) and (b) are output and input characteristics in a 4-terminal structure as in Fig. 1-4 (b). 0.1M pH6 Potassium Phosphate (KH_2PO_4 + K_2HPO_4) is used as the front gate buffer solution. I_D-V_D in Fig. 4-10 (a) is same with Fig. 4-9, only the experiments are split according to front buffer gate voltage instead of back gate, and the substrate is biased at 0V. Front gate voltage increase causes the wide variation of the current characteristics, which is because the Au atoms in percolation connection react inside buffer solution. Subsequent I_D-V_G characteristics measurement does not show the variation as in Fig. 4-19.

Metal channel devices connected in percolation form are easily damaged with the probing voltage, which requires low measurement voltage, and since the characteristics vary rather sensitively with the surface condition, stable characteristics are likely to be obtained in inert gas or vacuum environment.



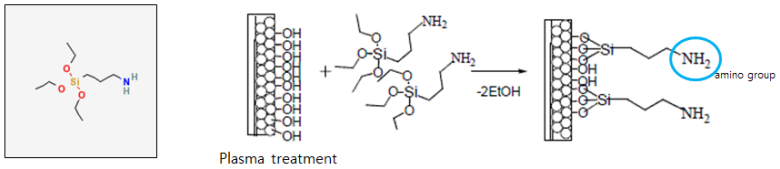
(a)



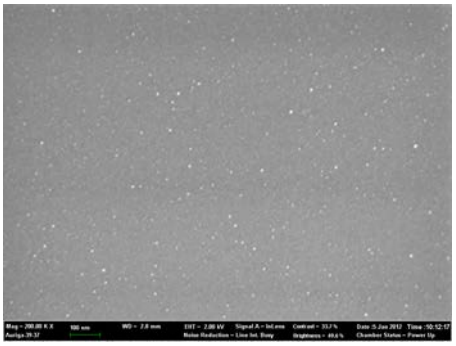


(b) (c)

Fig. 4-1. (a) Schematic diagram of bias condition for channel narrowing and SEM view of (b) before channel narrowing and (c) after channel narrowing using $HAuCl_4$ solution of pH1.1



(a)



(b)

Fig. 4-2. (a) Schematic view of APTES surface treatment and (b) SEM view of Au nanoparticle (~100nm) on oxide surface after APTES treatment

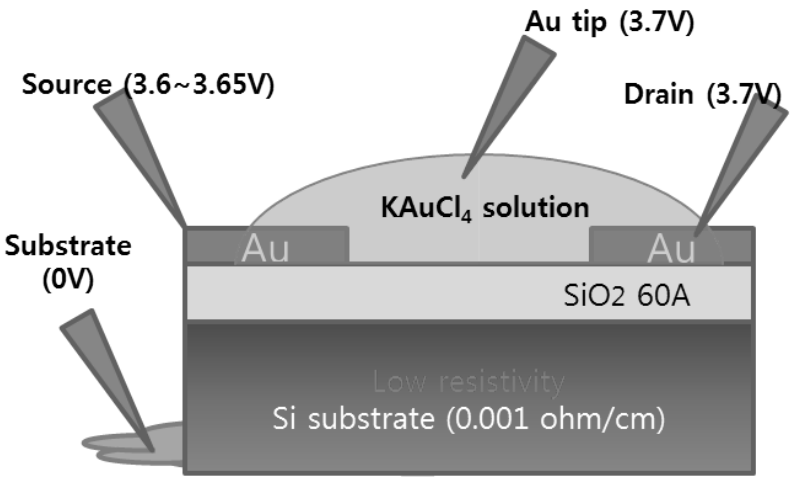


Fig. 4-3. Schematic diagram showing the metal channel formation process when the tunneling electroplating process is used in an electrolytic solution of $HAuCl_4$.

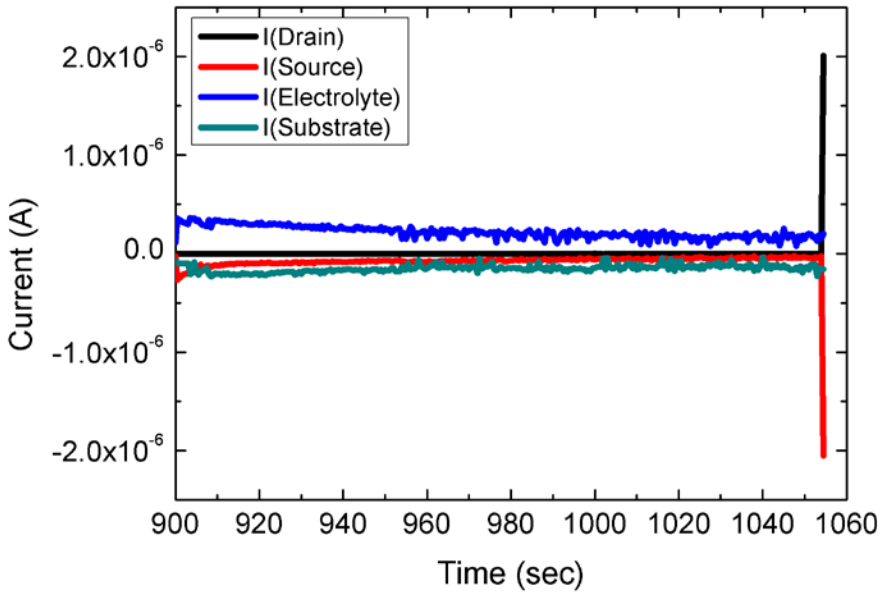
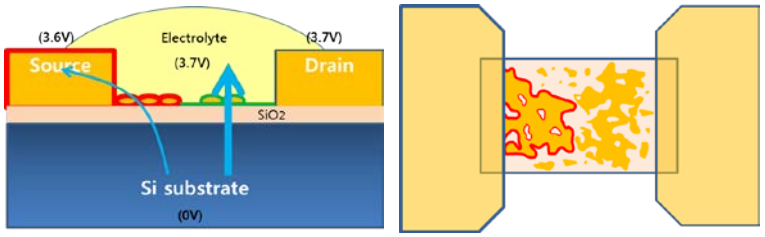
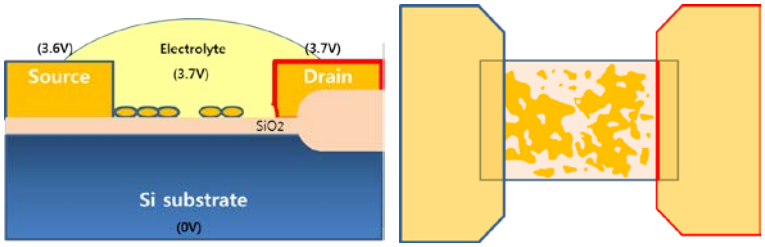


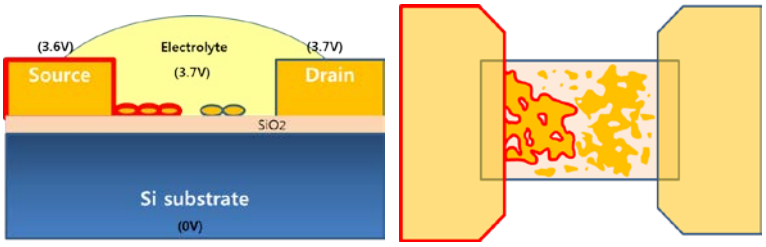
Fig. 4-4. Current vs. time characteristics during the metal channel formation process


(3.6V)
Electrolyte
(3.7V)
(3.7V)
Source
Drain
SiO2
Si substrate
(0V)

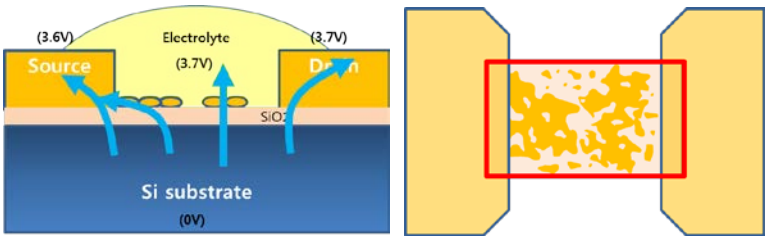
(a)


(3.6V)
Electrolyte
(3.7V)
(3.7V)
Source
Drain
SiO2
Si substrate
(0V)

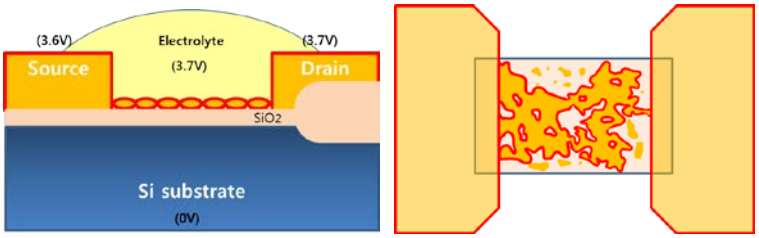
(b)


(3.6V)
Electrolyte
(3.7V)
(3.7V)
Source
Drain
SiO2
Si substrate
(0V)

(c)

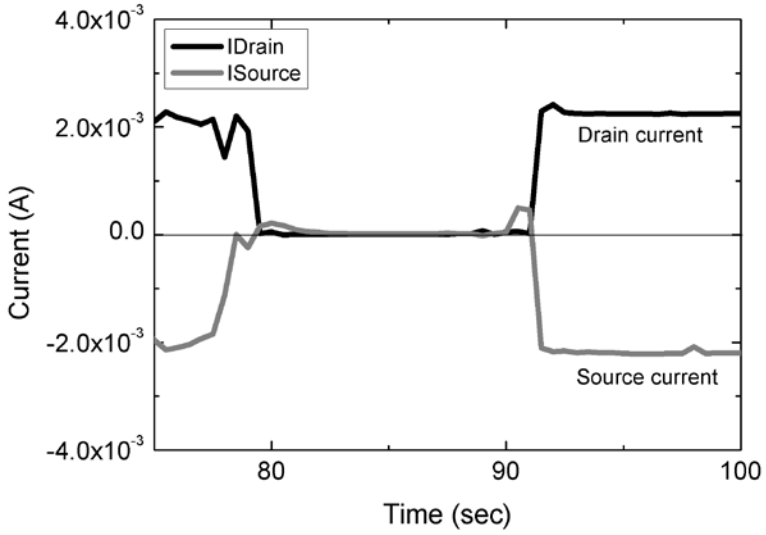


(d)



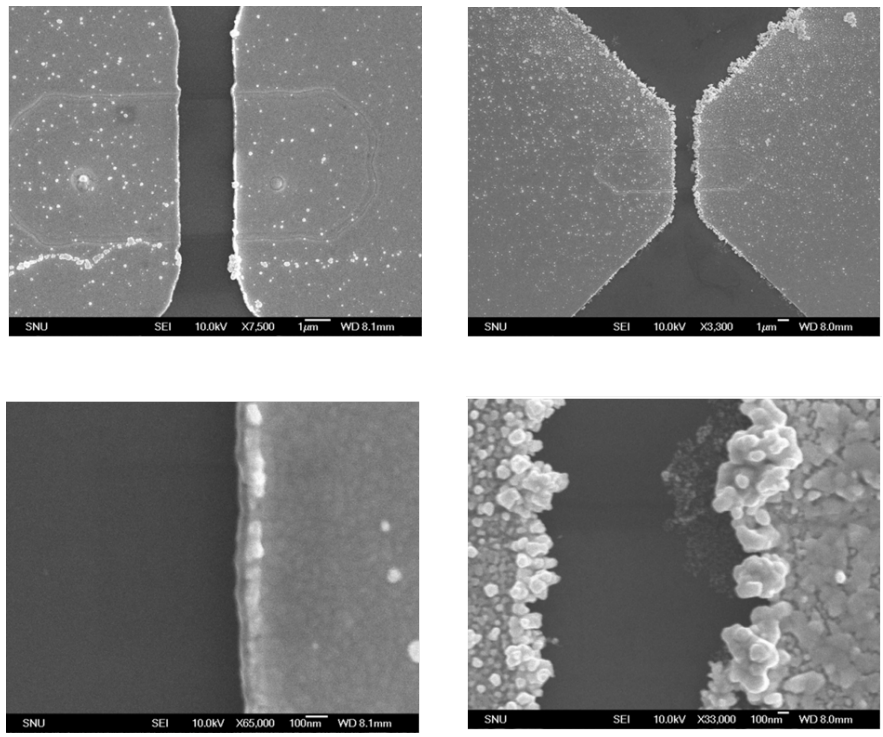
(e)

Fig. 4-5. Schematic view for explanation of self-limitation method during the metal channel formation process using (a) electrolyte current, (b) drain current and (c) source current, (d) substrate current, (e) percolation theory



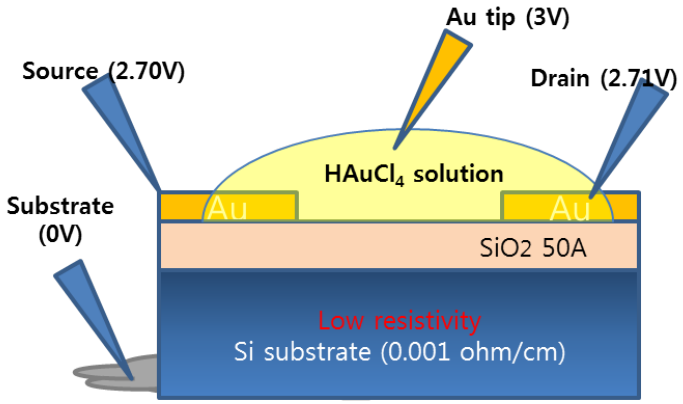
(a)

Fig. 4-6. Current vs. time characteristics after the connection of metal channel between source and drain

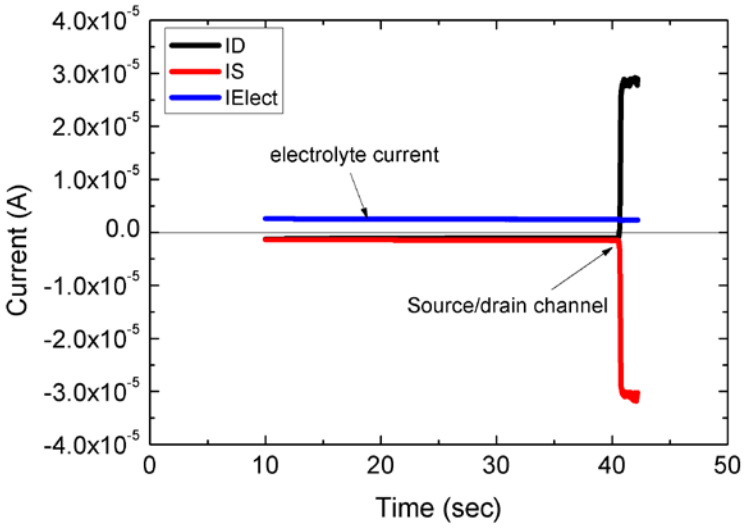


(a) (b)

Fig. 4-7 SEM view of test pattern of (a) fresh sample and (b) metal channel formation processed sample

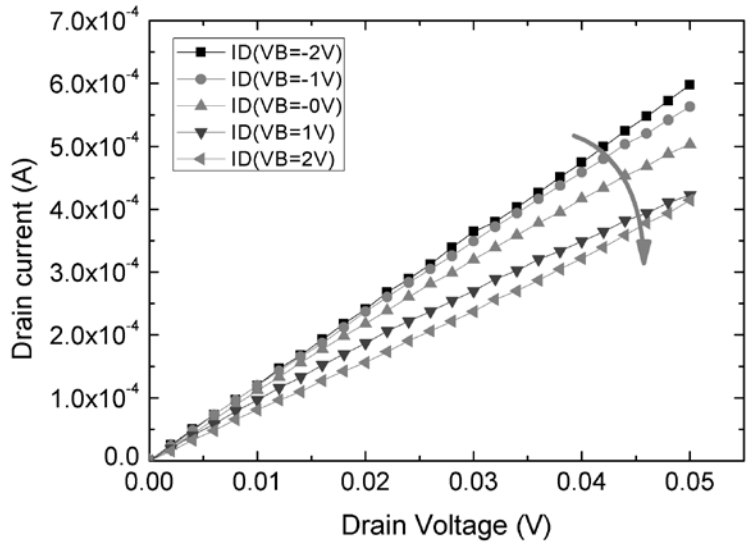


(a)

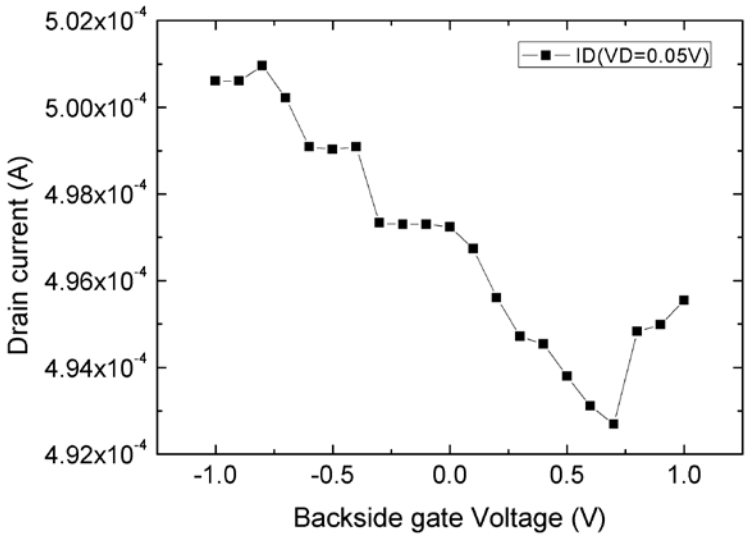


(b)

Fig. 4-8 (a) Schematic view of the metal channel formation process and (b) current vs. time characteristics during the process

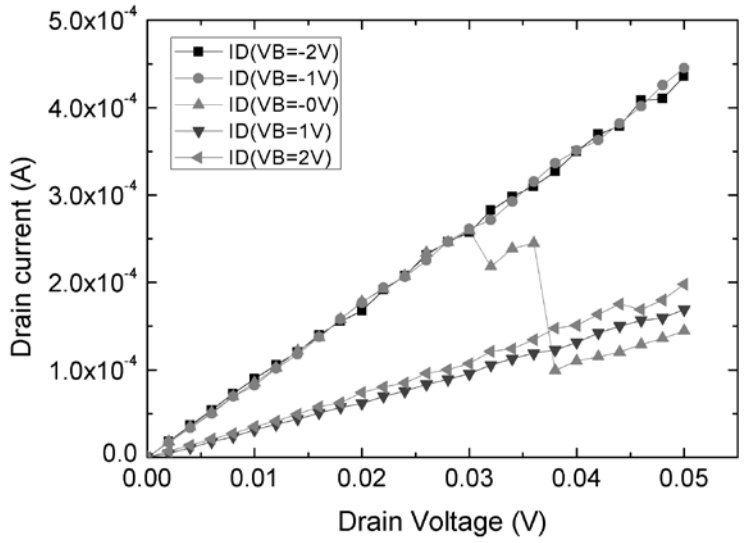


(a)

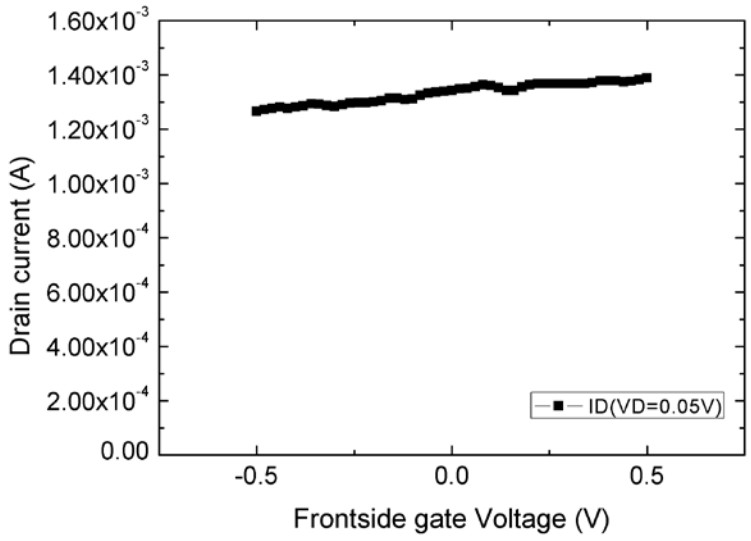


(b)

Fig. 4-9 (a) I_D-V_D characteristics and (b) I_D-V_G characteristics of the 3-terminal metal channel device (using backside gate bias)



(a)



(b)

Fig. 4-10 (a) I_D-V_D characteristics and (b) I_D-V_G characteristics of the 4-terminal metal channel device (using buffer solution for front side gate bias)

Chapter 5

Conclusions

5.1 Summary

In this thesis, by controlling the tunneling current through the insulator layer, it has been developed a technique that effectively forms metal nano-particles (or film) on the insulator layer of the EOS system. This method is referred to as ‘tunneling electroplating’. Typically, conductive films on the surface of SiO_2 are deposited by physical methods such as the sputter deposition process or chemical methods using chemical vapor deposition (CVD). Because metal film deposited on SiO_2 does not adhere to the surface very well and forms lumps due to the difference in the surface energy levels, it is difficult to create a uniform nano-sized metal layer on a SiO_2 surface. However, it has been shown in this thesis work that the tunneling electroplating process using a ‘self-limitation’ method can deposit an extremely thin metal layer, even on a non-planar active area such as the trench structure or FinFET

structure.

Energy levels of hydrogen ions and gold ions in the MEM system were studied and, correlation with the reduction reaction has been made using band diagram

The proposed tunneling electroplating approach has been applied to a conventional EOS device. It has been found that the degradation is caused by the H+ ion penetration under the positive bias for the electroplating condition. By applying the specific voltage cycle, it has been shown that the degraded oxide is largely cured under the negative bias condition. From the measurements, the EOS device is converted to an Electrolyte-Metal-Oxide-Silicon (EMOS) device, which means that Au nanoparticles are successfully formed on the tunneling oxide. Moreover, also it has been reported that the thin conductive film on the surface of the EOS system protects the oxide film against the penetration of the H+ ions, thereby stabilizing the resultant EMOS system.

With the help of the information obtained during MEM and EOS system experiments, metal channel devices were fabricated through tunneling electroplating, the self-limitation effect model was produced in the process, and the metal channel devices were electrically characterized.

The proposed technique can selectively deposit an extremely thin metal layer on active sites with a self-alignment feature. Moreover, it can be readily used for the fabrication of various devices with a metal layer as the sensor channel for bio- or photo-sensor applications.

5.2 Future works

Tunneling electroplating generates metal particles on an oxide surface due to the large amount of electrons that tunnel through the oxide. The large Fowler-Nordheim tunneling current causes leakage due to oxide stress, which affects the reliability of the oxide film adversely. Commercialization of metal channel devices would require a clear understanding of the relationship between the device oxide lifetime and the electrons that tunnel through the oxide during the manufacturing process, as well as rigorous research on hydrogen extraction inside the oxide and using nanogap pattern to reduce the total tunneling charge during tunneling electroplating. [73-83]

Further, nanometer size metal particles can serve as very good surface plasmon resonance (SPR) sources. Metal channel device contains numerous nanosized metal particles, and their optical resonance or SPR enhance effects will be relevant research topics. [84-85]

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한글 초록

반도체 공정이 미세화함에 따라 소자를 구동하는 실리콘의 집적도는 이미 한계에 도달하고 있다. 보다 나은 특성을 위하여 III-V 족 재료나 탄소나노튜브, 그래핀등의 새로운 소재를 사용한 소자의 개발이 계속하여 진행되고 있으며, 특히 단원자 또는 단원자층으로 구성되는 박막을 만들어 이를 전계효과 트랜지스터의 채널로 이용하려는 연구가 지속되고 있다.

본 논문에서는 메탈 채널을 이용하는 소자의 구조와 동작 및 제작에 대한 방법을 신규 제안한다. 또한 관련한 공정 프로세스를 구성하고, 테스트 패턴을 제작하였으며, 일련의 과정에서 터널링 도금법이라는 새로운 공정을 만들어 실험 테이블 위에서 나노미터 두께의 금속막을 절연체 위에 구성하는 신규 공정을 개발하였다.

메탈 채널 소자를 효율적으로 제작하기 위해 기본 구조인 금속-전해질-금속 구조에 대하여 분석을 하고, 이를 환원 전위와 비교하여 밴드다이어그램에 이온의 에너지 준위를 적정하게 위치하여 도금을 전기적으로 이해하였다. 아울러 절연막 위에 나노미터 두께의 금속막을 만들기 위한 실험으로서 전해질-산화막-실리콘 구조와 전해질-메탈-산화막-실리콘 구조의 소자를 제작하고, 이에 흐르는 전류를 분석하여

전해질을 통해 산화막을 터널링 하여 흐르는 전류는 산화막의 양단에 걸리는 전위에 의해 제한되는 것을 알았다. 또한 전해질-산화막-실리콘 구조에서 반복된 측정에 의한 전류의 급격한 증가는 산화막 내에 침투하는 수소이온의 영향으로 인한 유효 산화막 두께의 감소임을 이해하였고, 수소이온의 주기적으로 방출하는 산화막 회복 방법을 제안하여, 절연막의 파괴 없이 효과적으로 산화막의 표면에 나노미터 두께의 금속막을 구성할 수 있음을 확인하였다.

터널링 도금을 진행하는 동안 절연막 상부에서 발생하는 금속 입자의 산화막 흡착을 돕기 위하여, 표면에 SAM (Self Assembled Monolayer) 처리하는 방법으로서 APTES (3-Aminopropyltriethoxysilane)를 도포하고 도금을 진행하여 도금막 형성 공정을 완성하였다.

또한 터널링 도금 공정 중에 테스트 패턴을 통해 흐르는 전해질, 소스, 드레인, 기판 전류를 분석하여, 자기 제한법에 의해 산화막 위에 형성되는 금속 입자의 두께가 증가하지 않도록 하는 금속막의 형성과정과 최종 채널의 연결에 대하여 설명하였다.

제안된 터널링 도금 방법을 이용하여 채널 등의 용도로 사용될 수 있는 금속막을 전계 트랜지스터의 형태로 제작할 경우, 상온에서 쉽게 제작할 수 있고 CMOS 공정과 호환이 가능하고, 기 제작된 소자의 상부에 추가 공정을 통해 집적이 가능하므로 쉽게 대량 생산이 가능하다. 이는 향후 전개될 수나노미터급 트랜지스터나 금속을 이용한 센서의 제작을 통해

다양한 응용 소자로 이용할 수 있다.

주요어 : 터널링, 일렉트로플레이팅, 도금, 채널, MOSFET, MOS, EOS, EMOS

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