Ph. D. DISSERTATION

Analysis of Reliability Issues and Lifetime Estimation in NAND Flash Memory

낸드 플래시 메모리에서의 신뢰성 분석 및
새로운 수명 평가 방법 연구

BY

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DEPARTMENT OF ELECTRICAL ENGINEERING
AND COMPUTER SCIENCE
COLLEGE OF ENGINEERING
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ABSTRACT

Analysis of Reliability Issues and Lifetime Estimation in NAND Flash Memory

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As NAND flash memory continues to be aggressively scaled down, it becomes more susceptible to reliability problems. As a result, the lifetime estimation of the device is now serious topic for mass production. However, the apparent activation energy (E_{aa}) in the conventional temperature-accelerated lifetime test method of NAND flash memory does not follow the Arrhenius model, since various failure mechanisms occur concurrently. Therefore, this conventional Arrhenius model has a huge error in the lifetime prediction. Generally well-known dominant failure mechanisms in NAND flash memory are detrapping, interface trap (N_{it}) recovery, and trap-assisted tunneling (TAT).

In this thesis, we propose an advanced charge loss model and completely separate three dominant failure mechanisms in terms of the time-constant (τ) and the final ΔV_{th} in

various generations (A, B, C) of NAND flash test element group (TEG) cells and sub 20-nm multi-level cell (MLC) NAND flash memory main-chip. As a result, it is observed that each τ of the mechanisms follows the Arrhenius law well, which means that each has its own activation energy (E_a). In addition, we deeply investigate the retention characteristics of the dominant mechanisms in various conditions, such as the number of P/E cycling times, probability level of the V_{th} cumulative distribution, and states in sub 20-nm MLC NAND flash memory. We also extracte the contribution rate (CR) of each failure mechanisms at criterion of $|\Delta V_{th\_Total}|$ according to baking temperature. The results give the physical reason for abnormal retention behaviors such as E_{aa} roll-off at the PV3 and negative E_{aa} at the ERS. P/E cycling stress generates traps in the tunnel oxide layer. We extract the trap profile in the tunnel oxide in space and energy distributions using 3D TCAD simulation.

For the first time, we reveal the origin of abnormal E_{aa} characteristics and derive a mathematical formula for E_{aa} as a function of each $E_{a(\text{mechanism})}$ in NAND flash memory. We propose two different accurate lifetime estimation models for sub 20-nm NAND flash memory. The first model is the E_{aa} integration method. Using the analytically modeled E_{aa} equation, the lifetime of NAND flash memory is accurately predicted. The second model is the advanced extrapolation method using the trends of extracted parameters. Using the proposed model, accurate lifetime is estimated in all states (PV3, PV2, PV1, and ERS). Since the proposed model takes into account the retention characteristics for various mechanisms, this model provides much accurate prediction on the lifetime of NAND flash memory. Also, the lifetime

estimation for the next generation of NAND flash memory is analyzed using 3D TCAD simulation. As a result, the lifetime for the next generation is expected to decrease as much as 66 % of the lifetime for the current generation.

Keywords: MLC NAND flash memory, failure mechanisms, Arrhenius model, activation energy (E_a), P/E cycling stress, lifetime estimation

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Chapter 1

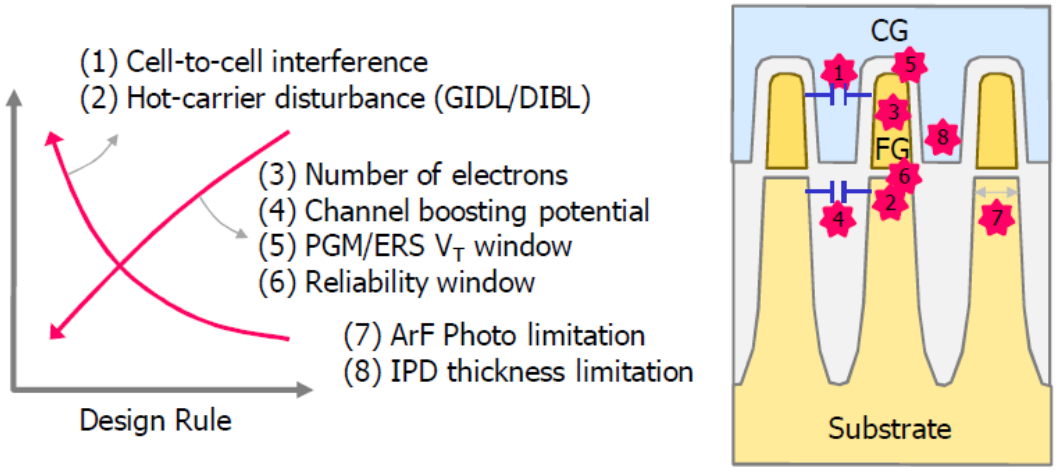
Introduction

1.1 Reliability Issues in NAND Flash Mempry

Recently, demand for non-volatile memory has explosively increased since digital applications such as smart phones, tablet PCs, and solid-state drives (SSDs) are continuously increasing in the market [1]-[3]. In order to meet the steadily increasing market demand, semiconductor based memories are commonly used and researchers are trying to scale down the size of the device [4]-[5]. NAND flash memory has been extensively adopted as the main storage device owing to its ultrahigh storage capacity and low cost. The critical success factors of NAND flash memory can be explained by the rapid reduction in the feature size of memory cells and multi-level cell (MLC) operation, which have led to low cost production with higher density. During the past decade, the integration density has doubled every year, thus outstripping Moore's law [6]. However, as the dimensions of NAND flash memory cells are reduces, most of the electrical properties have become worse.

Fig. 1.1 shows various scaling limitations and trends in NAND flash memory [7]. The

cell-to-cell interference [8]-[12] and the hot-carrier disturbance [13] have been increasing as the cells are scaling down continuously. However, the number of electrons in the storage layer [14], the channel boosting potential [5], PGM/ERS V_{th} window [15]-[16], and reliability window [17]-[19] are continuously decreasing. As the devices are scaled down, the impact of a single electron has a tremendous influence on the retention characteristics because the amplitude of ΔV_{th} due to a single electron increases. Furthermore, the photolithography process with an ArF source have already been a critical limitation and gives a great burden to the process cost for overcoming the limitation using a double patterning technology [20]-[22]. Finally, the thickness of IPD (Inter-Poly Dielectric) occupies a significant portion in the cell dimension because other dimensions have reached a comparable thickness with IPD [23]. MLC technology requires narrow threshold voltage distribution. Thanks to the incremental step pulse programming (ISPP) scheme for program operation, the V_{th} distribution has very narrow distribution. However, those various limitations make the intrinsic V_{th} distribution more broaden and influence the read operations, as shown in Fig. 1.2. These problems cause the V_{th} window margin between MLC states becomes decreasing. Therefore, the lifetime of the device becomes shorten dramatically with scaling down. Now, deliberate design and accurate lifetime estimation is essentially required on highly scaled NAND flash memory.



(a) (b)

Fig. 1.1. Scaling limitations and trends in NAND flash memory [7].

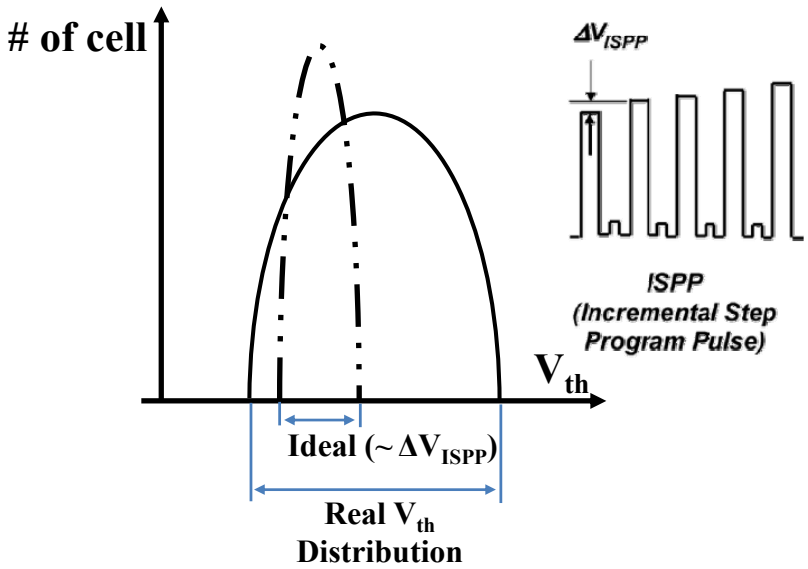
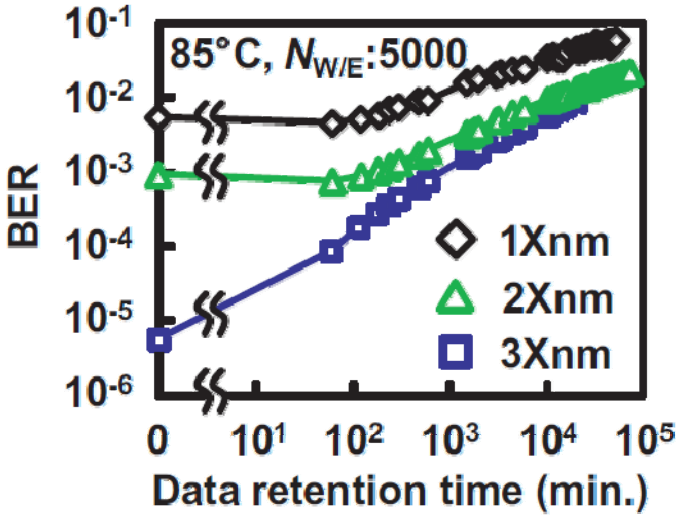


Fig. 1.2. Parasitic effects of scaling limitations on V_{th} distribution in NAND flash memory [8].

Fig. 1.3 show bit error rate (BER) according to data-retention time and block lifetime according to the number of cycling times with 1X-3X nm NAND flash memory at 85°C condition [19]. Block lifetime is defined as the data-retention time when all errors in a NAND block is correctable by error-correction code (ECC). The results show the scaling dependence with 1X to 3X nm NAND flash memories at 85°C condition. The reliability degradation by scaling is clearly observed. BER increases and block lifetime decreases as the device is scaled down. As a result, accurate lifetime estimation for highly scaled NAND flash memory is now getting serious and important topic for mass production.



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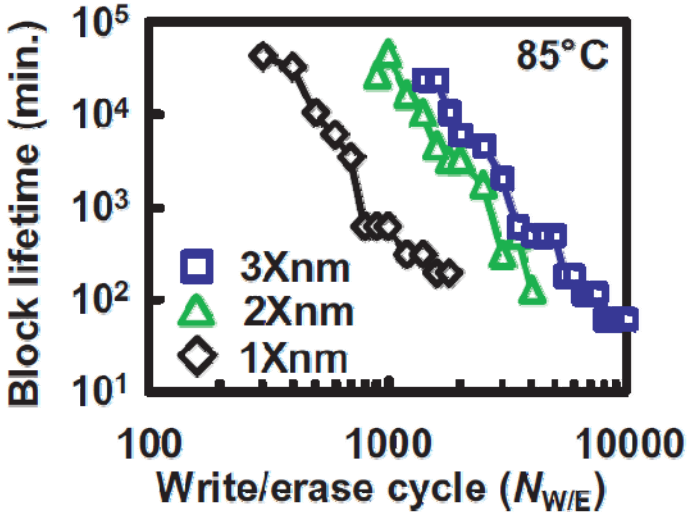


(b)

Fig. 1.3. (a) BER vs. data-retention time and (b) Block lifetime vs. the number of cycling times with 1X-3X nm NAND flash memory [19].

1.2 Review of Failure Mechanisms in NAND Flash Memory

In order to understand the abnormal retention characteristics in NAND flash memory, a good physical understanding of various failure mechanisms should be preceded. Reliability issue is mainly due to trap in tunneling oxide and/or interface of Si-SiO_2. There are various trap related failure mechanisms in NAND flash memory, as shown in Fig 1.4 [24]. Generally well known dominant failure mechanisms are the detrapping [25] -[27], the interface trap (N_{it}) recovery [28]-[31], and the trap-assisted tunneling (TAT) [32]-[35]. In this section, the dominant failure mechanisms are reviewed in detail.

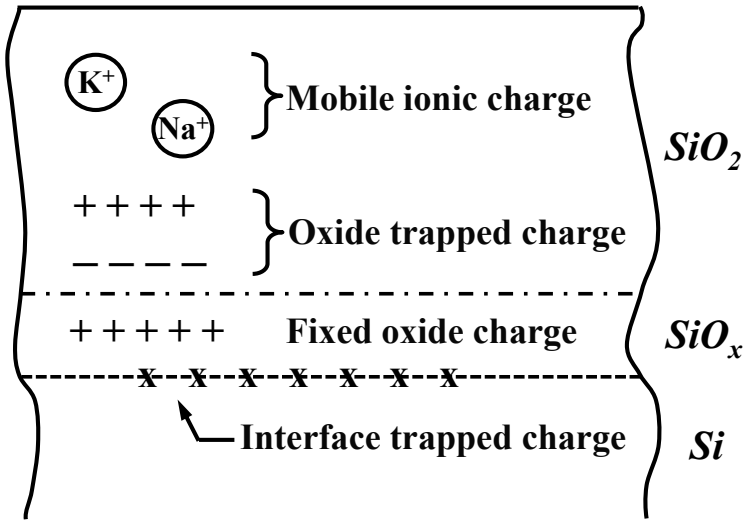
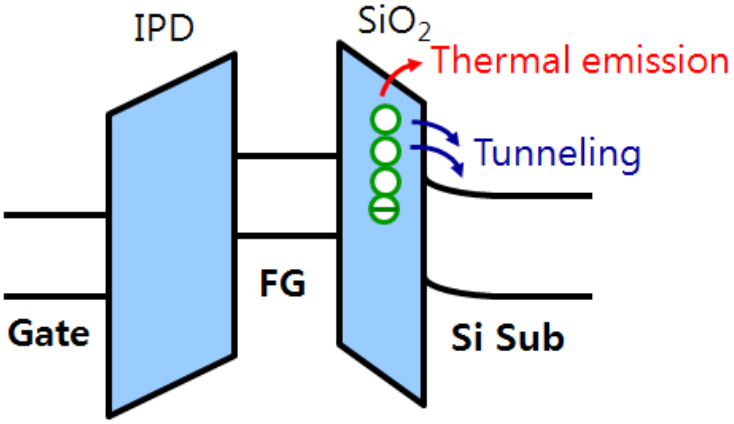


Fig. 1.4. Basic categorization of traps and charge in SiO2 and interface of Si-SiO_2 [24].

1.2.1 Detrapping Mechanism

Charge trapping in oxide layer can occur from program/erase (P/E) cycling stress-induced trap sites in NAND flash memory, causing V_{th} shift and string current reduction [25]-[26], [28]. Also, the trapped electron can be detrapped with thermal emission process and/or tunneling process from the tunnel oxide to substrate. The charge detrapping represents one of the most severe reliability issues for nanoscale NAND flash technologies, since a single charge trapped in the tunneling oxide can give even larger than 100 mV of V_{th} shift in sub 20-nm technology node [14]. In a high-temperature regime, trapped electrons in the oxide layer can be directly detrapped to the substrate with high thermal energy [25]-[26]. Therefore, this mechanism has greater temperature-dependence and a higher value of E_a. Generally, it is reported that the E_a value of the detrapping mechanism is around 1.0~1.2 eV [25], [27], [36]. Since the trapped carriers are unrelated to the percolation path, the carriers detrap generally without assistance of traps (one step process).

Fig. 1.5(a) shows a band diagram for explaining the detrapping mechanism in NAND flash memory [26]. In detrapping mechanism, both thermal emission with Poole-Frenkel model and tunneling from trap to substrate can be occurred at the same time [26], [37]. Fig. 1.5(b) shows the simulation results for the detrapping mechanism. For the traps close to the substrate, tunneling process is dominant than thermal emission, because the probability for tunneling is much higher with small energy barrier. While for the traps far away from the substrate, thermal emission is the main process compared to the tunneling process due to the low tunneling probability in large energy barrier.



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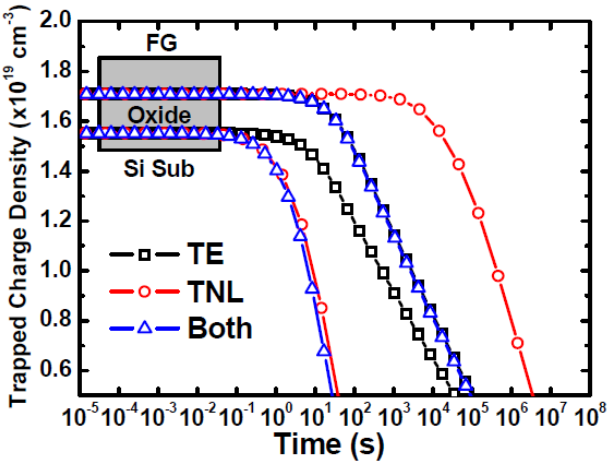


(b)

Fig. 1.5. (a) Band diagram to explain the detrapping mechanism in NAND flash memory. (b) comparison of thermal emission and tunneling processes for the detrapping mechanism according to the physical position for the generated trap sites [26].

1.2.2 Trap-assisted tunneling (TAT) Mechanism

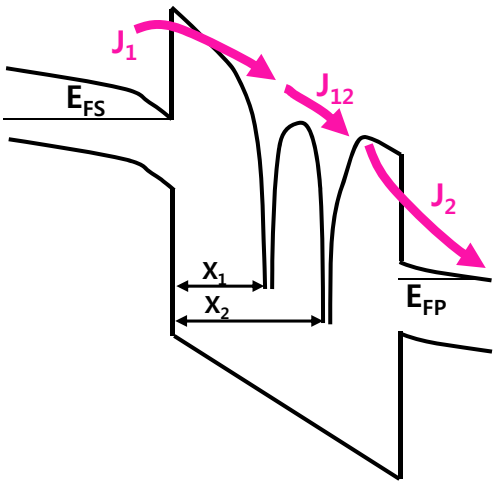
As NAND flash memory has been extremely scaled down for low-cost and high-density, electric properties have become worse and worse [7], [19]. Especially, the degradation of the tunneling oxide quality after P/E cycling seriously limits the reliability of scaled devices [28], [38]. Oxide defect generation due to higher electric field during P/E cycling stress is the main reliability concern. This oxide defects lead to excess leakage conduction known as stress-induced leakage current (SILC). The SILC across the tunnel oxides leads to enhanced charge loss/gain for the tail bits [32]-[35]. Due to the faster charge loss, these tail cells are characterized by shorter retention lifetime, thus are responsible for the failure of the whole array. The statistical distribution of SILC is therefore the key parameter for characterizing and/or estimating flash reliability. Trap-assisted tunneling (TAT) mechanism is generally accepted that the origin of the SILC and the resulting increase in the gate current at a low gate voltage in stressed devices [39]. In this reason, the physical analysis of the TAT mechanism in the retention behavior is significantly important. This mechanism is relatively dominant in the lower temperature regime, and low temperature dependence. It is generally reported that the E_a value of the TAT mechanism is about 0.1 ~ 0.3 eV [35]-[36], [40]-[41]. The TAT mechanism is dominantly occurring through more than two aligned traps. Detailed explanations for the TAT mechanism is following.

Fig. 1.6 shows schematics to explain the SILC phenomena in NAND flash memory [32]. A high field stress on the tunneling oxide increases the gate current density at low electric field, which is known as SILC [39]-[42]. The SILC is clearly attributed to

stress-induced oxide defects, which induces a trap assisted tunneling. The main parameters controlling SILC are the stress field, the amount of injection charge during the stress, and the tunneling oxide thickness. The leakage current increases strongly with reducing the tunneling oxide thickness [32]-[35]. Therefore, it has the trade-off between the scaling of the tunneling oxide thickness and device reliability.

Fig. 1.7 show the measured and calculated I-V characteristics of a tail cell. Calculations were made using the 2TAT model. The results are clearly in good agreement with measured data. The result shows that the SILC mechanism is dominantly occurring through more than two aligned traps (2TAT). Trap density strongly influences on the gate current in low electric field regime, while the gate current in high electric field regime strongly follows Fowler-Nordheim (FN) tunneling model regardless of trap density [32]. Therefore, reducing the trap density in the tunneling oxide layer is great important for the reliability.

Fig. 1.8 shows the simulation result for the electric filed strength across the tunneling layer. The plot shows the corner-to-corner electric field in the diagonal direction (A-A') [43]. Initially, the target V_{th} is set to 3V. Due to the higher electric field and trap density in the corner regime, the average electric barrier between traps is lower. Also, the degradation in the corner regime is larger as increasing the cycling times since the higher electric field causes the faster degradation rate in the corner [38], [43]-[44]. In this reason, the reliability problem due to the TAT mechanism is much vulnerable to the highly scaled device.



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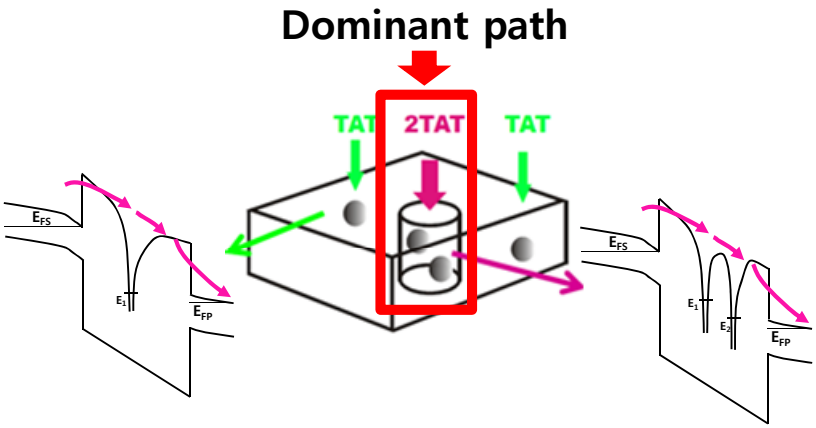


(b)

Fig. 1.6. (a) Schematic of the energy band diagram to explain the multitrap-assisted tunneling (2TAT) mechanism. (b) Schematics for the statistical model of SILC. The SILC is dominantly occurring at the spot with more than two cooperating defects (2TAT) [32].

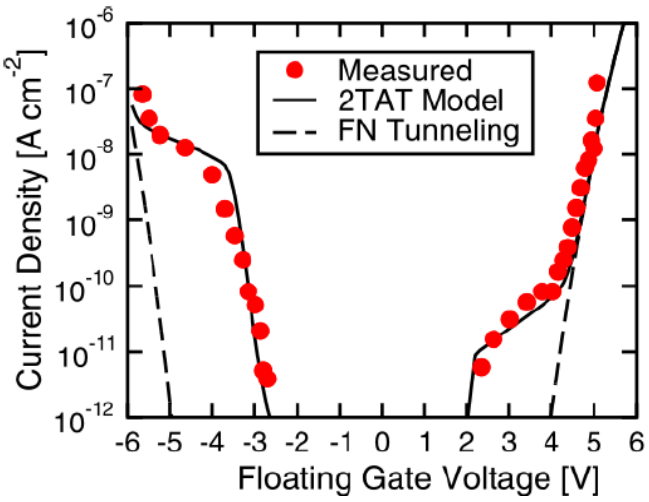


Fig. 1.7. Measured and calculated I-V characteristics of a tail cell compared with results of calculations using 2TAT model and with FN tunneling [32].

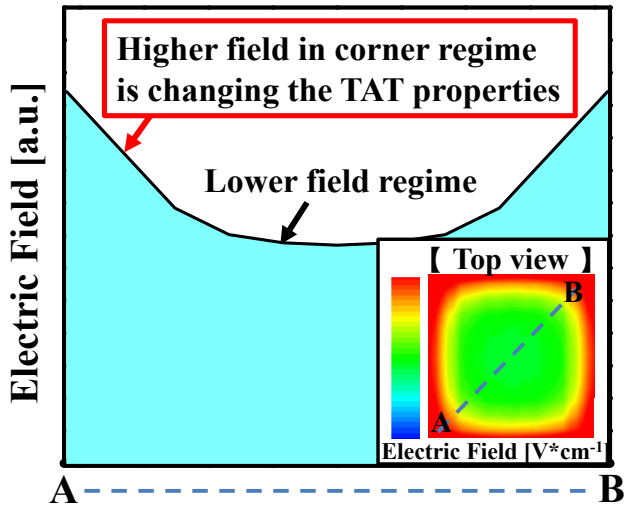
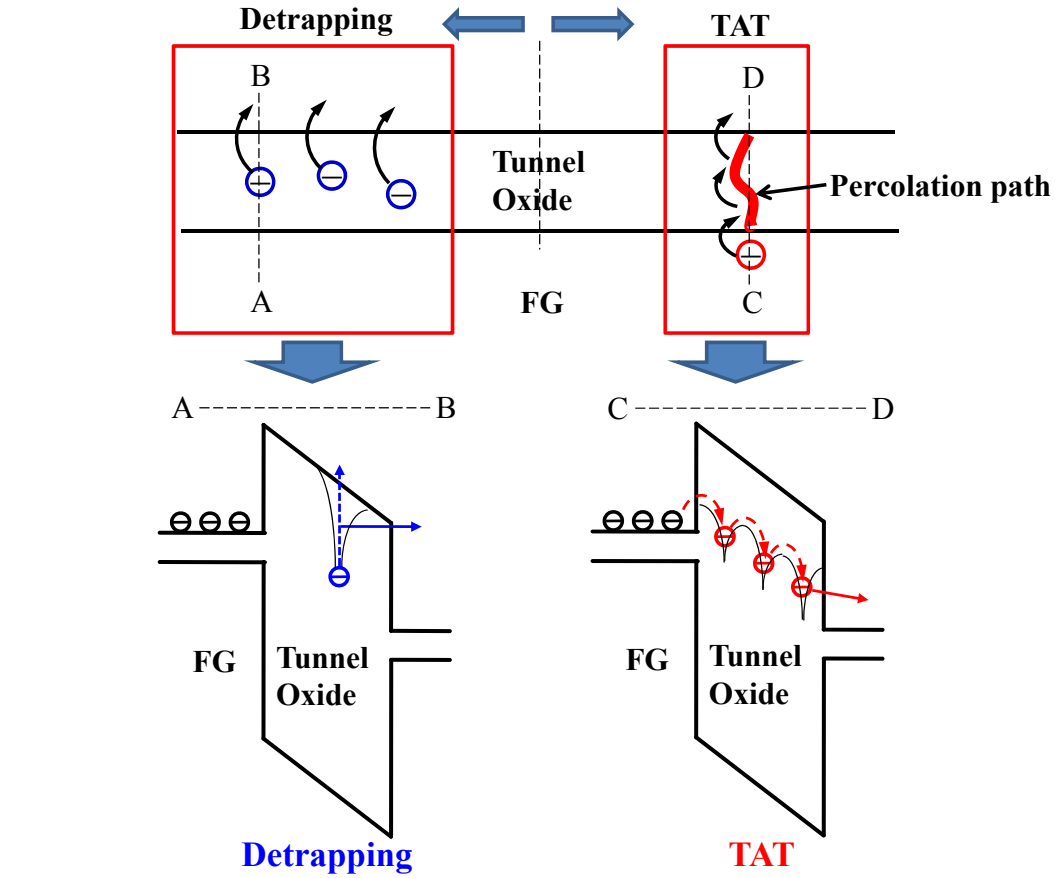


Fig. 1.8. The simulation result of corner-to-corner electric field across the tunneling oxide in the diagonal direction (A-A') shows that much higher field is crowded in the corner regime. The inset is the top view of it. The initial V_{th} is set to 3V [43].

1.2.3 Detrapping Mechanism vs. TAT Mechanism

Fig. 1.9 shows the difference between the detrapping mechanism and the TAT mechanism. Energy band diagrams with the vertical direction (FG-to-substrate) show the detailed conditions for each mechanism well. The trapped charge directly emits to the substrate with high thermal energy. Therefore, the average energy barrier for the detrapping mechanism is large enough so that this mechanism has greater temperature dependence and a higher E_a value (~1.1 eV) [25], [36]-[37]. However, the TAT mechanism is associated with aligned multi-trap. Therefore, the average energy barrier for the TAT mechanism is much smaller. It means the TAT mechanism has weak temperature dependence and a small E_a value (< 0.3 eV) [36], [40]-[42]. Even though the detrapping mechanism can be occurred randomly and relatively uniformly in the tunneling oxide layer, the spot for the TAT mechanism is localized with specific condition. The dielectric layer is not uniform and there can be the weak spot, which electrons are clouded near the interface between FG and dielectric layer such as the place below the grain boundary of poly silicon gate (FG) or the thinnest spot (tunneling oxide layer). It can be percolation path. As dielectric layer gets on the degradation, the percolation path becomes much conductive and the insulating layer breaks down by the path [42]. The generation probability of this percolation path is much higher in the edge/corner regime due to higher electric field stress and higher trap density [38], [43]-[44].



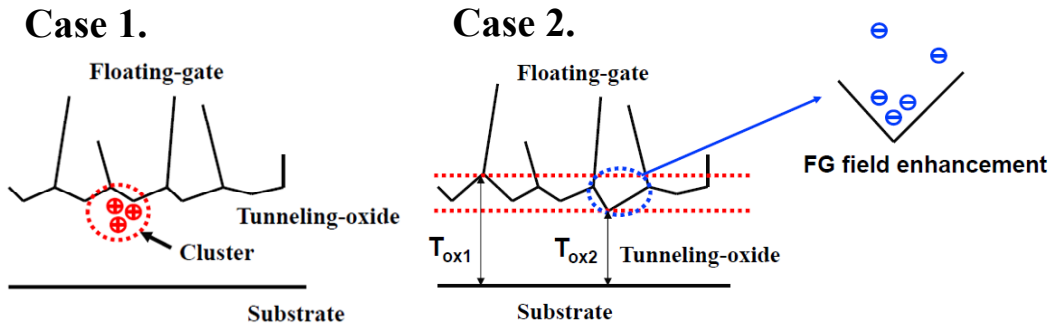


Fig. 1.9. Comparison of energy band diagrams for the detrapping and the TAT mechanisms. The detrapping mechanism can occur relatively all over the oxide layer, while the TAT mechanism occurs at specific spots.

1.2.4 Interface trap (N_{it}) recovery Mechanism

As the device size are scaled down, the degradation of the tunneling oxide layer is accelerating further [28], [43]-[44]. During FN current injection, electron-hole pairs are generated at silicon anode [45]. Some of the generated holes are injected into the oxide and generate hole trap site. The interface traps are generated by hydrogen atom released by detrapping holes from the trap site [28]-[31]. As a result of the damage, V_{th} instabilities increase such as enhanced random telegraph noise (RTN) fluctuations [46], hysteresis on I-V behavior [28], increasing subthreshold swing (SS) [17]-[18], and so on. In addition to that, the degradation partially recovers once stress is removed due to the charge detrapping and interface trap annealing [25], [28]-[29]. This behavior badly affect to the V_{th} instability. Therefore, the physical analysis of the interface trap (N_{it}) recovery mechanism is significantly important to understand the retention behavior in NAND flash memory.

In the crystalline structure, each silicon atom bonds with its neighboring atoms and the periodic structure makes forbidden gap in energy band. At the surface regime, however, the periodic structure is terminated and it makes active interface traps as shown in Fig 1.10(a). In this case, the interface trap density is about $D_{it} \approx 10^{14}$ $cm^{-2}eV^{-1}$. After oxidatio n, most interface traps are bonding with oxygens as shown in Fig 1.10(b). In this case, the interface trap density is about $D_{it} \approx 10^{12}$ $cm^{-2}eV^{-1}$. After hydrogen annealing, interfa ce trap density is further decreased as shown in Fig 1.10(c). In this case, the N_{it} density is approximately $D_{it} \approx 10^{10}$ $cm^{-2}eV^{-1}$. However, this Si-H bonds can easily break at stress conditions due to their lower binding energy and re-activate the N_{it} traps [48].

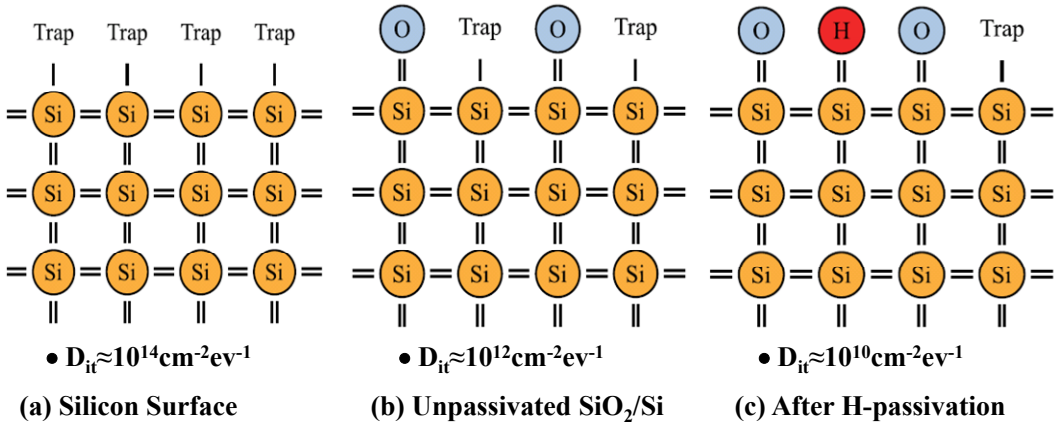


Fig. 1.10. (a) At the silicon surface, silicon atoms are terminated and it makes active interface traps. (b) After oxidation, most interface traps are bonding with oxygens. (c) After hydrogen annealing, interface trap density is further decreased [47].

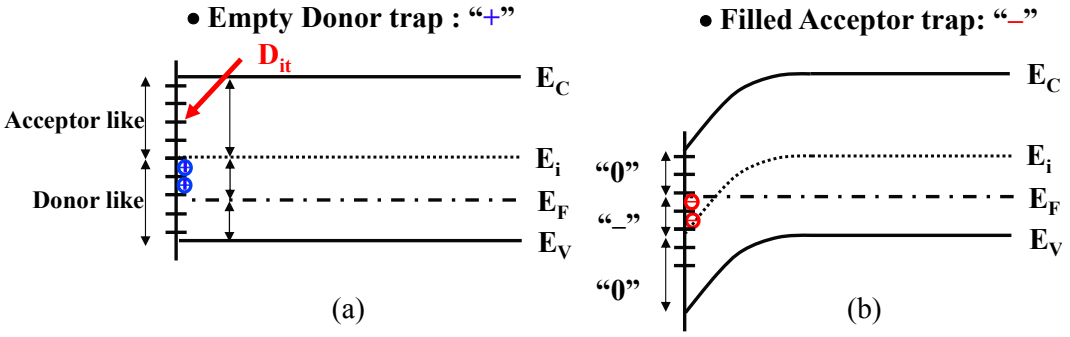


Fig. 1.11. Energy band diagrams of the Si substrate in the conditions of (a) flat band (V_{FB}) and (b) threshold voltage (V_{th}) [48]. Due to the interface states, the surface charge varies with bias condition. (a) positively and (b) negatively charged interface states.

Fig. 1.11 shows energy band diagrams of the Si substrate to explain the relationship between interface traps and V_{th} instability. Interface traps are electrically active defects with an energy distribution throughout the Si band gap. Interface traps at Si-SiO_2 interface consist of acceptor-like in the upper half and donor-like in the lower half of the band gap. Electrons occupy interface trap sites below the Fermi energy level, E_F. Due to this interface charge, Q_{it}, the threshold or the flat band voltage shifts with following relationship [17], [31]:

$$\Delta V_{FB} = -\frac{\Delta Q_{it}(\phi_S)}{C_{ox}} \tag{1.1}$$

where ϕ_s is the surface potential, C_{ox} is the oxide capacitance (ε_{ox}/t_{ox}), respectively.

Fig. 1. 11(a) and (b) show the conditions of flat band voltage (V_{FB}) and threshold voltage (V_{th}), respectively. Occupied donor-like traps and empty acceptor-like traps are neutral. However, Occupied acceptor-like traps act as negative charge and empty donor-like traps act as positive charge [48]. Therefore, the fraction of interface traps between mid gap and the Fermi level directly contributes to the interface charge. In this reason, the interface traps are positively charged in the flat band voltage condition and negatively charged in the threshold voltage condition, respectively.

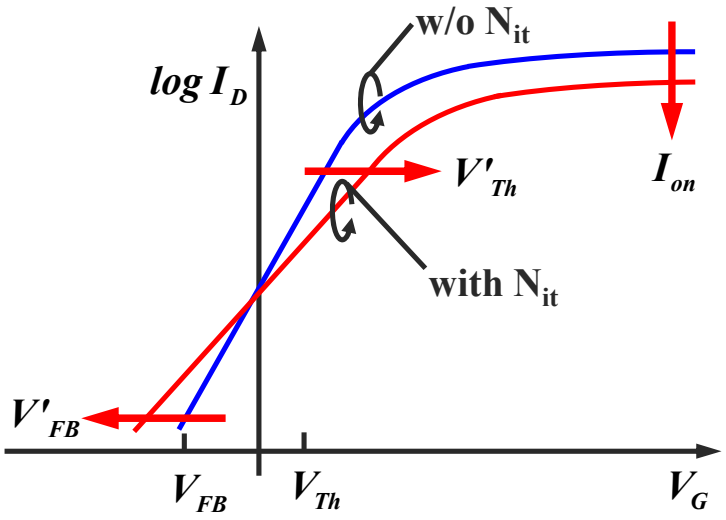
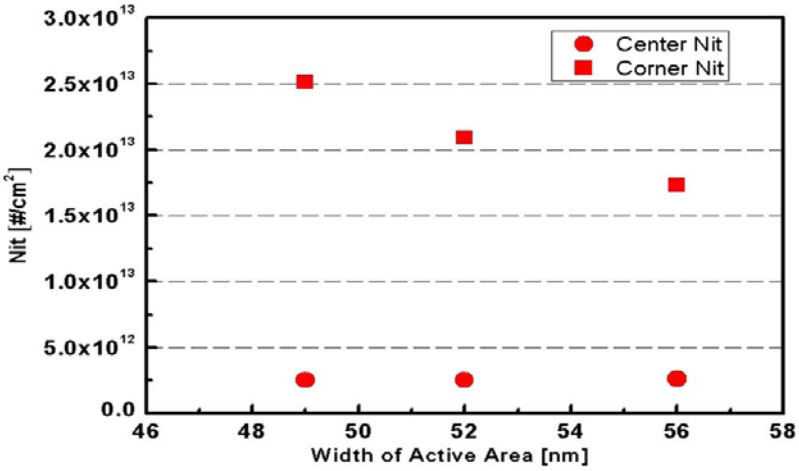


Fig. 1.12. Schematic of I-V characteristics of NAND flash memory cell to explain the impact of interface traps.

Fig. 1.12 shows a schematic to explain the impact of the interface traps on the I-V property of NAND flash memory cell. As explained in Fig. 1.11, there is additional positive interface charge in the flat band voltage condition and additional positive interface charge in the threshold voltage condition. By Eq. (1.1), the flat band voltage shifts to the left and the threshold voltage shifts to the right due to the existence of the interface traps. Therefore, the subthreshold slope (SS) and the V_{th} increase with the interface states. The interface trap density increases with P/E cycling stress in NAND flash memory. However, the generated interface traps can be partially recovered in the early phase during the retention so that the initial V_{th} shifts to the left.



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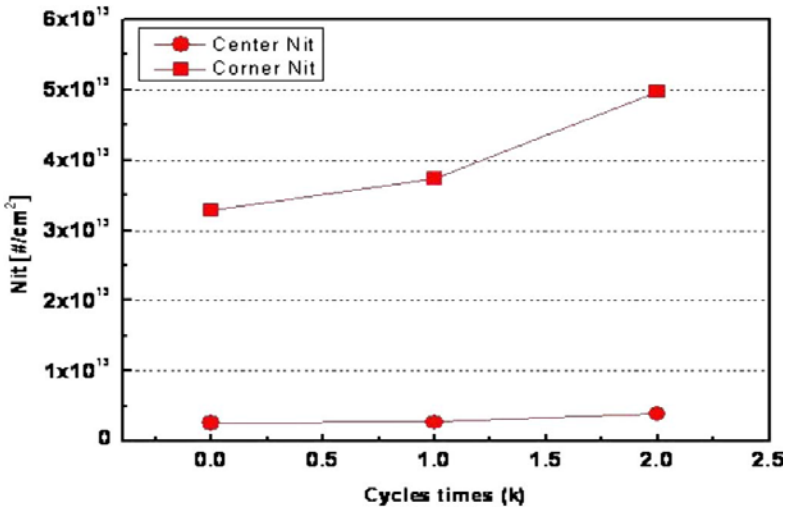


(b)

Fig. 1.13. Extracted center N_{it} and corner N_{it} of NAND flash memory with (a) three different generations and (b) three different P/E cycling stress conditions [38].

Fig. 1.13 shows the extracted center N_{it} and corner N_{it} of NAND flash memory at various generations and P/E cycling stress conditions [38]. In Fig. 1.13(a), it shows the N_{it} in the corner regime is much larger than the N_{it} in the center regime regardless of the width. The corner N_{it} is larger in smaller device, while the center N_{it} is almost constant regardless of the width. In Fig. 1.13(b), it shows that the degradation is larger with P/E cycling stress and the generation of the corner N_{it} is much larger than the center N_{it}. It has been generally reported that highly scaled device worse interface property due to etching damage or higher electric field stress in the corner regime as shown in Fig. 1.8 [28], [38], [43]-[44]. As the generation rate of the interface trap becomes increasing with the scaling, the interface trap generation and recovery are the most important mechanisms in the early phase of the data retention characteristics for the highly scaled NAND flash memory.

1.3 Motivation and Thesis Organization

As NAND flash memory continues to be aggressively scaled down to achieve higher memory densities, various reliability issues are becoming more severe with scaling such as cell-to-cell interference, hot-carrier injection (HCI), single electron effect, and so on [12]-[15]. These scaling limitations cause a broader intrinsic V_{th} distribution and then reduce V_{th} window margin between MLC states in highly scaled NAND flash memory. Therefore, the lifetime of the device is getting shorter and shorter with the scaling-down. However, there is no accurate lifetime estimation model for NAND flash memory up to now. Even though the Arrhenius model is the most popular prediction model, the retention characteristics of NAND devices do not simply follow the Arrhenius law due to coexistence of various mechanisms. Therefore, this conventional Arrhenius model has a huge error in the lifetime prediction. In order to predict the accurate lifetime of the d evice, physical mechanisms should be firstly understood.

This dissertation consists of five chapters and the organization is as follows . In Chapter 1, various failure mechanisms in NAND flash memory are reviewed. Generally well-known failure mechanisms in NAND flash memory are the detrapping [25]-[27], the interface trap (N_{it}) recovery [28]-[31], and the trap-assisted tunneling (TAT) [32]-[35]. In order to understand the abnormal retention characteristics in NAND flash memory, a good physical understanding of various failure mechanisms should be preceded. In Chapter 2, we confirm the abnormal behavior of the Arrhenius plot by the conventional high-temperature data-retention (HTDR) lifetime test and propose a new charge loss model, which involve the retention characteristics of various failure

mechanisms. In Chapter 3, we completely separate the three main failure mechanisms and extracted each activation energy (E_a) in three different generations (A, B, and C) of NAND flash memory test element group (TEG) cells. we also analyze the retention characteristics of each failure mechanism for different generations and cycling times. In Chapter 4, whole detailed procedure of parameter extraction is explained in detail. The parameters are extracted at all states (PV3, PV2, PV1, ERS) of sub 20-nm MLC NAND flash memory. Also, contribution rate (CR) of dominant failure mechanisms are extracted in various retention conditions at specific criterion of $|\Delta V_{th\_Total}|$ according to the baking temperature. From the results, the abnormal retention behaviors such as E_{aa} roll-off at the PV3 and negative E_{aa} at the ERS states are physically analyzed. In Chapter 5, we reveal the origin of abnormal E_{aa} characteristics and derive a mathematical formula for E_{aa} as a function of each $E_{a(\text{mechanism})}$ in NAND flash memory. Also, we propose two different accurate lifetime estimation models for sub 20-nm NAND flash memory. The first model is the E_{aa} integration method. Using the analytically modeled E_{aa} equation, the lifetime of NAND flash memory is accurately predicted. The second model is the advanced extrapolation method. Since the proposed models are developed based on physical retention characteristics of various mechanisms, it provides very accurate prediction on the lifetime of NAND flash memory.

Chapter 2

Introduction of Conventional Lifetime Estimation Model and Proposed Charge Loss Model

2.1 Introduction

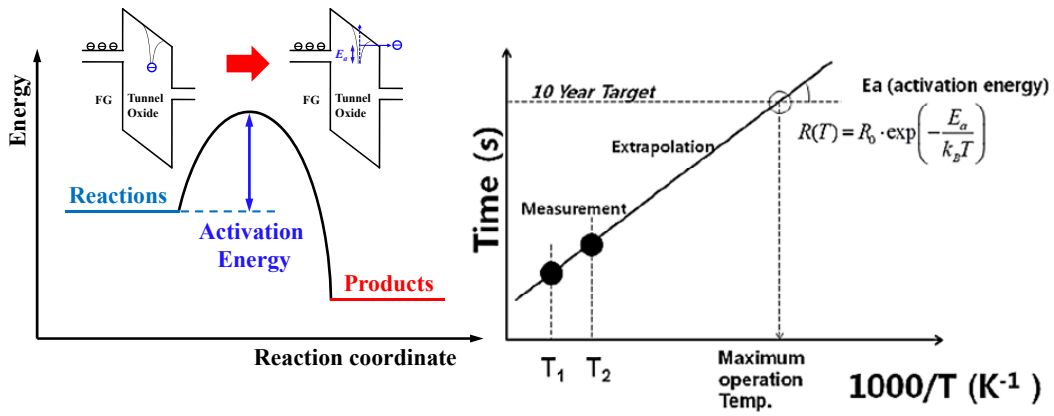
In order for the low cost and higher density, the feature size of NAND flash memory has continueously scaled down. However, the aggressive scaling makes a number of issues related to the reliability of the devices have become more serious and reduces the lifetime. Therefore, accurate lifetime estimation for the device is now important and serious topic for the mass production. There has been no accurate model to predict the lifetime of NAND flash memory up to now. Even though the Arrhenius model is the most popular prediction method [49], the retention characteristics of NAND devices do not simply follow the Arrhenius model due to coexistence of various mechanisms [50]-[52]. Therefore, this conventional model has a huge error. Lifetime of the device is defined as

estimated retention time at room-temperature (RT), when the amount of charge loss/gain reaches to specific criterion. Apparent activation energy (E_{aa}) is an equivalent energy value that can be inserted in the Arrhenius equation for reliability to calculate an acceleration factor applicable to changes with temperature of time-to-failure distributions in electric devices. This Arrhenius model is used under the assumption that the E_{aa} is constant with temperature. Even though the Arrhenius model is the most popular prediction method, the retention characteristics of NAND devices do not simply follow the Arrhenius model due to coexistence of various mechanisms. As a result, this conventional Arrhenius model has a huge error in the lifetime prediction [50]-[52]. In order to predict the accurate lifetime of the device, an accurate model should be developed based on the actual physical retention characteristics.

2.2 Conventional Lifetime Estimation Methods

2.2.1 Arrhenius Model (1/*T* Model)

Fig. 2.1 shows schematics to explain the activation energy and the Arrhenius model. Activation energy (E_a) is defined as the excess free energy over the ground state that must be acquired by an atomic or molecular system in order that a particular process can occur [36]. Each failure mechanism has their own activation energy. The Arrhenius model is the most general temperature-acceleration lifetime evaluation model, which predicts how time-to-fail varies with temperature. It is derived from the Arrhenius reaction rate equation proposed by the Swedish physical chemist Svandte Arrhenius in 1887.



(a) (b)

Fig. 2.1. Schematics for (a) the activation energy and (b) the Arrhenius model

Fig. 2.2 shows the extracted average value of E_{aa} of 20 cells cycled 1K times in generation A NAND flash memory using conventional data retention lifetime test. The common initial programmed threshold voltages (V_{th}) of 20 cells were 3 V by incremental step pulse program (ISPP) scheme. The retention time ($t_{R(bake)}$) was extracted when the average ΔV_{th} of 20 cells reached 0.2 V at each baking temperature. The device lifetime ($t_{R(room)}$) is obtained by the relationship [49]:

$$t_{R(\text{room})} = t_{R(bake)} \cdot \exp\left[\frac{E_a}{k}\left(\frac{1}{T_{room}} - \frac{1}{T_{bake}}\right)\right] \tag{2.1}$$

where $t_{R(room)}$ is the retention time at room temperature, $t_{R(bake)}$ is retention time at the baking temperature, E_a is the activation energy, k is the Boltzmann constant, T_{room} is room temperature, and T_{bake} is the baking temperature. By measuring parametric change caused by temperature, activation energy (E_a) in its physical sense can be estimated. Apparent activation energy (E_{aa}) is an equivalent energy value that can be inserted in the Arrhenius equation for reliability to calculate an acceleration factor applicable to changes with temperature of time-to-failure distributions in electric devices.

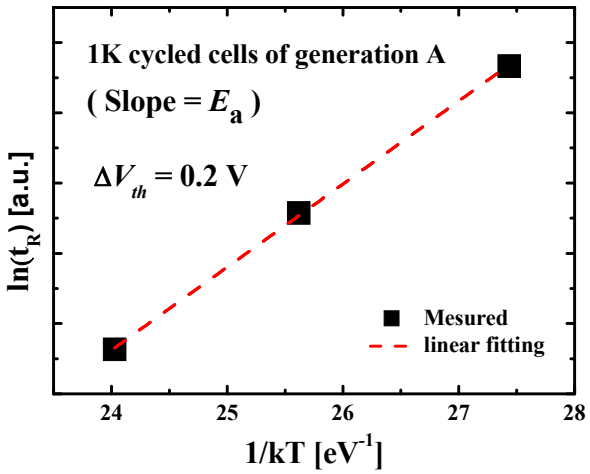


Fig. 2.2. Using the conventional data-retention lifetime test, the activation energy was extracted in 1k cycled NAND flash 20 cells of generation A. This process was conducted in a high temperature regime (150ºC ~ 210ºC), and the criterion of ΔV_{th} was 0.2 V.

Drawback of the Arrhenius Model

This Arrhenius model is used under the assumption that the E_{aa} is constant regardless of the ΔV_{th} criterion or the temperature regime. However, Fig. 2.3 shows the extracted E_a varies depending on the criterion of ΔV_{th} and on the temperature regime, as mixed failure mechanisms exist in NAND flash memory and the dominant mechanism changes depending on the baking temperature. For an accurate lifetime prediction of NAND flash memory, physical retention characteristics of various failure mechanisms should be reflected in the lifetime estimation model.

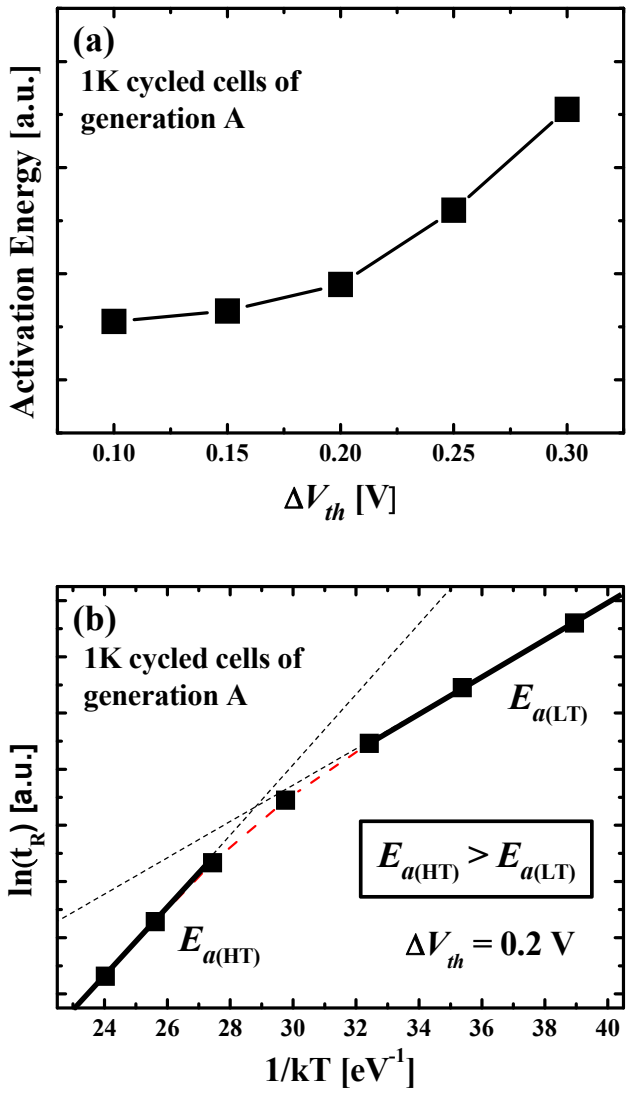


Fig. 2.3. Activation energy changes depending not only on (a) the criterion of ΔV_{th} but also on (b) the temperature regime, as various failure mechanisms appear together in NAND flash memory.

2.2.2 *T* model

In Fig. 2.3, it clearly appears that measured retention data do not fit a straight line as the conventional Arrhenius model (1/*T* model) would require. In ref. [52], De Salvo's group proposed the *T* Model, which is expressed by following equation :

$$t_{R(\mathrm{Low})} = t_{R(\mathrm{High})} \cdot \exp\left[\frac{T_{High} - T_{Low}}{T_0}\right] \tag{2.2}$$

where $t_{R(\mathrm{High})}$ is retention time at high temperature, $t_{R(\mathrm{Low})}$ is retention time at low temperature, T_{High} is high temperature, T_{Low} is low temperature, T_0 is a characteristic temperature of data-retention (in Fig. 2.4, T_0 = 21 K), respectively. From analyzing the ONO leakage current at various applied bias condition, the relationship between T_0 and the applied electric field F is empirically obtained as $T_0 = 6.5 \cdot F$. Using Eq. (2.2), effective activation energy E_a for the *T* Model can be derived as following:

$$E_a = \frac{\partial \ln(t_R)}{\partial\left(\frac{1}{kT}\right)} = \frac{kT^2}{T_0} \tag{2.3}$$

Fig. 2.5 show the calculated effective E_a and measured E_a by different authors.

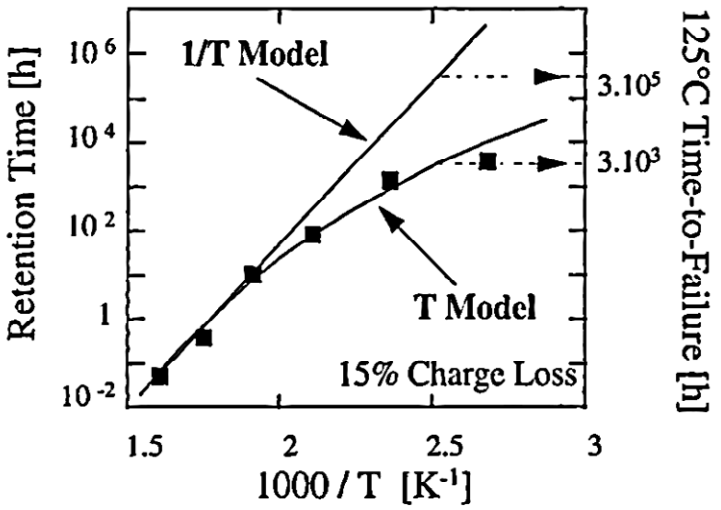


Fig. 2.4. Arrhenius plot of retention time characteristics. Time-to-failure using the 1/T Model and the T Model are extracted at 125 ºC. The criterion is 15% of normalized charge loss [52].

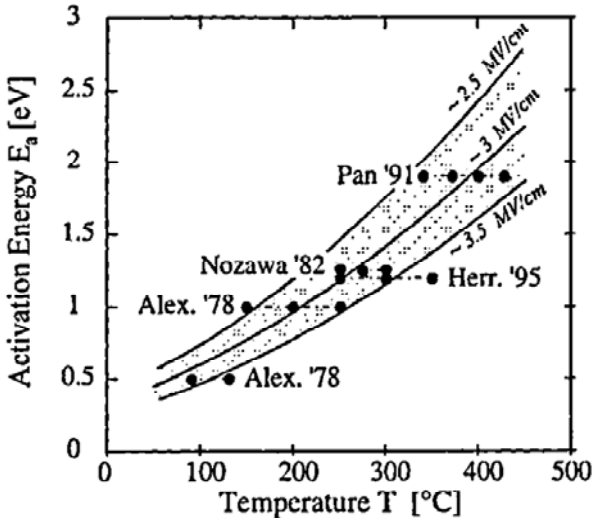


Fig. 2.5. Activation energy E_a [eV] verses temperature T [ºC]. Symbols (●) correspond to activation energy measured by different authors [52].

Drawback of the *T* Model

Even though the *T* Model seems showing a good agreement with E_{aa} roll-off behavior in retention characteristics, there are several problems.

1. This model is only considering the ONO leakage current, even though there are various charge loss mechanisms.

2. A characteristic temperature T_0 is function of the applied electric field F ($T_0 = 6.5 \cdot F$). It makes unreasonable result. For example, when the device in under the retention condition (no applying external voltage), the characteristic temperature T_0 should be 0 and it causes infinite value of E_a as show in Eq. (2.3).

3. This model still has error in the low temperature regime and the error is larger as temperature is lower. The retention test with this model is only conducted in high-temperature regime (100ºC ~ 350ºC).

4. This model cannot be applied for the other states such as the ERS state. In ERS state, the result of the retention test shows different behavior such as negative E_{aa} characteristic [see Fig. 4.10].

We found out the T Model also has several critical problems. In order to estimate the accurate lifetime for the device, physical based new retention model should be proposed.

2.3 Proposed Charge Loss Model

The E_{aa} is generally used to calculate a single acceleration factor even though there are various thermal acceleration factors associated with multiple failure mechanisms. Actually, the inadequacy of lifetime projection by simple Arrhenius model based on high-temp bake data is well known in the society. However, it is still commonly used for lifetime estimation since there is no adequate lifetime prediction model, which reflects abnormal retention behavior such as E_{aa} roll-off. In order to solve this problem, it is important to make accurate model for the time-to-failure distribution on the device retention test according to baking temperature.

2.3.1 Weibull Distribution Model (Stretched Exponential Model)

The behavior of the failure rate generally can be characterized by using the Weibull distribution model (stretched exponential model) [36], [53]-[55]. The stretched exponential decay can be mathematically expressed as a superposition of exponential terms and can be derived as follows [54]:

$$I(t) = \sum_{j=1}^{\infty} \alpha_j \exp\left(-\frac{t}{\tau_j}\right) = \int_0^{\infty} \exp\left(-\frac{t}{\tau}\right) \rho(\tau) d\tau = I_0 \exp\left[-\left(-\frac{t}{\tau}\right)^{\beta}\right] \qquad (2.4)$$

where α_j values are the fractional contribution of the components, $\rho(\tau)$ is the continuous distribution of lifetimes, τ is the characteristic time scale of the decay, β is a shape parameter, respectively. Weibull cumulative distribution function (CDF) is the normalized form of Eq. (2.4), which is the most often used to represent reliability failure mechanisms. The Weibull distribution, which can be written in closed form as

$$F(t) = 1 - \exp\left(-\left(t/\tau\right)^{\beta}\right) \tag{2.5}$$

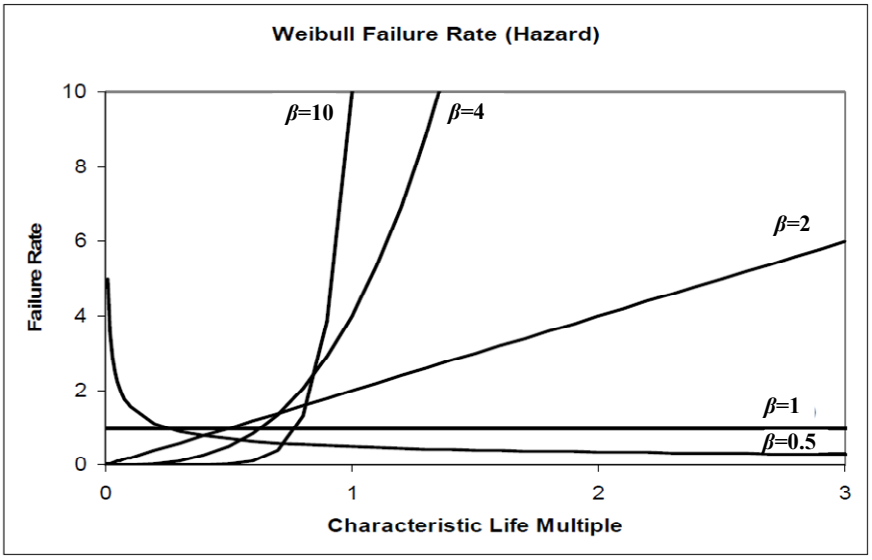


Fig. 2.6. Weibull Failure Rate according to characteristic lifetime [36].

Fig. 2.6 shows the Weibull failure rate according to characteristic lifetime with various shape parameter. The value of the shape parameter determines whether the failure rate (event probability) is increasing ($\beta > 1$), decreasing ($\beta < 1$), or constant ($\beta = 1$). As the distribution of $\rho(\tau)$ has wider, the shape parameter becomes smaller.

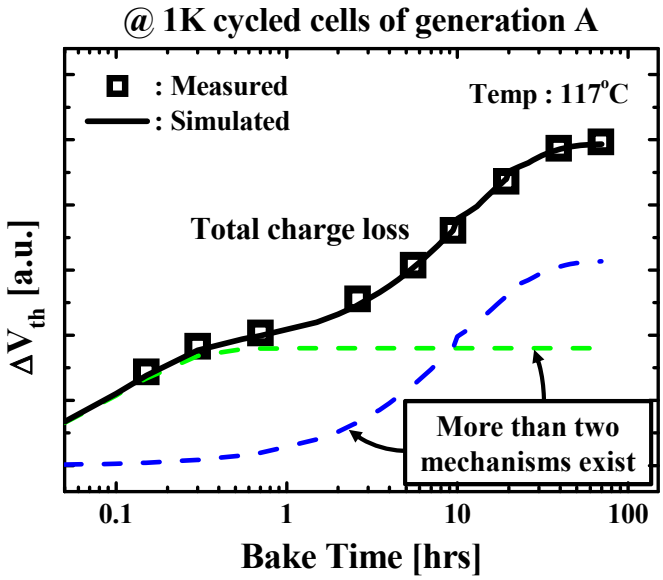


Fig. 2.7. Total charge loss of in NAND Flash memory of generation A according to the bake time at 117 °C. The behavior of total charge loss is not following simple curve. The result seems that more than two mechanisms occur concurrently.

To analyze the failure mechanisms for the generation and cycling dependence in NAND flash memory, a more accurate data-retention lifetime test was conducted. Since the total charge loss is proportional to the V_{th} shift, we observed the ΔV_{th} ($V_{th}(t_0)$ – $V_{th}(t_{bake})$) of the NAND samples in various baking temperature according to the baking time (t_{bake}) [42]. Here, $V_{th}(t_0)$ is the initial V_{th} of the samples and $V_{th}(t_{bake})$ is the value after baking.

Fig. 2.7 shows the total charge loss in NAND flash memory of generation A according to the bake time at 117 ºC. The symbols are the average ΔV_{th} values of 20 cells and the solid line is the best fitting result. The behavior of total charge loss is not following simple curve. Actual charge loss behavior in NAND flash memory cannot be expre ssed by single term of Weibull CDF as shown in following figure. The result seems that more than two mechanisms occur concurrently. Therefore, we assume that th ere are various failure mechanisms and each mechanism has their own temperature acceleration factor (activation energy):

$$\Delta V_{th\_Total}(t_R) = \sum_{k=1}^{n} \Delta V_{th\_k} \cdot \left[1 - \exp\left(-\left(t_R / \tau_k\right)^{\beta_k}\right)\right] \tag{2.6}$$

$$\tau_{LT} = \tau_{HT} \cdot \left[E_a \left(1/kT_{LT} - 1/kT_{HT}\right)\right] \tag{2.7}$$

2.3.2 Physical Background of New Model

The initial V_{th} distributions of NAND flash memory become dispersed due to various failure mechanisms through the retention test. Charge loss mechanism is dominant in the PV3 state, but the charge gain in the ERS state. In order to predict the accurate lifetime of the device, a physical analysis on the mechanisms is necessary.

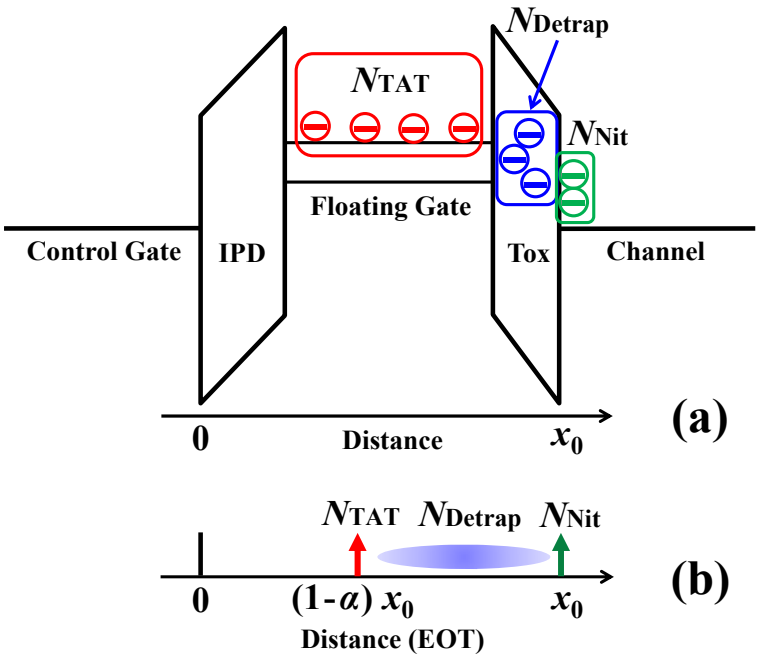


Fig. 2.8. (a) Schematic of energy band diagram for NAND flash memory. Various mechanisms are physically separated. (b) Charge distribution according to equivalent oxide thickness (EOT) distance in 1D.

Fig. 2.8(a) shows the schematic of energy band diagram for NAND flash memory. Various failure mechanisms are physically separated. Each box represents potential source of each mechanism ($\Delta V_{th(\text{mecha.})}$). N_{TAT}, N_{Detrap}, and N_{Nit} are the number of electrons in floating-gate, oxide traps in the tunneling oxide, and accept-like traps at the *Si-SiO₂* interface, respectively. Fig. 2.8(b) shows the charge distribution according to the equivalent oxide thickness (EOT) distance from control-gate to substrate. The charge distribution contributes to the initial V_{th} by Gauss's law. However, charge loss occurs with baking time through various mechanisms such as tunneling, thermal emission, trap annealing, and so on [26], [28]. The amount of total charge loss corresponds to $\Delta V_{th\_\text{Total}}$ with the following relationship:

$$\begin{aligned} \Delta V_{th\_TOTAL} &= \Delta V_{th\_TAT} + \Delta V_{th\_Detrap} + \Delta V_{th\_N_{it}} \\ &\approx K \frac{1}{\varepsilon_{OX}} \int_0^{x_0} x \cdot \rho(x)\, dx \end{aligned} \tag{2.8}$$

where K, ε_{ox}, and $\rho(x)$ are proportional constant ($0 < K < 1$), oxide permittivity, and volume density of net charge distribution, respectively. By the same principle, the amount of charge loss for each mechanism can be expressed as

$$\Delta V_{th\_\text{TAT}} = \text{A}(1-\alpha)\frac{qN_{\text{TAT}}}{C_{\text{total}}} \tag{2.9}$$

$$\Delta V_{th\_\text{Detrap}} = \mathrm{B}\frac{1}{\varepsilon_{\mathrm{OX}}}\int_{(1-\alpha)x_0}^{x_0} x \cdot \rho(x)\, dx \tag{2.10}$$

$$\Delta V_{th\_N_{\mathrm{it}}} = \mathrm{C}\frac{qN_{N_{\mathrm{it}}}}{C_{\mathrm{total}}} \tag{2.11}$$

where α is coupling ratio, C_{total} is normalized total capacitance (ε_{ox}/x_o), the proportional constants (A, B, and C) represent the amount of charge loss (0 < constants < 1). The remained parts [(1-A), (1-B), and (1-C)] represent the permanent parts, which do not contribute to the charge loss [29]. Since mechanisms are physically separated, each mechanism is approximately independent. Weibull cumulative distribution function (CDF) is the most often used to represent reliability failure mechanism [36], [54]. However, there are various failure mechanisms and each mechanism has their own activation energy. Therefore, total charge loss is superposition of each charge loss behavior and can be modeled as [43], [56]-[62]

$$\Delta V_{th\_TOTAL} = \Delta V_{th\_Det} \cdot \left[1 - \exp\left(- \left(\frac{t_R}{\tau_{Det}} \right)^{\beta_{Det}} \right) \right] + \Delta V_{th\_N_{it}} \cdot \left[1 - \exp\left(- \left(\frac{t_R}{\tau_{N_{it}}} \right)^{\beta_{N_{it}}} \right) \right] + \Delta V_{th\_TAT} \cdot \left[1 - \exp\left(- \left(\frac{t_R}{\tau_{TAT}} \right)^{\beta_{TAT}} \right) \right] \quad (2.12)$$

where t_R, $\tau_{(mecha.)}$, and $\beta_{(mecha.)}$ are the retention time, the time-constant for each mechanism, and the shape parameter for each mechanism, respectively. In the retention condition, the value of β is always smaller than 1 ($0 < \beta_{mecha.} < 1$). It means that the occurrence probability of failure mechanism decreases over time [36], [53]. Since the charge loss occurs during retention test, electric field at tunneling oxide becomes lower with time due to the reduced source for the mechanisms. Therefore, the probability of the charge loss event decreases with time.

2.4 Summary

As scaling down,reliability issues become serious problem in NAND flash memory. Therefore, accurate lifetime estimation is the most important topic for mass production. The Arrhenius model is the most general temperature-acceleration lifetime evaluation model, which predicts how time-to-fail varies with temperature. However, actual retention behavior does not follow the Arrhenius model due to coexistence of various failure mechanisms. As a result, this conventional Arrhenius model has a huge error in the lifetime prediction.

In this chapter, we propose an accurate charge loss model based on the physical retention characteristics for the mechanisms. Since mechanisms are physically separated, each mechanism is approximately independent. Therefore, we assume that the charge loss behavior of each mechanism follows the stretched exponential model, which is the most often used to represent reliability failure mechanisms. Also, each mechanism has their own activation energy. Therefore, total charge loss is modeled as superposition of each charge loss behavior.

Chapter 3

Activation Energiew (E_a) of Failure Mechanisms in Advanced NAND Flash Cells for Different Generations and P/E Cycling

3.1 Introduction

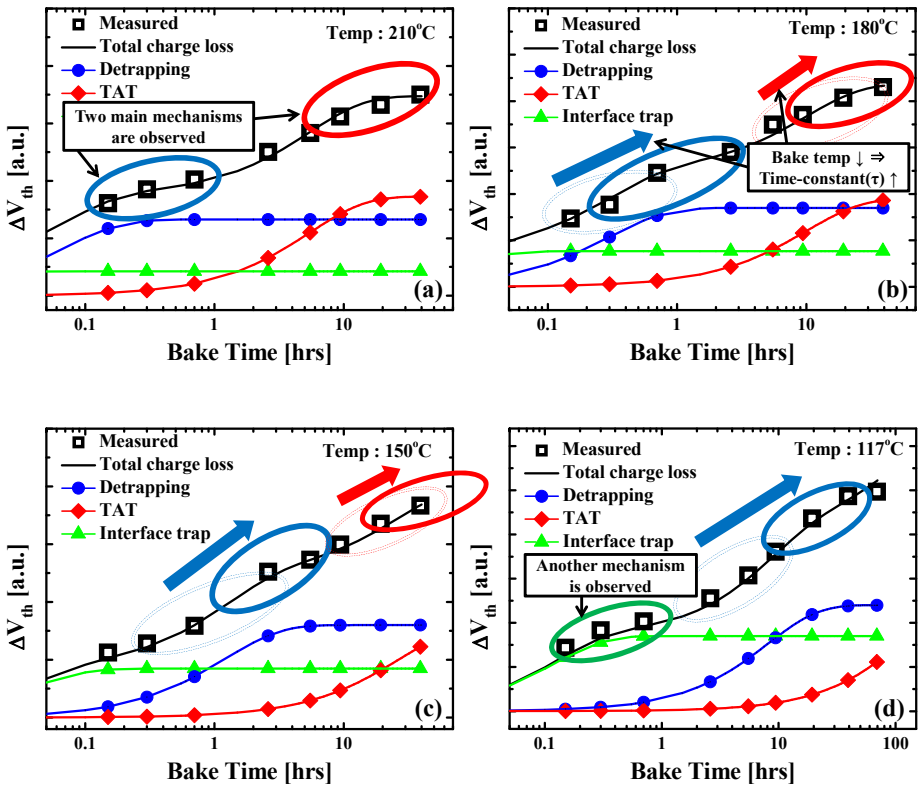
As the market volume of NAND flash memory has explosively expanded with extensive applications such as USB memory, tablet PCs, and smart phones, the demand for low-cost, high-density memory is continuously increasing [1]-[3]. In order to meet the steadily increasing market demand, the integration density has doubled every year, thus outstripping Moore's law [6]. However, the aggressive scaling-down of NAND flash memory makes this type of memory increasingly sensitive to reliability issues. As a result, the lifetime estimation of NAND flash memory is now a serious topic for mass

production. Although a high-temperature data-retention (HTDR) test using the Arrhenius model has been generally used for lifetime estimation of electric devices, a simple application of the Arrhenius model does not apply to NAND flash memory, as several failure mechanisms occur together [50]-[52]. Therefore, a new lifetime evaluation method for NAND flash memory should be formulated for accurate predictions of the lifetime.

In this chapter, we completely separate the three main failure mechanisms (the detrapping mechanism, the trap-assisted tunneling (TAT) mechanism, and the interface trap recovery mechanism) and extracted each activation energy (E_a) at three advanced generations (A, B, C) of NAND flash memory cells [57]. We also extract the E_a value of each failure mechanism in three generations (A, B, C) of advanced NAND flash cells. A, B, and C are three different generations of NAND flash memories. The procedure and the experimental results in three generations (A, B, C) of NAND flash cells are shown in this chapter. In addition to the results, we analyze the retention characteristics of each failure mechanism for different generations and cycling times. The results showe that the E_a value of the detrapping mechanism has extremely weak dependence not only on the generation but also on the cycling times. However, the E_a value of the TAT mechanism is dependent on both. The reason for this is discussed in detail.

3.2 Procedure of Activation Energies (E_a) Extraction

In order to analyze the characteristics of each mechanism, the lifetime test was conducted with various baking temperatures and time splits. As a result, three dominant mechanisms were detected in NAND flash memory cells. We analyzed and extracted each activation energy (E_a). The detailed procedure of mechanism separation is following.



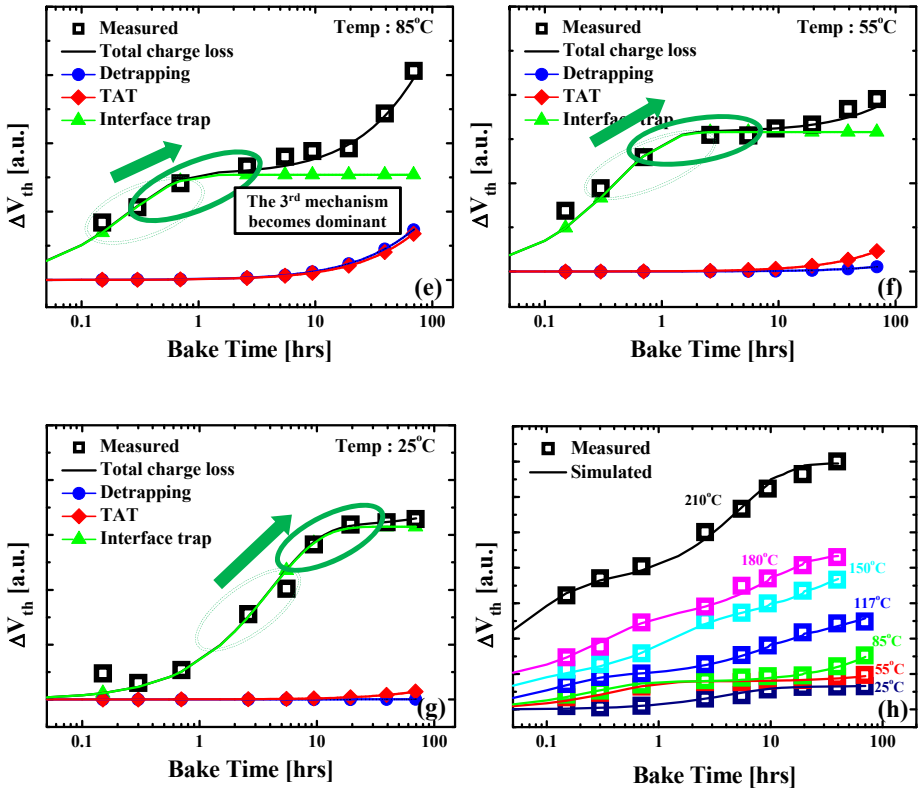


Fig. 3.1. Total charge loss of in NAND flash memory of generation A according to the bake time and temperature. Each measured instance of data is the average value of 20 1k-cycled cells at (a) 210ºC, (b) 180ºC, (c) 150ºC, (d) 117ºC, (e) 85ºC, (f) 55ºC, and (g) 25ºC. All measured data and fitting results are shown in (h). The convex parts correspond to the time-constant (τ) of each mechanism. Each time-constant (τ) of the mechanisms becomes larger as the temperature decreases. In the high-temperature regime (210ºC ~ 180ºC), two dominant mechanisms are clearly observed. Below 117ºC, another mechanism is observed, and it becomes dominant as the bake temperature decreases.

Fig. 3.1 shows the total charge loss in NAND flash memory of the generation A according to the baking time and temperature. Each symbol for measured data represents the average value of 1k-cycled 20 cells at several baking temperatures ((a) 210ºC, (b) 180ºC, (c) 150ºC, (d) 117ºC, (e) 85ºC, (f) 55ºC, and (g) 25ºC). All measured data and fitting results are shown in (h). The convex parts (marked by ellipses) correspond to the time-constants (τ) of each mechanism. In Fig. 3.1(a), two dominant mechanisms are clearly observed, which have different time-constants (τ). In Fig. 3.1(b) and (c), it is shown that the time-constants (τ) of each mechanism become larger as the baking temperature is reduced. In Fig. 3.1(d), another failure mechanism is observed with a very short time-constant (τ). In Fig. 3.1(e), (f), and (g), the third mechanism becomes dominant because the time-constants (τ) of the other mechanisms are already too large. As a result, three dominant mechanisms were observed from the analysis with various baking temperatures and time splits. Based on the experimental result, the total charge loss (ΔV_{th}) model was modeled as the superposition of three main mechanisms as follows:

$$\begin{aligned}\Delta V_{th\_TOTAL} = & \Delta V_{th\_Det} \cdot \left[1 - \exp\left(-\frac{t_R}{\tau_{Det}}\right)\right] \\ & + \Delta V_{th\_N_{it}} \cdot \left[1 - \exp\left(-\frac{t_R}{\tau_{N_{it}}}\right)\right] \\ & + \Delta V_{th\_TAT} \cdot \left[1 - \exp\left(-\frac{t_R}{\tau_{TAT}}\right)\right]\end{aligned} \tag{3.1}$$

In here, we assume that the shape parameter, β, is '1' in order to simplify [63]-[64].

It is anticipated that the mechanisms with shorter and longer time-constants (τ) in Fig. 3.1(a) are the detrapping mechanism and the TAT mechanism, respectively. The third mechanism in Fig. 3.1(e) is the interface trap recovery mechanism based on the theoretical background, as follows:

1) Detrapping mechanism: In a high-temperature regime, trapped electrons in the oxide layer can be directly detrapped to the substrate with high thermal energy [25]-[27]. Therefore, this mechanism has greater temperature- dependence and a higher value of E_a. Generally, it is reported that the E_a value of the detrapping mechanism is around 1.1~1.2 eV [25], [36]-[37].

2) TAT mechanism: It is generally accepted that the origin of the stress-induced leakage current (SILC) and the resulting increase in the gate current at a low gate voltage in stressed devices is trap-assisted tunneling (TAT) [39]. This mechanism is dominant in the lower temperature regime, and the value of E_a is reported to be around 0.3 eV [35]-[36].

3) Interface trap recovery mechanism: The process of this mechanism is generally accepted that P/E cycling stress generates interface traps by the breaking of Si–H(D) bonds and the release of hydrogen/deuterium at or near the oxide/silicon interface [31]. The fast recovery of the generated interface trap occurs after the stress is removed [29]-[30]. The generally reported value of E_a is less than 0.2 eV [30], [65].

In Fig. 3.1, the total charge loss (ΔV_{th}) is the result of the best fitting using Eq. (3.1). From Fig. 3.1, each failure mechanism was separated.

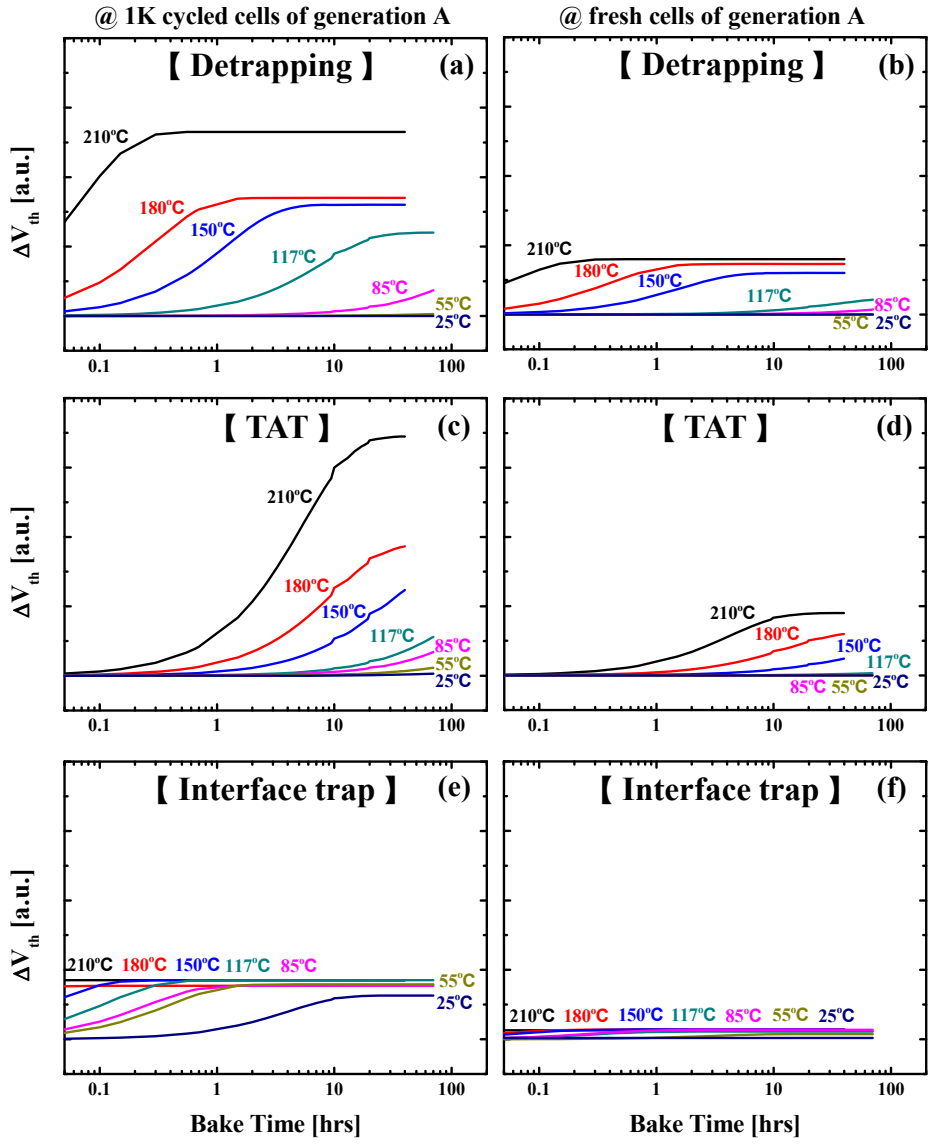
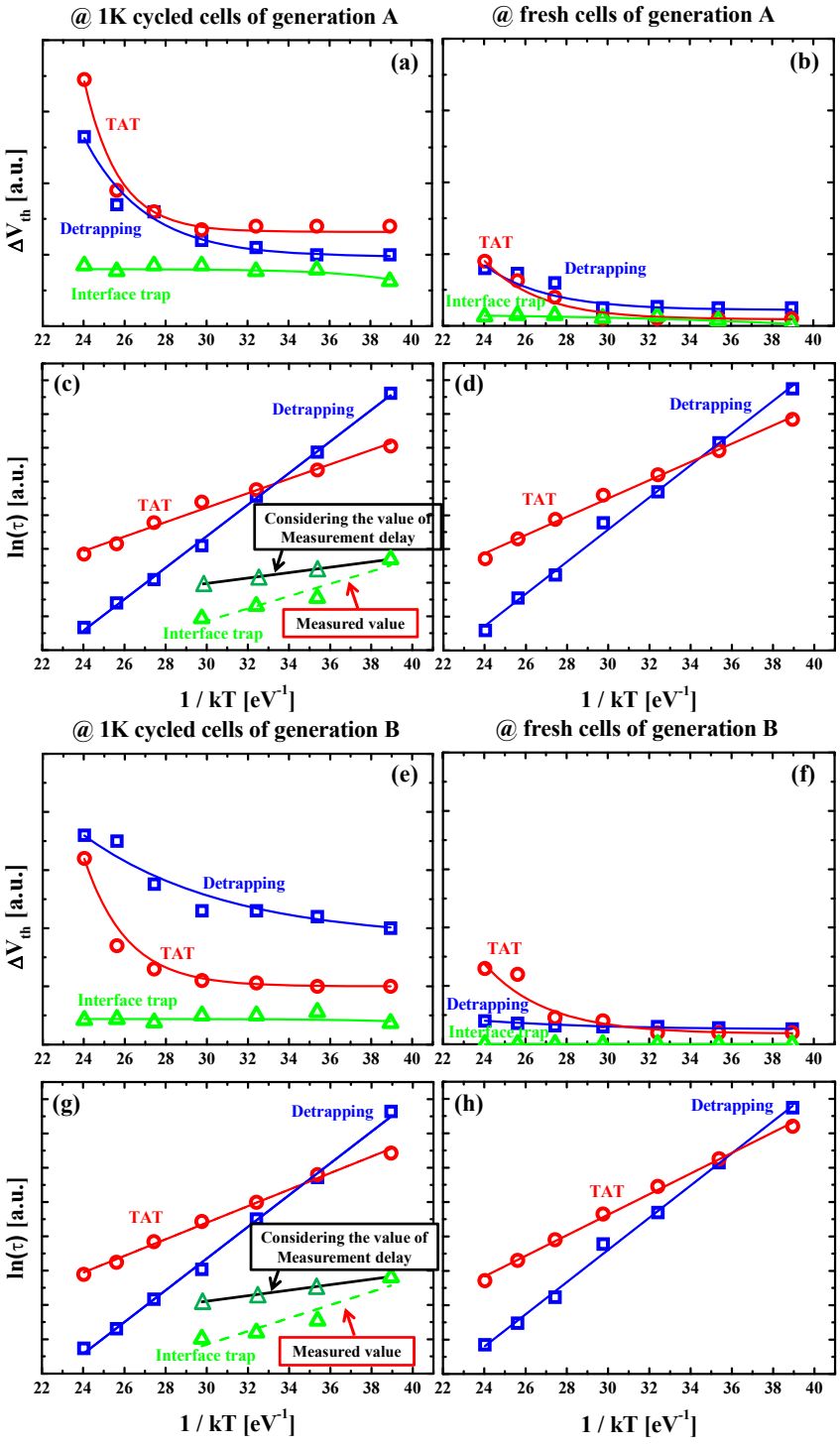


Fig. 3.2. The behavior of each failure mechanism according to the bake time at various baking temperatures (25ºC, 55ºC, 85ºC, 117ºC, 150ºC, 180ºC, and 210ºC). The component of the detrapping mechanism in (a) the 1k-cycled and (b) fresh cells. The TAT mechanism in (c) the 1k-cycled and (d) fresh cells. The interface trap mechanism in (e) the 1k-cycled and (f) fresh NAND flash cells of generation A.

Fig. 3.2 shows the temperature characteristics of the detrapping mechanism in (a) the 1k-cycled and (b) fresh cells; the TAT mechanism in (c) the 1k-cycled and (d) fresh cells; and the interface trap recovery mechanism in (e) the 1k-cycled and (f) fresh NAND flash cells of generation A at various baking temperatures according to the baking time. Each mechanism in Fig. 3.2 corresponds to each term in Eq. (3.1), which are the best fitting results. It is clearly observed that the time-constants (τ) of all mechanisms become shorter and that the amplitude of the final value of ΔV_{th} is larger at a higher baking temperature, as the reaction rate of each failure mechanism is higher and because the amount of the reaction source is greater.

Fig. 3.3(a) and (b) show the trend of final ΔV_{th} amplitude of each failure mechanism for the 1k-cycled and fresh NAND cells of the generation A type according to the baking temperature conditions. Fig. 3.3(c) and (d) show the temperature behavior of the time-constants (τ) of the main mechanisms in the 1k-cycled and fresh NAND cells of generation A, respectively. The experimental results of the other generations are also shown below. Fig. 3.3(e), (f), (i), and (j) show the amplitude of the final ΔV_{th} of the three failure mechanisms in 1k-cycled and fresh cells of generation B and 1k-cycled and fresh cells of generation C depending on the baking temperatures, respectively. Fig. 3.3(g), (h), (k), and (l) show the time-constant (τ) behavior of each failure mechanism of 1k-cycled and fresh cells of generation B and 1k-cycled and fresh cells of generation C depending on the baking temperature, respectively. All mechanisms follow the Arrhenius law well. As we assumed, this result confirms that the detrapping mechanism has strong

temperature-dependence (larger E_a) and small time-constant (τ) in high temperature regime. The TAT mechanism has weak temperature- dependence (smaller E_a) and the interface trap recovery mechanism has a time-constant (τ) that is too small to be detected in a high-temperature regime as well as very weak temperature-dependence, as shown in Fig. 3.3(c). The interface trap recovery has short time-constant (τ) even at room temperature. In order to measure the V_{th} shift, I-V sweep should be conducted at room-temperature. Therefore, interface trap mechanism still progresses during measuring the V_{th}. For this reason, the measurement delay of the interface trap recovery mechanism should be considered. However, the delay effect of the other mechanisms can be ignored since the time-constants (τ) of the other mechanisms are long enough at room-temperature. Considering the measurement delay, the E_a value of the interface trap recovery mechanism is expected to be around 0.2 eV. All of the amplitude of final ΔV_{th} values, especially in the interface trap recovery component, increase after the cells are 1k P/E cycled due to the generated oxide and the interface traps during the stress.


@ 1K cycled cells of generation A
@ fresh cells of generation A
(a)
(b)
(c)
(d)
TAT
Detrapping
Interface trap
ΔV_th [a.u.]
ln(τ) [a.u.]
Considering the value of Measurement delay
Measured value
1 / kT [eV^-1]
@ 1K cycled cells of generation B
@ fresh cells of generation B
(e)
(f)
(g)
(h)

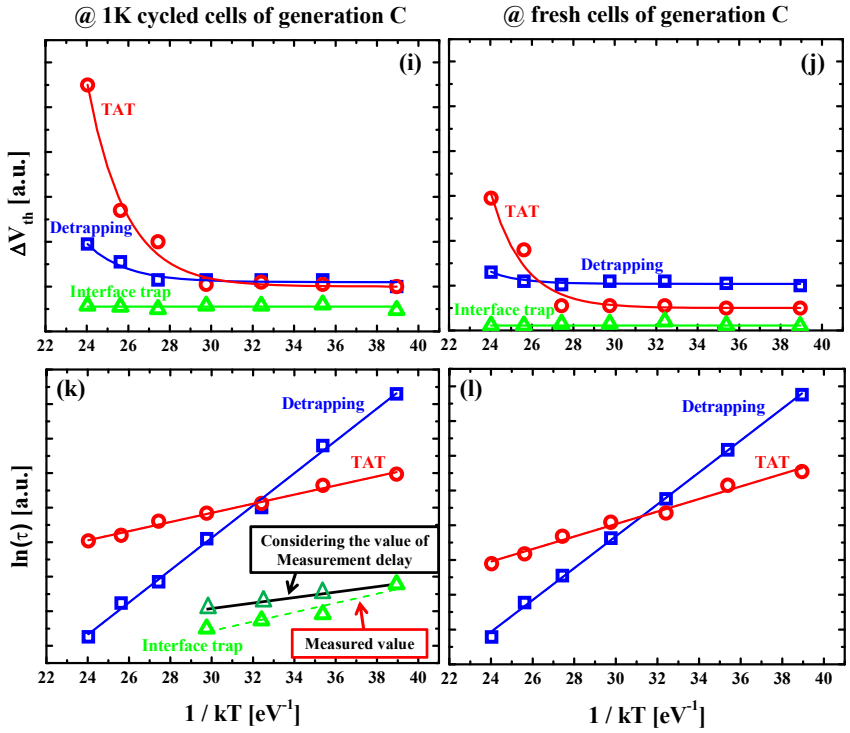


Fig. 3.3. Amplitude of the final ΔV_{th} of the three failure mechanisms in 1k-cycled cells of (a) generation A, (e) generation B, and (i) generation C and fresh cells of (b) generation A, (f) generation B, and (j) generation C depending on the baking temperatures (25ºC, 55ºC, 85ºC, 117ºC, 150ºC, 180ºC, and 210ºC). Time-constant (τ) behavior of each failure mechanism of 1k-cycled cells of (c) generation A, (g) generation B, and (k) generation C and fresh cells of (d) generation A, (h) generation B, and (l) generation C depending on the baking temperature. Each mechanism follows the Arrhenius law well.

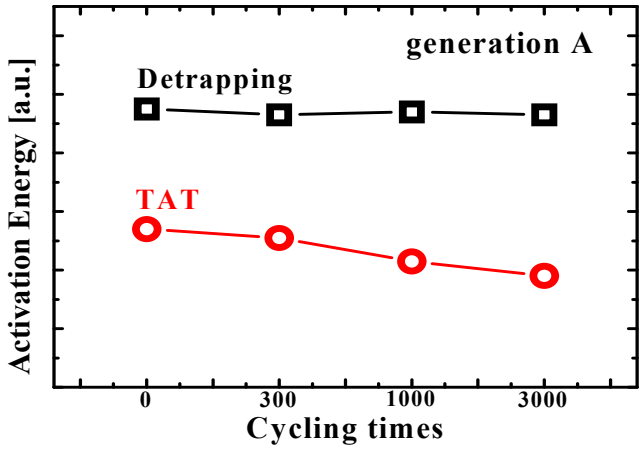


Fig. 3.4. Activation energies of two main failure mechanisms according to the cycling times. The E_a value of the detrapping mechanism remains constant while the TAT mechanism decreases according to the number of cycling.

Fig. 3.4 shows the cycling dependence of E_a of the two mechanisms (the detrapping mechanism and the TAT mechanism). The E_a values of the detrapping mechanism remains at approximately 1.0 eV regardless of the number of cycles. However, the E_a of the TAT mechanism continuously decreases as the number of cycling times is increasing [42], [58]. The cycling dependence of the interface trap recovery mechanism is not shown in Fig. 3.4 because the component in 300 cycled and fresh cells are so small that error is too large. In addition to this, it is difficult to extract the exact value of E_a of the interface trap mechanism due to the measurement delay, even though the extracted values in 1k- and 3k-cycled NAND flash cells are quite same.

3.3 Analysis of Failure Mechanisms

The extracted E_a values of each failure mechanism for different generation and P/E cycling are in Table 3.1. The extracted E_a values of the detrapping mechanism are similar regardless of the generation or the number of cycling. However, E_a of the TAT mechanism depends on the generation ($E_{aB} > E_{aA} > E_{aC}$) and the number of cycling times ($E_a > E_a'$). E_a of the interface trap in the 1k-cycled cells has quite small values ($E_a \sim 0.2$ eV) regardless of the generation. In this chapter, we analyze the retention characteristics of each failure mechanism, especially in terms of the generation and degree of cycling dependence.

TABLE 3.1

THE EXTRACTED E_A VALUES OF EACH FAILURE MECHANISM ACCORDING TO EACH GENERATION ($E_{aB} > E_{aA} > E_{aC}$) AND P/E CYCLING ($E_a > E_a'$).

	Detrapping			**TAT**			**Interface trap**		
	A	**B**	**C**	**A**	**B**	**C**	**A**	**B**	**C**
Fresh	**~ 1.0 eV**			E_{aA}	E_{aB}	E_{aC}	•	•	•
1K cycled				E_{aA}'	E_{aB}'	E_{aC}'	**~ 0.2 eV**		

3.3.1 Detrapping Mechanism

Fig. 3.5 shows schematic of the detrapping mechanism in NAND flash memory. The extracted E_a value of the detrapping mechanism are similar regardless of the generation and the cycling times, as they are mainly determined by the change rate of the detrapping probability of each trapped electron from the trap site according to the baking temperature. Therefore, the contributions from both the device surface area and trap density are small.

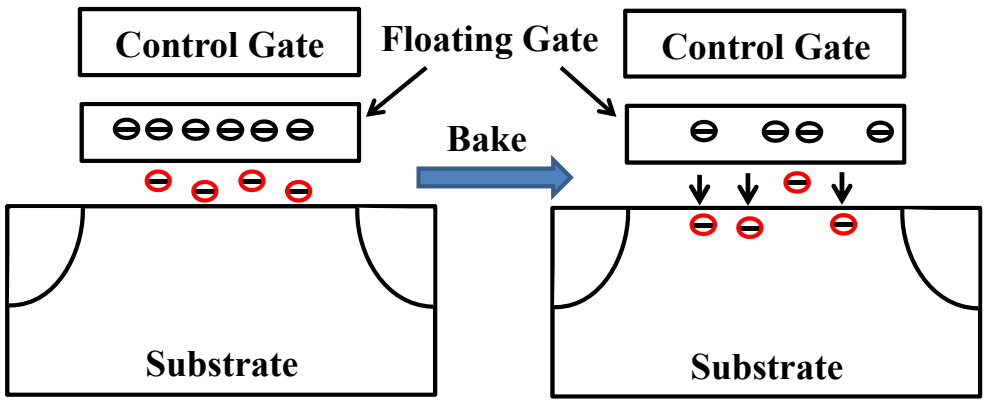


Fig. 3.5. Schematic of the detrapping mechanism in NAND flash memory. The extracted E_a values of the detrapping mechanism are similar regardless of the device generation and cycling characteristics.

3.3.2 TAT Mechanism (Generation dependence)

As shown in Table 3.1, E_a of the TAT mechanism is dependent on the device generation ($E_{aB} > E_{aA} > E_{aC}$). Because the energy barrier height at the interface between the floating gate (FG) and the gate oxide (~ 3 eV) is much higher than the thermal energy of electrons in the FG even at high temperature [see Fig. 3.6(a)], the probability of thermionic electron emission is extremely low. Therefore, the dominant trap profile in terms of both energy and space plays a primary role in the retention characteristics [23]. Fig. 3.6(b) explains the relationship between E_a of the TAT mechanism and the dominant trap energy level. Deep traps have lower values of E_a and are more conductive due to the better alignment between the dominant trap energy level and the average energy level of the electrons in the FG. However, the capture times of shallower traps are more sensitive than deeper traps to the baking temperature and much shorter in the high temperature regime. Moreover, shallow traps have higher E_a values due to misalignment; hence, they show strong temperature acceleration characteristics [23],[51].

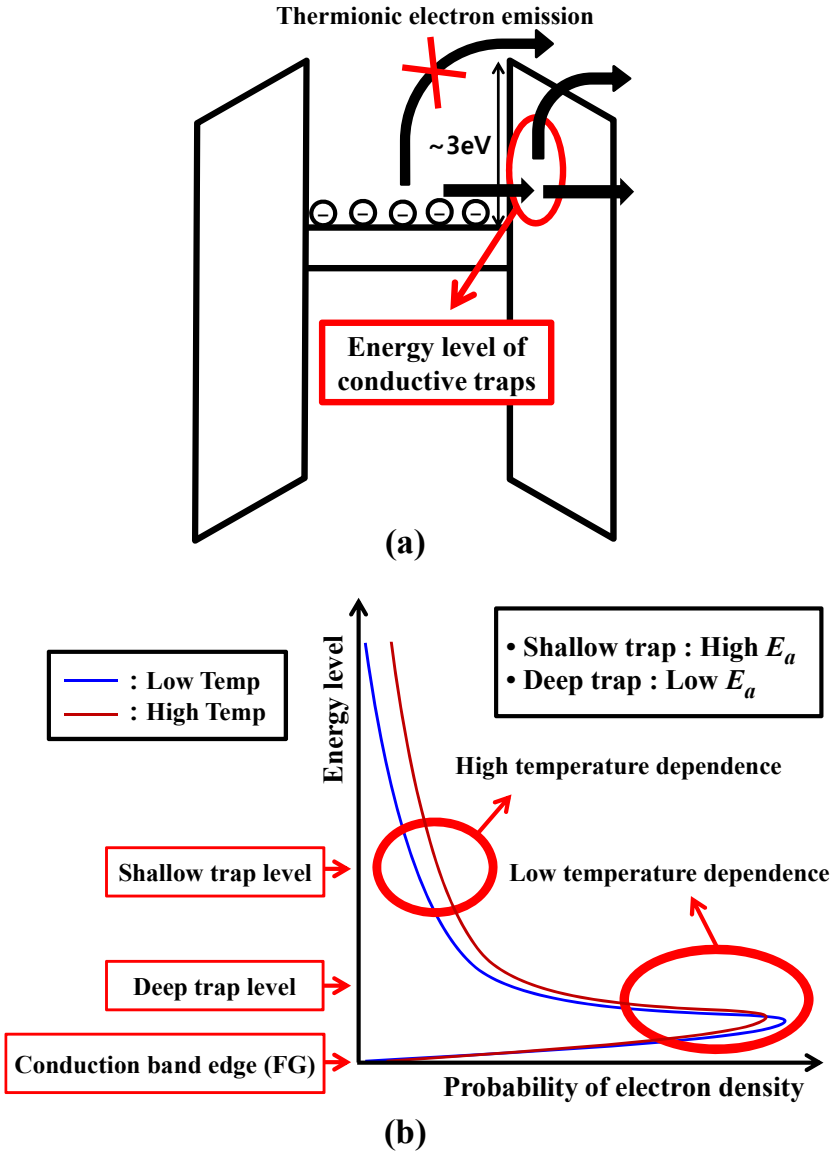


Fig. 3.6. (a) Band diagram showing several paths for electron leakage from the FG. Because the probability of thermal emission is very low, dominant traps play a primary role. (b) The relationship between E_a of TAT and the trap energy level. Note that the CB edge of SiO_2 is the reference level for all trap depths.

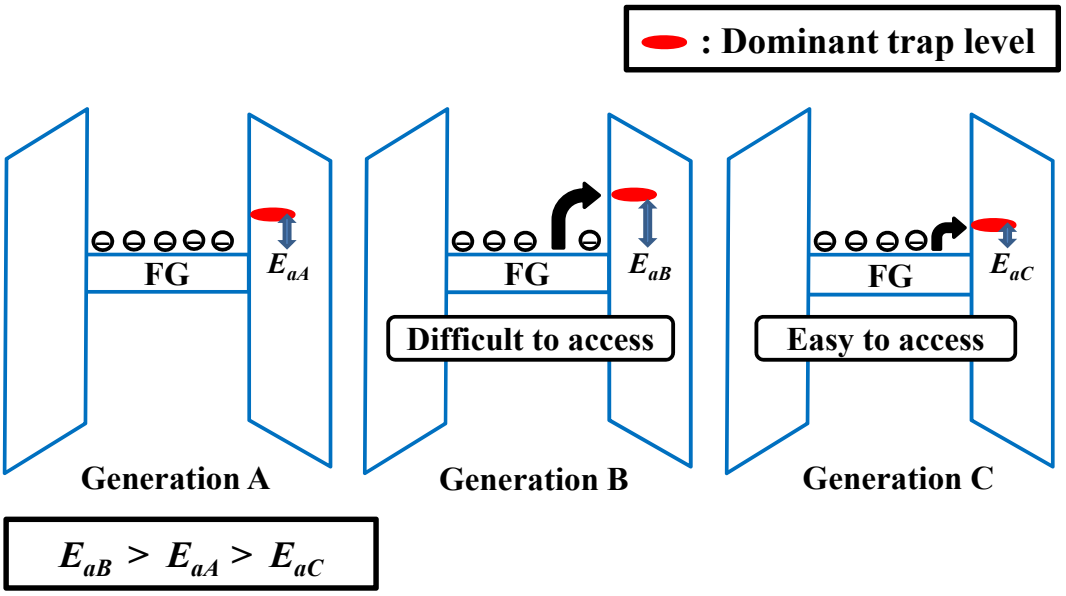


Fig. 3.7. Dominant trap energy level of each generation. Generation B has dominant traps with shallow energy level while generation C has dominant traps with deep energy level.

Fig. 3.7 shows the expected relative trap energy levels among the three generations of NAND flash memory. The generation B device has dominant traps with shallow energy level, while the generation C device has dominant traps with deep energy level. The generation B device has stronger temperature- dependence and better retention characteristics at room temperature compared to the generation C device.

3.3.3 TAT Mechanism (P/E cycling dependence)

Fig. 3.8 shows the total energy diagram corresponding to the electron transition from a filled trap to empty one. Newly generated traps by P/E cycling stress causes the mean distance between the traps to decrease. Therefore, E_a' (after cycling) is lower than E_a (before cycling) in all generations.

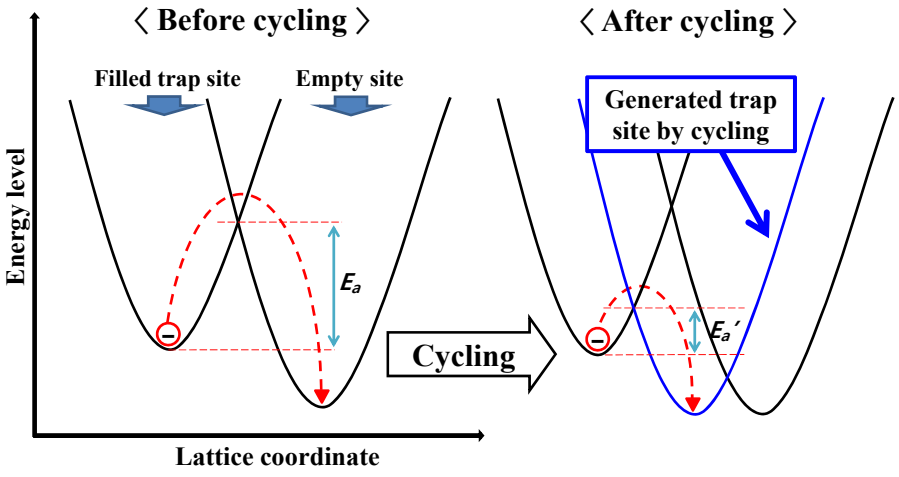


Fig. 3.8. Total energy diagram corresponding to the electron transition from a filled trap site to an empty site. E_a' (after cycling) is lower than E_a (before cycling) because the generation of new traps by cycling causes the average distance between the traps to decrease.

3.4 Summary

Since various failure mechanisms occur together in NAND flash memory, the reliability characteristics does not follow the Arrhenius model. We assumed that the total charge loss (ΔV_{th}) is the superposition of the behavior of several mechanisms. By careful observations across a broad bake temperature range (210ºC ~ 25ºC) and with best fitting, the behavior of each mechanism was obtained. We confirm that each mechanism follows the Arrhenius model well. For the first time, we completely separated three mechanisms and extracted the E_a of each mechanism for different generation and the cycling times in advanced NAND flash memory. By analyzing the extracted E_a values of three generations of NAND cells, it was observed that the E_a of the detrapping mechanism has no dependence, not only on the generation but also on the cycling characteristics, as the change rate of the detrapping probability depends on the baking temperature and not the surface area or the trap density. However, the E_a of the TAT mechanism is dependent on both because the dominant trap energy level and average distance between the traps play important roles in the retention characteristics. The interface trap recovery mechanism has fast recovery characteristics and the activation energy has a very small value of ~ 0.2 eV.

Chapter 4

Mechanism Separation and Analysis of Retention Characteristics in Sub 20-nm NAND Flash Main-Chip

4.1 Introduction

Lifetime of an electric device is defined as estimated retention time at room-temperature (RT), when the amount of charge loss/gain reaches to specific criterion. Apparent activation energy (E_{aa}) is defined as an equivalent net effect of thermal acceleration factor associated with multiple failure mechanisms, which is often used to calculate the lifetime of NANA flash memory using the Arrhenius equation for a given time-to-failure distribution.

Previously, we introduce the proposed charge loss/gain model for NAND flash memory, which is taking into account various failure mechanism in Chapter 2. We also introduce a technique to separate the dominant mechanisms in NAND flash memory cells

in Chapter 3. However, this model should be applicable in the device main-chip in order for the practicality. However, there are lots of parameters in the proposed model, it is difficult to extract them accurately without a detailed guideline.

In this Chapter, we experiment the retention test for sub 20-nm multi-level cell (MLC) NAND flash memory main-chip and observe the abnormal retention behaviors such as E_{aa} roll-off at the PV3 and negative E_{aa} at the ERS. Also, whole detailed procedure of parameter extraction is explained. The parameters are extracted at all states (PV3, PV2, PV1, ERS) and various P/E cycling stress conditions (1k, 2k, 3k, and 5k). We extract the contribution rate (CR) of dominant failure mechanisms at specific criterion of $|\Delta V_{th\_Total}|$ according to the baking temperature. From the results, the abnormal retention behaviors such as E_{aa} roll-off at the PV3 and negative E_{aa} at the ERS states are physically analyzed. In addition to this, the retention behaviors of each failure mechanism are studied in detail according to the probability level of the V_{th} distributions.

4.2 Observation of Abnormal Retention Characteristics in Sub 20-nm NAND Flash Memory Main-Chip

Various failure mechanisms can cause reliability issues, such as the dispersion of the V_{th} distributions due to charge loss/gain [7], [59]. This phenomenon leads to failed bits, which means that the stored data in the NAND flash memory is distorted. The edge states of NAND flash memory, such as PV3 and ERS, are more vulnerable to the reliability issues since a higher electric field at the tunneling oxide layer accelerates charge loss/gain. Therefore, the retention characteristics for the edge states are more intensively analyzed in this section.

Fig. 4.1 shows the retention characteristics for the PV3 and ERS state of 3k-cycled NAND flash memory at various baking temperatures (40 °C, 55 °C, 70 °C, 85 °C, 100 °C, and 125 °C). To reproduce the real on-field use of the devices, the distributed-cycling scheme was applied in this experiment [25]. The red square symbols represent the retention time measured at each of the baking temperatures, and the solid line is that predicted by the Arrhenius model. The star symbols are the predicted lifetimes by the Arrhenius model (black) and the proposed model (red). The lifetime estimated by using the conventional Arrhenius model was extracted by the extrapolating from three points within a high temperature regime (85 °C–125 °C) to RT. The criterion for $|\Delta V_{th\_\mathrm{Total}}|$ is of 0.2 V. The data that were measured do not follow the conventional Arrhenius model, and the gap between the conventional model and the measured data becomes larger as the temperature decreases. The real lifetime is overestimated at PV3 due to the E_a roll-off behavior in the LT regime, and it is underestimated at the ERS due to the negative E_a

behavior in the HT regime. At RT, the difference between the lifetime predicted by the Arrhenius model and the measured lifetime can be greater than a factor of ten. Therefore, a more accurate model based on the actual physical characteristics of the devices should be used in order to calculate the precise lifetimes of NAND flash memory devices.

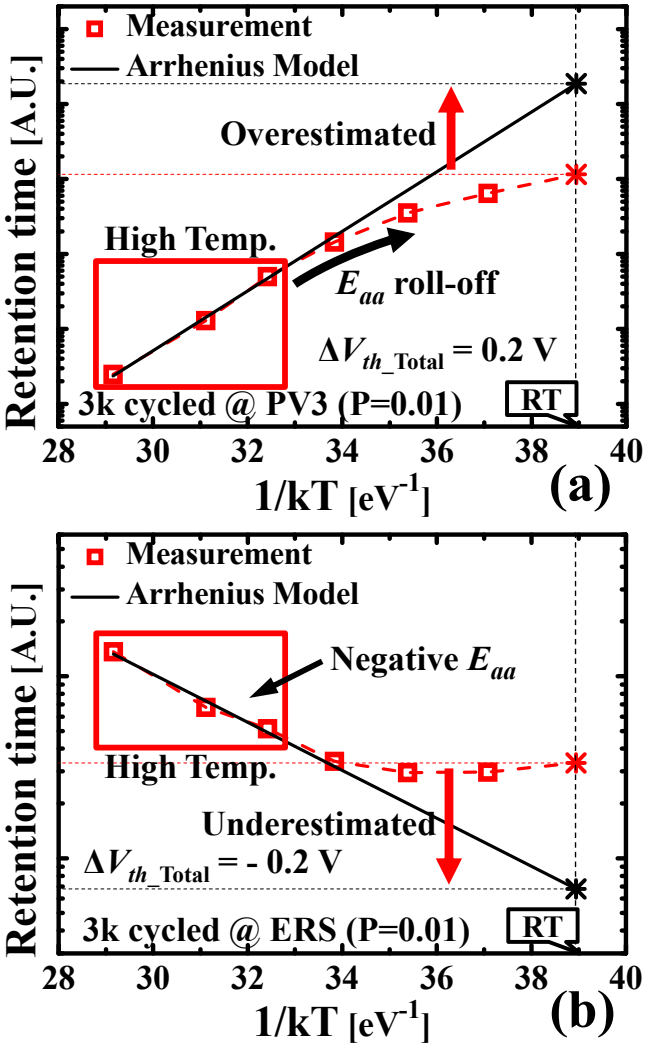


Fig. 4.1. Comparison of the lifetimes estimated by using the conventional Arrhenius model and measured data at the (a) PV3 and (b) ERS state of a 3k-cycled NAND flash memory. The criterion for $|\Delta V_{th\_Total}|$ is 0.2 V. The measured data were extracted at various baking temperatures (40 °C – 125 °C), and the total experimental retention time is of 3024 hours for 40 °C, 55 °C, 70 °C, 85 °C and of 1512 hours for 100 °C and 125 °C

4.3 Parameter Extraction in NAND Main-Chip

There are lots of parameters in the newly proposed model. In order to extract the accurate value for the parameters, plenty of clues in experimental and in literature should be collected as much as possible. In this section, the procedure of parameter extraction is explained step by step.

4.3.1 Parameter Extraction in the PV3 state

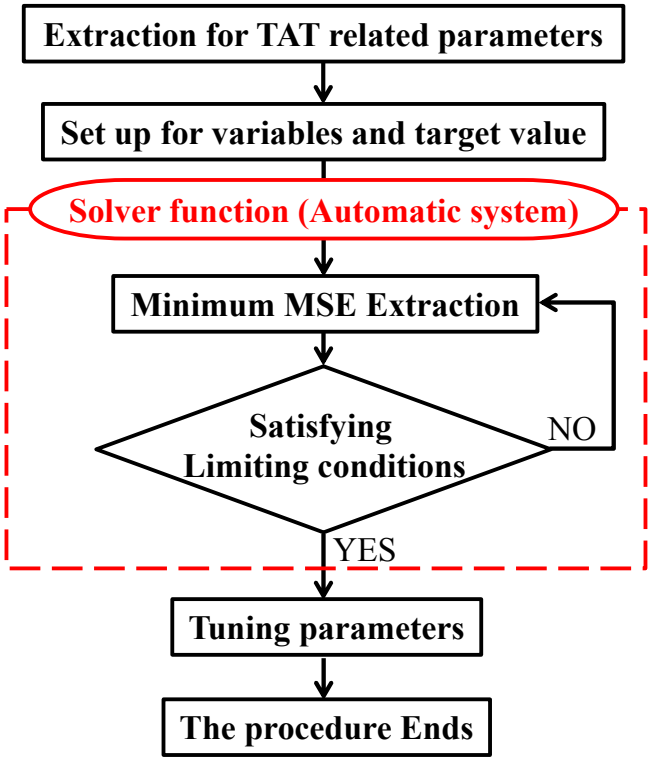


Fig. 4.2. Flow chart for parameters extraction implemented in this work.

Fig. 4.2 shows a flow chart for the parameters extraction implemented in this work. In order to conduct automatic iteration system in red dashed box, solver function in Microsoft Excel 2010 was used. Full details for the procedure are explaining in sequence. Since the extraction for the parameters at the PV3 is relatively easy and accurate, the parameters are firstly extracted at the PV3 state.

A. TAT related Parameter Extraction

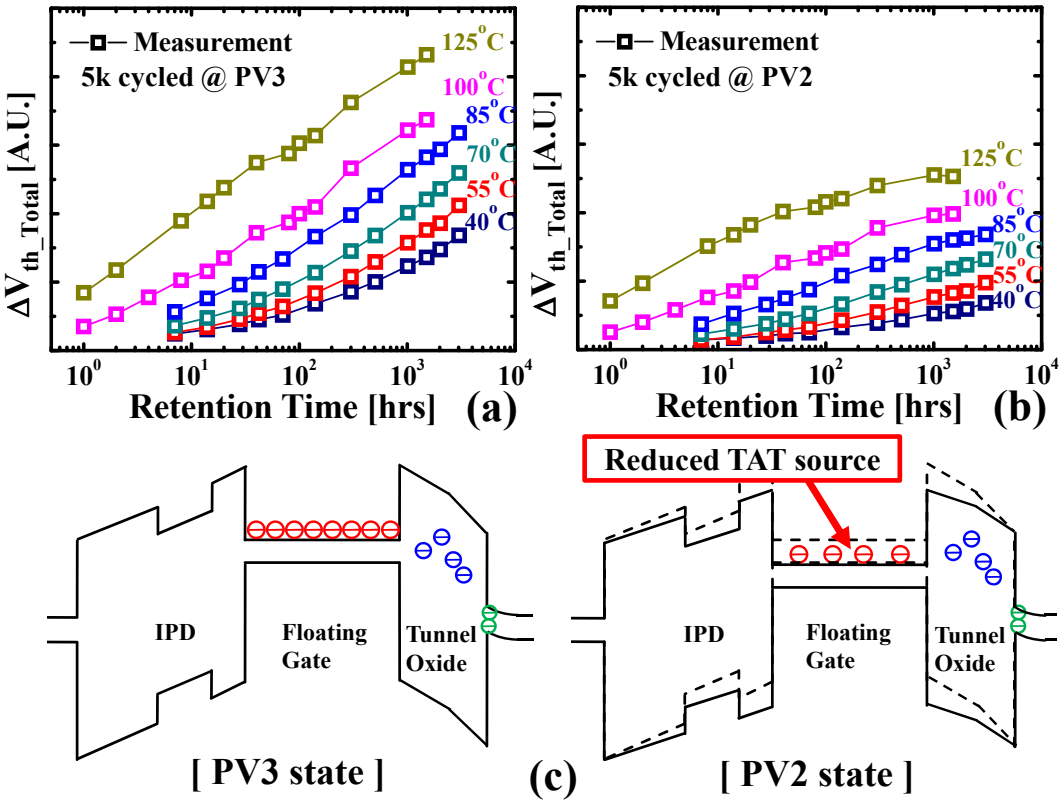


Fig. 4.3. The charge loss characteristics of 5k-cycled NAND flash memory in the (a) PV3 and (b) PV2 states according to baking time at various baking temperatures (40 °C –

125 °C). (c) Schematic of energy band diagrams with charge distribution for PV3 and PV2 states.

Fig. 4.3(a) and (b) show experimentally measured charge loss behaviors of 5k-cycled NAND flash memory in the PV3 and PV2 states according to baking time at various baking temperature (40 °C, 55 °C, 70 °C, 85 °C, 100 °C, and 125 °C). In this paper, all experimentally measured date are extracted at a lower probability level (P=0.01) of the V_{th} cumulative distribution, which is near tail bit regime [25], [58]. Fig. 4.3(c) shows the schematic of energy band diagrams with charge distribution for PV3 and PV2 states. Since the P/E cycling times are exactly the same in both data, the degree of degradation on tunneling oxide layer might be almost the same. However, the amount of the injected electrons in floating-gate has large difference according to the PV state. Therefore, the difference of the charge loss between the PV3 and the PV2 states is dominantly the TAT mechanism component.

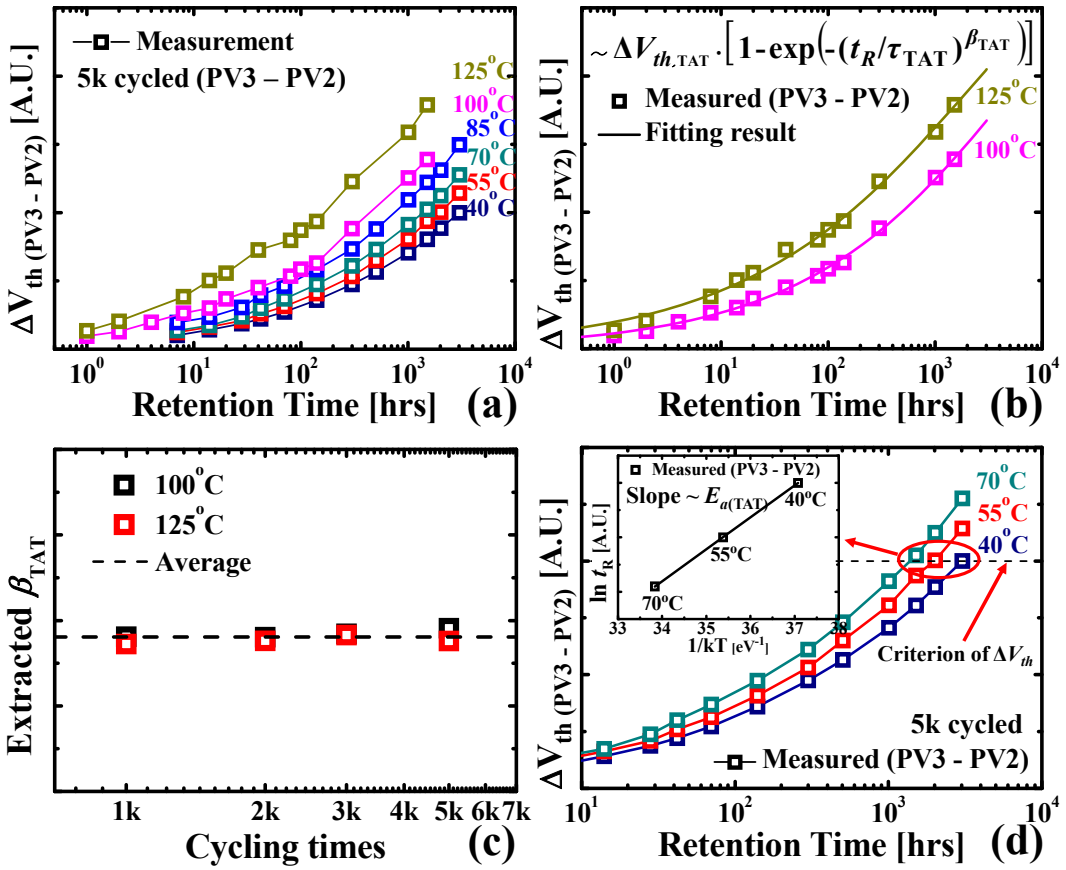


Fig. 4.4. (a) The difference of the charge loss behaviors at PV3 and PV2 states. (b) Parameter extraction of $\tau_{(TAT\_ref@125°C)}$ and β_{TAT} by the best fitting. (c) Parameter of β_{TAT} extraction. (d) Parameter of $E_{a(TAT\_ref)}$ extraction.

Fig. 4.4(a) shows the difference of the charge loss behavior between the PV3 and the PV2 states of 5k-cycled NAND flash memory according to baking time. Since the degree of degradation due to P/E cycling stress on tunneling oxide layer is the same, the detrapping and the N_{it} recovery components should be almost the same. Therefore, the

difference results should be dominantly due to the TAT mechanism. From these results, the parameters related to the TAT mechanism can be inferred. Fig. 4.4(b) shows the best fitting results, which have minimum mean squared error (MSE) value between the difference results and following Eq. (4.1) [66]:

$$\Delta V_{th(\mathrm{PV3-PV2})} \approx \Delta V_{th\_\mathrm{TAT}} \cdot \left[1 - \exp\left(-\left(t_R / \tau_{\mathrm{TAT}}\right)^{\beta_{\mathrm{TAT}}}\right)\right] \tag{4.1}$$

At high-temperature (HT) regime, the amount of charge loss is larger. Therefore, the parameters can be more accurately extracted. Fig. 4.4(c) shows the extracted β_{TAT} values at the HT regime with various P/E cycling conditions. Since the extracted β_{TAT} seems not to be affected by P/E cycling times and baking temperature, we used the average value in all test conditions. Fig. 4.4(d) shows the difference results in Fig. 4.4(a) at low-temperature (LT) regime. In the LT regime, the amount of charge loss source for the TAT mechanism is almost the same. Therefore, activation energy ($E_{a(\mathrm{TAT})}$) can be extracted by the Arrhenius plot at specific criterion of ΔV_{th}. Generally, it is reported that the $E_{a(\mathrm{TAT})}$ value is lower than 0.27 eV [35]-[36]. The result corresponds with the literature. This extracted E_a is defined as a reference activation energy, $E_{a(\mathrm{TAT\_ref})}$. However, the difference of the charge loss has noise components (not pure TAT component), actual $E_{a(\mathrm{TAT})}$ value may not be exactly the same with the $E_{a(\mathrm{TAT\_ref})}$ but similar. Therefore, we assume that the real $E_{a(\mathrm{TAT})}$ value is in the range of [$E_{a(\mathrm{TAT\_ref})}$ ± 10 %]. In the same principle, the extracted $\tau_{(\mathrm{TAT@125°C})}$ in Fig. 4.4(b) is defined as a reference time-constant for the TAT mechanism, $\tau_{(\mathrm{TAT\_ref@125°C})}$. We assume that the real

ln $\tau_{(TAT@125°C)}$ value is in the range of [ln $\tau_{(TAT@125°C)}$ ± 5 %]. The range can be carefully adjusted. However, the amount of calculation increases in wider range, while the solution cannot be found in too narrow range.

B. Additional limiting conditions (PV3 state)

Since the amount of stored electrons in floating-gate is much larger than trapped charge in tunneling oxide layer at the PV3 state, we assume that $\Delta V_{th(TAT)}$ is larger than sum of the other mechanisms' one: [$\Delta V_{th(Nit)} + \Delta V_{th(Detrap)} < \Delta V_{th(TAT)}$]. Since the amount of source for each mechanism at LT regime cannot be larger than the source at HT regime: [$\Delta V_{th(LT)} < \Delta V_{th(HT)}$]. Generally reported E_a value of the detrapping mechanism is 1.0 ~ 1.2 eV [25], [36]-[37]. The origin of this value is under the assumption that the extracted E_{aa} value at HT regime is close to the $E_{a(Detrap)}$ value since the detrapping mechanism is dominant [25], [42]. However, there are the other mechanisms contributing to the charge loss in the HT regime [28], [30], [59]. Also, there is no solution in the range of [$E_{a(Detrap)} > 1.1$ eV], which meets all the limiting conditions. Therefore, we assume that the real $E_{a(Detrap)}$ has the value in the range of [0.7 eV < $E_{a(Detrap)}$ < 1.1 eV], which is slightly lower range. Generally reported E_a value for the N_{it} recovery mechanism is in the range of 0.1 ~ 0.5 eV [30]-[31]. Since the N_{it} recovery mechanism has very short τ and the TAT mechanism has long τ, we assume that $\tau_{Nit@125°C}$ is shorter than 10 hrs and τ of each mechanism should follow this order: [$\tau_{Nit@125°C}$ < 10 hrs], [$\tau_{Nit} < \tau_{Detrap} < \tau_{TAT}$]. The parameter of $\beta_{mecha.}$ has relevance to the degree of variation on the mechanism. The parameter $\beta_{mecha.}$ becomes lower with larger variation. Also, the value of $\beta_{mecha.}$ cannot be larger than 1 during

retention condition, without external bias condition ($0 < \beta_{mecha.} < 1$) [36]. The TAT mechanism can occur with series of more than two traps [32]-[33]. However, the detrapping mechanism can occur with only one trap site [26]. Therefore, the detrapping mechanism should have lower variation than the TAT mechanism: [$\beta_{TAT} < \beta_{Detrap} < 1$]. On the same principle, the N_{it} recovery mechanism also should have lower variation: [$\beta_{TAT} < \beta_{Nit} < 1$]. In Table 4.1, all the limiting conditions for parameter extraction are summarized at the PV3 state.

Fig. 4.5(a) shows the measured retention behavior of the 5k-cycled NAND flash memory in the PV3 state with a baking time of up to 1512 hrs at 125 ºC (symbols). The solid line is the best fitting result using the proposed superposition model. The blue, red, and green of dashed lines represent the charge loss characteristic of the detrapping, the TAT, and the N_{it} recovery mechanism according to the baking time, respectively [56]-[62]. Fig. 4.5(a), (b), and (c) show the separated charge loss characteristics of the detrapping mechanism, the interface trap recovery mechanism, and the TAT mechanism according to baking time at various baking temperatures (40ºC, 55ºC, 70ºC, 85ºC, 100ºC, 125ºC) [56]-[57]. It is clearly observed that each τ is shorter and the amplitude of the final value of ΔV_{th} is larger at a higher baking temperature, as the reaction rate of each failure mechanism is higher and because the amount of the reaction source is greater. The results also show that the temperature dependence of the detrapping mechanism is strong and the TAT mechanism is weak relatively.

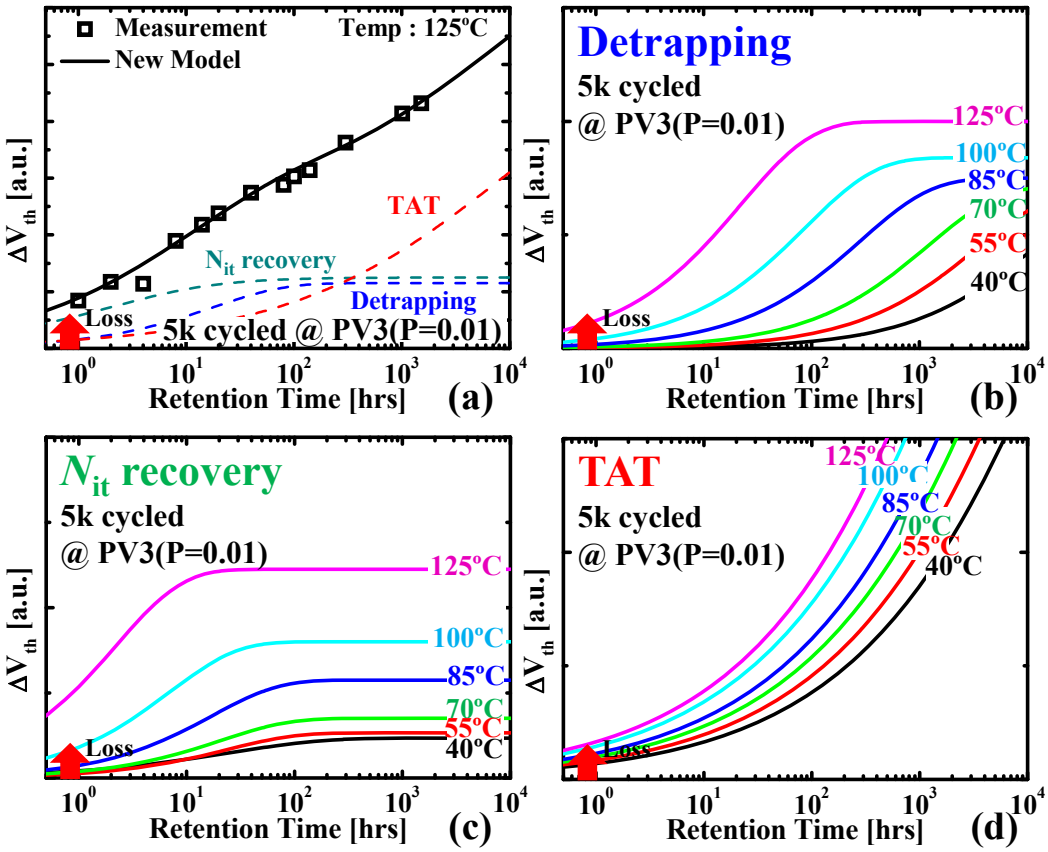


Fig. 4.5. (a) The charge loss behavior and best fitting results with the new model for the PV3 state of 5k-cycled NAND flash memory at 125 °C. The retention characteristics of (b) the detrapping mechanism, (c) the interface trap recovery mechanism, and (d) the TAT mechanism according to baking time at various baking temperature conditions (40ºC ~ 125ºC).

TABLE 4.1

SUMMARY OF LIMITING CONDITIONS

FOR PARAMETER EXTRACTION AT THE PV3 STATE.

- [$E_{a(\mathrm{TAT})} \sim E_{a(\mathrm{TAT\ ref})} \pm 10\ \%$]
- [$0.7\ \mathrm{eV} < E_{a(\mathrm{Detrap})} < 1.1\ \mathrm{eV}$]
- [$0.1\ \mathrm{eV} < E_{a(\mathrm{Nit})} < 0.5\ \mathrm{eV}$]
- [$\beta_{\mathrm{TAT}} < \beta_{\mathrm{Detrap}} < 1$]
- [$\beta_{\mathrm{TAT}} < \beta_{\mathrm{Nit}} < 1$]
- [$\beta_{\mathrm{Detrap}(125\ ^{\circ}\mathrm{C})} = \beta_{\mathrm{Detrap}(100\ ^{\circ}\mathrm{C})} = \beta_{\mathrm{Detrap}(85\ ^{\circ}\mathrm{C})} \cdots$]
- [$\beta_{N\mathrm{it}(125\ ^{\circ}\mathrm{C})} = \beta_{N\mathrm{it}(100\ ^{\circ}\mathrm{C})} = \beta_{N\mathrm{it}(85\ ^{\circ}\mathrm{C})} \cdots$]
- [$\Delta V_{th(N\mathrm{it})} + \Delta V_{th(\mathrm{Detrap})} < \Delta V_{th(\mathrm{TAT})}$]
- [$\Delta V_{th(\mathrm{LT})} \leq \Delta V_{th(\mathrm{HT})}$]
- [$\ln \tau_{(\mathrm{HT})} \leq \ln \tau_{(\mathrm{LT})}$]
- [$\ln \tau_{(\mathrm{TAT@125^{\circ}C})} \sim \ln \tau_{(\mathrm{TAT\_ref@125^{\circ}C})} \pm 5\ \%$]
- [$\tau_{N\mathrm{it}} < \tau_{\mathrm{Detrap}} < \tau_{\mathrm{TAT}}$]
- [$\tau_{N\mathrm{it}@125^{\circ}\mathrm{C}} < 10\ \mathrm{hrs}$]

C. Set-up for Parameters Extraction

The total charge loss behavior does not follow simple curve due to coexistence of all dominant mechanisms, which can be modeled by Eq. (2.12) [59]-[62]. There are errors between Eq. (2.12) and experimentally measured charge loss data [Fig. 4.3(a)]. Total error between the model and data can be obtained by summation of all mean squared error (MSE) values [59]-[62], [66]:

$$\text{Total Error} = \sum_{\text{Bake Temp.}} \text{Error},$$

$$\text{Error} = \sum_{\text{Bake Time}} \left(\text{New Model} - \text{Measured data}\big|_{\text{bake time}}\right)^2 \tag{4.2}$$

Satisfying the minimum total error is necessary condition for exact parameters extraction. Using various tools such as the solver function in EXCEL 2010, the optimized parameters with minimum total error can be extracted. Even though the total error reaches to the minimum value, it would be incorrect result if the parameters do not meet the physical limiting conditions [see Table 4.1]. The solver function automatically finds out the optimized parameters with satisfying the minimum total error, which correspond to all the limiting conditions through automatic iterating system.

In order to reduce the number of variable parameters and find the parameters easily, only E_a and $\tau_{(125^oC)}$ of each mechanism are set as variable and the other τ are automatically calculated by following Arrhenius equation [36], [49], [67]-[68]:

$$\tau_{\text{LT}} = \tau_{125^\circ\text{C}} \cdot \left[E_a \left(1/kT_{\text{LT}} - 1/kT_{125^\circ\text{C}}\right)\right] \tag{4.3}$$

Since our previous results show that τ characteristic of each mechanism according to baking temperature follows the Arrhenius law well, this assumption is reasonable [56]-[59]. The solver function automatically finds the parameter values. If the initial value of E_a is too large, the τ at the LT regime becomes exponentially larger and the $\Delta V_{th(\text{LT})}$ should be larger, too. However, the limiting condition, $[\Delta V_{th(\text{LT})} < \Delta V_{th(\text{HT})}]$, makes

larger error at LT regime. Contrastively, when the E_a is too small, the value of $\tau_{(LT)}$ and $\Delta V_{th(LT)}$ become small. Therefore, the charge loss behavior gets saturated and then the error at latter part on baking time becomes larger. Since there are a lot of physical limiting conditions, the optimized unique solution can be extracted. After this stage, cut off the Arrhenius relationship between each $\tau_{(LT)}$ and E_a. And then, each τ and ΔV_{th} can be slightly tuned for more accurate parameters.

4.3.2 Parameter Extraction in the Other state

In order to extract the parameters for the other states, the results at the PV3 state should be referred, because the extraction for the parameters at the PV3 is relatively easy and accurate. Therefore, the parameter extraction for the state should be descending order: [PV3 → PV2 → PV1 → ERS]. We assume that the β values of each mechanism are all the same regardless of the state: [$\beta_{mecha.(PV3)} = \beta_{mecha.(PV2)} = \beta_{mecha.(PV1)} = \beta_{mecha.(ERS)}$]. Also, we assume that E_a of each mechanism in the neighbor state is not abruptly changed and is in the range of [$E_{a(\text{neighbor state})} \pm 0.1$ eV]. In the same principle, we assume that the τ of each mechanism between neighbor states has the similar value and it has in the range of [ln $\tau_{(\text{neighbor state})} \pm 5$ %]. Finally, since the degradation on the tunneling oxide layer is the same due to the same number of P/E cycling times induced, the amount of source for the detrapping and N_{it} recovery mechanism is almost the same. In Table 4.2, all the limiting conditions for parameter extraction at the other states are summarized.

TABLE 4.2

SUMMARY OF LIMITING CONDITIONS

FOR PARAMETER EXTRACTION AT THE OTHER STATES (PV2, PV1, ERS).

- PV3 → PV2 → PV1 → ERS
- [$\beta_{\mathrm{TAT(PV3)}} = \beta_{\mathrm{TAT(PV2)}} = \beta_{\mathrm{TAT(PV1)}} = \beta_{\mathrm{TAT(ERS)}}$]
- [$\beta_{\mathrm{Detrap(PV3)}} = \beta_{\mathrm{Detrap(PV2)}} = \beta_{\mathrm{Detrap(PV1)}} = \beta_{\mathrm{Detrap(ERS)}}$]
- [$\beta_{N\mathrm{it(PV3)}} = \beta_{N\mathrm{it(PV2)}} = \beta_{N\mathrm{it(PV1)}} = \beta_{N\mathrm{it(ERS)}}$]
- [$E_{a(\mathrm{mechanism@PV2})} \sim E_{a(\mathrm{mechanism@PV3})} \pm 0.1$ eV]
- [$E_{a(\mathrm{mechanism@PV1})} \sim E_{a(\mathrm{mechanism@PV2})} \pm 0.1$ eV]
- [$E_{a(\mathrm{mechanism@ERS})} \sim E_{a(\mathrm{mechanism@PV1})} \pm 0.1$ eV]
- [$\ln \tau_{(\mathrm{mechanism@PV2})} \sim \ln \tau_{(\mathrm{mechanism@PV3})} \pm 5\ \%$]
- [$\ln \tau_{(\mathrm{mechanism@PV1})} \sim \ln \tau_{(\mathrm{mechanism@PV2})} \pm 5\ \%$]
- [$\ln \tau_{(\mathrm{mechanism@ERS})} \sim \ln \tau_{(\mathrm{mechanism@PV1})} \pm 5\ \%$]
- [$\Delta V_{th(\mathrm{Detrap@PV2})} \leq \Delta V_{th(\mathrm{Detrap@PV3})}$]
  ($\Delta V_{th(\mathrm{Detrap@PV2})} \sim \Delta V_{th(\mathrm{Detrap@PV3})}$)
- [$\Delta V_{th(\mathrm{Detrap@PV1})} \leq \Delta V_{th(\mathrm{Detrap@PV2})}$]
  ($\Delta V_{th(\mathrm{Detrap@PV1})} \sim \Delta V_{th(\mathrm{Detrap@PV2})}$)
- [$\Delta V_{th(\mathrm{Detrap@ERS})} \leq \Delta V_{th(\mathrm{Detrap@PV1})}$]
  ($\Delta V_{th(\mathrm{Detrap@ERS})} \sim \Delta V_{th(\mathrm{Detrap@PV1})}$)
- [$\Delta V_{th(N\mathrm{it@PV3})} \sim \Delta V_{th(N\mathrm{it@PV2})} \sim \Delta V_{th(N\mathrm{it@PV1})} \sim \Delta V_{th(N\mathrm{it@ERS})}$]

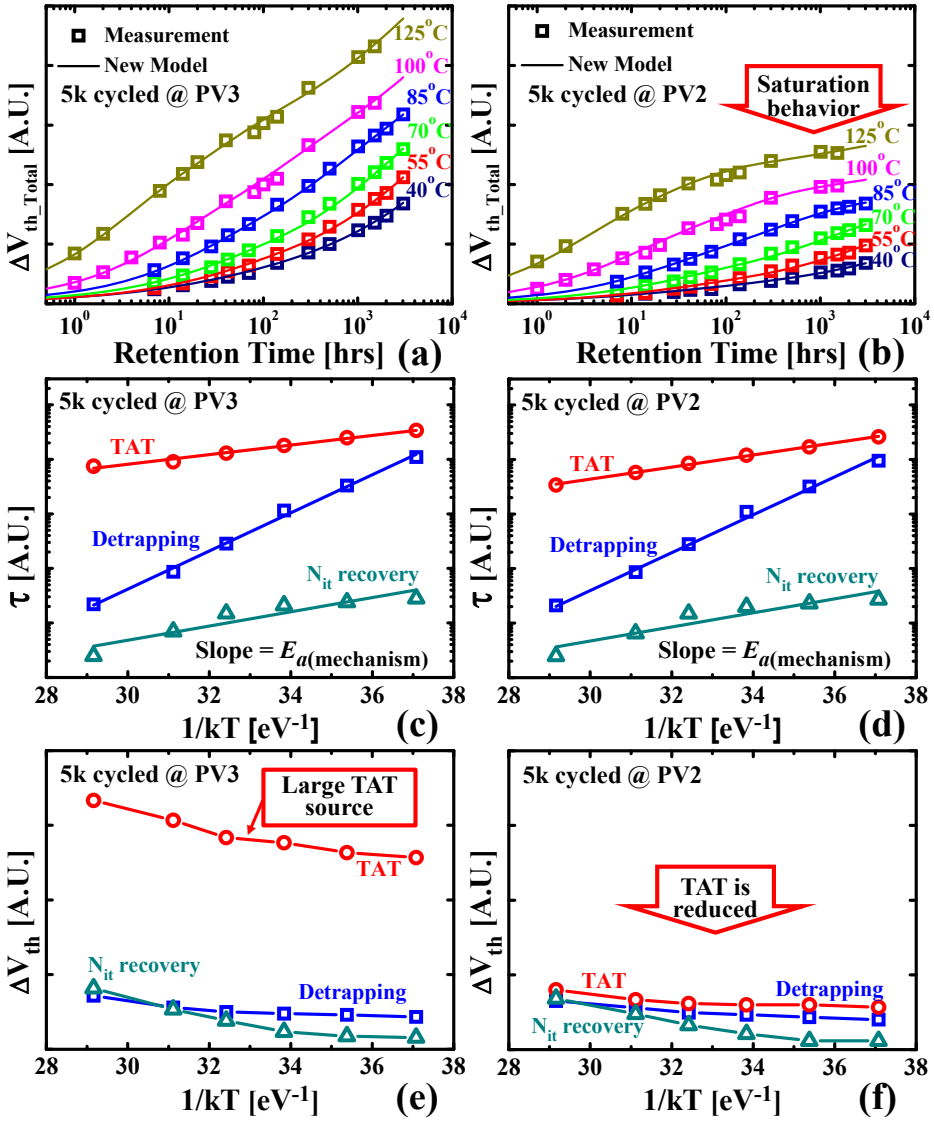


Fig. 4.6. The charge loss behavior and best fitting results with the new model for 5k-cycled NAND flash memory at (a) PV3 and (b) PV2 states according to baking time at various baking temperatures (40 °C – 125 °C). τ behavior for each mechanism at (c) PV3 and (d) PV2 states on baking temperatures. Final ΔV_{th} extracted for each mechanism at (e) PV3 and (f) PV2 states.

Fig. 4.6 shows the results of parameters extraction for 5k-cycled NAND flash memory at the PV3 and PV2 states. In Fig. 4.6(a) and (b), the symbols are the experimental charge loss results from retention test at various baking temperatures (40 °C – 125 °C) and the lines are the results for the best fitting by the proposed superposition model at the PV3 and PV2 states, respectively. The charge loss characteristics in the PV2 show saturation behavior in the latter part, while the charge loss behaviors in the early part are similar between the PV3 and PV2 states. Fig. 4.6(c) and (d) show the τ characteristics for each mechanism according to baking temperature at the PV3 and PV2 states, respectively. Each mechanism follows the Arrhenius law well. The slope of each τ behavior, E_a of each mechanism, has similar value regardless of the state. Fig. 4.6(e) and (f) show the final ΔV_{th} amplitude for each dominant failure mechanism according to baking temperature at the PV3 and PV2 states, respectively. The amount of charge loss source for the detrapping and the N_{it} recovery mechanisms is similar behavior. These results are due to the same degradation on the tunneling oxide layer by P/E cycling stress. However, the source of the TAT mechanism is much reduced at the PV2 state because much less electrons are injected into the floating-gate at lower state. Since the TAT has the longest τ among dominant mechanisms, it dominantly determines the charge loss behavior in the latter part [see Fig. 4.6(b)]. Therefore, the main difference of the charge loss between the PV3 and the PV2 states is dominantly due to the TAT mechanism component. The results of extracted parameters give a good physical explanation for the retention characteristics of NAND flash memory.

4.4 Analysis of Retention Characteristics

Various failure mechanisms can cause reliability issues, such as the dispersion of the V_{th} distributions due to charge loss/gain [7], [59]. This phenomenon leads to failed bits, which means that the stored data in the NAND flash memory is distorted. In this section, intensive analysis of retention characteristics are conducted in detail

4.4.1 P/E Cycling times and State Dependence

The contribution rate (CR) of dominant mechanisms varies with the retention condition. Also, it provides the physical reason for the abnormal retention behaviors. In this section, we analyze the retention behavior for each mechanism according to the P/E cycling times and states in detail.

In Fig. 4.7, the symbols are the measured charge loss behavior of 3k-cycled NAND flash memory in the PV3 state with a baking time of up to 3024 hours at 85 °C. The solid line is the result for the best fitting using the proposed superposition model by the solver function in Microsoft EXCEL 2010, introduced in section 4.3. The blue, red, and green of dashed lines represent the charge loss characteristic of the detrapping, the TAT, and the N_{it} recovery mechanism according to the baking time, respectively [59],[61]-[62]. The inset shows the percent contributions of the three dominant failure mechanisms at specific criterion of $\Delta V_{th\_\mathrm{Total}}$. The sum of contribution rates for all mechanisms is 100 %, which corresponds to the specific criterion of $\Delta V_{th\_\mathrm{Total}}$. Even though the amount of the TAT source is much larger than that of the N_{it} recovery source ($\Delta V_{th(\mathrm{TAT})} > \Delta V_{th(\mathrm{Nit})}$), the contribution rates for both mechanisms show very similar level. This result is due to the τ

difference of both mechanisms. The fast mechanism can make large contribution on the charge loss at specific criterion of ΔV_{th_Total}, even if the final ΔV_{th} for the mechanism is small. Since the contribution rate of each mechanism directly influences on the retention time, it is also important to analyze the contribution rate for deep understanding on the abnormal retention characteristics of NAND flash memory.

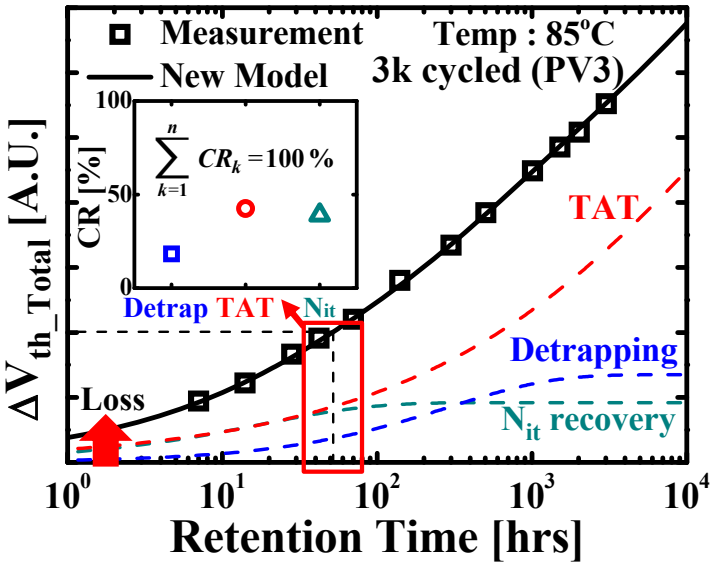


Fig. 4.7 Retention behavior of the 3k-cycled NAND flash memory in the PV3 state with a baking time of up to 3024 hrs at 85 ºC. The total charge loss is the superposition of the various mechanisms. The inset shows the extracted contribution rate (CR) of each mechanism at a specific criterion of ΔV_{th_Total}.

A. Analysis of Retention Characteristics for the PV3 state

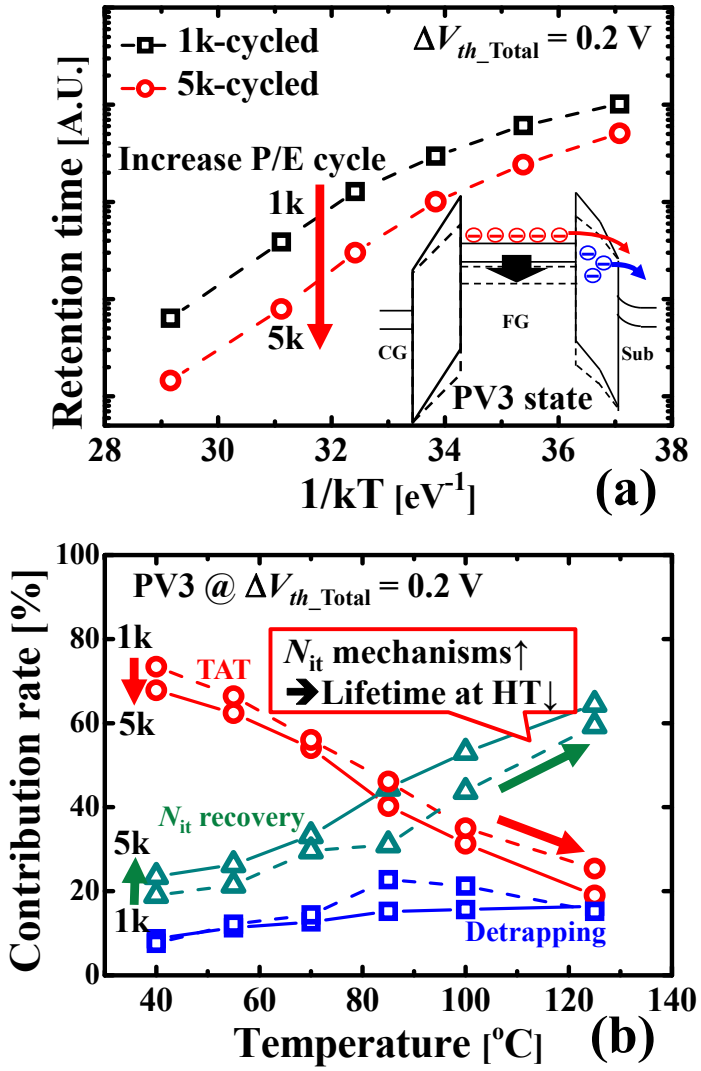


Fig. 4.8. (a) Retention time characteristics for the PV3 state of the NAND flash memory for all baking temperatures. The criterion for ΔV_{th_Total} is of 0.2 V. The insert schematically show the band diagram for the PV3 state. (b) The contribution rate of each failure mechanism to the criterion of ΔV_{th_Total}.

Fig. 4.8(a) shows the characteristics of the retention time for the PV3 state of the NAND flash memory at all baking temperatures. The criterion for $\Delta V_{th\_\mathrm{Total}}$ is 0.2 V. The retention time is observed to become shorter as the baking temperature or the cycling times increase. The insert schematically show the band diagram for the PV3 state. In this condition, all mechanisms contribute to the charge loss. Fig. 4.8(b) shows the percent contributions of the three dominant failure mechanisms on the criterion of $\Delta V_{th\_\mathrm{Total}}$ in the PV3 state of NAND flash memory according to the baking temperature. $|\Delta V_{th\_\mathrm{Total}}|$ corresponds to the left-hand side of Eq. (2.12), and the portion of each mechanism corresponds to each term in the right-hand side of Eq. (2.12). Even though the final ΔV_{th} of the TAT mechanism is overwhelmingly larger [see Fig. 4.6(e)], its contribution rate is not large enough, especially in the HT regime [see Fig. 4.8(b)]. This phenomenon is a result of the TAT mechanism having a fairly larger τ than the other mechanisms, and the difference in τ becomes larger as the baking temperature increases [see Fig. 4.6(c)].

Fig. 4.8(b) explains the E_a roll-off behavior in terms of the retention characteristics in the PV3 state, as shown in Fig. 4.1(a). In the LT regime, the contribution rate of the TAT mechanism is dominant among all other mechanisms. Since the TAT mechanism has weak dependence on temperature, low apparent E_a characteristics are observed [36]. However, the fast mechanisms, such as the N_{it} recovery, become dominant as the temperature increases [28], [30]. As a result of this physical phenomenon, the retention time becomes shorter quite rapidly and has a stronger dependence on temperature as the temperature increases. Therefore, the E_a roll-off behavior is relevant to the retention

characteristics. As the cycling times increase, more N_{it} traps are generated, so the contribution rate of the fast mechanism becomes larger. Therefore, the retention time becomes shorter over all baking temperature regimes.

B. Analysis of Retention Characteristics for the ERS state

The charge loss in the ERS state has complex behavior due to the coexistence of the charge loss and charge gain mechanisms. Fig. 4.9 shows the retention behavior of the ERS state of 0.1k- and 5k-cycled NAND flash memory with the baking time up to 1008 hrs at various baking temperatures (40 ºC ~ 125 ºC). All the data in this paper were extracted at lower probability level (P = 0.01) of the V_{th} cumulative distribution in the ERS state. Lower P level is near the valley between the ERS state and the lowest PV (PV1) state. In Fig. 4.9(a), the retention characteristics of 0.1k-cycled data shows larger charge gain at higher baking temperature. However, the result in Fig. 4.9(b) shows opposite trend as increasing the cycling times. It means that the retention time (t_R) becomes longer at higher temperature regime as increasing the cycling times. It indicates that the retention time (t_R) becomes longer at higher temperature regime for increased cycling times. It is opposite trend with the behavior in PV states.

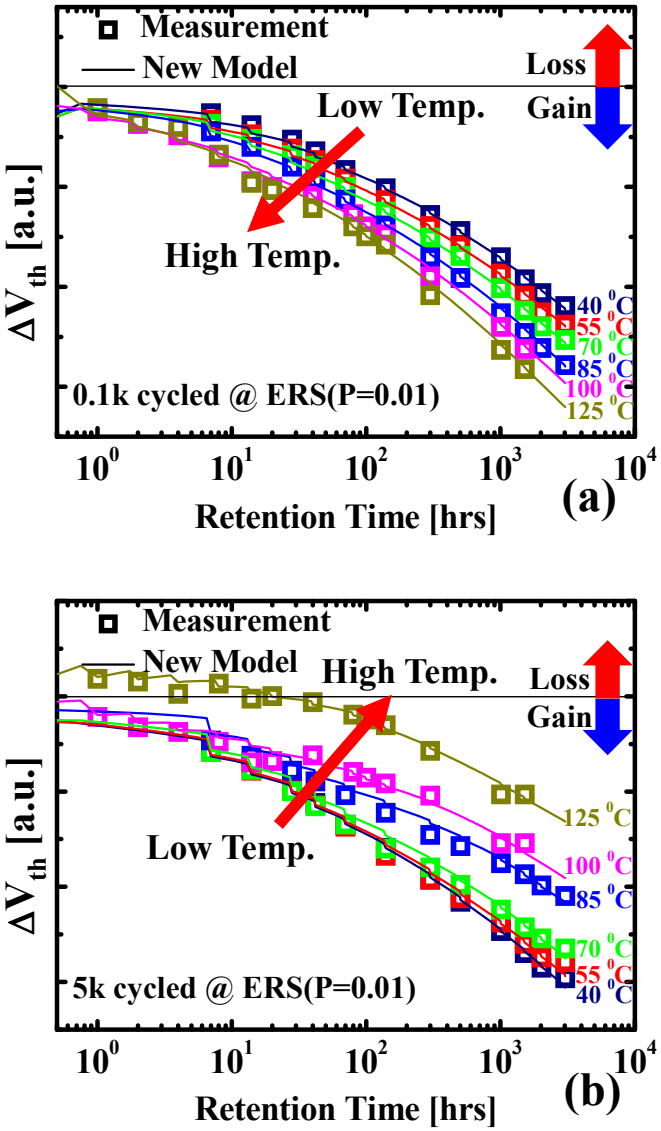


Fig. 4.9. The retention data at the ERS state of (a) 0.1k-cycled and (b) 5k-cycled NAND Flash memory with baking time up to 1008 hrs at various baking temperatures (40 ºC ~ 125 ºC).

Fig. 4.10(a) shows the retention time characteristics of the NAND flash memory in the ERS state for all baking temperatures. The criterion for $|\Delta V_{th\_Total}|$ is 0.2 V. In the ERS state, the retention characteristics are much more complicated. The retention time for 1k-cycled data becomes shorter as the baking temperature increases. However, the retention time for the 5k-cycled memory exhibits the opposite trend [59]. In addition, the retention time becomes longer as the cycling times increase, especially in the HT regime. The insert schematically show the band diagram for the ERS state. In this condition, the TAT mechanism contributes to the charge gain since the negative electric field at the tunneling oxide layer made in the opposite direction, while the N_{it} recovery and the detrapping mechanism still contribute to the charge loss [59]. Fig. 4.10(b) shows these phenomena well. The contribution rate of the TAT mechanisms is larger than 100% due to the cancellation effect, and the P/E cycling stress induces degradation in the tunneling oxide layer, so the source of N_{it} recovery and detrapping becomes larger. In addition, more detrapping electrons are injected into the floating-gate, increasing the energy level of the floating-gate particularly in the HT regime. This behavior reduces the strength of the electric field at tunneling oxide and suppresses the TAT mechanism. In order to achieve the criterion for $|\Delta V_{th\_Total}|$, the TAT mechanism should be generated further, as shown in Fig. 4.10(b). Therefore, the retention time for large-cycled data can be longer at HT, and this phenomenon explains the negative E_a behavior.

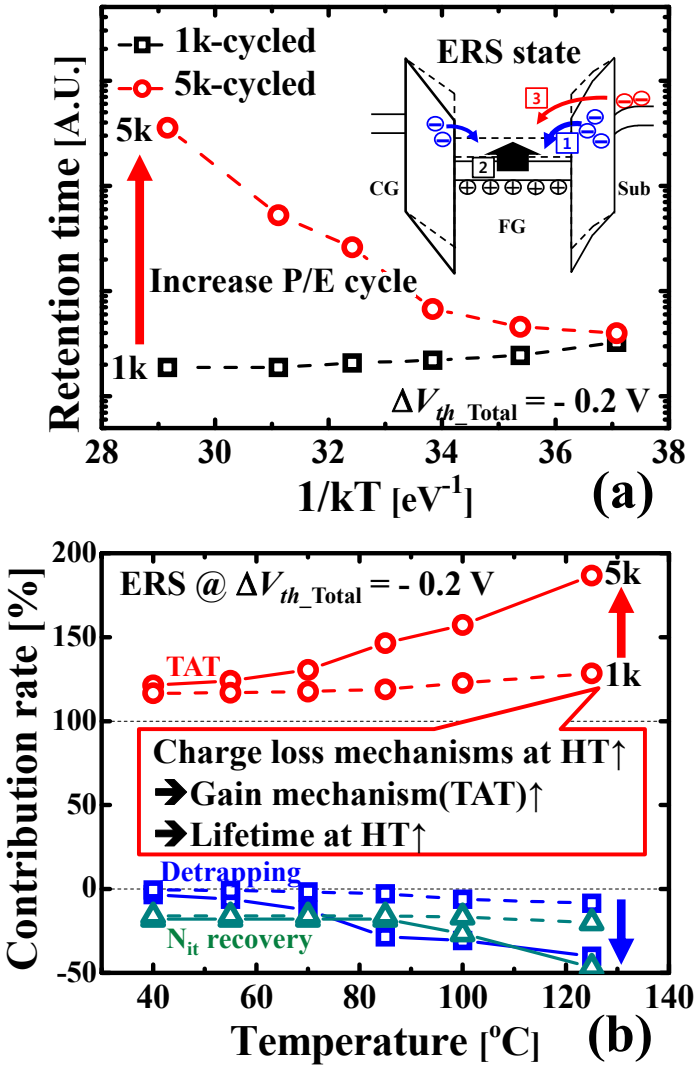


Fig. 4.10. (a) Retention time characteristics for the ERS state of the P/E-cycled NAND flash memory for all baking temperatures. The criterion for $|\Delta V_{th\_Total}|$ is 0.2 V. The insert schematically show the band diagram for the ERS state. (b) The portion of each failure mechanism contributing to the criterion of ΔV_{th_Total}.

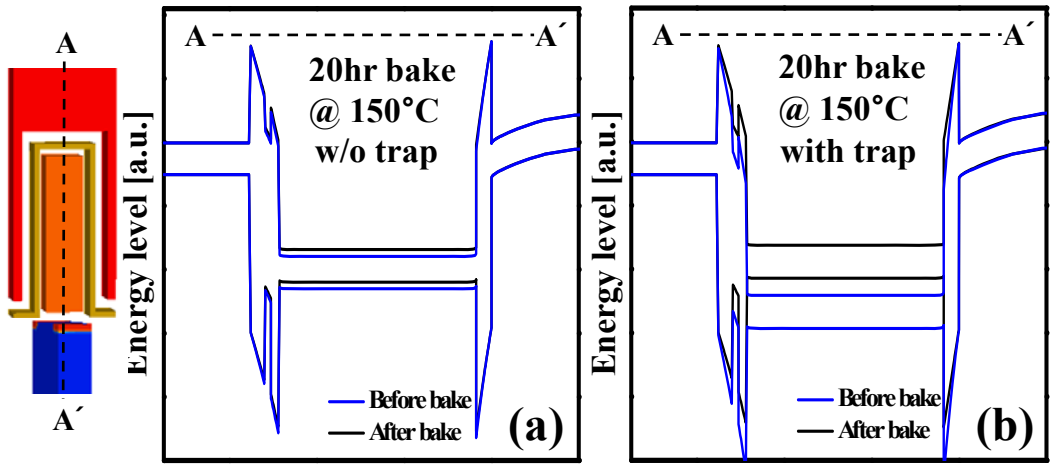


Fig. 4.11. The simulation results show the energy level of FG in a direction A to A' of the cell (b) with trap in tunneling oxide layer increases more than the cell (a) without trap after 20 hrs bake at 150 ºC. The initial V_{th} is set to -2 V. The detrapping mechanism increases the energy barrier larger and reduces the electric field at the tunneling oxide layer.

Fig 4.11 shows the technology computer aided design (TCAD) device simulation results that the energy level of FG of NAND Flash cell in a direction A to A' with trap in tunneling layer increases more than the cell without trap after 20 hrs bake at 150 ºC. The initial V_{th} is set to -2 V at TCAD device simulation. The detrapping component raises the energy barrier FG and reduces the electric field at the tunneling oxide layer. The simulation results show good agreement with the result in Fig. 4.10.

C. TAT mechanism vs. Detrapping mechanism

In this section, analysis of the TAT mechanism is conducted in detail in extremely scaled NAND flash memory. It is observed that the final ΔV_{th} of the TAT mechanism increases according to the baking temperature, while the detrapping mechanism has almost constant behavior. We also extract the E_a for the TAT mechanism in various conditions and compare with the E_a of the detrapping mechanism. As a result, we deeply understand the retention behavior for the TAT mechanism especially in trap-density and electric field dependence.

In Fig. 4.12(a), the symbols show the time-constant (τ) behaviors for the detrapping and the TAT mechanisms according to the baking temperature extracted at the PV3 state of 3k-cycled NAND flash memory. Procedure of the parameter extraction is explained in detail in ref [61]. The τ behavior between high-temperature (HT) and low-temperature (LT) follows the Arrhenius relation, $\tau_{k(\mathrm{LT})} = \tau_{k(\mathrm{HT})} \cdot \exp[E_{ak}(1/kT_{\mathrm{LT}} - 1/\mathrm{kT_{HT}})]$, which are expressed as lines. The slope of τ in log-time over 1/kT is corresponding to each mechanism's E_a. Fig. 4.12(b) shows the final ΔV_{th} behavior for the detrapping and the TAT mechanisms with baking temperature. In the final ΔV_{th} characteristics, the source of the TAT mechanism is much larger than that of the detrapping mechanism. It means that the TAT mechanism makes much more contribution to the charge loss in the long term. Therefore, the investigation on the TAT mechanism is great important to understand the retention characteristics of NAND flash memory. The amount of the final ΔV_{th} for the TAT mechanism increases with the baking temperature, while the detrapping mechanism has almost constant behavior.

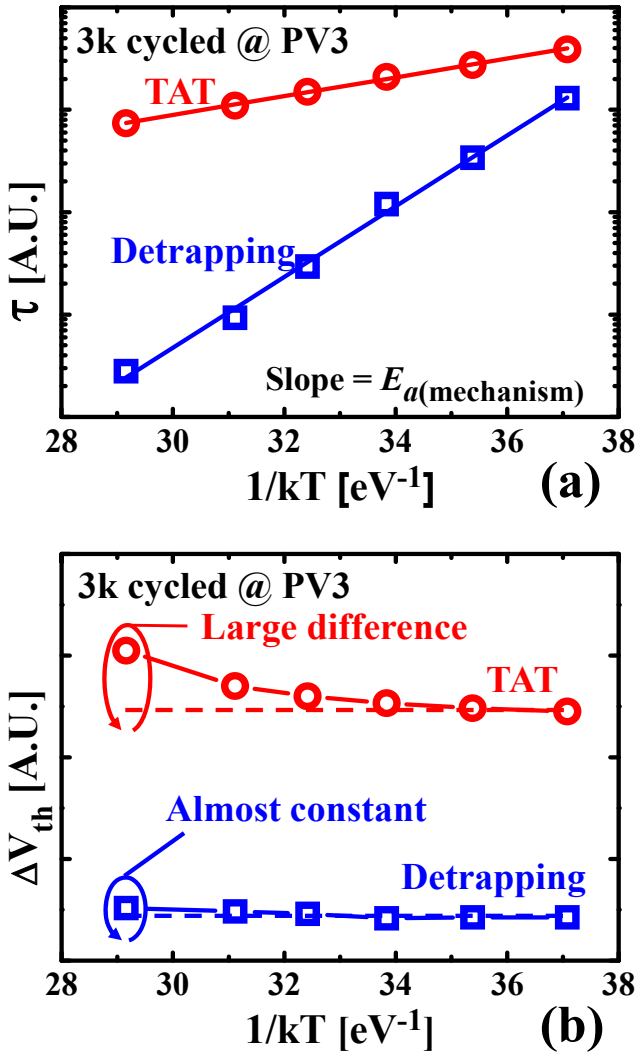
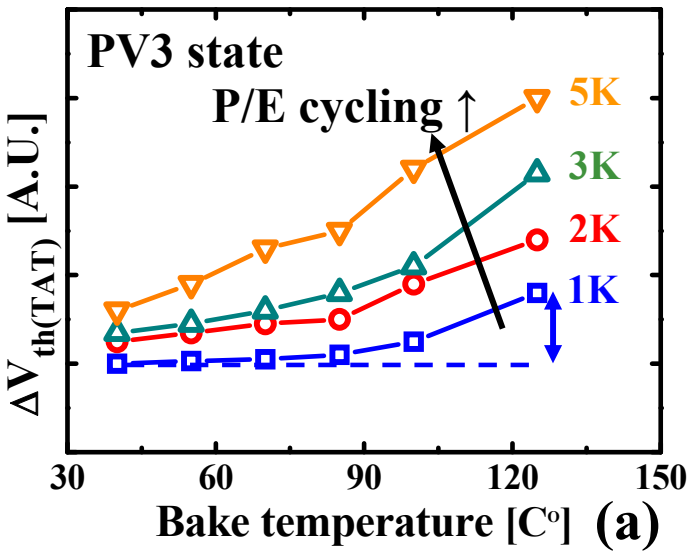


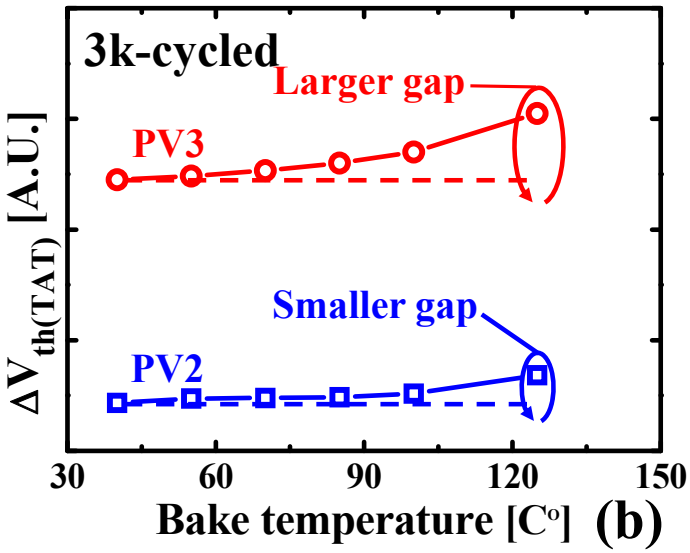
Fig. 4.12. (a) τ behavior and (b) the amplitude of final ΔV_{th} for the detrapping and the TAT mechanisms with baking temperature (40 °C–125 °C) extracted at the PV3 state of 3k-cycled NAND flash memory. Each mechanism follows the Arrhenius law well. The final ΔV_{th} of the TAT mechanism increases with temperature, while the detrapping mechanism has almost constant behavior.

Fig. 4.13(a) shows the P/E cycling stress dependence on the final ΔV_{th} behavior of the TAT mechanisms according to the baking temperature, extracted at the PV3 state of NAND flash memory. The source of the TAT mechanism is larger with P/E cycling times and this trend is much larger in HT regime. Since P/E cycling stress generates traps in tunneling oxide layer and at/near SiO_2-Si interface, the device with larger P/E cycling stress might have higher trap-density [57].

Fig. 4.13(b) shows the PV states dependence on the final ΔV_{th} of the TAT mechanisms according to the temperature, extracted at 3k-cycled NAND flash memory. Since the P/E cycling times are exactly the same in both data, the degree of degradation on tunneling oxide layer might be almost the same. However, the amount of the injected electrons in floating-gate is much larger in the PV3 than in the PV2. Therefore, the source of the TAT in the PV3 is much larger than the source in the PV2 state [61]. This trend (larger source with temperature) is much obvious in the PV3 state. Main different condition between the PV3 and the PV2 states is the strength of electric field in tunneling oxide layer [43].

Fig. 4.13(c) exhibits the difference value of final ΔV_{th} for the TAT mechanism between extracted at 125 °C and at 40 °C ($\Delta V_{th(125\,°C)} - \Delta V_{th(40\,°C)}$) in various P/E cycling times and the PV states. The difference value becomes larger with P/E cycling times and with higher PV state. The P/E cycling stress induces higher trap density in the tunneling oxide layer [43], [57]. Also, the intensity of electric filed increases in the tunneling oxide as the PV state is higher. Therefore, the results obviously show that the temperature dependence of the difference value is mainly affected by both the trap density and the strength of electric field in tunneling oxide layer.


PV3 state
P/E cycling ↑
5K
3K
2K
1K
ΔV th(TAT) [A.U.]
30
60
90
120
150
Bake temperature [Co]
(a)


3k-cycled
Larger gap
PV3
Smaller gap
PV2
ΔV th(TAT) [A.U.]
30
60
90
120
150
Bake temperature [Co]
(b)

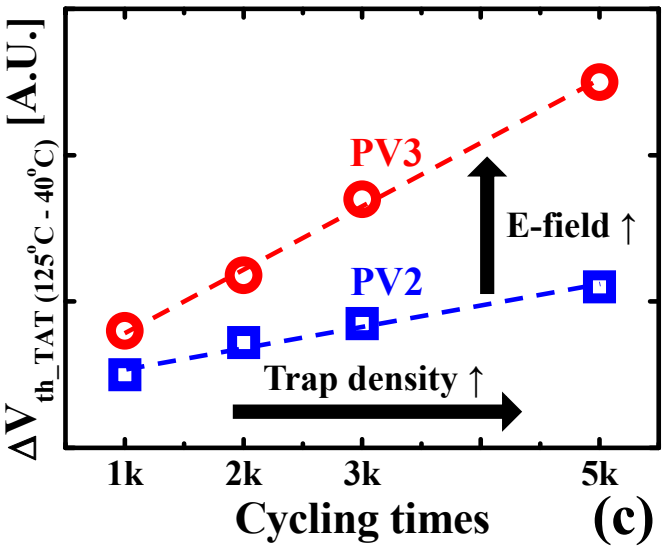


Fig. 4.13. The final ΔV_{th} behavior for the TAT mechanism with baking temperature according to (a) P/E cycling times and (b) program states. (c) The difference of final ΔV_{th} for the TAT mechanism between extracted at 125 °C and at 40 °C according to P/E cycling times. The difference value increase with P/E cycling times and with higher PV state.

Fig. 4.14. show the extracted E_a values of the TAT and the detrapping mechanisms at the PV3 and the PV2 states according to P/E cycling times (1k ~ 5k times). The E_a of the both mechanisms continuously decreases as the number of cycling times increases. Also, the E_a values are larger at higher PV state. However, the E_a of the TAT mechanism shows much higher dependence on both P/E cycling times and PV states, while the E_a of the detrapping mechanism shows very weak dependence on the both [43], [57].

The strong P/E cycling dependence of the E_a for the TAT mechanism is mainly due to the newly generated traps. These traps reduce the mean distance between the traps in the percolation path across the tunneling oxide layer. Therefore, the effective electrical barrier between traps is lower. However, the detrapping mechanism is generally one-step process. In other words, trapped carriers directly emit from the trap site to substrate with thermal energy. Therefore, the effective electrical barrier is weakly affected by P/E cycling stress.

The TAT mechanism occurs with the combination of tunneling and thermal-emission mechanisms. In higher PV state, the number of electrons in the FG is larger. It increases the strength of electric field across the tunneling oxide layer. Therefore, the portion of tunneling mechanism is larger and thermal dependence is weaker [43]. It makes stronger electric field dependence on the E_a for the TAT mechanism. In the detrapping mechanism case, the effective energy barrier is large enough. Therefore, thermal-emission mechanism is much stronger, even though Poole-Frenkel effect slightly reduces the E_a value [69]. In this reason, the E_a for the detrapping mechanism has weaker electric field dependence.

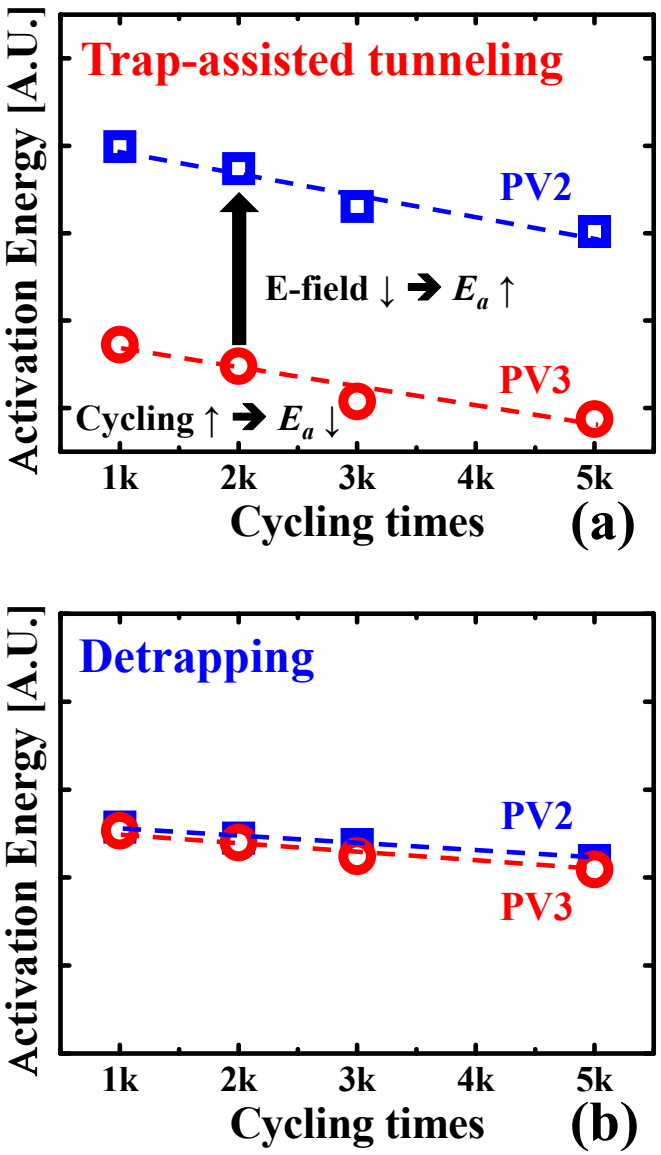
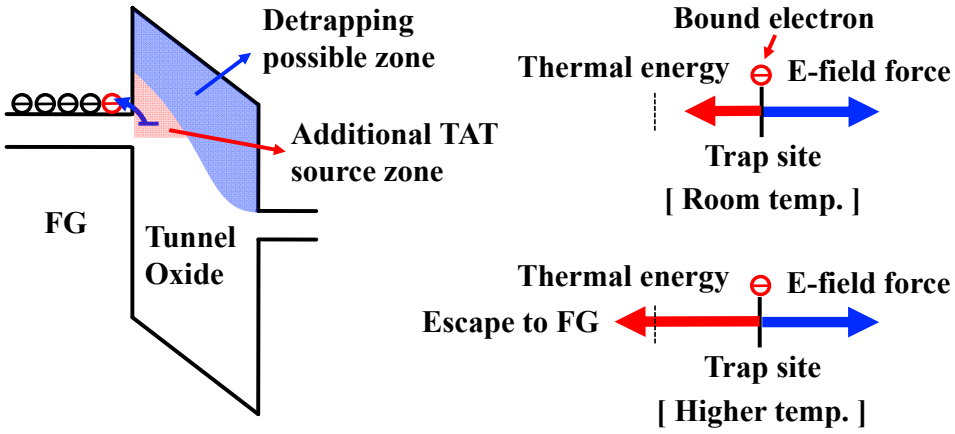
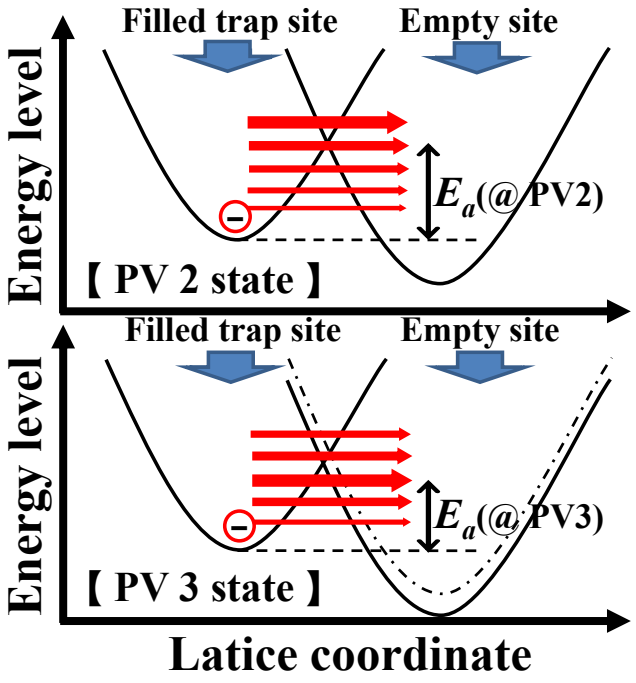


Fig. 4.14. The extracted E_a of (a) the TAT and (b) the detrapping mechanisms at PV3 and PV2 states according to the cycling times (1k ~ 5k times). The E_a of the TAT mechanism shows much higher dependence on P/E cycling times and PV states.


Detrapping
possible zone
Additional TAT
source zone
FG
Tunnel
Oxide
Bound electron
Thermal energy
E-field force
Trap site
[Room temp.]
Thermal energy
E-field force
Escape to FG
Trap site
[Higher temp.]

(a)


Filled trap site
Empty site
Energy level
E_a(@ PV2)
【 PV 2 state 】
Filled trap site
Empty site
Energy level
E_a(@ PV3)
【 PV 3 state 】
Latice coordinate

(b)

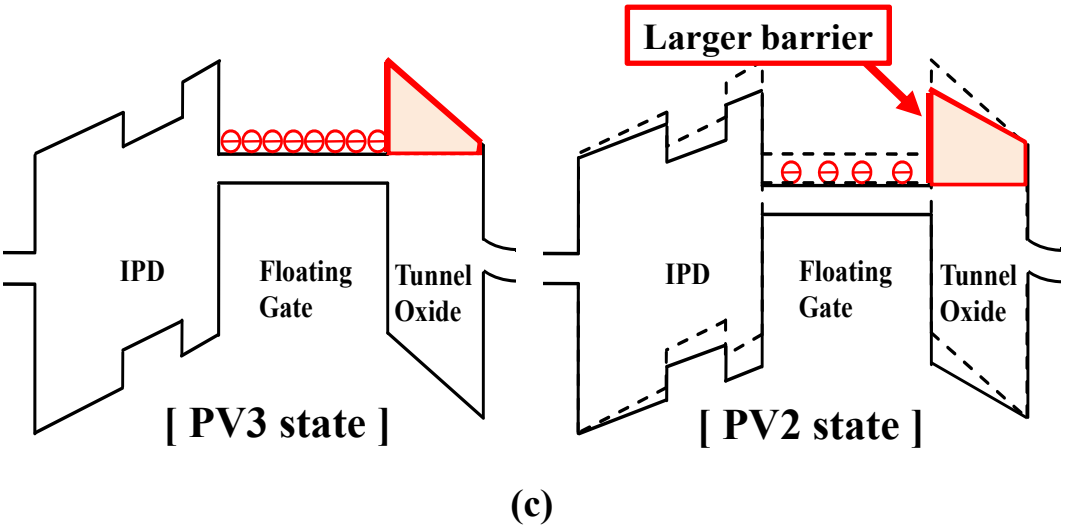


Fig. 4.15. (a) Schematic of energy band diagram explaining the origin of the final ΔV_{th} behavior for the TAT mechanism. (b) Total energy diagram corresponding to the electron transition from a filled trap site to an empty one at PV3 and PV2 states, explains the dependence of the E_a on PV state (electric field). (c) Energy band diagrams explain the relationship between the E_a and PV states.

Fig. 4.15(a) shows a schematic of energy band diagram to explain the origin of P/E cycling times and PV states dependence on the difference value ($\Delta V_{th(125\,^{\circ}C)} - \Delta V_{th(40\,^{\circ}C)}$) for the TAT mechanism. For the trapped carriers close to the substrate, the detrapping mechanism occurs easily [26]. However, the trapped carrier close to FG cannot emit to the substrate within the time of interest due to large energy barrier. Also, the direction of electric field makes the carrier confined. However, the confined electrons can escape to FG with high thermal energy. Therefore, the source for the TAT mechanism is larger with temperature. Also, the amount of the confined electrons can be larger with higher trap

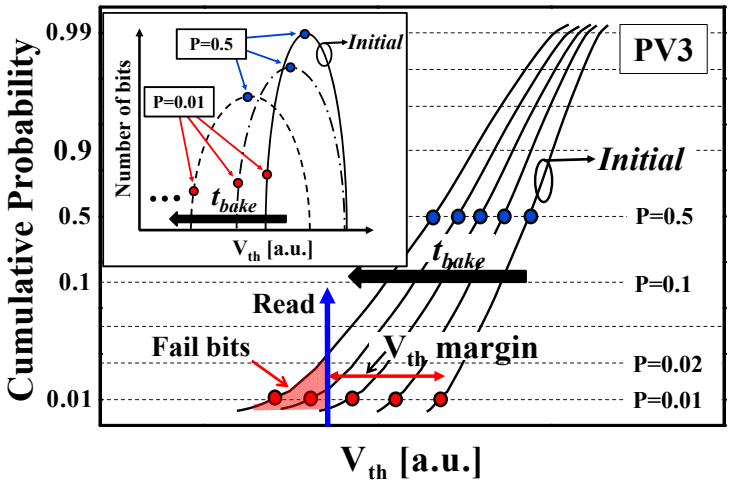
density and with larger strength of confining electric field.

Fig. 4.15(b) shows total energy diagram corresponding to the electron transition from a filled trap site to an empty one at PV3 and PV2 states. It explains the dependence of the E_a on PV state (electric field). The red arrows represent the possible transitions of multiphonon between the different resonant vibrational eigenfunctions [43], [70]. The average energy difference between the trapped electron and the average path is corresponding to the activation energy of this mechanism. The cell at higher state (PV3) has larger number of electrons in the FG, which induces higher electric field across the tunneling oxide layer. The E_a of TAT mechanism is proportional to the height of the average energy barrier among the traps related to the TAT mechanism [57]. Since the higher electric field reduces the energy barrier, the E_a values for the TAT mechanism at the PV3 are lower than that at the PV2.

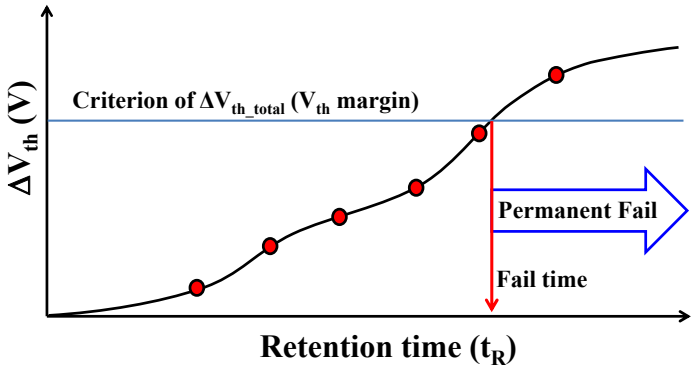
In Fig. 4.15(c), the band diagrams explain the relationship between the E_a and PV states. In lower PV state, effective energy barrier is larger and it makes higher temperature dependence. Therefore, the E_a increases with lower PV state.

4.4.2 Probability Level Dependence

Fig. 4.16(a) shows the initial V_{th} cumulative distribution and the distributions after bake in the PV3 state of extremely scaled NAND flash main-chip. The inset shows the V_{th} distribution after program operation, which changes to flat and wide shape from initial distribution state due to the charge loss/gain of various failure mechanisms [56]-[61]. The blue dots (P = 0.5) represent the charge loss behavior for the center regime of the V_{th} distribution and the red dots (P = 0.01) represent the charge loss behavior around the tail bit regime. Previously, we analyzed the failure mechanisms with the average ΔV_{th} value of 20 TEG cells in Chapter 3 [56]-[57]. The result represents the general charge loss behavior of normal cells only. In the main-chip case, however, the ΔV_{th} of tail bit regime determines the real lifetime of the device due to the limit of capability of repair algorithm such as error correction code (ECC), redundancy, and so on [62]. The probability level is corresponding to the maximum number of capable error bits by ECC over total number of bits in the V_{th} distribution. For example, if the number of cell in PV3 is 10,000 and the capability of ECC is 100, our interesting P-level in the chip should be 0.01 (100/10,000). The probability level should be adjusted depending on the capacity of ECC. Using larger ECC can make it allow the higher probability level. In this section, the retention characteristics in various P-level (P = 0.01, 0.1, and 0.5) are compared and analyzed in detail. Fig. 4.16(b) shows the charge loss behavior at specific P-level (P = 0.01) according to retention time. The number of fail bits increases with retention time. When the amount of V_{th} shift at the criterion P-level is larger than the criterion of ΔV_{th}, the device goes into permanent failure.



(a)



(b)

Fig. 4.16. Initial V_{th} cumulative distribution and the distributions after bake in the PV3 state of extremely scaled NAND flash main-chip. The blue dots (P=0.5) represent the charge loss behavior of the center and the red dots (P=0.01) represent the charge loss behavior of the tail bit regime. The number of fail bits increases with baking time. (b) The charge loss behavior at specific P-level according to retention time.

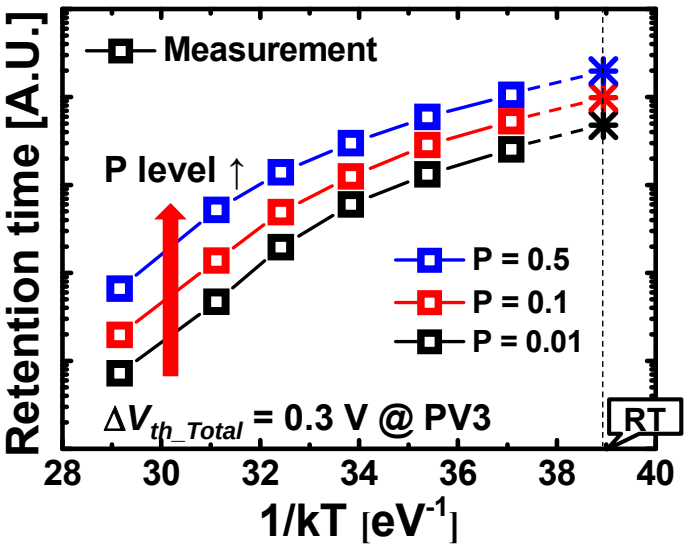


Fig. 4.17. Retention time characteristics for the PV3 state of 3k-cycled NAND flash memory with various probability levels (P = 0.01, 0.1, and 0.5) according to the baking temperature. The criterion for ΔV_{th_Total} is of 0.3 V.

Fig. 4.17 shows the characteristics of the retention time for the PV3 state of the NAND flash memory main-chip according to baking temperature. The data are extracted at various probability levels (P = 0.01, 0.1, and 0.5). The criterion for ΔV_{th_Total} is 0.3 V. Actual criterion of ΔV_{th_Total} is slightly increasing as the probability level is higher [see Fig. 4.16(a)]. However, we fix the criterion of ΔV_{th_Total} in this section in order to simplify it. The retention time is observed to become longer as the probability level increases. In order to estimate the accurate lifetime for the device, analysis of retention characteristics on each mechanism according to the probability level is necessary.

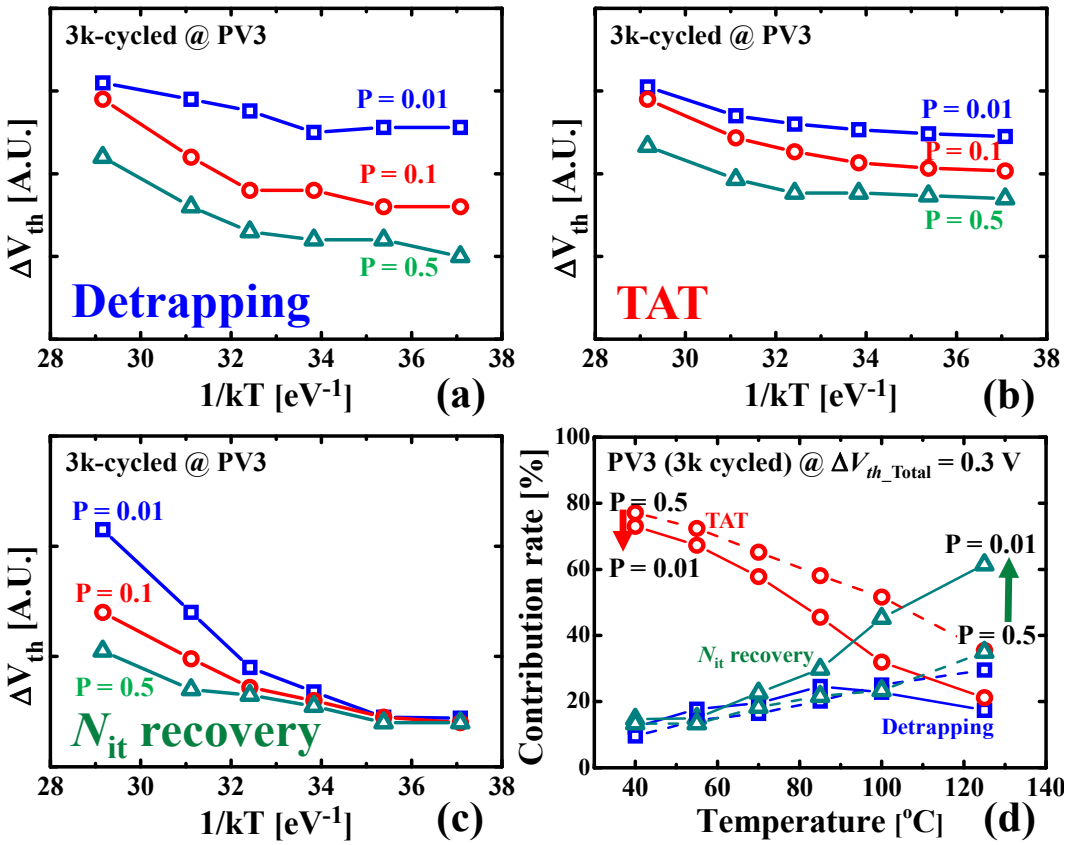


Fig. 4.18. The temperature dependence of final ΔV_{th} of (a) the detrapping, (b) the TAT, and (c) the N_{it} recovery mechanisms according to the P-level. As the P-level is lower, the final ΔV_{th} of each mechanism is larger. (d) The contribution rate of each failure mechanism to the criterion of ΔV_{th_Total}. The criterion for ΔV_{th_Total} is of 0.3 V. As the P-level is lower, the retention time becomes shorter for all baking temperatures because the contribution rate of the fast mechanism becomes larger and that of the slow mechanism becomes smaller.

Fig. 4.18(a), (b), and (c) show the final ΔV_{th} of the detrapping, the TAT, and the N_{it} recovery mechanisms at PV3 state of 3k-cycled sub 20-nm NAND flash memory main-chip according to the probability levels and baking temperatures. It was observed that the amount of charge loss becomes larger with the lower probability level (P = 0.01) because relatively inferior cells gather more at lower probability level with increasing baking time whereas superior cells are left at higher probability level [58].

Fig. 4.18(d) shows the contribution rate of the three dominant failure mechanisms on the criterion of ΔV_{th_Total} according to the baking temperature. The criterion for ΔV_{th_Total} is of 0.3 V. It is corresponding to the left-hand side of Eq. (2.12), and the portion of each mechanism corresponds to each term in the right-hand side of Eq. (2.12). As the probability level is lower, relatively inferior cells gather more and the N_{it} trap density in the cells is higher, so the contribution rate of the fast mechanism becomes larger. Therefore, the retention time becomes shorter over all baking temperature regimes. Since the quality of cell is highly affected by the probability level, the lifetime of the device highly depends on the V_{th} margin and the capability of ECC.

4.4.3 Analysis of Detrapping Mechanism using 3D TCAD simulation

Reliability issues in NAND flash memory are dominantly related to traps in the tunneling oxide. Electrical stress due to repeated P/E cycling is a main cause the damage of tunnel oxide [25].

Fig. 4.19 shows the retention characteristics for the detrapping mechanism extracted at PV3 state of 1k-cycled sub 20-nm NAND flash memory main-chip using proposed charge loss model as introduced in section 4.3. In this section, analysis of detrapping mechanism is conducted using 3D TCAD simulation in order for deeper understanding of the retention characteristics in the detrapping mechanism.

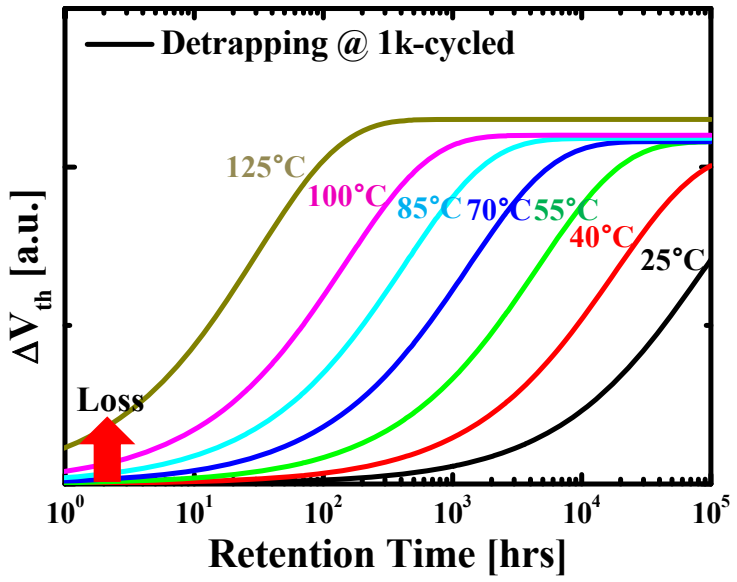


Fig. 4.19. Extracted the detrapping component for the PV3 state of 1k-cycled NAND flash memory using the proposed model.

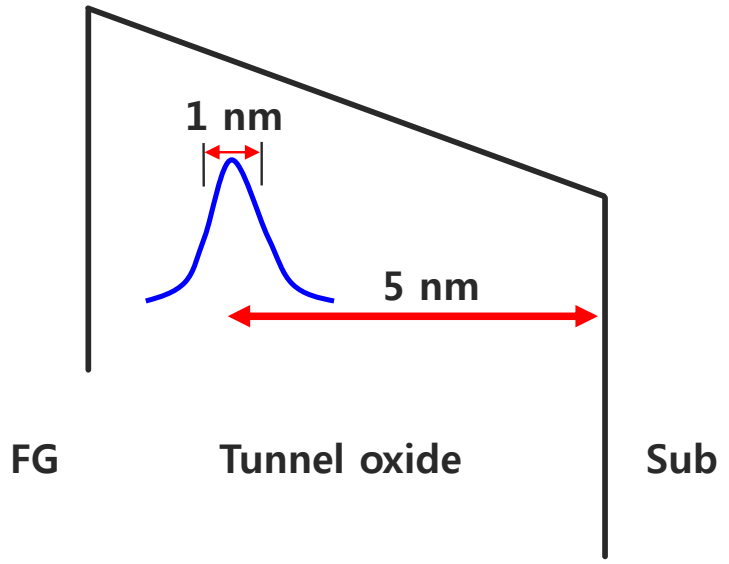
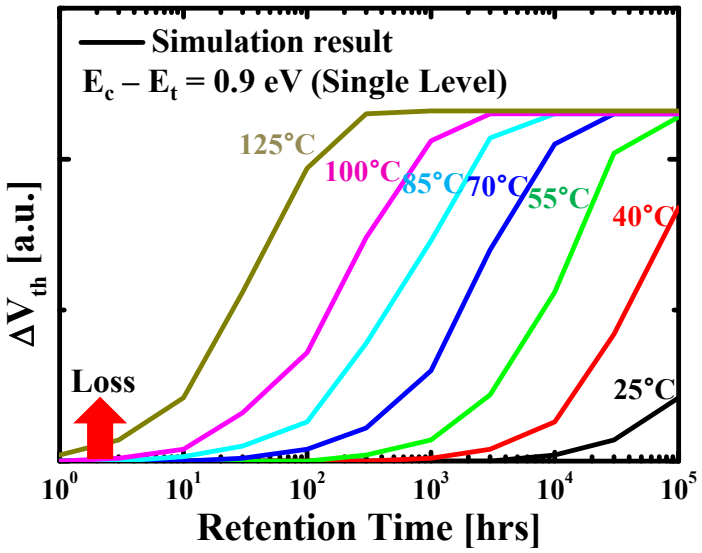
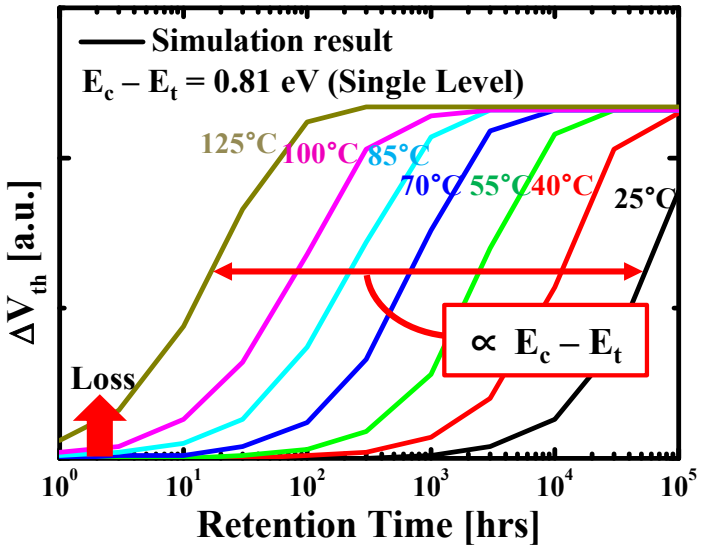


Fig. 4.20. Trap distribution in tunneling oxide for 3D TCAD simulation work.

Fig. 4.20 shows trap distribution in tunneling oxide in TCAD simulation set-up for the retention characteristic of the detrapping mechanism. Trap distribution is Gaussian peak is 5 nm far away from substrate with the concentration of 6.95 x 10^{18} cm^{-3}. Space sigma of the Gaussian distribution is 1 nm. The trap-unfilled initial V_{th} is set to 3 V. For the detrapping mechanism, trap sites are initially filled with electrons. Using this trap distribution, retention simulation was conducted according to bake time up to 10^5 hrs (~10 years) and various retention temperatures (25 °C, 40 °C, 55 °C, 70 °C, 85 °C, 100 °C, and 125 °C).



(a)



(b)

Fig. 4.21. 3D TCAD simulation result for the detrapping charge loss according to the retention time and temperature. The results show the temperature dependence on the trap energy level.

Fig. 4.21 shows 3D TCAD simulation result for the detrapping charge loss according to the retention time and temperature. First, we assume that trap has single energy level. The results show the temperature dependence on the trap energy level. Higher temperature dependence (higher activation energy) was observed in the case of larger energy level difference between conduction edge in oxide layer and trap level. $E_{a(\mathrm{Detrap})}$ is proportional to the energy level difference ($E_c - E_t$). Using this relationship, trap energy level was found ($E_c - E_t = 0.81$ eV).

Fig. 4.22(a) shows the extracted the detrapping component using the proposed model (black line) and simulation results with single energy level (red square) and Gaussian energy level (blue square) at 25°C for the PV3 state of 1k-cycled NAND flash memory. Fig. 4.22(b) shows schematic for trap profiles in energy level for simulation works. The results show that β_{Detrap} parameter value changes with trap energy distribution and the trap level with Gaussian distribution is much more reasonable. In section 4.3, extracted β_{Detrap} parameter value is about 0.67. In case of single level, β_{Detrap} is close to 1. However, β_{Detrap} value is lower in Gaussian distribution. As energy sigma increases, β_{Detrap} value becomes decreasing. It is observed that optimized energy sigma is σ~0.084 eV. All the finalized fitting parameter values are summarized in Table 4.3.

Fig. 4.23 shows the retention characteristic for the detrapping mechanism according to retention time at various temperatures in the PV3 state of 1k-cycled NAND flash memory. The lines are extracted results using the proposed charge loss model. The symbols are simulation results using parameter values in Table 4.3. The both results are observed to be in good agreement.

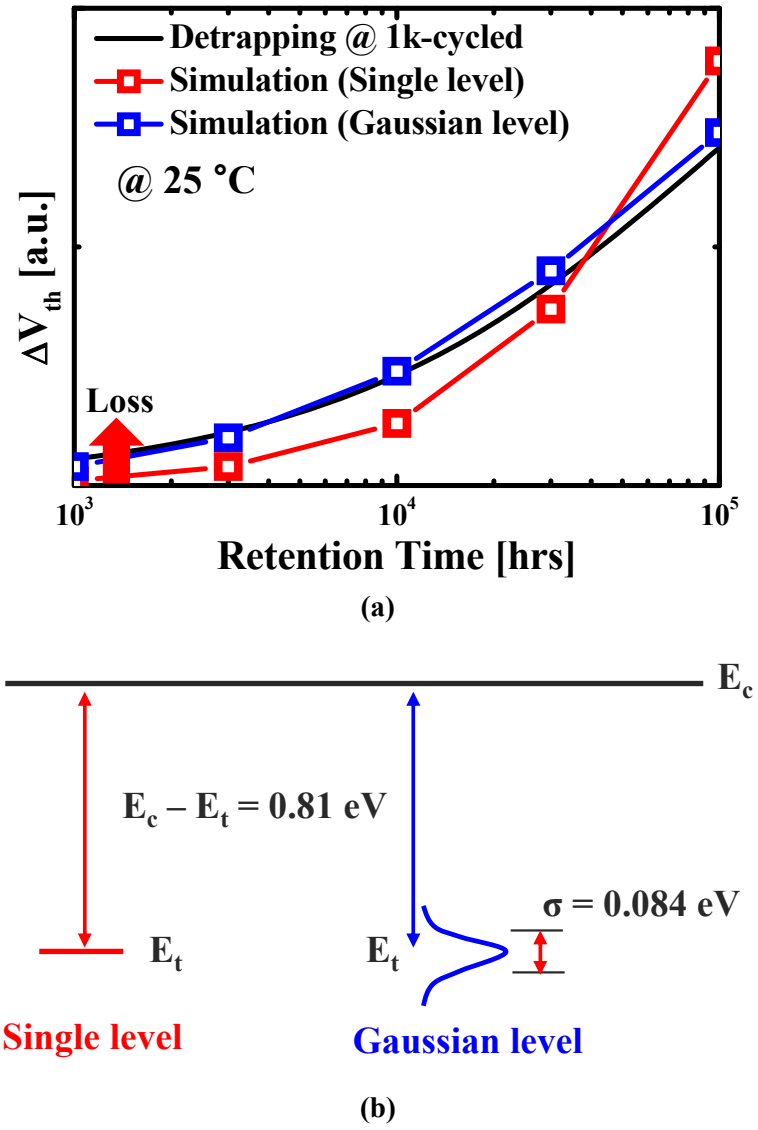


Fig. 4.22. (a) β_{Detrap} parameter fitting results using trap energy level distribution. (b) trap profile in energy level for simulation works. The results show that Gaussian distribution is much more reasonable.

TABLE 4.3

FINAL PARAMETER VALUES FOR THE DETRAPPING MECHANISM IN TCAD SIMULATION

	Spatial profile (Gaussian distribution)	Energy profile (Gaussian distribution)
Position	5 nm from sub	$E_c - E_t$ = 0.81 eV
Sigma	1 nm	0.084 eV
Density	Peak=6.95 x 10^{18} cm^{-3}	

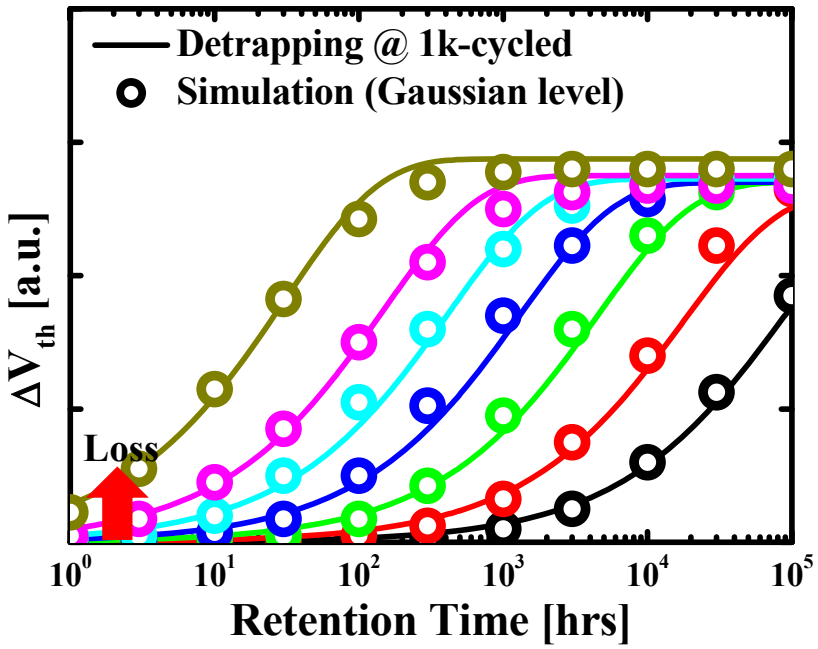


Fig. 4.23. Retention characteristic for the detrapping mechanism in the PV3 state of 1k-cycled NAND flash memory. The lines are extracted results using the proposed charge loss model. The symbols are simulation results using parameter values in Table 4.3.

4.5 Summary

In this Chapter, we investigate the retention characteristics in sub 20-nm NAND flash memory main-chip. Previously, we propose the new charge loss model in Chapter 2. However, there are lots of parameters in the new model. In order to extract the accurate value for the parameters, plenty of clues in experimental and in literature should be collected as much as possible. In this Chapter, the procedure of parameter extraction is explained in detail. We extract the contribution rate (CR) of dominant failure mechanisms at specific criterion of $|\Delta V_{th\_Total}|$ according to the baking temperature by new model. The results provide the physical reason for abnormal retention behaviors such as E_{aa} roll-off at the PV3 and negative E_{aa} at the ERS. Also, analysis of the TAT mechanism is conducted in detail and the retention characteristics are compared with the detrapping mechanism. It is observed that the final ΔV_{th} of the TAT mechanism increases according to the baking temperature, while the detrapping mechanism has almost constant behavior. We also extract the E_a for the TAT mechanism in various conditions and compare with the E_a of the detrapping mechanism. As a result, it is found that the TAT mechanism is much affected by trap density as well as strength of electric field in tunneling oxide layer. The retention characteristics change with the probability level of the cumulative V_{th} distribution. Moreover, we deeply analyze the P-level dependence on retention behavior of each mechanism. We also analyze the detrapping mechanism using 3D TCAD simulation in order for deeper understanding of the retention characteristics in the detrapping mechanism. As a result, trap profiles in tunnel oxide are extracted in space and energy distributions.

Chapter 5

Analytical Model for Apparent Activation Energy (E_{aa}) and Proposed Lifetime Estimation Method

5.1 Introduction

Apparent activation energy (E_{aa}) is an equivalent energy value that can be inserted in the Arrhenius equation for reliability to calculate an acceleration factor applicable to changes with temperature of time-to-failure distributions in electric devices [36]. The Arrhenius model is widely used method predicting the lifetime for NAND flash memory. This Arrhenius model is used under the assumption that the E_{aa} is constant with temperature. However, it has been continuously reported that the Arrhenius plot shows not a straight line but the E_{aa} roll-off behavior mainly due to coexistence of various failure mechanisms [50]-[52]. In order to predict the accurate lifetime of the device, a physical mechanisms on the abnormal E_{aa} behavior should be understood.

Generally well-known dominant failure mechanisms in NAND flash memory are detrapping [25]-[27], interface trap (N_{it}) recovery [28]-[31], and trap-assisted tunneling (TAT) [32]-[35]. We previously introduced a technique to separate the dominant mechanisms in NAND flash memory [56]-[62]. Each mechanism follows the Arrhenius law well (constant E_a), which means that each has its own activation energy (E_a) [56]-[62]. However, the correlation between E_{aa} and each E_a could not be found out. Misinterpretation of E_{aa} can cause serious error in the lifetime estimation results.

In this chapter, we investigate the abnormal behavior of E_{aa} in sub 20-nm NAND flash memory. In the HT regime, the N_{it} recovery mechanism dominantly contributes to the V_{th}-loss [28], [30]. However, there is significant difference between E_{aa} and $E_{a(\mathrm{Nit})}$. The E_{aa} can be even larger than the largest E_a among the charge loss mechanisms. For the first time, we uncover the root cause of the E_{aa} roll-off characteristic and the relationship between E_{aa} and each $E_{a(\mathrm{mechanism})}$. As a result, the general equation of E_{aa} is derived as a function of each $E_{a(\mathrm{mechanism})}$. We propose two different accurate lifetime estimation models for sub 20-nm NAND flash memory. The first model is the E_{aa} integration method. Using the analytically modeled E_{aa} equation, the lifetime of NAND flash memory is accurately predicted. The second model is the advanced extrapolation method. The results are compared to those of a conventional Arrhenius model [50]-[52]. The estimated results show a large gap between two models. As the proposed model fully considers physical behaviors of various mechanisms, it provides very accurate prediction on the lifetime of NAND flash memory.

5.2 Modeling for Apparent Activation Energy (E_{aa})

Fig. 5.1 show the retention time and E_{aa} characteristics for the highest programmed threshold voltage (V_{th}) cumulative distribution (PV3) state of sub 20-nm NAND flash memory according to baking temperature. The criterion for ΔV_{th} is 0.3 V. A distributed-cycling scheme was applied in this experiment to reproduce the real in-the-field use of the devices [25]. Each measured data was extracted at a lower probability level (P=0.01) of the V_{th} cumulative distribution [58]-[59]. The probability level is corresponding to the number of error bit over total number of bits, which is full capacity of error correction code (ECC). The probability level should be adjusted depending on the capacity of ECC. Using larger ECC can make it allow the higher Probability level. However, interesting probability level may be in the range of 0.005 ~ 0.05. In this paper, lower probability level (P=0.01) is randomly selected as a reference level. The measured data were extracted at various baking temperatures (40 °C – 125 °C), and the total experimental retention time was of 3024 hours at 40 °C, 55 °C, 70 °C, 85 °C and of 1512 hours at 100 °C and 125 °C. E_{aa} is defined as the slope of the three neighboring data points in the Arrhenius plot [$E_{aa} \equiv \partial (\ln t_R) / \partial (1/kT)$].

Fig. 5.1(a) and (b) show the P/E cycling dependence on the retention time and the E_{aa} characteristics, respectively. The measured data were extracted at various cycling times (1k, 2k, 3k, and 5k). P/E cycling stress induces the degradation on tunnel oxide layer and reduces the retention time over all baking temperature regimes. E_{aa} is not constant but larger with temperature. Also, it becomes larger with cycling times [see Fig. 5.1(b)].

Fig. 5.1(c) and (d) show the probability level dependence on the retention time and the

E_{aa} characteristics in 3k-cycled NAND flash, respectively. The measured data were extracted at various probability levels (0.01, 0.1, and 0.5). It shows similar behavior with P/E cycling dependence. Relatively inferior cells gather more at lower probability level (close to the tail) whereas superior cells are left at high probability level [58]. Therefore, charge loss characteristic in lower probability level has effectively larger degradation behavior. Fig. 5.1(e) shows the Arrhenius plot for the retention time (t_R) extracted at 3k-cycled NAND flash memory. In order to estimate the device lifetime using the Arrhenius model, E_{aa} should be a constant. However, real experimental data shows E_{aa} roll-off characteristics [50]-[52]. Fig. 5.1(f) shows a comparison of the results for the extracted E_{aa} with the E_a of each mechanism according to the baking temperature. Although the E_a of each mechanism has a constant value regardless of the baking temperature [56]-[62], the E_{aa} becomes larger as the baking temperature increases [52]. E_{aa} becomes even larger than $E_{a(\mathrm{Detrap})}$, which is the largest among the dominant failure mechanisms. In order to predict the accurate lifetime of the device, a physical analysis on the abnormal E_{aa} characteristics is necessary.

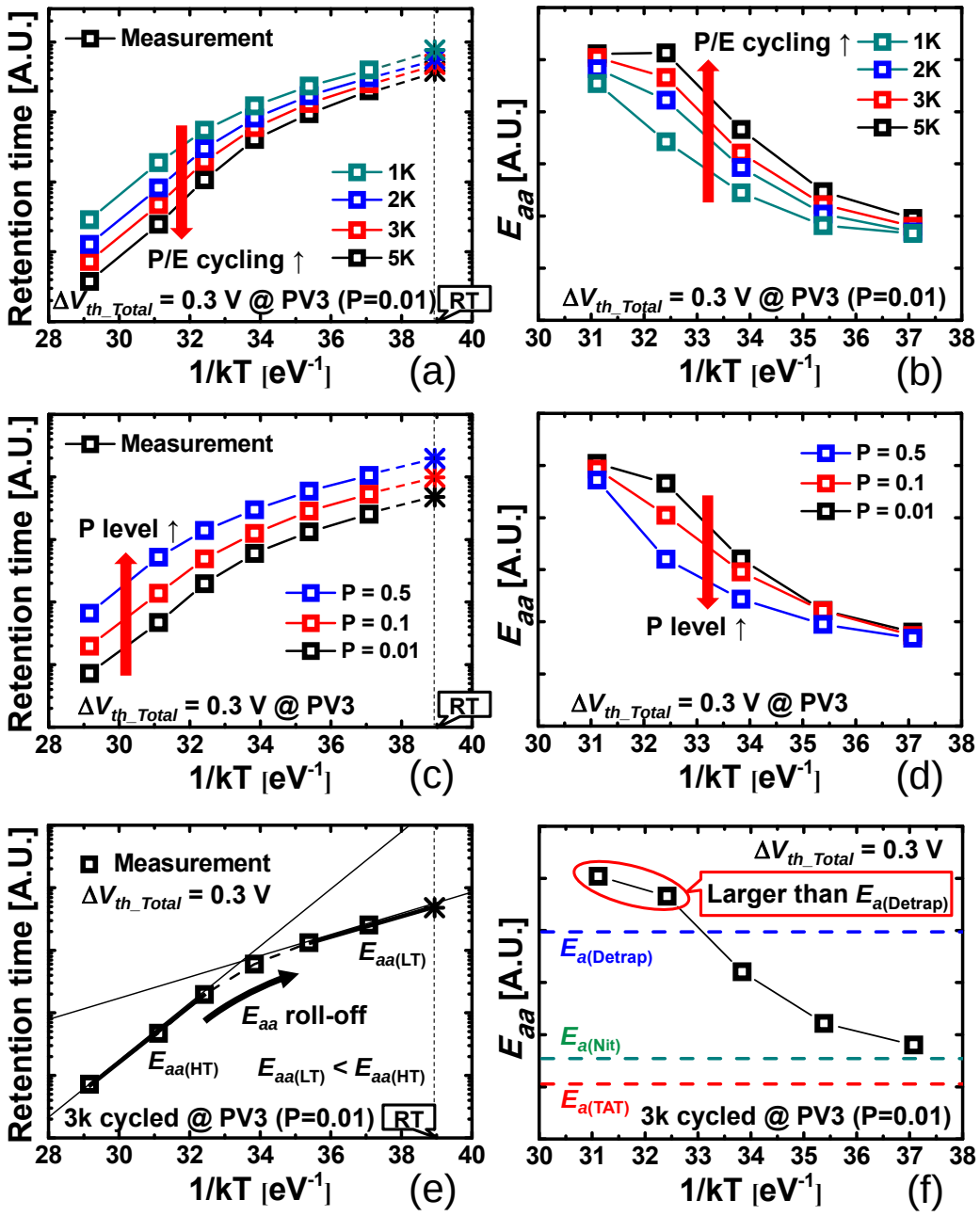


Fig. 5.1. Retention time and E_{aa} characteristics for the PV3 state of sub 20-nm NAND flash memory according to baking temperature (1/kT). P/E cycling dependence on (a) the retention time and (b) the E_{aa} characteristics show complex behavior. P level dependence

on (c) the retention time and (d) the E_{aa} characteristics show similar behavior with cycling dependence. (e) Arrhenius plot extracted for 3k-cycled NAND flash memory. Reference P level is 0.01. It does now follow the Arrhenius raw but shows E_{aa} roll-off characteristic. (f) The extracted E_{aa} becomes larger as the baking temperature increases. In a high-temperature (HT) regime, E_{aa} is even larger than $E_{a(\mathrm{Detrap})}$, which is the largest value among the dominant mechanisms.

If there is only one mechanism that contributes to the charge loss, E_{aa} should be exactly the same as the E_a of the mechanism. However, the coexistence of more than two mechanisms can distort the E_{aa}. Fig. 5.2 shows the schematics for intuitional understand on the origin of E_{aa} in the case of the coexistence of two mechanisms. In Case 1, the CR of each mechanism is constant across all temperature regimes. In this case, E_{aa} should be the value of the interval between $E_{a(\mathrm{A})}$ and $E_{a(\mathrm{B})}$. Also, the value of E_{aa} value is closer to the $E_{a(\mathrm{mechanism})}$ with a larger CR. Therefore, E_{aa} is the simple average value of $E_{a(\mathrm{mechanisms})}$. However, the CR of each mechanism generally changes according to the temperature regime like Case 2. At LT regime, CR_A is larger than CR_B. Therefore, the retention time should be closer to $\ln(\tau_A)$. At the HT regime, however, it has the opposite CR ratio, so the retention time should be closer to $\ln(\tau_B)$. In this case, E_{aa} can be even larger than the largest between $E_{a(\mathrm{A})}$ and $E_{a(\mathrm{B})}$, as shown in Fig. 5.2(c). Since CR is not constant but is a function of the temperature, it also affects the E_{aa}.

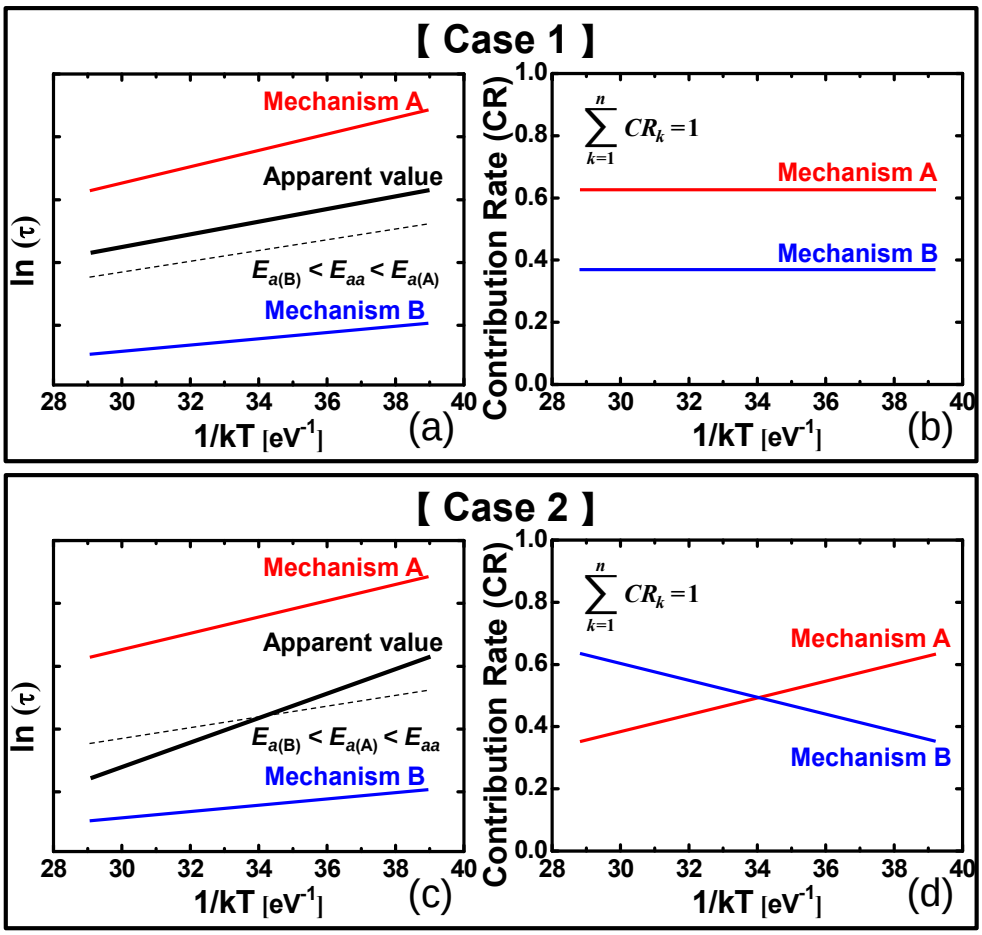


Fig. 5.2. Schematics to explain the principle for the E_{aa} determination in the condition with a coexistence of two mechanisms. Case 1 shows that the contribution rates (CR) of the mechanisms are constant for all temperature regimes. In this case, E_{aa} should be the interval value between $E_{a(A)}$ and $E_{a(B)}$. Case 2 shows the CR of the mechanisms that change according to the temperature regime. In this case, E_{aa} can be larger than the largest between $E_{a(A)}$ and $E_{a(B)}$. It means that the change of the CRs also affects on the E_{aa} value.

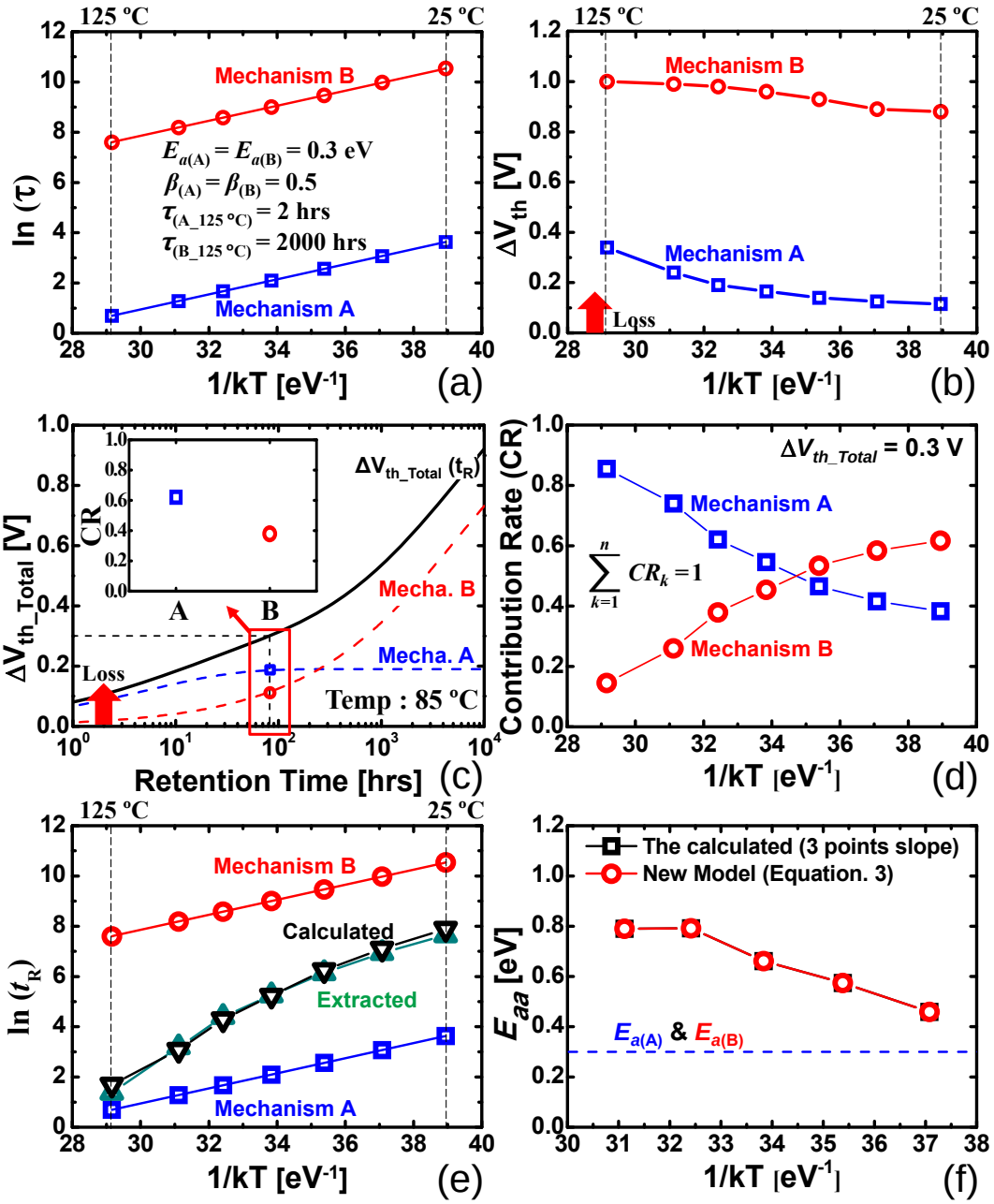


Fig. 5.3. Virtual mechanisms to explain the abnormal retention characteristics. The parameters are arbitrarily selected. (a) Time-constant (τ) behavior of two mechanisms (A : fast mechanism, B : slow mechanism, $E_{a(A)} = E_{a(B)} = 0.3$ eV). (b) Total charge loss

source ($\Delta V_{th\_\text{mechanism}}$) of the mechanisms according to baking temperature. (c) Simulated charge loss behavior at specific temperature (85 °C). (d) The contribution rate (CR) of the mechanisms according to the temperature. (e) The Arrhenius plot and (f) the E_{aa} behavior on temperature.

Fig. 5.3 shows virtual mechanisms to explain the abnormal retention characteristics and to derive the relationship between E_{aa} and each $E_{a(\text{mechanism})}$ in NAND flash memory. In order to help understanding, we assume that there are only two mechanisms. Previously, we introduced that the total charge loss is sum of each mechanism's loss and can be expressed as following [59],[61]:

$$\Delta V_{th\_Total}(t_R) = \sum_{k=1}^{n} \Delta V_{th\_k} \cdot \left[1 - \exp\left(-\left(t_R / \tau_k\right)^{\beta_k}\right)\right] \tag{5.1}$$

where ΔV_{th_k}, τ_k, t_R, and β_k are the amount of total charge loss source for each mechanisms, the time-constant (τ) for each mechanism, the retention time, and the shape parameter for charge loss distribution [36], respectively. In the retention condition, the value of β is always smaller than 1 ($0 < \beta_k < 1$). It means that the occurrence probability of the charge loss mechanism decreases over time [36], [53]. As shown in Fig. 5.3(a) and (b), the parameters are arbitrarily selected under the conditions of ($\Delta V_{th\_k(\text{LT})} \leq \Delta V_{th\_k(\text{HT})}$) and ($\tau_{k(\text{HT})} \leq \tau_{k(\text{LT})}$) [57], [61]. Fast mechanism (A) and slow mechanism (B) have the same E_a ($E_{a(\text{A})} = E_{a(\text{B})} = 0.3$ eV). In Fig. 5.3(c), $\tau_{k(85°\text{C})}$ can be obtained by the Arrhenius relation, $\tau_{k(85°\text{C})} = \tau_{k(125°\text{C})} \cdot \exp[E_{ak}(1/kT_{85°\text{C}} - 1/\text{kT}_{125°\text{C}})]$. The charge loss behavior for 85 °C is

simulated using Eq. (5.1) and given parameters [see Fig 5.3(a) and (b)]. Fig. 5.3(d) shows the contribution rate (CR) of the mechanisms for total charge loss according to the temperature. The criterion for ΔV_{th} is 0.3 V, which corresponds to CR = 1. The mechanism A becomes dominant in HT regime, while the mechanism B is dominant in low-temperature (LT) regime in this result. Fig. 5.3(e) shows the Arrhenius plot of the simulated data. The E_{aa} roll-off behavior is observed. In HT regime, CR of fast mechanism (CR_A) is larger so that $\ln(t_R)$ is close to $\ln(\tau_A)$. However, $\ln(t_R)$ is close to $\ln(\tau_B)$ in LT regime due to larger CR of slow mechanism (CR_B). In this principle, $\ln(t_R)$ can be approximately obtained by following equation:

$$\begin{aligned} \ln t_R &\approx CR_{\mathrm{A}} \cdot \ln \tau_{\mathrm{A}} + CR_{\mathrm{B}} \cdot \ln \tau_{\mathrm{B}} \\ &= \sum_{k=1}^{n} CR_k \cdot \ln \tau_k \end{aligned} \tag{5.2}$$

The extracted (green triangle) data are the retention time when the amount of the simulated charge loss ($\Delta V_{th\text{-}Total}$) becomes 0.3 V [see Fig. 5.3(c)]. The calculated (black inverted triangle) data are obtained by Eq. (5.2). Since the both have strong correlation, t_R can be replaced by Eq. (5.2). By the definition, the general equation for E_{aa} can be expressed as following:

$$
\begin{aligned}
E_{aa} &\equiv \partial \ln t_R / \partial (1/kT) \\
&\approx \sum_{k=1}^{n} \partial \left(CR_k \cdot \ln \tau_k \right) / \partial (1/kT) \\
&= \sum_{k=1}^{n} \left[CR_k \cdot E_{a(k)} + \ln \tau_k \cdot \frac{\partial CR_k}{\partial (1/kT)} \right]
\end{aligned}
\tag{5.3}
$$

Fig. 5.3(f) shows the E_{aa} behavior according to temperature. The black square symbols are obtained by 3 points slope of the calculated one in Fig. 5.3(e). The red circle symbols are obtained by Eq. (5.3). Both results are exactly the same. Therefore, availability of the E_{aa} equation is verified. The results show that E_{aa} can be much larger than the highest E_a among mechanisms.

Fig. 5.4(a) shows the CR extracted for the three dominant failure mechanisms in the PV3 state of 3k-cycled NAND flash memory with respect to the baking temperature [61]. In the LT regime, the contribution rate of the TAT mechanism is dominant among all other mechanisms. Since the TAT mechanism has weak dependence on temperature, low apparent E_a characteristics are observed [36]. However, the N_{it} trap annealing effect becomes larger as the baking temperature increases [28], [30]. As the CR of fast mechanism (N_{it} recovery) is larger with temperature, the CR of the TAT mechanism becomes rapidly smaller. Since the TAT mechanism has much larger τ than the other mechanisms one, $CR_{TAT} \cdot \ln \tau_{TAT}$ is dominant factor for $\ln t_R$. Therefore, t_R is much shorter quite rapidly as expressed in Eq. (5.2) and has a stronger dependence on temperature as the temperature increases. This non-uniform CR characteristic makes the E_a roll-off behavior.

Fig. 5.4(b) shows the E_{aa} values extracted according to the baking temperature. The black square symbols represent the values that are experimentally measured. The red circular symbols are extracted using Eq. (5.3). In the HT regime, the CR of the N_{it} recovery mechanism is the largest. However, the actually extracted E_{aa} values are more than three times larger, as shown in Fig. 5.1(b). However, the E_{aa} calculated with Eq. (5.3) and the measured value were observed to be in good agreement. Therefore, the new model for the general E_{aa} has been successfully verified. The new model shows that E_{aa} can be much larger than the E_a of each mechanism.

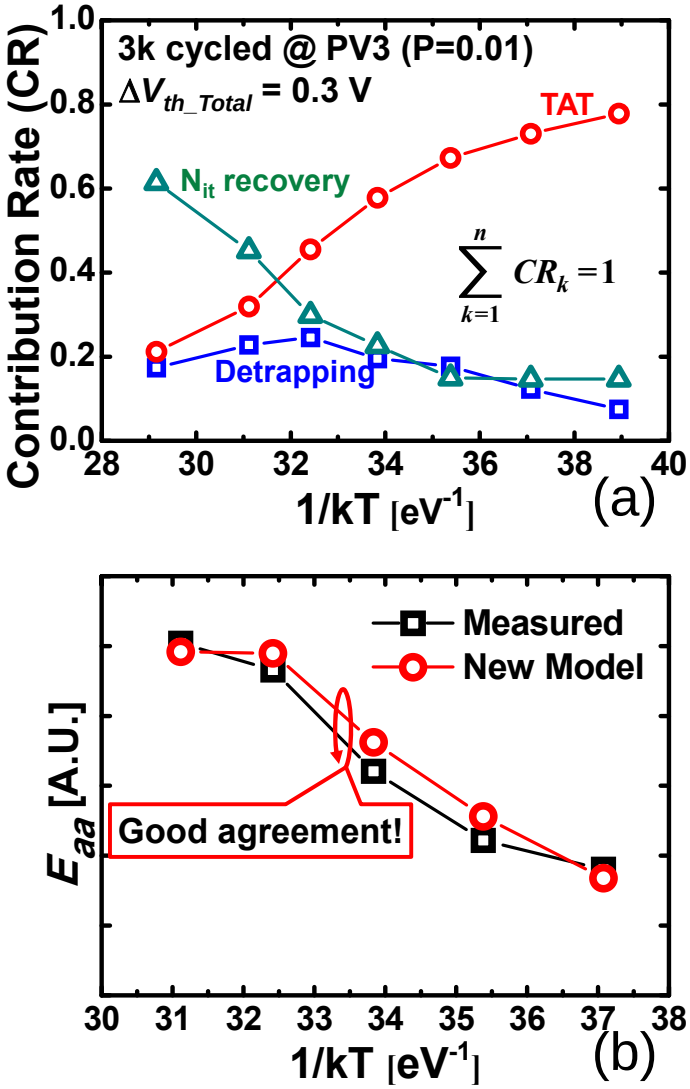


Fig. 5.4. (a) Actual CR of each mechanism that contributes to the charge loss criterion (ΔV_{th} = 0.3 V) according to the baking temperature, which are extracted from 3k-cycled NAND flash memory. (b) Comparison of the results for E_{aa} result those were measured and calculated by new model. The measured and calculated values show in good agreement.

5.3 Proposed Lifetime Estimation Method

In previous sections, we introduced the procedure of parameter extraction for the new model and analyzed the abnormal retention characteristics in sub 20-nm NAND flash memory. Also, the E_{aa} equation was derived as a function of the E_a of each mechanism. In this section, two accurate lifetime estimation methods are proposed using the extracted parameters and the E_{aa} equation.

5.3.1 E_{aa} Integration Method

Fig. 5.5(a) shows the extracted E_{aa} values by the Arrhenius and the proposed model. The results of the two models have large gap especially in the LT regime. The values for edge E_{aa} (125 °C and RT) are extracted by extrapolating the near two points slope. Fig. 5.5(b) shows the estimated lifetime results by the two models. The blue triangular and red circular symbols are the predicted values by the Arrhenius and proposed models, respectively. The lifetime is calculated by integrating the E_{aa} using following equation:

$$t_{R(\mathrm{RT})} = \exp\left[\int_{1/kT(125°\mathrm{C})}^{1/kT(\mathrm{RT})} E_{aa}(T)\,d(1/kT) + \ln t_{R(125°\mathrm{C})}\right] \tag{5.4}$$

While the lifetime for the Arrhenius model is overestimated due to the assumption on constant E_{aa}, the lifetime for the proposed model shows reasonable result. Since the measured data at highest temperature [ln $t_{R(125\ °\mathrm{C})}$] is used as the initial value for the integration, small disparity between the measured and the calculated one can be

compensated. Since very good agreement between measured and analytically modeled E_{aa} is achieved, the lifetime for the device can be accurately extracted by integrating the calculated E_{aa}.

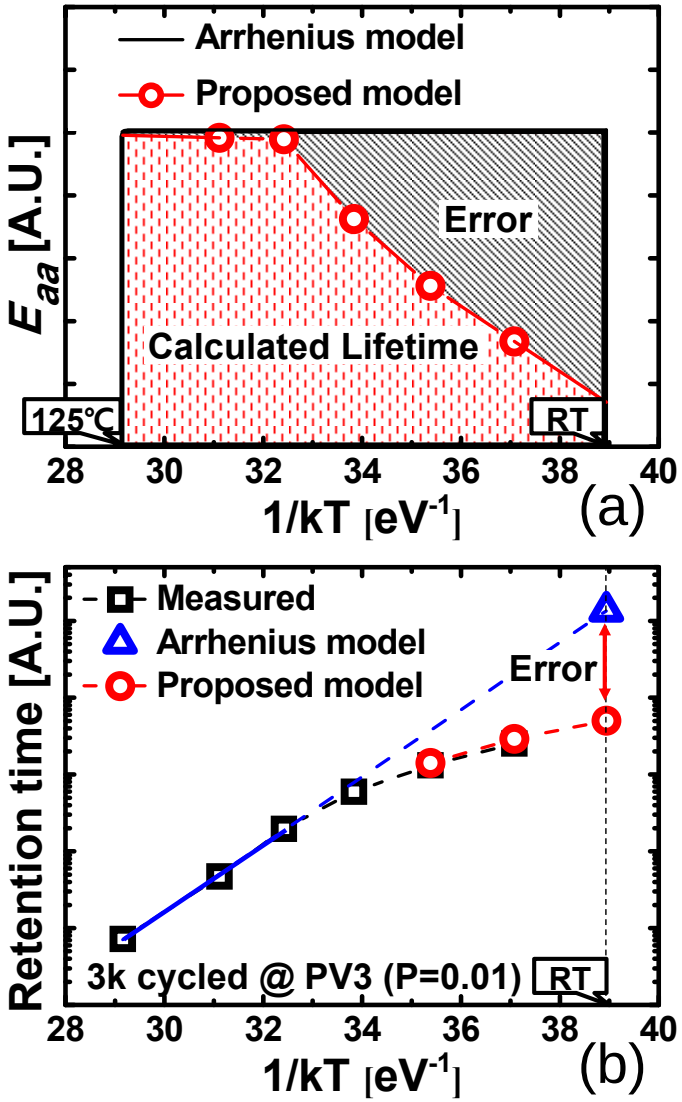


Fig. 5.5. (a) E_{aa} values extracted using the Arrhenius and the proposed model. (b) Lifetime prediction results by the two models. By integrating the E_{aa}, the lifetime is

calculated.

5.3.2 Advanced Extrapolation Method

Fig. 5.6 shows the results for the extracted parameters of the τ and the final ΔV_{th} according to the baking temperature at 3k-cycled NAND flash memory in the PV3 state. The τ of each mechanism is proportional to the average charge loss time for each mechanism. The final ΔV_{th} of each mechanism is the amount of shift in V_{th} when the retention time goes to infinity. All of the data were extracted at the PV3 state of the 3k-cycled NAND flash memory for various baking temperatures (40 °C–125 °C). The symbols were obtained using solver function in Microsoft Excel 2010 by the procedure introduced in section 4.3. The function automatically extracts parameters which have minimum mean squared error (MSE) value between data and Eq. (5.1) [58]-[59], [66]. In order to obtain unique solution, all the limiting conditions in Table 4.1 and Table 4.2 should be satisfied. The lines represent the trends for the symbols, and since the reaction velocity for each mechanism is higher at a higher temperature, the τ for each mechanism becomes shorter as the baking temperature increases. Since each mechanism conforms well to the Arrhenius law, the τ for each mechanism at RT is easily predictable by extrapolating [see Fig. 5.6(a)]. Since the final ΔV_{th} for each mechanism is saturated as the temperature decreases, the final ΔV_{th} for each mechanism at RT can also be easily estimated by these trends [see Fig. 5.6(b)].

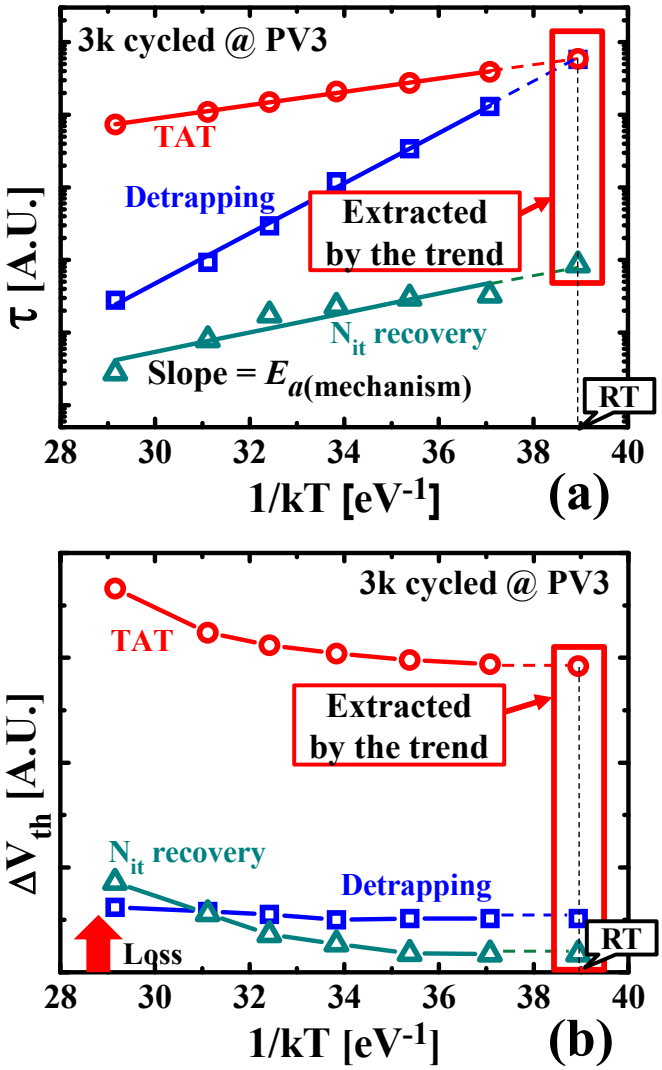
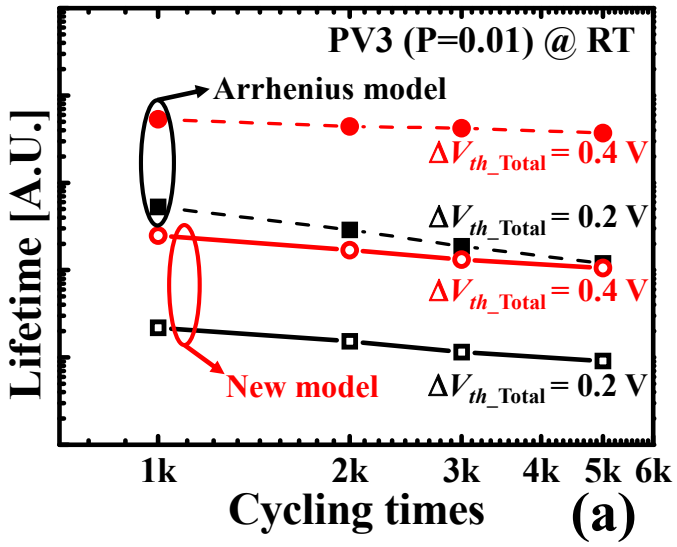
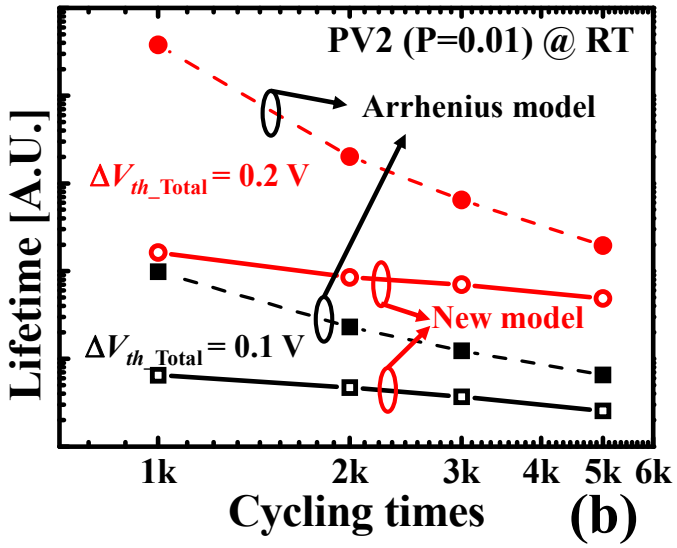


Fig. 5.6. (a) The time-constant (τ) extracted for each mechanism at various baking temperatures (40 °C–125 °C) and τ estimated at RT by extrapolating on 1/kT. (b) The final ΔV_{th} extracted for each dominant failure mechanism and the final ΔV_{th} estimated at RT by the saturation trend of each mechanism at the lower temperature for the PV3 state of the 3k-cycled NAND flash memory.

Figs. 5.7 (a), (b), and (c) show a comparison of the results for the lifetime extracted at

RT by the two models under various states of NAND flash memory according to the P/E cycling times. The results of the lifetime extracted by two models have a large gap under all criteria for the cycling times and $|\Delta V_{th\_\mathrm{Total}}|$. In some cases, the difference in predictions for the lifetime can be as large as thirty times in magnitude. For the PV3 and PV2 states, the lifetime is overestimated when using the conventional method [see Fig. 5.7(a) and (b)]. Since the contribution rate of the fast mechanism such as N_{it} recovery increase with baking temperature, the retention time becomes much shorter in HT regime. This E_a roll-off behavior is the cause for the overestimation in the lifetime prediction. On the other hand, the lifetime is underestimated in the ERS state [see Fig. 5.7(c)]. Since greater TAT sources are required at the HT regime to cancel out the charge loss, the retention time becomes even longer as the baking temperature increases. Therefore, this negative E_a behavior causes an underestimation in the lifetime prediction.


PV3 (P=0.01) @ RT
Arrhenius model
ΔV_th_Total = 0.4 V
ΔV_th_Total = 0.2 V
ΔV_th_Total = 0.4 V
New model
ΔV_th_Total = 0.2 V
Lifetime [A.U.]
1k
2k
3k
4k
5k
6k
Cycling times
(a)


PV2 (P=0.01) @ RT
Arrhenius model
ΔV_th_Total = 0.2 V
New model
ΔV_th_Total = 0.1 V
Lifetime [A.U.]
1k
2k
3k
4k
5k
6k
Cycling times
(b)

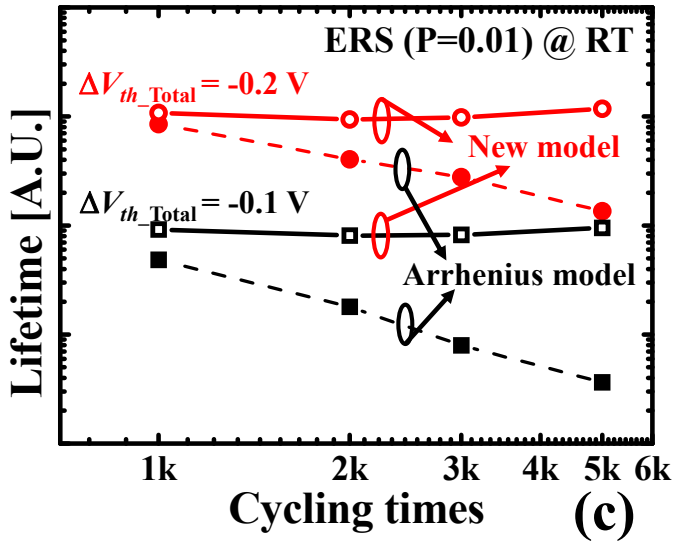


Fig. 5.7. Comparison of the results for the lifetime extracted at RT with both models at the (a) PV3, (b) PV2, and (c) ERS state of the NAND main chip, according to various P/E cycling times and to the criteria for $|\Delta V_{th}|$. The lifetime given by the new model is much shorter for PV3 and is much longer for ERS.

Fig. 5.8 shows a simulation result for the charge loss/gain behavior at RT for 3k-cycled NAND flash memory in all states according to a retention time of ten years. The results are based on the superposition model with the extracted parameters for RT [see Fig. 5.6]. The τ for each mechanism at RT is easily predictable by extrapolating and the final ΔV_{th} for each mechanism at RT can also be easily estimated by the saturation trends. The result exhibits that the charge loss mechanism is dominant for the PV3 and PV2 states, while the charge gain is dominant for the PV1 and ERS states in the long term. It is mainly due to the TAT mechanism. The electric field on the tunneling oxide layer determines the

direction for the TAT mechanism. Since the physical characteristics of each mechanism are considered in the new lifetime estimation model, this method provides a much more accurate lifetime prediction, even at the non-measured temperature regime including RT.

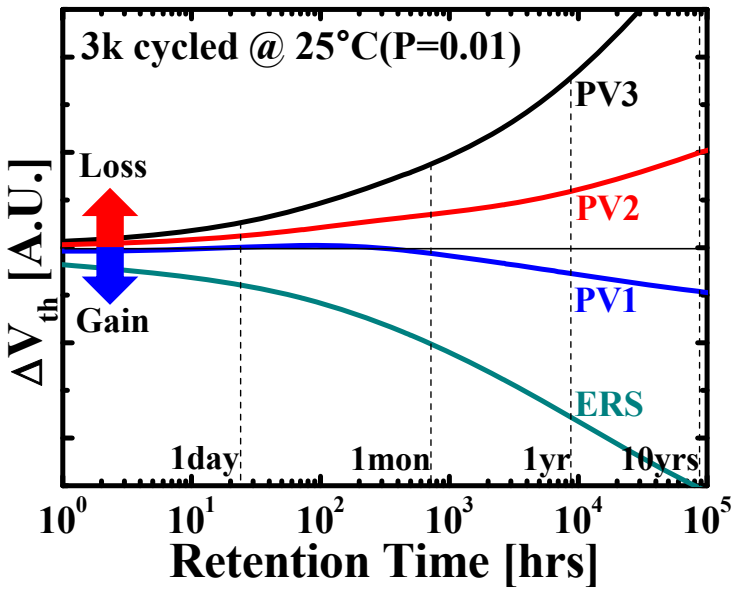


Fig. 5.8. Charge loss/gain behaviors at RT for 3k-cycled NAND flash memory in all states. The results are simulated by using the new compact model.

5.4 Lifetime Estimation for the Next Generation

In order to develop next generation of NAND flash memory, the research and development costs are enormous. In this reason, it is important to calculate profits and losses based on accurate estimation on electric properties and lifetime for the device. However, the lifetime for the device is abruptly reducing with scaling. Therefore, lifetime estimation for the next generation is a major consideration. In this section, lifetime estimation for the next generation of NAND flash memory is analyzed using 3D TCAD simulation. The structure specifications in various generations are determined refer to the 2013 International Technology Roadmap for Semiconductors (ITRS) projects [71]. The values are summarized in Table. 5.1. In this work, coupling ratio is set to be 0.6.

Fig. 5.9 shows the technology computer aided design (TCAD) device simulation results for electric field distribution at tunneling oxide layer for the next generation of NAND flash memory when program pulse is applied (the electric field distribution when erase pulse is applied is symmetric with the condition with program pulse). The target program V_{th} is 3 V. The length (or width) of active layer for the next generation is about 0.71 times smaller than that of the current generation which means the memory density becomes doubled. When the P/E cycling stress is applied, the effective electric field becomes increasing and the field distribution is changing, as device dimension is reduced. First, we analyze the electric distribution on tunneling oxide layer when program stress is analyzed according to the device scaling. Using the electric distribution, the trends with scaling for each parameter values in the proposed charge loss model is estimated.

TABLE 5.1

STRUCTURE SPECIFICATION ACCORDING TO THE GENERATIONS.

Category	Generation and structure spec.				
	1y nm	1x nm	2y nm	2x nm	3x nm
T_{ox} thickness	6.6	6.7	6.8	6.9	7
ONO	3/3/5	3/3/5	3/3/5	3/3/5	3/3/5
FG height	20.3	23	24	27	29.3

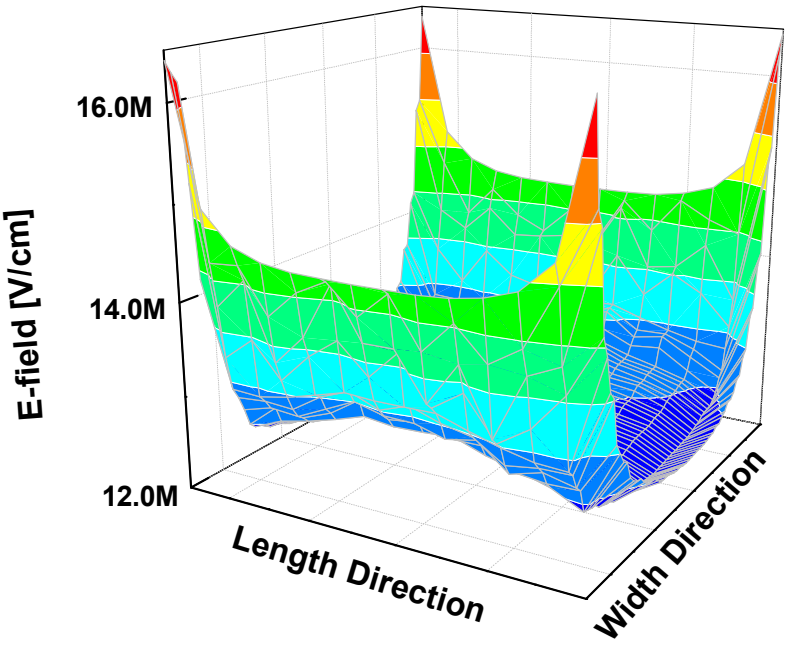


Fig. 5.9. Electric field distribution at tunneling oxide layer for the next generation of NAND flash memory when program pulse is applied.

5.4.1 Detrapping Parameter Extraction

Trap generation has been identified as a serious problem in non-volatile memory devices, leading to data retention and program-cycling endurance limitations, long before dielectric breakdown is important [72]. Reliability issue is mainly due to trap in the tunneling oxide. The trap density becomes increasing high electric field and tunneling current during P/E cycling stress [26]. We assume that the amount of the detrapping source is proportional to the amount of the generated N_{ot} traps. Electric field enhanced N_{ot} trap generation model can be expressed by following equation [72]:

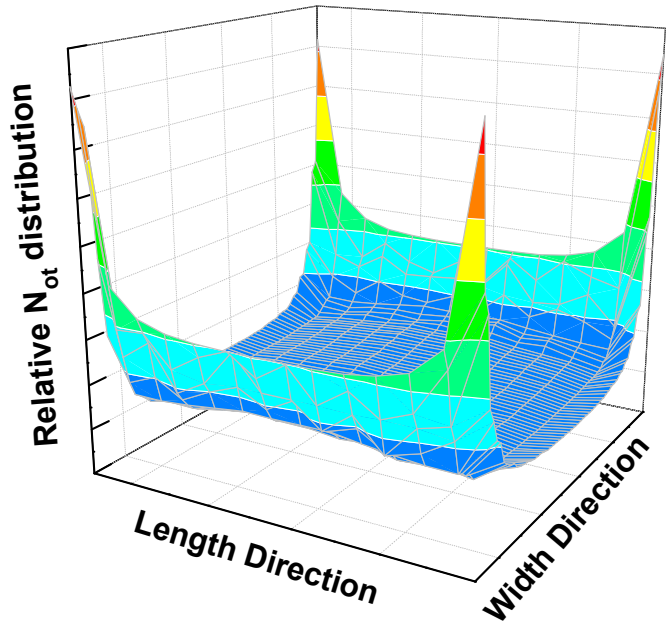
$$\Delta N_{ot(Generation)} \propto \mathrm{A} \times \exp\left(\frac{\left(-0.32 + \mathrm{a} \times E_{ox}\right) eV}{kT}\right) \tag{5.5}$$

where A is proportional constant, a is field acceleration parameter (~0.012 cm/MV), and E_{ox} is electric field in tunneling oxide, respectively.

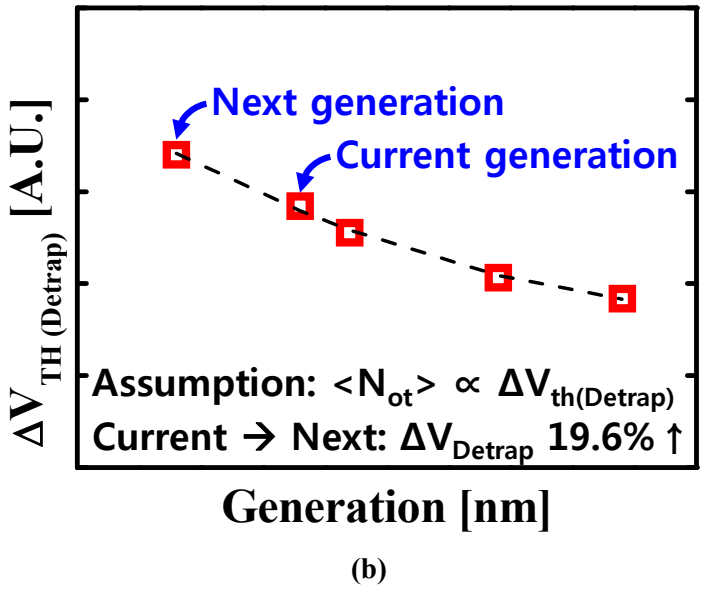
Fig. 5.10 shows calculated relative N_{ot} trap distribution using Eq. (5.5) in tunneling oxide layer for the next generation and calculated final ΔV_{th} of the detrapping mechanism according to scaling. We assume that the amount of the detrapping source is proportional to the amount of the generated N_{ot} traps and the final ΔV_{th} of the detrapping mechanism is proportional to the average value of N_{ot} trap distribution. Since the final ΔV_{th} of the detrapping mechanism was extracted in section 4.3, the final ΔV_{th} of the detrapping mechanism for the next generation can be calculated through calibration using relative N_{ot} trap distribution. In the next generation, the final ΔV_{th} of the detrapping mechanism may

increase about 19.6 % compared to the current generation. However, the time-constant for the detrapping mechanism (τ_{Detrap}) may be almost similar value because it is proportional to average detrapping time for each trap site and it is almost one-step process. It means τ_{Detrap} has weak density dependence. Therefore, we assume that the time-constant for the detrapping mechanism (τ_{Detrap}) in the next generation is the same with the value in the current generation.

Fig. 5.11 shows the trend for the detrapping parameters according to the device scaling down. The dashed line is expected trend, which is extracted using 3D simulation as shown in Fig. 5.10. The red rectangular symbols are extracted by experimental retention tests in various generations of NAND flash memory. The previous generations (3x nm, 2x nm, and 2y nm) is extracted in test element group (TEG) cells. However, the current generation (1x nm) is extracted in the main-chip. In order for an accurate comparison in the generation dependence, the current generation (1x nm) is extracted at probability level is 0.5 (P = 0.5) [58] and the previous generations are extracted with beta values in section 4.3. (Previously, we assume that beta values are '1' in section 3.). The experimental results and the simulation works are in good agreement in both final ΔV_{th} and time-constant of the detrapping mechanism.

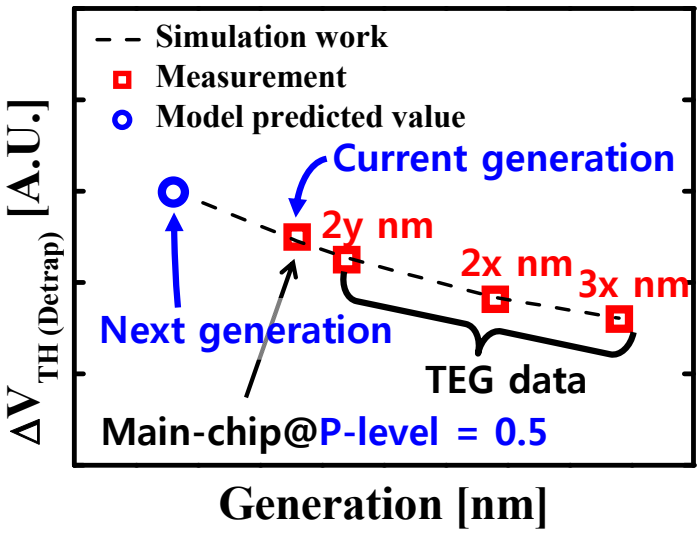


(a)

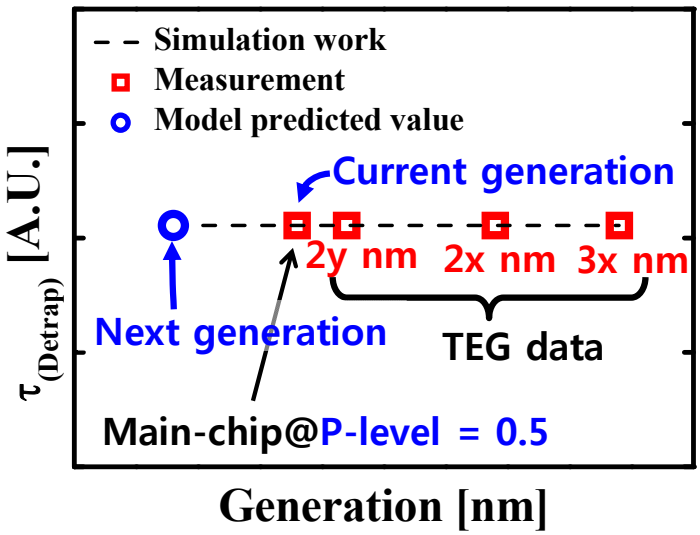


(b)

Fig. 5.10. (a) Calculated relative N_{ot} trap distribution in tunneling oxide layer for the next generation. (b) Calculated final ΔV_{th} of the detrapping mechanism according to scaling.



(a)



(b)

Fig. 5.11. Verification for the simulation works in (a) final ΔV_{th} and (b) time-constant of the detrapping mechanism using measurement data of various generations.

5.4.2 N_{it} recovery Parameter Extraction

P/E cycling stress induces interface trap generation and part of the generated interface traps become recovery with time [28]. We assume that the amount of N_{it} recovery is proportional to the amount of the generated interface traps. Electric field enhanced interface trap generation model can be expressed by following equation [73]:

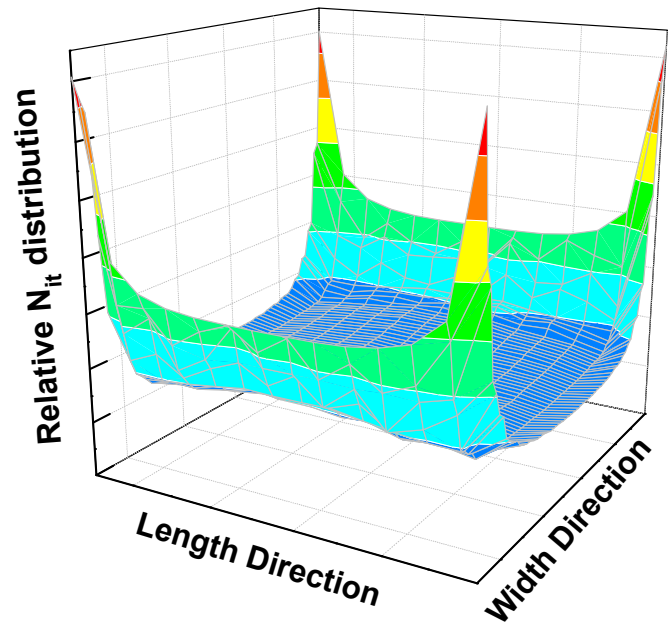
$$\Delta N_{it(Generation)} \propto \mathrm{A} \times \exp\left(\frac{2\gamma E_{\mathrm{ox}}}{3} \right) \tag{5.6}$$

where A is proportional constant, γ is field acceleration parameter (~0.6 cm/MV), and E_{ox} is electric field in tunneling oxide while erase pulse is applide, respectively.

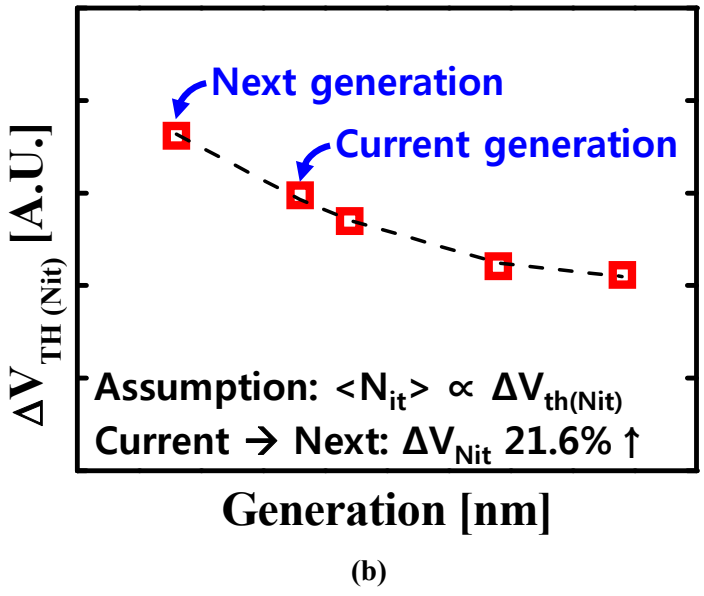
Fig. 5.12 shows calculated relative N_{it} trap distribution using Eq. (5.6) in tunneling oxide layer for the next generation and calculated final ΔV_{th} of the N_{it} recovery mechanism according to scaling. We assume that the amount of N_{it} recovery is proportional to the amount of the generated interface traps and the final ΔV_{th} of the N_{it} recovery mechanism is proportional to the average value of N_{it} trap distribution. Since the final ΔV_{th} of the N_{it} recovery mechanism was extracted in section 4.3, the final ΔV_{th} of the N_{it} recovery mechanism for the next generation can be calculated through calibration using relative N_{it} trap distribution. In the next generation, the final ΔV_{th} of the N_{it} recovery mechanism may increase about 21.6 % compared to the current generation. However, the time-constant for the N_{it} recovery mechanism (τ_{Nit}) may be almost similar value because it is proportional to average recovery time for each trap site. It means τ_{Nit} has weak density

dependence. Therefore, we assume that the time-constant for the N_{it} recovery mechanism (τ_{Nit}) in the next generation is the same with the value in the current generation.

Fig. 5.13 shows the trend for the N_{it} recovery parameters according to the device scaling down. The dashed line is expected trend, which is extracted using 3D simulation as shown in Fig. 5.12. The red rectangular symbols are extracted by experimental retention tests in various generations of NAND flash memory. The previous generations (3x nm, 2x nm, and 2y nm) is extracted in TEG cells. However, the current generation (1x nm) is extracted in the main-chip. In order for an accurate comparison in the generation dependence, the current generation (1x nm) is extracted at probability level is 0.5 (P = 0.5) [58] and the previous generations are extracted with beta values in section 4.3. (Previously, we assume that beta values are '1' in section 3.). The N_{it} recovery mechanism has very fast time-constant and small final ΔV_{th}. Therefore, it is difficult to extract accurate values in both time-constant and final ΔV_{th}. In Fig. 5.13(a), the experimentally extracted final ΔV_{th} values of N_{it} recovery mechanism have similar range with the simulation-based trend (dashed line) in all generations. Therefore, the final ΔV_{th} value for the next generation is reasonable result. In Fig. 5.13(b), the experimentally extracted time-constant of N_{it} recovery mechanism for TEG data have similar values. However, there is a gap between the main-chip data (current generation) and TEG data (previous generations). Since the time-constant of N_{it} recovery mechanism is relatively much shorter than the others, there could be measurement delay [57]. Considering the measurement delay, we assume that the time-constant for the N_{it} recovery mechanism for the next generation may be almost similar value with the current generation.

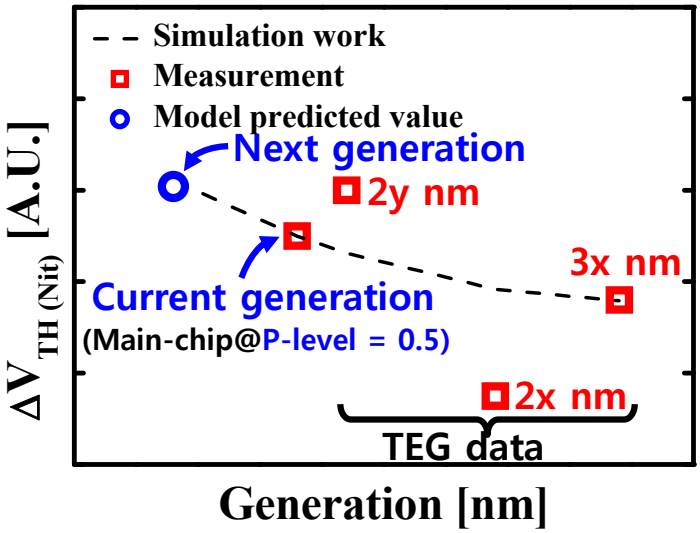


(a)

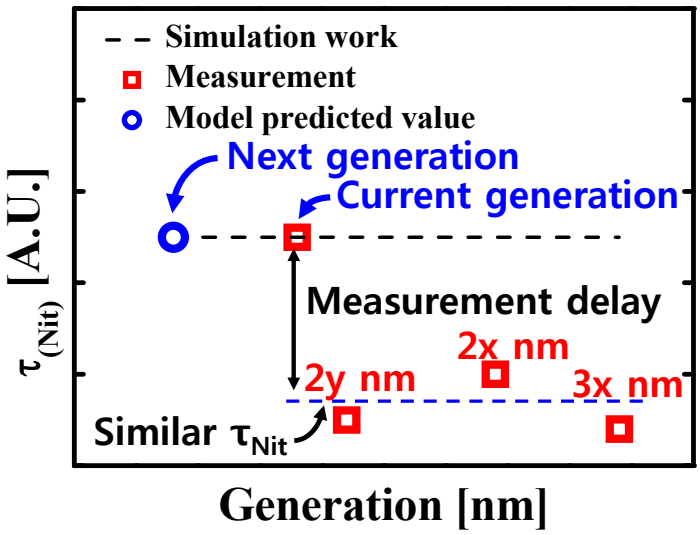


(b)

Fig. 5.12. (a) Calculated relative N_{it} trap distribution in tunneling oxide layer for the next generation. (b) Calculated final ΔV_{th} of the N_{it} recovery mechanism according to scaling.



(a)



(b)

Fig. 5.13. Verification for the simulation works in (a) final ΔV_{th} and (b) time-constant of the N_{it} recovery mechanism using measurement data of various generations.

5.4.3 TAT Parameter Extraction

Fig. 5.14 shows electric field across the tunneling oxide layer in channel length direction when program pulse is applied at various generations of NAND flash memory. The results show that the strength of maximum electric field is all the same regardless of generations. Electric field is much more crowding in corner regime. About 1.3 nm from the edge, abrupt electric field change was observed [see Fig. 5.14(a)]. Therefore, we assume that width of high field regime is the same regardless of the generation.

There are two main factor to determine the $\Delta V_{th(\mathrm{TAT})}$.

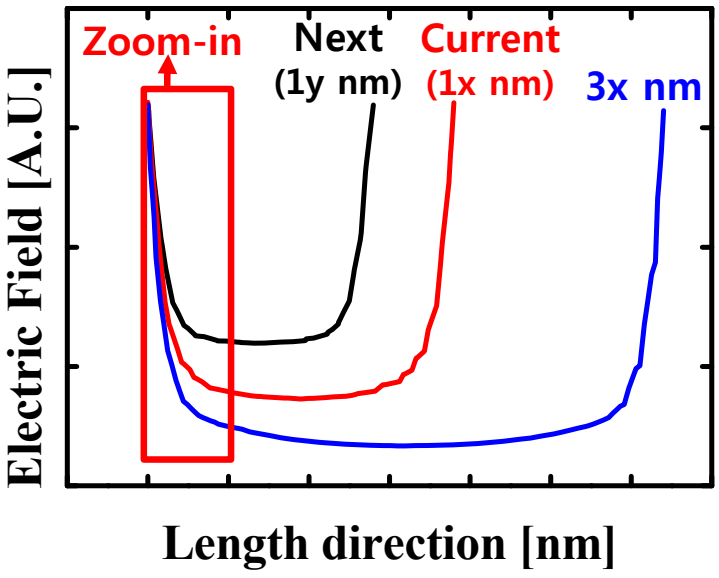
1) Number of electrons in FG

The absolute number of electrons in FG becomes decreasing and single electron effect is increasing with the device scaling [14]. However, the initial V_{th} is the same for all the generations (V_{th} = 3 V). Also, $\Delta V_{th(\mathrm{TAT})}$ is much larger than the other mechanisms' sources ($\Delta V_{th(\mathrm{Nit})}$, $\Delta V_{th(\mathrm{Detrap})} << \Delta V_{th(\mathrm{TAT})}$). The decreased part for $\Delta V_{th(\mathrm{TAT})}$ due to increased parts for the others ($\Delta V_{th(\mathrm{Nit})}$, $\Delta V_{th(\mathrm{Detrap})}$) can be ignorable. Therefore, the number of electrons per dimension should be almost the same.

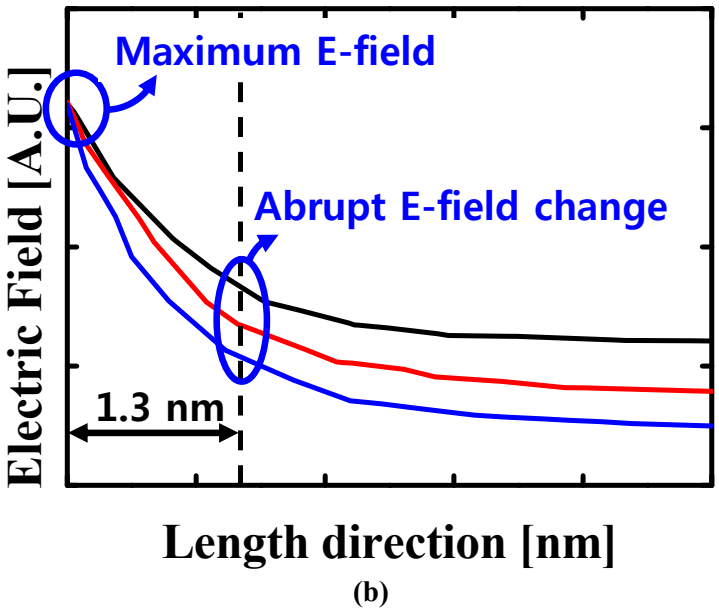
2) Trap density around the percolation path

Larger trap density around the percolation path reduces the energy barrier. Therefore, more electrons can leak out from FG to substrate [57]. This effect is main factor to determine the $\Delta V_{th(\mathrm{TAT})}$.

Percolation path could be generated in the corner regime due to the higher electric field. However, maximum electric field is the same regardless of the generation. Therefore, we assume that the $\Delta V_{th(\mathrm{TAT})}$ is the same in the next generation.



(a)



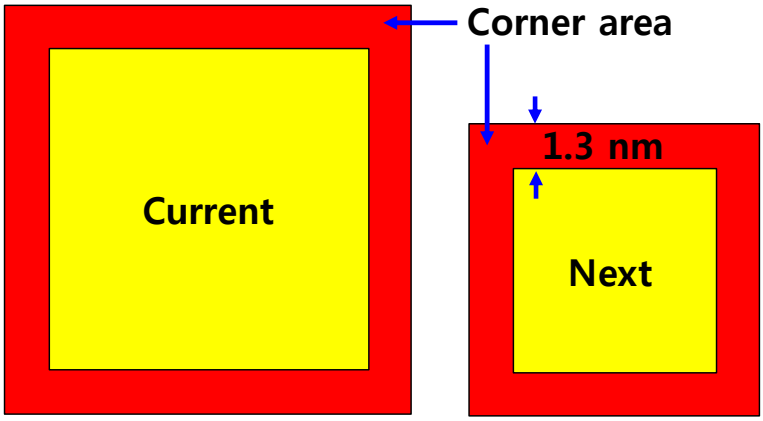
(b)

Fig. 5.14. Electric field at tunneling oxide for various generations (a) across the length direction and (b) corner regime when program pulse is applied.

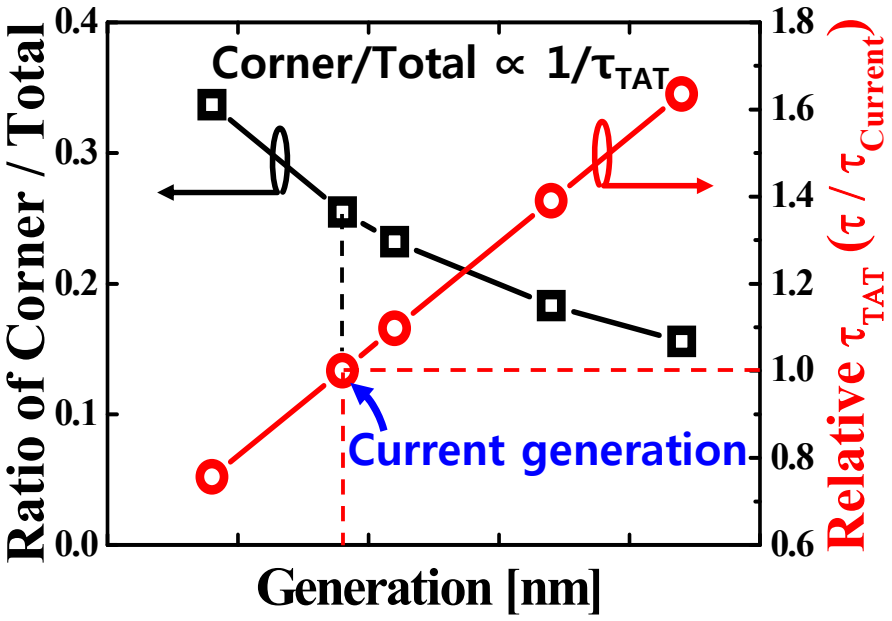
Fig. 5.15(a) shows the schematic to explain the portion of the corner area over total active area according to the generations. As the device scaled, the portion of corner area is larger. We assume that TAT mechanism is occurred only in the corner regime due to much higher trap density. Previously, we assumed that the $\Delta V_{th(\mathrm{TAT})}$ is the same regardless of the scaling due to the same strength of maximum electric field. However, the leakage path is wider since the portion of corner area (corner area/total area) becomes increasing. Therefore, time-constant for the TAT mechanism should be shorter in the next generation compared to the current generation. If the TAT mechanism is only occurred in the corner area, the time-constant for the TAT mechanism should be inversely proportional to the portion of corner area.

Fig. 5.15(b) shows the calculated ratio of corner/total and relative time-constant for the TAT mechanism according to the device scaling. In this work, constant width for the corner area (1.3 nm) is used in all the generations to simplify. The dimension of corner area can be calculated as: L x W – [(L – 2.6) x (W – 2.6)]. L is channel length and W is channel width. The calculated time-constant of the TAT mechanism for the next generation shows a 32.2% reduction compared to the current generation.

Fig. 5.16 shows the trend for the TAT parameters according to the device scaling down. The dashed line is expected trend, which is extracted using 3D simulation as shown in Fig. 5.15. The red rectangular symbols are extracted by experimental retention tests in various generations of NAND flash memory. The previous generations (3x nm, 2x nm, and 2y nm) is extracted in TEG cells. However, the current generation (1x nm) is extracted in the main-chip. In order for an accurate comparison in the generation dependence, the current

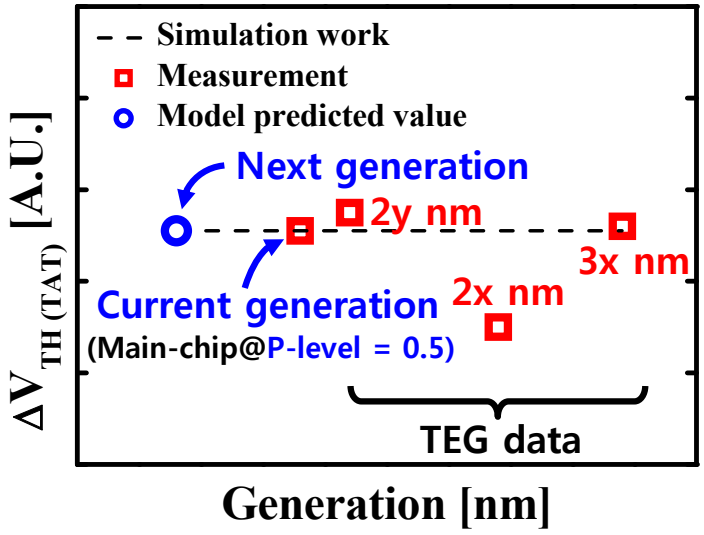


(a)

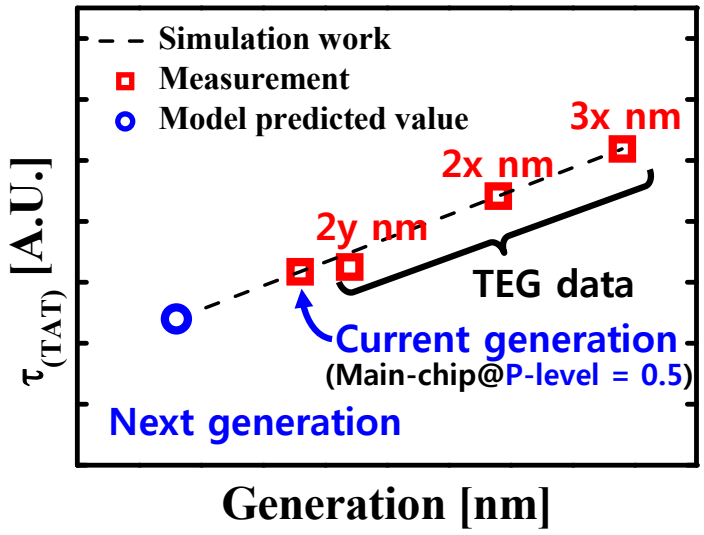


(b)

Fig. 5.15. (a) Schematic to explain the portion of the corner area over total active area according to the generations. (b) Ratio of corner/total and relative time-constant for the TAT mechanism according to the device scaling.



(a)



(b)

Fig. 5.16. Verification for the simulation works in (a) final ΔV_{th} and (b) time-constant of the TAT mechanism using measurement data of various generations.

TABLE 5.2

EXPECTED RELATIVE PARAMETER VALUES FOR

THE NEXT GENERATION OF NAND FLASH MEMORY.

	$\Delta V_{th(Nit)}$	$\Delta V_{th(Detrap)}$	$\Delta V_{th(TAT)}$	τ_{Nit}	τ_{Detrap}	τ_{TAT}
Next Gen. (compared to current)	**21.6% ↑**	**19.6% ↑**	**~similar**			**32.2% ↓**

generation (1x nm) is extracted at probability level is 0.5 (P = 0.5) [58] and the previous generations are extracted with beta values in section 4.3. (Previously, we assume that beta values are '1' in section 3.). The experimental results and the simulation-based trend are in good agreement in both final ΔV_{th} and time-constant of the TAT mechanism. Therefore, the final ΔV_{th} and time-constant of the TAT mechanism for the next generation are estimated using the simulation-based trend and the results are very reasonable. All the expected relative parameter values for the next generation of NAND flash memory are summarized in Table 5.2.

5.4.4 Lifetime Estimation Results according to the Generations

Fig. 5.17. shows the estimated device lifetime according to generation and P/E cycling times. The criterion of ΔV_{th} is 0.2 V. The results show that P/E cycling reduces the lifetime in all generation. Also, lifetime becomes shorter with the device scaling. The reason for this is dominantly electric field crowding effects. Higher electric field generates more traps so that the sources of the interface trap recovery and the detrapping mechanisms are increasing in the next generation. Also, the portion of corner area is larger with the device scaling so that the time-constant for the TAT mechanism becomes shorter. As a result, the lifetime for the next generation becomes shorter. In this analysis, the lifetime reduction is about 34 % when the criterion of ΔV_{th} is 0.2 V.

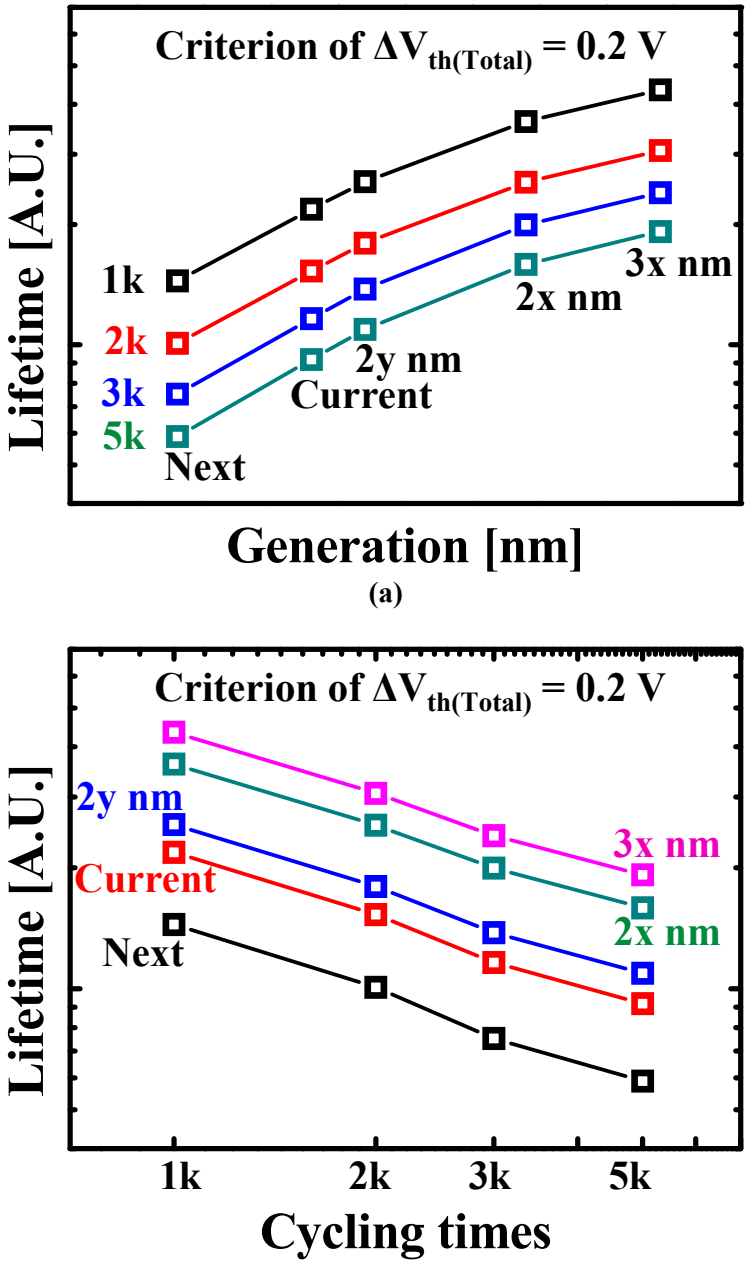


Fig. 5.14. Estimated device lifetime according to (a) generation and (b) P/E cycling times. The criterion of ΔV_{th} is 0.2 V.

5.5 Summary

Misunderstanding on apparent activation energy (E_{aa}) can cause serious error in the lifetime predictions. In this chapter, the E_{aa} characteristics for sub 20-nm NAND flash memory are investigated and accurate lifetime for NAND flash memory is estimated by two different proposed models. In a high-temperature (HT) regime, interface trap (N_{it}) recovery mechanism has the greatest impact on the charge loss. However, the values of E_{aa} and $E_{a(\mathrm{Nit})}$ have wide difference. Also, lifetime of the device cannot be estimated by the Arrhenius model due to the E_{aa} roll-off behavior. For the first time, we reveal the origin of abnormal characteristics on E_{aa}. The E_{aa} is determined by not only each $E_{a(\mathrm{mechanism})}$ value but also the change rate of the CR with baking temperature. We derive a mathematical formula for E_{aa} as a function of each $E_{a(\mathrm{mechanism})}$ in NAND flash memory. Two different accurate lifetime estimation models for sub 20-nm NAND flash memory are proposed. Firstly, accurate lifetime for the device is estimated by integrating the proposed E_{aa} equation. Secondly, the accurate lifetime is calculated by extrapolations of the trends for extracted parameters. Since the proposed models are developed based on physical retention characteristics of various mechanisms, it provides very accurate result of the lifetime prediction on NAND flash memory. Also, the lifetime estimation for the next generation of NAND flash memory is analyzed using 3D TCAD simulation. Each mechanism's component in the proposed charge loss model is calculated using electric field distribution with scaling. As a result, the lifetime for the next generation becomes shorter as much as 66 % of the lifetime in the current generation when the criterion of ΔV_{th} is 0.2 V.

Conclusions

In this dissertation, we investigate abnormal retention characteristics and introduce a physical based new charge loss model for sub 20-nm MLC NAND flash memory. We also propose two accurate lifetime prediction methods for the device.

In Chapter 1, varilus reliability issues and failure mechanisms in highly scaled NAND flash memory device are reviewed. Also, Motivation and organization for this thesis are introduced. In Chapter 2, serious drawbacks of conventional lifetime estimation model are reviewed. This Arrhenius model is used under the assumption that the E_{aa} is constant with temperature. However, it varies with retention conditions so that the calculated lifetime prediction has huge error. We propose new charge loss model, based on the physical retention characteristics. A detailed review on physical meaning of the parameters is also covered. In Chapter 3, we completely separate the dominant failure mechanisms and extract the E_a of each mechanism in various generations (A, B, C) of NAND flash TEG cells. We analyze the retention characteristics of each mechanism for different generations and P/E cycling times. The results show that the E_a for the detrapping mechanism has extremely weak dependence not only on the generation but also on the cycling times. However, the E_a for the TAT mechanism has strong dependent on both. In Chapter 4, abnormal retention characteristics such as E_{aa} roll-off behavior in the PV3 state and negative E_{aa} behavior in the ERS state are observed in sub 20-nm MLC NAND flash memory main-chip. Also, whole detailed procedure of parameter extraction

is explained. The parameters are extracted at all states (PV3, PV2, PV1, ERS). Contribution rate (CR) of the each mechanism is extracted at specific criterion of $|\Delta V_{th\_Total}|$ according to the baking temperature. From the results, the abnormal retention behaviors such as E_{aa} roll-off at the PV3 and negative E_{aa} at the ERS states are physically analyzed. Retention behavior is analyzed in various conditions of the states, P/E cycling, probability level of V_{th} distribution. Also, the detrapping mechanism is deeply analyzed using 3D TCAD simulation. As a result, trap profile in the tunnel oxide is extracted in space and energy distributions. In Chapter5, the general equation of E_{aa} is derived as a function of each $E_{a(\text{mechanism})}$. We also propose two accurate lifetime estimation models for sub 20-nm NAND flash memory. The first one is the integration method using the proposed E_{aa} Equation. The second one is the advanced extrapolation method using the trends of extracted parameters. As the proposed models are developed based on physical characteristics of various mechanisms, it offers very accurate prediction on the lifetime of NAND flash memory. Using 3D TCAD simulation, lifetime for the next generation of NAND flash memory is estimated. As the device is scaled, electric field in the tunnel oxide is more crowed and it induces more N_{it} and N_{ot} traps. As a result, the lifetime for the next generation becomes shorter.

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초 록

NAND 플래시 메모리가 지속적으로 고집적, 소형화 되어감에 따라 다양한 신뢰성 문제에 취약해지고 있다. 결과적으로, 제품의 양산을 위해 소자의 정확한 수명 예측은 가장 중요한 주제 중 하나가 되었다. 하지만, NAND 플래시 메모리에는 다양한 불량 메커니즘이 혼재되어 있기 때문에 기존의 고온-가속 평가 방법으로 추출한 겉보기 활성화 에너지 (E_{aa}) 가 Arrhenius 모델을 따르지 않기 때문에 기존 모델로 예측한 수명은 실제 수명을 반영하지 못하고 큰 오차를 야기한다. 따라서, 소자의 정확한 수명을 예측할 수 있는 새로운 모델 개발이 절대적으로 필요하다. 일반적으로 잘 알려진 주요 불량 메커니즘으로는 detrapping, interface trap (N_{it}) recovery, trap-assisted tunneling (TAT) 메커니즘 등이 있다.

본 논문에서는 새로운 전하 손실/이득 모델을 제안하고, 여러 세대의 NAND 플래시 TEG cell 과 20-nm 이하급 MLC NAND 플래시 main-chip 에서 세가지 불량 메커니즘을 완벽하게 분리하였다. 결과적으로, 각 불량 메커니즘은 고유의 활성화 에너지 (E_a) 를 가지며, 온도에 따른 각 메커니즘의 시상수는 Arrhenius 모델을 잘 따름을 확인하였다. 우리는 다양한 retention 조건에서 각 메커니즘의 E_a 비교 및 분석을 통해 각 메커니즘의 물리적 특성을 심도있게 분석하였다. 우리는 또한 불량 기준 (ΔV_{th_Total}) 에 기여하는 각 메커니즘의 기여도를 온도에 따라 추출하였다. 이 결과로부터 PV3 state 에서의 E_{aa} roll-off 현상이나 ERS state 에서의 negative E_{aa} 현상과 같은 비이상적인 리텐션 특성에 대한 물리적 원인을 분석하였다. 또한, 3 차원

시뮬레이션을 이용하여 P/E cycling 스트레스로 인한 산화막에 생성되는 트랩의 공간과 에너지상의 분포를 예측하였다.

우리는 세계최초로 NAND 플래시 메모리에서의 비이상적인 E_{aa} 특성의 원인을 밝혔으며, E_{aa} 와 각 메커니즘의 E_a 의 관계를 수학적으로 유도하였다. 우리는 앞서 분석한 내용을 바탕으로 두 가지 새로운 수명평가 모델을 제안하였다. 첫번째 모델은 앞서 유도한 E_{aa} 수식을 적분하여 수명을 예측하는 방법이다. 두번째 모델은 새로운 전하 손실/이득 모델식으로 추출한 각 파라미터의 온도에 따른 경향을 외삽법으로 예측하는 방법이다. 새롭게 제안된 모델을 이용하여 NAND 플래시 메모리의 모든 states (PV3, PV2, PV1, and ERS) 에 대한 정확한 수명을 예측하였다. 우리가 제시한 모델을 이용한 수명 예측 결과와 기존 Arrhenius 모델을 이용한 수명 예측 결과에서 크게는 수십배에 가까운 차이가 발생함을 확인하였다. 우리의 새롭게 제안한 모델은 여러 불량 메커니즘의 물리적 특성을 충분히 반영하고 있기 때문에 NAND 플래시 메모리의 수명을 매우 정확하게 예측한다고 할 수 있다. 또한, 3 차원 시뮬레이션을 이용하여 다음세대 소자의 수명을 예측하였다. 먼저, 소자의 scaling 에 따른 tunnel oxide 에서의 전계 분포를 분석하여, 이를 이용하여 각 메커니즘의 상대적 크기를 예측한 결과, 다음세대 소자의 수명은 현재 세대 소자의 수명 대비 34%정도 단축될 수 있음을 확인하였다.

주요어 : 낸드 플래시 메모리, 불량 메커니즘, 아르헤니우스 모델, 활성화 에너지, 쓰기/지우기 반복 스트레스, 수명 예측

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