Ph.D. DISSERTATION

Field-Effect Transistors based on Organic and Carbon Nanotube for Memory Devices

메모리 소자를 위한 유기물과 탄소 나노튜브 기반의 전계 효과 트랜지스터에 관한 연구

BY

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DEPARTMENT OF ELECTRICAL ENGINEERING AND
COMPUTER SCIENCE
COLLEGE OF ENGINEERING
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지도 교수 홍 용 택

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Abstract

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With continued development in flexible and large area devices, there is increasing interest organic semiconductor materials and other semiconductor materials such as carbon based materials instead of traditional silicon based materials in electronic devices. These materials have intrinsic flexibility and versatile processing capability, which provide a broad range of applications in electronic device such as active-matrix organic light-emitting diode (AMOLED), logic circuit, and thin film transistors (TFTs) instead of conventional silicon based materials. Among these applications, TFTs are key elements for practical applications in flexible displays, logic circuits and memory applications such as memory transistors. In memory transistor devices, conventional thin films floating gate have been used for charge

floating gate, but these conventional memory devices encounter difficulties of floating gate cell-to-cell interference and parasitic capacitance, and charge loss; these affect the overall device performance and reliability, when used with miniaturized cell sizes and in high densities. So many groups reported discrete nano-floating gate memory using metal nanoparticles such as gold nanoparticle because discrete nanoparticles have advantages that it is easy to control the trap density and distribution. Among the various potential candidates for the charge storage layer, graphene offers an advantage of introducing metallic properties. However, the two-dimensional continuous planar structure of graphene typically has difficulty in storing sufficient charge for non-volatile memory function, because the charge carrier stored in the continuous charge storage layer is easily lost through the thin tunneling dielectric. From this point, floating gate memory transistor using discrete charge floating gate are discussed by controlling synthesize of graphene in this thesis. We fabricated the graphene floating gate into the organic nonvolatile memory transistors (ONVMT) with bottom-gate/top-contact structure using pentacene and polystyrene (PS) as active and charge tunneling dielectric layers, respectively. For the floating gate, we proposed a discrete graphene layer formed by controlling growth time of the graphene layer during a conventional CVD process, and then simply transferring it onto the gate dielectric layer. The fabricated ONVMTs exhibited large memory windows (～40 V) and a good data retention ability. The shift of the transfer curves at various gate biases indicated a clear charge-trapping and de-trapping behavior in the partially grown graphene within a short period of time (100 ms). The data retention properties of our devices showed an on/off ratio of

about 5×10^4 even after 10^5 s, which leads to the estimated charge storage time of more than a year. The fabricated ONVMTs were reliable after more than one-hundred repeated programming/erasing cycle tests.

Furthermore, we also fabricated SWCNT transistors based on inkjet printing technology for logic circuit applications. The carbon nanotubes (CNTs) has been widely studied for many aspects in recent years for their unique properties, which are valuable for nanotechnology, electronics, optics and other fields of materials science and technology. In particular, single-walled carbon nanotubes (SWCNTs) shows high electrical conductivity or semiconducting behavior according to their rapping direction. From these electrical properties, SWCNTs, especially semiconducting SWCNTs, have been expected to be used as alternative semiconducting material for field effect transistors. Based on these backgrounds, we illustrated SWCNT transistors based on inkjet printing technology for high performance and uniformity and illustrated advantages of inkjet printing method compared to other deposition method. For successful inkjet printing of SWCNTs solution, we optimized jetting conditions such as ink jetting velocity and drop-space. In SWCNT transistor, it is critical that the ink wets the targeted surface uniformly since networks of SWCNTs are formed during the drying of the ink. To deposit high density and uniform SWCNT films on substrate, we used surface treatment with poly-L-lysine (PLL) to enhance adhesion between SWCNTs and substrate. Also for source and drain in SWCNT transistor, we deposited Ag using inkjet printing method. Fabricated device showed high electrical performance and high uniformity without additional patterning. Also from this inkjet-printed SWCNT transistor, we fabricated

SWCNT circuit applications including inverter and SRAM by using inkjet-printing method. For full-swing SWCNT inverter, we used chemical encapsulation with ammonium hydroxide (NH_4OH). Also using this full-swing inverter, we fabricated SWCNT RAM by connecting two inverters' input and output.

Keywords: memory device, thin-film transistor (TFTs), organic semiconductor, graphene, floating gate, single-wall nanotube (SWCNT), inkjet-printing, inverter, static random access memory (SRAM)

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Chapter 1

Introduction

1.1 Organic Non-Volatile Memory Transistors

Recently, semiconductor device technology has been continually developed rapidly. As Moore's law, the number of transistors in a dense integrated circuit doubled approximately every two years since 1975. [1] As the process of fabrication become simple, the cost of fabrication continues to be lowered and their density has increased because of the size of semiconductor devices has decreased. There are many types of semiconductor devices, including switching devices, memory devices, and display device. [2] Among these many types of semiconductor devices, nowadays, there is a great interest in memory device because the amount and type of information are increasing rapidly. Especially, this memory device is widely used for data storage including computer, mobile phone, and many other portable devices. [3-6] In these devices, non-volatile memory property is important for data

storage. This means the stored data is maintained even when the power of device turned off. Therefore, many research groups have been made efforts to improve their device properties and lower their fabrication cost. [7, 8] In these memory devices, there are currently several types of devices available, which are categorized on the basis of their operating methods. Among these, memory transistor using a floating gate as the charge storage layer have been widely studied owing to their non-destructive data processing, reliable data storage, and simple structure; which typically comprises a single transistor so device scaling is easier than other types of memory devices. [9, 10] This memory device uses the threshold voltage shifts for data storage according to the memory states (programmed/ erased states) and their states can be verified by measuring the drain currents at reading biases. In all floating gate memory transistors, the memory properties can be determined by the floating gate and tunneling dielectric. So it is important to choose these floating gate and tunneling dielectric to improve the memory device's properties. To date, conventional thin films floating gate have been used in memory transistor devices, but these conventional memory devices encounter difficulties of floating gate cell-to-cell interference and parasitic capacitance, and charge loss; these affect the overall device performance and reliability, when used with miniaturized cell sizes and in high densities. [11] Therefore, many other research has been performed on flash memory devices with discrete charge trapping layers, such as silicon-oxide-nitride-oxide-silicon (SONOS) devices or nano-floating gate memory devices to replace those used in the conventional floating gates. [12, 13] Recently, some groups reported that SONOS-type flash memory device using Si_3N_4 as charge trapping layer, however, it is difficult to control the trap

density and distribution in memory device which affect memory characteristics. Another groups reported discrete nano-floating gate memory using metal nanoparticles such as gold nanoparticle as a charge floating gate. This discrete nanoparticles have advantages that it is easy to control the trap density and distribution because the density and location of the nanoparticles. [14] Among the various potential candidates for the charge storage layer, graphene offers an advantage of introducing metallic properties. [15] Therefore, it can enhance the performance of current memory devices in a facile manner, owing to its unique properties of high density of state, high work function, and low dimensionality. [16-21] However, the two-dimensional continuous planar structure of graphene typically has difficulty in storing sufficient charge for non-volatile memory function, because the charge carrier stored in the continuous charge storage layer is easily lost through the thin tunneling dielectric. Some groups have, therefore, selected to use discrete charge storage layers, such as metal nanoparticles, for the floating gate in non-volatile memory devices. [14, 22]

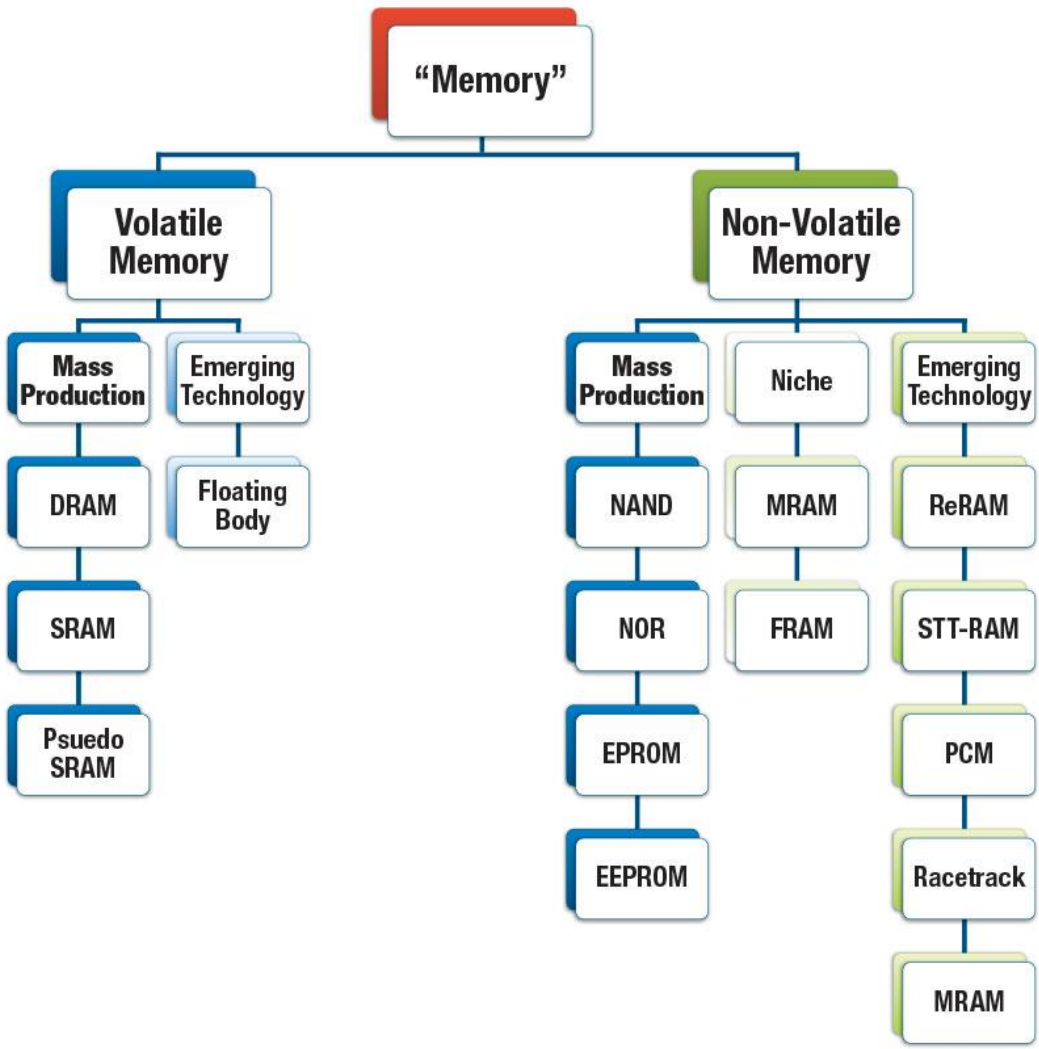

Figure 1.1. The schematic of various memory devices

1.2 Floating Gate Memory Transistors

The floating gate memory transistor is fundamental element for nonvolatile data storage device and first reported by Kahng and Sze in 1976. [23] As illustrated in Figure 1.2, the structure of floating gate memory transistor is similar to a conventional metal-oxide semiconductor field-effect transistor (MOSFET). [24] The gate of the floating gate memory transistor is electrically isolated, creating a floating node in DC, and a number of secondary gates or inputs are deposited above the floating gate and are electrically isolated from it. Since the floating gate is completely surrounded by highly resistive material, the charge contained in it remains unchanged for long periods of time. [17] For programming and erasing data in memory device, the charge is injected to the floating gate to change the threshold voltage by applying bias to gate electrode. The two modes of programming are hot-carrier injection and Fowler-Nordheim tunneling. Figure 1.3 shows the mechanisms of hot-carrier injection. Near the drain, the lateral field is at its highest level. The channel carriers acquire energy from the field and become hot carriers. When their energy is higher than the barrier of the gate/gate dielectric interface, they can be injected to the floating gate. At the same time, the high field also induces impact ionization. These generated secondary hot carriers can also be injected to the floating gate. The hot-carrier injection currents give rise to the equivalence of gate current in a regular MOSFET. Figure 1.3 (b) shows the original method of hot-carrier injection using drain-substrate avalanche. In this scheme, the floating-gate potential is more negative such that hot holes are injected instead. This injection is less efficient and no longer used in practice. Besides hot-carrier injection,

electrons can be injected by tunneling. In this programming mode, the electric field across the bottom oxide layer is most critical. On application of a positive voltage V_G to the control gate, an electric field is established in each of the two insulators. The current transport in insulators is generally a strong function of the electric field. When the transport is Fowler-Nordheim tunneling, the current density is affected by this electric field. Using either hot-carrier injection or tunneling as programming mechanism, after charging, the total stored charge Q is equal to the integrated injection current since the gate is floating. This causes a shift of the threshold voltage by the amount.

$$\Delta V_T = -\frac{dQ}{\varepsilon}$$

This threshold-voltage shift can be directly measured as shown in the I_D-V_G plot. To erase the stored data, a negative bias is put on the control gate. The process is the reverse of the tunneling process described above, and the stored charges tunnel out of the floating gate to the substrate. The programming and erasing sequence of a floating gate memory transistor can be understood with the energy-band diagrams in Figure 1.4. In the figure, E_C and E_V are the conduction and valence bands respectively, E_F is fermi level. The applied gate bias creates the electric field resulting in a potential barrier. This barrier provides a path for the electrons in the substrate to tunnel through the thin gate oxide. Without any gate bias, the device has equilibrium state as shown is Figure 1.4 (a). When a large voltage is applied at the control gate during programming, its energy band structure will be influenced as shown in Figure 1.4 (b). In this programming state, electron injection can be occurred due to hot carriers over the barrier or tunneling through the barrier. Figure

1.4 (c) shows that the accumulated negative charge at the floating gate cause the change of the threshold voltage compared to its initial condition in Figure 1.4 (a). This programmed charges are confined in floating gate because the floating gate is isolated by the dielectric. The tunneling oxide and gate oxide dielectric prevent the programmed charges from escaping. During erasing process, the energy band diagram is illustrated Figure 1.4 (d), when the large negative bias is applied to control gate. In this erasing process, the stored electrons are ejected from the floating gate to substrate. The main mechanism of the erasing process is also FN tunneling. After erasing operation, the memory device has energy band diagram of initial state as Figure 1.4 (a). Also threshold voltage of the device shifts to the negative direction due to ejected electrons. The threshold voltage shifts are illustrated in Figure 1.5 during programming and erasing operation. Read operation is verified whether the memory cell is programmed or not. If the drain current doesn't flow with applying 0V to the gate, the cell is decided to be successfully programmed. When the cell has been erased, the current would flow.

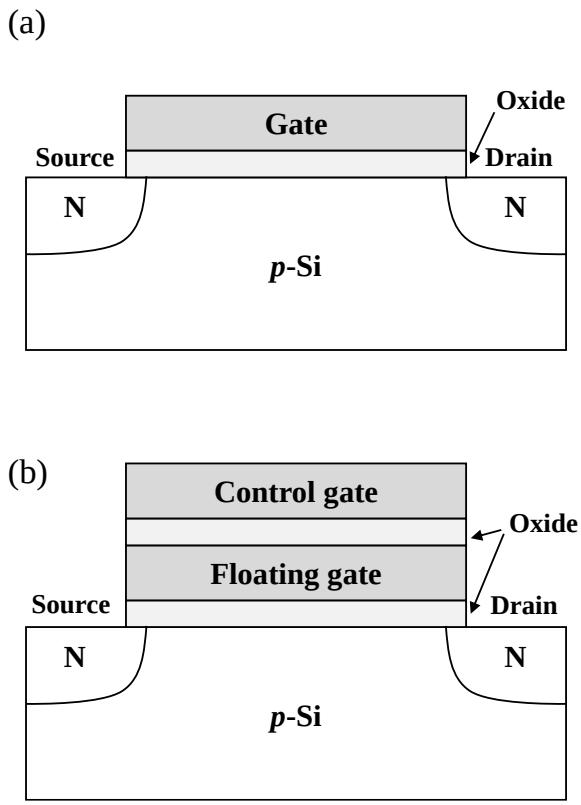

Figure 1.2 Structure of (a) field-effect transistor and (b) floating gate memory transistor

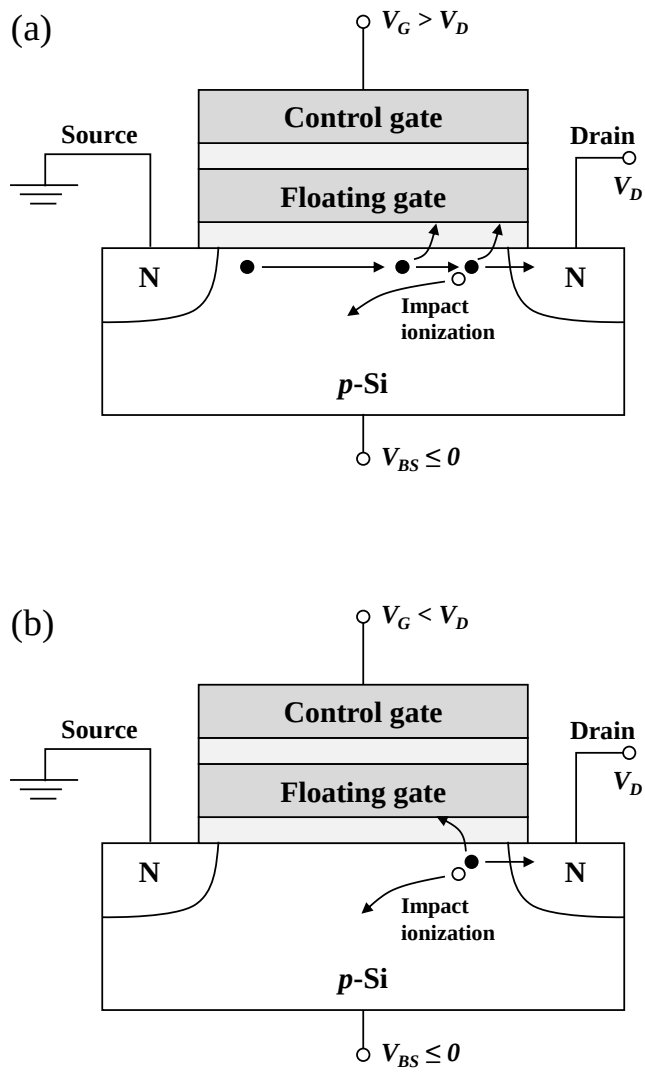

Figure 1.3 Charging of the floating gate by hot carriers. (a) Hot electrons from channel and impact ionization (b) Hot holes from drain avalanche

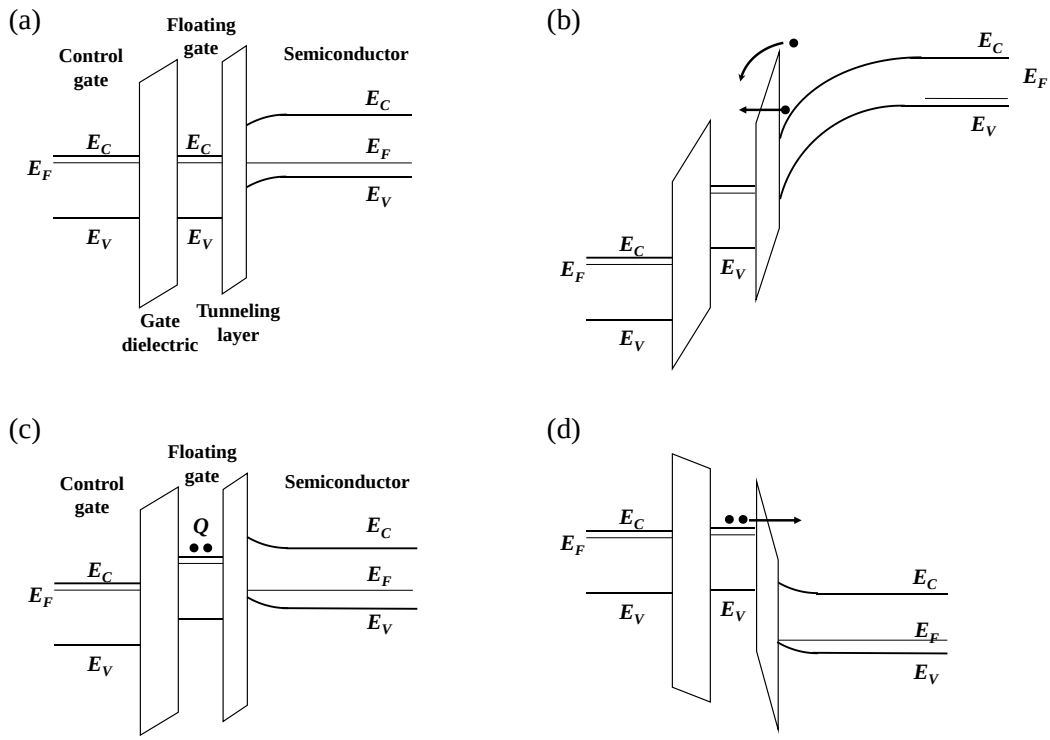

Figure 1.4 Band diagrams of floating gate memory operation in (a) Initial state (b) Programming operation (c) Programmed state (d) Erasing operation

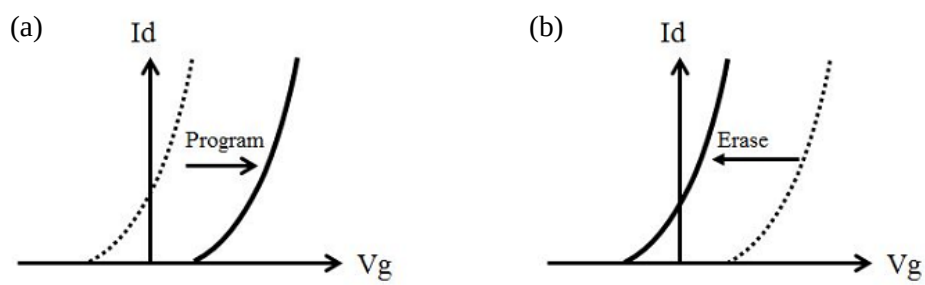

Figure 1.5 V_{th} shifts in memory transistor after (a) Programming operation (b) Erasing operation

1.3 Single-Wall Carbon Nanotube Transistors

Carbon nanotubes (CNTs) is considered as a cylinder formed by rolling a piece of graphene. The CNTs has been widely studied for many aspects in recent years for their unique properties, which are valuable for nanotechnology, electronics, optics and other fields of materials science and technology. [25-27] In particular, owing to their extraordinary thermal conductivity and mechanical and electrical properties, carbon nanotubes find applications as additives to various structural materials. [28, 29] According to its number of layers, the CNTs is divided to single-walled CNTs (SWCNTs) and multi-walled CNTs (MWCNTs). MWCNTs consist of multiple rolled layers of graphene. This MWCNTs has superior electrical conductivity. Due to their high conductivity, high aspect ratio, and natural tendency to form ropes, MWCNTs are ideal in providing inherently long conductive pathways even at ultra-low loadings. On the other hand, SWCNTs shows high electrical conductivity or semiconducting behavior according to their rapping direction. From this electrical properties, SWCNTs, especially semiconducting SWCNTs, have been expected to be used as alternative semiconducting material for field effect transistors. [26, 30] Field effect transistor are widely used and studied. In particular, thin film transistors (TFTs) are widely used for flat panel display, flexible electronics, and sensor applications. [31, 32] Various semiconducting materials have been used in TFTs applications such as α-Si, poly-silicon, organic and oxide semiconductors. Each semiconductor's properties are summarized in Table 1.1. The most common TFTs are using amorphous silicon (α-Si) or polysilicon as transistor channel. Amorphous silicon TFTs can satisfy the requirements of

large area, low-to-middle displaying speed, good uniformity, and fair stability. Poly-silicon TFTs own an advantage of high mobility. However, either of these two types of TFTs has its critical limitation so that neither of them can be widely applied in the more advanced displays. Amorphous silicon is sensitive to light. Also, the carrier mobility of the α-Si device is less than 2 $cm^2/V{\cdot}s$, which cannot satisfy the requirement of the high-speed display with a frame rate of 120 Hz or higher. Though poly-silicon TFT's mobility is large enough, it lacks flexibility and transparency, which is fatal for flexible devices. Organic TFT has flexibility and transparency, but its mobility is not enough for the high-speed display for high frame rate. [33, 34] Metal oxide TFT is one of the innovations to meet the requirements of mobility and transparency simultaneously. However, present metal oxide TFT is instable because it is sensitive to light, temperature, and water vapor. Also, it is instable and subjects to the negative bias illumination stress which can cause threshold voltage to shift to the negative voltage direction. [35] SWCNTs possess high mobility, high transparency, and good flexibility simultaneously. These attractive properties satisfy the requirements of thin film transistors, making CNTs the most promising candidates as the high-performance TFT channel material.

	a-Si TFTs	Poly-Si TFTs	Organic TFTs	Oxide TFTs	CNT TFTs
Mobility	<1	50~150	<1	1~80	<10
Uniformity	○	△	○	○	△
Stability	△	◎	△	○	△
Process Temp.	~250 °C	>250 °C	RT~250 °C	RT~ 250 °C	RT
Cost	○	△	◎	◎	◎
Substrate	Glass, Metal, Plastic	Glass, Metal	Glass, Metal, Plastic	Glass, Metal, Plastic	Glass, Metal, Plastic
Deposition Tech.	PECVD	Excimer Laser	Printing, Vacuum evaporation	Sputter, Printing	Printing, Solution deposition

Table 1.1 Comparison of a-Si, poly-Si, organic, oxide, and CNT TFTs

1.4 Static Random Access Memory

Static random-access memory (SRAM) is a type of semiconductor memory that uses bistable latching circuitry (flip-flop) to store each bit. SRAM exhibits data remanence but it is still volatile in the conventional sense that data is eventually lost when the memory is not powered. [36] A typical SRAM cell is made up of six MOSFETs as illustrated in Figure 1.6. Each bit in an SRAM is stored on four transistors (M1, M2, M3, M4) that form two cross-coupled inverters. This storage cell has two stable states which are used to denote 0 and 1. Two additional access transistors serve to control the access to a storage cell during read and write operations. In addition to such six-transistor (6T) SRAM, other kinds of SRAM chips use 4, 8, 10 (4T, 8T, 10T SRAM), or more transistors per bit. Four-transistor SRAM is quite common in stand-alone SRAM devices (as opposed to SRAM used for CPU caches), implemented in special processes with an extra layer of polysilicon, allowing for very high-resistance pull-up resistors. The principal drawback of using 4T SRAM is increased static power due to the constant current flow through one of the pull-down transistors.

An SRAM cell has three different states: standby (the circuit is idle), reading (the data has been requested) or writing (updating the contents). SRAM operating in read mode and write modes should have "readability" and "write stability", respectively. In standby state, if the word line is not asserted, the access transistors M5 and M6 disconnect the cell from the bit lines. The two cross-coupled inverters formed by M1 – M4 will continue to reinforce each other as long as they are connected to the supply. For reading data, reading only

requires asserting the word line WL and reading the SRAM cell state by a single access transistor and bit line, e.g. M6, BL. Nevertheless bit lines are relatively long and have large parasitic capacitance. To speed-up reading, a more complex process is used in practice: The read cycle is started by precharging both bit lines BL and BL, i.e. driving the bit lines to a threshold voltage by an external module. Then asserting the word line WL, enabling both the access transistors M5 and M6 which causes the bit line BL voltage to either slightly drop (bottom NMOS transistor M3 is ON and top PMOS transistor M4 is off) or rise (top PMOS transistor M4 is on). It should be noted that if BL voltage rises, the BL voltage drops, and vice versa. Then the BL and BL lines will have a small voltage difference between them. A sense amplifier will sense which line has the higher voltage and thus determine whether there was 1 or 0 stored. The higher the sensitivity of the sense amplifier, the faster the read operation. In writing process, the write cycle begins by applying the value to be written to the bit lines. If we wish to write a 0, we would apply a 0 to the bit lines, i.e. setting BL to 1 and BL to 0. This is similar to applying a reset pulse to an SR-latch, which causes the flip flop to change state. A 1 is written by inverting the values of the bit lines. WL is then asserted and the value that is to be stored is latched in. This works because the bit line input-drivers are designed to be much stronger than the relatively weak transistors in the cell itself so they can easily override the previous state of the cross-coupled inverters. In practice, access NMOS transistors M5 and M6 have to be stronger than either bottom NMOS (M1, M3) or top PMOS (M2, M4) transistors. This is easily obtained as PMOS transistors are much weaker than NMOS when same sized. Consequently when one transistor pair is only slightly overridden by the write process, the opposite transistors pair

(M1 and M2) gate voltage is also changed. This means that the M1 and M2 transistors can be easier overridden, and so on. Thus, cross-coupled inverters magnify the writing process.

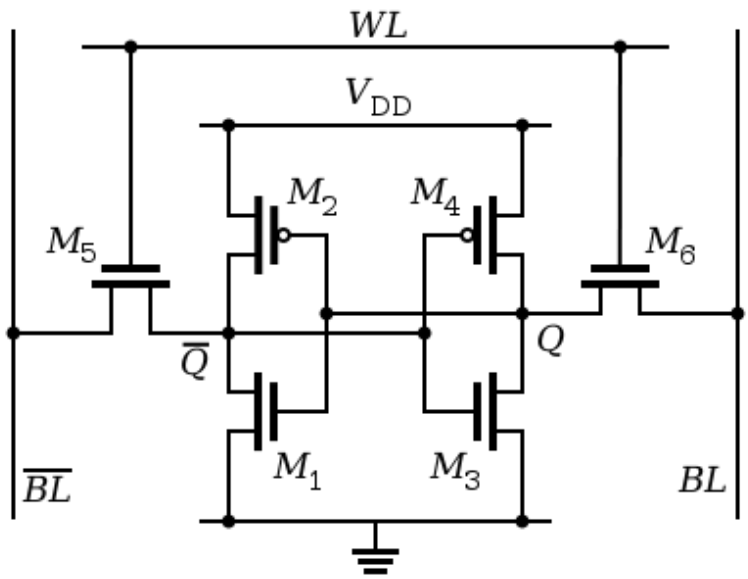

Figure 1.6 A six-transistor CMOS SRAM cell

1.5 Organization of This Dissertation

This thesis introduces the studies on the organic nonvolatile memory transistors (ONVMTs) and inkjet-printed SWCNT transistors and their applications. For ONVMTs, bottom-gate/top-contact structure using pentacene and solution processed polystyrene were used as active and charge tunneling dielectric layers respectively. For the floating gate, a discrete graphene layer was formed by controlling growth time during a conventional CVD process. For SWCNT transistor, SWCNT was used for semiconductor in transistor with inkjet printing method. From this inkjet-printed SWCNT transistor, we compared with other solution processed SWCNT transistor method. Also from SWCNT transistor, we fabricated SWCNT inverter and improve its electrical properties by chemical encapsulation. And finally, we fabricated and analyzed inkjet-printed SWCNT SRAM device.

Chapter 1 includes introduction of ONVMTs and SWCNT transistors with its brief history and its advantages compared to other processes and materials.

Chapter 2 covers the ONVMTs with graphene charge floating gate. For graphene charge floating gate, we proposes a new method for synthesize the partially grown graphene by controlling time of synthesize of graphene in CVD system. From this graphene charge floating gate, we fabricated ONVMTs and analyze their electrical properties and memory properties.

Chapter 3 focuses solution processed SWCNT transistors with inkjet printing method. In this chapter, we optimized inkjet printing condition and illustrated advantages of inkjet printing method compared to other deposition method. From this SWCNT transistor, we

fabricated circuit applications including inverter.

Chapter 4 covers inkjet-printed full-swing SWCNT inverter and SWCNT SRAM device. In this chapter, we fabricated SWCNT circuit applications including inverter and SRAM by using inkjet-printing method. For full-swing SWCNT inverter, we used chemical encapsulation with ammonium hydroxide (NH_4OH). Also using this full-swing inverter, we fabricated SWCNT RAM by connecting two inverters' input and output.

Chapter 5 summarizes the investigation of the ONVMTs using graphene charge floating gate and inkjet-printed SWCNT transistor and its circuit applications including inverter and SRAM.

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Chapter 2

Controlled Growth of a Graphene Charge-Floating Gate for Organic Non-Volatile Memory Transistors

2.1 Introduction

With continued development in information technology, there is increasing interest in non-volatile memory for use as data storage in electronic devices. There are currently several types of memory devices available, which are categorized on the basis of their operating methods. Among these, a floating gate memory transistor have been widely studied owing to their non-destructive data processing, reliable data storage, and simple structure; which typically comprises a single transistor. [1, 2] Those based on organic semiconductors, such as pentacene, have received particular interest by virtue of their

simple process and potentials for being used as flexible or stretchable device. [3] In all floating gate memory transistors, however, the memory properties can be determined by the floating gate and tunneling dielectric. To date, conventional thin films floating gate have been used in memory transistor devices, but these conventional memory devices encounter difficulties of floating gate interference and parasitic capacitance; both of which affect the overall device performance and reliability, when used with miniaturized cell sizes and in high densities. [4-9] To overcome these problems, a number of research groups are currently searching for suitable materials that could be used to replace those used in the conventional floating gates. Among the various potential candidates for the charge storage layer, graphene offers an advantage of introducing metallic properties. [10] Therefore, it can enhance the performance of current memory devices in a facile manner, owing to its unique properties of high density of state, high work function, and low dimensionality. [11-16] However, the two-dimensional continuous planar structure of graphene typically has difficulty in storing sufficient charge for non-volatile memory function, because the charge carrier stored in the continuous charge storage layer is easily lost through the thin tunneling dielectric. Some groups have, therefore, selected to use discrete charge storage layers, such as metal nanoparticles, for the floating gate in non-volatile memory devices. [17, 18] In this study, we fabricated the graphene floating gate into the organic nonvolatile memory transistors (ONVMT) with bottom-gate/top-contact structure using pentacene and polystyrene (PS) as active and charge tunneling dielectric layers, respectively. For the floating gate, we propose a discrete graphene layer formed by controlling growth time of the graphene layer during a conventional CVD process, and then simply transferring it onto

the gate dielectric layer. The fabricated ONVMT showed an anti-clockwise hysteresis in transfer curves with large memory windows (~ 40 V) and a reasonable program/erase cycle endurance greater than 100 times and an estimated long data retention time of >1 year although it was operated without encapsulation in an ambient condition.

2.2 Materials and Processes

2.2.1 Graphene

Graphene is a crystalline allotrope of carbon with 2-dimensional properties. This carbon atoms are densely packed in hexagonal pattern. In graphene structure, each atom has four bonds, one σ bond with each of its three neighbors and one π-bond that is oriented out of plane. [13] The atoms are about 1.42 Å apart. Graphene's hexagonal lattice can be regarded as two interleaving triangular lattices. This perspective was successfully used to calculate the band structure for a single graphite layer using a tight-binding approximation. Graphene's stability is due to its tightly packed carbon atoms and a sp^2 orbital hybridization – a combination of orbitals s, p_x and p_y that constitute the σ-bond. The final p_z electron makes up the π-bond. The π-bonds hybridize together to form the π-band and π^*-bands. These bands are responsible for most of graphene's notable electronic properties, via the half-filled band that permits free-moving electrons. [19] From this structure, graphene shows extraordinary thermal, mechanical, and electrical properties. The interest in graphene has mobilized both academic and industry realms making it an ideal candidate for the design of modern nanoscale transistors, chemical and biosensors, flexible and organic light-emitting diodes (OLEDs) displays, solar and fuel cells, and other innovations. [20, 21] For the applications of graphene, large-area, mass production and reproducibility is critical. To date, several techniques have been established for graphene synthesis. From the exfoliation method, there are various synthesis techniques have been introduced such as chemical exfoliation, chemical synthesis, and thermal chemical vapor deposition. Some

other techniques are also reported such as unzipping nanotube and microwave synthesis, but those techniques need to be more studied. [22-24] Each synthesis method has its own advantages as well as disadvantages depending upon the final application of graphene. For example, the mechanical exfoliation method is hard to get from graphite to mono layered graphene, and cannot be applicable to large area applications such as display. Furthermore, chemical synthesis processes graphene synthesized from reduced graphene oxides (RGOs) often causes incomplete reduction of graphite oxide and this results in the successive degradation of electrical properties depending on its degree of reduction. On the other hand, thermal CVD methods have more advantages compared to other methods. This CVD method is applicable large area application, and this method shows better quality of electrical and chemical properties than other methods because grapheme from this method has few defects. Also CVD method can be used for various applications because graphene can be easily transferred any substrate.

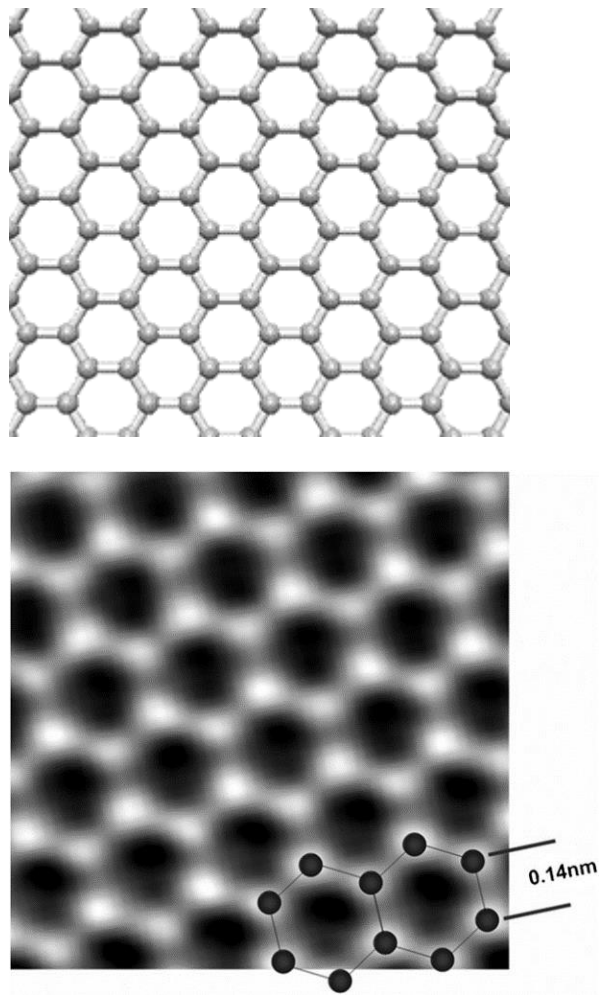

Figure 2.1 (a) Chemical structures and (b) High-resolution TEM images of graphene

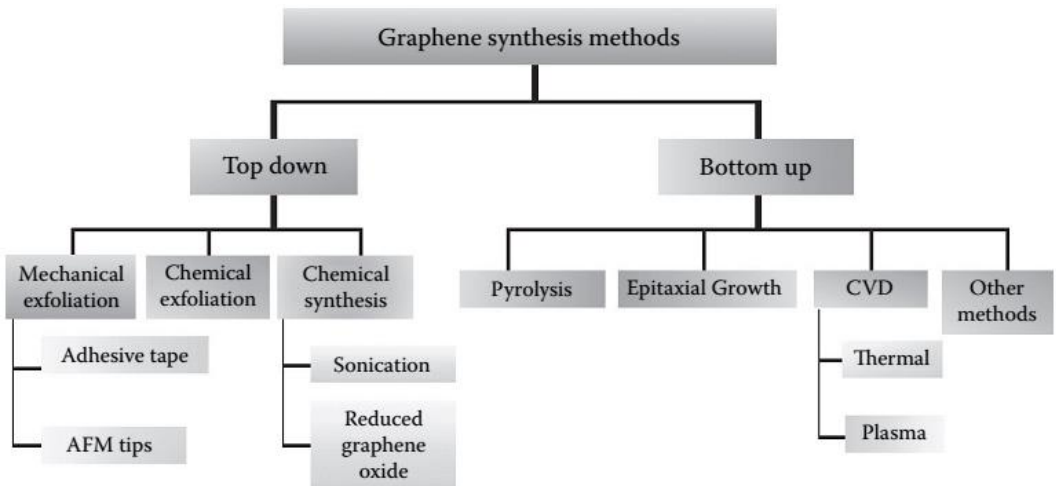

Figure 2.2 The schematic represents the different graphene synthesis methods

2.2.2 Chemical Vapor Deposition Graphene

The CVD method using copper substrate and gases, carbon sources discovered by Li and colleagues, opening the new route for fabricating large-scale graphene substrate. This method provides attractive advantages such as flexibility, high conductivity, and large scale compared to other methods. [25] Therefore, various CVD-grown graphene application have been demonstrated and showed excellent device performance. The CVD graphene was generally grown on the various metal substrates including Ne, Fe, and Cu substrate and the CVD method required a tubular furnace and law gases for carbon source. A graphene growth process by CVD method and transfer method are illustrated Figure 2.3. [26] A typical growth is composed with three steps. i) pre-annealing, ii) growth, and iii) cooling. The layer number and domain size of graphene can be controlled by changing the substrate thickness and growth time during growth process. In the process, the last cooling rate is critical in suppressing formation of multiple layers and for separating graphene layers efficiently from the substrate in the later process. The developed conditions of graphene preparation allowed observation of unique properties including a half-integer quantum Hall effect for both electrons and holes even at room temperature, extraordinarily high carrier mobility, and single-molecule detection. CVD-grown graphene also exhibits other superior characteristics of electronics, mechanical, optical, and transport nature compared to micromechanical or chemical exfoliation of graphite. These include ambipolar field effect, superlative mechanical strength, large specific surface are, high transparency, and high thermal conductivity. Transfer of graphene is important for flexible application.

Using transfer of graphene, applications of graphene are no longer to limited to the use of rigid substrates; instead, large flexible copper foils may be used in the form of a roll-type substrate fitting inside a tubular furnace to maximize the scale and homogeneity of the produced graphene films. The flexibility of the graphene and copper foils further allows efficient etching and transfer processes that use a cost- and time-effective roll-to-roll production method. There are three essential steps in the roll-to-roll transfer illustrated in Figure 2.4 [24] ; (i) adhesion of polymer supports to the graphene on the copper foil; (ii) etching of the copper layers; and (iii) release of the graphene layers and transfer onto a target substrate. In the adhesion step, the graphene film, grown on a copper foil, is attached to a thin polymer film coated with an adhesive layer by passing between two rollers. In the subsequent step, the copper layers are removed by electrochemical reaction with aqueous 0.1 M ammonium persulphate solution $(NH_4)_2S_2O_8$. Finally, the graphene films are transferred from the polymer support onto a target substrate by removing the adhesive force holding the graphene films. When using thermal release tapes, the graphene films are detached from the tapes and released to counter-substrates by thermal treatment. The third step is not necessary when the target substrate is directly attached to the copper foil in the first step by permanent adhesion

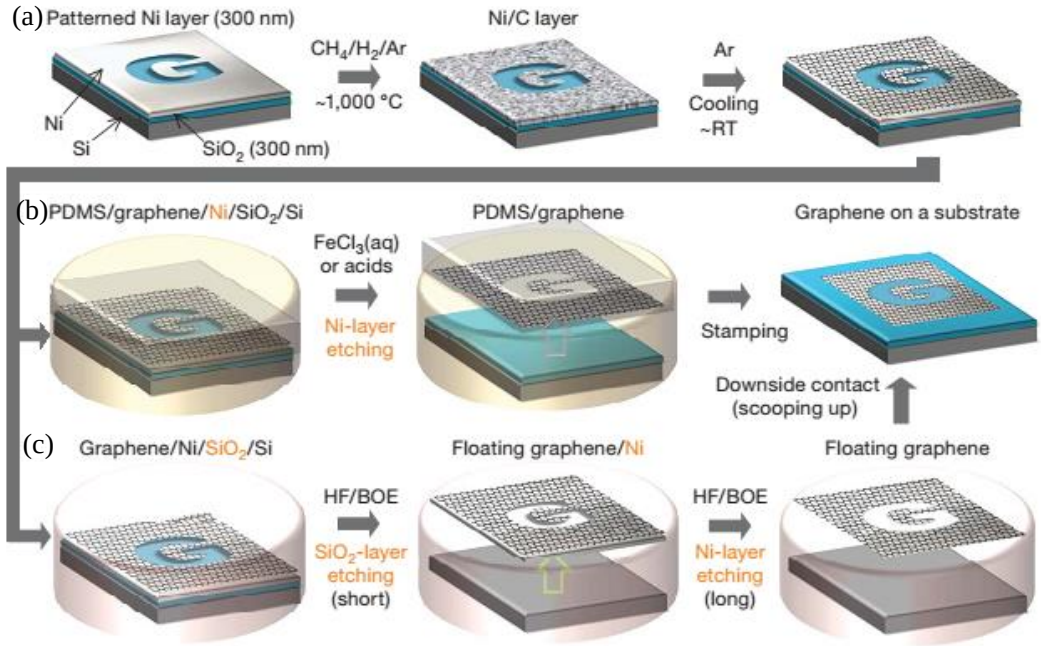

Figure 2.3 Synthesis, etching and transfer processes for the largescale and patterned graphene films. (a) Synthesis of patterned graphene films on thin nickel layers. (b) Etching using $FeCl_3$ and transfer of graphene films using a PDMS stamp (c) Etching using BOE or hydrogen fluoride (HF) solution and transfer of graphene films

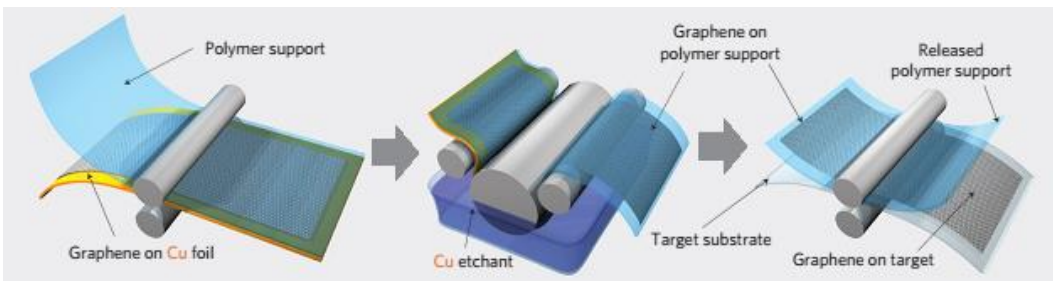

Figure 2.4 Schematic of the roll-based production of graphene films on a copper foil

2.3 Experiments

In order to fabricate the partially grown graphene layer, a roll of copper foil containing 150 ppm of silver was first inserted into a quartz tube of the chemical vapor deposition (CVD) system and then heated to 1,000°C for 40 min with flowing 40 sccm CH_2 and 5 sccm H_2 at 50 mTorr. After reaching 1,000°C, the sample was annealed for 20 min without changing the flow rate and pressure. Partially grown graphene layer was synthesized by controlling the growth time, which was varied (1, 20, 40 and 60 seconds) maintaining the total pressure at 100 mTorr. The CVD chamber was cooled down to room temperature with flowing only 5 sccm H_2. After the sample was taken out of the chamber, poly(methyl methacrylate) (PMMA) was poured on the graphene film grown on the copper foil. When floated in an aqueous solution of 0.1M ammonium persulphate ($(NH_2)_4S_2O_8$), the PMMA with the partially grown graphene layer was separated from the copper foil. [27, 28]

For the memory device fabrication, a heavily doped silicon (Si) substrate with thermally grown 200 nm thick silicon dioxide insulator was used. For cleaning process, the substrate was cleaned with acetone, isopropyl alcohol (IPA) and deionized (DI) water in bath type ultra-sonicator for 20 min, respectively. In order to evaluate the charge storage function, two types of devices were fabricated. One is organic field effect transistor without graphene charge floating gate, and the other is organic nonvolatile memory transistor with graphene floating gate. For the device with the floating gate, the partially grown graphene film was first transferred from the PMMA layer onto the SiO_2 surface.

For the charge tunneling dielectric, PS was dissolved in toluene at 3.5 mg/ml and the

solution was stirred in for 24 hours. Then, PS was deposited by spin-coating at 3,000 rpm for 40 sec. The film was then annealed at 120 ℃ for 60 minutes in the nitrogen atmosphere. The thickness of the obtained layer was 15 nm by AFM. Finally, to deposit the active semiconductor layer and source/drain electrodes, 50 nm pentacene and 70 nm Au layers were sequentially deposited by a thermal evaporation process. When deposit pentacene and Au layer, each deposit rate was 50 Å/s and 150 Å/s under high vacuum about $1x10^{6}$ Torr. The channel length and width were 50 and 1000 μm, respectively.

Atomic force microscopy (AFM) images of the graphene films were taken by using a non-contact mode of atomic force microscopy system (XE-100, Park System). Raman spectrum was measured by using Raman microsystem 2000 (Renishaw). All fabricated devices were electrically characterized in ambient and dark conditions by using a semiconductor parameter analyzer (Agilent HP 4155C).

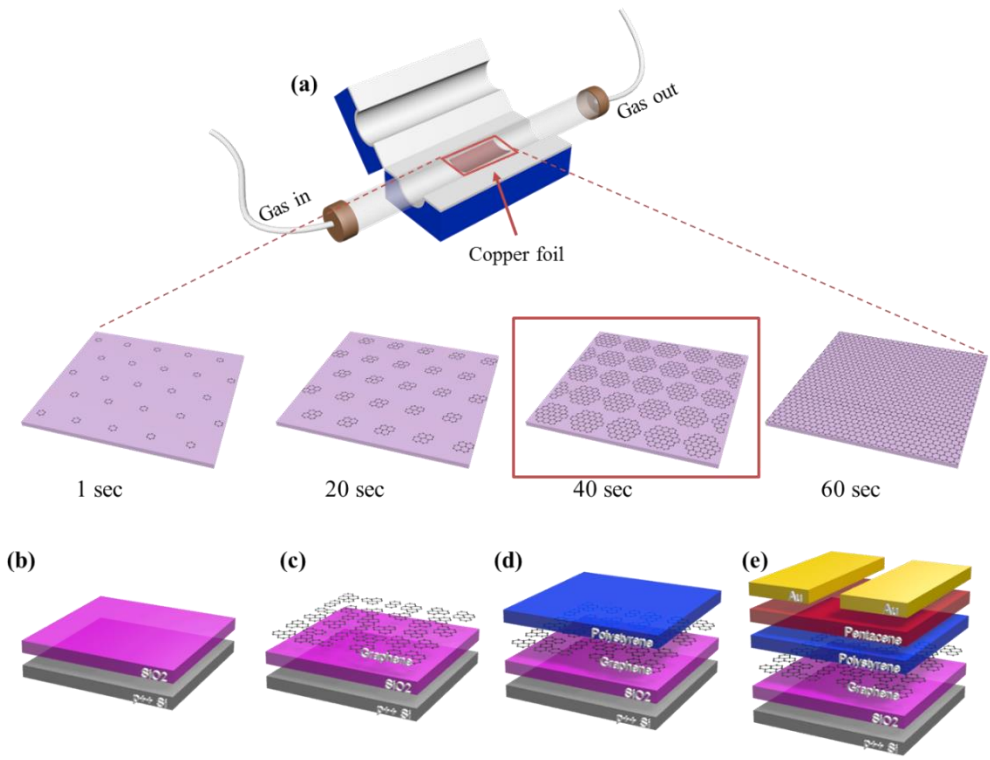

Figure 2.5 Schematic diagram of the ONVMT fabrication process used. (a) Synthesis of partially grown graphene (b) Cleaning of SiO_2/Si substrate. (c) CVD graphene growth and transfer. (d) Spin-coating of PMMA tunneling layer. (e) Active layer and source/drain deposition using thermal vapor deposition

2.4 Results and Discussion

Figure 2.6 (a) illustrates schematic image of graphene growth process on Cu foil using Ag as nucleation seeds and Figure 2.6 (b) shows condition of graphene synthesis with total reactant gas flow rate. By controlling of growth time of graphene, partially grown graphene layers with various flake size were synthesized. As shown in FE-SEM images of Figure 2.7 (a) to (d), graphene seed and grain grow larger with time. After 60 sec (Figure 2.7 (d)), graphene covered all area of Cu foil with a continuous single layer. For the discrete graphene floating gate, we selected the partially grown graphene with 40 seconds growth time in order to ensure a large coverage of surface and guarantee discrete flake formation simultaneously. Raman spectroscopy was also used to ensure the quality of the transferred single layer graphene, the results of which are shown in Figure 2.8 (b). The Raman spectrum of graphene is characterized by three main characteristic peaks. The G peak, D band, and 2D peak showed at near 1580 cm^{-1}, 1350 cm^{-1}, and near 2700 cm^{-1}, respectively. Also the Raman spectra are measured on the edge, middle and center areas of one partially grown graphene (10×10 m^2) and illustrated in Figure 2.9. The formation of monolayer graphene flakes is confirmed by a sharp 2D-band (~ 40 cm) and no peak at D band (~ 1350 cm^{-1}). Also Raman maps were measured on partially grown graphene of the G peak (1560 to 1620 cm^{-1}), 2D peak (2660 to 2700 cm^{-1}), and D peak (1300 to 1400 cm^{-1}), bands. (e to f) Raman mapping of I_{2D}/I_G and I_D/I_G intensity ratio respectively

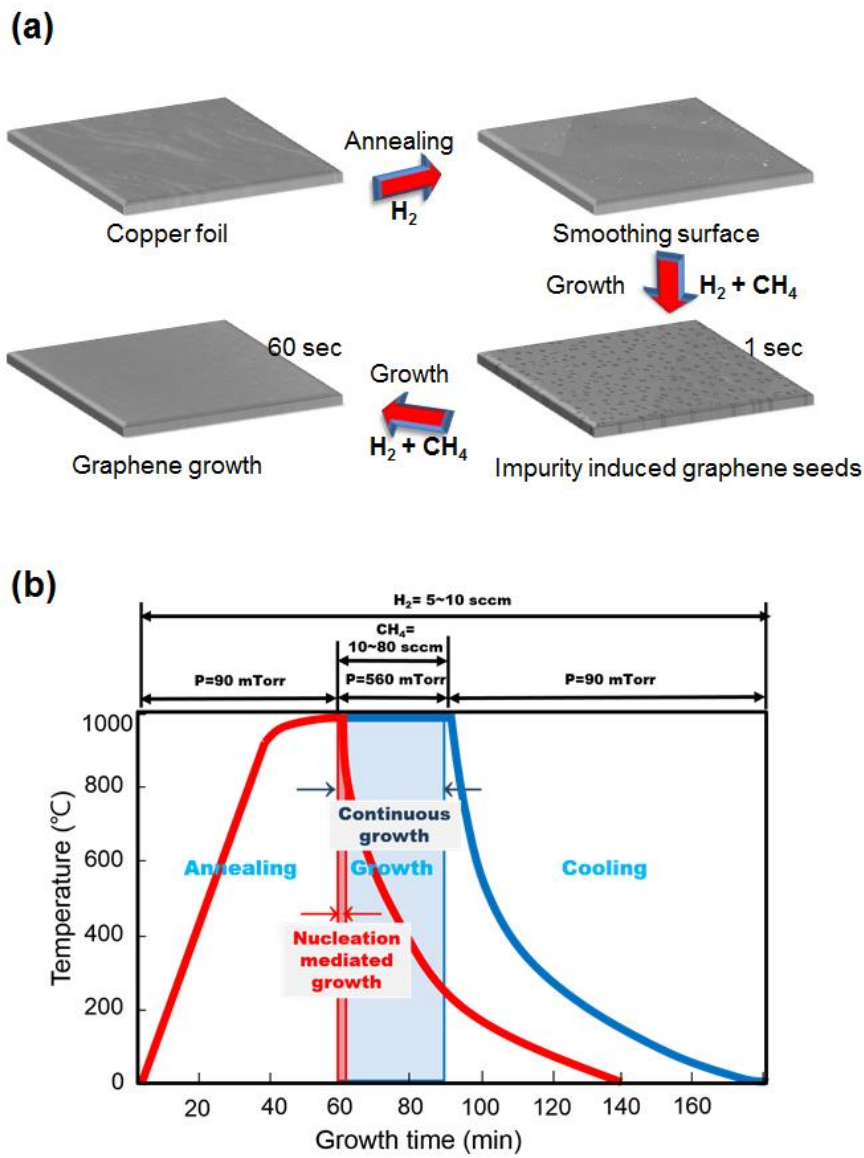

Figure 2.6 **(**a) Schematic diagram of graphene growth on Cu foil using Ag as nucleation seeds. (b) CVD growth of graphene at 1000 ℃ with total reactant gas flow rate

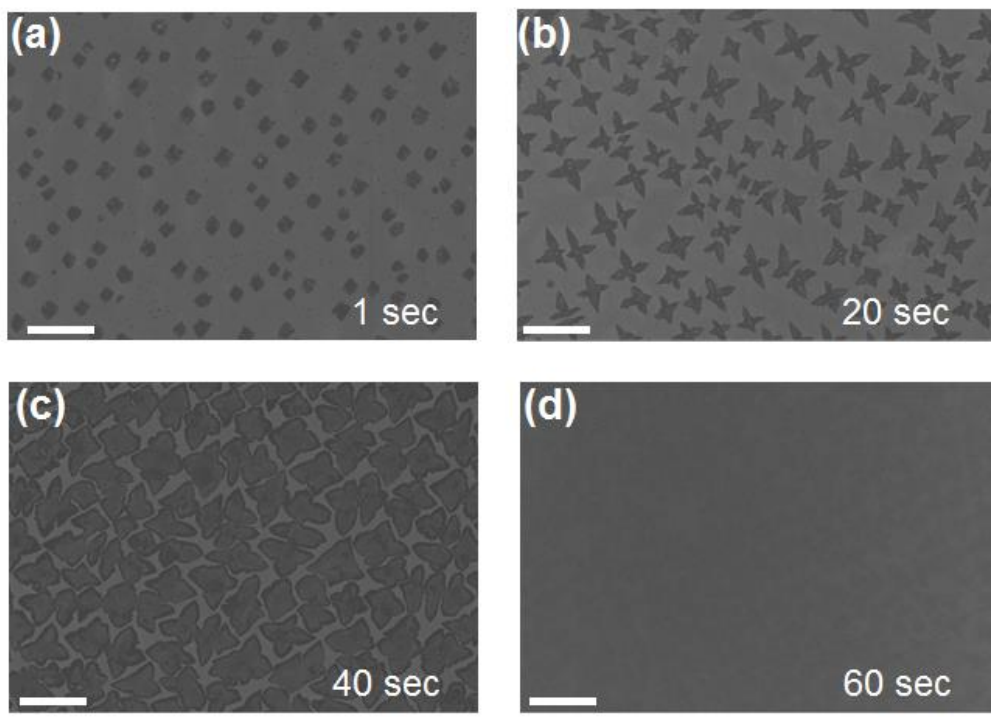

Figure 2.7 SEM images of (a) 1s (b) 20s (c) 40sec (d) 60sec of graphene seeds and grains after the CVD process, respectively. All images were obtained on Cu foils. Image in (a) the smaller circle represents graphene nucleation sites induced by silver. In panel (c) the graphene domains have yet to join to form a continuous layer. In panel (d) the graphne under growth process for 1 min.

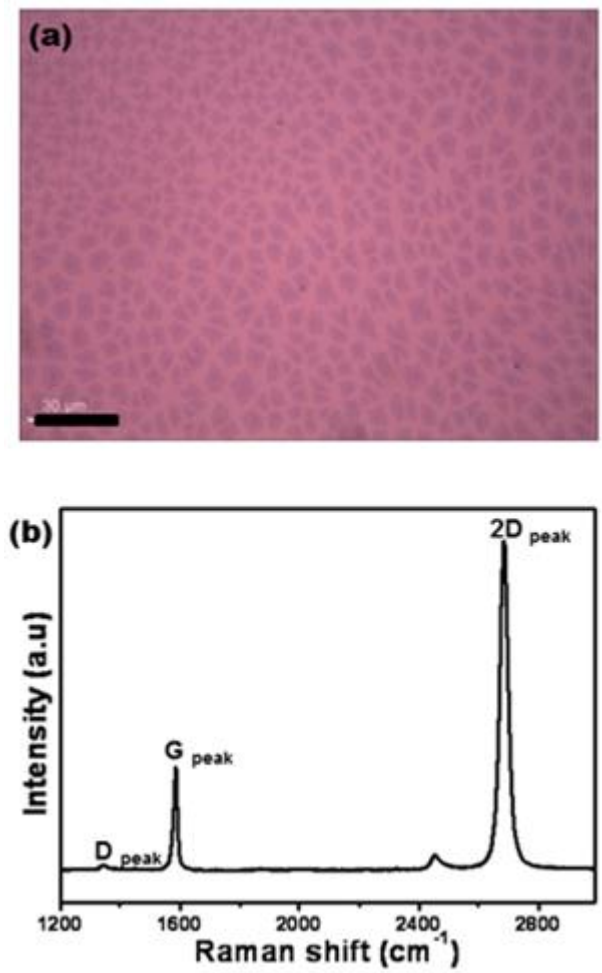

Figure 2.8 (a) Optical microscope images of partially grown graphene transferred on a SiO_2 substrate. (b) Raman spectroscopy of partially grown graphene.

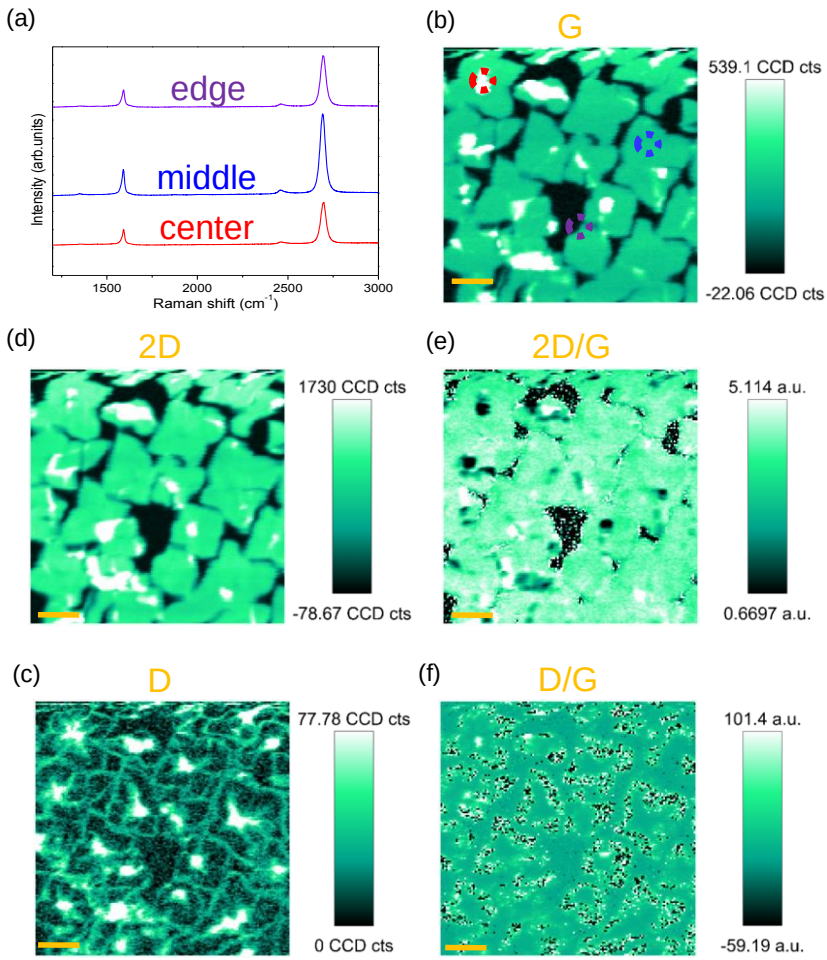

Figure 2.9 (a) Raman spectra taken from location red (center), blue (middle), and violet (edge) with corresponding the position. (b to d) Raman maps of the G peak (1560 to 1620 cm^{-1}), 2D peak (2660 to 2700 cm^{-1}), and D peak (1300 to 1400 cm^{-1}), bands. (e to f) Raman mapping of I_{2D}/I_G and I_D/I_G intensity ratio respectively.

A schematic illustration of the fabricated ONVMT is depicted in Figure 2.10 (a). AFM images of the evaporated pentacene and spin-coated PS layers are also shown in Figure 2.10 (b) and (c), respectively. The PS layer was measured to have an average thickness of ~15 nm and a root mean square roughness of 0.3 nm, which are good for an effective tunneling dielectric layer with a smooth surface for growth of the terraced pentacene film. The partially grown graphene used for the floating gate is shown in Figure 2.10 (d). It is noted that the graphene flake is 10 μm in the longest size and 1nm high on average. The graphene approximately covers 80 % of the total transferred area. Transmission electron micrographs (TEM) images (Figure 2.11 (a) and (b)) for the cross-section of the areas with and without graphene flakes in the transferred area clearly show the discrete floating gate formation.

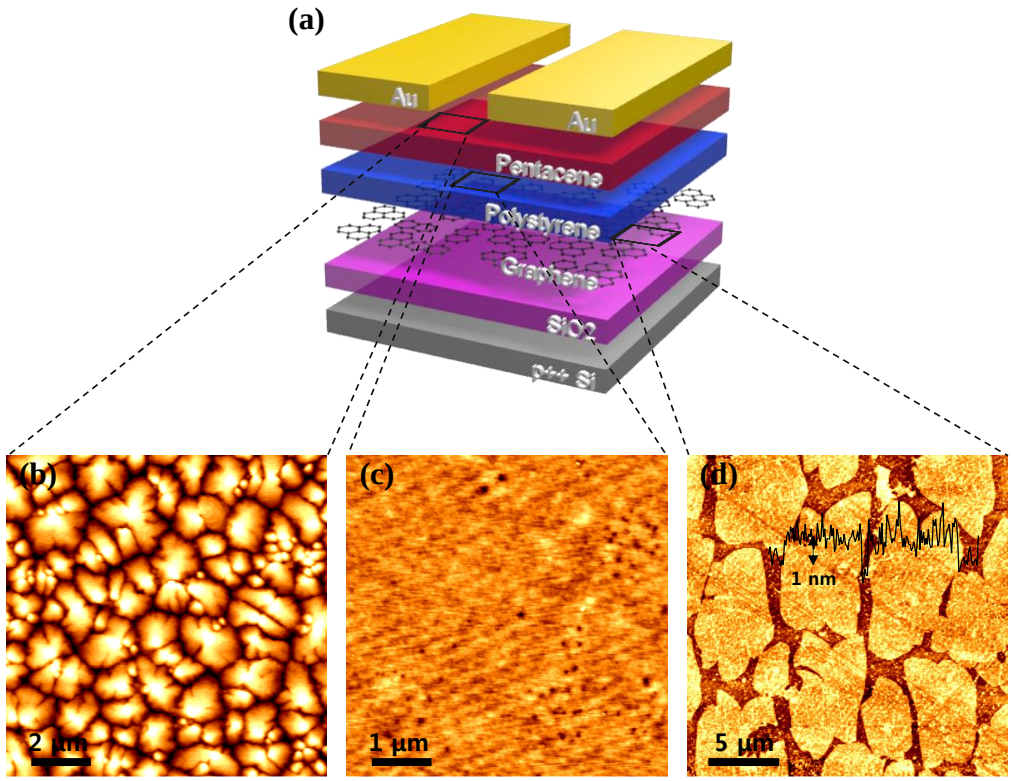

Figure 2.10 (a) Device schematics of ONVMTs. AFM topology images: (b) Pentacene layer on PS. (c) PS charge-tunneling layer on graphene. (d) Partially grown graphene flakes.

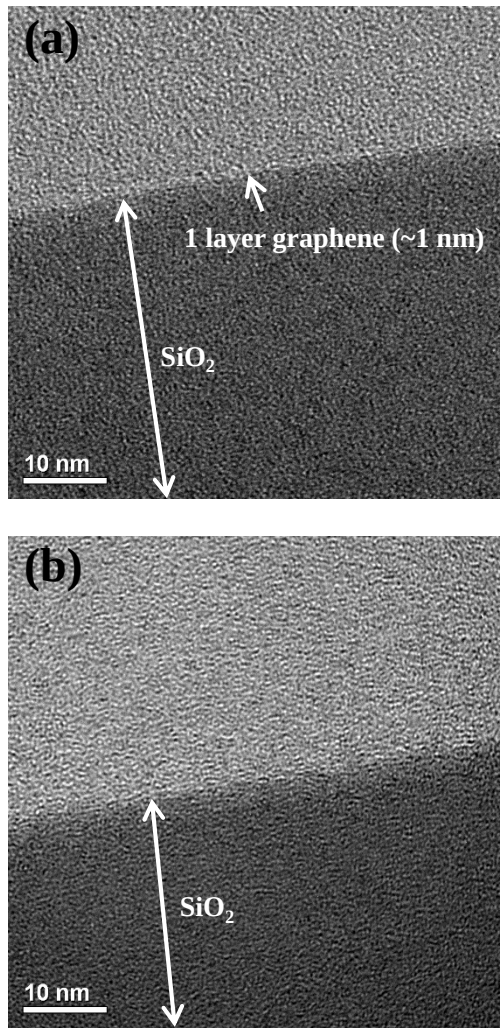

Figure 2.11 TEM images: partially grown graphene on SiO_2 (a) with graphene, and (b) without graphene

The electrical properties of the fabricated ONVMTs are shown and compared with those of the conventional OTFTs that contain no graphene floating gate (Figure 2.12). It is noted that the same structure of $p^{++}Si/SiO_2$/PS/pentacene/Au source-drain for OTFTs to compare the charge storage capability in both ONVMTs and OTFTs. Figure 2.12 (a) shows the transfer and output characteristics of the fabricated TFTs, which show a typical p-channel TFT behavior. Figure 2.12 (b) shows a double transfer curve, which obtained by sweeping gate voltage first from positive to negative values and then vice versa. Although there is a certain amount of hysteresis for the conventional OTFTs as previously reported for OTFTs with PVP gate dielectric [29-31], the hysteresis amount is very small (< 5 V) in comparison with that of the ONVMTs (~40 V) when the gate voltage was swept from +80 V to -80 V and then swept back to +80V. [30] Therefore, it can be concluded that there is almost negligible charging and discharging of the charge carriers in the bulk, or at the interfaces of the gate dielectric layer in our devices. For the fabricated OTFTs, we obtained a saturation mobility of 0.39 $cm^2/V \cdot s$, a threshold voltage of -13.2 V, a subthreshold swing of 2.6 V/decade, and an I_{on}/I_{off} ratio of $\sim 10^6$. The field-effect mobility (μ) and threshold voltage were subsequently calculated using the following equation:

$$I_D = \frac{W}{2L}\mu C_i(V_{GS} - V_{th})^2$$

where C_i is the insulator capacitance per unit area and V_{th} is the threshold voltage. We calculated capacitance using a HP-4284A LCR meter in air at room temperature.

When a graphene floating gate is inserted ($p^{++}Si/SiO_2$/graphene/PS/pentacene/Au source-drain), we obtained a larger hysteresis effect and enhanced charge storage capability.

The transfer and output characteristics of the fabricated ONVMTs are illustrated in Figure 2.13 (a). Similar to the devices without a graphene charge layer, they exhibit typical p-channel TFT characteristics but with a saturation mobility of 0.061 $cm^2/V \cdot s$, a threshold voltage of -10.1 V, a subthreshold swing of 8.5 V/decade, and an I_{on}/I_{off} ratio of 10^5. It is thought that the mobility degradation is caused by the graphene floating gate and the trapped charge carriers in the graphene layer close to the pentacene surface, which introduce positive charges at the semiconductor/dielectric interface and degrade the channel conductance. [17] Figure 2.13 (b) shows the transfer characteristics of the fabricated ONVMTs for various sweep ranges of gate voltages (V_G), in both the forward ($+V_G$ to $-V_G$) and reverse ($-V_G$ to $+V_G$) directions, at the same drain voltage (V_D) of -20 V. This demonstrates a clear hysteresis loop for all gate voltages and for the range of +80 V to -80 V, the resulting memory window was 40 V. This confirms that the charges were successfully transferred between the pentacene and the graphene layers. Moreover, the anticlockwise hysteresis direction indicates that electrons were injected from the pentacene to graphene layer when a positive gate bias was applied, and ejected from the graphene to pentacene layer when a negative gate bias was applied. [32]

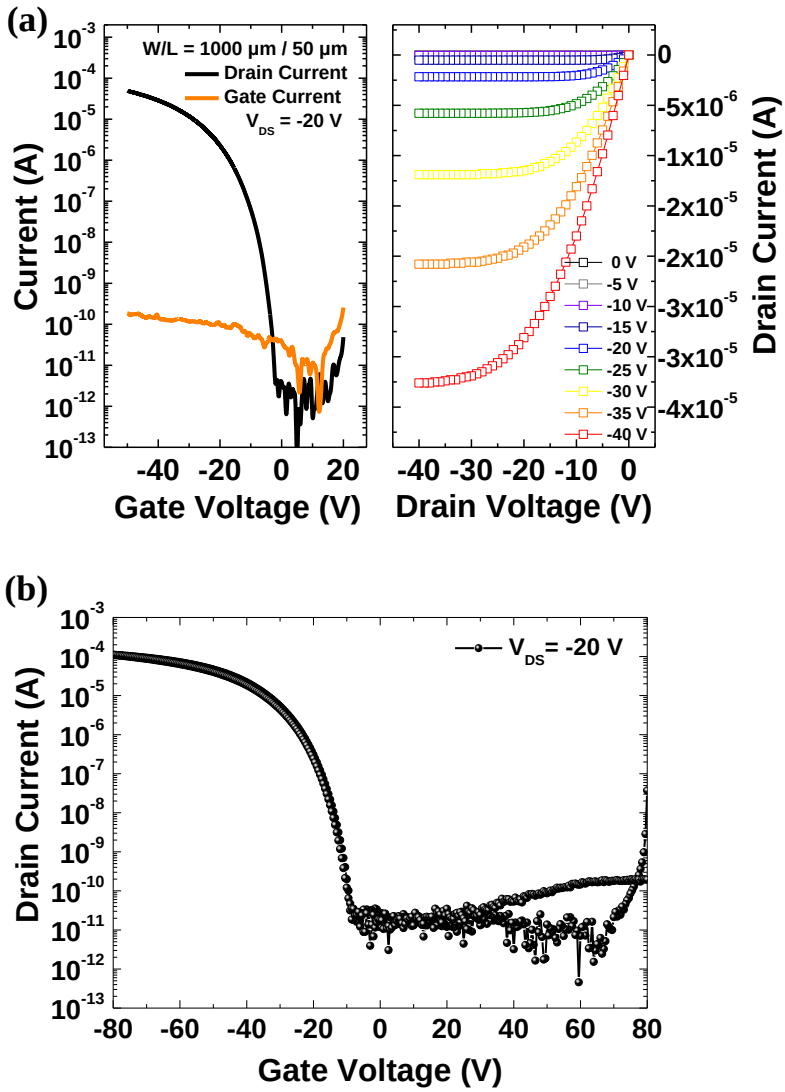

Figure 2.12 (a) Transfer and output characteristics of organic thin film transistors without a graphene layer (b) Double sweep of gate bias of organic thin film transistors from +80 V to -80V

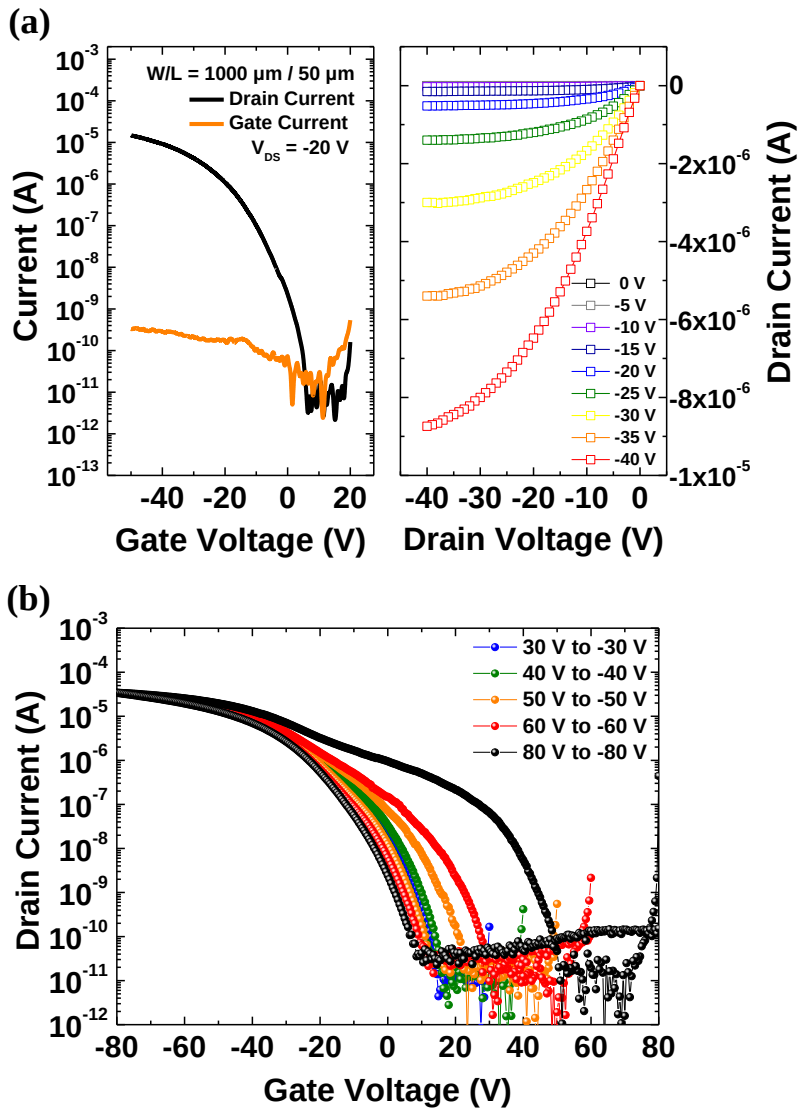

Figure 2.13 (a) Transfer and output characteristics of organic memory thin film transistors with a graphene layer (b) Double sweep of gate bias of organic thin film transistors for various gate voltage ranges

To evaluate the programming and erasing properties, the shift in the transfer curves from the initial state was measured after applying a gate voltage of +80 V and -80V, respectively, for 100 ms. The drain-source voltage was kept constant at -20 V in both measurements. Figure 2.14 (a) shows the programming and erasing characteristics of the ONVMT, in which large V_{th} shifts are shown. Specifically, the transfer curves were shift toward positive direction during programming, while erasing brings the transfer curves back close to their original states. The difference of the drain current was as large as 10^4 at V_{GS} = 0 V and V_{DS} = -20 V. The total shift in the threshold voltage (ΔV_{th}) was about 23 V. The observed memory behavior can be explained on the basis of the charging/discharging of the electrons in the graphene layer during the programing/erasing operations as shown in Figure 2.14 (b). When a high positive gate bias is applied, electrons from the lowest unoccupied molecular orbital (LUMO) of pentacene are transferred into the graphene through the PS tunneling dielectric. [30, 33, 34] Similar electron tunneling and memory effect of the organic TFT memory with a floating gate structure has been explained by Fowler-Nordheim tunneling followed by charge trapping, which is a dominant mechanism for charge injection through relatively thick tunneling dielectric (~15 nm) in the ONVMT. [1, 16, 32, 35] When a high negative gate bias is applied during the erasing period, the trapped electrons are tunnelled back from graphene to pentacene, and thus cause the threshold voltage to be negatively shifted.

In fact, from the amount of the V_{th} shift, we can calculate the surface density of the transferred charges (Δn) from pentacene to graphene after the programming process using the following equation. [34, 35]

$$\Delta n = \frac{\Delta V_{th} C_i}{e}$$

where e, ΔV_{th}, and C_i are the elementary charge, the shift in V_{th}, and the capacitance of the gate dielectric, respectively. With a gate dielectric capacitance C_i=1.6 ×10^{-8} F/cm^2, and ΔV_{th} = 23 V, the surface density of charges transferred from pentacene to graphene, Δn, was estimated to be 2.3 × 10^{12} charges/cm^2. The total coverage of partially grown graphene is about 80 % of the total channel area, and so the surface density of charges transferred in the graphene surface was estimated to be 2.87 × 10^{12} charges/cm^2, which is similar to the stored charges for other ONVMTs with various types of the floating gates such as Au nano particles and graphene oxide. [34-36]

Two factors that are the most important for a memory device are data retention ability and program/erase cycle stability. To first examine how long the memory device can sustain the stored charges, the drain current was monitored at the programmed/erased states with the same programming and erasing conditions that were used. The drain current was measured at 0 V of gate voltage with a -20 V drain voltage for each state. The measured on and off currents are illustrated in Figure 2.15 (a), in which the ON state current is dropped by half of the initial value after 10^5 sec while the OFF state current remains almost constant at 10^{-10} A over the same period of time. By extrapolating this result we can obtain a 10^3 on/off ratio after 1 year, which indirectly confirms that the device can maintain data and a distinguishable on/off ratio over this long period of time. The program/erase cycle properties were also measured as shown in Figure 2.15 (b). In order to measure the endurance properties, the programming/erasing operations were repeated with continuous

application of bias pulses with the magnitude of 80 V and -80 V, and time width of 0.5 seconds. In each programming/erasing operation, the drain current measured at 0 V of gate voltage with a -20 V drain voltage. Although some degradation of the drain current was observed with the program/erase cycles, a distinguishable on/off ratio of 10^3 is nonetheless obtained after 100 program/erase cycles. It is noted that the device was not encapsulated and measured in air. The measured current for the programmed and erased states degraded with time, but the memory performance was well maintained compared to other organic memory devices under similar conditions. Overall, our ONVMTs showed good data sustainability and endurance ability, making them promising candidates well suited to memory device applications.

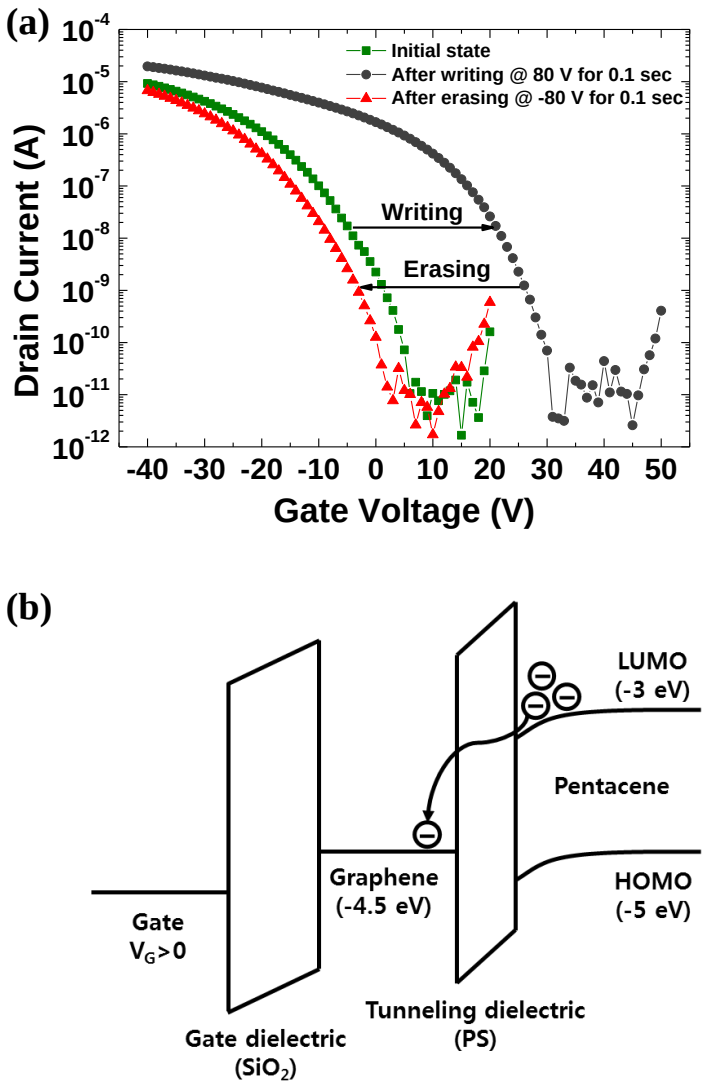

Figure 2.14 (a) Transfer characteristics of the organic memory devices according to the programming/erasing operations. Programming (+ 80 V) and erasing pulses (– 80 V) were applied to the gate for 100 ms. (b) Operating mechanism of floating gate memory device.

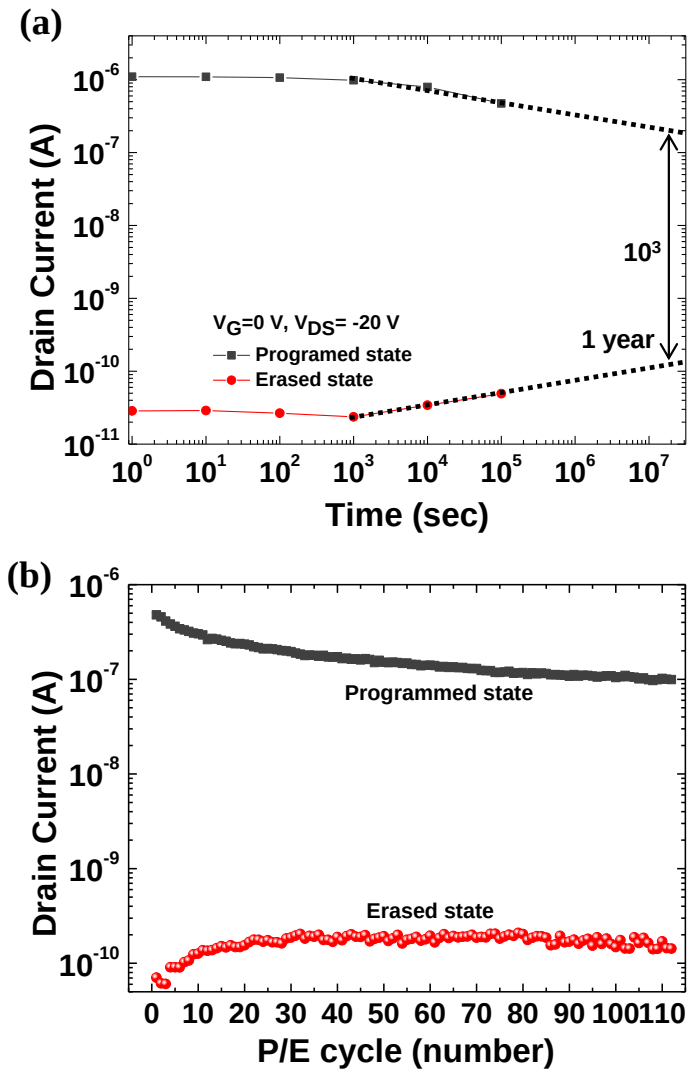

Figure 2.15 (a) Data retention characteristics of organic memory devices. (b) Endurance characteristics of memory devices after writing and erasing processes. A program/erase gate bias of 80 V was repeatedly applied for 0.5 sec, and a reading bias of -20 V was applied after each cycle to measure the drain current.

2.5 Conclusion

In summary, the ONVMTs based on the graphene floating gate have been demonstrated. In order to use graphene as a floating gate, partially grown graphene was synthesized by controlling the time of the graphene growth during a CVD process. The solution-processed PS dielectric layer was used as a charge-tunneling dielectric layer and pentacene was used as an active layer. The fabricated ONVMTs exhibited large memory windows (~ 40 V) and a good data retention ability. The shift of the transfer curves at various gate biases indicated a clear charge-trapping and de-trapping behavior in the partially grown graphene within a short period of time (100 ms). The data retention properties of our devices showed an on/off ratio of about 5×10^4 even after 10^5 s, which leads to the estimated charge storage time of more than a year. The fabricated ONVMTs were reliable after more than one-hundred repeated programming/erasing cycle tests. Although the memory performance needs to be further improved, the mechanical flexibility and optical transparency of the organic and the partially grown graphene layers are expected to show great promise for use in transparent and flexible next generation memory applications.

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Chapter 3

Inkjet-Printed Single-Wall Carbon Nanotube Transistors and Inverter

3.1 Introduction

Solution process technology, which uses the precursor type of nanoparticle type of material solutions, has been attracting great interest for use in various applications such as thin-film transistors, light emitting diodes, solar cells, and sensors. [1-4] Various solution process methods such as spin-coating, inkjet-printing, roll-to-roll, gravure-coating, and screen-printing have been used for the solution-based processes as shown in Figure 3.1. Solution-process method has the advantages of simple, low cost, and potential of applicable to large area substrate. [5-8] Among these technologies, inkjet printing technology has been attracting great interest for use in various applications. The advantages of this technology

include additive patterning, reduction of material waste, and compatibility with flexible and large area substrates. This printing technology can lead to a substantial reduction in cost and time in electronics manufacturing because patterns can be directly drawn on targeted locations without a patterning process and can be easily altered. [9, 10] For inkjet printing technology, selection of material is important for the device performance. In field effect transistor device, semiconductor material is critical for the electrical properties. Recently, novel active materials such as conjugated polymers and semiconducting metal oxides, have been explored for inkjet printing applications. In particular, organic and oxide semiconducting materials such as 6,13-bis (triisopropyl-silylethynyl) pentacene (TIPS-pentacene) and IGZO materials are usually used as active materials in field effect transistor device for inkjet printing technology. [11-13] But these semiconducting materials have disadvantages such as chemical stability and high temperature process and low carrier mobility. So recently, single-walled carbon nanotube (SWCNT) semiconducting materials are expected to enable the next generation high-performance, flexible electronic devices due to their intrinsic properties, such as high chemical stability, high carrier mobility, transparency, and remarkable mechanical properties. In general, SWCNT was deposited by solution process such as dipping method, spin-coating method. But these methods waste a lot of SWCNT material, and cover all of substrate. Thus, additional patterning process including photolithography is required to minimize gate leakage current. In this chapter, we illustrate SWCNT transistors based on inkjet printing technology for high performance and uniformity and illustrated advantages of inkjet printing method compared to other deposition method. For successful inkjet printing of SWCNTs solution, we optimized

jetting conditions such as ink jetting velocity and drop-space. In SWCNT transistor, it is critical that the ink wets the targeted surface uniformly since networks of SWCNTs are formed during the drying of the ink. To deposit high density and uniform SWCNT films on substrate, we used surface treatment with poly-L-lysine (PLL) to enhance adhesion between SWCNTs and substrate. [14, 15] To avoid SWCNT bundling, sequential inkjet printing multiple times has been used. Also for source and drain in SWCNT transistor, we deposited Ag using inkjet printing method. Also from this inkjet-printed SWCNT transistor, we fabricated and evaluated SWCNT inverter logic circuits. For inkjet-printed SWCNT inverter, we used inkjet-printed Ag gate and PVP gate dielectric was spin coated on glass substrate.

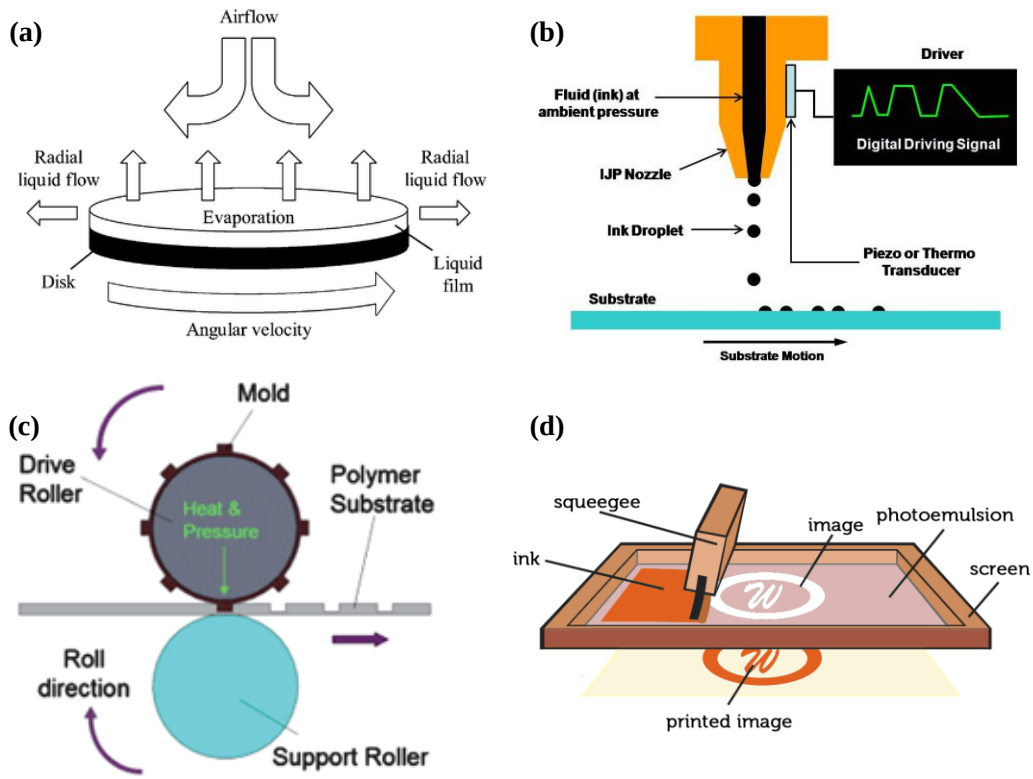


Figure 3.1 Various deposition techniques of solution-process: (a) spin-coating, (b) inkjet printing, (c) roll-to-roll and (d) screen printing

3.2 Materials and Process

3.2.1 Single-Wall Carbon Nanotubes

Carbon nanotubes (CNTs) is considered as a cylinder formed by rolling a piece of graphene. The CNTs has been widely studied for many aspects in recent years for their unique properties, which are valuable for nanotechnology, electronics, optics and other fields of materials science and technology. [16] In particular, owing to their extraordinary thermal conductivity and mechanical and electrical properties, carbon nanotubes find applications as additives to various structural materials. From this electrical properties, SWCNTs, especially semiconducting SWCNTs, have been expected to be used as alternative semiconducting material for field effect transistors. [17] Field effect transistor are widely used and studied. In particular, thin film transistors (TFTs) are widely used for flat panel display, flexible electronics, and sensor applications. Various semiconducting materials have been used in TFTs applications such as α-Si, poly-silicon, organic and oxide semiconductors. [18, 19] SWCNTs possess high mobility, high transparency, and good flexibility simultaneously. These attractive properties satisfy the requirements of thin film transistors, making CNTs the most promising candidates as the high-performance TFT channel material. There are some method to synthesize the CNT. To synthesize carbon nanotubes, arc discharge, laser ablation, and chemical vapor deposition (CVD) methods are used. Among these methods, the laser and arc methods require very high temperature to fabricate CNTs, while the location and alignment of the CNTs are difficult to control. So CVD is the most widely adopted due to its advantages of low cost, controllable synthesis,

and high throughput. [20-22] By controlling the parameters of catalyst, carbon source, gas pressure, and reaction temperature, CVD synthesize method can control the location, the orientation, and the diameter of CNTs for the specific applications. From this advantages, for thin film transistors, carbon nanotubes are usually synthesized by thermal CVD or plasma-enhanced chemical vapor deposition (PECVD). [23] In CVD synthesize method, PECVD is more widely used because of the advantages of PECVD that the products are mainly semiconducting nanotubes, with the ratio as high as 90%. The semiconducting CNT ratio is very critical for fabricating thin film transistors. In CNTs, graphene sheets are rolled at specific and discrete ("chiral") angles, and the combination of the rolling angle and radius decides the nanotube properties whether metallic or semiconducting. So in general, the semiconducting metallic nanotubes and semiconducting nanotubes coexist in the synthesized carbon nanotubes all the time. This is a fatal obstacle impeding the development of SWCNT-based electronics because the metallic CNTs lack gate control and degrade the ON/OFF ratio of devices. Separating metallic and semiconducting nanotubes is a very critical technology, which also have attracted extensive research efforts. Different innovative approaches have been proposed to solve this problem, including electrical breakdown, density gradient ultracentrifugation, gel-based separation, dielectrophoresis, and DNA sequence separation. [24, 25] Each of them has its advantages. For example, utilizing electrical breakdown to separate nanotubes does not need any extra-process step during the device fabrication. In these various purification methods, density gradient ultracentrifugation method is widely used because this method can achieve 98% purity of semiconducting carbon nanotubes. [24] After purification of CNTs, the semiconducting

CNTs can be used to fabricate field effect transistors or thin film transistors. For thin film transistors, CNTs are used in form of CNT film, which is composed of random networks. There are various methods to deposit carbon nanotube on substrate, including filtration, dip coating, transfer printing, ink-jet printing, spray coating. Each method has its advantages and disadvantages. [26] Using filtration process can form uniform CNT films, and the films allow to be transferred to the other substrates. However, the process is relatively complicated. Dip coating, spray coating, and transfer printing are all low-temperature processes. Spray coating and dip coating are both simple fabrication processes. However, spray coating cannot be used for large area or mass production and films fabricated by spray coating lack uniformity. Dip coating lacks controllability. In inkjet printing method, SWCNT solution was used as ink and prints SWCNT onto the substrate to form thin film. This inkjet printing technology is illustrated more in specific in next chapter.

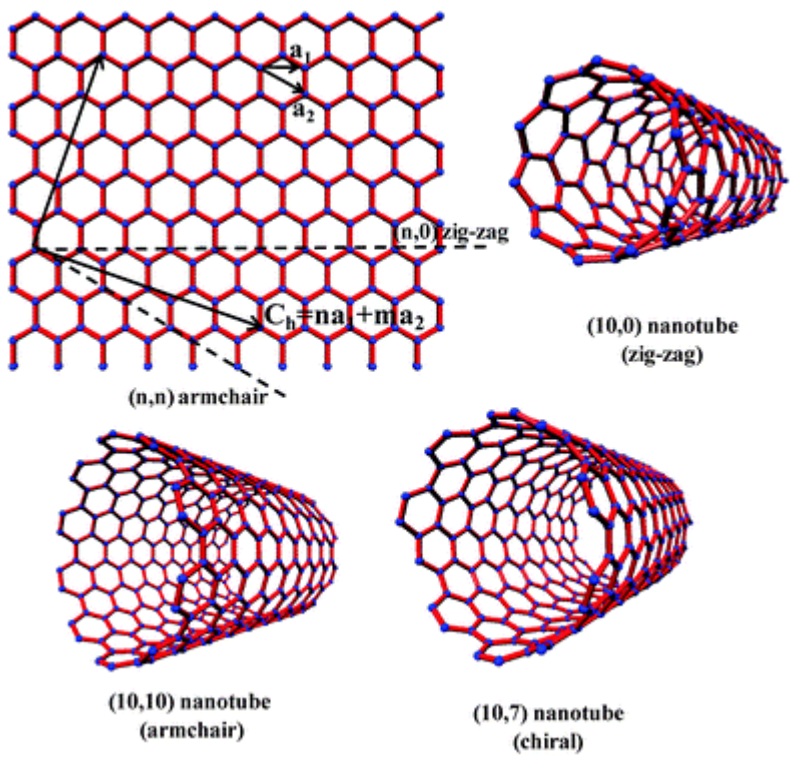


Figure 3.2 Schematic representation of the relation between nanotubes and graphene

3.2.2 Inkjet-Printing Systems

Inkjet printing method is one of the solution-based processes, which has advantages of maskless patterning due to direct pattern definition, non-vacuum process, large area manufacturing, high throughput and economical use of the inks. In general, inkjet printing is familiar method for transferring electronic data to paper or plastic substrate. However, in recent years, much effort has been invested in turning inkjet printing into a versatile tool for various industrial manufacturing processes, in order to accurately deposit minute quantities of materials. [7] Compared to previous conventional photo-lithography, this inkjet printing method is much cheaper and simpler because this process doesn't need any material waste and contamination from mask contact or PR deposition / strip. [10, 27, 28] From this advantages, inkjet printing is considered to be one of the key technologies in the industrial fields such as defined polymer deposition, particularly in relation to the manufacturing of multicolor polymer light-emitting diode (PLED) displays. [28] The display is printed pixel-wise using solutions of differently colored electroluminescent polymers. In general, inkjet printing system used drop-on-demand mode. In this mode, uniformly spaced and sized droplets are obtained by imposing a periodic perturbation. A piezo-electrical pulse ejects ink droplets from a cartridge of printer through a nozzle. This inkjet printing relies on the deformation of some piezoelectric material to cause a sudden volume change and hence generate an acoustic pulse. Therefore, the most crucial part of inkjet printing technology is the optimization of ink properties such as the viscosity and surface tension. [29, 30]

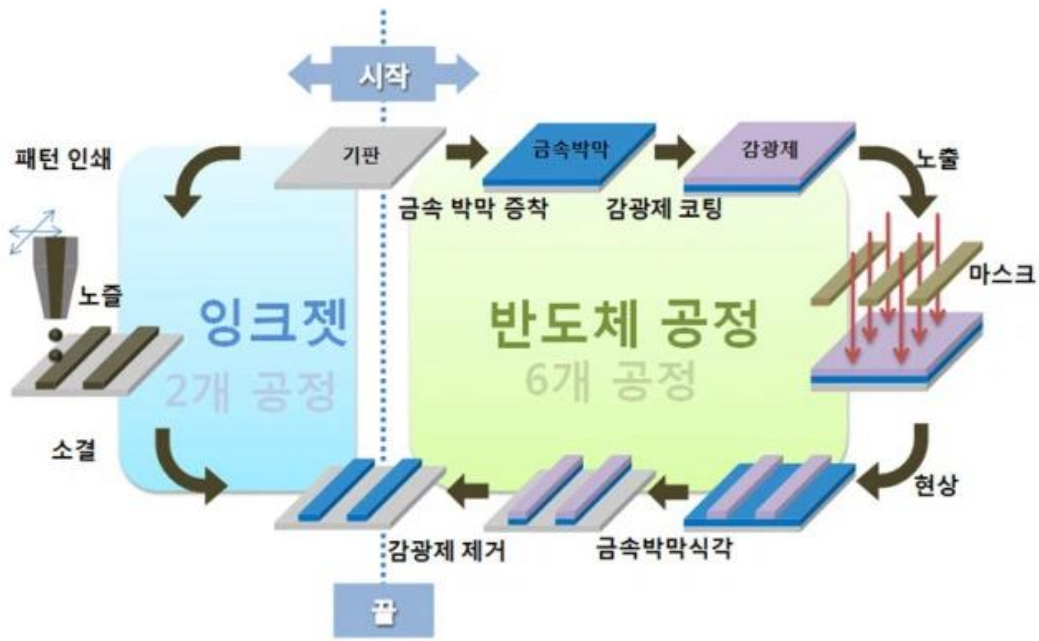


Figure 3.3 Inkjet printing process comparing with conventional photolithography

3.3 Inkjet-Printed SWCNT Transistors

3.3.1 Experiments

To compare effect of fabrication method, we fabricated two type of SWCNT transistors. One device is fabricated by inkjet printing method the other device is fabricated by dipping method. For the SWCNT film as an active channel, both method used 95% of semiconducting SWCNT solution purchased from Nanointegris Inc.. In this solution, 95% semiconducting SWCNT was dispersed in DI water with ionized surfactant for stabilizer. For each SWCNT transistor, we used the heavily doped p-type Si substrate with thermally grown 200 nm thick silicon dioxide dielectric. For cleaning process, the substrate was cleaned with acetone, isopropyl alcohol (IPA) and deionized (DI) water in bath type ultra-sonicator for 20 min, respectively. To deposit SWCNT on SiO_2 dielectric, surface treatment was necessary. To optimize the surface energy of SiO_2 layer with PLL solution, ultraviolet light/ozone (UVO) treatment was performed on the SiO_2 dielectric for 10 min to lower the surface energy with the remained organic particles. This process made the surface of SiO_2 layer hydrophilic. To functionalize the surface of substrate, the substrate was immersed in PLL solution for 10 min at ambient condition and rinsed with DI water to enhance subsequent SWCNT adhesion. To deposit SWCNT film on SiO_2 by dipping method, PLL treated substrate was immersed in 95% of SWCNT solution by dipping method for 5 min, then followed by a thorough rinse with DI water and dried with a nitrogen gun. To deposit the SWCNT film by inkjet printing method, we used the piezoelectric type inkjet printer (DMP-2831 corp.) and the 10 pL cartridge (DMC-11601), which has 16 numbers of multi-

nozzles and the diameter of each nozzle is about 21 μm. During inkjet printing of SWCNT solution, the substrate was kept at 40 ℃. We used only 1 nozzle for uniform film quality and the drop spacing was adjusted to 25 μm. After printing, substrate was dried in air for 30 min. It was then followed by a thorough rinse with DI water and dried with a nitrogen gun, resulting in uniform assembly of SWCNT random network over the printed surface of the substrate. In both device, to deposit source and drain electrodes, we used precursor type silver ink (JET-600C). During printing, the substrate was kept at 40 ℃ and the drop spacing of inkjet printing system was adjusted to 40 μm. 1 nozzle was used for the silver inkjet-printing. After the inkjet printing of silver source and drain, substrate was sintered in a convection oven at 150 ℃ for 1 h to evaporate the solvent of silver ink. Electrical characteristics of device was measured by Agilent 4155C semiconductor parameter analyzer in ambient condition.

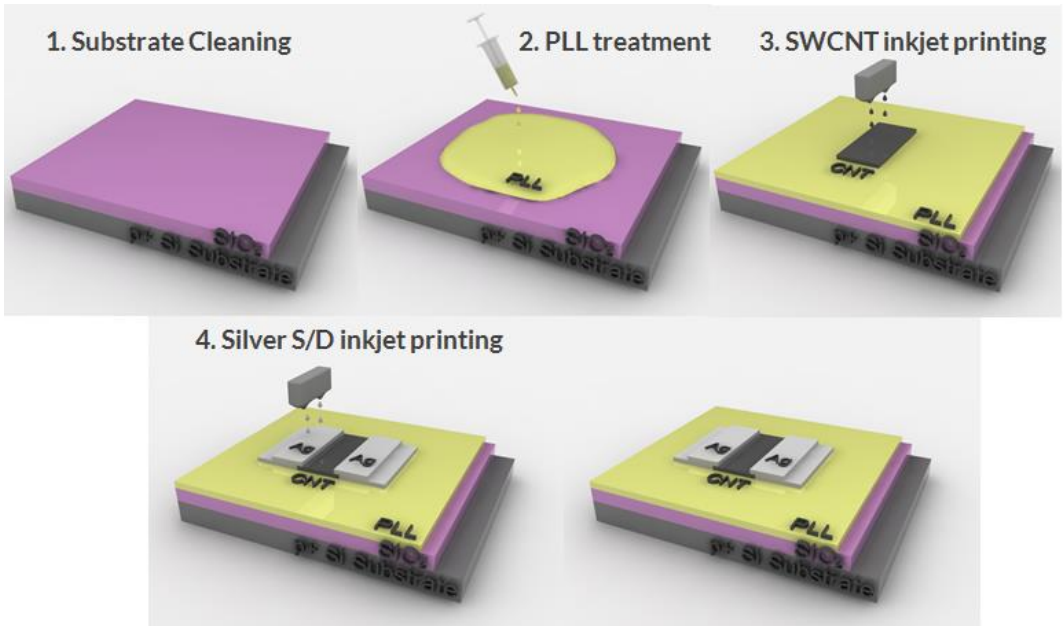


Figure 3.4 Fabrication process of inkjet-printed SWCNT transistor

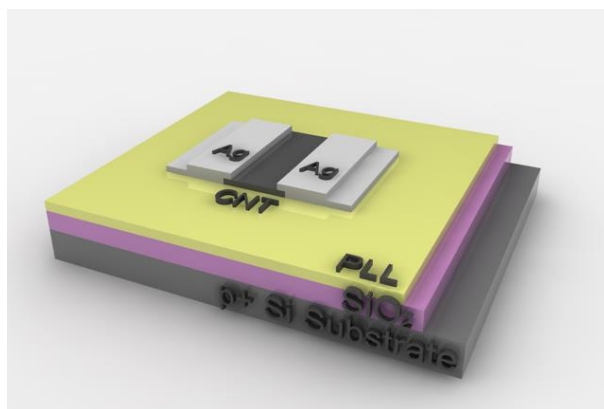


Figure 3.5 Schematic of SWCNT transistors

3.3.2 Results

To investigate the deposition of SWCNT channel in both devices, AFM were performed at area of active area of both devices. Figure 3.6 (a), (b) show the AFM images of SWCNT network on each SiO_2 substrate by inkjet printing method and dipping method. It can be clearly observed that SWCNT film coverage by both methods is uniform and densely distributed. Figure 3.7 (a), 4(b) show transfer and output characteristics of SWCNT TFT fabricated by dipping method. The devices measurements were performed in ambient conditions using a 4155C semiconductor parameter analyzer. First, SWCNT TFT device by inkjet printing method shows a high intrinsic mobility of 2.1 $cm^2/V \cdot s$, I_{on}/I_{off} of $4x10^2$, and a threshold voltage of - 0.7 V. The field-effect mobility μ and threshold voltage were subsequently calculated using the following equation:

$$I_D = \frac{W}{2L}\mu C_i(V_{GS} - V_{th})^2$$

where C_i is the insulator capacitance per unit area and V_{th} is the threshold voltage. We calculated C using a HP-4284A LCR meter in air at room temperature. In the case of SWCNT transistor fabricated by dipping method, high gate leakage current measured in transfer characteristics as shown in Figure 3.7 (a). In addition, output characteristics in Figure 3.7 (b) shows the distortion of the drain current at low V_{DS} bias condition. It indicates that SWCNT transistor fabricated by dipping method cannot operate at low V_{DS} due to the high gate leakage current. On the other hand, SWCNT transistor fabricated by inkjet printing method showed enhanced electrical performance of reduced gate leakage current with the low drain current when the device turned off. The high gate leakage current

in dipping method was resulted from the not patterned SWCNT film which covered all the surface of device. This not patterned of SWCNT film provide the leakage paths between gate electrode and S/D electrode. Thus, additional patterning process including photolithography is required to minimize gate leakage current in dipping method. Figure 3.8 (a), (b) show typical transfer and output characteristics of SWCNT TFT by inkjet printing method. The output characteristics showed linear curve at low drain voltages (V_D < -1 V), indicating that the contact resistance of SWCNT and the S/D electrode is negligible. The transfer characteristic was measured between gate voltage of 5 V and -5 V with fixed drain bias of -1 V. This device shows a high intrinsic mobility of 10 $cm^2V^{-1}s^{-1}$, I_{on}/I_{off} of $1x10^6$, and a threshold voltage of 1 V.

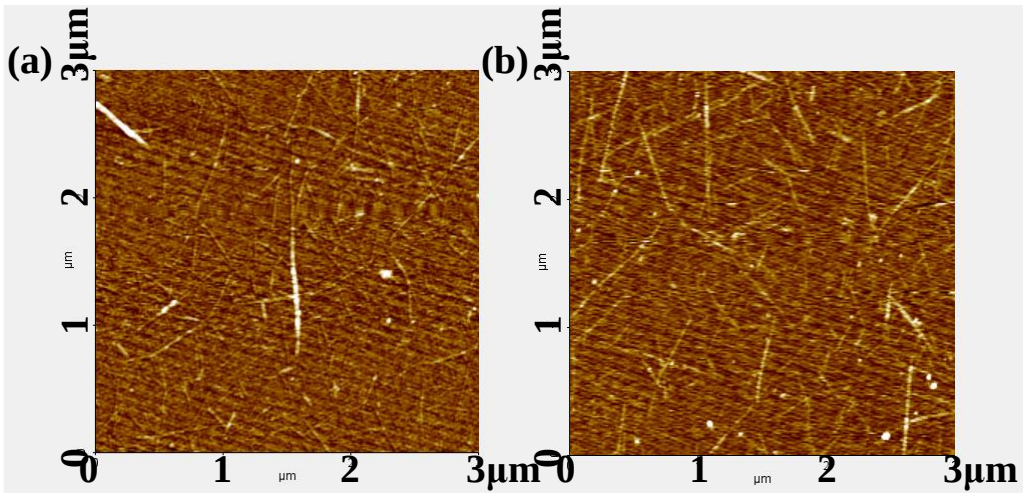
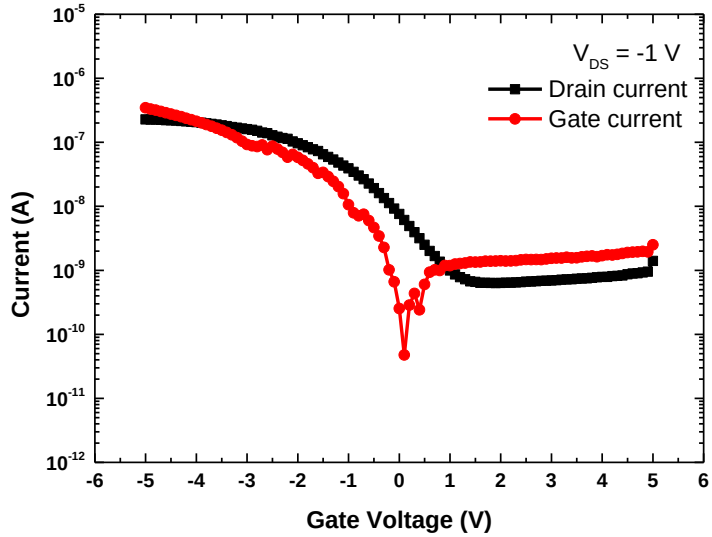


Figure 3.6 AFM image of SWCNT in dipping method, and inkjet printing method

(a)



(b)

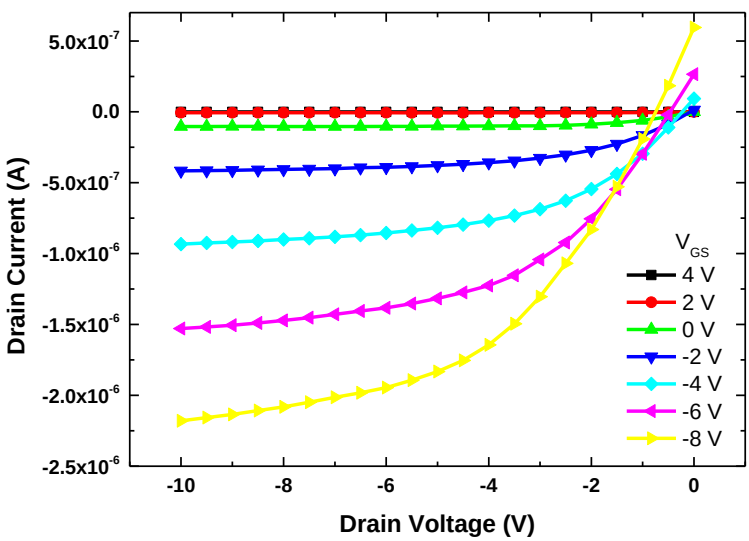


Figure 3.7 (a) Transfer characteristics and (b) output characteristics of SWCNT transistors by dipping method

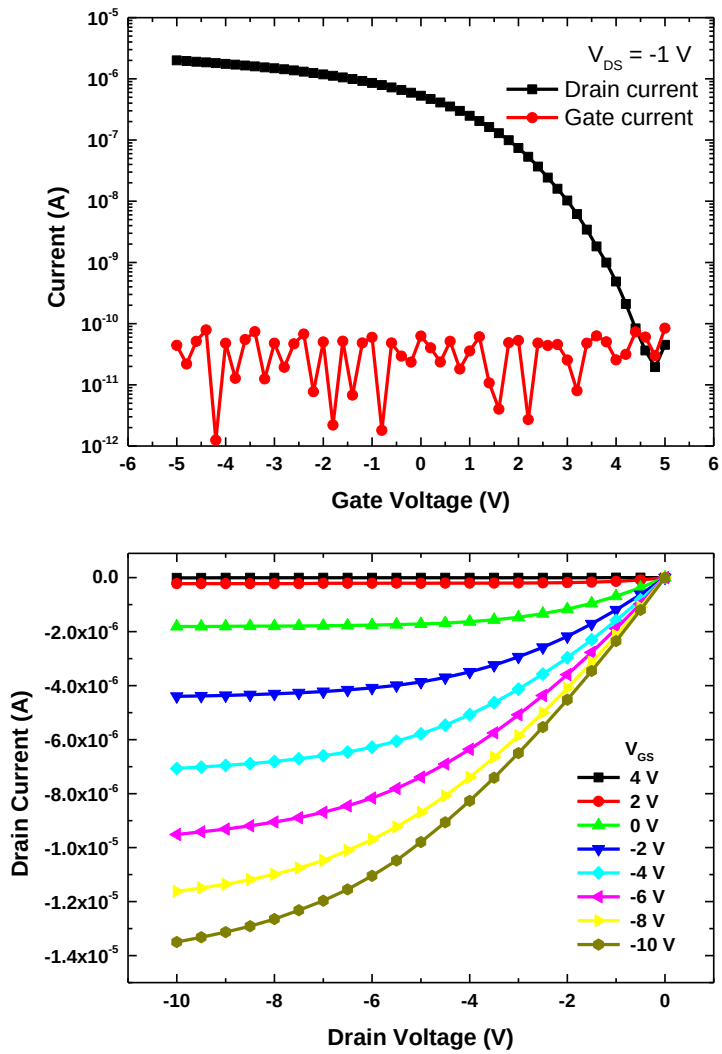


Figure 3.8 (a) Transfer characteristics and (b) output characteristics of SWCNT transistors by inkjet printing method

3.4 Inkjet-Printed SWCNT Inverter

The inverter is most-basic unit for a logic circuit to invert the input signal applied. The inverter circuit outputs a voltage representing the opposite logic-level to its input. If the applied input is low then the output becomes high and vice versa. Inverters can be constructed using a single NMOS transistor or a single PMOS transistor coupled with a resistor. Since this 'resistive-drain' approach uses only a single type of transistor, it can be fabricated at low cost. However, because current flows through the resistor in one of the two states, the resistive-drain configuration is disadvantaged for power consumption and processing speed. Alternatively, inverters can be constructed using two complementary transistors in a complementary metal–oxide–semiconductor (CMOS) configuration. This configuration greatly reduces power consumption since one of the transistors is always off in both logic states. Processing speed can also be improved due to the relatively low resistance compared to the NMOS-only or PMOS-only type devices. Inverters can also be constructed with bipolar junction transistors in either a resistor–transistor logic or a transistor–transistor logic configuration. Digital electronics circuits operate at fixed voltage levels corresponding to a logical 0 or 1. An inverter circuit serves as the basic logic gate to swap between those two voltage levels.

3.4.1 Experiments

The inkjet-printed SWCNT inverter was fabricated on 2 cm x 2 cm bare glass substrate (Eagle X) and its structure and fabrication process are illustrated in Figure 3.9. First, glass substrate was cleaned sequentially with acetone, isopropyl alcohol (IPA) and deionized (DI) water in the ultra-sonicator at 40 ℃ for 20 min, respectively. Before inkjet printing of gate electrode, ultraviolet light/ozone (UVO) treatment was performed on the glass substrate for 5 min to lower the surface energy with cleaning the remained organic particles, so that the surface of glass was modified more hydrophilic. For the inkjet printing, we used the piezoelectric type inkjet printer (DMP-2831, Dimatix corp.) and the 10 pL cartridge (DMC-11601), which has 16 numbers of multi-nozzles and the diameter of each nozzle is about 21 μm. Ink-jetting conditions were carefully optimized to obtain uniform layer by controlling a waveform voltage, a cartridge temperature, an ink drop velocity and a fire frequency considering ink properties. For bottom gate electrode formation, a transparent metal-organic precursor type ink ANP ink was inkjet-printed. The silver ink was printed with a drop velocity of about 5 m/s, and a drop spacing of 25 μm which mean distance between ink drops. These two parameters determine thickness and width of the silver electrodes. Substrate temperature was maintained at 40^{o}C during the inkjet-printing process to vaporize silver ink solvent quickly, resulting in better surface properties, film uniformity and shiny appearance. The printed gate electrode has 18 mm x 5 mm size to minimize the gate leakage current. After the gate electrode was printed, the substrate was annealed at 150 ℃ for 30 min on hotplate under atmospheric environment. We obtained a sheet

resistance of 0.4 Ω/□ from the 200 nm thick silver electrodes. For dielectric, poly (4-vinylphenol) (PVP) was deposited on the fabricated silver gate electrode by spin coating method. Cross-linked PVP is one of the most widely used organic insulating materials due to its good insulating performance and low-temperature thermal curing condition. The PVP solution was composed of 10 wt% of PVP and 2 wt% of poly(melamine-co-formaldehyde) as a cross-linking agent (CLA) dissolved in propylene glycol methyl ether acetate (PGMEA) as a solvent from Sigma-Aldrich Corp. PVP and CLA concentration was critical factor for thickness of film and this affect capacitance and insulating properties. PVP solution through a hydrophilic filter was spin-coated on the gate printed glass substrate at 3000 rpm for 40 s in air. Soft-baking was performed on the hot plate at 120 ℃ for 20 min in air to evaporate the solvent of PVP. Then, the films were annealed at 200 ℃ for 30 min in air under atmospheric condition to obtain the cross-linked gate dielectric layer. To deposit the SWCNT semiconductor by inkjet printing method, surface was treated using poly-L-lysine (PLL) solution on UVO treated PVP surface. To optimize the surface energy with PLL solution, UVO treatment was performed on the PVP dielectric for 10 min to lower the surface energy. For PLL treatment, the substrate was immersed in PLL solution for 10 min at ambient condition and rinsed with DI water to enhance subsequent SWCNT adhesion. During inkjet printing of SWCNT solution, the substrate was kept at 40 ℃. We used only 1 nozzle and the drop spacing was adjusted to 25 μm. After printing, substrate was dried in air for 30 min. It was then followed by a thorough rinse with DI water and dried with a nitrogen gun, resulting in uniform assembly of SWCNT random network over the printed surface of the substrate. To deposit source and drain electrodes, we used precursor type

silver ink (JET-600C). To deposit silver source and drain, the substrate was kept at 40 ℃. And the drop spacing of inkjet printing system was adjusted to 40 μm. 2 nozzle was used for the silver inkjet-printing. After the inkjet printing of silver source and drain, substrate was sintered in a convection oven at 150 ℃ for 1 h to evaporate the solvent of silver ink. Electrical characteristics of device was measured by Agilent 4155C semiconductor parameter analyzer in ambient condition.

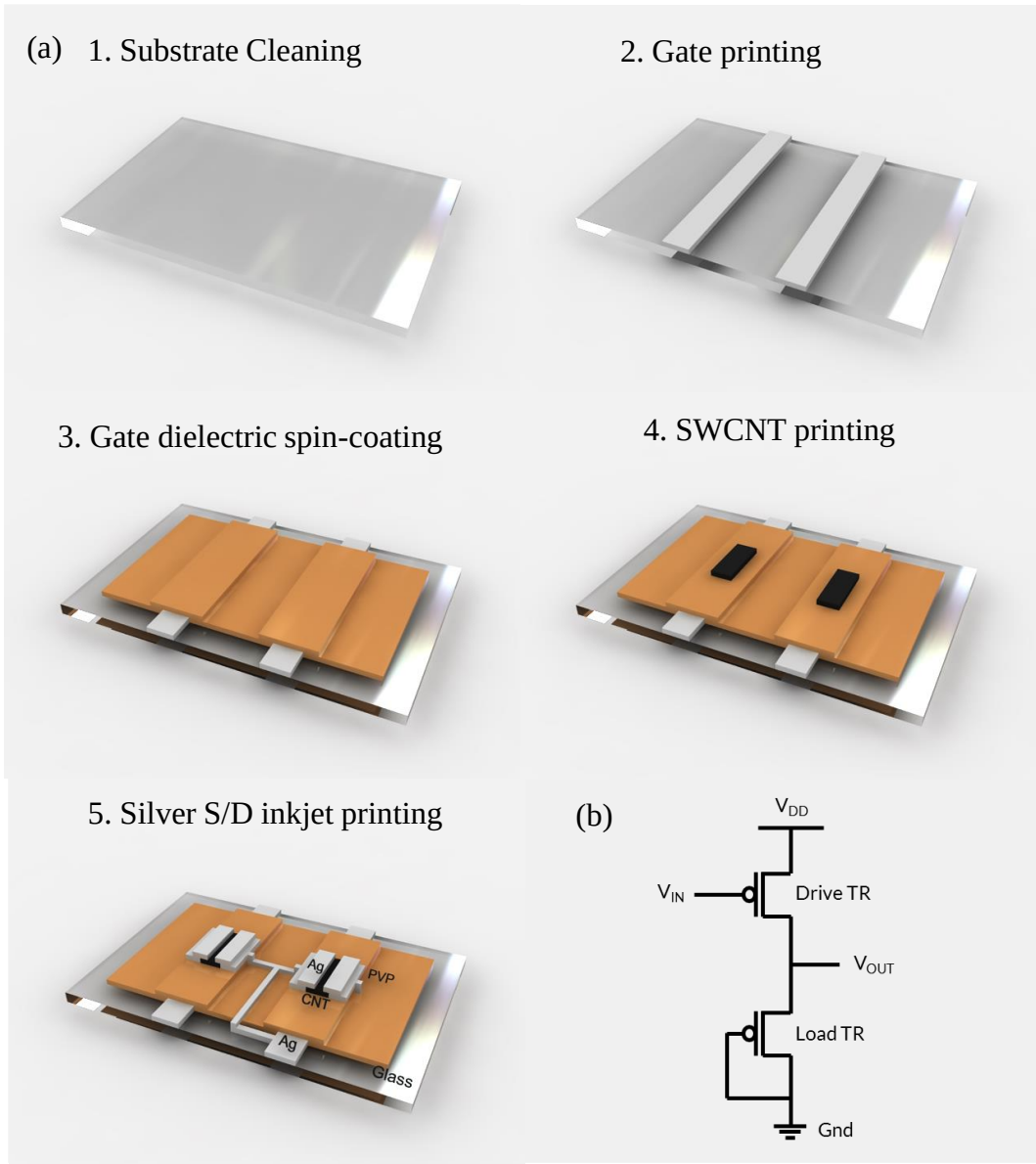


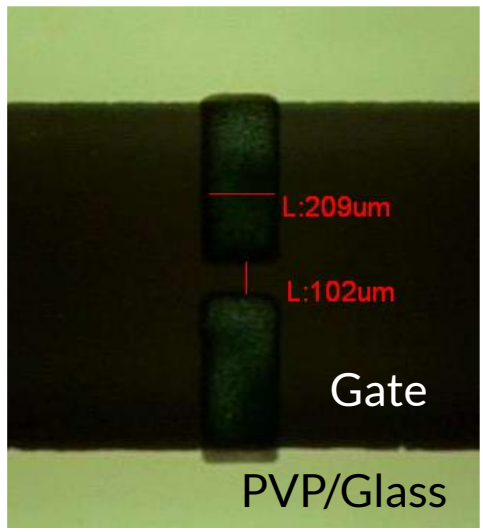
Figure 3.9 (a) Fabrication process and (b) circuit schematic of inkjet-printed SWCNT inverter

3.4.2 Results

The complementary circuit that is composed of n-channel and p-channel transistors is the best choice because the voltage transfer characteristic is nearly ideal due to the full swing characteristic, high noise margin and high inverting gain. However, the performance of n-channel SWCNT TFTs is significantly lower than that of p-channel SWCNT TFTs and most of n-type SWCNT TFTs are unstable in the atmosphere. Therefore, many SWCNT circuits are based on the p-channel SWCNT TFTs. Figure 3. 10 (a), (b) shows optical image of the fabricated SWCNT transistor on glass substrate and SWCNT inverter. Figure 3.11 (a), (b) shows the electrical characteristics of the top contact SWCNT TFT on glass substrate using inkjet printing method. Inkjet-printed Ag was used as gate electrode, and the spin-coated PVP was used as gate dielectric on glass substrate. This inkjet-printed SWCNT TFTs device has 2 cm^2/Vs of field effect mobility, 1 V of threshold voltage and 10^5 of I_{on}/I_{off} ratio. This results are similar to previous inkjet-printed SWCNT TFT on SiO_2 substrate but shows lower mobility than pervious results. From these results, we fabricated SWCNT inverter. For inkjet-printed SWCNT inverter, we connected two inkjet-printed SWCNT transistor as illustrated in Figure 3. 9 (b). Electrical performance of inverter is often measured using the voltage transfer curve (VTC), which is a plot of output vs. input voltage. From such a graph, device parameters including noise tolerance, gain, and operating logic levels can be obtained. Ideally, the VTC appears as an inverted step function but in real devices, a gradual transition region exists. The VTC indicates that for low input voltage, the circuit outputs high voltage; for high input, the output tapers off towards the

low level. The slope of this transition region is a measure of quality and steep slopes yield precise switching. The electrical properties of fabricated inkjet-printed SWCNT inverter is illustrated in Figure 3.12. To measure the electrical performance, we applied input voltage from 5 V to -10 V depending on various V_{DD} condition to confirm transition region. As shown VTC characteristic, fabricated inkjet-printed SWCNT inverter was operated normally. But fabricated SWCNT inverter showed low gain with maximum value of 0.9 as shown in Figure 3.12 (b). This value is larger than previously reported organic inverter because of high mobility of SWCNT TFT, but is not good for circuit applications. To improve the inverter performance, further optimization of current-matching, enhancement of SWCNT transistor's property and reduction of parasitic capacitance by patterning the gate electrodes were required.

(a)



(b)

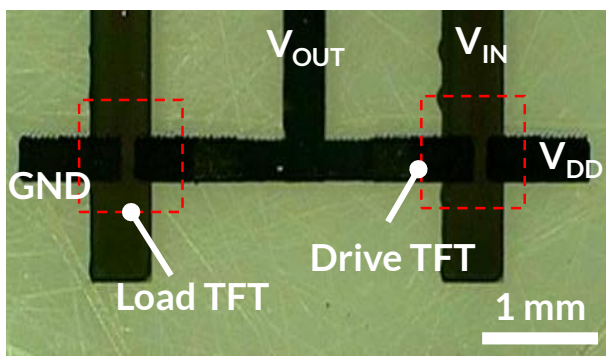


Figure 3.10 Optical image of (a) inkjet-printed SWCNT TFTs on glass substrate and (b) inkjet-printed SWCNT inverter

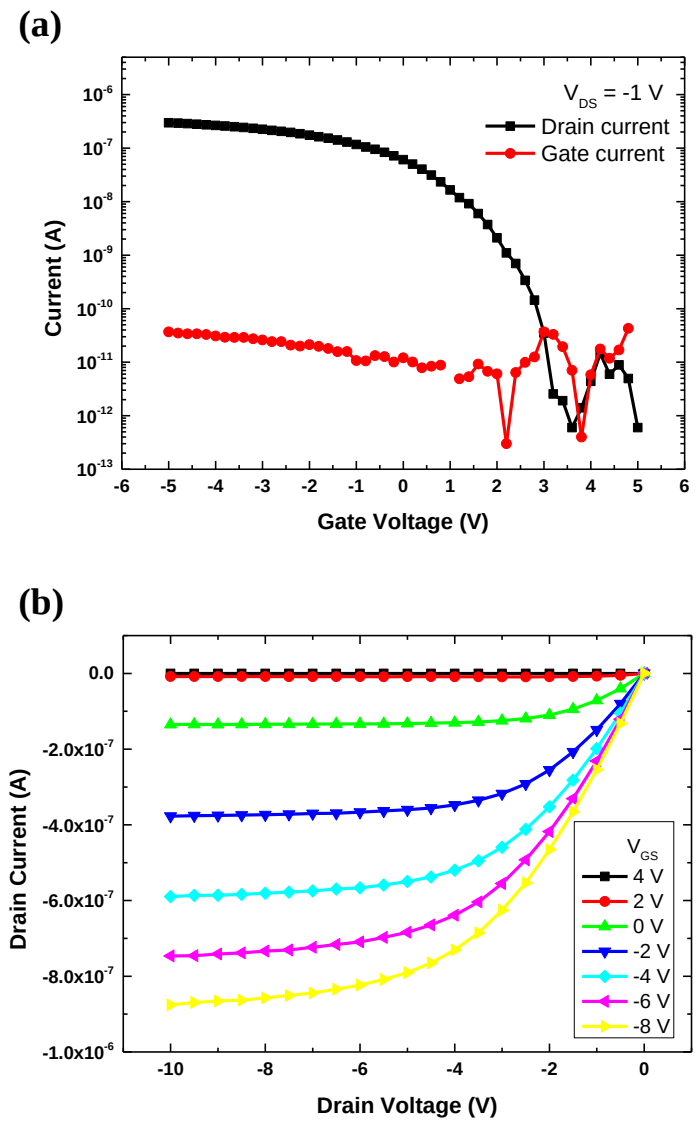


Figure 3.11 (a) Transfer characteristics and (b) output characteristics of SWCNT transistors on PVP dielectric by inkjet printing method

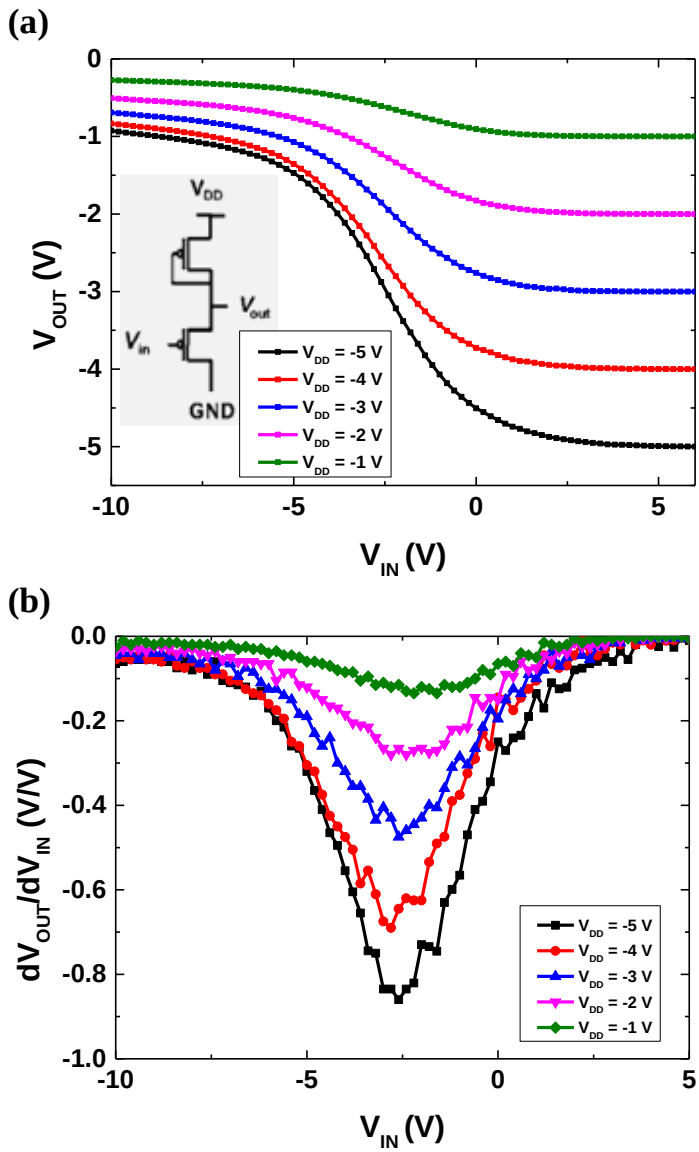


Figure 3.12 (a) Inkjet-printed SWCNT inverter with two p-type SWCNT transistor and circuit schematic and (b) inverter gain

3.5 Conclusion

Inkjet printing method is one of the solution-based processes, which has advantages of maskless patterning due to direct pattern definition, non-vacuum process, large area manufacturing, high throughput and economical use of the inks. From this advantages, inkjet printing is considered to be one of the key technologies in the industrial fields such as TFTs and display application. In the fabrication of inkjet-printed TFTs, organic semiconductors such as TIPS-pentacene and oxide semiconductors are usually used as active layer for inkjet-printed TFTs. However, most SWCNT films were deposited by spin-coating, or dipping method so that additional processes were added to pattern the active area. So in this chapter, we reported inkjet-printed SWCNT transistors and SWCNT inverter. By using optimized inkjet printing method, we deposited the semiconducting SWCNT and source and drain electrodes. For inkjet-printed SWCNT transistor, we deposited the semiconducting SWCNT solution on SiO_2 substrate and Ag source/drain electrodes by inkjet printing method. The fabricated inkjet-printed SWCNT transistors showed high electrical performance and low gate leakage current without any patterning method. For SWCNT inverter, we deposited semiconducting SWCNT and Ag gate and source/drain electrodes by inkjet printing method on glass substrate with spin-coated PVP. The fabricated SWCNT inverter by inkjet printing method showed clear transfer characteristics. From this method, we could archive inverter characteristics. Our fabrication method using inkjet printing was simple, fast, and cost effective. Furthermore, it was not required patterning process such as photolithography.

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Chapter 4

Inkjet-Printed SWCNT Random Access Memory

4.1 Introduction

Recently, the utility of the single-wall carbon nanotube (SWCNT) transistors is extended to the logic circuitry for the low-end smart card or identification tag as well as to the pixel-driving transistor or display driving circuit. [1-4] Also complex circuits have been demonstrated using SWCNT transistors, such as shift register, radio-frequency identification circuitry, and memory device. Among these devices, static random-access memory (SRAM) is a type of semiconductor memory that uses bi-stable latching circuitry (flip-flop) to store each bit. SRAM exhibits data remanence but it is still volatile in the conventional sense that data is eventually lost when the memory is not powered. Therefore,

the simplicity of the SWCNT circuit configuration and the high noise immunity become important. From this point of view, the complementary circuit that is composed of n-channel and p-channel transistors is the best choice because the voltage transfer characteristic (VTC) is nearly ideal due to the full swing characteristic, high noise margin and high inverting gain. However, the performance of n-channel SWCNT is significantly lower than that of p-channel SWCNT and most of n-type carbon nanotubes semiconductor shows poor electrical properties in the atmosphere. [5] Therefore, many SWCNT circuits are based on the p-channel SWCNT. Furthermore, in the case of SWCNT SRAM, complementary designs have a number of problems associated with the low field-effect mobility and poor air stability of n-channel SWCNT TFTs, which is the reason why we chose to implement a PMOS, rather than a complementary, SRAM. [5] However, solution-processed SWCNT TFTs usually shows depletion-mode characteristics. [6-8] So, in addition to the high mobility, good uniformity, and good air stability of the SWCNT TFTs, the systematic control of the threshold voltage was critical for the low-voltage SRAM design. [9, 10] The threshold-voltage control provided a good balance for the switching characteristics of the inverters in the SWCNT SRAM. So, in this section, we illustrated technology to tune V_{TH} in inkjet-printed SWCNT TFTs employing chemical encapsulation with ammonium hydroxide (NH_4OH). [11] The fabricated SWCNT inverter device showed voltage transfer curve having the high performance. Also from this result, we fabricated and analyzed inkjet-printed SWCNT SRAM.

4.2 Inkjet-Printed Full-Swing SWCNT Inverter

4.2.1 Fabrication Process

Inkjet-printed SWCNT transistor having full-swing characteristics was fabricated on bare glass substrate (Eagle X). First, the substrate was cleaned sequentially with acetone, isopropyl alcohol (IPA) and deionized (DI) water in the ultra-sonicator for 20 min, respectively. Before inkjet printing of gate electrode, ultraviolet light/ozone (UVO) treatment was performed on the glass substrate for 5 min to lower the surface energy with cleaning the remained organic particles, so that the surface of glass was modified more hydrophilic. For bottom gate electrode formation, a transparent silver ink JET-600C ink (Hisense Electronics, Kunshan, China) was printed on glass substrate. The printed gate electrode has 18 mm x 5 mm size to minimize the gate leakage current. After the gate electrode was printed, the substrate was annealed at 150 ℃ for 30 min on hotplate under atmospheric environment. For dielectric, poly (4-vinylphenol) (PVP) was deposited on the fabricated silver gate electrode by spin coating method as above experiment. Soft-baking was performed on the hot plate at 120 ℃ for 20 min in air to evaporate the solvent of PVP. Then, the films were annealed at 200 ℃ for 30 min in air under atmospheric condition to obtain the cross-linked gate dielectric layer. To deposit the SWCNT semiconductor by inkjet printing method, surface was treated using poly-L-lysine (PLL) solution on UVO treated PVP surface. [12, 13] To optimize the surface energy with PLL solution, UVO treatment was performed on the PVP dielectric for 10 min to lower the surface energy. For PLL treatment, the substrate was immersed in PLL solution for 10 min at ambient condition

and rinsed with DI water to enhance subsequent SWCNT adhesion. For inkjet-printed full-swing SWCNT inverter, we fabricated two SWCNT TFTs for drive TFTs and load TFTs. For each TFTs, we varied deposition time of inkjet-printed SWCNT to control density of SWCNT film. During inkjet printing of SWCNT solution, the substrate was kept at 40 ℃. We used only 1 nozzle and the drop spacing was adjusted to 25 μm. For drive SWCNT TFTs and load SWCNT TFTs, substrate was dried in air for 30 min and 20 min each after printing. It was then followed by a thorough rinse with DI water and dried with a nitrogen gun, resulting in uniform assembly of SWCNT random network over the printed surface of the substrate. To deposit source and drain electrodes, we used precursor type silver ink (JET-600C). A channel width is 1000 μm for drive TFT and 300 μm for load TFT. A channel length 150 μm was used for both devices. After the inkjet printing of silver source and drain, substrate was sintered in a convection oven at 150 ℃ for 30 min to evaporate the solvent of silver ink. Finally, we immersed SWCNT TFTs in 0.1 M of ammonium hydroxide (NH_4OH) (purchased from Sigma Aldrich Corp.) solution in water to tune the threshold voltage of SWCNT TFTs, by dipping method, then followed by a thorough rinse with DI water and dried with a nitrogen gun to remove residue solution and particles. [11]

Electrical characteristics of devices were measured by HP-4145B semiconductor parameter analyzer and HP-4284A LCR meter in the ambient condition. Also, to investigate a thickness of dielectric films and morphology of pentacene layer, atomic force microscopy (AFM, XE-100) was used.

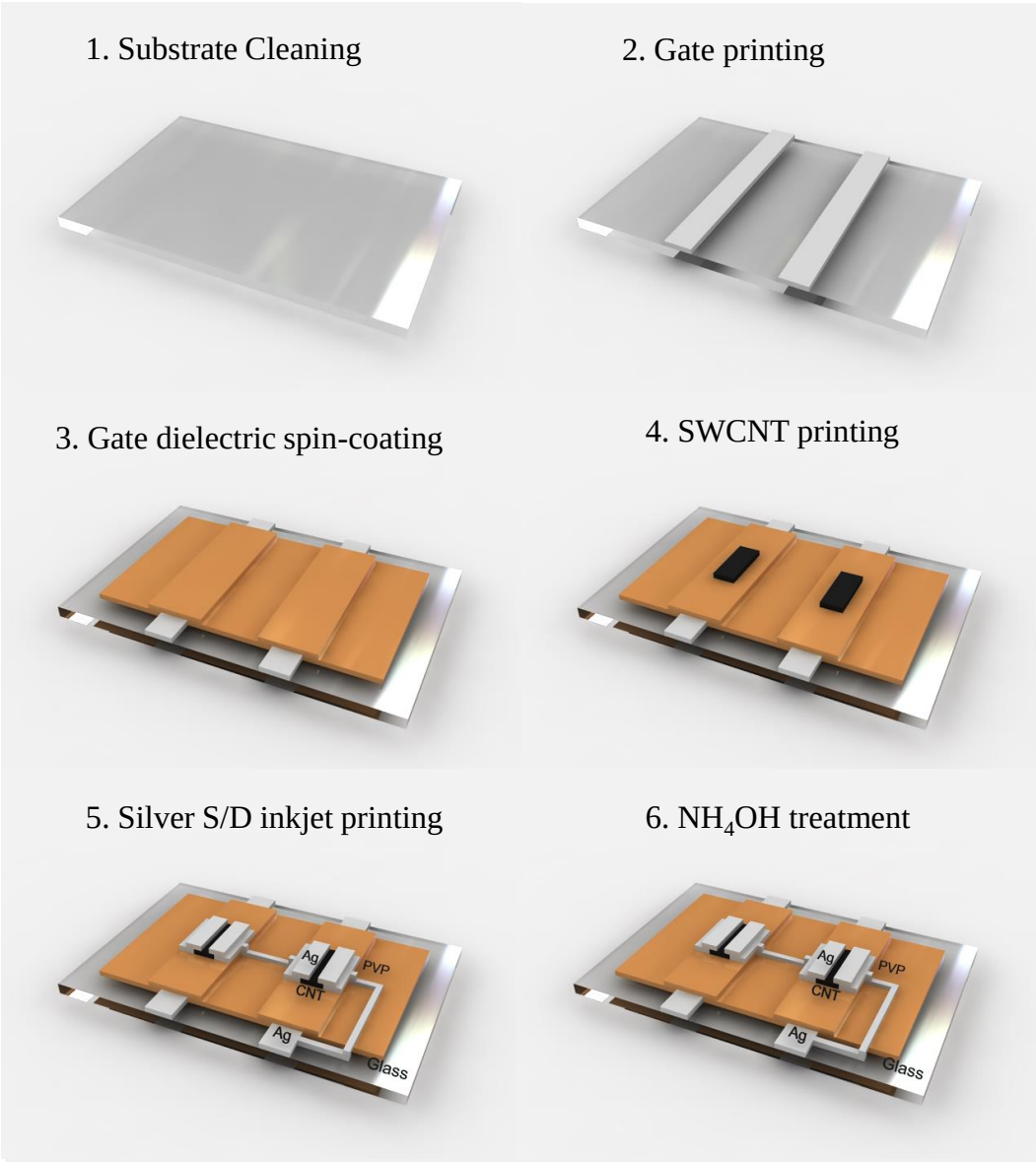


Figure 4.1 Fabrication process of inkjet-printed full-swing inverter

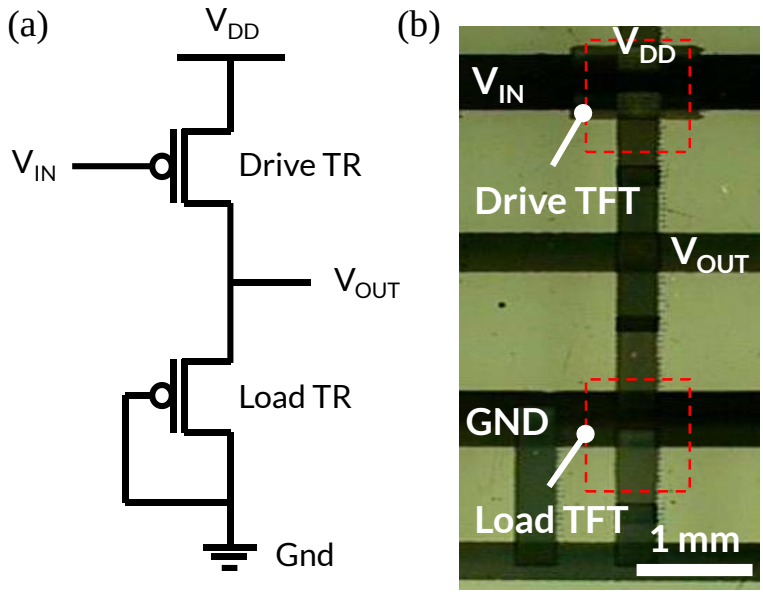


Figure 4.2 (a) Circuit diagram and (b) optical image of SWCNT full-swing inverter

4.2.2 Results

Figure 4.2 (a), (b) shows the schematic diagram and optical image of fabricated the full-swing organic inverter which is composed of driver transistor and load transistor. Fabricated inverter has the top contact structure on glass substrate using inkjet printing method. Inkjet-printed Ag was used as gate electrode, and the spin-coated PVP was used as gate dielectric on glass substrate. For inkjet-printed full-swing SWCNT inverter, we fabricated two SWCNT TFTs for drive TFTs and load TFTs. For each TFTs, we varied deposition time of inkjet-printed SWCNT to control density of SWCNT film. Transfer characteristics of each device are illustrated in Figure 4.3 (a), (b). This inkjet-printed SWCNT TFTs devices have 0.6 cm^2/Vs of field effect mobility, -0.5 V of threshold voltage and 10^4 of I_{on}/I_{off} ratio for drive TFTs and 0.02 cm^2/Vs of field effect mobility, -1.6 V of threshold voltage and 10^4 of I_{on}/I_{off} ratio for drive TFTs. This results are similar to previous inkjet-printed SWCNT TFT on SiO_2 substrate but shows lower mobility than pervious results. Fabricated inkjet-printed SWCNT TFTs for drive TFT showed depletion-mode characteristics. It is essential to tune the threshold voltage (V_{TH}) of SWCNT TFTs for full-swing inverter. To tune V_{TH} in inkjet-printed SWCNT TFTs, we used chemical encapsulation with NH_4OH. Figure 4.4 shows the effect of NH_4OH. In the graph, transfer curve is shifted to negative direction after NH_4OH treatment. Inkjet-printed SWCNT device after NH_4OH treatment showed 0.25 cm^2/Vs of field effect mobility, -2.7 V of threshold voltage and 10^3 of I_{on}/I_{off} ratio for drive TFTs. This degradation of mobility after treatment is originated from the increased contact resistance. [14] From these results, we fabricated

SWCNT inverter by connecting two TFTs. Electrical performance of inverter is often measured using the voltage transfer curve (VTC), which is a plot of output vs. input voltage. From such a graph, device parameters including noise tolerance, gain, and operating logic levels can be obtained. Ideally, the VTC appears as an inverted step function but in real devices, a gradual transition region exists. The VTC indicates that for low input voltage, the circuit outputs high voltage; for high input, the output tapers off towards the low level. The slope of this transition region is a measure of quality and steep slopes yield precise switching. The electrical properties of fabricated inkjet-printed SWCNT inverter is illustrated in Figure 4.5 (a), (b). To measure the electrical performance, we applied input voltage from 5 V to 0 V to confirm transition region with DC bias V_{DD} of 5V. As shown VTC characteristic, the curves show the full-swing characteristic with the minimum output voltage falling to about 0 V when the input voltage is equal to V_{DD}. Also fabricated inverter showed high gain with maximum value of 5 as shown in Figure 4.5 (b). This value is larger than previous SWCNT inverter, but inverting transition of output voltage didn't take place around $V_{DD}/2$ at given V_{DD} values. This is originated V_{TH} of SWCNT TFTs and can be improve by controlling the time of dipping in NH_4OH solution and additional encapsulation. Also to improve the gain of inverter, it is good way to use gate dielectric with high capacitance such as AlO_x.

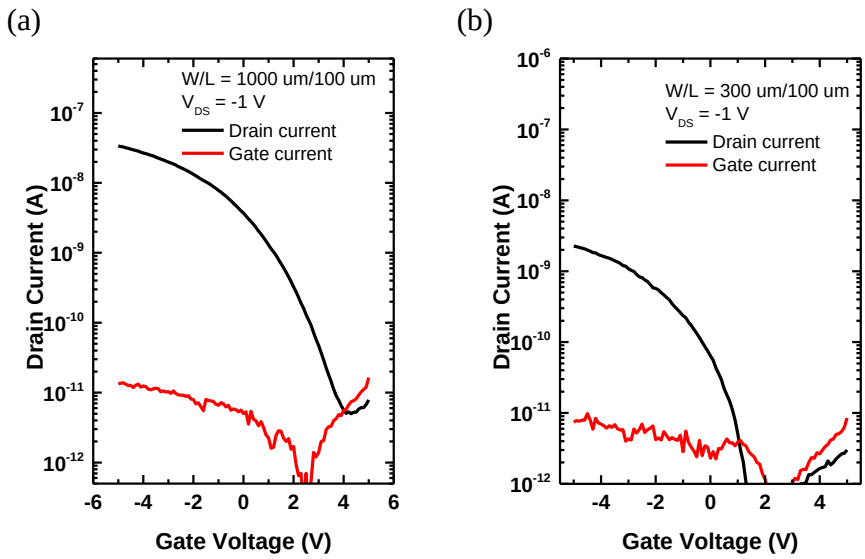


Figure 4.3 Transfer characteristics of (a) driver transistor and (b) load transistor

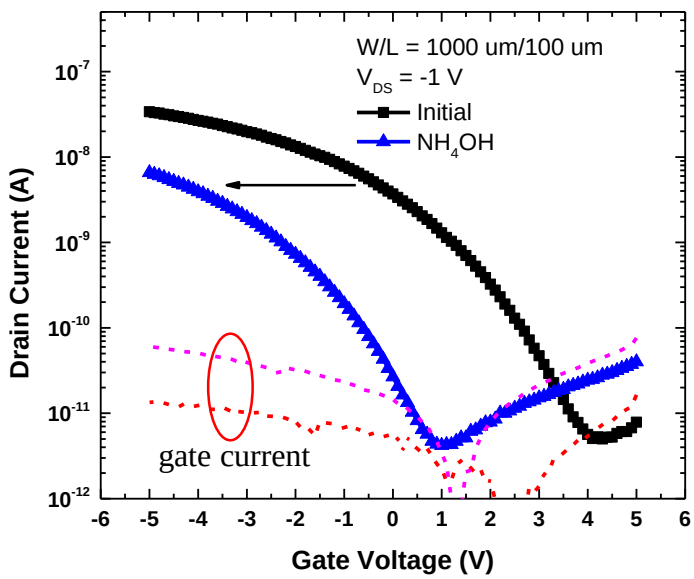
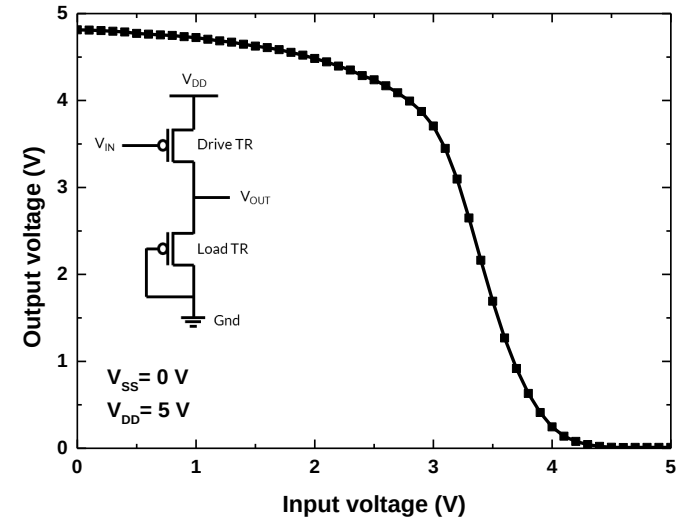


Figure 4.4 Transfer characteristics of inkjet printing SWCNT treated with NH_4OH on PVP dielectric for tuning threshold voltage

(a)



(b)

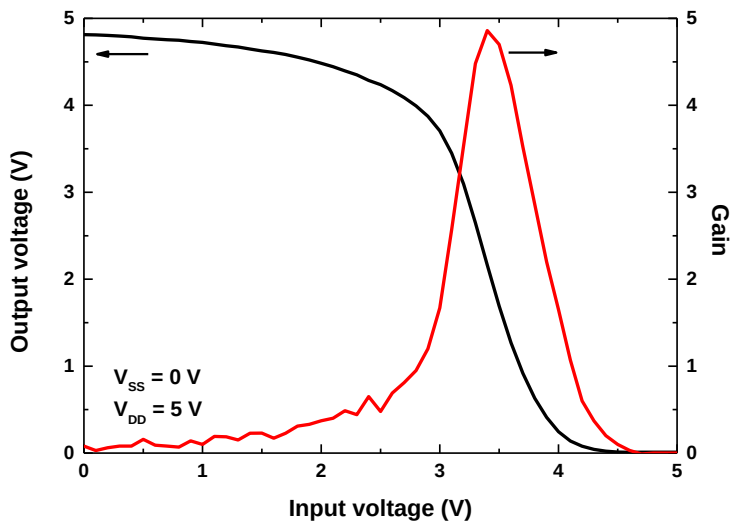


Figure 4.5 (a) The voltage transfer characteristics (b) gain of the fabricated of inkjet printing SWCNT inverter.

4.3 Inkjet-Printed SWCNT Static Random Access Memory

4.3.1 Fabrication Process

Inkjet-printed SWCNT SRAM connected with two inverter having full-swing characteristics was fabricated on bare glass substrate (Eagle X). First, the substrate was cleaned sequentially with acetone, IPA and DI water in the ultra-sonicator for 20 min, respectively. Before inkjet printing of gate electrode, UVO treatment was performed on the glass substrate. For bottom gate electrode and connection line for SRAM, a transparent silver ink JET-600C ink was printed on glass substrate. After the gate electrode was printed, the substrate was annealed at 150 ℃ for 30 min on hotplate under atmospheric environment. For dielectric, PVP was deposited on the fabricated silver gate electrode by spin coating method as above experiment. Soft-baking was performed on the hot plate at 120 ℃ for 20 min in air to evaporate the solvent of PVP. Then, the films were annealed at 200 ℃ for 30 min in air under atmospheric condition to obtain the cross-linked gate dielectric layer. To deposit the SWCNT semiconductor by inkjet printing method, surface was treated using PLL solution on UVO treated PVP surface. To optimize the surface energy with PLL solution, UVO treatment was performed on the PVP dielectric for 10 min to lower the surface energy. For PLL treatment, the substrate was immersed in PLL solution for 10 min at ambient condition and rinsed with DI water to enhance subsequent SWCNT adhesion. For inkjet-printed SWCNT SRAM, we fabricated two inkjet-printed full-swing SWCNT inverter having two SWCNT TFTs for drive TFTs and load TFTs as illustrated Figure 4.7 (a). For each TFTs, we varied deposition time of inkjet-printed SWCNT to control density

of SWCNT film. During inkjet printing of SWCNT solution, the substrate was kept at 40 ℃. We used only 1 nozzle and the drop spacing was adjusted to 25 μm. For drive SWCNT TFTs and load SWCNT TFTs, substrate was dried in air for 30 min and 20 min each after printing. It was then followed by a thorough rinse with DI water and dried with a nitrogen gun, resulting in uniform assembly of SWCNT random network over the printed surface of the substrate. To deposit source and drain electrodes, we used precursor type silver ink (JET-600C). A channel width is 1000 μm for drive TFT and 300 μm for load TFT. A channel length 150 μm was used for both devices. Also electrode line for SRAM was deposited by inkjet printing method. After the inkjet printing of silver source and drain, substrate was sintered in a convection oven at 150 ℃ for 30 min to evaporate the solvent of silver ink. Finally, we immersed each SWCNT TFTs in 0.1 M of ammonium hydroxide (NH_4OH) (purchased from Sigma Aldrich Corp.) solution in water to tune the threshold voltage of SWCNT TFTs, by dipping method, then followed by a thorough rinse with DI water and dried with a nitrogen gun to remove residue solution and particles.

Electrical characteristics of devices were measured by HP-4155C semiconductor parameter analyzer and HP-4284A LCR meter in the ambient condition. Also, to investigate a thickness of dielectric films and morphology of pentacene layer, atomic force microscopy (AFM, XE-100) was used.

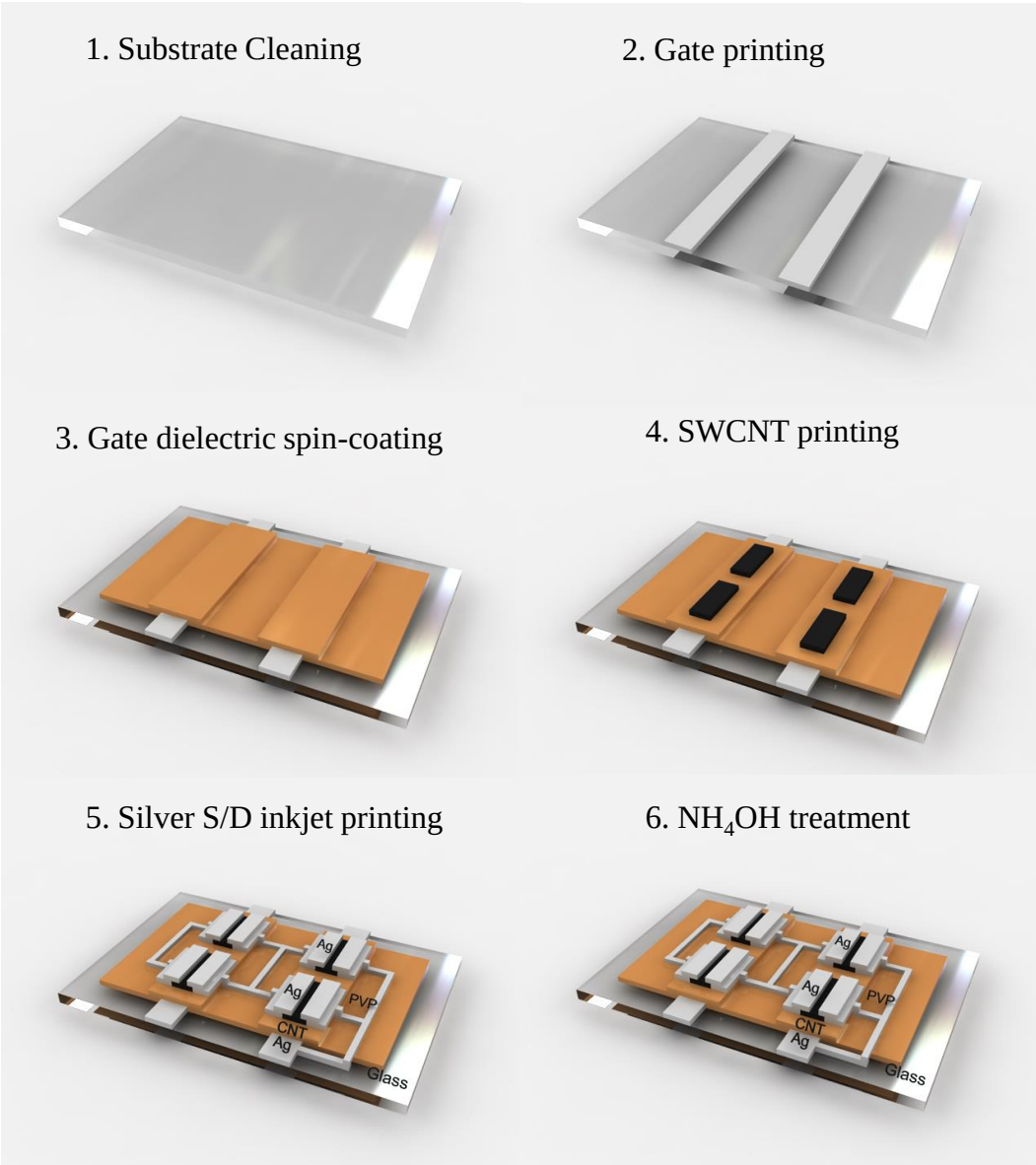
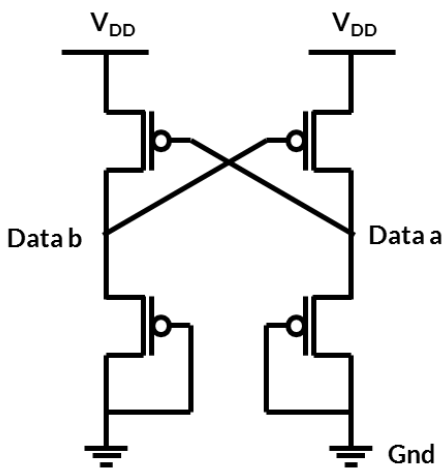


Figure 4.6 Fabrication process of inkjet-printed SWCNT SRAM cell

(a)



(b)

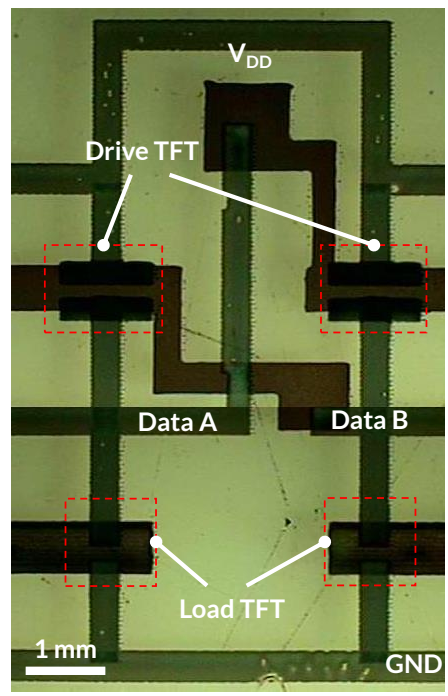


Figure 4.7 (a) Circuit diagram and (b) optical image of inkjet-printed SWCNT SRAM cell

4.3.2 Results

Commercial silicon-based SRAM usually employs a complementary (CMOS) design, because complementary circuits have larger noise margins and lower power consumption than unipolar (PMOS) circuits. However, in the case of SWCNT SRAM, complementary designs have a number of problems associated with the low field-effect mobility and poor air stability of SWCNT n-channel TFTs, which is the reason why we chose to implement a PMOS, rather than a complementary, SRAM. Figure 4.7 (a), (b) shows the schematic diagram and optical image of fabricated inkjet-printed SWCNT RAM with the full-swing SWCNT inverter which is composed of driver transistor and load transistor. Each inverter has the top contact structure on glass substrate using inkjet printing method. Inkjet-printed Ag was used as gate electrode, and the spin-coated PVP was used as gate dielectric on glass substrate. For inkjet-printed SRAM, we fabricated two full-swing SWCNT inverter under same experiment condition. As mentioned above section, full-swing SWCNT inverter consist of two SWCNT TFTs for drive TFTs and load TFTs. For each TFTs, we varied deposition time of inkjet-printed SWCNT to control density of SWCNT film. Because fabricated inkjet-printed SWCNT TFTs showed depletion-mode characteristics, it is essential to tune the threshold voltage (V_{TH}) of SWCNT TFTs for full-swing inverter. To tune V_{TH} in inkjet-printed SWCNT TFTs, we used chemical encapsulation with NH_4OH. After chemical treatment, fabricated each SWCNT inverter showed voltage transfer characteristics illustrated in Figure 4.8 (a), (b). To measure the electrical performance, we applied input voltage from 5 V to 0 V to confirm transition region with DC bias V_{DD} of 5V.

Each inverter showed near full-swing characteristics with the minimum output voltage falling to about 0 V when the input voltage is equal to V_{DD}. Also fabricated each inverter showed high gain with maximum value of 4 and 3 as shown in Figure 4.8 (b). From these results, we fabricated SWCNT SRAM cell by connecting two inverters' input and output as shown Figure 4.7 (b). When the output of each inverter is connected to the input of the other inverter, two different stable states are possible in (Data a, Data b): the outputs can take on the values (1, 0) or (0, 1). A logical 1 is written into memory by forcing the circuit into the (0, 1) state and a logical 0 is written by forcing the circuit into the (1, 0) state. To test the working of the memory cell, we attached a voltage source to one input and wrote a logical 1 to V_{out} by driving V_{in} to 0 V. The switch at V_{in} was then opened after 3 sec and the memory cell maintained a logical 1 at the output until the switch was closed after 30 s. Then we wrote a logical 0 into V_{out} by driving V_{in} to 5 V. When the switch was opened again, the memory cell maintained a logical 0 at the output. As illustrated Figure 4.9 (b), these data demonstrate the stable memory function of SWCNT SRAM cell. The SRAM cell showed fairly stable retention ability in logical 1 data when the input data is 0, but showed high output voltage (~2.5 V) in logical 0 data when the input data is 1. These results is originated from a small static noise margin of ~0.4 as shown Figure 4.9 (a). As shown Figure 4.8, two inverter showed not-fully inverting characteristics which output voltage is ~ 0.8 V when the input voltage is 5 V. Also inverting transition of output voltage didn't take place around $V_{DD}/2$ at given V_{DD} values. From these reasons, SWCNT SRAM device showed low static noise margin. This will be improved by controlling the time of dipping in NH_4OH solution and additional encapsulation.

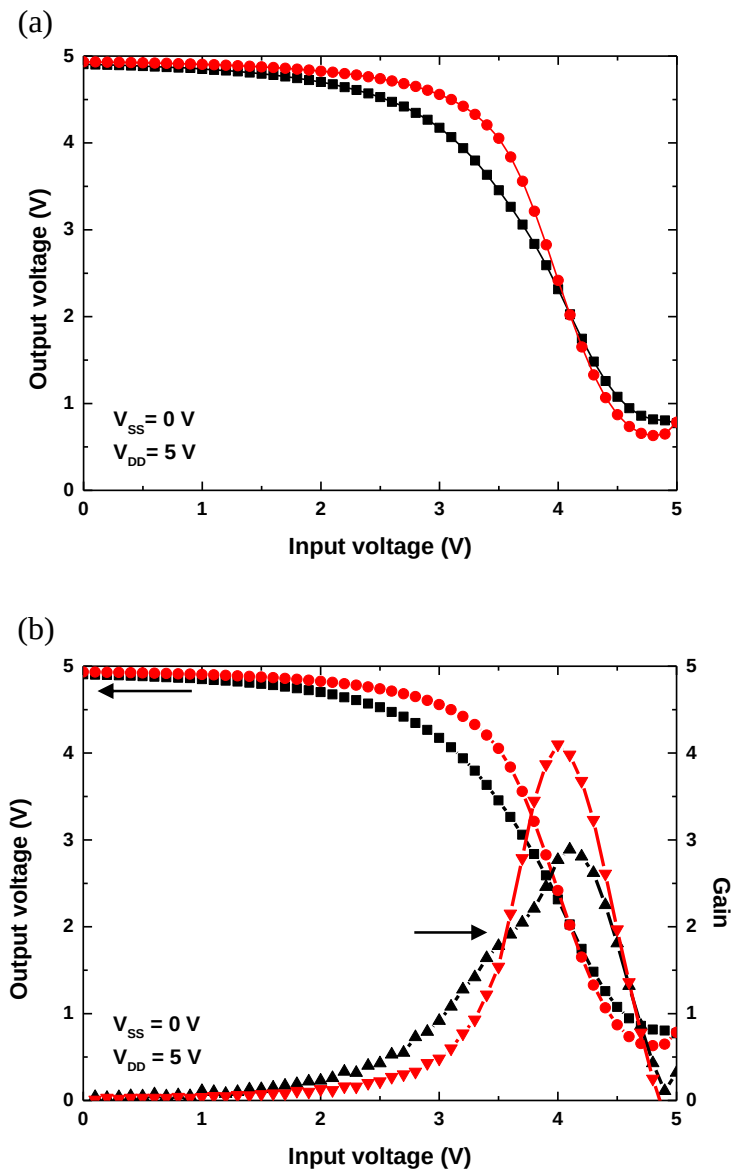


Figure 4.8 (a) Static transfer characteristics and (b) Gain characteristics of the two inverters of an SRAM cell

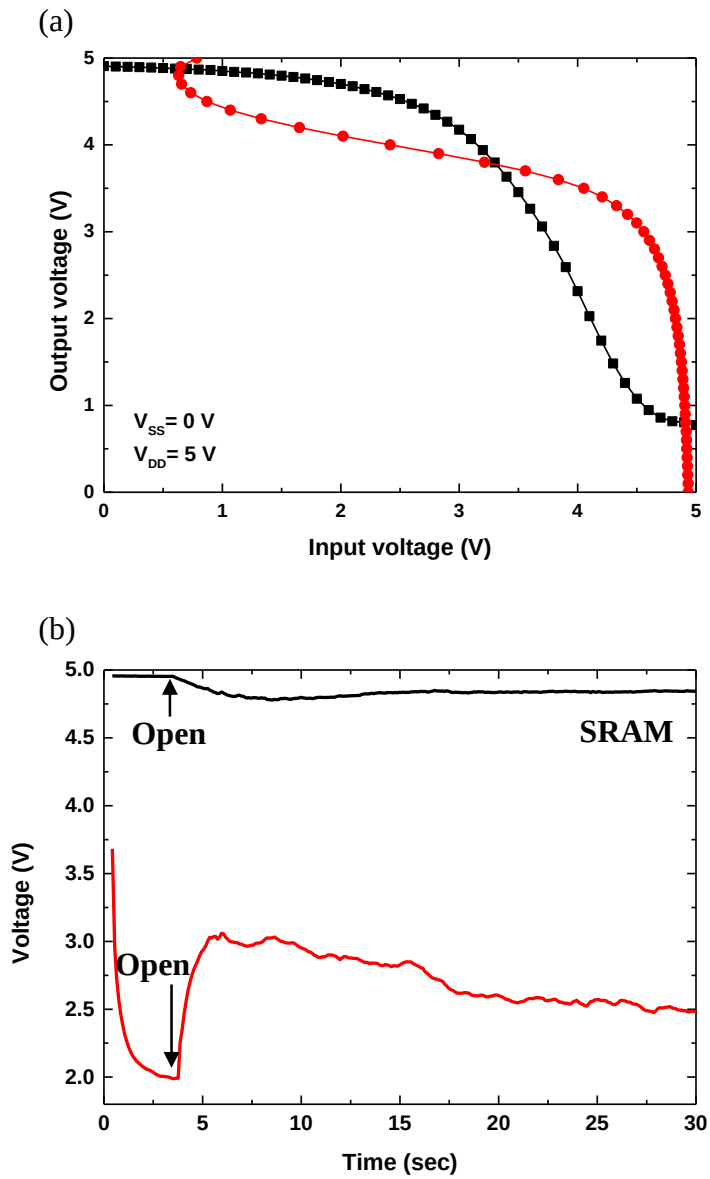


Figure 4.9 (a) Butterfly curve of an SRAM cell (b) Output voltage of SRAM cell. The output logical stays at 0 or 1 after the switch to the input has been opened.

4.4 Conclusion

Recently, the utility of the SWCNT transistors is extended to the logic circuitry for the low-end smart card or identification tag as well as to the pixel-driving transistor or display driving circuit. Also complex circuits have been demonstrated using SWCNT transistors, such as shift register, radio-frequency identification circuitry, and memory device. So, in this chapter, we reported inkjet-printed full-swing SWCNT transistors and SWCNT SRAM cell as applications of inkjet-printed SWCNT TFTs. By using optimized inkjet printing method, we deposited the semiconducting SWCNT and silver source and drain electrodes on glass substrate. For inkjet-printed full-swing SWCNT inverter, we deposited the semiconducting SWCNT solution on PVP dielectric and silver source/drain electrodes by inkjet printing method. Because solution-processed SWCNT TFTs usually shows depletion-mode characteristics, we controlled threshold-voltage of SWCNT TFTs to balance the switching characteristics of the inverters by employing chemical encapsulation with a NH_4OH. The fabricated SWCNT inverter device showed voltage transfer curve having the high performance. Also from these results, we fabricated and analyzed inkjet-printed SWCNT SRAM cell by connecting two inverters' input and output. The SWCNT RAM cell demonstrated the data switching characteristics and fairly stable retention ability. There are some challenges to improve including device uniformity, not-fully inverting characteristics, and inverting transition voltage. But these will be improved by optimization of inkjet-printing condition, controlling the time of dipping in NH_4OH solution and additional encapsulation.

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Chapter 5

Conclusion

In this thesis, organic nonvolatile memory transistor and single-wall carbon nanotube (SWCNT) transistor were fabricated. The organic nonvolatile memory transistors were fabricated using partially grown graphene as charge floating gate. In SWCNT transistor, we fabricate SWCNT transistor with inkjet printing method without any patterning process. Furthermore, we demonstrated SWCNT inverter using inkjet printing method.

For organic nonvolatile memory transistor, partially grown graphene was synthesized for charge floating gate by controlling the time of the graphene growth during a CVD process. The solution-processed PS dielectric layer was used as a charge-tunneling dielectric layer and pentacene was used as an active layer. The fabricated memory device showed large memory windows (～40 V) and a good data

retention ability. Also fabricated device exhibited a clear charge-trapping and de-trapping behavior in the partially grown graphene within a short period of time (100 ms). The data retention properties of our devices showed an on/off ratio of about 5×10^4 even after 10^5 s, which leads to the estimated charge storage time of more than a year. Furthermore, the memory device were reliable after more than one-hundred repeated programming/erasing cycle tests. Although the memory performance needs to be further improved, the mechanical flexibility and optical transparency of the organic and the partially grown graphene layers are expected to show great promise for use in transparent and flexible next generation memory applications.

For inkjet-printed SWCNT transistor, we deposited the semiconducting SWCNT and source and drain electrodes by using optimized inkjet printing method. The fabricated inkjet-printed SWCNT transistors showed high electrical performance and low gate leakage current without any patterning method without any additional patterning process. For SWCNT inverter, we deposited semiconducting SWCNT and Ag gate and source/drain electrodes by inkjet printing method on glass substrate with spin-coated PVP. The fabricated SWCNT inverter by inkjet printing method showed clear transfer characteristics. Furthermore, we fabricated inkjet-printed full-swing SWCNT inverter. For full-swing inverter, we used NH_4OH treatment to tune the threshold voltage of device. From this method, we could archive full-swing inverter characteristics with high gain. Finally, we fabricated and analyzed inkjet-printed SWCNT SRAM cell by connecting two inverters' input and output. The SWCNT

RAM cell demonstrated the data switching characteristics and fairly stable retention ability. Our fabrication method using inkjet printing was simple, fast, and cost effective. Furthermore, it was not required patterning process such as photolithography.

한글 초록

최근 전기 소자 분야에서 유연성을 갖는 소자의 연구와 대면적을 가지는 소자에 대한 관심이 많아짐에 따라 이러한 소자에 대한 많은 연구가 진행되고 있다. 이러한 배경에서 유연성을 가지고 대면적화에 적합한 반도체 재료에 대한 관심 또한 많아지고 있으며, 그 중 유기물 기반의 반도체 재료, 그리고 탄소 기반의 반도체 재료에 대한 연구가 활발하게 진행되고 있다. 이러한 유기물과 탄소 기반의 반도체 재료들은 기존에 사용되고 있던 실리콘 기반의 소자들을 대신하여 유기 발광 트랜지스터, 논리 회로, 등 많은 분야에 기초 재료가 될 것으로 기대되고 있다. 여러 응용분야 중에서, 특히 박막 트랜지스터는 가장 기본적인 스위칭 소자로써, 능동 행렬 액정표시장치와 능동 행렬 유기발광 다이오드의 백플레인으로 사용될 수 있고, 뿐만 아니라 여러 논리 회로, 정보 저장 장치에 응용될 수 있다. 이 중, 정보 저장 장치는 최근 정보의 양이 증가함으로써, 그 필요성과 중요성이 점점 증가하고 있다.

이러한 배경에서, 본 연구에서는 첫 번째로, 그래핀을 이용하여 유기 비휘발성 메모리소자를 제작하고 이 소자의 특성을 평가하는 실험을 진행하였다. 그래핀을 유기 비휘발성 메모리소자 내의 전하 저장 층으로

이용하기 위해, 그래핀 합성시에 합성 시간을 조절하여 부분 성장한 그래핀을 합성하였다. 이렇게 합성한 그래핀을 전사 방법을 통하여 원하는 기판에 올려 전하 저장 층으로 활용하였고, 유기물 반도체인 pentacene 층과 Ag 소스/드레인 전극을 열 증착 방법을 통해 증착하여, 유기 비휘발성 메모리 소자를 제작하였다. 이렇게 제작된 메모리 소자는 읽기와 쓰기가 가능한 메모리 특성을 보였고, 이를 통해 전하가 저장되고 빠져나가는 것을 확인할 수 있었다. 또한 이러한 메모리 소자는 시간이 지나도 그 정보를 구분할 수 있을 정도의 정보 저장 능력을 가짐을 확인할 수 있었고, 반복된 쓰기/지우기 시험 동안 큰 열화 없이 정상적으로 동작하는 것을 확인할 수 있었다. 보다 나은 특성을 가지는 메모리 소자를 위해서는 좀 더 최적화를 통해 개선해야 하지만, 이러한 실험을 통해 투명하고 유연성을 가지는 메모리 소자에 응용 가능성을 확인할 수 있었다.

두 번째로 용액 공정 기반의 탄소 나노 튜브를 반도체 층으로 사용하는 탄소 나노 튜브 박막 트랜지스터 소자를 제작하고 그 특성을 평가하였다. 반도체 특성을 가지는 탄소 나노 튜브를 기판 위에 형성하기 위해서 잉크젯 프린팅 공정을 이용하였다. 이를 위해 잉크젯 프린팅에 필요한 인쇄 조건과 인쇄 후 박막 형성에 필요한 시간들과 같은 조건들을 최적화 하였다. 반도체 층뿐만 아니라, Ag 소스/드레인 전극 또한 잉크젯 프린팅 공정으로 제작하였다. 이를 통해 추가적인

패터닝 공정이 없이 고성능의 전기적 특성을 갖고 탄소 나노 튜브 박막트랜지스터를 얻을 수 있었다. 또한 이러한 방법으로 제작한 박막트랜지스터 소자를 기반으로, 인버터 논리 회로를 제작하고 그 특성을 확인하였다. 뿐만 아니라, NH_4OH 용액을 이용하여 탄소 나노 튜브 박막 트랜지스터의 문턱전압을 조절하였고, 이를 통해 full-swing이 가능한 인버터를 제작하고 그 특성을 확인하였다. 그 결과 제작된 소자는 full-swing 특성을 가지고 최적화를 통해 인버터의 특성이 향상되는 것을 확인할 수 있었다. 또한 이렇게 제작한 full-swing 특성을 가지는 인버터를 이용하여 데이터를 저장할 수 있는 인쇄 공정을 이용한 탄소 나노 튜브 static random access memory (SRAM)을 제작하고 그 특성을 확인하였다.

주요어: 유기 비휘발성 메모리 트랜지스터, 그래핀, 박막트랜지스터, 유기 반도체, 탄소 나노 튜브, 정적 램, 용액 공정, 잉크젯 프린팅

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