Ph. D. DISSERTATION

HIGHLY STABLE FIELD-EFFECT TRANSISTORS BASED ON ORGANIC/NANO MATERIALS

유기물과 나노물질 기반의 고안정성
전계효과 트랜지스터

BY

JEONGKYUN ROH

AUGUST 2016

DEPARTMENT OF
ELECTRICAL AND COMPUTUER ENGINEERING
COLLEGE OF ENGINEERING
SEOUL NATIONAL UNIVERSITY

HIGHLY STABLE FIELD-EFFECT TRANSISTORS BASED ON ORGANIC/NANO MATERIALS

유기물과 나노물질 기반의 고안정성
전계효과 트랜지스터

지도교수 이 창 희

이 논문을 공학박사 학위논문으로 제출함

2016 년 8 월

서울대학교 대학원

전기컴퓨터 공학부

노 정 균

노정균의 공학박사 학위논문을 인준함

2016 년 8 월

위 원 장 : 이 종 호 (인)
부위원장 : 이 창 희 (인)
위 원 : 홍 용 택 (인)
위 원 : 정 병 준 (인)
위 원 : 진 성 훈 (인)

Abstract

HIGHLY STABLE FIELD-EFFECT TRANSISTORS BASED ON ORGANIC/NANO MATERIALS

JEONGKYUN ROH
DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING
COLLEGE OF ENGINEERING
SEOUL NATIONAL UNIVERSITY

Field-effect transistors (FETs) are the fundamental element of modern electronics. FETs are commonly used as switches, and one of the major applications is the backplane for displays. For decades, silicon has been chosen as a channel material of FETs to drive displays. As display technology has made a rapid progress, however, the demand for new FET technology has also arisen. High resolution, flexibility, transparency, low manufacturing cost, and broad applicability are the representative

features of next-generation displays. Considering those expected features of the future displays, a variety of nanomaterials have been introduced for FET applications. Among various types of nanomaterials, organic semiconductors and low-dimensional nanomaterials, in particular transition metal dichalcogenides (TMDCs), have gained considerable attention as the great candidates for the channel materials in next-generation FETs. There has been a huge progress on a drawback of each material such as low field-effect mobility of organic semiconductors and scalability issue of TMDCs. The last piece for practical uses of organic semiconductors and TMDCs, hence, would be the stability issues.

In this thesis, the stability issues of FETs based on organic semiconductors and nanomaterials, particularly TMDCs, were discussed in terms of environmental stability and operational stability.

Firstly, we demonstrated the improved air stability of n-type OFETs with an electrically active interfacial layer. With the interfacial layer composed of poly(9-vinylcarbazole) (PVK), the air stability of n-type OFETs based on N,N′-ditridecylperylene-3,4,9,10-tetracarboxylic diimide (PTCDI-C13) was remarkably improved. In addition, the high glass transition temperature of PVKs enabled thermal post annealing of the active layer, which resulted in a high electron mobility of 0.61 $cm^2/V \cdot s$. This high mobility was maintained at 90% and 59% after 4 days and 105 days stored in air, respectively. The PVK interfacial layer reduced the trapped charges in the OFETs for air exposure because of electron donating property of PVKs.

Next, we demonstrated the novel method to overcome the tradeoff between mobility and bias stability of the OFETs regarding a self-assembled monolayer (SAM)-treatment. Four types of silazane-based SAMs with different alkyl chain lengths in the range of 1 to 8 were used. The mobility was increased from 0.29

$cm^2/V \cdot s$ (without SAM-treatment) to 0.46 $cm^2/V \cdot s$, 0.61 $cm^2/V \cdot s$, 0.65 $cm^2/V \cdot s$, and 0.84 $cm^2/V \cdot s$ after the SAM-treatment with an alkyl chain length of 1, 3, 4, and 8, respectively. On the other hand, inverse proportional relationship was observed between the bias stability and the SAM alkyl chain length. To overcome this tradeoff, a novel method for interface engineering, two-step SAM-treatment, was introduced. By treating long SAM and short SAM in sequence, both the high mobility and good bias stability were achieved. With the two-step SAM-treatment, the OFET showed the improved bias stability as the short SAM-treated OFETs, maintaining the high mobility as the long SAM-treated OFETs.

Lastly, the stability issues of TMDC FETs are discussed. We demonstrated highly stable molybdenum disulfide (MoS_2) FETs with a negligible hysteresis gap via multiple annealing scheme, followed by systematic investigation for long term air stability with time of MoS_2 FETs with (or without) CYTOP passivation. The extracted life time of the device with CYTOP passivation in air was dramatically improved from 7 to 377 days, and even for the short-term bias stability, the experimental threshold voltage shift, outstandingly well matched with the stretched exponential function, indicates that the device without passivation has approximately 25% larger the barrier distribution ($\Delta E_B = k_B T_o$) than that of device with passivation. This work manifests that CYTOP encapsulation can be one of efficient methods to isolate external gas (O_2 and H_2O) effects on the electrical performance of FETs, especially with low dimensional active materials like MoS_2.

This thesis discusses the stability issues of FETs based on organic semiconductors and TMDCs. Electrically active interfacial layer was employed to improve the air stability of the OFETs, and two-step SAM-treatment was introduced to overcome the tradeoff between the bias stability and mobility of the OFETs regarding on the SAM-treatment. In addition, highly stable MoS_2 FETs were

fabricated via multiple annealing schemes followed by the systematic investigation of CYTOP passivation effect on the long term air stability and short term bias stability of the MoS_2 FETs. The proposed methods to solve the stability issues of the FETs based on organic semiconductor and TMDCs can be also used in other types of nanoelectronic devices.

Keywords: Field-Effect Transistors, Organic Semiconductors, Transition Metal Dichalcogenides, Interface engineering, Stability

Student Number: 2012-30935

Contents

List of Figures

List of Tables

Chapter 1

Introduction

1.1 Field-Effect Transistors (FETs)

Field-effect transistors (FETs) are the fundamental element of modern electronic devices. FETs are three terminal devices with a source, drain, and gate electrode (shown in Fig. 1.1 (a)), and they act as voltage-controlled current sources. FETs are commonly used as switches in electronic devices, and one of the major applications is the backplane for displays. Array of FETs in the backplane controls the light output of each pixels of the front plane according to the signals. Figure 1.1 (b) and Fig. 1.1 (c) show the FET driving circuit of liquid crystal display (LDC) and organic light-emitting diode (OLED) display, respectively.

For decades, silicon has been chosen as a channel material of FETs to drive displays. As display technology has made a rapid progress, however, the demand of

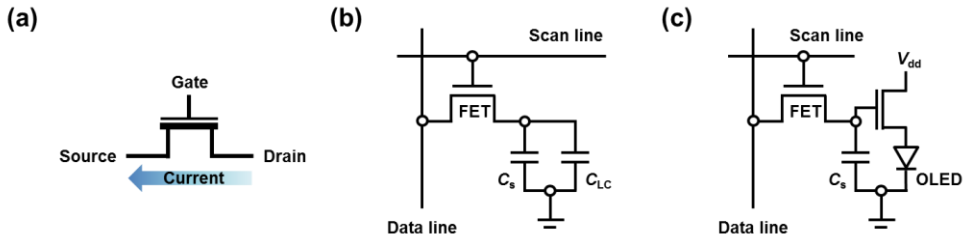

Figure 1.1 (a) Symbol of the FET. Pixel circuit for driving (b) LCD and (c) OLED.

new FET technology has also arisen. Figure 1.2 shows the progress of displays and corresponding transition of FETs. For the early stage of LCD, amorphous silicon (a-Si) FETs was used in the backplane. As the resolution of displays became higher, FETs were required to drive larger current flow. Thus, polycrystalline silicon (poly-Si)-based FETs were used instead of a-Si FETs because of higher mobility. As display market was moved from LCD to OLED display, backplane for driving OLED displays adopted a new type of semiconductor, metal oxide, other than silicon because of poor uniformity of poly-Si FETs.

As can be seen in the example of OLED display, there will be a growing demand of new materials for FETs to drive next-generation displays. Considering the expected features of future displays such as high resolution, flexibility, transparency, low manufacturing cost, and scalability, it can be expected that FETs based on nano materials will take the next spot. Various types of nanomaterials have been introduced as a channel material in FETs, and we will briefly review them in the following session.

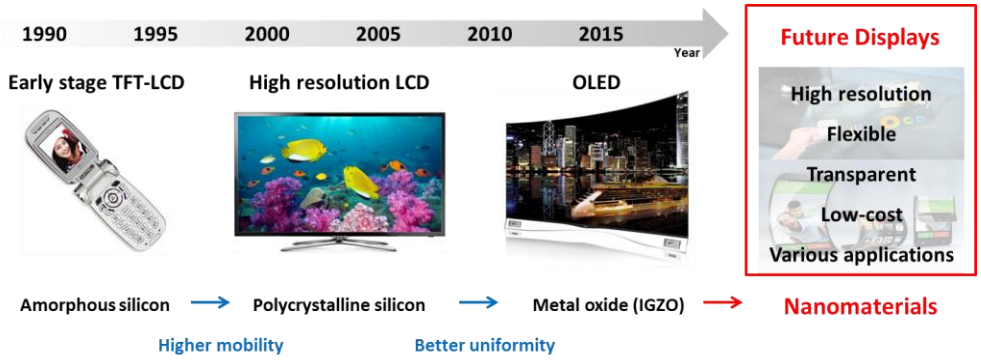

Figure 1.2 Progress of the display technology and corresponding transition of channel materials for FETs.

1.2 FETs based on Nanomaterials

There have been diverse efforts on adopting nanomaterials as a channel material in FETs. Figure 1.3 illustrates several candidates of nanomaterials for FET applications including amorphous metal oxide (a-metal oxide, e.g., IGZO), organic semiconductors (e.g., fullerene, pentacene, and poly(3-hexylthiophene-2,5-diyl)), two-dimensional layered materials (e.g., graphene, molybdenum disulfide, and black phosphorous), carbon nanotubes (e.g., single-walled carbon nanotubes (SWCNTs)), nanocrystal (colloidal quantum dots, e.g., cadmium selenide), and perovskite (lead iodide perovskite).

Figure 1.4 shows the comparison of semiconducting nanomaterials in terms of field-effect mobility and current on-to-off ratio. Both high current on-to-off ratio and high field-effect mobility are required to be adopted as a channel material of FETs in

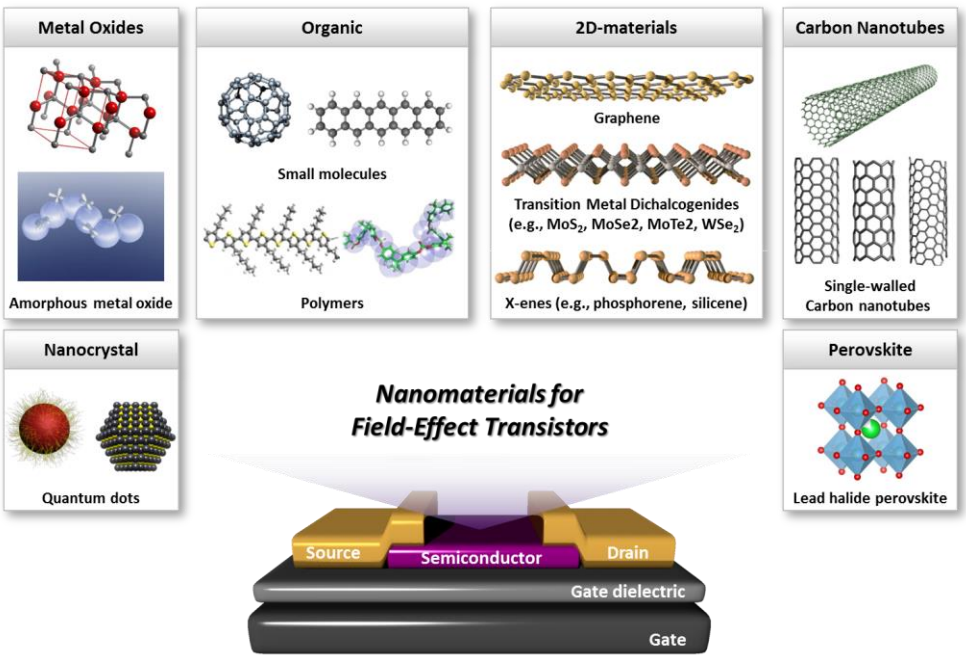

Figure 1.3 Various nanomaterials as a candidate for FET applications.

the display backplane. As shown in Fig. 1.4, graphene is not placed in the favorable position with poor current on-to-off ratio ($<10^3$), although it shows extremely high field-effect mobility ($>10^3$ $cm^2/V \cdot s$). Amorphous metal oxide is located in the proper place with reasonable field-effect mobility and current on-to-off ratio. As can be seen in Fig. 1.4, organic semiconductors and TMDCs also have a potential for FET applications. Although organic semiconductors exhibit relatively low field-effect mobility, it is worth investigating them because organic FETs are suitable for low-cost (even disposable) applications. In addition, the mobility of organic FETs has increased significantly, and exceeded 50 $cm^2/V \cdot s$. [1] TMDCs are placed in the most desired position with high field-effect mobility and current on-to-off ratio. In this thesis, we focused on those two nanomaterials, organic semiconductors and TMDCs, for next-generation FET applications.

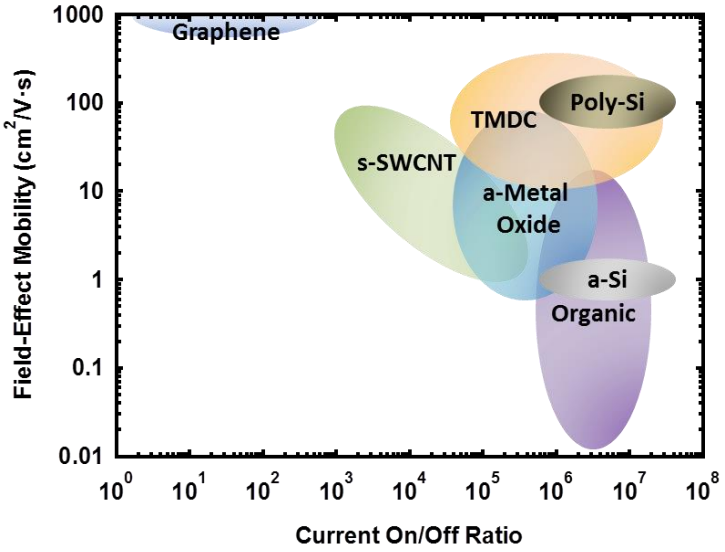

Figure 1.4 Comparison of the field-effect mobility and current on-to-off ratio of various semiconducting nanomaterials. [2-6]

1.2.1 Organic FETs

Organic FETs (OFETs) have intensively studied for the last few decades because of its suitability for large-area flexible and low cost electronics. [7-9] OFETs are considered to be a long term solution for the backplane of flexible displays and low-cost electronics, such as radio frequency identification (RFID) tags, and the application area is being enlarged to the various sensing devices for temperature, liquid, gas, pressure, light, and biochemical materials.[10-12]

Figure 1.5 shows some examples of representative organic semiconducting materials. Organic semiconductors can be classified by four categories according to the polarity (i.e., n-type or p-type) and molecular weight (i.e., small molecule or polymer). p-type semiconductors have been more frequently studied because of poor air stability of n-type semiconductors. However, remarkable improvement on n-type organic semiconductors has been reported in terms of air stability as well as electron field-effect mobility.

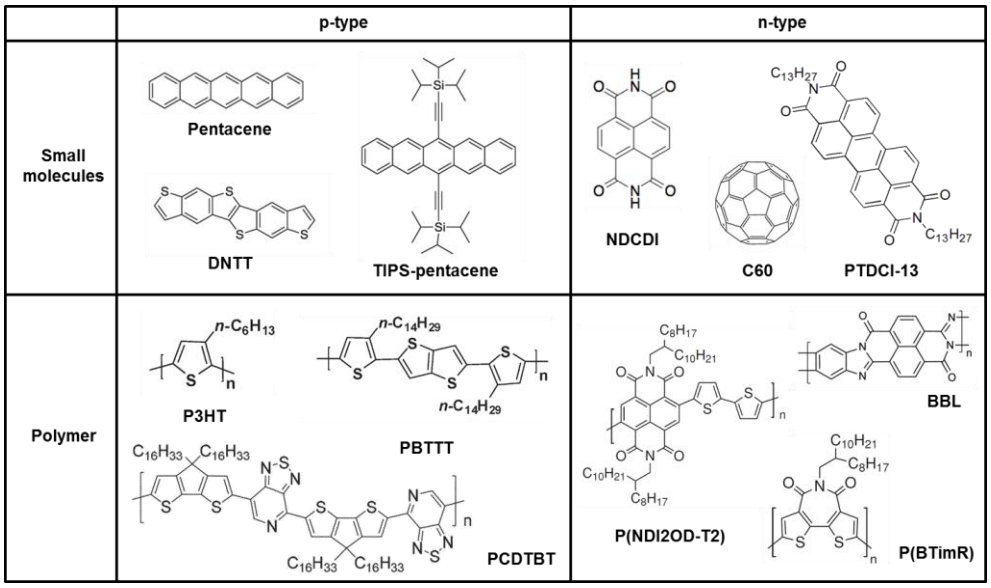

Figure 1.5 Examples of organic semiconductors for FET applications.

1.2.2 Transition Metal Dichalcogenides (TMDCs) FETs

Transition metal dichalcogenides (TMDCs) are two-dimensional layered materials with a chemical formula of MX_2 where M is the transition metal (e.g., Cr, Mo, W, V, Nb, Ta, Ti, Zr, and Hf) and X is the chalcogen (e.g., S, Se, and Te). Figure 1.6 shows the three-dimensional illustration of the structure of TMDCs, and Fig. 1.7 shows the possible combinations of TMDCs in the periodic table of elements. Each layer is weakly bonded with Van der Waals force while in-plane of TMDCs is strongly bonded. Thus, we can mechanically exfoliate some layers of TMDCs from the bulk crystal just like the graphene.

TMDCs have recently received tremendous attention and been actively researched for another opportunity in electronic applications beyond Si era because of their novel electrical, [13-15] optical, [16] and chemical properties. [17, 18] Particularly sizable direct (or indirect) bandgap property unlike graphene as well as an ultra-thin form of layers for TMDCs can be one of the most appealing aspects for the applications of next-generation field effect transistors (FETs), [13, 19, 20] photodetectors, [16, 21] chemical and gas sensors, [17, 22] and nonvolatile memory cells, [23, 24] thereby so many research activities based on TMDCs in this field have been dramatically reported up to now.

Among the TMDCs, molybdenum disulfide (MoS_2) and has been intensively studied because of its promising electrical and optical properties. High theoretical charge carrier mobility (410 $cm^2/V \cdot s$, at room temperature) and a sizable bandgap (1.9 eV, monolayer) are the appealing features of field-effect transistors (FETs). [3, 25, 26] High-performance monolayer and multilayer MoS_2 FETs have been reported, and various applications such as photodetectors, bio and gas sensors, nonvolatile

memory cells, and integrated circuits have been demonstrated by using MoS_2 FETs [24, 27-30].

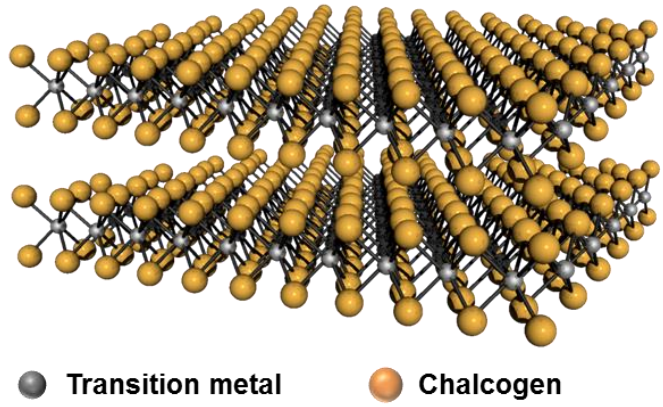

Figure 1.6 Three-dimensional illustration of structure of TMDCs. The spacing between each layer is 6.5 Å .

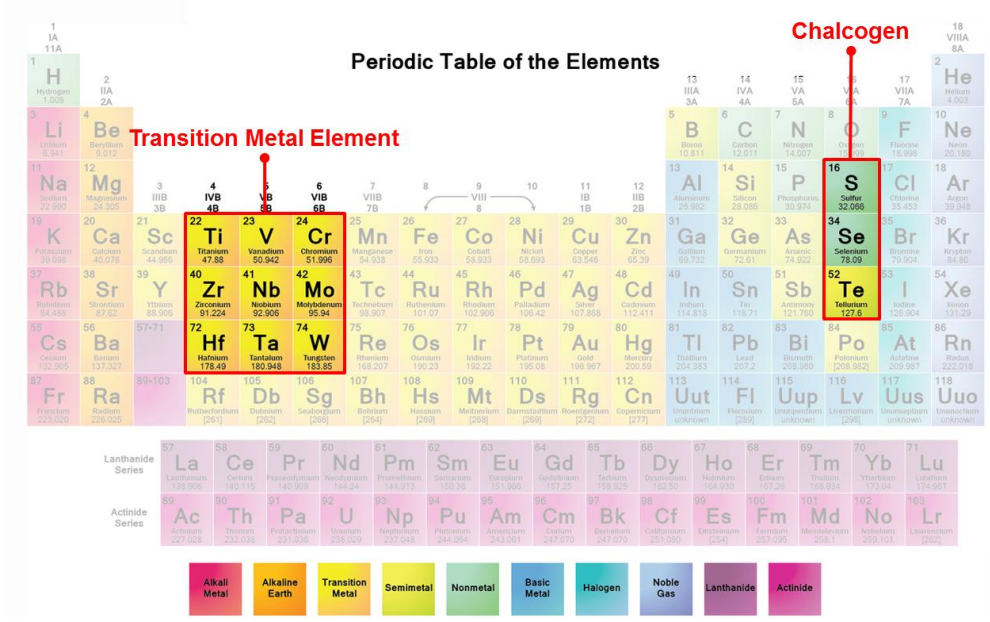

Figure 1.7 Periodic table of the elements. (Image source: 2013 Todd Helmenstine chemistry.about.com, sciencenotes.org)

1.3 Stability Issues of FETs

There are several stabilities required for FETs such as bias stability, air stability, thermal stability, photo stability, and mechanical stability. Achieving high stability is of significance not only practical uses of FETs in various applications but also studying intrinsic nature of nanomaterials.

1.3.1 Stability Issues of OFETs

Stability issues are still a hindrance for the mass commercialization of OFETs. Among the stability issues, air stability and bias stability have been most intensively studied because of its importance in display and integrated circuit applications.

The air stability is related to oxidation in air and charge trapping at the interface between organic semiconductor and gate insulator. The air stability issue has been considered more seriously for n-type OFETs. n-type organic semiconductors are normally oxidized in air easily because of lower redox potential than p-type organic semiconductors. In addition, interfacial charge trapping happens in air by deprotonation of SiOH on the SiO_2 gate insulator. [31]

The bias stability of OFETs is associated with the bias-stress-induced charge trapping inside the devices, and charge trapping occurs in the major locations of organic semiconductors, gate insulators and the interface between organic semiconductor and gate insulator. [32] In this regard, there have been many studies on improving the bias stability of OFETs via reducing charge trapping states in those locations.

1.3.2 Stability Issues of TMDC FETs

Similar to other types of low-dimensional materials, TMDCs have the intrinsic nature of instability because of large surface-to-volume ratio and the easy adsorption of gaseous molecules. Because of the instability of TMDCs, the exploration of the intrinsic characteristics of TMDCs has been limited. [33, 34] The instability of TMDCs is represented by a large hysteresis gap of TMDC-FETs; hysteresis gap is defined as the threshold voltage difference between the forward and backward sweeps. The large hysteresis of TMDCs FETs has often been observed in many systems regardless of the device structure (i.e., top-gated or bottom-gated) and the number of layers. [33, 35-37]

1.4 Outline of Thesis

This thesis consists of six chapters. In **Chapter 1,** the basic introductory of FETs and their future perspectives is reviewed. **Chapter 2** contains relevant theories on FETs including the working principle, fundamental electrical parameters, contact property and bias stability. In addition, the detailed experimental methods to fabricate OFETs and TMDC-FETs are delivered. After covering the overall background of this thesis, stability issues of FETs are discussed through Chapter 3 to Chapter 5. Chapter 3 and Chapter 4 deal with the stability issues of OFETs, and Chapter 5 discusses the stability issues of TMDC FETs.

In **Chapter 3**, improved air stability of OFETs with an electrically active interfacial layer is demonstrated. Normally, hydrophobic insulating polymers are employed as an interfacial layer in OFETs to improve air stability. We adopted an electrically active material, poly(9-vinylcarbazole) (PVK), as an interfacial layer in the n-type OFETs based on N,N′-ditridecylperylene-3,4,9,10-tetracarboxylic diimide (PTCDI-C13). PVK is well known material for hole transporting layer (HTL) in organic light-emitting diodes (OLEDs). Four types of PVKs with different molecular weight were employed as an interfacial layer in the n-type OFETs, and electrical performance and air stability were investigated and compared to the ones of the n-type OFETs with the conventional interfacial layer composed of cyclic olefin copolymer (COC). With a help of high glass transition temperature of PVKs, high electron mobility was achieved via thermal annealing process. Also, the n-type OFETs exhibited improved air stability because interfacial charge trapping was reduced because of electron donating property of HTL material, PVK.

In **Chapter 4**, improved bias stability of organic FETs with high field-effect mobility via two-step self-assembled monolayer (SAM)-treatment is discussed.

Previously, we investigated the relationship between the alkyl chain length of SAMs and the performance of OFETs in terms of mobility and bias stability. [38] From previous studies, we found out that the mobility of the OFETs with SAM-treatment was increased as the alkyl chain length of SAMs increased. On the other hand, inverse proportional relationship was observed between the bias stability and SAM alkyl chain length. To overcome the tradeoff relationship between the mobility and bias stability of OFETs concerning the SAM alkyl chain length, two-step SAM treatment is employed. By treating long SAM and short SAM in sequence, both the high mobility and good bias stability were achieved. With two-step SAM-treatment, the OFET showed high mobility as a long SAM-treated OFET and good bias stability as a short SAM-treated OFET.

Chapter 5 discusses the stability issues of TMDC-FETs, particularly passivation effect. We used molybdenum disulfide (MoS_2) as a representative TMDCs, and systematically investigated the effect of CYTOP passivation on the stability of MoS_2 FETs. Firstly, we implemented MoS_2 FETs with a negligible hysteresis gap via multiple annealing schemes to isolate the origins of device instability, coming from either internal device issues or external environmental issues. After confirming the low defect levels were included in the MoS_2 FET itself from the negligible hysteresis gap, the long term air stability and short term bias stability of MoS_2 FETs with (or without) CYTOP passivation were evaluated.

Finally, in **Chapter 6**, we summarize our experimental results and make concluding remarks.

Chapter 2

Theory and Experimental Methods

2.1 Principles of FETs

2.1.1 Operation Mechanism

Figure 2.1 shows the working principle of FETs. When the external bias is applied to the gate-to-source electrodes, charges are accumulated near the interface between the semiconductor and gate insulator. Those accumulated charges form a conductive channel, and charges flow through the channel (i.e., from the source electrode to the drain electrode) by the potential difference.

The current-voltage relationship of FETs can be expressed in two different forms according to the condition of the applied gate-to-source voltage (V_{GS}), drain-to-source voltage (V_{DS}), and threshold voltage (V_{TH}).

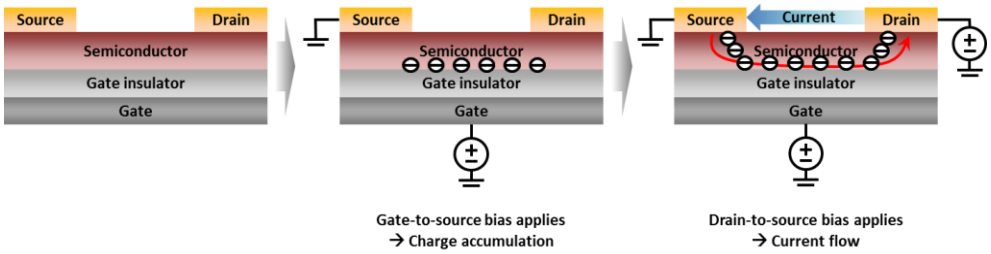

Figure 2.1 Simplified illustration for operating mechanism of FETs.

When $|V_{GS}-V_{TH}| > |V_{DS}|$, the FETs are operated in a linear regime and the drain-to-source current (I_{DS}) can be expressed as the following equation

$$I_{DS} = \frac{W}{L} C_{OX} \mu_{FET} \cdot \left(V_{GS} - V_{TH} - \frac{1}{2} V_{DS} \right) \cdot V_{DS} ,$$

(2.1)

where μ_{FET} is the field-effect mobility, W is the channel width, L is the channel length, and C_{ox} is the gate insulator capacitance per unit area. The transconductance (g_m) is defined as $g_m = \partial I_{DS}/\partial V_{GS}|V_{DS}$= const, and the field-effect mobility can obtained from the following relationship, $\mu_{FET} = g_m L \times (W C_{ox} V_{DS})^{-1}$.

When $|V_{GS}-V_{TH}| \leq |V_{DS}|$, the FETs are operated in a saturation regime and the drain-to-source current (I_{DS}) is described by the following equation

$$I_{DS} = \frac{1}{2} \cdot \frac{W}{L} C_{OX} \mu_{FET} \cdot \left(V_{GS} - V_{TH} \right)^2 .$$

(2.2)

The field-effect mobility and threshold voltage can be extracted from the slope of square root of drain-to-source current ($I_{DS}^{1/2}$) versus gate-to-source voltage (V_{GS}) plot.

Figure 2.2 (a) and 2.2 (b) show the typical transfer and output characteristics of n-type OFETs, respectively.

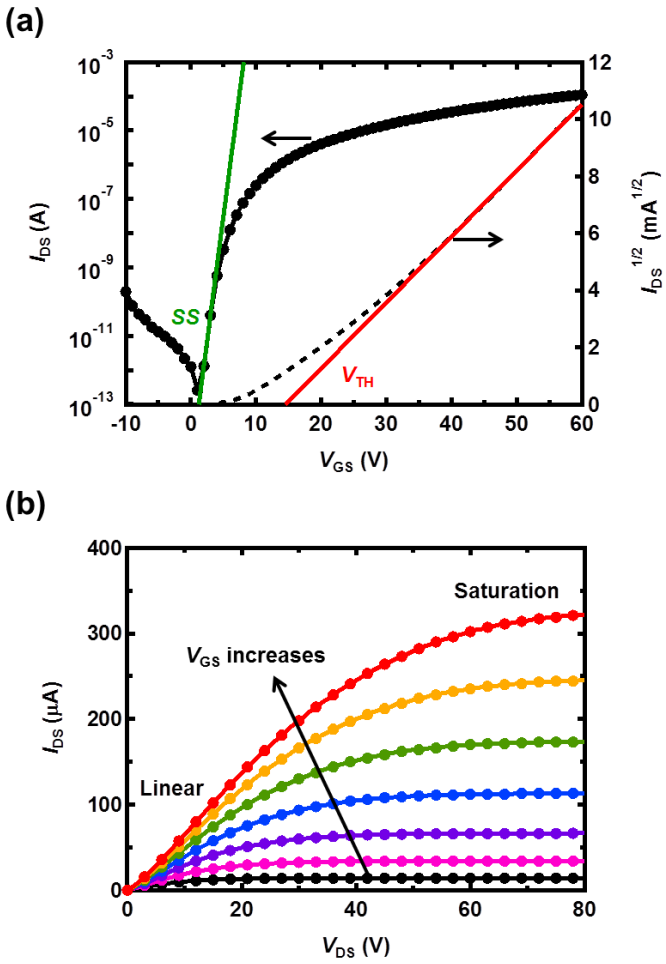

Figure 2.2. Examples of the typical (a) transfer characteristics (in a saturation regime) and (b) output characteristics of n-type OFETs.

2.1.2 Major Interfaces in FETs

In FETs, there are several interfaces which have a significant influence on the device performance. Figure 2.3 shows the major interfaces in FETs; metal-semiconductor interface, gate insulator-semiconductor interface, and semiconductor-atmosphere interface. Among those major interfaces, the gate insulator-semiconductor interface and the semiconductor-atmosphere interface are of importance for device stability. Interfacial charge trapping at the gate insulator-semiconductor interface is strongly related to both air and bias stability of FETs. In addition, semiconductor-atmosphere interface should be engineered property in order to prevent oxidation of semiconductor and adsorption of gaseous molecules, which leads to device instability.

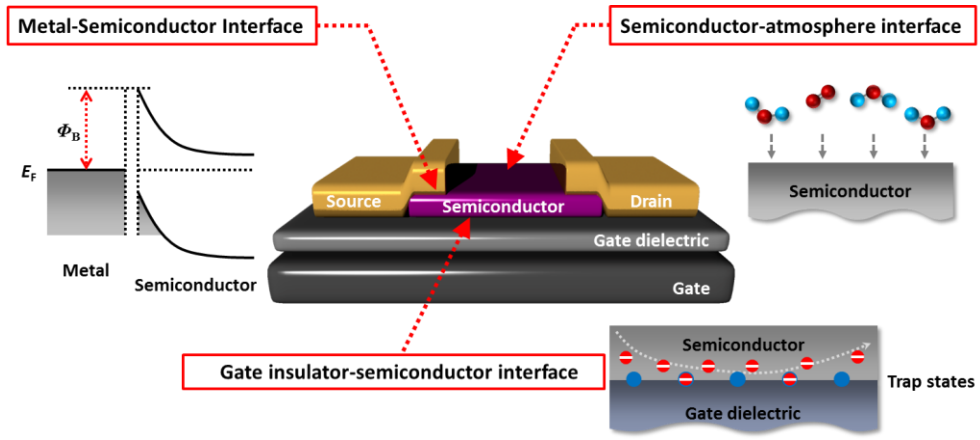

Figure 2.3 Major interfaces in FETs and their effects on device performance.

2.1.3 Contact Resistance Extraction

A variety of methods have been proposed to evaluate the contact resistance of FETs. Among those methods, transmission line method (TLM) and Y-function method (YFM) have been most widely employed. The TLM can obtain the contact resistance quite specifically while the YFM can estimate contact resistance roughly. However, the YFM only requires a single device, so it has been often employed to evaluate contact resistance of FETs when multiple devices with good uniformity cannot be fabricated easily. For applying TLM, a set of devices (more than 3) with different channel lengths are needed.

The TLM starts with a simple modeling of the FETs as a series connection of three resistances; contact resistance at a source electrode (R_{source}), channel resistance (R_{CH}) and contact resistance at a drain electrode (R_{drain}). Thus, the total resistance (R_{TOT}) can be expressed as a summation of the channel resistance (R_{CH}) and the two contact resistances ($R_C = R_{source} = R_{drain}$), and it can be described as a function of channel length by using the relationship $R_{CH} = R_S \cdot L/W$ where R_S is the sheet resistance of the semiconductor; $R_{TOT} = R_S \cdot L/W + 2R_C$. The total resistance can be calculated from the slope of the output curve in the early part where $V_{GS}-V_{TH} >> 1/2V_{DS}$, and the contact resistance can be extracted from the y-intercept of the plot; i.e., the channel resistance approaches to zero when the channel length is zero. The transfer length (L_T) is the effective length of the electrodes which actually participate in the charge injection, and it can be extracted from the x-axis intercept of the width-normalized total resistance versus the channel length plot. [39, 40] The example of obtaining contact resistances by using the TLM is described in Fig. 2.4.

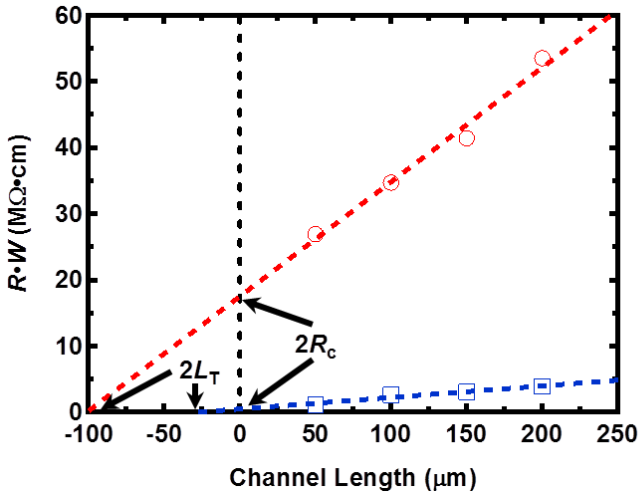

Figure 2.4 Example of evaluating contact resistance by using the TLM. The y-intercepts indicate contact resistances and x-intercepts represent transfer lengths.

The YFM was established by Ghibaudo for the evaluation of the MOSFET parameters including low-field mobility (μ_0) and contact resistance (R_c) [41]. The YFM has proven to be a powerful method of evaluating the contact property of FETs with a single device, and is also often employed in the MoS_2 FETs [42-44]. The Y-function is defined as

$$Y = \frac{I_{DS}}{\sqrt{g_m}} = \sqrt{\frac{W}{L} C_{ox} \mu_0 V_{DS}} \cdot (V_{GS} - V_{TH}) \cdot$$

(2.3)

From the Y versus gate-to-source voltage (V_{GS}) plot, and the low-field mobility (μ_0) can be extracted from the slope of the Y-function. Because low-field mobility is the maximally achievable mobility in the system, thus we can roughly estimate the contact resistance from the ratio of field-effect mobility to low-field mobility. For more quantitative evaluation, the mobility attenuation factor (θ) can be extracted from the plot of one over the square root of transconductance (g_m) with respect to the gate-to-source voltage (V_{GS}), according to the relationship

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = \frac{W}{L} C_{ox} \frac{\mu_0}{\{1 + \theta(V_{GS} - V_{TH})\}^2} \cdot V_{DS} \cdot$$

(2.4)

The contact resistance can be calculated with an approximation of $\theta \sim \mu_0 C_{ox} R_c W/L$ in a strong inversion regime where $V_{GS} - V_{TH} >> V_{DS}$.

2.1.4 Bias Stability

The threshold voltage shift caused by the gate bias stress can be described as the stretched exponential function [45]

$$\left|\Delta V_{TH}(t)\right| = \left|V_{GS} - V_{TH}(0)\right| \times [1 - \exp\{-(t/\tau)^{\beta}\}],$$

(2.5)

where V_{GS} is the applied gate bias stress, $V_{TH}(0)$ is the initial threshold voltage, τ is the relaxation time, and β is a dispersion parameter. The relaxation time (τ) is one of the representative parameter to describe the bias stability of FETs because it is understood as the average life time of mobile charge carriers before being trapped. The dispersion parameter (β) is related to the broadness of the trapping barrier distribution by the relationship $\Delta E_B = k_B T/\beta$, where ΔE_B is the distribution of the activation energy for charge trapping, k_B is the Boltzmann constant and T is substrate temperature.

The bias-stress-induced threshold voltage shift can be also described by the stretched hyperbola formula

$$\left|\Delta V_{TH}\right| = \left|V_{GS} - V_{TH}(0)\right| \times \left[1 - \left\{\exp\left(\frac{k_B T \cdot \ln(\omega t) - E_A}{k_B T_0}\right) + 1\right\}^{\frac{1}{1-\alpha}}\right]$$

(2.6)

where E_A is the activation energy for trap creation, $k_B T_0$ is the distribution of energy barriers, α is the stretching factor, k_B is the Boltzmann constant, and ω is the attempt-to-escape frequency. [32] For an optimal fit, as reported elsewhere, α and ω are normally assumed to be 1.5 and 10^5 Hz, respectively. [32, 46, 47] The stretched

hyperbola function gives useful information on the energetic structure for charge trapping. The activation energy (E_A) is the average energy barrier height of charge trapping, and the characteristic energy (k_BT_0) indicates the energy barrier distribution. Charge trapping occurs when the carriers overcome the energy barriers. Thus, a high energy barrier results in a low possibility of charge trapping. A large bias-stress-induced threshold voltage shift in FETs is attributed to the easier charge trapping which is resulted by the low energy barriers for trap creation. In addition to the energy barrier for charge trapping (E_A), the barrier distribution for trapping (k_BT_0) should be considered simultaneously. The narrow distribution of barriers is favorable because a broad distribution indicates the existence of low energy barriers that can be overcome easily; rapid device degradation, therefore, occurs in the early stages of operation.

2.2 Materials

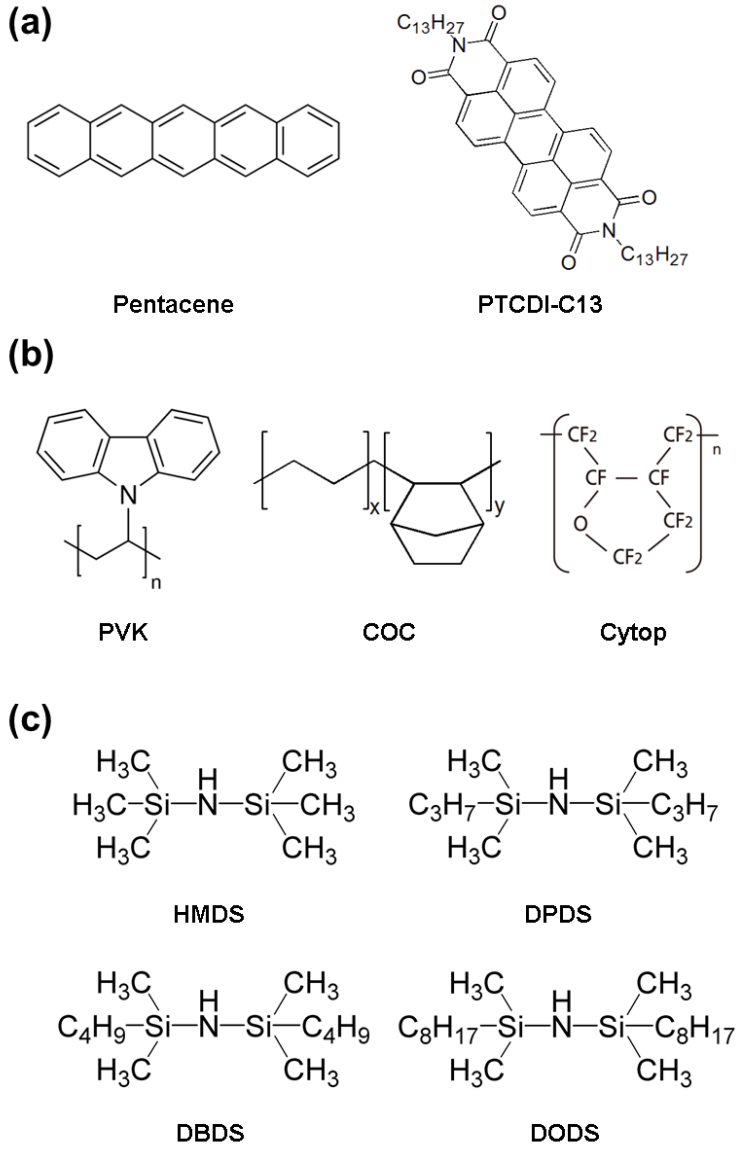

Figure 2.5 Chemical structures of (a) organic semiconductors, (b) insulating polymers for the interfacial layer and passivation layer, and (c) self-assembled monolayers.

2.2.1 Organic Semiconductors

Pentacene and N,N´-Ditridecylperylene-3,4,9,10-tetracarboxylic diimide (PTCDI-C13) were employed as p- and n-channel material, respectively, considering reasonable mobilities and commercial availability. Pentacene was purchased from Tokyo Chemical Industry (TCI), and PTCDI-C13 was obtained from Sigma Aldrich, and they were used as received without any further purification. Their chemical structures were shown in Fig. 2.5(a).

2.2.2 Polymers

For the interfacial layer in OFETs, the various types of Poly(9-vinylcarbazole) (PVK) were purchased from various companies (Polyscience, Aldrich, and Acros), and cyclic olefin copolymer (COC) was obtained from Polyscience. Fluorinated polymer, CYTOP (Asahi Glass), was employed as a passivation layer in MoS_2 FETs. The chemical structure of polymers were described in Fig. 2.5(b).

2.2.3 Self-Assembled Monolayers (SAMs)

Hexamethyldisilazane (HMDS) was obtained from Sigma Aldrich, and 1,3-di-n-propyl-1,1,3,3-tetramethyldisilazane (DPDS), 1,3-di-n-butyl-1,1,3,3-tetramethyl disilazane (DBDS), and 1,3-di-n-octyl-1,1,3,3-tetramethyldisilazane (DODS) were supplied by Gelest. Their chemical structures were shown in Fig. 2.5(c).

2.2.4 Preparation of MoS_2 Flakes

Bulk crystal of molybdenum disulfide (MoS_2) was purchased from SPI Supplies (429ML-AB). Multilayers of molybdenum disulfide (MoS_2) flakes were mechanically exfoliated from bulk MoS_2 crystals (SPI Supplies, 429ML-AB) by

using a thermal tape. After spreading MoS_2 flakes on the thermal tape, we used poly dimethylsioxane (PDMS) elastomer to transfer MoS_2 flakes from the tape to the Si/SiO_2 substrate.

2.3 Device Fabrication and Characterization

2.3.1 Device Fabrication and Characterization of OFETs with Polymeric Interfacial Layers

The molecular weight (M_w) of PVKs was measured by gel permeation chromatography except PVK of Sigma Aldrich with M_w 1100 kDa. Glass transition temperature (T_g) of each PVK was measured by differential scanning calorimetry measurements (heating rate 10℃/min). Herein, we refer PVKs as PVK (A), (B), (C) and (D) in the order of molecular weight; PVK (A): Sigma Aldrich, M_w 1100 kDa, PVK (B): Polyscience, M_w 225 kDa, PVK (C): Acros, M_w 109 kDa, and PVK (D): Aldrich, M_w 68 kDa. Glass transition temperature of each of the PVKs were in the range of 176℃ to 198℃, which is high enough for thermal annealing process for PTCDI-C13. The PVKs and COC (T_g 180℃) were spin-coated on the UV-treated SiO_2 substrates and the spin-coating speed was properly adjusted depending on the molecular weight of polymers to obtain a similar thickness. The capacitance per unit area of the PVKs and COC thin films made in the thickness range between 25 nm and 30 nm were measured to be from 25.3 nF/cm^2 to 27.7 nF/cm^2. The polymeric thin films were baked on a hotplate at 120℃ for 30 min.

On the polymeric interfacial layer, PTCDI-C13 was thermally evaporated at a rate of 0.3-0.5 Å/s while the substrate temperature was held at 30℃. After depositing 50 nm of PTCDI-C13 films, the substrates were transferred to a vacuum oven. The films were then annealed at 140℃ for 1 h, and cooled slowly down to 30℃. The samples were moved to a thermal evaporator, and 70 nm of Au was then deposited as the source and drain electrodes. The channel width and length of the OFETs were 2000 μm and 200 μm, respectively. The transfer characteristics of the OFETs were measured using a semiconductor parameter analyzer (Agilent 4155C)

in the saturation regime, where drain-to-source voltage (V_{DS}) was 30 V. To evaluate air stability of the n-type OFETs, the devices were stored in ambient condition with temperature of ~25℃ and humidity of 25% to 40%.

2.3.2 Device Fabrication and Characterization of OFETs with SAM-Treatment

Prior to the SAM-treatment, highly doped n-type silicon wafers with 100 nm thermally grown SiO_2 dielectric were cleaned by piranha solution. The substrates were placed into a crystallization dish with a small vial containing 15 mg of the SAMs. The crystallization dish was covered with aluminum foil and placed into a vacuum oven. The pressure of the vacuum oven was properly adjusted according to the boiling point of the SAMs. The temperature of the vacuum oven was maintained at 100℃ for 2 h, and cooled slowly down to room temperature. Subsequently, the substrates were cleaned by toluene and isopropyl alcohol (IPA) to remove the residual layers.

The pentacene OFETs were fabricated on surface modified SiO_2 substrates by thermal evaporation. A 50 nm pentacene film was evaporated thermally at a rate of 0.5 Å/s with a shadow mask. The substrate temperature was held at 60℃ during deposition. The Au source and drain electrodes with a thickness of 70 nm were deposited through a shadow mask at a rate of 1 Å/s. The devices were exposed to air while they were moved out of the vacuum chamber and transferred to a N_2 filled box. The electrical characteristics of the OFETs were measured in the N_2 filled box using a semiconductor parameter analyzer (Agilent 4155C). The transfer curve was observed in the saturation regime where the drain-to-source voltage (V_{DS}) was −30 V, and the channel length and width were 50 μm and 1000 μm, respectively. For the evaluation of bias stability, a gate bias stress of −30 V was applied for 2 h and the threshold voltage (V_{TH}) and drain-source current (I_{DS}) was measured. To reduce the effect of the contact resistance, gate bias stress test was performed with a device having a large channel length of 200 μm with a channel width of 2000 μm.

2.3.3 Device Fabrication and Characterization of MoS_2 FETs

The conventional photolithography process was employed to fabricate the MoS_2 FETs. Figure 2.6 shows a process scheme for the fabrication of the back-gated MoS_2 FETs. An n-type silicon wafer with heavy phosphorus doping (ρ~0.005 ohm·cm) was used as a starting substrate, followed by dry oxidation at 950℃. Multilayers of MoS_2 were mechanically exfoliated from bulk MoS_2 crystals by using poly dimethylsioxane (PDMS) elastomer, subsequently transferred onto Si substrates with 10 nm thick thermal-oxide. Then, each sample was annealed in a mixed gas (~Ar/H_2) for one hour at 400℃ for desorption of carbon residues or/and water molecule associated with exfoliation process. Photolithographic patterning and thermal evaporation of Au (~50 nm), followed by lift-off in acetone, created source and drain electrodes on multilayer MoS_2 with good Ohmic contact. [13, 48] After forming source and drain electrodes, additional annealing, with the same condition as the first annealing, was executed to remove PR residues or/and adsorbed water molecules, typically contaminated during photolithography and lift off process. Each sample contains at least larger than 10 devices with the same physical dimension of channel length (L_{ch}~ 10 um) on the same substrate. The back channel of MoS_2 FETs were passivated by a fluorinated polymer CYTOP (t_{CYTOP}~ 400 nm) with a typical spin coating process, immediately followed by annealing at 100℃ for 1 h in a vacuum oven. Finally, CYTOP film over the source and drain electrodes was etched away by using plasma etching reported elsewhere. The electrical characteristic for each device was measured by using a precision semiconductor parameter analyzer (Agilent, B1500A).

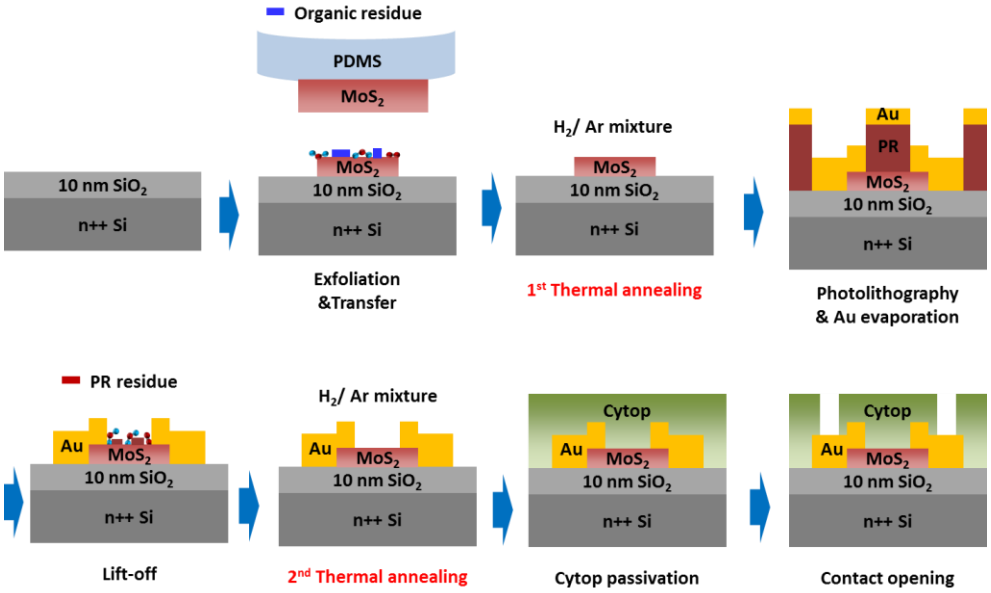

Figure 2.6 Process scheme for fabrication of the back-gated MoS_2 FETs.

2.4 Thin Film Analysis

2.4.1 Contact Angle Analysis

Surface energy can be analyzed by using the contact angles of two types of liquid, namely, deionized (DI) water and diiodomethane. From the contact angles of the two liquids, the surface energy can be calculated from this equation

$$\left(1+\cos\theta\right)\cdot\gamma_t = 2\cdot\left(\gamma_t^d\gamma_s^d\right)^{0.5} + 2\cdot\left(\gamma_t^p\gamma_s^p\right)^{0.5}, \quad \textbf{(2.7)}$$

where γ_t and γ_s are the surface energies of the tested liquid and solid surface, respectively, and θ is the contact angle. The surface energy consists of dispersive and polar components, which are denoted in this equation by the superscripts of *d* and *p*, respectively.

2.4.2 Atomic Force Microscopy

The surface morphology of organic semiconductors and the thickness of MoS_2 flakes were characterized by atomic force microscopy (AFM, Park system, XE-100) with a non-contact mode.

Chapter 3

Air Stability of Organic Field-Effect Transistors

To fabricate organic complementary metal oxide semiconductor (CMOS)-like circuits, both p-type and n-type organic semiconductors are required. The performance of the organic CMOS-like circuit is normally limited by n-type OFET because organic materials mostly exhibit superior p-type characteristics. Recently, considerable progress in new n-type materials has been made and their performance has been improved dramatically. [49-51] N,N′-ditridecylperylene-3`,4,9,10-tetracarboxylic diimide (PTCDI-C13) is a typical n-type material that has attracted attention since a high electron mobility of 2.1 $cm^2/V \cdot s$ after a thermal annealing process was reported. [52] On the other hand, high electron mobility was only

observed in a vacuum, and the device lost its transistor characteristics in ambient air. Previously, various studies have been performed to improve the air stability of PTCDI-C13 based n-OFET. Oh et al. employed n-doping to the PTCDI-C13 layer and compensated for the trapped electrons. [53] Chung et al. used an induced dipole by SAM to increase the redox potential of PTCDI-C13. [54] Another approach is to modify the organic-insulator interface by a hydrophobic polymer dielectric. Tanida et al. introduced 8-nm poly(methyl methacrylate) (PMMA) at the organic semiconductor-gate dielectric interface, and showed improved air stability through passivation of interfacial electron traps. [55] Among those methods, engineering the organic semiconductor-gate dielectric interface with a hydrophobic polymer is one of the most efficient ways because surface traps can be removed easily with a simple process. One of the disadvantages of this method, however, is that many types of polymer can be damaged during the thermal annealing process because of the low glass transition temperature (T_g). Air operable PTCDI-based OFETs with a polymer-modified dielectric normally exhibit low electron mobility because of the absence of a high temperature annealing process. [55, 56] To overcome this problem, Jang et al. introduced a high T_g copolymer, ethylene-norbornene cyclic olefin copolymer (COC), as an interfacial layer. [57, 58] They achieved high electron mobility by a thermal annealing process, and produced air operable PTCDI-C13 based OFETs.

This study employed poly(9-vinylcarbazole) (PVK), which is a well-known material for the hole transporting layer (HTL) in organic light emitting diodes (OLEDs). Nakayama et al. first reported the use of an electrically active material as an interfacial layer. Small molecule HTL materials were used as the interfacial layer

to enhance the air stability of n-OFET. [59] On the other hand, small molecules usually exhibit low glass transition temperature, which suggests that high crystallinity of the active layer cannot be obtained by thermal annealing. In terms of glass transition temperature, PVK is a better candidate for the interfacial layer than small molecule HTL materials. In addition, PVK has an advantage in the deposition method because it can be formed through a simple spin-coating. The performance of PVK as an interfacial layer was evaluated using COC as a target material. In addition, four types of PVKs with different molecular weight (M_w) were used in this work because molecular weight is one of the important factors for polymer's physical properties.

3.1 Electrical Performance of n-type OFETs

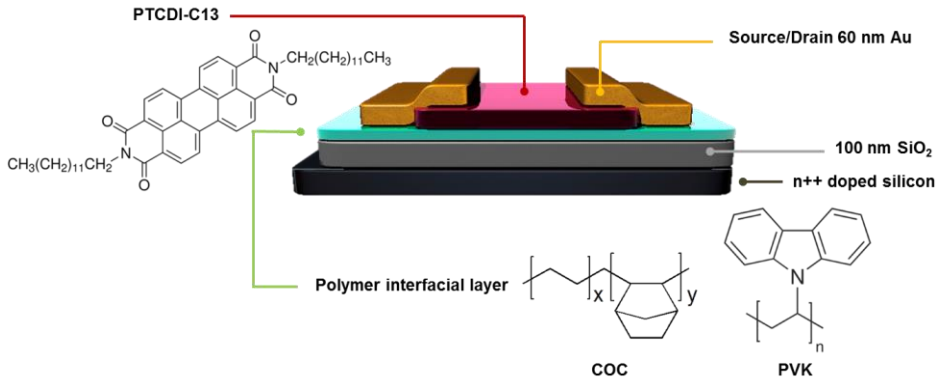

Figure 3.1 Device structure of the n-type OFETs based on PTCDI-13 with the interfacial layer, PVK or COC.

Figure 3.1 shows the device structure of the n-type OFETs based on PTDCI-13 with the interfacial layer. The transfer characteristics of the n-type OFETs were first obtained in a N_2 glove box, and then evaluated in ambient air to examine the short term air stability. As can be seen in Fig. 3.2(a) and 3.2(b), all the devices with the polymer interfacial layer show good performance in both N_2 atmosphere and air. The field-effect mobility and threshold voltage were extracted by using the Eq. 2.2. Table 3.1 lists the electrical characteristics of the n-type OFETs with the interfacial layer measured in N_2 atmosphere and ambient air. Among the devices, the device with the PVK (B) interfacial layer showed the highest electron field-effect mobility both in N_2 and air. With the PVK (B) interfacial layer, the field-effect mobility in N_2 atmosphere was 0.61 $cm^2/V \cdot s$ which is higher than the one of the device with the COC interfacial layer, 0.55 $cm^2/V \cdot s$.

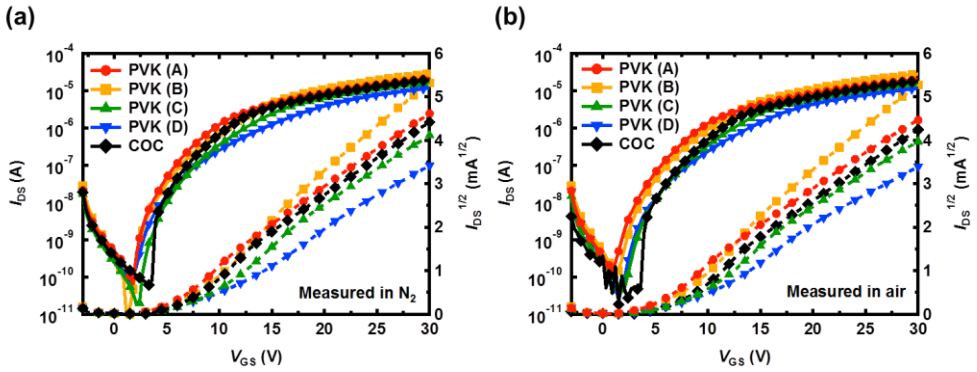

Figure 3.2 Transfer characteristics of the n-type OFETs based on PTCDI-C13 with the PVK or COC interfacial layer measured in (a) N_2 atmosphere and (b) ambient air.

Table 3.1 Summary of the device performance of the n-type OFET with the interfacial layer in N_2 atmosphere or ambient air.

Samples	Mobility in N_2 (in air) ($cm^2/V \cdot s$)	V_{TH} in N_2 (in air) (V)	Subthreshold slope (V/dec)	Density of interfacial trap states (cm^{-2})
PVK (A)	0.41 (0.39)	5.34 (5.06)	0.39	9.73×10^{11}
PVK (B)	0.61 (0.61)	7.41 (6.91)	0.39	9.34×10^{11}
PVK (C)	0.47 (0.47)	8.61 (8.52)	0.36	8.07×10^{11}
PVK (D)	0.30 (0.31)	9.55 (8.99)	0.85	2.04×10^{12}
COC	0.55 (0.52)	6.89 (7.31)	0.19	3.17×10^{11}

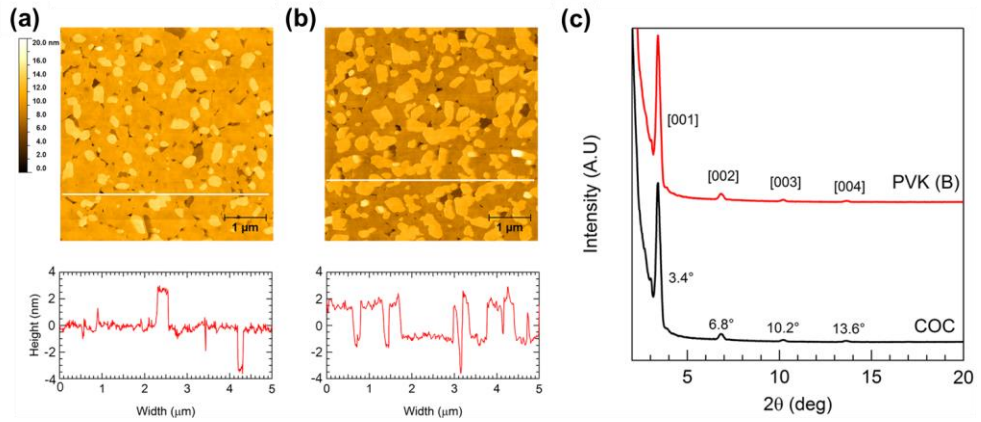

Figure 3.3 (a) AFM images and (b) XRD profiles of the PTCDI-C13 thin-film on PVK (B) and COC.

Fig. 3.3(a) and 3.3(b) show the atomic force microscopy (AFM) images of PTCDI-C13 thin film on PVK (B) and COC. Similar to the previous work by Jang et al. using COC, PTCDI-C13 formed well-ordered structure with large grain size on PVK (B). Terrace structured grains with size larger than 1 μm were observed from the AFM images. Figure 3.3 (c) shows X-ray diffraction (XRD) data of PTCDI-C13 thin film on PVK (B) and COC. Several orders of the layer diffraction were clearly observed. The diffraction peaks for [001] was observed at 2θ= 3.4° corresponding to a lattice spacing of 26 Å , which is similar to other works. [52, 58, 60]

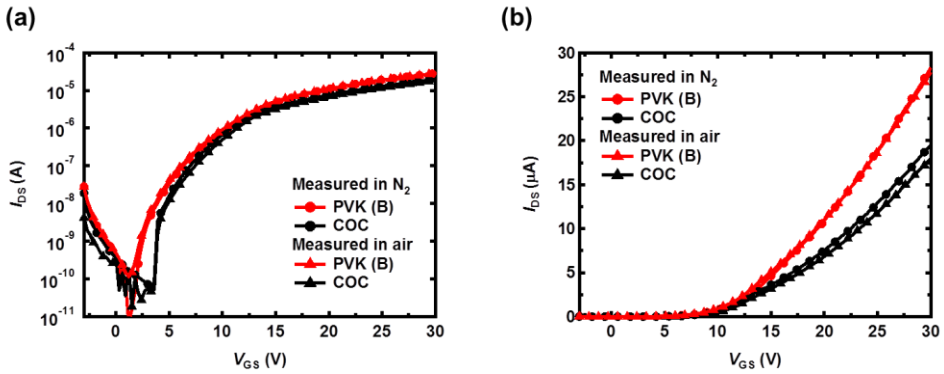

Figure 3.4 Comparison for the drain-to-source current of the n-type OFETs with PVK (B) and COC interfacial layer in (a) log and (b) linear scale.

As shown in Fig. 3.4(a) and 3.4(b), the device with PVK (B) showed similar characteristics in N_2 and air, whereas the device with COC exhibited slight degradation in air. The density of trap states at the organic semiconductor-gate insulator interface (N_{it}) can be calculated from the following equation [61]

$$N_{it} = \left(\frac{SS \cdot \log e}{kT/q} - 1 \right) \cdot \frac{C_i}{q} \qquad \textbf{(3.1)}$$

where SS is the subthreshold slope, k is the Boltzmann constant, q is the electronic charge, and C_i is the capacitance per unit area of the gate insulator. From the equation, the density of interfacial trap states values of the device with PVK (B) and COC were 9.34×10^{11} cm^{-2}, and 3.17×10^{11} cm^{-2}, respectively. Interestingly, the device with PVK (B) has three times as many trap states than the device with COC, even though the mobility degradation in air occurred more in the device with COC than PVK (B). Therefore, the mechanisms for enabling air operable OFET with the COC or PVK interfacial layer might be somewhat different. In the case of COC, air

operable n-type OFET was enabled by the reduction of surface traps. On the other hand, the reduction of surface traps might not be the main reason for the good air stability of the n-type OFETs with the PVK interfacial layer. This can be explained by the electron donating property of the HTL material. Nakayama et al. reported that surface traps can be occupied by electrons donated from the HTL materials. [59] In the same manner, electrons donated from the PVK in this work fill the trap states at the interface. As a result, the electrons in the conduction channel are less trapped, which results in less degradation in air. Figure 3.5 illustrates the comparison of the proposed mechanism for enabling air-operable OFETs with the COC and PVK interfacial layer.

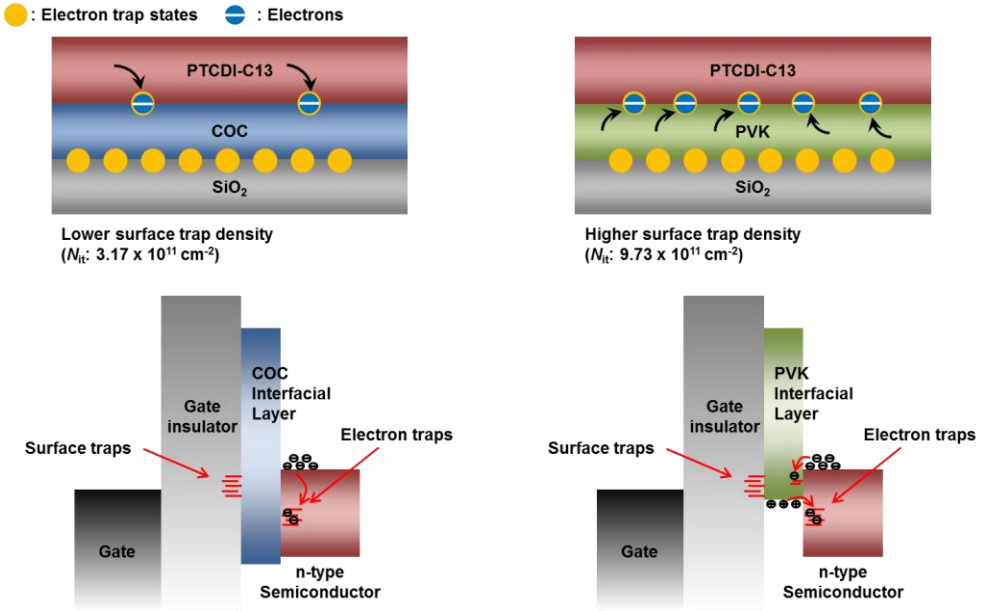

Figure 3.5 Schematic comparison of the proposed mechanism for enabling air operable OFETs with the COC and PVK interfacial layers.

3.2 Long Term Air Stability

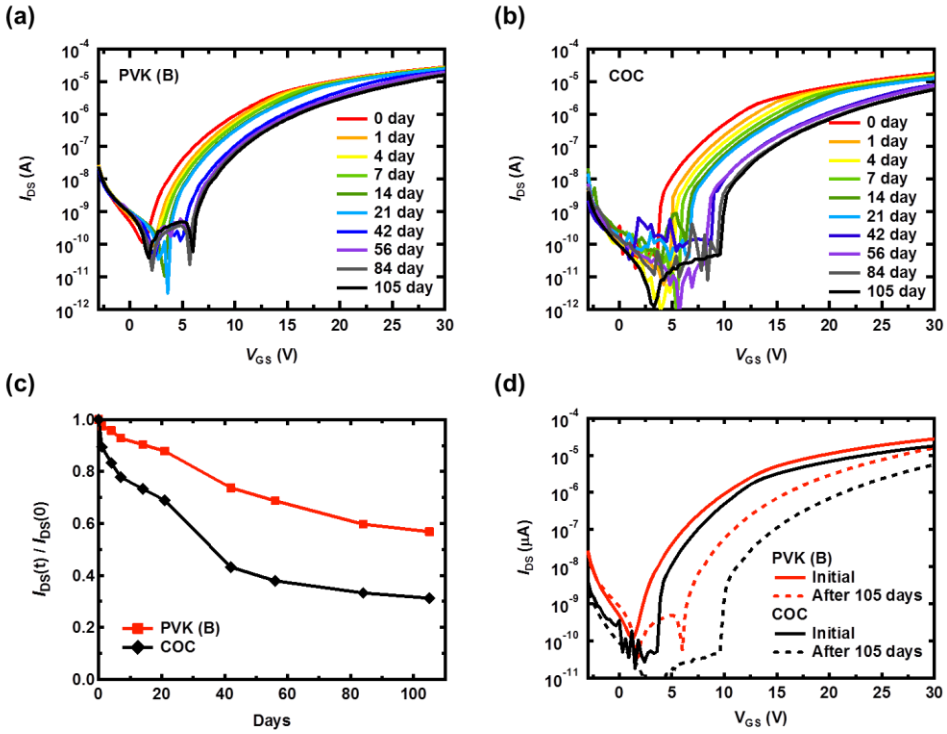

Figure 3.6 Air-stability measurements of OFETs with (a) PVK (B), and (b) COC

To examine the long term air stability of the n-type OFETs with the interfacial layers, the devices were stored under ambient conditions and the electrical characteristics were measured for 105 days. Figure 3.6(a) and 3.6(b) show the evolution of transfer characteristics of the device with the PVK (B) and COC interfacial layer for 105 days, respectively. During 105 days, the drain-to-source on-current and mobility degradation and the V_{TH} shift were observed, but they still showed acceptable performance. Figure 3.6 (c) shows the normalized drain-to-source on-current of the OFETs with the PVK (B) and COC interfacial layer. The drain-to-source on-current was degraded to 57% from the original level (27.8 μA to

15.8 μA) with the PVK (B) interfacial layer, and 31% from the original level (18.0 μA to 5.62 μA) with the COC interfacial layer. Figure 3.6 (d) compares the transfer characteristics of the OFETs with the PVK (B) and COC interfacial layer before and after stored in air for 105 days. Threshold voltage shift of the device with the PVK (B) and COC interfacial layer were 5.39 V and 8.75 V, respectively. The V_{TH} shift is related to the number of trapped charges, n_t, by the equation $n_t = \Delta V_{TH} C_{OX}/q$. The trapped charge density of each device with the PVK (B) and COC interfacial layer after 105 days were 8.84 x 10^{11} cm^{-2} and 1.29 x 10^{12} cm^{-2}, respectively.

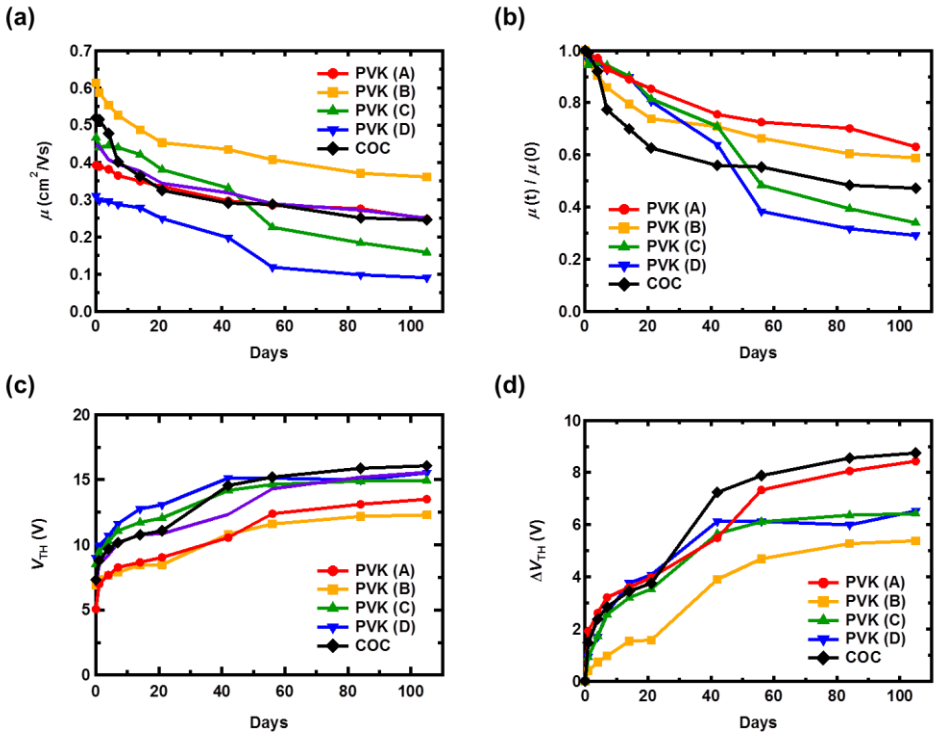

Figure 3.7 Time-dependent (a) electron field-effect mobility, (b) normalized field-effect mobility, (c) threshold voltage and (d) threshold voltage shift of the OFETs with various molecular weight-PVKs and COC interfacial layer.

In order to investigate how the molecular weight (M_w) of PVK influences on the long term air stability, we compared the time-dependent mobility degradation and threshold voltage shift of the OFETs with the PVK (A), (B), (C), and (D) interfacial layer to the ones of the device with the COC interfacial layer. As shown in Fig. 3.7, the OFETs with PVKs with relatively high molecular weight, PVK (A) and PVK (B), exhibited less mobility degradation than the one of the device with COC. With the relatively low molecular weight PVK (C) and PVK (D), the mobility was degraded faster than the ones of the device with COC. The air stability of the devices with a relatively high molecular weight-PVK was found to be superior to the device with COC. The superior air stability of the device with the high molecular weight-PVK interfacial layer can be explained by the density of polymer chain ends. Previous study has reported that the gaseous molecules such as water can stay in the free volumes at the polymer chain ends creating charge trapping states. [62] Lower molecular weight indicates more polymer chain ends, thus more charge trapping happens in air. Figure 3.8 shows the graphical illustration of the molecular weight-dependent charge trapping in the PVK interfacial layer.

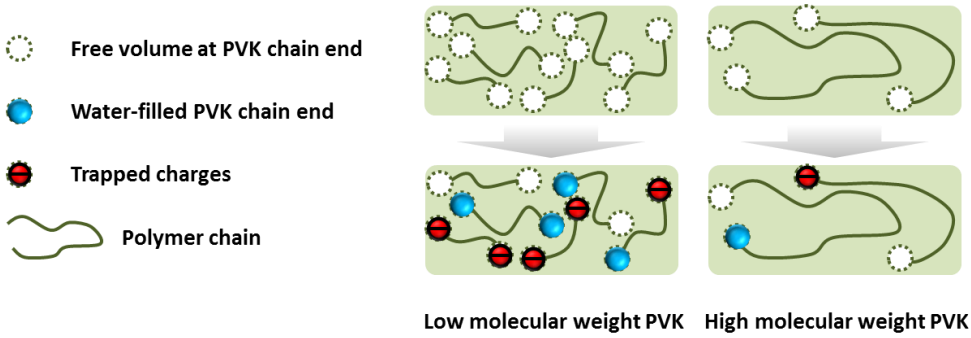

Figure 3.8. Graphical illustration of the molecular weight-dependent charge trapping in the PVK interfacial layer.

3.3 Summary

We demonstrated improved air stability of the n-type OFETs with an electrically active interfacial layer composed of PVK. A thermal annealing process was enabled thanks to the high glass transition temperature of PVKs, which resulted in high electron mobility of PTCDI-C13 OFETs. The electron donating property of PVK reduces interfacial charge trapping from the conducting channel of PTCDI-C13, which is attributed to the improved air stability of the OFETs. This platform using the PVK interfacial layer to improve air stability of n-type OFETs can help revealing n-channel behaviors of other new organic semiconducting materials in air. Air stable n-type OFETs realized by this system can be utilized for achieving various applications such as chemical and biological sensors.

Chapter 4

Bias Stability of Organic Field-Effect Transistors

For the commercial uses of OFETs, both the high mobility and good bias stability are required. Engineering the organic semiconductor-gate insulator interface is one of the most effective ways to improve electrical performance and stability of OFETs. A variety of methods have been introduced to engineer the organic semiconductor-insulator interface. A self-assembled monolayer (SAM) has often been used because of its distinct features including solution-process compatibility, thermal stability and roll-to-roll processability. Diverse SAM materials and deposition methods have been introduced, and intensive studies have been performed to improve the mobility or bias stability of OFETs by a SAM-treatment. Many groups have reported an improvement in the mobility of OFETs using various SAMs with different

characteristics. [63-67] In addition, there have been some reports on the improved bias stability of OFETs with a SAM-treatment. [68] Previous studies, however, focused mainly on either the mobility or bias stability, and overlooked the relationship between the mobility and bias stability of OFETs regarding SAM-treatment. Because both the high mobility and good bias stability are essential for practical uses, more systematic studies will be needed to reveal how the mobility and bias stability change simultaneously according to the SAM-treatment.

Previously, we investigated the effect of SAM alkyl chain length on the performance of OFETs in terms of mobility and bias stability. [38] We found out that there is a tradeoff relationship between mobility and bias stability of OFETs concerning the SAM alkyl chain lengths; the mobility of the OFETs with SAM-treatment was increased as the alkyl chain length of SAMs increased while inverse proportional relationship was observed between the bias stability and SAM alkyl chain length.

As a follow-up study, we demonstrated an efficient method to overcome the tradeoff relationship between the mobility and bias stability of OFETs regarding the SAM alkyl chain length. To overcome this tradeoff, a method for surface engineering using a two-step SAM-treatment is proposed. By treating long SAM and short SAM in sequence, both the high mobility and good bias stability were achieved. With two-step SAM-treatment, the OFET showed high mobility as a long SAM-treated OFET and good bias stability as a short SAM-treated OFET. We will start this chapter with a brief summary of the previous study, [38] and then move on to the two-step SAM-treatment to overcome the tradeoff relationship.

4.1 Electrical Performance

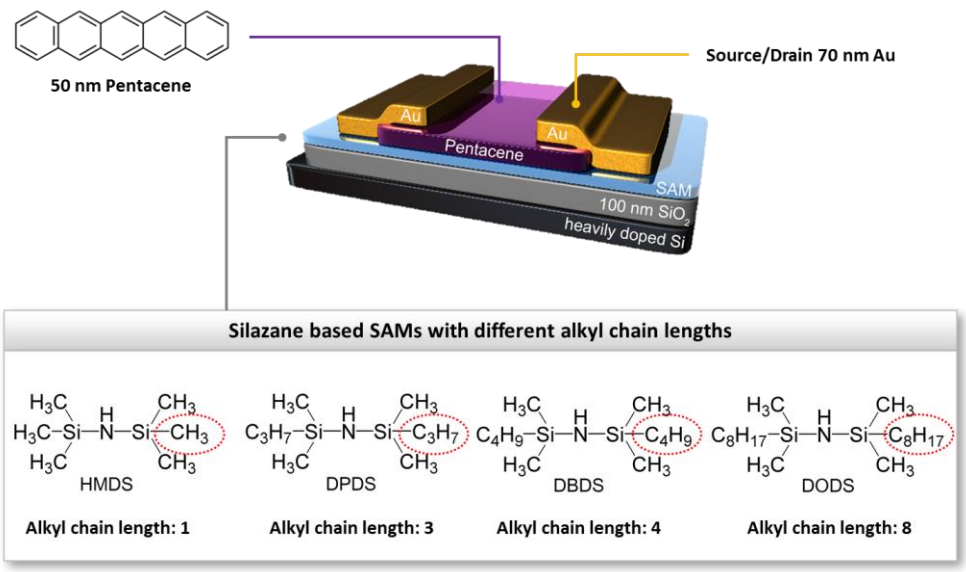

Figure 4.1 Schematic diagram of the pentacene-based OFET used in the present study and chemical structure of silazane-based SAMs with different alkyl chain lengths.

Figure 4.1 shows the device structure of the OFETs and chemical structures of SAMs. The silazane-based SAMs in this work have different alkyl chain lengths of 1 (for HMDS), 3 (for DPDS), 4 (for DBDS), and 8 (for DODS). Silazane-based SAMs were used instead of alkyltrichlorosilane SAMs considering the processability. Although OFETs with alkyltrichlorosilane SAM showed superior performance, they might not be suitable for a large-area or roll-to-roll process because of the sensitivity of alkyltrichlorosilane SAMs. [69] Many studies have examined the sensitivity of alkyltrichlorosilane SAMs, and it has been shown that the device performance varies considerably depending on the SAM structure. [70] Depending on the treatment conditions, alkyltrichlorosilane SAMs can react with each other, resulting in vertical

polymerization. [71] On the other hand, silazane-based SAMs show relatively good processability. Compared to alkyltrichlorosilane SAMs, silazane-based SAMs have mild treating conditions because it has one active group. [72] One example of silazane-based SAMs, HMDS, is already being used widely in photolithography as an adhesion promoter for the photoresist because of its good processability.

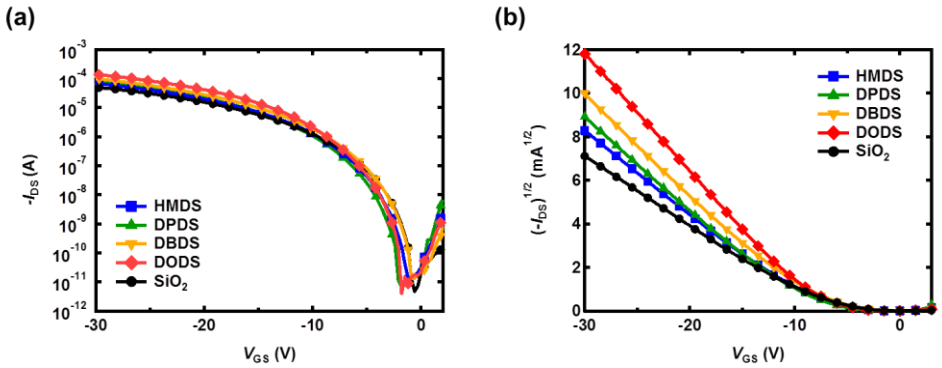

Figure 4.2 (a) Transfer characteristics of the OFETs with silazane-based SAMs at drain-to source voltage was −30 V. (b) Square root of the drain-to-source current versus gate-to-source voltage plot.

The mobility of the SAM-treated OFETs was first evaluated. Fig. 4.2(a) shows the transfer characteristics of the silazane-based SAM-treated OFETs. As shown in Fig. 4.2(b), mobility of the SAM-treated OFETs was clearly increased compared to the one of the OFETs without SAM-treatment. With the SAM-treatments, the average mobility was improved from 0.29 $cm^2/V \cdot s$ (bare SiO_2) to 0.46 $cm^2/V \cdot s$ (HMDS-treated), 0.61 $cm^2/V \cdot s$ (DPDS-treated), 0.65 $cm^2/V \cdot s$ (DBDS-treated), and 0.84 $cm^2/V \cdot s$ (DODS-treated). Figure 4.3 shows the mobility and threshold voltage values with respect to the SAM alkyl chain length. As shown in Fig. 4.3, there was a direct proportional relationship between the SAM alkyl chain length and mobility. Many studies on SAM alkyl chain length dependent mobility have been conducted in various systems, such as trichlorosilane SAMs on SiO_2, phosphonic acid SAMs on AlO_x, HfO_2 and SiO_2. [64-67] The optimized mobility of previous studies was obtained at an intermediate SAM alkyl chain length, suggesting that the mobility increased with increasing SAM alkyl chain length up to certain point and then

decreased. In the present study, only the increasing part was observed because this study used relatively short SAMs with an alkyl chain length less than 10.

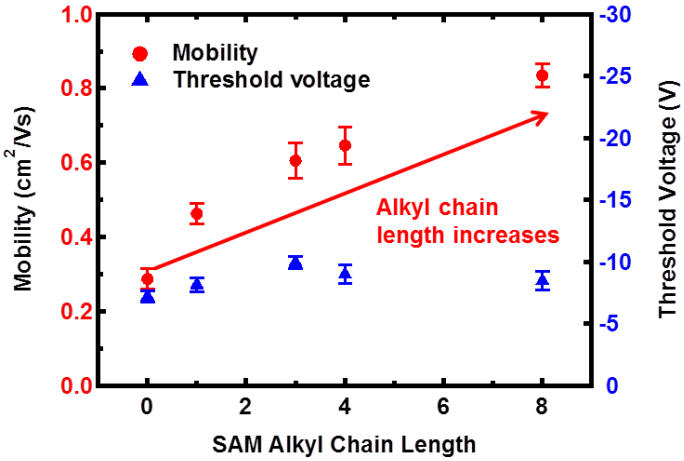

Figure 4.3 Mobility and threshold voltage values of the SAM-treated OFETs with respect to the SAM alkyl chain lengths.

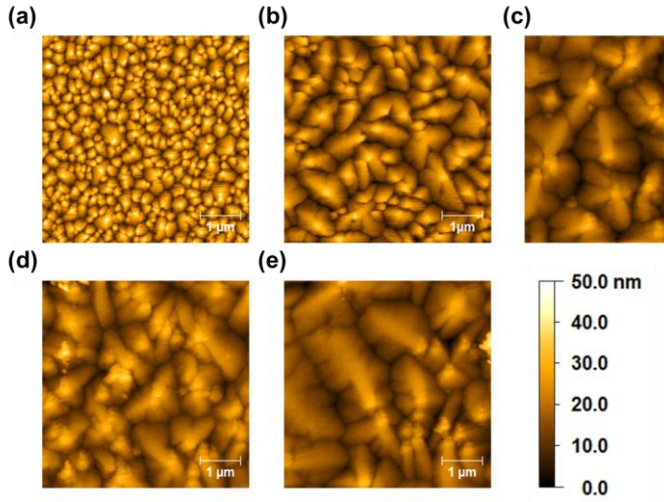

Figure 4.4 5 × 5 µm^2 AFM images of 50 nm pentacene thin films on (a) SiO_2, (b) HMDS, (c) DPDS, (d) DBDS, and (e) DODS. **[38]**

Figure 4.4 shows the AFM topographical images of the 50-nm pentacene thin films on various SAMs. The grain size and interconnection between grains affect charge transportation. [73, 74] Fewer grain boundaries are beneficial for better charge transportation because there are many trap states at the grain boundaries. Larger grains result in fewer grain boundaries, so a higher field-effect mobility can be obtained. As can be seen in Fig. 4.4(a), pentacene molecules form small grains on the SiO_2 surface but produce relatively larger pentacene grains on the SAM-treated SiO_2 surface. Similar to previous studies, the largest pentacene grains were observed in the device with the highest mobility. Direct proportional relationship was observed between the grain size of pentacene on SAM-treated SiO_2 surface and SAM alkyl chain length. This was well matched to the mobility of the SAM-treated OFETs, which represented that longer SAMs had better surface states for pentacene film growth. An increased pentacene grain size on the longer SAMs was one of the main reasons for the improved mobility.

The contact resistance (R_c) of the devices was also evaluated because the improved mobility might be also attributed to the reduced R_c. [75] The $R_c \cdot W$ values of the devices were obtained using the transmission line method. The $R_c \cdot W$ of each samples were similar regardless of the SAM-treatment (27–33 kΩ·cm at V_{GS}= −30 V). The SAM-treatment did not have a significant effect on R_c. Therefore, the improved mobility was induced mainly by the better charge transport in the larger pentacene grains.

4.2 Bias Stability

The bias stability of the SAM-treated OFETs was evaluated. The threshold voltage shift was observed for 2 h at a gate bias of −30 V (equivalent to −3 MV/cm of electric field). Figure 4.5(a) and 4.5(b) show the transfer characteristics of the OFETs with HMDS and DODS-treatment, respectively, with stress time. Figure 4.5(c) shows the threshold voltage shift of the devices as a function of the gate bias stress. As shown in Fig. 4.5(c), the threshold voltage shift of the OFET without SAM reached 50% of the applied gate bias stress in 2 hours, which indicated poor bias stability of the device without the SAM-treatment. The SAM-treated OFETs showed a smaller threshold voltage shift and were more stable under a high electric field of 3 MV/cm. Figure 4.5(d) shows the relationship between the bias-stress-induced threshold voltage shift and the SAM alkyl chain lengths. The threshold voltages of the devices with longer SAMs tended to change more than that of the devices with shorter SAMs. The threshold voltage shift of the DODS-treated device was 7.14 V, which was larger than that of the HMDS-treated device, 5.69 V. The bias instability is caused by the trapping states, which is strongly related to the surface hydroxyl group. Different threshold voltage shifts of the devices are related to different amounts of remanent hydroxyl groups on the SAM-treated SiO_2 surface. [31, 68, 76] Figure 4.6 shows the simplified illustration of SiO_2 surface before and after short and long SAM-treatment. The threshold voltage shift of the SAM-treated devices indicates that the shorter SAMs may cover more of the SiO_2 surface than the longer SAMs, reducing more surface trap states. Silazane-based SAMs with three alkyl groups normally form a disordered and amorphous structure due to the monofunctional reaction. Therefore, disordered long alkyl chains in SAMs can be expected to disrupt high packing, leading to poor passivation of hydroxyl groups on

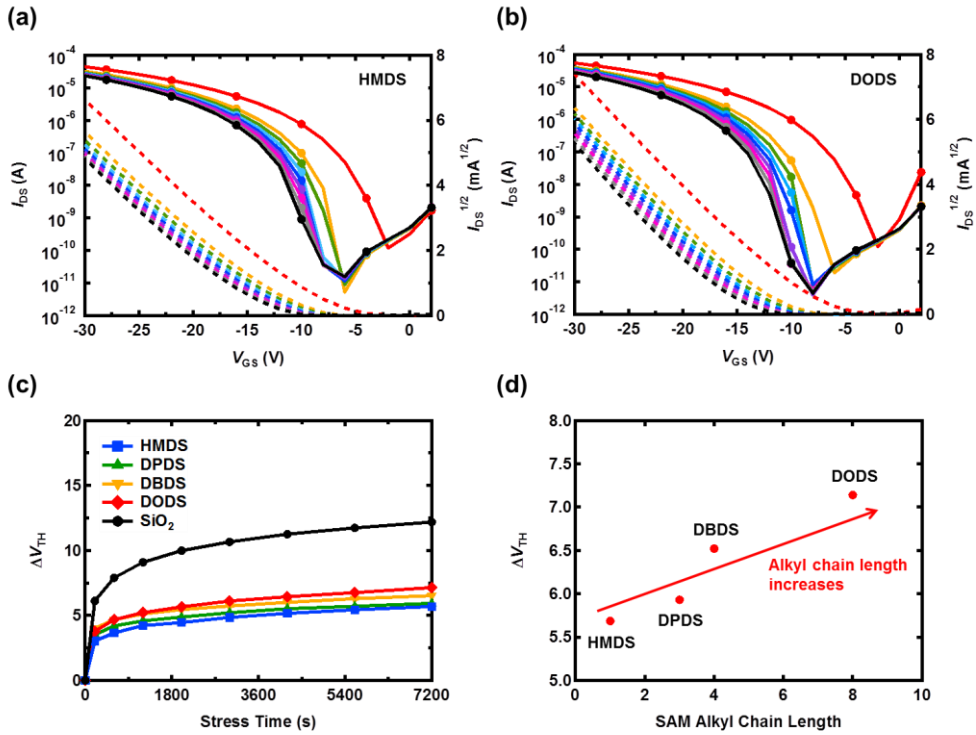

Figure 4.5 Transfer characteristics of the OFETs with (a) HMDS- and (b) DODS-treatment with stress time. Electrical bias of V_{GS}= −30 V, V_{DS}= 0V was applied to the device for 2 h. (c) Electrical evolution of threshold voltage shift of the OFETs with the SAM-treatment. (d) Bias-stress-induced threshold voltage shift of the OFETs with the SAM-treatment with respect to the SAM alkyl chain lengths.

the surface.

The threshold voltage shifts of the SAM-treated OFETs were well fitted to Eq. 2.5, the stretched exponential function for describing bias-stress-induced threshold voltage shift. The relaxation time (0.6–6 × 10^6 sec) and dispersive parameter (0.16–0.20) of the SAM-treated OFETs were comparable to the values in a previous study, which used a phenethyltrichlorosilane SAM on SiO_2 (β= 0.19, τ= 1–7 × 10^6 sec). [68] The relaxation time of the SAM-treated devices was longer than that of the device without the SAM-treatment.

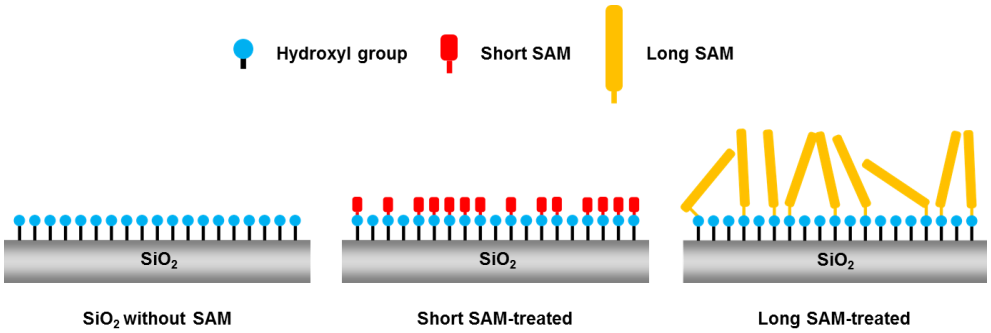

Figure 4.6 Simplified illustration of SiO_2 surface before and after short and long SAM-treatment. Short SAM covers more hydroxyl group on SiO_2 surface than long SAM.

4.3 Overcoming the Tradeoff Relationship

As discussed previously, a SAM with the long alkyl chain length is beneficial for high mobility, whereas SAM with a short alkyl chain length is beneficial for better bias stability with respect to the SAM-treatment with an alkyl chain length of 1 to 8. To overcome this tradeoff, a method for surface engineering, a two-step SAM-treatment was introduced. The surface states of the long SAM (DODS) were favorable for pentacene growth to achieve high mobility, but the low surface coverage of the long SAM led to gate bias instability. To reduce the residual hydroxyl groups on DODS-treated SiO_2 surface, DODS-treated SiO_2 was treated one more time by HMDS. As described in Fig. 4.7(a), a short SAM, HMDS, was used to passivate the residual hydroxyl groups of the DODS-treated SiO_2. The device performance with a two-step SAM-treatment was evaluated and compared with the other devices. Figure 4.7(b) shows the I_{DS} degradation under gate bias stress. As shown in Fig. 4.7(b), the electrical performance of two devices, DODS-treated and two-step SAM-treated, exhibited a similar drain-to-source on-current (at V_{GS}= V_{DS}= −30 V) at the beginning. As gate bias stress was applied, the DODS-treated device showed sharper on-current degradation compared to the two-step SAM-treated device. Figure 4.7(c) shows the threshold voltage shift of the two-step SAM-treated device. The threshold voltage shift was 5.35 V, which is similar to that with the HMDS-treatment, 5.69 V. The DODS-treated device with an extra HMDS-treatment improved the bias stability, whereas the high mobility remained the same. The electrical performance of the two step SAM-treated device remained high similar to the DODS-treated devices, and its bias stability was improved, similar to the one of the HMDS-treated device. Table 4.1 lists the electrical performance and bias stability of the SAM-treated OFETs.

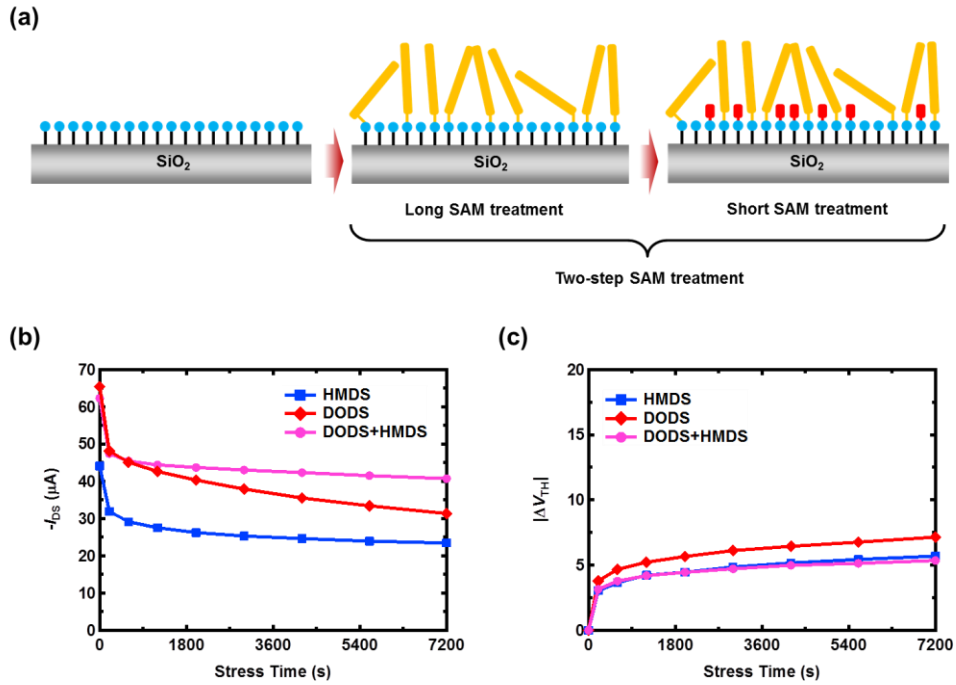

Figure 4.7. (a) Simplified illustration of two-step SAM-treatment. Improved bias stability of the OFETs by using two-step SAM-treatment in terms of (b) drain-to-source on-current degradation and (c) threshold voltage shift under the gate bias stress of −30 V for 2 h.

Table 4.1 Device parameters of the OFETs with SAM-treatment.

Samples	Mobility ($cm^2/V \cdot s$)	V_{TH} (V)	I_{on}/I_{off}	ΔV_{TH} after 2 h [V][a]	Relaxation time (sec)	Dispersion parameter
SiO_2	0.29 (±0.03)	−7.20 (±0.48)	~10^6	12.19	2.58×10^4	0.24
HMDS	0.46 (±0.03)	−8.15 (±0.59)	~10^6	5.69	2.38×10^6	0.20
DPDS	0.61 (±0.05)	−9.95 (±0.51)	~10^7	5.93	6.25×10^6	0.16
DBDS	0.65 (±0.05)	−8.97 (±0.76)	~10^7	6.52	5.57×10^6	0.16
DODS	0.84 (±0.03)	−8.45 (±0.76)	~10^7	7.14	6.22×10^5	0.20
DODS +HMDS	0.88 (±0.03)	−9.10 (±0.22)	~10^7	5.34	1.67×10^7	0.16

[a] Under gate bias stress of −30V

4.4 Summary

In summary, the relationship between mobility and bias stability of OFETs regarding SAM-treatment was studied systematically. Using four types of silazane-based SAMs with different alkyl chain lengths, it was found that the mobility increased with increasing SAM alkyl chain length. On the other hand, the bias stability was inversely proportional to the SAM alkyl chain length, which represented tradeoff between the mobility and bias stability regarding the SAM-treatment. To overcome this tradeoff, two-step SAM-treatment method was employed, and high mobility and good bias stability were achieved. This is the significant observation of a tradeoff relationship between the mobility and bias stability of OFETs regarding a SAM-treatment, which indicates that a new approach is required to improve both the mobility and bias stability. The proposed two-step SAM-treatment can solve the tradeoff simply, and it may also be applied to other systems.

Chapter 5

Air and Bias Stability of Molybdenum Disulfide Field-Effect Transistors

One of key limitations for TMDCs devices like other types of low dimensional materials is coming from the intrinsic nature of instability associated with easy adsorption of gaseous molecules such as oxygen and moisture due to large surface areas of low dimensional materials. [33, 34, 77] Even though several studies, adopting plasma-enhanced chemical vapor deposition (PECVD), [33] atomic layer deposition (ALD), [78] PMMA passivation, [79] for the improvement of instability of TMDC devices were reported, their approaches have several drawbacks, in the sense of requiring relatively high temperature process (~350°C), cost-ineffectiveness, and non-ideal surface chemistry of passivation layers, prone to easy permeation of

moisture. Thus, one of representative hydrophobic polymers, CYTOP passivation was lately reported to improve the instability of TMDC FETs and optical sensors in diodes. [80] However, their evaluations on electrical characteristics for the effectiveness of CYTOP passivation were very limited, thereby not fully enlightened in the respects of reliability (or longevity) in air and bias temperature instability when CYTOP passivation was adopted.

In this study, we systemically studied to evaluate the effects of CYTOP passivation for molybdenum disulfide (MoS_2) FETs as one of representative TMDCs, especially for two respects. The first is to isolate the origins of device instability, coming from either internal device issues or external environmental issues; for the validation of this issues, we first implemented highly stable MoS_2 FETs with negligible hysteresis gaps (ΔV_{HYS}~ 0.1 V), indicating low defect levels were included in the device itself, via multiple annealing schemes and then, the long term stability of MoS_2 FETs with (or without) passivation in air were evaluated by tracking electrical properties up to 50 days. Furthermore, the bias stability of the MoS_2 FETs with (or without) passivation were directly investigated by analyzing short-term reliability. For the validation of CYTOP passivation effects, their electrical parameters such as electrical field-effect mobility, contact resistance, device life time, and the characteristic trapping time, the energy barrier distribution for the multi-layer MoS_2 FETs with (or without) passivation were extracted and compared accordingly.

5.1 Fabrication MoS_2 FETs with Negligible Hysteresis

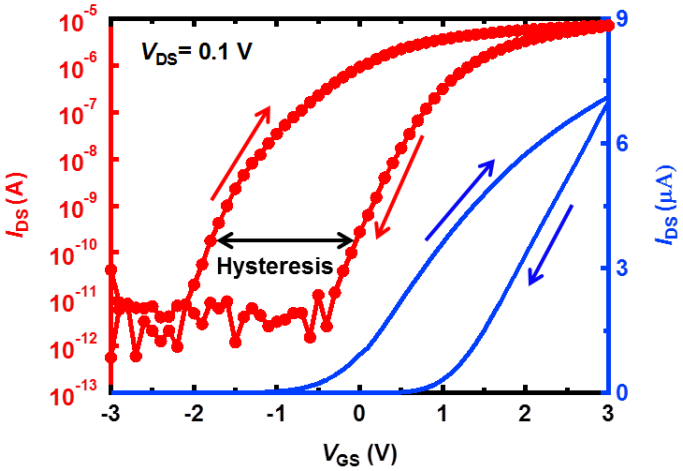

Figure 5.1 Typical transfer characteristics of the back-gated MoS_2 FETs without thermal annealing.

The instability of MoS_2 FETs is on account of the nature of two-dimensional materials, which is related to the large surface-to-volume ratio and the easy adsorption of gaseous molecules [81]. The instability can be represented by a large hysteresis gap of devices; hysteresis gap is defined as the threshold voltage difference between the forward and backward sweeps. The large hysteresis of MoS_2 FETs has often been observed in many studies regardless of the device structure (i.e. top-gated or bottom-gated) and the number of layers [33, 35-37]. Figure 5.1 shows a typical transfer characteristic of the back-gated MoS_2 FETs. As shown in the Fig. 5.1, a large hysteresis (ΔV_{TH}) of 1.4 V was observed. The number of trapped charges (n_t) calculated from the relationship, $n_t = \Delta V_{TH} \cdot C_{ox}/q$, was 3.01 × 10^{12} cm^{-2} which represents the destitute stability of the devices. This large number of trapped charge indicates that high defect levels were included in the device itself.

To reduce the hysteresis, the possible origins of surface trap states were first classified as followed; carbon residues contaminated during the exfoliation and transfer process, photoresist residues, and adsorbed H_2O and O_2 molecules. The above-mentioned attributes for surface trap creation should be eliminated to reduce the hysteresis in MoS_2 FETs. High temperature thermal annealing has often been employed to remove gaseous adsorbates and organic residue on MoS_2 [36, 82-84]. Previous studies, however, did not aim to achieve hysteresis-free FETs; thus, a significant hysteresis gap was often observed even after employing the thermal annealing process. To achieve the hysteresis-free behavior of MoS_2 FETs (i.e., to eliminate the possible origins of surface trap creation), thermal annealing was performed twice in the fabrication process. The first annealing was applied in between the transfer and the photolithography process, and the second annealing was executed after the lift-off process. Thermal annealing was performed at 400 ℃ for 1 h in a mixture gas of H_2/Ar.

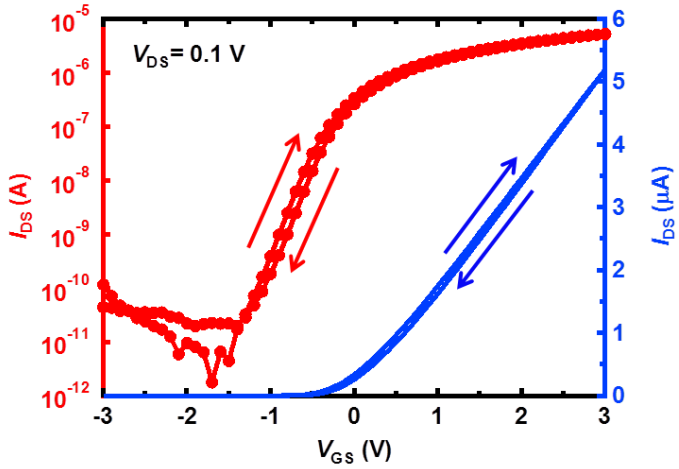

Figure 5.2 Transfer characteristics of the back-gated MoS_2 FETs with negligible hysteresis by employing thermal annealing.

Figure 5.2 shows the transfer characteristics of the MoS_2 FETs with thermal annealing. As shown in Fig. 5.2, a negligible hysteresis gap (ΔV_{TH}) of 0.1 V was observed, which indicates that the possible origins of surface traps are remarkably removed through thermal annealing. Note that this negligible hysteresis in ambient air is achieved with a back-gated structure without any further passivation layer. Furthermore, all the fabricated devices (more than 30 devices) exhibit similar hysteresis gaps (ΔV_{TH}) of from 0.05 V to 0.1 V which represents the uniformity and reproducibility of the method.

5.2 CYTOP Passivation Effect

After implementing the MoS2 FETs with negligible hysteresis, we investigated the effect of CYTOP passivation layer on both long term air stability and short term bias stability. Fig. 5.3 (a) shows a perspective view of the multilayer MoS_2 FETs passivated with CYTOP which has been employed as an excellent inhibitor for permeation of moisture (or/and oil) due to a hydrophobic, fluorinated ending group. [85-87] The typical thickness of multi layers of MoS_2 turned out to be within the range of 13 nm which approximately corresponds to 20 layers.

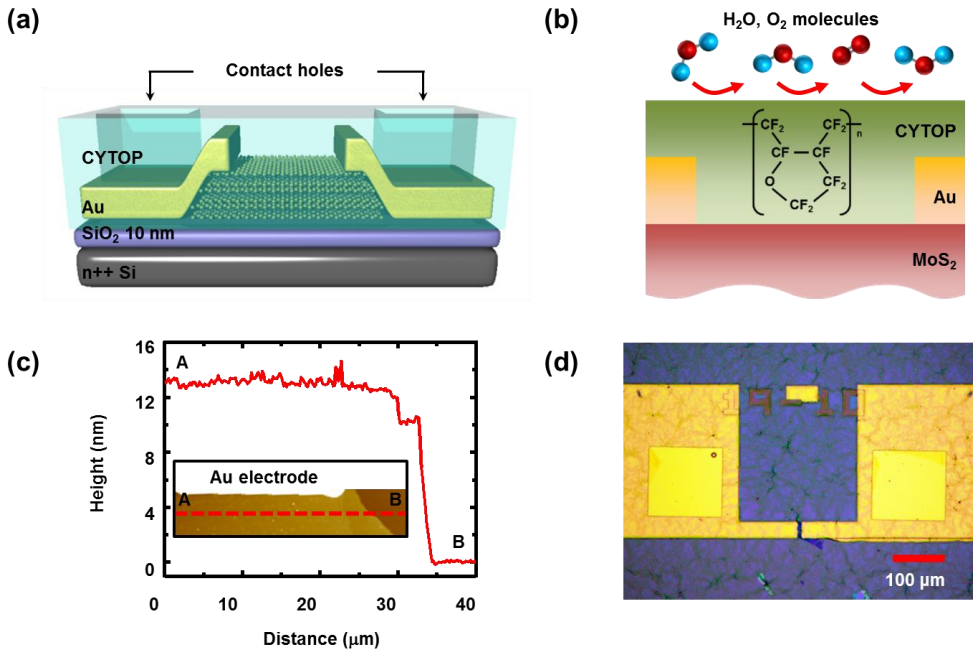

Figure 5.3 (a) A perspective view of the multilayer MoS_2 FETs with CYTOP passivation. (b) Schematic to explain a conceptual model for blocking water and oxygen molecules by CYTOP passivation (c) AFM profile of the multilayer MoS_2 flakes. (d) An optical microscope image of the fabricated MoS_2 FETs after contact opening process. The device has a physical dimension (W/L~30/10 μm).

Fig. 5.4(a) shows the transfer characteristics of the multilayer MoS_2 FETs with a ratio of width to length (W/L=30/10 μm) before and after CYTOP passivation. The transfer characteristics at a drain-to-source voltage (V_{DS}) of 0.1 V were measured before CYTOP passivation and then, consecutively measured *I-V* properties right after passivation of CYTOP on the same device. As shown in Fig. 5.4(a), the multilayer MoS_2 FETs even before passivation show a negligible hysteresis gap (ΔV_{HYS}= 0.1 V), indicating that optimized annealing process via multiple annealing scheme leads to the elimination of possible candidates of traps on the surface of the multilayers of MoS_2 associated with absorbates (i.e., moisture or/and carbon residues). [35, 77] Also, the MoS_2 FETs show good switching property with sub-threshold slope (*SS*) of 247 mV/dec and on/off ratio of ~10^7. Furthermore, there was no noticeable degradation observed in turn-on regime even after passivation, and the extracted field-effect mobility (μ_{FET}) and threshold voltage (V_{TH}) of the multilayer MoS_2 FETs after passivation are 16.8 $cm^2/V{\cdot}s$ and −0.04 V, which are similar to the values before passivation, respectively. Each field-effect mobility (μ_{FET}) before and after passivation in the linear regime was extracted at a maximum point of transconductance (g_{m_max} ~ 1.75 μS) according to $\mu_{FET}= g_m L\times(WC_{ox}V_{DS})^{-1}$, where C_{ox} and g_m are the gate insulator capacitance per unit area and the transconductance, respectively. However, in the off-current regime, slightly increased off-current right after CYTOP passivation was observed and then relieved back to the initial off-current level (~a few pA) after one day later, which is speculated coming from temporal charge generation and relaxation effects in CYTOP layer, [80, 85] typically observed after encapsulation of the fluorinated polymers. [88, 89] Figure 5.4(b) shows output characteristics of the MoS_2 FET after passivation. The device showed typical n-type modulation properties as gate-to-source voltage (V_{GS})

increased from 0 V to 3 V and a good saturation behavior was observed in an operation regime of saturation, indicating the device itself after passivation sustained its virgin characteristics before passivation.

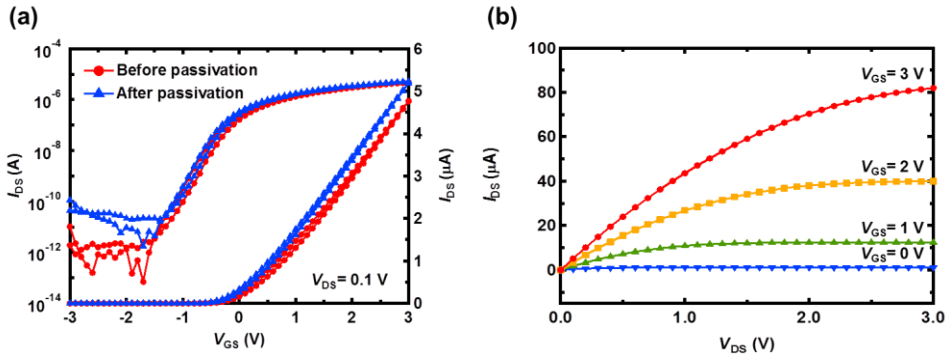

Figure 5.4 (a) Transfer characteristics of the MoS_2 FETs before and after CYTOP passivation. The electrical measurements were performed in a linear regime at V_{DS}= 0.1 V. (b) Output characteristic of the MoS_2 FETs with CYTOP passivation.

5.3 Long Term Air Stability

For the evaluation of CYTOP passivation effects on longevity (or long term stability) of the MoS_2 FETs, the multilayer MoS_2 FETs were fabricated and selected as having similar both its flake thickness (~13 nm) and electrical characteristics (~16 $cm^2/V{\cdot}s$, on/off ratio> 10^6) at initial, followed by CYTOP passivation. The MoS_2 FETs with (or without) passivation were stored in ambient air. The electrical characteristics for each device were measured with time up to 50 days in air. Figure 5.5(a) and 5.5(b) show that the transfer characteristics for the representative MoS_2 FETs without and with passivation with time, respectively. Overall, the devices without passivation show huge degradation in on-current and large threshold voltage shift toward positive direction, whereas the passivated MoS_2 FETs showed slight current reduction, but all of sub-threshold slope (*SS*) with time were mostly consistent within the error range of experimental measurement. In addition, the same trends for the passivation effects on the MoS_2 FETs were consistently observed for all other devices (~ at least larger than 5 devices) on the same sample.

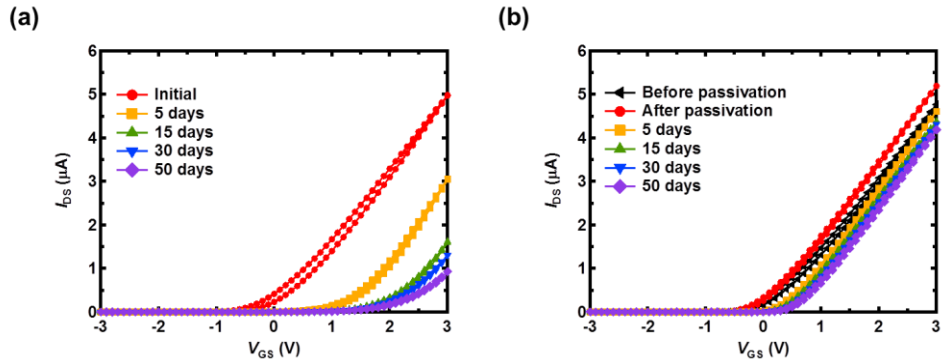

Figure 5.5 Transfer characteristics of the MoS_2 FETs (a) without and (b) with CYTOP passivation as the time stored in air increased. All electrical characteristics were measured in air.

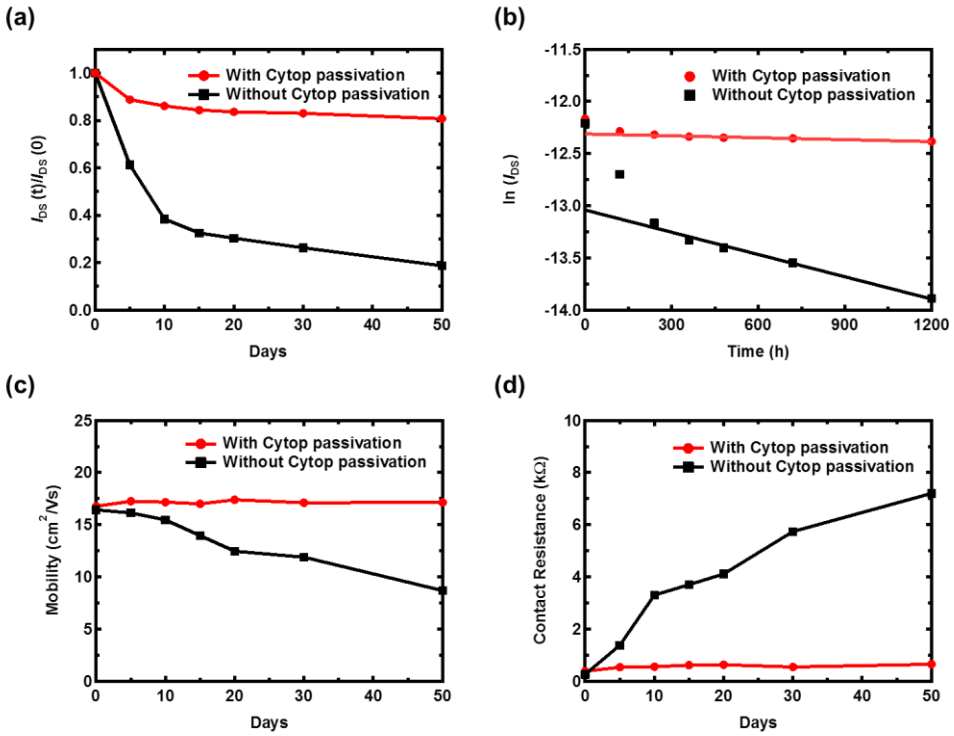

Figure 5.6 (a) Normalized drain-to-source current (I_{DS}) behavior with time for the MoS_2 FETs with (or without) CYTOP passivation. Each value (I_{DS}) was extracted with time at a bias condition (i.e., V_{GS}= 3 V, V_{DS}= 0.1 V). I_{DS} (0) indicates the current level at initial (t= 0 sec). (b) Semi-logarithmic plots for log (I_{DS}) versus time and each solid line in the inset correspond to its extrapolated line. The time constant for the device with (or without) passivation is $\gamma_{w/}$= 6.1 × 10^{-5} sec (or $\gamma_{w/o}$= 4 × 10^{-3} sec), respectively. Electrical evolution of (c) field-effect mobility (μ_{FET}) and (d) contact resistance (R_c) for MoS_2 FETs with and without CYTOP passivation with time stored in air.

For more quantitative analysis for both of the devices in degradation, normalized current level with time was depicted in Fig. 5.6(a) and their current degradation behavior in the Fig. 5.6(b) was also replot in semi-logarithmic scale, indicating exponential decay of drain current with time [90] so that it can be analytically expressed as

$$I_{DS}(t) = I_{DO}\exp(-\gamma t), \quad \textbf{(5.1)}$$

where I_{DO} is the initial on-current in air with (or without) passivation and γ is the slope obtained from the plot of $\log(I_{DS})$ versus time as shown in Fig. 5.6(b). The extracted values of γ for both of the devices are 6.1×10^{-5} (with passivation) and 4.0×10^{-3} (without passivation). The life times, extracted as the time when the on-current are deteriorated to a half of the initial current for both of the devices, are 377 days (with passivation) and 7 days (without passivation), respectively. In addition, for the analysis of CYTOP passivation effects on electrical performance of the MoS_2 FETs, field-effect mobility (μ_{FET}) and contact resistance (R_c) with time were extracted and compared for both of the devices stored in air. For the estimation of the electrical contact properties, contact resistance (R_c) was extracted by using Y-function method reported elsewhere. [41, 42, 91] Figure 5.6(c) and 5.6(d) show that field-effect mobility (μ_{FET}) and contact resistance (R_c), respectively, for the MoS_2 FETs with passivation remains consistently within experimental error range (~4%) with time in air. On the other hand, as the exposure time in air increases the MoS_2 FETs without passivation show the noticeable degradation of field-effect mobility (μ_{FET}) from 16.2 $cm^2/V{\cdot}s$ to 8.7 $cm^2/V{\cdot}s$ and the significant increase of contact resistance (R_c) from 0.26 kΩ to 7.3 kΩ . The noticeable decrease of field-effect

mobility (μ_{FET}) with time is mainly attributed to the chemisorption of oxygen or/and water molecules on the back channel of MoS_2, which could act as local Coulomb scatters for accumulated charge (i.e., electron) centroid nearly located in the front channel. In addition, the increase of contact resistance (R_c) with time is speculated coming from the increase of Schottky barrier ($\sim\phi_{SB}$) between MoS_2 and Au associated with the increase of effective work function ($\sim\phi_m$) of Au where is nearby S/D contact regions due to chemisorption of oxygen [92] on the surface of contact regions of MoS_2 ($\sim\phi_s$). Therefore, the dramatic reduction of life time for the MoS_2 FETs without passivation is mainly ascribed to both the noticeable deterioration of field-effect mobility (μ_{FET}) and the significant increase of contact resistance (R_c) associated with chemisorption (or/and penetration) of oxygen or/and water molecule, predominantly on the back surface of MoS_2. The analyses on field-effect mobility (μ_{FET}) and contact resistance (R_c), rigorously extracted from Fig. 5.6(c) and 5.6(d), substantiate that the CYTOP passivation for MoS_2 FETs can be one of efficient methods to prevent oxygen or/and water molecules from penetration into channel areas of MoS_2 FETs, which lead to the reliable operation in air.

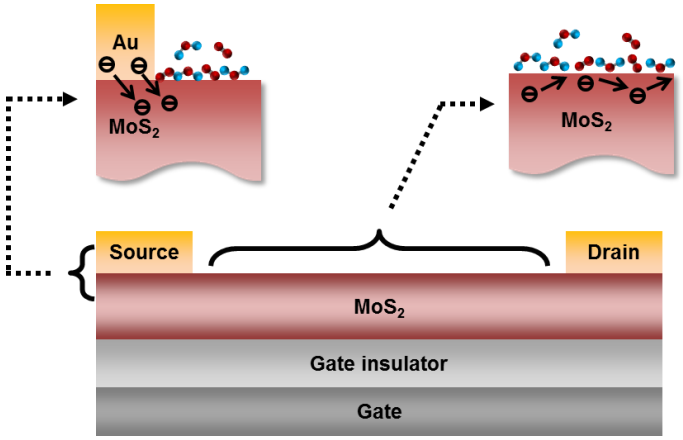

Figure 5.7 Conceptual models for degradation of the MoS_2 FETs in air without CYTOP passivation.

5.4 Bias Stability

The effect of CYTOP passivation on bias stability in air can be one of key aspects to be investigated for evaluation of reliability of MoS_2 FETs. For the investigation of bias stress effects, MoS_2 FETs were implemented and their electrical properties showed field-effect mobility (μ_{FET} ~ 22 $cm^2/V{\cdot}s$), threshold voltage (V_{TH}~ −0.58 V), and high on/off ratio (~10^7), respectively. To examine the effects of bias stress, we applied gate-to-source voltage (V_{GS}) of 3 V to the MoS_2 FETs with (or without) passivation while holding drain-to-source voltage (V_{DS}) at 0 V During the bias temperature stress, the substrate temperature and effective stress time were fixed as 60°C and 1800 sec, respectively. To avoid the device variation effects on reliability characteristics of MoS_2 FETs, the bias stress was first applied to the MoS_2 FETs

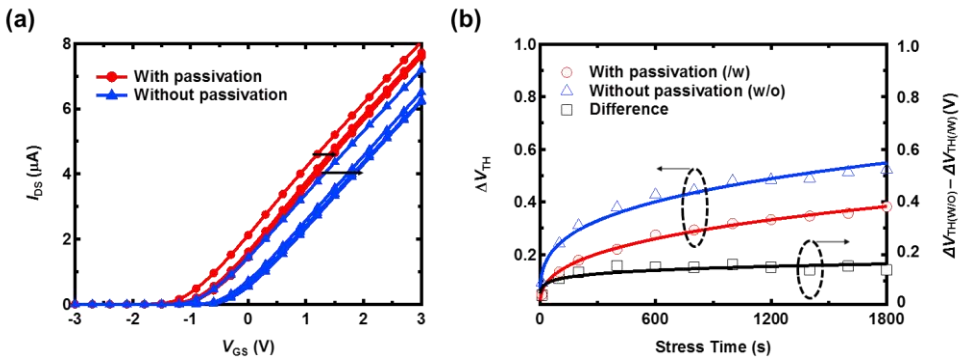

Figure 5.8 (a) Transfer characteristics of the MoS_2 FETs with (or without) CYTOP passivation with stress time. Electrical bias of V_{GS}= 3 V, V_{DS}= 0V was applied to the device for 1800 sec at the substrate temperature of T_{sub}= 60°C. (b) Electrical evolution of threshold voltage shift of the MoS_2 FETs with (or without) CYTOP passivation with stress time. ΔV_{TH}(w/) and ΔV_{TH}(w/o) correspond to the threshold voltage shift for the device with and without CYTOP encapsulation, respectively.

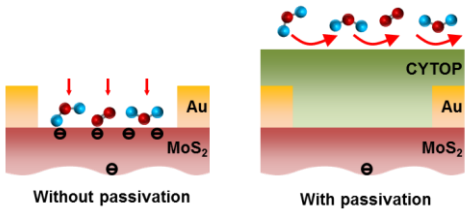

Figure 5.9 Conceptual models to explain gas adsorption for the MoS_2 FETs with (or without) CYTOP passivation.

without passivation, and then all the electrical characteristics were analyzed, followed by baking at 150°C for 30 min in a glove box to promote the recovery of electrical characteristics to the virgin state. After confirmation of recovery of electrical characteristics for the MoS_2 FETs, subsequently CYTOP passivation was performed, and then the same stress conditions were applied to the same device with passivation. Figure 5.8(a) indicates the evolution of transfer characteristics for each MoS_2 FET with (or without) passivation. The behaviors of threshold voltage shifts (ΔV_{TH}) are noticeably different; the threshold voltage shift (ΔV_{TH} (w/) (or ΔV_{TH} (w/o))) for the MoS_2 FETs with (or without) passivation after bias stress test is 0.38 V (or 0.52 V), respectively.

To get some insights, we analyzed the behaviors of threshold voltages depending on stress time for the MoS_2 FETs with (or without) passivation as shown in Fig. 5.8(b). The bias stress-induced threshold voltage shift (ΔV_{TH}) can be described by the stretched exponential function, Eq. 2.5. One of the extractable values from the stretched exponential function, the value of dispersion parameter (β) is related to the distribution of the activation energy for charge trapping ($\Delta E_B = k_B T/\beta$) where k_B is the Boltzmann constant and T is substrate temperature. Typically the energy structure of each trap site can be described by E_τ (i.e., the mean barrier height) and

the barrier distribution ($\Delta E_B = k_B T_o$). [62] Even though the validity of this model (i.e., Eq. 2.5) to the system of MoS_2 FETs is not yet clear, but needs to be studied separately later, the electrical fittings for the experimental threshold voltage shifts are outstandingly well fitted, which are assessed by its coefficient of determination [93] ($R^2 \sim$ 0.994 for with and 0.976 for without passivation, respectively) and the extracted values of the barrier distribution for the MoS_2 FETs with (or without) passivation correspond to 7.76×10^{-2} eV (or 1.02×10^{-1} eV). The data suggest that the barrier distribution for the device without passivation is about 25% large as much as that of device with passivation. This difference is, at least partly, a consequence of chemisorption of oxygen and water molecules on the back channel of the MoS_2 FETs which results in the increase of the chance for trapping of electrons in the back channel. In addition, the graph (square symbols) in Fig. 5.8(b), representing the difference of a threshold voltage shift (ΔV_{TH}) for each device with (or without) passivation, shows a reasonably good fit with Eq. 2.5; the extracted values of threshold voltage shift (ΔV_{TH}), characteristic trapping time (τ) and dispersion parameter (β) are 0.14 V, 2.2×10^9 sec and 0.2, respectively. Moreover, the barrier distribution ($\Delta E_B = k_B T_o$) for the curve (square symbols) was extracted as 1.43×10^{-1} eV which is about 40% larger than that of device without passivation. This suggests that the increased barrier distribution ($\Delta E_B = k_B T_o$) is probably associated with the net effects of back channel regions where the events of trapping might promote to occur via trap sites with wide barrier distribution due to external gases (i.e., O_2 and H_2O). Notice that subtraction of the values which are extracted for each device with (or without) passivation conceptually reflects the pure portion of back channel region in terms of trapping events, on the assumption that CYTOP passivation perfectly prevents external gases (i.e., O_2 and H_2O) from permeation into

back channel. In the respect of FETs based on other materials such as organic semiconductor, the gate bias instability is typically resulted from charge trapping in a gate insulator, at the interface between insulator and semiconductor, and in a semiconductor itself. In the case of the MoS_2 FETs, among the afore mentioned several attributes of origins for device instability, the back channel portion can be much more pronounced due to charge trapping on the back channel region of the MoS_2 FETs, ascribed by easy adsorbed water or/and oxygen molecules. This is attributed to the nature of high surface-to-volume ratio of 2D structure and hydrophilicity of the MoS_2 surface. [33, 34]

5.5 Summary

In summary, we implemented multiplayer MoS_2 FETs with negligible hysteresis gap via multiple annealing schemes, and the device instability issues associated with internal (i.e., gate dielectric, interface of semiconductor and dielectrics, and contact properties) and external (i.e., gas ambient effects) attributes were systematically analyzed by investigating life times in air and short-term bias instabilities for the devices with (or without) passivation of CYTOP. For the quantitative analyses on device degradation in air, field-effect mobility (μ_{FET}) and contact resistance (R_c) with time were extracted, and the results indicate that the noticeable degradation of field-effect mobility (μ_{FET}) and increase of contact resistance (R_c) for the device without passivation in air could be one of main attributes in current degradation. Furthermore, the short-term reliability for the devices with (or without) passivation were analytically evaluated by using both stretched exponential decay formula and experimental threshold voltage shift (ΔV_{TH}), and their characteristics trapping time (τ), dispersion parameter (β), and energy barrier distribution ($\Delta E_B = k_B T_o$) indicate that external effects, associated with O_2 and H_2O, possibly increase the energy distribution of energy barrier, which result in fast decay in the early stage of current-voltage behaviors. In addition, CYTOP passivation can be one of good candidates to achieve long term and short-term reliability of MoS_2 FETs based on cost-effective, low-temperature process scheme, enlightening the feasibility on usage for different types of 2D materials including graphene and other TMDC materials for the envisioned application.

Chapter 6

Conclusion

In this thesis, the stability issues of the OFETs and MoS_2 FETs were investigated in terms of air stability and bias stability.

Firstly, we demonstrated the improved air stability of n-type OFETs by employing an electrically active interfacial layer. PVK was employed as an interfacial layer because of two aspects; high glass transition temperature of PVK enables thermal post annealing of the active layer and electron donating property of PVK can reduce the interfacial charge trapping of the organic semiconductor. With the PVK interfacial layer, the n-type OFETs based on PTCDI-C13 exhibited high mobility and improved air stability. The PVK interfacial layer was found to be an efficient interfacial layer for enabling high performance and air stable n-type OFETs.

Next, we demonstrated the method to overcome the tradeoff relationship between the bias stability and mobility of the OFETs regarding SAM-treatment. The

finding from the previous study is that the mobility of the OFETs with SAM-treatment increased as the SAM alkyl chain length increased while inverse proportional relationship was observed between the bias stability and SAM alkyl chain length. To overcome this tradeoff, we used two-step SAM-treatment; sequential treatment of long SAM and short SAM. As a result, the OFET showed improved bias stability as short SAM-treated OFETs, maintaining the high mobility as a long SAM-treated OFET.

Lastly, the highly stable MoS_2 FETs was demonstrated, followed by the systematic studies of the CYTOP passivation effect on the long term air stability and short term bias stability. We implemented highly stable MoS_2 FETs with a negligible hysteresis gap via multiple annealing schemes, and then the effect of CYTOP passivation on the long term air stability and short term bias stability were investigated. The results indicate that the noticeable degradation of field-effect mobility and increase of contact resistance for the device without passivation in air could be one of main attributes in air instability. Furthermore, the results of short-term bias stability implies that external effects, associated with O_2 and H_2O, possibly increase the energy distribution of energy barrier, which result in fast decay in the early stage of current-voltage behaviors.

In conclusion, this thesis provides efficient methods to improve the air and bias stability of the FETs based on organic semiconductors and TMDCs. Engineering the semiconductor-gate insulator interface by polymeric layer or SAM was used to improve the air or bias stability of the OFETs. For improving the stabilities of TMDC FETs, semiconductor-atmosphere interface was property engineered by employing thermal annealing and CYTOP passivation layer. Achieving highly stable FETs is of significance not only for the practical uses in various applications but also for studying the intrinsic nature of nano materials. The proposed methods to

improve the stability of the FETs can be also applicable to other types of nano optoelectronic devices such as light-emitting diodes and photovoltaic cells.

Bibilography

[1] C. Luo, A.K.K. Kyaw, L.A. Perez, S. Patel, M. Wang, B. Grimm, G.C. Bazan, E.J. Kramer, A.J. Heeger, General Strategy for Self-Assembly of Highly Oriented Nanocrystalline Semiconducting Polymers with High Mobility, *Nano Lett.* **14**, 2764-2771 (2014).

[2] D. Jariwala, V.K. Sangwan, L.J. Lauhon, T.J. Marks, M.C. Hersam, Emerging Device Applications for Semiconducting Two-Dimensional Transition Metal Dichalcogenides, *ACS Nano* **8**, 1102-1120 (2014).

[3] D. Lembke, S. Bertolazzi, A. Kis, Single-Layer MoS2 Electronics, *Acc. Chem. Res.* **48**, 100-110 (2015).

[4] D. Akinwande, N. Petrone, J. Hone, Two-dimensional flexible nanoelectronics, *Nat. Commun.* **5**, 5678 (2014).

[5] D.-m. Sun, M.Y. Timmermans, Y. Tian, A.G. Nasibulin, E.I. Kauppinen, S. Kishimoto, T. Mizutani, Y. Ohno, Flexible high-performance carbon nanotube integrated circuits, *Nat Nano* **6**, 156-161 (2011).

[6] M. Gsänger, D. Bialas, L. Huang, M. Stolte, F. Würthner, Organic Semiconductors based on Dyes and Color Pigments, *Adv. Mater.* **28**, 3615-3645 (2016).

[7] M. Kaltenbrunner, T. Sekitani, J. Reeder, T. Yokota, K. Kuribara, T. Tokuhara, M. Drack, R. Schwodiauer, I. Graz, S. Bauer-Gogonea, S. Bauer, T. Someya, An ultra-lightweight design for imperceptible plastic electronics, *Nature* **499**, 458-463 (2013).

[8] H. Minemawari, T. Yamada, H. Matsui, J.y. Tsutsumi, S. Haas, R. Chiba, R. Kumai, T. Hasegawa, Inkjet printing of single-crystal films, *Nature* **475**, 364-367 (2011).

[9] Y. Diao, B.C.K. Tee, G. Giri, J. Xu, D.H. Kim, H.A. Becerril, R.M. Stoltenberg, T.H. Lee, G. Xue, S.C.B. Mannsfeld, Z. Bao, Solution coating of large-area organic semiconductor thin films with aligned single-crystalline domains, *Nat. Mater.* **12**, 665-671 (2013).

[10] C.-a. Di, F. Zhang, D. Zhu, Multi-Functional Integration of Organic Field-Effect Transistors (OFETs): Advances and Perspectives, *Adv. Mater.* **25**, 313-330 (2013).

[11] X. Ren, P.K.L. Chan, J. Lu, B. Huang, D.C.W. Leung, High Dynamic Range Organic Temperature Sensor, *Adv. Mater.* **25**, 1291-1295 (2013).

[12] P. Lin, F. Yan, Organic Thin-Film Transistors for Chemical and Biological Sensing, *Adv. Mater.* **24**, 34-51 (2012).

[13] B. Radisavljevic, A. Radenovic, J. Brivio, V. Giacometti, A. Kis, Single-layer MoS2 transistors, *Nat. Nanotechnol.* **6**, 147-150 (2011).

[14] B. Radisavljevic, A. Kis, Mobility engineering and a metal–insulator transition in monolayer MoS2, *Nat. Mater.* **12**, 815-820 (2013).

[15] Y. Yoon, K. Ganapathi, S. Salahuddin, How Good Can Monolayer MoS2 Transistors Be?, *Nano Lett.* **11**, 3768-3773 (2011).

[16] O. Lopez-Sanchez, D. Lembke, M. Kayci, A. Radenovic, A. Kis, Ultrasensitive photodetectors based on monolayer MoS2, *Nat. Nanotechnol.* **8**, 497-501 (2013).

[17] F.K. Perkins, A.L. Friedman, E. Cobas, P.M. Campbell, G.G. Jernigan, B.T. Jonker, Chemical Vapor Sensing with Monolayer MoS2, *Nano Lett.* **13**, 668-673 (2013).

[18] D.J. Late, Y.-K. Huang, B. Liu, J. Acharya, S.N. Shirodkar, J. Luo, A. Yan, D. Charles, U.V. Waghmare, V.P. Dravid, C.N.R. Rao, Sensing Behavior of Atomically Thin-Layered MoS2 Transistors, *ACS Nano* **7**, 4879-4891 (2013).

[19] S. Kim, A. Konar, W.-S. Hwang, J.H. Lee, J. Lee, J. Yang, C. Jung, H. Kim, J.-B. Yoo, J.-Y. Choi, Y.W. Jin, S.Y. Lee, D. Jena, W. Choi, K. Kim, High-mobility and low-power thin-film transistors based on multilayer MoS2 crystals, *Nat. Commun.* **3**, 1011 (2012).

[20] R. Cheng, S. Jiang, Y. Chen, Y. Liu, N. Weiss, H.-C. Cheng, H. Wu, Y. Huang, X. Duan, Few-layer molybdenum disulfide transistors and circuits for high-speed flexible electronics, *Nat. Commun.* **5**, 5143 (2014).

[21] Z. Yin, H. Li, H. Li, L. Jiang, Y. Shi, Y. Sun, G. Lu, Q. Zhang, X. Chen, H. Zhang, Single-Layer MoS2 Phototransistors, *ACS Nano* **6**, 74-80 (2012).

[22] H. Li, Z. Yin, Q. He, H. Li, X. Huang, G. Lu, D.W.H. Fam, A.I.Y. Tok, Q. Zhang, H. Zhang, Fabrication of Single- and Multilayer MoS2 Film-Based Field-Effect Transistors for Sensing NO at Room Temperature, *Small* **8**, 63-67 (2012).

[23] S. Bertolazzi, D. Krasnozhon, A. Kis, Nonvolatile Memory Cells Based on MoS2/Graphene Heterostructures, *ACS Nano* **7**, 3246-3252 (2013).

[24] J. Wang, X. Zou, X. Xiao, L. Xu, C. Wang, C. Jiang, J.C. Ho, T. Wang, J. Li, L. Liao, Floating Gate Memory-based Monolayer MoS2 Transistor with Metal Nanocrystals Embedded in the Gate Dielectrics, *Small* **11**, 208-213 (2015).

[25] A. Kuc, N. Zibouche, T. Heine, Influence of quantum confinement on the electronic structure of the transition metal sulfide TS2, *Phys. Rev. B* **83**, 245213 (2011).

[26] K. Kaasbjerg, K.S. Thygesen, K.W. Jacobsen, Phonon-limited mobility in n-type single-layer MoS2 from first principles, *Phys. Rev. B* **85**, 115317 (2012).

[27] X. Wang, P. Wang, J. Wang, W. Hu, X. Zhou, N. Guo, H. Huang, S. Sun, H. Shen, T. Lin, M. Tang, L. Liao, A. Jiang, J. Sun, X. Meng, X. Chen, W. Lu, J. Chu, Ultrasensitive and Broadband MoS2 Photodetector Driven by Ferroelectrics, *Adv. Mater.* **27**, 6575-6581 (2015).

[28] D. Sarkar, W. Liu, X. Xie, A.C. Anselmo, S. Mitragotri, K. Banerjee, MoS2 Field-Effect Transistor for Next-Generation Label-Free Biosensors, *ACS Nano* **8**, 3992-4003 (2014).

[29] B. Liu, L. Chen, G. Liu, A.N. Abbas, M. Fathi, C. Zhou, High-Performance Chemical Sensing Using Schottky-Contacted Chemical Vapor Deposition Grown Monolayer MoS2 Transistors, *ACS Nano* **8**, 5304-5314 (2014).

[30] H. Wang, L. Yu, Y.-H. Lee, Y. Shi, A. Hsu, M.L. Chin, L.-J. Li, M. Dubey, J. Kong, T. Palacios, Integrated Circuits Based on Bilayer MoS2 Transistors, *Nano Lett.* **12**, 4674-4680 (2012).

[31] D. Kumaki, T. Umeda, S. Tokito, Influence of H2O and O2 on threshold voltage shift in organic thin-film transistors: Deprotonation of SiOH on SiO2 gate-insulator surface, *Appl. Phys. Lett.* **92**, 093309 (2008).

[32] W.H. Lee, H.H. Choi, D.H. Kim, K. Cho, 25th Anniversary Article: Microstructure Dependent Bias Stability of Organic Transistors, *Adv. Mater.* **26**, 1660-1680 (2014).

[33] D.J. Late, B. Liu, H.S.S.R. Matte, V.P. Dravid, C.N.R. Rao, Hysteresis in Single-Layer MoS2 Field Effect Transistors, *ACS Nano* **6**, 5635-5641 (2012).

[34] H. Qiu, L. Pan, Z. Yao, J. Li, Y. Shi, X. Wang, Electrical characterization of back-gated bi-layer MoS2 field-effect transistors and the effect of ambient on their performances, *Appl. Phys. Lett.* **100**, 123104 (2012).

[35] T. Li, G. Du, B. Zhang, Z. Zeng, Scaling behavior of hysteresis in multilayer MoS2 field effect transistors, *Appl. Phys. Lett.* **105**, 093107 (2014).

[36] A. Pezeshki, S.H. Hosseini Shokouh, S.R.A. Raza, J.S. Kim, S.-W. Min, I. Shackery, S.C. Jun, S. Im, Top and back gate molybdenum disulfide transistors coupled for logic and photo-inverter operation, *J. Mater. Chem. C* **2**, 8023-8028 (2014).

[37] X. Zou, J. Wang, C.-H. Chiu, Y. Wu, X. Xiao, C. Jiang, W.-W. Wu, L. Mai, T. Chen, J. Li, J.C. Ho, L. Liao, Interface Engineering for High-Performance Top-Gated MoS2 Field-Effect Transistors, *Adv. Mater.* **26**, 6255-6261 (2014).

[38] J. Roh, Study on interface engineering for organic thin film transistors: electrical performance and operational stability, *MSc Thesis ,Seoul National University* pp23-pp34 (2012).

[39] A. Hoppe, D. Knipp, B. Gburek, A. Benor, M. Marinkovic, V. Wagner, Scaling limits of organic thin film transistors, *Org. Electron.* **11**, 626-631 (2010).

[40] F. Ante, D. Kälblein, T. Zaki, U. Zschieschang, K. Takimiya, M. Ikeda, T. Sekitani, T. Someya, J.N. Burghartz, K. Kern, H. Klauk, Contact Resistance and Megahertz Operation of Aggressively Scaled Organic Transistors, *Small* **8**, 73-79 (2012).

[41] G. Ghibaudo, New method for the extraction of MOSFET parameters, *Electron. Lett.* **24**, 543-545 (1988).

[42] H.-J. Kwon, S. Kim, J. Jang, C.P. Grigoropoulos, Evaluation of pulsed laser annealing for flexible multilayer MoS2 transistors, *Appl. Phys. Lett.* **106**, 113111 (2015).

[43] J. Na, M. Shin, M.-K. Joo, J. Huh, Y. Jeong Kim, H. Jong Choi, J. Hyung Shim, G.-T. Kim, Separation of interlayer resistance in multilayer MoS2 field-effect transistors, *Appl. Phys. Lett.* **104**, 233502 (2014).

[44] H.-Y. Chang, W. Zhu, D. Akinwande, On the mobility and contact resistance evaluation for transistors based on MoS2 or two-dimensional semiconducting atomic crystals, *Appl. Phys. Lett.* **104**, 113504 (2014).

[45] F.R. Libsch, J. Kanicki, Bias-stress-induced stretched-exponential time dependence of charge injection and trapping in amorphous thin-film transistors, *Appl. Phys. Lett.* **62**, 1286-1288 (1993).

[46] J. Kim, S.H. Kim, T.K. An, S. Park, C.E. Park, Highly stable fluorine-rich polymer treated dielectric surface for the preparation of solution-processed organic field-effect transistors, *J. Mater. Chem. C* **1**, 1272-1278 (2013).

[47] K. Suemori, S. Uemura, M. Yoshida, S. Hoshino, N. Takada, T. Kodzasa, T. Kamata, Threshold voltage stability of organic field-effect transistors for various chemical species in the insulator surface, *Appl. Phys. Lett.* **91**, 192112-192113 (2007).

[48] N. Kaushik, A. Nipane, F. Basheer, S. Dubey, S. Grover, M.M. Deshmukh, S. Lodha, Schottky barrier heights for Au and Pd contacts to MoS2, *Appl. Phys. Lett.* **105**, 113505 (2014).

[49] Y. Wen, Y. Liu, Recent Progress in n-Channel Organic Thin-Film Transistors, *Adv. Mater.* **22**, 1331-1345 (2010).

[50] H. Usta, A. Facchetti, T.J. Marks, n-Channel Semiconductor Materials Design for Organic Complementary Circuits, *Acc. Chem. Res.* **44**, 501-510 (2011).

[51] Y. Zhao, Y. Guo, Y. Liu, 25th Anniversary Article: Recent Advances in n-Type and Ambipolar Organic Field-Effect Transistors, *Adv. Mater.* **25**, 5372-5391 (2013).

[52] S. Tatemichi, M. Ichikawa, T. Koyama, Y. Taniguchi, High mobility n-type thin-film transistors based on N,N′-ditridecyl perylene diimide with thermal treatments, *Appl. Phys. Lett.* **89**, 112108 (2006).

[53] J.H. Oh, P. Wei, Z. Bao, Molecular n-type doping for air-stable electron transport in vacuum-processed n-channel organic transistors, *Appl. Phys. Lett.* **97**, 243305 (2010).

[54] Y. Chung, E. Verploegen, A. Vailionis, Y. Sun, Y. Nishi, B. Murmann, Z. Bao, Controlling Electric Dipoles in Nanodielectrics and Its Applications for Enabling Air-Stable n-Channel Organic Transistors, *Nano Lett.* **11**, 1161-1165 (2011).

[55] S. Tanida, K. Noda, H. Kawabata, K. Matsushige, Ultrathin polymer gate buffer layer for air-stable, low-voltage, n-channel organic thin-film transistors, *Polym. Adv. Technol.* **21**, 528-532 (2010).

[56] F.-C. Chen, C.-H. Liao, Improved air stability of n-channel organic thin-film transistors with surface modification on gate dielectrics, *Appl. Phys. Lett.* **93**, 103310 (2008).

[57] J. Jang, S. Nam, W.M. Yun, C. Yang, J. Hwang, T.K. An, D.S. Chung, C.E. Park, High Tg cyclic olefin copolymer/Al2O3 bilayer gate dielectrics for flexible organic complementary circuits with low-voltage and air-stable operation, *J. Mater. Chem.* **21**, 12542-12546 (2011).

[58] J. Jang, S. Nam, D.S. Chung, S.H. Kim, W.M. Yun, C.E. Park, High Tg Cyclic Olefin Copolymer Gate Dielectrics for N,N′-Ditridecyl Perylene Diimide Based Field-Effect Transistors: Improving Performance and Stability with Thermal Treatment, *Adv. Funct. Mater.* **20**, 2611-2618 (2010).

[59] N. Ken-ichi, I. Motomi, Y. Masaaki, Improvement in Mobility and Stability of n-Type Organic Field-Effect Transistors with a Hole Transporting Interfacial Layer, *Applied Physics Express* **2**, 021501 (2009).

[60] Y. Zhang, H.-S. Seo, M.-J. An, J.-H. Choi, Perylrene-based n-type field-effect transistors prepared by the neutral cluster beam deposition method, *Org. Electron.* **10**, 895-900 (2009).

[61] H. Klauk, Organic thin-film transistors, *Chem. Soc. Rev.* **39**, 2643-2666 (2010).

[62] H.H. Choi, W.H. Lee, K. Cho, Bias-Stress-Induced Charge Trapping at Polymer Chain Ends of Polymer Gate-Dielectrics in Organic Transistors, *Adv. Funct. Mater.* **22**, 4833-4839 (2012).

[63] D. Kumaki, S. Ando, S. Shimono, Y. Yamashita, T. Umeda, S. Tokito, Significant improvement of electron mobility in organic thin-film transistors based on thiazolothiazole derivative by employing self-assembled monolayer, *Appl. Phys. Lett.* **90**, 053506 (2007).

[64] D.H. Kim, H.S. Lee, H. Yang, L. Yang, K. Cho, Tunable Crystal Nanostructures of Pentacene Thin Films on Gate Dielectrics Possessing Surface-Order Control, *Adv. Funct. Mater.* **18**, 1363-1370 (2008).

[65] K. Fukuda, T. Hamamoto, T. Yokota, T. Sekitani, U. Zschieschang, H. Klauk, T. Someya, Effects of the alkyl chain length in phosphonic acid self-assembled monolayer gate dielectrics on the performance and stability of low-voltage organic thin-film transistors, *Appl. Phys. Lett.* **95**, 203301 (2009).

[66] O. Acton, G.G. Ting, P.J. Shamberger, F.S. Ohuchi, H. Ma, A.K.Y. Jen, Dielectric Surface-Controlled Low-Voltage Organic Transistors via n-Alkyl Phosphonic Acid Self-Assembled Monolayers on High-k Metal Oxide, *ACS Appl. Mater. Interfaces* **2**, 511-520 (2010).

[67] I. Hill, C. Weinert, L. Kreplak, B. van Zyl, Influence of self-assembled monolayer chain length on modified gate dielectric pentacene thin-film transistors, *Appl. Phys. A: Mater. Sci. Process.* **95**, 81-87 (2009).

[68] T. Miyadera, S.D. Wang, T. Minari, K. Tsukagoshi, Y. Aoyagi, Charge trapping induced current instability in pentacene thin film transistors: Trapping barrier and effect of surface treatment, *Appl. Phys. Lett.* **93**, 033304 (2008).

[69] M. Hancer, The effect of humidity on the stability of octadecyltrichlorosilane for the self-assembled monolayer coating applications, *Prog. Org. Coat.* **63**, 395-398 (2008).

[70] S.R. Walter, J. Youn, J.D. Emery, S. Kewalramani, J.W. Hennek, M.J. Bedzyk, A. Facchetti, T.J. Marks, F.M. Geiger, In-Situ Probe of Gate Dielectric-Semiconductor Interfacial Order in Organic Transistors: Origin and Control of Large Performance Sensitivities, *J. Am. Chem. Soc.* **134**, 11726-11733 (2012).

[71] A.Y. Fadeev, T.J. McCarthy, Self-Assembly Is Not the Only Reaction Possible between Alkyltrichlorosilanes and Surfaces: Monomolecular and Oligomeric Covalently Attached Layers of Dichloro- and Trichloroalkylsilanes on Silicon, *Langmuir* **16**, 7268-7274 (2000).

[72] R. Anwander, I. Nagl, M. Widenmeyer, G. Engelhardt, O. Groeger, C. Palm, T. Röser, Surface Characterization and Functionalization of MCM-41 Silicas via Silazane Silylation, *J. Phys. Chem. B* **104**, 3532-3544 (2000).

[73] H. Yang, S.H. Kim, L. Yang, S.Y. Yang, C.E. Park, Pentacene Nanostructures on Surface-Hydrophobicity-Controlled Polymer/SiO2 Bilayer Gate-Dielectrics, *Adv. Mater.* **19**, 2868-2872 (2007).

[74] C. Kim, A. Facchetti, T.J. Marks, Gate Dielectric Microstructural Control of Pentacene Film Growth Mode and Field-Effect Transistor Performance, *Adv. Mater.* **19**, 2561-2566 (2007).

[75] C. Liu, Y. Xu, Y. Li, W. Scheideler, T. Minari, Critical Impact of Gate Dielectric Interfaces on the Contact Resistance of High-Performance Organic Field-Effect Transistors, *J. Phys. Chem. C* **117**, 12337-12345 (2013).

[76] P.A. Bobbert, A. Sharma, S.G.J. Mathijssen, M. Kemerink, D.M. de Leeuw, Operational Stability of Organic Field-Effect Transistors, *Adv. Mater.* **24**, 1146-1158 (2012).

[77] K. Cho, W. Park, J. Park, H. Jeong, J. Jang, T.-Y. Kim, W.-K. Hong, S. Hong, T. Lee, Electric Stress-Induced Threshold Voltage Instability of Multilayer MoS2 Field Effect Transistors, *ACS Nano* **7**, 7751-7758 (2013).

[78] J. Na, M.-K. Joo, M. Shin, J. Huh, J.-S. Kim, M. Piao, J.-E. Jin, H.-K. Jang, H.J. Choi, J.H. Shim, G.-T. Kim, Low-frequency noise in multilayer MoS2 field-effect transistors: the effect of high-k passivation, *Nanoscale* **6**, 433-441 (2014).

[79] W. Park, J. Park, J. Jang, H. Lee, H. Jeong, K. Cho, S. Hong, T. Lee, Oxygen environmental and passivation effects on molybdenum disulfide field effect transistors, *Nanotechnology* **24**, 095202 (2013).

[80] P.J. Jeon, S.-W. Min, J.S. Kim, S.R.A. Raza, K. Choi, H.S. Lee, Y.T. Lee, D.K. Hwang, H.J. Choi, S. Im, Enhanced device performances of WSe2-MoS2 van der Waals junction p-n diode by fluoropolymer encapsulation, *J. Mater. Chem. C* **3**, 2751-2758 (2015).

[81] S.-L. Li, K. Wakabayashi, Y. Xu, S. Nakaharai, K. Komatsu, W.-W. Li, Y.-F. Lin, A. Aparecido-Ferreira, K. Tsukagoshi, Thickness-Dependent Interfacial Coulomb Scattering in Atomically Thin Field-Effect Transistors, *Nano Lett.* **13**, 3546-3552 (2013).

[82] S. Namgung, S. Yang, K. Park, A.-J. Cho, H. Kim, J.-Y. Kwon, Influence of post-annealing on the off current of MoS2 field-effect transistors, *Nanoscale Res. Lett.* **10**, 62 (2015).

[83] W. Fenglin, S. Petr, G. Mason, L. Chun Ning, Annealing and transport studies of suspended molybdenum disulfide devices, *Nanotechnology* **26**, 105709 (2015).

[84] R. Yang, X. Zheng, Z. Wang, C.J. Miller, P.X.-L. Feng, Multilayer MoS2 transistors enabled by a facile dry-transfer technique and thermal annealing, *J. Vac. Sci. Technol. B* **32**, - (2014).

[85] S.-H. Choi, J.-H. Jang, J.-J. Kim, M.-K. Han, Low-Temperature Organic (CYTOP) Passivation for Improvement of Electric Characteristics and Reliability in IGZO TFTs, *IEEE Electron Device Lett.* **33**, 381-383 (2012).

[86] D.S. Chung, J.-S. Lee, J. Huang, A. Nag, S. Ithurria, D.V. Talapin, Low Voltage, Hysteresis Free, and High Mobility Transistors from All-Inorganic Colloidal Nanocrystals, *Nano Lett.* **12**, 1813-1820 (2012).

[87] J. Granstrom, J.S. Swensen, J.S. Moon, G. Rowell, J. Yuen, A.J. Heeger, Encapsulation of organic light-emitting devices using a perfluorinated polymer, *Appl. Phys. Lett.* **93**, 193304 (2008).

[88] S.-m. Seo, C.-H. Jang, J.-H. Park, Influence of passivation with non-charged fluorinated ethylene propylene on the properties of pentacene organic thin film transistor, *Org. Electron.* **9**, 899-902 (2008).

[89] S. Park, S. Nam, L. Kim, M. Park, J. Kim, T.K. An, W.M. Yun, J. Jang, J. Hwang, C.E. Park, Synthesis and characterization of a fluorinated oligosiloxane-containing encapsulation material for organic field-effect transistors, prepared via a non-hydrolytic sol–gel process, *Org. Electron.* **13**, 2786-2792 (2012).

[90] S.H. Han, J.H. Kim, J. Jang, S.M. Cho, M.H. Oh, S.H. Lee, D.J. Choo, Lifetime of organic thin-film transistors with organic passivation layers, *Appl. Phys. Lett.* **88**, 073519 (2006).

[91] H.-J. Kwon, J. Jang, S. Kim, V. Subramanian, C.P. Grigoropoulos, Electrical characteristics of multilayer MoS2 transistors at real operating temperatures with different ambient conditions, *Appl. Phys. Lett.* **105**, 152105 (2014).

[92] V. Derycke, R. Martel, J. Appenzeller, P. Avouris, Controlling doping and carrier injection in carbon nanotube transistors, *Appl. Phys. Lett.* **80**, 2773-2775 (2002).

[93] F. Colléaux, J.M. Ball, P.H. Wöbkenberg, P.J. Hotchkiss, S.R. Marder, T.D. Anthopoulos, Bias-stress effects in organic field-effect transistors based on self-assembled monolayer nanodielectrics, *Phys. Chem. Chem. Phys.* **13**, 14387-14393 (2011).

Publication

[1] International Journals

1. **J. Roh**, J.-H. Lee, S. H. Jin, and C. Lee, "Negligible hysteresis of molybdenum disulfide field-effect transistors by employing thermal annealing", *J. Inf. Disp.*, DOI: 10.1080/15980316.2016.1179688 (2016).

2. **J. Roh**, H. Roh, H. Shin, H. Kim, and C. Lee, "Organic complementary ring oscillators using a functional polymer interfacial layer for highly improved oscillation frequency", *Polym. Bull.*, DOI: 10.1007/s00289-016-1681-8 (2016).

3. J. Y. Kim, J. Kim, **J. Roh**, H. Kim, and C. Lee, "Efficiency improvement of organic photovoltaics adopting Li- and Cd-doped ZnO electron extraction layers", *IEEE J. Photovolt.* 6, 930 (2016).

4. H.-J. Song, **J. Roh,** and C. Lee, "Simultaneous engineering of the substrate temperature and mixing ratio to improve the performance of organic photovoltaic cells", *J. Nanosci. Nanotechnol.*, 16, 5104 (2016).

5. C.-m. Kang, J. Wade, S. Yun, J. Lim, H. Cho, **J. Roh**, H. Lee, S. Nam, D. D. C.

Bradley, J.-S. Kim, and C. Lee, "1-GHz pentacene diode rectifiers enabled by controlled film deposition on SAM-treated Au anodes", *Adv. Electron. Mater.* 2, 1500282 (2016). **Front Cover Paper**

6. **J. Roh**, I.-T. Cho, H. Shin, G. W. Baek, B. H. Hong, J.-H. Lee, S. H. Jin, and C. Lee, "Fluorinated CYTOP passivation effects on electrical reliability of multilayer MoS_2 field-effect transistors", *Nanotechnology*, 26, 455201 (2015).

7. **J. Roh**, C. Lee, J. Kwak, B. J. Jung, and H. Kim, "Vapor-phase-processed fluorinated self-assembled monolayer for organic thin-film transistors", *J. Korean Phys. Soc.* 67, 941 (2015).

8. J. Y. Kim, E. Cho, J. Kim, H. Shin, **J. Roh**, M. Thambidurai, C.-m. Kang, H.-J. Song, S. Kim, H. Kim, and C. Lee, "Improved photovoltaic performance of inverted polymer solar cells through a sol-gel processed Al-doped ZnO electron extraction layer", *Opt. Express* 23, 243417 (2015).

9. I.-T. Cho, J. I. Kim, Y. Hong, **J. Roh**, H. Shin, G. W. Baek, C. Lee, B. H. Hong, S. H. Jin, and J.-H. Lee, "Low frequency noise characteristics in multilayer WSe_2 field effect transistor", *Appl. Phys. Lett.* 106, 023504 (2015).

10. J.-W. Ha, Y. Kim, **J. Roh**, J. I. Park, J. Kwak, C. Lee, and D.-H. Hwang, "Thermally curable polymers consisting of alcohol-functionalized cyclotetrasiloxane and melamine derivatives for use as insulators in OTFTs", *Org. Electron.* 15, 3666 (2014).

11. J.-W. Ha, Y. Kim, **J. Roh**, F. Xu, J. I. Park, J. Kwak, C. Lee, and D.-H. Hwang, "Thermally curable organic/inorganic hybrid polymers as gate dielectrics for organic thin-film transistors", *J. Polym. Sci. Pol. Chem.*52, 3260 (2014).

12. C.-M. Kang, H. Cho, M. Park, **J. Roh**, and C. Lee, "Effects of insertion of hole injection layers on pentacene rectifying diodes", *J. Nanosci. Nanotechnol.* 14, 5301 (2014).

13. **J. Roh**, C.-m. Kang, J. Kwak, C. Lee, and B. J. Jung, "Overcoming tradeoff between mobility and bias stability in organic field-effect transistors according to the self-assembled monolayer chain lengths", *Appl. Phys. Lett.* 104, 173301 (2014).

14. Y. Kim, **J. Roh**, J.-H. Kim, C.-M. Kang, I.-N. Kang, B. J. Jung, C. Lee, and D.-H. Hwang, "Photocurable propyl-cinnamate-functionalized polyhedral oligomeric silsesquioxane as a gate dielectric for organic thin film transistors", *Org. Electron.* 14, 2315 (2013).

15. **J. Roh**, J. Lee, C.-m. Kang, C. Lee, and B. J. Jung, "Air stability of PTCDI-C13 based n-OFETs on polymer interfacial layers", *Phys. Status Solidi-Rapid Res. Lett.* 7, 469 (2013).

16. J. Y. Kim, S. Noh, Y. M. Nam, J. Y. Kim, **J. Roh**, M. Park, J. J. Amsden, D. Y. Yoon, C. Lee, and W. H. Jo, "Effect of nanoscale SubPc interfacial layer on the performance of inverted polymer solar cells based on P3HT/$PC_{71}BM$", *ACS Appl. Mater. Interfaces* 3, 4279 (2011).

[2] International Conferences

1. **J. Roh**, J. Song, J. Kim, and C. Lee, "Investigating light-induced degradation of amorphous polymers by employing transistor structure", International Conference of Synthetic Metal (ICSM), Guangzhou, China (Jun, 2016)

2. **J. Roh**, I.-T. Cho, J.-H. Lee, S. H. Jin, and C. LEE, "Bias-stress-induced instability of multilayer molybdenum disulfide field-effect transistors", Materials Research Society (MRS) spring meeting, Phoenix, USA (Mar, 2016).

3. **J. Roh**, H. Kim, and C. Lee, "Surface modification effect of SiO_2 dielectric on operational stability using buffer layer with various polarity in organic thin film transistors", The 3rd International Conference on Advanced Electromaterials (ICAE), Jeju, Korea (Nov, 2015).

4. **J. Roh**, I.-T. Cho, H. Shin, B. H. Hong, J.-Ho Lee, S. H. Jin, and C. Lee, "Highly stable hysteresis-free molybdenum disulfide field-effect transistors", The 15th International Meeting on Information Display (IMID), Daegu, Korea (Aug, 2015). ***Oral presentation, selected as an IMID 2015 awardee for KIDS awards gold (1st prize).***

5. **J. Roh**, H. Kim, H. Shin, H. Roh, J. Kwak, B. J. Jung, and C. Lee, "Effect of alkyl chain length of self-assembled monolayer on bias stability of organic thin film transistors", International Symposium on Flexible Organic Electronics (ISFOE), Thessaloniki, Greece (Jul, 2015).

6. **J. Roh**, C.-m. Kang, H. Shin, J. Kwak, B. J. Jung, and C. Lee, "Semiconductor-insulator interface engineering using self-assembled monolayer for organic field-effect transistors", The 14th International Meeting on Information Display

(IMID), Daegu, Korea (Aug, 2014). ***Oral presentation.***

7. **J. Roh**, C.-m. Kang, H. Shin, J. Kwak, B. J. Jung, and C. Lee, "Semiconductor-dielectric interface engineering for organic transistors using self-assembled monolayer", The 4th UK-KOREA Workshop on Plastic Electronics, Seoul, Korea (Jul, 2014). ***Oral presentation.***

8. **J. Roh**, C.-mo Kang, H. Shin, J. Kwak, B. J. Jung, and C. Lee, "n-type organic thin film transistors with high operational stability", The 52nd Society for Information Display (SID) Display Week, San Diego, USA, (Jun, 2014).

9. **J. Roh**, J. Lee, C.-m. Kang, B. J. Jung, and C. Lee, "Improved electrical performance and operational stability through interface engineering for organic thin film transistors", The 8th German-Korean Polymer Symposium, Hamburg, Germany (Aug, 2013). ***Invited talk.***

10. **J. Roh**, C.-m. Kang, H. Shin, J. Kwak, B. J. Jung, and C. Lee, "The effect of surface polarity of gate dielectric buffer layer on operational stability in organic thin film transistors", The 51st Society for Information Display (SID) Display Week, Vancouver, Canada (May, 2013).

11. **J. Roh**, C.-m. Kang, J. Kwak, B. J. Jung, and C. Lee, "Improved electrical performance and operational stability of organic thin film transistors by modifying insulator surface using low-*k* polymers", Materials Research Society (MRS) Fall meeting, Boston, USA (Nov, 2012).

12. **J. Roh**, C.-m. Kang, J. Kwak, B. J. Jung, and C. Lee, "Pentacene thin film transistors on fluorinated self-assembled monolayer-treated gate insulator and their gate bias stress effect", International workshop on flexible and printable

electronics (IWFPE), Muju, Korea (Nov, 2012).

13. **J. Roh**, M. Park, C.-m. Kang, H. Cho, and C. Lee, "Enhanced performance of all-solution-processed n-type organic thin film transistor by employing self-assembled monolayer", The 11th International Meeting on Information Display (IMID), Goyang, Korea (Oct, 2011).

한글 초록

전계효과 트랜지스터 (field-effect transistor, FET)는 현대 전자산업의 핵심이 되는 기초 소자이다. 전계효과 트랜지스터는 주로 스위치로써 사용되는데, 주된 응용분야 중 하나가 디스플레이를 구동하기 위한 백플레인이다. 오랜 시간 동안 실리콘을 기반으로 한 전계효과 트랜지스터가 디스플레이 구동을 위한 백플레인에 사용됐다. 하지만 디스플레이 산업이 급속하게 발전됨에 따라 차세대 디스플레이를 구동하기 위한 새로운 종류의 전계효과 트랜지스터 개발에 대한 요구가 증가하였다. 고해상도, 유연성, 투명성, 낮은 공정 가격, 다양한 응용분야에의 적용 등이 차세대 디스플레이의 특징이며, 이를 구동하기 위한 전계효과 트랜지스터 역시 이러한 특성을 만족시켜야 한다. 다양한 종류의 나노물질들이 전계효과 트랜지스터 응용을 위해 사용되었으며, 이중 유기물과 이차원 전이금속 칼코겐화합물 (tranisition metal dichalcogenides, TMDCs) 이 많은 관심을 받으며 연구되었다. 유기물의 경우 낮은 이동도, 이차원 전이금속 칼코겐화합물의 경우 대면적 적용과 같은 문제점들이 존재하였지만 최근 많은 연구를 통해서 해결되었다. 이들 물질을 이용한 전계효과 트랜지스터가 실제 차세대 디스플레이 구동을 위해 적용되기 위한 남은 과제로는 안정성 향상을 들 수 있다.

본 학위 논문에서는 유기물과 이차원 전이금속 칼코겐화합물을 기반으로 하는 전계효과 트랜지스터의 공기 중 안정성과 동작 안정성 향상에 관해 논하였다.

첫째로, 전기적으로 활성화 된 계면층 도입을 통한 유기 전계효과 트랜지스터 (organic field-effect transistors, OFETs)의 공기 중 안정성 향상에 관한 연구를 논하였다. N,N'-ditridecylperylene-

3,4,9,10-tetracarboxylic diimide (PTCDI-C13)를 기반으로 하는 n 형 유기 전계효과 트랜지스터가 제작되었고, 공기 중 안정성 향상을 위해 유기반도체와 절연체 사이에 계면층이 도입되었다. 계면층으로는 높은 유리 전이온도 (glass transition temperature, T_g) 를 가져 유기반도체의 열처리를 용이하게 해 주면서도 전자공여성이 강하여 계면 전하트랩을 줄일 수 있는 poly(9-vinylcarbazole) (PVK)가 사용되었다. PVK 계면층을 도입한 n 형 유기 전계효과 트랜지스터의 경우 0.61 $cm^2/V{\cdot}s$ 의 높은 초기 이동도가 관찰되었고, 공기 중 보관 4 일 후 초기 이동도의 90% 수준, 105 일 후 59% 수준을 유지함을 확인하였다. 전기공여성을 가지는 PVK 로 구성된 계면층이 계면 전하트랩을 줄여주고, 그 결과로 n 형 유기 전계효과 트랜지스터의 공기 중 안정성 향상을 이룰 수 있었다.

둘째로, 유기 전계효과 트랜지스터에서 자기조립 단분자막 (self-assembled monolayer, SAM) 처리를 통해 발생하는 이동도와 동작안정성 간의 트레이드오프 관계를 개선하는 연구에 대해 논하였다. 알킬 사슬의 길이 1 부터 8 을 가지는 4 가지 종류의 실라잔 SAM 을 도입하였고, 계면처리 결과 이동도는 SAM 알킬 사슬의 길이가 1, 3, 4, 8 로 길어짐에 따라 0.29 $cm^2/V{\cdot}s$ 에서 각각 0.46 $cm^2/V{\cdot}s$, 0.61 $cm^2/V{\cdot}s$, 0.65 $cm^2/V{\cdot}s$, 0.84 $cm^2/V{\cdot}s$ 로 증가함을 알 수 있었다. 반대로 동작 안정성의 경우 SAM 알킬 사슬의 길이가 길어짐에 따라 더 나빠지는 것을 확인할 수 있었다. 이러한 트레이드오프 관계를 해결하기 위하여 긴 알킬 사슬을 가지는 SAM 을 먼저 처리하고 짧은 알킬 사슬을 가지는 SAM 을 연속적으로 처리하는 2 단계 SAM 처리기술을 도입하였다. 2 단계 SAM 처리기술을 통해서 긴 알킬 사슬 SAM 을 처리하였을 때의 장점인 높은 이동도와 짧은 알킬 사슬 SAM 을 처리하였을 때의 장점인 우수한 동작 안정성을 모두 얻을 수 있었다.

마지막으로 전이금속 칼코겐화합물을 기반으로 하는 전계효과 트랜지스터의 안정성 향상에 관한 연구를 논하였다. 대표적인 전이금속

칼코겐화합물인 이황화몰리브덴 (molybdenum disulfide, MoS_2)을 기반으로 하는 전계효과 트랜지스터의 안정성 향상을 위해 CYTOP 패시베이션을 도입하였고, 패시베이션이 소자의 공기 중 안정성과 동작 안정성에 끼치는 영향을 조사하였다. 먼저, 패시베이션 이외의 다른 영향을 최소화하기 위하여 다중 어닐링 공정을 도입하여 무시할 정도의 작은 히스테리시스 (ΔV_{HYS}) 를 가지게 제작한 후 CYTOP 패시베이션을 적용하였다. 공기 중 안정성을 관찰하기 위하여 50 일 동안 공기 중에서 소자의 열화를 관찰하였고, 수명을 추출한 결과 CYTOP 패시베이션을 적용함에 따라 수명이 7 일에서 377 일로 급격히 향상됨을 확인하였다. 동작안정성 또한 평가되었으며 바이어스 스트레스에 따라 변하는 문턱전압을 스트레치드 지수함수 (stretched exponential function)를 이용하여 분석한 결과, 패시베이션을 적용하지 않은 소자가 CYTOP 패시베이션을 적용한 소자보다 약 25%의 더 넓은 전하트랩 장벽의 분포도를 가짐을 알 수 있었다. 이 연구를 통하여 CYTOP 패시베이션이 외부 가스 분자들을 효율적으로 막아줌으로써 이황화몰리브덴과 같은 저차원 물질을 사용한 전계효과 트랜지스터의 안정성을 크게 향상시킬 수 있음을 확인하였다.

본 논문은 유기물과 전이금속 칼코겐화합물을 기반으로 하는 전계효과 트랜지스터의 공기 중 안정성과 동작 안정성 향상에 관한 연구를 진행하였다. 전기적으로 활성화 된 계면층을 도입하여 n 형 유기 전계효과 트랜지스터의 공기 중 안정성을 향상시켰으며, 2 단계 SAM 처리를 도입하여 높은 이동도와 향상된 동작 안정성을 가지는 유기 전계효과 트랜지스터를 제작하였다. 또한 다중 어닐링을 도입하여 히스테리시스가 없는 이황화몰리브덴 전계효과 트랜지스터를 만든 후 CYTOP 패시베이션이 소자 안정성에 끼치는 영향을 체계적으로 분석하였다. 본 연구에서 제시된 계면처리 기술은 유기물, 전이금속 칼코겐화합물을 기반으로 하는 다른 나노 전자소자의 안정성 향상을 위해 사용될 수 있을 것이다.

주요어: 전계효과 트랜지스터, 유기반도체, 전이금속 칼코겐화합물, 계면 처리기술, 안정성

학번: 2012-30935