Ph.D. DISSERTATION

A STUDY ON BROADBAND GAN PHEMT POWER AMPLIFIER USING NON-FOSTER MATCHING

비 포스터 정합을 이용한 광대역 GaN pHEMT 전력증폭기에 관한 연구

BY

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SCHOOL OF ELECTRICAL ENGINEERING AND
COMPUTER SCIENCE COLLEGE OF ENGINEERING
SEOUL NATIONAL UNIVERSITY

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지도 교수 서 광 석

이 논문을 공학박사 학위논문으로 제출함

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이 상 호

이상호의 박사 학위논문을 인준함

2017 년 2 월

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Abstract

In this thesis, a study on broadband GaN pHEMT power amplifier (PA) using non-Foster matching is presented.

A watt-level PA with multi-octave bandwidth is required for broadband applications such as jamming system for electronic warfare (EW). To guarantee the high power operation, GaN device is suitable due to its high power density and high voltage operation. Therefore, in this thesis, the high PAs are fabricated through a GaN device. For broadband operation, a new wideband PA structure with high gain and high efficiency is proposed. The new broadband PA using non-Foster circuit (NFC) is referred to as a negative impedance matched power amplifier (NMPA).

The bandwidth limitation from high-Q interstage matching is overcome through the use of negative capacitor, which is realized with a negative impedance converter (NIC) using the cross-coupled GaN FETs. However, since the negative impedance transducer also has a frequency limit, the following design strategy has been established. For high power operation over the entire bandwidth, the natural interstage matching is optimized for the upper sub-frequency band and the lower sub-frequency band is compensated by the negative capacitance (NC) presented by NFC. For this strategy, detailed analysis is performed to understand the

frequency limitation of NIC approach, which shows that high-frequency limit comes from the self-resonance and the low-frequency limit from the power handling capability.

Besides, to overcome the frequency and power limits of NFC, a cascaded stage negative impedance converter (CSNIC) structure is proposed with improved positive loop gain. In addition, the cause of the NIC loss at the high frequency is also analyzed and solved using CSNIC.

Two NMPAs with NIC and a NMPA with CSNIC are fabricated with commercial 0.25-μm GaN pHEMT process. The implemented PA with 2× combining shows the output powers of 35.7-37.5 dBm with the power added efficiencies (PAEs) of 13-21% from 6 to 18 GHz. The 4× combining PA achieves over 5 W output power from 7 to 17 GHz. The NMPA with CSNIC shows the output powers of 7.6-10.4 W with the PAEs of 16-23% from 7 to 18 GHz. At frequencies, where NFC is optimized for interstage matching, the power improvement by 1.2 dBm and PAE improvement by 5.7% have been achieved. The NFC boosts the efficiencies and power below 12 GHz to achieve broadband performance without using any lossy matching or negative feedback. This work also demonstrates that the CSNIC overcomes the frequency and power capability limit of the conventional NIC.

To our knowledge, this is the first demonstration of NIC-based broadband amplifiers with Watt-level output power. The NMPA can

provide a new perspective in designing the broadband PAs.

Keyword : cascaded stage negative impedance converter (CSNIC), GaN, negative capacitance (NC), negative impedance converter (NIC), non-Foster circuit (NFC), power amplifier (PA), negative impedance matched power amplifier (NMPA),

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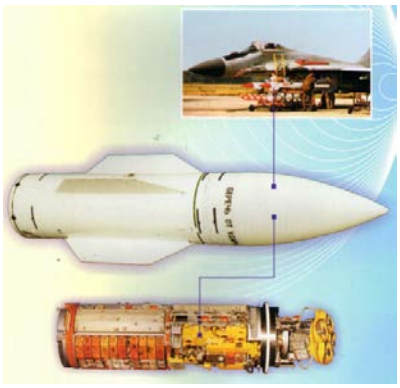
Chapter 1

Introduction

1.1. Motivation

Since the Second World War, the importance of electronic warfare (EW) has become increasingly important in modern warfare. EW includes several actions that use the electromagnetic spectrum. EW can be divided into electronic attack (EA), electronic protection, and electronic support. The typical action of EA is jamming and it is used in communications systems or radar systems. The active electronically scanned array (AESA) radar is a typical example, and the radar missile seeker, the tracking radar, and the improvised explosive device (IED) are subjects of jamming (Fig. 1.1). The jamming at long distances requires a high output power signal, and broadband frequency operation is required because the object operates at unknown frequencies.

(a)



(b)

(c)

Fig. 1.1. Photograph of (a) the AESA radar, (b) the radar missile seeker, and (c) the IED.

The MMIC is a core component of the radar system and the jamming system, but the drawback is that the output power of the solid state power amplifier (PA) is relatively weak compared to the traveling wave tube. Although compound semiconductors, such as GaAs pHEMT, are widely used for military applications, they are not sufficient for obtaining high power to constitute a jamming system. On the other hand, GaN device is suitable for this application due to its high power density and high voltage operation.

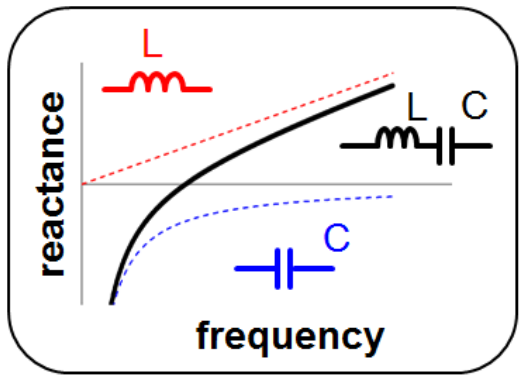
TABLE 1.1

Performance Comparison of Si, GaAs, and GaN Device

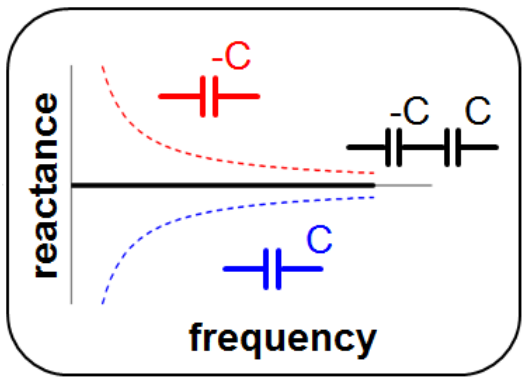
Property	Si	GaAs	GaN
Energy Gap (eV)	1.11	1.43	3.4
Critical Electric Field (MV/cm)	0.3	0.5	3.5
Charge Density ($x10^{13}/cm^2$)	0.3	0.3	1
Mobility ($Cm^2/V/s$)	1350	8000	1500
Saturation velocity ($x10^7$ cm/V)	1	1.4	2.7

Table 1.1 compares the performance of GaN devices with Si and GaAs. GaN devices have high breakdown voltage due to its high energy gap and critical electric field properties. Therefore, high voltage operation over 28 V is possible. Although there are problems such as thermal and trap effects, it is the best device to implement a high PA because other performance such as mobility and saturation velocity is not inferior. Therefore, in this thesis, all PAs are fabricated using GaN pHEMT devices.

However, designing a broadband PA is also very difficult. The output power and efficiency of a broadband PA are inferior to those of a narrowband PA. Fortunately, because GaN devices can operate with high voltage, it is advantageous to match the optimum load



(a)



(b)

Fig. 1.2. Basic concepts of (a) L-C resonance matching, (b) non-Foster matching.

impedance of the transistor (TR) in multi-octave bandwidth. Of course, simply using a GaN device cannot design a broadband PA and requires a special PA structure. The distributed amplifier (DA) and the reactive matched power amplifier (RMPA) are commonly used topology for multi-octave PA. However, DAs suffer from small gain and RMPAs suffer from low efficiency. In this thesis, a new wideband PA structure with high gain and high efficiency using non-Foster circuit (NFC) is proposed.

To achieve broadband characteristics, it is important to reduce

the Q-factor. NFC can be used to implement the negative capacitance (NC). Fig. 1.2 shows that using NC can reduce the reactance of a capacitor to broadband, unlike using an inductor. Therefore, the use of NFC can reduce the Q-factor without additional lossy network. The first NFC was using the TRs proposed about 60 years ago. Many circuits using NFC have been announced, but so far they have been mostly applied to low frequency and small signal applications. This is because the NFC has a frequency limit and a power handling capability limit. In this thesis, NFC was applied to high frequency (X-band) and large-signal (PA) applications. The new broadband PA designed using NFC is called negative impedance matched power amplifier (NMPA).

1.2. Outline of This Thesis

This thesis is composed of three sections. In the first section, chapter 2, the researches on two-stage GaN PAs using NFC for broadband operation ranging from 6 to 18 GHz are presented. It contains the overall design concept of the NMPA and the operation principle of the NFC. The NFC realized with the cross-coupled GaN FETs is applied to the interstage matching to cancel out the large input capacitance of the power-stage FETs. The frequency and power limits of NFC, and the detailed NFC-based PA circuit design methodology are included. This is the first demonstration of negative impedance converter (NIC) based broadband amplifiers with Watt-level output power. The noise figure of the PA is also added to understand the impact of NIC of the noise performance of the amplifier.

In chapter 3, more detailed small-signal analysis to understand the high frequency limitation of the NIC is presented. In addition, the large-signal behavior of the NIC is analyzed by using the full nonlinear GaN FET models. The combined results of small- and large- signal analyses are used to find the optimum TR size and bias points to extend the operation frequency and power range of the NIC. These are extended analysis of chapter 2 and another NMPA with higher output power and more effective NIC is presented.

In chapter 4, the improved NFC structure “Cascaded stage negative impedance converter (CSNIC)” is presented that can solve all the NFC problems of self-resonating frequency (SRF), loss, and power handling capability. The main causes of the limitations of NFC and conditions for obtaining broadband NC are analyzed. The CSNIC is designed using cascaded gain cell structure and compared with the characteristics of conventional NIC. In addition, the technique to reduce the loss of NFC is analyzed and low-loss NFC is implemented through CSNIC structure. Finally, GaN broadband NMPA with CSNIC is implemented. ,

Chapter 2

A 6-18 GHz GaN pHEMT Power Amplifier Using Non-Foster Matching

2.1. Introduction

A watt-level PA with multi-octave bandwidth is required for broadband applications such as EW system. GaN device is suitable for this application due to its high power density and high voltage operation, which results in relatively large load impedance. The DA is a commonly used topology for multi-octave PA (Fig. 2.1 (a)). The input and output capacitances are absorbed into the artificial transmission line to overcome the frequency limitation. However, DAs suffer from small gain and requires a relatively large die area.

The RMPAs are also widely used as multi-octave PAs (Fig. 2.1 (b)). RMPAs utilize a multiple-stage design to realize high gain.

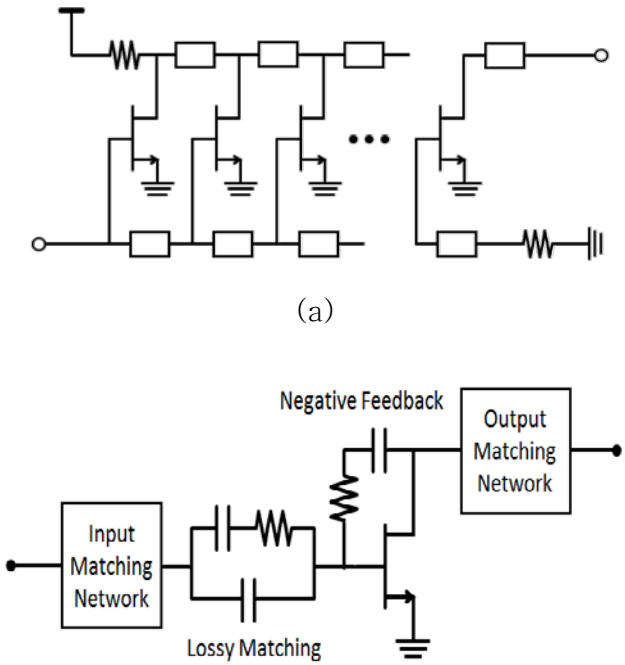


Fig. 2.1. Multi-octave PA structures of (a) DA and (b) RMPA

However, it has the bandwidth problem coming from Bode-Fano criterion [1]. To achieve broadband characteristics, lossy matching and negative feedback method are used to lower the Q-factor. This results in low efficiency and requires large chip size and has difficulty in achieving the required gain flatness over a wide bandwidth.

Reconfigurable matching concept has also been proposed for multi-stage PAs to overcome the bandwidth limitation coming from Bode-Fano criteria in the interstage matching [2], [3]. However, the overall PA efficiency may be degraded due to the switch loss. Moreover, the linearity and power handling capability of the switch may limit its use for multi Watt-level PAs.

A potential alternative for wideband matching is the use of a NFC. Typical examples of non-Foster components are the negative inductors and negative capacitors. On the Smith chart, S-parameter traces of the non-Foster components move in counter-clockwise direction as the frequency increases. The first NFC using the TRs was proposed by Linvill in 1954 [4]. The NFC was used to compensate for the parasitic effects of various circuits such as filters, varactors and VCOs [5]. For example, the negative slope of the reactance versus frequency is used to overcome the limitation of the antenna size and Q-factor at 800 MHz [6]. The gain-bandwidth enhancement of DA has been demonstrated using the NC in [7]. However, its application was limited to small-signal operation. Although the non-Foster matching is effective in cancelling out the reactance over a broad bandwidth, there are three major challenges using NFC, noise, stability and power handling capability. Due to the power handling issues, little work has been presented to demonstrate a broadband PA using NFC.

In this chapter, a 5 W 6-18 GHz GaN PA has been developed using NFC in the interstage matching to achieve multi-octave power bandwidth. The NFC realized with the cross-coupled GaN FETs to cancel out the large input capacitance of the power-stage FETs.

2.2. Interstage Matching with NFC

A simplified block diagram of the two-stage GaN PA with the proposed NFC is shown in Fig. 2.2. The unit FET size of the PA is $6\times125\ \mu m$, which has a maximum available gain of 12 dB at 18 GHz. To achieve overall gain higher than 15 dB, a two-stage design is required, in which case the bandwidth limitation often comes from the high-Q interstage matching rather than the output matching. If the driver load impedance is different from the optimum impedance, the power delivered to the power-stage is not sufficient. In this case, even if the output load impedance is optimum, high output power cannot be obtained. In this work, the NFC is employed in the interstage matching to cancel out the large input capacitance of the power-stage FETs, lowering the Q-factor of interstage matching.

The output matching is composed of a conventional two-section matching network and the output powers from each FET are combined through a Wilkinson power combiner to achieve 36-dBm output power over the target frequency range of 6-18 GHz. In theory, the addition of NFCs in the output matching network can further improve the power bandwidth. However, the power handling capability of NFC has to scale with the RF power, which increases the DC power consumption of NFC and degrades the power added efficiency (PAE) of the overall PA. Therefore, in this work, NFC is employed in the interstage matching only.

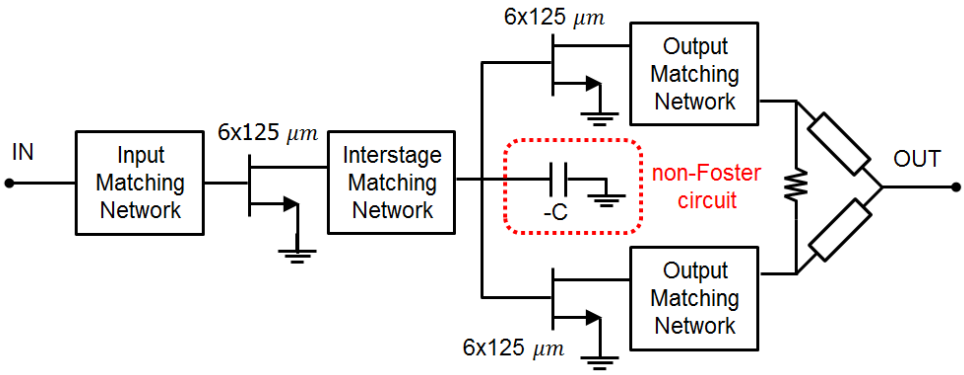


Fig. 2.2. Block diagram of the two-stage PA with non-Foster matching network.

Another practical issue with NFC is the limited operating frequency; the bandwidth limitation comes from the SRF, which is limited by f_T of the device. GaN FETs have a gate length of 0.25 μm and the NFC using these FETs show self-resonance around 11 GHz, which is not high enough to cover the entire bandwidth up to 18 GHz. So, the interstage matching network is optimized separately for two sub-frequency regions. Natural interstage matching is optimized for the upper sub-frequency band above 11 GHz, where the NC is not available. The subsequent power mismatch in the lower sub-frequency band is compensated by the NC presented by NFC.

To better understand the benefit of NFC in the interstage matching, the input impedance of the power stage is simulated together with the optimum load impedance of the driver-stage FET

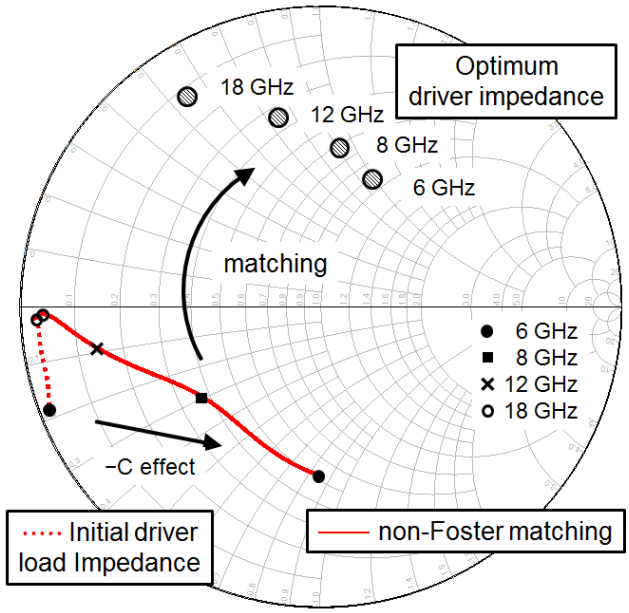


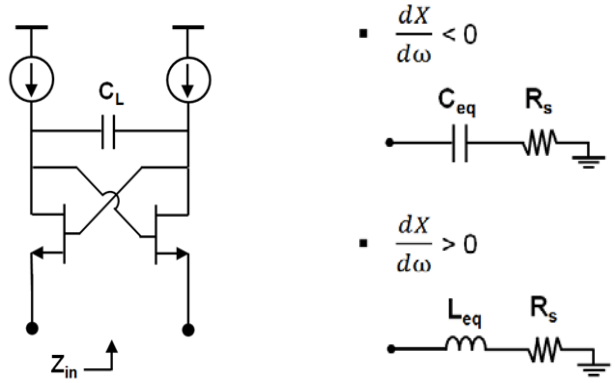
Fig. 2.3. Simulated interstage impedance matching with NFC.

in Fig. 2.3. The optimum driver-stage impedance moves along a constant-g circle in counter-clockwise direction as the frequency increases. The input impedance of the power stage is highly capacitive due to the large input gate capacitance of 1.4 pF. It is thus very difficult to provide optimum impedance matching across the entire bandwidth. Upper frequencies above 11 GHz are matched using an inductive line and shunt stubs. The impedance mismatch in the lower frequency sub-band is solved by employing a negative shunt capacitance of -2.5 pF, which basically reduces the Q-factor of the input impedance of the power stage impedance from 10.30 to 1.62 at 6 GHz and 4.39 to 0.78 at 8 GHz. In this way, the same matching circuit consisting of the inductive line and the shunt

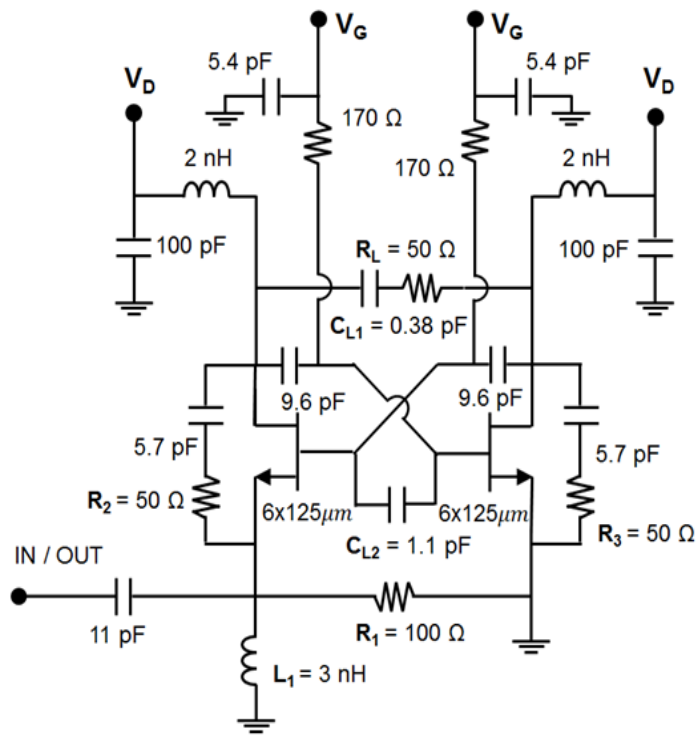
inductance can be used to match the lower sub-band frequencies below 11 GHz as well.

2.3. Non-Foster Circuit

The NFC used in the interstage matching is based on the Linvill's NIC (Fig. 2.4 (a)). The NIC is composed of the cross-coupled FETs with capacitors, resistors and inductors. The detailed circuit schematic of NFC is shown in Fig. 2.4 (c). The cross coupled FETs used in the NFC are 6×125 μm GaN FETs. The resistor R_1, R_2, and R_3 are used to prevent instability. R_L helps to reduce the equivalent series resistance, R_s, due to the impedance inversion effect of the cross-coupled pair. The main operation of the NIC is to invert the polarity of C_L to an effective capacitance, C_{eq} ($= -k C_L$). The coefficient, k, is a function of the frequency since the actual equivalent circuit is much more complicated than a simple capacitor; it is composed of series and parallel resistances, parasitic capacitances and inductances, which cannot be neglected at microwave frequencies. For analysis, it is useful to represent the NIC with a simplified equivalent circuit of a series resistor (R_s) and either NC (C_{eq}) or inductance (L_{eq}), depending on the frequency, as shown in Fig. 2.4 (b).



(a) (b)



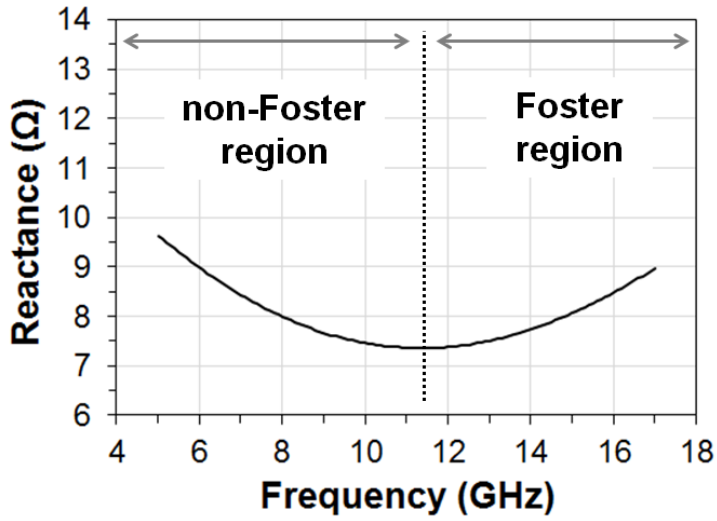
(c)

Fig. 2.4. (a) Linvill's NIC block diagram, (b) the simplified equivalent of the NIC, and (c) the detailed schematic of the proposed NIC

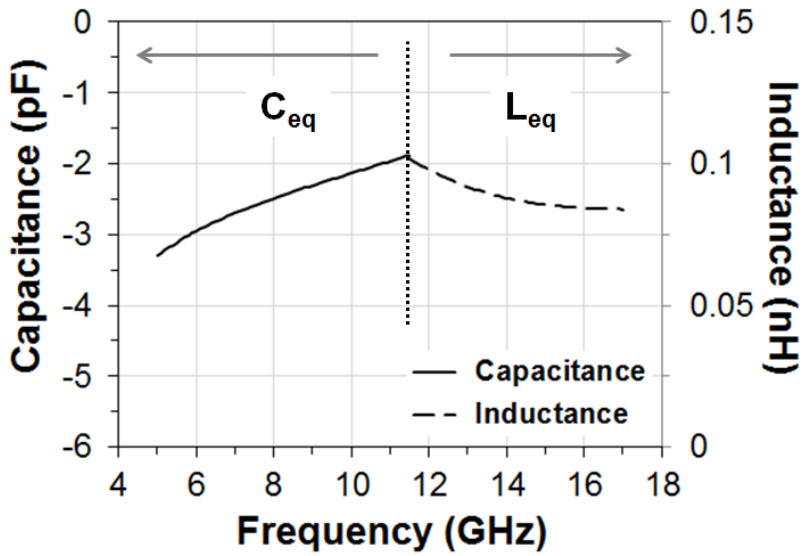
2.4. The limitation of Non-Foster Circuit

2.4.1. High Frequency Limit

The simulated frequency-dependent reactance of the NFC is plotted in Fig. 2.5. The reactance decreases as the frequency increases up to 11 GHz, which clearly shows non-Foster characteristics. The equivalent capacitances of the NFC in this frequency range are -3 ~ -2 pF. The equivalent series resistance varies between 4.4 and 11.4 Ω. Above 11 GHz, where the self-resonance occurs, the positive reactance slope is observed and the circuit follows Foster's theorem. In this case, the NFC is represented with a series combination of a resistance and a positive inductance as shown in Fig. 2.4 (b).



(a)



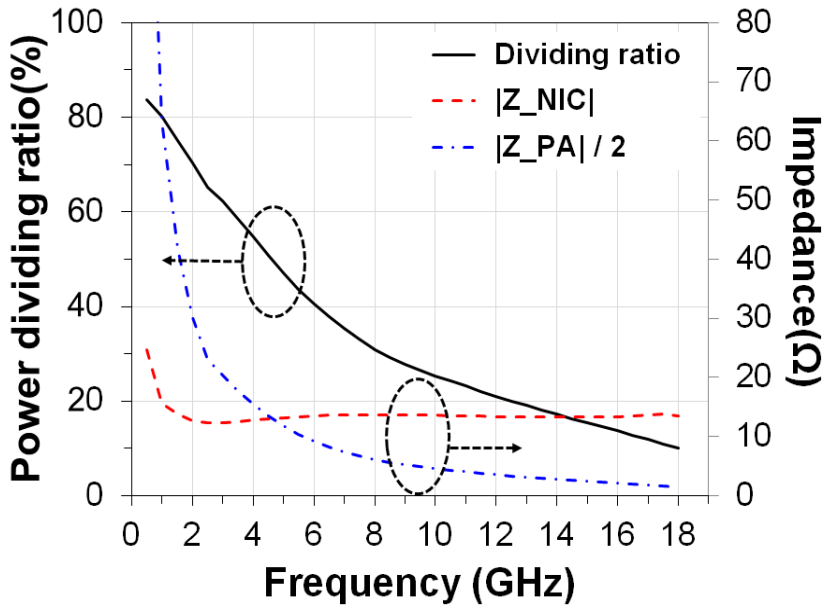
(b)

Fig. 2.5. Simulated (a) reactance of the NIC as a function of frequency and (b) equivalent capacitance or inductance.

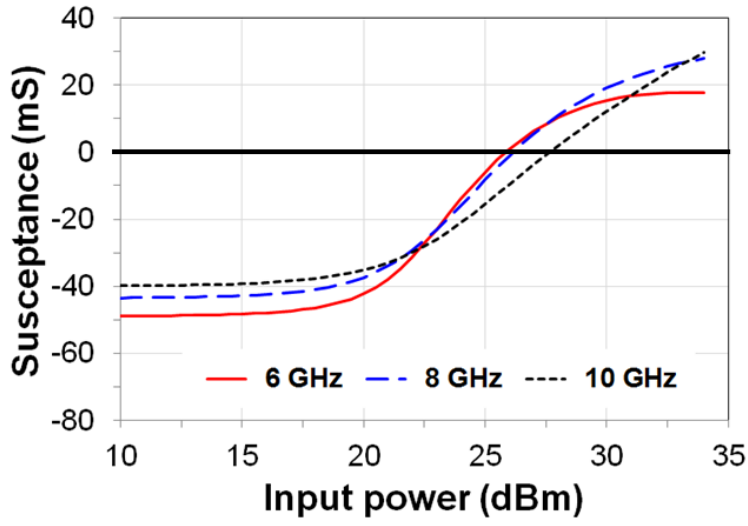
2.4.2. Low Frequency Limit

Another limitation in NFC operation may come from the power handling capability in the PAs. The NFCs cease to show negative impedance when they are driven with large RF power. As shown in Fig. 2.2, NFC shares the same node as the power-stage FETs. The RF power from the driver stage is divided into three paths with a different division ratio depending on the operating frequencies. Fig. 2.6 (a) shows the simulated power division ratio into the NFC versus the power FETs as a function of frequency. As the frequency decreases, more power is delivered to the NFC than to the power stages, which eventually reduces the loop gain in the NFC below a threshold level required to generate the negative impedance.

The delivered power to the NFC is not consumed but exists in the form of a standing wave. Like the power dividing ratio, the impedance of the NIC and PA increases as the frequency decreases. Therefore, the voltage swing of the standing wave also increases and the reduced loop gain of NFC comes from excessive voltage swing.



(a)



(b)

Fig. 2.6. (a) Simulation results of the power division ratio between the NIC and power stages. (b) Simulated susceptance of the NIC versus injected RF power.

To show the power handling capability, we have simulated the large-signal response of the NFC with 15 V drain voltage (Fig. 2.6 (b)). The negative susceptance, which is required to cancel out the positive susceptance due to the large power-stage input capacitance, decreases rapidly as the power increases. If the output power is 5 W and the power gain of the main stage is 3 dB, then the expected power delivered to the NFC is 1 W at 6 GHz. It is sufficient to cease the effect of NFC. Combining the results of Fig. 2.6 (a) and Fig. 2.6 (b), it is predicted that the low frequency operation of the NFC is vulnerable to large-signal operation. So, it is expected that the effective frequency range of the NIC in our PA is limited to 6-11 GHz, corresponding to the previously mentioned "lower-frequency sub-band".

2.5. Measurement Results

A two-stage broadband PA with the proposed NFC is fabricated using a commercial 0.25-μm GaN pHEMT foundry process. The tests were performed by RF probe under continuous wave conditions and a test fixture with eutectic bonding was used for mitigating the self-heating of the PA. The test fixture was composed of a 5-mm-thick Au-plated Cu carrier and heat sink with thermal grease.

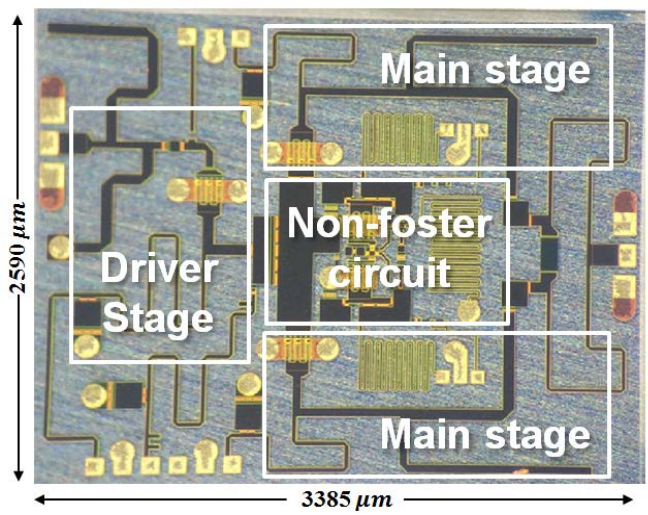
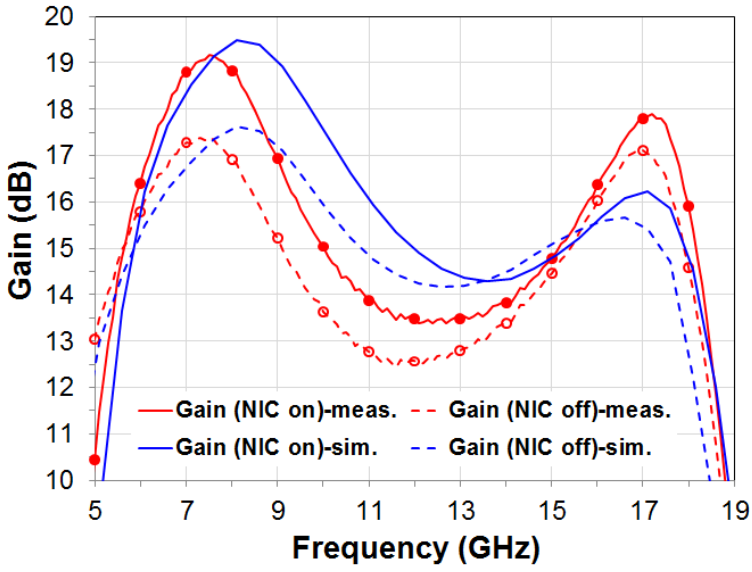


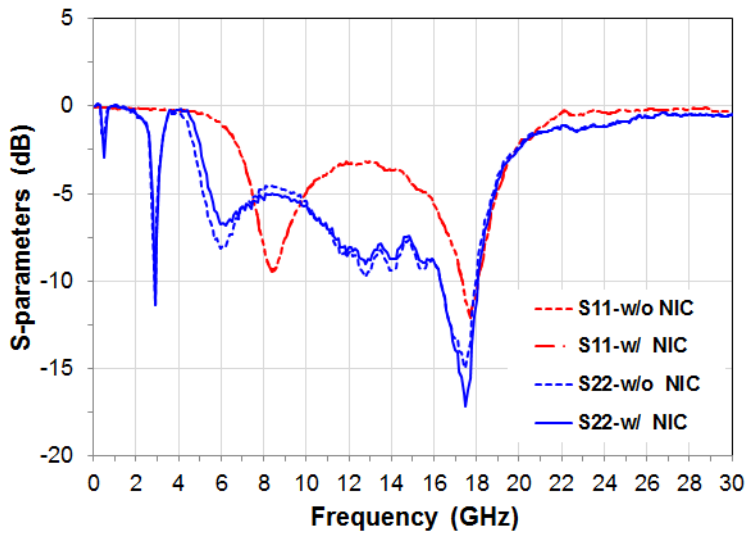
Fig. 2.7. Fabricated chip photograph of the PA with NIC.

2.5.1. PA with 2× Combining

Fig. 2.7 is the die photograph of the fabricated PA. As a reference, we have also tested the PA without NIC. The drain bias



(a)



(b)

Fig. 2.8. (a) Measured small-signal gain of 2× combined PA with and without the NIC. (b) Measured return losses of 2× combined PA with and without the NIC.

voltage to the PA is 28 V while that to the NIC is 15 V. Fig. 2.8 (a) shows the measured small-signal gain with and without the NIC. To

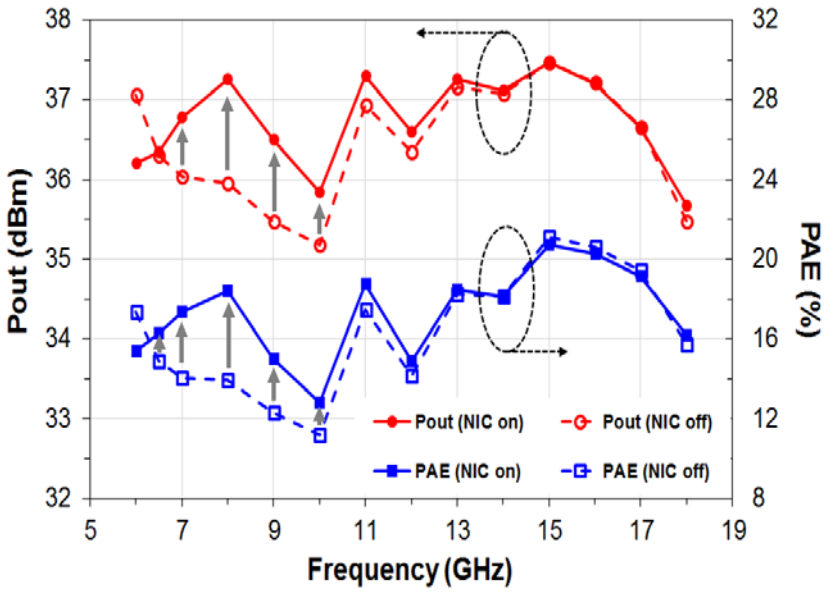


Fig. 2.9. Measured performance of 2× combined PA with and without the NIC.

show the effect of NIC on the return losses, S_{11} and S_{22} are also measured in Fig. 2.8 (b) with NIC turned on and off. Although the S_{11} and S_{22} remain almost same with and without the NIC, S_{21} increases by up to 2 dB in the lower-frequency sub-band from 6 to 11 GHz with the NIC. More meaningful improvement can be observed in the power characteristics (Fig. 2.9) since NIC-based interstage matching circuit is designed to provide the optimum load impedance to the driver stage in the lower-frequency sub-band. With the NIC, the output power and PAE improves by up to ~ 1.2 dB and ~ 4 %, respectively, between 6 and 11 GHz. For example, at 8 GHz, the output power is increased from 36 to 37.3 dBm and the PAE is improved by 4.5 %. The peak PAE of 13-21 % and the

output power of 35.7−37.5 dBm are achieved across the 6−18 GHz frequency bandwidth. The overall PAE degradation due to the power consumption of NIC is estimated to be ~ 1.5 %.

2.5.2 Noise Performance of NIC

The effect of NIC on the noise performance is also measured in Fig. 2.10. At the frequencies where the overall gain improves with NIC, the noise figure also improves. The noise is not analyzed separately because it is outside the scope of this thesis. However, the noise data of the NFC will be meaningful in receiver or antenna application area.

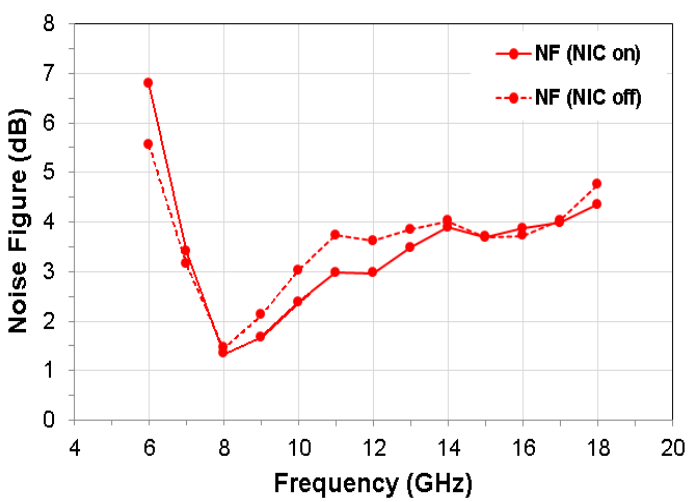


Fig. 2.10. Measured noise figure of 2× combined PA with and without the NIC.

2.5.3 Comparison Table

Table 2.1 compares the performance of our PA with the state-of-the-art DA and RMPA using GaN pHEMTs. As the first demonstration of the NMPA, the results are promising even though they do not match the best reported power and PAE data. One thing to note is that the overall die size was much smaller than the previous work since NIC implementation was possible in a very small die size, and no lossy matching or feedback was required in our work.

TABLE 2.1

Performance Comparison of GaN Broadband PAs

Ref.	Freq (GHz)	Topology	Process	PAE (%)	Pout (W)	Gain (dB)	Area (mm^2)
[8]	2-18	DA	0.25-μm GaN	20-38	9-15	10-14	15.3
[9]	2-20	DA	0.2-μm GaN	15-36	9.9-21.6	9-15	38
[10]	6-18	RMPA	0.25-μm GaN	14-24	3.2-20	17-28	19.25
[11]	6-18	RMPA	0.25-μm GaN	13-25	6-10	18-24	19.8
This work	**6-18**	**NMPA**	**0.25-μm GaN**	**13-21**	**3.7-5.6**	**13.5-19.1**	**8.77**

2.6. Conclusion

In this chapter, a non-Foster matched GaN PA has been developed for multi-octave PA operation. The bandwidth limitation due to high-Q matching has been mitigated through the use of a NC in the interstage matching. Detailed analysis is performed to understand the frequency limitation of NIC approach, which shows that high-frequency limit comes from the self-resonance and the low-frequency limit from the power handling capability. A 6-18 GHz PA fabricated with 0.25-μm GaN pHEMT process shows the maximum output power reaching 37.5 dBm with 21% PAE at 15 GHz. The NIC boosts the efficiencies and power below 11 GHz to achieve broadband performance without the use of any lossy matching circuits or negative feedback. To our knowledge, this is the first demonstration of NIC-based broadband amplifiers with Watt-level output power.

Chapter 3

A Broadband NMPA with Higher Output Power and Detailed Analysis for NFC

3.1. Introduction

Although the NMPA is successfully implemented in the previous chapter, more power is required to use it in the jamming system. Also, since NMPA is the first attempted technique, there is a need to optimize it. In particular, since the frequency and power capability limits are interrelated, the NFC should be able to operate in high power and high frequency operation at the same time.

First of all, the overall design procedure of NMPA should be established. The NFC has been in development for over 60 years, and there are many advantages and disadvantages [12]. Since a positive feedback loop gain is basically used, many studies on

stability have been carried out [13], and analysis of noise characteristics for application to an antenna is also a very important issue of NFC [14][15]. The NMPA has a special structure to mitigate high-Q matching by applying NFC to the interstage as a shunt connection. Therefore, NFC topology suitable for NMPA should be analyzed and selected.

Second, more accurate modeling of NFC is needed. Since existing NFCs operate mainly at low frequencies, a simple model was sufficient, but more detailed modeling is required at high frequencies.

Third, it is necessary to analyze the small-signal and large-signal characteristics of the NFC. As mentioned in the previous chapter, the high frequency limit of NFC comes from small-signal analysis, which is directly related to the operating bandwidth of the NFC. Not only does the low frequency limit of NFC come from large-signal analysis, to improve the power performance of the NMPA, the power capability of the NFC should be maximized

In this chapter, two-stage GaN NMPA has been developed with higher output power for broadband operation ranging from 7 to 17 GHz. This chapter presents more detailed small-signal analysis to understand the high frequency limitation of the NIC. In addition, the large-signal behavior of the NIC is analyzed by using the full nonlinear GaN FET models. The combined results of small- and large- signal analyses are used to find the optimum TR size and

bias points to extend the operation frequency and power range of the NIC.

3.2. Two-stage GaN PA with NFC

3.2.1. Overall Design Procedure of NMPA

A simplified block diagram of the two-stage GaN PA with the proposed NFC is shown in Fig. 3.1. The GaN FET with a size of 6×125 μm shows a cut-off frequency (f_T) of 21.7 GHz, an f_{max} of 74.6 GHz, and a trans-conductance (G_m) of 227 mS/mm at 28 V drain bias. The load-pull measurement on a 6×125 μm FET cell shows a maximum output power density of 2.8 W/mm, a PAE of 41.6%, and a power gain of 9.3 dB at 15 GHz under continuous wave conditions. Even though the TR performance merits do not match those of the state-of-the-art GaN TRs [8][9][10], the concept of NIC-based PA can be proven by comparing the PA performance with and without NICs.

For wide bandwidth, lowering the Q-factor of interstage matching network is essential. Since Q-factor is the ratio between the stored energy and power loss, it can be reduced by increasing the power loss and decreasing the stored energy. The example of the former is the RMPA with lossy matching and the latter is L-C resonance matching. But, L-C resonance reduces the stored energy only over a narrow bandwidth. On the other hand, non-Foster matching can reduce the stored energy over a broad bandwidth. NMPA use the NFC for the interstage matching to cancel out the

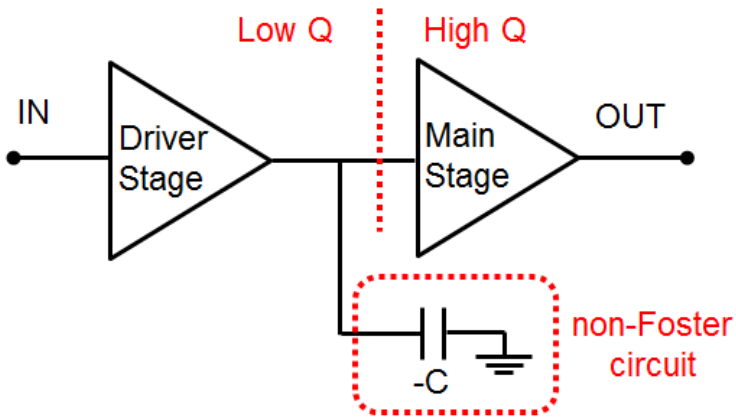


Fig. 3.1. Block diagram of the two-stage PA with NFC.

large input capacitance of the power-stage FETs and lowering the Q-factor of interstage matching.

Output matching is realized with a conventional two-section matching network. The output powers from each FET are combined through a Wilkinson power combiner to achieve > 5 W over the target frequency range of 6-18 GHz.

One of the key practical issues with NFC is the limited operating frequency. The bandwidth limitation comes from the self-resonance. The SRF is limited by the f_T of the device. As will be shown in the next sub-section, the SRF is limited to ~ 11 GHz, which is not high enough to cover the entire bandwidth up to 18 GHz. Therefore, the interstage matching network is optimized separately for two sub-frequency regions. The natural interstage matching is optimized for the upper sub-frequency band above 11

GHz, where the NC is not available. The impedance mismatch in the lower sub-frequency band below 11 GHz is compensated for by the NC presented by NFC.

3.3. Detailed Analysis for NFC

3.3.1. Topologies of the NFC

There are many types of NFCs, including 2−4 FETs depending on how the FETs form the positive feedback [12]. In this chapter, the goal is to use two FETs to build a stable and optimized NFC and apply it to NMPA. The topologies of a typical NFC using two FETs are shown in Fig. 3.2. Two NICs and a negative impedance inverter (NII) structures are representative. The NIC converts the sign of the load impedance, but NII inverts the frequency characteristic of the load impedance [16]. Therefore, in order to make an NC, NII needs an inductor for the load. The NII is known to have better frequency characteristics, but its equivalent circuit is complicated and has a lot of parasitic, making it difficult to use NC. In addition, the loaded inductor is difficult to control, the size is large, and the Q value is not so good, which makes it more inconvenient than a capacitor.

The NICs are also divided into the open circuit stable (OCS) and the short circuit stable (SCS) types, which are classified according to their stability. It can be seen that the application of NIC is divided according to whether it is series or parallel connection. However, the OCS type has better frequency characteristics because it can contain the C_{gd} value when constructing the load capacitance [17].

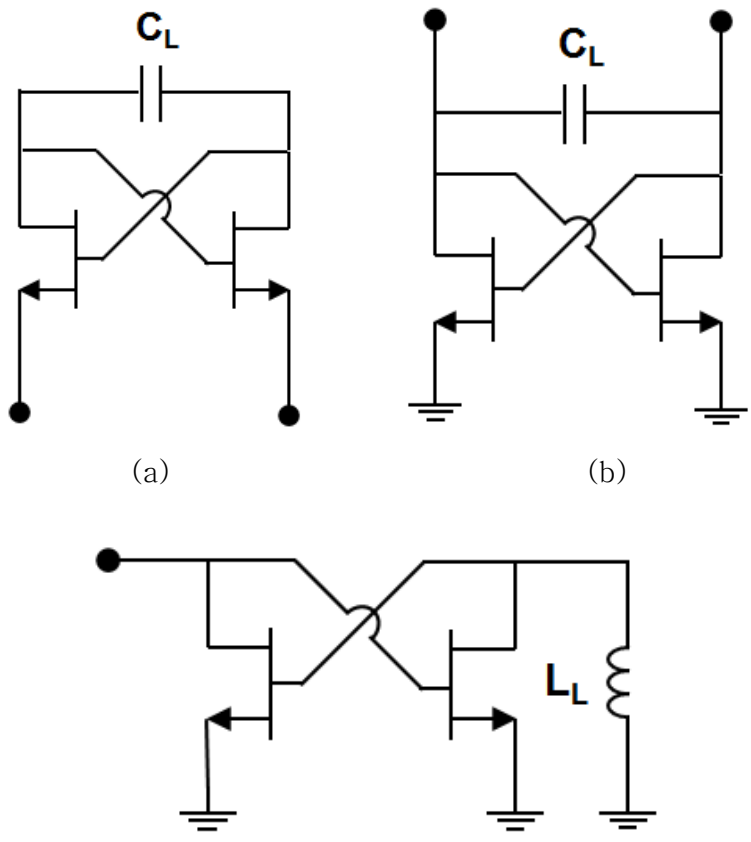


Fig. 3.2. The NFC topology of (a) OCS type NIC, (b) CSC type NIC, and (c) NII.

The NFC used in the NMPA is important in its size, not only the SRF must be high, but also the loss cannot be ignored, so the OCS type NIC is finally selected.

3.3.2. Frequency Limitation and Equivalent circuit of the NFC

The NFC used in the interstage matching is based on the Linvill's NIC (Fig. 2.4 (a)). However, the NIC cannot generate the NC in the low G_m condition. For example, high-frequency operation or large signal-operation leads to low gain conditions. In this case, NIC operates just like normal inductor. Small-signal characteristics of the NIC can be understood from a simple analysis using C_{gs} and G_m. With the two identical TRs, the input impedance, Z_{in}, and the SRF(ω) can be expressed by the following equations [18];

$$Z_{in} = \frac{1}{\omega_T^2 - \omega^2 + 2s\cdot\omega_T}\left[s\cdot\left(\frac{2}{C_{gs}} + \frac{1}{C_L}\right) + \frac{2\omega_T}{C_{gs}} - \frac{\omega_T^2}{s\cdot C_L}\right] \tag{3.1}$$

$$Im\left[Z_{in}\right] = 0 \quad \text{at} \quad \omega = \omega_T \Big/ \sqrt{1 + 2C_L/C_{gs}} \tag{3.2}$$

where ω_T is $2\pi\cdot f_T$. The equivalent circuit shown in Fig. 3.3 is derived from the first equation. The equivalent circuit of NIC is composed of a complicated combination of resistors, inductors, and capacitors. As a result, the input impedance is a strong function of frequency. At frequencies higher than the f_T of the TR, NIC cannot convert the loaded capacitor to NC. However, as can be seen from equation (3.2), the SRF is much lower than f_T due to the additional capacitances and inductances. For example, SRF is only 11.6 GHz

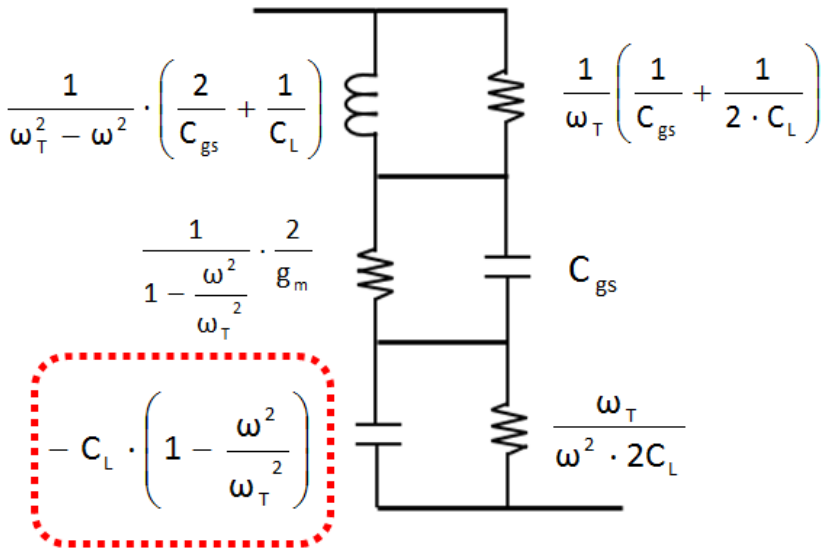


Fig. 3.3. The reduced equivalent circuit of the NIC.

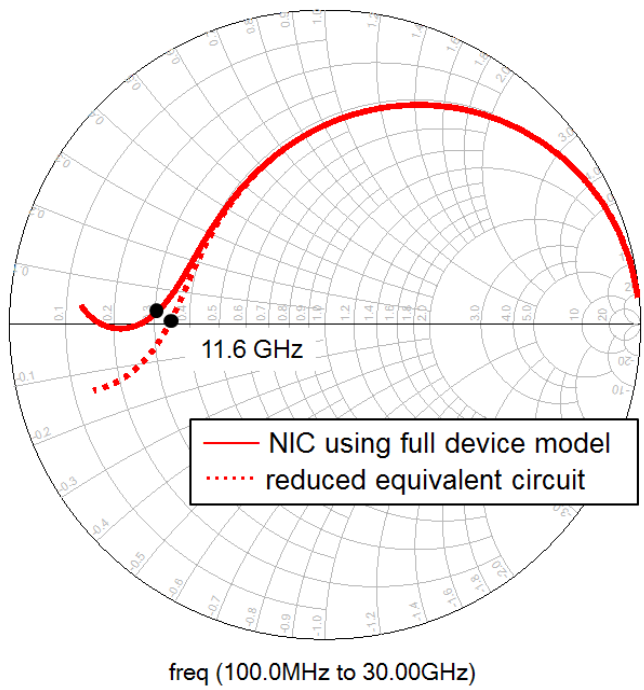


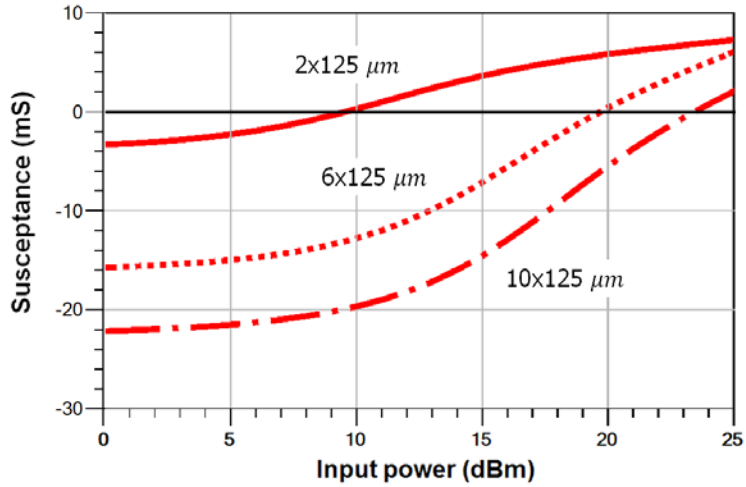
Fig. 3.4. Simulated S-parameters of the NIC using the full device model and the reduced equivalent circuit.

even if f_T is 21.7 GHz for a 6×125 μm GaN FET (C_L =1.5 pF and C_{gs} =1.2 pF). Fig. 3.4 shows the simulated S-parameter of the NIC using the simplified equivalent circuit of Fig. 3.3 and the full FET model provided by the foundry. The equivalent circuit of the intrinsic FET model contains the low-frequency dispersion effect with the thermal and trap sub-circuits [19] and the equations for I_{ds}, I_{gs}, I_{gd}, and C_{gs} are based on the Angelov model. The full device model simulation predicts an SRF of 13 GHz while the simplified model shows an SRF of 11.6 GHz. The difference between the two results comes from C_{ds} and other parasitic effects not accounted for in the simplified equivalent circuit.

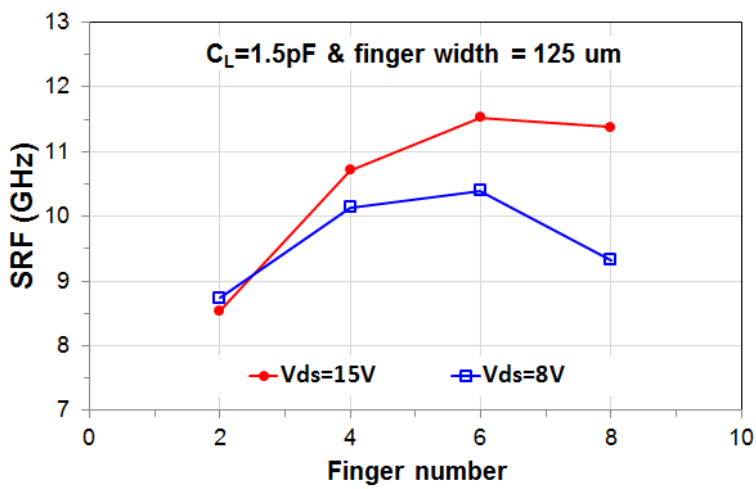
3.3.3. Detailed NFC Design for Broadband PAs

Key design parameter is the value of the load capacitance, C_L, in the NFC (see Fig. 2.4 (a)) since it determines $-C_{eq}$ in Fig. 2.4 (b). Larger C_L results in a larger NC, which allows the compensation of larger input TR capacitance. This means that a smaller number of NFCs are required to compensate for the given power-stage TRs. The dc power consumption of the NFC can be reduced in this way. However, SRF is inversely proportional to $\sqrt{1+C_L/C_{gs}}$ and one needs to carefully select C_L and C_{gs} considering the required bandwidth.

The TR size used in the NFC determines C_{gs}. The TR size also



(a)



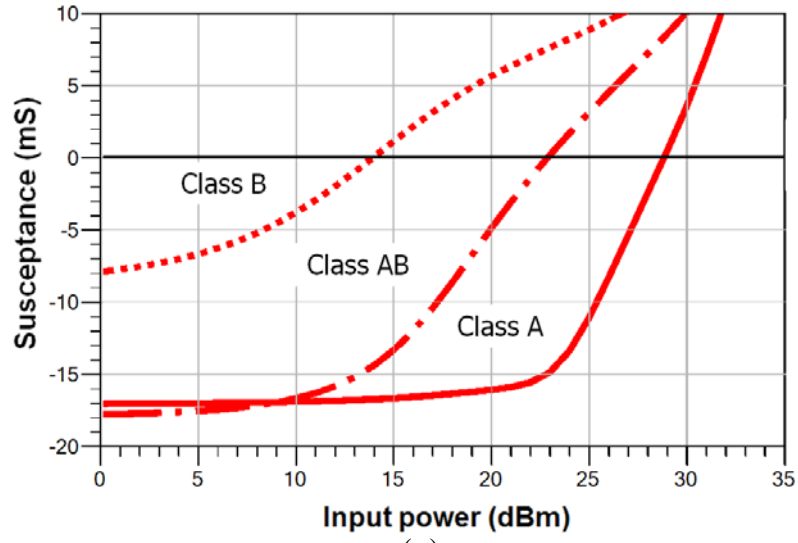
(b)

Fig. 3.5. Simulated (a) power handling capability of the NFC and (b) SRF with various unit TR size.

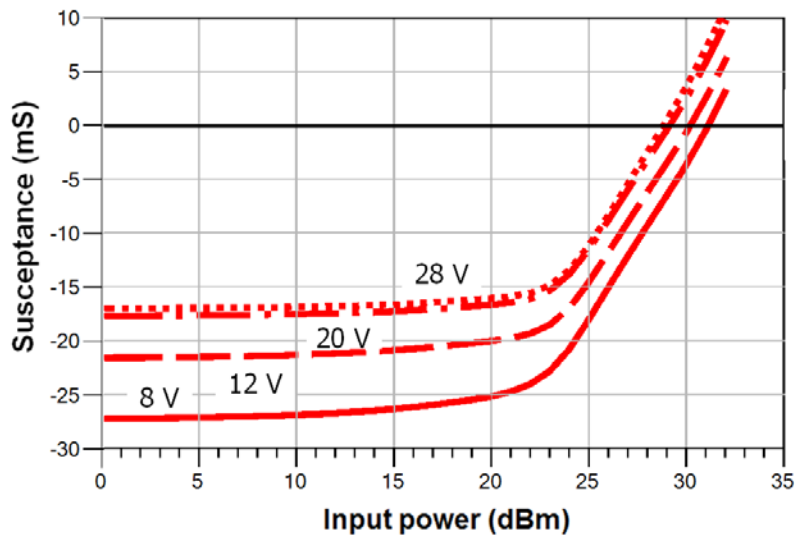
determines the power handling capability of the NFC. Fig. 3.5 (a) shows the simulated power handling capability of the NFC with the various TR sizes. The negative susceptance represents the effect of the NFC and the power capability can be determined by the input

power when the susceptance crosses zero. The power limit of the NFC improves with the TR size. This can be understood from the load seen by the cross-coupled TRs in the NFC. Each TR has the output load composed of the C_L and the other TR, which presents relatively low impedance. Due to the large bias voltage of the GaN TRs, the power limitation of the NFC arises from the current clipping rather than the voltage clipping. Larger TRs provide higher current driving capability and thus improved power handling capability. However, one cannot increase the TR size indefinitely since it will negatively impact the high-frequency operation limit of the TRs and their cut-off frequencies. To find the optimal TR size for SRF, we have calculated SRF as the TR size is varied in Fig. 3.5 (b). C_L and the unit gate finger width are fixed at 1.5 pF and 125 μm, respectively, and the number of gate fingers is increased from 2 to 8. The simulation is repeated for two drain bias voltages, 8 and 15 V. As shown in Fig 3.5 (b), it is clear that the optimal SRF can be achieved with 6×125 μm TRs at both 8 and 15 V bias conditions. In this work, a TR size of 6×125 μm is used together a C_L value of 1.5 pF. The resulting C_L / C_{gs} is 1.27, and SRF is around 11.6 GHz.

The side effect of using larger TRs in NFC is the increased power consumption. The NFCs employed for antenna matching have employed Class-C or Class-B biasing to avoid the dc power consumption under small-signal operation [20]. However, a similar



(a)



(b)

Fig. 3.6. Simulated negative susceptance of NFC vs. the input power at various (a) gate bias and (b) drain bias.

biasing may not be applicable for large signal operation as in PAs. In an attempt to find the optimum bias points, the power handling capability of the simple NFC is simulated by sweeping the gate and

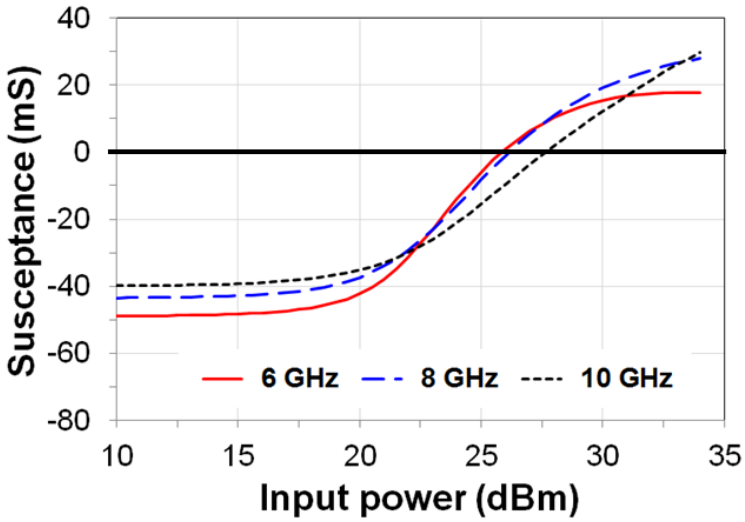


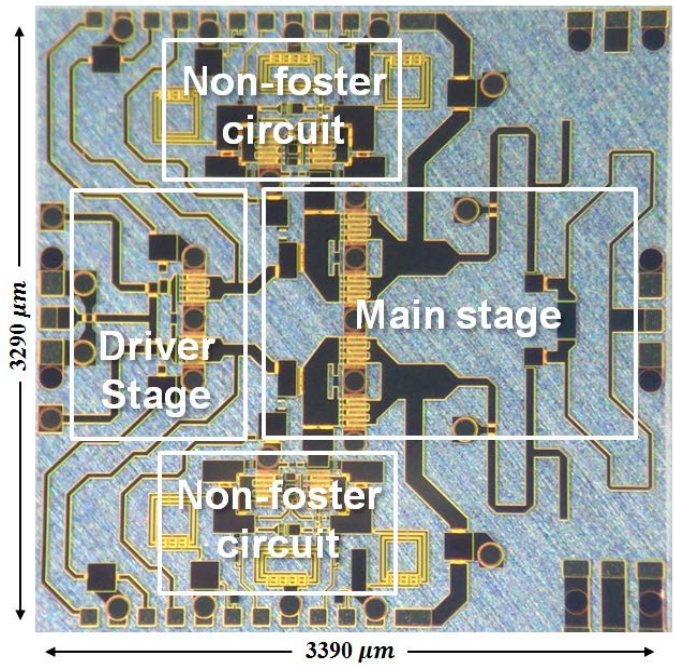
Fig. 3.7. Simulated susceptance of the NIC versus injected RF power.

drain biases at 8 GHz in Fig. 3.6. The large-signal TR model employed in this work predicts the PA power performance with reasonable accuracy. However, it has limited accuracy in predicting the bias dependence of the PA. The modeling accuracy can be improved by using more sophisticated GaN FET models [21][22]. As shown in Fig. 3.7, the NFC used in the interstage matching should present the negative susceptance up to ~ 26 dBm input power to cover the frequency range down to 6 GHz. Fig. 3.6 (a) clearly shows that Class-B biasing provides insufficient power limit. In this work, Class A~AB biasing is used. Unlike the case of the gate bias, the drain bias can be reduced to 8 V without impacting the power handling capability as shown in Fig. 3.6 (b). This can be

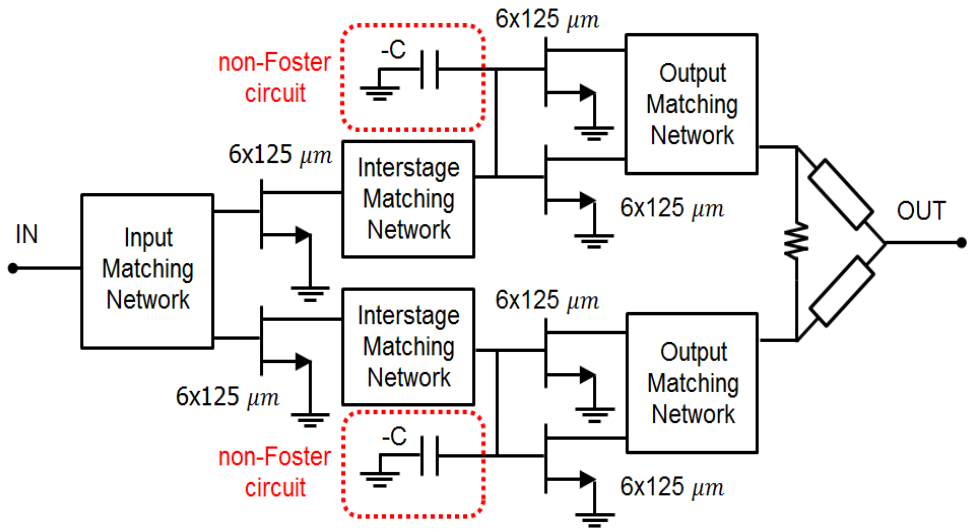
understood from the fact that the current clipping is the main limiting mechanism rather than voltage clipping, and that the TR G_m peaks around 6–10 V and degrades slightly as the drain bias is increased. At high drain bias, GaN power TRs can show G_m degradation due to self–heating [23][24]. In this work, a drain bias of 8 V and 15 V are employed for the cross–coupled TRs used in the NFC.

3.4. Measurement Results

The PA is designed with non-Foster matching network and fabricated using a commercial 0.25-μm GaN pHEMT foundry process. The PA is based on a two-stage design with the NFC employed in the interstage matching circuit. The PA is designed to achieve higher output power by combining the output powers of four 6×125 μm GaN FETs. It consists of two parallel PA chains, each with two power FETs combined using a shared output matching network. Wilkinson coupler is employed to combine the output powers from each PA chain. The expected output power is 1-2 dB higher instead of 3 dB with power combining due to the insertion and mismatch losses of the on-chip broadband Wilkinson coupler. The interstage matching for the second PA is optimized to show more pronounced NFC effect in a slightly shifted frequency range with focus on 8-12 GHz. For testing, the PA chips are mounted on 5-mm-thick Au-plated Cu carrier with eutectic bonding to mitigate self-heating. On-wafer probing using ground-signal-ground probes (the Infinity probes from Cascade Microtech) is used to measure both small-signal and large-signal characteristics. Continuous wave signal is used to measure the power characteristics.



(a)



(b)

Fig. 3.8. (a) Fabricated chip photograph and (b) block diagram of 4× combined PA with NFC.

3.4.1. Parallel Combined PA with 4× Combining

The die photograph and the block diagram of the 4× combining PA are shown in Fig. 3.8. For this PA, the drain bias to the power FETs is 28 V while that to the NFC FETs is reduced to 8 V based on the analysis presented in the previous section. Fig. 3.9 represents the measured small-signal gain with and without NIC. Similar to the result of the 2× combining PA, S_{21} increases in the low-frequency sub-band from 7 to 12 GHz with the NIC. The gain improvement is more pronounced at slightly higher frequencies in this design since the interstage circuit is further optimized to achieve better matching near 8-12 GHz. The gain improvement up to 3.9 dB can be observed at 11 GHz.

The measured power characteristics with and without NIC are shown in Fig. 3.10. Unlike the case of 2× combining PA which showed the power improvement (~ 1.2 dB) only up to ~ 10 GHz, this circuit showed significant power improvement (~2 dB) up to 12 GHz. Over a slightly shifted frequency range of 7 to 17 GHz, the output power higher than 5 W is achieved. The lower frequency limit for this design is around 7 GHz, below which no power improvement is observed with the NIC. The PAE degradation due to the power consumption of NIC is estimated to be less than 0.5%.

Fig. 3.11 compares the power sweep characteristics at 10 GHz between the two PA circuits. With NIC, the output power is

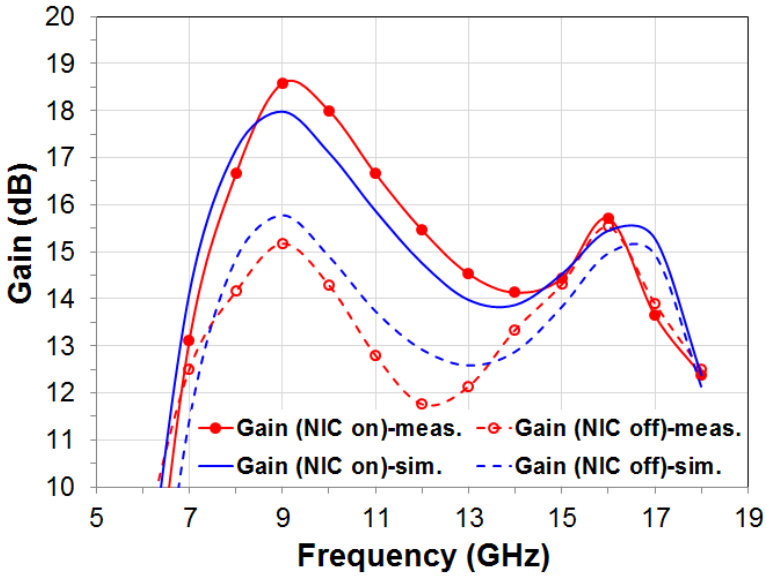


Fig. 3.9. Measured small-signal gain of 4× combined PA with and without the NIC.

increased by as much as 2.1 dBm from 36.1 to 38.2 dBm and the PAE is improved by 4.5% in 4× combining PA while the improvement is limited to 0.66 dBm and 1.6% for 2× combining PA. This is again attributed to the further optimized interstage network at this frequency. The output power increase in 4× combining PA compared with 2× PA is 1~2 dB from 7 to 17 GHz. At the band edges, the output power improvement is limited due to the increased loss of the power combiner. The measured PAE of the 4× combining PA is also lower than the 2× PA due to the power combiner loss.

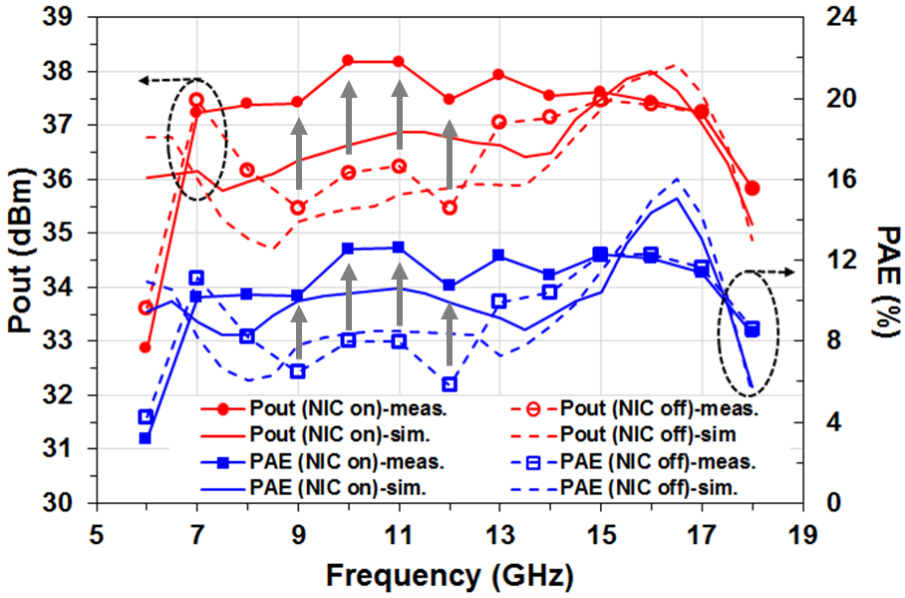


Fig. 3.10. Measured output power of 4× combined PA with and without the NIC.

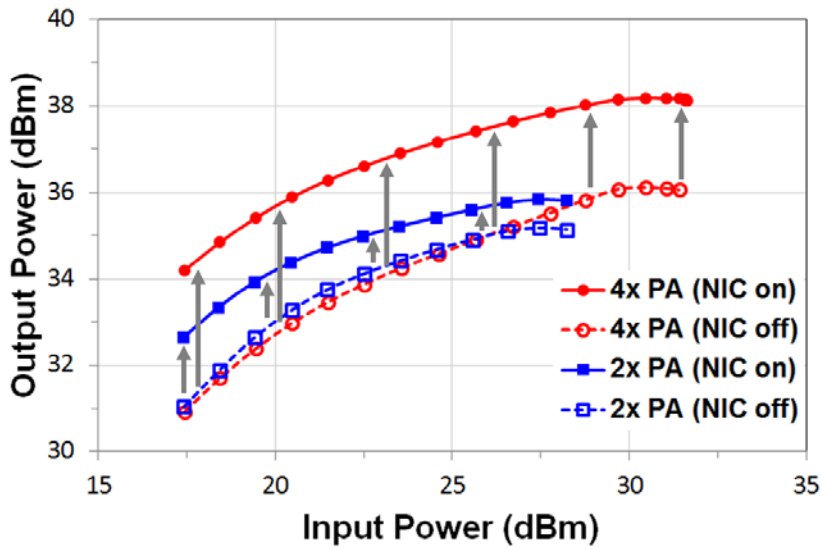


Fig. 3.11. Measured power sweep characteristics of 2× and 4× PAs at 10 GHz.

3.4.2 Comparison Table

Table 3.1 compares the performance of the PA of this work with the state-of-the-art DA and RMPA using GaN pHEMTs. This work is an extended version of our previous work in chapter 2 [25], which is the first demonstration of the NMPA. Even though the measured power and PAE do not match the state-of-the-art results due to the limited device performance, this work shows that NIC can be an effective method to realize a broadband PA in a small die area without lossy matching or feedback.

TABLE 3.1

Performance Comparison of GaN Broadband PAs

	[8]	[9]	[26]	[27]	[10]	[28]	[11]	[29]	[29]	This Work
Freq. (GHz)	2–18	2–20	8–18	2–18	6–18	8–18	6–18	6–18	6–18	**7–18**
Topology	DA	DA	DA	DA	RM PA	RM PA	RM PA	RM PA	RM PA	**NM PA**
Process	0.25 μm GaN	0.2 μm GaN	0.25 μm GaN	0.2 μm GaN	0.25 μm GaN	0.25 μm GaN	0.25 μm GaN	0.25 μm GaN	0.25 μm GaN	**0.25 μm GaN**
PAE (%)	20–38	15–36	15–21	5–15	14–24	25–35	13–25	15	19	**10.2–12.3**
Pout (W)	9–15	9.9–21.6	7.9–10.9	0.8–2	3.2–20	1.25–2	6–10	20	15.1	**5.3–6.6**
Gain (dB)	10–14	9–15	12.2–14.1	18–21	17–28	7–9	18–24	9.6	9.3	**13.1–18.6**
Area (mm^2)	15.3	38	15	8	19.25	10.44	19.8	19.2	19.2	**11.15**
Power density (W/mm^2)	0.59–0.98	0.26–0.57	0.53–0.73	0.1–0.25	0.17–1.04	0.12–0.19	0.30–0.51	1.04	0.79	**0.48–0.59**

3.5. Conclusions

In this chapter, two-stage GaN NMPA with more than 5 W output power has been developed for multi-octave broadband power applications. The bandwidth limitation due to high-Q interstage matching has been mitigated through the use of a shunt NC. To guarantee the high power operation over the entire bandwidth, natural interstage matching is optimized for the upper sub-frequency band and the lower sub-frequency band is compensated for by the NC presented by NFC. The NFC topology suitable for NMPA is analyzed and selected. Detailed analysis is performed to understand the frequency limitation of NIC approach, which shows that high-frequency limit comes from the self-resonance and the low-frequency limit from the power handling capability. The fabricated 4× combining PA shows output powers higher than 5 W from 7 to 17 GHz. At frequencies, where NFC is optimized for interstage matching, the power improvement by 2.1 dBm and PAE improvement by 4.5% have been achieved.

Chapter 4

A Broadband GaN pHEMT Power Amplifier Using Cascaded Stage Negative Impedance Converter

4.1. Introduction

There are many issues with NFC. First, it is an operating frequency limitation. As frequency increases, the circuit changes frequency characteristics from non-Foster to Foster and resonates with parasitic components, and makes SRF. Second, there is a problem that it is difficult to make large NC. Since the SRF is determined as a function of C_L / C_{gs}, large NC and high operating frequency are hard to exist at the same time [30]. Third, there is a problem with power handling capability. In the large-signal operation, the positive feedback loop gain of NFC is reduced and

impedance conversion is not possible [31]. Using a large-sized TR can solve this problem, but because of the small unity gain f_T, the SRF is decreased. Larger DC power dissipation is also a problem. Fourth, it is difficult to obtain a low loss negative capacitor as it operates at higher frequencies. Finally, stability and noise problems are also a well-known problem.

In this chapter, a CSNIC structure is proposed that can solve all the problems of SRF, loss, and power handling capability.

4.1.1. Cause of losing non-Foster operation

There are two main reasons why non-Foster operation is lost. First, the gain of the unit TR constituting the NFC decreases as the frequency increases, and the feedback loop gain becomes insufficient. Second, the phase delay of the feedback gradually goes away from 0° and does not result in a positive feedback. Therefore, using a unit cell with sufficient positive feedback loop gain up to high frequency is the solution.

Several well-known gain cells are candidates. For example, distributed gain cell, stacked FET structure, Darlington cell [32], feedback with inductive peaking, and cascaded gain cell. In more detail, there are various types of DA, such as cascaded single stage DA [33], multi-stage DA [34], and matrix DA [35]. Therefore, it can be said that there are many types of broadband gain cells.

Therefore, we need to look more closely at the conditions for successful operation of NFC.

4.1.2. NFC conditions for obtaining broadband NC

As mentioned earlier, first, the unit cell must have enough gain to high frequency. Second, the phase delay must be configured to form a positive feedback. The use of inductive peaking techniques is not advantageous because of the larger losses due to phase delays. Third, there should be no stability problem to prevent oscillation. In the case of Darlington cells or stacked FET structures, it is not appropriate because gain increases but stability decreases. In addition, there are other frequency limits for stacked FET structures [36]. Fourth, the input and output impedances of the gain cell must be capacitive to obtain NC. The gate or drain parasitic inductance is connected in series to the load impedance. This inductance resonates with the load and acts like a Foster circuit or is converted into negative inductance. Thus, the inductive input and output impedance of the gain cell will drastically reduce the SRF. Therefore, a broadband NC cannot be obtained using a distributed gain cell that behaves like a transmission line. Finally, since we want a broadband NC for susceptance cancellation, these conditions must also be satisfied in the broadband.

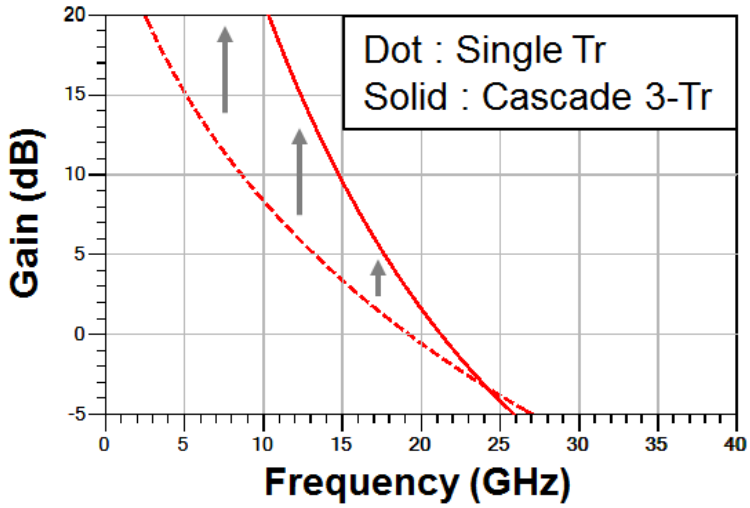
4.2. Cascaded Stage Negative Impedance Converter

4.2.1. Operation Principle and Circuit Design

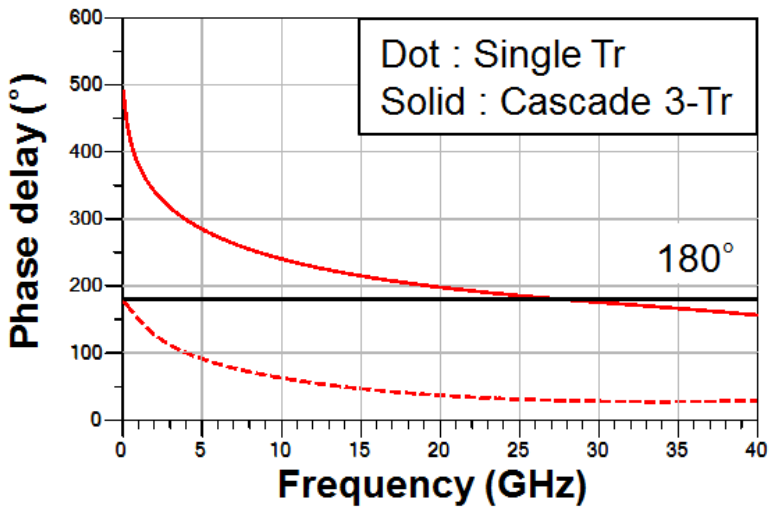
The cascaded stage TR was selected as the broadband gain cell, finally. Cascade structure not only provides high gain easily but also has good stability. As shown in Fig. 4.1 (a), the cascade method increases the gain from 5 dB to 15 dB at 10 GHz. Furthermore, by adjusting the size and number of stages of the TR, the phase delay can be adjusted to produce a positive feedback.

Fig. 4.2 (b) shows the phase delay of a single stage and cascaded 3-stage with 6×125 μm size TR at 50 ohm termination conditions. As the frequency increases, the phase delay goes away from 180 degrees. However, in the case of the cascaded stage, it can be seen that the delay of 180 is shown again at about 23 GHz. Fig. 4.2 shows the phase delay of each NIC according to the number of TRs constituting the cascade cell. When the phase delay target is set to 180° +/- 90° , it can be seen that the NIC using four TRs can operate satisfactorily at 6 GHz to 18 GHz.

Moreover, input and output impedance of the cascade cell are similar to those of single TR. Fig. 4.3 shows the equivalent circuit of 2-stage cascade CS. Except for the small C_{gd} effect, C_{gs} and C_{ds} still constitute the main input and output impedance.



(a)



(b)

Fig. 4.1. (a) The gain of a single stage and cascaded 3-stage CS. (b) The phase delay of a single stage and cascaded 3-stage CS.

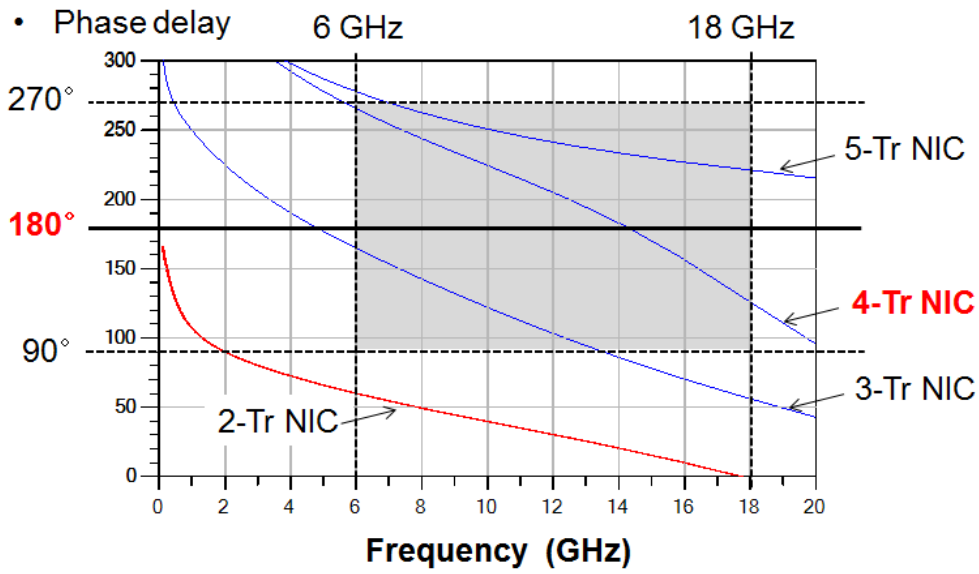
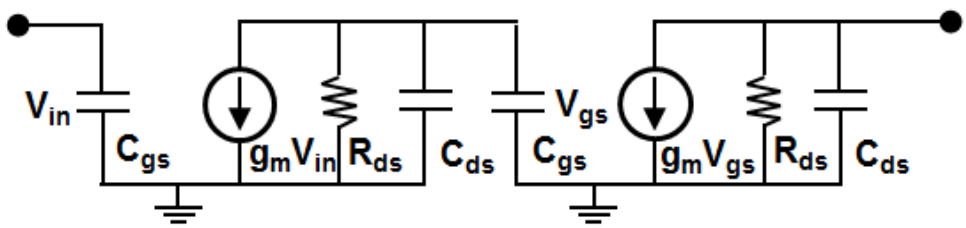
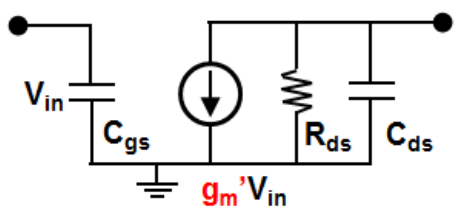


Fig. 4.2. The phase delay of each NIC according to the number of TRs constituting the cascade cell.



(a)



$$g_m' = g_m \left(\frac{-g_m R_{ds}}{1 + j\left(C_{gs} + C_{ds}\right) R_{ds} \omega} \right)$$

(b)

Fig. 4.3. (a) The small-signal FET model of 2-stage cascaded CS and (b) the equivalent circuit model.

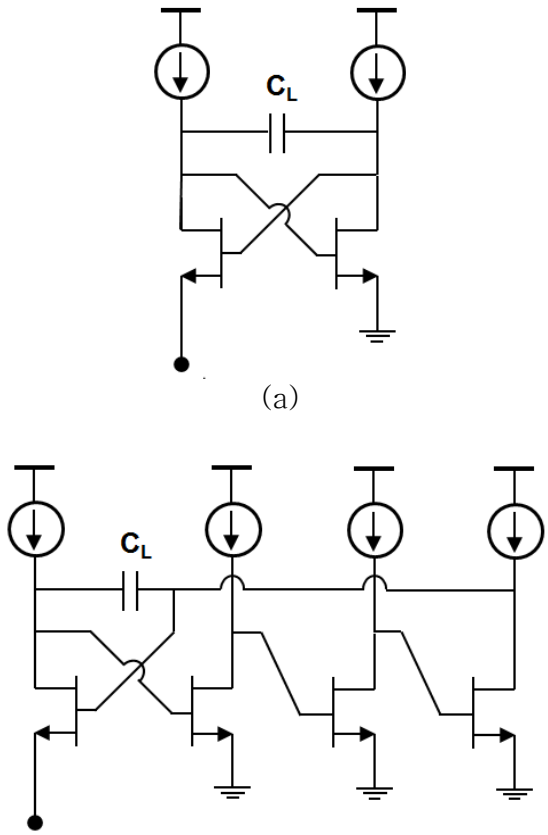
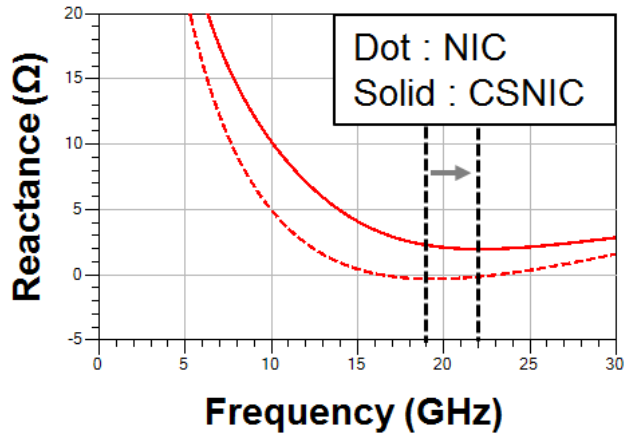


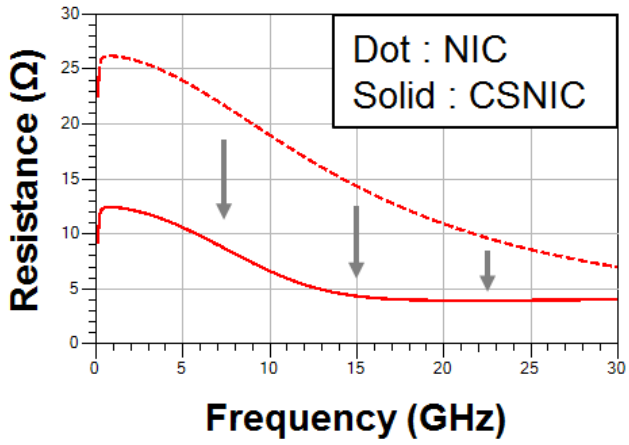
Fig. 4.4. (a) Conventional NIC structure. (b) Proposed CSNIC structure.

As a result, the cascade cell can be seen as an equivalent gain cell with increased G_m and worsened phase delay. This gain cell is suitable for NFC because it can obtain positive feedback loop gain at high frequency. Conventional NIC structure and CSNIC structure proposed in this chapter are shown in the Fig. 4.4.

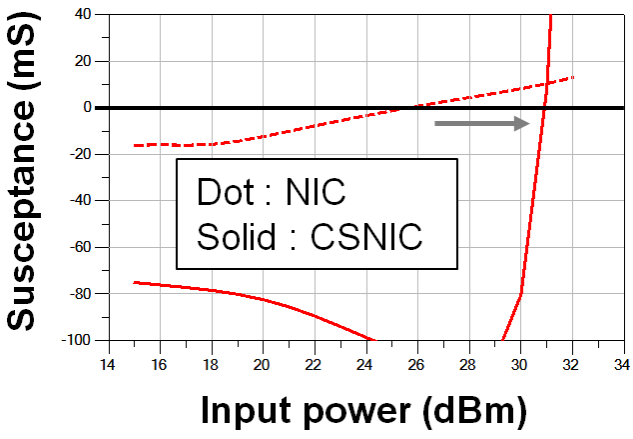
Since the SRF of the NIC can be enhanced through CSNIC, it can be configured using a $10\times125\,\mu$m size TR with lower f_T but better power handling capability. As can be seen in Fig. 4.5, we can



(a)



(b)



(c)

Fig. 4.5. The improved performance of (a) SRF, (b) loss, and (c) power capability with CSNIC

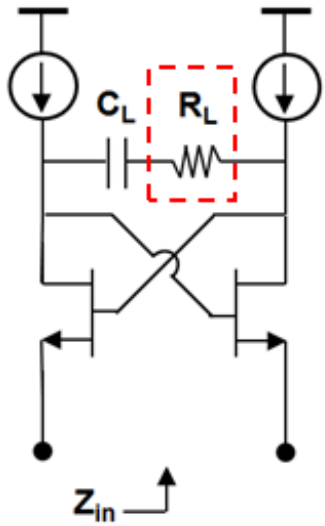
achieve increased SRF and loss reduction effects even with larger TR. Both NFCs are simulated with a C_L value of 1.0 pF. The power capability of the CSNIC is also significantly higher than that of the NIC (Fig. 4.5 (c)).

4.2.2. Loss Compensation of NFC

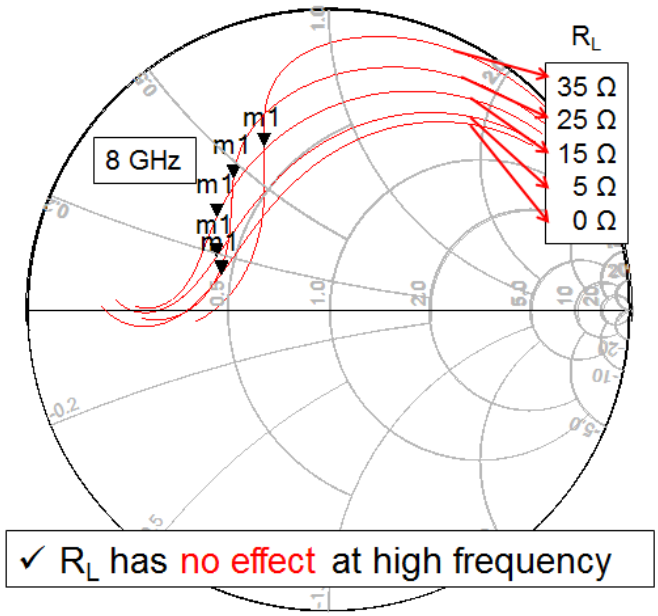
The NIC has parasitic resistance inversely proportional to G_m [12]. If G_m is high, the loss of NIC is small. However, other parasitic effects appear at higher frequencies. Therefore, a method of compensating losses using resistive load R_L is mainly used (Fig. 4.6 (a)). The R_L is converted to negative resistance (NR) and can compensate for parasitic resistance. In this way, a high-Q negative capacitor can be realized.

However, NR also has a frequency limit. At higher frequencies, the loss cannot be compensated as intended. Fig. 4.6 (b) shows the simulated input S-parameter of the NIC according to the R_L value. In the low-frequency region, the low-loss characteristic is shown as the R_L value increases. However, the effect of NR is no longer observed at 8 GHz.

The frequency limitation of the NR can be obtained from the input impedance of the NIC. The input impedance of the NIC corresponding to Fig. 4.6 (a) is as follows.



(a)



(b)

Fig. 4.6. (a) The conventional NIC structure with loss compensation technique. (b) The simulated input S-parameter of the NIC according to the R_L value.

$$Z_{in} = \frac{1}{\omega_T^2 - \omega^2 + s\cdot(2\omega_T)}\left[s\cdot\left(\frac{2}{C_{gs}} + \frac{1}{C}\right) + \frac{2\omega_T}{C_{gs}} - R_L\left(\omega^2 + \omega_T^2\right) - \frac{\omega_T^2}{s\cdot C}\right] \quad (4.1)$$

$$Z_{in} = \frac{1}{\omega_T^2 - \omega^2 + 2s\cdot\omega_T}\left[s\cdot\left(\frac{2}{C_{gs}} + \frac{1}{C_L}\right) + \frac{2\omega_T}{C_{gs}} - \frac{\omega_T^2}{s\cdot C_L}\right] \quad \text{(cf. without } R_L\text{)}$$

where ω_T is the radian cutoff frequency of the TR. The equivalent circuit is shown in Fig. 4.7. R_L has two effects on the NIC. The $-R$ reduce the loss of NIC and the $-C'$ increases SRF by reducing the total NC. From equation (4.1), SRF is derived as follows.

$$Im\left[Z_{in}\right] = 0 \quad \text{at} \quad \omega = \frac{\omega_T}{\sqrt{1 + 2\cdot C_L / C_{gs} - R_L C_L \omega_T}} \quad (4.2)$$

$$Im\left[Z_{in}\right] = 0 \quad \text{at} \quad \omega = \omega_T \Big/ \sqrt{1 + 2C_L / C_{gs}} \quad \text{(cf. without } R_L\text{)}$$

However, as can be seen from the above simulation results, loss compensation is not affected by R_L above a certain frequency. This can be explained by adding the C_{ds} effect. The NIC input impedance of Figure 4.8 is shown in the following equations.

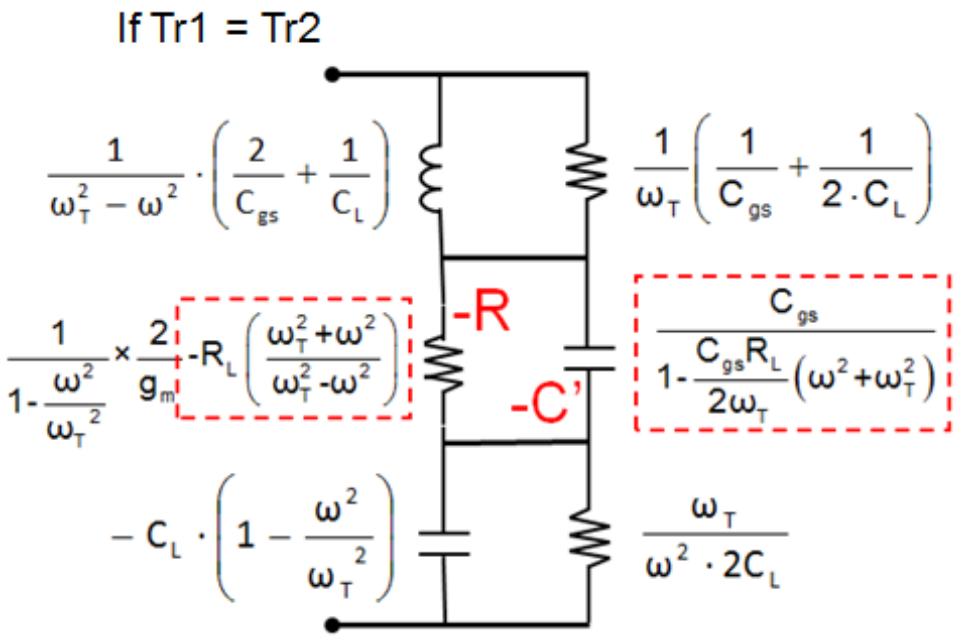


Fig. 4.7. The equivalent circuit of conventional NIC with loss compensation technique.

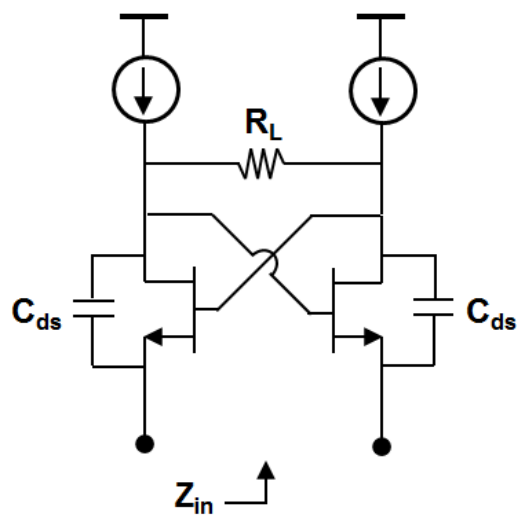


Fig. 4.8. The conventional NIC structure with loss compensation technique and C_{ds} effects.

$$Z_{in} = \frac{1}{\left(\omega_T - 2R_L C_{ds}\omega^2 + k_c s\right)\left(\omega_T + k_c s\right)} \times \left[s \cdot \left(\frac{2k_c}{C_{gs}} \right) + \frac{2\omega_T}{C_{gs}} - R_L \left(k_c^2 \omega^2 + \omega_T^2 \right) \right] \quad (4.3)$$

$$Z_{in} \cong \frac{1}{\omega_T^2 - k_c^2 \omega^2 + s \cdot \left(2k_c \omega_T\right)} \left[s \cdot \left(\frac{2k_c}{C_{gs}} \right) + \frac{2\omega_T}{C_{gs}} - R_L \left(k_c^2 \omega^2 + \omega_T^2 \right) \right] \quad (4.4)$$

$$Z_{in} = \frac{1}{\omega_T^2 - \omega^2 + s \cdot \left(2\omega_T\right)} \left[s \cdot \left(\frac{2}{C_{gs}} \right) + \frac{2\omega_T}{C_{gs}} - R_L \left(\omega^2 + \omega_T^2 \right) \right] \quad \text{(cf. without } C_{ds}\text{)}$$

At $k = \omega / \omega_T$, $k_c = 1 + C_{ds} / C_{gs}$, $\omega_T \gg 2R_L C_{ds} \omega^2$

Comparing with the equation (4.4) and equation without the C_{ds} effect, it can be seen that ω increases to $k_c\omega$ and the frequency characteristic deteriorates. The resistance value corresponding to the loss can be calculated as follows.

$$\mathrm{Re}[Z_{in}] \cong \frac{1}{1 + k_c{}^2 k^2} \left[\left(\frac{2}{\omega_T C_{gs}} \right) - R_L \left\{ 1 - \left(k_c{}^2 + 4C_{ds} / C_{gs} \right) k^2 \right\} \right] \quad (4.5)$$

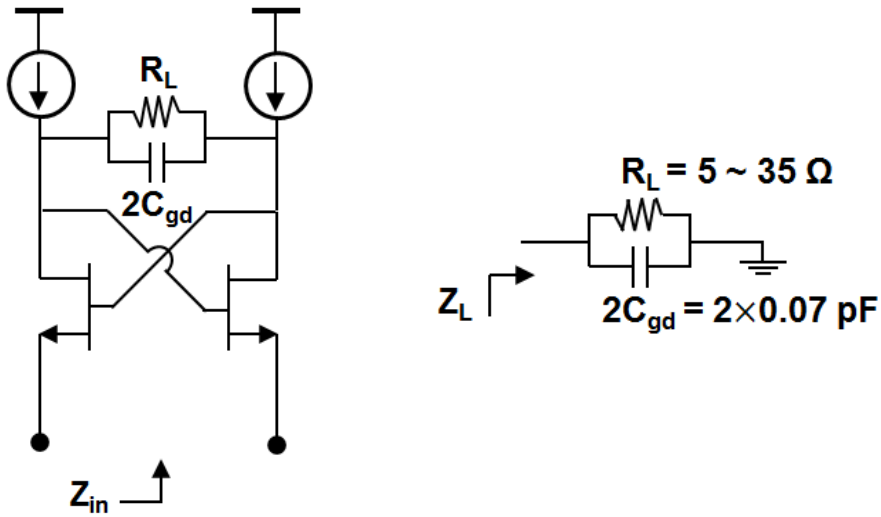
$$\mathrm{Re}[Z_{in}] = \frac{1}{1 + k^2} \left\{ \left(\frac{2}{\omega_T C_{gs}} \right) - R_L \left(1 - k^2 \right) \right\} \quad \text{(cf. without } C_{ds}\text{)}$$

Therefore, the frequency limitation of the NR is derived as follows.

$$\omega_{\lim} = \frac{\omega_T}{\sqrt{1 + 6 \cdot C_{ds} / C_{gs} + \left(C_{ds} / C_{gs} \right)^2}} \quad (4.6)$$

The variables that make up the frequency limit of R_L are ω_T and C_{ds}/C_{gs}. When C_{gs} = 1.37 pF, C_{ds} = 0.37 pF, ω_{lim} is about 0.61 ω_T. However, since C_{ds} and C_{gs} are generally proportional, it is difficult to significantly reduce the C_{ds}/ C_{gs}. Fortunately, ω_T can be improved under limited conditions. Because ω_T is proportional to G_m and is inversely proportional to C_{gs}, increasing the G_m value while maintaining C_{gs} can increase ω_T. Cascade gain cells enhance the G_m with little change in input and output impedance. If a positive feedback loop is constructed by adjusting the phase delay, ω_T is improved at least that frequencies. Thus, the CSNIC can increase the frequency limit of the NR.

C_{gd} also affects the NR. Fig. 4.9 shows the effect of C_{gd}. Since the C_{gd} is connected in parallel with the load impedance, it plays a role of reducing the effect of the R_L at high frequency. However, since the C_{gd} value is usually very small (0.07 pF for 6×125 μm size TR), the effect is large when the R_L is large. As shown in Fig. 4.10, even if a 30 ohm resistor is used for the load, it behaves like a resistor of 24 ohms.



(a) (b)

Fig. 4.9. (a) The conventional NIC structure with loss compensation technique and C_{gd} effect. (b) The load impedance of NIC with C_{gd}.

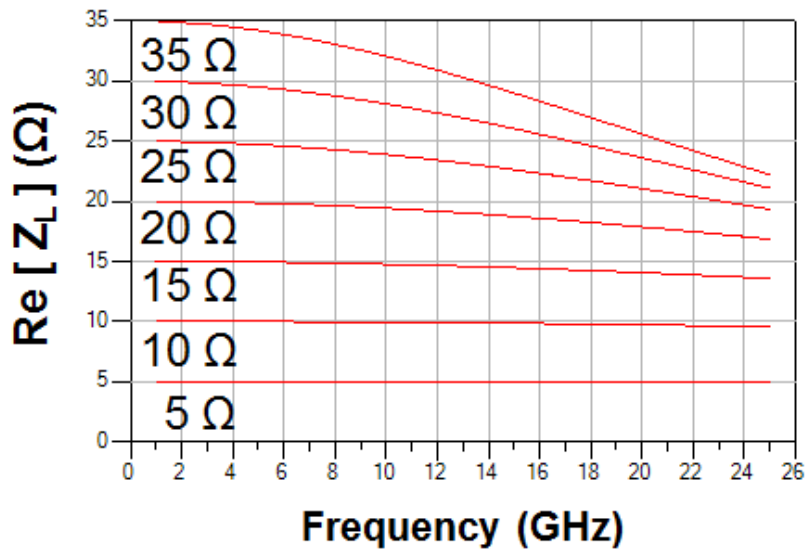
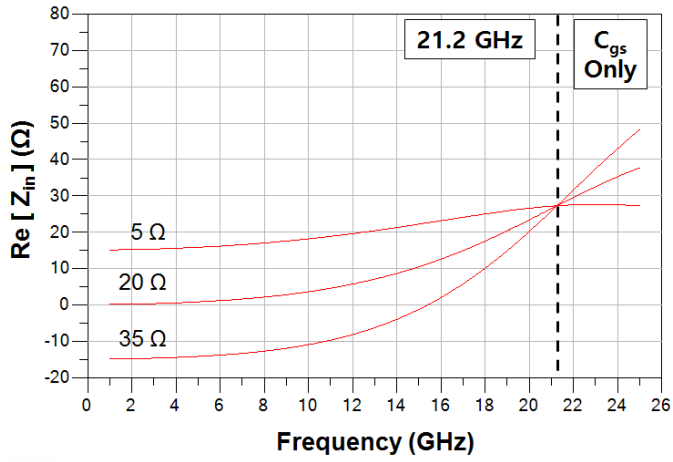
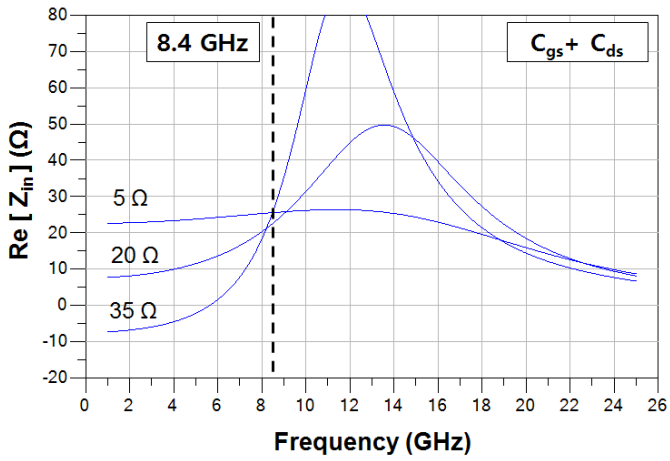


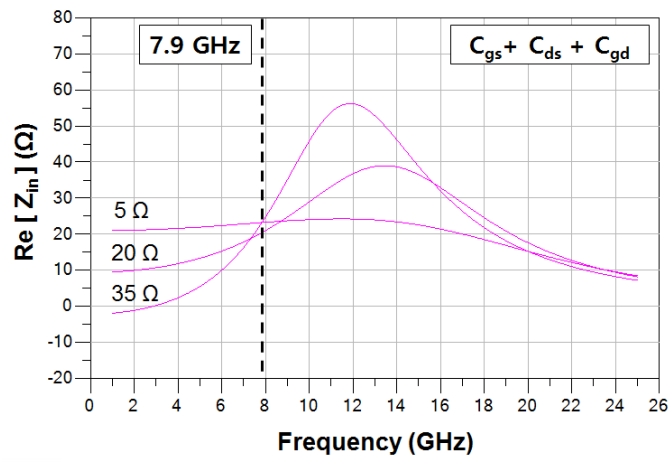
Fig. 4.10. The load resistance value of NIC with C_{gd} according to the R_L value.



(a)



(b)



(c)

Fig. 4.11. The frequency limits of NR with the effects of (a) C_{gs} only, (b) C_{gs} and C_{ds}, and (c) C_{gs}, C_{ds}, and C_{gd}.

The Fig. 4.11 shows the resistance simulation results with ideal FET model including G_m and C_{gs} values. When the effects of C_{ds} and C_{gd} are added, the frequency limit of NR decreases. 7.9 GHz, which is the simulation result of frequency limit including C_{gs}, C_{ds}, and C_{gd}, is similar to the previous simulation result with full FET model (Fig. 4.6 (b)). The Table 4.1 shows the summarized results of the frequency limit.

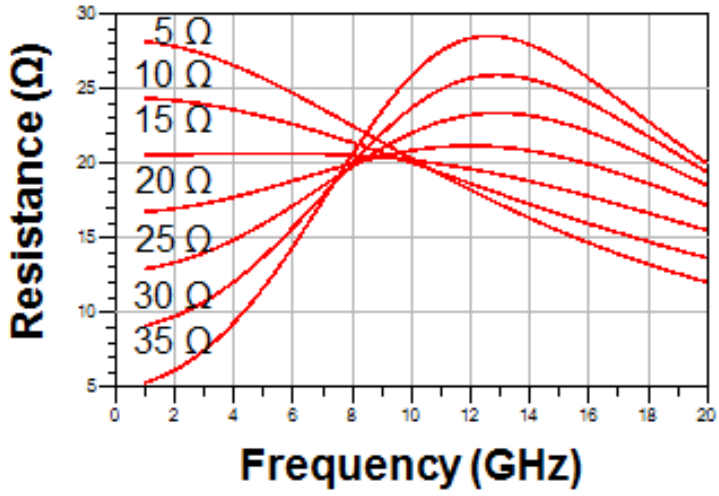
TABLE 4.1

Frequency limit of NIC from Parasitic Effects

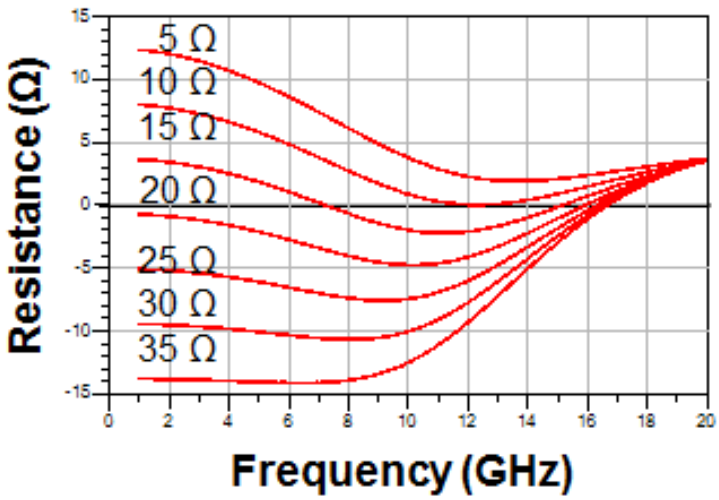
Parasitic effect	Ideal FET model	Full FET model
C_{gs}	21.2 GHz	–
C_{gs} + C_{ds}	8.4 GHz	–
C_{gs}+C_{ds}+C_{gd}	7.9 GHz	8.5 GHz

The Fig. 4.12 (a) shows the simulated loss compensation effects of the NIC when the R_L of 5 ~ 35 ohms is used. 6×125 μm size full-FET TR model is used, and the effect of the R_L is lost at about 8 GHz. On the other hand, when the resistance value of the CSNIC is simulated, it can be confirmed that the R_L is effective even at a frequency of about 16 GHz or more (Fig. 4.12 (b)).

Fig. 4.13 compares the resistance values of the CSNIC with and without R_L. When the R_L of 10 ohm is used, it can be confirmed that the resistance value is less than 5 ohm at all the frequencies.



(a)



(b)

Fig. 4.12. The simulated loss compensation effects of (a) the NIC and (b) CSNIC according to the R_L value.

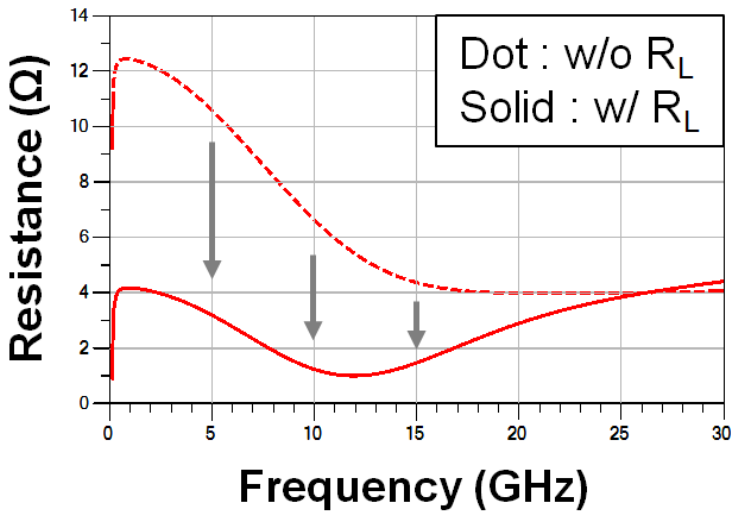


Fig. 4.13. The resistance values of the CSNIC with and without R_L.

Table 4.2 compares the performance of the CSNIC with that of the NIC. CSNIC can also use a 10×125 μm size TR because it can obtain sufficient SRF even with large size TR. This can be beneficial in terms of loss and power capability.

TABLE 4.2

Performance Comparison of NFCs

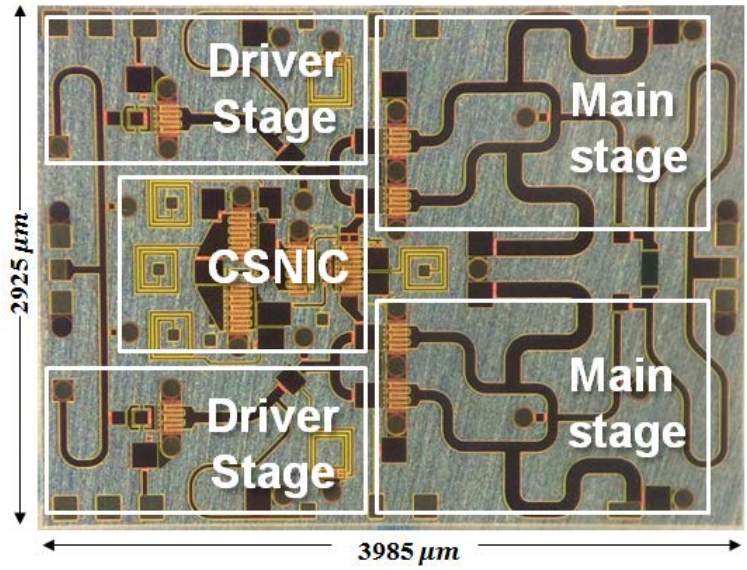
Topology (size)	NIC (6×125 um)	CSNIC (6×125 um)	**CSNIC (10×125 um)**
SRF	Low	High	**Middle**
Loss	Bad	Good	**Good**
Power capability	Low	Low	**High**

4.3. Measurement Results

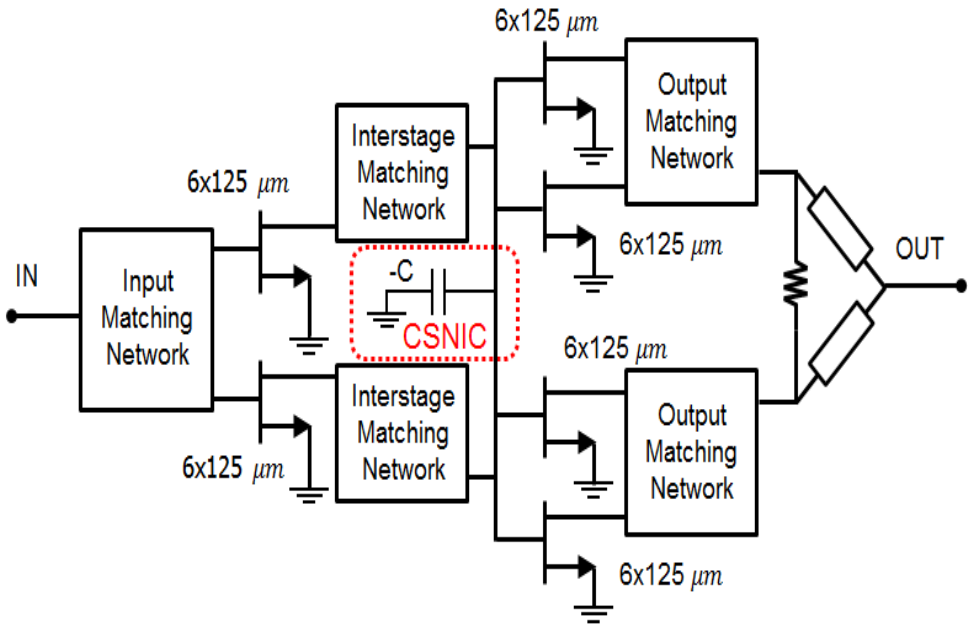
A PA is designed with CSNIC and fabricated using a commercial 0.25-μm GaN pHEMT foundry process. The PA is also based on a two-stage design with the CSNIC employed in the interstage matching circuit. The PA is designed to achieve 10W output power by combining the output powers of four 6×125 μm GaN FETs. The single NFC consisting of the cascade gain cells with the 10×125 μm TR size is used to cancel out the input capacitance of four power FETs. The CSNIC and interstage matching for this PA are also designed for optimum power performance in the lower sub-frequency band from over 6 to 10 GHz.

4.3.1 NMPA with CSNIC

The die photograph and the block diagram of the NMPA with CSNIC are shown in Fig. 4.14. The drain bias to the power FETs is 28 V while that to the CSNIC FETs is reduced to 6 V based on the analysis presented in the previous chapter 3.2.3. Fig. 4.15 (a) compares the S-parameter measurement results with the simulation results. The operating frequency increased by about 0.5 GHz, and the S_{21} is decreased by about 1.5 dB. This is due to the G_m degradation from thermal and parasitic effects. Fig. 4.15 (b) represents the measured small-signal S-parameters with and

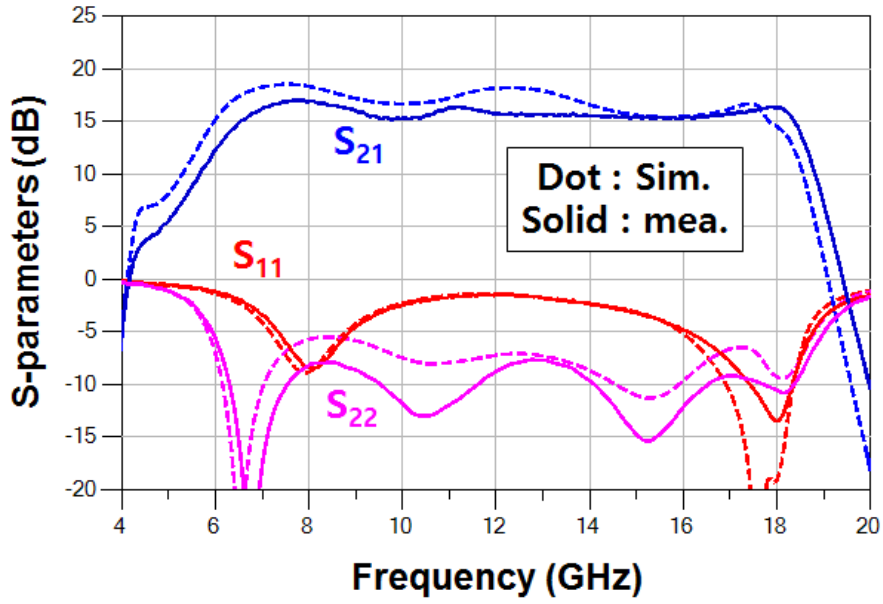


(a)

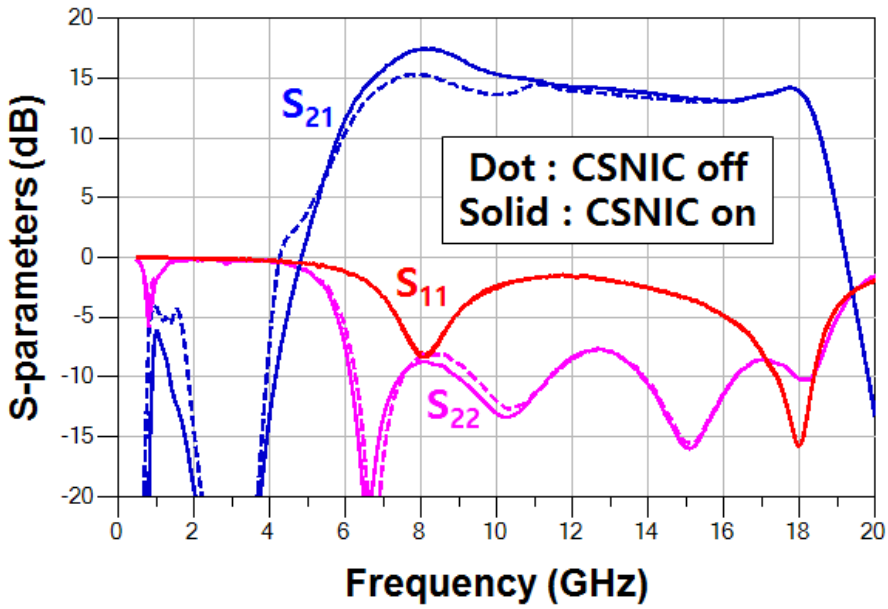


(b)

Fig. 4.14. (a) Fabricated chip photograph and (b) block diagram of NMPA with CSNIC



(a)



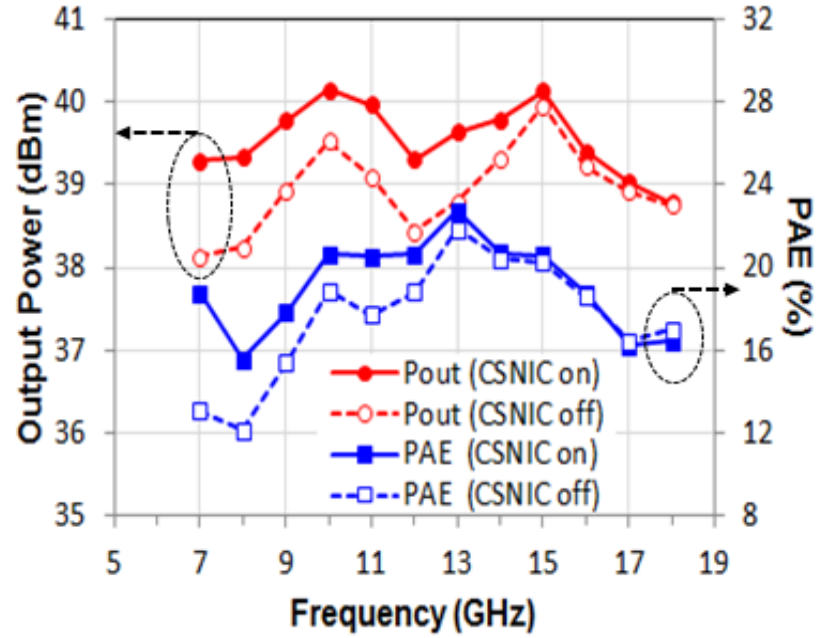
(b)

Fig. 4.15. (a) Simulated and Measured small-signal S-parameters results of NMPA without the CSNIC. (b) Measured small-signal S-parameters results of NMPA with and without the CSNIC.

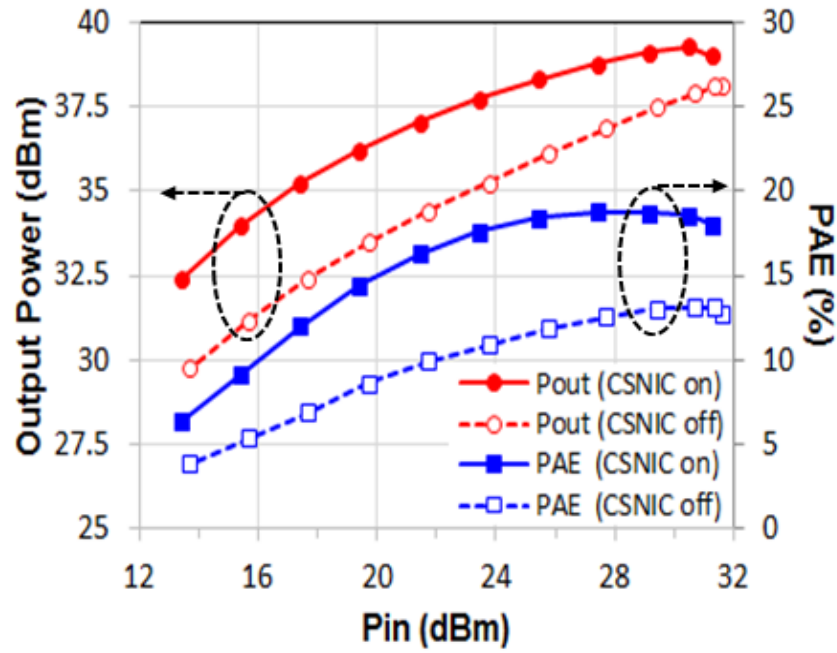
without NIC. Similar to the results of the previous chapters, S_{21} increases in the low-frequency sub-band from 6 to 11 GHz with the CSNIC. The gain improvement up to 2.5 dB can be observed at 8 GHz.

The measured power characteristics with and without CSNIC are shown in Fig. 4.16. The PA showed significant power improvement (~1.2 dB) up to 15 GHz. The output power higher than 39 dBm is achieved in the 7-17 GHz frequency range. Fig. 4.16 (b) compares the power sweep characteristics at 7 GHz with and without the CSNIC. With NIC, the output power is increased by as much as 1.2 dBm from 36.1 to 38.2 dBm and the PAE is improved by 5.7% while the PAE improvement is limited 4% and 4.5% for 2× and 4× combining PA, respectively. Since the power consumption of the CSNIC is only 2.3 to 6.6% of the total DC power (0.98 to 2.4 W) at all input power ranges, the decrease of the PAE in the upper sub-frequency band is very small.

Fig. 4.17 compares the power characteristics of 2× combining PA and NMPA with CSNIC. The average output power increased by 2.8 dB from 36.8 dBm to 39.6 dBm and the average PAE increased by 1.6% from 17.5% to 19.1%. By using CSNIC, the output power and PAE can be increased at the same time.

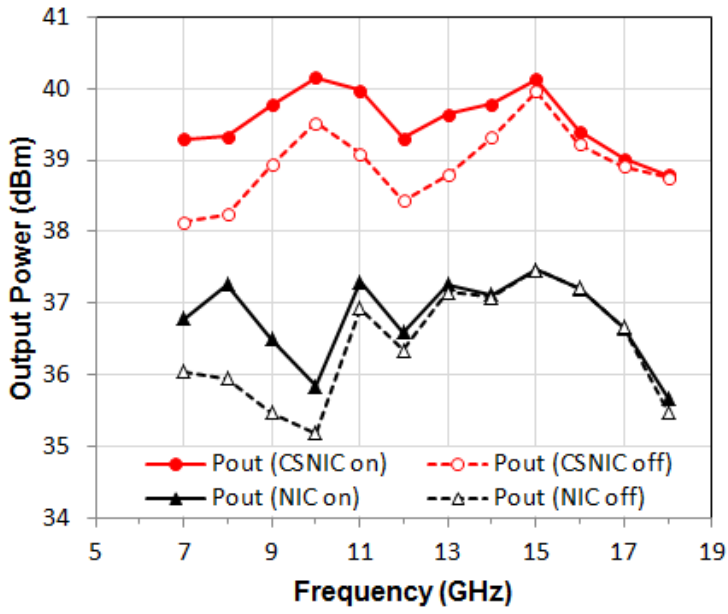


(a)

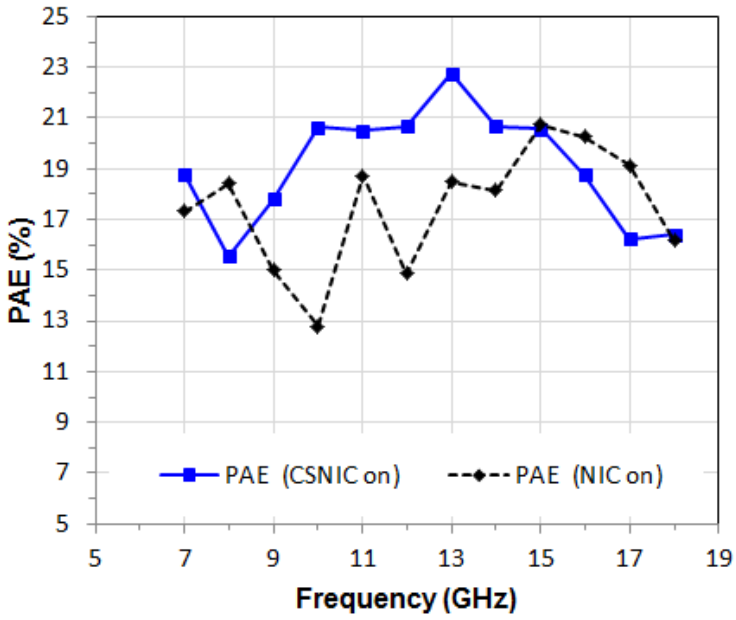


(b)

Fig. 4.16. (a) Measured output power and PAE of NMPA with and without the CSNIC, (b) Measured power sweep characteristics of NMPA with and without the CSNIC at 7 GHz.



(a)



(b)

Fig. 4.17. (a) The measured output power of 2× combining PA with NIC and NMPA with CSNIC. (b) The measured PAE of 2× combining PA with NIC and NMPA with CSNIC.

4.3.2 Frequency Limit of CSNIC

To measure the frequency limit of the CSNIC, the test patterns are fabricated (Fig. 4.18). For comparison, the NIC with 6×125 μm size TR, the NIC with 10×125 μm size TR, and the CSNIC with 10×125 μm size TR are designed. Each chip consists of a NFC and swamping network to prevent oscillation.

Fig. 4.19 (a) shows the S-parameter measurement result of the test pattern with NIC using 6×125 μm size TR. Using the NC from NIC reduces the Q-factor of the swamping network. A slight difference in the high frequency region is due to the parasitic input feeding inductance. Fig. 4.19 (b) shows the measured susceptance of the test pattern with and without NIC. The susceptance is canceled out to 11.2 GHz, which is the frequency limit.

Since the low frequency limit is associated with the power capability, it can be seen in a large-signal operation. Fig. 4.20 shows the measured power characteristics of NMPA with CSNIC. Since the output power has been shown to improve even at 6 GHz, the low frequency limit is below 6 GHz. The frequency limits of 2× and 4× combining PAs with NIC using 6×125 μm size TR were 6.5 and 7 GHz, respectively.

The high frequency limit is known from the test pattern measurement results, but the low frequency limit is indirectly known from the NMPA measurement results. In addition, the power

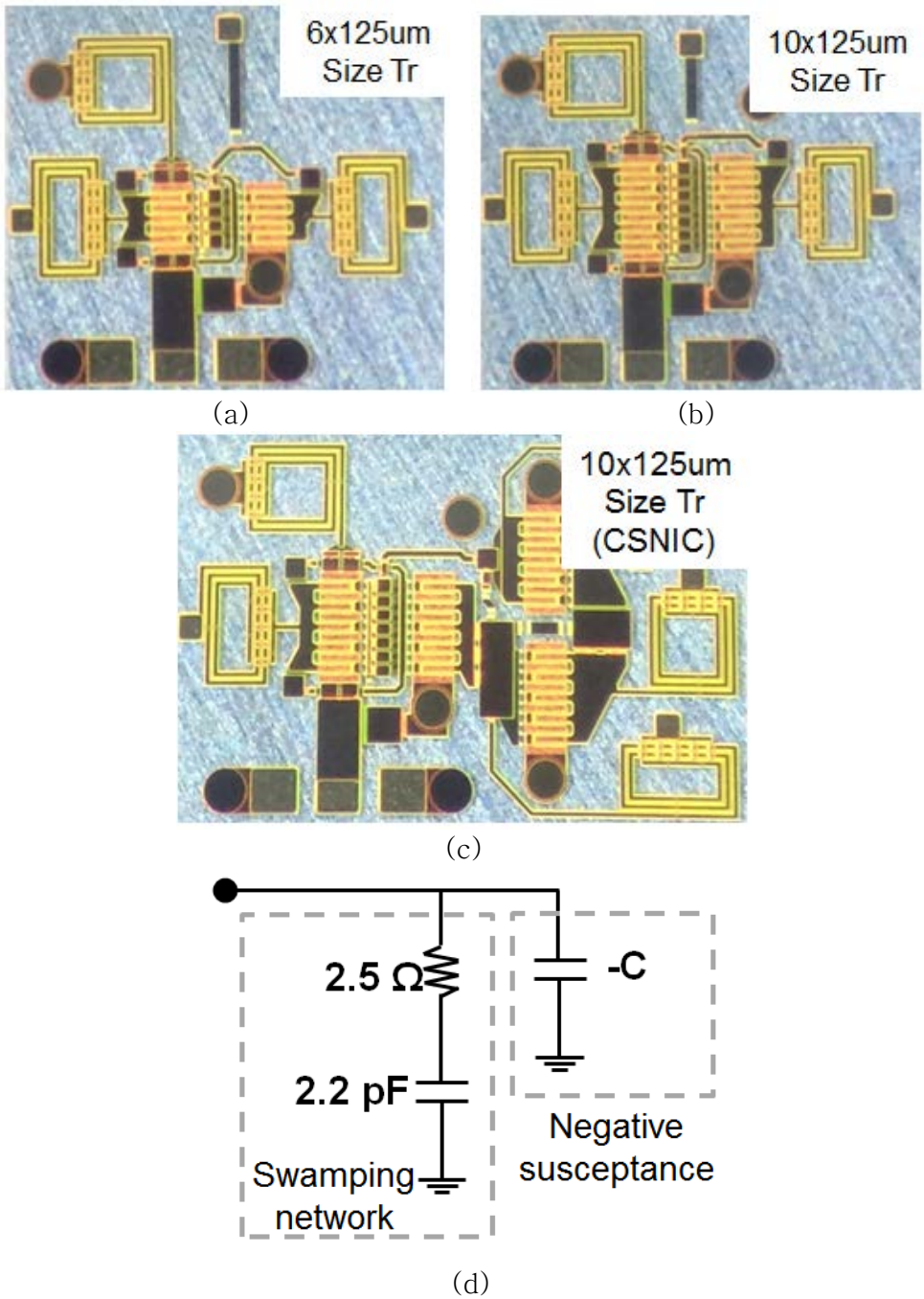
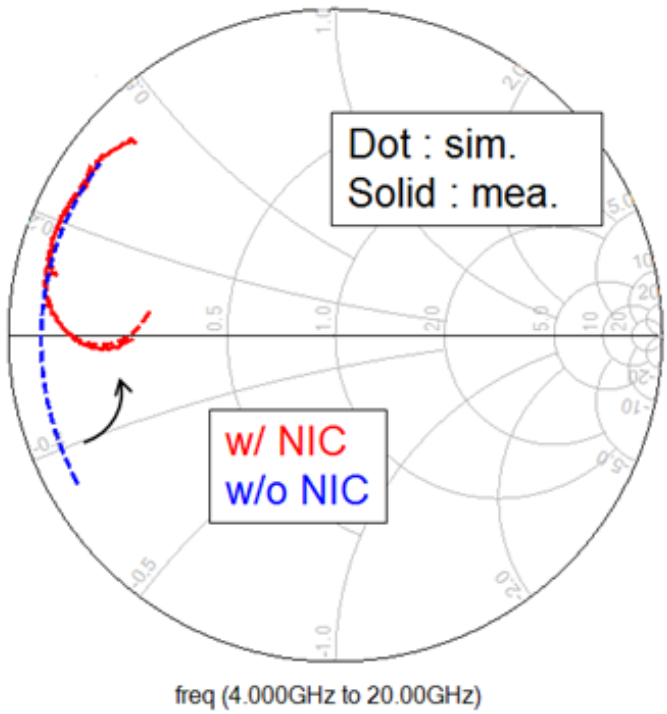
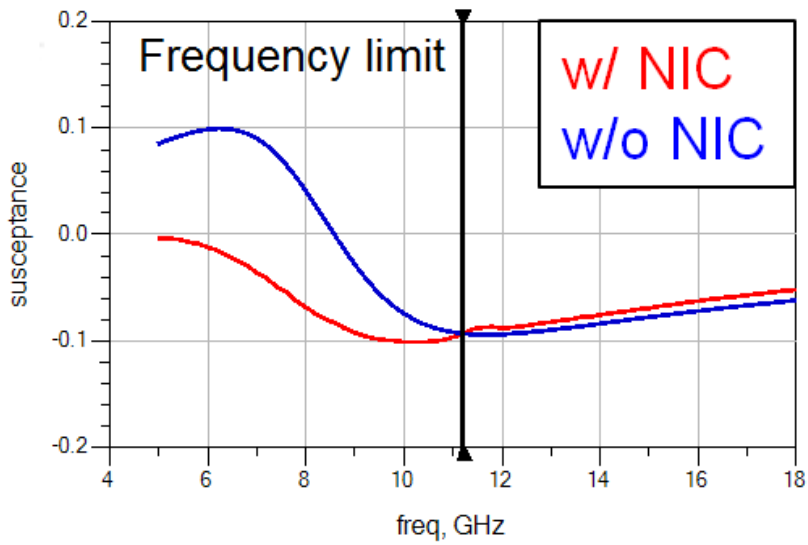


Fig. 4.18. Fabricated chip photograph of NFC test patterns. (a) NIC with 6×125 μm size TR, (b) NIC with 10×125 μm size TR, (c) CSNIC with 10×125 μm size TR, and (d) simplified equivalent circuit.



(a)



(b)

Fig. 4.19. (a) The S-parameter measurement result of the test pattern with NIC using 6×125 μm size TR. (b) The measured susceptance of the test pattern with NIC using 6×125 μm size TR.

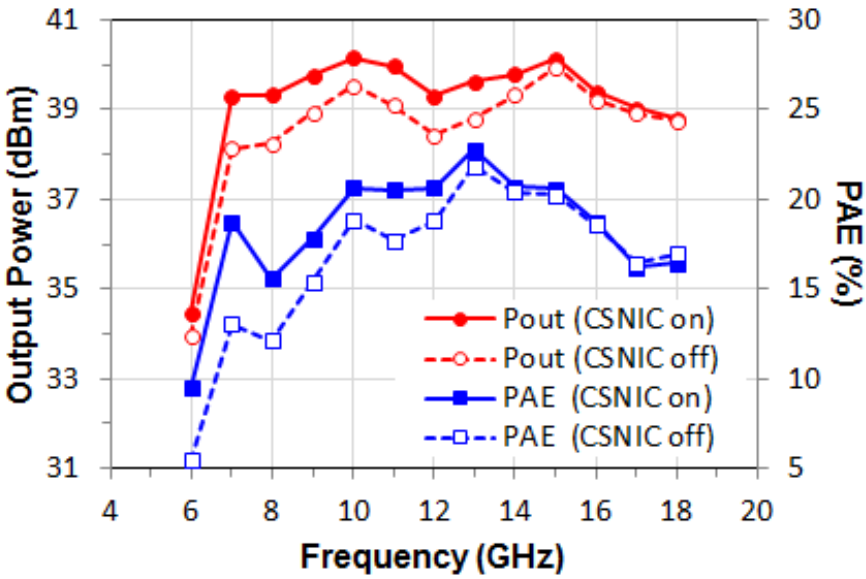


Fig. 4.20. Measured output power and PAE of NMPA with and without the CSNIC.

handling capability of NFC itself is more difficult to measure. Table 4.3 summarizes the measured NFC performance. The low frequency limit is indirectly obtained from the measurement results of 2× combining PA, 4× combining PA, and NMPA with CSNIC. The power limit value is the maximum output power by the NMPA in the low-frequency sub-band. The CSNIC overcomes the frequency and power capability limit of the NIC.

TABLE 4.3

Measured Performance Comparison of NFCs

Topology (Tr size)	High freq. Limit	Power Limit*	Low freq. Limit**
NIC (10×125um)	9.8 GHz	High	–
NIC (6×125um)	11.2 GHz	Low (6.6 W)	7.0 GHz 6.5 GHz
CSNIC (10×125um)	**11.6 GHz**	**High (10.4 W)**	**< 7 GHz**

* Unmeasurable (maximum power of PA with NFC)

** Measured with PA

4.3.3 Noise performance of CSNIC

The effect of CSNIC on the noise performance is also measured in Fig. 4.21. At the frequencies where the overall gain improves with NIC, the noise figure also improves. This trend is similar to previous NMPA noise measurements (chapter 2). Detailed noise characteristic analysis is beyond the scope of this thesis and is not covered.

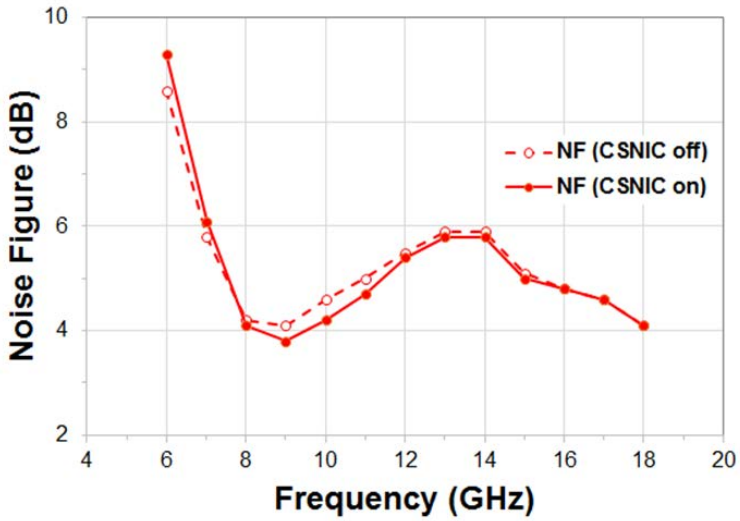


Fig. 4.21. Measured noise figure of NMPA with and without the CSNIC.

4.3.4 Comparison Table

Table 4.4 compares the performance of the NMPA of this work with the state-of-the-art DA and RMPA using GaN pHEMTs. this work shows that CSNIC can be an effective method to realize a broadband PA in a small die area without lossy matching or feedback.

TABLE 4.4

Performance Comparison of GaN Broadband PAs

	[8]	[9]	[26]	[27]	[10]	[28]	[11]	[29]	[29]	This Work
Freq. (GHz)	2–18	2–20	8–18	2–18	6–18	8–18	6–18	6–18	6–18	**7–18**
Topology	DA	DA	DA	DA	RM PA	RM PA	RM PA	RM PA	RM PA	**NM PA**
Process	0.25 μm GaN	0.2 μm GaN	0.25 μm GaN	0.2 μm GaN	0.25 μm GaN	0.25 μm GaN	0.25 μm GaN	0.25 μm GaN	0.25 μm GaN	**0.25 μm GaN**
PAE (%)	20–38	15–36	15–21	5–15	14–24	25–35	13–25	15	19	**16–23**
Pout (W)	9–15	9.9–21.6	7.9–10.9	0.8–2	3.2–20	1.25–2	6–10	20	15.1	**7.6–10.4**
Gain (dB)	10–14	9–15	12.2–14.1	18–21	17–28	7–9	18–24	9.6	9.3	**15.5–17.5**
Area (mm^2)	15.3	38	15	8	19.25	10.44	19.8	19.2	19.2	**11.66**
Power density (W/mm^2)	0.59–0.98	0.26–0.57	0.53–0.73	0.1–0.25	0.17–1.04	0.12–0.19	0.30–0.51	1.04	0.79	**0.65–0.89**

4.4. Conclusion

In this chapter, two-stage GaN NMPA with CSNIC has been developed for multi-octave broadband power applications. The frequency and power capability limitations of conventional NIC have been overcome by the use of cascaded gain cell with improved positive loop gain. Detailed analysis is performed to understand the limitation of NFC and conventional loss compensation technique for NFC. The NMPA is fabricated with 0.25-μm GaN pHEMT process and shows the output powers of 7.6-10.4 W with the PAEs of 16-23% from 7 to 18 GHz. At frequencies, where NFC is optimized for interstage matching, the power improvement by 1.2 dBm and PAE improvement by 5.7% have been achieved. This work demonstrates that the CSNIC overcomes the frequency and power capability limit of the conventional NIC.

Chapter 5

Conclusions

In this thesis, a study on broadband GaN pHEMT PA using non-Foster matching is presented.

A watt-level PA with multi-octave bandwidth is required for broadband applications such as jamming system for EW. To guarantee the high power operation, GaN device is suitable due to its high power density and high voltage operation. For broadband operation, a new wideband PA structure with high gain and high efficiency using NFC is proposed.

The bandwidth limitation from high-Q interstage matching is overcome through the use of negative capacitor, which is realized with a NIC using the cross-coupled GaN FETs. For high power operation over the entire bandwidth, the natural interstage matching is optimized for the upper sub-frequency band and the lower sub-frequency band is compensated for by the NC presented by NFC. Detailed analysis is performed to understand the frequency limitation of NIC approach, which shows that high-frequency limit

comes from the self-resonance and the low-frequency limit from the power handling capability.

To overcome the frequency and power limits of NFC, a CSNIC structure is proposed with improved positive loop gain. In addition, the cause of the NIC loss at the high frequency is also analyzed and solved using CSNIC.

Two NMPAs with NIC and a NMPA with CSNIC are fabricated with commercial 0.25-μm GaN pHEMT process. The implemented PAs show the watt-level output powers with more than 10 % of the PAE across the 6-18 GHz frequency bandwidth. This work also demonstrates that the CSNIC overcomes the frequency and power capability limit of the conventional NIC.

To our knowledge, this is the first demonstration of NIC-based broadband amplifiers with Watt-level output power. The NMPA can provide a new perspective in designing the broadband PAs.

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초록

본 학위 논문에서는 비 포스터 정합을 이용한 광대역 GaN pHEMT 전력 증폭기에 대한 연구를 제시하였다.

전자전의 대표적인 전파 공격 분야 중 하나인 재밍 시스템은 고 출력의 광대역 특성을 요구한다. 이를 위한 전력 증폭기는 멀티 옥타브 대역폭에서 동작하면서 수 와트 이상의 출력 전력을 낼 수 있어야 한다. 고 전력의 출력을 얻기 위해서, GaN 소자는 그 높은 전력 밀도 및 고전압 동작 특성 때문에 전력 증폭기에 가장 적합하다. 때문에, 본 연구에서는 GaN 소자를 통해 고 출력 전력 증폭기를 제작하였다. 또한, 광대역 특성을 얻기 위해 전력증폭기에 비 포스터 회로를 적용하는 새로운 토폴로지를 제시하였다. 비 포스터 정합을 사용하여 광대역에서 고 이득 및 고 효율을 얻어 내는 전력증폭기를 부성 임피던스 정합 전력증폭기(NMPA)라고 한다.

전력증폭기에서 대역폭의 제한은 높은 Q 값을 갖는 인터스테이지 정합에서 발생한다. 이는 교차 결합 형 GaN FET를 사용하는 부성 임피던스 변환기로 인해 구현되는 음의 커패시턴스를 통해서 극복될 수 있다. 다만, 부성 임피던스 변환기도 주파수 제한을 갖고 있기 때문에, 다음과 같은 설계 전략을 세웠다. 전력증폭기는 부성 임피던스 변환기와 관계 없이 그 자체로 상위 부 주파수 대역에서 고 출력을 내도록 최적화한다. 그리고 하위 부 주파수 대역은 비 포스터 회로에 의해 제공되는 음의 커패시턴스에 의해 그 손실을 보상한다. 이 전략을 위해서 부성 임피던스 변환기의 주파수 제한에 대한 상세한 분석이

수행되었다. 부성 임피던스 변환기의 주파수 제한은 자체 공진 현상과 전력 수용 능력의 한계에서 비롯된다는 것을 분석하였다.

이에 더 나아가, 비 포스터 회로의 주파수 및 전력 한계를 극복하기 위해, 향상된 양의 되먹임 이득을 갖는 캐스케이드 된 스테이지 부성 임피던스 변환기(CSNIC) 구조를 제한하였다. 또한 고주파에서 부성 임피던스 변환기의 손실의 원인을 분석하고 CSNIC를 사용하여 해결하였다.

NIC가 사용된 두 개의 NMPA와 CSNIC가 사용된 NMPA가 상용 0.25μm GaN pHEMT 공정으로 제작되었다. 제작된 2× 결합 전력증폭기는 6−18 GHz에서 13−21%의 전력 추가 효율(PAE)과 35.7−37.5 dBm의 출력 전력을 보였다. 4× 결합 전력증폭기는 7−17 GHz에서 5 W 이상의 출력을 제공하였다. CSNIC가 사용된 NMPA는 7.6−10.4 W의 출력 전력을 보이면서 7−18 GHz에서 16−23%의 PAE를 나타내었다. 비 포스터 회로는 하위 부 주파수 대역에서 1.2 dBm의 출력 전력 향상과 5.7%의 PAE 개선을 보여주었다. 비 포스터 회로는 손실 정합 또는 음의 되먹임을 사용하지 않고도 광대역 성능을 달성할 수 있었다. 그 결과 약 12 GHz 이하의 주파수에서 효율 및 출력 전력이 향상되었다. 또한 CSNIC가 기존 부성 임피던스 변환기의 주파수 및 전력 수용 능력 한계를 극복하였음을 보여주었다.

본 연구는 와트 레벨 출력 전력을 갖춘 광대역 전력증폭기에 부성 임피던스 변환기를 적용한 첫 시도이다. NMPA는 광대역 전력증폭기 설계에 새로운 시각을 제공하였다.