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Ph.D. DISSERTATION

GaN Non-uniform Distributed Power Amplifier
Design for enhanced power and efficiency

 출력전력 및 효율 향상을 위한 질화갈륨 분산전력증폭기 설계

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Abstract

In this thesis, I propose a non-uniform distributed power amplifier design (NDPA) for enhanced power and efficiency using a commercial gallium nitride (GaN) semiconductor process to realize a wideband power amplifier which is an essential component of electronic warfare systems such as active electronically scanned array (AESA) radars and electronic jammers.

First, large signal modeling including thermal effect which is the basis of the NDPA design is carried out. DC and RF measurements are performed on a 6×125 μm GaN high-electron-mobility transistor (HEMT) and the measured data are fitted to Angelov-based model equations. Also, a thermal model equivalent circuit is constructed by extracting the thermal resistance through the pulsed IV measurement, and the RF $I_{ds}$ and the DC $I_{ds}$ are separately modeled to reflect the frequency dispersion phenomenon. The thermal resistance is measured by thermally pasting the device on the same jig so as to be similar to the actual monolithic microwave integrated circuit (MMIC) measurement environment. For the model verification, a 6 ~ 18 GHz, 8.1 W uniform distributed power amplifier (DPA) MMIC is designed and compared with the measurement. The output power characteristics of DPA which is designed by in-house GaN HEMT large signal model show better agreement with the measured value than those by the model provided by the foundry.

Second, to increase output power in the wideband, the previous NDPA design is modified. The conventional NDPA design method assumes that the drain-source capacitance ($C_{ds}$) is absorbed in the transmission line. However, the larger the transistor size is and the higher the frequency, the more its effect cannot be ignored. Also, in the process of arranging the drain line impedance so that each transistor in the NDPA has the optimum output load impedance ($R_{opt}$), the first drain line
impedance usually becomes greater than 100 Ω, which causes a problem that the metal line width is too narrow to be fabricated by a commercial process. The conventional NDPA design uses a large-sized transistor at the first section to avoid this limitation so that increased gate-to-source capacitances and drain-to-source capacitances degrade power gain and output power at high frequencies. In this study, an NDPA design is proposed that reflects the drain-source capacitance. After the $C_{ds}$ is added to the existing drain line impedance to make an equivalent model with the π-type line, the line impedance is readjusted to have the $R_{opt}$ at the center frequency. By applying this design method to the NDPA, the average output power could be improved by 0.4 dB at 6 – 18 GHz than the conventional method. Besides, instead of using a large-sized transistor at the first section in the NDPA, a method of halving the characteristic impedance ($Z_0$) by doubling the phase of the drain line is proposed. As a result of analyzing loss due to the increase of the line length, the high-frequency loss is reduced compared with the conventional method, and power gain and the output power characteristics close to the ideal NDPA’s can be obtained. Meanwhile, to further increase output power, NDPAs are required to be power-combined. In this case, there has been a problem that due to long gate/drain lines, the chip size becomes large. In this work, a compact power combining scheme is proposed that shares the drain lines of each NDPA. Sharing the drain lines reduces the chip size and loss by decreasing the number of impedance transformers and power combiners required for power combining. Moreover, it reduces the line length by half if the line impedance is kept as the same impedance as before sharing the drain line. Because this approach increases the compactness in the power combining, it contributes to increasing the power density of NDPAs. Besides, the shared drain line allows the drain-to-source resistance ($R_{ds}$) of each transistor to be connected in parallel, thus providing additional benefit to improve the output return loss when using large size devices. The proposed design method is applied to NDPA MMICs using commercial 0.25
μm GaN MMIC process. A 2-way, 2-stage, and 8-section NDPA MMIC is designed using 6×125 μm GaN HEMT devices. As a result, the fabricated MMIC shows the linear gain of 16.8 ~ 21.8 dB, the continuous wave (CW) output power (P_{out}) of 21 W and the power added efficiency (PAE) of 19.2 % at 6 ~ 18 GHz. In particular, it accomplishes the highest power density of 1.9 W/mm² in similar broadband frequency bands. A 4-way, 2-stage NDPA MMIC is also designed and fabricated by extending the proposed power combining structure. Because the number of power combining is increased to 4, a 6×75 μm GaN HEMT device is used instead of a 6×125 μm. It shows the linear gain of 13 ~ 17 dB, the average CW P_{out} of 20.8 W and the average PAE of 14 % at 6 ~ 18 GHz. In particular, the average P_{out} of 26 W is measured at the pulsed power measurement, and the maximum P_{out} of 40 W is obtained at 13 GHz. The proposed compact power combining scheme allows four NDPAs to be power-combined, resulting in the highest output power characteristics in similar broadband frequency bands. From the above results, the validity and effectiveness of the proposed NDPA design method can be verified.

Third, an NDPA design for enhanced power efficiency is proposed. To obtain high efficiency in the NDPA, power gain needs to be increased. Varying the gate line termination resistance (R_{gt}) in the NDPA can increase power gain according to frequencies. When designing an NDPA, drain line termination resistors are usually eliminated to prevent output power and efficiency from degrading due to power loss through termination loads. In this case, the reflected wave components of the gate line and the drain line, which have been neglected are increased according to the magnitude of R_{gt} as shown in the power gain expression of the distributed amplifier theory, thereby forming ripples of power gain depending on the frequency. Using these ripples, power efficiency can be improved when the power gain is increased at a desired frequency. However, when the NDPA MMIC is fabricated using the proposed idea, the P_{out} and PAE of NDPA are only increased by 0.22 dB and 1.2%,
respectively. Simulation results show that the peak power gain decreases when the NDPA operates under low $R_{gt}$ due to gate line loss. The reduced peak gain degrades NDPA’s PAE. To compensate for this degradation, an inductive line is inserted in front of the $R_{gt}$ to improve the input return loss. On the other hand, as the operating frequency increases in the NDPA, the $R_{opt}$ for determining the drain line impedance is observed to increase. As a result, the maximum output power cannot be obtained according to the frequency, and mismatch occurs, which degrades the overall power efficiency. To make up for this mismatch, the four drain line impedances of the front end are designed according to the $R_{opt}$ of 6 GHz, and the four drain line impedances of the rear end are designed according to the $R_{opt}$ of 18 GHz. This rearrangement of the drain line impedances is because the transistors and drain lines on the rear end of the NDPA are more susceptible to high frequencies. Simulation results show that the proposed design method improves $P_{out}$ by 0.3 dB and PAE by 2.8% at 6 ~ 18 GHz. The proposed design concepts are applied to the second fabrication of the NDPA MMIC. As a result, the average $P_{out}$ is 39.8 dB, and the average PAE is 20% at 6 ~ 18 GHz. When the $R_{gt}$ is tuned according to the frequency, there is the $P_{out}$ improvement of 0.3 dB and the PAE improvement of 2.3%. Notably, at 13 GHz, the $P_{out}$ is improved by 1.24 dB and the PAE is increased by 6.8% when the $R_{gt}$ is optimally tuned. In conclusion, the insertion of inductive line and drain line impedance re-design considering frequency-dependent optimum load impedance improve the average $P_{out}$ of 0.9 dB and the average PAE of 6.5% compared to the first MMIC in operating frequency band. Also, the PAE’s increment when the $R_{gt}$ is optimally tuned is improved by 1.1%. When compared to the conventional NDPA using the same process, the proposed efficiency enhanced design increases the PAE by 3%. It is verified that the proposed idea contributes to the power efficiency improvement of the NDPA. Then an additional circuit is designed for automatically switching the $R_{gt}$ depending on the frequency. A part of the input signal is taken in a
10 dB coupler and passed through a Wilkinson power divider to allow one signal to be used to sense the input RF power and the other to enter the power detector. Then the same circuit as the gate lines of the NDPA is separately made using MMIC test patterns and shunt-connected to the front of the power detector. This circuit is to reproduce the standing wave caused by the mismatch of the gate line termination in the NDPA according to frequencies, so that the power detector can read the voltage swing generated here, so that frequency-dependent (or, gain-ripple dependent) voltage values are generated. If generated voltages are amplified by the op-amp and then input to the comparator and compared with the reference voltage, the desired voltage can be generated so that the gate line termination resistance is switched in the direction that the $P_{out}$ of the NDPA is higher at the desired frequency. Finally, the generated voltage enters the gate port of the variable resistance transistor. As a result of the experiment, it is confirmed that the NDPA operates at the ideal $R_{gt}$ value in the frequency band where the power efficiency difference is large according to the $R_{gt}$, and the reduction of PAE due to the voltage generation error is only average 0.1 % in the operating frequency band. Therefore, it is verified that the efficiency of NDPA can be improved through the programmable gate line termination resistance switching technique and the drain line impedance re-design considering frequency-dependent $R_{opt}$.

In this thesis, the NDPA design method is improved, and a novel NDPA is implemented with average output power of 20 W or more and power density of 1.9 W/mm$^2$ at 6 ~ 18 GHz. The newly proposed programmable gate line termination resistance switching technique accomplishes a wideband power amplifier with an average output power of 10 W and an average power added efficiency of 20% or more at 6 ~ 18 GHz.

**Keywords:** GaN, non-uniform distributed amplifier, power combining, wideband,
power added efficiency (PAE), MMIC

**Student number**: 2003-21561
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Chapter 1

Introduction

1.1 Motivation

Watt-level power amplifiers (PAs) with the octave bandwidth are prerequisite components to electronic warfare systems such as an active electronically scanned array (AESA) and a radar jammer as shown in Fig. 1 (a) and (b) [1]. Usually, tens of watts of RF power through the octave bandwidth is required to meet the output power specification of electronic warfare systems.

Fig. 1.1. (a) Active electronically scanned array (AESA) radar system (b) radar jammers in electronic warfare.

Because GaN has the wide bandgap property and the high charge density with competitive mobility and saturation velocity with GaAs, GaN devices can operate in
high voltage and high current mode at RF frequencies as shown in Fig. 2 (a) and (b) [2], [3]. Thus, GaN PAs have great advantages for wideband PAs. During the past decade, wideband GaN PAs have been actively researched, so that they arise as a substitute for bulky traveling wave tube amplifiers (TWTAs) [4]-[13].

<table>
<thead>
<tr>
<th>Property</th>
<th>Si</th>
<th>GaAs</th>
<th>SiC</th>
<th>GaN</th>
</tr>
</thead>
<tbody>
<tr>
<td>Energy Gap (eV)</td>
<td>1.11</td>
<td>1.43</td>
<td>3.2</td>
<td>3.4</td>
</tr>
<tr>
<td>Critical Electric Field (MV/cm)</td>
<td>0.3</td>
<td>0.5</td>
<td>3.0</td>
<td>3.5</td>
</tr>
<tr>
<td>Charge Density (# x 1x10^{13}/cm^2)</td>
<td>0.3</td>
<td>0.3</td>
<td>0.4</td>
<td>1</td>
</tr>
<tr>
<td>Thermal Conductivity (W/cm/K)</td>
<td>1.5</td>
<td>0.5</td>
<td>3.7</td>
<td>1.5</td>
</tr>
<tr>
<td>Mobility (cm^2 /V/s)</td>
<td>1350</td>
<td>8000</td>
<td>900</td>
<td>1500</td>
</tr>
<tr>
<td>Saturation Velocity (x10^7 cm/V)</td>
<td>1</td>
<td>1.4</td>
<td>2</td>
<td>2.7</td>
</tr>
</tbody>
</table>

(a)

(b)

Fig. 1.2. (a) GaN’s characteristics as power devices (b) Device’s power density.

Wideband PAs are largely divided to reactive matched PAs (RMPAs) and distributed amplifiers (DAs). Most recently, wideband GaN PAs with non-Foster circuit have been developed to mitigate the bandwidth limitation due to high-Q interstage matching [12]. Nevertheless, DAs are still attractive in that they can
provide the ultra-wideband performance as transistor parasitic components can be absorbed as a part of transmission lines. Also, they are advantageous to multiple power combining as they do not need the bulky output load matching circuits. Recently, compact power-combined DA with high power density is demonstrated [14].

It is desirable that all of the FET cells look an optimum load to maximize output power in the DA. A NDPA theory achieves this principle by tapering the characteristic impedances of each stage’s drain lines [5], [15]. According to a NDPA theory, in the process of arranging the drain line impedance so that each transistor in the NDPA can have the optimum output load impedance ($R_{opt}$), the first drain line impedance usually becomes greater than 100 $\Omega$. It causes a problem that the metal line width is too narrow to be fabricated by a commercial process. The conventional NDPA design uses a large-sized transistor at the first section to avoid this limitation.

The output power of a NDPA is limited by the fixed FET periphery. If NDPAs want to obtain higher power, load impedances should be lowered and the total FET periphery should be increased. Thus, NDPA should consist of larger-sized FETs which have larger parasitic capacitances. In this condition, NDPA design needs to be modified. The conventional NDPA design assumes that the drain-source capacitance ($C_{ds}$) is absorbed in the transmission line. However, the larger the transistor size is and the higher the frequency, the more its effect cannot be ignored. Also, the usage of a large-sized transistor at the first section degrades power gain and output power at high frequencies due to increased gate-to-source capacitances and drain-to-source capacitances. In the proposed NDPA, the drain-source capacitance is included in designing the optimum drain line impedance. Besides, the new design approach to
avoid the usage of the large-sized transistor at the first section in the NDPA is proposed.

The power added efficiency is another important specification of wideband PAs. Especially, because GaN PAs operate under high voltages more than 25 V, they may require bulky DC power supplies according to current consumption. It determines the volume and portability of overall electronic warfare system. Unfortunately, both RMPAs and DAs have shown poor PAE as they cannot adopt conventional efficiency enhancement techniques such as harmonic tuning to wideband operation. In a few reported NDPAs, the NDPA has obtained PAE over 20 % but it has been fabricated by the internal advanced GaN MMIC process with the excellent GaN HEMT’s maximum oscillation frequency ($f_{\text{MAX}}$) [5]. Although a specific group improves PAE by proposing the stage-scaled DA design topology, the enhanced PAE is only 2 % at specific frequencies and it could not be applied to NDPA [16]. In this work, the programmable gate line termination resistance switching technique (PGT) is proposed as the PAE enhancement technique in the NDPA.

As a result, the proposed modified-NDPA provides output power and PAE better than the conventional NDPA.
1.2 Dissertation organization

Fig. 1.2 is a block diagram that shows the scope of this dissertation of general wideband GaN PA architectures.

In chapter 2, large signal modeling including thermal effect which is the basis of the NDPA design is carried out. DC and RF measurements are performed on a 6 × 125 μm GaN high-electron-mobility transistor (HEMT) and the measured data are fitted to Angelov-based model equations. For the model verification, a 6 ~ 18 GHz, 8.1 W uniform distributed power amplifier (DPA) MMIC is designed and compared with the measurement. The output power characteristics of DPA which is designed by in-house GaN HEMT large signal model show better agreement with the measured value than those by the model provided by the foundry.

In Chapter 3, to increase output power in the wideband, the previous NDPA design is modified. In this chapter, the conventional NDPA design is analyzed so that the increased capacitances degrade output power at high frequencies. An NDPA design is proposed that considers the effect of the drain-source capacitance and a method of halving the characteristic impedance (Z₀) by doubling the phase of the drain line is proposed. To further increase output power, a compact power combining scheme is proposed that shares the drain lines of each NDPA. The proposed design method is applied to NDPA MMICs using commercial 0.25 μm GaN MMIC process. A 2-way and a 4-way NDPA MMIC are designed and fabricated commercial 0.25 μm GaN MMIC process. From the measurement results, the validity and effectiveness of the proposed NDPA design method could be verified.

Chapter 4 focuses on the NDPA design for enhanced power efficiency. The newly proposed programmable gate line termination resistance switching technique is
explained. When the NDPA MMIC is designed and fabricated using the proposed idea, the power added efficiency of NDPA could be improved by the programmable gate line termination resistance switching technique. Programmable gate line termination resistance switching technique implementation to non-uniform distributed amplifiers is also introduced.

In chapter 5, pulsed power measurement to avoid thermal limit is explained. The fabricated NDPA MMICS are measured and compared by CW and pulsed power measurements.

Finally the dissertation ends with conclusions in Chapter 6 which summarizes the modified NDPA design techniques, demonstrated in this dissertation.

Fig. 1.3. Wideband GaN PA architectures and the scope of this work.
1.3 References


Chapter 2

Basic theory and background of GaN Distributed Power Amplifiers

2.1 Introduction

A wideband RF power amplifier (PA) is an essential component in many RF applications, such as electronic warfare (EW) systems and security communications. In the past, the traveling wave tube amplifier (TWTA) has been most commonly used to achieve wideband output power above watt levels [1], [2]. However, the emergence of GaN PAs raises the prospect of replacing bulky TWTA with compact solid state power amplifiers (SSPAs) [3]. GaN high-electron-mobility transistors (HEMTs) have several inherent advantages, including high breakdown voltage, high current density, and high saturation velocity resulting from their wide band gap properties [4]. Unfortunately, unlike GaAs or InP HEMTs, GaN HEMTs have a large power dissipation, which causes a prominent self-heating phenomenon that degrades the RF performance of devices [5]. Thus, the self-heating effect must be considered when designing wideband RF GaN PAs. An accurate large-signal model that includes a thermal model therefore becomes an inevitable requirement. Large-signal models provided by the foundry service are still not mature and do not guarantee
model accuracy up to frequencies close to the maximum oscillation frequency ($f_{m\text{AX}}$). In-house large-signal modeling should definitely be performed, based on measured data. This paper describes the development of in-house large-signal models of a GaN HEMT that include a thermal model.
2.2 GaN HEMT Large Signal Modeling including Thermal Effect

2.2.1 Angelov based Large Signal Model

Our in-house models are based on an Angelov model [6], [7]. Fig. 2.1 shows an Angelov model-based GaN HEMT large-signal equivalent circuit including a thermal model. Our in-house models consist of the Angelov model library supported by Keysight’s ADS 2013 program and thermal sub-circuits [10]. Thermal sub-circuits inform a temperature-dependent large-signal model of the channel temperature raised by $R_{th}$. In particular, our in-house models incorporate a nonlinear drain current ($I_{ds}$) that is divided into a nonlinear drain DC current ($DC\ I_{ds}$) and a nonlinear drain RF current ($RF\ I_{ds}$). This expression can make the $I_{ds}$ models reflect the frequency dispersion effect [11]. At high frequencies above a few megahertz, the $RF\ I_{ds}$ is activated through virtual inductances in the equivalent circuit model.

![Fig. 2.1. Angelov model-based GaN HEMT large-signal model including thermal model.](image)
Equations for the DC Ids are defined in (1) – (10). Each model parameter is optimized and fitted in comparison with measured DC-IV curves and S-parameters by ADS 2013. The RF Ids uses the same equation as the DC Ids. Nonlinear capacitances \((C_{gs}, C_{gd}, \text{and } C_{ds})\) are fitted to well-known Angelov’s nonlinear capacitance model equations [6].

\[
\text{DC } I_{ds} = I_{pk0,T}(1 + \tanh(\psi)\tanh(\alpha V_{ds})(1 + \lambda V_{ds})
\]

(1)

\[
I_{pk0,T} = I_{pk0}(1 + TCI_{pk0}(T - T_0))
\]

(2)

\[
\psi = P_{1m}(V_{gs} - V_{pkm}) + V_{eff1} + V_{eff2}
\]

(3)

\[
P_{1m} = P_{1r}\left(1 + \frac{B_t}{\cosh(B_2 V_{ds})^2}\right)
\]

(4)

\[
P_{1,T} = P_1(1 + TCP_1(T - T_0))
\]

(5)

\[
V_{pkm} = V_{pks} - DV_{pks}(1 - \tanh(\alpha V_{ds}))
\]

(6)

\[
V_{eff1} = P_{21}\left(\frac{V_{gst} - V_{gsta}}{2}\right)^2 + P_{22}\left(\frac{V_{gst} + V_{gsta}}{2}\right)^2
\]

(7)

\[
V_{eff2} = P_{31,dc}\left(\frac{V_{gst} - V_{gsta}}{2}\right)^3 + P_{32}\left(\frac{V_{gst} + V_{gsta}}{2}\right)^3
\]

(8)

\[
\alpha = A_1 + A_2(1 + \tanh(\psi))
\]

(9)

\[
V_{gst} = V_{gs} - V_{pkm}
\]

(10)

\[
V_{gsta} = \text{constant}
\]

(11)

Fig. 2.2 shows the large-signal modeling procedures. First, DC-IV curves are measured in a device under test (DUT) by an HP 4142B DC source and a Keysight’s IC-CAP program. The sample dies of GaN HEMT, provided by the foundry service, are used as DUTs. The S-parameter is then measured by a vector network analyzer.
(VNA). The extrinsic parameters and intrinsic parameters are extracted separately by performing hot and cold measurements, respectively. The small-signal model parameters are then extracted from the measured S-parameters according to multiple biases.

Nonlinear large-signal model parameters, such as gate-source capacitances \( (C_{gs}) \), gate-drain capacitances \( (C_{gd}) \), drain-source capacitance \( (C_{ds}) \), DC \( I_{ds} \), and RF \( I_{ds} \), are modeled by Angelov model-based tangent-hyperbolic equations. In addition, the thermal effect is reflected by performing a pulsed IV measurement using a DIVA D265 instrument and a thermal chuck. A thermal resistance \( (R_{th}) \) is extracted using the pulsed IV measurement method [8], [9]. The thermal resistance is measured by thermally pasting the device on the same jig so as to be similar to the actual monolithic microwave integrated circuit (MMIC) measurement environment. Fig.
2.3 (a) and (b) shows the power dissipation versus drain current on the condition of isothermal state and the temperature versus drain current on the condition of no power dissipation. From Fig. 2.2, the extracted $R_{th}$ is $21.4 \degree C/W$. Compared to the same-sized GaN HEMTs on the on-wafer whose $R_{th}$ is $36.9 \degree C/W$, it is lowered due to the thermal attachment.

The DC $I_{ds}$ is fitted, including the extracted $R_{th}$, to represent negative current slopes by the thermal effect under high drain voltage and high drain current regions. The RF $I_{ds}$ is measured under a quiescent bias condition and fitted to the RF $I_{ds}$ equations. An initially-equipped large-signal model is verified by comparison with the measured DC $I_{ds}$, RF $I_{ds}$, and S-parameters. Finally, the complete model is optimized by some iterations of the above procedures. The size of the GaN HEMT for large-signal modeling is selected as 6 (fingers) × 125 $\mu m$ (gate width) under the criteria of $F_{max}$ over 20 GHz and load pull power over 34 dBm from 6 to 18 GHz. The extracted $I_{ds}$ model parameters are summarized in table 2.1

![Fig. 2.3. Pulsed power measurement for $R_{th}$ extraction (V$_{ds} = 10V$, pulse width = 200 ns, pulse period = 1 ms) (a) power dissipation vs drain current (b) temperature versus drain current.](image)
TABLE 2.1
MODEL PARAMETERS IN NONLINEAR DRAIN CURRENT EQUATIONS OF 6×125 μM GAN HEMTS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>DC</th>
<th>RF</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{pk0}$ (A)</td>
<td>0.35</td>
<td>0.308</td>
</tr>
<tr>
<td>$T_{Cl pk0}$</td>
<td>0.0024</td>
<td>-0.002</td>
</tr>
<tr>
<td>$P_1$</td>
<td>0.013</td>
<td>0.047</td>
</tr>
<tr>
<td>TCP</td>
<td>0.152</td>
<td>0.004</td>
</tr>
<tr>
<td>$B_1$</td>
<td>1.45</td>
<td>1.37</td>
</tr>
<tr>
<td>$B_2$</td>
<td>0.155</td>
<td>0.054</td>
</tr>
<tr>
<td>$V_{pks}$ (V)</td>
<td>3.40</td>
<td>3.99</td>
</tr>
<tr>
<td>$DV_{pks}$ (V)</td>
<td>0.0001</td>
<td>0.6744</td>
</tr>
<tr>
<td>$A_1$</td>
<td>0.002</td>
<td>0.000</td>
</tr>
</tbody>
</table>

Fig. 2.4 shows a comparison of the DC-IV curves between the measurements and the models, measured at drain voltages ($V_{ds}$) of 0 ~ 36 V and gate-source voltages ($V_{gs}$) of -3.6 ~ -1.6 V. The in-house model shows better agreement with the measured data than is observed with the model provided by the foundry service. Fig. 2.4 shows an RF $I_{ds}$ according to temperature. Under 24 V of a quiescent drain voltage ($V_{dsq}$) and -2.0 V of a quiescent gate voltage ($V_{gsq}$), a pulsed $I_{ds}$ is measured and an RF $I_{ds}$ equation is fitted. The pulse width is 200 ns. The in-house model predicts a reduced RF $I_{ds}$ when temperature increases.
Fig. 2.4. Comparison of DC-IV curves between measurements and models (GaN HEMT $6 \times 125 \, \mu m$, $V_{ds}$: $0 \sim 36 \, V$, $V_{gs}$: $-3.6 \sim -1.6 \, V$).

(a)  

(b)  

Fig. 2.5. RF $I_{ds}$ according to temperature (GaN HEMT $6 \times 125 \, \mu m$, $V_{dsq}$: $24 \, V$, $V_{gsq}$: $-2.0 \, V$, solid: model, circle: measurement) (a) temperature $= 25 \, ^\circ C$, (b) temperature $= 85 \, ^\circ C$.  

16
2.2.2. Model Verification

Fig. 2.6. Comparison of S-parameters between measurements and models (GaN HEMT 6 × 125 μm, V_{ds}: 24 V, V_{gs}: -2.0 V, frequency range: 0.5 ~ 60 GHz).

Fig. 2.7. Comparison of the optimum load pull contour at 10 GHz (GaN HEMT 6 × 125 μm, V_{ds}: 28 V, I_{ds}: 70 mA, P_{in}: 24 dBm).

Fig. 2.5 represents the comparison between the measured S-parameters and the simulated S-parameters from 0.5 to 60 GHz. As shown in Fig. 2.5, the in-house
model shows better agreement with the measured data up to high frequencies at S22 when compared to the model provided by the foundry service. This results from the exact RF Ids modeling by the pulsed IV measurement. Finally, a load pull data at 10 GHz is compared between the measurement and the model. As shown in Fig. 2.7, the in-house model predicts a more realistic output power than is obtained with the model provided by the foundry service. This result confirms the validity of our large-signal model that includes a thermal model [16].
2.3 GaN uniform distributed power amplifier design

2.3.1 Circuit design

DAs show good potential for high power density, as they do not require the bulky output load matching circuits that are indispensable to conventional PAs. Size-efficient GaN PA design is important because making SSPAs more compact reduces GaN foundry costs. Previously reported GaN DA MMICs, while showing excellent output power from C-band to Ku-band [11–13, 15], have not considered the issue of efficient chip size. This circuit proposes a size-efficient GaN DA for output power densities higher than those achieved in previous studies.

The main reasons GaN DAs are bulky are their long gate/drain lines and the sparse distribution of FETs in a line [11–13, 15]. Most of the reported GaN DAs have removed drain line termination resistances to minimize power loss. This requires more careful design of wideband output matching. Fig. 2.8 shows the simplified equivalent circuit of drain lines in DAs without drain line termination impedances. Arranging small-sized FETs in the DA increases the cut-off frequency due to reduced drain–source capacitances (C_ds) and increased output resistances (R_ds). However, to obtain high power above watt-level, the number of FETs in a line should be increased. On the other hand, large-sized FETs require long drain lines to maintain the same characteristic impedance due to increased C_ds. The cut-off frequency decreases accordingly. Hence, both cases commonly result in bulky DAs.
As shown in Fig. 2.8 output impedance ($Z_{out,n}$) in the DA without drain line termination impedances can be calculated as follows:

$$Z_{out,n} = \frac{(R_{dsn} // C_{dsn}) // Z_{out,n-1} + j\omega L_d}{1}$$  \hspace{1cm} (12)$$

Decreasing the size of the $n^{th}$ FET increases $Z_{out,n}$, because $R_{dsn}$ increases and $C_{dsn}$ decreases. This is helpful to achieve wideband output matching without any drain line termination impedances or extra impedance transformers. Moreover, as the first term of (1) increases, the drain line inductance ($L_d$) needed for matching decreases. This helps reduce the length of drain lines. Fig. 2.9 represents improved output return loss when unequal-sized FETs are applied in the DA. When equal-size FETs are used, $L_d$ needs to be doubled (thereby increasing drain line length) to improve output return loss; however, the cut-off frequency is reduced. Fig. 2.10 shows the schematic of the proposed GaN DA. It comprises two DAs in cascade. A main power stage consists of a DA with eight gain cells. Without drain line termination impedances, the proposed DA mostly uses $6 \times 125 \mu m^2$ GaN HEMTs, but the last two sections have
$2 \times 125 \, \mu\text{m}^2$ GaN HEMTs. Owing to the use of small-sized FETs in the last two sections, a $10 \times 125 \, \mu\text{m}^2$ GaN HEMT is used in the first section to maintain the total

Fig. 2.9. Calculated output return loss of equal-sized FET DAs and unequal sized FET DAs.

Fig. 2.10. Schematic of the proposed GaN DPA.
FET periphery of the DA. As shown in Fig. 2.11, when the DA adopts unequal-sized FETs, overall output power ($P_{\text{out}}$) is enhanced by 1 dB in comparison with the DA, which adopts equal-sized FETs. This enhancement reflects the boost in gain achieved by the improved output matching.

![Simulated DA output power and linear gain against frequency](image)

Fig. 2.11. Simulated DA output power and linear gain against frequency ($P_{\text{in}} = 30$ dBm, $V_{D1}=V_{D2} = 27$ V, $V_{G1}=V_{G2} = -2.4$ V).

### 2.3.1 Measurement results

The proposed circuit has been fabricated using a commercial 0.25 μm GaN HEMT MMIC process with $f_T$ of 23 GHz and $f_{\text{MAX}}$ of 65 GHz. Fig. 2.12 is a die photograph of the proposed DA, whose size is 3.7 mm × 1.8 mm containing probe pads. Notably, the main stage DA occupies only 3.0 mm × 0.7 mm. The use of unequal sized FETs in output matching reduces the length of drain lines. To keep the same phase, the gate-line lengths are also reduced proportionally. Reduced drain and gate lines also enable source via holes of GaN HEMTs to be shared, reducing chip size. Fig. 2.13 shows the measured S-parameter of the fabricated DA. The DA shows power gains...
higher than 10 dB from 2 to 19 GHz with a peak gain of 15.1 dB at 13.6 GHz. Input return loss is better than 8.9 dB from DC to 21 GHz and output return loss is better than 8 dB from 7.4 to 25 GHz. It is presumed that an inaccurate meander inductor model and an unknown bias tee models at high frequencies cause the discrepancy between the simulation and the measurement.

Fig. 2.12. Die photograph of proposed DA (chip size: 3.7 mm × 1.8 mm).

Fig. 2.13. Measured S-parameter of fabricated DA at $V_{D1}=V_{D2}=27$ V, $V_{G1} = V_{G2} = -2.4$ V (solid line: measurement and dashed line: simulation).
As shown in Fig. 2.14, the proposed DA delivers $P_{out}$ of 37.9–40.1 dBm, power added efficiency (PAE) of 7.4–16.0% and gain of 5.1–8.1 dB from 6 to 18 GHz at drain voltages of 36 V [17]. Specially, for the purpose of our model verification, the simulated output power of DA designed by our in-house model or foundry provided model are compared with the measured output power in Fig. 2.15. The output power
characteristics of DPA which is designed by in-house GaN HEMT large signal model show better agreement with the measured value than those by the model provided by the foundry.
2.4 Basic non-uniform distributed power amplifier design theory

It is desirable that all of the FET cells look an optimum load to maximize output power in the DA. A NDPA theory achieves this principle by tapering the characteristic impedances of each stage’s drain lines [11], [14].

Fig. 2.16 is the schematic of generalized NDPA and the N\textsuperscript{th} FET output circuit model.

From the N\textsuperscript{th} FET output circuit model, the optimum characteristic impedances of each drain line sections can be expressed as followed [11];

\[
R_{opt,n} = \frac{V}{I_{Mn}} = \frac{Z_{o,n} (I_{mn} + \sum_{i=1}^{n-1} I_{mi})}{I_{mn}} = \frac{Z_{o,n} (\sum_{i=1}^{n} \omega_{Mi})}{\omega_{Mn}}
\]

(13)

\[
Z_{o,n} = \frac{R_{opt,n}}{\sum_{i=1}^{n} \omega_{Mi}} \omega_{Mi} = \frac{R_{opt, (\Omega \cdot mm)}}{\sum_{i=1}^{n} \omega_{Mi}} \Omega 
\]

(14)

\((R_{opt,n} : N\textsuperscript{th} FET’s optimum load impedance, \ \omega_{Mi} : \text{FET M}_i \text{’s total gate periphery,})

\(R_{opt} (\Omega \cdot mm) : \text{normalized optimum load impedance})

Meanwhile, our NDPA’s main specifications are that the operating frequency band is from 6 to 18 GHz and the required output power is more than average 10 W. Our
commercial foundry provides the GaN HEMTs of which the normalized $R_{opt}$ is 70 $\Omega$/mm and the power density is 4 W/mm at the operation band. Usually, for convenience’ sake, the output load impedance of NDPAs is selected as 50 $\Omega$. Then, if the NDPA theory is applied to our NDPA design, the total FET periphery is $70/50=1.4$ mm and the maximum output power is $4\times1.4=5.6$ W. Therefore, to satisfy the output power specification, the output load impedance should be decreased and it means that our NDPA should increase the total FET periphery. If the number of gain sections is fixed, our NDPA should inevitably use the large sized FETs for enhanced output power. This requirement is the scope of our NDPA design.
2.5 Conclusions

In this work, before designing wideband GaN PAs, we have built up an Angelov-based GaN HEMT large-signal model that incorporates a thermal model and is based on various measurements. The in-house GaN HEMT model is effectively used to design a DPA up to frequencies close to the device’s $f_{\text{MAX}}$. For the purpose of our model verification, a 6–18 GHz, 8.1 W GaN DPA monolithic microwave integrated circuit (MMIC) is presented with compact size. To accomplish high-output power density with compact size, the last two sections of the DA consist of small-sized FETs. This approach improves the output return loss and allows the drain line lengths to be reduced thereby increasing the drain cut-off frequency and reducing circuit size, which results in increased gain and output power characteristics up to higher frequencies. Source via holes of GaN HEMTs are also shared to reduce chip size. The proposed DA is implemented as a two-stage DA using a commercial 0.25 μm GaN MMIC process. It shows 8.1 W average continuous wave output power and 6.8 dB average associated gain from 6 to 18 GHz under 36 V drain bias with 6.7 mm$^2$ chip area. The proposed DA obtains 1.21 W/mm$^2$ output power density and 1.02 dB/mm$^2$ gain density. The output power characteristics of DPA which is designed by in-house GaN HEMT large signal model show better agreement with the measured value than those by the model provided by the foundry.

Next, basic non-uniform distributed power amplifier design theory is investigated to enhance the output power of DA. From budgeting the specification, we have found the challenge that our NDPA should inevitably use the large sized FETs for enhanced output power.
2.6 References


Chapter 3

GaN Non Uniform Distributed Power Amplifier using Novel Power Combining Technique for Enhanced Power

3.1 Introduction

According to a NDPA theory, in the process of arranging the drain line impedance so that each transistor in the NDPA can have the optimum output load impedance \(R_{\text{opt}}\), the first drain line impedance usually becomes greater than 100 \(\Omega\). It causes a problem that the metal line width is too narrow to be fabricated by a commercial process. The conventional NDPA design uses a large-sized transistor at the first section to avoid this limitation.

The output power of a NDPA is limited by the fixed FET periphery. If NDPAs want to obtain higher power, load impedances should be lowered and the total FET periphery should be increased. Thus, NDPAs should consist of larger-sized FETs which have larger parasitic capacitances. In this condition, NDPA design needs to be modified. The conventional NDPA design assumes that the drain-source capacitance \(C_{\text{ds}}\) is absorbed in the transmission line. However, the larger the transistor size is
and the higher the frequency, the more its effect cannot be ignored. Also, the usage of a large-sized transistor at the first section degrades power gain and output power at high frequencies due to increased gate-to-source capacitances and drain-to-source capacitances. In the proposed NDPA, the drain-source capacitance is included in designing the optimum drain line impedance. Besides, the new design approach to avoid the usage of the large-sized transistor at the first section in the NDPA is proposed.

Although GaN PAs show output power densities higher than GaAs PAs, a single GaN PA cannot generate tens of watts of output power through the octave bandwidth. A power-combining technique is the inevitable approach. Conventional reactive matched PAs (RMPAs) require large chips due to the heavy output matching circuits, which makes RMPAs too bulky to be power-combined. When distributed amplifiers (DAs) are power-combined, long drain/gate lines and bulky power combiners increase the chip size. The large chip size not only increases the foundry cost but also causes problems in the process of thermally mounting the chip on modules or carriers, which degrades the performance of PAs. In this work, the compact power-combining structure of non-uniform distributed power amplifiers (NDPAs) is proposed.
3.2 Modified Non-uniform Distributed Power Amplifier Design

3.2.1 Drain line impedance design considering $C_{ds}$ effect

Fig. 3.1 represents the procedure of the drain line impedance design considering $C_{ds}$. First, the size of FET should be determined considering the operating frequency and the output power specification of NDPA and the FET’s $f_{\text{MAX}}$. In this work, the operating frequency band is from 6 to 18 GHz and the required output power is more than average 10 W. In our commercial GaN foundry, we select a 6×125 $\mu$m GaN FET. It has the cut-off frequency ($f_{t}$) of 23 GHz and the maximum oscillation frequency ($f_{\text{MAX}}$) of 65 GHz. In that case, the optimum number of NDPA’s gain sections is eight [1]. Second, the $R_{\text{opt}}$ of selected FET excluding $C_{ds}$ is investigated by a load-pull simulation. The $C_{ds}$ of a 6×125 $\mu$m GaN FET is extracted as 0.3 pF from S-parameter measurements. Our 6×125 $\mu$m GaN FET’s $R_{\text{opt}}$ represents 90 $\Omega$ under a drain voltage of 30 V. Third, the initial drain line impedance ($Z_{o,n}$) at each gain section is calculated according to the NDPA design equation introduced in [2]. Practically, the drain line can be modeled as a $\pi$-typed line which consists of a transmission line with the initial drain line impedance and two shunt $C_{ds}/2$. Thus, the drain line impedance is re-calculated including $C_{ds}$, as shown in Fig. 3.2. By ABCD matrix, the re-calculated drain line impedance ($Z'_{o,n}$) can be expressed as followed [3];

\[
Z'_{o,n} = \sqrt{\frac{Z'}{N'}} \\
Z' = jZ_{o,n}\sin\beta l \\
Y' = j\frac{2}{Z_{o,n}}\tan\frac{\beta l}{2} + j\omega \frac{C_{ds}}{2} \tag{3}
\]
Where $\beta$ is the phase constant, and $l$ is the line length, and $\omega$ is angular frequency. $Z'_{o,n}$ becomes frequency dependent because of the $C_{ds}$ term. For convenience’ sake, we specify $Z'_{o,n}$ at mid-frequency of operating frequency range. Lastly, the phase of drain lines is adjusted for the equal phase delay with gate lines.

---

**Fig. 3.1.** Procedure of the drain line impedance design considering $C_{ds}$.

**Fig. 3.2.** Drain line impedance’s conversion using $\pi$ typed-line model with $C_{ds}$.
Table 1 compares the drain line impedances before and after considering $C_{ds}$ effect. When $C_{ds}$ is included in designing the drain line impedances in the NDPA, the drain line impedances, especially in the front-end, increase. Fig. 3.3 shows the simulated output power of NDPA considering $C_{ds}$ effect. Compared to NDPA without $C_{ds}$ effect, NDPA with $C_{ds}$ effect represents the output power enhanced by average

<table>
<thead>
<tr>
<th>N</th>
<th>$Z_{o,n}$ ($\Omega$)</th>
<th>$Z'_{o,n}$ ($\Omega$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>70</td>
<td>280</td>
</tr>
<tr>
<td>2</td>
<td>35</td>
<td>88</td>
</tr>
<tr>
<td>3</td>
<td>23</td>
<td>45</td>
</tr>
<tr>
<td>4</td>
<td>18</td>
<td>31</td>
</tr>
<tr>
<td>5</td>
<td>14</td>
<td>21</td>
</tr>
<tr>
<td>6</td>
<td>12</td>
<td>17</td>
</tr>
<tr>
<td>7</td>
<td>10</td>
<td>13</td>
</tr>
<tr>
<td>8</td>
<td>9</td>
<td>12</td>
</tr>
</tbody>
</table>

Fig. 3.3. Simulated output power comparison between NDPA with $C_{ds}$ effect and NDPA without $C_{ds}$ effect.
0.4 dB from 6 to 18 GHz. The power enhancement at the high-frequency band over 15 GHz is notable. This enhancement results from a more realistic NDPA design.

3.2.2 High impedance line design without using a large sized FET

The conventional NDPA design uses a large-sized transistor at the first section to mitigate high impedance drain lines. However, this approach degrades power gain and output power at high frequencies due to increased parasitic capacitances. A quantitative analysis to this is as followed. Fig. 3.4 is the circuit schematic of general NDPAs. The power gain of DA (G) can be expressed as followed;

$$G = \frac{P_L}{P_{\text{avg}}} = \frac{|I_o|^2 R_L}{|V_s|^2/(4Z_s)}$$

$$|I_o|^2 = |I_1 + I_2 + I_3 \cdots + I_N|^2$$

Where $P_L$ is the power delivered to the load and $P_{\text{avg}}$ is the power available from the source and $I_o$ is the total output current and $R_L$ is the output load and $V_s$ is the source voltage wave and $Z_s$ is the source impedance. For the simplicity, the analysis assumes that the reversed wave is all absorbed to the termination load or canceled out. As seen from eq. (4), gain is proportion to $|I_o|^2$ that is related to the summation of each FET’s current. Thus, if two DAs have the same load impedance, the gain difference between two DAs results from the difference of total current between two DAs. Here, we can compare gain between an ideal NDPA and a practical NDPA using a large-sized transistor by analyzing each NDPA’s total current. Practically, two NDPA’s each current is equal to each other except for $I_1$ because only the transistor size at the first section is different. Gain analysis is simplified as the comparison of $I_1$. The equation about $I_1$ is as followed;
\[ I_1 = \frac{1}{2} V_{in} g_m e^{-N\theta_d} e^{-(\theta_g - \theta_d)/2} \]  \hspace{1cm} (5)

\[ \theta_g = \gamma_g l_g = (\alpha_g + \beta_g) l_g \]  \hspace{1cm} (6)

\[ \theta_d = \gamma_d l_d = (\alpha_d + \beta_d) l_d \]  \hspace{1cm} (7)

Where \( V_{in} \) is the incident input voltage and \( g_m \) is the transconductance and \( \gamma_{g/d} \) is the gate/drain line’s propagation constant and \( l_{g/d} \) is the gate/drain line length and \( \alpha_{g/d} \) is the gate/drain attenuation constant and \( \beta_{g/d} \) is the gate/drain phase constant.

Fig. 3.5 (a) and (b) are the equivalent circuit of a single cell of the gate/drain line. From the equivalent circuit of Fig. 3.5 (a) and (b), \( \alpha_{g/l} \) and \( \alpha_{d/l} \) can be expressed as followed [1];

Fig. 3.4. Circuit schematic of NDPA.

Fig. 3.5. Equivalent circuit of the single section of gate/drain line ((a) gate line (b) drain line).
\[ a_d l_d = \text{Re}\left\{ \sqrt{(j\omega L_d + R_d) \left( \frac{1}{R_{ds}} + jC_{ds}\omega \right)} \right\} \quad (8) \]

\[ a_g l_g = \frac{Z_{g\omega}^2 R_{c_{gs}}^2}{2} \quad (9) \]

Where \( L_d \) is the drain line inductance and \( R_d \) is the drain line resistance and \( R_{ds} \) is the drain-source resistance of FET and \( R_{ch} \) is the channel resistance of FET and \( C_{gs} \) is the gate-source capacitance of FET.

Now, our GaN FET model parameters are used to calculate the first output current of an ideal NDPA (\( I_1 \)) and that of a practical NDPA (\( I'_1 \)). In table 3.2, according to the each section of NDPAs, the FET size, model parameters and drain line impedances are compared between an ideal NDPA and a practical NDPA.

| TABLE 3.2
| COMPARISON OF DESIGN PARAMETERS BETWEEN AN IDEAL NDPA AND A PRACTICAL NDPA |

<table>
<thead>
<tr>
<th>FET Size (( \mu m ))</th>
<th>( Z_{\alpha,n} ) (( \Omega ))</th>
<th>( g_m ) (mS)</th>
<th>( C_{gs} ) (fF)</th>
<th>( C_{ds} ) (fF)</th>
<th>( R_{ds} ) (( \Omega ))</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ideal NDPA (( N=1 ))</td>
<td>750</td>
<td>160</td>
<td>200</td>
<td>1.3</td>
<td>0.3</td>
</tr>
<tr>
<td>2</td>
<td>750</td>
<td>75</td>
<td>200</td>
<td>1.3</td>
<td>0.3</td>
</tr>
<tr>
<td>3</td>
<td>750</td>
<td>45</td>
<td>200</td>
<td>1.3</td>
<td>0.3</td>
</tr>
<tr>
<td>4</td>
<td>750</td>
<td>33</td>
<td>200</td>
<td>1.3</td>
<td>0.3</td>
</tr>
<tr>
<td>5</td>
<td>750</td>
<td>24</td>
<td>200</td>
<td>1.3</td>
<td>0.3</td>
</tr>
<tr>
<td>6</td>
<td>750</td>
<td>19</td>
<td>200</td>
<td>1.3</td>
<td>0.3</td>
</tr>
<tr>
<td>7</td>
<td>750</td>
<td>16</td>
<td>200</td>
<td>1.3</td>
<td>0.3</td>
</tr>
<tr>
<td>8</td>
<td>750</td>
<td>13</td>
<td>200</td>
<td>1.3</td>
<td>0.3</td>
</tr>
<tr>
<td>Practical NDPA (( N=1 ))</td>
<td>1250</td>
<td>105</td>
<td>333</td>
<td>2.2</td>
<td>0.5</td>
</tr>
<tr>
<td>2</td>
<td>750</td>
<td>62</td>
<td>200</td>
<td>1.3</td>
<td>0.3</td>
</tr>
<tr>
<td>3</td>
<td>750</td>
<td>36</td>
<td>200</td>
<td>1.3</td>
<td>0.3</td>
</tr>
<tr>
<td>4</td>
<td>750</td>
<td>27</td>
<td>200</td>
<td>1.3</td>
<td>0.3</td>
</tr>
<tr>
<td>5</td>
<td>750</td>
<td>22</td>
<td>200</td>
<td>1.3</td>
<td>0.3</td>
</tr>
<tr>
<td>6</td>
<td>750</td>
<td>19</td>
<td>200</td>
<td>1.3</td>
<td>0.3</td>
</tr>
<tr>
<td>7</td>
<td>750</td>
<td>16</td>
<td>200</td>
<td>1.3</td>
<td>0.3</td>
</tr>
<tr>
<td>8</td>
<td>750</td>
<td>13</td>
<td>200</td>
<td>1.3</td>
<td>0.3</td>
</tr>
</tbody>
</table>
The ratio of $I_1$ and $I'_1$ calculated by Eq. (5)-(9) is shown in Fig. 3.6. As expected, at low frequency below 12 GHz, $I'_1$ is larger than $I_1$ due to larger $g_m$ but above 12 GHz, $I'_1$ starts to be smaller than $I_1$ due to larger $C_{gs}$ and $C_{ds}$. Fig. 3.7 (a) and (b) represent the simulated gain and output power of an ideal NDPA and a practical NDPA. In a practical NDPA, because of larger $C_{ds}$ and $C_{gs}$ originated from a larger-sized FET, both gain and output power are degraded at high frequencies.

Fig. 3.6. Ratio of the first output currents of an ideal NDPA ($I_1$) and that of a practical NDPA ($I'_1$).

Fig. 3.7. Simulated (a) Gain and (b) output power of an ideal NDPA and a practical NDPA.
To mitigate this degradation, this work proposes the method to relax the impedance of the first section’s drain line without using a large-sized FET at the first section. The design method is halving the characteristic impedance by doubling the phase of the drain line. As shown in Fig. 3.8, the first drain line can be approximately modeled as a series inductor (L) and two shunt $C_{ds}/2$. A series inductor is equivalent to two parallel-connected forms of two cascaded inductors. This can be transformed as two cascaded forms of two parallel-connected inductors. Then a drain line whose characteristic impedance is $Z_o$ and line length is $l$ is qualitatively equivalent to a drain line with $Z_o/2$ and $2l$. In Fig. 2, if $Z_{o,n}/2$ and $2l$ are substituted for $Z_{o,n}$ and $l$, the modified drain line’s $Z$-parameter ($Z''$) and $Y$-parameter ($Y''$) can be expressed by the following equations;

$$Z'' = j(Z_o/2)\sin(2\beta l)$$

$$Y'' = j \frac{2}{(Z_o/2)} \tan \left( \frac{2\beta l}{2} \right) + j\omega \left( \frac{C_{ds}}{2} \right)$$

If the line length is small and $C_{ds}$ or $Z_o$ is large, eq. (10) and (11) are approximated as followed.

$$Z'' = j(Z_o/2)\sin(2\beta l) \approx jZ_o\beta l \approx jZ_o\sin\beta l \approx Z'$$

$$Y'' = j \frac{2}{(Z_o/2)} \tan \left( \frac{2\beta l}{2} \right) + j\omega \left( \frac{C_{ds}}{2} \right) \approx Y'$$

Fig. 3.8. Ratio of the first output currents of ideal NDPA ($i_1$) and that of practical NDPA ($i_1'$).
Usually, the impedance of the first section’s drain line is higher than 100 Ω and the line length is smaller than $\lambda/12$ at the center frequency. Our NDPA consists of FETs whose $C_{ds}$ is larger than 0.2 pF. Therefore, the proposed method is also quantitatively valid. When the proposed method is applied to an ideal lossless transmission line whose characteristic impedance is 200 Ω and line length is 10° at 18 GHz, the characteristic impedance is reduced to 100 Ω and the line length increases to 20° at 18 GHz. Fig. 3.9 (a) and (b) show the comparison of the simulated S-parameters of two lines. As expected from the above analysis, two lines show almost identical characteristics.

Fig. 3.9. Simulated s-parameter of two lines (circled line: 200Ω, 10° line, dashed line: 100Ω, 20° line) ((a) the magnitude and phase of $S_{11}$, (b) the magnitude of phase of $S_{21}$).
The proposed high impedance line design is applied to NDPA and the output power is simulated in comparison with an ideal NDPA and a practical NDPA in Fig. 3. In the case of the proposed NDPA, the original 1st drain line impedance with $Z_o = 160\ \Omega$, $\phi = 20^\circ$ at 18 GHz is converted to that with $Z_o = 80\ \Omega$, $\phi = 40^\circ$ at 18 GHz. As shown in Fig. 3.10, the proposed NDPA shows the output power characteristics closer to the ideal NDPA’s than the practical NDPA.

At the above analysis, we assume that the transmission line is lossless. If the line is lossy, because the line length increases by twice in the proposed NDPA, the line loss may have a negative influence on overall gain of a NDPA. In the proposed NDPA, the line loss effect needs to be analyzed. In similar way to the above analysis, the ratio of $I_3$ and $I_3'$ calculated by Eq. (5)-(9) is investigated according to line loss (R). Here, $I_3$ is the first output current of the ideal NDPA and $I_3'$ is that of the
proposed NDPA. From Fig. 3.11, as line loss increases, the ratio of $I_1$ and $I'_1$ becomes rather close to 1. The reason is found from Eq. (8). As known from Eq. (8), line’s attenuation loss depends more on the inductance term than the resistance term. Thus, as the resistance term increases in Eq. (8), the portion of inductance in the attenuation loss decreases relatively. This means the lossy line helps to alleviate loss induced from the increased line length in the proposed method. Fig. 3.12 shows the simulated gain degradation when the ideal NDPA is changed by the proposed NDPA in each case of $R = 0 \, \Omega$ and $R = 5 \, \Omega$. In case of $R = 5 \, \Omega$, the gain degradation does not get worse. The proposed design method is not vulnerable to the line loss.

Fig. 3.11. Ratio of the first output currents of ideal NDPA ($I_1$) and that of practical NDPA ($I'_1$).

Fig. 3.12. Gain degradation between ideal NDPA and the proposed NDPA according to line loss.
Fig. 3.13 is the simulated output power between ideal NDPA and the proposed NDPA according to frequencies. Compared to the previous NDPA, the proposed NDPA represents the output characteristics similar to ideal NDPAs without degradation at high frequencies.

Fig. 3.13. Simulated output power between ideal NDPA and the proposed NDPA according to frequencies (a) Pin=33 dBm (b) Pin=36 dBm.
3.3 Novel Power Combining Technique by Sharing Drain Lines

When distributed amplifiers (DAs) are power-combined as shown in Fig. 3.14 (a), long drain/gate lines and bulky power combiners increase the chip size [4], [5]. The large chip size not only raises the foundry cost but also degrades the performance of PAs in the process of attaching the chip to modules by thermal pastes. In this work, the compact power-combining structure of NDPAs is proposed as shown in Fig. 3.14 (b). To minimize the increased chip size due to power combining, the drain lines and gate lines are shared among the combined NDPAs. Sharing drain (or gate) lines also reduces the line length by half, keeping the same characteristic impedances as the drain (or gate) lines before they were shared. Due to the proposed structure, power-combined NDPAs can be expanded to four ways in a compact size. The number of impedance transformers and the number of output power combiners decrease by two, respectively.

![Block diagram of the four-way power-combined NDPA](image)

Fig. 3.14. Block diagram of the four-way power-combined NDPA (a) conventional structure (b) proposed structure.
According to NDPA theory, the characteristic impedance of the nth drain line ($Z_{o,n}$) can be calculated based on the optimum load impedance of nth field effect transistor (FET) [6]. As shown in Fig. 3.15 (a), a drain line in the NDPA can be modeled as a π-section line that consists of a series transmission line and two halves of the shunt drain-source capacitance ($C_{ds}$). When two NDPAs share the same drain lines, $Z_{o,n}$ decreases by half because the input impedance looking from the $n^{th}$ FET of both NDPAs is parallel-connected by sharing the same lines. The shunt capacitances double. The π-section line’s ABCD matrix can be expressed as follows [3]:

$$
\begin{bmatrix}
1 + \frac{ZY}{2} & Z \\
Y \left(1 + \frac{ZY}{2}\right) & 1 + \frac{ZY}{2}
\end{bmatrix}
\begin{bmatrix}
Z = j \frac{Z_{o,n}}{2} \sin \beta l, & Y = j \frac{2}{\frac{Z_{o,n}}{2}} \tan \left(\frac{\beta l}{2}\right) + j \omega C_{ds}
\end{bmatrix}
$$

(14)

Where $\beta$ is the phase constant, and $l$ is the line length.

If $\beta l$ is small and $Z_{o,n}$ is larger than $\tan \beta l$, then the $Z$ and $Y$ parameters of equation (14) are approximated as follows:
\[ Z = \left( \frac{z_{o,n}}{2} \sin \beta l \right) + j Z_{o,n} \sin \left( \frac{\beta l}{2} \right) \]  \hspace{1cm} (15)

\[ Y = \left( \frac{2}{Z_{o,n}} \right) \tan \left( \frac{\beta l}{2} \right) + j \omega C_{ds} \approx \left( \frac{2}{Z_{o,n}} \right) \tan \left( \frac{\beta l}{4} \right) + j \omega C_{ds} \]  \hspace{1cm} (16)

Usually in the DA, the drain line’s electrical length is not larger than \( \lambda/8 \) at the center frequency. Thus, equations (15) and (16) mean if the characteristic impedances of the drain lines double, then the line lengths can be reduced by half. If we apply this principle to the multi-way combined NDPAs that share the same drain lines, then the drain line lengths could be halved, keeping the same characteristic impedances as a single NDPA. Because this approach increases the compactness in the power combining, it contributes to increasing the power density of NDPAs.

In the proposed power combining structure, the phase mismatch in the shared drain line is analyzed and simulated. At first, the same NDPA is simulated with shared drain lines or without shared drain lines and power gain is compared to each other. Then, \( \pm 20 \% \) phase variation in the drain lines of NDPAs is added to the simulation. Fig. 3.16 shows the simulation results on the in-phase condition with gate lines and Fig. 3.17 (a) and (b) shows the simulation results on the mismatched phase condition with gate lines due to \( \pm 20 \% \) phase variation in the drain lines of NDPAs. As shown in Fig. 3.16 and Fig. 3.17 (a), (b), the NDPA with shared drain lines shows the gain degradation similar to the conventional power combined NDPA without shared drain lines when the phase mismatch of drain lines occurs. Serious gain degradation by phase mismatch is not appeared when drain lines are shared. The proposed power combining structure is not vulnerable to the phase mismatch by process variation or design error.
Fig. 3.16. Simulated gain comparison of NDPAs on the in-phase condition with gate lines.

(a)

(b)

Fig. 3.17. Simulated gain comparison of NDPAs on the phase-mismatched condition with gate lines (a) +20 % phase mismatch (b) -20 % phase mismatch.
The influence that the proposed NDPA combining structure has on the output return loss is analyzed. The power combined NDPA with shared drain lines is compared to the power combined NDPA without shared drain lines. The simplified drain line equivalent circuits of each drain lines are shown in Fig. 3.18 (a) and (b), respectively.

Fig. 3.18. Simplified drain line equivalent circuits of each drain lines ((a) power combined NDPA without shared drain lines (b) power combined NDPA with shared drain lines).

Fig. 3.19. More simplified equivalent circuits of (a) NDPA without shared drain lines (b) NDPA with shared drain lines.
For more simplified approach, it assumes that $C_{ds}$ is absorbed in drain lines. In that case, the drain-line impedances of each drain lines return to the original optimum drain-line impedances. Fig. 3.19 (a) and (b) represent more simplified drain line equivalent circuits of each NDPAs.

The equations about output impedances of a NDPA without shared drain lines can be expressed as followed.

\[
Z_{\text{out},1} = Z_{0,1} \frac{R_{ds} + jZ_{0,1} \tan \beta l}{Z_{0,1} + jR_{ds} \tan \beta l} \quad (17)
\]

\[
Z_{\text{out},n} = Z_{0,n} \frac{(Z_{\text{out},n-1}/R_{ds}) + jZ_{0,n} \tan \beta l}{Z_{0,n} + j(Z_{\text{out},n-1}/R_{ds}) \tan \beta l} \quad (18)
\]

\[
Z_{0,n} = \frac{R_{\text{opt}}}{n} \quad (19)
\]

Likewise, the equations about output impedances of a NDPA with shared drain lines can be expressed as followed.

\[
Z_{\text{out},1} = Z_{0,1} \frac{R_{ds} + jZ_{0,1} \tan \beta l}{\frac{Z_{0,1}}{2} + j\frac{R_{ds}}{2} \tan \beta l} \quad (20)
\]

\[
Z_{\text{out},n} = Z_{0,n} \frac{(Z_{\text{out},n-1}/R_{ds}) + jZ_{0,n} \tan \beta l}{\frac{Z_{0,n}}{2} + j\frac{(Z_{\text{out},n-1}/R_{ds})}{2} \tan \beta l} \quad (21)
\]

The output return loss calculated by above equations is shown in Fig. 3.20. $N$ is fixed to 8 and 6×125 um GaN HEMT models having $R_{\text{opt}} = 90 \, \Omega$, $R_{ds} = 250 \, \Omega$ and $C_{ds} = 300 \, \text{fF}$, are used to the calculation. The proposed NDPA combining shows definitely better output return loss than the conventional NDPA combining. To find out the reason, the output return loss is calculated according to $R_{ds}$ in Fig. 3.21. As known from Fig. 3.21, as $R_{ds}$ is reduced to 100 $\Omega$, the output return loss is improved more and more. The shared drain line in the proposed NDPA combining structure allows the drain-to-source resistance ($R_{ds}$) of each transistor to be connected in...
parallel, thus contributing to improving the output return loss when using large size devices. Unfortunately, when $C_{ds}$ is included in the equivalent circuit of the drain lines, the improvement of output return loss decreases as shown in Fig. 3.22. Although, the proposed NDPA combining structure still shows the better output return loss performance than the conventional NDPA power combining.

![Fig. 3.20. Calculated output return loss of the simplified drain lines.](image)

![Fig. 3.21. Output return loss calculated according to $R_{ds}$.](image)
Fig. 3.22. Calculated output return loss of the simplified drain lines including $C_{ds}$. 
3.4 Practical Design Example and Measurement Results

For design verification, two modified NDPA MMICs have been fabricated by a commercial 0.25 $\mu$m GaN HEMT process. As mentioned above, the modified NDPA design which considers $C_d$ effect and uses the lower impedance line by doubling the phase of the first drain line instead of using a large-sized transistor at the first section is applied to both NDPAs. Also, the proposed compact power combining NDPA structure are applied to two NDPA MMICs. The first NDPA is designed as a two-way power-combined NDPA and the second NDPA is designed a four-way power-combined NDPA with a focus on high power [7].

Both NDPA MMICs are measured with mounted on 5-mm-thick Au-plated Cu zig with eutectic bonding to facilitate thermal dissipation. Both small-signal and large-signal measurements are performed by on-wafer probing using ground–signal–ground (GSG) probes and a probe station. To measure the output power of two NDPAs, pulsed signal as well.

3.4.1 Two-way power combined non-uniform distributed power amplifier

Fig. 3.23 is the circuit schematic of the two-way power-combined NDPA. It consists of a drive stage DA and a main stage NDPA. In order to drive input power enough to saturate output power of a main stage NDPA, a drive stage DA is also designed as a NDPA type. Each NDPA consists of eight gain cells considering linear gain, bandwidth and output power. Unequal-sized FETs are applied in the NDPA to improve output return loss without drain line termination impedances [8]. The NDPA mostly uses $6 \times 125$ $\mu$m GaN HEMTs, but the last three sections have a $6 \times 75$ $\mu$m
and two $2 \times 125 \, \mu m$ GaN HEMTs. The unequal-sized FETs at last three sections also raise the output impedance in the NDPA. This approach relieves the burden of high transform ratio for impedance matching. Two four-to-one impedance transformers are used at interstage and output stage in the NDPA to transform the output load impedance to $50 \, \Omega$.

A Ruthroff impedance transformer which has low loss and broadband characteristics is used as a four-to-one impedance transformer [9]. It can be implemented as a compact meander type replacing a band-limited quarter-wave length transmission line transformer. Its ground port is also used to supply drain biases without an external bias tee.

Fig. 3.23. Circuit schematic of the two-way power-combined GaN NDPA.
Fig. 3.24. Photograph of the two-way power-combined GaN NDPA (size = 4.8 mm x 2.3 mm).

Fig. 3.25. S-parameters of the proposed GaN NDPA (V\textsubscript{D1}=21 V, V\textsubscript{D2}=24 V, V\textsubscript{G1}=V\textsubscript{G2}=-2.4 V, solid lines: simulation, dotted lines: measurement).

Fig. 3.24 is a die photograph of the two-way power-combined NDPA. The fabricated NDPA has a die size of 4.8 mm × 2.3 mm. Fig. 3.25 shows the measured and simulated S-parameters of the NDPA. The measured small signal gain (S21) is somewhat lower than the simulated one due to overestimated gain of GaN HEMT.
models and underestimated loss of the impedance transformer circuit. Nevertheless, the fabricated NDPA shows small signal gains higher than 16.8 dB from 6 to 18 GHz with a peak gain of 21.8 dB at 10.8 GHz. Input return loss is better than 10 dB from 6 to 18 GHz except for 14.8 to 16.4 GHz in which it is better than 7.5 dB and output return loss is better than 6.9 dB from 6 to 18 GHz. Fig. 3.26 shows the measured output power (Pout), associated gain and power added efficiency (PAE) of the NDPA from 6 to 18 GHz. Bias condition is optimized to obtain the best PAE. The proposed NDPA delivers continuous wave (CW) Pout of 41.6 ~ 44.2 dBm (average 43.2 dBm), PAE of 13.2 ~ 23.7 % and gain of 10.8 ~ 12.6 dB from 6 to 18 GHz at drain voltages of 30 V. When a pulsed input power and a pulsed bias are simultaneously supplied at the NDPA with 20 ms pulse width and 400 ms period, Pout increases to the extent of 42.5 ~ 44.8 dBm (average 43.8 dBm) at a drain voltage of 33 V as shown in Fig. 3.26. As result of the modified NDPA design, without steep degradation at 18 GHz, output power characteristics of the fabricated NDPA is flatter than other previous reported NDPAs [2], [5].
3.4.2 Four-way power combined non-uniform distributed power amplifier

Fig. 3.27 is the circuit schematic of the proposed NDPA. It consists of a drive stage NDPA and a main stage NDPA. When the NDPA is practically designed, using a commercial GaN monolithic microwave integrated circuits (MMIC) foundry process, the 1100-μm-long drain line is shortened to 550 μm. The gate line length can also be reduced in the same manner. Therefore, the proposed NDPA combining structure can be more compact than before. To drive the input power enough to saturate the output power of the main stage NDPA, a drive stage amplifier is also designed as a type of NDPA. Each NDPA consists of eight gain cells to optimize the linear gain, bandwidth and output power. As mentioned in our previous work, unequal-sized FETs are
applied in the NDPA to improve the output return loss and the power gain at a high frequency without drain line termination impedances [8]. The proposed NDPA mostly uses $6 \times 75 \, \mu m$ GaN HEMTs, but the last section has $2 \times 125 \, \mu m$ GaN HEMTs. A Ruthroff impedance transformer, which has low loss and broadband characteristics, is used as a four-to-one impedance transformer at the output stage in the NDPA to transform the output load impedance to $50 \, \Omega$ [9], [10]. The transformer is implemented as a compact meander type, replacing a band-limited quarter-wave length transmission line transformer. The ground port is used to supply drain biases without external bias tees.

![Fig. 3.27 Schematic of the proposed 4-way power combined NDPA.](image)

The proposed circuit was fabricated using a commercial $0.25 \, \mu m$ GaN HEMT MMIC process with a cut-off frequency ($f_T$) of 23 GHz and a maximum oscillation frequency ($f_{MAX}$) of 65 GHz. Fig. 3.28 is a die photograph of the proposed NDPA. The fabricated NDPA MMIC has a die size of $7.8 \, mm \times 2.7 \, mm$. Fig. 3.29 shows
the measured and simulated S-parameters of the proposed NDPA and shows small signal gains higher than 13.5 dB from 6 to 18 GHz with a peak gain of 18 dB at 11.2 GHz. The measured small signal gain (S21) is somewhat lower than the simulated gain due to the overestimated gain of the GaN HEMT models and the underestimated loss of the impedance transformer circuit. The input return loss is better than 10 dB from 6 to 18 GHz, and the output return loss is better than 3.5 dB from 6 to 18 GHz. Fig. 3.30 shows the measured output power (Pout), associated gain and power added efficiency (PAE) of the NDA from 6 to 18 GHz. The bias condition is optimized to obtain the best PAE. The proposed NDA delivers continuous wave (CW) Pout of 41.0–44.7 dBm (average 43.1 dBm), PAE of 8.8–18.4 % and gain of 8.0–12.1 dB from 6 to 18 GHz at drain voltages of 33 V. When pulsed input power and pulsed bias are simultaneously supplied to the NDA with 20 ms pulse width and 400 ms period, Pout increases to 41.4–45.9 dBm (average 44.1 dBm). The proposed NDA produces pulsed Pout of about 40 W at 13 GHz.

Fig. 3.28 Die photograph of the proposed 4-way power combined NDPA (chip size: 7.8 mm x 2.7 mm).
Fig. 3.29 S-parameters of the proposed 4-way power combined GaN NDPA ($V_{D1}=V_{D2}=30$ V, $V_{G1}=V_{G2}=V_{G3}=-2.6$ V, solid lines: simulation, dotted lines: measurement).

Fig. 3.30 Measured output power, PAE and gain of the fabricated NDPA at $V_{D1}=24$ V, $V_{D2}=33$ V, $V_{G1}=V_{G2}=V_{G3}=-2.0$ V (Pin = 31–33 dBm).
Table 3.3 compares the performance of the NDPA of this work with the state-of-the-art GaN NDPAs and RMPAs using GaN MMIC process. To the best of our knowledge, the two-way NDPA of this work represents the highest RF power among the reported GaN PAs with octave bandwidth higher than Ku-band. The four-way NDPA of this work represents the highest power density among the reported GaN PAs with octave bandwidth higher than Ku-band. This improvement results from more efficiently-modified NDPA design which

<table>
<thead>
<tr>
<th>Ref.</th>
<th>Freq. (GHz)</th>
<th>Topology</th>
<th>Pout (W)</th>
<th>PAE (%)</th>
<th>Linear Gain (dB)</th>
<th>Area (mm²)</th>
<th>Power density (W/mm²)</th>
<th>Number of combining</th>
</tr>
</thead>
<tbody>
<tr>
<td>[11]</td>
<td>6-18</td>
<td>RMPA⁺</td>
<td>20.0</td>
<td>15.0</td>
<td>15-18</td>
<td>19.2</td>
<td>1.04 (pulsed)</td>
<td>1-way</td>
</tr>
<tr>
<td>[2]</td>
<td>2-17</td>
<td>NDPA</td>
<td>9.1</td>
<td>26.0</td>
<td>10-14</td>
<td>12.6</td>
<td>0.72 (CW)</td>
<td>1-way</td>
</tr>
<tr>
<td>[4]</td>
<td>6-18</td>
<td>NDPA</td>
<td>12.9</td>
<td>18.0</td>
<td>8-10</td>
<td>18.7</td>
<td>0.69 (pulsed)</td>
<td>2-way</td>
</tr>
<tr>
<td>[12]</td>
<td>2-15</td>
<td>NDPA</td>
<td>5.5</td>
<td>25.0</td>
<td>10-13</td>
<td>10.1</td>
<td>0.55 (CW)</td>
<td>1-way</td>
</tr>
<tr>
<td>[13]</td>
<td>6-18</td>
<td>RMPA⁺</td>
<td>7.7</td>
<td>17.6</td>
<td>18-25</td>
<td>19.8</td>
<td>0.39 (CW)</td>
<td>1-way</td>
</tr>
<tr>
<td>[5]</td>
<td>2-20</td>
<td>NDPA</td>
<td>16</td>
<td>25.9</td>
<td>10-15</td>
<td>38.3</td>
<td>0.42 (CW)</td>
<td>2-way</td>
</tr>
<tr>
<td>[14]</td>
<td>6-18</td>
<td>RMPA⁺</td>
<td>10.6</td>
<td>16.9</td>
<td>20-25</td>
<td>19.3</td>
<td>0.55 (CW)</td>
<td>1-way</td>
</tr>
<tr>
<td>[10]</td>
<td>16-40</td>
<td>NDPA</td>
<td>13</td>
<td>16</td>
<td>24</td>
<td>15.6</td>
<td>0.83 (pulsed)</td>
<td>2-way</td>
</tr>
<tr>
<td>This work 1</td>
<td>6-18</td>
<td>2-way NDPA</td>
<td>21.0</td>
<td>19.2</td>
<td>17-21</td>
<td>11.0</td>
<td>1.9 (CW)</td>
<td>2-way</td>
</tr>
<tr>
<td>This work 2</td>
<td>6-18</td>
<td>4-way NDPA</td>
<td>20.8</td>
<td>13.6</td>
<td>13-17</td>
<td>21.0</td>
<td>0.99 (CW)</td>
<td>4-way</td>
</tr>
</tbody>
</table>

Table 3.3 compares the performance of the NDPA of this work with the state-of-the-art GaN NDPAs and RMPAs using GaN MMIC process. To the best of our knowledge, the two-way NDPA of this work represents the highest RF power among the reported GaN PAs with octave bandwidth higher than Ku-band. The four-way NDPA of this work represents the highest power density among the reported GaN PAs with octave bandwidth higher than Ku-band. This improvement results from more efficiently-modified NDPA design which
considers the $C_{ds}$ effect and remove the usage of the large sized FET at the first gain section. Besides, a compact and efficient NDPA power combined structure also contributes to improving output power with high power density because sharing a drain line reduce the drain line length by half with no necessity of bulky and lossy power combiners.
3.5 Conclusions

In this work, the modified NDPA is designed and implemented to obtain the enhanced wideband power and power added efficiency. The effect of output capacitance is considered in the NDPA design. After the $C_{ds}$ is added to the existing drain line impedance to make an equivalent model with the $\pi$-type line, the line impedance is readjusted to have the $R_{opt}$ at the center frequency. By applying this design method to the NDPA, the average output power could be improved by 0.4 dB at 6 ~ 18 GHz than the conventional method. Besides, instead of using a large-sized transistor at the first section in the NDPA, a method of halving the characteristic impedance ($Z_o$) by doubling the phase of the drain line is proposed. As a result of analyzing loss due to the increase of the line length, the high-frequency loss is reduced compared with the conventional method, and power gain and the output power characteristics close to the ideal NDPA’s can be obtained. As practical design examples, the compact two-way and four-way power-combined NDPA are demonstrated using a commercial 0.25 $\mu$m GaN HEMT MMIC process. The proposed NDPA successfully achieves RF power of tens of watts through the octave bandwidth, which is required for electronic warfare systems. Moreover, by applying the common drain line-shared NDPA, high power density with reduced chip size is accomplished. This combining technique is expected to contribute to more compact and wideband PA MMICs with higher power, replacing TWTAs.
3.6 References


Chapter 4

GaN Non Uniform Distributed Power Amplifier using Programmable Gate Line Termination Resistance Switching Technique for Enhanced Power Added Efficiency

4.1 Introduction

The power added efficiency is another important specification of wideband PAs. Especially, because GaN PAs operate under high voltages more than 25 V, they may require bulky DC power supplies according to current consumption. It determines the volume and portability of overall electronic warfare system. Unfortunately, both RMPAs and DAs have shown poor PAE as they cannot adopt conventional efficiency enhancement techniques such as harmonic tuning to wideband operation. In [1], the NDPA has obtained PAE over 20 % but it has been fabricated by the internal advanced GaN MMIC process with the excellent GaN HEMT’s maximum oscillation frequency ($f_{MAX}$). Although [2] improves PAE by proposing the stage-scaled DA design topology, the enhanced PAE is only 2 % at specific frequencies and it could not be applied to NDPA. In this work, the programmable gate line termination resistance switching technique (PGT) is proposed as the PAE
enhancement technique in the NDPA. On the other hand, as the operating frequency increases in the NDPA, the $R_{\text{opt}}$ for determining the drain line impedance is observed to increase. As a result, the maximum output power cannot be obtained according to the frequency, and mismatch occurs, which degrades the overall power efficiency. To make up for this mismatch, the four drain line impedances of the front end are designed according to the $R_{\text{opt}}$ of 6 GHz, and the four drain line impedances of the rear end are designed according to the $R_{\text{opt}}$ of 18 GHz. This rearrangement of the drain line impedances is because the transistors and drain lines on the rear end of the NDPA are more susceptible to high frequencies. In this work, the frequency-dependence for optimum load impedance is considered in designing the optimum drain line impedances. As a result, the proposed modified-NDPA provides output power and PAE better than the conventional NDPA.
4.2 Operation Principle of the Proposed Power Added Efficiency Enhancement Technique

To improve PAE, a NDPA should increase output power keeping the same DC power consumption at the same input power. From eq. (4) of chapter 3.2.2, $|I_o|$ term needs to be increase without extra DC power consumption. When the gate line termination resistance ($R_{gt}$) is variable, this work investigates what effect it has on $|I_o|$ term in the NDPA. In this case, the reversed traveling wave appears more strongly due to mismatched $R_{gt}$. The effect by mismatches at the termination loads in the DA is well-explained in [3]. Fig. 4.1 (a) and (b) is the simplified equivalent circuit of gate lines and drain lines at the DA with the mismatched termination load. Then eq. (4) of chapter 3.2.2 can be rewritten as follows.

![Fig. 4.1 Simplified equivalent circuit of (a) gate line and (b) drain line at the DA with the mismatched termination load.](image)
\[ G = \frac{p_L}{p_{\text{ave}}} = \frac{|I_o|^2 Z_L}{|W_d|^2/(4Z_s)} = 4Z_L \cdot Z_s \cdot |V_k|^2 \cdot |I_{o1} + I_{o2} + I_{o3} + I_{o4}|^2 \]  

(1)

\[ I_o = -\sum_{k=1}^{N} g_m V_{i,k} \frac{Z_{dl,k}}{Z_{dl,k} + Z_{dr,k}} e^{-\left(N-k+\frac{1}{2}\right)\gamma_d d} \]

\[ = -\sum_{k=1}^{N} g_m V_{i,k} \frac{1 + \Gamma_{dt} e^{-2(k-\frac{1}{2})\gamma_d d}}{2} e^{-\left(N-k+\frac{1}{2}\right)\gamma_d d} \]

\[ = V_x \cdot V_s \cdot \left( I_{o1} + I_{o2} + I_{o3} + I_{o4} \right) \]  

(2)

\[ V_x = \frac{g_m}{2} \cdot \frac{1}{1 + j\omega R_{in} C_{in}} \cdot \frac{Z_g}{Z_s + Z_g} \cdot \frac{1}{1 - \Gamma_{gt} e^{-2N\gamma g l g}} \]  

(3)

\[ I_{o1} = e^{-\frac{1}{2}(\gamma g l g + \gamma d d)} \cdot \frac{e^{-N\gamma g l g} - e^{-N\gamma d d}}{e^{\gamma g l g} - e^{-\gamma d d}} \]  

(4)

\[ I_{o2} = \Gamma_{gt} e^{\frac{1}{2}(\gamma g l g + \gamma d d)} e^{-2N\gamma g l g} \cdot \frac{e^{N\gamma g l g} - e^{-N\gamma d d}}{e^{\gamma g l g} - e^{-\gamma d d}} \]  

(5)

\[ I_{o3} = \Gamma_{dt} e^{-\frac{1}{2}(\gamma g l g - \gamma d d)} e^{-2N\gamma d d} \cdot \frac{e^{-N\gamma g l g} - e^{-N\gamma d d}}{e^{-\gamma g l g} - e^{-\gamma d d}} \]  

(6)

\[ I_{o4} = \Gamma_{dt} \Gamma_{gt} e^{-\frac{1}{2}(\gamma g l g + \gamma d d)} \cdot \frac{e^{N\gamma g l g} - e^{-N\gamma d d}}{e^{-\gamma g l g} - e^{-\gamma d d}} \]  

(7)

Where \( \Gamma_{gt} \) is the gate termination reflection coefficient and \( \Gamma_{dt} \) is the drain termination reflection coefficient and \( R_{in} \) (or \( C_{in} \)) is the gate input resistance (or capacitance). As known form eq. (1) - (7), power gain of the DA is proportional to \(|I_o|^2\). \( I_{o1} \) is an output current term generated from forward traveling wave component. \( I_{o2} \) and \( I_{o3} \) are output current terms generated from gate line and drain line reflected wave components. \( I_{o4} \) is an output current generated from multiplied term of reflected wave components. If both gate and drain termination loads are well-matched, only \( I_{o1} \) remains. However, in case of NDPAs, a drain line termination load is usually eliminated to reduce power loss. Because \( \Gamma_{dt} \) becomes 1, \( I_{o3} \) and \( I_{o4} \) are no longer negligible. In this condition, NDPA’s total gain is strongly influenced by \( \Gamma_{gt} \) and fluctuates according to frequencies owing to \( \Gamma_{gt} \).
variation, or $R_{gt}$ variation. As shown in Fig. 4.2, from the simulation, it is found that
the effective range of $R_{gt}$ in which gain fluctuates is largely from 10 to 100 $\Omega$.

![Fig. 4.2 Simulated S21 of NDPA according to $R_{gt}$ variation.](image)

For example, in case of lossless lines ($\alpha_g, \alpha_d = 0$) and equal electrical lengths of
gate/drain lines ($\beta_g \ell_g = \beta_d \ell_d = \theta$) satisfying $\Gamma_{dt} = 1$, -1 < $R_{gt}$ < 1, each output
current components of a NDPA can be simplified as following equations;

\[ I_{o1} = Ne^{-jN\theta} \]  

\[ I_{o2} = \frac{\Gamma_{gt}e^{-j2N\theta}\sin(N\theta)}{\sin(\theta)} \]  

\[ I_{o3} = \frac{e^{-j2N\theta}\sin(N\theta)}{\sin(\theta)} \]  

\[ I_{o4} = N\Gamma_{gt}e^{-j3N\theta} \]  

$(0 < \theta < 2)$
Using GaN FET models provided by our commercial foundry, $|I_o|$ is calculated from eq. (16a) – (19a). Fig. 4.3 is the calculated $|I_o|$ on the condition of $R_{gt} = 10 \ \Omega$ and 100 $\Omega$. As shown in Fig. 4.3, $|I_o|$ is fluctuated according to $\theta$ by mismatched $R_{gt}$. The fluctuation of $|I_o|$ at low $R_{gt}$ is the opposite direction to that at high $R_{gt}$.

**Fig. 4.3 Calculated $|I_o|$ on the condition of $R_{gt} = 10 \ \Omega$ and 100 $\Omega$.**

**Fig. 4.4 Simulated S21 of NDPA on the condition of $R_{gt} = 10 \ \Omega$ and 100 $\Omega$.**
Fig. 4.4 is the simulated S21 of NDPA on the condition of $R_{gt} = 10 \, \Omega$ and $100 \, \Omega$. Due to the $R_{gt}$ variation, $|I_o|$ fluctuates according to $\theta$ and because gain is proportional to $|I_o|^2$, simulated S21 of NDPA also fluctuates similarly to $|I_o|$ as shown in Fig. 4.4. Likewise, output power is proportional to $|I_o|^2$ and output power and PAE fluctuates according to frequencies depending on $R_{gt}$ in Fig. 4.5 (a) and (b).

![Graph (a)](image_url)

![Graph (b)](image_url)

Fig. 4.5 Simulated (a) Pout and (b) PAE of NDPA according to $R_{gt}$ from 6 to 18 GHz.
As power gain and output power of DA is proportional to $|I_o|^2$, if $R_{gt}$ can be so programmable that a NDPA can have the peak gain according to frequencies, a NDPA can increase output power keeping the same DC power consumption at the same input power. This increases PAE of a NDPA. Assuming that $R_{gt}$ can be programmable as shown in Fig. 4.6 (b), the simulated PAE result of a NDPA using ideal design components is shown in Fig. 4.6 (a). As shown in Fig. 4.6 (a), PAE is ideally increased from 22.5 to 27 % in comparison with that of the conventional NDPA with fixed $R_{gt}$. We call the proposed PAE enhancement method “programmable gate line termination switching technique (PGT)”.

![Diagram](image1.png)

Fig. 4.6 (a) Simulated PAE of NDPA according to (b) variable $R_{gt}$ versus fixed $R_{gt}$. 73
4.3 Frequency-dependence Consideration for Optimum Load Impedance

As we have seen in chapter 2.4 and 3, the optimum load impedance (R\text{opt}) determines drain line impedances in NDPAs. On the other hand, as the operating frequency increases in the NDPA, the R\text{opt} for determining the drain line impedance is observed to increase. Fig. 4.7 represents the R\text{opt} variation according to frequencies on the condition that the FET size is 6 × 125 μm and input power is 25 dBm at drain voltages of 30 V. As a result, the maximum output power cannot be obtained according to the frequency, and mismatch occurs, which degrades the overall power efficiency. For designing the more efficient NDPA, the frequency dependence of this R\text{opt} should be considered.

<table>
<thead>
<tr>
<th>R\text{opt} (Ω)</th>
<th>Pin=25 dBm</th>
</tr>
</thead>
<tbody>
<tr>
<td>6 GHz</td>
<td>88.6</td>
</tr>
<tr>
<td>9 GHz</td>
<td>90.1</td>
</tr>
<tr>
<td>12 GHz</td>
<td>115</td>
</tr>
<tr>
<td>15 GHz</td>
<td>113</td>
</tr>
<tr>
<td>18 GHz</td>
<td>116.5</td>
</tr>
</tbody>
</table>

Fig. 4.7 R\text{opt} variation according to frequencies (FET size: 6 × 125 μm, Pin: 25 dBm).
To make up for this mismatch, the four drain line impedances of the front end are designed according to the $R_{\text{opt}}$ of 6 GHz, and the four drain line impedances of the rear end are designed according to the $R_{\text{opt}}$ of 18 GHz. This rearrangement of the drain line impedances is because the transistors and drain lines on the rear end of the NDPA are more susceptible to high frequencies.

Fig. 4.8 shows the simplified schematic of a generalized NDPA and table 4.1 compares the drain line impedances at each sections according to the $R_{\text{opt}}$ setting.

![Simplified schematic of a generalized NDPA](image)

**Table 4.1**

<table>
<thead>
<tr>
<th>$Z_{o1}$ ($\Omega$)</th>
<th>$Z_{o2}$ ($\Omega$)</th>
<th>$Z_{o3}$ ($\Omega$)</th>
<th>$Z_{o4}$ ($\Omega$)</th>
<th>$Z_{o5}$ ($\Omega$)</th>
<th>$Z_{o6}$ ($\Omega$)</th>
<th>$Z_{o7}$ ($\Omega$)</th>
<th>$Z_{o8}$ ($\Omega$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{\text{opt}}=90$ $\Omega$</td>
<td>90</td>
<td>45</td>
<td>30</td>
<td>23</td>
<td>18</td>
<td>15</td>
<td>13</td>
</tr>
<tr>
<td>$R_{\text{opt}}=115$ $\Omega$</td>
<td>115</td>
<td>58</td>
<td>38</td>
<td>29</td>
<td>23</td>
<td>19</td>
<td>17</td>
</tr>
<tr>
<td>Mixed $R_{\text{opt}}$</td>
<td>90</td>
<td>45</td>
<td>30</td>
<td>23</td>
<td>23</td>
<td>19</td>
<td>17</td>
</tr>
</tbody>
</table>
At table 4.1, the $R_{\text{opt}}$ setting of 90 $\Omega$ is focused on the optimum output power at low frequencies near 6 GHz, while the $R_{\text{opt}}$ setting of 115 $\Omega$ is focused on the optimum output power at high frequencies above 12 GHz. In this work, the compromise is done in relation to frequency dependent $R_{\text{opt}}$. We call it the “mixed” $R_{\text{opt}}$ setting at table 4.1. Fig. 4.9 (a) and (b) show the simulated output power and PAE comparison between previous NDPA designed with the $R_{\text{opt}}$ setting of 90 $\Omega$ and new NDPA designed with “mixed” $R_{\text{opt}}$ setting.

Fig. 4.9 Simulated (a) output power and (b) PAE comparison between previous NDPA designed with the $R_{\text{opt}}$ setting of 90 $\Omega$ and new NDPA designed with “mixed” $R_{\text{opt}}$ setting.
From fig. 4.9 (a) and (b), simulation results show that the proposed design method improves average $P_{out}$ by 0.3 dB (from 40.9 to 41.2 dBm) and average PAE by 2.8% (from 18.6 to 21.4 %) at 6 ~ 18 GHz. When frequency-dependence for optimum load impedance is considered in the NDPA, both $P_{out}$ and PAE increase.
4.4 Practical Design and Measurement Results

4.4.1 Non-uniform distributed power amplifier design with a FET variable resistor

For design verification, two modified NDPA MMICs with a FET variable resistor has been fabricated by a commercial 0.25 \( \mu \text{m} \) GaN HEMT process. As mentioned above, the modified NDPA design which considers \( C_{ds} \) effect and uses the lower impedance line by doubling the phase of the first drain line instead of using a large-sized transistor at the first section is applied to two modified NDPA MMICs. Both NDPA MMICs are measured with mounted on 5-mm-thick Au-plated Cu zig with eutectic bonding or thermal epoxy to facilitate thermal dissipation. Both small-signal and large-signal measurements are performed by on-wafer probing using ground–signal–ground (GSG) probes and a probe station.

For PGT operation, \( R_{gt} \) is implemented as a FET variable resistor [3], [4]. To obtain the wanted \( R_{gt} \) variation range, a FET variable resistor should use the proper sized FET. Fig. 4.10 (a) and (b) represent the comparison of \( R_{gt} \) contours between \( 2 \times 125 \ \mu \text{m} \) GaN HEMTs and \( 4 \times 125 \ \mu \text{m} \) GaN HEMTs on the smith charts from 1 to 20 GHz. As shown in Fig. 4.10 (a) and (b), as the FET size is larger, a drain-source capacitance is larger at high \( R_{gt} \) mode. A large drain-source capacitance degrades output power and PAE at high frequencies under high \( R_{gt} \) mode. On the other hand, if the FET size is small, a resistance is too large to meet the wanted \( R_{gt} \) under low \( R_{gt} \) mode. In this NDPA, a \( 4 \times 125 \ \mu \text{m} \) GaN HEMT is selected. At high \( R_{gt} \) mode, a FET variable resistor acts as a capacitive resistor. The parasitic capacitance of a FET variable resistor makes the leakage of the reflected traveling wave at termination...
loads so that it seriously degrades output power and PAE at high frequencies. Fig. 4.11 (a) and (b) shows the degradation of S21, output power and PAE at 10 GHz by the parasitic capacitance of a FET variable resistor. Thus, a shunt inductor is connected with a FET variable resistor for $C_{ds}$ compensation at high frequencies under high $R_{gt}$ mode. As shown in Fig. 4.13, a FET variable resistor with a shunt inductor at high $R_{gt}$ brings about better PAE than that without a shunt inductor.

![Diagram](image1)

(a)

![Diagram](image2)

(b)

Fig. 4.10 Comparison of $R_{gt}$ contours between (a) 2 × 125 μm GaN HEMTs and (b) 4 × 125 μm GaN HEMTs on the smith charts from 1 to 20 GHz.
Fig. 4.11 Simulated (a) $S_{21}$ and (b) output power and PAE at 10 GHz of NDPA with a FET variable resistor with or without parasitic capacitances.

Fig. 4.12 Simulated PAE improvement due to a FET variable resistor with a shunt inductor at high $R_{gt}$. 

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At first, the first NDPA MMIC is designed and fabricated. The schematic of the first NDPA MMIC with a FET variable resistor is shown in Fig. 4.13. It consists of the six gain sections using $6 \times 125 \mu m$ GaN HEMTs and the two sections using $6 \times 75 \mu m$ and $2 \times 125 \mu m$ GaN HEMTs. Fig. 4.14 is a die photograph of the first NDPA with a FET variable resistor. The fabricated NDPA has a die size of $5.0 \text{ mm} \times 1.7 \text{ mm}$. As in the NDPAs of chapter 3, a Ruthroff impedance transformers are used at the output stage in the NDPA.

The measured output power and PAE at a drain voltage of 30 V according to $V_{\text{cont}}$ are shown in Fig. 4.15. Fig. 4.15 represents output power and PAE at $V_{\text{cont}}$ that
provides the optimum PAE according to frequencies in comparison with those at $V_{\text{cont}} = -2.4$ V. When the fabricated NDPA operates at the optimum $V_{\text{cont}}$, output power increases by average 0.22 dB (from 38.95 to 39.17 dBm) and PAE increases by average 1.2 % (from 14.6 to 15.8 %) compared to NDPA at $V_{\text{cont}} = -2.4$ V.

Fig. 4.15 Measured (a) output power and (b) PAE at the optimum $V_{\text{cont}}$ according to frequencies.
Although output power and PAE is increased at the first NDPA when output power is measured at the optimum $V_{\text{cont}}$ according to frequencies, the improvement does not satisfy the expectation. In particular, under low $R_{\text{gt}}$ ($V_{\text{cont}}=1 \, \text{V}$), the increase of output power and PAE is negligible when compared to ideal simulation. This is because peak gain at low $R_{\text{gt}}$ is decreased due to Q-factor lowered by gate line loss. Fig. 4.16 represents the decreased gain at $R_{\text{gt}} = 10 \, \Omega$ when ideal passive models such as transmission lines and MIM capacitors are replaced by practical passive design kits.

Fig. 4.16 Simulated gain at $R_{\text{gt}} = 10 \, \Omega$ when ideal passive models such as transmission lines and MIM capacitors are replaced by practical passive design kits.

To compensate loss at $R_{\text{gt}} = 10 \, \Omega$, inductive line is newly inserted before $R_{\text{gt}}$. In this case, the phase of $S21$ is upside-down but input return loss is improved so that gain at $R_{\text{gt}} = 10 \, \Omega$ largely increases as shown in Fig. 4.17 (a) and (b). So, including the inductive line, we have revised the first NDPA MMIC with a FET variable resistor. In addition, as mentioned above, the NDPA design considering the frequency dependent optimum load impedance is applied to the revised NDPA.
The schematic of the second NDPA MMIC with a FET variable resistor is shown in Fig. 4.18. It consists of the identical eight gain sections using $6 \times 125 \, \mu m$ GaN HEMTs. An inductive line is inserted in front of a FET variable resistor. As mentioned earlier, this is helpful to enhance PAE because input return loss is
improved and gain is increased at low $R_{gt}$ mode. Fig. 4.19 is a die photograph of the second GaN NDPA with a FET variable resistor. The fabricated NDPA has a die size of $5.0 \, \text{mm} \times 1.7 \, \text{mm}$.

Fig. 4.18 Circuit schematic of the second NDPA MMIC with a FET variable resistor.

Fig. 4.19 Photograph of the second GaN NDPA with a FET variable resistor (size = $5.0 \, \text{mm} \times 1.7 \, \text{mm}$).

Fig. 4.20 shows the measured S-parameters of NDPA according to variable $R_{gt}$ control bias ($V_{cont}$). Because of process variation, the pinch-off voltages of FET is
shifted to lower values than the first GaN process run. So, the reference \( V_{\text{cont}} \) is changed from -2.4 to -2.7 V. As expected from analysis, the measured \(|S21|\) fluctuates with the reference to \(|S21|\) at \( V_{\text{cont}} = -2.7 \) V according to \( V_{\text{cont}} \). The fluctuating \(|S21|\) range is from 8.0 to 11.7 dB from 6 to 18 GHz. The measured output power and PAE at a drain voltage of 30 V according to \( V_{\text{cont}} \) are shown in Fig. 4.21. In similar way to \(|S21|\) in Fig. 4.20, they fluctuates from 6 to 18 GHz according to \( V_{\text{cont}} \). Fig. 4.22 represents output power and PAE at \( V_{\text{cont}} \) that provides the optimum PAE according to frequencies in comparison with those at \( V_{\text{cont}} = -2.7 \) V. When the fabricated NDPA operates at the optimum \( V_{\text{cont}} \), output power increases by average 0.3 dB (from 39.8 to 40.1 dBm) and PAE increases by average 2.3 % (from 20 to 22.3 %) compared to NDPA at \( V_{\text{cont}} = -2.7 \) V.

### Table 4.2

**PERFORMANCE COMPARISON BETWEEN THE FIRST NDPA AND THE SECOND NDPA**

<table>
<thead>
<tr>
<th></th>
<th>Pout (dBm)</th>
<th>PAE (%)</th>
<th>DE (%)</th>
<th>( \Delta ) PAE (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>First NDPA</td>
<td>39.2</td>
<td>15.8</td>
<td>20.1</td>
<td>1.2</td>
</tr>
<tr>
<td>Second NDPA</td>
<td>40.1</td>
<td>22.3</td>
<td>26.1</td>
<td>2.3</td>
</tr>
<tr>
<td>( \Delta ) (Sum)</td>
<td>+0.9</td>
<td>+6.5</td>
<td>+6</td>
<td>+1.1</td>
</tr>
</tbody>
</table>
Fig. 4.20 Measured S-parameters of NDPA according to $V_{\text{cont}}$ ($V_{\text{D1}} = 27 \text{ V}, V_{\text{G1}} = -2.8 \text{ V}$).

Fig. 4.21 Measured output power and PAE of NDPA according to $V_{\text{cont}}$ ($V_{\text{D1}} = 30 \text{ V}, V_{\text{G1}} = -2.8 \text{ V}$, input power $= 31 \sim 33 \text{ dBm}$).
Input power versus output power and PAE is shown in Fig. 4.23. At 7 GHz, the PAE at $V_{\text{cont}} = 1.0$ V is higher by 4.3% than that at $V_{\text{cont}} = -2.7$ V, while at 13 GHz, the PAE at $V_{\text{cont}} = -5.0$ V is higher by 6.8% than that at $V_{\text{cont}} = -2.7$ V.

Table 4.2 summarizes the performance comparison between the first NDPA and the second NDPA. Output power increases by average 0.9 dB (from 39.2 to 40.1 dBm) and PAE increases by average 6.5% (from 15.8 to 22.3%) when the second NDPA is compared to the first NDPA. The remarkable performance improvement confirms the effectiveness of the proposed compensation ideas and the NDPA design considering the frequency dependent optimum load impedance.

For the fair comparison, several NDPA MMICs having both a FET variable resistor and a thin film resistor (TFR) as $R_{gt}$ are measured. Two MMICs which have almost the same output power and PAE characteristics are selected. One MMIC removes a
TFR by a laser-cutter and the other MMIC removes a FET variable resistor by a laser-cutter. The measured results of two MMICs are shown in Fig. 4.24. When compared to the conventional NDPA with a TFR, the proposed NDPA obtains the increased output power by average 0.5 dB (from 38.6 to 39.1 dBm) and the increased PAE by average 3.1 % (from 18.3 to 21.4 %) at a drain voltage of 27 V.

Fig. 4.23 Input power versus output power and PAE according to \( V_{\text{con}} \) at (a) 7 GHz and (b) 13 GHz.
4.4.2 Programmable gate line termination resistance switching technique implementation to non-uniform distributed amplifiers

From the above measurements, it can be confirmed that the proposed PGT method is effective to enhance the PAE of NDPA. Now, PGT remains to be actually implemented. It can be achieved by digitally assisted automatic switching. The block diagram of the PGT implementation is shown in Fig. 4.25. The operation principle is as follows. Input power sensed by an RF coupler is entered to a power divider. Two port signals come from a power divider. One of two port signals enters to a power detector and the other enters to a power meter for monitoring input power. A test pattern which is the almost same as gate lines of a NDPA is connected to the input of a power detector.
The test pattern receives a signal coming from one output port of a power divider and produces the standing wave similar to one caused by the reflection at gate lines of NDPA. A power detector converts the standing wave to dc voltages in proportion to the frequency-dependent voltage swing of the standing wave signal. The converted dc voltage is amplified by a non-inverting voltage gain amplifier using op-amps. A comparator compares the amplified dc voltage with the reference voltage and if it is higher than the reference voltage, a comparator outputs 1 V and otherwise, -5 V. Finally, a dc voltage outputted from a comparator is supplied to the gate voltage of a FET variable resistor in the NDPA MMIC, so that the NDPA MMIC can operate by PGT. The experimental set-up for PGT operation of NDPA is shown in Fig. 4.26.
MACP-010562 from MA/COM Inc. is used as a power detector and AD8067 from Analog Devices Inc. is used as an op-amp and a comparator. Total power consumption of the set-up is only 52.5 mW. It does not almost affect to the overall PAE of NDPA. Fig. 4.27 represents the dc output voltages converted by a power detector according to frequencies. As expected, the standing wave generated by the test pattern results in the fluctuating dc voltages according to frequencies similarly to a NDPA. But above 15 GHz, due to high frequency effect, the test pattern exactly reproduces the standing wave generated from the gate lines of a NDPA and the gain fluctuation by $V_{cont}$ variation is small as observed in Fig. 4.20. This is the reason to fail to obtain the wanted $V_{cont}$ values at high frequencies above 15 GHz. Although the PAE difference by $V_{cont}$ variation is not large at high frequencies as observed in Fig. 4.21, this is room to need to be improved in the future.
Fig. 4.27 Output voltage from a power detector at input power of 14 dBm according to frequencies (the marked numbers indicate the measured $V_{\text{cont}}$ values and the numbers in parentheses indicate the wanted $V_{\text{cont}}$ values).

Fig. 4.28 Measured output power and PAE comparison between manual $V_{\text{cont}}$ switching and PGT operation in the identical NDPA ($V_{G1} = 27$ V, $V_{G1} = -2.9$ V, input power = 31 ~ 33 dBm).
Fig. 4.28 shows the measured output power and PAE comparison between manual $V_{\text{cont}}$ switching and PGT operation in the identical NDPA under a drain voltage of 27 V. When the NDPA operates at the fixed $V_{\text{cont}} = -2.7$ V, the measured output power is average 38.67 dBm and the measured PAE is average 17.98 % from 6 to 18 GHz. When the NDPA operates by PGT, the measured output power increases by average 0.37 dB (from 38.67 to 39.04 dBm) and the measured PAE increases by average 2.09 % (from 17.98 to 20.07 %). Compared to the NDPA by manual $V_{\text{cont}}$ switching, the NDPA by PGT degrades output power and PAE only by 0.06 dB and 0.09 % on average.

The power sweep characteristics of NDPA using PGT at 7 GHz and 13 GHz is measured as shown in Fig. 4.29 (a) and (b). At 7 GHz, until $P_{\text{in}}$ is smaller than 27 dBm, NDPA operates under $V_{\text{cont}} = -5$ V, which is the default value in the comparator and when $P_{\text{in}}$ is larger than 27 dBm, $V_{\text{cont}}$ starts to increase toward 1.0 V. When $P_{\text{in}}$ is equal to about 31 dBm, $V_{\text{cont}}$ is changed to 1.0 V and output power and PAE increase rapidly so that the NDPA obtains more enhanced output power and PAE at 7 GHz. At 13 GHz, because the wanted $V_{\text{cont}}$ is equal to the default value in the comparator, $V_{\text{cont}}$ keep the initial value to the end and the NDPA obtains the wanted output power and PAE at 13 GHz. From these measurements, it is verified that the proposed PGT is successfully implemented with help to analog and digital circuits in an external PCB and improves the performance of NDPA.
Fig. 4.29 Measured power sweep characteristics of NDPA using PGT at (a) 7 GHz and (b) 13 GHz.
Table 4.3 compares the performance of the NDPA of this work with the state-of-the-art GaN NDPAs and RMPAs using GaN MMIC process. The NDPA of this work obtains PAE more than 20 % due to the proposed PGT. This represents the second highest PAE among wideband GaN PAs having more than 10 W. [1], [7] and [9]

<table>
<thead>
<tr>
<th>Ref.</th>
<th>Freq. (GHz)</th>
<th>Topology</th>
<th>Pout (W)</th>
<th>PAE (%)</th>
<th>Linear Gain (dB)</th>
<th>Area (mm²)</th>
<th>Power density (W/ mm²)</th>
<th>Number of combining</th>
</tr>
</thead>
<tbody>
<tr>
<td>[5]</td>
<td>6-18</td>
<td>RMPA¹</td>
<td>20.0</td>
<td>15.0</td>
<td>15-18</td>
<td>19.2</td>
<td>1.04 (pulsed²)</td>
<td>1-way</td>
</tr>
<tr>
<td>[1]</td>
<td>2-17</td>
<td>NDPA</td>
<td>9.1</td>
<td>26.0</td>
<td>10-14</td>
<td>12.6</td>
<td>0.72 (CW)</td>
<td>1-way</td>
</tr>
<tr>
<td>[6]</td>
<td>6-18</td>
<td>NDPA</td>
<td>12.9</td>
<td>18.0</td>
<td>8-10</td>
<td>18.7</td>
<td>0.69 (pulsed)</td>
<td>2-way</td>
</tr>
<tr>
<td>[7]</td>
<td>2-15</td>
<td>NDPA</td>
<td>5.5</td>
<td>25.0</td>
<td>10-13</td>
<td>10.1</td>
<td>0.55 (CW)</td>
<td>1-way</td>
</tr>
<tr>
<td>[8]</td>
<td>6-18</td>
<td>RMPA</td>
<td>7.7</td>
<td>17.6</td>
<td>18-25</td>
<td>19.8</td>
<td>0.39 (CW)</td>
<td>1-way</td>
</tr>
<tr>
<td>[9]</td>
<td>2-20</td>
<td>NDPA</td>
<td>16</td>
<td>25.9</td>
<td>10-15</td>
<td>38.3</td>
<td>0.42 (CW)</td>
<td>2-way</td>
</tr>
<tr>
<td>[10]</td>
<td>6-18</td>
<td>RMPA</td>
<td>10.6</td>
<td>16.9</td>
<td>20-25</td>
<td>19.3</td>
<td>0.55 (CW)</td>
<td>1-way</td>
</tr>
<tr>
<td>[11]</td>
<td>16-40</td>
<td>NDPA</td>
<td>13</td>
<td>16</td>
<td>24</td>
<td>15.6</td>
<td>0.83 (pulsed)</td>
<td>2-way</td>
</tr>
<tr>
<td>This work 1</td>
<td>6-18</td>
<td>2-way NDPA</td>
<td>21.0</td>
<td>19.2</td>
<td>17-21</td>
<td>11.0</td>
<td>1.9 (CW)</td>
<td>2-way</td>
</tr>
<tr>
<td>This work 2</td>
<td>6-18</td>
<td>4-way NDPA</td>
<td>20.8</td>
<td>13.6</td>
<td>13-17</td>
<td>21.0</td>
<td>0.99 (CW)</td>
<td>4-way</td>
</tr>
<tr>
<td>This work 3</td>
<td>6-18</td>
<td>NDPA+PGT³</td>
<td>10.3</td>
<td>22.3</td>
<td>8-12</td>
<td>8.5</td>
<td>1.21 (CW)</td>
<td>1-way</td>
</tr>
</tbody>
</table>

¹ Reactive Matched PA,
² Pulsed wave signal power measurement
³ Programmable Gate termination resistance Technique
have been fabricated by the advanced internal GaN MMIC process. It is notable that the NDPA of this work obtains PAE more than 20% and output power more than 10 W by applying a simple circuit idea using a commercial GaN MMIC process.
4.5 Conclusions

In this work, to obtain enhanced PAE, the programmable gate line termination resistance switching technique is proposed and verified experimentally in the NDPA. Programmable gate line termination resistance effectively increases output power and PAE by boosting power gain through the standing wave generated by mismatched terminations according to frequencies. A shunt inductor is connected with a FET variable resistor for $C_{ds}$ compensation at high frequencies under high $R_{gs}$ mode. To compensate loss at low $R_{gs}$ mode, inductive line should be inserted before $R_{gs}$. In this case, the phase of S21 is upside-down but input return loss is improved so that gain at low $R_{gs}$ mode largely increases. For designing the more efficient NDPA, the frequency dependence of this $R_{opt}$ should be considered. To make up for this mismatch, the four drain line impedances of the front end are designed according to the $R_{opt}$ of 6 GHz, and the four drain line impedances of the rear end are designed according to the $R_{opt}$ of 18 GHz. Output power increases by average 0.9 dB (from 39.2 to 40.1 dBm) and PAE increases by average 6.5 % (from 15.8 to 22.3 %) When the proposed design are applied to NDPAs. The remarkable performance improvement confirms the effectiveness of the proposed compensation ideas and the NDPA design considering the frequency dependent optimum load impedance.

The practical implementation to programmable gate line termination resistance switching technique can be achieved by digitally assisted automatic switching. Compared to the NDPA by manual $V_{cont}$ switching, the NDPA by programmable gate line termination resistance switching technique degrades output power and PAE only by 0.06 dB and 0.09 % on average. From these measurements, it is verified that the proposed programmable gate line termination resistance switching technique is
successfully implemented with help to analog and digital circuits in an external PCB and improves the performance of NDPA. In conclusion, the NDPA of this work obtains PAE more than 20 % due to the proposed PAE enhancement method. This represents the second highest PAE among wideband GaN PAs having more than 10 W.
4.6 References


Chapter 5

Pulsed Power Measurement to Avoid Thermal Limit

5.1 Introduction

In this chapter, the pulsed power measurement is introduced to avoid thermal limit. The GaN NDPA MMICs fabricated in the previous chapters are tested in this measurement. In this experiment, we will investigate how the output power of each NDPA improves when the thermal degradation is minimized by pulse measurement. Also, the influence of the pulse driven method is investigated to each NDPA and the output power characteristics of NDPA is measured according to the period and the duration of the pulse.

5.2 Measurement Set-up

The pulsed power measurement can be done by two way. One way is to supply only pulsed input power to a device under test (DUT) and the other way is to supply both pulsed input power and pulsed DC biases. In the case of GaN MMICs, because of high drain voltages more than 25 V, DC power consumption is larger than any other MMICs and thermal degradation by biases itself is non-negligible. Therefore, the latter is expected to minimize thermal effects to GaN NDPA MMICs. Fig. 5.1 shows the block diagram of pulsed power measurement set-up in this work. A HP 83650B signal generator supplies pulsed input signal to a DUT. An Agilent 33250A function generator supplies a pulsed gate bias to a DUT. At the same time, a HP 83650B is connected to an Agilent 33250A function generator to the synchronization of pulsed signal. Then, a pulsed input power and a pulsed gate bias are simultaneously supplied at the NDPA. Because drain biases can give more serious damage to DUTs than gate biases, they are supplied as DC type by an E3649A, general DC power supply. The
pulsed output signal from a DUT is measured by Agilent N1912A peak power meters and N1921A peak power sensors.

Fig. 5.1 Block diagram of pulsed power measurement set-up.

Fig. 5.2 Pulsed power sweep according to (a) the pulse width and (b) the duty cycles in the NDPA at 11 GHz and \( V_{D1} = 27 \, \text{V} \).
By the measurement set-up in Fig. 5.1, pulsed power is swept according to the pulse width and duty cycles. One-way NDPA with a FET variable resistor in chapter 4 is used as a DUT. Fig. 5.2 represents the measurement results. Measured output power does not agree with theoretical expectation. The limited sensitivity of power supply does not make DUTs reflect thermal improvement by pulsed power measurement. Even if there is a sensing limit in this set-up, we have found that the pulse width has more affect to output power than the duty cycle from these measurements. We take the sensing limit at the pulse width of 20 ms and the duty cycle of about 10%.

5.3 Measurement Results

Three NDPA MMICs are all tested at the pulse width of 20 mA and the duty cycle of 5 ~ 10 % by the measurement set-up in Fig. 5.1. First, a two-way NDPA MMIC is tested. When a pulsed input power and a pulsed bias are simultaneously supplied at the NDPA with 20 ms pulse width and 400 ms period, pulsed $P_{out}$ increases by 0.2 dB (average 43.2 dBm) compared to CW at drain voltages of 30 V and at drain voltages of 33 V, $P_{out}$ increases to the extent of 42.5 ~ 44.8 dBm (average 43.8 dBm) as shown in Fig. 5.3.

![Fig. 5.3 Measured pulsed power of a two-way NDPA MMIC.](image)
Second, a four-way NDPA MMIC is tested in the same way. When a pulsed input power and a pulsed bias are simultaneously supplied at the NDPA, pulsed $P_{\text{out}}$ increases by 1.2 dB (average 43.8 dBm) compared to CW at drain voltages of 30 V and at drain voltages of 33 V, $P_{\text{out}}$ increases by 1.0 dB (average 44.1 dBm) as shown in Fig. 5.4 (a) and (b).

Fig. 5.4 Measured pulsed power of a four-way NDPA MMIC at (a) $V_{\text{d2}}=30$ V and (b) $V_{\text{d2}}=33$ V.
Finally, a one-way NDPA MMIC with a FET variable resistor is tested in the same way. When a pulsed input power and a pulsed bias are simultaneously supplied at the NDPA, pulsed $P_{\text{out}}$ increases by 0.29 dB (average 40.26 dBm) compared to CW at drain voltages of 30 V and at drain voltages of 33 V, $P_{\text{out}}$ increases to average 40.54 dBm as shown in Fig. 5.5.

![Fig. 5.5 Measured pulsed power of one-way NDPA MMIC with a FET variable resistor at $V_{D1}=30$ V and $V_{D1}=33$ V.](image)
5.4 Conclusions

In this chapter, the pulsed power measurement is performed to avoid thermal limit. The GaN NDPA MMICs fabricated in the previous chapters are tested in this measurement. A pulsed input power and a pulsed gate bias are simultaneously supplied at the NDPA. Even if there is a sensing limit in this set-up, we have found that the pulse width has more affect to output power than the duty cycle from these measurements. We take the sensing limit at the pulse width of 20 ms and the duty cycle of about 10 %. Three GaN NDPA MMICs are all tested at the pulse width of 20 mA and the duty cycle of 5 ~ 10 % by the measurement set-up. From the measurement results, a four-way GaN NDPA MMIC shows the most improved output power performance among the three GaN NDPAs when the pulsed power is measured. This means that as the number of combining increases in the GaN NDPA, the thermal limitation inevitably become apparent, so that it degrades the output power performance. Therefore, when the number of combining increases in the GaN NDPA, more careful thermal dissipation techniques are required such as thermal attachment, thermal cooling and FET layout etc.
Chapter 6

Conclusions

In this work, the modified NDPA is designed and implemented to obtain the enhanced wideband power and power added efficiency. We have built up an Angelov-based GaN HEMT large-signal model that incorporates a thermal model and is based on various measurements. The output power characteristics of DPA which is designed by in-house GaN HEMT large signal model show better agreement with the measured value than those by the model provided by the foundry.

Next, basic non-uniform distributed power amplifier design theory is investigated to enhance the output power of DA. From budgeting the specification, we have found the challenge that our NDPA should inevitably use the large sized FETs for enhanced output power.

The effect of output capacitance is considered in the NDPA design. After the $C_{ds}$ is added to the existing drain line impedance to make an equivalent model with the π-type line, the line impedance is readjusted to have the $R_{opt}$ at the center frequency. Besides, instead of using a large-sized transistor at the first section in the NDPA, a
method of halving the characteristic impedance ($Z_o$) by doubling the phase of the drain line is proposed. Power gain and the output power characteristics close to the ideal NDPA's can be obtained through the simulation and the analysis. As practical design examples, the compact two-way and four-way power-combined NDPA are demonstrated using a commercial 0.25 μm GaN HEMT MMIC process. The proposed NDPA successfully achieves RF power of tens of watts through the octave bandwidth, which is required for electronic warfare systems.

On the other hand, to obtain enhanced PAE, the programmable gate line termination resistance switching technique is proposed and verified experimentally in the NDPA. Programmable gate line termination resistance effectively increases output power and PAE by boosting power gain through the standing wave generated by mismatched terminations according to frequencies. A shunt inductor is connected with a FET variable resistor for $C_{ds}$ compensation at high frequencies under high $R_{gt}$ mode. To compensate loss at low $R_{gt}$ mode, inductive line should be inserted before $R_{gt}$. For designing the more efficient NDPA, the frequency dependence of this $R_{opt}$ should be considered. To make up for this mismatch, the four drain line impedances of the front end are designed according to the $R_{opt}$ of 6 GHz, and the four drain line impedances of the rear end are designed according to the $R_{opt}$ of 18 GHz. When the proposed design are applied to NDPAs. The remarkable performance improvement confirms the effectiveness of the proposed compensation ideas and the NDPA design considering the frequency dependent optimum load impedance.

The practical implementation to programmable gate line termination resistance switching technique can be achieved by digitally assisted automatic switching. From various measurements, it is verified that the proposed programmable gate line
termination resistance switching technique is successfully implemented with help to analog and digital circuits in an external PCB and improves the performance of NDPA.

The pulsed power measurement is performed to avoid thermal limit. The GaN NDPA MMICs fabricated in the previous chapters are tested in this measurement. A pulsed input power and a pulsed gate bias are simultaneously supplied at the NDPA. From the measurement results, a four-way GaN NDPA MMIC shows the most improved output power performance among the three GaN NDPAs when the pulsed power is measured. Therefore, when the number of combining increases in the GaN NDPA, more careful thermal dissipation techniques are required such as thermal attachment, thermal cooling and FET layout etc.

In conclusion, When the modified NDPA design are applied to NDPAs, the high power density with output power over 20 W and the high PAE over 20 % can be achieved by the fabricated NDPAs. This work demonstrates that the modified NDPA can provide more enhanced output power and power added efficiency performance in the wideband GaN PAs.
초록

본 학위 논문에서는 군수용 농동 전자주사식 위상배열 레이더와 전파 방해 시스템의 핵심부품인 광대역 전력증폭기를 구현하고자 고주파 전력 특성이 우수한 상용 갈륨질화 (GaN) 반도체 공정을 사용하여 광대역에서 고출력, 고효율의 출력전력을 얻기 위한 연구를 진행하였다.

먼저 전력증폭기 설계에 근간이 되는 열효과를 포함한 대신호 모델링을 진행하였다. 6×125 μm GaN HEMT 소자에 대해 DC 및 RF 측정을 수행하였고 얻어진 값을 잘 알려진 Angelov 모델 수식에 맞추어 모델링하였다. 또한 펄스 IV 측정을 수행하여 열저항 값을 추출하여 열모델 등가회로를 구성하였으며 주파수 분산 현상을 반영하기 위해 RF Ids 와 DC Ids 를 구분하여 각각 모델링하였다. 열저항 추출 시 실제 MMIC 측정 환경과 유사한 상태를 되도록 동일한 지그 위에 소자를 thermal pasting 하여 측정하였다. 모델 검증을 위해 6 ~ 18 GHz, 8.1 W 균일 분산전력증폭기를 설계하여 측정값과 비교하였으며 파운드리에서
제공하는 대신호 모델보다 더 측정치에 가까운 출력전력특성을 얻을 수 있었다.

둘째로, 광대역에서 출력전력을 향상시키기 위해 기존 비균일 분산전력 중폭방식 설계를 개선하는 연구를 수행하였다. 기존 설계 방식은 드레인-소스 캐패시턴스가 전송선로에 흡수된다는 가정 하에 이것의 영향을 무시하고 설계를 하였으나 출력전력을 높이기 위해 트랜지스터의 사이즈를 키울 경우 그리고 주파수가 높아질수록 더 이상 무시할 수 없는 상태가 된다. 또한 분산전력중폭기를 구성하는 각 트랜지스터가 최적의 출력임피던스를 갖게 되도록 드레인 라인 임피던스를 구성하는 과정에서 첫 번째 드레인 라인 임피던스의 크기가 통상 100 Ω 이상이 되어 공정 한계를 넘어가게 되는 문제가 발생하게 된다. 기존 설계 방식은 이를 막기 위해 앞단에 큰 사이즈의 트랜지스터를 사용하므로 증가된 게이트-소스 캐패시턴스 및 드레인-소스 캐패시턴스가 고주파 전력이득 및 출력전력 을 떨어뜨리는 원인이 된다. 본 연구에서는 드레인-소스 캐패시턴스를 반영한 비균일 분산전력중폭기 설계를 제안하였는데 기존 드레인 라인 임피던스에 드레인-소스 캐패시턴스를 추가하여 π-type 라인으로 등가 모
델화한 후 중심 주파수에서 최적의 출력임피던스를 갖도록 라인 임피던스를 재조정하였다. 이러한 설계 방법을 적용하여 기존 방식보다 6 ~ 18 GHz에서 평균 0.4 dB의 출력전력을 향상시킬 수 있었다. 또한 앞단에 큰 사이즈의 트랜지스터를 사용하는 대신 드레인 라인의 위상을 두 배로 증가시켜 임피던스를 절반으로 낮추는 방식을 제안하였다. 라인 길이 증가에 따른 손실을 분석한 결과 기존 방식보다 고주파 손실이 줄어들게 되어 이중적인 분산전력증폭기에 가까운 전력이득 및 출력전력 특성을 얻을 수 있었다. 한편 출력전력을 더욱 증가시키기 위해 비균일 분산전력 증폭기를 전력 결합하게 되는데 이 경우 게이트 라인 및 드레인 라인 길이가 길어져 칩 사이즈가 커지는 문제가 있어 왔다. 이를 개선하기 위하여 본 연구에서는 전력 결합되는 각 분산전력증폭기의 드레인 라인을 공유하는 전력결합방식을 제안하였다. 드레인 라인을 공유하게 되면 전력 결합에 필요한 임피던스 변환기와 전력결합기의 개수가 줄어들어 칩 사이즈 및 손실을 줄일 수 있으며 라인 임피던스를 드레인 라인을 공유하기 전과 동일한 임피던스로 가져갈 경우 라인 길이가 절반이라 줄어들게 되어 보다 컴팩트한 구조로 광대역에서 출력전력 및 전력밀도를 높일 수 있었다.
있게 된다. 뿐만 아니라 드레인 라인 공유로 인해 각 트랜지스터의 드레인-소스 저항이 병렬 연결되므로 큰 사이즈의 소자를 사용할 경우 감소된 드레인-소스 저항으로 인하여 출력 리턴로스가 향상되는 부가적인 이득을 얻을 수 있다.

이상에서 제안된 설계방식을 상용 0.25 μm GaN 단일 고주파 집적회로공정을 사용하여 실제 MMIC에 적용 및 검증해보았다. 6×125 μm의 GaN HEMT 소자를 사용하여 2-way, 2단, 8차 비균일 분산전력증폭기 MMIC를 설계 및 제작하여 측정한 결과 6 ~ 18 GHz에서 16.8 ~ 21.8 dB의 선형이득과 평균 21 W의 연속파 출력전력 및 19.2 %의 전력부가효율을 나타내었다. 특히 제안된 설계방식을 통해 유사한 광대역 주파수 대역에서 가장 높은 1.9 W/mm²의 전력밀도를 얻을 수 있었다. 이번에는 제안된 전력결합방식을 확장하여 4-way, 2단 비균일 분산전력증폭기 MMIC를 설계, 제작하여 측정하였다. 전력결합수를 늘리는 대신 6×75 μm의 GaN HEMT 소자를 사용하였다. 6 ~ 18 GHz에서 13 ~ 17 dB의 선형이득과 평균 20.8 W의 연속파 출력전력 및 14 %의 전력부가효율을 나타내었다. 특히 펄스파 측정 시 평균 26 W의 출력전력을 나타내었으며 13 GHz에서는 40
W의 최대출력전력을 얻을 수 있었다. 제안된 컴팩트한 전력 결합 방식을 통해 4개의 비균일 분산전력증폭기를 전력 결합할 수 있었고 이로 인해 유사한 광대역 주파수 대역에서 가장 높은 출력전력 특성을 얻을 수 있었다. 이상의 결과를 통해 제안된 설계방식의 타당성과 효과를 검증할 수 있었다.

셋째로는, 광대역에서 전력효율을 향상시키기 위한 분산전력증폭기 설계를 제안하였다. 고효율로 동작하는 분산전력증폭기를 얻기 위해 게이트 라인 종결저항을 가변시켜 주파수에 따라 전력이득을 높게 가져가는 구조를 제안함으로 효율을 향상시킬 수 있었다. 일반적으로 비균일 분산전력증폭기를 설계할 때 출력전력 및 효율의 손실을 막기 위해 드레인 종결저항을 제거하게 된다. 이 경우 분산전력증폭기의 전력이득 수식으로부터 게이트 라인 종결저항의 값에 따라 그동안 크기가 작아 무시되어 오던 게이트 라인 및 드레인 라인의 반사파 성분들이 커지게 되고 이것에 따라 전력이득의 리플을 형성하게 된다. 이 리플을 활용하여 원하는 주파수에서 전력이득을 크게 가져갈 경우 기존보다 전력효율을 향상시킬 수 있게 된다. 그러나 이러한 아이디어를 반영하여 1차 분
산전력증폭기 MMIC를 제작한 결과, 분산증폭기의 출력 전력 및 전력부가효율 증가가 각각 0.22 dB와 1.2 %에 머물렀다. 시뮬레이션 분석 결과, 게이트 라인의 손실로 인해 낮은 게이트 라인 종결 저항 값에서 최대 전력이득이 감소하는 문제를 확인하였고 이를 보상하기 위해 게이트 라인 종결 저항 앞에 인덕티브한 라인을 삽입하여 입력리턴로스를 향상시킴으로써 전해진 전력이득을 증가시킬 수 있었다. 한편 동작주파수가 증가할수록, 드레인 라인 임피던스를 결정하는 최적의 부하저항 값이 증가하는 현상이 관찰되었다. 이로 인해 주파수에 따라 최적의 출력전력을 얻지 못하고, mismatch가 생겨나 효율 손실을 일으키는 문제가 발생한다.

이것을 만회하기 위해 앞단 4개의 드레인 라인 임피던스는 6 GHz의 최적 부하저항 값에 따라 설계하고, 뒷단 4개의 드레인 라인 임피던스는 18 GHz의 최적 부하저항 값에 따라 설계하였다. 이렇게 정한 이유는 뒷단의 트랜지스터와 드레인 라인들이 더욱 고주파의 영향을 많이 받기 때문이다. 시뮬레이션 결과 제안된 설계방식을 통해 6 ~ 18 GHz에서 0.3 dB의 출력전력 및 2.8 %의 전력부가효율 향상을 나타내었다. 이상의 설계를 분산전력증폭기 2차 MMIC 제작에 반영하였다. 측정 결과 6 ~ 18 GHz에서
평균 39.8 dB의 출력전력 및 20 %의 전력부가효율을 나타내었고 주파수에 따라 게이트 라인 종결 저항 값을 튜닝할 경우 0.3 dB의 출력전력 향상 및 2.3 %의 전력부가효율 향상을 얻을 수 있었다. 특히 13 GHz에서는 게이트 라인 종결 저항 튜닝 시 1.24 dB의 출력전력 향상 및 6.8 %의 전력부가효율 향상을 보였다. 결론적으로 인덕티브 라인의 삽입 및 주파수 의존적 최적 부하 저항을 고려한 드레인 라인 임피던스 재조정 설계의 도입으로 1차 MMIC 대비 대역 평균 0.9 dB의 출력전력 향상과 6.5 %의 전력부가효율 향상과 더불어 게이트 라인 종결 저항 튜닝 시 1.1 %의 추가적인 전력부가효율향상을 얻을 수 있었다. 또한 동일한 공정을 사용한 기존 분산전력증폭기 대비 3 %의 효율 향상을 얻을 수 있었다. 제안한 아이디어가 분산전력증폭기의 효율 향상에 기여함을 검증할 수 있었다. 이제 주파수에 따라 게이트 라인 종결 저항 값을 자동으로 스위칭하기 위한 회로를 구성하였다. 입력 신호의 일부를 10 dB 커플러로 가져와 일킨슨 전력분배기를 통과시켜 한쪽 신호는 기존 사용하던 RF 전력을 감지하는 용도를 사용하고 나머지 한쪽 신호는 power detector로 들어가게 하는데 이 때 분산전력증폭기의 게이트 라인 회로와 동일한 회로를 따로
만들어 power detector 앞에 shunt로 연결시켜준다. 이것은 주파수에 따라 분산전력증폭기의 게이트 라인 종결저항의 mismatch로 인해 발생하는 standing wave를 재현시켜주는 용도로, 여기서 발생하는 전압스윙을 power detector가 읽도록 하여 주파수에 따라 다른 전압 값을 내보내도록 하기 위한 것이다. 이것을 op-amp로 증폭시킨 후 비교기에 입력시켜 기준 전압과 비교하게 하면 주파수에 따라 출력전력이 높은 게이트 라인 종결 저항 값이 되도록 원하는 전압을 생성시키게 만들어줄 수 있는 것이다. 이 생성된 전압이 가변저항용 트랜지스터의 게이트 단자로 들어가게 된다. 테스트 결과 게이트 라인 종결 저항 값에 따라 효율 차이가 심한 주파수 대역에서 이상적인 종결저항 값으로 분산전력증폭기가 동작하는 것을 확인할 수 있었으며 전압 생성 오류로 인한 효율 감소는 대역 평균 0.1 %에 불과했다. 따라서 프로그램이 가능한 게이트 라인 종결 저항 스위칭 방식과 주파수 의존적 최적 부하 저항을 고려한 드레인 라인 임피던스 재조정 설계를 통해 분산전력증폭기의 효율을 향상시킬 수 있음을 확인할 수 있었다.

본 연구를 통해 기존 비균일 분산전력증폭기 설계방법을 개선하여 6 ~
18 GHz에서 평균 20 W 이상의 출력전력과 1.9 W/mm²의 전력밀도를 갖는 비균일 분산전력증폭기를 구현하였고 프로그램이 가능한 게이트 라인 종결 저항 스위칭 방식을 통해 6~18 GHz에서 평균 출력전력 10 W, 평균 20 % 이상의 전력부가효율을 갖는 광대역 전력증폭기를 구현할 수 있었다.

주요어 : GaN, 비균일 분산전력증폭기, 전력결합, 광대역, 효율, MMIC

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