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Ph.D. DISSERTATION

Characteristics of La-incorporated TiN and Ru-based metal gates on Hf-based Gate Dielectrics for CMOSFETs

by

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Characteristics of La-incorporated TiN and Ru-based metal gates on Hf-based Gate Dielectrics for CMOSFETs

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Abstract

The minimum feature size, including gate oxide thickness, of complementary metal oxide semiconductor field effect transistors (CMOSFETs) has decreased exponentially until now. However, with this method, scaling slows down at the 90 nm node as SiO$_2$ runs out of atoms and further scaling is limited due to the increase of gate-leakage current. To continue the scaling of transistors, various high-$k$ oxide materials have been studied intensively for the past few decades. The semiconductor industry has already converged on Hf-based oxides for the first generation CMOS products featuring high-$k$ gate dielectrics and metal gate electrodes. However, even though various metal materials were already used on Hf-based oxides, there are still several crucial problems that need to be considered; an effective work function (EWF) modulation for adjusting the threshold voltage ($V_t$) of transistors and further scaling of equivalent oxide thickness (EOT), which was approximately 1.0 nm for the first generation high-$k$/metal gate device.

Continued gate length ($L_g$) scaling for the 32 nm and beyond with a planer structure requires sub-nm EOT to suppress short-channel effects. Fully depleted device structures, such as FinFET or extremely thin SOI (ETSOI), improve short-channel control and thus relax the requirements for EOT scaling. However, the insertion point of such device architectures is expected to be the 22 nm and beyond and sub-nm EOT may be still required at those advanced technology nodes.

To meet continued EOT scaling until the turning point in device architectures, mainly three possible EOT scaling approaches are studied in this work: (1) a high-$k$ material with $k$-value greater than that of HfO$_2$ (so-called “higher-$k$”), (2) the physical thickness reduction of interfacial layer (IL) (so-called “scavenging”), (3) suppression of low-$k$ dielectric layer between metals and dielectrics (so-called “deadlayer effect”).

Firstly, the relation between the permittivity and microstructures of atomic layer deposited Hf$_{1-x}$Si$_x$O$_y$ (HfSiO) thin films with different Si concentrations as a function of post-deposition annealing (PDA) temperature was investigated. The PDA at high temperature results in the separation of crystallized HfO$_2$ phase from the much higher Si-
containing amorphous-like matrix. Tetragonal phase HfO₂ formation with higher permittivity than the monoclinic HfO₂ phase is induced with an appropriate Si concentration in the film (~10–20%). In the crystallized HfSiO film, the Si concentration in the phase-separated HfO₂ (mainly consisting of HfO₂) could be controlled by PDA temperature, which determines the degree of phase separation. The increased PDA temperature reduces the Si concentration in the phase-separated HfO₂ which induced monoclinic phase formation. Therefore, the PDA temperature for maximized permittivity of the crystallized HfSiO films (maximized tetragonal phase portion in the film) depends on the Si concentration of the HfSiO film in the as-deposited state. However, considering the maturity of Hf-based high-κ gate dielectrics, scaling SiO₂-based IL in conjunction with Hf-based oxides may be more practical in meeting the requirements for the 22 nm technology node and beyond.

Secondly, lanthanum (La)-incorporated TiN metal gates, such as TiN/La/TiN (TLT) and TiLaN (TLN), on HfO₂/Si substrates were investigated focusing on the flat band voltage (VFB) modulation for nMOS and IL scaling to almost zero. The maximum VFB modulation value of the TLT/HfO₂/Si stack was −423 mV compared to the VFB of the TiN single metal case, which is superior to that of TLN (−247 mV). This is because the TiN barrier layer in the TLT metal stack prevents interfacial oxidation. Both TLT and TLN gate metals effectively shrink the IL thickness to values below 0.5 nm. In the case where the TLT metal gate was annealed at 600 °C for 30s, the IL thickness was almost zero and the equivalent oxide thickness (EOT) was decreased to 0.8 nm even though the maximum temperature was limited to 600°C. However, the La-incorporated TiN metal gates can not adopt for pMOS due to their low work function, and another method must be pursued to scale the EOT of p-type MOSFET.

Thirdly, the influences of RuO₂ metal gate on the dielectric performance of high-k HfO₂ film on Si substrate were examined. Dielectric materials with a higher-k value also suffer from a dead-layer effect that the effective dielectric constant decreases with decreasing thickness, which becomes even more serious as the bulk k value increases. The EOT of HfO₂ film can be scaled down by ~ 0.5 nm in the EOT range from 0.8 to 2.5
nm compared with the standard Pt gate case by using the electrically conducting RuO$_2$ without sacrificing any other performance of the MOS capacitor. RuO$_2$ is one of the rare materials, which contain polarizable ions, high electrical conductivity, and high work function (WF) which is necessary for the p-type MOSFET. This was attributed to the suppression of the dielectric dead-layer effect at the HfO$_2$/RuO$_2$ interface due to the possible ionic polarization of RuO$_2$ within the screening length of the electrode. In addition, the estimated work function of RuO$_2$ on HfO$_2$ is $\sim 5.0$ eV suggesting the appropriateness of RuO$_2$ for p-MOSFET.

Finally, RuO$_2$ metal gates were fabricated by a reactive sputtering method under the different O$_2$ gas ratio. For the given sputtering power of 60 W, $\sim 13$ % O$_2$ ratio was the critical level below or over which RuO$_2$ film have hyperstoichiometric and stoichiometric compositions, which resulted in the effective work function difference by $\sim 0.2$ eV. The stoichiometric RuO$_2$ film imposed almost no damaging effect to the underlying SiO$_2$ and HfO$_2$ gate dielectrics. RuO$_2$ gate decreased the equivalent oxide thickness by $\sim 0.5$ nm and leakage current by $\sim$ two orders of magnitude compared with the Pt-gated samples.

**Keywords :** High-$k$ gate dielectrics, Hafnium Oxide, Hafnium silicate, Higher-$k$ dielectrics, Metal gate, Lanthanum metal gate, Ruthenium metal gate, RuO$_2$ metal gate, Scavenging effect, Deadlayer effect.

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# Table of Contents

Abstract .................................................................................................................. i
Table of Contents ..................................................................................................... iv
List of Tables .......................................................................................................... ix
List of Figures ......................................................................................................... x
List of Abbreviations ............................................................................................... xviii

I. Introduction ........................................................................................................... 1
  1.1 Introduction ..................................................................................................... 1
  1.2 Reference ...................................................................................................... 4

II. Literature Review ............................................................................................... 6
  2.1 High-\(k\) dielectrics ...................................................................................... 6
    2.1.1 Introduction of high-\(k\) gate dielectrics ................................................ 6
    2.1.2 Selection of high-\(k\) gate dielectrics .................................................... 11
    2.1.3 Research trend of high-\(k\) gate dielectrics ........................................... 14
    2.1.4 High-\(k\) gate dielectrics on Ge and III-\(V\) substrates ......................... 25
  2.2 Metal gates .................................................................................................... 27
    2.2.1 Introduction of metal gates ................................................................. 27
    2.2.2 Effective work function ...................................................................... 29
      2.2.2.1 Definition of effective work function ............................................ 29
      2.2.2.2 Extraction of effective work function .......................................... 34
    2.2.3 Control of effective work function ...................................................... 37
      2.2.3.1 Selection of metal gate materials ................................................. 37
      2.2.3.2 Interface modulation .................................................................. 39
    2.2.4 Metal gate integration .......................................................................... 43
      2.2.4.1 Gate-first integration ................................................................. 43
2.2.4.2 Gate-last integration

2.3 Issues of high-\textit{k} dielectrics/metal gates

2.3.1 Fermi level pinning effect

2.3.2 Flat band roll off effect

2.3.3 Further EOT scaling

2.3.3.1 Higher-\textit{k} dielectrics

2.3.3.2 Scavenging effect

2.3.3.3 Deadlayer effect

2.4 Reference

III. Experiments and Analyses

3.1 Atomic layer deposition of high-\textit{k} dielectrics

3.2 Sputtering deposition of metal gates

3.3 Film characterization

3.4 Fabrication of MOS capacitor

3.5 Fabrication of terraced oxide substrate

3.6 Extraction of effective work function

3.7 Electrical measurements

IV. Results and Discussions

4.1 ALD grown Hf-silicate (Hf\textsubscript{x}Si\textsubscript{1-x}O\textsubscript{y}) for gate dielectrics

4.1.1 Introduction

4.1.2 Experimental

4.1.3 Growth and physical properties

4.1.3.1 ALD growth of HfSiO

4.1.3.2 Physical properties of HfSiO

4.1.4 Dielectric constant and insulating properties

4.1.5 Conclusion
List of Tables

Table 2.1 Static dielectric constant (k) of the several candidate gate dielectrics.
Table 2.2 Summary of material characteristics of HfO₂ and major doping dielectrics.
Table 2.3 Characteristics of several potential channel materials compared to Si at 300 K.
Table 3.1 Physical and chemical properties of TEMAHf and tri-DMAS.
Table 3.2 Process conditions of thermal ALD grown HfO₂ and SiO₂.
Table 3.3 Process conditions of sputtered various metal films in this work.
Table 4.1 Properties of ruthenium (Ru) and ruthenium oxide (RuO₂).
Table 4.2 Summary of the various parameters extracted from Fig. 4.30 for the different MIS and MIM samples.
**List of Figures**

Figure 2.1 The ITRS roadmap of gate leakage current density on LSTP device (2003).

Figure 2.2 The schematic diagram of the field effect transistor (FET).

Figure 2.3 The schematic diagram of the capacitance equivalent thickness (CET) and equivalent oxide thickness (EOT).

Figure 2.4 Schematic diagram of the band offset values of the several candidate gate dielectrics.

Figure 2.5 Correlation graph between the dielectric constants and the band offset values of the several candidate gate dielectrics.

Figure 2.6 Gibbs free energy for the oxide formation of the several candidate gate dielectrics as a function of temperature.

Figure 2.7 (a) XRD patterns of HfO₂ and Al-doped HfO₂ films with respect to the number of unit cycles in a HfO₂ sub-cycle after PDA [14] (b) XPS spectra of Si 2p of HfO₂ and Al-doped HfO₂ films before and after PDA [15].

Figure 2.8 $k$-value extracted from MIM capacitors as a function of the Si concentration ($x$) and annealing temperature. The characters $a$, $m$, and $t$ denote the film structures as amorphous, monoclinic and tetragonal, respectively [17].

Figure 2.9 The crystallization temperature as a function of Zr compositions in Hf₁₋ₓZrxO₂. (b) GAXRD spectra of Hf₁₋ₓZrxO₂ with various Zr compositions after annealing at 550°C [21].

Figure 2.10 Band diagram of Metal-Oxide-Semiconductor (MOS) capacitor.

Figure 2.11 (a) Ideal and (b) real C-V curves of Metal-Oxide-Semiconductor (MOS) capacitor.

Figure 2.12 Plot of oxide thickness as a function of V FB from CV curves of Metal-Oxide-Semiconductor (MOS) capacitors.

Figure 2.13 (a) A schematic diagram of the stack showing a fixed high-$k$ dielectric material on a varying interfacial SiO₂ layer and (b) $V_{FB}$ versus EOT curve used to extract the EWF [36].
Figure 2.14 Plot of (a) vacuum work functions of various metal materials for gate metal [38] and effective work function on SiO₂ versus bulk work function reported in literature [39].

Figure 2.15 Interface dipole moment model. EWF shift is proportional to dipole moment due to the charge transfer in the Hf-O-RE(rare earth) configuration [42].

Figure 2.16 Metal/high-\(k\) dielectric interface modulation model using cladding layer on gate [43].

Figure 2.17 Schematics depicting a cross-section of typical gate-first integrated (a) nMOS and (b) pMOS devices, and TEM images of Globalfoundries’ gate-first integrated (c) nMOS and (d) pMOS at 32nm technology node [47].

Figure 2.18 Schematics depicting a cross-section of typical gate-last integrated (a) nMOS and (b) pMOS in replacement-gate process, and TEM images of Intel’s gate-last integrated pMOS at (c) 45nm and (d) 32nm technology node [47].

Figure 2.19 Band diagram depicting a Fermi level pinning (FLP) of metal/high-\(k\)/Si stack. Fermi level (EF) of metal tends to shift toward near the midgap of Si after annealing.

Figure 2.20 Dependence of \(V_{FB}\) on EOT in high-\(k\) terraced-oxide capacitors with metal electrodes of different WF values. Each trend line corresponds to a specific metal electrode.

Figure 2.21 Roll-off suppressions by (a) low-temperature oxygen annealing and (b) incorporating fluorine into the interfacial SiO₂ layer. (Inset) CV characteristics of the capacitor stacks with F-doped IL and control [53].

Figure 2.22 EOT of SiO₂/HfO₂ metal-inserted poly-Si stack (MIPS) structure as a function of \(\Delta G^0_{1000}\) per oxygen atom for scavenging element. TiN electrodes doped with various metals are compared with literature data [54,57].

Figure 2.23 Schematics of direct- and remote-scavenging techniques [54].

Figure 2.24 (a) Effective series capacitance structure formed from ferroelectric material plus its two surface dead layers, illustrating metal/dielectric/metal structure and (b) schematic behavior of \(\varepsilon_{eff}\) as a function of film thickness [58].
Figure 2.25 Comparison of the potential profiles inside the SRO/STO/SRO capacitor system. Black curve is obtained by Stengel and Spaldin using \textit{ab initio} techniques. Red curve is the potential expected from classical electrostatics. [59].

Figure 3.1 Schematic diagram of the thermal ALD system used in these experiments.

Figure 3.2 The sputtering system with 5-angle cluster module; (a) schematic diagram of sputtering equipments and (b) enhanced magnetic field structure of cathode (right) compared to the general type (left) and (c) schematic diagram of magnetic-field in quarter cathode system.

Figure 3.3 Schematic diagram of (a) a shadow mask used in this work and (b) Pt electrode on the dielectrics and (c) other metal insertion between Pt and dielectrics on Si substrate and (d) scope image of a dot.

Figure 3.4 Schematic diagram of preparing terraced oxide substrate and final sample structure; (a) sample wet-etching and (b) vertical diagram and (c) measured thermal SiO$_2$ thicknesses of several samples after wet-etching and (d) final sample diagram after metal electrode deposition.

Figure 3.5 (a) C-V curves measured from a terraced oxide sample and (b) flat band voltage ($V_{FB}$) versus EOT plot of Pt electrode from only terraced SiO$_2$ sample and terraced SiO$_2$/HfO$_2$ stack sample.

Figure 3.6 BTI and $D_{it}$ measurement system in these experiments.

Figure 3.7 Schematic diagram of BTI and $D_{it}$ measurement in MOS capacitor devices.

Figure 4.1 Plots of thickness and growth rate as a function of cycle and schematic diagrams of cycle of (a) HfO$_2$ and (b) SiO$_2$.

Figure 4.2 (a) Schematic diagram of ALD super-cycle of HfSiO film consisting of HfO$_2$ and SiO$_2$ sub-cycle and (b) sample preparation condition in this work.

Figure 4.3 The growth rate and thickness as a function of a super-cycle of HfSiO film with Si:Hf feeding ratio of (a) 3:1, (b) 1:1, (c) 1:3, and (d) 1:7.

Figure 4.4 Correlation graphs (a) between calculated growth rate and real growth rate of super cycles and (b) between the source feeding ratio, calculated by sub-cycle
feeding number, and the atomic ratio, estimated from XPS peak area ratio of Hf 4f and Si 2p.

Figure 4.5 (a) Hf 4f and (b) Si 2p core level XPS spectra for HfSiO films with Si:Hf ratio of 1:7 (Si 16%) to 3:1 (Si 81%), including ALD grown HfO2 and SiO2.

Figure 4.6 (a) Hf 4f and (b) Si 2p core level XPS spectra for HfSiO films with Si:Hf ratio of 1:7 (Si 16%) after PDA (800°C and 1000°C) including as-deposited HfO2.

Figure 4.7 AES depth profiles of as-deposited HfSiO films with Si:Hf ratio of (a) 1:7 (Si 16%), (b) 1:5 (Si 20%), (c) 1:3 (Si 33%), and (d) 1:1 (Si 57%). Film thicknesses are almost 15nm.

Figure 4.8 XRD spectra of HfSiO films with Si:Hf ratio of 1:9 (Si 14%) to 3:1 (Si 81%) including SiO2 and HfO2 films as a function of PDA temperature from 400°C to 1000°C. Film thicknesses are almost 15nm.

Figure 4.9 (a) The permittivity of as-deposited HfSiO films as a function of Si concentrations and (b) the inverse slope of the EOT vs. physical thickness for as-deposited HfSiO film with Si 16%, 57%, and 80% including HfO2. The dielectric constants are extracted from 3.9 divided by slope.

Figure 4.10 (a) The permittivity changing as a function of PDA temperatures for HfO2 and HfSiO films with Hf:Si ratio of 1:1 (Si 57%) and 1:7 (Si 16%). For the evaluation of permittivity, (b) the inverse slope of the CET vs. physical thickness for HfSiO film with Si 16% before and after PDA (800°C), and TEM images and FFT pattern of HfO2 before and after PDA (700°C).

Figure 4.11 TEM micrographs and FFT patterns of about 7-nm-thick HfSiOx films with Si concentration of 16% after PDA at (a) 800°C and (b) 1000°C for 30 s in N2 atmosphere and (c) the phase ratio of both films analyzed from randomly selected 30 points by FFT and (d) EELS mapping image of Si of the film after 1000°C for 30 s in N2 atmosphere.

Figure 4.12 (a) XRD patterns of HfSiOx films with Si concentration of 57% after PDA from 400 to 1000°C for 30 s under N2, (b) TEM micrographs and (inset) FFT patterns, and (c) the phase ratio of the film after PDA 1000°C for 30 s.
Figure 4.13 Plot of CET vs. J_g for (a) as-deposited HfO_2 and HfSiO_x films with various Si concentrations, and annealed HfO_2 and HfSiO_x films with a Si concentration of 16 and 57% at (b) 800°C, (c) 900°C, and (d) 1000°C 30 s (Simulation result for HfO_2 is indicated by a dashed line).

Figure 4.14 (a) Plot of the resistivity and deposition rate of Pt films as a function of Pt target power and (b) C-V curves under various deposition conditions and (c) dc plasma current vs. voltage correlation with various process pressures and (d) final Pt deposition condition.

Figure 4.15 (a) The resistivity of TiN films as a function of (a) process pressure and (b) N2 flow rate and (inset) target power, and the C-V curves of TiN/SiO_2/Si capacitors with various TiN thicknesses and EWF of TiN films as a function of TiN thickness, extracted from thermal SiO_2 with various thicknesses.

Figure 4.16 (a) TEM images of no metal, TiN, Ti and La metal layers on HfO_2 and (b) schematic diagram of scavenging effect of metal/HfO_2/Si stack and (c) plot of interfacial layer (IL) thicknesses from TEM images and Gibbs free energies of each metal layers.

Figure 4.17 Schematic diagrams of MOS capacitors with (a) bottom and (b) top sites of La metal layer with various thicknesses on HfO_2 and C-V plots as a function of each (c) bottom and (d) top La layers.

Figure 4.18 Schematic diagrams of MOS capacitors with (a) TiN/La/TiN (TLT) and (b) TiLaN (TLN) metal gates on HfO_2 and the AES profiles of as-deposited and PDA (600°C), (a) TLT(~5/5/5nm)/ HfO_2/Si and (b) TLN(~25nm)/HfO_2/Si gate stacks.

Figure 4.19 The summary of V_FB shift amounts of the MIS capacitors with TLT of varying bottom TiN thicknesses and TLN of varying La concentrations, extracted from (inset) each of the C-V curves.

Figure 4.20 Illustration of bi-metal stack structure. (a) Fermi level (E_f) shift in thin metal-l layer and (b) no E_f shift in thick metal-l layer, showing that electrons in the metal-2 flow into the metal-1 electrode in relative band structure.
Figure 4.21 Plot of $V_{FB}$ vs. EOT of Pt, TiN and TLT gates using (a) terraced SiO$_2$ and (b) HfO$_2$-terraced SiO$_2$ oxide for extraction of EWF for various metal gates (Pt, TiN 20nm/Pt, TLT (3/5/3nm /Pt)).

Figure 4.22 Plot of EOT as a function of HfO$_2$ thickness for extraction of IL thicknesses for various metal gates. And summary of IL thicknesses for various metal gates (Pt, TiN20nm/Pt, TLN(42% La, 15 nm)/Pt, TLT (3/5/3nm /Pt).

Figure 4.23 HRTEM images of (a) as-deposited TLT(10/5/10nm) and (b) PDA TLT (3/5/3nm) on HfO$_2$ (3–4nm)/Si gate stacks capped by Si. (c) $J_g$–EOT graphs of various samples (Pt, TiN20nm/Pt, TLN(42% La, 15 nm)/Pt, TLT3/5/3nm/Pt).

Figure 4.24 CV curves of TLT and TTT including Pt and TiN on HfO$_2$/Si stacks at (a) as-deposition and (b) after PDA. And plot of EOT as a function of HfO$_2$ thickness for extraction of IL thicknesses and summary of IL thicknesses for TLT and TTT with references of Pt and TiN.

Figure 4.25 La 3$d$ regions of XPS spectra for (a) TLT(5/5/5nm)/HfO$_2$/Si and (b)TLN (~15nm) with 42% La/HfO$_2$/Si gate stacks capped by the poly-Si (~30nm).

Figure 4.26 Ti 2$p$ regions of XPS spectra for (a) TLT(5/5/5nm)/HfO$_2$/Si and (b)TLN (~15nm) with 42% La/HfO$_2$/Si gate stacks capped by the poly-Si (~30nm).

Figure 4.27 Dit characteristics of TLT and TLN metal gates including Pt and TiN single metal gates on HfO$_2$/Si, evaluated by the conductance method. (a) Plot of $D_{it}$ as a function of gate voltage (or energy state) and (b) summary of $D_{it}$ in TLT and TLT as a function of La power at the midgap of Si band gap.

Figure 4.28 Plots of EOT as a function of HfSiO film (with (a) several Si compositions and (c) 800°C annealed film of 16% Si) thickness including HfO$_2$ film for extraction of IL thicknesses and dielectric constant (k), and (b) EOT IL reduction and k-value drop amounts via remote-scavenging from TLT electrodes as a function of Si composition in HfSiO compared to that of Pt. And (d) the C-V curves of several gate stacks.

Figure 4.29 (a) Ru 3$d$ and (b) O 1$s$ regions of the XPS spectra for Ru (10 nm) and RuO$_2$ (30 nm) on SiO$_2$/Si.
Figure 4.30 Variation of EOT as a function of HfO$_2$ oxide thickness with various electrodes in (a) MIS (Metal electrodes/HfO$_2$/Si) and (b) MIM (Metal electrodes/HfO$_2$/Pt). ( Insets are CV curves (a) before and after FGA in MIS and (b) of as-deposited MIM)

Figure 4.31 Schematic diagrams of dipolar polarization in HfO$_2$ dielectrics in (a) MIS (Metal electrodes/HfO$_2$/Si) and (b) MIM (Metal electrodes/HfO$_2$/Pt). RuO$_2$ electrode eliminated the intrinsic dead-layer due to conducting oxide property.

Figure 4.32 HRTEM images of the interfacial layers between Si and HfO$_2$ with (a) as-deposited Ru, (b) RuO$_2$, (c) Pt and (d) TiN electrodes. And the images of thin (~2nm) (e) Ru and (f) RuO$_2$ layers on SiO$_2$.

Figure 4.33 Variations of Hf layer density for a given HfO$_2$ thickness and Ru (and Ti) layer densities as a function of sputtering time of Ru, RuO$_2$, and TiN electrodes.

Figure 4.34 Plots of $V_{FB}$ vs. CET for various electrodes using (a) terraced SiO$_2$ and (d) HfO$_2$/terraced SiO$_2$ oxide, and C-V curves of (b) 6nm-thick SiO$_2$ and (d) 3.3nm-thick HfO$_2$ films with different electrodes.

Figure 4.35 Plot of (a) EOT vs. $J_g$ of MIS with Pt, thin RuO$_2$(2nm)/Pt and thick RuO$_2$ electrodes on HfO$_2$/Si stack and (b) $J_g$ as a function of gate voltage of MIM with Pt, thin RuO$_2$(2nm)/Pt and thick RuO$_2$ electrodes on HfO$_2$/Pt stack.

Figure 4.36 Variations of (a) Ru layer density of RuO$_2$ films at 30 and 60 W as a function of O$_2$ ratio and (inset) Hf layer density for a given HfO$_2$ thickness and Ru layer density as a function of deposition time of RuO$_2$ electrodes, and (b) GAXRD spectra of as-deposited Ru (~10 nm) and RuO$_2$ (~30 nm) with various O$_2$ ratios and (inset) the variations in the grain size of the films estimated from the two XRD peaks using the Scherrer equation.

Figure 4.37 (a) Ru 3$d$ and (b) O 1$s$ regions of the XPS spectra for Ru (10 nm) and RuO$_2$ (30 nm) with various O$_2$/($Ar$+$O_2$) ratio on SiO$_2$/Si and AES profiles of as-deposited RuO$_2$ films with (c) 10.4% O$_2$ and (d) 14.3% O$_2$ ratios on SiO$_2$/Si.
Figure 4.38 Cross-section TEM (a, b) and plan-view SEM (c, d) images of RuO$_2$ films with O$_2$ ratios of (a, c) 10.4 % and (b, d) 14.3 % on SiO$_2$/Si.

Figure 4.39 Plot of $V_{FB}$ vs. CET for various electrodes using terraced SiO$_2$ and HfO$_2$/terraced SiO$_2$ oxide, and (b) variation of EOT as a function of HfO$_2$ oxide thickness and (inset) plot of $J_g$ vs. EOT with various electrodes on HfO$_2$/Si.

Figure 4.40 (a) Variation of EOT as a function of SiO$_2$ and HfO$_2$ and HfSiO oxide thickness with Pt and RuO$_2$ (10.4% O$_2$) electrodes in MIS and (b) summary of the variation plot of EOT vs. thickness.
### List of Abbreviations

- **AES**: Auger electron spectroscopy
- **AFM**: Atomic force microscope
- **ALD**: Atomic layer deposition
- **CBO**: Conduction band offset
- **CET**: Capacitance equivalent oxide thickness
- **CMOS**: Complementary metal oxide semiconductor
- **CVD**: Chemical vapor deposition
- **C-V curve**: Capacitance – voltage curve
- **DI water**: Deionized water
- **Dit**: Interface trap charge
- **DRAM**: Dynamic random access memory
- **EOT**: Equivalent oxide thickness
- **$E_{\text{ext}}$**: External electric field
- **$E_{\text{dep}}$**: Depolarizing field
- **$E_{\text{ox}}$**: Electric field
- **$E_g(\text{oxide})$**: Bandgap of the oxide
- **$E_g(\text{Si})$**: Bandgap of the Si substrate
- **EWF**: Effective Work Function
- **GAXRD**: Glancing angle incidence X-ray diffraction
- **HF**: Hydrofluoric acid
- **HRTEM**: High resolution transmission electron microscopy
- **HP 4155**: Hewlett-Packard 4155
- **HP 4194A**: Hewlett-Packard Impedance/Gain-Phase Analyzer 4194A
- **Icp**: Charge pumping current
- **IL**: Interfacial Layer
- **$J_g$**: Leakage current density
- **$J_g$ –V curves**: Leakage current density – voltage curve
<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>k value</td>
<td>Dielectric constant value</td>
</tr>
<tr>
<td>MOSFET</td>
<td>Metal oxide semiconductor field effect transistor</td>
</tr>
<tr>
<td>MOSCAP</td>
<td>Metal oxide semiconductor capacitor</td>
</tr>
<tr>
<td>MIS</td>
<td>Metal insulator semiconductor capacitor</td>
</tr>
<tr>
<td>MIM</td>
<td>Metal insulator metal capacitor</td>
</tr>
<tr>
<td>NBTI</td>
<td>Negative bias temperature instability</td>
</tr>
<tr>
<td>PBTI</td>
<td>Positive bias temperature instability</td>
</tr>
<tr>
<td>PDA</td>
<td>Post deposition annealing</td>
</tr>
<tr>
<td>Poly-Si</td>
<td>Polycrystalline Silicon</td>
</tr>
<tr>
<td>PEALD</td>
<td>Plasma-enhanced atomic layer deposition</td>
</tr>
<tr>
<td>RTA</td>
<td>Rapid thermal annealing</td>
</tr>
<tr>
<td>SEM</td>
<td>Scanning electron microscope</td>
</tr>
<tr>
<td>tphy</td>
<td>physical thickness</td>
</tr>
<tr>
<td>TEM</td>
<td>Transmission electron microscopy</td>
</tr>
<tr>
<td>TEMAH</td>
<td>Tretrakis-Ethyl-Methyl-Amino-Hafnium</td>
</tr>
<tr>
<td>TMA</td>
<td>Tri-Methyl-Aluminum</td>
</tr>
<tr>
<td>VBO</td>
<td>Valence band offset</td>
</tr>
<tr>
<td>V_FBB</td>
<td>Flat band voltage</td>
</tr>
<tr>
<td>V_g</td>
<td>Gate voltage</td>
</tr>
<tr>
<td>V_th</td>
<td>Threshold voltage</td>
</tr>
<tr>
<td>XPS</td>
<td>X-ray photoelectron spectroscopy</td>
</tr>
<tr>
<td>XRD</td>
<td>X-ray Diffraction</td>
</tr>
</tbody>
</table>
I. Introduction

1.1 Introduction

The number of transistors on integrated circuits has doubled approximately every two years (generally 18 months) according to Moore’s Law. In other words, the minimum feature size of complementary metal oxide semiconductor field effect transistors (CMOSFETs) has decreased exponentially until now. Because the capabilities of many digital electronic devices are strongly influenced by their chip performance, which has been mainly dominated by transistor channel length of CMOSFETs. One of the key methods to enable transistor channel length scaling in CMOSFETs is to scale the gate dielectrics. However, with this method, scaling slows down at the 90 nm node as SiO$_2$ runs out of atoms and further scaling is limited due to the increase of gate-leakage current [1]. To continue the scaling of transistors, various high-$k$ oxide materials have been studied intensively for the past few decades, especially since 2000. Finally, to decrease the gate leakage in highly scaled transistors, Hf and Zr-based high-$k$ gate dielectrics have been considered to be the most promising candidates to replace SiO$_2$ gate dielectrics [2–4]. Especially, Hf-based high-$k$ gate dielectrics have already been employed in the current technology node, where several companies such as Intel and Samsung have used high-$k$ gate dielectrics below 45 nm technology node [5]. However, the use of the high-$k$ gate dielectrics do not cleared all the problems involved in the scaling of transistors for improving the performance. As a requirement to meet high performance continuously increases, Hf-based high-$k$ gate dielectrics will be faced with a limit to the scaling of
physical thickness like SiO$_2$ gate dielectrics in the near future. For the occasion to encounter the limit of the scaling, various studies on high-$k$ materials such as higher-$k$ gate dielectrics and interfacial layer scaling need to be investigated very intensively.

Integration of the high-$k$ gate dielectrics with a poly-Si gate electrode into the existing process flow has encountered several key issues. Adoption of metal gates in CMOSFETs with a high-$k$ gate dielectric is indispensable to overcome the issues of poly-Si gates, such as gate depletion [6], boron penetration, and high gate resistance [3], involving interaction between the poly-Si electrode and the high-$k$ dielectrics. However, even though various metal materials were used instead of the poly-Si electrode, there are still several crucial problems that need to be considered; an effective work function (EWF) modulation for adjusting the threshold voltage ($V_t$) of transistors, which is difficult because doping gate metals is impossible unlike poly-Si gates.

Recently, two basic approaches were introduced for the integration of gate stacks using high-$k$ gate dielectrics and a metal gate electrode: a gate-first approach [7] and a gate-last approach [8]. In the gate-first approach, the high-$k$ gate dielectrics as well as metal gate electrodes need to have high thermal stability, because of the formation of the gate stack before activation annealing of the source and drain, as in a conventional CMOSFET process. Recent research to modulate the $V_t$ of gate electrodes has focused on applying a capping layer such as La$_2$O$_3$ for n-MOS and Al$_2$O$_3$ for p-MOS, between the high-$k$ dielectric and gate metal, which helps to form interfacial dipoles to modulate the flat band voltage ($V_{FB}$) after high thermal budget [9,10]. However, this approach has introduced several unintended issues such as the increase of equivalent oxide thickness (EOT) as well as EWF due to high thermal budget, mobility reduction, and increase of interface-
state density \( (D_n) \) [11]. In case of the gate-last approach, the high-\( k \) gate dielectrics as well as metal gate electrodes can be integrated widely without limit of materials, because of the formation of the gate stack after activation annealing of the source and drain. Therefore, recent research to integrate the metal gates on high-\( k \) dielectrics below 28nm technology node has based on the gate-last approach.

In this study, correlation between micro structure and dielectric constant of atomic layer deposited Si-doped HfO\(_2\) gate dielectrics was firstly investigated. And plausible \( V_{FB} \) modulation as well as interfacial layer scavenging effect by Lathanium (La) was accomplished by using physical vapor deposition. Also, physical and electrical properties of Ru-based gate electrodes such as Ru and RuO\(_2\) films were studied for EOT scaling of p-MOS transistor.
1.2 Reference


II. Literature review

2.1 High-\textit{k} gate dielectrics

2.1.1 Introduction of high-\textit{k} gate dielectrics

Silicon has been a main material of the semiconductor industry over the past several decades. Also, the most important electronic device is the complementary metal oxide semiconductor field effect transistors (CMOSFETs) made from silicon. One of the key elements that allowed the successful scaling of silicon based CMOSFETs is certainly SiO$_2$, which has physical and electrical excellent properties as the gate dielectrics. SiO$_2$ gate dielectrics indeed have several important features that have allowed its use as gate insulator; 1) Amorphous SiO$_2$ can be thermally grown on Si with excellent control in thickness and uniformity, and naturally forms a very stable interface with the Si substrate, with a low density of intrinsic interface defects, with presenting excellent thermal and chemical stability, which can easily integrate the CMOSFETs due to high immunity to endure high temperature annealing over 1100℃. 2) SiO$_2$ has quite large bandgap (~ 9eV), which results in the excellent electrical isolation properties, such as its large band offset with the conduction band (CB~3.5eV) and valence band (VB~4.4eV) of Si.

The thickness of the SiO$_2$ layer presently used as the gate dielectric is so thin (under 1.3nm at 90nm technology node) that the gate leakage current becomes too high due to direct tunneling of electrons through the SiO$_2$. The simulated gate leakage current was expected to exceed the leakage limit on gate leakage current density, as shown in Fig. 2.1, so that high-\textit{k} gate dielectrics became to need to replace SiO$_2$ as a gate oxide by 2006.
This expectation was realized in 2007 when Intel announced the use of Hf-based high-$k$ gate dielectrics in 45nm technology node.

Direct tunneling current through gate oxide decreases exponentially with increasing gate oxide thickness. A CMOSFETs is a capacitance-operated device, where the source-drain current ($I_{on}$) of the FET depends on the gate capacitance (Fig. 2.2)

![Figure 2.1 The ITRS roadmap of gate leakage current density on LSTP device (2003)](image-url)
Figure 2.2 The schematic diagram of the field effect transistor (FET)

\[ I_{on} = \frac{\mu_{eff} C_{ox,inv} W}{2} \frac{W}{L} (V_{gs} - V_{th})^2 \]  \hspace{1cm} (1)

where \( I_{on} \) is the source-drain current of FET, \( \mu_{eff} \) is the effective mobility of carrier, \( C_{ox} \) is the gate capacitance, \( W \) and \( L \) are the width and length of transistor and \( V_{gs} \) and \( V_{th} \) are the operating and threshold voltages of transistor. Hence, \( I_{on} \) depends on \( C_{ox,inv} \).

\[ C_{ox,inv} = \frac{kE_0 A}{t} \]  \hspace{1cm} (2)
where $\varepsilon_0$ is the permittivity of free space, $k$ is the relative permittivity (or dielectric constant), $A$ is the area and $t$ is the oxide thickness. Hence, the solution to the direct tunneling problem is to replace SiO$_2$ with a physically thicker new material of higher permittivity ($k$) [1]. This approach keeps the same capacitance or increases the gate capacitance but decreases the gate leakage current. The larger the permittivity of high-$k$ dielectrics becomes, the more the gate leakage current can be decreased. These new gate oxides with high permittivity are called high-$k$ dielectrics. Also, it is convenient to define an electrical thickness of the new gate oxide in terms of its equivalent SiO$_2$ thickness, or “equivalent oxide thickness” (EOT) as

$$EOT = \frac{3.9\varepsilon_0}{k} t_{high-k} = \frac{3.9}{k} t_{high-k}$$  \hspace{1cm} (3)

where 3.9 is the static dielectric constant of SiO$_2$ and $t_{high-k}$ is the physical thickness of high-$k$ oxide. Hence, the most important point is to develop high-$k$ dielectrics which allow scaling to continue to ever lower values of EOT.

In this study, another term of EOT, or “capacitance equivalent thickness” (CET) is often used because it can be extracted easily from capacitance values of high-$k$ dielectrics. CET is as

$$CET = \frac{3.9\varepsilon_0 A}{C_m}$$  \hspace{1cm} (4)
where $C_m$ is the maximum capacitance value under accumulation condition of carrier and $A$ is the area of capacitance. Also, CET is the sum of EOT and any quantum mechanical (QM) effects (0.3~0.4nm), which means EOT equals CET minus 0.3~0.4 nm as shown in Fig. 2.3.

![Figure 2.3 The schematic diagram of the capacitance equivalent thickness (CET) and equivalent oxide thickness (EOT)](image)
2.1.2 Selection of high-\(k\) gate dielectrics

As mentioned above, the solution to the direct tunneling problem is to replace the SiO\(_2\) layer with a physically thicker layer of new material of higher dielectric constant (\(k\)). These new gate oxides are called high-\(k\) gate dielectrics, which are chosen from a large part of the Periodic Table.

The new high-\(k\) gate dielectrics have to meet several requirements as follows [1]:
1. Its \(k\) value must be high enough to be used for a reasonable number of years of scaling.
2. The oxide is in direct contact with the Si channel, so it must be thermodynamically stable with it.
3. It must be kinetically stable and be compatible to processing to 1000 °C for 5 s (in present gate first process flows).
4. It must act as an insulator, by having band offsets with Si of over 1 eV to minimize carrier injection into its bands.
5. It must form a good electrical interface with Si.
6. It must have few bulk electrically active defects.

Among these requirements, several important factors are so critical that they have to be fully understood before adopting the high-\(k\) materials in CMOS applications.

Firstly, the relative dielectric constant of the new materials should be somewhere between 12 and 30. There is a trade off with the band offset condition, which requires a reasonably large band gap. The band offset between the gate oxide and Si defines the potential barrier for Schottky injection of electrons or holes into the oxide bands. The potential barrier at each band must be over 1 eV in order to give an adequately low gate leakage current [2, 3]. Table 2.1 and Fig. 2.4 show static dielectric constants and band
offset values, respectively, of the several candidate gate dielectrics, calculated by Robertson [2]. Conduction band offset (CBO) of most high-\textit{k} dielectrics tends to be the smaller than valence band offset (VBO), which means the CBO is one of the key criteria for selecting the new high-\textit{k} dielectrics. Also, the correlation graph between the dielectric constants and the CBO values of the several candidate gate dielectrics is shown in Fig. 2.5. There is an inverse relationship between dielectric constant and band gap, or band offset. In the graph, there are several oxides with large dielectric constants, such as TiO\textsubscript{2} and SrTiO\textsubscript{3}, which are candidates for dielectrics in DRAM capacitors [4], but these oxides have a too low CBO as well as low band gap to select the gate oxides.

<table>
<thead>
<tr>
<th>Material</th>
<th>Dielectric constant ($\kappa$)</th>
<th>Band gap ($E_g$ eV)</th>
<th>$\Delta E_C$ (eV) to Si</th>
<th>Crystal structure(s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiO\textsubscript{2}</td>
<td>3.9</td>
<td>8.9</td>
<td>3.2</td>
<td>Amorphous</td>
</tr>
<tr>
<td>Si\textsubscript{3}N\textsubscript{4}</td>
<td>7</td>
<td>5.1</td>
<td>2</td>
<td>Amorphous</td>
</tr>
<tr>
<td>Al\textsubscript{2}O\textsubscript{3}</td>
<td>9</td>
<td>8.7</td>
<td>2.8\textsuperscript{a}</td>
<td>Amorphous</td>
</tr>
<tr>
<td>Y\textsubscript{2}O\textsubscript{3}</td>
<td>15</td>
<td>5.6</td>
<td>2.3\textsuperscript{a}</td>
<td>Cubic</td>
</tr>
<tr>
<td>La\textsubscript{2}O\textsubscript{3}</td>
<td>30</td>
<td>4.3</td>
<td>2.3\textsuperscript{a}</td>
<td>Hexagonal, cubic</td>
</tr>
<tr>
<td>Ta\textsubscript{2}O\textsubscript{5}</td>
<td>26</td>
<td>4.5</td>
<td>1.5\textsuperscript{b}</td>
<td>Orthorhombic</td>
</tr>
<tr>
<td>TiO\textsubscript{2}</td>
<td>80</td>
<td>3.5</td>
<td>1.2</td>
<td>Tetrag.\textsuperscript{c} (rutile, anatase)</td>
</tr>
<tr>
<td>HfO\textsubscript{2}</td>
<td>25</td>
<td>5.7</td>
<td>1.5\textsuperscript{a}</td>
<td>Mono\textsuperscript{b}, tetrag.\textsuperscript{e}, cubic</td>
</tr>
<tr>
<td>ZrO\textsubscript{2}</td>
<td>25</td>
<td>7.8</td>
<td>1.4\textsuperscript{a}</td>
<td>Mono\textsuperscript{b}, tetrag.\textsuperscript{e}, cubic</td>
</tr>
</tbody>
</table>

Table 2.1 Static dielectric constant ($\kappa$) of the several candidate gate dielectrics
Figure 2.4 Schematic diagram of the band offset values of the several candidate gate dielectrics compared to that of SiO₂

Figure 2.5 Correlation graph between the dielectric constants and the conduction band offset values of the several candidate gate dielectrics
Secondly, the high-\(k\) dielectrics to use the gate oxide need to have thermodynamic stability. The high-\(k\) oxides must not react with Si substrate to form either SiO\(_2\) or a silicide according to the unbalanced reactions (\(\text{MO}_2 + \text{Si} = \text{M} + \text{SiO}_2\) or \(\text{MO}_2 + 2\text{Si} = \text{MSi} + \text{SiO}_2\)). The formation of SiO\(_2\) or unpretended silicide between the oxides and Si would increase the EOT. Therefore, the high-\(k\) dielectrics should have a large Gibbs free energy of formation to prevent the reactions. Figure 2.6 show Gibbs free energy as a function of temperature for the oxide formation of the several candidate gate dielectrics [5]. Although SiO\(_2\) have very high thermodynamic stability, there are various high-\(k\) dielectrics to have higher formation energy than SiO\(_2\), which indicates that the higher formation energy of several high-\(k\) dielectrics suppresses the unbalanced reaction. Moreover, oxygen diffusion coefficients must be low because they will cause uncontrolled interfacial layer regrowth.

Finally, the high-\(k\) dielectrics must form a good electrical interface with Si, because the oxides are in direct contact with the Si channel. The carriers in the channel flow within angstroms of the interface between the oxide and Si. Hence, this interface must be of the highest electrical quality. In other word, low interface trap defect density, \(D_{it}\), typically less than \(10^{11} \text{ cm}^{-1}\text{eV}^{-1}\) is required.

To satisfy these various requirements for selecting new high-\(k\) dielectrics, various kinds of high-\(k\) gate dielectrics such as \(\text{Al}_2\text{O}_3\), \(\text{Ta}_2\text{O}_3\), \(\text{ZrO}_2\), \(\text{HfO}_2\), \(\text{TiO}_2\), \(\text{La}_2\text{O}_3\), and many others have been widely investigated for the past decade. \(\text{Ta}_2\text{O}_3\), \(\text{TiO}_2\) and \(\text{Al}_2\text{O}_3\) as new gate dielectrics had been studied in the early days due to their maturity in memory capacitor applications. However, these materials except \(\text{Al}_2\text{O}_3\) are not thermodynamically stable in direct contact with Si. In addition, \(\text{TiO}_2\) and \(\text{Ta}_2\text{O}_3\) have a relatively low conduction band offset with silicon, which can lead to increase electron tunneling currents [2]. In the case
of Al₂O₃, its dielectric constant (~9) was not enough to satisfy the requirement of high-\(k\) gate dielectrics although it has superior thermodynamic and kinetic stability. Considering proper dielectric constant and large band gap and high thermochemical stability, Hf and Zr-based high-\(k\) dielectrics including their silicates must have been the leading candidates.

Figure 2.6 Gibbs free energy for the oxide formation of the several candidate gate dielectrics as a function of temperature [5].
2.1.3 Research trend of high-\(k\) gate dielectrics

Recently, Hf-based high-\(k\) gate dielectrics with a metal gate have been implemented in a mass production by Intel [6]. However, in case of Zr-based high-\(k\) dielectrics similar with Hf-based oxide, they were not selected due to lack of compatibility with other materials used in MOSFET processing. Indeed, the dielectrics were shown to exhibit serious interaction with the poly-silicon gate electrodes [7, 8]. Although there was the serious interaction with the poly-silicon in Zr-based high-\(k\) dielectrics, the dielectrics are still attractive candidate as a gate oxide due to the replacement of poly-silicon gate electrode with the metal gate. Besides Hf and Zr-based high-\(k\) dielectrics, various lanthanide oxides such as La\(_2\)O\(_3\) and Gd\(_2\)O\(_3\) that satisfy several criterions are being consistently studied due to relative large dielectric constant and very high thermodynamic stability.

Above all, the main method for improving physical and electrical characteristics of Hf-based high-\(k\) dielectrics is based on the doping or mixing of another material such as Al\(_2\)O\(_3\), SiO\(_2\), and ZrO\(_2\) into the conventional binary oxide (HfO\(_2\)). Several papers have reported that the doping with Al\(_2\)O\(_3\), SiO\(_2\), and ZrO\(_2\), etc. increased the dielectric constant of HfO\(_2\) due to the phase transformation from monoclinic (~17) to tetragonal or cubic structure with a higher permittivity (~30-40) [9-12]. On the other hand, the doping of Al\(_2\)O\(_3\) and SiO\(_2\) with very high crystallization temperature can help high-\(k\) gate oxide to obtain the reduced gate leakage because these doping oxides may suppress the formation of grain boundaries which act as a path for leakage current. Table 2.2 summarized the material characteristics of HfO\(_2\) and major doping dielectrics. The properties of each dopant such as Al\(_2\)O\(_3\), SiO\(_2\), and ZrO\(_2\) be discussed and summarized briefly.
<table>
<thead>
<tr>
<th>Compound</th>
<th>HfO₂</th>
<th>Hf₁₋ₓAlₓOᵧ</th>
<th>Hf₁₋ₓSiₓOᵧ</th>
<th>Hf₁₋ₓZrₓOᵧ</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dielectric constant (k)</td>
<td>~17 (amor./mono.)</td>
<td>9 (amor.)</td>
<td>3.9 (amor.)</td>
<td>~35 (tetra.)</td>
</tr>
<tr>
<td>Band offset (eV)</td>
<td>CB : 1.5 VB : 3.4</td>
<td>CB : 2.8 VB : 4.9</td>
<td>CB : 3.5 VB : 4.4</td>
<td>CB : 1.4 VB : 3.3</td>
</tr>
<tr>
<td>Band gap (eV)</td>
<td>6.0</td>
<td>8.8</td>
<td>9.0</td>
<td>5.8</td>
</tr>
</tbody>
</table>

Table 2.2 Summary of material characteristics of HfO₂ and major doping dielectrics.
Firstly, Al-doped HfO₂ is discussed.

Al₂O₃ oxide is frequently used to improve the thermal stability of high-$k$ HfO₂ dielectrics as well as to suppress the crystallization of the high-$k$ films and the Si out-diffusion into the high-$k$ film after PDA at a high temperature [13]. Especially, the Si-diffusion from Si substrate into HfO₂ would degrade dielectric properties such as dielectric constant and leakage current. The suppression of Si-diffusion can be understood from basic thermodynamic considerations; the mixing enthalpy and entropy term of the Al-doped HfO₂ stabilizes the high-$k$ layer so that the driving force for Si-diffusion decreases. Several studies reported the enhanced thermal stability as well as the Si-diffusion suppression of Al-doped HfO₂ films due to Al₂O₃ was confirmed by XRD and XPS analyses [14, 15]. Figure 2.7 (a) shows the XRD patterns of HfO₂ and Hf₁ₓAlₓO₂ films with various cycle ratios in the Al-doped HfO₂ (1 : number of HfO₂ cycles) after PDA [14]. While the monoclinic phase was only observed in the pure HfO₂ film, the peaks corresponding to the tetragonal phases appeared in the Hf₁ₓAlₓO₂ films as the Al-concentration increases. The tetragonal phase transformation due to the Al-doping could increase the dielectric constant of HfO₂, because the lower permittivity of Al₂O₃ (~9) could be a critical draw-back increasing the EOT of high-$k$ films. Also, Figure 2.7 (b) shows XPS spectra of Si 2$p$ of HfO₂ and Al-doped HfO₂ films before and after PDA (850°C) [15]. Although the intensity of the peaks corresponding to Si-O bonding (near the binding energy of 102-104 eV) were similar in both cases of the HfO₂ and Hf₁ₓAlₓO₂ film before PDA (not shown here), the increase in the peak intensity after PDA was suppressed in the case of the Hf₁ₓAlₓO₂ film. This suggests that the Al₂O₃ in the film suppressed the silicate reaction, or Si-diffusion from the substrate, and interfacial layer.
growth [15].

Also, it was reported that Al-doping into the HfO$_2$ film decreased the $J_g$ level significantly. A plot of $J_g$ vs. EOT for the as-deposited Hf$_{1-x}$Al$_x$O$_2$ films shows the improved electrical properties of the Al-doped HfO$_2$ films with a 2 orders of magnitude decrease in $J_g$ compared to the non-doped HfO$_2$ film [15].

Figure 2.7 (a) XRD patterns of HfO$_2$ and Al-doped HfO$_2$ films with respect to the number of unit cycles in a HfO$_2$ sub-cycle after PDA [14] (b) XPS spectra of Si 2p of HfO$_2$ and Al-doped HfO$_2$ films before and after PDA [15]
Secondly, Si-doped HfO$_2$ is discussed.

Generally, the existence of a Si-related phase in the high-$k$ film is considered undesirable because it normally originates from Si-diffusion during high-$k$ film growth or PDA. The Si existence induces to increase EOT due to the low dielectric constant of SiO$_2$ ($\sim$3.9). However, several papers have reported that the intentional incorporation of an appropriate amount of Si (doping) increased the permittivity of HfO$_2$ film by modifying the crystalline structure of the film from monoclinic to tetragonal [16, 17]. Unlike the Al-doping HfO$_2$ discussed above, Si with a concentration $<$10 % could modify the crystalline structure of the HfO$_2$ film [17]. The permittivity of the Si-doped HfO$_2$ increased abruptly at the PDA temperature of 700°C, whereas those of the two films were similar until 600°C [16]. Optimization of the concentration of Si dopant in the high-$k$ film is important. The Si-doped HfO$_2$ film with Si concentrations ranging from 4 to 10 % crystallized into the cubic (or tetragonal)-like phase, but the pure HfO$_2$ film crystallized into the monoclinic phase. This phase transformation should affect the permittivity of the films. Figure 2.8 shows the permittivity of the Si-doped HfO$_2$ films as a function of the Si concentration, extracted from MIM capacitors (Au/Hf$_{1-x}$Si$_x$O$_2$/Pt) [17]. The permittivity of the amorphous Si-doped HfO$_2$ film decreased with increasing Si concentration because of the lower permittivity of the SiO$_x$ phase. On the other hand, the crystallized Si-doped HfO$_2$ films with the proper Si concentrations have higher permittivity ($\sim$27) than the amorphous films. Nevertheless, such Si-composition dependent crystallization behaviors have been observed from rather thick (>10 nm) films and on Pt substrate, which has little relevance to actual MOSFET applications. The Si-doped HfO$_2$ dielectrics as gate oxide will be detailedly discussed in result and discussion of Hf-silicate shown later.
Figure 2.8 $k$-value extracted from MIM capacitors as a function of the Si concentration ($x$) and annealing temperature. The characters $a$, $m$, and $t$ denote the film structures as amorphous, monoclinic and tetragonal, respectively [17].

Figure 2.9 The crystallization temperature as a function of Zr compositions in Hf$_{1-x}$Zr$_x$O$_2$. (b) GAXRD spectra of Hf$_{1-x}$Zr$_x$O$_2$ with various Zr compositions after annealing at 550°C [21].
Thirdly, Zr-doped HfO$_2$ is discussed

As mentioned above, ZrO$_2$ has proper dielectric constant and conduction band offset (CBO) similar with HfO$_2$ but has not received as much attention as HfO$_2$ because of its relatively insufficient thermal stability with Si (or poly-Si). However, since the replacement of the poly-Si with metal gate, ZrO$_2$ dielectrics certainly became to receive renewed interests. ZrO$_2$ films have a monoclinic, tetragonal, and cubic crystal structure depending on the temperature and pressure [18]. Moreover, when the ZrO$_2$ films are crystallized, the micro-structure of the films would be easily transformed from amorphous to tetragonal. In particular, the tetragonal phase shows a higher dielectric constant and smaller grain size in a crystallized film than the monoclinic phase [19, 20]. Figure 2.9 shows GAXRD spectra performed on annealed Hf$_{1-x}$Zr$_x$O$_2$ films with various Zr compositions to understand the effect of the Zr composition on the crystallization temperature and crystalline phase of Hf$_{1-x}$Zr$_x$O$_2$ films, as shown in Fig. 2.9 [21]. As shown in Fig. 2.9 (b), the crystallized ZrO$_2$ and HfO$_2$ have a tetragonal and monoclinic phase, respectively. The surface energy of the tetragonal phase is generally lower than that of the monoclinic phase. Therefore, the tetragonal phase can be stabilized when the grain size of the oxide material (or thin film) is small [22]. As a result, the grain size of the tetragonal phase film is smaller than that of the monoclinic phase film in both HfO$_2$ and ZrO$_2$ [23]. There is another merit of ZrO$_2$ dielectrics that in terms of the $V_{th}$ shift under PBTI stress in nMOSFET, ZrO$_2$ shows a much smaller $V_{th}$ shift than that of HfO$_2$ [24]. This suggests that Zr-doped HfO$_2$ dielectrics have more stable reliability than HfO$_2$. The origin of the $V_{th}$ shift reduction in ZrO$_2$ (Hf$_{1-x}$Zr$_x$O$_2$) is related to the reduced electron trap density, or lower oxygen vacancy concentration, in the bulk ZrO$_2$ than HfO$_2$. 

22
Finally, various lanthanide oxides such as La$_2$O$_3$ are discussed. La$_2$O$_3$ dielectrics have been attracting much attention due to their high dielectric constant (\(\sim 27\)) and large CBO with Si (\(\sim 2.3\) eV) and high thermal stability [25, 26]. However, the La$_2$O$_3$ dielectrics still have several critical problems such as the limited selection of precursors, inducement of unstable film growth due to its hygroscopic behavior, and serious Si diffusion from the substrate into the La$_2$O$_3$ film during deposition or PDA. In practice, these issues have limited the La$_2$O$_3$ oxides as gate dielectrics, and the La$_2$O$_3$ layer has been recently used to modulate flat band in general gate first approach.

Recent reports show that lanthanum-based ternary oxides, such as lanthanum scandate (LaScO$_3$) and lanthanum lutetium oxide (LaLuO$_3$), can have properties of amorphous dielectrics with high thermal stability, high dielectric constant (\(\sim 22\) to 23), wide bandgap (\(E_g = 5.5\) eV), and low leakage current. However, these lanthanide oxide films had nanometer-thick interfacial layers when deposited on Si substrates, which made it impossible to scale the EOT to the subnanometer range. However, recent research shows that ALD-deposited LaScO$_3$ and LaLuO$_3$ thin films have desirable structural and electrical properties, and are free of interfacial layers [27]. Nevertheless, La-based high-\(k\) dielectrics need more studies to replace the Hf-based dielectrics as gate dielectrics.
2.1.4 High-\(k\) gate dielectrics on Ge and III-V substrates

Although high-\(k\) dielectrics and metal gates have been used to improve the performance of transistors on Si substrate, Si-base CMOSFET is approaching its limit due to severe surface carrier mobility degradation. Therefore, various attempts such as modified channel materials have been investigated in attempts to improve device performance by enhancing the carrier mobility in the channel region. One of several possible modifications for the channel region involves replacing the conventional Si channel by alternative semiconductor materials such as Ge and III-V compound semiconductors. Table 2.3 summarized the characteristics of several potential channel materials compared to Si at 300 K. Compared to Si substrate, the bulk hole and electron mobility of Ge and III-V semiconductor materials shows higher values. Therefore, the higher mobility as well as smaller band gap of Ge and III-V semiconductor materials as a channel material has a number of advantages owing to the improvement in injection current density and the scaling of the supply voltage, which results in high speeds and a low power consumption.

However, there are several obstacles the Ge and III-V semiconductor materials face for being used as channel materials. The lack of a stable oxide and the necessity of a lower temperature process are the most critical problems among several issues. Because Ge substrates including InSb-like III-V materials has lower thermal stability, they start to melt above 900°C, which limits the maximum temperature that can be used in a Ge containing process.

As mentioned above, Si substrates have been successfully used in CMOSFETs, because of the existence of SiO\(_2\), which have physical and electrical excellent properties
as the gate dielectrics. Until now, there have been so many studies to find most suitable oxides, especially high-\textit{k} dielectrics, on Ge and III-V semiconductor materials. At the same time, various passivation methods have been investigated to stabilize the interface between Ge and III-V semiconductor materials and gate oxides and to suppress the volatilization of unstable oxide products, such as GeO and GaO\textsubscript{x}, from substrates.

In case of Ge substrates, the passivation methods between gate oxide and substrate are mainly surface nitridation, GeO\textsubscript{2} layer growth, sulfur clean (S-termination on Ge), Si monolayer deposition, and rare earth oxide growth. In III-V semiconductor materials, sulfur clean as well as stable oxide layer such as Al\textsubscript{2}O\textsubscript{3} has been mainly used as passivation techniques.

Usually sulfur-passivation on a Ge and III-V surfaces was carried out by preparing an aqueous (NH\textsubscript{4})\textsubscript{2}S solution. It has been reported that the sulfur termination is very effective in preventing the formation of the unwanted slow interface traps [28] and induces a lower Schottky barrier height for electrons and improved uniformity on the diode [39]. In case of passivation oxide layer, Al\textsubscript{2}O\textsubscript{3} layer has being mainly used due to self-cleaning effect, which means TMA source to grow Al\textsubscript{2}O\textsubscript{3} passivates the surface of substrates and suppresses the growth of unwanted interfacial oxide products such as Ga-O and As-O. However, in the case of using Al\textsubscript{2}O\textsubscript{3} as gate oxide, its dielectric constant (~9) was not enough to satisfy the requirement of high-\textit{k} gate dielectrics. Still, Hf-based high-\textit{k} dielectrics have been widely investigated as gate oxides on Ge and III-V semiconductor materials with several passivation methods.
## The Characteristics of Several Potential Channel Materials Compared to Si at 300 K

<table>
<thead>
<tr>
<th>Mobility (cm²/V·s)</th>
<th>Si</th>
<th>Ge</th>
<th>GaAs</th>
<th>InSb</th>
<th>InP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Electrons (µ_e)</td>
<td>~ 1500</td>
<td>~ 3900</td>
<td>~ 8500</td>
<td>~ 8000</td>
<td>~ 4600</td>
</tr>
<tr>
<td>Hole (µ_h)</td>
<td>~ 450</td>
<td>~ 1900</td>
<td>~ 400</td>
<td>~ 1250</td>
<td>~ 150</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Effective density of state (/cm³)</th>
<th>N_c (conduction band)</th>
<th>N_v (valence band)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si</td>
<td>1.04x10¹⁹</td>
<td>6.0x10¹⁸</td>
</tr>
<tr>
<td>Ge</td>
<td>2.8x10¹⁹</td>
<td>7.0x10¹⁸</td>
</tr>
<tr>
<td>GaAs</td>
<td>4.7x10¹⁷</td>
<td>7.3x10¹⁸</td>
</tr>
<tr>
<td>InSb</td>
<td>4.2x10¹⁶</td>
<td>1.1x10¹⁹</td>
</tr>
<tr>
<td>InP</td>
<td>5.7x10¹⁷</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bandgap, E_g (eV)</th>
<th>Si</th>
<th>Ge</th>
<th>GaAs</th>
<th>InSb</th>
<th>InP</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.12</td>
<td>0.66</td>
<td>1.42</td>
<td>0.17</td>
<td>1.35</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Electron affinity, χ (eV)</th>
<th>Si</th>
<th>Ge</th>
<th>GaAs</th>
<th>InSb</th>
<th>InP</th>
</tr>
</thead>
<tbody>
<tr>
<td>4.0</td>
<td>4.05</td>
<td>4.07</td>
<td>4.59</td>
<td>4.38</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Melting point, T_m (℃)</th>
<th>Si</th>
<th>Ge</th>
<th>GaAs</th>
<th>InSb</th>
<th>InP</th>
</tr>
</thead>
<tbody>
<tr>
<td>1412</td>
<td>937</td>
<td>1240</td>
<td>527</td>
<td>1060</td>
<td></td>
</tr>
</tbody>
</table>
2.2 Metal gates

2.2.1 Introduction of metal gates

As mentioned earlier, one of the key elements that allowed the successful scaling of silicon based CMOSFETs is certainly SiO$_2$. Like SiO$_2$ gate oxide on Si substrate, poly-Si gate electrode on SiO$_2$ gate oxide is another key element that allowed the superior improvement of transistor’s performance and the easy integration of CMOS process. The purpose of the gate electrode in CMOS is to shift the surface Fermi ($E_f$) of the Si channel to the appropriate band edge. An NMOS transistor consists of a p-doped Si channel and its gate electrode with low work function (~ 4.05eV) will move $E_f$ at the channel surface to its conduction band. A PMOS transistor has a n-doped Si channel and its gate electrode with 5.15eV will shift $E_f$ into its valence band. A difference in work function (WF) of gate electrodes is almost 1.1eV, or the Si band gap.

In CMOSFETs used above 45nm technology node, the gate electrodes are polycrystalline Si doped highly n-type or p-type, respectively, for NMOS and PMOS. Their WFs of n- and p-type doped poly Si gates are usually 4.05eV and 5.15eV, respectively. The doped poly-Si material has the advantage that it is refractory, easily deposited and doped, and compatible with SiO$_2$ and the process flows. Especially, the controllability of the WF through implantation of dopants has facilitated the easy adjustment of threshold voltage of CMOSFETs.

However, need for metal gates in next-generation scaled CMOS devices was firstly discussed by an early paper which was published in International Electron Devices Meeting 1997. As CMOS devices were scaling down to sub-micron technology node,
poly-Si gate electrode used generally in conventional CMOSFETs was faced with several critical issues such as poly-Si gate depletion, boron penetration and high gate resistance. Doped poly-Si gate electrode has limited carrier density, and so it contributes a depletion length of order 0.2nm to the capacitance equivalent thickness (CET) of the gate stack. Also, the penetration of doping element, especially boron, into Si channel through the gate oxide has deteriorated reliability of CMOSFETs. At an introduction of high-$k$ gate dielectrics, poly-Si gate electrode has been found to be fundamentally incompatible with $\mathrm{ZrO}_2$ or $\mathrm{HfO}_2$ oxide. It was found that the reducing ambient during the CVD deposition poly-Si from silane causes a gross reduction of the $\mathrm{ZrO}_2$ or $\mathrm{HfO}_2$, leading to silicide formation, leakage paths, Hf–Si bonds and nuclei for the large grain poly-Si growth [30, 31]. Therefore, high-$k$ gate oxides and metal gates must to be introduced simultaneously.

The gate metals to be used must to be ‘band edge metals’, with WFs equal to the band edge energies of Si, 4.05 and 5.15 eV. Also, the gate metals must to have the thermal stability of that metal in contact with the gate oxide and the process compatibility such as etch. Although replacement of the poly-Si gate electrode with the metal gate has been already implemented below 45nm technology node, there are still several issues. For example, NMOS metals with small WF are too reactive and unstable to maintain the low WF, while PMOS metals with high WF are too noble and difficult to etch.
2.2.2 Effective work function

2.2.2.1 Definition of effective work function

Firstly, let us consider how the WF of the gate electrode can affect flat band voltage ($V_{FB}$) of a MOS capacitor, or threshold voltage ($V_t$) of transistor. The WF is important for design of the metal–semiconductor junction in Schottky diodes. The WF difference between metal and silicon in a MOS capacitor is related to the $V_{FB}$ (i.e. the voltage that induces zero net charge in the underlying semiconductor) and the equivalent oxide charge per unit area at the oxide-silicon interface. The WF difference ($\phi_{ms}$) of a MOS capacitor is given by (see Fig. 2.10)

$$\phi_{ms} = \phi_m - \phi_s$$ \hspace{1cm} (5)

If the oxide and interface are ideal without fixed charges, the $V_{FB}$ of a MOS capacitor is determined by the WF difference, as shown in Fig. 2.11 (a). It is given by

$$V_{FB} = \phi_m - \phi_s = \phi_{ms}$$ \hspace{1cm} (6)

Also, the $V_t$ is determined by the $V_{FB}$.

$$V_t = V_{FB} + 2 \varphi_F + V_{ox}$$ \hspace{1cm} (7)

where $\varphi_F$ is the surface potential in the silicon, and $V_{ox}$ is the potential in the gate dielectric. Therefore, the WF of metal electrode is directly adjusting the $V_t$ of transistor.

From this equation (6), an effective work function (EWF) of the gate metal, $\phi_{m,\text{eff}}$, can be derived from the measured flat band voltage of the CV plot of the MOS capacitor, by referencing to the WF of Si substrate ($\phi_{ms}$), $\sim 4.1\text{eV}$ and $5.1\text{eV}$ for a n-type and p-type Si, respectively.

$$\phi_{m,\text{eff}} = V_{FB} + \phi_s$$ \hspace{1cm} (8)
Vacuum level

\[ \phi_m \]

\[ \phi_s \quad (4.05\text{eV}) \]

\[ \phi_s \quad (\sim 5.1\text{eV}) \]

Low WF (for NMOS)

High WF (for PMOS)

\[ \phi_{ms} \]

\[ 1.12\text{eV} \]

\[ q \]

\[ \chi \]

\[ F \]

\[ \phi \]

\[ F_s \]

\[ E_c \]

\[ E_i \]

\[ E_v \]

Metal

Oxide

Si

Figure 2.10 Band diagram of Metal-Oxide-Semiconductor (MOS) capacitor.
Figure 2.11 (a) Ideal and (b) real C-V curves of Metal-Oxide-Semiconductor (MOS) capacitor
However, for metal electrodes on an arbitrary high-$k$ oxide, definition of EWF has to consider two factors, which can change the $V_{FB}$ shifted by EWF; a Fermi level pinning and a fixed charge in gate stack. Fermi level pinning has been commonly known as a Fermi level pinning between the gate and high-$k$ dielectric caused by high-$k$ dielectrics such as HfO$_2$. Therefore, EWF of gate metals is different with its expected value depending on the underlying high-$k$ dielectrics. Researchers introduced a pinning factor $(S)$ as the change of EWF divided by the change in the metal’s vacuum WF. $S$ factor can be extracted from a slope of the vacuum work function as a function of the extracted EWFs of various metals on arbitrary oxide. Yeo et al extracted a slope of $S$ on HfO$_2$ and ZrO$_2$ are 0.53 and 0.41, respectively [32].

Also, changed by fixed charges in gate oxide and at oxide-silicon interface, the $V_{FB}$ become to sum an fixed charge term with $\phi_{ms}$, as shown in Fig. 2.11 (b),

$$V_{FB} = \phi_{ms} - \frac{Q_{ox}}{C_{ox}} = \phi_{ms} - \frac{Q_{ox}}{\varepsilon_{ax}}d_{ax}$$

(9)

where $Q_{ox}$ is fixed charge density, $\varepsilon_{ax}$ is permittivity of oxide, and $d_{ax}$ is thickness of oxide. Like the preceding, using this equation (9), real EWF of the gate metal, $\phi_{m,eff}$, can be derived from the plot (Fig. 2.12) of $d_{ox}$ as a function of the $V_{FB}$ of the CV curves of the MOS capacitor, by referencing to the WF of Si substrate ($\phi_s$), ~4.1eV and 5.1eV for a n-type and p-type Si, respectively. For example, in Fig. 2.12, y-intercept is $\phi_{ms}$ value. EWF(eV) = $\phi_{ms}$ + 5.1 for p-type Si substrate and EWF(eV) = $\phi_{ms}$ + 4.1 for n-type Si substrate. A slope of the plot (Figure 2.12) means also fixed charge density divided by the
permittivity of oxide (in case of SiO$_2$ : 3.9$\varepsilon_0$).

Also, this equation (9) can be changed in terms of EOT (Fig. 2.12 inset),

$$V_{FB} = \phi_{ms} - \frac{Q_{ox}}{C_{ox}} = \phi_{ms} - \frac{Q_{ox}}{\varepsilon_{SiO_2}} EOT$$

(10)

where $\varepsilon_{SiO_2}$ is permittivity of SiO$_2$, which is 3.9$\varepsilon_0$.

Figure 2.12 Plot of oxide thickness as a function of $V_{FB}$ from CV curves of Metal-Oxide-Semiconductor (MOS) capacitors.
2.2.2.2 Extraction of effective work function

As mentioned above, extraction of the flatband voltage ($V_{FB}$) of Capacitance–Voltage (C–V) curves for a dielectric thickness series has traditionally been the method for EWF extraction on SiO$_2$ dielectrics (linear extraction of the $V_{FB}$ vs. equivalent oxide thickness (EOT) relationship) [33]. To use the equation (9) and (10) for extracting EWF, bulk and interface fixed charges in the dielectrics have to be constant although varying high-$k$ dielectric thicknesses. However, it is difficult to maintain a constant fixed charge in the bulk and at the Si–dielectric interface because the high-$k$ dielectrics react with the substrate silicon to form interfacial SiO$_x$. Therefore, the terraced oxide method was proposed as a more accurate methodology for EWF in both oxide (SiO$_2$)-only and high-$k$ dielectric stacks through the linear extraction from the $V_{FB}$-EOT relationship [34, 35]. Experiment details of terraced oxide structures in the reference 35 are as in the following:

- Thermal SiO$_2$ growing (5nm) on highly doped n-type (or p-type) Si substrate
- Wet etching of the SiO$_2$ using spin etcher: stepwise thickness (1, 1.5, 2.5, 3.5nm)
- HfO$_2$ deposition (3nm) using atomic layer deposition (ALD)
- TiN (10nm) metal gate and poly-Si(or W) capping layer using ALD
- C-V curves were measured at 100 kHz
- $V_{FB}$ and EOT values were computed from the NCSU CVC program

Figure 2.13 shows a schematic diagram of the terraced oxide stack showing a fixed high-$k$ dielectric material on a varying interfacial SiO$_2$ layer and $V_{FB}$ versus EOT curve used to extract the EWF [36]. The colored bands on the wafer are regions of different SiO$_2$ thickness (oxide thicknesses in this image are extremely thick and for visual demonstration only; actual device SiO$_2$ thicknesses can vary from 10 to 100 Å). The
transmission electron microscopy inset shows a schematic cross-section of the typical device [36].

Figure 2.13 (a) A schematic diagram of the stack showing a fixed high-κ dielectric material on a varying interfacial SiO₂ layer and (b) $V_{FB}$ versus EOT curve used to extract the EWF [36].
By using a single wafer, a constant Si/SiO₂ interface fixed charge can be maintained, and the influence of high-\(k\) bulk charges is limited with a single thickness of high-\(k\). For easy analysis, researchers have chosen a simplified three charge model including the normal oxide-silicon interface charge density \((Q_f)\), an interfacial oxide (SiO₂)-high-\(k\) film interface charge \((Q_i)\), and a bulk high-\(k\) film charge density \((\rho_b)\), assumed uniformly distributed. This simplified model neglects bulk charge in the interfacial oxide because of thermal SiO₂. The relation equation yields the following relationship between measured \(V_{FB}\) and the other parameters of the structure,

\[
V_{FB} = \phi_{ms} - \frac{Q_f \cdot EOT_h}{\varepsilon_{SiO_2}} - \frac{\rho_b \cdot (\varepsilon_{SiO_2}) \cdot EOT_h^2}{2\varepsilon_{SiO_2}} - \frac{Q_f \cdot EOT}{\varepsilon_{SiO_2}} \tag{11}
\]

where EOTₕ is EOT of high-\(k\) film and EOT is EOT of high-\(k\)/SiO₂ stack.

By maintaining a fixed high-\(k\) thickness is sufficiently thin (2~3nm), the second and third terms become a constant (~very small values, ~tens of mV). Finally, this equation (11) can be like equation (10),

\[
V_{FB} = \phi_{ms} - \frac{Q_f \cdot EOT}{\varepsilon_{SiO_2}} \tag{12}
\]

Therefore, EWFs of gate metals on high-\(k\) dielectrics can be more accurately extracted by using the linear \(V_{FB}\)-EOT extraction from the terraced oxide stack approach.
2.2.3 Control of effective work function

2.2.3.1 Selection of metal gate materials

The metal work function ($\phi_m$) is a very important consideration in the selection of metal gate materials for transistor integration because it directly affects the threshold voltage ($V_t$) and gate leakage density ($J_g$) of a transistor. Effective work function (EWF) should be predominately determined by the bulk/vacuum work function of the material, which is mostly determined by the electronic and ionic structure of the metal. The vacuum work function for materials in the periodic table is summarized by Michaelson et al. [37]. Materials in columns IIIB, IVB, and VB are suitable for n-type EWFs, while materials in column VIII have p-type EWFs. The EWF of various metal gate materials on SiO$_2$ oxide have been demonstrated to exhibit reasonably similar trend with the bulk (vacuum) work function (WF). Figure 2.14 shows the vacuum (bulk) WFs of various metal materials for gate metal and EWF on SiO$_2$ versus bulk WF [38,39]. Therefore, various metal materials can be selected for matching target work function (5.0–5.2 eV for PMOS, and 4.1–4.3 eV for NMOS) to maintain the low $V_t$ in CMOS devices.

However, NMOS gate metals such as La and Sr with small WF are too reactive and unstable to maintain the low WF, while PMOS metals such as Pt and Ru with high WF are too noble and difficult to etch. In addition, The Fermi level ($E_f$) pinning effect between the metal/high-$k$ is believed to be the intrinsic limitation for obtaining band-edge EWF metal electrodes. Also, interface stability of the pure metals with high-$k$ dielectrics is a concern due to additional thermal budgets arising from post gate stack processing. From the thermal stability concerns of metals on HfO$_2$ and the influence of bulk/interface charges from the dielectric itself, the extracted EWF based on the linear $V_{FB}$-EOT
relationships is observed to be different from that on SiO₂ and has shown a great disparity even within a single metal system.

As a result, metal alloys (or compounds) such as TiAlN and TiN have been evaluated and are proposed as an improved metal gate with both the low and high WFs. In addition to the elemental metals, other metallic materials such as metal silicides, metal nitrides, metal oxides, and metal alloys are also considered as potential metal gate candidates.

Although an extensive and systematic study of metal EWFs on high-κ dielectrics has been reported, the range of EWF tunability for thermally stable metal electrodes is mostly found to be limited to ~4.2–4.9 eV. The interface between the metal gate and high-κ dielectric is found to be critical in determining the EWF, and recent research focus has changed to utilizing interface control for EWF modulation.

Figure 2.14 Plot of (a) vacuum work functions of various metal materials for gate metal [38] and (b) effective work function on SiO₂ versus bulk work function reported in literature [39].
2.2.3.2 Interface modulation

As mentioned above, the lack of direct correlation between EWF on high-\(k\) dielectrics and bulk WF suggests other factors besides the bulk work function (such as \(E_f\) pinning, interfacial reactions, film structural changes, etc.) also impact the EWF. Therefore, EWFs for metal gate electrodes on high-\(k\) dielectrics extracted from the flatband voltage (\(V_{FB}\)) can be a combination of the true work function (WF) + dielectric stack charges + interface dipole formation or other factors such as Fermi-level pinning [35]. Recently, the several factors, which can induce to shift \(V_{FB}\) of metal gate/high-\(k\) stack, have been used to modulate EWF of various metal materials because EWF is generally extracted from the \(V_{FB}\).

One such technique is via insertion of a dielectric capping layer between the metal/high-\(k\) dielectric. Representatively, La-/Al-based interface layer (IL) such as \(\text{La}_2\text{O}_3\) (or La) and \(\text{Al}_2\text{O}_3\) (or Al) of ~ 1 nm has been proposed for modulating the \(V_{FB}\) of NMOS and PMOS, respectively [40,41]. The EWF values of metal electrodes with Al-based IL increased by ~0.25 eV over their initial values, independent of the metal electrode system. Engineering the interface toward n–type EWF is also consistently demonstrated with the use of lanthanide-based dielectrics (\(\text{La}_2\text{O}_3\), \(\text{Y}_2\text{O}_3\)). The effect is theorized to be due to the formation of a dipole layer at the high-\(k\)/SiO\(_x\) interface [42]. In a dipole mechanism, rare earth (RE) oxides such as \(\text{LaO}_x\) and \(\text{SrO}_x\) likely diffuses to the high-\(k\)/low-\(k\) (SiO\(_x\)) interface and forms a dipole momentum (Hf-O-RE configuration) at the interface, as shown in Fig. 2.15. The configuration can result in a charge transfer and tune the \(V_{FB}\). The amount of charge transfer determines the magnitude of the dipole (\(\mu\)). \(\mu\) is determined by \(+Q\) (charge on + pole) and \(-Q\) (charge on – pole), separated by a distance
(d). This dipole vector shifts the EWF a variable amount $\Delta$ depending on dopant electronegativity and radii than their valence. For example, $V_{FB}$ shift ability in MG/REO$_x$/HfSiON stacks indicates the following order: Sr>Er>Sc+Er>La>Sc, in which SrO showed maximum NMOS $V_t$ tuning of $\sim$ 600mV [42]. However, La$_2$O$_3$ (or LaO$_x$) dielectric has been widely used for tuning NMOS’s $V_t$ due to a process availability and affordable source.

Figure 2.15 Interface dipole moment model. EWF shift is proportional to dipole moment due to the charge transfer in the Hf-O-RE (rare earth) configuration [42].
Other techniques include interface modulation by diffusion of additional species (such as Al, La) to the metal/high-k interface; this utilizes lessons learned from alloyed metals, but can only be implemented in the gate last flow, where the thermal stability requirement is less stringent. Vt modulations for NMOS and PMOS in TiN/HfO2 gate stacks can be obtained via low temperature anneal and selective cladding layers on metal gate. Oxygen concentration near the TiN/HfO2 interface has been correlated to shifts in the Vt, as shown in Fig. 2.16 [43]. For NMOS optimization, Al migration from the cladding to the TiN/HfO2 interface during forming gas annealing in conjunction with low O concentration in the TiN enables a low EWF. For PMOS optimization, the use of non-migrating W cladding along with a N-induced dipole, resulting from displacement of N during the low temperature oxidizing anneal of the TiN, facilitates high EWF.

Many studies of such an oxygen control at the metal/high-k interface have been published, suggesting that an increased oxygen level at the interface can modulate the EWF toward PMOS needs (high). One hypothesis proposed the cause to be a reduction of oxygen vacancies in the dielectric, but recent reports suggest the increased oxygen level at the interface may be due to the displacement of N in nitride electrodes with O, thus forming an N-induced dipole at the TiN/HfO2 interface [44].
Figure 2.16 Metal/high-	extit{k} dielectric interface modulation model using cladding layer on gate [43].
2.2.4 Metal gate integration

Besides the achievement of the appropriate effective work function at the metal–
dielectric interface, one of the most important challenges in the high-k/metal gate CMOS
technology is the integration of two different types of metal gates in a device fabrication
process. The industry is divided between gate-first [45] and gate-last [46] integration
schemes at the 45 nm and 32 nm device technology nodes. Intel has started to use the
gate-last integration scheme at 45 nm technology node, while other companies such as
IBM and Samsung have used the gate-first integration scheme at 32 nm technology node.
However, most chipmakers will use the gate-last approach in a conventional CMOSFET
process below 28 or 22 nm technology node because of various integration issues.

2.2.4.1 Gate-first integration

The gate-first integration scheme is characterized by deposition of the high-k/metal
gate stack at the start of the process. Because, in a conventional CMOSFET process, high
temperature activation annealing is necessary for activating dopants in source and drain
regions. The high-k/metal gate stack is then processed through the high temperature (>~1000°C) of the source and drain activation anneal. Therefore, in the gate-first integration
scheme the high-k gate dielectrics need to have the high thermal stability due to the
formation of the gate stack before the activation annealing of the source and drain, as in a
conventional CMOSFET process. Figure 2.17 shows cross-section schematics for typical
gate-first integrated devices and TEM images of Globalfoundries’s gate-first integrated
devices at 32 nm technology node. In the cross-section schematics, the noticeable features
are the dielectric capping layers specifically engineered to create favorable dipoles for
tunning the EWFs. The metal nitride electrode provides for high carrier densities to eliminate polysilicon depletion effects. The first challenge in a gate-first flow is integration of the dual dielectric capping layers. The first dielectric capping layer (typically Al₂O₃ for the PMOS device) is deposited across the entire wafer. Then the Al₂O₃ is selectively removed from the NMOS regions via a photolithography step and a wet etch step that is selective to the underlying HfO₂ gate dielectric. Next, the NMOS capping layer (typically La₂O₃) is deposited and similarly patterned and wet-etched from the PMOS regions [48]. The metal nitride gate electrode and polysilicon top electrode are deposited, and the entire gate stack must be patterned to define the active gates. The next critical step occurs during the junction activation, which exceeds temperatures of 1000°C. This anneal not only diffuses and activates dopants in the junctions, but provides the thermal budget to trigger the EWF setting of the dielectric capping layers. However, this step also requires a balance between these beneficial mechanisms and the diffusion of metal from the capping layers to the dielectrics/Si-substrate interface, which would cause deleterious Vᵢ shifts and mobility degradation [48]. For example, although Al and La additions induced positive and negative ΔVᵢ of up to 148mV and 433mV, respectively, due to interface dipole modulation, hole and electron mobilities for Al and La additions was lowered. Moreover, the mobility of hole decreased gradually by Al addition increase, while that by La addition was constant [48]. The rest of the gate-first flow follows the conventional CMOS flow. The structure of the Globalfoundries’s gate-first integrated transistors is detailed in Fig. 2.17 (c) and (d). The gates were almost fully silicided with tensile nitride for channel stress. The sidewall spacers have been etched back, perhaps to enhance the stress. Titanium nitride (TiN) for n/pMOS appears to be the work-function
metal on no-dopant Hf-based high-\( k \) dielectric. Also, the capping layers are used even if not detected in the images.

Figure 2.17 Schematics depicting a cross-section of typical gate-first integrated (a) nMOS and (b) pMOS devices, and TEM images of Globalfoundries’s gate-first integrated (c) nMOS and (d) pMOS at 32nm technology node [47].
2.2.4.2 Gate-last integration

The gate-last integration scheme, however, is characterized by deposition of the high-$k$/metal gate stack after the high temperature activation annealing, which is benefiting from the low temperature thermal budget (less than 500 °C) of the back-end processes. Figure 2.18 shows cross-section schematics for typical gate-last integrated devices in replacement-gate process and TEM images of Intel’s gate-last integrated pMOS at 45 nm (1st generation replacement gate process) and 32 nm (2nd generation replacement gate process) technology node. When Intel started firstly to use high-$k$/metal gate stack at 45 nm technology node, the gate-last process did not replace first-deposited high-$k$ dielectric/thin metal layer, and the remained high-$k$ dielectric/thin metal layer was used as gate stack. However, Intel changed the 1st gate-last integration scheme into 2nd all replacement gate-last scheme, in which first-deposited high-$k$ dielectric layer including thin metal layer was replaced by new-deposited high-$k$ dielectric and metal gate. In the 2nd replacement gate-last integration scheme, the noticeable feature is the presence of high-$k$ dielectric and metal gate electrode films deposited alongside the interior walls of the spacer. This requires the removal of a dummy gate electrode (typically polysilicon) prior to the high-$k$/metal gate stack deposition. The removal of the dummy polysilicon is challenging, requiring chemical-mechanical polishing to expose the dummy gates and selective removal (a wet etch process utilizing NH$_4$OH) of the silicon dioxide underneath the dummy gate. An atomic layer deposition process for high-$k$ dielectric and the nMOS and pMOS metal electrodes deposition is needed to ensure highly conformal deposition at the bottom of the gate stack. The critical step at this point in the flow is the selective patterning of the opposite electrode material from its complementary gate, which requires
challenging photolithography and etching of the metal gate from the narrow gate trench. The gate stack formation is completed with the deposition of the metal fill material (typically Al). A final planarization of the surface using chemical-mechanical polishing completes the device formation [49]. The structure of the Intel’s PMOS transistor is detailed in Fig. 2.18 (c) and (d). In 45 nm technology node, the pMOS work-function metal appears to be ~2 nm titanium nitride (TiN), deposited on top of the HfO$_2$ before the polysilicon. After polysilicon removal a tantalum-based barrier layer (~1 nm) is laid down, followed by ~9 nm more TiN that seems to act as a barrier layer for the NMOS work-function materials. The nMOS work-function metal is a ~2 nm TiAlN layer. The thick TiN and Ta barrier layers used in the PMOS devices were etched back in the NMOS regions, and a Ti/Al (54/46%) layer deposited into the common gate trenches; on the TiN prepoly layer in the NMOS gates, and on the thick TiN in the PMOS.

When contrasting the advantages and challenges of gate-first versus gate-last processes, the control of the EWF is the deciding factor. Since the gate-last flow only exposes the gate stack to the low thermal budget of the back end, the EWF can be set and controlled to the desired band-edge target. This is especially important for the pMOS device, which has typically been susceptible to work function roll-off at high thermal budget, which will be discussed later. EOT control is another important aspect, since the use of dielectric capping layers in the gate-first flow results in a larger electrical thickness (~2 Å) on pMOS than nMOS. This is not the case for the gate-last flow, where the same EOT can be achieved on both nMOS and pMOS structures. The gate-last scheme is becoming a favorite among many device manufacturers [36].
Figure 2.18 Schematics depicting a cross-section of typical gate-last integrated (a) nMOS and (b) pMOS in replacement-gate process, and TEM images of Intel’s gate-last integrated pMOS at (c) 45nm and (d) 32nm technology node [47].
2.3 Issues of High-\textit{k} dielectrics/Metal gates

2.3.1 Fermi level pinning effect

As mentioned above, high dielectric constant (high-\textit{k}) oxides such as HfO\textsubscript{2} has replaced SiO\textsubscript{2} as the gate dielectric and various metal gates have replaced polycrystalline Si as the gate electrode. However, there are still several issues to have been not solved until now. Especially, HfO\textsubscript{2} was chosen as the gate oxide because it does not react with Si. The gate metals are chosen so that their Fermi energies should align with the conduction or valence band edges of Si, for n-FETs and p-FETs, respectively. However, it has proved difficult to find suitable metals to achieve this and withstand annealing to 1000 °C. The gate Fermi level (\(E_F\)) tends to shift toward an energy independent of the metal, near the midgap of Si, a problem referred to as “Fermi level pinning (FLP)” \([50,51]\). This is particularly acute for high work function p-metals at low effective oxide thickness (EOT) gate.

The first report was that Fermi pinning at the polysilicon/metal oxide interface causes high threshold voltages in MOSFET devices. Many papers reported the pinning occurs due to the interfacial Si–Hf bonds for poly-Si electrode on HfO\textsubscript{2}. Also it was reported that oxygen vacancies at polysilicon/HfO\textsubscript{2} interfaces lead to Fermi pinning \([50]\). However, although various metal gates have replaced poly-Si as the gate electrode, FLP effect still makes it difficult to modulate \(V_t\) of CMOSFET, especially pMOS. Figure 2.19 shows the band diagram of FLP effect of metal electrode/high-\textit{k} dielectric/Si substrate stack. FLP effect that Fermi level (\(E_F\)) of metal tends to shift toward near the midgap of Si induces the WF difference (\(\phi_{m,i}\)) value to decrease abruptly which means \(V_t\) of CMOSFET.
increases (See section. 2.2.2).

Figure 2.19 Band diagram depicting a Fermi level pinning (FLP) of metal/high-k/Si stack. Fermi level ($E_F$) of metal electrode tends to shift toward near the midgap of Si after annealing.
There have been several possible explanations for FLP such as metal induced gap states (MIGS), specific bonding configurations and oxygen vacancy model. MIGS theory is only a first approximation to the problem since it only considers the bulk contribution to the Fermi pinning and does not take into account the atomic bonding at the interface with the gate. In poly-Si/high-$k$ dielectrics stack, it was generally concluded that the effect is due to interaction between the poly-Si gate and the HfO$_2$ layer causing a Fermi level pinning at the gate-HfO$_2$ interface. On the other hand, in metal gates/high-$k$ dielectrics stack, the physical mechanisms for FLP and flat band voltage ($V_{FB}$) shifts are not well understood.

Studies found that high work function metals such as Pt, Re, or Ru show an instability in oxygen-deficient conditions, and their $E_F$ moves toward midgap when annealed above 500 °C. These metals are transparent to oxygen and hydrogen at high temperatures, and the shift could be reversed by annealing in oxygen. However, the work function of Pt metal varies little with small oxygen content. This suggests that pinning is extrinsic and may be related to oxygen vacancies in the oxide layer [52]. In terms of extrinsic FLP, the pinning effect can be inhibited by reoxidation of vacancies at a low enough temperature that it does not cause thickening of the SiO$_2$ interlayer. It appears in some cases that the oxidation of a Ru electrode can also contribute to the $V_{FB}$ shifts. However, the generality of pinning behavior suggests that this is not the main cause. Additionally, dipole layers at the HfO$_2$–SiO$_2$ interface could arise, but a vacancy model is a natural mechanism [52]. For one reason or another, the FLP effect can still affect the $V_t$ modulation for CMOSFET, especially pMOS.
2.3.2 Flat band roll-off effect

Since employing metal electrodes with high-\(k\) dielectrics, one of the most difficult things is obtaining n- and p-type metal gate electrodes with work functions (WFs) matching the Si valence- and conduction-band edges, respectively. By using metals with appropriate intrinsic WFs as well as various engineering approaches, both n- and p-type EWFs have been demonstrated. However, when these gate stacks consisting of the metal electrode, high-\(k\) dielectric, and interfacial SiO\(_2\) layer (IL) were used in devices with scaled-down equivalent oxide thicknesses (EOTs), their EWF values were found to be significantly less than those obtained in test structures with thicker gate stacks. This phenomenon, which significantly limits the available options for metal/high-\(k\) transistor fabrication, is called V\(_{FB}\) roll-off.

V\(_{FB}\) roll-off is a general phenomenon observed in all known types of high-\(k\)/metal gate stacks fabricated with transition metal oxides, as shown in Fig. 2.20. A model should explain the following general dependences [53];

1) Thickness of the interfacial SiO\(_2\) layer: starts at a certain minimal thickness of a SiO\(_2\) interfacial layer and increases as the SiO\(_2\) becomes thinner.

2) Temperature: increases with a higher thermal budget, i.e., higher temperatures and/or longer anneal times.

3) Electrode WF: increases with higher WF

4) High-\(k\) thickness and composition: increase with high-\(k\) thickness and higher Hf content in the case of hafnium silicate (HfSiO) dielectrics

5) Si substrate type: is slightly greater on p-type substrates.
Figure 2.20 Dependence of $V_{FB}$ on EOT in high-$k$/SiO$_2$ terraced-oxide capacitors with metal electrodes of different WF values. Each trend line corresponds to a specific metal electrode [53].

Figure 2.21 Roll-off suppressions by (a) low-temperature oxygen annealing and (b) incorporating fluorine into the interfacial SiO$_2$ layer. (Inset) CV characteristics of the capacitor stacks with F-doped IL and control [53].
While several models for the roll-off have been proposed, the physical mechanisms for the roll-off are not well understood like FLP. Recently, a proposed model for the roll-off mechanism explained as in the following [53]; 1) Positively charged defects (oxygen vacancies) are generated in the interfacial SiO$_2$ layer due to its interaction with the high-$k$ dielectric, and the density of these defects increases 2) in a thin (< 2.5 nm) SiO$_2$ layer, with 3) higher processing temperatures, 4) thicker high-$k$ film, and 5) higher metal electrode WFs.

Indeed, thicker high-$k$ films (up to a certain thickness value defined by the vacancy diffusion length under given process conditions) function as a stronger source of oxygen vacancies in the interfacial SiO$_2$ layer, leading to greater roll-off. Similarly, higher WF electrodes, which exhibit higher efficiency in generating oxygen vacancies in transition metal oxides, are expected to enhance roll-off by increasing the oxygen vacancy supply to the interfacial oxide. Both generation and diffusion of oxygen vacancies in dielectric stacks are controlled by the thermal budget, leading to strong roll-off temperature dependence. Since the charge state of oxygen vacancies in the interfacial SiO$_2$ layer depends on the position of the substrate Fermi level, the probability for a vacancy to be in a positive charge state (rather than in neutral one) increases in a gate stack fabricated with p-Si, which explains the roll-off dependence on substrate type [53].

The roll-off phenomenon could be suppressed by using passivating oxygen vacancy. Figure 2.21 shows that the roll-off suppressions by low-temperature oxygen annealing (LTOA) to prevent interface growth and by substituting oxygen (O) with fluorine (F), which is known to form a stronger bond with Si, to suppress vacancy generation in the SiO$_2$ interfacial layer (IL).
2.3.3 Further EOT scaling methods

The semiconductor industry has already converged on Hf-based oxides, such as HfO$_2$ or HfSi$_x$O$_y$, for the first generation CMOS products featuring high-$k$ gate dielectrics and metal gate electrodes. The equivalent oxide thickness (EOT) for the first generation high-$k$/metal gate device is approximately 1.0 nm [49]. Continued gate length ($L_g$) scaling for the 32 nm and beyond with a planer structure requires sub-nm EOT to suppress short-channel effects. Fully depleted device structures, such as FinFET or extremely thin SOI (ETSOI), improve short-channel control and thus relax the requirements for EOT scaling. However, the insertion point of such device architectures is expected to be the 22 nm and beyond and sub-nm EOT may be still required at those advanced technology nodes.

A typical high-$k$/metal gate stack structure contains a silicon oxide based interfacial layer (IL), a high-$k$ dielectric, followed by a metal gate electrode. This system is equivalent to two capacitors connected in series. Thus, the total EOT of the high-$k$/metal gate stack can be expressed as follows.

$$EOT_{\text{total}} = EOT_{\text{IL}} + EOT_{\text{high-k}}$$  \hspace{2cm} (13)

An apparent way to scale $EOT_{\text{high-k}}$ is to reduce the physical thickness of the high-$k$ layer, however, there is little room in this direction. However, the industry-integrated high-$k$/metal gate devices already employ the thinnest possible high-$k$ layer. Therefore, this leaves us with three possible EOT scaling approaches: (1) Introduce a new high-$k$ material with k-value greater than that of HfO$_2$ (so-called “higher-$k$”); (2) Reduce the physical thickness of IL (so-called “scavenging”); (3) Increase the k-value of IL [54].

Current status and challenges for each approach and discuss the EOT scaling strategy for future CMOS devices are reviewed.
2.3.3.1 Higher-\(k\) dielectrics

Higher-\(k\) dielectrics are materials having dielectric constant (\(k\))-values greater than HfO\(_2\), which is one of the most widely used high-\(k\) materials, showing a \(k\)-value of approximately 20. In pursuit of higher-\(k\) materials, the tradeoff between \(k\)-value and band gap (or band offset) needs to be taken into account (See 2.1.2). It is generally known that band gap values have a roughly inverse dependence on \(k\)-values (actually \(E_g \sim k^{-0.65}\)) [55]. As already showed in Fig. 2.5, a search for higher-\(k\) oxides should consider oxides of smaller band gap, which would also include those with poor stability against Si, such as Ta or Ti. Also, the conduction band offset (CBO) is smaller than the valence band offset, so the CBO value is more critical. In this case, the lanthanides stand out as they have characteristically larger CBOs than the HfO\(_2\) or ZrO\(_2\) series. Therefore, materials with too high \(k\)-values typically result in excessive direct tunneling currents and most work showing promising EOT-leakage current density (\(J_g\)) characteristics has been achieved with \(k\)-value ranging from 20 to 30 [54].

In addition, a doping of another kind of atoms into HfO\(_2\) was a many reported way to stabilize the higher-\(k\) phase (tetragonal or cubic) of HfO\(_2\), even if the doping material had a quite low dielectric constant such as Si, Al, Zr, La, and Gd. This is a practical means to attain a modest \(k\)-value increase, however, controllability of crystallinity in an ultra thin HfO\(_2\) thickness regime (<2 nm) has yet to be demonstrated. Recently, other groups have reported that La-based higher-\(k\) materials such as LaAlO\(_3\), LaLuO\(_3\), and LaScO\(_3\) demonstrate a lot of promise to outperform Hf-based high-\(k\) on a device level.

Apart from the higher-\(k\) materials, a La\(_2\)O\(_3\) capping layer on a Hf-based high-\(k\) layer, widely used to adjust the \(V_t\) of nMOSFET, is a less disruptive way to increase the \(k\)-value.
of SiO$_2$-based IL. Because some portion of the La elements diffuse through the high-$k$ layer and form La-silicate IL after high temperature anneals. However, the aggressive scaling is accompanied with effective work function (EWF) shift toward the Si conduction band minimum (CBM) in most cases. Formation of dipoles such as La, Lu, and Sr makes application of these materials to pMOSFET extremely difficult.

### 2.3.3.2 Scavenging effect

Considering the maturity of Hf-based high-$k$ gate dielectrics, scaling SiO$_2$-based interfacial layer (IL) in conjunction with Hf-based oxides may be more practical in meeting the requirements for the 22 nm technology node and beyond. Introduced as an oxygen-gettering metal overlayer in high-$k$ metal oxide/silicon interface [56], scavenging reaction has become a mainstream approach to scale the IL in recent years. The scavenging effect means that metal ions on high-$k$ dielectrics take oxygen from the IL and decrease the IL thickness, which induces EOT$_{IL}$ to decrease (or means EOT$_{total}$ scaling).

Several important factors for these IL scavenging processes are as in the following [54]: (1) IL growth condition, (2) Choice of scavenging element, (3) Location of scavenging element, (4) Maximum process temperature.

Firstly, it was reported that EOT scaling via IL scavenging strongly depends on the growth condition of the initial IL [57]. In this work, room temperature chemical oxide ILs showed more EOT scaling compared to in-situ steam generation (ISSG) oxide ILs at 760-900 °C and thermal oxide ILs at 1,100 °C. Since IL scavenging reaction is a reverse reaction of IL growth, a uniform SiO$_2$ layer with low formation energy may be preferred as a starting IL to facilitate the scavenging reaction at later stages of process flow.
Secondly, scavenging element is one of the most important factors for IL scavenging reaction, which is more accelerated when the Gibbs free energy for oxide formation of scavenging element becomes higher (see Fig. 2.6). The EOT trend for metal-inserted poly-Si stack (MIPS) with SiO$_2$/HfO$_2$ gate dielectrics is summarized in Fig. 2.22 as a function of the Gibbs free energy change at 1,000 K ($\Delta G_{1000}^0$) per oxygen atom ($\Delta G_{1000}^0$/O) for the scavenging element [54,57]. As shown in Figure 2.22, most thermally stable metals studied in the early phase of high-$k$/metal gate development (e.g., W, TaN) have negative $\Delta G_{1000}^0$/O values, resulting in IL regrowth during high temperature activation anneal. On the other hand, transition elements such as Ti, Hf and La with much more positive $\Delta G_{1000}^0$/O values result in strong scavenging effect from IL, while coming with a severe penalty in thermal stability due to high reactivity with high-$k$ layers. Thus, direct capping of very strong scavenging metals may not be compatible with the state-of-the-art CMOS integration requiring higher process temperatures. To overcome this trade-off, doping of scavenging metals with high $\Delta G_{1000}^0$/O values into a thermally stable TiN electrode was proposed. This technique enables highly controllable IL scavenging for both gate-first and gate-last integrations.

Thirdly, based on the locations of the scavenging elements in the gate stacks, direct-scavenging and remote-scavenging effects can be divided. Figure 2.23 illustrates the difference between the two categories. Direct-scavenging schemes incorporate the scavenging elements within the high-$k$ layers, whereas the remote-scavenging schemes isolate the scavenging elements from the high-$k$ layers. Early IL scavenging works fall into the direct-scavenging category since the scavenging metals are incorporated within the high-$k$ layers either by direct capping (or TaN-M alloy).
Figure 2.22 EOT of SiO$_2$/HfO$_2$ metal-inserted poly-Si stack (MIPS) structure as a function of $\Delta G^0_{1000}$ per oxygen atom for scavenging element. TiN electrodes doped with various metals are compared with literature data [54,57].

![Figure 2.22 EOT of SiO$_2$/HfO$_2$ metal-inserted poly-Si stack (MIPS) structure as a function of $\Delta G^0_{1000}$ per oxygen atom for scavenging element. TiN electrodes doped with various metals are compared with literature data [54,57].](image)

<table>
<thead>
<tr>
<th>Type</th>
<th>Direct</th>
<th>Remote</th>
</tr>
</thead>
<tbody>
<tr>
<td>Scavenging element (M)</td>
<td>Within High-k</td>
<td>Isolated from High-k</td>
</tr>
<tr>
<td>Schematics</td>
<td>Metal Gate</td>
<td>TaN-M alloy</td>
</tr>
<tr>
<td></td>
<td>High-k</td>
<td>High-k</td>
</tr>
<tr>
<td></td>
<td>SiO$_2$</td>
<td>SiO$_2$</td>
</tr>
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</table>

Figure 2.23 Schematics of direct- and remote-scavenging techniques [54].

Because the direct-scavenging do not require such a strong driving force of the reaction, a
relatively weak scavenging metal such as Ti can cause aggressive EOT scaling. However, this approach induces effective work function (EWF) change either by inherently low vacuum work function of scavenging metals or by formation of fixed charges and/or interface dipoles [54]. To overcome these problems, the concept of remote-scavenging emerged as doping scavenging elements into a thermally stable TiN electrode, which cause IL scavenging reaction without out-diffusion of the scavenging elements into the high-\(k\) layer. Such a process enables EOT scaling without extrinsic degradation in carrier mobility and leakage current and with no change in EWF.

Finally, the maximum process temperature after the deposition of M-doped TiN electrodes can affect the scavenging effect (IL reduction amount). Most of the EOT scaling effect from the doped TiN already took place at 600 °C and little further change occurred with the 1,000 °C process [54]. The doped TiN served two purposes. One is the substantial EOT scaling via IL scavenging at the temperature between 400 and 600 °C. The other is the suppression of IL regrowth at the higher temperature. The IL scavenging reaction proceeds in a remote way as the oxygen vacancies in the HfO\(_2\) layer act as mediators for oxygen transport from the IL to the TiN electrode. However, the required thermal budget for remote-scavenging strongly depends on the choice of scavenging element.

Although IL scaling can provide performance improvement, extreme IL scaling (e.g., zero-IL) ends up with loss of EWF control both in gate-first/-last processes and with severe penalty in reliability. Therefore, the technique has to adjust the IL thickness to the optimum point where both performance and reliability requirements are satisfied.
2.3.3.3 Metal/dielectric interface deadlayer

Thin-film capacitors do not perform as well as electrostatic theory predicts. This dramatic drop in capacitance is traditionally attributed to the so-called “dead layer” effect [58]. The dead layer is thought to be as a low-permittivity thin layer at the metal/dielectric interface connected in series with the rest of the dielectric. Indeed early experimental works and subsequently many others have reported the effects of the disruptive dead-layer for nanometer sized films, as shown in Fig. 2.24 [58]. The effective capacitance \( C_{\text{eff}} \) of metal/dielectric/metal stack with regions of low interfacial capacitance density at the metal-dielectric interfacial layer (i.e. the dead layer) \( C_i \), connected in series with the nominal capacitance \( C_0 \) of the dielectric is typically expressed as:

\[
\frac{1}{C_{\text{eff}}} = \frac{1}{C_i} + \frac{1}{C_0} + \frac{1}{C_i}
\]

(14)

The interfacial capacitance \( C_i \) is taken as the additional capacitance introduced into the system due to the penetration of the electric field into the metal electrodes, while the nominal capacitance \( C_0 \) of the dielectric layer is that predicted by classical electrostatics.

The presence of this dead layer is attributed to a variety of reasons including a secondary low-permittivity phase at the surface of the films, nearby surface variation of polarization (field induced or spontaneous), presence of misfit dislocations, electric field penetration into the metal electrodes among others. In addition, the dead layer in thin films could arise from growth induced defects, strains and grain boundaries rather than from the intrinsic properties of the ideal interface [59]. Unfortunately, until very recently, the implications of experiments and modeling appeared to conflict with each other: most papers from modeling pointed out that the substantially better electronic screening
provided by elemental metals such as Pt should result in dead layer free capacitors; other papers suggested that the high ionic contributions to short-range polarizability provided by electrodes such as SrRuO$_3$ or RuO$_2$ should yield improved screening, supported by experiments.

*Ab initio* calculations by Stengel and Spaldin [59] on SrRuO$_3$/SrTiO$_3$/SrRuO$_3$ and Pt/SrTiO$_3$/Pt thin film capacitors with atomistically smooth interfaces (to exclude effects due to, e.g., misfit dislocations) have confirmed that electric field penetration occurs in real metal electrodes giving rise to a passive dead layer at the metal-dielectric interface. In the conventional picture of a capacitor, the electrode is an ideal metal and the electrical field inside the dielectric is perfectly screened. However, both experiments and *ab initio* simulations have shown that in real systems, screening of electric fields takes place over a finite spatial extent inside the metal. Because of the penetration of electric field into the metal, there is a potential drop inside the metal electrode which then introduces an additional capacitance into the system. Figure 2.25 shows the potential curve inside SrRuO$_3$/SrTiO$_3$/SrRuO$_3$, expected from classical electrostatics, compared with the curve obtained by using *ab initio* simulation. Typically, this effect is modeled by requiring the free charges in the electrode to form a layer of finite thickness at the metal-dielectric interface. When a free charge layer of finite thickness is assumed in the electrode, the center of charge in the electrode is separated by a finite distance from the polarization bound charge in the dielectric and an additional capacitance is introduced.
Figure 2.24 (a) Effective series capacitance structure formed from ferroelectric material plus its two surface dead layers, illustrating metal/dielectric/metal structure and (b) schematic behavior of $\varepsilon_{eff}$ as a function of film thickness [58]

Figure 2.25 Comparison of the potential profiles inside the SRO/STO/SRO capacitor system. Black curve is obtained by Stengel and Spaldin using ab initio techniques. Red curve is the potential expected from classical electrostatics. [59]

63
2.4 Reference


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III. Experiments and Analyses

In this section the main features of the experimental techniques are described. More detailed information can be found from the corresponding result section.

3.1 Atomic layer deposition of high-\(k\) dielectrics

The dielectric films were grown onto 2x2 cm\(^2\) substrates using a thermal atomic layer deposition (ALD) reactor (CN1 Corp., Suwon, Korea). Argon (Ar, purity 99.999\%) was used as a carrier and a purging gas. In most of the experiments the substrates were p-type silicon, but also Pt and Ge substrates were used.

Figure 3.1 shows schematic diagram of the thermal ALD system used in these experiments. The ALD system has traveling-type chamber and four precursors (or canisters) and ozone generator. With programming process sequence, four other precursors can be used independently for various dielectric films. Also, ozone generator can supply \(O_2\) gas with various ozone (O\(_3\)) concentrations from 0 to \(~300\) g/Nm\(^3\).

The reactants were evaporated from external canisters depending on the vapor pressure of sources. In case of hafnium (Hf) and zirconium (Zr) sources, because the vapor pressures are properly low at room temperature, these sources were heated at 60°C and carried by Ar gas. Silicon (Si) and aluminum (Al) sources were cooled at 5°C due to the high vapor pressure at room temperature and the evaporated source gases were traveled into the chamber. In this work, Hf and Si sources were only used for gate oxides in the MOS capacitor devices.
Figure 3.1 Schematic diagram of the thermal ALD system used in this work.
In this work, the HfO$_2$ and Hf$_x$Si$_{1-x}$O$_y$ (HfSiO) films were deposited directly on hydrofluoric acid (HF) cleaned Si wafers by ALD at a wafer temperature of 270 °C. Hf[N(C$_2$H$_5$)(CH$_3$)]$_4$ and SiH[N(CH$_3$)$_2$]$_3$ and ozone (typical concentration of 170 g/m$^3$) were used as the Hf-/Si- precursors and oxidant, respectively, in the deposition of the HfO$_2$ and HfSiO gate dielectric layers. The standard precursor pulse - precursor purge – ozone pulse – ozone purge time was 3 – 20 – 3 – 10 sec in HfO$_2$ and 3 – 15 – 3 – 10 in SiO$_2$, respectively, which was confirmed as within the well saturated ALD window. Physical and chemical properties of the two precursors are summarized in Table 3.1, and process conditions are summarized in Table 3.2.

<table>
<thead>
<tr>
<th>Chemical Formula</th>
<th>Hf precursor (TEMAHf)</th>
<th>Si precursor (tri-DMAS)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Hf[N(CH$_3$)$_2$H$_3$]$_4$</td>
<td>SiH[N(CH$_3$)$_2$]$_3$</td>
</tr>
<tr>
<td>Thermal decomposition</td>
<td>272 °C</td>
<td>N/A</td>
</tr>
<tr>
<td>Vapor pressure</td>
<td>0.23torr @ 60 °C</td>
<td>2.1torr @ 5 °C</td>
</tr>
<tr>
<td>Carrier gas</td>
<td>Ar</td>
<td>-</td>
</tr>
</tbody>
</table>

Table 3.1 Physical and chemical properties of TEMAHf and tri-DMAS.
### Table 3.2 Process conditions of thermal ALD grown HfO₂ and SiO₂

<table>
<thead>
<tr>
<th></th>
<th>HfO₂</th>
<th>SiO₂</th>
</tr>
</thead>
<tbody>
<tr>
<td>Metal precursor</td>
<td>Hf[N(CH₃)C₂H₅]₄</td>
<td>SiH[N(CH₃)₂]₃</td>
</tr>
<tr>
<td>Oxidant</td>
<td>Ozone (170 g/Nm³)</td>
<td></td>
</tr>
<tr>
<td>Growth temperature</td>
<td>270 °C</td>
<td></td>
</tr>
<tr>
<td>Carrier Ar flow rate</td>
<td>200 sccm</td>
<td>-</td>
</tr>
<tr>
<td>Canister temperature</td>
<td>60 °C</td>
<td>5 °C</td>
</tr>
<tr>
<td>Line temperature</td>
<td></td>
<td>90 °C</td>
</tr>
<tr>
<td>Feeding time</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Precursor pulse</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>Precursor purge</td>
<td>20</td>
<td>15</td>
</tr>
<tr>
<td>Ozone pulse</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>Ozone purge</td>
<td>10</td>
<td>10</td>
</tr>
</tbody>
</table>

Table 3.2 Process conditions of thermal ALD grown HfO₂ and SiO₂
3.2 Sputtering deposition of metal gates

Various metal films were deposited by dc and rf magnetron sputtering using a 5-angle cluster-type system (SN-38, SNTek Corp., Suwon, Korea). Figure 3.2 shows the sputtering equipment with 5-angle cluster system and the modified cathode to enhance the magnetic field at the target surface compared to the general type. As shown in Fig. 3.2 (c), installing the center and side magnets to the back-side of target and changing the magnets with higher magnetic field resulted in higher magnetic fields at the target surface than that of a general type. Also, the magnetic housing of the cathode was designed to maximize the magnetic field on the surface of the target and to minimize the distance between the center and edge magnets.

The deposition of metal films was performed on a rotational substrate in the sputtering module at room temperature. The distance between the substrate and the target was about 10 cm. Argon (Ar) gas was used as the sputtering gas. Nitrogen (N\textsubscript{2}) and oxygen (O\textsubscript{2}) gases were used for depositing nitride or oxide compounds. The base pressure before deposition was below 3×10\textsuperscript{-7} torr and the sputtering pressure was used from 1.6×10\textsuperscript{-2} torr to 4.0×10\textsuperscript{-3} torr.

In this work, the used metal films are Pt, TiN, La, poly-Si, and Ru (or RuO\textsubscript{2}) films, etc., which were deposited under detail condition in Table 3.3.
Figure 3.2 The sputtering system with 5-angle cluster module; (a) schematic diagram of sputtering equipments and (b) enhanced magnetic field structure of cathode (right) compared to the general type (left) and (c) schematic diagram of magnetic-field in quarter cathode system.
Table 3.3 Process conditions of sputtered various metal films in this work.

<table>
<thead>
<tr>
<th></th>
<th>Pt</th>
<th>TiN</th>
<th>La</th>
<th>RuO₂</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Target</strong></td>
<td>Pt (99.9%)</td>
<td>Ti (99.99%)</td>
<td>La (99.9%)</td>
<td>Ru (99.9%)</td>
</tr>
<tr>
<td><strong>Base Pressure</strong> (torr)</td>
<td></td>
<td></td>
<td></td>
<td>&lt;3.0×10⁻⁷</td>
</tr>
<tr>
<td><strong>Sputtering Pressure</strong> (torr)</td>
<td>1.6×10⁻²</td>
<td>4.0×10⁻³</td>
<td>4.0×10⁻³</td>
<td>1.5×10⁻²</td>
</tr>
<tr>
<td><strong>Sputtering Gas Flow</strong> (sccm)</td>
<td>Ar : 30</td>
<td>Ar : 20</td>
<td>Ar : 20</td>
<td>Ar : 30</td>
</tr>
<tr>
<td><strong>Reactant Gas Flow</strong> (sccm)</td>
<td>-</td>
<td>N₂ : 1.0</td>
<td>-</td>
<td>O₂ : 3.5 ~ 5.0</td>
</tr>
<tr>
<td><strong>Sputtering Power</strong> (W/cm²)</td>
<td>12 ~ 105</td>
<td>100</td>
<td>60</td>
<td>60</td>
</tr>
<tr>
<td><strong>Target-Substrate Distance</strong> (cm)</td>
<td></td>
<td></td>
<td></td>
<td>10</td>
</tr>
<tr>
<td><strong>Substrate Rotation Rate</strong> (rpm)</td>
<td></td>
<td></td>
<td></td>
<td>15</td>
</tr>
<tr>
<td><strong>Substrate Temperature</strong></td>
<td>Room Temperature</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
3.3 Film characterization

Dielectric film thicknesses on Si or Pt were determined at center area of the 2x2 cm$^2$ substrate using an ellipsometer (L116D, Gaertner Corp., US) with a single light source (633 nm) and spectroscopic ellipsometry (SE; M2000, Woollam Corp., US) with wide light source (193 ~ 1690 nm). The physical thicknesses of metal films including dielectric films were confirmed by the layer density and the vertical image of the films.

The layer density of the dielectric films as well as metal films was determined by X-ray fluorescence spectroscopy (XRF; Themoscientific, ARL Quant’x).

The chemical bonding states of the films were examined by X-ray photoelectron spectroscopy (XPS). The XPS measurements were carried out using a Kratos AXIS-HSi system equipped with a Mg K$\alpha$ source (1253.6eV) for the excitation of photoelectrons. The positions of all peaks were calibrated to the surface carbon C 1s peak at 284.5eV.

The atomic concentrations and depth profiles of the films were analyzed by Auger electron spectroscopy (AES). The AES measurements were carried out using a Perkin-Elmer PHI 660 system.

The crystalline structure of the films was examined by glancing angle incidence X-ray diffraction (GAXRD, PANalytical, X’pert Pro).

The microstructure and vertical image of the films was analyzed using a high-resolution transmission electron microscopy (HRTEM; Tecnai F20, field-emission, 200kV), Fast Fourier Transformation (FFT), and the electron energy loss spectroscopy (EELS ; GIF Tridiem 863).
3.4 Fabrication of MOS capacitor

Firstly, the high-\textit{k} gate dielectrics (HfO$_2$ or HfSiO) with various thicknesses films were deposited directly on hydrofluoric acid (HF)-cleaned Si wafers by ALD at a wafer temperature of 270°C. When thermal budget on the high-\textit{k} dielectrics was needed, post deposition annealing (PDA) was performed at various temperatures in a N$_2$ ambient using a rapid thermal annealing (RTA) process for 30 sec. Various top metal electrodes, such as platinum (Pt) and titanium nitride (TiN), were sputtered on the dielectric films using a shadow mask to define the gate electrodes. Finally, forming gas annealing (FGA) was performed in the mixture gas of N$_2$ (95%) and H$_2$ (5%) at 450°C for 10min.

Figure 3.3 shows the schematic diagram of a shadow mask and MOS capacitor used in this work. Various metal layers between Pt and gate oxide was in-situ inserted for investigating electrical property. Size of a dot deposited on samples using the shadow mask was about 90,000 ~ 100,000 um$^2$. 
Figure 3.3 Schematic diagram of (a) a shadow mask used in this work and (b) Pt electrode on the dielectrics and (c) other metal insertion between Pt and dielectrics on Si substrate and (d) scope image of a dot.
3.5 Fabrication of terraced oxide substrate

As mentioned in section 2.2.2.2, the terraced oxide method was proposed as a more accurate methodology for extracting the effective work function (EWF) with minimizing the several charge effects in bulk and interface. For the extraction of the method, the terraced SiO$_2$ substrates were necessary in this work. Firstly, thermal grown SiO$_2$ of 8nm thickness on p-type Si substrate was wet-etched gradually by dipping the sample (thermal SiO$_2$) into HF solution (20:1) and pulling slowly the sample from the solution. Figure 3.4 shows sequentially the terraced oxide sample preparation. After the gradual wet-etching, the thermal SiO$_2$ oxide layer became terraced (Fig. 3.4 (b)) and the measured remain oxide thicknesses of the samples were from 7nm at top to 1~10nm at bottom position, as shown in Fig. 3.4 (c). And HfO$_2$ gate dielectrics of thickness of ~ 3nm were deposited on the terraced SiO$_2$ substrates using ALD. Then, as explained in section 3.4, various metal gate stacks were deposited by sputtering. Fig. 3.4 (d) shows the final sample vertical diagram for the terraced SiO$_2$/HfO$_2$/metal gate stack.
Figure 3.4 Schematic diagram of preparing terraced oxide substrate and final sample structure; (a) sample wet-etching and (b) vertical diagram and (c) measured thermal SiO$_2$ thicknesses of several samples after wet-etching and (d) final sample diagram after metal electrode deposition.
3.6 Extraction of effective work function

The terraced SiO$_2$/HfO$_2$/metal gate stack as well as only terraced SiO$_2$/metal gate stack was used for extracting EWF. Figure 3.5 (a) shows example for C-V curves measured from the terraced SiO$_2$/metal electrode stack, in which capacitance density values increased with measuring from top to bottom position of sample due to the decrease of gate oxide thickness. From the C-V curves, EOT values can be calculated by considering any quantum mechanical (QM) effects (0.3~0.4nm) from CET (calculated from the maximum capacitance value) and flat band voltages ($V_{FB}$) can be computed from the NCSU CVC program. $V_{FB}$ versus EOT (or CET) values, extracted from C-V curves (Fig. 3.5 (a)), were plotted as Fig. 3.5 (b).

In plot of $V_{FB}$ vs. EOT, the EWF from the y-intercept and fixed charges in the stack from the slope can be extracted (see section 2.2.2.2). As explained in section 2.2.2.1, EWF of metal electrode is “EWF(eV) = $\phi_{ms}+5.1$” for p-type Si substrate because the y-intercept is $\phi_{ms}$ value and the fixed charges are “$Q_{oxide} = -slope*3.9*\varepsilon_o$” because the slope is $slope = \frac{Q_{oxide}}{\varepsilon_{SiO_2}}$ from equation (10).

Also, EWF on SiO$_2$ from the terraced SiO$_2$/metal electrode stack and EWF on HfO$_2$ from the terraced SiO$_2$/HfO$_2$/metal electrode stack were extracted. In case of Pt electrode, EWF was 5.5eV on SiO$_2$ and 5.0eV on HfO$_2$, where the drop of EWF on HfO$_2$ was due to the Fermi level pinning (see section 2.3.1). Also, $V_{FB}$ roll-off phenomenon was shown in t-SiO$_2$/HfO$_2$/Pt stack.
Figure 3.5 (a) C-V curves measured from a terraced oxide sample and (b) flat band voltage ($V_{FB}$) versus EOT plot of Pt electrode from only terraced SiO$_2$ sample and terraced SiO$_2$/HfO$_2$ stack sample.
3.7 Electrical measurements

A HP 4194A Impedance/Gain-Phase Analyzer for Capacitance-Voltage (C-V) curve and a HP 4140B pA Meter/DC Voltage Source for I-V characterization were used in the MOS capacitor devices.

Bias temperature instability (BTI) and Interface trap density (D_{it}) from the MOS capacitor are also measured by using a Hewlett-Packard (HP) 4155 semiconductor parameter analyzer and a HP 4284 LCR meter system. The measurement system and schematics of BTI and D_{it} measurement in MOS capacitor devices were illustrated in Figure 3.6 and 3.7. During the BTI measurements, a constant voltage (or field) stress was applied to the gate of MOS capacitor, while the Si substrate was grounded. The gate voltage (V_g) was swept from -1 to 1 V at 1,3,5,10,22,47,100,216,465,500sec during 500sec at 100 kHz for measuring C-V. However, the inversion condition can hardly be achieved from the usual MOSCAP device due to the lack of source and drain, so the depletion/accumulation condition must be used to evaluate the BTI characteristics. Therefore, V_{FB} values extracted from the C-V curves after gate bias stress were used instead of V_t values in MOSFET.
Figure 3.6 BTI and Dit measurement system in these experiments

Figure 3.7 Schematic diagram of BTI and Dit measurement in MOS capacitor devices.
IV. Results and Discussions

In this chapter the results of the Hf-silicate dielectrics and various metal gates reported by the author are described. In addition to the published papers, more detailed results are included in this chapter.

4.1 Hf-silicate (HfxSi1-xOy) grown by ALD

4.1.1 Introduction

One of the key methods to enable transistor channel length scaling in complementary metal-oxide-semiconductor field effect transistors (CMOSFETs) is to scale the gate dielectrics. However, with this method, scaling slows down at the 90 nm node as SiO$_2$ runs out of atoms and further scaling of the gate-leakage current is limited [1]. To decrease the gate leakage in highly scaled transistors, Hf and Zr-based high-$k$ gate dielectrics have been considered to be the most promising candidates to replace SiO$_2$ gate dielectrics [2-4]. Hf-based high-$k$ gate dielectrics have already been employed in the current technology node [5]. Hf$_{1-x}$Si$_x$O$_y$ (HfSiO) gate dielectrics as an alternative to HfO$_2$ have advantages such as increased crystallization temperature [6], reduced growth of the interfacial oxide layer at the silicon/high-$k$ interface [7], and higher band gap [8].

Recently, two basic approaches were introduced for the integration of gate stacks using high-$k$ gate dielectrics and a metal gate electrode: a gate-first approach [9] and a gate-last approach [10]. In the gate-first approach, the high-$k$ gate dielectrics need to have high
thermal stability, because of the formation of the gate stack before activation annealing of
the source and drain, as in a conventional CMOSFET process. Therefore, Hf-silicate film
would be a suitable candidate for the gate-first process, because of its high thermal
stability as well as its process maturation. In gate-last approach, the thermal stability of
the gate dielectric is not crucial.

The incorporated Si in HfO₂ films does not only increase the crystallization
temperature but also changes the crystalline phase [11-13]. A certain concentration of Si
in HfSiO film induced the crystalline phase transformation of the film from monoclinic to
tetragonal, over which the sacrifice of the permittivity was observed [14]. The tetragonal
phase has a higher permittivity than that of monoclinic phase, so that achieving the
tetragonal phase is desirable. Optimization of the post-deposition annealing (PDA)
temperature for crystallization of the film is crucial, as much as that of Si concentration in
the film for tetragonal phase formation, because high-temperature annealing induces Si
diffusion from a substrate into the film and an interfacial layer growth, which would
deteriorate the overall permittivity of the film [15].

Therefore, in this study, the PDA temperature for phase transformation of atomic layer
deposited HfSiO film with various Si concentrations was systematically examined and
optimized. Although there have been many reports on the structural and electrical changes
in the HfSiO film with the PDA process, the detailed study on the structural evolution of
the film and accompanying dielectric properties depending on the Si concentration has
not been reported. In addition, the analysis data for the relevant thickness range (<< 10
nm) is quite rare. In this study, therefore, the changes in the microstructure of HfSiO film
with various annealing temperatures and Si concentrations were traced by high-resolution
transmission electron microscopy (HRTEM), and the electrical properties of the various films were also examined.

4.1.2 Experimental

HfSiO films were deposited on HF cleaned p-type Si (100) substrates by atomic layer deposition (ALD) at a wafer temperature of 270°C. The Si/(Hf+Si) concentration in the HfSiO film was controlled from 14% to 81%. The ALD grown HfO₂ and SiO₂ films were also included as references to compare their properties with HfSiO films. The physical thicknesses of various HfSiO films measured by ellipsometry were ~10 nm and ~3–8 nm for physical and electrical analysis, respectively. PDA was performed by rapid thermal process (RTP) at temperatures ranging from 400 to 1000°C under N₂ atmosphere for 30 sec. A circular shape 80-nm-thick Pt top electrode with a 300 um diameter was deposited though metal shadow mask by dc magnetron sputtering to fabricate metal-insulator-semiconductor (MIS) capacitors for electrical measurements. Capacitance-voltage (C-V) and gate-leakage current density-voltage (Jᵥ-V) characteristics were examined using a Hewlett-Packard 4194A Impedance/Gain-Phase analyzer and a Hewlett-Packard 4140B pA meter/dc voltage source, respectively. The capacitance equivalent thickness (CET) was calculated from the accumulation capacitance in the measure C-V curves at a frequency of 100 kHz with a voltage sweep range from -2.5 to +2.5 V. The chemical bonding states in the HfSiO films with various Si/(Hf+Si) ratios were examined by x-ray photoelectron spectroscopy (XPS; AXIS-His). The crystallinity of the HfSiO films was estimated by a glancing angle x-ray diffraction (GAXRD, PANalytical X’Pert PRO
MPD), and the microstructure of the films was analyzed using a HRTEM (Tecnai F20, field-emission, 200kV), Fast Fourier Transformation (FFT), and the electron energy loss spectroscopy (EELS ; GIF Tridiem 863).

### 4.1.3 Growth and Physical properties

#### 4.1.3.1 ALD growth of HfSiO

HfSiO films were deposited on HF cleaned p-type Si (100) substrates by atomic layer deposition (ALD) at a wafer temperature of 270°C, using Tetrakis[EthylMethylAmino] Hafnium (Hf[N(CH3)(C2H5)]4) and Tris(DiMethylAmino) Silane(SiH[N(CH3)2]3) as precursors and ozone gas (concentration of 170 gm⁻³) as the oxygen source. The ALD grown HfO2 and SiO2 films were also included as references to compare their properties with HfSiO films. Figure 4.1 (a) and (b) show the well-saturated ALD growth of HfO2 and SiO2, respectively. Growth rate of HfO2 and SiO2 was saturated to 0.12 nm/cycle and 0.072 nm/cycle, respectively, when the precursor pulse/purge/ozone pulse/purge times for the HfO2 and SiO2 films were 3/20/3/10 s and 3/15/3/10 s, respectively.

The HfSiO films were deposited by the appropriate control of the cycle ratio of HfO2 and SiO2 film growth processes. Figure 4.2(a) shows the ALD super-cycle schematic for HfSiO film, which consists of a HfO2 sub-cycle and a SiO2 sub-cycle. The composition of Si/(Hf+Si) in HfSiO films was controlled using the number of HfO2 and SiO2 sub-cycles in a super-cycle. The sub-cycle ratio of the SiO2 sub-cycle to the HfO2 sub-cycle was controlled from 3:1 to 1:9 which corresponds to the Si/(Hf+Si) feeding ratio from 0.75 to 0.1, as shown in Fig. 4.2(b).
Figure 4.1 Plots of thickness and growth rate as a function of cycle and schematic diagrams of cycle of (a) HfO$_2$ and (b) SiO$_2$. 

- **(a) HfO$_2$**
  - G/R (Å/cycle) : 1.2

- **(b) SiO$_2$**
  - G/R (Å/cycle) : 0.72
Figure 4.2 (a) Schematic diagram of ALD super-cycle of Hf$_x$Si$_{1-x}$O$_y$ (HfSiO) film consisting of HfO$_2$ and SiO$_2$ sub-cycle and (b) sample preparation condition in this work.
The growth rate per a super-cycle of HfSiO film is comparable with the summation of component sub-cycle growth rate, which is $0.12 \times \text{HfO}_2$ sub-cycle number + $0.072 \times \text{SiO}_2$ sub-cycle number. For examples, the growth rate per a super-cycle of HfSiO films with Si:Hf feeding ratio of 0.75 (3:1), 0.5 (1:1), and 0.125 (1:7) was 0.35 nm, 0.2 nm, and 0.91 nm, respectively. Figure 4.3 shows that the real growth rate per a super-cycle of HfSiO film with Si:Hf feeding ratio of 3:1, 1:1, 1:3, and 1:7 was 0.35 nm, 0.2nm, 0.45nm, and 0.91nm, respectively, which were well coincident with the expected summation of component sub-cycle growth rate. In addition, each the calculated growth rate and calculated source feeding ratio ($\text{Si}/(\text{Hf}+\text{Si})$) for various combinations of sub-cycles had good linearity with the real growth rate (see Fig. 4.3) and real atomic ratio ($\text{Si}/(\text{Hf}+\text{Si})$) extracted from XPS peak area ratio, as shown in Fig. 4.4.

These results mean the growth behavior of HfO$_2$ and SiO$_2$ sub-cycles are maintained in the HfSiO super-cycles. In other words, the growth of Hf-O layer on Si-O terminating surface is almost identical to that on the Hf-O surface itself, and growth of Si-O layer on Hf-O terminating surface is almost identical to that on the Si-O surface itself.
Figure 4.3 The growth rate and thickness as a function of a super-cycle of HfSiO film with Si:Hf feeding ratio of (a) 3:1, (b) 1:1, (c) 1:3, and (d) 1:7.
Figure 4.4 Correlation graphs (a) between calculated growth rate and real growth rate of super cycles and (b) between the source feeding ratio, calculated by sub-cycle feeding number, and the atomic ratio, estimated from XPS peak area ratio of Hf 4f and Si 2p.
4.1.3.2 Physical properties of HfSiO

Figure 4.5 (a) and (b) shows Hf 4f and Si 2p core levels XPS spectra, respectively, for as-deposited HfO$_2$, SiO$_2$, and HfSiO films with various Si concentrations. The binding energy of all peaks has been calibrated by centering the carbon 1s peak at 284.5 eV. In Fig. 4.5(a), HfO$_2$ (top black line) shows a sharp doublet according to spin-orbital splitting into Hf 4f$_{5/2}$ and Hf 4f$_{7/2}$ peaks with binding energies of 18.2 eV and 16.6 eV, respectively, which is consistent with the data reported previously [16]. In general, as the Si concentration in HfSiO increases, the Hf 4f peak position gradually shifts to higher binding energy direction with the distortion of the peak shape. This is because the increased Si-O bonds in the film affect the Hf-O bonding characteristics [17].

Figure 4.5(b) shows the Si 2p core level XPS spectra of the same samples shown in Fig. 4.5(a). The binding energy of the Si 2p peak of HfSiO increased with increasing Si concentrations, from 101.7 eV (HfSiO with a Si concentration of 16%) to 103.2 eV (ALD grown SiO$_2$), which is consistent with the previous report that Si-O bonding energy in SiO$_2$ shifts to lower energy because of the change of Si’s second nearest neighbor from Si to Hf [17,18]. The XPS data shown in Fig. 4.5 reveal that the Hf, Si and O ions in the as-deposited films are homogeneously mixed.

When the HfSiO films with Si:Hf ratio of 1:7 (Si 16%) were annealed at 800°C and 1000°C, the Hf 4f peak position gradually shifts to higher binding energy direction like as if Si concentration in HfSiO were increased and the Si 2p peak position also shifts to higher binding energy direction with the increase of the peak intensity, as shown in Fig. 4.6. This result indicated that the post deposition annealing (PDA) causes the Si atoms to diffuse from Si substrate into HfSiO film.
Figure 4.5 (a) Hf 4f and (b) Si 2p core level XPS spectra for HfSiO films with Si:Hf ratio of 1:7 (Si 16%) to 3:1 (Si 81%), including ALD grown HfO2 and SiO2.

Figure 4.6 (a) Hf 4f and (b) Si 2p core level XPS spectra for HfSiO films with Si:Hf ratio of 1:7 (Si 16%) after PDA (800°C and 1000°C) including as-deposited HfO2.
For analyzing impurities and Hf/Si atomic concentrations, the HfSiO films with various Si compositions were investigated by AES. Figure 4.7 shows the AES depth profiles of as-deposited HfSiO films with Si:Hf ratio of 1:7 (Si 16%), 1:5 (Si 20%), 1:3 (Si 33%), and 1:1 (Si 57%). Low residual carbon was detected in HfSiO films with various Si compositions. Also, in terms of Si/(Hf+Si) ratio, identical results to the XPS analysis are confirmed.

The effect of the thermal budget on the degree and phase of crystallization was examined by using X-ray diffraction (XRD) as shown in Fig. 4.8. After depositing HfSiO films with various Si compositions, PDA was performed from 400°C to 1000°C. As-deposited HfO₂ as well as HfSiO films with high Hf compositions show broad XRD peaks. The films seem to crystallize partially due to the thick thickness of 15 nm. In the case of HfO₂, after annealing at 400°C, clear XRD peaks, corresponding to the monoclinic phase, are observed [12]. In the as-deposited HfSiO films, no significant XRD peaks were observed irrespective of Si composition, and this was also the case for all HfSiO films until the annealing temperature reached to 600°C, suggesting all films were amorphous. After annealing at 700°C, HfSiO films with very low Si composition shows clear XRD peaks that correspond to the tetragonal phase [12]. After annealing at 1000°C, HfSiO films with high Si composition (over 80% Si) were still amorphous. This suggests that the incorporation of a small amount of Si can not only induces the transformation of microstructure from the monoclinic phase to the tetragonal phase, but also increases the crystallization temperature. It was reported that such transformations into the tetragonal phase (approximately 10% of Si/(Hf+Si)) induced higher dielectric constants in metal-insulator-metal (MIM) structures with HfSiO insulators [12].
Figure 4.7 AES depth profiles of as-deposited HfSiO films with Si:Hf ratio of (a) 1:7 (Si 16%), (b) 1:5 (Si 20%), (c) 1:3 (Si 33%), and (d) 1:1 (Si 57%). Film thicknesses are almost 15nm.
Figure 4.8 XRD spectra of HfSiO films with Si:Hf ratio of 1:9 (Si 14%) to 3:1 (Si 81%) including SiO₂ and HfO₂ films as a function of PDA temperature from 400°C to 1000°C.
4.1.4 Dielectric constant and insulating properties of ALD Hf-Silicate

Figure 4.9 (a) shows the variation of permittivity of as-deposited HfO₂, SiO₂, and HfSiO films as a function of the Si concentration. The permittivity was extracted by dividing 3.9 by the slope of the CET vs. thickness plot as shown in Fig. 4.9 (b), which excludes the influence of the interfacial layer. The Si incorporation into the film led to lower permittivity.

However, the change in the permittivity of HfSiO films after PDA depends on the Si concentration in the film, as shown in Fig. 4.10 (a). Here, the permittivity was also calculated from the slope of the CET vs. thickness curves, one example of which is also included in Fig. 4.10 (b) for the HfSiO films with a Si concentration of 16%. The as-deposited HfO₂ film in this thickness range was amorphous (Fig. 4.10 (c)) and has a bulk permittivity of 17.5. After the PDA at 700 and 800 °C, the HfO₂ film crystallized into a monoclinic phase, as shown in Fig. 4.10 (d), which was evidenced by the inset FFT pattern. The permittivity was slightly decreased to 14 due to the Si diffusion from a substrate into the film during PDA, which was explained in Fig. 4.6. It must be noted that the Si-diffusion from the substrate does not induce the phase transformation of HfO₂ phase from monoclinic to tetragonal. This suggests that the diffused Si atoms from the substrate do not diffused into the crystallizing grains of HfO₂. However, the situation is quite different when the crystallization proceeds from the HfSiO film as shown below.

In the case of HfSiO with a Si concentration of 16%, although the permittivity of the as-deposited film was quite low (~11), the permittivity of the film increased two times compared to that of as-deposited film after PDA at 800°C (~ 21) as shown in Fig. 4.10 (a).
Figure 4.9 (a) The permittivity of as-deposited HfSiO films as a function of Si concentrations and (b) the inverse slope of the EOT vs. physical thickness for as-deposited HfSiO film with Si 16%, 57%, and 80% including HfO$_2$. The dielectric constants are extracted from 3.9 divided by slope.
Figure 4.10 (a) The permittivity changing as a function of PDA temperatures for HfO$_2$ and HfSiO films with Hf:Si ratio of 1:1 (Si 57%) and 1:7 (Si 16%). For the evaluation of permittivity, (b) the inverse slope of the CET vs. physical thickness for HfSiO film with Si 16% before and after PDA (800°C), and TEM images and FFT pattern of HfO$_2$ (c) before and (d) after PDA (700°C).
This is attributed to the tetragonal phase formation in the film by PDA at 800°C. It is believed that the presence of SiO$_2$ component in the as-deposited film induced the crystallization of the HfSiO film with the tetragonal phase. Interestingly, the permittivity of HfSiO film with a Si concentration of 16% decreased after PDA above 900°C. This could be induced by the transformation from tetragonal to monoclinic of the separated HfO$_2$ phase. This was confirmed by HRTEM result in Fig. 4.11 that shows the typical HRTEM micrographs of HfSiO film with a Si concentration of 16% after PDA at (a) 800°C and (b) 1000°C. Although it is not clearly resolved in those figures, the crystallized films show segregation of phases into several crystalline phases, and each phase was identified using the FFT technique. The change in the phase ratio in the film as a function of PDA temperature was summarized in Fig. 4.11 (c), where the phase information of the film was randomly collected from more than 30 points from the HRTEM images. Here, the “unclear” region corresponds to the crystallized part but unequivocal identification of phase is not possible perhaps due to the overlapping lattice images. After the PDA at temperatures higher than 800°C, the films were almost fully crystallized, but the distribution of the phase varies with the PDA temperature. While the tetragonal phase ratio in the film decreased, the monoclinic phase ratio in the film increased with an increased PDA temperature. This can be understood from the following. The metastable amorphous HfSiO film crystallizes with separated phases of Hf-rich and Si-rich regions, which must be more amorphous-like structure, during the PDA. It is believed that the tetragonal phase formation, which is induced with the help of a certain amount of Si incorporated in the film (~10–20%) [12], was disturbed by the deficiency of Si in the film because of the severe phase separation of the film into SiO$_2$ (mainly consisted of SiO$_2$)
Figure 4.11. TEM micrographs and FFT patterns of about 7-nm-thick HfSiO films with Si concentration of 16% after PDA at (a) 800°C and (b) 1000°C for 30 s in N₂ atmosphere and (c) the phase ratio of both films analyzed from randomly selected 30 points by FFT and (d) EELS mapping image of Si of the film after 1000°C for 30 s in N₂ atmosphere.
and HfO₂ (mainly consisted of HfO₂) after PDA above 900°C. The phase separation of the film after PDA at 1000°C is rarely observed in the HRTEM image of Fig. 4.11 (b), due to the overlap of crystalline image with amorphous-like image. However, the EELS mapping image of the Si of the HfSiO film after PDA at 1000°C in Fig. 4.11 (d) confirmed that the separated SiO₂ phase segregated at the film surface and partially in the film, which is indicated by white region in the figure [11]. The enhanced Si diffusion from the substrate into the film also contributed to the decreased permittivity of the film.

In the case of HfSiO film with the Si concentration of 57%, the permittivity of the film remained at the low value (~ 8) up to the PDA temperature of 800 °C, due to the retained amorphous structure (Fig. 4.12 (a)), but increased at the PDA temperature of 1000°C. It is notable that the permittivity of the film with such a high Si concentration (57%) is comparable to that of the film with the lower Si concentration (16%) after the PDA at 1000°C. This can be understood from the composition of formed phases at that temperature as shown in Fig. 4.12. The XRD patterns of the HfSiO film with Si concentration of ~57% before and after PDA at various temperatures in Fig. 4.12 (a) show that the crystalline temperature of the film reached to 1000°C (although the nanocrystalline structure might be formed below 1000°C). The HRTEM micrograph of the film with FFT images [Fig. 4.12 (b)] and the phase ratio in the film [Fig. 4.12 (c)] show that the portion of tetragonal phase in the HfSiO film with Si concentration of 57% after PDA at 1000°C (~50%) is higher than that of the film with Si concentration of 16% (~35%). Figure 4.12 (b) clearly shows the separated crystalline phases with remaining amorphous parts due to the higher Si concentration. This is due to that the remaining Si concentration in the separated (mostly) HfO₂ phase is higher compared to the other case.
because of the originally higher Si concentration. Then, this higher Si concentration in the HfO₂ phase retains the tetragonal phase more efficiently. PDA at an even higher temperature, over 1000°C, of the film might induce the decrease in the permittivity, because the further reduction of Si concentration in the separated HfO₂ phase (further phase separation) would enhance more monoclinic phase formation. However, this cannot be confirmed experimentally owing to the limited temperature condition for the RTP system (max. 1000 °C) used in this study.

Figure 4.13 shows the plot of Jₚ vs. CET of the HfO₂ and HfSiO films with various Si concentrations before and after PDA at 800, 900, and 1000°C. Simulation result for HfO₂ film indicated by a dash line and experimental result for pure SiO₂ film were also included for comparison [19]. The insulating property of the as-deposited films degrades with increasing Si concentration because of the low permittivity of SiO₂, as shown in Fig. 4.13 (a). However, the insulating property of HfO₂ film drastically degrades after PDA at temperatures higher than 800 °C which is worse than even that of HfSiO film with a Si concentration of 57% [Fig. 4.13 (b)]. In contrast, HfSiO film with a Si concentration of 16% keeps the promising insulating property after PDA up to 900°C [Fig. 4.13 (c)]. HfSiO film with a Si concentration of 57% also has promising thermal stability, but the CET is generally large because of a high Si concentration. After PDA at 1000°C, the result for HfO₂ film is hard to obtain because the Jₚ of HfO₂ film is too large to achieve the stable C-V curves. Both HfSiO films with a Si concentration of 16 and 57% also degrade severely, to a similar level, after PDA at 1000°C [Fig. 4.13 (d)]. The insulating property of HfSiO film with a Si concentration of 16% seems to degrade more abruptly with increasing PDA temperature, which is attributed to the decreased permittivity of the
film after PDA over 800°C. Nevertheless, it should be noted that HfSiO film with a Si concentration of 16% showed superior electrical performance up to 900 °C.

Figure 4.11. (a) XRD patterns of HfSiOx films with Si concentration of 57% after PDA from 400°C to 1000°C for 30 s under N2 atmosphere, (b) TEM micrographs and (inset) FFT patterns, and (c) the phase ratio of the film after PDA 1000°C for 30 s.
Figure 4.13 Plot of CET vs. $J_g$ for (a) as-deposited HfO$_2$ and HfSiO films with various Si concentrations, and annealed HfO$_2$ and HfSiO films with a Si concentration of 16% and 57% at (b) 800°C, (c) 900°C, and (d) 1000°C 30 s (Simulation result for HfO$_2$ is indicated by a dashed line).
4.1.5 Conclusion

The relation between the permittivity and the micro structures of atomic layer deposited HfSiO films with various Si concentrations as a function of PDA temperature was systematically examined using MIS capacitor and HRTEM analysis. The permittivity of the crystallized HfSiO films with a Si concentration of ~16% abruptly increased after PDA at 800°C, because of tetragonal phase formation with the help of an appropriate amount of Si in the film. However, it decreased after PDA at 1000°C, because the crystallization proceeds with higher proportion of monoclinic HfO\textsubscript{2} phase due to more severe segregation of Si into the SiO\textsubscript{2} phase. In contrast, the permittivity of HfSiO films with a Si concentration of ~57% increased considerably after PDA at 1000°C, because an appropriate Si concentration remained in the separated HfO\textsubscript{2} to form the tetragonal phase due to the initially high Si concentration. The electrical measurement showed that an optimized Si concentration (~ 16%) in the HfSiO film maintained promising electrical properties up to 900 °C. However, the PDA at 1000°C degraded the electrical performance severely irrespective of the Si concentration.
4.2 Gate engineering using La-incorporated TiN metal gates

4.2.1 Introduction

Metal gates have already been implemented in the complementary metal insulator semiconductor (MIS) field effect transistors with high-\(k\) gate dielectrics because of several issues such as poly-Si gate depletion, boron penetration and high gate resistance [3]. However, the effective work function (EWF) of these metal gates cannot be modulated by doping, which is necessary to adjust the threshold voltage of the transistors to appropriate values. Therefore, various gate materials and integration schemes for n/p-MIS devices are being studied for next generation transistors. These include approaches that introduce capping layers, such as La\(_2\)O\(_3\) (for NMOS) and Al\(_2\)O\(_3\) (for PMOS), on the high-\(k\) dielectrics to modulate flat band voltage (\(V_{FB}\)), and those that employ multi-layer metals to modulate the EWF of gate metal [20-22]. However, the use of capping layer has several unintended degradations such as the increase of equivalent oxide thickness (EOT) and mobility reduction due to the working of scattering centers. The multi-layer metal gate approach has several merits over the others such as lower process temperatures and scaling of the interfacial layer (IL) by the scavenging effect, which are both crucial for the gate last approach under the 28nm technology node. Therefore, in this study, the potential of lanthanum (La) insertion into TiN based metal gates was evaluated in two different configurations: the multi-layer TiN/La/TiN (TLT) structure and alloyed TiLaN (TLN). Their performance is evaluated in terms of flat band (\(V_{FB}\)) modulation and IL reduction in the MIS structure.
4.2.2 Experimental

Atomic layer deposited (ALD) HfO$_2$ films were grown on a p-type Si substrate at 270 °C using tetrakis[ethylmethylamino] hafnium (Hf[N(CH$_3$)(C$_2$H$_5$)]$_4$) and ozone gas with a concentration of 170 g/Nm$^3$ as the Hf precursor and oxygen source, respectively. The TLT metal gate consists of bottom TiN (2 ~ 10 nm), middle La (~5 nm), and top TiN (2 ~ 10 nm) layers. The equally sputtered bottom and top TiN films were grown at a dc power of 100 W using a 5 % N$_2$/(Ar + N$_2$) reactive gas. The inserted La metal layer was grown at an rf power of 60 W using a pure La metal target (~99.9 %). The TLN metal gate was prepared by reactive co-sputtering using Ti and La metal targets in a 5 % N$_2$/(Ar + N$_2$) gas ambient. The La concentration [La/(Ti + La)] was controlled by varying the rf power applied to the La target from 20 W to 60 W at a fixed dc power of 100 W for the Ti target. In-situ sputtered Pt (~80 nm) was grown on top of both TLT and TLN gates for stable electrical measurements. All metal layers were patterned through a shadow mask and electrode dimensions were estimated by optical microscopy. The EWFs of the various metal gates on SiO$_2$ and HfO$_2$ were extracted from terraced samples [23]. Post deposition annealing (PDA) was performed at 600 °C for 30s in a N$_2$ atmosphere by a rapid thermal annealing process. All MIS capacitors were then subjected to forming gas (5 % H$_2$/95 % N$_2$) annealing at 400 °C for 30 min. The atomic concentrations and structure profiles of the films were analyzed by Auger electron spectroscopy (AES) and high-resolution transmission electron microscopy (HRTEM). The chemical binding states of the films were examined by X-ray photoelectron spectroscopy (XPS). For the AES and XPS analyses, in-situ sputtered Si layers (10~25 nm) were grown on the metal layers to minimize oxidation during air exposure. The Si layer was in-situ etched out using Ar$^+$.
sputtering with low power prior to the analyzing the region of interest in the AES and XPS chambers. Capacitance-Voltage (C-V) characteristics were examined using a HP 4194A at 500 kHz. The measured C-V curves were simulated using Hauser’s CVC program to obtain the $V_{FB}$ and EOT values [24].

### 4.2.2.1 Pt electrode setup

Before various metal electrodes deposited using sputtering method were investigated in this work, the first setup of stable platinum (Pt) electrode, used generally as noble gate electrode, was necessary for stable electrical measurements. Pt films were grown at a dc power from 5 to 100 W using Ar gas. Figure 4.14 (a) shows the resistivity and deposition rate of Pt films as a function of Pt target power. The resistivity was saturated to about 25 $\mu$-ohm-cm, while the deposition rate of the film increased continuously with the target power increasing. However, MOS capacitors using Pt electrodes deposited at various target powers on thermal SiO$_2$ gate oxide (3nm) showed various C-V characteristics, which were from bad to good as shown in Fig. 4.14 (b). C-V curves became deteriorated as the target power increased as well as the process pressure of deposition decreased. This means Pt atoms with heavy atomic mass (~ 195 g/mol) collided more strongly on the SiO$_2$ surface under the high target power and the low process pressure. Figure 4.14 (c) shows the high plasma voltage for generating same plasma power (voltage x current) with decreasing the process pressure. Therefore, Pt electrodes in this work were deposited at 1.6x10$^{-2}$torr (high process pressure) and through 4-step power, as shown in Fig. 4.14 (d).
Figure 4.14 (a) Plot of the resistivity and deposition rate of Pt films as a function of Pt target power and (b) C-V curves under various deposition conditions and (c) dc plasma current vs. voltage correlation with various process pressures, and (d) final Pt deposition condition.
4.2.2.2 TiN electrode setup

For the TiN metal electrode setup, various process conditions such as process pressure and N2 flow rate, etc. were investigated using a dc sputtering of Ti target (99.999%). Firstly, the resistivity of TiN films as a function of process pressure was shown in Fig. 4.15 (a), with fixing a power of 200W and N2 flow of 1.0 sccm (a 5 % N2/(Ar + N2)). Also, the resistivity of TiN films decreased with decreasing N2 flow rate and increasing Ti target power because of becoming Ti-rich TiN film and high density TiN film, respectively, as shown in Fig. 4.15 (b) and inset. However, as mentioned above, high plasma power and low process pressure could deteriorate C-V characteristic. To obtain TiN films with proper resistivity and low damage, the target power and process pressure were optimized under a 5 % N2/(Ar + N2), in which the stoichiometry of TiN film was Ti : N of almost 1:1.

Thickness of TiN films deposited at a fixed dc power of 100 W for the Ti target and a process pressure of 4.0X10^-3 torr was controlled by sputtering time. Figure 4.15 (c) shows the C-V curves of MOS capacitors consisting of TiN metal gates with various thicknesses from 1nm to 20nm on thermal SiO2 gate oxide. Changes in V_{FB} are observed due to EWF changes. Also, similar values of V_{FB} are obtained for a TiN thickness of between 3 and 20 nm. No variation has been also observed for thicker TiN films. Extracted from thermal SiO2 with various thicknesses, EWFs of TiN films were almost same value (~ 4.5eV) above 3nm thickness of TiN film, as shown in Fig. 4.15 (d), which was coincident with the result of CV curves. The optimized TiN film of 3 nm thickness was sufficient to determine the flatband voltage and the EWF of the MOS capacitor.
Figure 4.15 (a) The resistivity of TiN films as a function of (a) process pressure and (b) N₂ flow rate and (inset) target power, and the C-V curves of TiN/SiO₂/Si capacitors with various TiN thicknesses and EWF of TiN films as a function of TiN thickness, extracted from thermal SiO₂ with various thicknesses.
4.2.2.3 Pre-evaluation for selecting materials as oxygen scavenger

Firstly, the negative free energies for oxide formation of the transition metals such as Hf, Ti, and La were compared with that of Si in Fig. 2.6. Since the scavenging effect, where metal ions take oxygen from the interfacial layer (IL) and decrease the overall thickness, is more accelerated when the negative energy becomes higher, La metal having a higher negative free energy and Ti metal having a similar energy as that of SiO\textsubscript{2} formation were selected for a comparison in this work. In addition, La metal with low work function (WF) of 3.5 eV and Ti metal with that of 4.33 eV were also selected for the comparison of WF modulation ability.

Figure 4.16 (a) shows TEM images of as-deposited transition metals on HfO\textsubscript{2} to confirm the scavenging effect. For the substantive investigation, the thick transition metals including the TiN single layer and no metal layer were also examined by depositing directly on HfO\textsubscript{2} dielectrics. After deposition of various metal layers on HfO\textsubscript{2}, the IL thicknesses were measured from TEM images. As mentioned above, the scaling amount of IL thickness through the scavenging effect (Fig. 4.16 (b)) was well coincident with the negative free energies for oxide formation of the metals, as shown in Fig. 4.16 (c). In case of La layer on HfO\textsubscript{2}, the IL thickness decreased from 2 nm to ~ 0.5 nm even though there was no additional annealing, while 1.0 – 1.5 nm thick IL remained for the Ti and TiN metals.

In this work, the effects of inserting the metal layers (Ti, La) into TiN metal gate as well as cosputtered the TiLaN metal gate on the decrease of IL thickness as well as the modulation of effective work function (EWF) were investigated.
Figure 4.16 (a) TEM images of no metal, TiN, Ti and La metal layers on HfO₂ and (b) schematic diagram of scavenging effect of metal/HfO₂/Si stack and (c) plot of interfacial layer (IL) thicknesses from TEM images and Gibbs free energies of each metal layers.
4.2.2.4 Pre-evaluation for site selection of La metal layer

It was confirmed whether La atoms diffuse or not from La-incorporated TiN metal gates to top and bottom of HfO$_2$ dielectrics to cause $V_{FB}$ shift. It was also for confirming how the La capping layers upper and under HfO$_2$ affect the $V_{FB}$ shift and capacitance value (or CET), which were investigated from CV curves. In this pre-evaluation, for substantive investigation, there was an additional annealing for 30 sec at 600℃ to diffuse La atoms from capping site to IL.

Figure 4.17 (a) shows that the $V_{FB}$ shifted to the negative direction with increasing La layer thickness due to La capping effect (or dipole effect) between HfO$_2$ and Si substrate, while the capacitance density (or CET) decreased with increasing the La layer due to adding additional La-O oxide layer into total capacitance. In case of La layers on HfO$_2$, the $V_{FB}$ did not shift at original position even though the La layer thickness increased, and the capacitance density decreased like bottom La layer samples. It was because the additional annealing at middle temperature (600℃) did not make the La atoms to diffuse from top of HfO$_2$ to IL. Also, this result indicated that only La atoms between HfO$_2$ dielectrics and Si substrate can shift the $V_{FB}$ to the negative direction, while La layers induce the total capacitance of MOS capacitor of Pt/HfO$_2$/Si stack to decrease due to the oxidation of La layers. On the other word, the La atoms positioned on HfO$_2$ (if diffused from La-incorporated TiN metal gates) may not cause the $V_{FB}$ shift.

Therefore, in this work, the effects of inserting the metal layers (Ti, La) into TiN metal gate, excepting La atoms diffusion and decrease of the total capacitance, were investigated.
Figure 4.17 Schematic diagrams of MOS capacitors with (a) bottom and (b) top sites of La metal layer with various thicknesses and C-V plots as a function of each (c) bottom and (d) top La layers
4.2.3 EOT scaling and physical/electrical properties

4.2.3.1 Comparison of TiLaN and TiN/La/TiN

The La-inserted structure of the TiN/La/TiN (TLT) (~5/~5/~5nm) layer and the La concentration of the TiLaN (TLN) (~25 nm) film with 80 % La was confirmed by their AES depth profiles, as shown in Figs. 4.18. It can be understood that the gate metals already have rather high oxygen concentrations, probably due to the residual oxygen in the chamber (base pressure ~ 2-3 x10^{-7} torr) and the scavenging effect. Although oxygen content in the TLT layer is rather high, the LaO_x (x < 1) layer is expected to maintain its metallic property. The AES profiles of the same samples after the PDA did not show any notable changes (only the O data is shown for the case after PDA for clarity) since the resolution of the measurements was not high enough to detect the small changes in the IL caused by the scavenging effect.

Figure 4.19 shows the V_{FB} shift amounts of the MIS capacitors with the two types of metal gates at various bottom TiN thicknesses for the TLT structure and as a function of La concentration for the TLN structure. The normalized C-V curves of MIS capacitors with reference metal gates (Pt and TiN), a TLT gate with various TiN thicknesses from 3 nm to 2nm, and a TLN gate with various La concentrations from 30% to 80% are shown in the inset of Fig. 4.19. The V_{FB} of the TLT/HfO_2/Si stack is increasingly shifted to the negative direction as the thickness of the bottom TiN layer decreases from ~10 to 3 nm. When the bottom TiN thickness is ~3 nm, the V_{FB} shift has its maximum value; 423 and 1130 mV away from the V_{FB} of the TiN and Pt single metal gate cases, respectively. This phenomenon can be explained by the carrier redistribution mechanism [25].
Figure 4.18 Schematic diagrams of MOS capacitors with (a) TiN/La/TiN (TLT) and (b) TiLaN (TLN) metal gates on HfO₂ and the AES profiles of as-deposited and PDA (600°C) (a) TLT(~5/5/5nm)/HfO₂/Si and (b) TLN(~25nm)/HfO₂/Si gate stacks.
Figure 4.19 Summary of $V_{FB}$ shift amounts of the MIS capacitors with TLT of varying bottom TiN thicknesses and TLN of varying La concentrations, extracted from (inset) each of the C-V curves.
When two metal layers (Al/TaN) with different work functions come into contact, charge transfer occurs between them and the Fermi levels of the two metal layers are adjusted until they reach equilibrium values [25]. Figure 4.20 shows illustrations of the relative band structure of bi-metal stack with different work functions. When the metal-1 layer is very thin, electron density of the thin metal-1 layer increases more easily than that of thick metal-1 layer. Therefore, TiN layer in TLT gate stack was so thin that work function of thin TiN layer decreased due to La layer with very low work function.

Interestingly, the $V_{FB}$ shifted into the opposite direction when the bottom TiN thickness was 2 nm. Fillot et al. reported that TiN layers thinner than 2.2 nm do not maintain their original structure and property due to various reasons [26]. Since the bottom TiN layer is in direct contact with the HfO$_2$, it is very likely that it will be locally oxidized, which would prohibit the film from sustaining its originally low work function when film thickness is extremely small. Li et al. reported that oxidized TiN has a higher work function than its normal counterpart, which supports this point of view [27]. It is also possible that the La(O) layer was further oxidized, which could also contribute to the increase of work function. The sum of these factors can explain the abnormal $V_{FB}$ shift observed for the 2 nm bottom TiN case.

The $V_{FB}$ shift caused by the TLN metal gate appears to be negligible compared to the TiN single metal gate until the La concentration reaches 42 %, while it shows a $V_{FB}$ shift of 247 mV at a La concentration of 80 %. However, the C-V characteristics were deteriorated in this case due to damage from the high plasma power required to introduce such high La concentrations (right inset Fig. 4.19). Therefore, the TLN sample with 42 % La was used for electrical property analysis.
Figure 4.20 Illustration of bi-metal stack structure. (a) Fermi level ($E_F$) shift in thin metal-1 layer and (b) no $E_F$ shift in thick metal-1 layer, showing that electrons in the metal-2 flow into the metal-1 electrode in relative band structure.
As mentioned above, the oxidation of La in the TLN films may increase the \( V_{FB} \) of the overall device because some La atoms may be in direct contact with the HfO\(_2\) film [27]. Therefore, the TLT stacked gate is expected to be more effective in modulating the EWF of the metal gates compared to the TLN mixed gate.

EWFs were extracted by extrapolating the linear fits of the \( V_{FB} \) vs. EOT (Fig. 4.21) profiles to the y-axis because \( V_{FB} \) shifts are attributed to the presence of fixed charges and interface dipoles as well as changes in the EWF. The EWFs of TiN and TLT metal gates on single-terraced SiO\(_2\) films were 4.54 and 4.06 eV, respectively. A similar trend was observed in the EWFs of TiN and TLT metal gates on the HfO\(_2\)/terraced SiO\(_2\) structure, which were 4.68 and 4.25 eV, respectively. A slight Fermi level pinning is observed on HfO\(_2\) compared to SiO\(_2\). Both cases showed that La-incorporation into the films lowered the EWF value compared to the TiN metal gate by as much as ~480 and ~430 meV on SiO\(_2\) and HfO\(_2\), respectively, which is coincident with the \( V_{FB} \) shift result in Fig. 4.19. Although the Pt and TiN on SiO\(_2\) case has a negligible slope in Fig. 4.20 (a), all other samples show very small positive slopes that correspond to fixed charge densities of -5.8x10\(^{11}\), -3.8x10\(^{11}\), and -7.9x10\(^{11}\) cm\(^{-2}\) for the TLT/SiO\(_2\), TiN/HfO\(_2\)/SiO\(_2\), and TLT/HfO\(_2\)/SiO\(_2\) stacks, respectively, which have almost negligible influence over the \( V_{FB} \) shift compared to the change in EMF.

The La incorporated TiN metal gates have another benefit other than EWF modulation, i.e., the IL scavenging effect, which means that the La metal ions remove oxygen from the IL to decrease the overall EOT of the capacitor. Figure 4.22 (a) shows the EOT vs. HfO\(_2\) thickness profiles of the MIS capacitors with TLT, TLN, and reference Pt and TiN single metal gates before and after PDA. The IL EOT of the various samples is
represented by the y-intercept of the graphs in Fig. 4.22 (a). The plots show different y-axis intercepts depending on the types of electrode, while the slopes increased slightly as the scavenging effect became stronger. A dielectric constants (3.9 divided by slope) of HfO₂ under as-deposited Pt, TiN, and TLT electrodes decreased slightly from 17 to 15.8 and 14, respectively. It was because if scavenging has occurred, the dielectric constant usually decreases due to possible diffusion of Si into the film. The IL thicknesses of various samples extracted from the y-intercept of graphs in Fig. 4.22 (a) are summarized in Fig. 4.22 (b).

In the as-deposited state, the TLT and TLN metal gates as well as the TiN single metal showed a superior IL scavenging effect compared to the Pt single metal gate. After PDA, the Pt and TiN single metal gates showed an abrupt increase in IL EOT after PDA, while both TLT and TLN metal gates suppressed IL growth to extremely small values, as shown in Fig. 4.22 (b). This is because incorporating La into TiN (both of TLT and TLN) increases the oxygen solubility in it [28]. Especially, the TLT metal gate showed an IL EOT of ~0.3 nm after PDA and it also showed a more desirable VFB shift. The abrupt decrease of EOT at a HfO₂ thickness of ~ 3.5 nm suggests a larger degree of scavenging occurs at thinner HfO₂ thicknesses. The scavenging effect was confirmed by HRTEM as shown in Fig. 4.23. The as-deposited TLT stacks with thick (~10nm) bottom TiN layers (Fig. 4.23 (a)) showed the ~ 1-nm-thick IL which was as much as that by only TiN single gate. However, the thick IL layer almost disappeared after PDA in the TLT stack with thin bottom TiN layer (Fig. 4.23 (b)). Figure 4.23 (c) shows the Jg – EOT graphs of various samples. Different gate stacks show negligible difference except for the TLN case which is thought to come from sputter damage as discussed above.
Figure 4.22 Plot of EOT as a function of HfO$_2$ thickness for extraction of IL thicknesses for various metal gates. And summary of IL thicknesses for various metal gates.

Figure 4.23 HRTEM images of (a) as-deposited TLT(10/5/10nm) and (b) PDA TLT (3/5/3nm) on HfO$_2$ (3~4nm)/Si gate stacks capped by Si. (c) $J_g$ – EOT graphs of various samples (Pt, TiN20nm/Pt, TLN(42% La, 15 nm)/Pt, TLT(3/5/3nm)/Pt).
In case of inserting Ti layer into TiN metal layers, the ability of $V_{FB}$ shift and IL scaling was expected by considering the Gibbs free energy and intrinsic work function of Ti metal. Figure 4.24 shows the comparison of CV curves and IL thicknesses of TLT and TiN/Ti/TiN (TTT) metal gates with references of Pt and TiN single gates. As expected, TTT gate stack showed the ability similar to TiN single gate in terms of modulating the $V_{FB}$ and scaling the IL thickness. However, after PDA the TTT gate stack showed superior suppression of IL re-growth than TiN, as shown in Fig. 4.24 (d).

Figure 4.24 CV curves of TLT and TTT including Pt and TiN on HfO$_2$/Si stacks at (a) as-deposition and (b) after PDA. And plot of EOT as a function of HfO$_2$ thickness for extraction of IL thicknesses and summary of IL thicknesses for TLT and TTT with references of Pt and TiN.

128
The oxidation of elements in the gate metal and at the interface with the HfO₂ film was confirmed by XPS analysis. Figure 4.25 shows the La 3d core-level XPS spectra of the TLT (~5/5/5 nm)/HfO₂/Si stack and the TLN (~15 nm) with 42% La/HfO₂/Si stack before and after PDA. Both XPS spectra show a peak at ~834.5 eV which corresponds to metallic La (3d₅/₂) and a clear satellite peak. Satellite peaks that have a higher energy binding than core-levels are commonly observed in cases where a certain amount of oxidation or nitridation occurs [29]. Considering the difference in the relative intensities of the shake-up features for the La 3d core-levels in the TLT and TLN films, it can be seen that the La atoms in the TLT film are primarily bonded with O, while those in the TLN film are primarily bonded with N. The non-oxidized atoms remaining in the TLT and TLN layers seem to have a metallic property. In the Ti 2p core-level XPS spectra of the films shown in Fig. 4.26, the main and shoulder Ti 2p₃/₂ peak at 455 and 457.5 eV correspond to TiN and TiOₓNᵧ, respectively [30]. The lower intensity of the TiOₓNᵧ peak in the TLT film compared to the TLN film suggests that the La metal layer in the TLT film easily takes O from the TiN layer, while the La ions in the TLN film have a hard time breaking Ti-O bonds in the film. The XPS data given here points out that the IL scavenging effect discussed above can be explained by the partial oxidation of the gate metal films in both TLT and TLN films. However, it is important to point out that the vertical distribution of the main oxidized element is different in the two cases. The La metal layer in the TLT film is separated from the HfO₂ film by the bottom TiN layer when it is thicker than ~3 nm, but the La in the TLN film is in direct contact with the HfO₂ film. Therefore, the oxidation of Ti in the TLN film increased the EWF which resulted in a lowered V₉B modulation compared to the TLT film.
Figure 4.25 La 3$d$ regions of XPS spectra for (a) TLT(5/5/5nm)/HfO$_2$/Si and (b)TLN (~15nm) with 42% La/HfO$_2$/Si gate stacks capped by the poly-Si (~30nm).

Figure 4.26 Ti 2$p$ regions of XPS spectra for (a) TLT(5/5/5nm)/HfO$_2$/Si and (b)TLN (~15nm) with 42% La/HfO$_2$/Si gate stacks capped by the poly-Si (~30nm).
Finally, Figure 4.27 shows the interface state density (Dit) measured by the conductance method [31] at the midgap of Si band gap energy for MOS capacitors with TLT and TLN metal gate as well as Pt and TiN single metal gates. Dit increased gradually with increasing La deposition power in both TLT and TLN gate stacks. In La 60W, the appropriate La power of both gate stacks, Dit of TLT was slightly lower than that of TLN. However, considering the Dit level of ~1.0x10^{-12} cm^{-2}eV^{-1} for HfO2/Si gate stack with the Pt and TiN single metal gates, the degradation of Dit for both of TLT and TLN metal gates (~1.5x10^{-12} and ~2.2x10^{-12} cm^{-2}eV^{-1}, respectively) was tolerable, which was caused by the decreased IL due to the scavenging effect of those gate metal layers.

Figure 4.27 Dit characteristics of TLT and TLN metal gates including Pt and TiN single metal gates on HfO2/Si, evaluated by the conductance method. (a) Plot of Dit as a function of gate voltage (or energy state) and (b) summary of Dit in TLT and TLN as a function of La power at the midgap of Si band gap.
4.2.3.2 TiN/La/TiN metal gate on HfSiO

Until now, IL scavenging works were investigated on HfO₂ as gate dielectrics by La-incorporated TiN metal gates. In order to understand the role of high-\(k\) layer on IL scaling using scavenging reaction, TiN/La/TiN (TLT) electrodes were employed on various compositions of Hf\(_{1-x}\)Si\(_x\)O\(_y\) layers with the Si/(Hf + Si) ratio ranging from 0% (HfO₂) to 82% and metal-oxide-semiconductor (MOS) capacitors were fabricated. Hf\(_{1-x}\)Si\(_x\)O\(_y\) (HfSiO) was studied in section 4.1 about dielectric constant and crystal structure in which Pt electrodes on HfSiO were prepared as reference samples. As-deposited TLT electrodes on HfSiO with several thicknesses were fabricated. Figure 4.28 (a) and (b) shows the plot of EOT as a function of HfSiO film thickness including HfO₂ film for extraction of IL thicknesses and dielectric constant (\(k\)) drop amount and EOT reduction amount by remote IL scavenging (i.e., EOT difference between the TLT and the Pt) as a function of the Si/(Hf+Si) ratio of HfSiO, respectively. TLT electrodes, even as-deposited, as the Si/(Hf+Si) ratio is increased, the EOT reduction amount decreased gradually compared to that for HfO₂ up to Si/(Hf+Si) ratio of 50% and then it reached almost to zero. This trend indicates that ionic bonds (Hf-O) play a key role in remote-scavenging and the effect is hampered as the ratio of covalent bonds (Si-O) is increased [32]. HfO₂ and ZrO₂ are very effective mediators of remote-scavenging from this perspective. As mentioned above, if the scavenging reaction has occurred, the dielectric constant of HfO₂ usually decreases due to possible diffusion of Si into the film. However, the dielectric constant of HfSiO did not decrease as shown in Fig. 4.28 (b). This result indicated that Si atoms in HfSiO with Si composition above ~ 20% film may suppress to diffuse other Si atoms from Si substrate. Also, in case of 800°C annealed HfSiO film with 16% Si, Fig.
4.28(c) shows that TLT electrode induced further EOT scaling due to the IL scavenging, with increasing the permittivity (means low slope). Although TLT metal gate induced the IL scavenging of PDA HfSiO films, the remained IL EOT lowered the capacitance density of PDA HfSiO compared to that of TLT on HfO2, shown in Fig. 4.28(d).

Figure 4.28 Plots of EOT as a function of HfSiO film (with (a) several Si compositions and (c) 800°C annealed film of 16% Si) thickness including HfO2 film for extraction of IL thicknesses and dielectric constant (k), and (b) EOT IL reduction and k-value drop amounts via remote-scavenging from TLT electrodes as a function of Si composition in HfSiO compared to that of Pt. And (d) the C-V curves of several gate stacks.
4.2.3 Conclusion

In summary, the $V_{FB}$ modulation and IL scavenging effect of TLN and TLT (or TTT) metal gates were examined in the MIS capacitor structure. While both TLT and TLN metal gates have superior IL scavenging effects compared to Pt and TiN single metal gates, the TLT metal shows a better scavenging effect and $V_{FB}$ modulation than the TLN metal. In case of TLT on HfSiO, the Si/(Hf+Si) ratio is increased, the EOT reduction amount decreased gradually compared to that for HfO$_2$ up to Si/(Hf+Si) ratio of 50% and then it reached almost to zero. Therefore, the La-inserted TiN metal gate process is a suitable candidate for fabricating n-type MIS devices, especially on HfO$_2$ or HfSiO with low Si compositions, in the gate-last approach, where high temperature annealing is rarely performed.
4.3 Gate engineering using Ru and RuO₂ metal gates

4.3.1 Introduction

Thin high-\(k\) dielectric films play crucial roles in modern semiconductor devices, including the capacitor dielectrics for dynamic random access memory (DRAM) [33] and gate dielectric film in complementary metal oxide semiconductor field effect transistors (CMOSFETs) with the metal gate [2]. Recent progresses in this field made the attainable equivalent oxide thickness (EOT) with satisfactory leakage current reaches down to \(\sim 0.5\) nm or even smaller, which corresponds to a huge capacitance density of \(\sim 70\) fF\(\mu\)m\(^{-2}\). The physical thickness (\(t_{\text{phy}}\)) for such an extremely small EOT has already approached to its quantum mechanical tunneling limit (\(\sim 6\) nm for DRAM, and \(\sim 2\) nm MOSFET) so further scaling of \(t_{\text{phy}}\) inevitably must be accompanied with a too high leakage current. Therefore, another method must be pursued. Adopting a material with an even higher-\(k\) value, may allow for a higher \(t_{\text{phy}}\). However, dielectric materials with a higher-\(k\) value also suffer from the potential leakage current problem due to the generally lower band gap [3]. An even more serious problem is that the effective dielectric constant decreases with decreasing thickness, which becomes even more serious as the bulk \(k\) value increases. Such problems have been extensively studied in the metal-insulator-metal (MIM) structure where the insulator is typically perovskite materials with \(k\) values > 100 [34-36]. Recently, Lee et al. [37], reported that such a problem can occur even in a medium high-\(k\) material, such as ZrO\(_2\) of which \(k\) value is \(\sim 35\), suggesting that the most prevailing high-\(k\) material in CMOSFET, HfO\(_2\), in the metal-insulator-semiconductor
(MIS) structure may also suffer from a similar problem, which has not been seriously studied. However, this could be a crucial component in further scaling of EOT in MIS given the fact that the available EOT is already < 1 nm.

Such degradation in \( k \) value with decreasing \( t_{\text{phy}} \) is a sort of intrinsic property of the high-\( k \) dielectrics because the high-\( k \) value is an outcome from the mutual interaction of highly polarizable dipoles in the high-\( k \) layer itself, even without any adverse physico-chemical interactions between the dielectrics and electrodes. Therefore, the dipolar polarization must be decreased at the interface region with the electrode due to the absence of neighboring dipoles, making the effective \( k \) value smaller at smaller \( t_{\text{phy}} \). When a high-\( k \) is placed in an external electric field (\( E_{\text{ext}} \)), the dipoles in the materials polarize according to the \( E_{\text{ext}} \), which brings about the development of the internal depolarizing field (\( E_{\text{dep}} \)). When metal electrodes are in contact with the polarized dielectrics, the compensating charges develop at the interfaces, which (partly) nullify the \( E_{\text{dep}} \). However, due to the finite screening length (Thomas-Fermi length) of typical metals (< ~ 0.1 nm) and the finite Fermi level (\( E_F \)) [38] such a polarization charge screening effect is not complete, making the depolarization effect more severe at smaller \( t_{\text{phy}} \). So, polarizable electrodes with high electrical conductivity are necessary to suppress such an intrinsic adverse effect, which are usually contradictory characteristics for an electrical conductor to have. In this regard, Si as an electrode in the MIS structure is a very unfavorable material even in its inversion or accumulation state due to its relatively low electrical conductivity and non-polarizable nature. Therefore, capacitance equivalent oxide thickness (CET) is usually larger than the EOT by 0.2 – 0.3 nm [39]. In addition, the high-\( k \)/Si interface is almost always intervened with the low-\( k \) SiO\(_2\) layer, which is
somehow necessary for the improved quality of the electrically active interface, so that most of the engineering works have been focused on the high-\( k \)/Si interface [2]. The metal gate/high-\( k \) interface in MOSFET was also studied extensively mostly due to the \( E_F \) pinning and accompanied instability in threshold voltage [40]. However, its influences on the dielectric performance of high-\( k \) film have been rarely studied.

In this work, it was found that an EOT gain as high as 0.5 nm can be achieved by replacing the standard Pt gate metal with the electrically conducting RuO\(_2\) without sacrificing any other performance of the MOS capacitor. RuO\(_2\) is one of the rare materials, which contain polarizable ions, high electrical conductivity, and high work function (WF) which is necessary for the p-type MOSFET. Also, physical characteristics of RuO\(_2\) films with the oxygen partial pressure (\( P_{O_2} \)) (\( O_2/[Ar+O_2] \)) in the reactive sputtering were studied on effective work function (EWF), extracted from terraced SiO\(_2\) substrates and HfO\(_2\) on terraced SiO\(_2\) substrates, compared to that of Pt. Also, fixed charge of Pt and RuO\(_2\) metal gates were investigated with increasing the oxygen partial pressure.
4.3.2 Experimental

Atomic layer deposited (ALD) HfO$_2$ films were grown with the thickness of 2 ~ 6 nm on a HF cleaned p-type Si substrate (100) for MIS samples, and with the thickness of 15 ~ 35 nm on Pt substrates for MIM samples at a substrate temperature of 270 °C using tetrakis(ethylmethylamino)hafnium (Hf(N(CH$_3$)(C$_2$H$_5$)$_2$)$_4$) and ozone gas with a concentration of 170 g/Nm$^3$ as the Hf precursor and oxygen source, respectively. Thermal SiO$_2$ (6 nm) or terraced SiO$_2$ (3 to 8 nm) was also used as the dielectric layer in MIS for comparison. On the terraced SiO$_2$ film, 3nm-thick ALD HfO$_2$ was deposited to achieve various EOT values for estimating the flat band voltage ($V_{FB}$), which is free from the bulk charge effects. 10nm-thick Ru and 30nm-thick RuO$_2$ films were grown by rf magnetron sputtering using an Ru target (~99.9%) through the metal shadow mask (area of 90,000 um$^2$). In the RuO$_2$ sputtering process, the Ar+O$_2$ mixture was used as the sputtering gas and the O$_2$/($Ar+O_2$) flow ratio was fixed at 10.4 % (O$_2$ 3.5 sccm with Ar gas flow at 30 sccm) for investigating deadlayer shrinkage effect of Ru and RuO$_2$ electrode, while the O$_2$/($Ar+O_2$) gas flow rate (O$_2$ ratio) was varied from 3.3 % to 16.7 % and from 1 sccm to 5 sccm, respectively, at fixed Ar 30 sccm for analyzing physical and electrical properties of RuO$_2$ electrode. For comparison, sputtered 50nm-thick Pt and 10nm-thick TiN films were grown on the same gate dielectric stacks. TiN films were grown at the dc power of 100 W using the 3-in. pure Ti metal target (~99.99 %) and 5 % N$_2$/($Ar+N_2$) reactive gas. For comparison to deadlayer shrinkage effect of Ru and RuO$_2$ electrodes, stacked metal electrodes (2nm-thick Ru/50nm-thick Pt and 2nm-thick RuO$_2$/50nm-thick Pt) were also fabricated on the dielectrics without vacuum break. On the 10nm-thick Ru, 30nm-thick RuO$_2$ and 10nm-thick TiN, as well as a 50nm-thick Pt layer was grown in-situ for stable
contact in electrical measurements. In case of MIS capacitors, forming gas (5 % H2/95 % N2) annealing was performed at 400 °C for 30 min. Samples were examined by X-ray fluorescence (XRF), X-ray photoelectron spectroscopy (XPS), X-ray reflectivity (XRR), spectroscopic ellipsometry (SE), Auger electron spectroscopy (AES), and high-resolution transmission electron microscopy (HRTEM). The film thickness of only HfO2 was carefully measured using the XRR and SE excluding the interfacial layer (IL) thickness. After the gate electrode formation, forming gas (5 % H2/95 % N2) annealing was performed at 400 °C for 30 min. Capacitance-Voltage (C-V) characteristics were examined using a Hewlett-Packard 4194A Impedance/Gain-Phase Analyzer at 100 kHz. The measured C-V curves were simulated using Hauser’s CVC program to obtain the EOT values [39].

4.3.2.1 Ru and RuO2 electrode setup

Ru and RuO2 electrode films were reviewed about physical and electrical characteristics before optimizing sputtering condition for study in this work. Ruthenium (Ru) is rate transition metal that belongs to platinum group metal with Pt, Ru, Pd, Os and Ir. These metals have a inert property against most chemical gases and can be oxidized to conducting oxides such as RuO2 (oxidation state +4) or IrO2. Ru and RuO2 films are known to exhibit low resistivity of ~7 and ~35 $\mu \cdot \Omega \cdot \text{cm}$, respectively, at 273.15K and good thermal stability and chemical stability. Ru and RuO2 films have the hexagonal closed packed (hcp) and rutile structures, respectively. The properties of Ru and RuO2 are compared in Table 4.1. In case of RuO2 film, the molar volume is 2.3 times larger than that of Ru film because RuO2 has two oxygens. Ru and RuO2 growth rates will be
compared as a function of O$_2$/(Ar+O$_2$) ratio later. Although the Ru electrode has intrinsic work function (WF) of ~4.7 eV, the film has shown various WFs from 4.7 eV to ~5.2 eV due to the oxidation of the film in several papers. In case of RuO$_2$ electrode, WF is intrinsic 5.1 ~ 5.3eV which has been reported similarly in most papers.

<table>
<thead>
<tr>
<th></th>
<th>Ru (Ruthenium)</th>
<th>RuO$_2$ (Ruthenium oxide)</th>
<th>Crystal structures of Ru and RuO$_2$</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>atomic number</strong></td>
<td>44</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>element category</strong></td>
<td>transition metal</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>atomic radius</strong></td>
<td>0.134 nm</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>lattice parameter</strong></td>
<td>a = 0.271 nm</td>
<td>c = 0.426 nm</td>
<td></td>
</tr>
<tr>
<td><strong>atomic weight</strong></td>
<td>101.07 g/mol</td>
<td>133.07 g/mol</td>
<td></td>
</tr>
<tr>
<td><strong>density</strong></td>
<td>12.45 g/cm$^3$</td>
<td>6.97 g/cm$^3$</td>
<td></td>
</tr>
<tr>
<td><strong>electrical resistivity</strong></td>
<td>71 m$\Omega$·m</td>
<td>350 m$\Omega$·m (~35$\mu$Ω·cm)</td>
<td></td>
</tr>
<tr>
<td><strong>crystal structure</strong></td>
<td>Hexagonal</td>
<td>Rutilte (tetragonal)</td>
<td></td>
</tr>
<tr>
<td><strong>coordination geometry</strong></td>
<td></td>
<td></td>
<td>Octahedral (Ru$^4^+$); trigonal planar (O$^{2-}$)</td>
</tr>
<tr>
<td><strong>magnetic ordering</strong></td>
<td>paramagnetic</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>electron configuration</strong></td>
<td>[Kr] 4d$^5$ 5s$^1$ (2.8.16.15.1)</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Work Function</strong></td>
<td>4.7 eV</td>
<td>~ 5.1 eV</td>
<td></td>
</tr>
<tr>
<td><strong>electron affinity</strong></td>
<td>101.3 kJ/mol</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>ionization energy</strong></td>
<td>710.2/1620/2747 (kJ/mol)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 4.1 Properties of ruthenium (Ru) and ruthenium oxide (RuO$_2$)
4.3.3 EOT scaling and physical/electrical properties

4.3.3.1 Deadlayer shrinkage effect of Ru and RuO₂

Figures 4.29 (a) and (b) show an XPS spectra of Ru 3d and O 1s peaks, respectively, of the 10nm-thick Ru and RuO₂ films grown on SiO₂/Si. The XPS peak positions were calibrated using the deconvoluted C 1s peak (binding energy (BE) of 284.5 eV), indicated by the dash-dot line in Fig. 4.29 (a) from the peak observed near the BE of 285 eV, which is composed of Ru 3d₃/₂ and C 1s peaks. Figure 4.29 (a) shows that the peak position of Ru 3d₃/₂ in RuO₂ film was located at \( \sim 281 \) eV, which corresponds to the binding energy of Ru 3d₃/₂ in RuO₂, while that of Ru film was found near the BE of \( \sim 280 \) eV which corresponds to metallic Ru, indicating that the films are mostly RuO₂ and Ru, respectively [41]. O 1s peaks in Fig. 4.29 (b) corroborate this, but there are certainly oxygen signals from the surface oxide and other contaminants even on Ru film. The estimated atomic ratio of Ru : O in RuO₂ films was \( 1 : \sim 2.15 \) from the areas of Ru 3d and O 1s peaks. Although the oxidation state of the Ru region, which is in contact with the HfO₂, cannot be examined by the present XPS, the possibility of partial oxidation cannot be completely ruled out.

Figure 4.30 (a) illustrates the variations in EOT for the MIS samples with different types of metal electrodes as a function of HfO₂ film thickness, and the inset figure shows the representative C-V curves of the 3.3nm-thick HfO₂ film with Pt and RuO₂ electrodes showing the largely different dielectric performance depending on the electrodes for the given dielectric layer. The inset figure also shows the C-V curves of the same HfO₂ film with Pt and RuO₂ electrodes before FGA. It can be understood that the FGA largely
improve the curve by curing various interfacial defects and trapping sites while the accumulation capacitance was hardly influenced by the FGA. It can be immediately seen that the EOT values of the MIS samples with 30nm-thick RuO₂ electrodes are smaller than those of Pt electrode by ~ 0.5 nm irrespective of the HfO₂ thickness revealing the effectiveness of the RuO₂ in reducing EOT. Due to such an improvement, the minimum EOT that was achieved from the 2nm-thick HfO₂ was as small as ~0.8 nm, of which leakage current density was ~ 4.0x10⁻¹ Acm⁻² at V_FH -1 V. It must be mentioned that the EOT values of the present work are generally larger than the status-of-the-art values by ~0.4 nm due to the use of O₃ during ALD, which makes IL too thick (~ 1.5 - 2 nm). However, the aim of the present work is to systematically examine the electrode effect, so this does not matter. While the MIS samples with other electrodes showed intermediate EOT values, it is quite evident that HfO₂ film with a thicker RuO₂ layer demonstrated smaller EOT values. The y-axis intercept and slope of the best-linear-fitted graphs correspond to the EOT contributed by IL at the HfO₂/Si interface and the possible dielectric dead-layer at the HfO₂/metal interface, and the bulk dielectric constant of HfO₂ (3.9 divided by slope), respectively. It can be understood that Pt, Ru, and RuO₂ electrodes, irrespective of their thickness, produced almost identical bulk k values of 17, while the adoption of the TiN electrode resulted in the bulk k values of 14. In contrast, the y-axis intercept values are very dependent on the types of electrodes, which resulted in the largely different EOT values. Although the bulk k value of TiN gated MIS samples is smaller and EOT values are generally larger than that of the thick RuO₂ gated MIS samples, the y-axis intercept values of the two types of samples are almost identical. These peculiar behaviors of the TiN gated samples are understood from the oxygen
scavenge effect of TiN on thin HfO$_2$/SiO$_2$ stacked gate as reported elsewhere [42]. In order to understand the origin of such variations in y-axis intercept values, the EOT values of MIM samples having Pt/HfO$_2$/Pt and RuO$_2$/HfO$_2$/Pt with varying HfO$_2$ thicknesses are plotted in Fig. 4.30 (b), where the inset figure shows the typical C-V curves. Here, the slopes of the best-linear-fitted graphs also revealed a common bulk k value of 17, but the y-axis intercept shows a difference of $\sim 0.4 - 0.5$ nm suggesting that the Pt/HfO$_2$ and RuO$_2$/HfO$_2$ bears the origin of the EOT variation. Figure 4.31 (a) and (b) show the schematic diagrams of dipole polarization in HfO$_2$ dielectrics in MIS and MIM with Pt or RuO$_2$ electrode. Intensity of polarized dipoles near interface between Pt and HfO$_2$ seem to be weakened by screening electric field penetration, while RuO$_2$ electrodes may maintain the intensity of polarized dipoles near interface between RuO$_2$ and HfO$_2$ because of their possible ionic polarization as the conducting oxide. In MIM of metal electrode/HfO$_2$/Pt stack, the dead-layer shrinkage seems to be induced by RuO$_2$ top electrode. In addition, Table 4.2 summarizes the various parameters extracted from Fig. 4.30 for the different MIS and MIM samples.

Figure 4.29 (a) Ru 3$d$ and (b) O 1$s$ regions of the XPS spectra for Ru (10 nm) and RuO$_2$ (30 nm) on SiO$_2$/Si.
Figure 4.30 Variation of EOT as a function of HfO$_2$ oxide thickness with various electrodes in (a) MIS (Metal electrodes/HfO$_2$/Si) and (b) MIM (Metal electrodes/HfO$_2$/Pt). (Insets are CV curves (a) before and after FGA in MIS and (b) of as-deposited MIM)
Figure 4.31 Schematic diagrams of dipolar polarization in HfO₂ dielectrics in (a) MIS (Metal electrodes/HfO₂/Si) and (b) MIM (Metal electrodes/HfO₂/Pt). RuO₂ electrode eliminated the intrinsic dead-layer due to conducting oxide property.
<table>
<thead>
<tr>
<th></th>
<th>slope</th>
<th>k</th>
<th>EOT IL</th>
<th>WF from t-SiO₂</th>
<th>EWF from HfO₂/t-SiO₂</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pt</td>
<td>0.229</td>
<td>17.0</td>
<td>0.98</td>
<td>5.42</td>
<td>5.0</td>
</tr>
<tr>
<td>TiN(20nm)</td>
<td>0.270</td>
<td>14.5</td>
<td>0.51</td>
<td>4.54</td>
<td>4.68</td>
</tr>
<tr>
<td>Ru(10nm)</td>
<td>0.224</td>
<td>17.4</td>
<td>0.63</td>
<td>5.2</td>
<td>~5.0</td>
</tr>
<tr>
<td>RuO₂(30nm)</td>
<td>0.229</td>
<td>17.0</td>
<td>0.46</td>
<td>5.3</td>
<td>~5.0</td>
</tr>
<tr>
<td>Ru(2nm)/Pt</td>
<td>0.233</td>
<td>16.7</td>
<td>0.74</td>
<td>5.4</td>
<td>~5.0</td>
</tr>
<tr>
<td>RuO₂(2nm)/Pt</td>
<td>0.234</td>
<td>16.7</td>
<td>0.71</td>
<td>5.4</td>
<td>~5.0</td>
</tr>
</tbody>
</table>

Table 4.2 Summary of the various parameters extracted from Fig. 4.30 for the different MIS and MIM samples.
This was further backed up by Fig. 4.32, where the cross-section HRTEM images of the (a) 10nm-thick Ru, (b) 30nm-thick RuO₂, (c) 50nm-thick Pt, and (d) 10nm-thick TiN electrode on HfO₂/SiO₂/Si are shown. All the HfO₂ films show an amorphous structure, and the IL thickness was almost invariant (~2nm) except for the TiN case (~1nm) due to the scavenging effect. These results elucidate that the EOT variations shown in Fig. 4.30 (a) are not due to the change in the status of IL, except for the TiN case. The figures in Figs. 4.32 (e) and (f) shows the microstructures of 2nm-thick Ru and RuO₂ layers deposited on SiO₂ (~6nm). The layers are not atomically flat but certainly show agglomerated grains, suggesting the possible diffusion of Pt onto the dielectric surface when the 50nm-thick Pt layer was deposited on top. This could be the appropriate explanation for the less efficient reduction of EOT values when the thin (2nm) Ru and RuO₂ layers were interposed between the HfO₂ and Pt layers; the portion where the Pt/HfO₂ contacts are made suffered from the dead-layer effect.

Meanwhile, the sputtering of heavy metals, such as Pt and Ru, could induce various damaging effects and even sputter etching especially for the case of RuO₂ due to the presence of negatively charged oxygen ions, which may heavily bombard the HfO₂ film surface. Therefore, the possible influences of these adverse effects must be ruled out to correctly understand the dead-layer effect from the high-k/metal gate system. Therefore, the physical states of the HfO₂ films under the various electrodes are examined carefully by XRF. XRF counts the number of Hf atoms per area (layer density) since the penetration depth for the characteristic X-ray of Hf atoms is far higher than the sum of the all the film thicknesses. Figure 4.33 shows the variation of Hf layer density for a given HfO₂ thickness (given in figure) and Ru (or Ti) layer densities as a function of sputtering
Figure 4.32 HRTEM images of the interfacial layers between Si and HfO2 with (a) as-deposited Ru, (b) RuO2, (c) Pt and (d) TiN electrodes. And HRTEM images of thin (~2 nm) (e) Ru and (f) RuO2 layers on SiO2.
time of Ru, RuO₂, and TiN electrodes. The data for Pt electrode, unfortunately, cannot be given here due to the overlap of Hf and Pt signals in the present XRF equipment. It can be understood that the Hf layer density does not show any systematic variation within the experimental error with the varying sputtering time, while the Ru and Ti layer densities increased very linearly suggesting the accuracy of the measurement as well as the well-controlled sputtering processes of the electrodes. The inset figure shows the linear correlation between the Hf layer density and the ellipsometric thickness of HfO₂, again showing the accuracy of XRF. This reveals that the sputtering process of the electrodes did not induce any sputter etching of the HfO₂ film.

Figure 4.33 Variations of Hf layer density for a given HfO₂ thickness and Ru (and Ti) layer densities as a function of sputtering time of Ru, RuO₂, and TiN electrodes.
Next, the electrical states of the HfO$_2$ films under the different electrodes were characterized by checking the variation in $V_{FB}$. Prior to that, the effective work function (EWF) of each electrode was estimated using the SiO$_2$ dielectrics, which is free from the Fermi level pinning effect. Figure 4.34 (a) shows the variation of $V_{FB}$ values for the terraced SiO$_2$ MIS samples, which were extracted from each C-V and CVC fitting, as a function of CET of SiO$_2$. The EWF values, extracted from the extrapolation of the best-linear-fitted graphs to the y-axis and the $E_F$ of Si (~5.1eV), are also tabulated in table 4.2. The values coincide well with the literature values [43,44] suggesting the appropriateness of the gate material of the present work. There are small differences in the slope of the best-linear-fitted graphs suggesting a small difference in the induced charges by the different electrode processes, but they are small enough to be ignored. Figure 4.34 (b) shows the typical C-V curves of the 6nm-thick thermal grown SiO$_2$ films with different electrodes. Although the $V_{FB}$ values are quite distinctive due to the different WF of the gate metals, the extracted capacitance values are identical, which is in stark contrast to the results shown in Figs. 4.30 (a) and 4.34 (c) where the C-V curves of 3.3nm-thick HfO$_2$ films with different electrodes are shown. The absence of variation in capacitance values regarding SiO$_2$ can certainly be understood from the lack of strong dipole-dipole interaction in SiO$_2$, of which the chemical bonding nature is closer to covalent one. Figure 4.34 (d) shows the variation of $V_{FB}$ of the 3nm-thick HfO$_2$/terraced SiO$_2$ MIS samples as a function of their CET. It must be noted that the CET values here are varied by the variation of SiO$_2$ thickness. In contrast to the SiO$_2$ MIS samples, the $V_{FB}$ values of these samples with the various electrodes, except for the TiN case, converges to a single trend line, which can be understood from the well-known Fermi level pinning effect [40].
The roll-off of the $V_{FB}$ with decreasing CET when it is $< \sim 3\text{nm}$ is also well consistent with the report by Bersuker et al. [45]. The deviation of data from the TiN gated samples in both SiO$_2$ and HfO$_2$/SiO$_2$ MIS samples can be understood from the chemical activity of TiN (scavenging effect), while all other electrodes are quite chemically inert to the dielectrics. These observations clearly demonstrate that there are hardly any physico-chemical and electrical modifications of the high-$k$ dielectric layers depending on the types of electrodes tested in this work, again, except for the TiN. Therefore, it can be safely assumed that the improvement in the EOT by adopting the RuO$_2$ electrode is ascribed to the suppression of the dead-layer effect at the HfO$_2$/metal gate interface.

The dielectric dead-layer effect of high-$k$ materials has been a topic for the very active theoretical and experimental research works. As mentioned above, the dead-layer effect is inevitable as long as the screening length of any metal cannot be zero. Recently, Stengel and Spaldin [46] suggested an improved screening behavior, which lowered the dead-layer effect, from Pt electrode compared with oxide electrode, ca. SrRuO$_3$, through a theoretical work. This is mainly attributed to the higher electron density of pure metal than that of oxide electrodes. However, such a dead-layer effect has always been more severe from pure metal, typically the Pt electrode in experiments, which may be attributed to the non-ideal situation at the dielectric/Pt interface compared with more lattice matched dielectric/SrRuO$_3$ interface. Meanwhile, Vendik et al. [47] already indicated the possible suppression of such a dead-layer effect by adopting oxide electrodes, such as RuO$_2$, IrO$_2$, or SrRuO$_3$, thanks to their possible ionic polarization, which was indeed experimentally observed [48,49]. The presence of the finite screening length conversely means that the electrode material within the screening length can experience the electric
field, and the dipolar polarization can even be induced in the electrode within the screening length of such minimal thickness if there are polarizable ions. This can explain the suppression of the dead-layer effect and consequent improvement in EOT in the MIS sample having an HfO$_2$ dielectric and RuO$_2$ electrode. It must be noted that such a suppression of the dead-layer effect has been reported extensively in the MIM system with higher-$k$ dielectrics, such as TiO$_2$ ($k \sim 100$) and SrTiO$_3$ ($k > \sim 200$), when the electrodes are conducting oxides [50,51]. It is slightly unexpected to observe that the relatively low high-$k$ (17) value of HfO$_2$ can induce such a clear dead-layer effect, and changing the pure metallic electrode with the oxide electrode enhanced the EOT performance so profoundly.

Figure 4.35 (a) shows the plot of $J_g$ vs. EOT of MIS capacitors with as-deposited Pt, thin RuO$_2$ ($\sim$2nm)/Pt and thick ($\sim$30nm) RuO$_2$/Pt electrodes on HfO$_2$($\sim$3.3nm)/Si stack. Thick RuO$_2$ electrodes showed the improved insulating property as much as EOT scaling amount induced by suppressing the deadlayer effect. Also, the thin RuO$_2$/Pt stack electrode showed the less efficient reduction of $J_g$ than thick RuO$_2$, which was well coincident with the less efficient reduction of EOT values as shown in Fig. 4.30 (a).

The leakage characteristics of MIM capacitors with as-deposited Pt, thin RuO$_2$ ($\sim$2nm)/Pt and thick ($\sim$30nm) RuO$_2$/Pt electrodes on HfO$_2$($\sim$32nm)/Pt stack are shown in Fig. 4.35 (b). On the contrary to MIS, thin RuO$_2$/Pt stack electrodes showed the improved insulating property due to suppression of the deadlayer effect. The leakage current of thick RuO$_2$ electrode increased than Pt only electrode. Because the shottky barrier height of thick RuO$_2$ seems to be lower than that of Pt due to the lower WF of RuO$_2$, while the barrier height of thin RuO$_2$/Pt stack seems to be as high as Pt electrode. However, the thin
RuO$_2$/Pt showed negligible EOT scaling as shown in Fig. 4.30 (b).

Figure 4.34 Plots of $V_{FB}$ vs. CET for various electrodes using (a) terraced SiO$_2$ and (d) HfO$_2$/terraced SiO$_2$ oxide, and C-V curves of (b) 6nm-thick SiO$_2$ and (d) 3.3nm-thick HfO$_2$ films with different electrodes.
Figure 4.35 Plot of (a) EOT vs. $J_g$ of MIS with Pt, thin RuO$_2$(2nm)/Pt and thick RuO$_2$ electrodes on HfO$_2$/Si stack and (b) $J_g$ as a function of gate voltage of MIM with Pt, thin RuO$_2$(2nm)/Pt and thick RuO$_2$ electrodes on HfO$_2$/Pt stack.
4.3.3.2 O\textsubscript{2}/(Ar+O\textsubscript{2}) ratio effect in RuO\textsubscript{2} deposition

Figure 4.36 (a) shows the variations of Ru layer density of RuO\textsubscript{2} films, estimated by XRF, for the two rf powers (30 and 60 W) as a function of O\textsubscript{2} ratio when the deposition was performed for 600 s. In both cases, the Ru layer density decreases almost linearly with the increasing O\textsubscript{2} ratio up to a certain critical value (~ 6 and 13 % for the 30 and 60 W, respectively), and then drops to a very low value. Such a behavior can be understood from the well-known behavior of reactive sputtering using a metal target where the increasing reactive gas ratio (O\textsubscript{2} ratio in this case) poisons (oxidizes) the target surface [52]. Up to the critical O\textsubscript{2} ratio, target surface maintains the metallic state so that the sputtered atoms are mostly metal, which then oxidized to the oxide film on the substrate. Increasing O\textsubscript{2} ratio enhances the resputtering effect due to the bombardment of negatively charged oxygen ions on growing film. In contrast, the Ru target surface is almost fully oxidized when the O\textsubscript{2} ratio was higher than the critical value, and sputtered materials are mostly oxidized Ru molecules, meaning that the oxidation of growing film on the substrate plays relatively minor role. Due to the generally very low growth rate for the case of 30 W, following experiments were performed with 60 W. The inset of Fig. 4.36 (a) shows the variations of Ru layer density with the deposition time for the O\textsubscript{2} ratios of 10.4 and 14.3 %, which is below and over the critical value, respectively. While the data in Fig. 4.36 (a) showed a substantially different Ru layer density (a 15-fold difference) under these two O\textsubscript{2} ratios, the actual growth rate, calculated from the slopes in the inset figure, was not so different (by only a factor of 2), meaning that the high O\textsubscript{2} ratio condition induced a quite long incubation time for the nucleation of the film. Also, the inset figure showed the Hf layer density of the HfO\textsubscript{2} film beneath the RuO\textsubscript{2} with O\textsubscript{2} ratio
of 14.3\% decreased slightly compared with that of 10.4\% case, suggesting the HfO\(_2\) films were slightly etched by 0.1~0.2nm during the long incubation period for RuO\(_2\) deposition. Figure 4.36 (b) shows the variations in the GAXRD spectra of the RuO\(_2\) films according to the O\(_2\) ratio. The deposited film was hexagonal Ru when the O\(_2\) ratio is 0, while other films show clear peaks corresponding to tetragonal RuO\(_2\) phase when the O\(_2\) ratio was \(>\sim\) 5\%. Furthermore, the intensities of (110) peak (2 theta \(\sim\) 28\(^\circ\)) and (101) peak (2 theta \(\sim\) 35\(^\circ\)) decreases and increases, respectively, with increasing O\(_2\) ratio. The inset of Fig. 4.36 (b) shows the variations in the grain size of the films estimated from the two XRD peaks using the Scherrer equation \(I = \frac{k \cdot \lambda}{\beta \cdot \cos \theta}, k = 0.9\) for arbitrary particles \[53\]. It can be understood the grain size is relatively small and constant up to the critical O\(_2\) ratio but abruptly increases when the O\(_2\) ratio increases over that value, which can be understood from the lower growth rate under this condition. These results indicate that O\(_2\) ratio during the deposition of RuO\(_2\) determine the growth rate as well as growth direction and grain size of the film that could affect electrical property.

Chemical properties of the films deposited under the O\(_2\) ratio of 0 \%, 3.2 \%, 10.4 \% and 14.3 \%, respectively, were estimated by XPS and AES. Figures 4.37 (a) and (b) show XPS spectra of Ru 3\(d\) and O 1\(s\) peaks, respectively, for Ru and RuO\(_2\) on SiO\(_2\) substrate. Here, the Ru and RuO\(_2\) films were \(\sim\) 10- and \(\sim\) 30-nm-thick, respectively. The XPS peak positions were calibrated using the deconvoluted C 1\(s\) peaks (284.5 eV) and Ru 3\(d_{5/2}\) peaks from the Ru and RuO\(_2\) samples. Figure 4.37 (a) shows that the films deposited under O\(_2\) containing environment showed the Ru 3\(d_{5/2}\) peak located at \(\sim\) 281.2 eV, which corresponds to the binding energy of Ru 3\(d_{5/2}\) in RuO\(_2\), while the film with zero O\(_2\) ratio showed Ru 3\(d_{5/2}\) peak locating at \(\sim\) 280 eV, which corresponds to metallic Ru [54].
Figure 4.36 Variations of (a) Ru layer density of RuO$_2$ films at 30 and 60 W as a function of O$_2$ ratio and (inset) Hf layer density for a given HfO$_2$ thickness and Ru layer density as a function of deposition time of RuO$_2$ electrodes, and (b) GAXRD spectra of as-deposited Ru (~10 nm) and RuO$_2$ (~30 nm) with various O$_2$ ratios and (inset) the variations in the grain size of the films estimated from the two XRD peaks using the Scherrer equation.
Slight shoulder intensity at \( \sim 281 \) eV suggests that the surface of the film was oxidized. O 1s peaks in Fig. 4.37 (b) revealed slightly different oxidation states of the films; the films show Ru-O bonding peaks as RuO\(_2\) and RuO\(_x\) (possibly RuO\(_3\)) phases at the binding energies of 529.2 eV and 530.6 eV, respectively. Interestingly, the film grown at higher O\(_2\) ratio shows the higher peak intensity at 530.6 eV, suggesting that the oxide film grown at lower O\(_2\) ratio contains higher portion of less stable hyperstoichiometric oxide, which is most evidently seen in for the case of 0\%. This is in accordance with the estimated Ru:O ratio from the XPS peak area ratio; the atomic Ru : O ratios of the RuO\(_2\) films with 3.2 \%, 10.4 \% and 14.3 \% O\(_2\) ratios were 1 : 1.87, 2.15 and 2.0, respectively. The hypostoichiometric composition of the RuO\(_2\) film grown under the O\(_2\) ratio of 3.2 \% could be understood from the insufficient oxygen content in the sputtering chamber. However, the higher oxygen content of the film grown at 10.4 \% than that of the film at 14.3\% suggests that the film grown at the condition of slightly lower O\(_2\) ratio than the critical value could have unstable structural and electrical properties as the gate metal. It appears that the RuO\(_2\) films dominantly formed by the oxidation of Ru metal layer have a tendency to contain hyperstoichiometric oxide component. On the other hand, the sputtering from the oxidized target surface, which must also contain the quite high RuO\(_3\) component, results in the stoichiometric RuO\(_2\) since the possibly sputtered out RuO\(_3\) molecules along with the desired RuO\(_2\) molecules (of course, molecules with several other meta-stable oxide forms must be present too) from the target are evacuated out due to their much higher vapor pressure. Therefore, the stable stoichiometric RuO\(_2\) film can be achieved under the condition of O\(_2\) ratio slightly higher than the critical value. The AES depth profiles shown in Figs. 4.37 (c) and (d) for the samples with the O\(_2\) ratio of
10.4 % and 14.3 % O$_2$, respectively, corroborate the XPS results. It can be understood that the RuO$_2$ layer with 10.4 % O$_2$ ratio has rather high oxygen concentration than that with 14.3 %. Abe et al. claimed that at the higher sputter-growth rate of RuO$_2$ film, the Ru atoms sputtered from the target react with oxygen on the substrate surface to form the RuO$_2$ films, while at the low growth rate, RuO$_2$ films are deposited by the sputtering of oxidized target surface [55].

![Figure 4.37](image)

Figure 4.37 (a) Ru 3$d$ and (b) O 1$s$ regions of the XPS spectra for Ru (~10 nm) and RuO$_2$ (~30 nm) with various O$_2$ ratios on SiO$_2$/Si, and the AES profiles of as-deposited RuO$_2$ films with O$_2$ ratios of (c) 10.4 % and (d) 14.3 % on SiO$_2$/Si.
Figure 4.38 shows cross-section TEM images of ~30 - 40 nm thick RuO₂ films with 10.4 % and 14.3 % O₂ ratio on SiO₂ (6nm)/Si stack. In order to reveal the different morphologies and grain shapes somewhat thicker films were selected for this analysis although the actual application requires a much lower thickness. TEM of RuO₂ films on HfO₂ dielectrics barely discerned the two layers. In the case of RuO₂ with 10.4 % O₂ ratio, the film appears to be composed of less clearly resolved columnar grains due to the possible involvement of amorphous-like regions. In contrast, the RuO₂ film grown with 14.3% O₂ ratio shows distinctive crystallization with well-developed columnar grain morphologies. Plan-view scanning electron microscopy (SEM) images shown in Figs. 4.38 (c) and (d) corroborate the TEM results. The larger grain size shown in Figs. 4.38 (b) and (d) also coincides with the XRD data shown in inset figure of Fig. 4.36 (b).

Figure 4.39 (a) shows the variations of $V_{FB}$ as a function of capacitance equivalent thickness (CET) of SiO₂ dielectric for the cases of RuO₂ gate with the O₂ ratio of 10.4 % and 14.3 % O₂, respectively. For comparison, the data for the Pt gate was also included. From the y-axis intercepts and slopes of the best-linear-fitted graphs, the work function difference ($\phi_m$) between gate (EWF) and Si substrate (5.1 eV), and fixed interface charge density ($Q_i$), respectively, were extracted [56]. The EWF of RuO₂ on SiO₂ with 10.4 % and 14.3 % O₂ ratio were estimated to be 5.29 and 5.37 eV, respectively, and that of Pt was 5.49 eV suggesting the high reliability of the present experiment. More importantly, the $Q_i$ level of SiO₂ dielectrics with RuO₂ gate with 10.4 % and 14.3 % O₂ ratios was $\sim3.8 \times 10^{11}$ and $\sim1.4 \times 10^{11}$ cm$^{-2}$, respectively, while that of Pt gate sample was as high as $\sim1.2 \times 10^{12}$ cm$^{-2}$. This means that the RuO₂ film grown with the O₂ ratio of 14.3% shows an optimum performance having a high enough EWF as the gate for p-type MOSFET and
minimized defect generation in the gate dielectric.

Figure 4.38 Cross-section TEM (a, b) and plan-view SEM (c, d) images of RuO$_2$ films with O$_2$ ratios of (a, c) 10.4% and (b, d) 14.3% on SiO$_2$/Si.

Figure 4.39 (a) also shows the variations for the samples with HfO$_2$ dielectrics. Due to the well-known Fermi level pinning effect, the EWFs of Pt and both RuO$_2$ films decreased to $\sim 5.1 - 5.2$ eV, but still the lower Q$_f$ and higher EWF were achieved from the RuO$_2$ with O$_2$ ratio of 14.3% ($\sim 9.8 \times 10^{10}$ and $\sim 7.3 \times 10^{10}$ cm$^{-2}$, 5.06 and 5.19 eV for the O$_2$ ratios of 10.4 and 14.3%). Figure 4.39 (b) shows the variation of the EOT as a function of physical oxide thickness (POT) of the HfO$_2$ film for the three metal gates.
While the bulk $k$ values, estimated from the slope of the best-linear-fitted graphs, are commonly 17, the EOT of RuO$_2$-gated films are generally lower than that of Pt-gated samples by $\sim$ 0.5 nm, which is in accordance with the results of previous section 4.3.3.1. The different O$_2$ ratio, however, did not bring about any notable difference in this EOT-POT plot. The inset figure shows the current density ($J_g$ measured at $V_{FB} - 1V$) vs. EOT performance. The RuO$_2$-gated HfO$_2$ films generally show a lower J level by $\sim$ two orders of magnitude compared with Pt-gated films, which is probably attributed to the scaled EOT as well as the lower damaging effect as revealed by the lower $Q_f$ level. However, the two different RuO$_2$ films did not show any notable difference in this regard despite the different EWF probably due to the $V_{FB}$ roll-off and Fermi level pinning effects.

Figure 4.39 (a) Plot of $V_{FB}$ vs. CET for various electrodes using terraced SiO$_2$ and HfO$_2$/terraced SiO$_2$ oxide, and (b) variation of EOT as a function of HfO$_2$ oxide thickness and (inset) plot of $J_g$ vs. EOT with various electrodes on HfO$_2$/Si.
4.3.3.3 RuO$_2$ metal gate on HfSiO

Until now, works on suppression of dead-layer effect and deposition condition (O$_2$ ratio) of RuO$_2$ films were investigated on HfO$_2$ as gate dielectrics. In order to understand the role of high-$k$ layer on EOT scaling using dead-layer shrinkage effect, RuO$_2$ (deposited at 10.4% O$_2$ ratio) electrodes were employed on various compositions of Hf$_x$Si$_{1-x}$O$_y$ (HfSiO) layers with the Si/(Hf + Si) ratio ranging from 0% (HfO$_2$) to 82% and metal-oxide-semiconductor (MOS) capacitors were fabricated. HfSiO dielectrics were studied in section 4.1 about dielectric constant and crystal structure from which Pt electrodes on HfSiO were used as reference data. As-deposited RuO$_2$ electrodes on HfSiO with several thicknesses were fabricated. Figure 4.40 (a) shows the plot of EOT as a function of HfSiO film thickness including HfO$_2$ and SiO$_2$ films for extraction of EOT IL thicknesses. Figure 4.40 (b) summarized the extracted dielectric constant (k) and EOT reduction amount by suppressing the dead-layer effect (i.e., EOT difference between RuO$_2$ and Pt electrodes) as a function of the Si/(Hf+Si) ratio of HfSiO, respectively.

As the Si/(Hf+Si) ratio is increased, the EOT reduction amount decreased gradually compared to ~ 0.5nm for HfO$_2$ up to Si/(Hf+Si) ratio of 57 % and then it reached almost to zero. This trend indicates that the dielectric constant play a key role in deadlayer suppression and the deadlayer effect disappeared due to the decrease of the dielectric constant as the ratio of Si/(Hf+Si) is increased, which is well coincident with previous Lee et al.’s first-principles approach report [37] that the interfacial effect was negligible in a Au/MgO (k~8) interface, while the local dielectric constant for a Ni/ZrO$_2$ (k~30) interface shows a signature of intrinsic dead layers.
Figure 4.40 (a) Variation of EOT as a function of SiO$_2$ and HfO$_2$ and HfSiO oxide thickness with Pt and RuO$_2$ (10.4% O$_2$) electrodes in MIS and (b) summary of the variation plot of EOT vs. thickness.

<table>
<thead>
<tr>
<th>Dielectric</th>
<th>EOT scaling amount (A)</th>
<th>Dielectric constant (k)</th>
</tr>
</thead>
<tbody>
<tr>
<td>HfO$_2$</td>
<td>~5.0</td>
<td>~17</td>
</tr>
<tr>
<td>7:1 (Si~16%)</td>
<td>~3.7</td>
<td>~14</td>
</tr>
<tr>
<td>1:1 (Si~57%)</td>
<td>~2.5</td>
<td>~8</td>
</tr>
<tr>
<td>1:3 (Si~80%)</td>
<td>0</td>
<td>~6</td>
</tr>
<tr>
<td>SiO$_2$</td>
<td>0</td>
<td>~3.5</td>
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</tbody>
</table>
4.3.4 Conclusion

In summary, the EOT of HfO$_2$ film can be scaled down by $\sim 0.5$ nm in the EOT range from 0.8 to 2.5 nm by adopting the RuO$_2$ metal gate compared with the standard Pt gate even without any scavenging effect of IL. This was attributed to the suppression of the dielectric dead-layer effect at the HfO$_2$/RuO$_2$ interface due to the possible ionic polarization of RuO$_2$ within the screening length of the electrode. It was also confirmed that the physical deposition process (sputtering) for the different types of electrodes did not induce any change in the physico-chemical and electrical properties of the underlying dielectric layer and interface with the Si. The estimated work function of RuO$_2$ on HfO$_2$ is $\sim 5.0$ eV suggesting the supreme performance of RuO$_2$ as the metal gate for p-type MOSFET. In addition, the effects of O$_2$ ratio during sputter-deposition of RuO$_2$ gate metal on the physical and electrical properties of the film as well as the underlying gate dielectrics were examined. The growth behavior follows the well-known reactive sputtering tendency; $\sim 13$ % O$_2$ ratio was the critical level below or over which the Ru target surface is not oxidized or oxidized. According to this change in the status of target, the RuO$_2$ metal gates with 10.4 % and 14.3 % O$_2$ ratio have hyperstoichiometric and stoichiometric compositions, which resulted in the EWF difference by $\sim 0.2$ eV.

However, although this work showed the suppression of the intrinsic deadlayer effect by using the RuO$_2$ metal gate, the controversial deadlayer suppression is still in need of additional verification. For example, deadlayer study with different noble metal gates, such as Au (gold), should be investigated with focusing on the metal to oxide interface and comparing it with the various metals including the conducting oxide.
4.4 Reference


[29] B. Coss, H.-C. Kim, F. S. Aguirre-Tostado, R. M. Wallace, and J. Kim,


V. Conclusions

The semiconductor industry has already converged on Hf-based oxides for the first generation CMOS products featuring high-\(k\) gate dielectrics and metal gate electrodes. However, even though various metal materials were already used on Hf-based oxides, there are still several crucial problems that need to be considered; an effective work function (EWF) modulation for adjusting the threshold voltage (\(V_T\)) of transistors and further scaling of equivalent oxide thickness (EOT), which is approximately 1.0 nm for the first generation high-\(k\)/metal gate device.

To meet continued EOT scaling until the turning point in device architectures, mainly three possible EOT scaling approaches are studied in this work: (1) a high-\(k\) material with \(k\)-value greater than that of HfO\(_2\) (so-called “higher-\(k\)”), (2) the physical thickness reduction of interfacial layer (IL) (so-called “scavenging”), (3) suppression of low-\(k\) dielectric layer between metals and dielectrics (so-called “deadlayer effect”).

Firstly, the relation between the permittivity and microstructures of atomic layer deposited Hf\(_{1-x}\)Si\(_x\)O\(_2\) (HfSiO) thin films with different Si concentrations as a function of post-deposition annealing (PDA) temperature was investigated. The relation between the permittivity and the microstructures of atomic layer deposited HfSiO films with various Si concentrations as a function of PDA temperature was systematically examined using MIS capacitor and HRTEM analysis. The permittivity of the crystallized HfSiO films with a Si concentration of \(~16\%) abruptly increased after PDA at 800°C, because of tetragonal phase formation with the help of an appropriate amount of Si in the film. However, it decreased after PDA at 1000°C, because the crystallization proceeds with
higher proportion of monoclinic HfO$_2$ phase due to more severe segregation of Si into the SiO$_2$ phase. In contrast, the permittivity of HfSiO films with a Si concentration of $\sim$57% increased considerably after PDA at 1000°C, because an appropriate Si concentration remained in the separated HfO$_2$ to form the tetragonal phase due to the initially high Si concentration. The electrical measurement showed that an optimized Si concentration ($\sim$16%) in the HfSiO film maintained promising electrical properties up to 900 °C. However, the PDA at 1000°C degraded the electrical performance severely irrespective of the Si concentration.

Secondly, lanthanum (La)-incorporated TiN metal gates, such as TiN/La/TiN (TLT) and TiLaN (TLN), on HfO$_2$/Si substrates were investigated focusing on the flat band voltage ($V_{FB}$) modulation for nMOS and IL scaling to almost zero. Especially, the multi-layer metal gate approach has several merits over the others such as lower process temperatures and scaling of the IL by the scavenging effect, which are both crucial for the gate last approach under the 22nm technology node. The maximum $V_{FB}$ modulation value of the TLT/HfO$_2$/Si stack was $-423$ mV compared to the $V_{FB}$ of the TiN single metal case, which is superior to that of TLN ($-247$ mV). This is because the TiN barrier layer in the TLT metal stack prevents interfacial oxidation. Both cases showed that La-incorporation into the films lowered the EWF value compared to the TiN metal gate by as much as $\sim$480 and $\sim$430 meV on SiO$_2$ and HfO$_2$, respectively, which is coincident with the $V_{FB}$ shift result. Both TLT and TLN gate metals effectively shrink the IL thickness to values below 0.5 nm by the IL scavenging effect which means that the La metal ions remove oxygen from the IL to decrease the overall EOT of the capacitor. In the case where the TLT metal gate was annealed at 600 °C for 30s, the IL thickness was almost zero and the
EOT was decreased to 0.8 nm even though the maximum temperature was limited to 600°C. Therefore, the La-inserted TiN metal gate process is a suitable candidate for fabricating n-type MIS devices in the gate-last approach, where high temperature annealing is rarely performed.

Thirdly, the influences of RuO$_2$ metal gate on the dielectric performance of high-$k$ HfO$_2$ film on Si substrate were examined. The EOT of HfO$_2$ film can be scaled down by $\sim$ 0.5 nm in the EOT range from 0.8 to 2.5 nm by adopting the RuO$_2$ metal gate compared with the standard Pt gate even without any scavenging effect of IL. This was attributed to the suppression of the dielectric dead-layer effect at the HfO$_2$/RuO$_2$ interface due to the possible ionic polarization of RuO$_2$ within the screening length of the electrode. The dielectric dead-layer effect of high-$k$ materials has been a topic for the very active theoretical and experimental research works. The dead-layer effect is inevitable as long as the screening length of any metal cannot be zero. The presence of the finite screening length conversely means that the electrode material within the screening length can experience the electric field, and the dipolar polarization can even be induced in the electrode within the screening length of such minimal thickness if there are polarizable ions. It was also confirmed that the physical deposition process (sputtering) for the different types of electrodes did not induce any change in the physico-chemical and electrical properties of the underlying dielectric layer and interface with the Si. The estimated work function of RuO$_2$ on HfO$_2$ is $\sim$ 5.0 eV suggesting the supreme performance of RuO$_2$ as the metal gate for p-type MOSFET.

Finally, the effect of O$_2$/($Ar+O_2$) flow ratio (O$_2$ ratio) during sputtered deposition on the physical and electrical properties of the RuO$_2$ metal gates were examined with
comparing Pt. The growth behavior follows the well-known reactive sputtering tendency; for the given sputtering power of 60 W, ~ 13 % O₂ ratio was the critical level below or over which the Ru target surface is not oxidized or oxidized. According to this change in the status of target, the RuO₂ metal gates with 10.4 % and 14.3 % O₂ ratio have hyperstoichiometric and stoichiometric compositions, which resulted in the EWF difference by ~ 0.2 eV. The stoichiometric RuO₂ film imposed almost no damaging effect to the SiO₂ and HfO₂ gate dielectrics. Adoption of RuO₂ gate decreased the EOT by ~ 0.5 nm and leakage current by ~ two orders of magnitude for the given EOT compared with the Pt-gated samples. Also, although this work showed the suppression of the intrinsic deadlayer effect by using the RuO₂ metal gate, the controversial deadlayer suppression is still in need of additional verification. For example, deadlayer study with several noble metal gates, such as Au and Pt, should be investigated with focusing on the metal to oxide interface and comparing it with the various metals including the conducting oxide.
List of Publications

1. SCI Journal

[1] 1st author

4. **Hyo Kyeom Kim**, Il-Hyuk Yu, Jae Ho Lee, Tae Joo Park, and Cheol Seong Hwang, "Controlling the work function and damaging effects of sputtered RuO$_2$ gate electrodes for sub-1 nm equivalent oxide thickness ", accepted in ACS Applied Materials & Interfaces (2013. 1)


[2] Co-author


2. **International Conference**

(1) 1$^{st}$ author


gates on ALD Hf$_{1-x}$Si$_x$O$_y$ gate dielectrics", ALD 2012, Dresden, Germany, June (17-20), June 18th (2012)-poster.


(ECS Transaction 2010 33 (3): 241-247)

(2) Co-author

12. Han Joon Kim, Min Hyuk Park, Yu Jin Kim, **Hyo Kyeom Kim**, Il-Hyuk Yu, and Cheol Seong Hwang, "Effect of Composition on the ferroelectric properties of Hf<sub>x</sub>Zr<sub>1-x</sub>O<sub>2</sub> thin film", KJC-FE09, Ulsan, Korea, August (07-10), August 8th (2012) - Poster.

11. Min Hyuk Park, Han Joon Kim, Yu Jin Kim, **Hyo Kyeom Kim**, Il-Hyuk Yu, and Cheol Seong Hwang, "Examination on the ferroelectricity in Hf<sub>x</sub>Zr<sub>1-x</sub>O<sub>2</sub> thin film", KJC-FE09, Ulsan, Korea, August (07-10), August 8th (2012) - Contributed Talk.


3. Domestic Conference

1) 1st author

2) Co-author


상보형 금속 산화 반도체 소자 (트랜지스터)의 성능을 향상시키기 위해 게이트 길이 및 산화막 두께를 지속적으로 감소 (스케일링)시켜 왔다. 하지만, 기존 실리콘 산화막의 경우 90nm 게이트 공정에 이르러서 산화막 두께의 한계에 도달하여, 추가적인 두께 감소는 게이트 누설전류 증가로 인하여 불가능하였다. 그래서, 계속적인 트랜지스터의 스케일링을 위하여, 등가 산화막 두께 (EOT)를 유지하면서 물리적인 두께를 증가시킬 수 있는 고유전율 산화막에 대한 연구가 진행되어 왔으며, 반도체 산업계는 이미 하프늄 기반의 고유전율 게이트 산화막을 도입하여 제품에 적용하고 있는 상황이다. 비록 금속 게이트와 하프늄 기반 고유전율 게이트 산화막이 이미 사용되고 있지만, 몇가지 중요 문제들은 지속적으로 연구가 필요하다. 그 중 트랜지스터 분극 전압 조절을 위한 유효 일함수 (EWF) 조절과 EOT의 추가적 감소가 있다. 평판형 트랜지스터에서 32nm 혹은 그 이하로 계속하여 게이트 길이를 감소하게 될 경우 쇼트 채널 효과를 억제하기 위해 서브 나노 두께로 EOT를 낮추어야 된다. 핀 구조 전계 효과 트랜지스터와 같이 소자 구조의 변화가 이러한 등가 산화막의 감소 요구를 다소 완화시켜 줄 수 있지만, 소자 구조의 변화가 도래하기까지 시간이 좀 더 걸릴 것으로 보인다.

이러한 소자 구조 변화 이전까지 계속되는 EOT의 감소 요구를 충족시키기 위해 물리적 두께 감소가 아닌 다른 접근 방법이 필요하게 되었다. 본 논문에서는 크게 세가지 방법이 연구되었으며, 그 방법으로는 (1) 하프늄 산화막보다 유전율이 높은 고유전율 산화막의 연구 (일명 higher-κ), 실리콘과 산화막 계면층의 감소 연구 (일명 scavenging 효과)와 금속 게이트와 산화막 계면의 저유전율층의 감소 연구 (일명 deadlayer 효과)가 있다.
첫번째로, 원자층 증착법으로 증착한 하프늄 실리페이트를 실리콘 조성과 후속 열처리 온도에 따른 유전율과 박막의 미세구조와 상관관계가 연구되었다. 고온 후속 열처리는 비정질 형태의 다량의 실리콘을 함유한 기지로부터 결정화된 하프늄 산화물을 상분리시킨다. 또한, 정방정상 (tetragonal phase)으로 결정화된 하프늄 산화막은 단사정상 (monoclinic phase)로의 결정화보다 더 높은 유전율을 가지게 되며, 적절한 실리콘 조성 (10~20%) 하에서 가장 높은 유전율을 가지게 된다. 결정화된 하프늄 실리페이트 산화막내에서 발생하는 결정화된 하프늄 산화물과 비정질 실리콘 산화막의 상분리는 후속 열처리 온도에 의해 변화하게 되며, 그 실리콘 조성은 상분리 정도 및 결정상을 좌우하게 된다. 그러므로, 하프늄 실리페이트가 가장 높은 유전율을 가지기 위한 최적의 열처리 온도는 해당 박막의 실리콘 농도에 의해 결정되어야만 한다.

두번째로, 앞에서 언급한 듯이 트랜지스터의 문턱 전압 조절에 중요 역할을 하는 금속의 일함수 조절과 게이트 산화막과 실리콘 계면층의 스케일링 (scavenging 효과) 관점에서 란타늄이 첨가된 타이타늄 질화막 (TiN/La/TiN: TLT)과 란타늄이 첨가된 타이타늄 질화막 (TiLaN: TLN) 금속 전극들이 연구되었다. 하프늄 산화막위에 TLT 금속 게이트를 적용할 경우 플랫 반도 전압 (V_{FB}) 이동이 최대 -423mV 가 이루어 졌으며, TLN 금속 게이트를 적용할 경우 최대 -247mV 가 이동하였다. 이것은 란타늄이 적층될 경우 상하의 타이타늄 질화막에 의해 산화가 억제되어 낮은 일함수를 유지하기 때문이다. 또한, 두 금속 게이트들의 EWF 를 산출하여 보아도 유사한 결과를 확인하였다. 더욱이, 두 금속 게이트들은 우수한 산화막과 실리콘 계면층의 스케일링 효과를 보여주었으며, 이는 란타늄 금속 원자들이 계면층의 산소를 끌어 올려 계면층의 실리콘 산화막이 제거됨으로써 가능하게 되었다. 이러한 Scavenging 효과를 이용하여, EOT 를 0.5 나노 미터 추가로
낮출 수 있었으며 이는 600℃ 이하의 낮은 후속 열처리만으로 이루어진 것이다.

세번째로, 하프늄 산화막 위에서 루테늄 산화물 금속 게이트를 이용하여 추가적인 EOT 스케일링에 관하여 연구되었다. 고유전율 산화물들은 박막의 두께가 얇아 질수록 박막 전체의 유전율이 낮아지는 현상을 보여주고 있는데, 이는 유전율이 높아 질수록 심하게 나타난다. 루테늄 산화물 금속 게이트를 적용시 그러한 현상(deadlayer 효과)이 억제되어, 하프늄 산화막의 EOT 를 0.5 나노 미터 정도 추가로 스케일링 가능하도록 하였다. 이는 하프늄 산화막과의 계면에서 루테늄 산화막 이온들의 분극 현상에 의한 것으로 추정된다. 또한, 루테늄 산화막은 우수한 전기 전도도와 높은 일함수를 보여주고 있어 p-타입 트랜지스터의 게이트에 사용하기에 적당하다 하겠다. 또한, 루테늄 산화막 증착시 산소와 아르곤의 비율을 조절하여 그 비율에 따른 루테늄 산화막의 성장 방향과 그레인 (grain) 크기 등의 물성과 전기적 특성에 관해 연구되었다. 산소 비율이 13 % 정도에서 루테늄 산화막의 성장 속도가 급속히 감소 하면서 (101) 방향의 그레인이 급성장하는 것을 확인하였고, 그 조건에서 일함수가 0.2 eV 정도 증가함을 확인하였다.

주요어 : 고유전율 게이트 산화막, 하프늄 산화물, 하프늄 실리케이트, 금속 게이트, 란타늄 금속 게이트, 루테늄 금속 게이트, 루테늄 산화물 금속 게이트, 스케빈징 효과, 데드레이어 효과.
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186