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Ph.D. DISSERTATION

Understanding the electrical contact characteristics in amorphous-In$_2$Ga$_2$ZnO$_7$ Thin Film Transistor and its vertical device applications

by

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Understanding the electrical contact characteristics in amorphous-In$_2$Ga$_2$ZnO$_7$ Thin Film Transistor and its vertical device applications

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Abstract

Amorphous oxide semiconductors (AOSs) have been widely researched for thin-film transistors (TFTs) in high performance display devices due to its transparency and superior carrier transport properties. Since the AOSs are composed of post-transition-metal cations which have a large wave function overlap with neighboring atoms in the s-orbitals, the electrical properties are not significantly altered from the atomically regular crystalline material even when in the amorphous structure. As a result, a high carrier density and mobility can be simultaneously obtained. Recently, it was reported that AOSs can be potentially utilized in low-voltage logic devices, as well as memory applications.

In this regard, the amorphous nature and high carrier mobility of In$_2$Ga$_2$ZnO$_7$ (a-IGZO) thin films, which can be achieved by simple sputtering processes at room temperature, attract a great deal of attention for this approach. In addition, the high performance of a-IGZO TFTs also allows them to be easily integrated with Si-based devices even at low processing temperature, which is another forte of this concept. However, despite these promising factors, research on applications for a-IGZO has mostly been focused on the development of thin-film transistors for display or planar-type devices. Furthermore, while there have been many efforts to improve the electrical performance of a-IGZO, only a few results have been reported about the device scaling or novel device applications. Although the issues related with scaling have not been highlighted for display devices, a proper understanding of the overall conduction mechanism is very important for new applications such as logic and memory devices. Therefore, it is very important to establish a concrete understanding of the device performance variation in
terms of device scaling and contact characteristics. Furthermore, to be implemented in novel devices applications, various device structures should be suggested and their electrical characteristics should be investigated.

In this dissertation, the operation characteristics of a-IGZO TFTs were investigated in detail. In addition, based on the understanding the operation characteristics, a vertically integrated TFT device (V-TFT) structure was suggested and a-IGZO V-TFTs with submicron channel length were fabricated using a sputtering-based low temperature process.

Firstly, to clarify the overall operation characteristics of amorphous In_{x}Ga_{y}ZnO_{z} (a-IGZO) amorphous oxide semiconductor thin film transistors (TFTs), a numerical simulation model was suggested. The localized states were considered in the simulation model and the influences of its energy-density profile within the channel layer were analyzed in terms of the transfer characteristics of a-IGZO TFTs. The origins of the device parameters such as threshold voltage, sub-threshold swing and mobility were investigated using this simulation model and its variation according to changes in material parameters were estimated. The simulation results were verified with experimental results and the transfer characteristics for various operation regimes were well reproduced by the simulation. From these results, the overall operation characteristics of a-IGZO TFTs were explained in detail.

In addition, using the transmission line method (TLM), the effects of device scaling are investigated by analysis of TFT electrical performance using an a-IGZO channel. Using the TLM, the channel characteristics independent of contact resistance were extracted for two different contact metals, Ti and Mo. Based on these results, the mobility characteristics
were compared in terms of devices scaling and contact structure in the source/drain overlap region. In addition, the transport characteristics according to the contact structure of the source/drain metal electrode were investigated in detail and the results were quantitatively evaluated by comparison with the simulation results. Furthermore, Asymmetric Schottky contact thin-film-transistors (ASC-TFTs) with an a-IGZO channel were fabricated, and their operation characteristics were examined. Ti, Ni and Pt were evaluated as source/drain metal, and the variations in device performance were analyzed in terms of energy level and bias polarity, which were carefully simulated to understand the influence of the contact properties on the device performance. Based on these results, by applying different metal for each source and drain metal, ASC-TFTs integrating TFTs and Schottky diodes were fabricated, which showed a rectification ratio of drain current higher than $10^8$ according to the bias direction. In addition, the transfer and output characteristics of ASC-TFTs were evaluated for various operation regimes, and the roles of the Schottky junction in device operation were studied in detail.

Finally, based on the understanding the operation characteristics of a-IGZO, a vertically integrated TFT device (V-TFT) structure was suggested and a-IGZO V-TFTs with submicron channel length were fabricated using a sputtering-based low temperature process. Furthermore, the effect of device geometry on device performance was examined in detail. The fabricated V-TFTs show well behaved transfer characteristics with an $I_{on}/I_{off}$ current ratio greater than $10^4$ and a threshold voltage of 1.7V. The influence of the vertical structure on device performance was analyzed in detail. In addition, current polarity characteristics that arise from different metal/a-IGZO contacts were also examined.

In this dissertation, fundamental operation characteristics of a-IGZO TFTs were
investigated and based on the understanding of operation characteristics, the novel devices structures were proposed and fabricated. By analyzing the operation characteristics of fabricated devices, novel devices application of AOSs TFTs were suggested.

Keywords: Amorphous oxide semiconductors (AOSs), amorphous In$_2$Ga$_2$ZnO$_7$ (a-IGZO), Thin-Film Transistor (TFTs), Vertical devices, Schottky contact

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1. Introduction

1.1. Overview

Amorphous oxide semiconductors (AOSs) have been widely researched for thin-film transistors (TFTs) in high performance display devices due to its transparency and superior carrier transport properties. Since the AOSs are composed of post-transition-metal cations which have a large wave function overlap with neighboring atoms in the s-orbitals, the electrical properties are not significantly altered from the atomically regular crystalline material even when in the amorphous structure. As a result, a high carrier density and mobility can be simultaneously obtained. [1]

Since the report of Hosono in 2004 on transparent and flexible thin-film transistors (TFTs) using amorphous-indium-gallium–zinc-oxide (a-IGZO), a-IGZO have received considerable attention in display applications, such as active-matrix liquid-crystal displays, active matrix organic light-emitting diodes, and flexible displays, due to their superior electrical performance compared with conventional AOSs TFTs. Recently, it was reported that AOSs can be potentially utilized in low-voltage logic devices, as well as memory applications.[2-4]

The amorphous nature and high carrier mobility of a-IGZO thin films, which can be achieved by simple sputtering processes at room temperature, attract a great deal of attention for this approach. [5,6] In addition, the high performance of a-IGZO TFTs also allows them to be easily integrated with Si-based devices even at low processing temperature.[6-8] However, despite these promising factors, research on applications for
a-IGZO has mostly been focused on the development of thin-film transistors for display or planar-type devices. Furthermore, while there have been many efforts to improve the electrical performance of a-IGZO, only a few results have been reported about the device scaling or novel device applications. Although the issues related with scaling have not been highlighted for display devices, a proper understanding of the overall conduction mechanism is very important for new applications such as logic and memory devices. Therefore, it is very important to establish a concrete understanding of the device performance variation in terms of device scaling and contact characteristics. Furthermore, to be implemented in novel devices applications, various device structures should be suggested and their electrical characteristics should be investigated.

In this dissertation, the authors attempt to clarify the effects of material characteristic variation on device operation with a numerical simulation model. A Pao-Sah model that considers the various localized states in the band gap was applied for this purpose and the operation characteristics of a-IGZO TFTs were investigated in detail. [9-13] In the device simulation models mentioned in this paper, the localized states that originate from donor like states near the valance band edge and acceptor like states near the conduction band edge were considered. The influence of these energy states were also analyzed in terms of the transfer characteristics of the device. It is well known that the distribution of localized states affects the transfer characteristics. However, there has been no systematic report on the correlation between the localized states of an a-IGZO TFT and its transfer characteristics. In this work, the change of mobility characteristics and threshold voltage ($V_{th}$) of the simulated transfer curves according to a variation in the localized states were analyzed and compared with experimental results.
In addition, using the transmission line method (TLM), the effects of device scaling are investigated by analysis of TFT electrical performance using an a-IGZO channel.[14-17] The advantages of the TLM are that it gives useful information and the physical meaning of the extracted parameters is easy to understand. Using the TLM, the channel characteristics independent of contact resistance were extracted for two different contact metals. Furthermore, the transport characteristics according to the different metal electrodes in the source/drain contact were investigated in detail, and the results are quantitatively evaluated by comparison with the simulation results. Based on these results, the mobility characteristics were compared in terms of devices scaling and contact structure in the source/drain overlap region. In addition, the transport characteristics according to the contact structure of the source/drain metal electrode were investigated in detail and the results were quantitatively evaluated by comparison with the simulation results. Furthermore, Asymmetric Schottky contact thin-film-transistors (ASC-TFTs) with an amorphous-In$_x$Ga$_{2}$ZnO$_7$ (a-IGZO) channel were fabricated, and their operation characteristics were examined. Ti, Ni and Pt were evaluated as source/drain metal, and the variations in device performance were analyzed in terms of energy level and bias polarity, which were carefully simulated to understand the influence of the contact properties on the device performance. Based on these results, by applying different metal for each source and drain metal, ASC-TFTs integrating TFTs and Schottky diodes were fabricated, which showed a rectification ratio of drain current higher than $10^8$ according to the bias direction. In addition, the transfer and output characteristics of ASC-TFTs were evaluated for various operation regimes, and the roles of the Schottky junction in device operation were studied in detail.
Finally, based on the understanding the operation characteristics of a-IGZO, a vertically integrated TFT device (V-TFT) structure was suggested and a-IGZO V-TFTs with submicron channel length were fabricated using a sputtering-based low temperature process. Furthermore, the effect of device geometry on device performance was examined in detail. The fabricated V-TFTs show well behaved transfer characteristics with an $I_{on}/I_{off}$ current ratio greater than $10^4$ and a threshold voltage of 1.7V. The influence of the vertical structure on device performance was analyzed in detail. In addition, current polarity characteristics that arise from different metal/a-IGZO contacts were also examined.

In this dissertation, fundamental operation characteristics of a-IGZO TFTs were investigated and based on the understanding of operation characteristics, the novel devices structures were proposed and fabricated.
1.2 References


2. Investigation of overall operation characteristics for the Amorphous-In$_2$Ga$_2$ZnO$_7$ Thin Film Transistor considering localized states using Pao-Sah model

2.1. Introduction

Amorphous oxide semiconductors (AOSs) have been widely researched for thin-film transistors (TFTs) in high performance display devices due to its transparency and superior carrier transport properties. Since the AOSs are composed of post-transition-metal cations which have a large wave function overlap with neighboring atoms in the s-orbitals, the electrical properties are not significantly altered from the atomically regular crystalline material even when in the amorphous structure.[1] As a result, a high carrier density and mobility can be simultaneously obtained. Recently, it was reported that AOSs can be potentially utilized in low-voltage logic devices, as well as memory applications.[2-4]

However, the device physics and operation principles of AOS devices are not clearly understood yet, and there have been only a limited amount of simulation reports on the role of localized traps in the band gap, as well as its modeling in terms of device operation.[5-7] It is well known that device parameters such as threshold voltage, sub-threshold swing and mobility are crucial to achieve high performance devices, and that an accurate prediction of device characteristics according to different material parameter systems is a key factor required to design an optimal integrated circuit. Unfortunately, although there have been some reports on device operation modeling for amorphous-
In$_2$Ga$_2$ZnO$_7$ (a-IGZO), there has been no suitable simulation model that could thoroughly describe its overall operation characteristics.

In this work, the authors attempt to clarify the effects of material characteristic variation on device operation with a numerical simulation model. A Pao-Sah model that considers the various localized states in the band gap was applied for this purpose. [5-7,10] Although there were some previous reports on a-IGZO TFT modeling based on 2-D simulations [6,7], to describe the localized states, these models require an extremely large simulation cost and it is difficult to screen out various parasitic effects. However, the Pao-Sah model is much faster in terms of calculation speed and the physical meaning of the applied parameters is easy to understand, which prevents any misinterpretations that may occur in a more complex model.[5] Furthermore, it describes the transfer curves very well with a relatively small number of simulation parameters. In the device simulation models mentioned in this paper, the localized states that originate from donor like states near the valance band edge and acceptor like states near the conduction band edge were considered. The influence of these energy states were also analyzed in terms of the transfer characteristics of the device. It is well known that the distribution of localized states affects the transfer characteristics. [13,14,17] However, there has been no systematic report on the correlation between the localized states of an a-IGZO TFT and its transfer characteristics. In this work, the change of mobility characteristics and threshold voltage ($V_{th}$) of the simulated transfer curves according to a variation in the localized states were analyzed and compared with experimental results. Since the $V_{th}$ and sub-threshold swing (SS) in a TFT is interrelated with the energy-density profile of localized states and the internal electric field variation of the a-IGZO channel, the role
that channel thickness ($T_{ch}$) plays in devices operation was also investigated. It is well known that a decreased $T_{ch}$ increases the $V_{th}$ and improves SS in a TFT. [8] However, although there have been explanations for $V_{th}$ differences with a certain reference, they fail to explain the absolute $V_{th}$ at a given $T_{ch}$. From the simulation works in this paper, it was observed that the energy-density profile of the localized states have a considerable influence on device characteristic variation according to $T_{ch}$. In addition, the origin of $V_{th}$ shift in a-IGZO TFTs was investigated from the numerical simulation model. According to these results, the overall device operation characteristics were investigated.
2.2. Experimental procedure

The model and procedure for the device simulation were explained in detail in section 3.1. For the experiment, heavily doped p-type silicon and 100nm-thick thermal SiO₂ were used for the gate electrode and gate dielectric, respectively, in the bottom gate type TFT. For the channel material, 20nm, 40nm, and 60nm thick a-IGZO films were deposited by RF magnetron sputtering at room temperature. After patterning the a-IGZO active layer by photolithography, the channel was wet-etched with diluted hydrofluoric acid. 100nm thick source/drain electrodes were deposited via sputtering and patterned by the conventional lift-off method. Ti was used for the source/drain electrodes to evaluate the electrical performance of the TFTs. The fabricated TFTs were annealed in air at 200°C for 1 hour to stabilize the contact resistance between the a-IGZO layer and the electrodes. A schematic cross-section of a bottom-gate-type a-IGZO and its optical image are shown in Fig. 2.1 (a). The channel length and width are 4μm and 20μm, respectively.

Fig.2.1. (a) Schematic crosssections of bottom-gate-type a-IGZO TFT and its optical view, (b) trap density of states for a-IGZO TFT
2.3. Simulation model

For device simulation, the solving procedures for the 1D Poisson’s equation followed the shooting method [5] and to describe the operation current, the Pao-Sah current formulation was used.[10] The gradual channel approximation simplifies the two-dimensional problem of a long channel thin-film transistor. It assumes that the variation of the electrical field along the channel direction (y-direction) is much less than the corresponding variation of the field perpendicular to the channel (x-direction) (See upper right Fig. of Fig. 2.1 (a)). With this approximation the Poisson’s equation becomes one-dimensional.

\[
\nabla^2 \phi = \frac{\partial^2 \phi}{\partial x^2} + \frac{\partial^2 \phi}{\partial y^2} = -\frac{\rho(x,y)}{\varepsilon \varepsilon_0} \quad \ldots (1)
\]

\[
\rho(x,y) = q N_d - q N_c \exp(-\frac{E_c - E_{FN}(y)}{kT}) - \int_{E_c}^{E_F} Q_a(E) f(E - E_{FN}(y))dE
\]

\[
+ \int_{E_c}^{E_F} Q_d(E)(1 - f(E - E_{FN}(y)))dE \quad \ldots (2)
\]

\[
E_{FN}(y) = E_F + q \phi(x,y) - q V_{DS}(y) \quad \ldots (3)
\]

\[
Q_a(E) = q \left[ g_{a1} \exp\left(\frac{E - E_c}{E_{a1}}\right) + g_{a2} \exp\left(\frac{E - E_c}{E_{a2}}\right) \right] \quad \ldots (4)
\]

\[
Q_d(E) = q \left[ g_{d1} \exp\left(\frac{E - E}{E_{d1}}\right) + g_{d2} \exp\left(\frac{E - E}{E_{d2}}\right) \right] \quad \ldots (5)
\]
As shown in Fig. 2.1(b), the localized states were considered to be comprised of donor like traps ($Q_d$) close to valance band edge and acceptor like traps ($Q_a$) close the conduction band edge. In this model, two kinds of $Q_a$ were considered; shallow acceptor like traps ($Q_{a1}$) and deep acceptor like traps ($Q_{a2}$). The $g_{ta1}$ and $E_{ta1}$ were the $Q_{a1}$ density and its energy slope, respectively. Similarly, the $g_{ta2}$ and $E_{ta2}$ were the $Q_{a2}$ density and its energy slope, respectively. The differences between $Q_{a1}$ and $Q_{a2}$ are that $Q_{a1}$ has a large trap density and sharp trap distribution while $Q_{a2}$ has a small trap density and gradual distribution. Similarly, in this model, two kinds of $Q_d$ were considered under the same rationale; shallow donor like traps ($Q_{d1}$) and deep donor like traps ($Q_{d2}$). The $g_{td1}$ and $E_{td1}$ were the $Q_{d1}$ density and its energy slope, respectively. Again, the $g_{td2}$ and $E_{td2}$ were the $Q_{d2}$ density and its energy slope, respectively. The differences between $Q_{d1}$ and $Q_{d2}$ are identical to the difference between $Q_{a1}$ and $Q_{a2}$. As the $E_F$ is derived from the charge neutrality condition, the $E_F$ is strongly dependent on the distribution of $Q_a$ and $Q_d$. In addition, the $Q_a$ distribution affects the variation of mobile electron density and therefore affects the transfer characteristics of the a-IGZO TFT. The influence of the distribution of $Q_a$ and $Q_d$ will be discussed later in detail.

The a-IGZO has a large fully ionized donor density ($N_d$) that typically ranges from $10^{14}$ to $10^{17}$ cm$^{-3}$. [7,8] The physical implication of $N_d$ is the number of donor like traps positioned above the $E_F$. In addition, $N_d$ is also known to include the hydrogen related shallow donor [18]. This type of TFT that has a large electron concentration at flat band condition is called a depletion-type TFT [7]. In this paper, the position of the Fermi level ($E_F$) was calculated by implementing the charge neutrality condition with considerations on the localized states, along with the conventional concepts mentioned above.
The specific model parameters used for the simulations are shown in Table 2.1., and were first determined from previous works [5-7,12] and then optimized by comparison with experimental results. These model parameters will be termed as ‘reference values’ from here on. The simulated value of $E_F$ from these calculations was $0.103\text{eV}$ from the $E_C$.

The simulation results of the 1-D Poisson’s equation for the potential, electron density, and total charge distributions are shown in Fig. 2.2 when the source – drain voltage ($V_{DS}$) and flat band voltage ($V_{FB}$) were assumed to be zero at $T_{ch}$ of 20nm, 40nm and 60nm. Here, position means the distance from a-IGZO/SiO$_2$ interfaces into the IGZO channel region. When a positive gate bias was applied, a large amount of electrons were accumulated in the channel and the thickness of the electron accumulation layer was in the order of 10nm. Therefore, the thickness of the electron accumulation layers was not limited by the physical thickness of $T_{ch}$ even in the 20nm thick a-IGZO channel. Furthermore, when a positive gate bias is applied, the band bending in the channel region was insignificant. Since the $E_F$ is located close to the conduction band edge, the mobile electrons could be easily accumulated at the a-IGZO/SiO$_2$ interfaces. As a result, in the accumulation condition the band bending in the a-IGZO channel was minimized and the gate bias is mostly applied to the gate dielectrics.

When a negative gate bias applied, the channel was depleted and channel potential decreased. Since the a-IGZO channel has a large amount of $Q_d$, positive fixed charges should be piled up in the channel and electrons should be depleted. However, as the a-IGZO channel is floated, after the channel is depleted, the back surface potential of a-IGZO channel is decreased according to gate bias. As the $T_{ch}$ increased, the band bending during negative gate bias application increased.
TABLE 2.1. Simulation model parameters

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$N_C$</td>
<td>$6.0 \times 10^{18}$</td>
<td>cm$^{-3}$</td>
<td>Effective conduction band DOS</td>
</tr>
<tr>
<td>$N_d$</td>
<td>$2.2 \times 10^{17}$</td>
<td>cm$^{-3}$</td>
<td>Fully ionized donor density</td>
</tr>
<tr>
<td>$G_{n1}$</td>
<td>$4.0 \times 10^{19}$</td>
<td>cm$^{-3}$/eV</td>
<td>Shallow acceptorlike trap density of state</td>
</tr>
<tr>
<td>$E_{a1}$</td>
<td>0.02</td>
<td>eV</td>
<td>Shallow acceptor like trap energy slope in conduction band edge</td>
</tr>
<tr>
<td>$G_{n2}$</td>
<td>$3.0 \times 10^{17}$</td>
<td>cm$^{-3}$/eV</td>
<td>Deep acceptor like trap density of state</td>
</tr>
<tr>
<td>$E_{a2}$</td>
<td>0.3</td>
<td>eV</td>
<td>Deep acceptor like trap energy slope in conduction band edge</td>
</tr>
<tr>
<td>$G_{d1}$</td>
<td>$1.0 \times 10^{20}$</td>
<td>cm$^{-3}$/eV</td>
<td>Shallow donor like trap density of state</td>
</tr>
<tr>
<td>$E_{d1}$</td>
<td>0.06</td>
<td>eV</td>
<td>Shallow donor like trap energy slope in valance band edge</td>
</tr>
<tr>
<td>$G_{d2}$</td>
<td>$3.0 \times 10^{18}$</td>
<td>cm$^{-3}$/eV</td>
<td>Deep donor like trap density of state</td>
</tr>
<tr>
<td>$E_{d1}$</td>
<td>0.55</td>
<td>eV</td>
<td>Deep donor like trap energy slope in valance band edge</td>
</tr>
<tr>
<td>$\varepsilon_r$</td>
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<td></td>
<td>Dielectric constant</td>
</tr>
<tr>
<td>$\mu$</td>
<td>22</td>
<td>cm$^2$/Vs</td>
<td>Electron mobility</td>
</tr>
<tr>
<td>$Q_{int}$</td>
<td>$1.0 \times 10^{12}$</td>
<td>cm$^{-2}$</td>
<td>Interface trap density</td>
</tr>
</tbody>
</table>
Fig 2.2. Simulation result of Poisson’s equation for 20nm, 40nm, 60nm thick IGZO, (a) channel potential distribution, (b) mobile electron density in channel and (c) total charge density for 20nm a-IGZO channel, (d),(e),(f) correspond to identical simulation results for a 40nm thick channel and (g),(h),(i) represent the same cases for 60nm
As the total amount of depletion charges are related with the overall amount of mobile carriers in the channel, it is easier to deplete a thin a-IGZO channel than to deplete a thick a-IGZO channel. This can be seen by the fact that the back surface potential of the 20nm thick a-IGZO channel at a given negative $V_{GS}$ is lower than that of the 60nm thick a-IGZO channel. As a result, the band bending in thick a-IGZO channels is larger than thin a-IGZO channels.

The total amount of mobile electron density estimated from the integration of corresponding variation of mobile electron density along the x-direction and the channel depletion voltage ($V_{TD}$) was defined as the $V_{GS}$ when the total mobile electron density is $10^6 \, \text{cm}^{-2}$. In Fig. 2.3 (a), $V_{TD}$ as a function of $T_{ch}$ are shown for various $N_d$ densities. In addition, in Fig. 2.3 (b) the mobile electron densities as a function of $V_{GS}$ are shown for various $T_{ch}$ and Figs. (e), (f) correspond to identical results for different $N_d$ values. As the $T_{ch}$ increased, the $V_{TD}$ decreased (absolute value increases). Similarly, as the $N_d$ increased, the $V_{TD}$ decreased. As the gate bias for electron depletion in the channel is related to the overall amount of mobile carriers in the channel, a larger gate bias should be required to deplete thicker a-IGZO TFTs and a-IGZO TFTs with larger $N_d$. When a large $N_d$ is assumed, the $V_{TD}$ should be negative when the $V_{FB}$ is zero. However, the $V_{FB}$ is affected by the interface states between the a-IGZO and SiO$_2$. If there are no interface traps, the $V_{th}$ of an a-IGZO TFTs should have a negative $V_{th}$ due to the reasons mentioned above. Therefore, a positive $V_{th}$ can be attributed to the $V_{FB}$ shift caused by the SiO$_2$/a-IGZO interface traps ($Q_n$). As the $E_F$ is located near the $E_C$ at the $V_{FB}$, the $Q_n$ should be filled with electrons. The $Q_n$ was assumed to be $1.0 \times 10^{12} \, \text{cm}^{-2}$ in the simulations to account for the positive $V_{th}$ observed in the experimental results.
Fig. 2.3. (a) $V_{TD}$ as a function of $T_{ch}$ and (b),(c),(d) correspond to mobile electron density as a function of $V_{GS}$ for various $T_{ch}$. (b) $N_d 1.1 \times 10^{17} \text{cm}^{-3}$, (c) $N_d 2.2 \times 10^{17} \text{cm}^{-3}$, (d) $N_d 4.4 \times 10^{17} \text{cm}^{-3}$.

Fig. 2.4. (a) $V_{FG}$ in terms of $T_{ch}$ and (b) total charge density in a-IGZO as a function of ($V_{GS} - V_{FB}$) for various $T_{ch}$.
Considering the amorphous nature of the a-IGZO channel, interface traps at the a-IGZO/SiO₂ interface should have a large amount, and the order of \(10^{12} \text{ cm}^{-2}\) seems to be a reasonable value.[14,16] Due to the presence of \(Q_{it}\), even when no external voltage is applied to TFTs, there should be a built-in electric field in the device and a subsequent compensation field should also be induced in the a-IGZO channel. To compensate this built-in potential, the bands in the a-IGZO are bent upward until the total charge density is equal to \(Q_{it}\). As the \(V_{FB}\) corresponds to the gate voltage that yields a flat energy band in the a-IGZO, from the plot of total charge density as a function of \((V_{GS} - V_{FB})\), \(V_{FB}\) can be calculated when the total charge density in the a-IGZO channel is equal to \(Q_{it}\). Fig. 2.4 shows the \(V_{FB}\) as a function of \(T_{ch}\). Interestingly, the \(V_{FB}\) decreased as the \(T_{ch}\) increased. Since the compensation charges are related with the overall amount of positive charge in the channel, the band bending to compensate the \(Q_{it}\) of a thick a-IGZO is smaller than that of thin a-IGZO which results in the smaller \(V_{FB}\) for a thick a-IGZO channel. However, it should be noticed that the \(V_{th}\) (\(V_{TD}\)) shift according to \(T_{ch}\) is more dependent on \(N_d\) than \(Q_{it}\). Interestingly, when \((V_{GS} - V_{FB})\) is positive, there was no significant variation in the total charge density near the interface region between the a-IGZO and SiO₂ (Figs. 2.2 (c), (f), and (i) and Fig. 2.4 (b)). As the thickness of the electron accumulation layer is less than 10nm, the variation of mobile charge density according to \(T_{ch}\) is insignificant. In the negative region of \(V_{GS} - V_{FB}\), \(V_{TD}\) increased (absolute value decreased) as \(T_{ch}\) increased since a larger amount of positive compensating charge (for the negative \(Q_{it}\)) is available at thicker \(T_{ch}\) for the given (negative) \(V_{GS}\).

To estimated the drain current (\(I_{DS}\)), the Pao-Sah current formulation were applied.[10] Based on the quasi-equilibrium approximation, the potential distributions are obtained by
solving the 1D Poisson’s equation and the mobile charges are calculated numerically by integration of the electron concentration in the channel region. To simulate the operation current, the potential distribution was extracted from equation 2 and accumulated electrons were calculated from equation 6.

\[ n(y) = \int_{0}^{T_{ch}} N_C \exp\left(-\frac{E_C - (E_{F_H} + q\phi(x, y) - qV_{DS}(y))}{kT}\right)dx \]  \( \text{(6)} \)

Following the Pao-Sah current formulation [10], the operation current is calculated by integrating the potential from the source to the drain \( (V_{DS}) \). As a result, the current flows along the channel region only. The drain current, including both drift and diffusion carrier transport in the channel can be expressed by

\[ I_{DS} = \frac{W}{L} \mu_{eff} \int_{0}^{V_{os}} n(y)dV \]  \( \text{(7)} \),

where \( \mu_{eff} \) is the effective mobility and \( L \) and \( W \) are the channel length and channel width, respectively. For the simulation, the saturation mobility at a \( V_{DS} \) of 20V extracted from the experimental results of the a-IGZO TFTs with a \( T_{ch} \) of 40nm was used for the \( \mu_{eff} \). The simulation results and experimental results were compared in the linear and saturation operation regimes for TFTs operation in the following section.
2.4. Simulation results and experimental verification

The experimental and simulation results for the transfer curves of the 40 nm-thick a-IGZO TFTs are shown in Fig. 2.5 (a) and the mobility characteristics for various $V_{DS}$ are shown in Fig. 5(b). The transfer characteristics for linear and saturated operation regimes are well reproduced by the simulation. In Fig. 2.5 (a), the simulation results and experimental data overlap almost exactly so that they cannot be discerned. The simulated mobility characteristics are higher than the experimental results at $V_{DS}$ of 0.1V and 10 V in Fig. 2.5 (b). This can be understood by the non-negligible contact resistance that exists in the actual TFTs. For the Ti electrode case, the carrier transport at the interface is most likely governed by the Schottky mechanism due to the non-negligible Schottky barrier and possible oxidation of Ti at the Ti/a-IGZO interface.[11] As a result, the effective voltage applied to channel is reduced by this contact resistance. Because Schottky limited contact resistances have a strong dependency on applied voltage, increasing the $V_{DS}$ reduced the contact resistance (When $V_{DS} = 20$ V, simulation reproduces the experimental results almost exactly). Since the contact resistances were not considered in this simulation, the simulation results are naturally higher than the experimental results for the lower $V_{DS}$.

For a $V_{DS}$ of 0.1V, the linear mobility equation was used while the saturation mobility equation was used for the $V_{DS}$ of 10V and 20V. When the $V_{DS}$ were 0.1V and 20V, the mobility characteristics showed saturation when plotted as a function of $V_{GS}$, which is quite normal. In the accumulation condition, the negative charges include the mobile electrons and electrons in $Q_a$. When the $V_{DS}$ was 10V, the $V_{GS}$ dependent mobility
characteristics showed a different profile from the other two cases. This can be understood by the difference in TFT operation in the linear operation regime and the saturation operation regime depending on the $V_{GS}$ for this $V_{DS}$. The transfer curve should follow the saturation regime when $(V_{GS} - V_{th})$ is smaller than $V_{DS}$, while the transfer curve should follow the linear operation regime when $(V_{GS} - V_{th})$ is larger than $V_{DS}$. For the saturation operation regime, $I_{DS}$ is proportional to $(V_{GS} - V_{th})^2$ and $\mu_{mea}$ is derived from $(d(I_{1/2})/dV)^2$ while for the linear operation regime, $I_{DS}$ is proportional to $(V_{GS} - V_{th})$ and $\mu_{mea}$ is derived from $dI/dV$. The saturation mobility equation was used to extract mobility values for the transfer curve at $V_{DS}$ 10V, and, thus, the $\mu_{mea}$ shows typical mobility characteristics when $V_{GS} - V_{th}$ was less than $V_{DS}$. However, when $(V_{GS} - V_{th})$ is larger than $V_{DS}$, although the transfer curve follows linear operation characteristics, the saturation mobility equation was still used, and as a result when $(V_{GS} - V_{th})$ is larger than 10V, the $\mu_{mea}$ decreased as $V_{GS}$ increased with a trend proportional to $(V_{GS} - V_{th})^{-1}$. It should be noted here that the inflection point is related to the $V_{th}$ and the simulation results reproduced these characteristics successfully.
Fig. 2.5. (a) Transfer curves of the 40nm thick a-IGZO TFTs and (b) mobility characteristics as a function of \((V_{GS} - V_{FB})\) for various \(V_{DS}\). (Lines and symbols are simulation and experimental results respectively.)
Since only mobile electrons in the channel contribute to channel conductivity, the mobility should be scaled by the ratio of the number of mobile electrons to the total number of induced charges as shown in equation 8. [13]

$$\mu_{\text{mea}}(V_{GS}) = \mu_{\text{eff}} \frac{n_{\text{tot}}(V_{GS})}{n_{\text{tot}}(V_{GS}) + Q_{\text{atot}}(V_{GS})} \ldots (8),$$

where $\mu_{\text{mea}}$ is the measured mobility at given $V_{GS}$ and $n_{\text{tot}}$ and $Q_{\text{atot}}$ are the total mobile charges and total trapped electrons in $Q_a$, respectively. Here, it should be noted that the $\mu_{\text{mea}}$ is strongly dependent on the $Q_{\text{atot}}$ distributions. Since the $Q_{\text{atot}}$ is strongly dependent on the energy-density distribution of acceptor like traps and the position of $E_F$, by analyzing the $\mu_{\text{mea}}$ according to $V_{GS}$, information on the $Q_a$ distribution can be achieved.

In Fig. 2.6, the mobility characteristics were estimated for a range of $Q_a$ distributions. As discussed previously, two kinds of acceptor like traps were considered. The $Q_{a1}$ trap has a high trap density and sharp trap distribution. In addition, most of the traps from $Q_{a1}$ are located above the $E_F$, and therefore its influence on the $V_{th}$ is insignificant. Since the $Q_a$ is negatively charged when electrons are trapped in it and neutral when electrons are de-trapped, most of the $Q_{a1}$ traps remain empty at the $V_{FB}$ because they locate above the $E_F$. However, when the $V_{GS}$ is increased, the band is bended downward and a substantial portion of $Q_{a1}$ becomes filled with electrons. Due to its high trap density, these acceptor like trap states strongly affect the shape of the $\mu_{\text{mea}}$-$V_{GS}$ profile in the accumulation condition according to equation 8.
Fig. 2.6. Mobility characteristics as a function of $V_{GS}$ in linear operation regime, for (a) various shallow acceptor like trap densities and (b) various energy slopes. The same profiles for (c) various deep acceptor like trap densities and (d) various energy slopes.
Fig 2.7. Mobility characteristics as a function of $V_{GS}$ in linear operation regime, for (a) various shallow donor like trap densities and (b) various energy slopes. The same profiles for (c) various deep donor like trap densities and (d) various energy slopes.
While $Q_{a1}$ affects the mobility characteristics at high $V_{GS}$, $Q_{a2}$ affects the $V_{th}$ and mobility slopes at low $V_{GS}$. Since $Q_{a2}$ has a low trap density and gradual energy slope and its distribution extends to energies that overlap with $E_F$, the distribution of these acceptor like traps affects the $E_F$. The $V_{th}$ was found to increase with increasing $g_{m2}$ and $E_{ta2}$. The $E_F$ is lowered by an increase in $Q_a$ which results in a $V_{th}$ increase. In addition, while the $Q_{a1}$ affects in high $V_{GS}$ region, the $Q_{a2}$ has an influence over the entire $V_{GS}$ range. As a result, following from equation 8, the $\mu_{mea}$ is affected by $Q_{a2}$ even at small $V_{GS}$ values.

In Fig. 2.7, the mobility characteristics were estimated for a variation of $Q_{d}$ distributions. As discussed previously, two kinds of donor like traps were considered. Since the energy level of $Q_{d1}$ is located far below from the $E_F$, these traps had no significant effects on the mobility characteristics. Because $Q_{d}$ is positively charged when electrons are removed and neutral when electrons are trapped, and because the energy level of $Q_{d1}$ is located far below the $E_F$, most donor like traps remain neutral at flat band. Furthermore, even when a negative $V_{GS}$ is applied, the $E_F$ cannot reach $Q_{d1}$. As a result, $Q_{d1}$ has no effect on the mobility characteristics. However, $Q_{d2}$ had a considerable influence on the mobility characteristics. As the $Q_{d2}$ distribution also extends to energy levels near the $E_F$, the distribution of $Q_{d2}$ affects the $E_F$. The $V_{th}$ was found to decrease as the $Q_{d2}$ density and its energy slope increased. In addition, its effects on mobility characteristics were the opposite to the case with $Q_a$. As the TFTs operation regime is in the accumulation condition and the $E_F$ is close to the $E_C$, the alterations from $Q_d$ were less effective compared to $Q_a$ in terms of TFT operation characteristics. This implies that changes in the mobility characteristics from variation in trap states are dominated by $Q_a$. Therefore, the $Q_a$ distribution and its density can be estimated by examining the profile of $\mu_{mea}$ as a
function of $V_{GS}$. Furthermore, the transfer characteristics of a-IGZO TFTs are also
governed by the $Q_a$ because as mentioned above, $Q_d$ is so far away from $E_F$ that it has
almost no influence on the transfer curve in accumulation mode.

The $V_{GS}$-$I_{DS}$ characteristics of a-IGZO TFTs with various $T_{ch}$ are shown in Fig. 2.8. The
transfer curves showed a general trend to shift in the positive direction as the $T_{ch}$
decreased, and the simulation results were consistent with experimental results for all
operation regimes. The $V_{th}$ shift according to a change in $T_{ch}$ was successfully reproduced
by these simulation models. As discussed in Fig. 2.4 (b), the $V_{TD}$ increased (absolute
value decrease) as the $T_{ch}$ increased, and the $V_{TD}$ was also increased (absolute value
decrease) when the $N_d$ increased. As the $V_{GS}$ required for electron depletion in the channel
is closely related to the overall amount of mobile carriers in the channel, a larger gate bias
is required to deplete a thicker a-IGZO TFTs. As a result, the $V_{th}$ for thin a-IGZO TFTs is
larger than the $V_{th}$ for thick a-IGZO TFTs (Higher negative voltage is necessary to deplete
the thicker channel).
Fig. 2.9. Mobility characteristics as a function of $V_{GS}$ for various $T_{ch}$. (a) linear mobility at $V_{DS}$ of 0.1V, (b) saturation mobility at $V_{DS}$ of 10V and (c) at $V_{DS}$ of 20V.
Fig. 2.9 shows the more detailed results on the mobility-$V_{GS}$ characteristics for three different $V_{DS}$ at various $T_{ch}$, which was already mentioned in Fig. 2.5 (b) briefly. Again, the simulation results reproduce experimental results very well except for the thinnest channel case. The mobility of the thinnest channel appears to be influenced by the back surface of the a-IGZO channel which is not passivated appropriately. [19] Therefore, the mobility increase after the channel is turned on with $V_{GS}$ is slower than the simulation, which did not take into account the back surface effect of channel. However, thicker channels are free from this adverse effect and simulations well coincide with the experimental results. As discussed before, the mobility characteristics are affected by the acceptor like trap distribution, and the simulation results for the $V_{DS}$ of 0.1V are higher than the measured experimental results since the contact resistances were not considered in this simulation. For a $V_{DS}$ of 10V, the gate voltage for maximum mobility was varied according to $T_{ch}$. It should be noted here that the inflection point in the mobility curves are related to the $V_{th}$ and the $V_{GS}$ for maximum $\mu_{mea}$ corresponds to the voltage when $V_{GS} - V_{th}$ is equal to $V_{DS}$. Because an increase in $T_{ch}$ causes a decrease in $V_{th}$, the $V_{GS}$ at maximum $\mu_{mea}$ was increased for thin a-IGZO TFTs.

For the 60nm-thick a-IGZO channel, the increase rate of mobility with increasing $V_{GS}$ after the channel was turned on slightly degraded compared to the case with 40nm-thick a-IGZO channel. This can be understood by the different internal electric fields that are induced as $T_{ch}$ changes. As the $T_{ch}$ increased, the internal electric field in the channel should be decreased because in a thick a-IGZO channel, the total charge variation in the channel according to surface band bending is larger than in thin a-IGZO channels. Therefore, according to Poisson’s equation, a larger electric field is applied to the
interface of a-IGZO and SiO₂ for the thin a-IGZO TFTs. In Fig. 10, the electric field at the interface of a-IGZO and SiO₂ (E_{int}) is shown as a function of gate bias for 20nm, 40nm, and 60nm a-IGZO layers. As the T_{ch} was increased, the E_{int} showed a decreasing profile. These results are concurrent to the results of reference 2.

Fig. 2.10. E_{int} as a function (V_{GS}-V_{FB}) for various T_{ch}
2.5. Summary

In this work, a numerical simulation model was suggested to clarify the effects of material characteristics on device operation in a-IGZO TFTs. The localized states from donor-like states near the valance band edge and acceptor-like states near the conduction band edge were considered and the influence of these energy states were also analyzed in terms of the transfer characteristics of the device. Based on this model, the overall operation characteristics of a-IGZO TFT was investigated. The key issues of the paper can be summarized as follows;

First, to understand the $V_{th}$ characteristics in an a-IGZO TFT, the band bending characteristics of the a-IGZO channel were reproduced by the simulation model. As the $V_{th}$ is related to the depletion of the a-IGZO channel and because the $V_{GS}$ for electron depletion in the channel is related with the overall amount of mobile carriers in the channel, a larger gate bias is required for thicker a-IGZO TFTs and a-IGZO films with larger $N_d$ values. As a result, the $V_{th}$ shifted to the negative direction when $N_d$ and $T_{ch}$ were increased. Furthermore, due to the non-negligible amount of $Q_{it}$, the origin of a positive $V_{th}$ is attributed to a positive $V_{FB}$ caused by $Q_{it}$.

Second, to estimate the $I_{DS}$ characteristics, the Pao-Sah current formulation was applied and the mobility characteristics were analyzed based on these simulation results. The mobility characteristics were extracted from the simulated transfer curve using conventional mobility equations and the results were compared in terms of $T_{ch}$ and trap distribution in the sub-gap states. As only the concentration of mobile electrons in the channel attribute to the channel conductivity, the mobility should be scaled by the ratio of
the number of mobile electrons to the number of total induced charges. Furthermore, since the $Q_{\text{tot}}$ is strongly dependent on the energy-density distribution of acceptor like traps and the position of $E_F$, by analyzing the $\mu_{\text{mea}}$ according to $V_{GS}$, information on the $Q_a$ distribution can be achieved. As the $E_F$ is positioned close to $E_C$, the influence of $Q_d$ distribution was negligible compared to $Q_a$ distributions because they position near the valence band edge.

Third, to investigate the device performance variation according to $T_{ch}$, the transfer characteristics of a-IGZO TFTs with various $T_{ch}$ were estimated. As the $T_{ch}$ affects the internal band bending characteristics, the improvement of sub-threshold swing in thin a-IGZO TFTs can be attributed to the increased internal electric field in thin a-IGZO TFTs.

In conclusion, the effects of material characteristic variation on the device operation of a-IGZO TFTs were clarified with a numerical simulation model. The simulation results were verified with experimental results and the transfer characteristics for various operation regimes were well reproduced by the simulation. From these results, the overall operation characteristics of a-IGZO TFTs were understood in detail.
2.5. References


3. Controlling the threshold characteristics of amorphous-In$_2$Ga$_2$ZnO$_7$ Thin-Film Transistors with ultra-thin Al$_2$O$_3$ layer deposited by atomic layer deposition

3.1. Introduction

Amorphous oxide semiconductors have been widely researched for thin-film transistors (TFTs) in high performance display devices due to its transparency and superior carrier transport properties. Since the AOSs are composed of post-transition-metal cations which have a large wave function overlap with neighboring atoms in the s-orbitals, the electrical properties are not significantly altered from the atomically regular crystalline material even when in the amorphous structure. As a result, a high carrier density and mobility can be simultaneously obtained when compared with conventional amorphous silicon TFTs. Recently, it was reported that AOSs can be potentially utilized in low-voltage logic devices, as well as memory applications.[1-3]

Although there were some reports about the initial results for the integrated circuit, to be implement the commercially viable devices, there were still many issues to be solved. One of main issue for the application is the devices parameters such as threshold voltage ($V_{th}$) cannot be controlled which is a key factor required to design an optimal integrated circuit. As the a-IGZO TFTs could not be adopted the ion implantation that was commonly used in Si-based electronic devices to adjust the $V_{th}$, it was difficult to control the $V_{th}$ of a-IGZO TFTs for their circuit design criteria. Although there have been explanations for $V_{th}$ differences depending on process condition with a certain reference,
they failed to control the $V_{th}$ independently of conventional fabrication process of a-IGZO TFTs. [4,5]

In this regard, in this work, the performance variation of a-IGZO TFTs according to the thickness of thin Al$_2$O$_3$ passivation layer (<3nm) deposited by Atomic Layer Deposition (ALD) were monitored and their origin of performance variation were investigated. Interestingly, the $V_{th}$ was changed according to the ALD deposition cycle systematically while the variation of mobility characteristics was insignificant. This could be a viable solution to adjust the $V_{th}$ characteristics of a-IGZO TFTs. The variation of material characteristics of a-IGZO channel according the Al$_2$O$_3$ deposition cycle were investigated and the origin of $V_{th}$ shift in a-IGZO TFTs was investigated in detail.

The ultimate goal of this project is to fabricate an integrated circuit with amorphous oxide semiconductor (AOS), and this work reports the initial results of adjusting the devices parameters for the integrated circuit design.
3.2. Experimental Procedure

In this work, the a-IGZO TFT and Si/a-IGZO junction diode were fabricated. To investigate the operation characteristics of a-IGZO TFTs according to ALD deposition cycles, the a-IGZO TFTs with bottom gate structure were fabricated. Heavily doped p-type silicon and 100nm-thick thermal SiO₂ were used for the gate electrode and gate dielectric, respectively, in the bottom gate type TFT. For the channel material 60nm thick a-IGZO films were deposited by RF magnetron sputtering at room temperature. The channel thickness was measured using a spectroscopic ellipsometry (M-2000, J.A. Woollam). After patterning the a-IGZO active layer by photolithography, the channel was wet-etched with diluted hydrofluoric acid. 100nm thick source/drain electrodes were deposited via sputtering and patterned by the conventional lift-off method. The channel width (W) and the channel length(L) were fixed at 20 μm and 3 μm, respectively. Ti was used for the source/drain electrodes and thin Al₂O₃ was deposited by ALD at 150°C as a passivation layer. The precursor and oxygen source were trimethylaluminum (TMA) and O₃, respectively. The fabricated TFTs were annealed in air at 200°C for 1 hour to stabilize the contact resistance between the a-IGZO layer and the source/drain electrodes. The measurement was performed using a Hewlett-Packard 4155 semiconductor parameter analyzer at room temperatures.

To analyze the depletion capacitance, a-IGZO/p-type silicon junction diode fabricated. Heavily doped p-type silicon were used for the p-type semiconductor and after hydrofluoric acid cleaning the silicon, 60nm thick a-IGZO films were deposited by RF magnetron sputtering at room temperature. Thin Al₂O₃ was deposited by ALD at 150°C as
a passivation layer and 100nm thick Ti electrodes were deposited via sputtering and patterned by the conventional lift-off method. After patterning the a-IGZO active layer by photolithography, a-IGZO active layer was wet-etched with diluted hydrofluoric acid. Depletion capacitance was measured using the two frequency method (10kHz, 100kHz) and the measurement was performed using a Hewlett-Packard 4155 semiconductor parameter analyzer at room temperatures. In Fig. 3.1 (b), the schematic cross sections of fabricated devices were shown.

![Fig. 3.1. Schematic cross section of fabricated devices. (a) a-IGZO Thin-Film Transistor, (b) a-IGZO junction diode](image)
3.2. Results and discussions

The transfer curves (I_{DS} – V_{GS}) for fabricated devices and V_{th} characteristics for the different ALD deposition cycles are shown in Fig. 3.2 and its device parameters are shown in Fig. 3.3. The V_{th} was defined the V_{GS} at the I_{DS} of 10nA, the saturation mobility (\mu_n) was estimated following the Eq. (1) at the V_{DS} of 20V.

\[ \mu_n = \frac{2L}{WC_{ox}} \left( \frac{d\sqrt{I_{DS}}}{dV_{GS}} \right)^2 \]  

(1)

Interestingly, the transfer curves show a general trend of negative shift as the ALD cycle number increases. After the 30 deposition cycles of ALD Al_2O_3, the V_{th} of fabricated devices was up to -14.2V while the V_{th} of reference device was 1V. The mobility characteristics showed no notable change with the ALD cycle numbers. The estimated saturation mobility of fabricated devices were ~13 cm^2/Vs. In addition, as the ALD deposition cycle increased the sub-threshold swing increased. Since the \mu_n is related with the acceptor-like trap distribution in a-IGZO channel while the V_{th} is related with mobile electron density in a-IGZO channel, the experimental results represents the change of mobile electron density in a-IGZO channel without the change of acceptor-like trap distribution. It is well known that the acceptor-like trap distributions are thought to originate from the disorder of metal ion s-band, while the oxygen p-band disorder mainly contributed to the donor-like trap distribution.[6,7] Therefore, ALD Al_2O_3 deposition induced the variation of oxygen related bonding in a-IGZO channel.
Fig. 3.2. The transfer characteristics ($I_{DS} - V_{GS}$) of fabricated devices in terms of ALD Al$_2$O$_3$ deposition cycles.

Fig. 3.3. The variations of (a) the $V_{th}$ /sub-threshold swing characteristics and (a) the mobility characteristics in terms of ALD Al$_2$O$_3$ deposition cycles.
However, it is unclear the origins of variation in a-IGZO channel in terms of ALD Al$_2$O$_3$ deposition, therefore, in this work, the bulk properties of a-IGZO were investigated. Hosono et al. reported that the dielectric function of a-IGZO films was dependent on the bulk properties [8]. Therefore, to analyze the bulk property variation of a-IGZO in terms of ALD Al$_2$O$_3$ deposition cycle, the optical characteristics estimated from spectroscopic ellipsometry (SE). To estimate the material characteristics, Tauc-Lorentz model were employed and the dielectric function is expressed as

\[
\varepsilon(E) = \varepsilon_\infty + \varepsilon_{TL}(E) + \varepsilon_{pole}(E),
\]

\[
\varepsilon_{TL}(E) = \varepsilon_{TL,1} + i\varepsilon_{TL,2},
\]

\[
\varepsilon_{TL,1}(E) = \begin{cases} 
\frac{A_{TL}E_{g,TL}B_r(E - E_{g,TL})^2}{(E^2 - E_{g,TL}^2)^2 + B_r^2E^2} & E > E_g \\
0 & E \leq E_g 
\end{cases}
\]

\[
\varepsilon_{pole}(E) = \frac{A}{E_p^2 - E^2}.
\]

where the fitting parameters $A_{TL}$, $E_{0,TL}$, $B_r$, and $E_{g,TL}$ are the amplitude, transition energy, broadening, and Tauc gap of Tauc-Lorentz model, respectively. In addition, $A$ and $E_p$ are the amplitude and peak position of Lorentz pole, respectively. The real part of the dielectric function ($\varepsilon_{TL,1}$) is then obtained by using the Kramers-Kronig integration. In addition, following the previous results, the $E_{0,TL}$ of a-IGZO channel was fixed 3.7eV during the fitting procedure.[8] Fitting results for the a-IGZO are shown in Fig. 3.3(a) and the extracted parameters are shown in Table 3.1.
Table 3.1. Fitting results for a-IGZO film according to the ALD Al₂O₃ deposition cycle. The E₀,TL was fixed 3.7eV.

<table>
<thead>
<tr>
<th></th>
<th>ε∞</th>
<th>A(eV²)</th>
<th>E_p (eV)</th>
<th>A₁₁(eV)</th>
<th>E_p₁₁(eV)</th>
<th>B_r(eV)</th>
<th>E_g,TL(eV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ref.</td>
<td>1.869</td>
<td>32.5</td>
<td>7.653</td>
<td>112.56</td>
<td>3.7eV</td>
<td>5.3</td>
<td>3.16</td>
</tr>
<tr>
<td>Al₂O₃ 10cycle</td>
<td>1.845</td>
<td>30.7</td>
<td>7.467</td>
<td>114.7</td>
<td>3.7eV</td>
<td>4.94</td>
<td>3.18</td>
</tr>
<tr>
<td>Al₂O₃ 20cycle</td>
<td>1.856</td>
<td>29.3</td>
<td>7.41</td>
<td>114.8</td>
<td>3.7eV</td>
<td>4.95</td>
<td>3.18</td>
</tr>
<tr>
<td>Al₂O₃ 30cycle</td>
<td>1.857</td>
<td>28.4</td>
<td>7.36</td>
<td>115.1</td>
<td>3.7eV</td>
<td>4.96</td>
<td>3.18</td>
</tr>
</tbody>
</table>

Fig. 3.4. Dielectric functions of a-IGZO films extracted from the optical model analysis. The ε₁ and ε₂ denote the real and the imaginary parts of the dielectric functions, respectively.
The estimated $E_{\text{g,TL}}$ was 3.16 eV which is corresponding with the pervious works. [9] This suggests that the fitting results in this works are corrects. As shown in Fig. 3.3 (b) and Table 3.1, the material characteristics according to ALD Al$_2$O$_3$ deposition cycle were insignificant. These results represent that the bulk property variation of a-IGZO in terms of ALD Al$_2$O$_3$ deposition cycle was insignificant. However, as shown in Fig. 3.2, the $V_{\text{th}}$ characteristics of TFTs according to the ALD Al$_2$O$_3$ deposition cycle showed notable change. These results show that the $V_{\text{th}}$ variation of TFTs was affected by the insignificant change in a-IGZO channel which could not be monitored even in SE.

In order to understand the bonding structure of a-IGZO films, X-ray photoelectron spectroscopy (XPS) were used. The chemical state of In, Ga, Zn in the a-IGZO film according to the ALD Al$_2$O$_3$ deposition cycle was examined using XPS. Fig. 3.4 shows the XPS spectra of the In 3d$_{5/2}$, In 4d$_{3/2}$, Zn 3p$_{3/2}$, Ga 3d$_{5/2}$ according the ALD Al$_2$O$_3$ deposition cycle numbers. To calibrate the photo-electron binding energy, the C 1s peak for C–C bonds was assigned to 284.5 eV. As the ALD Al$_2$O$_3$ deposition cycle increase, binding energy of In 3d$_{5/2}$, In 4d and Zn 3p$_{3/2}$ shift to lower binding energy. As the Al$_2$O$_3$ thickness increases, peak intensity decreased due to the increase of Al$_2$O$_3$ thickness on top of a-IGZO film. However, the peak shifts to lower binding energy according to the increase of ALD Al$_2$O$_3$ deposition cycles were clearly shown. It is well known that the peak shift to lower binding energy indicates that metal ions are in oxygen deficient environment. These results represent the direct relationship between oxygen vacancy concentration and the number of ALD Al$_2$O$_3$ deposition cycles.
Fig. 3.5. XPS spectra of a-IGZO film in terms of ALD Al$_2$O$_3$ deposition cycle numbers.
It is well known that the increase of oxygen vacancy is cause of increase mobile electron density while the density of oxygen vacancy is insignificant compared with the density of oxygen which is bonding with metal ions.[11] As a result; the density variation of oxygen vacancy was not monitored in SE while the electrical characteristic was changed significantly.

To verify the increase of mobile electron density, a-IGZO and Si junction diode was fabricated and the depletion capacitance was measured. The depletion capacitance is directly related with mobile electron density and the large depletion capacitance means the large electron density in a-IGZO channel. As the doping level of p-type Si was ~ $10^{19}$ cm$^{-3}$ which was much larger than the mobile electron density in a-IGZO channel, the depletion width in p-type Si was ignored. Since there are many recombination centers in a-IGZO channel due to the amorphous nature, the depletion capacitance could not be measured with conventional CV curves. Therefore, to estimate the depletion capacitance, two frequency method was applied to eliminate the leakage current effects on capacitance value. [10] The advantage of two frequency method is that the accurate capacitance can be measure even in the high leakage current. Measuring the capacitance and dissipation at two different frequencies, the capacitance can be described following the equations

$$C = \frac{f_1^2C_1(1 + D_1^2) - f_2^2C_2(1 + D_2^2)}{f_1^2 - f_2^2}$$  \hspace{1cm} (1)$$

where $C_1$ and $D_1$ refer to the values measured at the frequency $f_1$ and $C_2$ and $D_2$ refer to the values measured at the frequency $f_2$.  

4 5
In addition the parasitic series and parallel resistance can be described following equations.

\[
R_p = \frac{I}{\sqrt{\omega^2 C_i (I + D_j^2) - \omega^2 C_j^2}} 
\]

\[
R_s = \frac{D_j}{\omega C_j (I + D_j^2)} - \frac{R_p}{I + \omega^2 C_j^2 R_p^2} 
\]

In Fig. 3.6(a) the equivalent circuit was shown and the depletion capacitance and parallel resistances were shown in Fig. 3.6 (b), (c) and (d). As the ALD Al₂O₃ deposition cycle increased, the depletion capacitance increased and the parallel resistance decreased. When the mobile electron density increased, the depletion width should be decreased and as a result, the depletion capacitance should increase. Furthermore, the decrease of depletion width was causes of decrease in parallel resistance. From these results, the ALD Al₂O₃ deposition causes of the increase mobile electron density in a-IGZO channel.
Fig. 3.6. (a) The equivalent circuit of fabricated a-IGZO/Si junction diodes. (b) The depletion capacitance, (c) Parallel resistance and (d) series resistance.
3.4 Summary

In this work, the performance variations of a-IGZO TFTs according to ALD Al₂O₃ deposition cycle were investigated. As the ALD Al₂O₃ deposition cycles increase, the $V_{th}$ show a general trend of negative shift according to the ALD Al₂O₃ deposition cycle while the $\mu_{n}$ characteristics was independent of ALD Al₂O₃. To estimate the origin of these characteristics, the optical characteristics and binding energy were analyzed by the SE and XPS, respectively. For the SE analysis, there was no significant difference according to the ALD Al₂O₃ deposition cycles. These results show that the $V_{th}$ variation of TFTs was affected by the insignificant change in a-IGZO channel which could not be monitored even in SE. However, for the XPS analysis, as the ALD Al₂O₃ deposition cycle increase, binding energy of In 3d₅/₂, In 4d and Zn 3p₃/₂ shift to lower binding energy, which represent that the metal ion is in oxygen deficient environments. These results show the direct relationship between oxygen vacancy concentration and the number of ALD Al₂O₃ deposition cycles. In addition, since the increase of oxygen vacancies are the causes of increase in mobile electron density, it is natural to understand the ALD Al₂O₃ causes of increase in mobile electron density. To verify the increase of mobile electron density, a-IGZO and Si junction diode was fabricated and the depletion capacitance was measured. As the ALD Al₂O₃ deposition cycle increased, the depletion capacitance also increased. Form these results, it was verified that the ALD Al₂O₃ process causes of increase in mobile electron density.
3.5. References


4. Performance variation according to device structure and the source/drain metal electrode of Amorphous-In$_2$Ga$_2$ZnO$_7$ Thin Film Transistors

4.1. Introduction

Thin-film transistors (TFTs) based on amorphous-indium-gallium–zinc oxide (a-IGZO) have received considerable attention in display applications, such as active-matrix liquid-crystal displays, active matrix organic light-emitting diodes, and flexible displays, due to their superior electrical performance compared with conventional amorphous silicon TFTs. It was recently reported that a-IGZO also have the potential to be used in logic devices and memory applications [1-3]. However, scaling is inevitable in these devices; as scaling progresses, the influence of device structure on its electrical performance becomes more prominent. Since a-IGZO TFTs are typically accumulation/depletion devices (lacking p-n junctions), the contact property between the source/drain metal and the a-IGZO channel plays an important role. This becomes even more important in highly scaled devices because the portion of the contact resistance over the total resistance increases as the channel length decreases. Therefore, it is very important to establish a concrete understanding of the device performance variation in terms of device scaling and contact characteristics between the a-IGZO and various metal electrodes for these systems to be implemented in new devices applications [4-7]. However, while there have been many efforts to improve the electrical performance of a-IGZO, only a few results have been reported about the device scaling. Although the issues related with scaling have not been highlighted for display devices, a proper understanding of the overall conduction...
mechanism in scaled devices is very important for new applications such as logic and memory devices.

In this work, using the transmission line method (TLM), the effects of device scaling are investigated by analysis of TFT electrical performance using an a-IGZO channel. The advantages of the TLM are that it gives useful information and the physical meaning of the extracted parameters is easy to understand. Using the TLM, the channel characteristics independent of contact resistance were extracted for two different contact metals, Ti and Mo. Furthermore, the transport characteristics according to the different metal electrodes in the source/drain contact were investigated in detail, and the results are quantitatively evaluated by comparison with the simulation results.
4.2. Experimental procedure

Heavily doped p-type silicon and 100-nm-thick thermally grown SiO$_2$ were used for the gate electrode and gate dielectric, respectively. For the channel material, a 40-nm-thick a-IGZO film was deposited by radio frequency magnetron sputtering at room temperature [8, 9]. The a-IGZO active layer was patterned by photolithography and wet-etched with a diluted solution of hydrofluoric acid. The channel width (W) was fixed at 20 µm and the channel length (L$_G$) was varied from 3 to 38 µm. Ti or Mo source/drain electrodes (100 nm thick) were deposited via sputtering and patterned using the conventional lift-off method. The sputtering process conditions of Ti and Mo are shown in Table I. The fabricated TFTs were annealed in air at 300°C for 1 hour to stabilize the contact resistance between the a-IGZO layer and the electrodes. The current in the TFT structures was simulated using a SILVACO technology computer-aided design (TCAD) simulator [10, 11]. Detailed simulation parameters are discussed in the following section. The electrical properties of the fabricated devices were measured using a Hewlett-Packard 4155 semiconductor parameter analyzer at room temperature.

Table 4.1. The Sputtering process conditions for each source/drain metal electrode

<table>
<thead>
<tr>
<th>Process Time</th>
<th>Ti Process Time</th>
<th>Mo Process Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>RF Power</td>
<td>300 W</td>
<td>250 W</td>
</tr>
<tr>
<td>Pressure</td>
<td>5 mTorr</td>
<td>5 mTorr</td>
</tr>
<tr>
<td>Ar Flow Rate</td>
<td>40 sccm</td>
<td>40 sccm</td>
</tr>
</tbody>
</table>
4.3. Results and discussion

In Fig. 4.1, the transfer curves (variation of source – drain current ($I_{DS}$) vs. gate voltage ($V_{GS}$)) are shown for various $L_G$ for different source/drain metal electrodes. To investigate the channel characteristics, a small drain voltage ($V_{DS} = 0.1$ V) was used to exclude any adverse currents that can be observed at higher drain voltages [7]. The inset Figs. show the same graphs in a linear scale. The TFTs show well-behaved transfer characteristics with a large on/off current ratio ($>10^5$) and a reasonable sub-threshold swing ($<1$ V/dec) even at a small $V_{DS}$. The saturation current decreases with increasing $L_G$ due to increased channel resistance. Although different metals were used for source/drain electrodes, the $I_{DS}$ characteristics were almost identical when $V_{GS}$ was sufficiently high. However, the Ti metal electrode showed superior $I_{DS}$-$V_{GS}$ characteristics in the sub-threshold operation regime compared to the Mo electrode. Since the sputtering process time of the Mo electrode was much longer than that of the Ti electrode (10 min for Mo vs. 4 min, 15 sec for Ti), the channel characteristics could be affected by plasma damage during the sputtering process or the source and drain contact could have an adverse effect, as discussed in detail below.

The variations in the extracted device parameters ($V_{th}$, which corresponds to $V_{GS}$ value when scaled $I_{DS}$, with $L_G$, equals to 10nA in (a) and field effect mobility in (b)) as a function of $L_G$ for the two different contact metals are summarized in Fig. 4.2. While the influences of $L_G$ on $V_{th}$ show some fluctuation, which might be related to the imprecisely controlled process variables, the mobility show certain trends with $L_G$ depending on electrode material.
Fig. 4.1. The transfer curves for various channel length, for (a) Ti metal electrodes and (b) Mo metal electrodes.

Fig. 4.2. The variations in the extracted device parameters as a function of $L_G$ for two source/drain metal, (a) $V_{th}$, which corresponds to $V_{GS}$ value when scaled $I_{DS}$, with $L_G$ equals to 10nA and (b) field effects mobility
With the Mo electrode, the mobility clearly increases with increasing \( L_G \), while that of the TFTs with the Ti electrode remains at a relatively constant level which is generally higher than that of the Mo samples. Typical mobility vs. \( V_{GS} \) characteristics showing this trend is shown in Fig. 4.3. Mobility is rather independent of contact metal type at longer gate length (~38 \( \mu m \)) but is quite dependent on that factor when it is ~3 \( \mu m \).

There are two possible reasons for these results: one is the plasma damage effect on the channel region from the sputtering process of the contact metals, while the other is the metal to source/drain contact resistances. Regarding the plasma damage, since the source and drain metals were sputter-deposited via the open area of the photo-resist pattern in the lift-off process, the plasma damage could extend from the edge region of the source and

Fig. 4.3. The field effect mobility characteristics as a function of \( V_{GS} \) for different source/drain metal and \( L_G \).
drain contacts onto the a-IGZO channel region. Although the influence of the plasma damage on the a-IGZO channel region properties is not quantitatively understood, it is reasonable to assume that the physical bombardment effect degrades the electron mobility. Therefore, as the LG decreases, the relative portion of the damaged region increases and the mobility decreases. The longer sputtering time and heavier bombardment effect of Mo compared to Ti have exaggerated this effect for the Mo contact. However, this is not actually the major reason for this effect as can be evidently understood from the following results using the TLM, which elucidates the importance of the TLM in assessing this problem.

It has been reported that different contact metals have different contact resistance, a factor that influences estimated mobility using the drain current in the linear operation regime as shown in Eq. (1) under the gradual channel approximation,

\[
I_{DS} = \mu_{eff} \frac{W}{L_G} C_{ox} (V_{GS} - V_{th} - \frac{V_{DS}}{2})V_{DS}, \quad (1)
\]

where \(\mu_{eff}\) is the field effect mobility of the electrons and \(C_{ox}\) is the gate insulator capacitance per unit area. It is well known that the drain current in planar TFTs does not flow through the entire source/drain contact area; rather, it flows through a limited region near the contact edges [12, 13]. As a result, the contact resistances are closely related to the overlap geometry between the source/drain and the a-IGZO channel. Moreover, a-IGZO TFTs do not have heavily doped Ohmic layers like the conventional metal oxide semiconductor field effect transistor (MOSFET), so the contact resistance is affected by
the interface properties between the naturally doped a-IGZO and the source/drain metal, which include the work function of the metal, the possible oxidation layer, and the chemical interaction. When intrinsic device parameters such as the contact resistance of the source/drain electrodes ($R_{SD}$) and the resistance per unit length of channel ($R_{sh}$) are assumed to be independent of the LG, the contact characteristics can be extracted from the correlations between $L_G$ and total device resistances ($R_T$) as shown by Eq. (2),

$$R_T = \frac{V_{DS}}{I_{DS}} = 2R_{SD} + \frac{L_G}{\mu_{eff} W C_{ox} (V_{GS} - V_{th} - \frac{V_{DS}}{2})}$$

$$= 2R_{SD} + R_{sh} L_G$$

Eq. (2)

$R_{SD}$ is generally interpreted as the series resistance of two components: the metal/a-IGZO interface resistance and the bulk resistance of the a-IGZO material beneath the contact area [14, 15]. To examine the difference between the Ti and Mo source/drain electrodes, the variation of $R_T$ is shown as a function of $L_G$ in Figs. 2.4 (a) and (b), respectively. $R_{sh}$ and $R_{T0}$, which corresponds to $R_T$ at $L_G = 0$ (and also $= 2R_{SD}$), were extracted using the slope and y-axis intercept of the plot, respectively. As shown in inset Figs., the $R_{T0}$ is noticeably different between the two contact materials. The physical implication of these results will be discussed later in detail.
Fig. 4.4. $R_T$ as a function of different channel length (a) Ti source/drain electrode (b) Mo source/drain electrode

Fig. 4.5. Extracted devices parameters, (a) channel sheet resistance ($R_{sh}$) and (b) field effect mobility as a function of $V_{GS}$ for two source/drain metal electrode
Since the extracted $R_{sh}$ does not include the contact resistance, the mobility characteristics independent of $R_{sd}$ can be extracted by plotting the $R_{sh}$ as a function of $(V_{GS} - V_{th})$, which is shown in Fig. 4.5 (a), and the extracted mobility, according to Eq. (2), is shown in Fig. 4.5 (b). It can be understood that the mobility characteristics, excluding the influences of source and drain contacts, as a function of $V_{GS}$ were almost identical for the Ti and Mo electrodes, suggesting that the characteristics of the channel material are not influenced by the contact metal type, and the above hypothesis based on the plasma damage effect must be defied. Therefore, the overall mobility degradation shown in Fig. 4.2 (b) in short channel devices using the Mo contact is induced by the contact characteristics. The identical mobility characteristics as a function of $V_{GS}$ of the samples using the different contact metals suggest that the acceptor-like trap distribution in the channel region was not influenced by contact metal type.

To examine the contact characteristics, $R_{T0}$ as a function of $V_{GS}$ for different source/drain metal should be considered. Fig. 4.6 (a) shows the variations of $R_{T0}$ as a function of $V_{GS} - V_{th}$ for the two metal electrodes. Interestingly, distinct characteristics were observed for $R_{T0}$, which decreased with increasing gate bias for the Ti electrode but remained constant for $V_{GS} - V_{th} > ~7V$ for the Mo electrode. In addition, the $R_{T0}$ of TFT with the Mo electrode decreased and even became negative when $V_{GS} - V_{th}$ decreased to the sub-threshold operation regime.

To understand these peculiar variations of $R_{T0}$ with gate bias for the two metal electrodes, the distribution of the current in the TFT structures was simulated using a SILVACO TCAD simulator [10, 11, 18-20] as shown in Fig. 4.7.
Fig. 3.6. (a) Extracted total device resistances corresponding to \(L_G=0\) \((R_T0)\) for different source/drain metals and (b) the simulation results.

Fig. 3.7. ATLAS simulation result of current path (a) for a Ti electrode and (b) for a Mo electrode.
For the simulation, the a-IGZO channel was assumed to have a donor-like trap density of $1 \times 10^{20} \text{ cm}^{-3}\text{eV}^{-1}$ with a characteristic energy slope of 0.1 eV near the valence band edge and an acceptor-like trap density of $3 \times 10^{19} \text{ cm}^{-3}\text{eV}^{-1}$ with the characteristic energy slope of 0.12 eV near the conduction band edge. These parameters were determined from the careful simulation of transfer characteristics. In Fig. 4.7 (a), the current density distributions are shown for a TFT composed of a Ti metal contact with a work function of 4.3 eV and a non-damaged a-IGZO with the electron affinity of 4.16 eV, which corresponds to a non-Ohmic contact with relatively small Schottky barrier height, for three VGS values of -3, 1, and 10 V. In Fig. 4.7 (b), the same simulation results with the Mo electrode are shown. Here, Mo was assumed to form an Ohmic contact with the a-IGZO, and the concentration of the donor-like traps of a-IGZO in the source and drain overlap regions were assumed to have a Gaussian distribution positioned 0.1 eV below the conduction band edge with a peak density of $5 \times 10^{18} \text{ cm}^{-3}\text{eV}^{-1}$ and 0.1 eV deviation. This is based on the assumption that the a-IGZO region below the Mo metal is damaged by electron charging and bombardment effect of Mo atoms during sputter deposition. The adverse effects of the Mo sputter deposition may include the oxygen vacancy formation having shallow trap energy, which can increase the carrier density but reduce the mobility by scattering. The diffusion of Mo into the underlying a-IGZO layer cannot be excluded. Recently, it was reported that the Mo doping deteriorates the electron mobility and increased resistivity of a-IGZO [17] when the doping concentration is high (> 4 atomic %). Therefore, the adverse effect of Mo deposition on a-IGZO can be the modest increase in the carrier concentration and serious degradation of carrier mobility by the defect (typically oxygen vacancy) formation and impurity diffusion. Overall, the
performances of the a-IGZO under the Mo contact as the oxide semiconductor are degraded. Considering that the degree of damage decreases in deep areas of the a-IGZO below the Mo contact metal, the boundary between the damaged and non-damaged a-IGZO was assumed to be slanted as shown in the Fig. 4.7 (b).

For the Ti contact case, the carrier transport at the interface is most likely governed by the Schottky mechanism due to the non-negligible Schottky barrier and the possible oxidation of Ti at the Ti/a-IGZO interface. However, the Schottky barrier at the Ti/a-IGZO interface can be hardly influenced by the $V_{GS}$ since the channel potential is largely determined by the drain voltage once the carrier accumulation region is formed. Therefore, the reason for the decreased $R_{T0}$ shown in Fig. 4.6 (a) with the increasing $V_{GS}$ must be found from the increased effective contact area, as shown in Fig. 4.7 (a). Under the high enough $V_{GS}$ the carrier accumulation region extends far into the contact region which reduces the contact resistance largely. Fig. 4.7 (a) also reveals that the conduction path shifts from the channel surface to the gate insulator/channel as the gate voltage increases, which also contributes to the increased effective contact area and decreased $R_{T0}$. Therefore, in this case, the contact resistance has a strong dependency on $V_{GS}$ [11] and the $R_{T0}$ simulation results explain these characteristics very well.

In contrast, the TFT with the Mo electrode showed a constant $R_{T0}$ irrespective of the $V_{GS}$ in the linear operation regime (Fig. 4.6 (a)). Barquinha et al. reported that there was no clear evidence of interfacial layer formation in the Mo/a-IGZO contact region, but there was clear interfacial layer formation in the Ti/a-IGZO contact region [16]. The causes of these results could be due to the higher oxidation resistance of Mo. Furthermore, MoO$_x$ (if any) is much more electrically conducting compared to TiO$_x$. As discussed
above, the stronger bombardment effect provided by the Mo atoms with longer sputtering time could form a Ohmic contact due to the higher damage-induced carrier concentration in the damaged a-IGZO region. Therefore, the contact characteristics should be distinct from those with Ti. Figure 3.7 (b) shows the critically different behavior of the conduction path in the linear operation regime compared with the Ti electrode case. The conduction channel near the interface with the gate insulator never widens into the damaged a-IGZO region even with a $V_{GS}$ as high as 10 V. This must be a reasonable consequence of the higher carrier concentration in the damaged a-IGZO region. In addition, the contacts between the Mo and the damaged a-IGZO as well as that between the damaged a-IGZO and the carrier-accumulated conduction path must be Ohmic, so there is no reason for the $R_{T0}$ to vary with increasing $V_{GS}$. The decreasing trend of $R_{T0}$ even to the unreasonable negative value with decreasing $V_{GS}$ in the sub-threshold regime can be understood from the following. A decrease in the $V_{GS}$ results in the shift of the current path to the upper portion (back surface) of the channel, where the actual channel length is shorter than the nominal value between the source and drain edges (defined by the photolithography). In Eq. (2), however, it was assumed that the $L_G$ is independent of $V_{GS}$. Furthermore, in the sub-threshold regime, $R_{sh}$ increases largely (Fig. 4.5 (a)) and becomes much larger than $R_{SD}$, exaggerating the error in estimating the $R_{T0}$ if there is any error in counting $L_G$. The $L_G$ actually decreases as the $V_{GS}$ decreases into the sub-threshold region, while a constant $L_G$ was assumed when the $R_{T0}$ is extracted using Eq. (2). Therefore, a negative value of $R_{T0}$ was extracted, which is an artifact from the wrong application of Eq. (2) for this case.

On the other hand, for the Ti electrode, the $L_G$ variation with respect to the $V_{GS}$ is
negligible so that application of Eq. (2) in the sub-threshold region did not invoke such a problem. Such variations in R_{T0} according to contact metal can be simulated using the assumed material parameters and contact geometries shown in Fig. 4.6 (b). The simulated result of R_{T0} as a function of V_{GS} is identical with that of the experimental result, suggesting that the L_G variation with V_{GS} is the main reason for the negative R_{T0} in the sub-threshold region. However, the absolute calculated values of the R_{T0} of the TFT with Mo contact are generally smaller than the experimental values. This could be due to the following two reasons. First, the actual Mo electrode could have higher resistivity than the bulk value used for the simulation due to the possible oxidation by the ejected oxygen atoms from the underlying a-IGZO during the Mo sputtering. Second, the Mo/IGZO contact may have a non-negligible contact resistance, even though it must be quite close to Ohmic [17], which was not considered in the simulation. Although there is a certain quantitative discrepancy between the calculation and the experimental results, the reasonable similarity between the two suggests that the model shown in Fig. 4.7 well represent the TFTs with different contact metals.

The changes in the transfer characteristics shown in Figs. 1 – 3, including the V_{th} and mobility depending on contact metal and L_G, can also be understood from these variations in the contact characteristics. From the comparison of Figs. 3.1 (a) and (b), slightly higher V_{th} value of the Mo sample can be understood to have mainly come from the degradation of sub-threshold slope, since the onset voltages of I_{DS} are almost identical (~0V). As the characteristics of channel regions are not different for the different contact metals, this is due to the influence of the contact region. The rapidly decreasing R_{T0} for the Ti electrode appears to contribute to the better sub-threshold behavior, which cannot be expected from
the Mo contact. The inferior electrical conduction property of the a-IGZO region below the Mo contact metal to the same below Ti contact metal generally decreased the mobility characteristics as shown in Fig. 4.3. When \( L_G \) is small (\(< \sim 5 \, \mu m\)) this adverse effect from the contact region became even serious as the portion of the damaged region to the overall conduction path increases. The non-decreasing contact resistance for the Mo contact even with the higher \( V_{GS} \) made the difference even bigger as shown in Fig. 4.3 for the shorter \( L_G \) devices.
4.4 Summary

The electrical characteristics of channel and contact regions were separately examined by using the TLM for TFTs with two different contact metals, Ti and Mo. The different device performance according to the source/drain metal electrode attributed to the different contact characteristics than the process damage to the channel region. In addition, the device performance degradation was more serious for short channel devices with Mo contact due to the more involvement of damaged contact a-IGZO region. The experimental transport characteristics according to the source/drain electrode metal were reproduced by the simulation model, which accurately elucidates the damage distribution in the contact region. When Ti was used as the contact electrode, the contact characteristics were governed by the interfacial Schottky-like property but the source/drain a-IGZO material itself was minimally damaged. However, when Mo was used as the contact electrode, the Mo/a-IGZO and a-IGZO/accumulated channel contact characteristics were quasi-Ohmic and the contact resistance was governed by bulk conduction over the damaged a-IGZO beneath the contacts. The higher bombardment effect of heavier Mo atoms with longer sputtering time induced heavy damage (probably oxygen vacancy formation accompanied with the donor-like trap formation and possible Mo diffusion) in the source/drain a-IGZO region, which generally degrades the device performance, especially when the gate length decreases to < ~10 μm. From these results, it is expected that the other source and drain patterning method, where the metal was deposited first by sputtering and wet-etched using photoresist pattern made on the metal layer, could be harmful for the a-IGZO channel performances. Therefore, a careful
control of the sputtering process not to induce to severe damaging effect on the channel is necessary for mass production. A damage-free deposition of source and drain metal contacts with low contact resistance is essential for the optimum TFT performance for the given device parameters.
4.5. References


5. The Electrical Properties of Asymmetric Schottky Contact Thin Film Transistors with Amorphous-In$_2$Ga$_2$ZnO$_7$

5.1. Introduction

The hetero-junction formation between the metal and semiconductor has played a crucial role in various electronic devices, and has provided the solid state physics and electrical engineering communities with intriguing research topics. Classical Schottky junction theory, which was originally developed for metal/single-crystal semiconductors, could be well used to explain many of the experimental results for metal/poly-crystalline semiconductors, and even metal/oxide semiconductor junctions, as long as the fluent (quasi-) Ohmic contact to the semiconductors at the opposite end is confirmed [1]. The theory can also be extended to the metal/amorphous semiconductor junctions where the amorphous semiconductor can be represented by hydrogenated amorphous Si [1,2]. Recently, amorphous In$_2$Ga$_2$ZnO$_7$ (a-IGZO) has received a great deal of attention for thin-film-transistor (TFT) applications in modern flat-panel display devices, due to its optical transparency and superior charge carrier transport properties [3]. In addition, it was also reported that a-IGZO has the potential to be used in logic devices and memory applications as alternatives to Si-based electronic devices, which has made it even more attractive for intensive research [4-6].

One of the main issues of a-IGZO TFTs is the contact formation between the source/drain metal and a-IGZO channel, as they lack the heavily doped source and drain regions that are commonly made in Si-based electronic devices by ion implantation. In
order to attain high performance a-IGZO TFTs, it is important to establish a concrete understanding of how the properties of the contact between the a-IGZO and various source/drain metals affect device operations [7-11]. a-IGZO TFTs made from different source and drain contact metals with largely different work functions (W_f) could be regarded as a diode when the channel is turned on by a sufficiently high gate voltage (V_{GS}), if one contact metal forms a high Schottky barrier while the other contact metal provides Ohmic-like contact. This could be a viable structure to examine Schottky junction properties more precisely than with conventional metal/a-IGZO two-terminal diodes [12,13]. The usual method to fabricate the metal/a-IGZO junction is to deposit the a-IGZO layer with different thicknesses (thinner and thicker than the expected depletion width, which depends on the types of metal and doping concentration of the a-IGZO), and forming the metal layer on top. The inverse process sequence, which involves metal deposition followed by deposition of the a-IGZO layer, is also feasible. In both cases, it has been reported that the sputtering process, which has been the most common method to deposit the amorphous oxide semiconductor (AOS) material stably at low temperature, influences the a-IGZO layers themselves, either by sputtering damage (ion bombardment effect) or thickness-dependent stress [14, 15]. Therefore, the sputtering time of the a-IGZO deposition for this type of structure varies not only the thickness but also the material properties of the a-IGZO layer. In TFT structure, an a-IGZO layer with a given thickness was utilized, and the carrier concentration in the AOS layer can be controlled independently from that of the diode bias by controlling V_{GS} (in this case, the diode bias can be regarded as the drain voltage while the source is grounded). As the channel length, which is the distance between the drain metal and source metal, could be much larger
than the depletion layer thickness, the full range of the junction property can be exploited from accumulation to full depletion.

In contrast, the three-dimensional and three-terminal structure of a TFT makes interpretation of the electrical measurement results quite complicated, compared to the simple two-dimensional geometry of a diode. Particularly, in the bottom gate structure of the TFT examined in this work, the carrier can be depleted at the metal/IGZO junction even under the accumulation bias condition of the TFT due to the contact potential effect. Therefore, careful analysis of the results based on the simulations of the field and carrier distribution is indispensable.

TFTs with asymmetric source and drain contacts could be used when a device simultaneously having diode and transistor functions is required. a-IGZO TFTs with different source and drain metals having largely different $W_F$ (Ti, Ni, and Pt) were fabricated, and the device characteristics were examined. The results are compared with TCAD simulations using a commercial software package (ATLAS) [16]. The fabricated TFTs show highly asymmetrical transfer characteristics depending on the types of source and drain metals, which may be used in devices where a TFT and diode are combined in a single device. Such a device can be called an asymmetric Schottky contact TFT (ASC-TFT). This type of device can be used in applications where switching and rectification with respect to the bias direction are simultaneously required.
5.2. Experimental procedure

Heavily doped p-type silicon and 100-nm-thick thermally grown SiO$_2$ were used as the gate metal and gate dielectric, respectively. For the channel material, a 40-nm-thick a-IGZO film was deposited by radio frequency magnetron sputtering at room temperature [17]. The channel thickness was measured using a spectroscopic ellipsometry (M-2000, J.A. Woollam). The a-IGZO active layer was patterned by photolithography and wet-etched with a diluted solution of hydrofluoric acid. For the symmetric source/drain metals, Ti, Ni and Pt was deposited via sputtering and patterned using the conventional lift-off method. For asymmetric source/drain metals, Ti was chosen as the Ohmic-like contact metal, and either Ni or Pt was used as the Schottky-like contact metal and patterned in the same manner. Using these process steps, a-IGZO TFTs were fabricated with three types of symmetric source/drain metals, Ti/Ti, Ni/Ni, and Pt/Pt, and two types of asymmetric source/drain metals, Ti/Ni and Ti/Pt. The channel width ($W$) was fixed at 20 $\mu$m, the channel length ($L_C$) was varied from 3 to 38 $\mu$m, and the source/drain overlap ($L_{OV}$) was fixed at 5 $\mu$m. Most of the electrical data were obtained from the TFTs with $L_G$ of 3 $\mu$m. The fabricated TFTs were annealed in air at 200 °C for 1 hour to stabilize the contact resistance between the a-IGZO layer and the metals. In Fig. 5.1, the optical microscope image (a) and schematic cross sections (b) of fabricated ASC-TFTs are shown. The electrical characteristics of the fabricated TFTs were evaluated by measuring the current flows from the source to drain ($I_{DS}$) while applying the drain voltage ($V_{DS}$) and the gate bias ($V_{GS}$). The measurement was performed using a Hewlett-Packard 4155 semi conductor parameter analyzer at temperatures ranging from room temperature to 120 °C.
Fig. 5.1. (a) optical view and (b) schematic cross section of fabricated ASC-TFTs
5.3. Results and discussions

5.3.1. Device performance variation in terms of source/drain metal work function

In Fig. 5.2, the transfer characteristics (I_DS - V_GS curves) of TFTs are shown for various symmetric source/drain metals, and the expected energy band diagrams at the interfaces between the a-IGZO and source/drain metals are shown in the insets. When Ti was used as the source/drain metal, as shown in Fig. 5.2 (a), the transistor was turned on well at ~0 V, and I_on (I_DS at V_GS and V_DS of 20 V) reached $5 \times 10^{-4}$ A. The $I_{on}/I_{off}$ (I_DS at V_GS of 20 V and V_DS of -10 V) ratio was higher than $10^8$, and the sub-threshold swing (S.S.) was less than 200 mV/dec. However, as shown in Figs. 4.2 (b) and (c), the transfer characteristics of the TFTs with Ni and Pt source/drain metal were inferior to that of the TFT with Ti source/drain metal. The threshold voltage (V_th) was shifted in the positive direction, and I_on for Ni and Pt source/drain metal were $3 \times 10^{-5}$ A and $6 \times 10^{-11}$ A, respectively, even at high V_GS of 20 V and high V_DS of 20 V. These characteristics can be explained by Schottky-type contact formation at the metal/a-IGZO channel interface primarily due to the higher work function (W_F) of Ni and Pt compared to Ti. When the Fermi level pinning effect was neglected, the Schottky barrier at the metal/semiconductor interface could be estimated simply as the difference between the W_F of metal and the electron affinity of the semiconductor. As the electron affinity of a-IGZO is ~4.15 eV [18-20], the Schottky barrier height ($\phi_B$) at the Ti/IGZO interface is calculated as ~0.18 eV, with the given W_F of Ti (4.33 eV), which is small enough to form a quasi-Ohmic contact [18].
Fig. 5.2. Transfer characteristics for various source/drain metal and the band diagram at the source metal to a-IGZO channel overlap region (inset) ; (a) Ti, (b) Ni and (c) Pt source/drain metals.

Fig. 5.3. $I_{DS}$-$V_{DS}$ characteristics for various source/drain metal; (a) Ti and (b) Ni metals.
In case of Ni or Pt contact, the \( \phi_B \) values at the metal/a-IGZO channel interface are calculated as \( \sim 1.0 \) eV and \( \sim 1.5 \) eV, respectively, since the \( W_F \) of Ni and Pt were 5.2 eV and 5.7 eV [22]. The difference between the \( W_F \) of the source/drain metal and the electron affinity of a-IGZO forms a Schottky barrier, the presence of which suppresses the injection of majority carriers (electron) to the channel. The bias with reverse polarity was applied to the Schottky junction of the source/a-IGZO channel overlap region, while forward bias was applied to that of the drain/a-IGZO channel overlap region. As the electrons injected to the Schottky junction are exponentially dependent on the Schottky barrier height (\( \phi_B \)), \( I_{DS} \) current is limited by the Schottky barrier between source/a-IGZO channel interfaces. However, it should be noted that the actual value of \( \phi_B \) is strongly affected by the interface states, and it can be largely deviated from the value obtained by the simple subtraction due to the Fermi level pinning [1,2,23].

The current path for \( I_{DS} \) flow should also be affected by the presence of a Schottky junction due to the depletion layer in the source/drain and a-IGZO channel overlap region. Since the Fermi energy level (\( E_F \)) of a-IGZO is located near the conduction band edge [18-21], the built-in potential (\( V_{bi} \)) and depletion width (\( W_D \)) at the interface between source/drain metal and a-IGZO could be large enough to influence the device performance of the TFTs with Ni or Pt source/drain metals. The depletion width can be estimated from the relation between \( V_{bi} \) and the doping level (\( N_D \)) as shown by Eq. (1),

\[
W_D = \sqrt{\frac{2\varepsilon_r}{qN_D}} \left( V_{bi} - V - \frac{kT}{q} \right)
\]  

(1)
where the $\varepsilon_r$ is the dielectric constant of a-IGZO (= 10), $N_D$ is the doping density and $V$ is the applied voltage at the contact [24]. When $E_F$ and the doping concentration ($N_D$) of a-IGZO were assumed to be 4.27 eV and $2.2 \times 10^{17}$ cm$^{-3}$ [18-21], $W_D$ in the Ti/a-IGZO channel interface was 17 nm, while that of the Ni/a-IGZO and Pt/a-IGZO channel interface were 32 nm and 66 nm, respectively, when $V = 0$V. The very high $V_{th}$ of the TFTs with Pt source/drain metal can be understood from the Schottky-type contact at the source/drain and a-IGZO channel overlap region. With doping density higher than $\sim 10^{17}$ cm$^{-3}$, the AOS is already quite electrically conductive, so the TFT channel easily conducts electricity when a drain voltage is applied even under small $V_{GS}$ if the source and drain make an intimate electrical contact with the ground and voltage source. This corresponds to the a-IGZO TFT with Ti metal contacts having small $W_D$. However, as the contacts become more highly Schottky-type due to mismatch of the energy levels, thicker $W_D$, which could be even larger than the IGZO thickness (for the Pt case), impedes the current flow between source and drain even when high $V_{DS}$ and $V_{GS}$ are applied. In addition, the $V_{GS}$ must be divided into the gate dielectric and a-IGZO channel, so a high $V_{GS}$ was required to accumulate electrons in depletion region, as shown in the inset of Fig. 5.2 (c). As a result, the current conduction can be further aggravated by this effect in the structure of the bottom-gated TFT. These effects are discussed in detail with the simulation results.

An even greater complication due to the highly depleted contact region can be found in Fig. 5.3, which shows the $I_{DS}$-$V_{DS}$ characteristics (variations of the $I_{DS}$ as a function of $V_{DS}$) for various $V_{GS}$ for the TFTs with Ti and Ni contact metals. When Pt was used as source/drain metal, $V_{th}$ was too high to measure the $I_{DS}$-$V_{DS}$ characteristics in this voltage range. When Ti was used as a source/drain metal, the $I_{DS}$-$V_{DS}$ curves showed normal $I_{DS}$-
$V_{DS}$ characteristics of a conventional TFT, such that $I_{DS}$ increased and saturated as $V_{DS}$ increased, and the saturation $I_{DS}$ level increased with increasing $V_{GS}$. However, interestingly, when Ni was used as a source/drain metal, the $I_{DS}$ decreased slightly as the $V_{DS}$ increased when the $V_{DS}$ was higher than 5 V at $V_{GS}$ of 20 V, although it showed normal behavior when $V_{DS} < ~5V$. It must also be noted that the general $I_{DS}$ level is smaller than that of Fig. 5.3 (a) by approximately one order of magnitude. This characteristic behavior can be explained by the channel depletion effects at the drain/a-IGZO channel overlap region in the high $V_{DS}$ and the current path change due to the presence of a depletion layer at the source/drain and a-IGZO channel overlap region. For a given $V_{GS}$, the accumulated electron density at the drain/a-IGZO channel overlap region should be decreased with the increasing $V_{DS}$, which decreases the channel conductance when $V_{DS}$ becomes higher than a certain value. This behavior is similar to the pinch-off effect in conventional Si-based metal oxide semiconductor field effect transistors (MOSFETs). However, with MOSFETs, the inversion layer and source/drain junction are located on the same surface of the Si channel, so such a decrease in $I_{DS}$ with increasing $V_{DS}$ is not observed, while the accumulation layer of the a-IGZO TFTs presented here is located at the gate dielectric surface, and the source/drain junction is located at the opposite side of the layer. Therefore, the carrier depletion effect at higher $V_{DS}$ was aggravated in the TFT case, which is explained in detail in Figs. 4.4 and 5.

Figs. 4.4 and 5 show the simulation results on the potential, electron density, and current density distributions for the Ti and Ni source drain metal cases, respectively.
TABLE 5.1. Simulation model parameters

<table>
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<tr>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
<th>Description</th>
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<td>cm$^{-3}$</td>
<td>Effective conduction band DOS</td>
</tr>
<tr>
<td>$N_D$</td>
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<td>cm$^{-3}$</td>
<td>Effective valance band DOS</td>
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<tr>
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<td>cm$^{-3}$</td>
<td>Fully ionized donor density</td>
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<td>cm$^{-3}$/eV</td>
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</tr>
<tr>
<td>$E_{a1}$</td>
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<td>eV</td>
<td>Shallow acceptor-like trap energy slope in conduction band edge</td>
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<tr>
<td>$G_{a2}$</td>
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<td>cm$^{-3}$/eV</td>
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<td>cm$^{-2}$</td>
<td>Interface charge density</td>
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</table>
Fig. 5.4. 2D simulation results for the Ti source/drain electrode; potential contour map at the (a) $V_{DS}$ of 10V and (b) $V_{DS}$ of 20V, electron density contour map at the (c) $V_{DS}$ of 10V and (d) $V_{DS}$ of 20V and current density contour map at the (e) $V_{DS}$ of 10V and (f) $V_{DS}$ of 20V.
Potential contour map

Electron density contour map

Current density contour map

Fig. 5.5. 2D simulation results for the Ni source/drain electrode; potential contour map at the (a) $V_{DS}$ of 10V and (b) $V_{DS}$ of 20V, electron density contour map at the (c) $V_{DS}$ of 10V and (d) $V_{DS}$ of 20V and current density contour map at the (e) $V_{DS}$ of 10V and (f) $V_{DS}$ of 20V.
It can be noted that most of the $V_{GS}$ is applied to the SiO$_2$ layer in both cases, which must be a reasonable result considering the much smaller capacitance of the SiO$_2$ layer compared with that of the a-IGZO layer. In addition, once the carrier accumulation starts to form at the a-IGZO/SiO$_2$ interface, it largely screens the $V_{GS}$. Nevertheless, the small portion of $V_{GS}$ applied to the a-IGZO layer induced the carrier accumulation layer at the a-IGZO/SiO$_2$ interface. However, this carrier accumulation layer can be easily disturbed by $V_{DS}$. When a $V_{DS}$ of 10 V was applied to the Ti drain, the voltage distributes rather uniformly across the channel length because the contact regions do not have any specific high resistance due to their quasi-Ohmic nature. This barely disturbs the carrier accumulation layer in the channel region, but that under the drain contact almost totally disappeared because the potential from the $V_{GS}$ was almost completely nullified by the $V_{DS}$ in that region. Therefore, the current flow through a wider range of source/channel overlap region and channel but a narrow region at the edge of the drain/channel overlap region as shown in Fig. 5.4 (e). When $V_{DS}$ increased to 20 V, the carriers in the drain/channel overlap region were completely depleted by the high $V_{DS}$. It must be noted that the condition at the a-IGZO/drain Ti corresponds to a highly forward bias in a normal semiconductor/metal Schottky diode, where the other junction maintains Ohmic contact, supplying the diode with sufficient majority carriers. Under this circumstance, the Schottky junction is always filled with sufficient electrons so that such a carrier-depletion never occurs. However, in TFT structure, the carrier supply from the source region is limited by the finite contact resistance and channel resistance, so that the drain region becomes carrier depleted, as shown in Fig. 5.4 (d). This results in the potential distribution concentrated near the drain contact edge, as shown in Fig 4.4 (b), where the
additional ~10 V (compared with Fig. 5.4 (a)) was dropped near the drain edge, so that the carrier accumulation layer in the channel region was hardly affected. However, due to such a field distribution, there forms a strong current path along the drain edge, as shown in Fig. 5.4 (f), so that the high $I_{DS}$ was maintained at such a high $V_{DS}$ even though the drain contact region becomes strongly carrier depleted, as shown in Fig. 5.3 (a). In contrast, quite a different potential distribution was achieved for the case of Ni contact metals, as shown in Fig. 5.5, which was mainly due to the very high contact resistance between Ni and a-IGZO originating from the high Schottky barrier.

When $V_{DS}$ was 10 V, most of the $V_{DS}$ was applied to the source contact region (Fig. 5.5 (a)), since the source contact had a strongly carrier-depleted configuration accompanied by high resistance, while the drain contact had a minimized carrier-depleted region (Fig. 5.5 (b)). Therefore, the carrier accumulation layer under the source contact completely disappeared. However, interestingly, the drain contact region maintains much lower resistance state due to the forward bias condition of this case, so that the carrier accumulation layer was retained even under the drain contact (Fig. 5.5 (c)), which is in a stark contrast with the Ti contact metal case. Therefore, the current path extended into the drain contact region, while it was restricted at the edge of the source contact, as shown in Fig. 5.5 (e). When $V_{DS}$ increases to 20 V, the increased 10 V was applied across the channel region, so that the channel potential varied greatly, as shown in Fig. 5.5 (b). This is accompanied by a large change in the carrier accumulation layer across the whole channel region, as shown in Fig. 5.5 (d). It can be understood that the electrons distribute rather uniformly across the thickness of the a-IGZO channel, or that even slightly higher electron concentration was achieved near the back surface of the channel under this bias
condition. This results in a shift of the major current path from the SiO₂/a-IGZO interface to back surface of the channel, which is vulnerable to contamination or any other detrimental influences from the fabrication processes. Therefore, under this circumstance, the channel conductance must decrease compared with the case shown in Fig. 5.5 (e), where the current still mainly flows near the SiO₂/a-IGZO interface. This can explain the abnormal decrease in I_Ds in the high V_Ds region shown in Fig. 5.3 (b).
5.3.2. Device performance of ASC-TFTs with Ti/Ni metal electrodes

Based on the understanding of metal W_F effects on the transfer characteristics of the a-IGZO TFTs described above, those of ASC-TFTs were examined. Ti was chosen to create a quasi-Ohmic contact, while Ni or Pt was adopted to form a Schottky contact at the opposite end of the TFT. The I_DS-V_GS characteristics of ASC-TFTs with Ti/Ni are shown in Fig. 5.6, where (a) shows the characteristics when the Ni was biased with V_DS while Ti was grounded, which is referred to as the V_Ni condition, and (b) shows them when the Ti was biased with V_DS while Ni was grounded, called the V_Ti condition. Similar characteristics with Ti/Pt are shown later. As Schottky contacts generally have asymmetric carrier transfer characteristics with respect to bias polarity, the transfer characteristics should be dependent on the drain bias direction. In addition, since the a-IGZO channel depletion in the source/drain overlap region (L_OV shown in Fig. 5.1 (a)) was controlled by the bias polarity, the role of W_F in the I_DS current must also be understood. As shown in Fig. 5.6, transfer characteristics for the V_Ni bias condition were similar to those of TFTs with Ti source/drain metal, while those of ASC-TFTs under V_Ti bias condition were similar to those of TFTs with Ni source/drain metal. The transfer characteristics of the ASC-TFT were far better under the V_Ni condition compared with the V_Ti condition. As shown in the inset of Fig. 5.6 (a), under the V_Ni bias condition, the applied bias significantly decreases the V_bi at the Ni/a-IGZO interface and the electron transport governed by the a-IGZO channel and Ti/a-IGZO contact, which results in a situation similar to the symmetric TFT with the Ti/Ti metals.
Fig. 5.6. Transfer characteristics for ASC-TFTs with Ti/Ni source/drain metal and the band diagram at the Ni metal to a-IGZO channel overlap region (inset); (a) $V_{Ni}$ bias condition and (b) $V_{Ti}$ bias condition
However, as shown in the inset of Fig. 5.6 (b), under the $V_{Ti}$ bias condition, the $I_{DS}$ currents should be limited by the Schottky barrier ($\phi_b$) of the Ni/a-IGZO interface of the overlap region, and as a result, the $I_{DS}$ currents were much lower than the $I_{DS}$ under the $V_{Ni}$ bias condition. This was further confirmed by the simulation of current density, potential contour, and electron density, which will be discussed later in detail.

To further verify the contact-limited characteristics of ASC-TFTs, the $I_{DS}$-$V_{GS}$ characteristics for various $L_C$ were examined. As shown in Fig. 5.7 (a), for the $V_{Ni}$ bias condition, the $I_{DS}$ decreased as the $L_G$ increased, while for the $V_{Ti}$ bias condition, the $I_{DS}$ were almost independent of $L_G$. Figs. 4.7 (b) and (c) show the transfer characteristics confirming this feature. These features can be explained by the relations between the total resistance ($R_{tot}$), contact resistance ($R_{cnt}$), and channel resistance ($R_{ch}$), as shown in Eq. (2):

$$
R_{tot} = \frac{V_{DS}}{I_{DS}} = R_{cnt} + \frac{L_C}{\mu_{eff} W C_{ox} \left(V_{GS} - V_{th} - \frac{V_{DS}}{2}\right)} = R_{cnt} + R_{ch}
$$

(2)

where $C_{ox}$ is the gate dielectric capacitance and $\mu_{eff}$ is the effective field effect mobility. When the $R_{cnt}$ is much larger than $R_{ch}$, the value of $R_{tot}$ is mainly attributed to the $R_{cnt}$, and as a result, the $I_{DS}$ characteristics are independent of $L_C$. For the $V_{Ti}$ bias condition (inset of Fig. 5.8 (b)), $I_{DS}$ is limited by the Schottky contact resistances, so the $R_{tot}$ is dominated by $R_{cnt}$, which is independent of $L_C$. In contrast, for the $V_{Ni}$ bias condition, $R_{ch}$ is comparable to $R_{cnt}$, and as a result, the $I_{DS}$ decreased as the $L_C$ increased, as shown in Figs. 4.7 (a) and (b), although the current level was generally higher.
Fig. 5.7. (a) $I_{DS}$ at 0.1V $V_{DS}$ for the various $V_{GS}$ as a function of channel length, (b) the $I_{DS}$-$V_{GS}$ curves of $V_{Ni}$ bias condition and (c) the $I_{DS}$-$V_{GS}$ curves of $V_{Ti}$ bias condition for the various channel length.
Even though $R_{cnt}$ is much larger than $R_{ch}$ under the $V_{Ti}$ condition, the $I_{DS}$ increased with increasing $V_{GS}$, as shown in Figs. 4.7 (a) and (c), which can be understood by the effective contact length and $W_D$ variations according $V_{GS}$. As $V_{GS}$ increased, the accumulated electron density in the a-IGZO channel region increased, which in turn contributed to the increased effective contact length and decreased $R_{cnt}$. Therefore, in this case, the contact resistance has a strong dependency on $V_{GS}$ [7-11]. Furthermore, the increased $V_{GS}$ increased the accumulated electron density in the a-IGZO channel, which further decreased $R_{ch}$.

Fig. 5.8 shows the variations of the $I_{DS}$-$V_{DS}$ characteristics of this ASC-TFT for various $V_{GS}$, and the inset shows the same graph in semi-log scale (left-hand panel) and equivalent circuit (right-hand panel). Under the $V_{Ni}$ bias condition, as shown in Fig. 5.8 (a), the variations of $I_{DS}$ according to the $V_{DS}$ are similar to those of the TFTs with Ti source/drain metals (Ti/Ti TFT), while under the $V_{Ti}$ bias condition (shown in Fig. 5.8 (b)), the variations of $I_{DS}$ according to the $V_{DS}$ are similar to that in the TFTs with Ni source/drain metals (Ni/Ni TFT). For the $V_{Ni}$ bias condition, as shown in the equivalent circuit in the inset of Fig. 5.8 (a), the $R_{tot}$ is affected by the $R_{cnt}$ of the Ti/a-IGZO channel interface when $V_{GS}$ and $V_{DS}$ are larger than $V_{th}$ and $\phi_B$. However, there is a certain discrepancy in the $I_{DS}$-$V_{DS}$ characteristics between the ASC-TFT and Ti/Ti TFT; the ASC-TFT shows a certain take-off voltage, which is $~0.7$ V for $V_{GS}$ of 10 V under this bias condition, which was not observed in the other case. This take-off voltage can be attributed to the presence of $V_{bi}$ of the Ni/a-IGZO junction at the drain contact. The $V_{bi}$ blocks the fluent current flow when the $V_{DS}$ is not high enough to reduce it.
Fig. 5.8. $I_{DS}$-$V_{DS}$ characteristics for ASC-TFTs with Ti/Ni source/drain metal and the same graph in log scale in insets; (a) $V_{Ni}$ bias operation regime and (b) $V_{Ti}$ bias operation regime.
It must be noted that 0.7 V does not correspond to \( V_{bs} \) itself, because the \( V_{DS} \) is spread across the Ni/a-IGZO junction, channel, and, though it is small, the Ti/a-IGZO junction region. In contrast, for the \( V_{Ti} \) bias condition, \( I_{DS} - V_{DS} \) characteristics were observed to be almost identical to those of the TFT with Ni source/drain metals. This is certainly understandable since the carrier injection across the Ni/a-IGZO junction at the source/a-IGZO channel interface dominantly governs the transfer characteristics regardless of \( V_{DS} \) value, and \( V_{bi} \) at the Ti/a-IGZO junction is negligible.

To verify these characteristics, the potential, electron density, and current density distributions for this ASC-TFT were simulated as they were done in Figs. 4.4 and 5. The simulation results corresponding to the \( V_{Ni} \) and \( V_{Ti} \) conditions were shown in Figs. 4.9 (a), (c), (e), and (b), (d), (f), respectively. It can be immediately understood that those distributions under the \( V_{Ni} \) and \( V_{Ti} \) conditions are almost identical to those of the TFTs with Ti/Ti and Ni/Ni source/drain metals, respectively. Therefore, the electrical characteristics of the ASC-TFTs can be well understood from those of the other two symmetric TFTs. As can be understood from the discussions given above, \( \phi_B \) influences the device performance largely. Therefore, it is necessary to estimate the \( \phi_B \) at the metal/a-IGZO interface quantitatively. In a usual Schottky diode, \( \phi_B \) can be estimated by measuring the I-V characteristics at different measurement temperatures \( (T_m) \) and analyzing the data according to the Richardson-Schottky equation. However, the estimation of \( \phi_B \) by an electrical mean is generally complicated. Since the \( \phi_B \) itself is a strong function of electric field at the interface, mainly due to the image force effect, and generally the zero-field Schottky barrier \( (\phi^0_B) \) needs to be considered for the estimation.
Fig. 5.9. 2D simulation results for ASC-TFTs with Ti/Ni source/drain electrodes; potential contour map at the (a) $V_{Ni}$ bias condition and (b) $V_{Ti}$ bias condition, electron density contour map at the (c) $V_{Ni}$ bias condition and (d) $V_{Ti}$ bias condition, current density contour map at the (e) $V_{Ni}$ bias condition and (f) $V_{Ti}$ bias condition. (For the $V_{Ti}$ bias condition, the current density was magnified 100 times).
Fig. 5.10. (a) E-filed max and $\Delta \phi_B$ at the Ni/a-IGZO interfaces as a function of $V_{GS}$, (b) conduction band diagram of a-IGZO channel at the Ni/a-IGZO overlap region for the various $V_{GS}$ and (c) 3D conduction band diagram of a-IGZO channel for the 0.1V$_{DS}$ and 20V $V_{GS}$. 

\[ \Delta \phi_B = 2 \sqrt{\frac{qE_{\text{max}}}{16 \pi \epsilon_s}} \]
\( \phi_B^o \) is not simply given as the difference between the \( W_F \) of metal and the electron affinity of the semiconductor, but is also affected by the presence of interface trap states, metal-induced-gap states, chemical interactions, etc., which tend to pin the Fermi level to a certain point within the band gap [1,2,23]. In a TFT structure, this becomes even more complicated. There are basically two ways to modify the electric field at the metal/a-IGZO interface, which induces barrier lowering by the image force effect: one is to change \( V_{GS} \), and the other is to change \( V_{DS} \). However, the former is quite inefficient in altering the interfacial electric field since most of the \( V_{GS} \) is applied to the thick SiO\(_2\) layer, and it is also screened by the charge accumulation layer as already discussed above. This is also well revealed in Fig. 5.10. In Fig. 5.10 (a), the electric field at the Ni/a-IGZO interface and accompanying barrier reduction by the image force effect \( (\Delta \phi_B) \) according to the equation included in the Fig. 5.4. are shown as a function of \( V_{GS} \), where \( V_{DS} \) and \( \phi_B \) were assumed to be 0.1 V and 0.32 eV, respectively. Even when \( V_{GS} \) increases from 10 V to 20 V, the field increases only marginally, and accordingly, \( \Delta \phi_B \) is < 0.01 eV. Figs. 4.10 (b) and (c) show the low sensitivity of \( \phi_B \) to the \( V_{GS} \) even more evidently, with the variation of potential along the thickness direction of a-IGZO under the Ni metal in the source region with the variation of \( V_{GS} \), and three-dimensional distribution of potential within the channel region, respectively. The potential distribution under the Ni contact was only marginally influenced by the change in \( V_{GS} \), which corroborates the electron and current density distribution shown in Figs. 4.9 (d) and (f). This can be understood in a slightly different way. Since the carrier accumulation layer extends into the Ni overlap region, the low potential of the drain (0.1 V) is well transported into that region through the formed conducting path. Therefore, the field is largely determined by the contact
potential even under the high $V_{\text{GS}}$, since the $V_{\text{GS}}$ is almost completely screened away by the extended accumulation layer.

The $I_{\text{DS}}$-$V_{\text{GS}}$ curves are measured at various $T_m$ as shown in Fig. 5.11 (a), and the $I_{\text{DS}}$ data at $V_{\text{GS}}$ values > 5 V are plotted according to the Richardson-Schottky equation (Eq. (3) below) to obtain the $\phi_B$ values at each $V_{\text{GS}}$, as shown in Fig. 5.11 (b). The inset graph shows the data set obtained when $V_{\text{GS}}$ was 14, 16, and 18 V, respectively, where the slope of the best linear fitted graph gives the $\phi_B$ value. According to the Richardson-Schottky equation, this type of plot must show a linearly decreasing trend with the increasing $(V_{\text{GS}})^{1/2}$, which is certainly not the case. This corroborates the simulation results on the variation of electric field and accompanying $\Delta\phi_B$ shown in Fig. 5.10, meaning that the Schottky barrier modulation by $V_{\text{GS}}$, which increases in the $I_{\text{DS}}$ with the increasing $T_m$, cannot be estimated by this method. The increase in $I_{\text{DS}}$ with the increasing $T_m$ is ascribed to the increased thermionic emission at the interface as well as the increase in the penetration of the accumulation region deeper into the source contact region.

The second method for altering the electric field at the Schottky metal/a-IGZO interface, i.e. changing $V_{\text{DS}}$, is not feasible either, as can be understood from the non-linear and complicated change of potential distribution near the interface with the varying $V_{\text{DS}}$ shown in Figs. 4.4, 5, and 9. Therefore, another method was attempted to estimate $\phi_B$. Fig. 5.12 (a) shows the $I_{\text{DS}}$ – $V_{\text{GS}}$ curves of the symmetric TFT with Ti source and drain metals measured with $V_{\text{DS}}$ of 0.1, 10, and 19.9 V, respectively (symbol), and simulated curves (line) under the assumptions tabulated in table I. The high coincidence between the experimental data and simulation results reveals the accuracy of the simulation procedure and adopted device parameters.
Fig. 5.12. Comparison of experimental transfer characteristics with simulation results for various source/drain metal; (a) $I_{DS}$-$V_{GS}$ curves of TFTs with Ti source/drain electrode, and $I_{DS}$-$V_{GS}$ curves of ASD-TFTs with Ni/Ti source/drain electrode of (b) $V_{Ni}$ bias condition, and (c) $V_{Ti}$ bias condition.

Fig. 5.11. (a) $I_{DS}$-$V_{DS}$ characteristics for various operation temperatures and (b) extracted $\phi_B$ as a function of $V_{GS}$. Inset Fig. 4. shows the estimated from the Schottky fitting, as a function of temperature.

Fig. 5.12. Comparison of experimental transfer characteristics with simulation results for various source/drain metal; (a) $I_{DS}$-$V_{GS}$ curves of TFTs with Ti source/drain electrode, and $I_{DS}$-$V_{GS}$ curves of ASD-TFTs with Ni/Ti source/drain electrode of (b) $V_{Ni}$ bias condition, and (c) $V_{Ti}$ bias condition.
Using the parameters related to the a-IGZO channel, the $I_{DS} - V_{GS}$ curves of the ASC-TFT under the $V_{Ni}$ and $V_{Ti}$ conditions are simulated as shown in Figs. 4.12 (b) and (c), respectively. Here, the key parameter for the appropriate simulation was the $\phi_B$ value at the Ni/a-IGZO interface, which largely influences the results shown in Fig. 5.12 (c), while its influence was marginal in Fig. 5.12 (b). There are certain discrepancies between the experimental data and simulation results, such as $V_{th}$ and sub-threshold slope, due mainly to the ignorance of the interface traps and accompanying charging effect in the simulation, but the most important parameter, saturation $I_{DS}$, which is the most critically influenced by the $\phi_B$ value, is well reproduced when the $\phi_B$ value was set to 0.32 eV. Therefore, the $\phi_B$ value at the Ni/a-IGZO interface is $\sim 0.32$ eV, which is quite different from the ideal value of $\sim 1.0$ eV ($W_F$ – electron affinity), suggesting that the Fermi level pinning is serious at the Ni/a-IGZO interface.

$$I_{DS} = A A^* T_{m}^{2} \exp \left( - \frac{q\left(\phi_B^0 - \sqrt{qE_{max}} / 4 \pi \epsilon_r \epsilon_F \right)}{kT_M} \right)$$  \hspace{1cm} (3)
5.3.3. Device performance of ASC-TFTs with Ti/Pt metal electrodes

The characteristics of the ASC-TFT with Ti/Pt metal were also examined, which is expected to show even higher rectifying transfer characteristics. Fig. 5.13 (a) and (b) show the $I_{DS} - V_{GS}$ characteristics of the ASC-TFT under the $V_{Pt}$ (Pt metal positively biased while the Ti metal was grounded) and $V_{Ti}$ bias condition (reverse situation of $V_{Pt}$), respectively. The corresponding band diagram near the Pt contact was shown in the inset of Fig. 5.13 (b). The transfer characteristics of ASC-TFTs with Ti/Pt source/drain metal were analogous to that of ASC-TFTs with Ti/Ni source/drain metals, but the rectifying behavior appears to be even more exaggerated. When the $V_{DS}$ was 0.1 V under the $V_{Pt}$ bias condition, the $I_{DS}$ current was lower than the measurement limit, which can be understood from the high $V_{bs}$ formed at the Pt/a-IGZO interface of the drain contact. As expected, in the $V_{Pt}$ bias condition, the transfer characteristics of ASC-TFTs with Ti/Pt source/drain metal are similar to the transfer characteristics of TFTs with Ti source/drain metal when the $V_{DS}$ is high enough to overcome the $V_{bs}$. Also, under the $V_{Ti}$ bias condition, the transfer characteristics are similar to those of the TFTs with Pt source/drain metal, showing the very low $I_{DS}$ of $\sim 1 \times 10^{-7}$ A, even at the $V_{GS}$ of 70 V and $V_{DS}$ of 20 V. This results from the severely limited electron injection over the very high Schottky barrier at the Pt/a-IGZO interface of the source contact, as schematically illustrated in the inset of Fig. 5.13 (b).
Fig. 5.13. Transfer characteristics for ASC-TFTs with Ti/Pt source/drain metal and the band diagram at the Pt metal to a-IGZO channel overlap region (inset); (a) $V_{Pt}$ bias condition and (b) $V_{Ti}$ bias condition.

Fig. 5.14. (a) $I_{DS}-V_{DS}$ characteristics for ASC-TFTs with Ti/Pt source/drain metal in $V_{Pt}$ bias condition and the same graph in log scale in insets. (b) Ideality factor for the various $V_{GS}$ as a function of $V_{DS}$. 
Fig. 5.14 (a) shows the $I_{DS} - V_{DS}$ characteristics for different $V_{GS}$ under the $V_{Pt}$ bias condition, which is similar to that of the ASC-TFT with Ti/Ni metals; they show good saturation behavior with increasing $V_{DS}$ at each applied $V_{GS}$. A certain take-off voltage was necessary, as indicated by the red lined box, which was also observed in the ASC-TFT with Ni/Ti contacts. The inset curves show the same characteristics in semi-log scale, and a schematic circuit diagram is also shown. On the other hand, the $I_{DS} - V_{DS}$ curves cannot be attained under the $V_{Ti}$ bias condition with identical $V_{DS}$ and $V_{GS}$ ranges because the current flow was almost completely blocked by the very high Schottky barrier at the Pt/a-IGZO interface of the source contact.

The variation of ideality factor ($\eta$) as a function of $V_{DS}$ for the various $V_{GS}$ values under $V_{Pt}$ condition is shown in Fig. 5.14 (b), assuming that the Pt/a-IGZO interface comprises a Schottky diode, since the $V_{Pt}$ condition corresponds to the forward bias condition of the diode. The $V_{GS}$ range tested here is far higher than $V_{th}$ to ensure sufficient turn-on of the channel, so that the supply of carriers into the forward-biased Schottky contact was sufficient. When the Schottky diode behaves ideally, $\eta$ should be close to 1. In contrast, when the recombination current or other parasitic effects dominate, such as bulk resistance, $\eta$ must increase [1, 24]. The $\eta$ of ASC-TFTs was 1.1 when $V_{DS}$ was lower than ~0.6 V suggesting that the Pt/a-IGZO contact behaves quite ideally under this forward bias condition. However, as the $V_{DS}$ increases further, $\eta$ starts to show a significant increase, suggesting that the channel starts to pinch off, and the parasitic resistance increases.

Finally, attempts were made to estimate the $\phi_{B}$ of the Pt/a-IGZO interface. In order to do this, the $I_{DS}$ must be measured under the $V_{Ti}$ condition, but, as shown in Fig. 5.13 (b),
this requires an exceedingly high $V_{GS}$ and $V_{DS}$ at room temperature. Therefore, the $T_m$ range for this device was shifted to higher values (75 – 120°C) compared with that for the Ti/Ni ASC-TFT. Fig. 5.15 shows the $I_{DS}$-$V_{DS}$ characteristics at various $T_m$ when $V_{Ti}$ was 0.1 V, where the $T_m$ range for this device was shifted to higher values (75 – 120°C) compared with that for the Ti/Ni to measure the appreciable current. As expected, $I_{DS}$ increases with increasing $T_m$ in all $V_{GS}$ regions, and the $V_{GS}$ value at which the appreciable current starts to show shifts toward the negative voltage region. However, it must be noted that the overall current range is still quite low, and the degree of shift is quite similar to that of the Ti/Ni ASC-TFT case, considering the different $T_m$ ranges adopted in this experiment. The increase in $I_{DS}$ with the increasing $T_m$ must be due to the increased thermionic emission and increased penetration of accumulation layer into the source contact area at higher $T_m$. Again, the strong interference of the accumulation layer with the $V_{GS}$ and the integral part of $V_{GS}$ by the SiO$_2$ does not allow for the estimation of the Schottky barrier at the Pt/a-IGZO interface using the standard Richardson-Schottky analysis. The very small current even with very high $V_{Ti}$ at room temperature did not allow for the appropriate simulation of the transfer characteristics, so the quantitative estimation of $\phi_B$ at that interface using the method shown in Fig. 5.12 was not feasible either. However, it is quite evident that $\phi_B$ at that interface is $>> ~ 1$ eV from the very small current.
Fig. 5.15. $I_D-S_D$ characteristics for various operation temperatures

S/D : Ti/Pt, $V_{TH} = 0.1V$

- 75°C
- 90°C
- 105°C
- 120°C
5.4. Summary

In summary, Ti, Ni and Pt were adopted as source/drain metals in a-IGZO TFTs, and the device performance variations according to the various source/drain metals were evaluated. The transfer characteristics of TFTs with Ti source/drain metal were superior to those of TFTs with Ni and Pt source/drain metal, which could be understood from the fact that Schottky-contacts were formed for the Ni and Pt cases due to the energy level differences between source/drain metal and a-IGZO, while the quasi-Ohmic nature at the Ti/a-IGZO interface resulted in fluent current flow. The device characteristics were well understood from the device simulation using the ATLAS package. The contact nature, whether it is of Schottky type or quasi-Ohmic, induced the largely different distribution of potential for the given gate and drain biases, which resulted in disparate carrier distribution and current path formation. The Schottky-type contact metals induced the channel formation even on the back surface of the channel when a high enough drain voltage was applied, even with the strong gate bias being applied, which would induce a strong carrier accumulation layer at the SiO₂/a-IGZO interface for the case of a quasi-Ohmic contact TFT.

Based on these results, ASC-TFTs, which integrate TFTs and Schottky diodes, were fabricated by applying different metal for each source and drain metal (Ti/Ni and Ti/Pt). When $V_{DS}$ was applied to high-$W_F$ metal, Ni or Pt, with grounded Ti metal, the transfer characteristics of ASC-TFTs were similar to the TFTs with Ti source/drain. When $V_{DS}$ was applied to Ti metal, however, the transfer characteristics of ASC-TFTs were similar to those of TFTs with the high-$W_F$ source/drain metal, i.e. Ni/Ni or Pt/Pt. The detailed
device characteristics were also well understood from the simulation of potential, carrier, and current distribution. The interfacial Schottky barrier at the Ni/a-IGZO interface was estimated to be ~0.32 eV, while that of the Pt/a-IGZO interface could not be estimated quantitatively. It was conjectured to be higher than ~1 eV from the very small electron injection at that interface. Even though the ASC-TFTs appear to be similar to the Schottky type diode in terms of the contact configuration, Schottky barrier modulation by varying gate bias voltage was not feasible due to the involvement of the thick gate dielectric layer and carrier accumulation layer, which penetrates into the contact metal overlap region.

The temperature-dependent current-voltage characteristics were governed by thermionic emission (and possible tunneling perhaps assisted by traps) at the rectifying Schottky junction, as well as the change of the current path below that contact region. It is expected that the peculiar electrical properties of ASC-TFTs may invoke new applications of such devices in the future.
5.5. References


6. Vertically integrated submicron amorphous-In$_2$Ga$_2$ZnO$_7$ Thin Film Transistor using a low temperature process

6.1. Introduction

Recently, vertically integrated transistors have received considerable attention in memory applications due to their potential to expand integration density to ultra-high values. [1-5] One representative example of such research efforts can be found in the vertically integrated NAND flash memory, where a charge-trap-type memory cell was fabricated using polycrystalline Si as the channel material of the memory thin film transistor (TFT). The selection of a polycrystalline material in this case tends to degrade device performance and hinder congruence among devices due to the presence of grain boundaries, which is unwanted for robust memory operation. [5] Furthermore, as silicon-based devices require high temperature processes to attain stable device performance, they cannot be easily implemented in devices that are fabricated on non-Si substrates. In this regard, the amorphous nature and high carrier mobility of In$_2$Ga$_2$ZnO$_7$ (a-IGZO) thin films, which can be achieved by simple sputtering processes at room temperature, attract a great deal of attention [6,7] for this approach, as shown in this report. The high performance of a-IGZO TFTs also allows them to be easily integrated with Si-based devices even at low processing temperature, which is another forte of this concept. [7-9] However, despite these promising factors, research on applications for a-IGZO has mostly been focused on the development of thin-film transistors for display or planar-type devices, and there are only a handful of reports on a-IGZO being implemented in novel
device structures. [8,10]

In this work, a vertically integrated TFT device (V-TFT) structure was suggested [11] and a-IGZO V-TFTs with submicron channel length were fabricated using a sputtering-based low temperature process. The effect of device geometry on device performance was examined in detail. The ultimate goal of this project is to fabricate a multi-layered vertically integrated NAND type flash memory, and this work reports the initial results of device fabrication and performance for a single-layer V-TFT. This structure is a very useful prototype that can check for the short channel effect and evaluate the influence of structural changes on the electrical performance of a-IGZO TFTs.
6.2 Experimental procedure

The a-IGZO V-TFTs were fabricated with a channel length (L) of 310nm as shown below. The entire process was performed at temperatures below 300 °C, suggesting it is applicable to plastic and glass substrates, as well as the Si wafer based process described in this study. Heavily doped n-type silicon was used as the substrate and source electrode, and a 300nm-thick SiO₂ layer deposited by plasma-enhanced chemical vapor deposition (PECVD) was implemented to separate the source and drain. A 300 nm-thick Molybdenum (Mo) layer was deposited as the drain metal electrode at room temperature and patterned as shown in Fig. 6.1 (a) using photolithography and wet-etching in a 50:1 H₂O₂/NH₄OH mixture solution. Part of the PECVD SiO₂ was dry etched, as can be seen in Figs. 1 (a) and (b), which show the plan-view optical microscopy and vertical scanning electron microscopy (SEM) images, respectively, of the fabricated samples. A 60nm-thick a-IGZO film was then deposited by RF magnetron sputtering at room temperature as the channel layer. [6] Since a-IGZO is a well-known n-type semiconductor, the heavily doped n-type silicon was used as the common source electrode, which may form a quasi-Ohmic contact with the a-IGZO, while the a-IGZO/Mo junction forms a non-negligible potential barrier in the contact region. The a-IGZO channel region was defined subsequently by a second step of photolithography and wet-etching in diluted hydrofluoric acid. Afterwards, 100nm-thick SiO₂ was deposited by PECVD at 200°C as the gate dielectric, and 300nm-thick Titanium (Ti) was deposited by sputtering at room temperature as the gate metal, which was then patterned as shown in Fig. 6.1 (a) using the same process as the Mo electrode. The fabricated V-TFTs were annealed in air at 200°C for one hour to stabilize
the contact resistance between the a-IGZO layer and the electrodes. The cross-section structure shown in Fig. 6.1 (b) conforms the vertical structure of the TFT along with the thickness of the a-IGZO channel layer, which is formed on the etched side area of the 300nm-thick PECVD SiO$_2$. The observed thickness was ~ 40 nm even though the target thickness was 60 nm, which is thought to come from the low step coverage of the RF sputtering process. This decreased channel thickness had no serious impact on device characteristics. The fabricated TFTs have a L of ~ 310nm due to the slightly slanted etching profile of the 300nm-thick PECVD SiO$_2$ layer. The channel width was maintained at 50 μm. The drain has a width of 20 μm while the source has an effectively infinite area. The electrical characteristics of the fabricated TFT devices were evaluated by measuring the current flowing from the source to the drain (I$_{DS}$) for a given drain voltage (V$_{DS}$) while applying gate bias (V$_{GS}$) to the Ti metal. The measurement was performed using a Hewlett Packard 4155B semiconductor parameter analyzer at room temperature.

![Fig. 6.1. (a) The plan-view optical microscopy and (b) vertical scanning electron microscopy images with channel length of 300nm](image)
6.3. Experimental results

The \( I_{DS}-V_{GS} \) characteristics of the a-IGZO V-TFTs for various \( V_{DS} \) are shown in Fig. 6.2 (a) and the inset figure shows the same graphs in the log scale. The V-TFTs show relatively well behaved transfer characteristics with an \( I_{on}/I_{off} \) (\( I_{on} \) is defined \( I_{DS} \) at \( V_{GS} \) of 10V and \( I_{off} \) is defined \( I_{DS} \) at \( V_{GS} \) of -10V) current ratio of \(~10^4\) and a threshold voltage \((V_{th})\) of 1.7V, where the \( V_{th} \) was determined from the linear fitting of an \( I_{DS}^{1/2}-V_{GS} \) plot at a \( V_{DS} \) of 10V. The sub-threshold swing (SS) at a \( V_{GS} \) of 0 and the \( I_{off} \) of the fabricated transistors are shown as a function of \( V_{DS} \) in Fig. 6.2 (b). It can be seen that as the \( V_{DS} \) increased, the SS also increased. The observed \( I_{on}/I_{off} \) current ratios are not large enough to suffice the requirements for memory applications, and this is rather strange considering the same IGZO channel material shows an \( I_{on}/I_{off} \) current ratio larger than \(~10^7\) in the bottom-gated planar structure. [6] The reason for such a relatively low performance comes from the high \( I_{off} \) and low \( I_{on} \) even at sufficiently large gate biases. Despite these pragmatic issues, the overall performance of the V-TFTs was still promising considering that these are only proto-types in a very premature stage.

The mobility characteristics evaluated using the following Eq. (1) showed that the mobility of the V-TFTs was only \(~0.03\)cm\(^2\)/Vs, which almost three orders of magnitude smaller than values observed in planer devices. This low effective mobility was attributed to the high parasitic resistances at the Mo/a-IGZO and n-type Si/a-IGZO interfaces and the high defect density in the a-IGZO channel that comes from the damage induced by the deposition of PECVD SiO\(_2\) on top, which both tend to decrease overall current. The low mobility (\( \mu \)) is related with the reduced \( I_{DS} \) as shown in Eq. (1).
Fig. 6.2. (a) The $I_{DS}-V_{GS}$ characteristics of the a-IGZO V-TFTs for various $V_{DS}$ and (b) sub-threshold slope at $V_{GS}$ of 0V and $I_{off}$ as a function of $V_{DS}$, where $I_{off}$ is defined $I_{DS}$ at $V_{GS}$ of -10V.
\[
\mu = \frac{2L}{WC_{ox}} \left( \frac{d\sqrt{I_{DS}}}{dV_{GS}} \right)^2
\]

(1)

where \( L, W, \) and \( C_{ox} \) are the channel length, width, and gate capacitance, respectively.

As described above, the V-TFTs show rather poor electrical performance because they have a high \( I_{off} \) and low \( I_{on} \). Resolving these issues require a thorough understanding on their causes, and therefore these aspects are studied in detail below. First, the possible reasons for the high \( I_{off} \) are examined. Fig. 6.2 (a) shows the transfer curves showing a general trend of being shifted into the negative voltage direction with an increased \( I_{off} \) when the \( V_{DS} \) is increased. This type of behavior is well known to be an outcome of drain induced barrier lowering (DIBL) in conventional metal oxide semiconductor field effect transistors (MOSFET). [12] However, there is no source-to-channel junction barrier in this a-IGZO TFT, so DIBL fails to explain this phenomenon. In order to understand this degradation in device performance with increasing \( V_{DS} \), the transfer characteristics are simulated with a TCAD simulator (SILVACO) using the device structures shown in Figs. 5.4 (b) and (c). The simulation parameters are: a donor-like trap density \( (N_d) \) of \( 1 \times 10^{20} \) cm\(^{-3}\)/eV with a characteristic energy slope of 0.2 eV, an acceptor-like trap density \( (N_a) \) of \( 1 \times 10^{18} \) cm\(^{-3}\)/eV with the characteristic energy slope of 0.3 eV, and an electron concentration \( (n_i) \) of \( 1.5 \times 10^{18} \) cm\(^{-3}\) in Fig. 6.3 (a); a \( N_d \) of \( 1 \times 10^{19} \) cm\(^{-3}\)/eV with a characteristic energy slope of 0.2 eV, an \( N_a \) of \( 1 \times 10^{17} \) cm\(^{-3}\)/eV with the characteristic energy slope of 0.3 eV, and an \( n_i \) of \( 1.5 \times 10^{17} \) cm\(^{-3}\) in Fig. 6.3 (b). Fig. 6.3 (a) generally well represents the experimental results especially when the \( V_{DS} \) and drain length \( (l_d) \) were 10 V and > 300 nm, respectively.
Fig. 6.3. TCAD simulation results of the transfer characteristics considering the different drain electrode length (5 to 600 nm), where the defects densities in (a) is assumed to be larger than that of (b) by one order of magnitude. Detailed defect densities are marked in the figures.
Fig. 6.3 (b) shows that the $l_d$ does not have a significant effect on $I_{\text{off}}$ and SS even with a $V_{DS}$ of 10 V when the defect densities ($N_d, N_a$) are low enough. However, when the defect density increased by one order of magnitude (Fig. 6.3 (a)), the curves show a large distortion in the sub-threshold–depletion region. The curves show a big hump in the sub-threshold–depletion region that results in a large increase in the SS value, and this tendency becomes even worse when $V_{DS}$ increases. This reproduces the experimental data shown in Fig. 6.2 (b) very well. Even when the $l_d$ is 5 nm, which actually corresponds to the planar structure when considering the drain geometry with respect to the channel, a certain amount of $V_{th}$ shift into the negative voltage direction is observed when increasing $V_{DS}$. However, this shift is largely increased when $l_d$ increases to $> 300$ nm, and it saturates when $l_d$ reaches 600 nm. This suggests that the large fringing field caused by the long drain electrode that lies perpendicular to the channel results in the high $I_{\text{off}}$ and large SS, in conjunction with the high defect density in the channel layer.

For long-channel TFTs, $V_{DS}$ does not affect channel depletion and the channel conductance is mainly governed by $V_{GS}$. In contrast, in short channel TFTs, the gate voltage induced depleted state of the channel can be affected by the $V_{DS}$, which may increase the $I_{\text{off}}$ even under large negative gate bias. In particular, the extended drain electrode structure shown in Fig. 6.1 (b) is very unfavorable to suppressing this adverse effect; when a large positive bias is applied to the drain, a positive electric field can be applied to the back surface of the channel due to the fringing field from the drain. When a negative $V_{GS}$ is applied to the gate, channel electrons are supposed to be depleted from the channel region. However, when the (positive) fringing field is large, the back surface of the a-IGZO can remain conductive due to the slight carrier accumulation in that region.
This would result in a large $I_{off}$ and negatively shifted $V_{th}$ in the output transfer curve of the device. This fringing field effect can also affect other parameters, such as the SS. The presence of a high defect density further enhances these negative effects. Compared with the standard back gate structure where the a-IGZO experiences almost no damage from other processing conditions, the PECVD SiO$_2$ layer implemented in this V-TFT structure severely damaged the channel region.

The much lower $I_{on}$ compared to planar TFTs (0.08µA vs. ~ 6.4µA at $V_{GS}$ and $V_{DS}$ of 10V) is also discussed below. Since a-IGZO TFTs are typical accumulation/depletion devices (lacking p-n junctions), the contact properties between the source/drain metal and the a-IGZO channel plays a very important role in deciding the output electrical characteristics of these devices. These properties become even more important in highly scaled devices because the ratio between the contact resistance and the total resistance increases as the channel length decreases. [10,13] The contact resistance is affected by the interfacial properties between the a-IGZO and the source/drain electrodes, which include the work function of the metal, the possible oxidation layer, and chemical interactions. As a metal-semiconductor contact generally has asymmetric carrier transfer characteristics with respect to bias polarity, the transfer characteristics should also be dependent on bias direction. It should be noted that V-FET has two different metal semiconductor interfaces, the Mo/a-IGZO junction and the a-IGZO/n-type heavily doped Si junction. The contact property between the Si and a-IGZO is mostly quasi-Ohmic because the electron affinity of a-IGZO and the work function of heavily doped n-type Si are similar (≈ 4.15 eV). [14] However, since the work function of Mo is 4.6 eV, the interface between Mo and a-IGZO could have a Schottky type contact. [15,16]
Fig. 6.4. (a) Sub-threshold slope and $I_{on}$ current as a function of $V_{DS}$, where $I_{on}$ is defined $I_{DS}$ at $V_{GS}$ of 10V and $I_{DS}$-$V_{GS}$ characteristics for various $V_{DS}$ in (b) forward bias and (c) reverse bias.
Considering these two contact types, it is expected that a higher electron current ($I_{on}$) flows when a positive $V_{DS}$ is applied to the Mo electrode, which is termed forward bias here. In contrast, a lower $I_{on}$ may flow when a positive $V_{DS}$ was applied to the n-type Si (defined as reverse bias) due to the non-negligible Schottky barrier at the Mo/IGZO interface. Fig. 6.4 (a) shows the SS and $I_{on}$ characteristics according to $V_{DS}$ for different bias directions, and Figs. 5.4 (b) and (c) show the corresponding transfer curves. The $I_{on}$ for the forward bias condition is much larger than the reverse bias condition, and the SS values of the reverse bias condition were larger than that of the forward bias condition. The parasitic resistance ($R_p$), which is the Mo/a-IGZO contact resistance in the case of reverse bias, degrades the SS of a TFT via. $SS = d(V_{GS} – I_{DS} R_p)/d(log I_{DS})$. [10] The asymmetric device performances are even more clearly seen in Fig. 6.5, which shows the variations of the $I_{DS}$ as a function of $V_{DS}$ for various $V_{GS}$. As discussed above, the $I_{DS}$ under forward bias conditions is much larger than the $I_{DS}$ under reverse bias conditions. However, even in the forward bias case, the non-negligible built in potential near the Mo junction decreases the $I_{on}$. Such asymmetrical transfer characteristics are usually not observed in planar devices, where both source and drain contacts are simultaneously made with the same materials. In addition, for the planar structure TFTs, the Mo source and drain contacts usually form quasi-Ohmic contact with the a-IGZO channel due to the heavy atom bombardment effect. [17, 18] However, in this case, the Mo layer was fabricated before the a-IGZO channel deposition, and intimate contact between the a-IGZO and Mo is not achieved.
Fig. 6.5. $I_{DS}$ as a function of $V_{DS}$ for various $V_{GS}$ (a) forward bias direction and (b) reverse bias direction.
A similar trend of asymmetrical transfer characteristics according to source/drain bias direction was also observed in a V-TFT with slightly different geometry but the same source (Si) and drain (Mo) junctions, which further confirms the theory presented here.

To estimate the asymmetric contact characteristics, another V-TFT of which schematic structure is shown in Fig. 6.6 (a) was fabricated and its characteristics are investigated. The advantage of this structure is that the contact area is independent of photo misalignments issue. As shown in Fig. 6.6 (b) above the $I_{sub} - V_{sub}$, which actually corresponds to the $I_{DS} - V_{DS}$ for zero gate voltage, shows the asymmetric transfer characteristics according to the bias polarity. These asymmetric characters are quite similar to that shown in Fig. 6.5, and the schematic band diagram shown in Fig. 6.7 explains well the results.

From the discussions above, it can be understood that the various degradations in the device parameters of this V-TFT device originated from the rather crude device geometry and fabrication processes, not from the inherent device characteristics. The large contact resistance between the Mo and a-IGZO can be easily improved by depositing a-IGZO before Mo deposition. The fringing field effect is difficult to alleviate as long as this type of device geometry is adopted. Perhaps short a $l_d$ will be helpful. However, the most effective method to suppress these adverse effects is to decrease defects in the a-IGZO layer, as can be understood from the simulation results shown in Fig. 6.3. As discussed earlier, defect generation in the a-IGZO channel layer is mostly induced by the PECVD of a gate dielectric layer on top, so a less defect-inducing process, such as atomic layer deposition, would be a feasible solution for these problems.
Fig. 6.6. (a) Schematic of a-IGZO V-TFT, (b) its transfer characteristics

Fig. 6.7. (a) Schematic of band diagram in terms of bias polarity
6.4 Summary

In summary, vertically integrated a-IGZO TFTs with submicron channel length (~310 nm) were fabricated using a simple and low temperature process (< 300 °C). The V-TFTs show well behaved transfer characteristics, with a relatively large $I_{on}/I_{off}$ ratio ($> 10^4$) and a $V_{th}$ of 1.7V. Even though this is a highly promising result considering the premature stage of vertically integrated a-IGZO TFTs, there are several problems that need to be improved in subsequent works: the high $I_{off}$, the low $I_{on}$, the large sub-threshold swing, and the asymmetric source/drain contact properties. These are mostly attributed to the high defect density in the a-IGZO channel region, which is mainly induced by the PECVD SiO$_2$ gate dielectric, and the large fringing field effect from the long and perpendicularly lying drain electrode. The high contact resistance between the Mo and a-IGZO resulted in the low $I_{on}$. However, it is believed that modifications in the fabrication process and device structure can improve overall device performance as these shortcomings are not of the intrinsic properties of the V-TFT.
6.5. References


7. Conclusions

In this dissertation, the operation characteristics of amorphous In$_2$Ga$_2$ZnO$_7$ (a-IGZO) Thin-Film-Transistors (TFTs) were investigated in detail. In addition, based on the understanding the operation characteristics, a vertically integrated TFT device (V-TFT) structure was suggested and a-IGZO V-TFTs with submicron channel length were fabricated using a sputtering-based low temperature process.

Firstly, a numerical simulation model was suggested to clarify the effects of material characteristics on device operation in a-IGZO TFTs. The localized states from donor-like states near the valance band edge and acceptor-like states near the conduction band edge were considered and the influence of these energy states were also analyzed in terms of the transfer characteristics of the device. Based on this model, the overall operation characteristics of a-IGZO TFT was investigated.

In addition, the electrical characteristics of channel and contact regions were separately examined by using the Transmission Line Method (TLM) for TFTs with two different contact metals, Ti and Mo. The different device performance according to the source/drain metal electrode attributed to the different contact characteristics than the process damage to the channel region. In addition, the device performance degradation was more serious for short channel devices with Mo contact due to the more involvement of damaged contact a-IGZO region. The experimental transport characteristics according to the source/drain electrode metal were reproduced by the simulation model, which accurately elucidates the damage distribution in the contact region.

Based on these results, Ti, Ni and Pt were adopted as source/drain metals in a-IGZO
TFTs, and the device performance variations according to the various source/drain metals were evaluated. The transfer characteristics of TFTs with Ti source/drain metal were superior to those of TFTs with Ni and Pt source/drain metal, which could be understood from the fact that Schottky-contacts were formed for the Ni and Pt cases due to the energy level differences between source/drain metal and a-IGZO, while the quasi-Ohmic nature at the Ti/a-IGZO interface resulted in fluent current flow. The device characteristics were well understood from the device simulation using the ATLAS package. The contact nature, whether it is of Schottky type or quasi-Ohmic, induced the largely different distribution of potential for the given gate and drain biases, which resulted in disparate carrier distribution and current path formation. The Schottky-type contact metals induced the channel formation even on the back surface of the channel when a high enough drain voltage was applied, even with the strong gate bias being applied, which would induce a strong carrier accumulation layer at the SiO$_2$/a-IGZO interface for the case of a quasi-Ohmic contact TFT.

Based on these results, asymmetric Schottky contact TFT (ASC-TFT), which integrate TFTs and Schottky diodes, were fabricated by applying different metal for each source and drain metal (Ti/Ni and Ti/Pt). When $V_{DS}$ was applied to high-$W_F$ metal, Ni or Pt, with grounded Ti metal, the transfer characteristics of ASC-TFTs were similar to the TFTs with Ti source/drain. When $V_{DS}$ was applied to Ti metal, however, the transfer characteristics of ASC-TFTs were similar to those of TFTs with the high-$W_F$ source/drain metal, i.e. Ni/Ni or Pt/Pt. The detailed device characteristics were also well understood from the simulation of potential, carrier, and current distribution. Even though the ASC-TFTs appear to be similar to the Schottky type diode in terms of the contact configuration,
Schottky barrier modulation by varying gate bias voltage was not feasible due to the involvement of the thick gate dielectric layer and carrier accumulation layer, which penetrates into the contact metal overlap region.

Finally, V-TFTs with submicron channel length (~310 nm) were fabricated using a simple and low temperature process (< 300 °C). The V-TFTs show well behaved transfer characteristics, with a relatively large $I_{on}/I_{off}$ ratio ($> 10^4$) and a $V_{th}$ of 1.7V.

In this dissertation, fundamental operation characteristics of a-IGZO TFTs were investigated and based on the understanding of operation characteristics, the novel devices structures were proposed and fabricated. By analyzing the operation characteristics of fabricated devices, novel devices application of AOSs TFTs were suggested.
List of Publications

1. SCI Journal


9. Ji Sim Jung, Sang-Ho Rha, Un Ki Kim, Yoon Jang Chung, Yoon Soo Jung, Jung-Hae Choi and Cheol Seong Hwang, "The charge trapping characteristics of Si3N4 and Al2O3


1. Taeyong Eom, Byung Joon Choi, Seol Choi, Tae Joo Park, Jeong Hwan Kim, Minha Seo, Sang Ho Rha, and Cheol Seong Hwang, "Ge_{2}Sb_{2}Te_{5} Charge Trapping Nanoislands with High-k Blocking Oxides for Charge Trap Memory", Electrochemical and Solid-State Letters, 12 (10) H378-H80 (2009) - Aug.
2. International Conference

10. Sang Ho Rha, Jisim Jung, Un Ki Kim, Yoon soo Jung, Yoon Jang Chung, Eun Suk Hwang, Byoung Keon Park, Mijung Lee, Jung-Hae Choi, and Cheol Seong Hwang,"Amorphous-In$_2$Ga$_2$ZnO$_7$ thin film transistor with the sub-micron vertical channel",2012 MRS Fall Meeting&Exhibit, Nov. 25 -30, Boston, MA 2012

9. Sang Ho Rha, Un Ki Kim, Jisim Jung, Woojin Jeon, Yeon Woo Yoo, Eun Suk Hwang, Byoung Keon Park, and Cheol Seong Hwang, "Performance variations of amorphous-In$_2$Ga$_2$ZnO$_7$ Thin-Film Transistors according to thin Al$_2$O$_3$ passivation layer deposited by atomic layer deposition", ECS 2012, Honolulu, Hawaii, Oct(7-12), Oct 9th (2012)


6. Jisim Jung, **Sang Ho Rha**, Yoon Soo Jung, Un Ki Kim, Yoon Jang Chung and Cheol Seong Hwang. "Study on the Charge Trapping Characteristics in Bottom-Gate InGaZnO Thin Film Transistors with Al₂O₃/SiO₂ Gate Dielectrics" 2011 MRS Fall Meeting & Exhibit, Nov. 28-Dec. 2, Boston, MA 2011


1. Taeyong Eom, Seol Choi, Byung Joon Choi, Sangho Rha, Woongkyu Lee, Cheol Seong Hwang and Moo Seong Kim, "Atomic Layer Deposition of (GeTe$_2$)$_x$(Sb$_2$Te$_3$)$_y$ Films Using Novel Precursors for Phase Change Memory.", MRS spring meeting 2010, San Francisco Marriott, April
3. Domestic Conference

7. Yoon Jang Chung, Un Ki Kim, Jeong Hwan Kim, Eric Hwang, Sang Ho Rha, and Cheol Seong Hwang, "Optical Modeling of NBIS instability and hole current in a-IGZO systems", 제 19회 한국반도체 학술대회, 고려대학교, 2월 15일~2월 17일


5. Taeyong Eom, Seol Choi, Byung Joon Choi, Min Hwan Lee, Taehong Gwon, Sang Ho Rha, Woongkyu Lee, Moo-Sung Kim, Manchao Xiao, Cheol Seong Hwang, "Atomic layer deposition of (GeTe2)1-x(Sb2Te3)x film for phase change memory", 제19회 반도체학술대회, 고려대학교 2/15~2/17, Feb 17th (2012)

3. Taeyong Eom, Seol Choi, Byung Joon Choi, **Sang Ho Rha**, Woongkyu Lee, Cheol Seong Hwang, Moo-Sung Kim, Manchao Xiao "Atomic Layer Deposition of \((\text{GeTe}_2)x(\text{Sb}_2\text{Te}_3)y\) films for phase change memories"(Oral), 제 18회 한국 반도체 학술대회, February 16-18 (2011)

2. T. Eom, S. Choi, B.J.Choi, **S.Rha**, W. Lee, C.S. Hwang, and M. S. Kim, "Atomic layer deposition of \((\text{GeTe}_2)x(\text{Sb}_2\text{Te}_3)y\) films using novel precursors", 제 17회 한국 반도체 학술대회, 호텔 인터불고 엑스코, 2. 24~26 (2010).

국문 초록

비정질 금속 산화물 반도체는 전기적 특성이 우수하고 투명하기 때문에 디스플레이 소자에 많은 연구가 진행 되어왔다. 이러한 특성은 금속 이온내의 S-orbital을 갖는 전자의 화동함수가 인접 금속과 중첩되는 영역이 크기 때문에, 비정질 상태에서도 결정상태와 동등한 수준의 전기적 특성을 갖는 특성이 있다. 그 결과로, 금속 산화물 반도체는 비정질 상태에서도 높은 전자 이동도와 높은 전자 밀도를 동시에 얻을 수 있다. 이러한 배경에서 amorphous-In_{2}Ga_{2}ZnO_{7} (a-IGZO)는 차세대 비정질 산화물 반도체로써 활발한 연구가 진행되고 있다. a-IGZO는 공정이 단순하고, 저온 공정에서도 우수한 전기적 특성 얻을 수 있는 장점이 있어 많은 연구가 진행되고 있으나, a-IGZO를 이용한 소자 개발연구는 소재의 우수한 특성에도 불구하고 주로 디스플레이 소자에 대해서만 연구되고 있다. 따라서, 본 논문에서는 a-IGZO Thin-Film-Transistor(TFT)의 동작 특성을 이해하고, 이러한 연구 결과를 기반으로 새로운 동작 특성을 갖는 TFT 소자를 제안함으로써, 메모리/로직 등의 반도체 소자에 적용 가능한 산화물 반도체 TFT소자의 기반 기술 확보를 목표로 하고 있다.

진행하였으며, 이와 함께 a-IGZO 내의 전자 밀도 및 계면 전하에 따른 소자의 동작 특성 변화를 분석하였다.

둘째로, 소자 scaling에 따른 소자 특성 연구를 진행하였다. 소자의 scaling에 따른 특성 연구 분야는 디스플레이 소자에서는 활발히 연구되지 않은 분야이지만, 메모리/로직과 같이 우수한 TFT 동작 특성을 요구하는 분야에서는 중요한 연구 분야이다. 본 연구에서는 Transmission Line Method (TLM)을 이용하여 소자의 scaling에 따른 전기적 특성 분석을 진행하였다. TLM 방법을 사용하게 되면 소스/드레인이 a-IGZO와 접촉면에 발생하는 접촉저항의 영향을 최소화하고, a-IGZO 채널층의 소자 특성을 얻어낼 수 있는 장점이 있다. 본 논문에서는 TLM 방법을 적용하여 소스/드레인의 접촉 저항이 scaling된 소자의 동작 특성에 미치는 영향을 분석하였다. 다양한 일람수를 갖는 금속을 소스/드레인 금속 전극으로 적용함으로써, 소스/드레인 전극이 소자의 동작 특성에 미치는 영향을 분석하였다. 특히 a-IGZO와 전극 금속의 일람수 차이를 이용하여 비대칭 쇼트키 접합을 갖는 TFT 소자(ASC-TFT)를 개발하였다. 새로 개발된 ASC-TFT 소자는 기존의 TFT 소자와 diode 특성을 동시에 나타내고 있으며, 매우 우수한 정류 특성을 나타내고 있을 뿐 아니라 게이트 전압에 따라 정류 특성을 조절할 수 있는 장점을 갖고 있다.

마지막으로, 수직 적층 구조의 TFT(V-TFT) 소자를 개발하였다. 고집적 고성능의 소자 특성을 요구하고 있는 메모리/로직 소자에 비정질 금속 산화물이 적용되기 위해서는 소재의 우수한 전기적 특성뿐만 아니라, 고집적의 소자를 제작할 수 있는 소자 기술이 요구된다. 본 논문에서는 산화물 반도체를 기반으로 하는 수직 적층 구조의 TFT 소자를 설계,
제작하였다. 제작된 V-TFT는 300nm의 매우 짧은 채널 길이를 갖고 있기 때문에, 이를 이용하여 산화물 반도체 TFT의 Short channel 효과와 소자의 구조에서 발생되는 유도 전계에 의한 TFT 소자 동작 특성 변화를 연구 진행하였다.

본 논문은, a-IGZO TFT의 동작 특성을 이해하고, 디스플레이 소자가 아닌 차세대 메모리/로직 소자에 응용을 위한 기반기술 확보를 목표로 하고 있다. 수치 해석 모델을 적용하여 a-IGZO 소자의 기본 동작 특성을 이해하고, 산화물 반도체의 물성과 TFT 소자의 구조적 특징이 소자의 동작 특성에 미치는 영향을 분석 하였다. 이러한 연구 결과를 바탕으로 새로운 동작을 갖는 ASC-TFT와 수직 구조 소자를 개발할 수 있었으며, 차세대 메모리/로직 반도체 소자에 금속 산화물 반도체가 적용되기 위한 기반 기술을 확보할 수 있었다.

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