M.S. THESIS

# Effects of Active Layer Thickness on the Electrical Characteristics of Solution-Processed In-Ga-Zn-O Thin Film Transistors

## 용액 공정 기반 IGZO 박막트랜지스터의 반도체층 두께 변화에 따른 전기적 특성 차이에 대한 연구

BY

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홍 예 원


홍예원의 공학석사 학위논문을 인준함
2016 년 2 월

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# Abstract

In recent years, amorphous indium gallium zinc oxide (a-IGZO) thin-film transistor (TFT) received great attention as one of the most promising candidates for the next generation of transparent and flexible electronics for displays due to favorable mobility in amorphous state, high large-area uniformity and so on. Moreover, to overcome problems of low performance and low uniformity of hydrogenated amorphous silicon (a-Si:H) and p-Si, respectively which were used widely as a switching and driving devices in the flat panel displays for the past few years, a-IGZO TFTs have been also suggested as potential replacements.

The film deposition methods based on vacuum process, such as radio frequency sputtering (rf sputtering), are generally used to deposit oxide semiconductor layer, but fabricating oxide TFTs using vacuum process is quite demanding because of high cost originated from expensive equipment. In contrast, solution process provides many advantages, such as low-cost, simplicity and high throughput, so several research groups have used sol-gel derived multicomponent oxide TFTs as active channel layer. Thus, many experiment of solution-processed a-IGZO TFTs have been reported to investigate their performances. However, further investigation about factors controlling electrical performances of solution-processed a-IGZO TFTs is still required to examine TFT characteristics. In this thesis, the active layer thickness ($t_{act}$) was investigated as one of these factors. We fabricated a-IGZO TFTs through two methods to change $t_{act}$, which were multi-stacking of active layers and depositing increased molarity of IGZO solution with decreased speed of spin-coating. Corresponding changes of electrical properties

with different $t_{act}$ were observed in both methods. As $t_{act}$ increases, the a-IGZO TFTs showed both decreased turn on voltage and threshold voltage owing to the increased free carriers in the channel and degraded field-effect mobility, on/off ratio and subthreshold swing because of increased surface roughness and trap density. These changes of performance of two different methods exhibited same dependence as changed $t_{act}$, however, the extent of changes was shown fairly different each other, to be more in detail, the result of second method exhibited more degraded one. Thus, in order to investigate the reason why these results were occurred, origins of change of electrical properties with different $t_{act}$ were investigated by X-ray reflection (XRR) and extraction of contact resistance ($R_C$) and comparison of results between two methods was also done. By analyzing this, the effect of $t_{act}$ on the electrical properties of solution-processed a-IGZO TFTs could be clarified to optimize electrical properties suitable for each applications and it could be also compared with that of vacuum-based TFTs. In addition, the results of solution-processed a-IGZO TFTs showed the significant improvement in the possibility of optimizing parameters controlling the electrical performances by changing $t_{act}$.

**Keywords:** thin film transistor (TFT), indium gallium zinc oxide (IGZO), solution process, active layer thickness, thin film density, contact resistance

**Student Number:** 2014-21695

# Contents

# List of Figures

# List of Tables

# Chapter 1

# Introduction

For a conventional active-matrix flat panel displays (AMFPD), hydrogenated amorphous silicon (a-Si:H) thin-film transistors (TFT) had been mostly used as a switching devices due to a merit of high large-area uniformity [1-2]. However, the mobility of a-Si:H is too low (< 1 $cm^2/Vs$) to be used as high resolution display and driving TFTs of active-matrix OLEDs (AMOLEDs). For this reason, many materials have been investigated, such as organic materials, Si-based materials and so on, and these days low-temperature polysilicon (LTPS) TFT is currently used for the commercial AMOLED display due to its high mobility (~ 100 $cm^2/Vs$) and good stability. However, LTPS TFTs also have the problems of low-uniformity and high fabrication cost [3].

Recently, amorphous oxide semiconductor (AOS) TFTs have received great attention as one of the most promising candidates for high performance next generation displays to overcome drawbacks of a-Si:H and LTPS TFTs since they have many advantages of favorable mobility (> 10 $cm^2/Vs$), good stability, and high uniformity [4]. In addition, thanks to high transparency in visible region and solution-processible fabrication, and capability of room-temperature process, they have been suggested as potential replacements for transparent and flexible electronics for displays. Characteristics comparison of various types of TFTs for display backplane is summarized in Table 1.1.

**Table 1.1 Characteristics comparison of various types of TFTs for display backplane [5]**

| | a-Si:H TFT | LTPS TFT | Oxide TFT |
|---|---|---|---|
| **Mobility ($cm^2/Vs$)** | ~ 1 | ~ 100 | ~ 30 |
| **Uniformity** | good | poor | good |
| **Stability** | poor | very good | good |
| **Light stability** | poor | good | Better than a-Si |
| **TFT type** | NMOS (LCD) | NMOS (LCD)<br>PMOS (OLED) | NMOS (LCD, OLED) |
| **TFT mask steps** | 4 ~ 5 | 5 ~ 11 | 4 ~ 5 |
| **Process temp.** | 150 ~ 350 ℃ | 350 ~ 450 ℃ | 150 ~ 400 ℃ |
| **Cost/yield** | Low/high | High/low | Low/high |
| **Possible display mode** | LCD, e-paper | High resolution LCD<br>OLED | LCD, OLED, e-paper |
| **Scalability** | Gen. 10 | Gen. 5.5 | Gen. 10 |
| **merits** | High uniformity | High stability | Low off current<br>No hot carrier effect |

Also, the characteristics of solution-processible fabrication made the manufacturing cost reduced due to inexpensive equipment compared with that of vacuum-process. Film deposition methods based on vacuum-process are generally used to deposit oxide semiconductor layer, but fabricating cost is high because of expensive equipment even if it enables film to be high-quality. In contrast, the solution process provides many merits besides cost, such as simplicity and high throughput, so several research groups have used sol-gel derived multicomponent oxide TFTs as active channel layer [6-7]. Many solution-processed oxide TFTs with various precursors, solvents, and stabilizers, such as ZTO, IZO, IZTO and

IGZO have been reported so far. One of these representative OS materials, IGZO has widely explored due to its great electrical performances. However, detailed investigation about solution-processed a-IGZO TFTs is still necessary and it is significant topic in order to realize optimized electrical performances of a-IGZO TFTs. Performance controllability would make control of performance of TFTs possible, resulting in suitable optimization of operation of TFTs for each required application. Therefore, further study about main factors of controlling the electrical properties of a-IGZO TFTs is important to examine TFT characteristics.

In this thesis, as one of these factors, an active layer thickness ($t_{act}$) was investigated. Different from the vacuum-processed TFTs with different $t_{act}$, the solution-based TFTs with different $t_{act}$ have not been so much demonstrated yet, thus, by this study, clarification of the effect of $t_{act}$ in solution-processed a-IGZO TFTs is possible and comparison of results between solution-based and vacuum-based changed $t_{act}$ a-IGZO TFTs is also available. Additionally, corresponding changes of electrical properties with different $t_{act}$ can be investigated and origins of those changes can be clarified, as well. These investigation can contribute to optimize electrical parameters for controlling performance of solution-processed a-IGZO TFTs. Therefore, to optimize electrical properties suitable for each applications and be compared with vacuum-process, the analysis of $t_{act}$ is necessary and it can be also a huge improvement in terms of realizing the low-cost and simple fabricating to control electrical parameters of TFTs.

We fabricated a-IGZO TFTs of two methods to change $t_{act}$, which were multi-stacking of active layers and using increased molarity of IGZO solution. Here, we focused on observing the effect of $t_{act}$ on the electrical performance of a-IGZO TFTs prepared by solution-processed method.

# Chapter 2

# Theory

## 2.1 Oxide Thin-Film Transistor

A thin-film transistor (TFT) is a special kind of field-effect transistor made by depositing thin films of an active semiconductor layer as well as dielectric layer and metallic contacts over a supporting substrate. The types of TFTs are classified according to semiconductor materials, such as Si-based, organic, oxide and so on. In other words, the oxide TFTs mean TFTs consisted of active layer of oxide materials, such as IZO, ZTO, IGZO, etc. Semiconductor materials can exist as not only crystalline phase but also amorphous phase, for example, of polycrystalline silicon (p-Si) and hydrogenated amorphous silicon (a-Si:H). In the case of p-Si, it usually shows high mobility and good stability against light, but they have problems of low-uniformity related with the grain boundaries during crystallization [3]. Therefore, amorphous semiconductors are preferred over polycrystalline ones for active layers in some aspects to overcome these problems. The a-Si:H has merits of processing temperature, simplicity of fabrication and uniformity of device characteristics compared to p-Si. However, it exhibited low-mobility associated with the intrinsic nature of the chemical bonding. Average carrier transport paths in a-Si:H consist of $sp^3$ orbitals with strong directivity, thus electronic levels are changed by the bond angle fluctuation significantly, resulting in high deep tail-states.

However, oxide semiconductors can show high mobility of over 10 $cm^2/Vs$ even in amorphous phase due to post-transition-metal cations [8]. Because of high ionicity originated from spatially spread metal *ns* orbitals with isotropic shape and the magnitude of overlap among the neighbouring metal *ns* orbitals with insensitivity in oxide semiconductors, they can show similar mobility compared with that of crystalline phase. The carrier transport paths of covalent semiconductors and oxide semiconductors are illustrated in Figure 2.1 [4]. These advantages of favorable performance and fabrication process attracts researchers to investigate to establish large-scale and high performance flat panel displays as replacement of silicon-based materials.

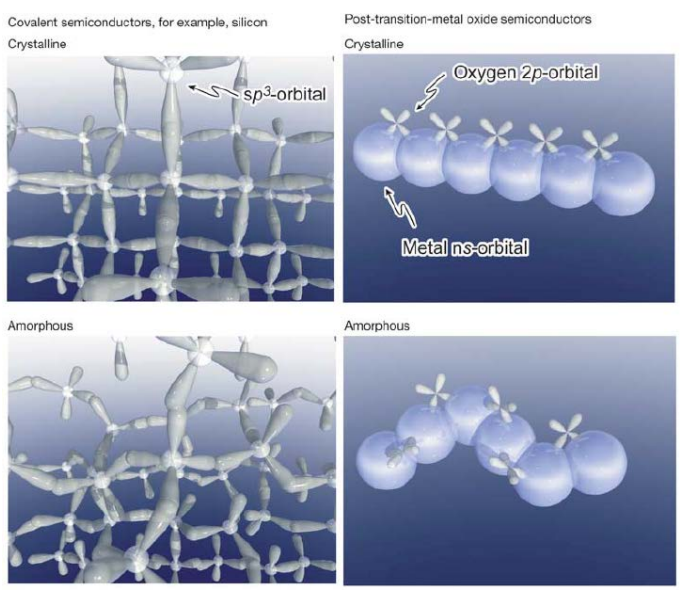
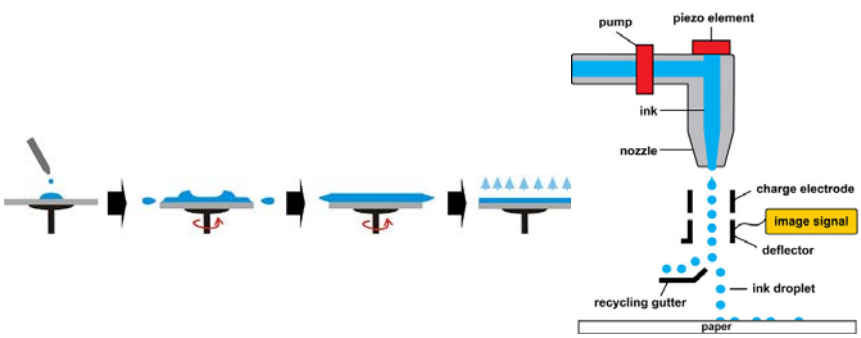



**Figure 2.1 Schematic orbital drawings for the carrier transport [4]**

In addition, oxide TFTs can be fabricated by solution-process as well as vacuum-process. To achieve low-cost process, solution-process should be necessary to be regarded. There are several possible ingredients that can be used to manufacture solution-processed oxide materials, such as metal alkoxide, metal organic acid salt, nitrate and chlorides. Many solution-processed oxide TFTs with various precursors, solvent and stabilizers, such as ZTO, IZO, IGZO and so on, have been reported. Oxide semiconductor solutions are manufactured mainly by spin coating and inkjet printing methods and their corresponding electrical properties were evaluated from many experiments. Under such circumstances, diverse coating and printing technologies and the corresponding material design were widely investigated and many groups succeeded in the manufacture of inkjet-compatible and spin-coatible high performance solution-processed oxide TFTs [9-10]. The illustration of spin coating and inkjet printing process is shown in Figure 2.2.




**(a)** **(b)**

**Figure 2.2 The illustration of (a) spin coating and (b) inkjet printing process**

Figure 2.3 shows the oxide TFT schematic structure with IGZO active layer. In this figure, the oxide TFT has bottom-gate and top-contact structure. Except for the fact that the active layer is oxide materials, the operation principles are same with those of a-Si TFT. Therefore, the drain current ($I_{DS}$) is modeled in the same way as a-Si TFT. The drain current equations of oxide TFTs are shown in equations (2.1) and (2.2) in linear and saturation region, respectively.

$$I_{DSsat} = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS} - V_{th})^2 \tag{2.1}$$

$$I_{DSlin} = \mu C_{ox}\frac{W}{L}\left(V_{GS} - V_{th} - \frac{V_{DS}}{2}\right)V_{DS} \tag{2.2}$$

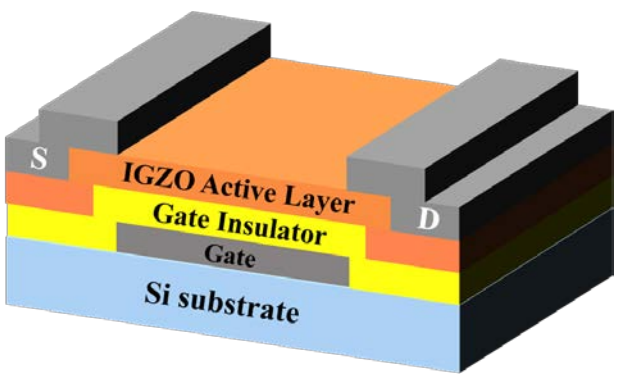



**Figure 2.3 Schematic IGZO TFT structure with bottom-gate and top-contact structure**

Structure of TFT is classified by where gate electrode is located with relative position of active layer. TFTs with gate electrode below the active layer are called as bottom-gate structure and with gate electrode above the active layer are called top-gate structure. Moreover, as location of the channel and source and drain

(S/D) electrodes, a coplanar type, which when they are in same plane, and staggered type, which when they are in different plane, can be divided. The common TFT device architectures and structures of oxide TFT are indicated in Figure 2.4 and Figure 2.5. The unique characteristics of oxide TFT compared with conventional TFT is etch stop layer (ESL) TFT. This structure is suggested for protection of back channel during formation of S/D electrodes and can guarantee high electrical stability even though it has a demerit of additional mask process because of formation of ESL pattern. Besides, the oxide TFT as TFT-LCD is necessary to show better electrical performances than that of a-Si:H TFT as the same BCE structure in the aspect of process compatibility with a-Si:H TFT and RC delay. Furthermore, many researches for overcoming issues, such as RC delay, S/D metallization, parasitic capacitance etc., about novel structure of oxide TFTs are being still investigated for being competitive compared to other TFTs.

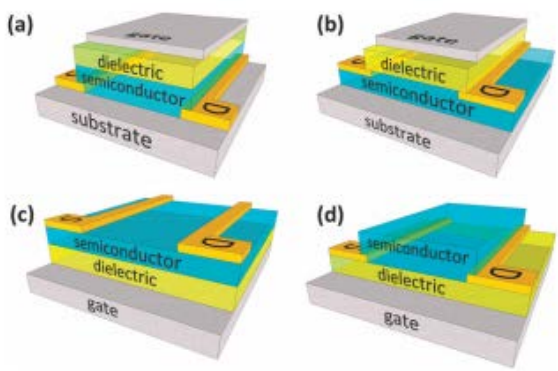



**Figure 2.4 Common TFT device architectures: (a) staggered, top gate; (b) coplanar, top gate; (c) staggered, bottom-gate; and (d) coplanar, bottom gate [11]**

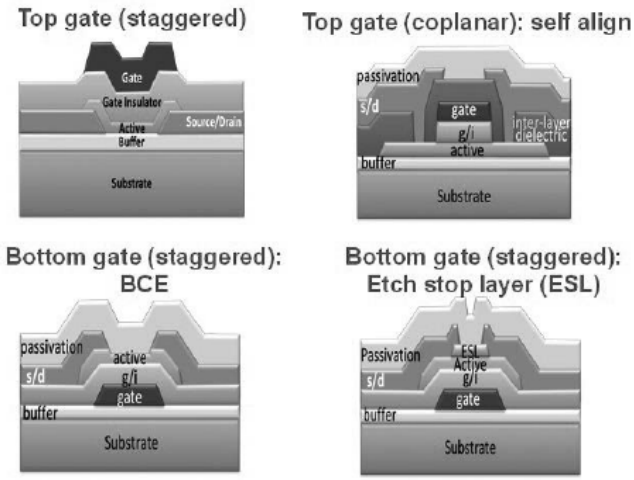



**Figure 2.5 Structures of oxide TFT [5]**

In these unique characteristics and novel efforts to achieve high performance TFTs, solution-processed metal oxide-based electronics is likely to become a significant contributor to future technological development in the area of large-area electronics.

## 2.2 Thin Film Property Analysis

### 2.2.1 X-ray Reflectivity Measurement

X-ray reflectivity (XRR) is a surface-sensitive analytical technique used in chemistry, physics, and material science to characterize surface, thin films and multilayers [12-13]. Thus, in order to analyze thin film properties, XRR measurement is widely used. The basic idea behind the technique is to reflect a

beam of x-rays from a flat surface and to then measure the intensity of x-ray reflected in the specular direction. The incident waves generate a specularly reflected wave, a refracted wave a diffused reflections, as shown in Figure 2.6. If the interface is not perfectly sharp and smooth then the reflected intensity will deviate from that predicted by the law of Fresnel reflectivity which is about the behavior of light when moving between media of differing refractive indices. The deviations can then be analyzed to obtain the density profile of the interface normal to the surface. X-ray reflection intensity curves from grazing incident X-ray beam to determine thin-film parameters including thickness, density and surface or interface roughness. The XRR method has the following characteristics:

1) It can be used to investigate a single-crystalline, polycrystalline or amorphous material.

2) It can be used to evaluate surface roughness and interface width nondestructively.

3) It can be used to investigate an opaque film under visible light.

4) It can be used to determine the layer structure of a multilayer or single-layer film.

5) It can be used to measure film thickness from several to 1000 nm.

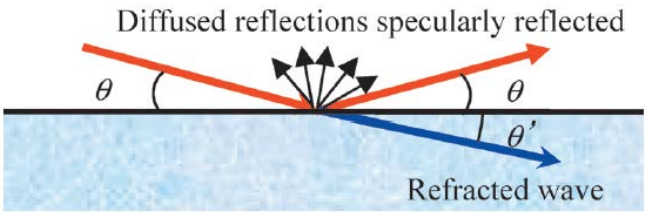



**Figure 2.6 Reflection and refraction of X-rays on material surface [14]**

In this regards, XRR measurement is appropriate to examine thin film properties. As it was mentioned above, information provided by XRR measurement can be film thickness, density and roughness. First of all, the intensity of X-ray reflectivity is calculated from each layer which is constructed from elemental species and filling rate of space. The reflectivity profile has oscillations caused by interference and these depend on the film thickness, and the thicker film, the shorter period of the oscillations. Secondly, the amplitude of oscillations and the critical angle for total reflection provide information on the density of films. The large the difference in the film density between substrate and film, the higher the amplitude of the oscillation. Lastly, in the case of rapid decrease of reflected X-ray means a large surface roughness. In other words, the larger roughness of a film, the faster the decay rate of X-ray reflectivity [14]. The XRR oscillation of solution-processed a-IGZO TFT is shown in Figure 2.7.

Due to the characteristics of nondestructive measurement of XRR, it can be widely used for evaluating the layer structure, thickness, density and surface or interface roughness of even a multilayer film. Also, many researches are using this method to analyze thin film properties [7, 15]. In this thesis, XRR measurement will be also used as analysis of film properties with different $t_{act}$ a-IGZO films.

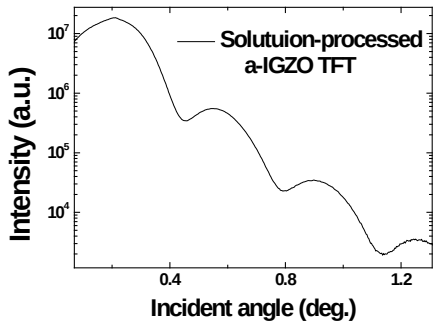



**Figure 2.7 The X-ray reflectivity result of solution-processed a-IGZO TFT**

## 2.3 Contact Resistance in Thin Film Transistor

### 2.3.1Transfer Length Method

In transistors and other electronic devices, such as TFTs, the contacts are a necessary part of the device and it is useful to determine the contact resistance so that some idea of how it might affect device performance can be obtained. In addition, it has an influence on performance degradation as well, thus it should be investigated in detail. A transfer length method (TLM) is one of the most common extraction of contact resistnace method. The TLM is a technique used in semiconductor physics to determine the contact resistance between a metal and semiconductor. In the case of TFT, it is the contact resistance between source/drain (S/D) electrodes and active channel layer. The TLM extracts contact resistance values from various channel lengths. The resistance between them is measured by applying a voltage across the contacts and measuring the resulting current, then a plot of resistance versus contact separation can be obtained. If the contact

separation is expressed in terms of the ratio of W/L, such a plot should be linear, with the slope of the line being the sheet resistance. The intercept of the line with the y-axis is twice of the contact resistance value.

Consider the TFT geometry shown in Figure 2.8. There are two types of contact resistance; one is channel resistance and the other is channel/metal(S/D) interface contact resistance. Thus, the total resistance can be expressed by equation (2.3).

$$\mathrm{R_T} = R_{ch} + 2R_C \tag{2.3}$$

where $R_T$ is the total resistance, $R_{ch}$ is channel resistance and $R_C$ is metal/channel resistance. Because there are two contacts between metal/channel, $R_C$ should be multiplied by 2.

$R_{ch}$ can be calculated from drain current equation (2.2) of TFT.

$$\mathrm{I_{DSlin}} = \mu C_{ox}\frac{W}{L}\left(V_{GS} - V_{th} - \frac{V_{DS}}{2}\right)V_{DS} \tag{2.2}$$

$$\mathrm{R_{ch}} = L/\mu C_{ox}W\left(V_{GS} - V_{th} - \frac{V_{DS}}{2}\right) \tag{2.4}$$

$$\mathrm{R_{ch}} = (L + \Delta 2L)/\mu C_{ox}W\left(V_{GS} - V_{th} - \frac{V_{DS}}{2}\right) \tag{2.5}$$

Equation (2.4) is extracted from ohm's law of equation (2.3) and at high $V_{GS}$, equation (2.5) is used in the replacement of equation (2.4) because channel length should be considered as effective channel length value, which is L+Δ2L and ΔL is gate-bias dependent value.

Therefore, the $R_T$ would be expressed as below equation (2.6).

$$R_T = (L + \Delta 2L)/\mu C_{ox} W \left(V_{GS} - V_{th} - \frac{V_{DS}}{2}\right) + 2R_C \qquad (2.6)$$

If TFTs of several different lengths are constructed, the total resistances of each can measured and plotted. A typical arrangement for a TLM pattern is shown in Figure 2.8. There is a single rectangular region that has the same doping (i.e. same sheet resistance) as the contact areas of the devices. Resistance measurements between each pair of contacts can be used to construct the TLM graph. In the case of TFT, with different $V_{GS}$ pairs, one can obtain the $\Delta L$ and $R_C$ as a function of the gate voltages, which is called as "paired $V_{GS}$ method" [16]. Therefore, with different effective channel lengths, the corresponding $R_T$ is extracted and thus $R_C$ can also be obtained.

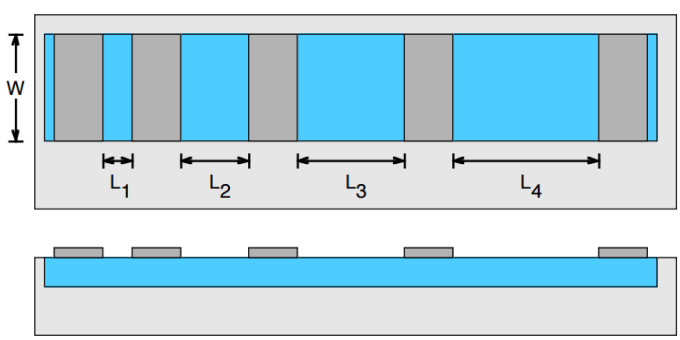



**Figure 2.8 A typical arrangement for different lengths contact areas**

# Chapter 3

# Experiments

## 3.1 Device Structure and Fabrication Flow

Bottom-gate and top-contact structure of a-IGZO TFTs were fabricated on heavily doped p-type Si substrate as gate electrode with a 200 nm thick thermally grown $SiO_2$ gate dielectric layer. The precursor solution of IGZO was prepared by dissolving total 0.137 M including zinc acetate, gallium nitrate and indium acetate in 2-methoxyethanol (2ME) solvent. To stabilize the solution, ethanolamine (EA) was added into the mixed solution and stirred at the temperature of 55 ℃ for 1 h.

Before depositing IGZO film, the substrate was cleaned in ultra-sonicator bath and ultraviolet (UV) ozone treatment was performed on the surface of $SiO_2$ for reducing residuals of organic particles to lower the surface energy. And then, the prepared solution was spin-coated at 4000 rpm for 30 s onto $SiO_2$ layer. The spin-coated IGZO TFTs were annealed at 500 ℃ in the furnace and the active layer was patterned using a conventional photolithography process. Samples with channel width of 1000 μm and length of 150 μm were fabricated. Aluminum (Al) deposition for S/D electrodes was performed by using a thermal evaporator. The performances of these a-IGZO TFTs were measured by semiconductor parameter analyzer (Agilent 4155C) in dark ambient condition. Total fabrication flow of spin-coated IGZO TFTs was illustrated in Figure 3.1.

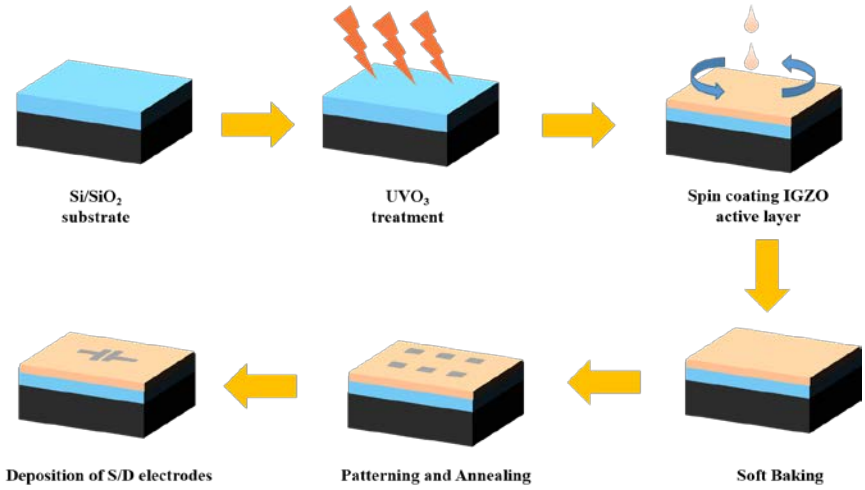



**Figure 3.1 Illustration of fabrication flow of spin-coated IGZO TFT on the heavily doped p-type Si substrate with thermally grown $SiO_2$, where Al S/D electrodes were thermally evaporated**

## 3.2 Sample Preparation

### 3.2.1 Two film depositing methods to change active layer thickness

Two-types of a-IGZO TFTs were fabricated to change active layer thickness ($t_{act}$). The first method is stacking layers several times with treating soft baking in the intervals of depositing layers. Thus, spin-coating and annealing were repeated as many times as the number of layers of multi-stacked active layers. Hereafter, this method will be called as “multi-coating”. In this experiment, the number of stacked layer was 1 (reference), 5 and 10. The multi-coating process illustration is shown in Figure 3.2. The second method to increase $t_{act}$ is changing molarity of solution and speed of spin-coating. According to already been found proof, the film thickness is proportional to deposited solution molarity and inversely proportional to spinning velocity of spin-coating [17]. Therefore, increasing the molarity of the solution and decreasing the speed of spin-coating could increase $t_{act}$. Hereafter, this method will be called as “molarity/speed”. In this experiment, three types of TFTs were fabricated; coated at 4000 rpm with reference solution (0.137 M), coated at 2500 rpm with three times higher molarity solution (0.411 M) and coated at 2500 rpm with five times higher molarity solution (0.685 M), respectively

The film thickness of these a-IGZO TFTs were measure by alpha-step (Nanospec AFT/2000) and atomic force microscopy (AFM, PSIA XE-100). These two-types of a-IGZO TFTs with different $t_{act}$ will be analyzed and compared each other in this thesis.

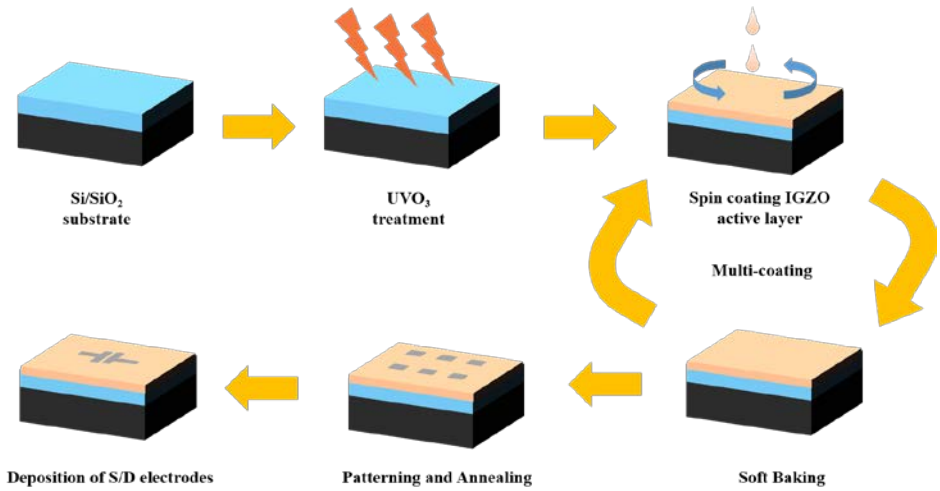



**Figure 3.2 The illustration of multi-coating process. TFTs coated once, 5 times and 10 times were fabricated**

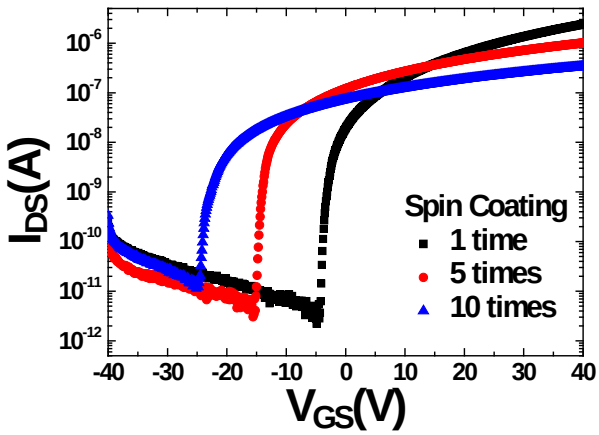
# Chapter 4

# Results and Discussion

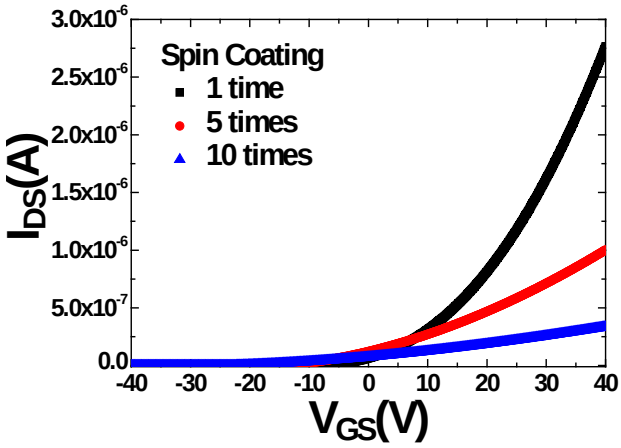
## 4.1 *I-V* characteristics

Figure 4.1 shows transfer curves of solution-processed a-IGZO TFTs with multi-coated active layers. It can be seen that the thickness of the channel layer is importance factor having strong impact on the TFT performance. According to AFM results, the once, 5 times and 10 times coating sample were 10, 65 and 130 nm, respectively. As $t_{act}$ increases, the turn-on voltage ($V_{on}$) and threshold voltage ($V_{th}$) of a-IGZO TFTs are shifted negatively. The on/off ratio decreases from 1.7E5 to 1.9E4 as the number of coting time changes from 1 to 10; off-current ($I_{off}$) increases and on-current ($I_{on}$) decreases. The mobility ($\mu$) is degraded with stacking layers from 1.05 to 0.072 $cm^2/Vs$. The subthreshold slope (S.S.) value of a-IGZO becomes high, which means a slow transition between off ($I_{off}$) and on ($I_{on}$). These changes of performance characteristics can be originated from not only change of film properties related to different $t_{act}$, but the effect of parasitic contact resistance. Therefore, in order to clarify this in detail, output characteristics is presented in Figure 4.2. The fact that there is no severe effect of parasitic contact resistance can be confirmed by the shape of output curves, such as no S-shape [18]. In other words, the parasitic contact resistance does not have a critical influence on the performance of a-IGZO TFTs we fabricated. It also shows a nice pinch-off and hard saturation, which is quite desirable for practical applications of the transistors. Consequently, it can be concluded that the change of transfer curves can be

contributed to the variation of film properties caused by different film thickness.

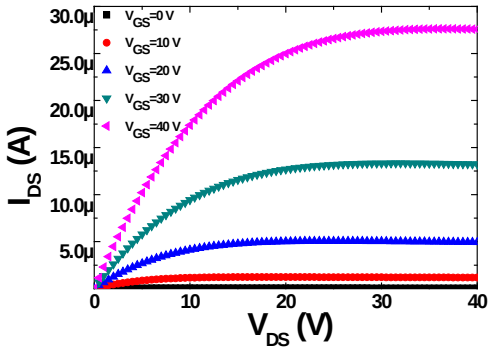



**(a)**

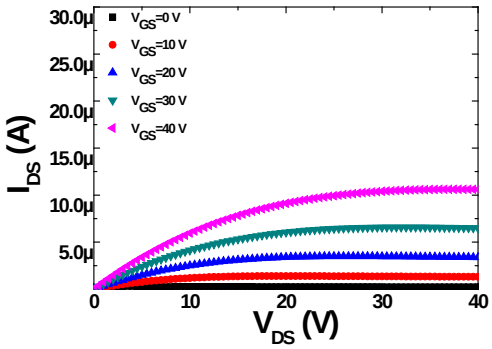



**(b)**

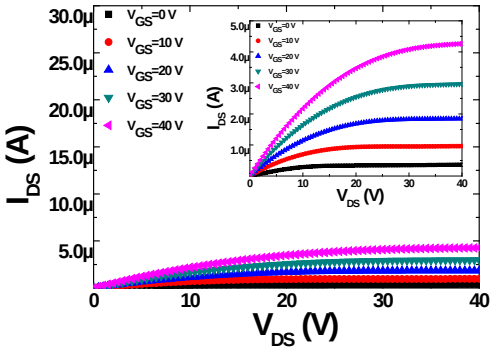
**Figure 4.1 Device performance of solution-processed a-IGZO TFTs with different active layer thickness (a) Transfer characteristics and (b) $I_{DS}$ vs. $V_{GS}$ at $V_{DS}$=1V with different number of coating times**




**(a)**

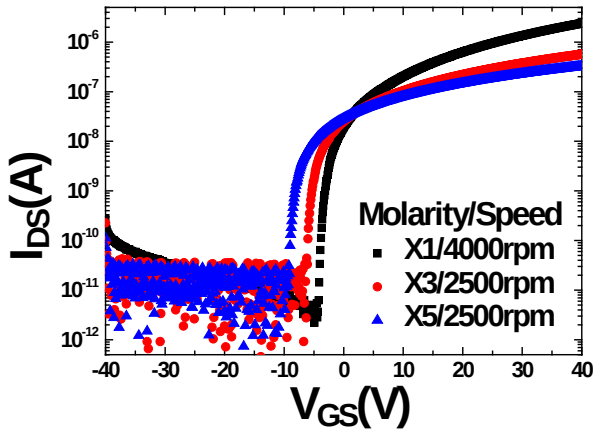



**(b)**

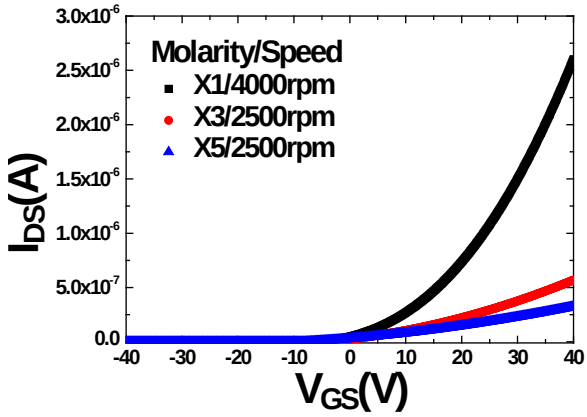



**(c)**

**Figure 4.2 Output characteristics for solution-processed a-IGZO TFTs of multi-stacked (a) once, (b) 5 times and (c) 10 times**




**(a)**

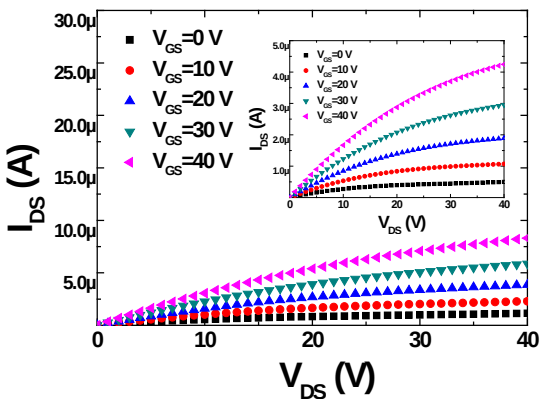



**(b)**

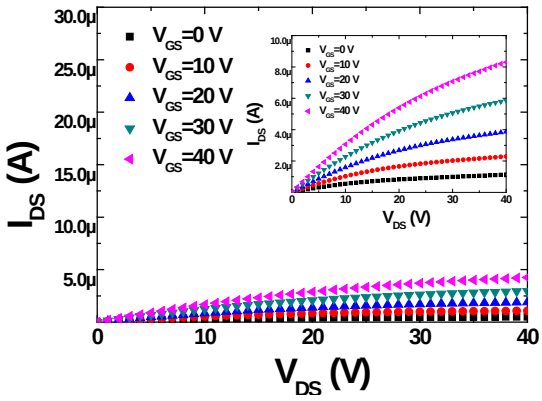
**Figure 4.3 Device performance of solution-processed a-IGZO TFTs with different active layer thickness (a) Transfer characteristics and (b) $I_{DS}$ vs. $V_{GS}$ at $V_{DS}$=1V with different molarity of solution and speed of spin coating**

In the case of changing solution molarity and spinning velocity of spin-coating, transfer curves are indicated in Figure 4.3. As a result of AFM measurement, the reference, 3 times higher molarity (0.411 M) with 2500 rpm and 5 time higher

molarity (0.685 M) with 2500 rpm coated samples were 10, 35 and 65 nm, respectively. As it can be seen in the Figure 4.3, the same dependence of change of performance as thicker $t_{act}$ was observed with that of multi-coating experiment, which means negatively shift of $V_{on}$ and degradation of on/off ratio, μ, and S.S. values. To be more specific, $V_{on}$, on/off ratio, μ, and S.S. are shifted from -5.19, 1.7E6, 1.05 and 0.36 to -8.53, 4.1E4, 0.089, and 1.16, respectively.




**(a)**




**(b)**

**Figure 4.4 Output characteristics for solution-processed a-IGZO TFTs coated in (a) 0.411 M solution at 2500 rpm and (b) 0.685 M solution at 2500 rpm**

Figure 4.4, and it had a nice pinch-off and hard saturation, which is appropriate for practical applications of the transistors without critical effects of parasitic contact resistance. These results mean as $t_{act}$ increases by either deposition method, $V_{on}$ shows negative shift and the other properties are degraded. Table 4.1 summarizes the device performances of a-IGZO TFTs with changing $t_{act}$ by two methods. A general shape of change of these parameters is shown in Figure 4.5.

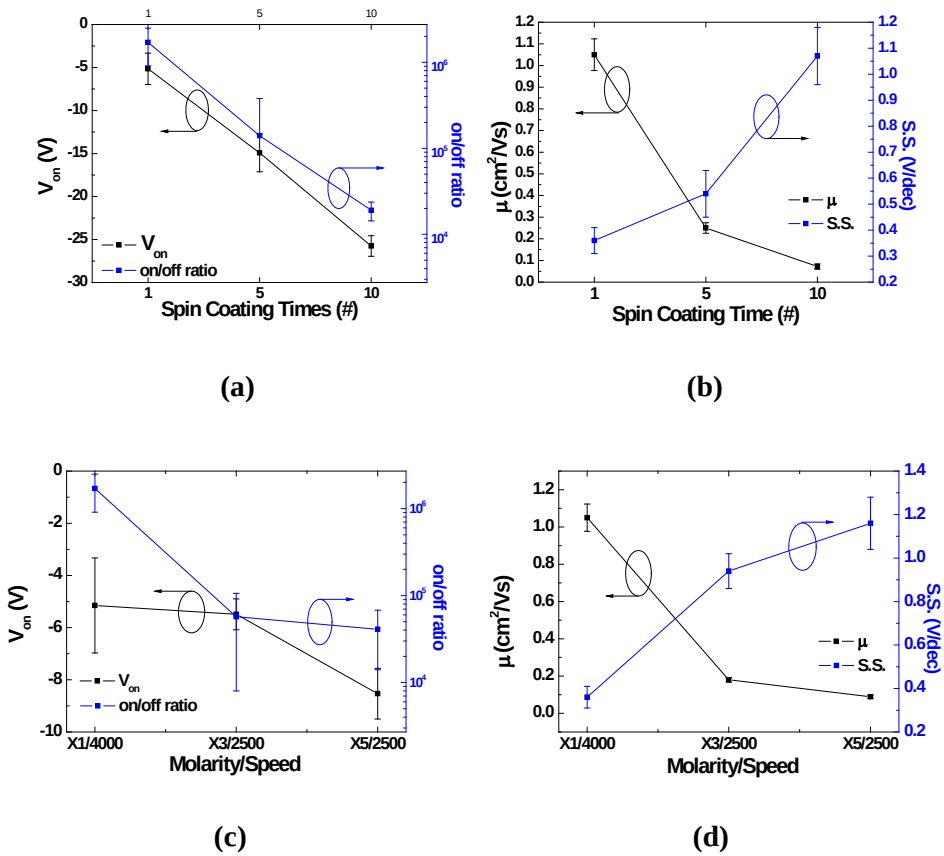



**Figure 4.5 The change of electrical parameters of the solution-processed a-IGZO TFTs characteristics for different active layer thickness fabricated by (a), (b) multi-coating and (c) and (d) molarity/speed**

**Table 4.1 Comparison of electrical characteristics with different active layer thickness fabricated by two methods for solution-processed a-IGZO thin films**

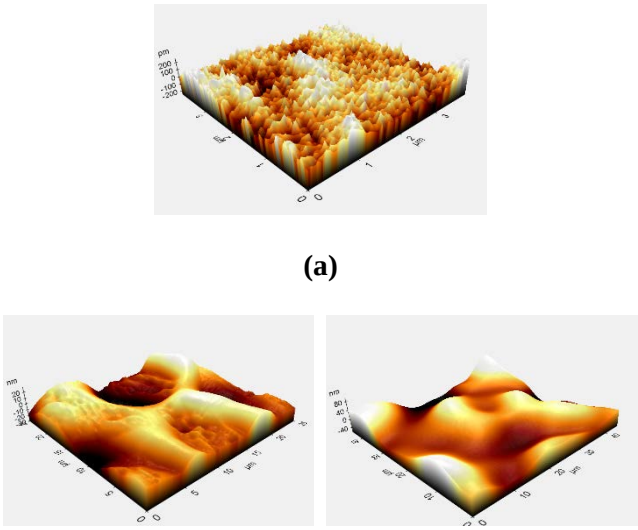
| | $V_{on}$ (V) | on/off ratio | μ ($cm^2$/Vs) | S.S. |
|---|---|---|---|---|
| **10 times** | -25.75 | 1.9E4 | 0.072 | 1.07 |
| **5 times** | -14.93 | 1.4E5 | 0.25 | 0.54 |
| **Reference** | -5.19 | 1.7E6 | 1.05 | 0.36 |
| **X3/2500 rpm** | -5.49 | 5.7E4 | 0.18 | 0.94 |
| **X5/2500 rpm** | -8.53 | 4.1E4 | 0.089 | 1.16 |

## 4.2 Analysis on Film Properties of a-IGZO TFTs with different active layer thickness

As it is indicated in Chapter 4.1, the change of performance with different $t_{act}$ can be confirmed. The origins of this phenomenon will be dealt with in this chapter. First of all, the negative shift of $V_{on}$ is contributed to the increased total number of free carriers in the channel region originated from the increased area of active layer. Therefore, to turn off the drain current, the higher absolute value of gate voltage is required for the device in the thicker film [19]. This can also explain the increased $I_{off}$ value as $t_{act}$ increases in Figure 4.1 and Figure 4.3. The increased free carriers lead to the high flow of electrons to pass through source and drain, resulting in increasing $I_{off}$ [20].

However, the thicker film has many defects and traps capturing electrons and the film density of the thick one is quite low because of the formation of middle interfaces in the case of multi-coating and many pores in the case of molarity/speed. Furthermore, the resistance between the channel and S/D electrodes also increases

due to the longer active channel layer region for electrons to flow and the more traps disturbing electron transport. Therefore, these phenomena contribute to the decreased $I_{on}$ with thicker film. According to AFM results, the root mean square (RMS) roughness of the a-IGZO films is 0.409, 11.648 and 22.562 nm for the number of 1, 5 and 10 times coating samples, respectively. This result is indicated in Figure 4.6.



**(a)**

**(b)** **(c)**

**Figure 4.6 AFM images of the a-IGZO thin films of (a) reference, (b) 5 times coating and (c) 10 times coating**

Because the RMS roughness monotonically increases with thicker $t_{act}$, it can be said that the influence of surface roughness on the carrier mobility is stronger at the increased film thickness. Thus, lower μ is observed with staking many layers and increasing solution molarity with decreased spinning velocity of coating as it can be seen in Table 4.1. The repeated deposition of layers in the case of the first

method using solution-process and the high molarity of solution in the case of second experimental one cause the increase of pores in the film, respectively. Carrier scattering resulting from the increased defects and film porosity with thicker layers can be also attributed to the decrease of μ [7]. The higher resistivity of thick film caused by the increased length for electrons to pass can be also one of the factors which make μ decreased. In the vacuum process, the $I_{on}$ and μ of oxide TFTs were independent on $t_{act}$ and this can be confirmed in Figure 4.7 [19]. However, it can be shown that the $I_{on}$ and μ of solution-based a-IGZO TFTs decrease with increased $t_{act}$ even though $V_{on}$ decreases. This different result is originated from the unique features of solution-process mechanism in comparison with those of vacuum-processed one, such as stacking layers, repetitive coating of the solution, and lowering speed of spin-coating as it is mentioned before. It means the solution-processed a-IGZO TFTs have a controllability of electrical properties by changing $t_{act}$.

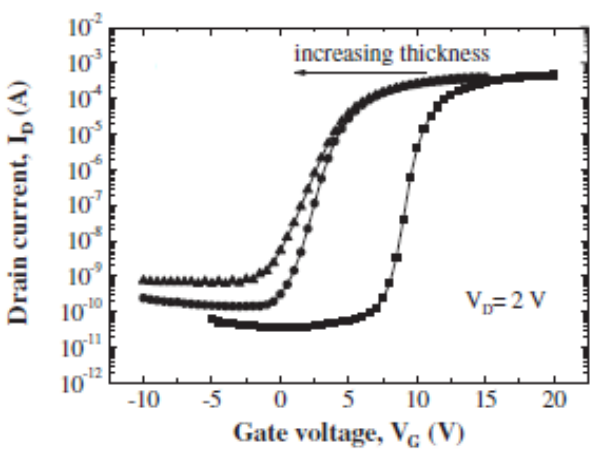



**Figure 4.7 Transfer characteristics of the vacuum-processed oxide (IZO) TFTs by rf (13.56 MHz) magneton sputtering as increasing $t_{act}$ from 15 to 60 nm**

With increasing $t_{act}$, the S.S. values of a-IGZO TFTs are getting high (i.e. the degradation of S.S.) as shown in Figure 4.4. From the S.S., the maximum density of surface sates, or the sheet trap density ($N_T$) can be inferred using the following equation (4.1).

$$N_T = \left\{S.S.\,(\log_{10} e)/(\frac{kT}{q}) - 1\right\} C_{ox}/q \tag{4.1}$$

where k is the Boltzmann's constant. T is the temperature and $C_{ox}$ is the unit gate capacitance. The degradation of S.S. with thicker film can be explained by the increased $N_T$. From the equation, it is shown that the S.S. of the a-IGZO TFTs is proportional to the $N_T$, which means as $t_{act}$ increases, the interfacial trap sites between gate dielectric and channel layer increase and it leads to high S.S. value. Additionally, the roughness is generally related to $N_T$; as the surface roughness value increases, defect levels trap more charges, and then the increased $N_T$ can be seen, which results in the deterioration of S.S. value, that is to say, the higher S.S. with thicker layer.

## 4.3 Comparison of a-IGZO TFTs with different active layer thickness fabricated by different methods

As it can be seen in Figure 4.1 and 4.3, two experimental methods exhibited same dependence of performance change with $t_{act}$, however, the extent of change of performance is quite different. Figure 4.9 exhibited plotted graphs of fabricated TFTs by two methods with thickness versus electrical performances, which are $V_{on}$, μ and on/off ratio, respectively. The mobility and on/off ratio values were plotted by log scale. For all performances, the results of molarity/speed method had more degraded ones at same thickness. Extracted slope of multi-coating results is -0.183, -0.021 and -0.011 and that of molarity/speed results is -0.329, -0.027 and -0.015 in the case of $V_{on}$, μ and on/off ratio, respectively. The absolute values of slope of molarity/speed are larger than those of multi-coating in all properties, which means steeper reduction of values, i.e. harder degradation.

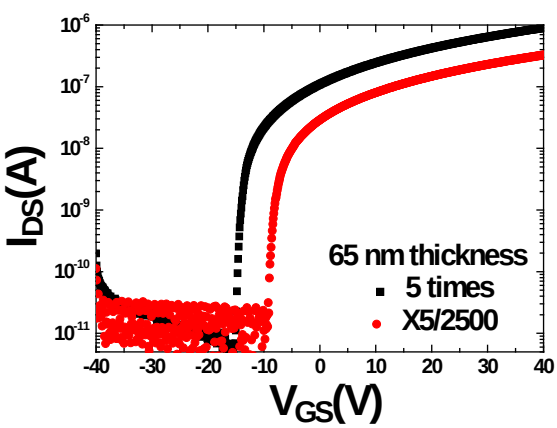
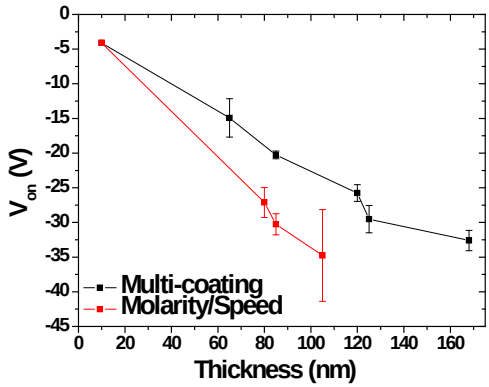
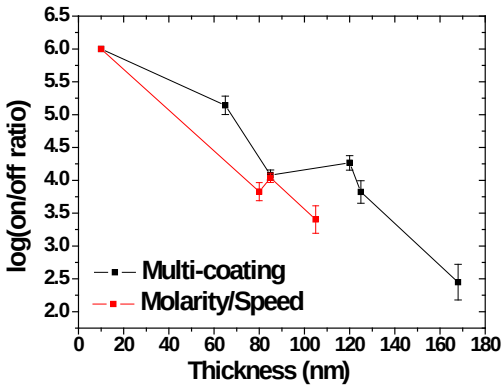


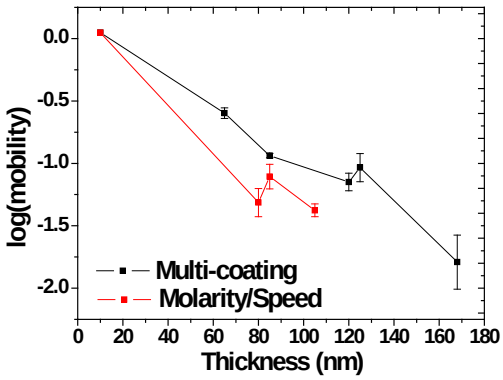

**Figure 4.8 Transfer characteristics of a-IGZO TFTs of same thickness fabricated by different methods each other**




**(a)**




**(b)**




**(c)**

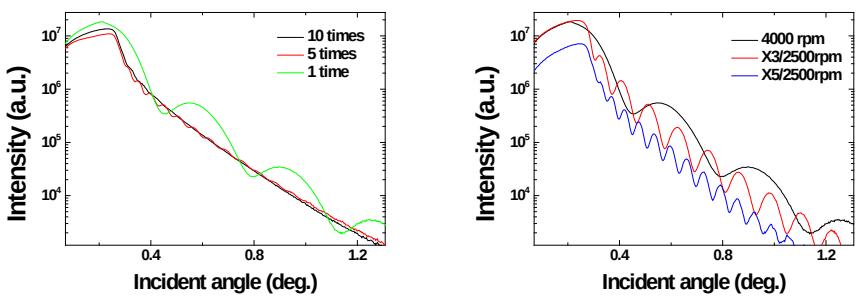
**Figure 4.9 Plotted results of fabricated TFTs by multi-coating and molarity/speed with thickness versus (a) $V_{on}$, (b) on/off ratio and (c) mobility**

For example, TFTs in Figure 4.8 are 5 times coated one (black) and used 5 times higher molarity solution with 2500 rpm (red) results, respectively. Both two TFTs are about 65 nm, however, their performance is not obviously same, to be more specific, the red one showed degraded result compared to that of the black one. This difference of properties between two results can be explained by film properties and contact resistance ($R_C$) and it will be considered in Chapter 4.3.1 in detail.

### 4.3.1 X-ray Reflectivity Results

Because it was turned out that the change of film properties with different $t_{act}$ had a significant influence on change of performance from previous investigation in Chapter 4.2, thus further analysis on film properties, such as density and roughness, of these two TFTs is worthwhile. In other words, it is inevitable to investigate fundamental interface and surface properties to look into the device performance closely. Therefore, XRR measurement was used as shown in Figure 4.10 and 4.11. First of all, Figure 4.10 shows XRR results of each coating methods, which are multi-coating and molarity/speed. Each result has same dependence of density and roughness with increased thickness, especially decreased density and increased roughness as thickness increases, which can be confirmed by smaller critical angle of first falling ripple and steeper slope of oscillations. However, in the case of multi-coating, the ripple of 10 times coating is very small and smooth since the thickness of film was too thick to be analyzed exactly by XRR, thus only the fact that the film of 10 times coating is thicker than that of 5 times coating could be verified by this result, instead of exact extracted value. Also, the critical angle of 5

times coating is similar with that of 10 times coating. However, because the amplitude of oscillation has also influence on the density, thus the fitted density result of 5 times coating considered all factors is larger than that of 10 times coating. The values of density of reference (i.e. 1 time and 4000 rpm in Figure 4.10 (a) and (b)), 5 times, 10 times, 3 times higher molarity solution with 2500 rpm and 5 times higher molarity solution with 2500 rpm are 5.493, 5.060, 4.961, 4.860 and 4.718, respectively, where the thickness is 8, 65, N/A, 35 and 65 nm, respectively. (As it was mentioned above, the exact value of thickness of 10 times coating could not be extracted)




**(a)** **(b)**

**Figure 4.10 XRR results of a-IGZO TFTs fabricated by different methods, which are (a) multi-coating and (b) molarity/speed**

Figure 4.11 exhibits XRR results of two TFTs of same thickness (65 nm) fabricated by different coating method. Compared with the reference (once coating with 4000 rpm), both samples have short distance of fringes, lower amplitude of oscillation and smaller critical angle, and the faster decay rate, which means thicker thickness, lower density and larger roughness [14]. However, if it is focused on

each result, graph of the molarity/speed experimental method showed lower density and harder roughness, which can be clarified by smaller critical angle and faster decay of reflected X-ray. In this result, the amplitude of oscillation of multi-coating is smaller than that of molarity/speed, however, the ripple also has an influence on not only density and but also roughness, thus when considered all factors, it can be said the density of multi-coating is larger than that of molarity/speed. This was also verified by XRR fitting simulation, which showed the density values of multi-coating and molarity/speed were 5.060 and 4.718 g/cm$^3$, respectively as it was mentioned above. Therefore, it can be concluded that lower film density and larger surface roughness significantly contributed to the harder performance degradation in the case of molarity/speed method, that is to say, lower μ, on/off ratio and S.S. characteristics.

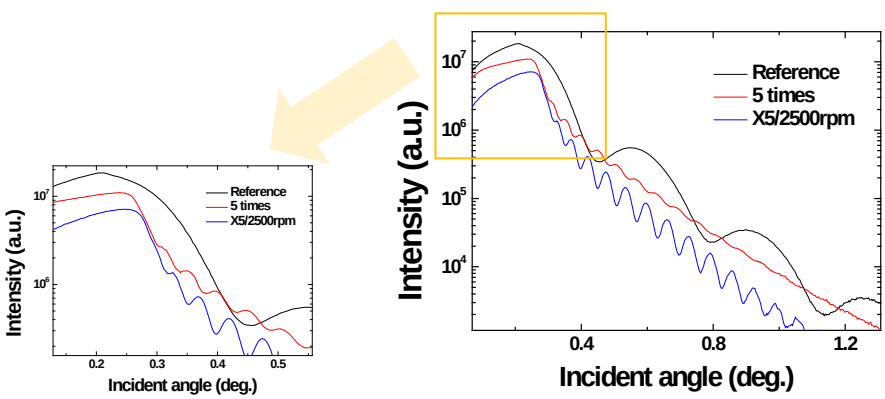
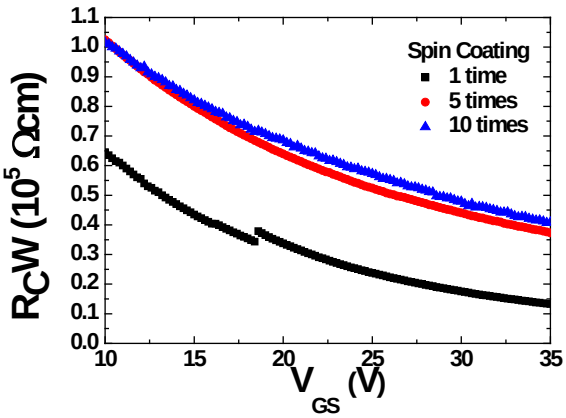


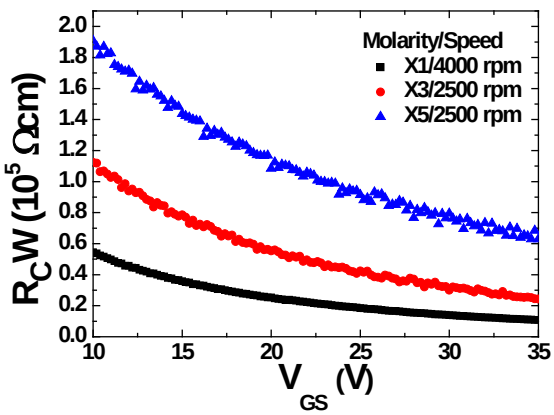

**Figure 4.11 XRR results of a-IGZO TFTs of same thickness fabricated by different methods each other**

### 4.3.2 Extraction of Contact Resistance

One of reasons to show the difference of change of performance between multi-coating and molarity/speed can be the effect of contact resistance ($R_C$) because $R_C$ strongly affects the device performance and there are many data also reported for oxide TFTs [21]. In this thesis, $R_C$ values were extracted by TLM, the channel width of TLM patterns was 1000 μm and the channel length was varied from 150 to 300 μm, while the gate voltage was modulated from 10 to 35 V. The width normalized resistance ($R_TW$) of the channel length is given by the sum of the channel resistance ($R_{ch}$) and $R_C$, depending on the gate voltage. The normalized contact resistance, $R_CW$ was calculated from the intersection of $R_TW$ for each gate voltage [16]. In the Chapter 4.1, it was proved that the $R_C$ did not have strong effect to performance of TFTs in the case of thicker film which were fabricated in above experiments owing to not much larger values compared to that of reference one. However, as shown in Figure 4.12, as $t_{act}$ increases in both methods, the $R_CW$ obviously increases as well because of longer channel layer region for electrons to flow and more traps disturbing electron transport. Therefore, this increased $R_CW$ would be attributed to the degradation of performance with thicker $t_{act.}$ In other words, the value of $R_CW$ is not large enough to affect change of performance itself, but obvious that it affects performance change as $t_{act}$ changes in both methods.




**(a)**




**(b)**

**Figure 4.12 Contact resistance of a-IGZO TFTs fabricated by (a) multi-coating and (b) molarity/speed method**

In Figure 4.12, the $R_CW$ of two methods exhibited same dependence with $t_{act}$, to be more in detail, the increase of $R_C$ with thicker layer, however, it is worthwhile to notice the exact value importantly. The $R_CW$ of molarity/speed is twice larger than that of multi-coating, which means this higher value of $R_CW$ impact directly on electron flow and the electrical properties of TFTs as well and it must have had an

influence on more severe degradation of performance in the case of molarity/speed method [22]. To sum up, extracted values of $R_C$ seem not to be critical to affect change of performance itself, however, the larger value of $R_C$ made TFTs fabricated by molarity/speed degraded more compared to multi-coating. In conclusion, the contact resistance has a contribution to degradation of performance in a-IGZO TFTs.

# Chapter 5

# Conclusion

In this thesis, the effect of active layer thickness ($t_{act}$) of solution-processed a-IGZO TFTs was investigated. The $t_{act}$ was controlled by multi-coating channel layers and increasing molarity of solution with decreased spinning velocity of spin-coating. It was shown changing $t_{act}$ could control the electrical performances of a-IGZO TFTs. The results could be also compared with those of vacuum-based oxide TFTs. Different from the results of vacuum-based one, which showed non-dependence of mobility and on/off ratio with $t_{act}$, the solution-processed a-IGZO TFTs with different $t_{act}$ showed consistent dependence of performance change with changed film thickness. The turn-on voltage and threshold voltage shifted negatively due to the increased free carriers with the increase of film thickness. As $t_{act}$ increase, the mobility, on/off ratio and subthreshold slope were degraded, which caused by the surface roughness and defect scattering in thicker film. The same dependence of performance with $t_{act}$ was exhibited in both fabrication methods, which are multi-coating and molarity/speed, thus it means either way can control electrical performance of solution-processed a-IGZO TFTs only with the change of $t_{act}$. However, the extent of change of performance for each case was found rather different. Generally, the result of molarity/speed showed more degraded one, such as lower mobility, on/off ratio and subthreshold slope compared to that of multi-coating and this was investigated by analysis of film property and contact resistance. By X-ray reflectivity (XRR) results, TFTs fabricated by molarity/speed had lower density and larger roughness even though it had same thickness with

TFTs fabricated by multi-coating. Thus, this lower density and harder roughness made performance deteriorated significantly, resulting in harder carrier scattering and so on in the case of molarity/speed. In addition, as a result of extraction of contact resistance by transfer length method, the contact resistance of molarity/speed method had twice larger than that of multi-coating at the same thickness of TFTs. In other words, the difference of contact resistance between two methods might affect the extent of performance degradation unequally.

By this investigation, the effect of $t_{act}$ of solution-processed a-IGZO TFTs could be clarified and examined in detail. The results showed the significant improvement in the possibility of optimizing parameters controlling electrical performances by changing $t_{act}$.

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# 국문 초록

# 용액 공정 기반 IGZO 박막트랜지스터의 반도체층 두께 변화에 따른 전기적 특성 차이에 대한 연구

서울대학교 대학원
전기정보공학부
홍 예 원

지난 수년간 디스플레이 기술의 바탕이 되었던 실리콘 (Si) 재료가 대면적이며 유연하고 투명한 차세대 디스플레이에의 이용에 전자 이동도와 대면적에서의 균등도 면에서 한계에 도달하면서 그 해결책으로써 비정질 인듐-갈륨-아연 산화물 반도체 기반의 박막 트랜지스터 (a-IGZO TFT)가 많은 주목을 받게 되었고 현재 그 연구와 개발이 활발히 이루어지고 있다. a-IGZO TFT는 투명 디스플레이에 적용이 가능한 넓은 광학적 밴드 갭을 갖고 있을 뿐 아니라, 비정질 상태임에도 불구하고 높은 전자 이동도와 대면적에서의 균등도로 고성능의 능동형 디스플레이 패널의 스위칭, 드라이빙 소자로도 사용될 수 있다는 장점이 있다. a-IGZO TFT는 진공 증착방식과 비진공 방식 기술로 만들어질 수 있는데, 기존의 진공 증착방식은 비싸고 복잡한 공정의 시스템을 이용하고 있어 최근에는 스핀코팅, 잉크젯 프린팅 등과 같은 비진공 방식 기술에 관한

연구가 활발히 이루어지고 있다. 이와 같은 방식을 용액공정이라고 부르며, 이는 가격이 저렴하고 공정이 단순하며 높은 수율을 낸다는 장점을 갖고 있다. 용액 공정 기반의 a-IGZO TFT에 대한 연구가 활발히 진행되고 있지만 그 성능을 조절하는 정확한 요소와 원인들에 대한 조사는 아직 미흡하다. 본 논문에서는 박막 트랜지스터의 반도체층을 그 중 하나의 요소로 보아, 용액 공정 기반의 a-IGZO TFT의 반도체층 두께 변화에 따른 성능 차이에 대한 연구를 수행하였다. 반도체층의 두께를 조절하기 위해 층을 반복하여 여러 번 쌓는 방식과 IGZO 용액의 농도를 높이고 스핀코팅 속도를 줄이는 방법을 사용했다. 그 결과 두 방법에서 모두 반도체층 두께 변화에 따라 전계효과 이동도, 문턱 전압, on/off 전류 비율, 문턱전압 이하에서의 기울기 등의 측면에서 같은 성능 변화 경향성이 발견되었다. 그러나 그 변화의 정도에서의 차이를 보였고 그 원인은 막의 밀도와 소스-드레인 전극과 반도체층 사이의 접촉 저항으로부터 기인한 것으로 분석되었다. 이 연구는 용액공정 기반 a-IGZO TFT의 반도체층 두께의 조절에 따라 그 성능의 결과를 예측하고 최적화할 수 있으며 각 원하는 응용처에 맞게 전기적 특성의 변화를 조절할 수 있다는 것을 시사한다.

Keywords: 박막 트랜지스터, 인듐-갈륨-아연 산화물 반도체, 용액 공정, 반도체층 두께, 박막 밀도, 접촉 저항
Student Number: 2014-21695

M.S. THESIS

# Effects of Active Layer Thickness on the Electrical Characteristics of Solution-Processed In-Ga-Zn-O Thin Film Transistors

## 용액 공정 기반 IGZO 박막트랜지스터의 반도체층 두께 변화에 따른 전기적 특성 차이에 대한 연구

BY

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FEBRUARY 2016

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING
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이 논문을 공학석사 학위논문으로 제출함
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서울대학교 대학원
전기·정보 공학부
홍 예 원


홍예원의 공학석사 학위논문을 인준함
2016 년 2 월

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| 위 원 장 | 이 창 희 | (인) |
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# Abstract

In recent years, amorphous indium gallium zinc oxide (a-IGZO) thin-film transistor (TFT) received great attention as one of the most promising candidates for the next generation of transparent and flexible electronics for displays due to favorable mobility in amorphous state, high large-area uniformity and so on. Moreover, to overcome problems of low performance and low uniformity of hydrogenated amorphous silicon (a-Si:H) and p-Si, respectively which were used widely as a switching and driving devices in the flat panel displays for the past few years, a-IGZO TFTs have been also suggested as potential replacements.

The film deposition methods based on vacuum process, such as radio frequency sputtering (rf sputtering), are generally used to deposit oxide semiconductor layer, but fabricating oxide TFTs using vacuum process is quite demanding because of high cost originated from expensive equipment. In contrast, solution process provides many advantages, such as low-cost, simplicity and high throughput, so several research groups have used sol-gel derived multicomponent oxide TFTs as active channel layer. Thus, many experiment of solution-processed a-IGZO TFTs have been reported to investigate their performances. However, further investigation about factors controlling electrical performances of solution-processed a-IGZO TFTs is still required to examine TFT characteristics. In this thesis, the active layer thickness ($t_{act}$) was investigated as one of these factors. We fabricated a-IGZO TFTs through two methods to change $t_{act}$, which were multi-stacking of active layers and depositing increased molarity of IGZO solution with decreased speed of spin-coating. Corresponding changes of electrical properties

with different $t_{act}$ were observed in both methods. As $t_{act}$ increases, the a-IGZO TFTs showed both decreased turn on voltage and threshold voltage owing to the increased free carriers in the channel and degraded field-effect mobility, on/off ratio and subthreshold swing because of increased surface roughness and trap density. These changes of performance of two different methods exhibited same dependence as changed $t_{act}$, however, the extent of changes was shown fairly different each other, to be more in detail, the result of second method exhibited more degraded one. Thus, in order to investigate the reason why these results were occurred, origins of change of electrical properties with different $t_{act}$ were investigated by X-ray reflection (XRR) and extraction of contact resistance ($R_C$) and comparison of results between two methods was also done. By analyzing this, the effect of $t_{act}$ on the electrical properties of solution-processed a-IGZO TFTs could be clarified to optimize electrical properties suitable for each applications and it could be also compared with that of vacuum-based TFTs. In addition, the results of solution-processed a-IGZO TFTs showed the significant improvement in the possibility of optimizing parameters controlling the electrical performances by changing $t_{act}$.

**Keywords:** thin film transistor (TFT), indium gallium zinc oxide (IGZO), solution process, active layer thickness, thin film density, contact resistance

**Student Number:** 2014-21695

# Contents

# List of Figures

# List of Tables

# Chapter 1

# Introduction

For a conventional active-matrix flat panel displays (AMFPD), hydrogenated amorphous silicon (a-Si:H) thin-film transistors (TFT) had been mostly used as a switching devices due to a merit of high large-area uniformity [1-2]. However, the mobility of a-Si:H is too low (< 1 $cm^2/Vs$) to be used as high resolution display and driving TFTs of active-matrix OLEDs (AMOLEDs). For this reason, many materials have been investigated, such as organic materials, Si-based materials and so on, and these days low-temperature polysilicon (LTPS) TFT is currently used for the commercial AMOLED display due to its high mobility (~ 100 $cm^2/Vs$) and good stability. However, LTPS TFTs also have the problems of low-uniformity and high fabrication cost [3].

Recently, amorphous oxide semiconductor (AOS) TFTs have received great attention as one of the most promising candidates for high performance next generation displays to overcome drawbacks of a-Si:H and LTPS TFTs since they have many advantages of favorable mobility (> 10 $cm^2/Vs$), good stability, and high uniformity [4]. In addition, thanks to high transparency in visible region and solution-processible fabrication, and capability of room-temperature process, they have been suggested as potential replacements for transparent and flexible electronics for displays. Characteristics comparison of various types of TFTs for display backplane is summarized in Table 1.1.

**Table 1.1 Characteristics comparison of various types of TFTs for display backplane [5]**

| | a-Si:H TFT | LTPS TFT | Oxide TFT |
|---|---|---|---|
| **Mobility ($cm^2/Vs$)** | ~ 1 | ~ 100 | ~ 30 |
| **Uniformity** | good | poor | good |
| **Stability** | poor | very good | good |
| **Light stability** | poor | good | Better than a-Si |
| **TFT type** | NMOS (LCD) | NMOS (LCD)<br>PMOS (OLED) | NMOS (LCD, OLED) |
| **TFT mask steps** | 4 ~ 5 | 5 ~ 11 | 4 ~ 5 |
| **Process temp.** | 150 ~ 350 ℃ | 350 ~ 450 ℃ | 150 ~ 400 ℃ |
| **Cost/yield** | Low/high | High/low | Low/high |
| **Possible display mode** | LCD, e-paper | High resolution LCD<br>OLED | LCD, OLED, e-paper |
| **Scalability** | Gen. 10 | Gen. 5.5 | Gen. 10 |
| **merits** | High uniformity | High stability | Low off current<br>No hot carrier effect |

Also, the characteristics of solution-processible fabrication made the manufacturing cost reduced due to inexpensive equipment compared with that of vacuum-process. Film deposition methods based on vacuum-process are generally used to deposit oxide semiconductor layer, but fabricating cost is high because of expensive equipment even if it enables film to be high-quality. In contrast, the solution process provides many merits besides cost, such as simplicity and high throughput, so several research groups have used sol-gel derived multicomponent oxide TFTs as active channel layer [6-7]. Many solution-processed oxide TFTs with various precursors, solvents, and stabilizers, such as ZTO, IZO, IZTO and

IGZO have been reported so far. One of these representative OS materials, IGZO has widely explored due to its great electrical performances. However, detailed investigation about solution-processed a-IGZO TFTs is still necessary and it is significant topic in order to realize optimized electrical performances of a-IGZO TFTs. Performance controllability would make control of performance of TFTs possible, resulting in suitable optimization of operation of TFTs for each required application. Therefore, further study about main factors of controlling the electrical properties of a-IGZO TFTs is important to examine TFT characteristics.

In this thesis, as one of these factors, an active layer thickness ($t_{act}$) was investigated. Different from the vacuum-processed TFTs with different $t_{act}$, the solution-based TFTs with different $t_{act}$ have not been so much demonstrated yet, thus, by this study, clarification of the effect of $t_{act}$ in solution-processed a-IGZO TFTs is possible and comparison of results between solution-based and vacuum-based changed $t_{act}$ a-IGZO TFTs is also available. Additionally, corresponding changes of electrical properties with different $t_{act}$ can be investigated and origins of those changes can be clarified, as well. These investigation can contribute to optimize electrical parameters for controlling performance of solution-processed a-IGZO TFTs. Therefore, to optimize electrical properties suitable for each applications and be compared with vacuum-process, the analysis of $t_{act}$ is necessary and it can be also a huge improvement in terms of realizing the low-cost and simple fabricating to control electrical parameters of TFTs.

We fabricated a-IGZO TFTs of two methods to change $t_{act}$, which were multi-stacking of active layers and using increased molarity of IGZO solution. Here, we focused on observing the effect of $t_{act}$ on the electrical performance of a-IGZO TFTs prepared by solution-processed method.

# Chapter 2

# Theory

## 2.1 Oxide Thin-Film Transistor

A thin-film transistor (TFT) is a special kind of field-effect transistor made by depositing thin films of an active semiconductor layer as well as dielectric layer and metallic contacts over a supporting substrate. The types of TFTs are classified according to semiconductor materials, such as Si-based, organic, oxide and so on. In other words, the oxide TFTs mean TFTs consisted of active layer of oxide materials, such as IZO, ZTO, IGZO, etc. Semiconductor materials can exist as not only crystalline phase but also amorphous phase, for example, of polycrystalline silicon (p-Si) and hydrogenated amorphous silicon (a-Si:H). In the case of p-Si, it usually shows high mobility and good stability against light, but they have problems of low-uniformity related with the grain boundaries during crystallization [3]. Therefore, amorphous semiconductors are preferred over polycrystalline ones for active layers in some aspects to overcome these problems. The a-Si:H has merits of processing temperature, simplicity of fabrication and uniformity of device characteristics compared to p-Si. However, it exhibited low-mobility associated with the intrinsic nature of the chemical bonding. Average carrier transport paths in a-Si:H consist of $sp^3$ orbitals with strong directivity, thus electronic levels are changed by the bond angle fluctuation significantly, resulting in high deep tail-states.

However, oxide semiconductors can show high mobility of over 10 $cm^2/Vs$ even in amorphous phase due to post-transition-metal cations [8]. Because of high ionicity originated from spatially spread metal *ns* orbitals with isotropic shape and the magnitude of overlap among the neighbouring metal *ns* orbitals with insensitivity in oxide semiconductors, they can show similar mobility compared with that of crystalline phase. The carrier transport paths of covalent semiconductors and oxide semiconductors are illustrated in Figure 2.1 [4]. These advantages of favorable performance and fabrication process attracts researchers to investigate to establish large-scale and high performance flat panel displays as replacement of silicon-based materials.

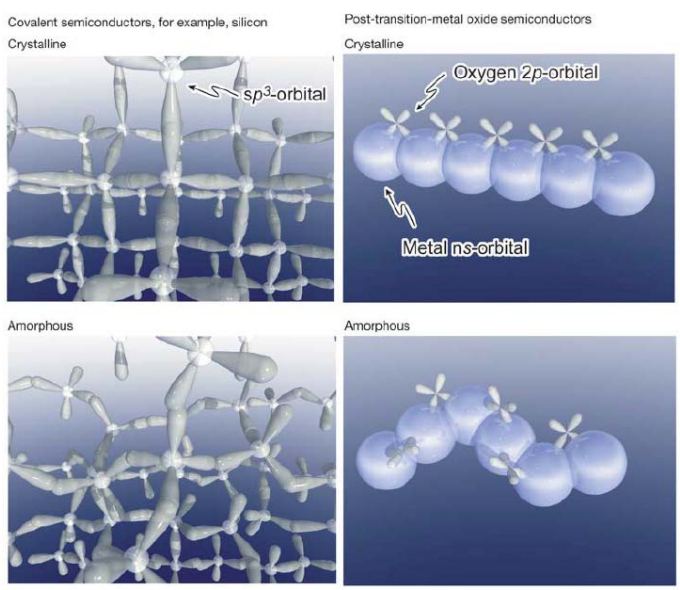
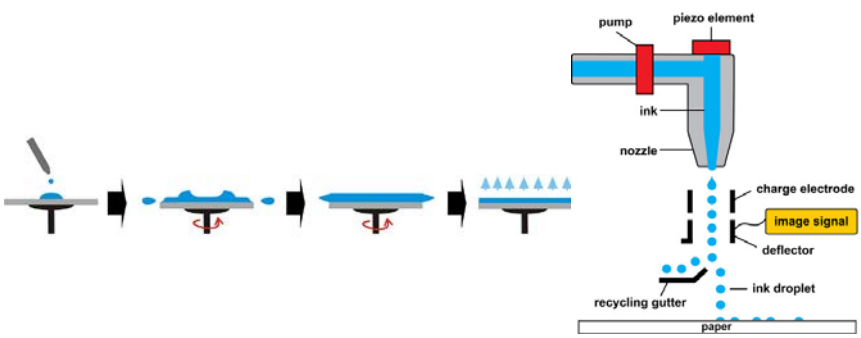



**Figure 2.1 Schematic orbital drawings for the carrier transport [4]**

In addition, oxide TFTs can be fabricated by solution-process as well as vacuum-process. To achieve low-cost process, solution-process should be necessary to be regarded. There are several possible ingredients that can be used to manufacture solution-processed oxide materials, such as metal alkoxide, metal organic acid salt, nitrate and chlorides. Many solution-processed oxide TFTs with various precursors, solvent and stabilizers, such as ZTO, IZO, IGZO and so on, have been reported. Oxide semiconductor solutions are manufactured mainly by spin coating and inkjet printing methods and their corresponding electrical properties were evaluated from many experiments. Under such circumstances, diverse coating and printing technologies and the corresponding material design were widely investigated and many groups succeeded in the manufacture of inkjet-compatible and spin-coatible high performance solution-processed oxide TFTs [9-10]. The illustration of spin coating and inkjet printing process is shown in Figure 2.2.




**(a)** **(b)**

**Figure 2.2 The illustration of (a) spin coating and (b) inkjet printing process**

Figure 2.3 shows the oxide TFT schematic structure with IGZO active layer. In this figure, the oxide TFT has bottom-gate and top-contact structure. Except for the fact that the active layer is oxide materials, the operation principles are same with those of a-Si TFT. Therefore, the drain current ($I_{DS}$) is modeled in the same way as a-Si TFT. The drain current equations of oxide TFTs are shown in equations (2.1) and (2.2) in linear and saturation region, respectively.

$$I_{DSsat} = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS} - V_{th})^2 \tag{2.1}$$

$$I_{DSlin} = \mu C_{ox}\frac{W}{L}\left(V_{GS} - V_{th} - \frac{V_{DS}}{2}\right)V_{DS} \tag{2.2}$$

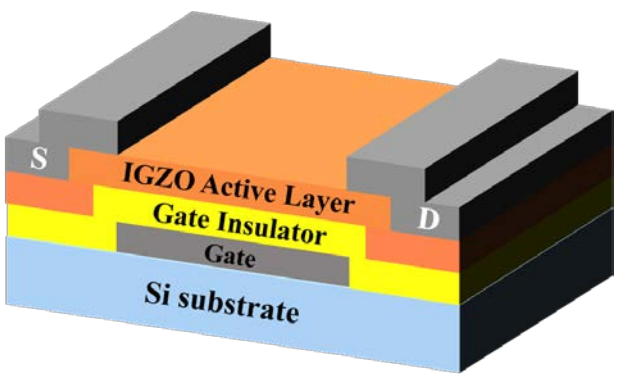



**Figure 2.3 Schematic IGZO TFT structure with bottom-gate and top-contact structure**

Structure of TFT is classified by where gate electrode is located with relative position of active layer. TFTs with gate electrode below the active layer are called as bottom-gate structure and with gate electrode above the active layer are called top-gate structure. Moreover, as location of the channel and source and drain

(S/D) electrodes, a coplanar type, which when they are in same plane, and staggered type, which when they are in different plane, can be divided. The common TFT device architectures and structures of oxide TFT are indicated in Figure 2.4 and Figure 2.5. The unique characteristics of oxide TFT compared with conventional TFT is etch stop layer (ESL) TFT. This structure is suggested for protection of back channel during formation of S/D electrodes and can guarantee high electrical stability even though it has a demerit of additional mask process because of formation of ESL pattern. Besides, the oxide TFT as TFT-LCD is necessary to show better electrical performances than that of a-Si:H TFT as the same BCE structure in the aspect of process compatibility with a-Si:H TFT and RC delay. Furthermore, many researches for overcoming issues, such as RC delay, S/D metallization, parasitic capacitance etc., about novel structure of oxide TFTs are being still investigated for being competitive compared to other TFTs.

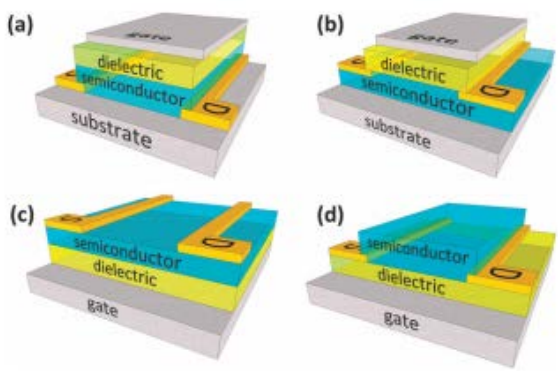



**Figure 2.4 Common TFT device architectures: (a) staggered, top gate; (b) coplanar, top gate; (c) staggered, bottom-gate; and (d) coplanar, bottom gate [11]**

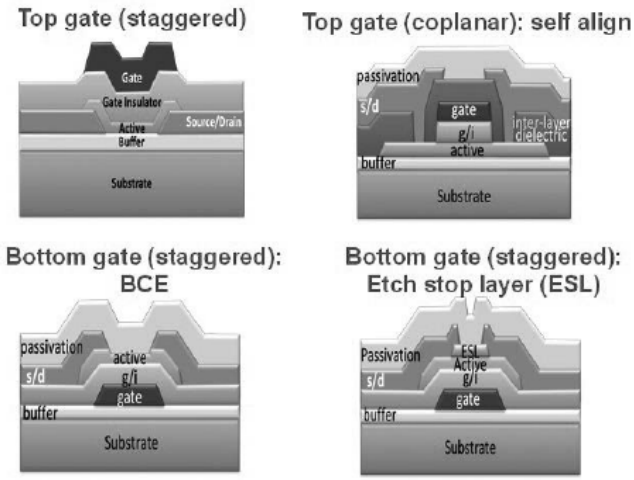



**Figure 2.5 Structures of oxide TFT [5]**

In these unique characteristics and novel efforts to achieve high performance TFTs, solution-processed metal oxide-based electronics is likely to become a significant contributor to future technological development in the area of large-area electronics.

## 2.2 Thin Film Property Analysis

### 2.2.1 X-ray Reflectivity Measurement

X-ray reflectivity (XRR) is a surface-sensitive analytical technique used in chemistry, physics, and material science to characterize surface, thin films and multilayers [12-13]. Thus, in order to analyze thin film properties, XRR measurement is widely used. The basic idea behind the technique is to reflect a

beam of x-rays from a flat surface and to then measure the intensity of x-ray reflected in the specular direction. The incident waves generate a specularly reflected wave, a refracted wave a diffused reflections, as shown in Figure 2.6. If the interface is not perfectly sharp and smooth then the reflected intensity will deviate from that predicted by the law of Fresnel reflectivity which is about the behavior of light when moving between media of differing refractive indices. The deviations can then be analyzed to obtain the density profile of the interface normal to the surface. X-ray reflection intensity curves from grazing incident X-ray beam to determine thin-film parameters including thickness, density and surface or interface roughness. The XRR method has the following characteristics:

1) It can be used to investigate a single-crystalline, polycrystalline or amorphous material.

2) It can be used to evaluate surface roughness and interface width nondestructively.

3) It can be used to investigate an opaque film under visible light.

4) It can be used to determine the layer structure of a multilayer or single-layer film.

5) It can be used to measure film thickness from several to 1000 nm.

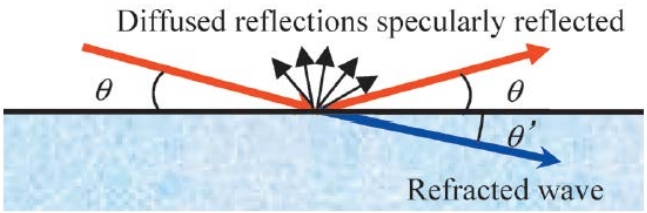



**Figure 2.6 Reflection and refraction of X-rays on material surface [14]**

In this regards, XRR measurement is appropriate to examine thin film properties. As it was mentioned above, information provided by XRR measurement can be film thickness, density and roughness. First of all, the intensity of X-ray reflectivity is calculated from each layer which is constructed from elemental species and filling rate of space. The reflectivity profile has oscillations caused by interference and these depend on the film thickness, and the thicker film, the shorter period of the oscillations. Secondly, the amplitude of oscillations and the critical angle for total reflection provide information on the density of films. The large the difference in the film density between substrate and film, the higher the amplitude of the oscillation. Lastly, in the case of rapid decrease of reflected X-ray means a large surface roughness. In other words, the larger roughness of a film, the faster the decay rate of X-ray reflectivity [14]. The XRR oscillation of solution-processed a-IGZO TFT is shown in Figure 2.7.

Due to the characteristics of nondestructive measurement of XRR, it can be widely used for evaluating the layer structure, thickness, density and surface or interface roughness of even a multilayer film. Also, many researches are using this method to analyze thin film properties [7, 15]. In this thesis, XRR measurement will be also used as analysis of film properties with different $t_{act}$ a-IGZO films.

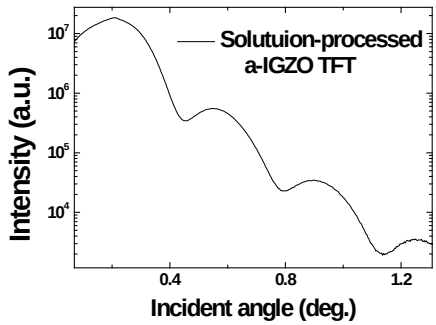



**Figure 2.7 The X-ray reflectivity result of solution-processed a-IGZO TFT**

## 2.3 Contact Resistance in Thin Film Transistor

### 2.3.1Transfer Length Method

In transistors and other electronic devices, such as TFTs, the contacts are a necessary part of the device and it is useful to determine the contact resistance so that some idea of how it might affect device performance can be obtained. In addition, it has an influence on performance degradation as well, thus it should be investigated in detail. A transfer length method (TLM) is one of the most common extraction of contact resistnace method. The TLM is a technique used in semiconductor physics to determine the contact resistance between a metal and semiconductor. In the case of TFT, it is the contact resistance between source/drain (S/D) electrodes and active channel layer. The TLM extracts contact resistance values from various channel lengths. The resistance between them is measured by applying a voltage across the contacts and measuring the resulting current, then a plot of resistance versus contact separation can be obtained. If the contact

separation is expressed in terms of the ratio of W/L, such a plot should be linear, with the slope of the line being the sheet resistance. The intercept of the line with the y-axis is twice of the contact resistance value.

Consider the TFT geometry shown in Figure 2.8. There are two types of contact resistance; one is channel resistance and the other is channel/metal(S/D) interface contact resistance. Thus, the total resistance can be expressed by equation (2.3).

$$\mathrm{R_T} = R_{ch} + 2R_C \tag{2.3}$$

where $R_T$ is the total resistance, $R_{ch}$ is channel resistance and $R_C$ is metal/channel resistance. Because there are two contacts between metal/channel, $R_C$ should be multiplied by 2.

$R_{ch}$ can be calculated from drain current equation (2.2) of TFT.

$$\mathrm{I_{DSlin}} = \mu C_{ox}\frac{W}{L}\left(V_{GS} - V_{th} - \frac{V_{DS}}{2}\right)V_{DS} \tag{2.2}$$

$$\mathrm{R_{ch}} = L/\mu C_{ox}W\left(V_{GS} - V_{th} - \frac{V_{DS}}{2}\right) \tag{2.4}$$

$$\mathrm{R_{ch}} = (L + \Delta 2L)/\mu C_{ox}W\left(V_{GS} - V_{th} - \frac{V_{DS}}{2}\right) \tag{2.5}$$

Equation (2.4) is extracted from ohm's law of equation (2.3) and at high $V_{GS}$, equation (2.5) is used in the replacement of equation (2.4) because channel length should be considered as effective channel length value, which is L+Δ2L and ΔL is gate-bias dependent value.

Therefore, the $R_T$ would be expressed as below equation (2.6).

$$R_T = (L + \Delta 2L)/\mu C_{ox} W \left(V_{GS} - V_{th} - \frac{V_{DS}}{2}\right) + 2R_C \qquad (2.6)$$

If TFTs of several different lengths are constructed, the total resistances of each can measured and plotted. A typical arrangement for a TLM pattern is shown in Figure 2.8. There is a single rectangular region that has the same doping (i.e. same sheet resistance) as the contact areas of the devices. Resistance measurements between each pair of contacts can be used to construct the TLM graph. In the case of TFT, with different $V_{GS}$ pairs, one can obtain the $\Delta L$ and $R_C$ as a function of the gate voltages, which is called as "paired $V_{GS}$ method" [16]. Therefore, with different effective channel lengths, the corresponding $R_T$ is extracted and thus $R_C$ can also be obtained.

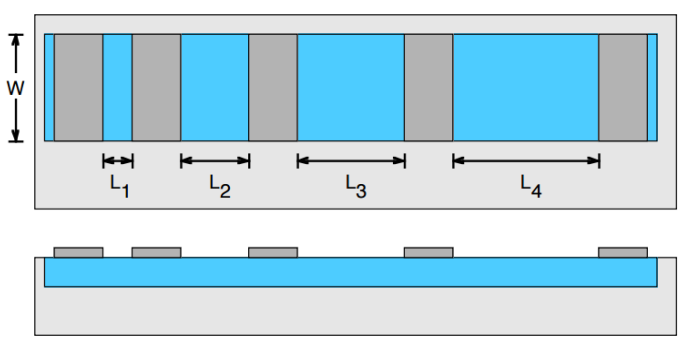



**Figure 2.8 A typical arrangement for different lengths contact areas**

# Chapter 3

# Experiments

## 3.1 Device Structure and Fabrication Flow

Bottom-gate and top-contact structure of a-IGZO TFTs were fabricated on heavily doped p-type Si substrate as gate electrode with a 200 nm thick thermally grown $SiO_2$ gate dielectric layer. The precursor solution of IGZO was prepared by dissolving total 0.137 M including zinc acetate, gallium nitrate and indium acetate in 2-methoxyethanol (2ME) solvent. To stabilize the solution, ethanolamine (EA) was added into the mixed solution and stirred at the temperature of 55 ℃ for 1 h.

Before depositing IGZO film, the substrate was cleaned in ultra-sonicator bath and ultraviolet (UV) ozone treatment was performed on the surface of $SiO_2$ for reducing residuals of organic particles to lower the surface energy. And then, the prepared solution was spin-coated at 4000 rpm for 30 s onto $SiO_2$ layer. The spin-coated IGZO TFTs were annealed at 500 ℃ in the furnace and the active layer was patterned using a conventional photolithography process. Samples with channel width of 1000 μm and length of 150 μm were fabricated. Aluminum (Al) deposition for S/D electrodes was performed by using a thermal evaporator. The performances of these a-IGZO TFTs were measured by semiconductor parameter analyzer (Agilent 4155C) in dark ambient condition. Total fabrication flow of spin-coated IGZO TFTs was illustrated in Figure 3.1.

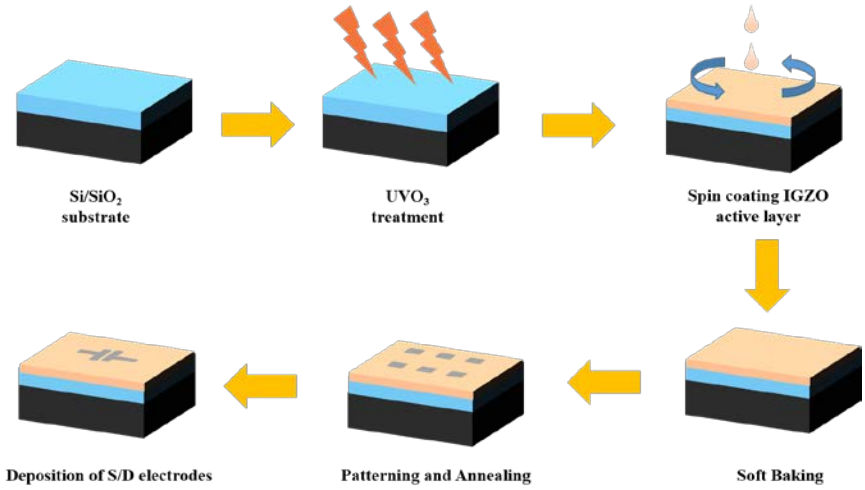



**Figure 3.1 Illustration of fabrication flow of spin-coated IGZO TFT on the heavily doped p-type Si substrate with thermally grown $SiO_2$, where Al S/D electrodes were thermally evaporated**

## 3.2 Sample Preparation

### 3.2.1 Two film depositing methods to change active layer thickness

Two-types of a-IGZO TFTs were fabricated to change active layer thickness ($t_{act}$). The first method is stacking layers several times with treating soft baking in the intervals of depositing layers. Thus, spin-coating and annealing were repeated as many times as the number of layers of multi-stacked active layers. Hereafter, this method will be called as “multi-coating”. In this experiment, the number of stacked layer was 1 (reference), 5 and 10. The multi-coating process illustration is shown in Figure 3.2. The second method to increase $t_{act}$ is changing molarity of solution and speed of spin-coating. According to already been found proof, the film thickness is proportional to deposited solution molarity and inversely proportional to spinning velocity of spin-coating [17]. Therefore, increasing the molarity of the solution and decreasing the speed of spin-coating could increase $t_{act}$. Hereafter, this method will be called as “molarity/speed”. In this experiment, three types of TFTs were fabricated; coated at 4000 rpm with reference solution (0.137 M), coated at 2500 rpm with three times higher molarity solution (0.411 M) and coated at 2500 rpm with five times higher molarity solution (0.685 M), respectively

The film thickness of these a-IGZO TFTs were measure by alpha-step (Nanospec AFT/2000) and atomic force microscopy (AFM, PSIA XE-100). These two-types of a-IGZO TFTs with different $t_{act}$ will be analyzed and compared each other in this thesis.

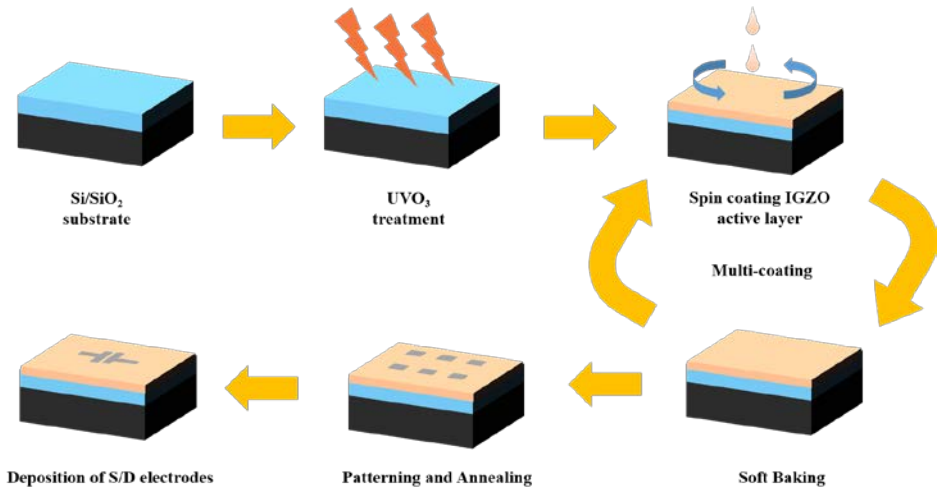



**Figure 3.2 The illustration of multi-coating process. TFTs coated once, 5 times and 10 times were fabricated**

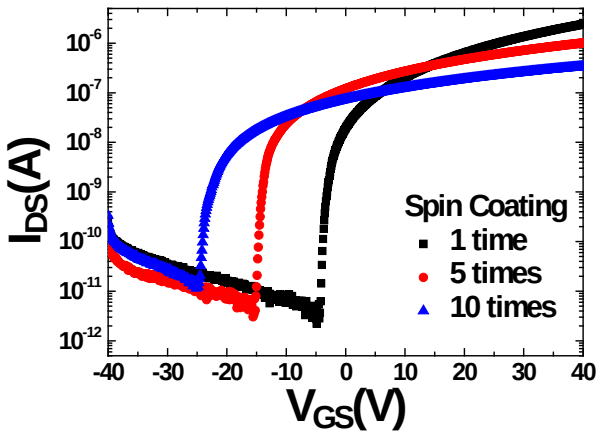
# Chapter 4

# Results and Discussion

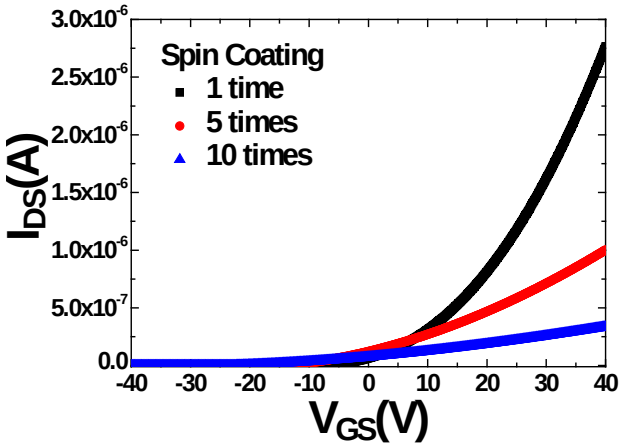
## 4.1 *I-V* characteristics

Figure 4.1 shows transfer curves of solution-processed a-IGZO TFTs with multi-coated active layers. It can be seen that the thickness of the channel layer is importance factor having strong impact on the TFT performance. According to AFM results, the once, 5 times and 10 times coating sample were 10, 65 and 130 nm, respectively. As $t_{act}$ increases, the turn-on voltage ($V_{on}$) and threshold voltage ($V_{th}$) of a-IGZO TFTs are shifted negatively. The on/off ratio decreases from 1.7E5 to 1.9E4 as the number of coting time changes from 1 to 10; off-current ($I_{off}$) increases and on-current ($I_{on}$) decreases. The mobility ($\mu$) is degraded with stacking layers from 1.05 to 0.072 $cm^2/Vs$. The subthreshold slope (S.S.) value of a-IGZO becomes high, which means a slow transition between off ($I_{off}$) and on ($I_{on}$). These changes of performance characteristics can be originated from not only change of film properties related to different $t_{act}$, but the effect of parasitic contact resistance. Therefore, in order to clarify this in detail, output characteristics is presented in Figure 4.2. The fact that there is no severe effect of parasitic contact resistance can be confirmed by the shape of output curves, such as no S-shape [18]. In other words, the parasitic contact resistance does not have a critical influence on the performance of a-IGZO TFTs we fabricated. It also shows a nice pinch-off and hard saturation, which is quite desirable for practical applications of the transistors. Consequently, it can be concluded that the change of transfer curves can be

contributed to the variation of film properties caused by different film thickness.

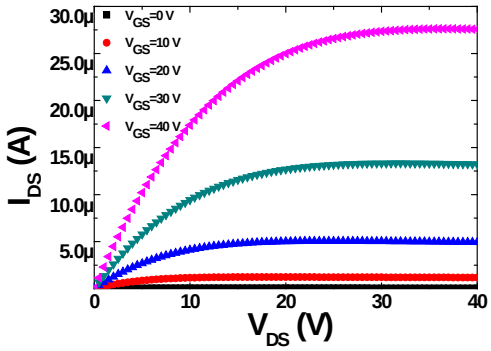



**(a)**

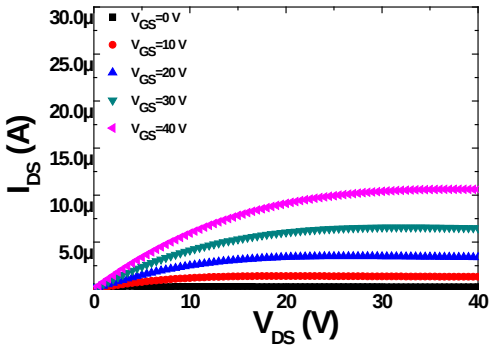



**(b)**

**Figure 4.1 Device performance of solution-processed a-IGZO TFTs with different active layer thickness (a) Transfer characteristics and (b) $I_{DS}$ vs. $V_{GS}$ at $V_{DS}$=1V with different number of coating times**




**(a)**

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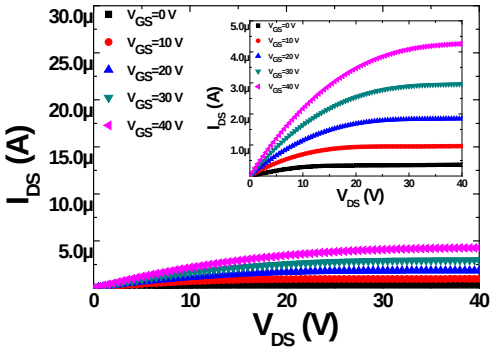
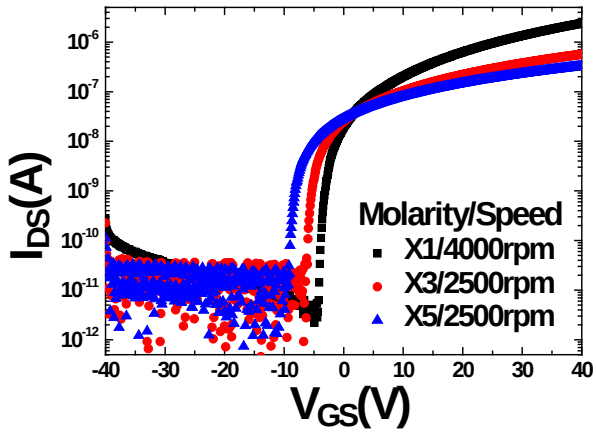
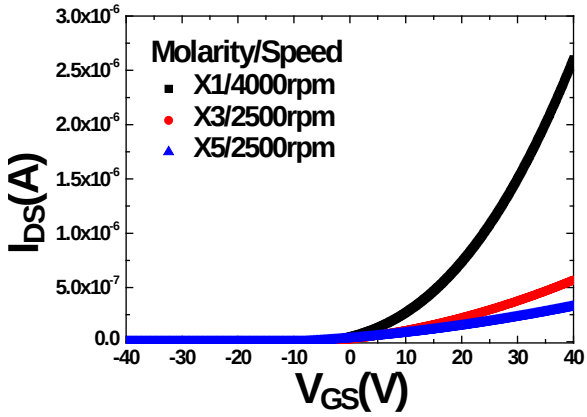



**(c)**

**Figure 4.2 Output characteristics for solution-processed a-IGZO TFTs of multi-stacked (a) once, (b) 5 times and (c) 10 times**




**(a)**

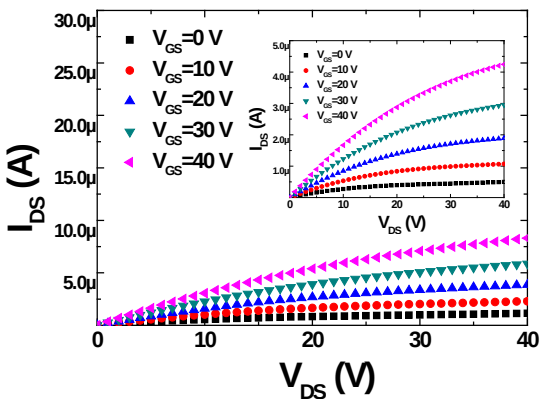



**(b)**

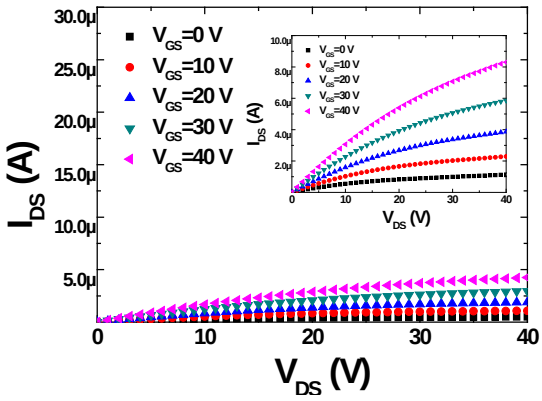
**Figure 4.3 Device performance of solution-processed a-IGZO TFTs with different active layer thickness (a) Transfer characteristics and (b) $I_{DS}$ vs. $V_{GS}$ at $V_{DS}$=1V with different molarity of solution and speed of spin coating**

In the case of changing solution molarity and spinning velocity of spin-coating, transfer curves are indicated in Figure 4.3. As a result of AFM measurement, the reference, 3 times higher molarity (0.411 M) with 2500 rpm and 5 time higher

molarity (0.685 M) with 2500 rpm coated samples were 10, 35 and 65 nm, respectively. As it can be seen in the Figure 4.3, the same dependence of change of performance as thicker $t_{act}$ was observed with that of multi-coating experiment, which means negatively shift of $V_{on}$ and degradation of on/off ratio, μ, and S.S. values. To be more specific, $V_{on}$, on/off ratio, μ, and S.S. are shifted from -5.19, 1.7E6, 1.05 and 0.36 to -8.53, 4.1E4, 0.089, and 1.16, respectively.




**(a)**




**(b)**

**Figure 4.4 Output characteristics for solution-processed a-IGZO TFTs coated in (a) 0.411 M solution at 2500 rpm and (b) 0.685 M solution at 2500 rpm**

Figure 4.4, and it had a nice pinch-off and hard saturation, which is appropriate for practical applications of the transistors without critical effects of parasitic contact resistance. These results mean as $t_{act}$ increases by either deposition method, $V_{on}$ shows negative shift and the other properties are degraded. Table 4.1 summarizes the device performances of a-IGZO TFTs with changing $t_{act}$ by two methods. A general shape of change of these parameters is shown in Figure 4.5.

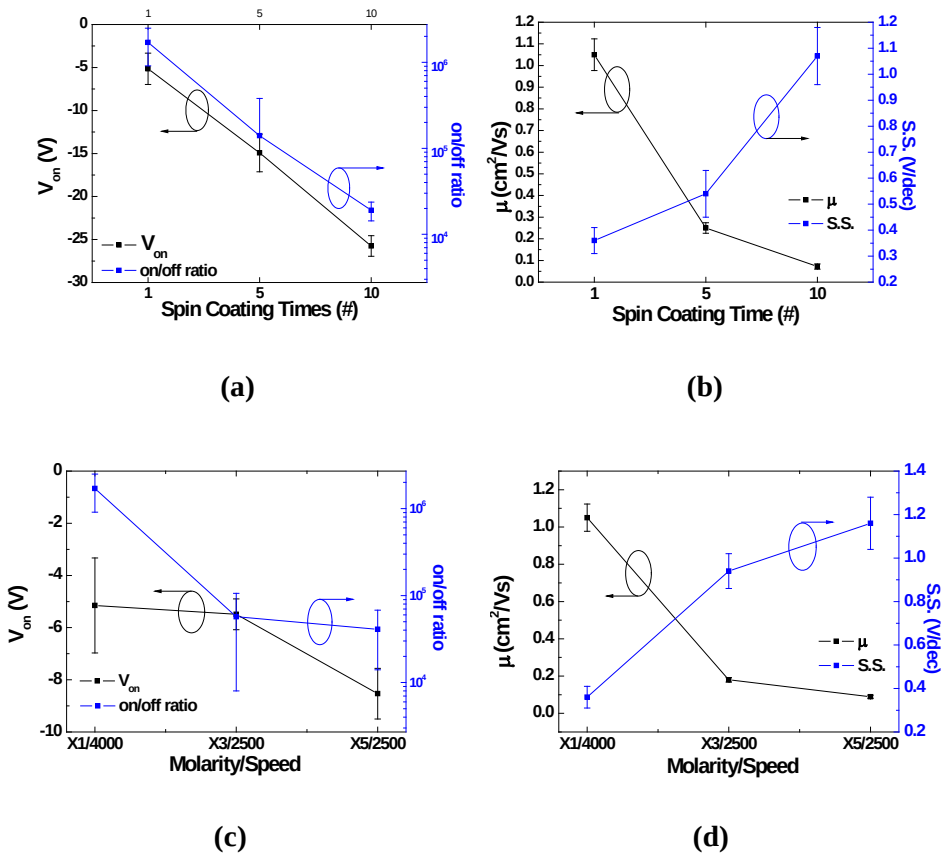



**Figure 4.5 The change of electrical parameters of the solution-processed a-IGZO TFTs characteristics for different active layer thickness fabricated by (a), (b) multi-coating and (c) and (d) molarity/speed**

**Table 4.1 Comparison of electrical characteristics with different active layer thickness fabricated by two methods for solution-processed a-IGZO thin films**

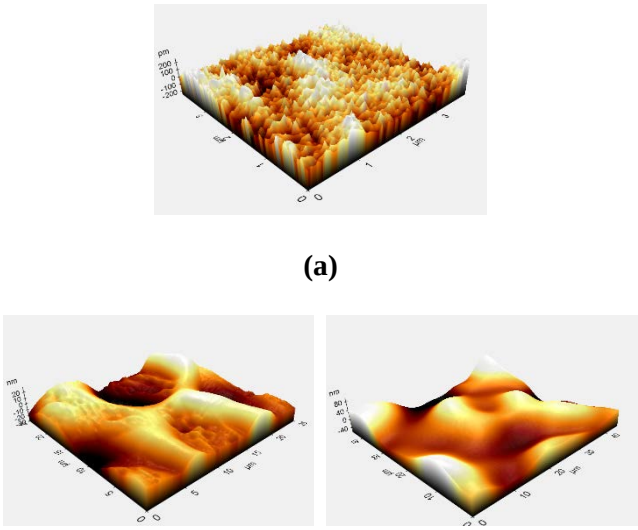
| | $V_{on}$ (V) | on/off ratio | μ ($cm^2$/Vs) | S.S. |
|---|---|---|---|---|
| **10 times** | -25.75 | 1.9E4 | 0.072 | 1.07 |
| **5 times** | -14.93 | 1.4E5 | 0.25 | 0.54 |
| **Reference** | -5.19 | 1.7E6 | 1.05 | 0.36 |
| **X3/2500 rpm** | -5.49 | 5.7E4 | 0.18 | 0.94 |
| **X5/2500 rpm** | -8.53 | 4.1E4 | 0.089 | 1.16 |

## 4.2 Analysis on Film Properties of a-IGZO TFTs with different active layer thickness

As it is indicated in Chapter 4.1, the change of performance with different $t_{act}$ can be confirmed. The origins of this phenomenon will be dealt with in this chapter. First of all, the negative shift of $V_{on}$ is contributed to the increased total number of free carriers in the channel region originated from the increased area of active layer. Therefore, to turn off the drain current, the higher absolute value of gate voltage is required for the device in the thicker film [19]. This can also explain the increased $I_{off}$ value as $t_{act}$ increases in Figure 4.1 and Figure 4.3. The increased free carriers lead to the high flow of electrons to pass through source and drain, resulting in increasing $I_{off}$ [20].

However, the thicker film has many defects and traps capturing electrons and the film density of the thick one is quite low because of the formation of middle interfaces in the case of multi-coating and many pores in the case of molarity/speed. Furthermore, the resistance between the channel and S/D electrodes also increases

due to the longer active channel layer region for electrons to flow and the more traps disturbing electron transport. Therefore, these phenomena contribute to the decreased $I_{on}$ with thicker film. According to AFM results, the root mean square (RMS) roughness of the a-IGZO films is 0.409, 11.648 and 22.562 nm for the number of 1, 5 and 10 times coating samples, respectively. This result is indicated in Figure 4.6.



**(a)**

**(b)** **(c)**

**Figure 4.6 AFM images of the a-IGZO thin films of (a) reference, (b) 5 times coating and (c) 10 times coating**

Because the RMS roughness monotonically increases with thicker $t_{act}$, it can be said that the influence of surface roughness on the carrier mobility is stronger at the increased film thickness. Thus, lower μ is observed with staking many layers and increasing solution molarity with decreased spinning velocity of coating as it can be seen in Table 4.1. The repeated deposition of layers in the case of the first

method using solution-process and the high molarity of solution in the case of second experimental one cause the increase of pores in the film, respectively. Carrier scattering resulting from the increased defects and film porosity with thicker layers can be also attributed to the decrease of μ [7]. The higher resistivity of thick film caused by the increased length for electrons to pass can be also one of the factors which make μ decreased. In the vacuum process, the $I_{on}$ and μ of oxide TFTs were independent on $t_{act}$ and this can be confirmed in Figure 4.7 [19]. However, it can be shown that the $I_{on}$ and μ of solution-based a-IGZO TFTs decrease with increased $t_{act}$ even though $V_{on}$ decreases. This different result is originated from the unique features of solution-process mechanism in comparison with those of vacuum-processed one, such as stacking layers, repetitive coating of the solution, and lowering speed of spin-coating as it is mentioned before. It means the solution-processed a-IGZO TFTs have a controllability of electrical properties by changing $t_{act}$.

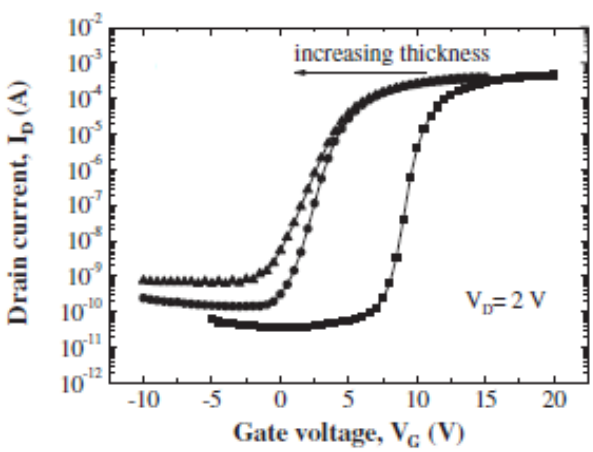



**Figure 4.7 Transfer characteristics of the vacuum-processed oxide (IZO) TFTs by rf (13.56 MHz) magneton sputtering as increasing $t_{act}$ from 15 to 60 nm**

With increasing $t_{act}$, the S.S. values of a-IGZO TFTs are getting high (i.e. the degradation of S.S.) as shown in Figure 4.4. From the S.S., the maximum density of surface sates, or the sheet trap density ($N_T$) can be inferred using the following equation (4.1).

$$N_T = \left\{S.S.\,(\log_{10} e)/(\frac{kT}{q}) - 1\right\} C_{ox}/q \tag{4.1}$$

where k is the Boltzmann's constant. T is the temperature and $C_{ox}$ is the unit gate capacitance. The degradation of S.S. with thicker film can be explained by the increased $N_T$. From the equation, it is shown that the S.S. of the a-IGZO TFTs is proportional to the $N_T$, which means as $t_{act}$ increases, the interfacial trap sites between gate dielectric and channel layer increase and it leads to high S.S. value. Additionally, the roughness is generally related to $N_T$; as the surface roughness value increases, defect levels trap more charges, and then the increased $N_T$ can be seen, which results in the deterioration of S.S. value, that is to say, the higher S.S. with thicker layer.

## 4.3 Comparison of a-IGZO TFTs with different active layer thickness fabricated by different methods

As it can be seen in Figure 4.1 and 4.3, two experimental methods exhibited same dependence of performance change with $t_{act}$, however, the extent of change of performance is quite different. Figure 4.9 exhibited plotted graphs of fabricated TFTs by two methods with thickness versus electrical performances, which are $V_{on}$, μ and on/off ratio, respectively. The mobility and on/off ratio values were plotted by log scale. For all performances, the results of molarity/speed method had more degraded ones at same thickness. Extracted slope of multi-coating results is -0.183, -0.021 and -0.011 and that of molarity/speed results is -0.329, -0.027 and -0.015 in the case of $V_{on}$, μ and on/off ratio, respectively. The absolute values of slope of molarity/speed are larger than those of multi-coating in all properties, which means steeper reduction of values, i.e. harder degradation.

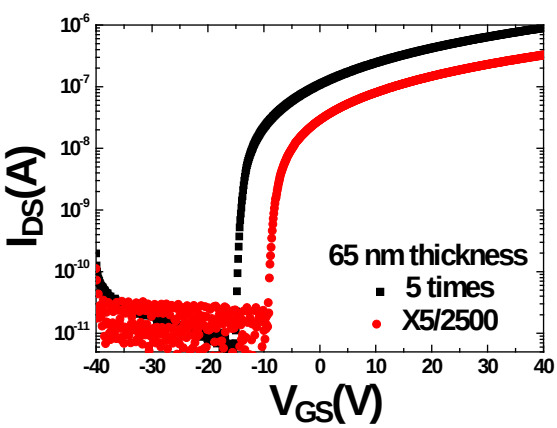
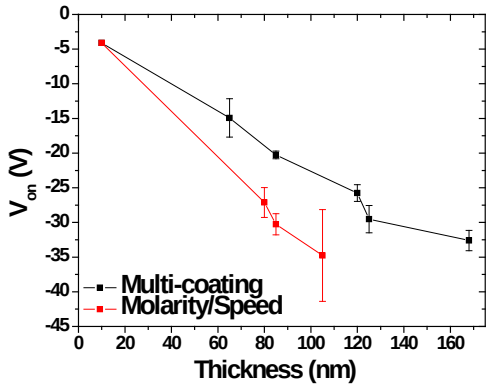
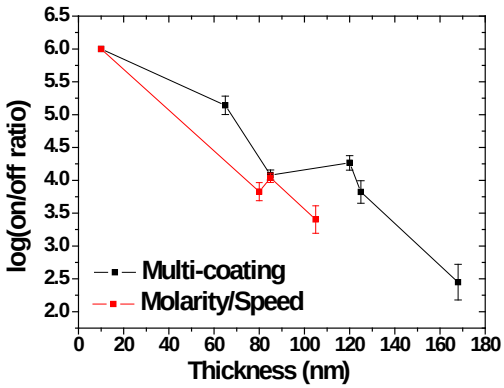



**Figure 4.8 Transfer characteristics of a-IGZO TFTs of same thickness fabricated by different methods each other**




**(a)**

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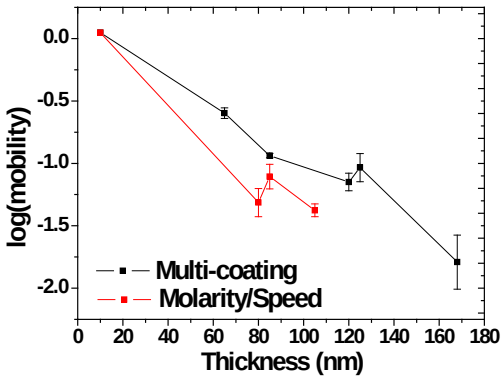



**(c)**

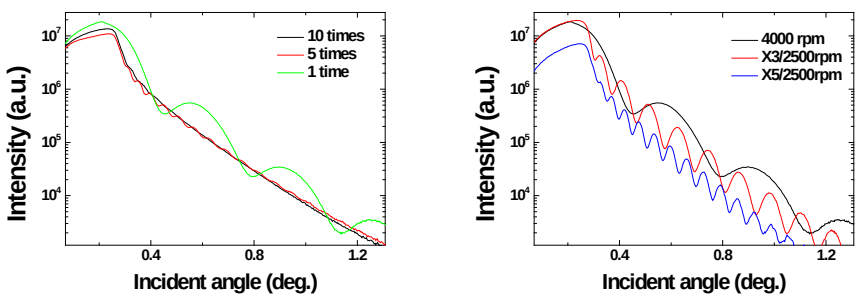
**Figure 4.9 Plotted results of fabricated TFTs by multi-coating and molarity/speed with thickness versus (a) $V_{on}$, (b) on/off ratio and (c) mobility**

For example, TFTs in Figure 4.8 are 5 times coated one (black) and used 5 times higher molarity solution with 2500 rpm (red) results, respectively. Both two TFTs are about 65 nm, however, their performance is not obviously same, to be more specific, the red one showed degraded result compared to that of the black one. This difference of properties between two results can be explained by film properties and contact resistance ($R_C$) and it will be considered in Chapter 4.3.1 in detail.

### 4.3.1 X-ray Reflectivity Results

Because it was turned out that the change of film properties with different $t_{act}$ had a significant influence on change of performance from previous investigation in Chapter 4.2, thus further analysis on film properties, such as density and roughness, of these two TFTs is worthwhile. In other words, it is inevitable to investigate fundamental interface and surface properties to look into the device performance closely. Therefore, XRR measurement was used as shown in Figure 4.10 and 4.11. First of all, Figure 4.10 shows XRR results of each coating methods, which are multi-coating and molarity/speed. Each result has same dependence of density and roughness with increased thickness, especially decreased density and increased roughness as thickness increases, which can be confirmed by smaller critical angle of first falling ripple and steeper slope of oscillations. However, in the case of multi-coating, the ripple of 10 times coating is very small and smooth since the thickness of film was too thick to be analyzed exactly by XRR, thus only the fact that the film of 10 times coating is thicker than that of 5 times coating could be verified by this result, instead of exact extracted value. Also, the critical angle of 5

times coating is similar with that of 10 times coating. However, because the amplitude of oscillation has also influence on the density, thus the fitted density result of 5 times coating considered all factors is larger than that of 10 times coating. The values of density of reference (i.e. 1 time and 4000 rpm in Figure 4.10 (a) and (b)), 5 times, 10 times, 3 times higher molarity solution with 2500 rpm and 5 times higher molarity solution with 2500 rpm are 5.493, 5.060, 4.961, 4.860 and 4.718, respectively, where the thickness is 8, 65, N/A, 35 and 65 nm, respectively. (As it was mentioned above, the exact value of thickness of 10 times coating could not be extracted)




**(a)** **(b)**

**Figure 4.10 XRR results of a-IGZO TFTs fabricated by different methods, which are (a) multi-coating and (b) molarity/speed**

Figure 4.11 exhibits XRR results of two TFTs of same thickness (65 nm) fabricated by different coating method. Compared with the reference (once coating with 4000 rpm), both samples have short distance of fringes, lower amplitude of oscillation and smaller critical angle, and the faster decay rate, which means thicker thickness, lower density and larger roughness [14]. However, if it is focused on

each result, graph of the molarity/speed experimental method showed lower density and harder roughness, which can be clarified by smaller critical angle and faster decay of reflected X-ray. In this result, the amplitude of oscillation of multi-coating is smaller than that of molarity/speed, however, the ripple also has an influence on not only density and but also roughness, thus when considered all factors, it can be said the density of multi-coating is larger than that of molarity/speed. This was also verified by XRR fitting simulation, which showed the density values of multi-coating and molarity/speed were 5.060 and 4.718 g/cm$^3$, respectively as it was mentioned above. Therefore, it can be concluded that lower film density and larger surface roughness significantly contributed to the harder performance degradation in the case of molarity/speed method, that is to say, lower μ, on/off ratio and S.S. characteristics.

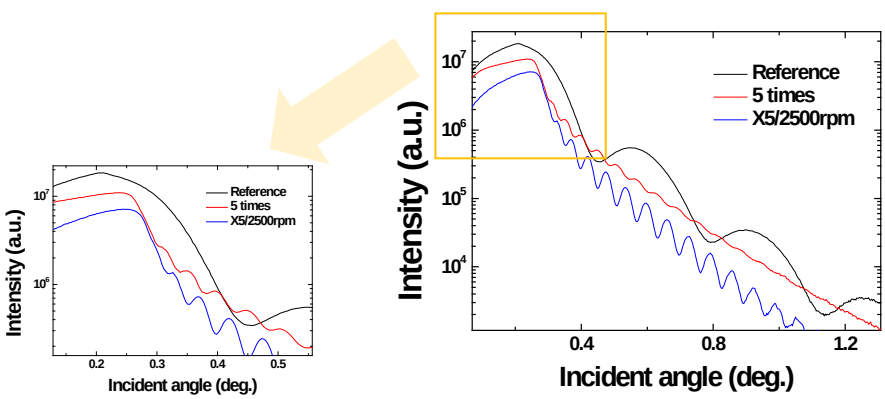
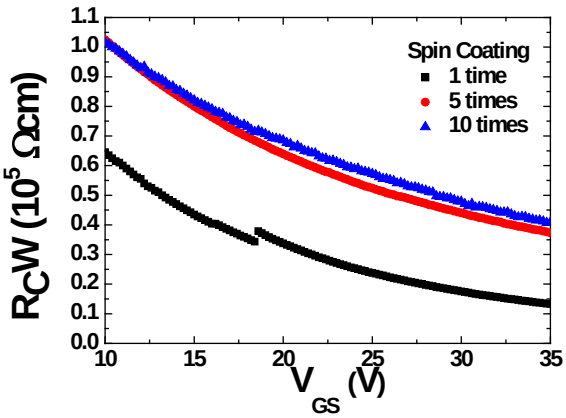


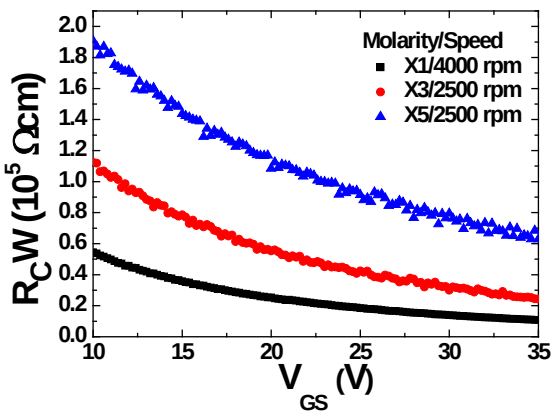

**Figure 4.11 XRR results of a-IGZO TFTs of same thickness fabricated by different methods each other**

### 4.3.2 Extraction of Contact Resistance

One of reasons to show the difference of change of performance between multi-coating and molarity/speed can be the effect of contact resistance ($R_C$) because $R_C$ strongly affects the device performance and there are many data also reported for oxide TFTs [21]. In this thesis, $R_C$ values were extracted by TLM, the channel width of TLM patterns was 1000 μm and the channel length was varied from 150 to 300 μm, while the gate voltage was modulated from 10 to 35 V. The width normalized resistance ($R_TW$) of the channel length is given by the sum of the channel resistance ($R_{ch}$) and $R_C$, depending on the gate voltage. The normalized contact resistance, $R_CW$ was calculated from the intersection of $R_TW$ for each gate voltage [16]. In the Chapter 4.1, it was proved that the $R_C$ did not have strong effect to performance of TFTs in the case of thicker film which were fabricated in above experiments owing to not much larger values compared to that of reference one. However, as shown in Figure 4.12, as $t_{act}$ increases in both methods, the $R_CW$ obviously increases as well because of longer channel layer region for electrons to flow and more traps disturbing electron transport. Therefore, this increased $R_CW$ would be attributed to the degradation of performance with thicker $t_{act.}$ In other words, the value of $R_CW$ is not large enough to affect change of performance itself, but obvious that it affects performance change as $t_{act}$ changes in both methods.




**(a)**




**(b)**

**Figure 4.12 Contact resistance of a-IGZO TFTs fabricated by (a) multi-coating and (b) molarity/speed method**

In Figure 4.12, the $R_CW$ of two methods exhibited same dependence with $t_{act}$, to be more in detail, the increase of $R_C$ with thicker layer, however, it is worthwhile to notice the exact value importantly. The $R_CW$ of molarity/speed is twice larger than that of multi-coating, which means this higher value of $R_CW$ impact directly on electron flow and the electrical properties of TFTs as well and it must have had an

influence on more severe degradation of performance in the case of molarity/speed method [22]. To sum up, extracted values of $R_C$ seem not to be critical to affect change of performance itself, however, the larger value of $R_C$ made TFTs fabricated by molarity/speed degraded more compared to multi-coating. In conclusion, the contact resistance has a contribution to degradation of performance in a-IGZO TFTs.

# Chapter 5

# Conclusion

In this thesis, the effect of active layer thickness ($t_{act}$) of solution-processed a-IGZO TFTs was investigated. The $t_{act}$ was controlled by multi-coating channel layers and increasing molarity of solution with decreased spinning velocity of spin-coating. It was shown changing $t_{act}$ could control the electrical performances of a-IGZO TFTs. The results could be also compared with those of vacuum-based oxide TFTs. Different from the results of vacuum-based one, which showed non-dependence of mobility and on/off ratio with $t_{act}$, the solution-processed a-IGZO TFTs with different $t_{act}$ showed consistent dependence of performance change with changed film thickness. The turn-on voltage and threshold voltage shifted negatively due to the increased free carriers with the increase of film thickness. As $t_{act}$ increase, the mobility, on/off ratio and subthreshold slope were degraded, which caused by the surface roughness and defect scattering in thicker film. The same dependence of performance with $t_{act}$ was exhibited in both fabrication methods, which are multi-coating and molarity/speed, thus it means either way can control electrical performance of solution-processed a-IGZO TFTs only with the change of $t_{act}$. However, the extent of change of performance for each case was found rather different. Generally, the result of molarity/speed showed more degraded one, such as lower mobility, on/off ratio and subthreshold slope compared to that of multi-coating and this was investigated by analysis of film property and contact resistance. By X-ray reflectivity (XRR) results, TFTs fabricated by molarity/speed had lower density and larger roughness even though it had same thickness with

TFTs fabricated by multi-coating. Thus, this lower density and harder roughness made performance deteriorated significantly, resulting in harder carrier scattering and so on in the case of molarity/speed. In addition, as a result of extraction of contact resistance by transfer length method, the contact resistance of molarity/speed method had twice larger than that of multi-coating at the same thickness of TFTs. In other words, the difference of contact resistance between two methods might affect the extent of performance degradation unequally.

By this investigation, the effect of $t_{act}$ of solution-processed a-IGZO TFTs could be clarified and examined in detail. The results showed the significant improvement in the possibility of optimizing parameters controlling electrical performances by changing $t_{act}$.

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# 국문 초록

# 용액 공정 기반 IGZO 박막트랜지스터의 반도체층 두께 변화에 따른 전기적 특성 차이에 대한 연구

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지난 수년간 디스플레이 기술의 바탕이 되었던 실리콘 (Si) 재료가 대면적이며 유연하고 투명한 차세대 디스플레이에의 이용에 전자 이동도와 대면적에서의 균등도 면에서 한계에 도달하면서 그 해결책으로써 비정질 인듐-갈륨-아연 산화물 반도체 기반의 박막 트랜지스터 (a-IGZO TFT)가 많은 주목을 받게 되었고 현재 그 연구와 개발이 활발히 이루어지고 있다. a-IGZO TFT는 투명 디스플레이에 적용이 가능한 넓은 광학적 밴드 갭을 갖고 있을 뿐 아니라, 비정질 상태임에도 불구하고 높은 전자 이동도와 대면적에서의 균등도로 고성능의 능동형 디스플레이 패널의 스위칭, 드라이빙 소자로도 사용될 수 있다는 장점이 있다. a-IGZO TFT는 진공 증착방식과 비진공 방식 기술로 만들어질 수 있는데, 기존의 진공 증착방식은 비싸고 복잡한 공정의 시스템을 이용하고 있어 최근에는 스핀코팅, 잉크젯 프린팅 등과 같은 비진공 방식 기술에 관한

연구가 활발히 이루어지고 있다. 이와 같은 방식을 용액공정이라고 부르며, 이는 가격이 저렴하고 공정이 단순하며 높은 수율을 낸다는 장점을 갖고 있다. 용액 공정 기반의 a-IGZO TFT에 대한 연구가 활발히 진행되고 있지만 그 성능을 조절하는 정확한 요소와 원인들에 대한 조사는 아직 미흡하다. 본 논문에서는 박막 트랜지스터의 반도체층을 그 중 하나의 요소로 보아, 용액 공정 기반의 a-IGZO TFT의 반도체층 두께 변화에 따른 성능 차이에 대한 연구를 수행하였다. 반도체층의 두께를 조절하기 위해 층을 반복하여 여러 번 쌓는 방식과 IGZO 용액의 농도를 높이고 스핀코팅 속도를 줄이는 방법을 사용했다. 그 결과 두 방법에서 모두 반도체층 두께 변화에 따라 전계효과 이동도, 문턱 전압, on/off 전류 비율, 문턱전압 이하에서의 기울기 등의 측면에서 같은 성능 변화 경향성이 발견되었다. 그러나 그 변화의 정도에서의 차이를 보였고 그 원인은 막의 밀도와 소스-드레인 전극과 반도체층 사이의 접촉 저항으로부터 기인한 것으로 분석되었다. 이 연구는 용액공정 기반 a-IGZO TFT의 반도체층 두께의 조절에 따라 그 성능의 결과를 예측하고 최적화할 수 있으며 각 원하는 응용처에 맞게 전기적 특성의 변화를 조절할 수 있다는 것을 시사한다.

Keywords: 박막 트랜지스터, 인듐-갈륨-아연 산화물 반도체, 용액 공정, 반도체층 두께, 박막 밀도, 접촉 저항
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