M.S. THESIS

Channel Stacked Array NAND Flash Memory With Vertically Stacked String Selection Line (SSL)

수직 적층된 ＳＳＬ을 갖는 스타구조 낸드 플래시 메모리 어레이 및 그 제조방법

BY

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DEPARTMENT OF ELECTRICAL ENGINEERING AND
COMPUTER SCIENCE
COLLEGE OF ENGINEERING
SEOUL NATIONAL UNIVERSITY

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지도교수 박 병 국

이 논문을 공학석사 학위논문으로 제출함

2012 년 8 월

서울대학교 대학원

전기컴퓨터공학부

서 주 연

서주연의 공학석사 학위논문을 인준함

2012 년 8 월

위 원 장 : 박 영 준 (인)

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ABSTRACT

Three-dimensional (3D) stacked memory devices are representative solutions that can lead to reduce bit cost of NAND flash memories. Recently, many groups have proposed various types of 3D stacked NAND flash memory devices. In this thesis, we propose a novel 3-D STacked Array (STAR) NAND flash memory featuring Gate-All-Around (GAA) structure with single crystalline Si channel.

In Chapter 1 and 2, we introduce a newly designed structure, compact STAR, and address the advantages of compact STAR over other types of 3D stacked NAND flash memories. By using TCAD simulation, we demonstrate that the proposed array structure can support fully compatible device operation with conventional NAND array.

In Chapter 3 and 4, we investigate the advantages of metal gates in a 3D stacked NAND flash memory compared with poly-Si gates in terms of the variation of dopant concentration. Also, we show the fact that NAND flash

memory cells featuring a GAA structure are less sensitive to the variation of the gate dimensions than cells featuring a DG structure.

In Chapter 5, we investigate the cell characteristics with respect to physical dimensions of channel and gate experimentally. Poly-Si channel with GAA structure flash memory cells are successfully fabricated.

Keywords: NAND flash memory, 3D memory, STacked-ARray (STAR), Si nanowire

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CONTENTS

1. INTRODUCTION

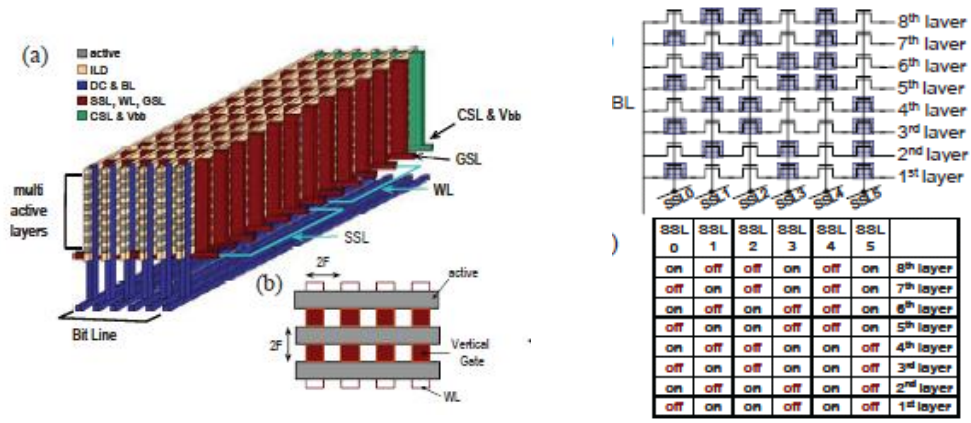
As the quest for higher storage capability continues, NAND flash memory has become the most attractive storage device. However, the limitation of photo-lithography technology hinders further scaling [1] of NAND flash memory. Consequently, many groups have proposed three-dimensional (3-D) stackable memory devices as one of the most promising solutions [2–7]. There are two types of stacking type in three-dimensional stackable memory devices; one is gate stacked type, and the other is channel stacked type. In case of gate stacked type memory devices, there are standardized structures [2], [3] adopted widely. However, many structures featuring stacked channels have been proposed, and all these structures have

pros and cons.

Fig.1.1 [4] is the proposed structure by Samsung Electronics in 2009. The layer selection is done by using the combination of String Selection Line (SSL) transistors, so it requires the smaller number of SSL transistors than the number of stacked layers. However, additional photo-lithography processes and ion implantation processes are required to fabricate string select line (SSL), which increases the fabrication cost as the number of the stacked layers is increased.

In [6], by using junctionless buried channels, the storage density can be increased. However, the size of pages is limited to the number of stacked layers, since bit-lines are tied in the same layer. This structure is an obstacle in expanding the capacity of memory. To overcome these issues, a newly

designed 3D stacked NAND flash memory structure is proposed. Compact Channel Stacked Array (Compact CSTAR) is designed for single crystalline channel that enables it to have higher mobility compared to poly crystalline channel. Also, Compact CSTAR features gate-all-around (GAA) structure with enhanced performance.



SSL 0	SSL 1	SSL 2	SSL 3	SSL 4	SSL 5	
on	off	off	on	off	on	8th layer
off	on	off	on	off	on	7th layer
on	off	on	off	off	on	6th layer
off	on	on	off	off	on	5th layer
on	off	off	on	on	off	4th layer
off	on	off	on	on	off	3rd layer
on	off	on	off	on	off	2nd layer
off	on	on	off	on	off	1st layer

Fig 1.1 (a) Structure of VG-NAND and SSL operation scheme [4]

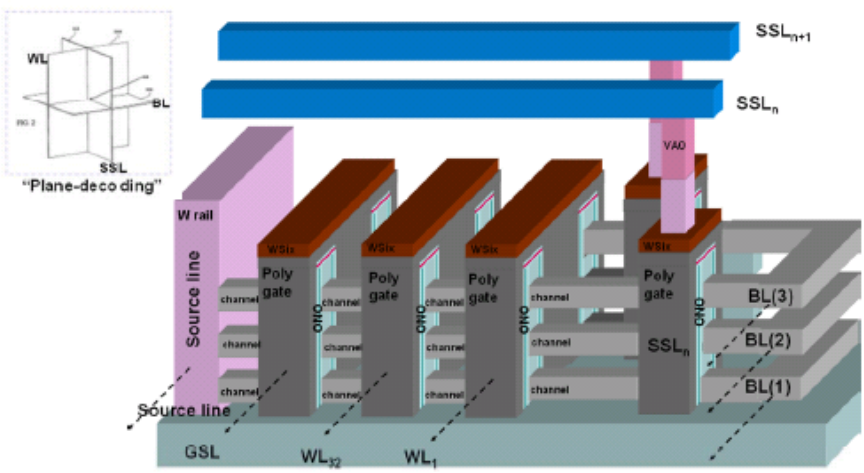


Fig. 1.2 Structure of 3D VG NAND [6]

2. Compact Channel STacked ARray (STAR)

2. 1 CONCEPT

Fig. 2.1 represents the bird's eye view of the designed structure and its equivalent circuit. The layer selection is carried out by turning on the SSL transistor corresponding to each layer. Once the layer is selected, the other operation method is the same as that of the conventional planar NAND flash memory array. The advantages of the designed structure are listed below:

i. There is no need of additional spaces notwithstanding the increase in the number of stacked layers, thus resulting in good expandability (Fig. 2.2).

ii. It can be operated with the conventional NAND array scheme,

which is a very critical issue for 3D stacked NAND memory to become commercialized.

iii. Since gates are formed in the last step of the process, metal can be utilized as gate material which assures stable program characteristics. The benefit we can obtain from metal gates will be covered in Chapter 3.

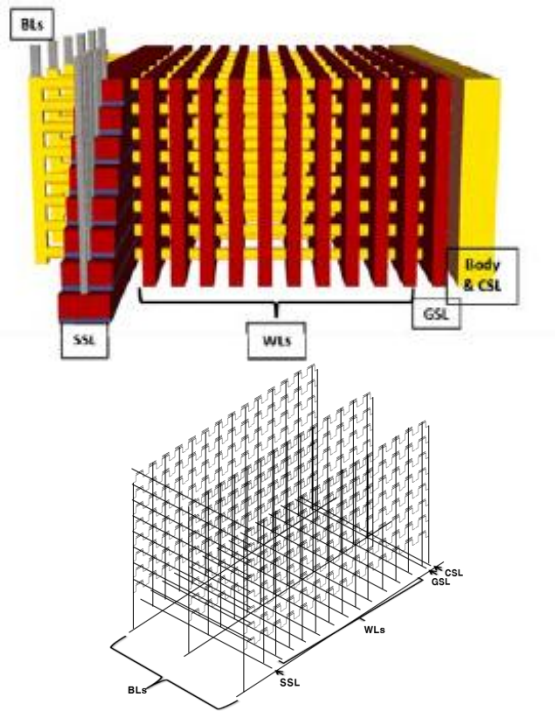


Fig. 2.1 Bird's eye view of the designed structure and its equivalent circuit

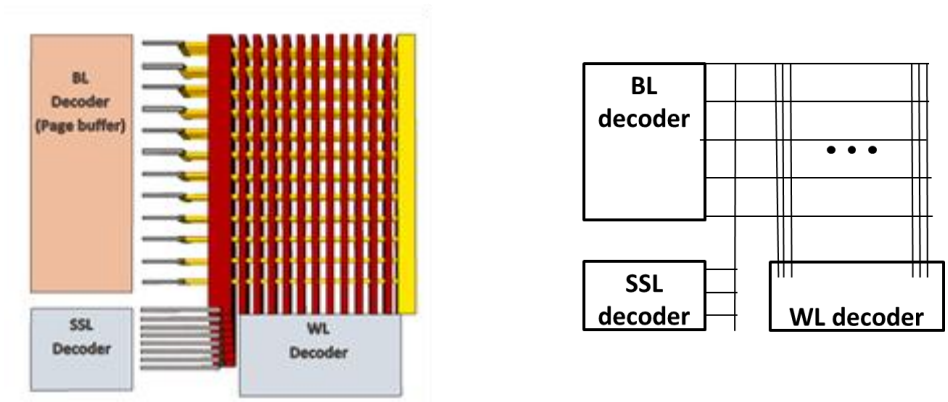


Fig. 2.2 Top view of the designed structure

2. 2 FABRICATION PROCESS

The fabrication process of compact STAR begins with bit-line patterning. (Fig. 2.3 (a)) For using single crystalline Si, SiGe layers are required for sacrificial layers. After patterning bit-lines, oxide is deposited. The region where SSL transistors are formed is opened, and then SiGe is removed by selective etch process [8] (Fig. 2.3 (b)). Depositing gate stack layers by chemical vapor deposition (CVD) process, poly-Si between layers are removed by isotropic etch process. While cells located in the same layer must share gates, cells in different layers must be separated. To realize the layer separation, the distance between gates in the same place must be smaller than the distance between different layers (Fig. 2.3 (c)).

After formation of SSL transistors to select layers, word-line patterning process (Fig. 2.3 (d)) is performed and followed by SiGe removal and oxide/nitride/oxide layer deposition (Fig. 2.3 (e)). At the end of the process, gates are deposited (Fig. 2.3 (f)). Since gate formation does not require gate etch process (self-alignment), metal gates can be implemented.

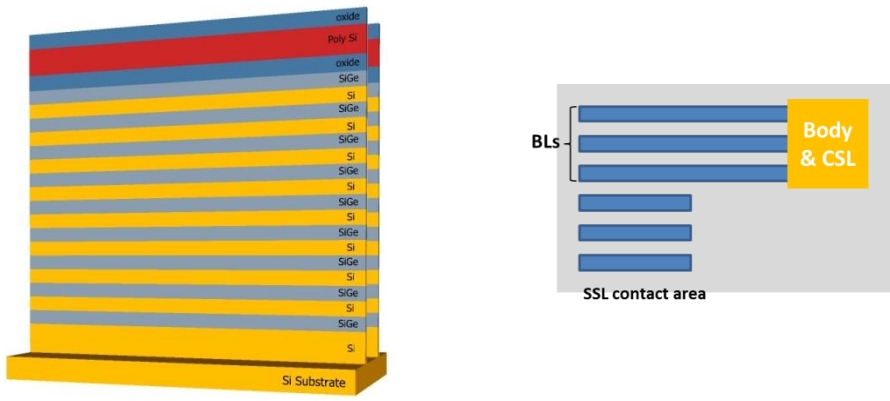


Fig. 2.3 (a) Bit-line patterning

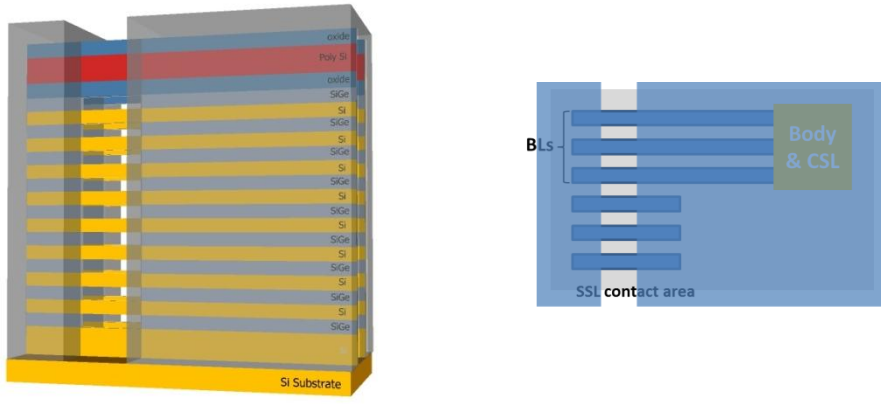


Fig. 2.3 (b) SiGe selective removal

Fig. 2.3 (c) SSL gate formation

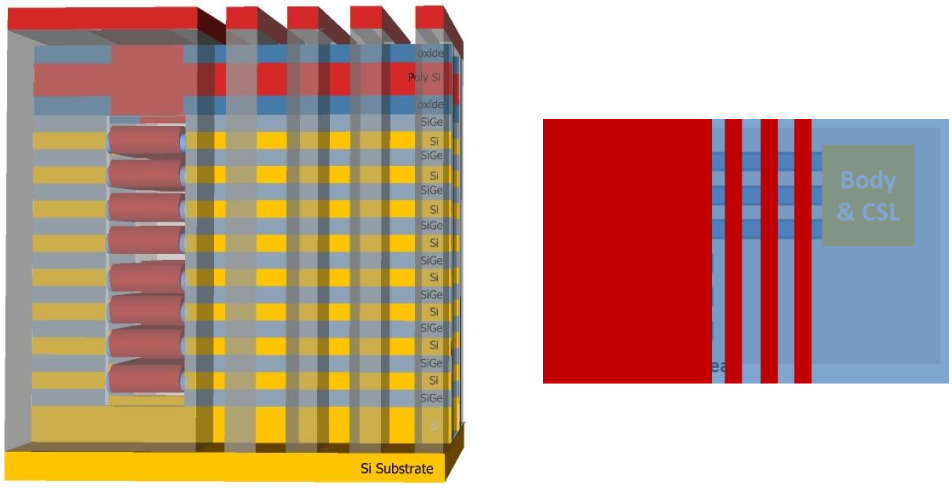


Fig. 2.3 (d) Word-line patterning

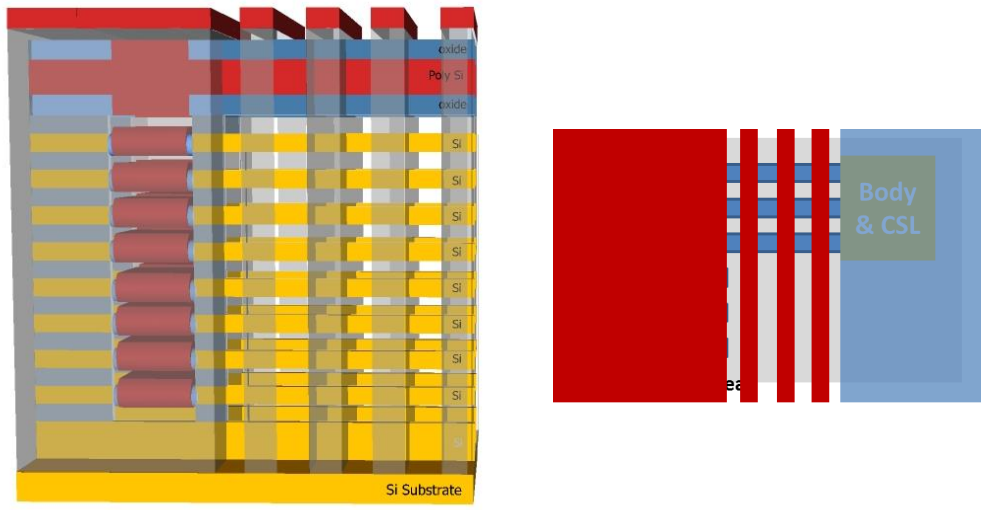


Fig. 2.3 (e) SiGe selective removal

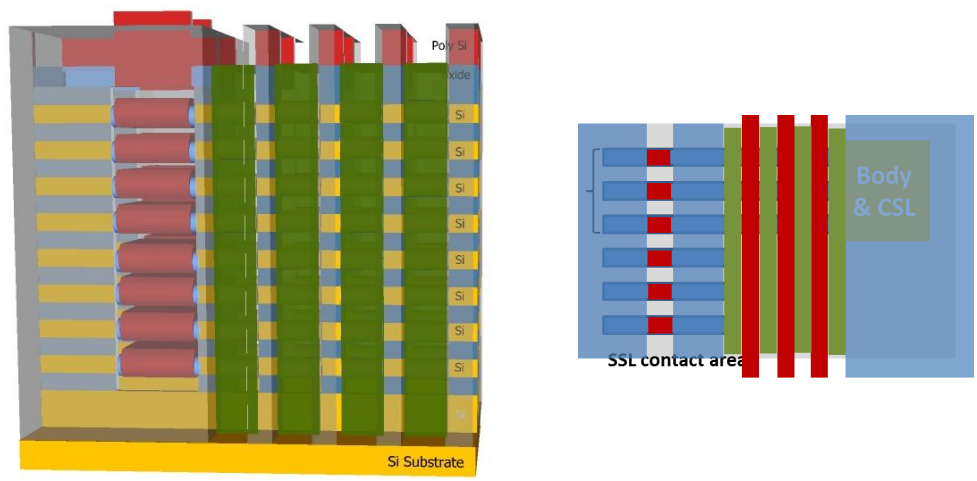


Fig. 2.3 (f) Word line gate formation

2. 3 SUMMARY

The newly designed 3D stacked array NAND flash architecture, compact STAR, is proposed. Separating SSL transistors corresponding to each layer makes the layer selection scheme easier. The benefit of compact STAR is its compatibility with the periphery circuits and area efficiency. Fabrication process of compact STAR is also designed, and the process can implement metal gates.

3. Poly depletion effect in 3D NAND flash array

3. 1 INTRODUCTION

As the demand for high scalability has increased, the distance between channels decreases. When channels get closer, difference of dopant concentration in poly-Si gates among certain parts may occur [9], which can affect the program characteristics among channels. This chapter reports how the difference of dopant concentration affects the program characteristics, and how the effects can be avoided by using a metal gate.

3.2 SIMULATION RESULTS

To investigate the program characteristics with respect to the doping concentration, TCAD simulation was performed by Sentaurus. Fig. 3.1 shows the simulated Gate-All-Around (GAA) structure. The radius of the channel is 10nm, and the thickness of tunnel oxide/nitride/blocking oxide layer is 3/6/6 nm, respectively. The distance between channels is 50nm. The simulation was carried out by varying the doping concentration of poly-Si gate, and the device with metal gate was also simulated.

When the dopant concentration of gate is below $10^{19}/cm^3$, the gate potential is not well applied to the blocking oxide layer (Fig. 3.2 and Fig. 3.3). The physical phenomenon responsible for the loss in gate potential is poly depletion effect [10]. The depletion region in poly-Si gate contributes to the

equivalent oxide thickness resulting in decreasing the gate capacitance. This means that the electric field is not strong enough to cause as many electrons to tunnel into the charge trap layer as required for efficient program operation (Fig. 3.4).

The difference of potential with respect to the dopant concentration of the gate affects the program characteristics, as shown in Fig. 3.5.

There is notable reduction of the program efficiency as the dopant concentration decreases. Since the structure featuring tungsten gate can maintain the potential constant, the uniform characteristics among channels will be guaranteed.

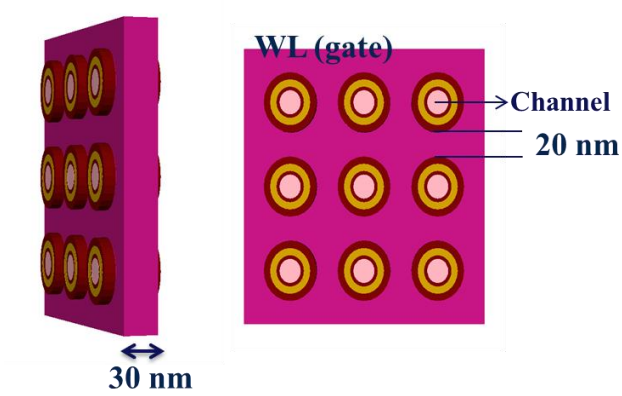


Fig. 3. 1 Simulated Gate- All-Around (GAA) structure

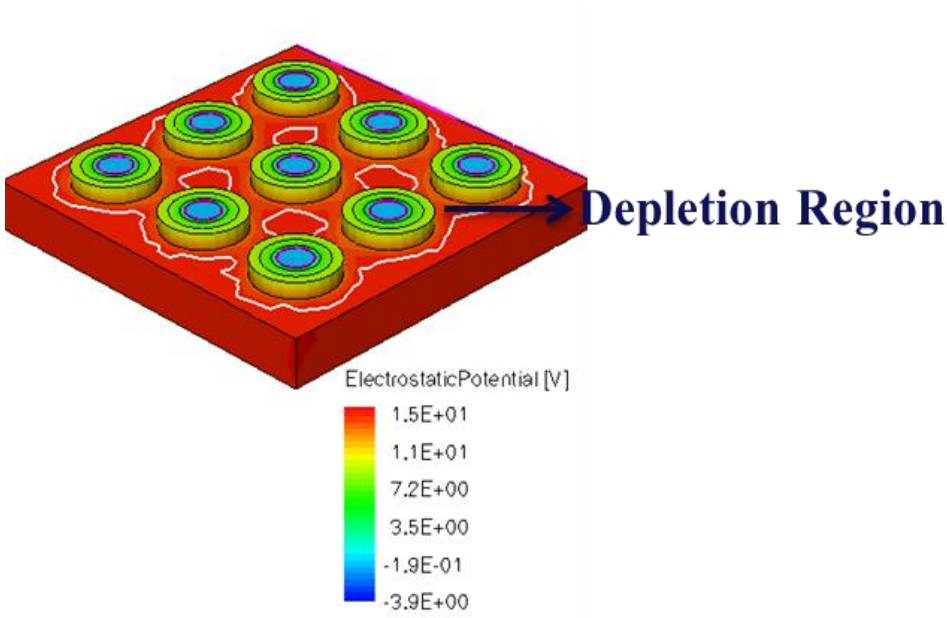


Fig. 3. 2 Potential contours when gate doping concentration is 10^{18} cm^{-3}

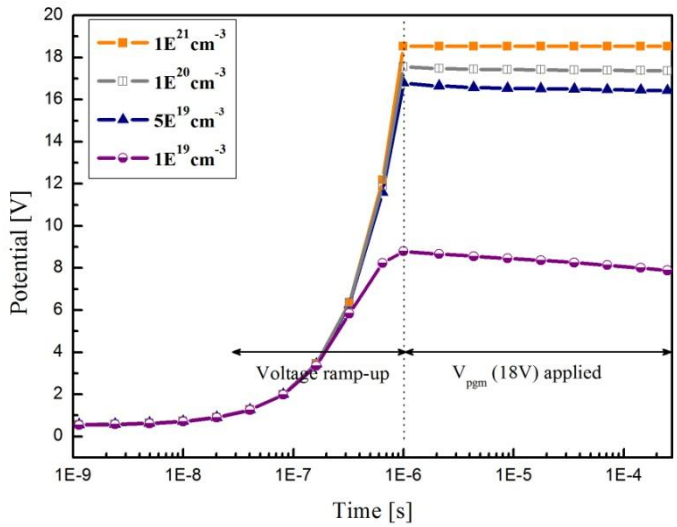


Fig 3.3 Potential at the interface between poly-Si gate and blocking oxide layer when the program voltage (18V) is applied to the gate.

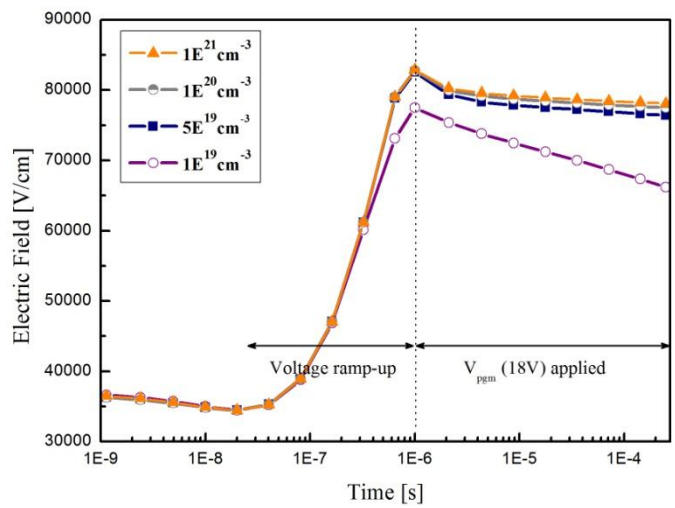


Fig. 3. 4 Electric field of channel when the program voltage (18V) is applied to the gate.

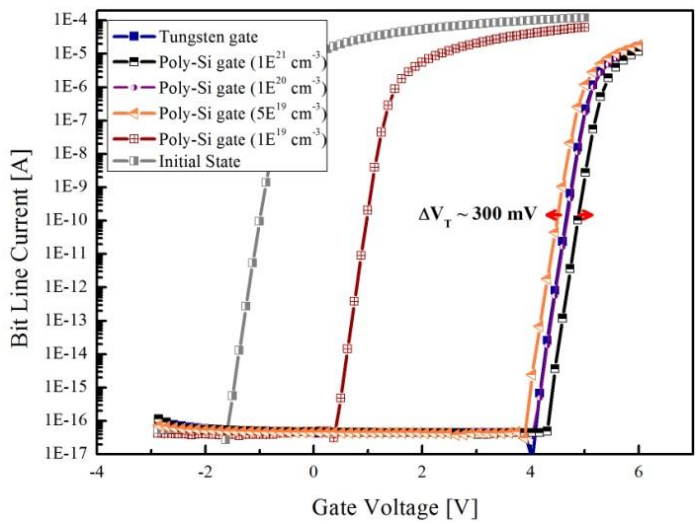


Fig. 3. 5 Program characteristics regarding to different gates.

3.3 SUMMARY

In this chapter, the effect of the doping concentration of poly-Si gates on the memory characteristics is studied by using TCAD simulation. The variation of dopant concentration in poly-Si gates reduces the efficiency of program operation. By adopting metal gates to the 3D NAND flash memory, consistent program characteristics can be guaranteed.

4. Effect of the Variation of Gate Dimensions on Program Characteristics in 3D NAND Flash Array

4. 1 INTRODUCTION

In 3D stacked NAND flash memory, the number of stacked layers tends to increase for high density storage capacity. In the highly stacked 3D array, a slight deviance from a right angle of the etch slope results in drastic change of the dimensions between the gates (Fig. 4.1). This chapter reports how the dimensions of the gates affect the program characteristics in 3D NAND flash array architectures. In this chapter, we investigate the effect of the variation of gate dimensions on the program characteristics in 3D NAND flash memory

array by using TCAD simulation. Also, we compare the cell characteristics of NAND flash with different structures, gate-all-around (GAA) and double gate (DG).

4. 2 SIMULATION RESULTS

We adopted the gate-all-around (GAA) structure and the double gate (DG) structure to perform the simulation. Three flash cells are connected in series, and the diameter of the nanowire and body thickness of the double gate structure is 20 nm. Flash cells have charge trap layers and the thickness of tunnel oxide/nitride/blocking oxide layer is 3/6/6 nm, respectively. Between the cell gates, virtual source and drain region is formed by the fringing field of the gates. With the same pitch size (100 nm), the gate length (L_g) is varied from 40 nm to 70 nm. Also, the length between adjacent channels in the same

layer is defined as L_{gap}, which is from 30 nm to 50 nm. As described in Fig. 2, the gates in the upper layer have shorter gate length, longer word line gap, and longer L_{gap}.

In the case of the GAA structure, the variation of L_g does not affect the program characteristics, when programming with 14 V for 100 μsec (Fig. 4.3 (a)). Whereas, DG structure shows cell characteristics that is relatively sensitive to the variation of gate length (Fig. 4.3 (b)). As gate length decreases from 70 nm to 40 nm, the amount of V_t shift reduces by 40%.

In addition, the program characteristic of the GAA structure is rarely changed by the variation of L_{gap} (Fig. 4.4(b)), which is the same for the DG structure (Fig. 4.4 (a)).

The field concentration effect of the DG structure is weaker so that the field from the gate to the channel is weaker than the GAA structure [11], [12]. Moreover, the fringing field is not sufficient enough to induce the inversion layer between gates as the distance between gates gets longer [13], which leads to the low electron density in the virtual source and drain region. These phenomena are proved by using TCAD simulation. Fig. 4.5 illustrates that the field induced by gate is weaker when double gates are adopted, and this causes low electron density. This means that DG NAND flash memory cells located in the upper layer do not guarantee stable program characteristics. In other words, DG structure in 3D NAND flash memory is unreliable due to its unstable cell characteristics with the variation of gate dimensions. Considering

overall effects, the GAA structure is suitable for highly stacked NAND flash array.

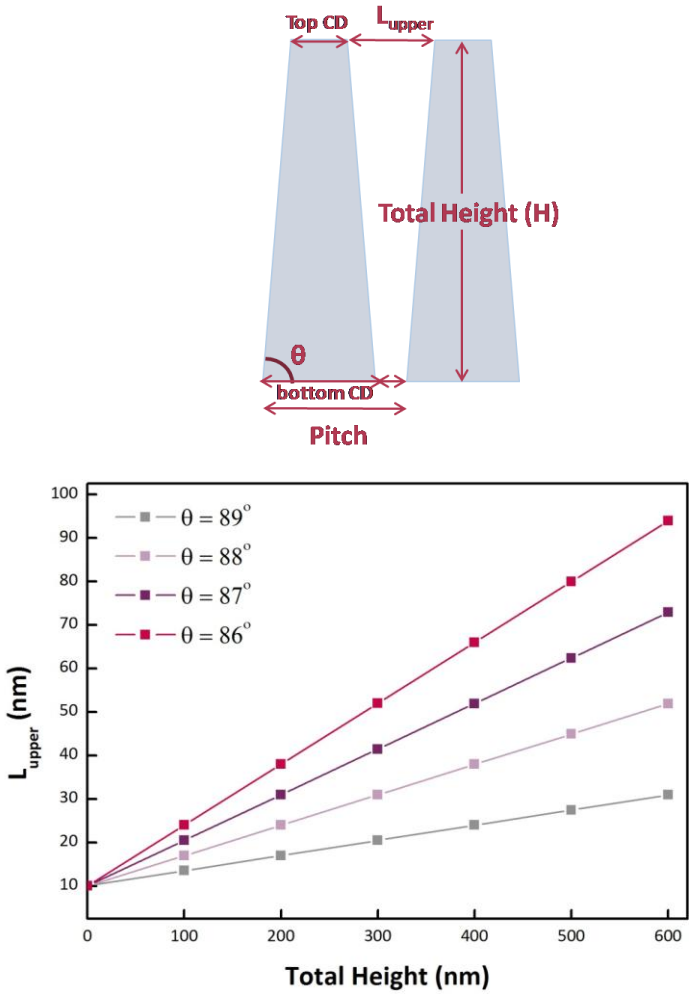
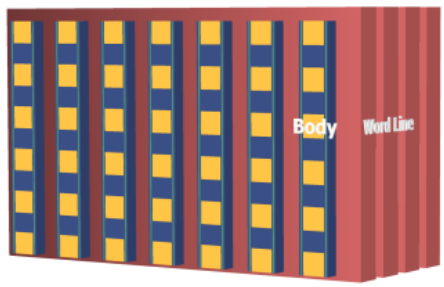
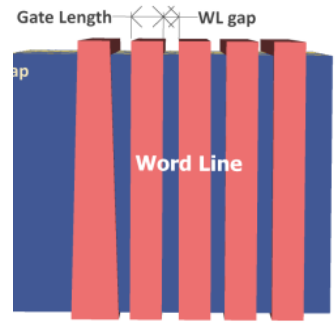


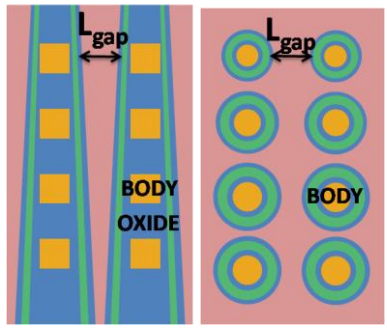
Fig. 4. 1 Definition of L_{upper} and its tendency as a function of total height and etch slope



(a)



(b)

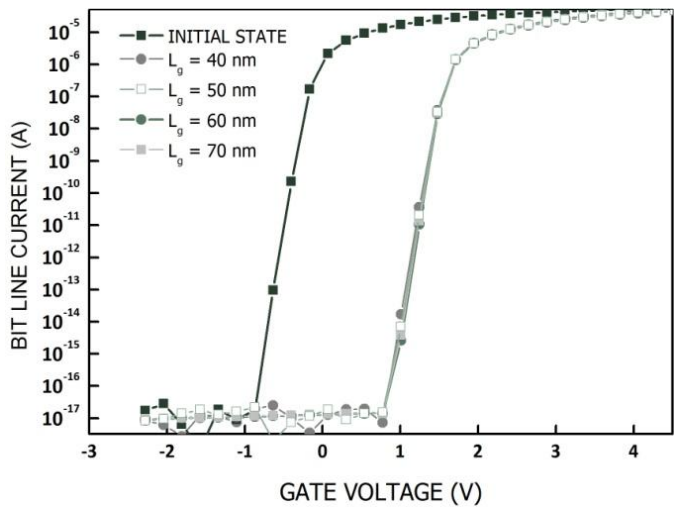


(c)

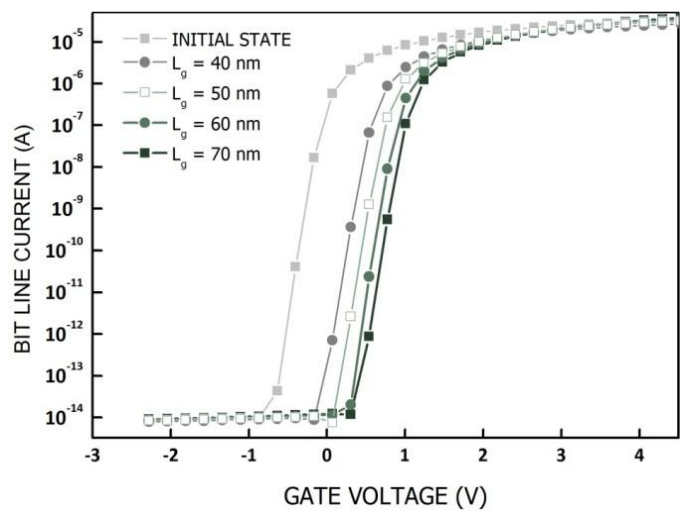
	Gate length (L_g)	WL gap	L_{gap}
Upper layer	↓	↑	↑
Lower layer	↑	↓	↓

(d)

Fig. 4. 2 (a) Double gate stacked NAND array (b) Gate length variation with etch slope (c) Definition of L_{gap} in double gate and GAA structure (d) Tendency of L_g, WL gap, and L_{gap} in different layers



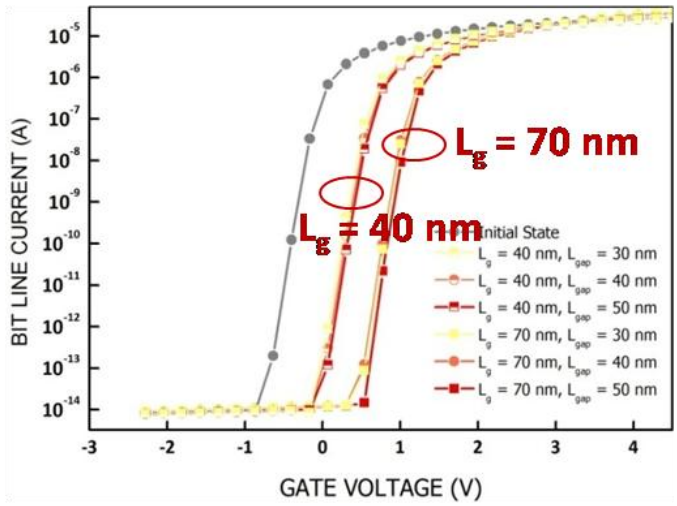
(a)



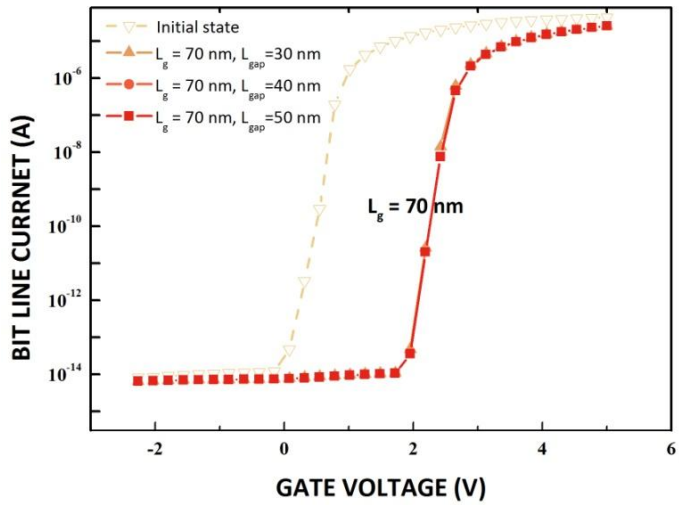
(b)

Fig. 4. 3 Program characteristics with different gate lengths (pitch size = 100 nm)

(a) gate-all-around (GAA) (b) double gate (DG)



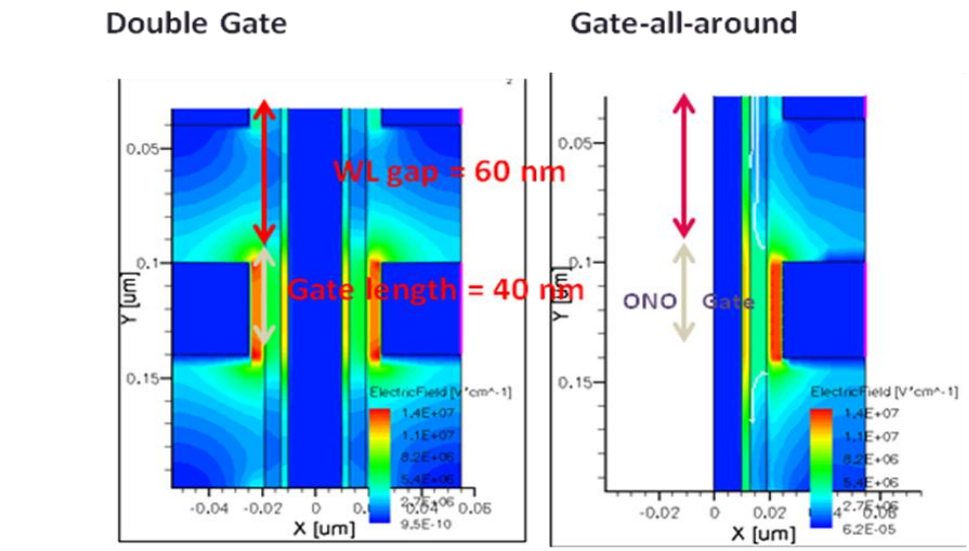
(a)



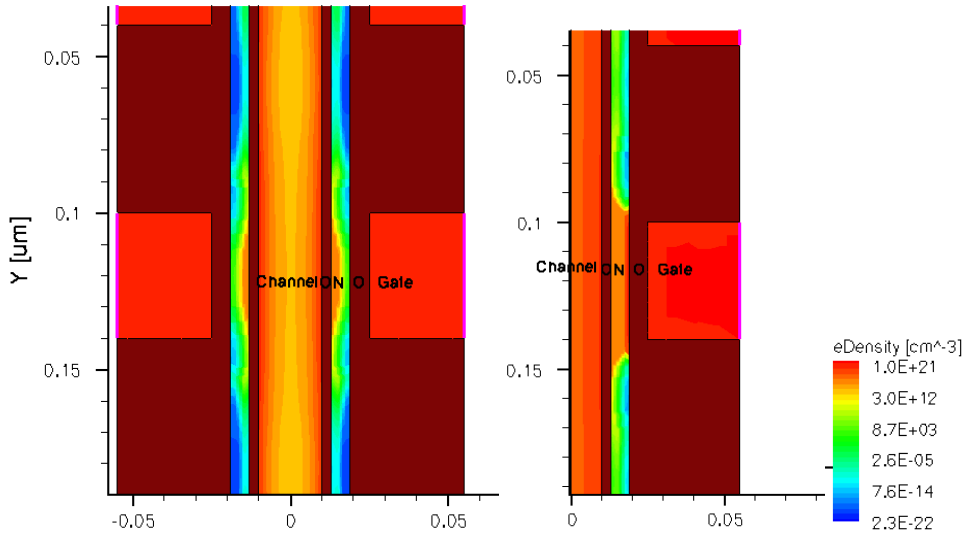
(b)

Fig. 4. 4 Program characteristics with different L_{gap} (pitch size = 100 nm)

(a) double gate (DG) (b) gate-all-around (GAA)



(a)



(b)

Fig. 4. 5 (a) Electric field contours and (b) electron density when programming

4. 3 SUMMARY

This chapter reports the effect of the gate dimension on a 3D NAND flash memory array by using TCAD simulation. NAND flash memory cells featuring a GAA structure are less sensitive to the variation of the gate dimensions than cells featuring a DG structure. Therefore, GAA structure is suitable to be adopted in 3D stacked NAND flash memory for ultra-high-density storage devices.

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5. Fabrication of Poly-Si Channel Stacked Array

5. 1 INTRODUCTION

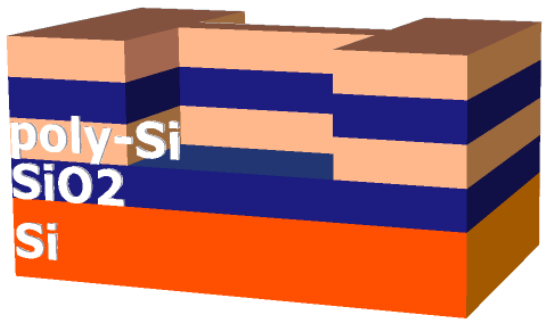
In this chapter, the gate-all-around (GAA) poly-Si channel NAND flash memories with charge trap layer (Si_3N_4) have been successfully fabricated. Also, the possibility of expanding the number of stacked channels is demonstrated by separating string selection line (SSL) transistors from the bulk. It can be adopted for 3D channel stacked NAND flash array structure whose layer selection is done by turning on the SSL corresponding to the each layer. Electric characteristics of fabricated devices including threshold voltage

shift with program/erase operation, retention characteristics have been investigated with various channel dimensions.

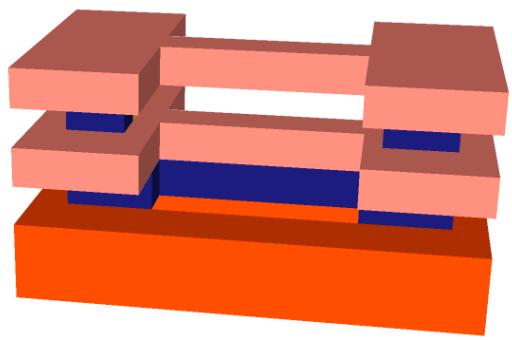
5.2 FABRICATION PROCESS

Flash memory cells were fabricated by initially depositing a 400-nm-thick tetra-ethyl-ortho-silicate (TEOS) oxide on 6-inch silicon wafer. A 40-nm-thick undoped amorphous-silicon (a-Si) layer was deposited by low-pressure chemical vapor deposition (LPCVD) at 550 ℃. Then, channels were defined with mix-and-match process consisting of e-beam and photolithography, followed by dry etch using HBr and O_2 gas plasma (HBr : 40 sccm, O_2 : 2sccm) (Fig. 5.1 (a)). To separate the Si channels from the bulk, the buried oxide was removed by wet etch with HF solution (Fig. 5.1 (b)). After SC1

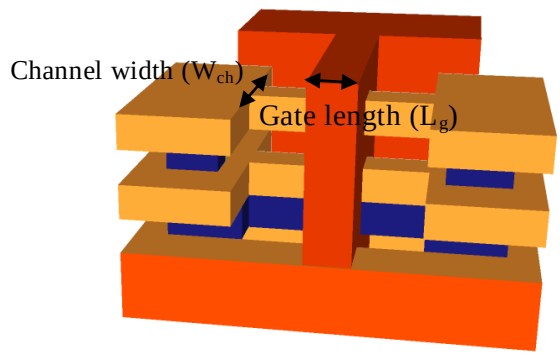
cleaning (NH_4OH : H_2O_2 : D.I. water = 1 : 8 : 64 solution at 65 ℃), medium temperature oxide (MTO) was formed as tunneling oxide layer, 3-nm-thick. A 6-nm-thick Si3N4 layer and a 8-nm-thick TEOS layer were sequentially deposited by LPCVD as a charge trap layer and blocking oxide, respectively. To form gate electrodes, in situ n^+ doped poly-Si layer was deposited and mix-and-match process and dry etch were performed (Fig. 5.1(c)). After source/drain ion implantation, back end process including contact hole etch, metal deposition, and metal line patterning was carried out.



(a)



(b)



(c)

Fig. 5.1 (a) Active patterning (b) Buried oxide removal (c) Gate patterning

(Gate length : L_g, Channel width : W_{ch})

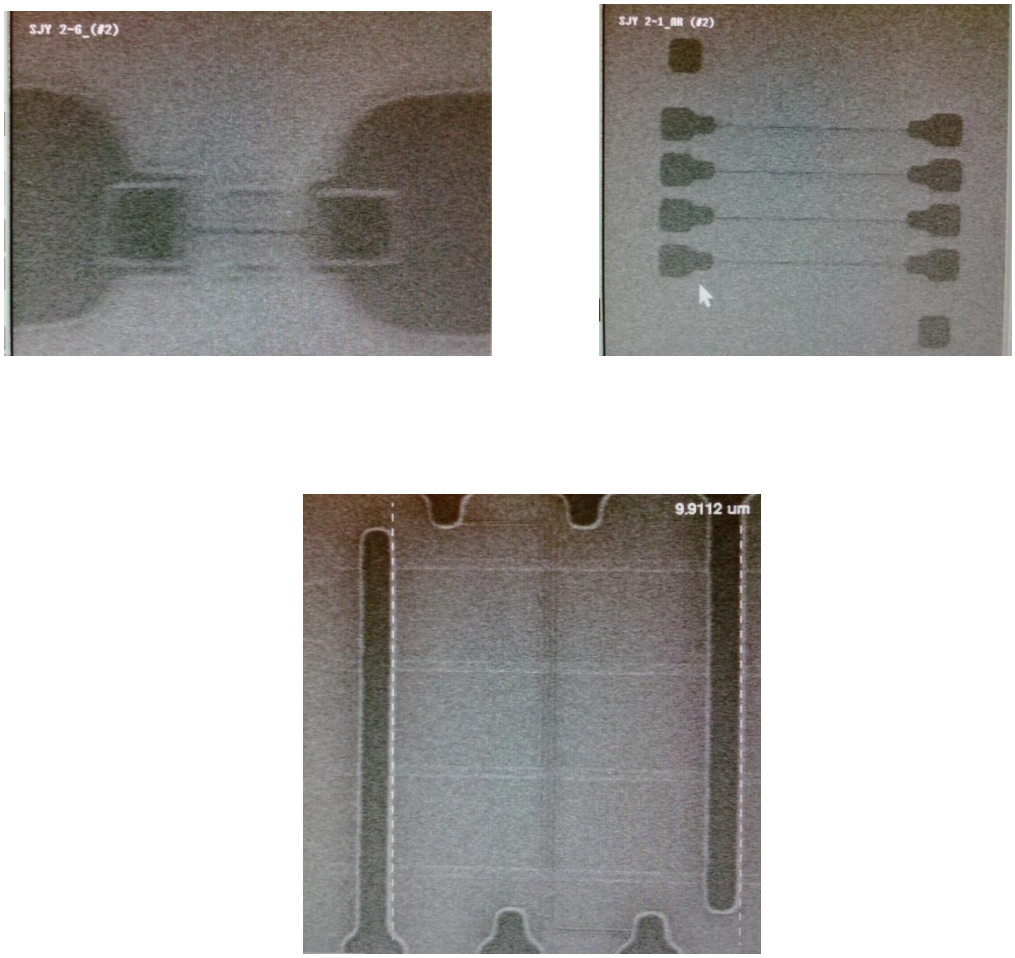
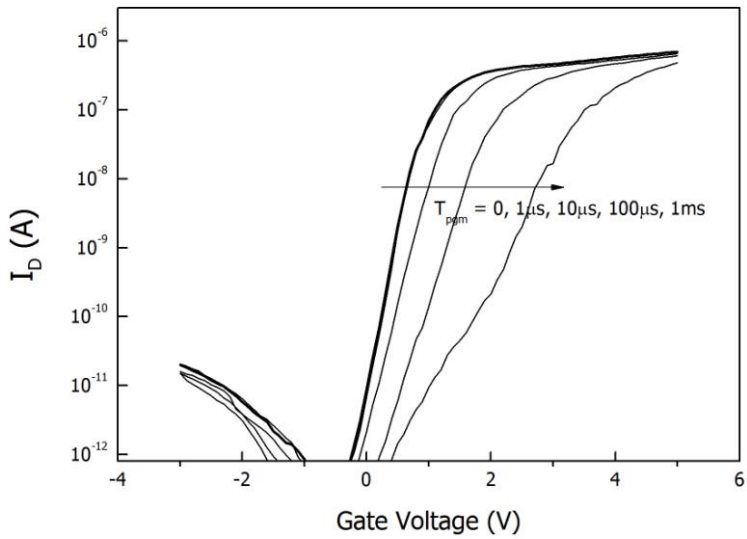


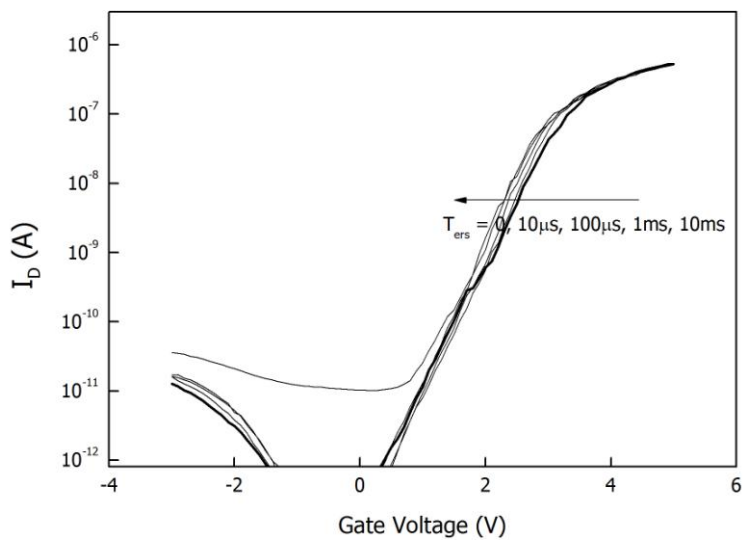
Fig. 5. 2 SEM images of fabricated devices

5.3 MEASUREMENT RESULTS

Fig. 5.3 shows electrical results from the fabricated devices (W_{ch} = 50 nm, L_g = 100 nm). 1.9V of ΔV_T from program operation can be achieved , but erase operation does not work well. Increasing negative bias applied on the gate results in V_T shift to the positive direction. This comes from the back tunneling through the blocking oxide. LPCVD TEOS used as blocking oxide shows more conductivity to F-N tunneling [14] compared to thermally grown oxides. Therefore, the back tunneling issue can be alleviated by using thermally grown oxide as a blocking oxide.



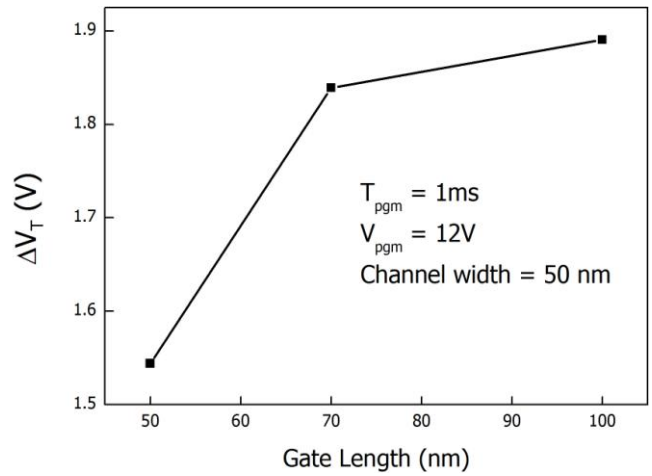
(a)



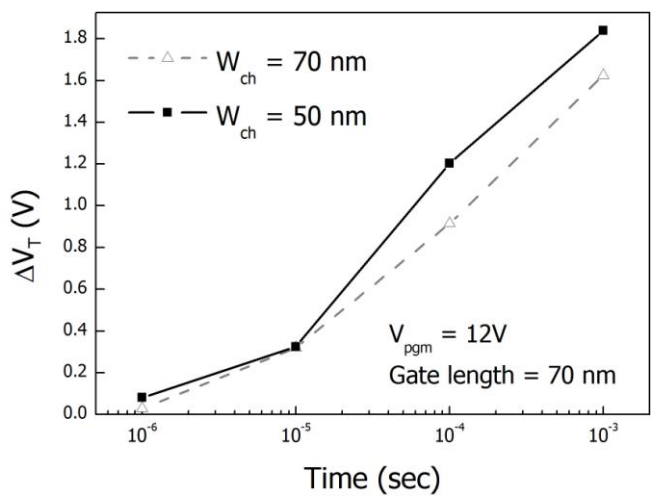
(b)

Fig. 5. 3 (a) Program (b) Erase operation (L_g=100 nm, W_{ch} = 50 nm)

Differently defined gate lengths (L_g) and channel widths (W_{ch}) result in different electrical characteristics. Fig. 5.4 (a) presents the amount of V_T shift when programming with 12 V for 1 ms as a function of gate length. As gate length increases, wider program windows were achieved. Fig. 5.4(b) shows the program speed with different channel widths. In this device, channel widths are related to the diameter of silicon nanowire. Devices with narrow channels show improved cell characteristics due to stronger field concentration effect. The field concentration effect that we can get from nanowire channel surrounded by gate is helpful to overcome the short channel effects.



(a)



(b)

Fig. 5.4 (a) V_T shift as a function of gate length (b) Program speed with different channel widths (50 nm, 70 nm)

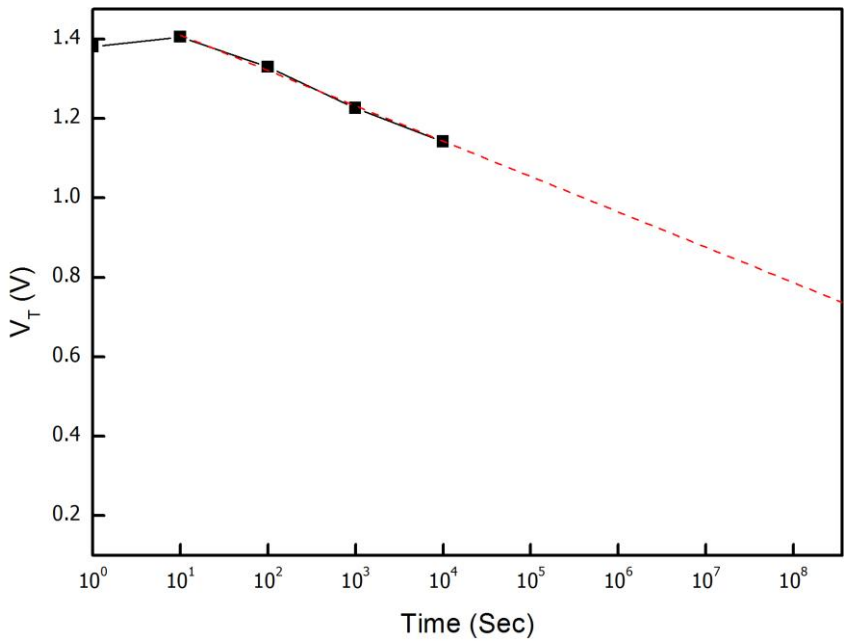


Fig. 5.5 Retention characteristics after programming with 12V for 100 μs

Fig 5.5 is retention characteristics obtained from programmed cell (12V, 100 μs) at 85 ℃. It is expected that about 50% of charges will be lost after 10 years. It is worthwhile to try improving this poor retention characteristics by using band engineered SONOS (BE-SONOS) [15] or silicon nanocrystal in nitride layer [16].

6. Conclusion

Flash memory technology scaling has enabled mobile device market such as smart phones, tablet PCs, solid-state drive, and MP3 players to explode by providing high density non-volatile storage. To achieve further scaling, new solutions are required to overcome scaling issues including limitation of lithography technology, short-channel effects, and floating-gate coupling. Three-dimensional stacked NAND flash memory is one of the most outstanding solutions.

A newly designed channel stacked array NAND flash memory structure, compact STAR, is proposed to be compatible with conventional peripheral circuits and enhance storage density. Compact STAR features gate-all-around (GAA) structure and single-crystalline channels. Fabrication process of compact STAR is also designed, and the process can implement metal gates.

To demonstrate the benefits from metal gates and GAA structure, simulation works are carried out. Metal gates can guarantee stable program characteristics compared to poly-Si gates, since metal gates are free from poly depletion effects. In addition to gate materials, the effect of physical structure of gates on the program characteristics has been studied. We can conclude that cells with GAA structure show better characteristics less sensitive to gate dimensions compared to double gate (DG) structure. It is because surrounding gates have strong field concentration effect.

Lastly, gate-all-around (GAA) poly-Si channel NAND flash with charge trap layer (Si_3N_4) have been successfully fabricated. Electrical characteristics were measured with various gate lengths and channel widths, and memory characteristics of fabricated devices were confirmed. Measurement results indicate much room for improvement, and it is noteworthy to fabricate high performance channel stacked array flash memories.

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초 록

본 논문에서는 고집적 낸드 플래시 메모리 구현을 위한 수직 적층형 3 차원 메모리에 대한 연구를 수행하였다. 기존에 제시된 수직 적층형 3 차원 메모리 어레이의 단점을 보완하고자 SSL 을 수직으로 적층하여 층 선택이 가능한 구조를 제안하였다. 또한 단결정 실리콘을 채널을 이용할 수 있고, 게이트 올 어라운드 구조를 채택할 수 있는 공정 방법을 제시하였다.

새롭게 제안한 컴팩트 스타 구조가 가질 수 있는 특징으로서 메탈 게이트의 장점을 전산모사를 통하여 확인하였다. 다결정 실리콘 게이트와의 특성을 비교하였을 때 메탈 게이트가 메모리 소자의 특성에 어떠한 영향을 미치는지 연구를 수행하였다.

그 다음장에서는 게이트 올 어라운드 구조가 더블 게이트 구조와 비교하

였을 때 3 차원 적층 구조에서 가질 수 있는 이점을 전산 모사를 통해 검증하였다.

마지막으로 게이트 올 어라운드 구조를 가지는 메모리 소자를 제작하여 그 특성을 확인하고 분석하였다.

주요어 : 3차원 메모리, 낸드 플래시 메모리, 적층형 어레이, 실리콘 나노와이어

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