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Investigation of Bipolar Resistive Switching Characteristics of Si$_3$N$_4$-based RRAM with MIS Structure

MIS구조의 실리콘질화막 기반 저항메모리의 양극성 저항스위칭 특성에 대한 연구

BY

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이 논문을 공학석사 학위논문으로 제출함

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서울대학교 대학원
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김성준

김성준의 공학석사 학위논문을 인준함

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ABSTRACT

New memories such as phase change RAM (PRAM), magnetoresistive RAM (MRAM) and resistive RAM (RRAM) are expected to replace Si-based DRAM and NAND Flash faced with technical and physical limits. RRAM is a strong candidate for high density and low power application because of its simple structure, CMOS compatibility, scalability and applicability of 3D structure and MLC operation. However, unsolved some critical issues such as the leakage currents at crossbar array, high operating current and poor uniformity are an obstacle for commercialization in market. Recently, RRAM using transition metal oxides (TMO) such as HfO₂, TaO₂ shows excellent resistive switching characteristics such as high endurance (>10⁹), fast writing speed (<10 ns), scalability (<10 nm). However, other resistive materials can be potential candidates when having comparative advantage and finding their suitable applications. Nitride-based RRAM have been recently reported with good endurance and retention and fast switching speed.
In this thesis, Si$_3$N$_4$-based RRAM with metal-insulator-silicon (MIS) was fabricated in respect to high density, mass production issues and new applications. MIS structure has an advantage of integrating with a selector such as diode or transistor without bottom electrode (BE) using metal which must require deposition and patterning. And, Ti as top electrode (TE) is used to avoid noble metals such as Pt, Au, and Ru which are expensive and hard to etch. Low pressure chemical vapor deposition (LPCVD) is used for deposition of Si$_3$N$_4$. LPCVD is suitable for vertical 3D stacking due to good step coverage for high density. The switching mechanism of this memory structure is explained by fitting in double logarithmic scale and temperature dependency. HRS and LRS are well agreement with SCLC (Space charge limited current). Forming-free behavior that is originated from thin thickness of switching layer is useful to low operation switching. And, self-compliance is observed by restriction of parasitic resistance without an external current limiter. Also, multi-level storage ability is demonstrated for potential of MLC operation for high density. Distinct set and reset transition that are gradually modulated by controlling voltage stop and
compliance current can be used to employ MLC operation. Finally, the potentiating and depressing of the current are performed by pulse and DC voltage mode for neuromorphic systems as new applications.

**Keywords:** Si$_3$N$_4$-based RRAM, forming-free, self-compliance, gradual set/reset, MLC, neuromorphic

**Student number:** 2011-20804
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Bibilography

Abstract in Korean
1. Introduction

It is still far from an ideal memory satisfying all aspects of high speed, low cost, and low power at the same time despite continuous efforts in the memory industry. Thus, some memories are required in memory hierarchy depending on the use such as cache, working memory and storage memory in Fig 1.1 [1]. Recently, charge trap memory like NAND flash and dynamic random access memory (DRAM) as major market driver has been faced with difficulties owing to scaling limits for high density and low power consumption for green environment [2]. Therefore, next generation non-volatile memory devices so called emerging memory such as PRAM, MRAM RRAM have been extensively investigated in Fig 1.2. These memories show high density, high speed and non-volatile in common.
Fig. 1.1 Memory Hierarchy [1]
Especially, RRAM which is a potential candidate to replace NAND flash as storage memory has many advantages of simple structure, easy fabrication, small cell size of $4F^2$ possibility and research in a wide variety of resistive materials [3-10]. Even though there are a lot of effects about improvement of resistive switching characteristics by optimizing switching layer and electrode materials, it is still needed to ensure better performance in terms of the operation current, uniformity, endurance and retention. Above all, unknown switching mechanism is an enormous obstacle in order to improve aforementioned issues. When limiting the scope in redox-based resistive switching in RRAM, three basic mechanisms are dominant: electrochemical metallization mechanism (ECM), valence change mechanism (VCM) in Fig. 1.3 [10].
Fig. 1.2 Tree of Memory including new memories [1].
Unipolar RRAM where resistive switching is determined by amplitude of the applied voltage but not polarity is well explained by conducting filament model based on TCM [11]. Thermochemical redox process like anti-fuse model driven by thermal effect is dominant over electrochemical process. However, resistive switching of bipolar RRAM depends on amplitude and polarity of the applied voltage. Especially, TMO showing bipolar switching is mostly based on VCM. Conducting filament is formed or ruptured depending on movement of oxygen vacancies by the applied voltage. And, resistive switching of conductive bridging RAM (CBRAM) is dominant on ECM. Metallic conducting bridge is formed and ruptured in insulator between TE and BE when the voltage bias is applied on an electrochemically conductive metal used as TE.
Fig. 1.3 Classification of the resistive switching effects [10].
The typical two resistive switching behaviors are observed in Fig. 1.4. High resistance state (HRS) requires the set process to turn into low resistance state (LRS). Usually, the compliance current (I\textsubscript{CC}) is needed during the set process in order to prevent permanent breakdown. Especially, first set process is called forming process which requires more voltage because of higher resistance at an initial state. In case of bipolar RRAM, the voltage of opposite polarity at the set process is applied to device cell for the reset process. By conducting filamentary model, the change of resistance is attributed to a formation and rupture of conducting filament.

From a memory cell and array design viewpoint, unipolar RRAM that is able to be realization of the 1D-1R crossbar array structure is competitive over bipolar RRAM [12]. For high density and low-power application, the reset
current ($I_{\text{RESET}}$) is significantly important [13]. When using diode as current source, $I_{\text{RESET}}$ must be continuously scaled to allow scaling to a smaller design rule in unipolar RRAM. When using the Si-based diodes with the high current density, the scaling can be possible into 10nm area [14]. However, unipolar RRAM shows poor repeatability and uniformity of parameters such as the set voltage ($V_{\text{SET}}$)/reset voltage ($V_{\text{RESET}}$) and LRS/HRS resistance. These are severe obstacles for mass production of RRAM, thus bipolar RRAM showing a relatively superior resistive switching is more extensively researched than unipolar RRAM nowadays.
Fig. 1.4 The typical I-V curves of unipolar RRAM (a) and bipolar RRAM (b)

[10]
2. Motivation

Extensive research on resistive switching characteristics in a wide variety of resistive material is ongoing since resistive switching device using TMO was reported in 2004 which used a large device area and showed high reset current, and a relatively slow switching speed and poor endurance [3]. There are a lot of improvements in resistive memory cells showing low reset current (<10 μA) [7-8], fast switching speed (<10 ns) [7], superior endurance [9], retention and selector device that shows good non-linear I-V characteristics, the current density and endurance [15-16]. However, for mass production, some critical issues such as the use of non-noble metal still remain to be addressed. Moreover, the cost is a significantly important factor in mass production, thus MLC [17], 3D stacking [18] and more scaling [19] are needed.
In RRAM. In addition, new applications such as neuromorphic computing can be driving force of expansion of memory market [20-22]. Until now, a wide variety of resistive materials have been investigated. Looking for a combination of proper resistive materials is effective ways to obtain excellent resistive switching characteristics for RRAM applications. For example, there are ferromagnetic materials such as Pr$_{1-x}$Ca$_x$MnO$_3$ [23], pervoskite oxides [24] such as SrTiO$_3$, SrZrO$_3$ and TMO such as NiO [3], TiO$_2$ [17], HfO$_2$ [7] and TaO$_2$ [8].

Nitride-based RRAM is being recently investigated due to good endurance and retention and fast switching speed. Especially, a lot of traps in silicon nitride (Si$_3$N$_4$) are favorable to RRAM applications because the traps can be a source for the formation and rupture of conducting filaments. In
addition, compatibility of being integrated in back end of line (BEOL) process in CMOS is another strong point. Usually, two types switching mechanism in nitride-based RRAM are known depending on an electrode. When using electrochemically conductive metal such as Ag, Cu, these can be a source of switching in Si₃N₄ dielectric [25]. Another case is explained by electron hopping through nitride related trap. However, the more detail switching mechanism of nitride-based RRAM is needed to be elucidated.
3. Fabrication Process

Electrical properties of Si$_3$N$_4$ films are different in several aspects by deposition methods. Thus, first of all, resistive characteristics of RRAM depending on nitride deposition methods must be investigated. In this thesis, Si$_3$N$_4$ was deposited by LPCVD. Silicon nitride by deposited by LPCVD is usually amorphous state and used for excellent passivation layers. Reproducible resistive switching was only reported in very thin thickness (< 15 nm) [26]. For high density, 3D vertical type RRAM requires ALD or CVD deposition. Thus, Si$_3$N$_4$-based RRAM using LPCVD, in particular, is applicable to 3D vertical RRAM in the future, because conformal deposition is possible due to good step coverage. Figure 3.1 shows the schematic drawing
of fabricated device. And, cross-sectional TEM image (a) and process flow (b) are in Fig. 3.2. More detailed fabrication process is depicted in Fig 3.3. First, 10-nm-thick SiO$_2$ was grown by dry oxidation for protection of damage cluster of during ion implantation. Subsequently, Si was doped with BF$_2$ (dose: 1×10$^{15}$ cm$^{-2}$, energy: 40 keV) by ion implanter in order to form p$^+$-Si on Si substrate. Next, 5 nm-thick Si$_3$N$_4$ was deposited by LPCVD at 785 °C after HF cleaning to remove SiO$_2$. Finally, Ti as TE was formed using an RF sputtering system and patterned by a conventional photolithography. TE size and thickness are 100 × 100 μm$^2$ and 100 nm, respectively. All electrical characterizations were performed by Agilent 4156C semiconductor parameter analyzer. And BE was grounded and the positive voltage bias was applied to the TE.
Fig. 3.1 The schematic drawing of Ti/Si$_3$N$_4$/p$^+$-Si RRAM device.

Fig. 3.2 Cross-sectional TEM image (a) and process flow (b).
Fig. 3.3 Illustration of fabrication process of Ti/Si$_3$N$_4$/p$^+$-Si RRAM device.
4. Electrical Characteristics and Analysis

In this chapter, the basic resistive switching characteristics including the conduction mechanism is investigated in Ti/Si$_3$N$_4$/p$^+$-Si RRAM stacked cell. Figure 4.1 shows that typical bipolar resistive switching is observed. Device is set at a current compliance of 100 $\mu$A to prevent permanent dielectric breakdown. First of all, the measured I-V fitting is analyzed in voltage sweep mode to investigate the conduction mechanism. I-V curve is plotted into other scales for the SCLC ($\log(I) \propto \log(V)$), Schottky barrier thermionic emission ($\log(I) \propto V^{1/2}$) and Poole-Frenkel emission ($I \propto \exp(V^{1/2})$). Fig. 4.2 shows the fitted plot by using a log-log scale to identify SCLC model. Both HRS and LRS are well fitted with trap controlled SCLC mechanism.
Fig. 4.1 Typical I-V characteristics of Ti/Si$_3$N$_4$/p$^+$-Si RRAM.

Fig. 4.2 Log-log plot of I-V curves.
The slope changes from the region 1 called Ohmic region (I~V) to region 2 called the Child’s square law region (I~V^2) at a threshold voltage (V_T) while trap filled charge increases. And in the higher voltage region between region 2 and region 3 where a current increased shapely. This charge transportation is related with SCLC which is explained in detail below. [27]

The current density for the Ohmic conduction in which thermally generated carrier is dominant can be expressed as follows:

\[ J_{\text{Ohm}} = q n_0 \mu_n \frac{V}{d_s} \]  \( (4.1) \)

Where, \( J_{\text{Ohm}} \) is current density, \( \mu_n \) is the electron mobility, \( V \) is the applied voltage and \( d_s \) is the thickness of the film.

The current density for the Child’s square law in which injected carrier is dominant can be expressed as follows:
\[ J_{\text{Child}} = \frac{9}{8} \varepsilon \mu_n \theta \frac{V^2}{d_s^3} \]  

Where, \( \varepsilon \) is permittivity of material, \( \theta \) is the ratio of occupied electron trap. When most electron taps are occupied (\( \theta \gg 1 \)), current density can be written by

\[ J = \frac{9}{8} \varepsilon \mu_n \frac{V^2}{d_s^3} \]  

Figure 4.3 shows the probable forward current transport diagram. As nitride related traps are occupied with increased voltage bias during the set process, conduction path (CP) is formed. The opposition to the set process, de-trapping occurs on critical point (\( V_{\text{RESET}} \)) in the reset process where current drops rapidly in LRS [28]. However, LRS is not metallic path according to fitting results using log-log scale does not follow Ohmic behavior and temperature dependency indicating semiconducting behavior in Fig. 4.4.
Fig. 4.3 Forward current transport drawing indicating trap to trap hopping behavior.

Fig. 4.4 LRS resistance as a function of temperatures.
Figure 4.5 shows that forming voltage ($V_{FORMING}$) is comparable to $V_{SET}$.

First set process (Forming process) is within a dispersion of subsequent set switching in all samples. This is attributed to the Si$_3$N$_4$ thickness of 5 nm and the initially high leakage due to nitride-based traps which help to lower $V_{FORMING}$. It is well known that $V_{FORMING}$ is easily tuned by thickness of switching layer [29]. Measured $V_{SET}/V_{RESET}$ and on/off resistance distribution are shown in Fig. 4.6. On/off resistance ratio is under 10 in some cycles. The main reason of decreased resistance ratio and failed endurance is the fact that the reset operation is not fully completed. Thus, it is needed to more accurate control during the reset process to make sure a reasonable on/off resistance ratio.
Fig. 4.5 Forming voltage and set voltage of 5 devices each (a) and statistic distribution of 50 devices (b).
Fig. 4.6 Cycling characteristics of set and reset voltage (a) and endurance (b).
To obtain increased resistance ratio, the compliance current ($I_{CC}$) dependency of resistance of HRS and LRS is investigated. Fig.4.7 shows that LRS has stronger dependency with $I_{CC}$ than HRS. It indicates that lower LRS resistance with more CP can lead to high resistance ratio in spite of disadvantage of having the higher reset current in Fig 4.8. Another advantage of having more than 100μA of $I_{CC}$ is self-compliance. It is presumably originated from the restriction of parasitic resistance in the device. Permanent breakdown can be stopped by self-compliance during the set process without external current limiter such as transistor. Also, a wider pulse margin is obtained and the overshoot effect that causes uncontrolled CP can be stopped by self-compliance.
Fig. 4.7 Resistance of HRS/LRS as a function of compliance current.

Fig. 4.8 On/off resistance ratio as a function of compliance current.
Fig. 4.9 Typical I-V curve (compliance current = 1 mA).
Next, the feasibility of MLC operation is demonstrated for high density cell. For MLC in RRAM, gradual resistance changes as well as high resistance ratio is essential. Figure 4.9 indicates typical I-V curve where a sudden increase of current occurs at 2.5 V. After that, few steps of current increase is observed in 2.5 ~ 3.5 V (Fig. 4.10 (a)). Although detailed conduction mechanism is still not clear as mentioned above, it is closer to filament bipolar model rather than interface model because a sudden change is observed during first set transition and \( V_{RESET} \) is well linear with \( I_{CC} \). Thus, in order to explain about the set transition, a possible scenario can be constructed by assuming the formation if tiny CPs at the current steps. Tiny CPs are sequentially produced during gradual set process after main path is formed near 2.5 V. The reset process can be explained by reversing sequence of the set process in
Fig. 4.10 (b).

![Graph showing Gradual Set behavior with voltage and current values.](image)

![Graph showing Gradual Reset behavior with voltage and current values.](image)
Fig. 4.10 Gradual set and reset in I-V curve.

Figure 4.11 shows multi-level states in case of both the set and reset state. During the set process, formation of CP is restricted by $I_{CC}$ (10 $\mu$A, 100 $\mu$A and 1 mA) to generate distinguish four resistance states in fig. 4. 11(a). And four distinctive resistance states are also formed by dividing states of gradually increasing resistance during the reset process in Fig 4. 11(b). Here, the stop of $V_{RESET}$ (-2 V, -2.2 V, -2.4 V) is controlled. The retention performance of Ti/Si$_3$N$_4$/p$^+$-Si RRAM is evaluated at the read voltage of 0.3 V as shown in Fig 4. 12. Four different resistances for multi-level exhibit little degradation during the $10^4$ second testing time.
Fig. 4.11 MLC operation at the set state (a) and reset state (b).
Fig. 4.12 Retention test for multi-level cell.
Next, the possibility of neuromorphic applications is investigated. New application can be a driving force for the expansion of memory market. Neuromorphic computing technology is now receiving the spotlight for an alternative of von Neumann bottleneck. Neuromorphic device which imitates biological synapse and neuron system is expected to be able to deal with parallel processing on large amounts of data [20-22]. Fabricated Ti/Si₃N₄/p⁺-Si stacked RRAM cell is measured in voltage sweep mode and pulse mode repeatedly at the same voltage. The current is incrementally overall increased or decreased by consecutive potentiating (sweep: 2.5 V, pulse: 3.5 V) or depressing signal sweep: -1.7 V, pulse: -2.4 V) in Fig 4.13 and Fig 4.14. It is noteworthy that the amount of small resistance at the same amplitude of voltage because it is different from conventional RRAM cell showing abrupt
resistance switching or graduation resistance changes only under a condition of varied voltage bias. However, additional demonstration of pulse test such as spike-timing-dependant plasticity (STDP) and the more accurate control are needed to confirm the possibility of the neuromorphic device applications.

Finally, the criteria and the improvement of fabricated RRAM cell in terms of high density and mass production issues are summarized in Table.

1. For 3D stacking structure, Ti as TE can be replaced with W that is available material to CVD deposition. And, plasma enhanced CVD (PECVD) whose process temperature is about 300 C can be a solution for low thermal budget when Si$_3$N$_4$ film is deposited.
Fig. 4.13 Successive writing processes (a) and erase processes (b).
Fig. 4.14 Pulse responses showing potentiation (a) and depression (b).
<table>
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<th>Parameters</th>
<th>Evaluation</th>
<th>Improvement and Solution</th>
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<tbody>
<tr>
<td>High density</td>
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<tr>
<td>MLC</td>
<td>Yes</td>
<td>Need more on/off ratio with no degradation</td>
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<tr>
<td>Extension to vertical 3D stacking</td>
<td>Yes</td>
<td>TE available CVD: ex) Tungsten (W)</td>
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<td>Mass production issues</td>
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<tr>
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<td>Yes</td>
<td>Extension to array structure with a selector</td>
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<td>Non-noble electrodes</td>
<td>Yes</td>
<td>Need better resistive characteristics: endurance, uniformity</td>
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<tr>
<td>Low thermal budget</td>
<td>No</td>
<td>PECVD (process temperature: 300°C)</td>
</tr>
</tbody>
</table>

Table.1 Criteria and improvement of fabricated RRAM cell in terms of high density and mass production issues
6. Conclusion

RRAM is one of the strong candidates with a lot of potentials in terms of simple structure, easy fabrication, high density and low power application. An ideal resistive material satisfying all memory requirements and the fabrication process have not been founded even though RRAM based on a wide variety of materials are extensively researched at the same time. Recently, Nitride-based RRAM showing superior resistive characteristics such as fast programming speed, excellent endurance and long lasting retention has been reported.

In this thesis, silicon nitride-based RRAM cell using fab-friendly materials was fabricated. P⁺-Si (BE) is directly fabrication on source/drain region of transistor, which is different from conventional RRAM using a metal as BE. Also, Ti is used as TE instead of noble metal that is expensive and difficult to etch. For high density, silicon nitride-based RRAM using CVD
deposition is easily applicable to vertical type RRAM in the future.

Ti/Si$_3$N$_4$/p$^+$-Si RRAM cell shows bipolar resistive switching where most operation is under -2 V ($V_{\text{RESET}}$) and 3 V ($V_{\text{SET}}$). And, conduction mechanism can be explained by trap controlled SCLC through log-log scale fitting and temperature dependency. Forming-less behavior and self-compliance effect is useful to circuit design. On/off ratio increases with $I_{cc}$ thus, MLC operation is obtained by controlling stop voltage during the reset process and $I_{cc}$ during the set process. Finally, synapse devices application is identified. Potentiation and depressinon of the current is controlled through both DC sweep mode and AC pulse mode by consecutively same voltage amplitude.
Bibliography

[1] Lecture note of Samsung Electronics Co.Ltd.


초 록

DRAM과 NAND Flash와 같은 기존의 실리콘 기반의 메모리 소자의 크기가 작아짐에 따라 기술적, 물리적 한계에 직면하고 있다. 따라서 PRAM, MRAM 그리고 RRAM(저항메모리) 같은 새로운 메모리가 기존 메모리의 대체를 위해 현재 활발히 연구중이다. 저항메모리는 단순한 구조, CMOS 구조와 호환성, 스케일링 가능성, 3차원 구조의 적응성 그리고 다중셀에 대한 동작 가능성을 고려하여, 특히 고집적화 저전력 적용을 위한 차세대 메모리에 적합하다. 하지만 어레이구조에서의 누설전류, 산포문제 그리고 높은 동작전류 등이 아직 상업화를 위한 큰 장애물로써 아직 해결되지 않은 문제점들이다. 최근에 HfOₓ, TaOₓ 같은 transition metal oxide(TMO)는 정보를 쓰고 지우는 횟수(> 10¹²), 빠른 스위칭 스피드(< 10 ns), 스케일링(< 10 nm)을
보여주고 있다. 그러나, 다른 저항물질들을 사용한 저항메모리 역시 각각의 특성에 맞는 적용가능한 어플리케이션 및 상대적인 특성에 대한 우위를 가지고 있어서, 다양한 물질들이 저항메모리의 사용을 위해서 활발히 연구가 되고 있다. 질화막 기반의 저항메모리 역시 최근에 우수한 읽고 쓰기 횟수, 메모리 상태 유지, 빠른 스위칭 스피드를 보여주는 문헌들이 보고가 되고 있다.

본 연구에서는 metal-insulator-metal (MIS) 구조를 가지는 질화막 기반의 저항메모리의 저항특성에 대해서 연구가 되었다. MIS 구조는 하부금속층이 필요없이 다이오드와 트렌지스터와 같은 셀렉터에 바로 연결이 될 수 있는 장점을 가지고 있다. 그리고 상부금속층으로 Ti 를 사용하므로써 웨이트 채인 적인 구조를 사용하였다. 또한 LPCVD (low pressure chemical vapor deposition) 을 이용하여 질화막 증착을 하여, 균일한 박막형성뿐만 아니라 우수한 step
coverage 로 기인하여 향후 3D 구조 저장매모리에 적합한 형태를 가지고 있다. 더블 로그 fitting 과 온도특성을 분석하여, 트랩을 통제하는 SCLC (space charge limited current) 컨덕션 메커니즘을 따름을 확인하였다. 5 nm 의 얇은 절화막의 두께로 인하여 포밍프리 현상이 관찰되었고, 또한 set 동작 시, 기생저항으로 인하여 자생전류제한 현상은 외부의 추가적인 전류제 한원을 두지 않아도 되는 장점을 가진다. 또한 다층셀의 가능성을 확인하기 위해, 점진적으로 변하는 저항을 전압과 전류를 통제를 함으로써 2 bit/cell 을 구현하였다. 그리고 각각의 저항의 상태에서 150 °C 에서 10^4 초 동안 저항의 변화가 거의 없음을 확인하여 우수한 정보유지 특성을 보였다. 마지막으로 DC 모드와 AC 모드에서 점진적인 저항 컨트롤을 통해 시냅스 소자에 대한 적용가능성을 확인하였다.
주요어: 질화막기반의 저항메모리, 포밍프리, 자생전류제한, 점진적인스위칭。

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