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M.S. THESIS

Analysis of Failure Mechanisms
based on 3D TCAD Simulation and Measurement
in NAND Flash memory cell

3D TCAD 시뮬레이션과 측정을 기반으로 하는 NAND
Flash 메모리 셀의 불량 메커니즘 분석

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ABSTRACT

As the device of NAND Flash memory has been extremely scaled down (sub-30nm), many reliability issues related to the device characteristics have appeared. Particularly, the retention characteristics cannot be explained anymore by the conventional lifetime evaluation method (Arrhenius model) because there are various failure mechanisms contributing to the charge loss of device. To estimate the accurate prediction of lifetime, we previously proposed a new lifetime evaluation method (proposed method) which is superposition of the behaviors of three dominant failure mechanisms (detrapping, trap-assisted tunneling (TAT), and interface trap (N_d) recovery mechanism). From the proposed method, we separated the amount of charge loss of each failure mechanism (\(\Delta V_{TH,Detrap}, \Delta V_{TH,TAT},\) and \(\Delta V_{TH,N_d}\)) from total charge loss (\(\Delta V_{TH,TOTAL}\)) in test element group (TEG) cells of the advanced NAND Flash memory for different generations (A, B, and C).

In this paper, we investigated the behavior of Arrhenius plot for lifetime
estimation in NAND Flash memory using 3D TCAD simulation, where the number of failure mechanisms and the criterion determining failure data \((\Delta V_{TH,FAIL})\), the percentage of total charge loss \((\Delta V_{TH,TOTAL})\) at specific temperature, are considered. When detrapping and trap-assisted tunneling (TAT) mechanism are applied to retention simulation together, abnormal behavior of Arrhenius plot was observed and explained by mechanism separation with the proposed method. In addition, as TAT mechanism proportion is larger than detrapping mechanism proportion in \(\Delta V_{TH,TOTAL}\), abnormal characteristics of Arrhenius plot was obviously observed. Finally, two experiments which are charge pumping (CP) and \(1/f\) noise analysis were conducted to verify the 3\(^{rd}\) mechanism extracted on generation A, B, and C in previous work. Relative \(N_{It}\) extracted by two experiments showed perfect correlation with the amount of charge loss of 3\(^{rd}\) mechanism \((\Delta V_{TH,NIt})\). As a result, the 3\(^{rd}\) mechanism was verified as \(N_{It}\) recovery mechanism.
**Keywords:** NAND Flash memory, Failure mechanism, Detrapping mechanism, Trap-assisted tunnelling (TAT) mechanism, Interface trap recovery (N\text{it}) mechanism, retention time (t\text{R}).

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1. Introduction

The aggressive scaling-down of NAND Flash memory makes this type of memory increasingly sensitive to reliability issues. As a result, accurate lifetime estimation in NAND Flash memory is important for a mass production. Until now, a high temperature-accelerated lifetime evaluation method known as conventional lifetime evaluation method has been generally used to estimate lifetime of electric device at user interface temperature [1]. However, this simple application cannot be applied anymore to lifetime estimation in NAND Flash memory because several failure mechanisms have an effect on the lifetime simultaneously and roll-off phenomenon of activation energy ($E_a$) is observed [2], [3]. Thus, we previously proposed a new method which is superposition of behaviors of three dominant failure mechanisms (detrapping mechanism [4], [5], TAT mechanism [4] and $N_r$ recovery mechanism [6], [7], [8]), separated total charge loss into the amount of charge loss of each failure mechanism, and extracted each $E_a$ in 21-nm NAND Flash memory cells [9] and in other generations [10].
In this work, we analyzed failure mechanisms using 3D TCAD simulation and experiments basically.

In chapter 2, at first, we explained various failure mechanisms, the conventional lifetime evaluation method (conventional method), and proposed lifetime evaluation method (proposed method). And then, retention simulation was conducted for the three cases using 3D TCAD simulation where the first and the second only include detrapping and TAT mechanism respectively and the third includes detrapping and TAT mechanism together. The behavior of Arrhenius plot was observed according to $\Delta V_{TH,FAIL}$ for the three cases. In addition, additional retention simulation was conducted when proportions of two mechanisms are changed in $\Delta V_{TH,TOTAL}$ at specific temperature as reference temperature while the amount of $\Delta V_{TH,TOTAL}$ is maintained.

In chapter 3, In order to verify the 3rd mechanism separated by proposed method in previous work [10], charge pumping (CP) measurement [11] and $1/f$ noise analysis were conducted. As a result, the 3rd mechanism was verified as $N_a$ recovery mechanism.

2
2. Analysis of Failure Mechanism using 3D TCAD Simulation

2.1 Introduction

As NAND Flash memory cell has been extremely scaled down (sub 30nm), the number of electrons determining the cell state is decreased, which enhances the effects on single-electron. Thus, there are many reliability issues directly associated with retention characteristics. To understand these reliability issues, it is important to study failure mechanisms which have an effect on retention characteristics. There are various failure mechanisms as shown in Fig. 2.1 visually. Where interface trap recovery is a charge loss mechanism when electrons captured at Si/SiO₂ interface trap get out of interface trap or generated interface traps are dissipated by annealing phenomenon (recovery), detrapping is a charge loss mechanism when electrons captured by SiO₂ defects (bulk traps) are thermally emitted to conduction band in SiO₂ or pass through SiO₂ layer as
tunneling process, intrinsic charge loss is a charge loss mechanism when electrons in the floating gate jump or pass through SiO$_2$ barrier (not shown in Fig. 2.1), trap-assisted tunneling is a charge loss mechanism when electrons on floating gate conduction band easily get out of the floating gate by tunneling process due to deep level defects which lower the SiO$_2$ barrier height and shorten effective tunneling distance, and there is a charge loss in ONO layer where electrons captured by SiO$_2$ or nitride defects get out of ONO layer. Each failure mechanism has intrinsic $E_a$. It has been reported that $E_a$ of detrapping mechanism is 1.1 – 1.2 eV [12]-[14], $E_a$ of TAT mechanism is below 0.3 eV [15]-[17], and $E_a$ of $N_{it}$ recovery mechanism is 0.1-0.2 eV [18]-[20].

All failure mechanisms shown in Fig. 2.1 do not always contribute to the charge loss. Some failure mechanisms dominantly influence the charge loss. For example, there are interface trap ($N_{it}$) recovery, detrapping, and trap-assisted tunneling (TAT) mechanism as mentioned in previous work [9], [10].

In this chapter, at first, two lifetime methods (conventional lifetime evaluation method and proposed method) was explained and compared. And
then, we analyzed retention characteristics for failure mechanisms based on TCAD 3D simulation. In the simulation, the two failure mechanisms (detrapping and TAT mechanism) were considered as dominant mechanism contributing to charge loss. Sentaurus TCAD simulation was used as simulation tool.

Fig. 2.1. Various failure mechanisms in NAND Flash memory cell.
2.2 Lifetime Evaluation Methods

2.2.1 Conventional Lifetime Evaluation Method

Generally, to estimate lifetime of device at room temperature or user interface temperature in case of mass product devices, Arrhenius model is commonly used which is known as conventional lifetime evaluation method (conventional method). For a given criterion determining failure data ($\Delta V_{TH,FAIL}$), lifetimes obtained by high temperature-accelerated lifetime evaluation method are extrapolated to low temperature range. Fig. 2.2 shows conventional method based on Arrhenius model. In the left side of the figure, there is a square box meaning high temperature range. In this box, there are lifetimes ($t_{HT}$) on the straight line. To obtain the device lifetime ($t_{LT}$) at the room temperature, this line is extended to symbol and it is expressed by the relationship [1]

$$AF = \frac{t_{LT}}{t_{HT}} = \exp \left[ \frac{E_a}{k} \left( \frac{1}{T_L} - \frac{1}{T_H} \right) \right]$$

$$\Rightarrow t_{LT} = t_{HT} \cdot \exp \left[ \frac{E_a}{k} \left( \frac{1}{T_L} - \frac{1}{T_H} \right) \right]$$

(2.1)
where $AF$ is acceleration factor between bake temperature and room temperature, $t_{LT}$ is retention time at the room temperature, $t_{HT}$ is retention time at the bake (high) temperature, $E_a$ is the activation energy which is slope of inverse $kT$ axis (x-axis) and logarithm of the retention time axis (y-axis), $k$ is Boltzmann’s constant, $T_{LT}$ is the room temperature, and $T_{HT}$ is the bake temperature. In order to use (2.1), $E_a$ should be a constant at all temperatures. Constant $E_a$ means that failure mechanism contributing to charge loss is only the one.

**Fig. 2.2.** Conventional lifetime evaluation method based on Arrhenius model.
2.2.2 Proposed Lifetime Evaluation Method

In extremely scaled NAND Flash memory cell, dominant failure mechanism contributing to charge loss is not the one as mentioned in previous section. Actually, extrapolation of lifetime is inconsistent with real lifetime at low temperature range since various failure mechanisms are mixed together and dominant failure mechanism is different on temperature. Therefore, a new lifetime evaluation method for NAND Flash memory is needed to extract accurate lifetime prediction. We previously proposed a new lifetime evaluation method (proposed method) which is superposition of behaviors of dominant failure mechanisms [9], [10]. The following is equation of proposed method.

\[
\Delta V_{TH, TOTAL} = \Delta V_{TH,1} \cdot \left[ 1 - \exp \left( - \frac{t_R}{\tau_1} \right) \right] + \Delta V_{TH,2} \cdot \left[ 1 - \exp \left( - \frac{t_R}{\tau_2} \right) \right] + \Delta V_{TH,3} \cdot \left[ 1 - \exp \left( - \frac{t_R}{\tau_3} \right) \right] \\
+ \Delta V_{TH,4} \cdot \left[ 1 - \exp \left( - \frac{t_R}{\tau_4} \right) \right] \ldots + \Delta V_{TH,N} \cdot \left[ 1 - \exp \left( - \frac{t_R}{\tau_N} \right) \right]
\]

(2.2)

where \( \Delta V_{TH, TOTAL} \) is the amount of total charge loss according to bake time at specific temperature, \( \Delta V_{TH,1} \) is the amount of charge loss of a failure mechanism...
after sufficient bake time passes (when saturated), \( \tau_f \) is time-constant of a failure mechanism, and \( t_R \) is retention time. \( \Delta V_{TH,I} \) and \( \tau_f \) rely on temperature. The others have the same physical meaning on the each failure mechanism. By using this method and measured data, we separated the total charge loss (\( \Delta V_{TH,TOTAL} \)) into the amount of charge loss of each failure mechanism. As a result, three dominant failure mechanisms (detrapping, TAT, and \( \text{N}_a \) recovery mechanism) were observed. Then, equation (2.2) can be revised as

\[
\Delta V_{TH,TOTAL} = \Delta V_{TH,\text{Detrap}} \left[ 1 - \exp \left( - \frac{t_R}{\tau_{\text{Detrap}}} \right) \right] + \Delta V_{TH,TAT} \left[ 1 - \exp \left( - \frac{t_R}{\tau_{\text{TAT}}} \right) \right] + \Delta V_{TH,\text{N}_a} \left[ 1 - \exp \left( - \frac{t_R}{\tau_{\text{N}_a}} \right) \right]
\]

(2.3)

When it comes to lifetime estimation, the proposed method is more accurate than conventional method. Fig. 2.3 shows lifetime obtained by conventional method (Arrhenius model) and obtained by measurement, where lifetimes at high and low temperature range (210°C ~ 55°C) are obtained at bake time when threshold voltage shift (\( \Delta V_{TH} \)) reaches at \( \Delta V_{TH,FAIL} \) and lifetime at room temperature (25°C) is obtained by proposed method based on measured
data because it takes a lot of time to measure the lifetime at room temperature.

While showing abnormal behavior of Arrhenius plot, measured lifetime is inconsistent with lifetime extrapolated by conventional method at low temperature range. Actually, $E_a$ is not constant value ($E_{a(HT)} > E_{a(LT)}$). It means that failure mechanism contributing to charge loss is more than one.

![Diagram](image)

**Fig. 2.3.** Lifetime obtained by conventional method (Arrhenius model) and obtained by measured data and proposed method.
To help understanding in next chapter, the following is separation procedure of each mechanism using proposed method. First, for generation A, B, and C, 20 cells were programmed at 3V by incremental step pulse program scheme after 1k cycling (program and erase process). And then, the average $\Delta V_{TH,TOTAL}$ behavior of 20 cells was extracted by $I_{\text{read}}$-$V_{\text{read}}$ curves according to bake time at various temperatures as shown in Fig. 2.4, where threshold voltage ($V_{TH}$) is read voltage ($V_{\text{read}}$) when read current ($I_{\text{read}}$) reaches at 0.1$\mu A$.

![Graph](image)

**Fig. 2.4.** $I_{\text{read}}$ - $V_{\text{read}}$ curves at 210°C on generation A. After 1k cycling, initial $I_{\text{read}}$ - $V_{\text{read}}$ curve was shifted according to bake time.
From the behaviors of average $\Delta V_{TH,TOTAL}$ at various temperatures, we separated $\Delta V_{TH,TOTAL}$ into the amount of charge loss of each failure mechanism. Fig. 2.5 shows behaviors of $\Delta V_{TH,TOTAL}$ and the amount of charge loss of each failure mechanism at the various temperatures. At first, $\Delta V_{TH,TOTAL}$ was fitted by the proposed method with the two stretched exponential functions (the 1\textsuperscript{st} term and the 2\textsuperscript{nd} term) in (2.2) because two convex curves were observed in behavior of $\Delta V_{TH,TOTAL}$ at 210°C. However, a stretched exponential function (the 3\textsuperscript{rd} term) was added since additional convex curve was observed at the low temperature range. Thus, all behaviors of charge loss are re-fitted by proposed method with the three stretched exponential functions. Fig. 2.5 (a), (b), and (c) show $\Delta V_{TH,TOTAL}$ fitted by proposed method and the amount of charge loss of each failure mechanism by considering the 3\textsuperscript{rd} term at 210°C, 180°C, and 150°C. As bake temperature decreases, time-constant ($\tau$) of each failure mechanism increases. In Fig. 2.5 (d), (e), and (f), additional mechanism was observed at 117°C, 85°C, and 55°C. As bake temperature decreases, additional mechanism (the 3\textsuperscript{rd} term) becomes dominant. And then, we extracted $E_a$ of each failure
mechanism, where time-constants ($\tau$) of each failure mechanism were plotted at various temperatures. Three mechanisms were confirmed as detrapping, TAT, and $N_{i}$ recovery mechanism respectively, where extracted $E_a$ compared with $E_a$ on literature. However, we cannot assure whether the 3$^{rd}$ mechanism is $N_{i}$ recovery mechanism or not since the 3$^{rd}$ mechanism has too short time-constant ($\tau_{N_{i}}$) and is mixed with detrapping mechanism at high temperature. In chapter 3, we verified the 3$^{rd}$ mechanism from two experiments.
Two main mechanisms are observed:

(a) Bake temp ↓ ⇒ Time-constant( τ ) ↑

(b) Bake Temp : 210°C

(c) Bake Temp : 180°C

(d) Bake Temp : 150°C

(e) Bake Temp : 117°C

(f) Bake Temp : 85°C

Another mechanism is observed

The 3rd mechanism becomes dominant

Fig. 2.5. Behaviors of $\Delta V_{TH, TOTAL}$ and charge loss separated as the 1st, the 2nd, and the 3rd term at (a) 210°C, (b) 180°C, (c) 150°C, (d) 117°C, (e) 85°C, and (f) 55°C on generation A.
### 2.3. 3D TCAD Simulation

In this section, we investigated the Arrhenius plot behavior for lifetime estimation according to the number of failure mechanisms, the criterion determining failure data ($\Delta V_{TH,FAIL}$) which is 10%, 20%, and 30% of $\Delta V_{TH,TOTAL}$ at 125°C, and proportions of failure mechanisms. And then, we confirmed what failure mechanisms have a dominant effect on lifetime at specific temperature. Sentaurus 3D TCAD simulation was used as simulation tool. Fig. 2.6 shows NAND Flash memory device structure used in simulation which is made of string structure with $WL_{n+1}$, $WL_n$ (target cell), and $WL_{n-1}$ cell to consider virtual source/drain. Gate width, gate length, and cell-to-cell distance are sub 20-nm, tunnel oxide thickness is sub 7-nm, and inter-poly dielectric (IPD) layer thickness is 14-nm as equivalent oxide thickness (EOT). In the simulation, detrapping and trap-assisted tunneling mechanism are only considered for tunnel oxide. To make programmed state ($V_{TH} = 3V$), electrons were injected in floating gate. As shown in Fig. 2.7, for detrapping mechanism, tunnel oxide is filled with
constant trap density (1.8x10^{18} \text{ cm}^{-3}) in all space, trap energy level (E_{\text{C,ox}} - E_{\text{trap}}) from tunnel oxide conduction band is 1eV, electron capture cross section ($\sigma_n$) is 1x10^{19} \text{ cm}^2, and local emission model is used [20]. For trap-assisted tunneling mechanism, there is a single electron trap in the center of tunnel oxide. It has a deep trap level with 3.1eV ($E_{\text{C,ox}} - E_{\text{trap}} = 3.1\text{eV}$) and trap interaction volume ($V_T$) is set to 7x10^{-10} \text{ um}^3. Nonlocal tunneling model is used [20].

Fig. 2.6. NAND Flash memory device structure viewed from side direction. String structure with WL_{n+1}, WL_{n} (target cell), and WL_{n-1} cell is considered due to virtual source/drain.
At first, in the programmed state ($V_{TH}=3\text{V}$), the bit-line, word-line, body were grounded and retention simulation was conducted according to bake time and various temperatures (185°C, 155°C, 125°C, 85°C, 55°C, and 25°C). It was performed for three cases, where the first and the second only include detrapping and TAT mechanism respectively and the third includes detrapping and TAT mechanism together. From the simulation result, lifetime obtained by Arrhenius model and obtained at bake time when threshold voltage shift ($\Delta V_{TH}$) reaches at $\Delta V_{TH,F A I L}$ (10%, 20%, and 30% of $\Delta V_{TH,T O T A L}$ at 125°C) were compared at all
temperatures. And the percentage of mechanism was investigated with proposed method at the given $\Delta V_{TH,FAIL}$ and all temperatures in case that two mechanisms exist together.

Fig. 2.8 (a) and (c) show behaviors of $\Delta V_{TH,TOTAL}$ according to bake time at various temperatures for detrapping and TAT mechanism respectively. $\Delta V_{TH,TOTAL}$ behaviors of detrapping mechanism are more directly dependent on the temperature than that of TAT mechanism.

Fig. 2.8 (b) and (d) show that retention characteristics for each failure mechanism follows Arrhenius model well. Lifetime obtained by Arrhenius model and obtained at bake time when $\Delta V_{TH}$ reaches at $\Delta V_{TH,FAIL}$ corresponds each other. Arrhenius plot is just shifted in parallel according to $\Delta V_{TH,FAIL}$.

Fig. 2.8 (e) indicates Arrhenius plots for each mechanism (detrapping and TAT mechanism) in the same scale. When the both are considered, detrapping and TAT mechanism is dominant at high temperature range and at low temperature range, respectively.

Fig. 2.9 (a) and (b) show that if two or more failure mechanisms exist,
behaviors of $\Delta V_{TH,TOTAL}$ can be expressed as the sum of charge loss of each failure mechanism and abnormal behavior of Arrhenius plot (roll-off phenomenon of $E_a$) is observed. This result shows that retention characteristics cannot be explained anymore by Arrhenius model because dominant failure mechanism is different according to the temperature. When $\Delta V_{TH,FAIL}$ decreases from 30% to 10%, extracted lifetime has large error rate (large roll-off of $E_a$) with lifetime obtained by Arrhenius model at room temperature. To analyze Fig. 2.9 (b) in detail, the proposed method was used to separate $\Delta V_{TH,TOTAL}$ into the amount of charge loss of each failure mechanism according to temperatures. And then, the percentage of mechanism in $\Delta V_{TH,FAIL}$ (10% and 30% of $\Delta V_{TH,TOTAL}$ at 125°C) was analyzed as shown in Fig. 2.9 (c). While the percentage of detrapping mechanism is nearly unchanged at high temperature range regardless of $\Delta V_{TH,FAIL}$, the percentage of TAT mechanism increases by around 100% at room temperature when $\Delta V_{TH,FAIL}$ decreases from 30% to 10%. This result indicates that TAT mechanism becomes more dominant at room temperature. Thus, abnormal behaviors of Arrhenius plots of Fig. 2.9 (b) can be explained.
(a) Detrapping Mechanism

Initial $V_{TH} = 3V$

- $185^\circ C$
- $155^\circ C$
- $125^\circ C$
- $85^\circ C$
- $55^\circ C$
- $25^\circ C$

(b) Detrapping Mechanism

$\Delta V_{TH,FAIL} = \%$ of $\Delta V_{TH,TOTAL}$ at $125^\circ C$

- 10\%
- 20\%
- 30\%

Arrhenius model
(c) TAT Mechanism
Initial $V_{TH} = 3V$

- Orange line: 185°C
- Blue line: 85°C
- Pink line: 155°C
- Red line: 55°C
- Green line: 125°C
- Black line: 25°C

(d) TAT Mechanism
$\Delta V_{TH,FAIL} = \%$ of $\Delta V_{TH,TOTAL}$ at 125°C

- 10% line
- 20% line
- 30% line

**Arrhenius model**
Fig. 2.8. Behaviors of $\Delta V_{TH,\text{TOTAL}}$ according to temperature for (a) detrapping and (c) TAT mechanism. Arrhenius plots according to $\Delta V_{TH,\text{FAIL}}$ for (b) detrapping and (d) TAT mechanism. (e) Arrhenius plots for each mechanism in the same scale.
(a) Detrapping and TAT mechanism

Initial $V_{TH} = 3V$

- $185^\circ C$
- $85^\circ C$
- $155^\circ C$
- $55^\circ C$
- $125^\circ C$
- $25^\circ C$

(b) Detrapping and TAT mechanism

$\Delta V_{TH,FAIL} = \% of \Delta V_{TH,TOTAL}$ at $125^\circ C$

- 10%
- 20%
- 30%

Arrhenius model

$\ln(t_R)$ [a.u.]

$1/kT$ [eV$^{-1}$]
Fig. 2.9. (a) behaviors of $\Delta V_{TH,TOTAL}$ according to temperature. (b) Arrhenius plots according to $\Delta V_{TH,FAIL}$. (c) the percentage of mechanism in $\Delta V_{TH,FAIL}$ when two mechanisms are considered.

In addition, to observe retention characteristics on proportions of failure mechanisms, additional retention simulation was conducted when proportions of two mechanisms (detrapping and TAT mechanism) were changed in $\Delta V_{TH,TOTAL}$ (constant) at 125°C.

Fig. 2.10 (a) indicates Arrhenius plots according to proportions of two mechanisms where $\Delta V_{TH,FAIL}$ is 20% of $\Delta V_{TH,TOTAL}$ at 125°C. When TAT
proportion increases and detrapping proportion decreases in $\Delta V_{TH,TOTAL}$, lifetime becomes slightly longer at high temperature range (185°C-125°C) and considerably shorter at low temperature range (55°C-25°C) inversely. With the proposed method, we exactly confirmed that the percentage of detrapping mechanism decreases and the percentage of TAT mechanism increases at all temperatures, especially at the low temperature range where the amount of variation of mechanisms is the largest as shown in Fig 2.10 (b).
Fig. 2.10. (a) Arrhenius plots and (b) the percentage of mechanism in $\Delta V_{TH,FAIL}$ (20% of $\Delta V_{TH,TOTAL}$ at 125°C) when proportions of two mechanisms are changed in $\Delta V_{TH,TOTAL}$ at 125°C as the reference temperature while maintaining the amount of $\Delta V_{TH,TOTAL}$. 
2.4 Conclusion

We analyzed the behavior of Arrhenius plot and how failure mechanisms have an effect on data retention characteristics in NAND Flash memory cell. Simulation results show that data retention characteristics follows Arrhenius model for a failure mechanism well. However, for two failure mechanisms, abnormal behavior of Arrhenius plot is observed because dominant failure mechanism is different on the temperature. In addition, variation of Arrhenius plots was observed according to $\Delta V_{TH,F_{AIL}}$ (10%, 20%, and 30% of $\Delta V_{TH,TOTAL}$ at 125°C) and proportions of two mechanisms. When $\Delta V_{TH,F_{AIL}}$ decreases and TAT proportion increases in $\Delta V_{TH,TOTAL}$, abnormal characteristics was obviously observed because the percentage of TAT mechanism obtained in $\Delta V_{TH,F_{AIL}}$ increases.
3. Experimental Verifications on $N_{it}$ Recovery Mechanism

3.1 Introduction

In the previous chapter, we introduced the proposed method. And from this method we separated the average $\Delta V_{TH, TOTAL}$ into the amount of charge loss of each failure mechanism ($\Delta V_{TH, Detrap}$, $\Delta V_{TH, TAT}$, and $\Delta V_{TH, Nit}$) according to bake time in test element group (TEG) cells of the advanced NAND Flash memory for different generations (A, B, and C) [10].

In this chapter, we especially focus on the 3rd mechanism ($N_{it}$ recovery mechanism) because the others (detrapping and TAT mechanism) are confirmed as reasonable value when compared with the literature. However, we cannot assure whether the 3rd mechanism is $N_{it}$ recovery mechanism or not since the 3rd mechanism has too short time-constant ($\tau_{Nit}$) and is mixed with detrapping mechanism at high temperature. To verify whether the 3rd mechanism is $N_{it}$
recovery mechanism or not, first, $\Delta V_{TH,Ni}$ (charge loss of the 3\textsuperscript{rd} mechanism) was seperated from the average $\Delta V_{TH,TOTAL}$ for different generations at room temperature where the 3\textsuperscript{rd} mechanism is completely dominant as shown in Fig. 3.1 and Fig. 3.2. And then, two experiments (charge pumping method and $I/f$ noise analysis) were conducted on generation A, B, and C.

![Graph showing $\Delta V_{TH}$ vs. Bake Time]

**Fig. 3.1.** the average $\Delta V_{TH,TOTAL}$ and the amount of charge loss of each mechanism separated by proposed method at room temperature on generation A.
Fig. 3.2. $\Delta V_{TH,Nit}$ extracted by proposed method at room temperature on generation A, B, and C.
3.2 Charge Pumping Experiment

To investigate interface characteristics between Si and SiO₂ (the amount of \( N_a \)) charge pumping experiment was conducted on each generation (A, B, and C). Fig. 3.3 simply shows charge pumping TEG description.

![Charge Pumping TEG Description](image)

**Fig. 3.3.** Charge pumping TEG description.
A number of cells are connected in parallel to make sufficient charge pumping current. And floating gate is short-circuited with control gate. Each of the charge pumping TEG exists on the same generation wafer. It means that charge pumping TEG goes through the same process step with TEG where $\Delta V_{TH, Nit}$ was extracted. Thus, interface characteristics between Si and SiO$_2$ is equivalent. Fig. 3.4 shows basic experimental setup for charge pumping measurement.

![Diagram of experimental setup](image)

**Fig. 3.4.** Basic experimental setup for charge pumping measurement.
Fig. 3.5 shows schematic illustration of the commonly used CP measurement method. It consists of applying a constant reverse bias at source drain, while sweeping the pulse base level from a low accumulation level to a high inversion level. The pulse amplitude \(V_{\text{pulse}}\), the frequency, and rising and falling times of pulse are kept constant. \(V_{\text{pulse}}\) should be sufficient amplitude to cover inversion layer and accumulation layer. By changing the pulse base level \(V_{\text{base}}\) with constant amplitude, maximum value of charge pumping current \(I_{\text{cp, max}}\) is obtained when \(V_{\text{pulse}}\) is greater than threshold voltage \(V_{TH}\) and \(V_{\text{base}}\) is smaller than flat band voltage \(V_{FB}\). And then, charge pumping current \(I_{\text{cp}}\) measured at the substrate is expressed by following equation.

\[
I_{\text{cp}} = q \times f \times A_g \times N_{it} \tag{3.1}
\]

In (3.1), \(q\) is electronic charge (magnitude), \(f\) is frequency of gate pulse, \(A_g\) is the area of \(N_{it}\) contributing to \(I_{cp}\) (channel area of cells connected in parallel), and \(N_{it}\) is the mean interface trap density. Using (3.1), the mean
interface trap density was extracted for generation A, B, and C.

Fig. 3.5. Schematic illustration of the measurement method. By changing the pulse base level $V_{\text{base}}$ with constant amplitude, $I_{cp}$ current is obtained.

Fig. 3.6 shows the extracted mean $N_{it}$ on generation A, B, and C. Among the generation A, B, and C, mean $N_{it}$ of generation C is the largest value followed by generation A and B ($N_{it}$ (C) > $N_{it}$ (A) > $N_{it}$ (B)). This result shows
correlation with the amount of charge loss of the 3\textsuperscript{rd} mechanism ($N_\text{it}$ recovery mechanism) as $\Delta V_{\text{TH},N\text{it}}(C) > \Delta V_{\text{TH},N\text{it}}(A) > \Delta V_{\text{TH},N\text{it}}(B)$. However, extracted $N_\text{it}$ is that of fresh cell (not cycled) because control gate is short-circuited with floating gate. Thus, additional experiment ($1/f$ noise analysis) was conducted to justify the 3\textsuperscript{rd} mechanism as $N_\text{it}$ recovery mechanism.

![Diagram](image)

**Fig 3.6.** The extracted mean $N_\text{it}$ on generation A, B, and C.
3.3 $1/f$ Noise Analysis Experiment

To observe the more accurate tendency of $N_a$, at equivalent condition with previous work, $1/f$ noise analysis was conducted at NAND TEG (not short-circuited between control gate and floating gate) on generation A, B, and C. Extracted $1/f$ noise power spectrum density (PSD) is the mean noise PSD of 6 cells cycled by 1k times. Fig. 3.7 shows basic experimental setup for $1/f$ noise analysis measurement.

![Figure 3.7](image.png)

**Fig. 3.7.** Basic experimental setup for $1/f$ noise measurement.
Fig. 3.8 shows result of $1/f$ noise analysis as noise PSD on generation A, B, and C. For all generations we confirmed that the noise PSD is inversely proportional to frequency and amplitude of the noise PSD of generation C is the largest value followed by generation A and B. This result means that the mean $N_{it}$ for all generations is $N_{it} (C) > N_{it} (A) > N_{it} (B)$ after 1k cycling.

Fig. 3.8. The extracted noise PSD on generation A, B, and C. Amplitude of the noise PSD on generation C is the largest value followed by generation A and B.
3.4 Conclusion

To verify whether the 3rd mechanism is $N_\alpha$ recovery mechanism or not, two experiments (charge pumping method and $1/f$ noise analysis) were conducted on generation A, B, and C. Initial $N_\alpha$ (not cycled cells) was extracted by charge pumping method. Among the generation A, B, and C, mean $N_\alpha$ of generation C is the largest value followed by generation A and B ($N_\alpha$ (C) > $N_\alpha$ (A) > $N_\alpha$ (B)). However, since previous work is carried out in 1k cycled cells, we cannot be sure that result of charge pumping measurement has perfect correlation with it.

To illustrate the more accurate tendency of $N_\alpha$, $1/f$ noise PSD was analyzed at the equivalent condition where $1/f$ noise PSD is the mean noise PSD of 6 cells cycled by 1k times. As a result, amplitude of the noise PSD of generation C is the largest value followed by generation A and B. This result means that the mean $N_\alpha$ for all generations is $N_\alpha$ (C) > $N_\alpha$ (A) > $N_\alpha$ (B) after 1k cyling.
Finally, from two experiments, the amplitude of $\Delta V_{TH,Nit}$ extracted by proposed method on three generations ($\Delta V_{TH,Nit}$ (C) > $\Delta V_{TH,Nit}$ (A) > $\Delta V_{TH,Nit}$ (B)) showed perfect correlation with the results of both CP method and 1/f noise PSD ($N_\mu$ (C) > $N_\mu$ (A) > $N_\mu$ (B)) because the amount of $N_\mu$ is proportional to $\Delta V_{TH,Nit}$. This good agreement with two experiments strongly shows that the 3rd mechanism is $N_\mu$ recovery mechanism.
4. Conclusion

In order to analyze failure mechanisms in detail, 3D TCAD simulation and two experiments were conducted.

To investigate limit of conventional lifetime evaluation method and abnormal behavior of Arrhenius plot for lifetime estimation, retention simulation was conducted for the number of failure mechanisms (detrapping and TAT mechanism). As a result, retention characteristics was determined by dominant mechanism at specific temperature. In addition, the percentage of mechanism was confirmed by proposed method according to $\Delta V_{TH,FAIL}$ and the proportions of two mechanisms at various temperatures. From this result, abnormal behavior of Arrhenius plot was explained.

$N_t$ recovery (3rd) mechanism was verified by charge pumping method and $1/f$ noise analysis. Extracted $\Delta V_{TH,Nt}$ showed perfect correlation with relative $N_t$ extracted by two experiments.
References


[9] K. Lee, M. Kang, S. Seo, et al., “Analysis of failure mechanisms and extraction of activation energies (Ea) in 21-nm NAND flash cells,”


초 록

낸드 플래쉬 메모리 소자의 크기가 매우 작아짐에 따라 (30-나노 이하), 소자 특성에 관련된 신뢰성 문제가 증가하고 있다. 특히, 소자의 전하 손실에 기여하는 다양한 불량 메커니즘으로 인해 보유 특성은 더 이상 기존의 수명 평가 방법으로 설명 할 수 없다. 정확한 수명을 예측하기 위해서, 이전에 세 가지 주요적인 불량 메커니즘 (detrapping, Trap-assisted tunneling, 과 계먼트 램 회복 메커니즘) 기동의 합으로 이루어진 새로운 수명 평가 방법을 제안했 다. 제안된 방법으로, 소자의 세대가 다름 (A, B, 와 C) 향상된 뱈드 플래쉬 메모리에서 총 전하 손실의 양으로부터 \( \Delta V_{TH,TOTAL} \) 각각의 불량 메커니즘의 전하 손실의 양으로 \( \Delta V_{TH,Detrap}, \Delta V_{TH,TAT} \), 과 \( V_{TH,Na} \) 분리 했다.

본 논문에서는 삼차원 시뮬레이션을 이용한 뱈드 플래쉬 메모리에서, 수명 예측을 위한 Arrhenius plot의 기등을 분석하였고, 이에 대하여 불량 메커니즘의 수와 특정한 온도에서 총 전하 손실 양의 비율을 의미하는 불량 데이터를 결정하는 기준을 \( \Delta V_{TH,FAIL} \) 고려 하였다. 보유 시뮬레이션에서,
detrapping 과 trap-assisted tunneling (TAT) 메커니즘 모두 적용된 경우에 대하여, 

\[ \Delta V_{TH,FAIL} \] 이 감소할 때, Arrhenius plot 의 비이상적인 가동이 관찰되었고, 제안된 방법으로 메커니즘 분리하여 비이상적인 가동을 설명하였다. 게다가, 

\[ \Delta V_{TH,TOTAL} \] 의 양에서 TAT 메커니즘의 비율이 detrapping 메커니즘의 비율보다 커짐에 따라, Arrhenius plot 의 비이상적인 특성이 분명하게 관찰되었다. 마지막으로, 소자의 크기가 다른 세대에서 (A, B, 와 C) 추출된 세 번째 메커니즘을 검증하기 위하여, charge pumping (CP) 과 \( I/f \) 노이즈 분석 실험이 수행되었다. 두 실험으로 추출된 상대적인 계면트랩 농도 크기는 세 번째 메커니즘 전하 손실 양의 크기와 완전한 연관성을 보여주었다. 그 결과, 세 번째 메커니즘은 계면트랩 회복 메커니즘으로 검증 되었다.

주요어: 날드 플래쉬 메모리, 불량 메커니즘, Detrapping 메커니즘, TAT 메커니즘, 계면트랩 회복 메커니즘, 보유시간 \((t_R)\).

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