M.S. THESIS

Neuron Circuit Using a Thyristor and Inter-Neuron Connection with Synaptic Device

사이리스터를 활용한 뉴런 회로 및 시냅스 소자와의 연결

BY

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COMPUTER SCIENCE
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지도교수 박 병 국

이 논문을 공학석사 학위논문으로 제출함

2014 년 8 월

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라지브 란잔

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ABSTRACT

For around last two decades the field of neuromorphic engineering has put an endeavor to develop practical neuro-computing devices that mimicked the principles and operations of biological brains, by directly exploiting the physics of electronic devices in mixed analog/digital VLSI system. However, there always was a clamor for a compact electronic system that can mimic the neural network as close as possible.

In this thesis, a simple and compact neuron circuit using a thyristor device has been proposed. The thyristor exhibits bi-stable characteristics when switched between high-impedance, low current OFF-state and low-impedance, high current ON-state with the help of assist circuit can mimic the action potential of the biological neuron. The circuit comprises of six transistor and one capacitor along with a thyristor making it area efficient to be implemented on the chip.

In addition inter-neuron connection circuit with synaptic device has also been presented here. The silicon-based floating-body synaptic device (SFST) is used as synaptic device. The circuit utilizes both short-term and long-term plasticity of the synaptic device as current through the device to transfer it to the post-synaptic neuron. The circuit is capable to keep the conductance of the synaptic device unaffected by the change in input voltage of the post-synaptic neuron.

Keywords: Neuromorphic System, neuron Circuit, thyristor, synaptic device, SFST

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CONTENTS

1. INTRODUCTION

Biological neural systems are highly efficient. The brain in particular, composed of billions of neural cells which when integrated into a brain architecture, can exhibit real-time complex behaviors with high precision while consuming very low power.

Mimicking brain functions and structures is very significant and challenging approach to perform highly intelligent information processing. The interest in building machines to function in dynamic environment has turned many attempts to emulate neural networks that are characterized by parallel processing and low power consumption. In order to build machines

which can function in dynamic environment, much can be learned from the rich temporal behavior of biological neural system. A step in this direction is the construction of model neuronal elements using electronic system which can compute in real time.

The early model of an artificial neuron was introduced by Warren McCulloch and Walter Pitts in 1943 as shown in fig. 1.1. This model has a precise mathematical definition but it only generates a binary output and also the weight and threshold values are fixed. Thus, we need to obtain the neural model with more flexible computational features. The integrate-and-fire neuron model is the most representative model used to build neuron circuit [1]. Fig. 1.2 shows a schematic of an integrate-and-fire neuron. A spike travel down the axon and is transformed by a low-pass filter, which converts the

voltage pulses to current pulse I(t) that charges the capacitor of integrate-and-fire circuit. Once the voltage over the capacitor goes above the threshold voltage, the neuron fires and sends out the output pulse.

The attempts to build a neuron circuit based on “Axon-Hillock” model proposed by Mead [2] has resulted in various integrate-and-fire neuron circuits [3]-[7] earlier. But in these previous work there has always been trade-off between actual size of the circuit and mimicking temporal characteristics of biological neuron : temporal integration, threshold triggering, depolarization, repolarization, hyperpolarization, and refractory period [8].

In chapter 2, structure and characteristics of device of interest; thyristor is explained. The device is known to exhibit bi-stable characteristics which has been utilized to emulate many of the essential temporal characteristics of the

biological neuron.

Chapter 3 is about the description and implementation of the proposed neuron circuit. The thyristor device is switched between the high-impedance, low current OFF-state and low-impedance, high current ON-state with the help of a simple assist circuit to mimic the many of the temporal characteristics of a biological neuron.

In chapter 4, the detail implementation of the inter-connect circuit between neurons using Silicon-based Floating-body Synaptic Transistor [9] as synaptic device has been proposed. The learning mechanism (both short-term and long-term) has been utilized by the inter-connect circuit.

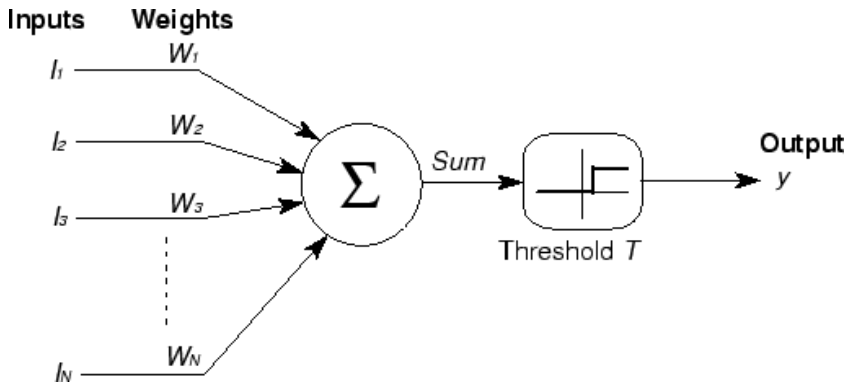

Fig 1.1 (a) McCulloch-Pitts neuron model

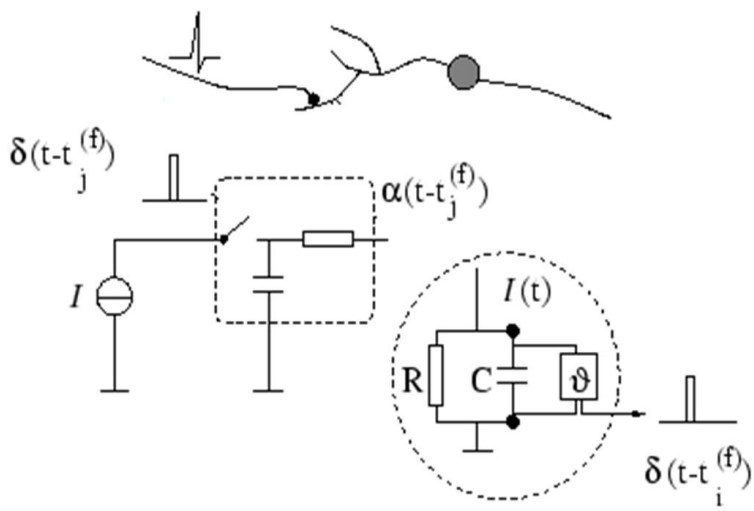

Fig. 1.2 Gerstner and Kistler spiking neuron model [1]

2. Device of Interest: Thyristor

2. 1. DEVICE CHARACTERISTICS

The structure of a thyristor device is shown in Fig. 2.1. It is four-layer p-n-p-n device with junction J_1, J_2 and J_3 in series. Fig. 2.2 shows the current-voltage characteristics of a thyristor having parameter shown in Table 2.1.

The basic I-V characteristics of a thyristor has a number of complex regions as shown in Fig. 2.2. In region 0-1 the device is in the forward blocking or OFF-state with very high impedance. Switching occurs where $dV/dI = 0$, and we define it as switching voltage or threshold voltage of the thyristor. Region 1-2 is the negative resistance region, and region 2-3 is the forward conduction or ON-state [17].

A thyristor operated in the forward region is thus a bi-stable device that can switch from a high-impedance, low-current, OFF-state to a low-impedance, high-current, ON-state, or vice versa.

The depletion-layer widths and voltage drop of a thyristor for the equilibrium, forward OFF-state and forward ON-state are shown in Fig. 2.3 [17]. In equilibrium there is at each junction a depletion region with a built-in potential that is determined by the impurity doping profile in the layers of the thyristor. In forward OFF-state the junction J_2 is reverse biased while the junction J_1 and J_3 will be forward biased. While in ON-state, all the junctions of the device are forward biased. Holes are injected from the P_1 region and electrons from the N_2 region to operate the device like a saturated transistor.

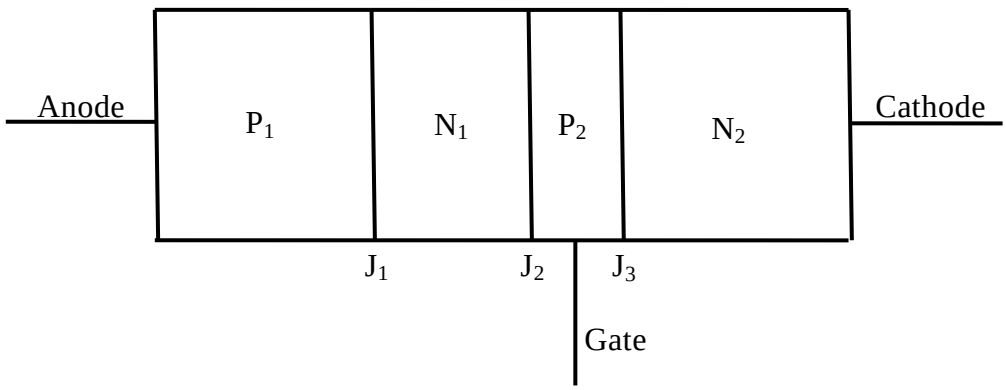

Fig. 2.1 Thyristor device structure showing its junctions and layers

Table 2.1. Device parameters used in the simulation

Layer	Width (μm)	Doping conc.(cm^{-3})
P_1	8	$1x10^{19}$
N_1	6.5	$2x10^{15}$
P_2	2.5	$2.9x10^{17}$
N_2	8	$1x10^{19}$

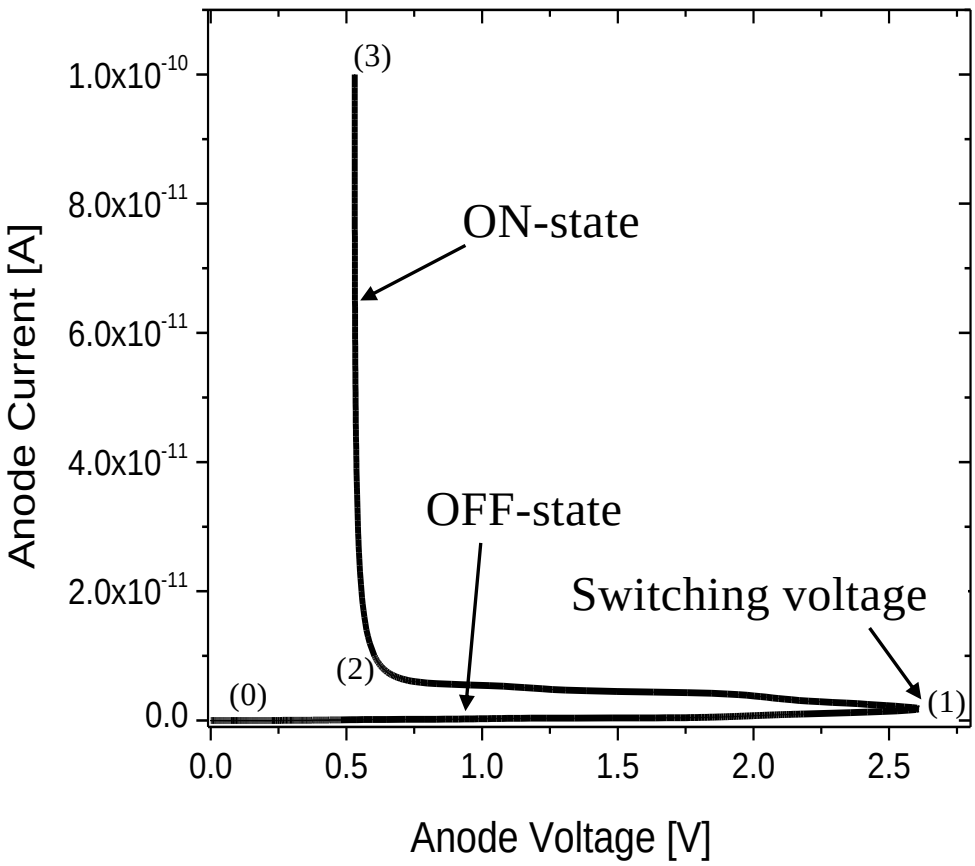

Fig. 2.2 Current-voltage characteristics of a thyristor.

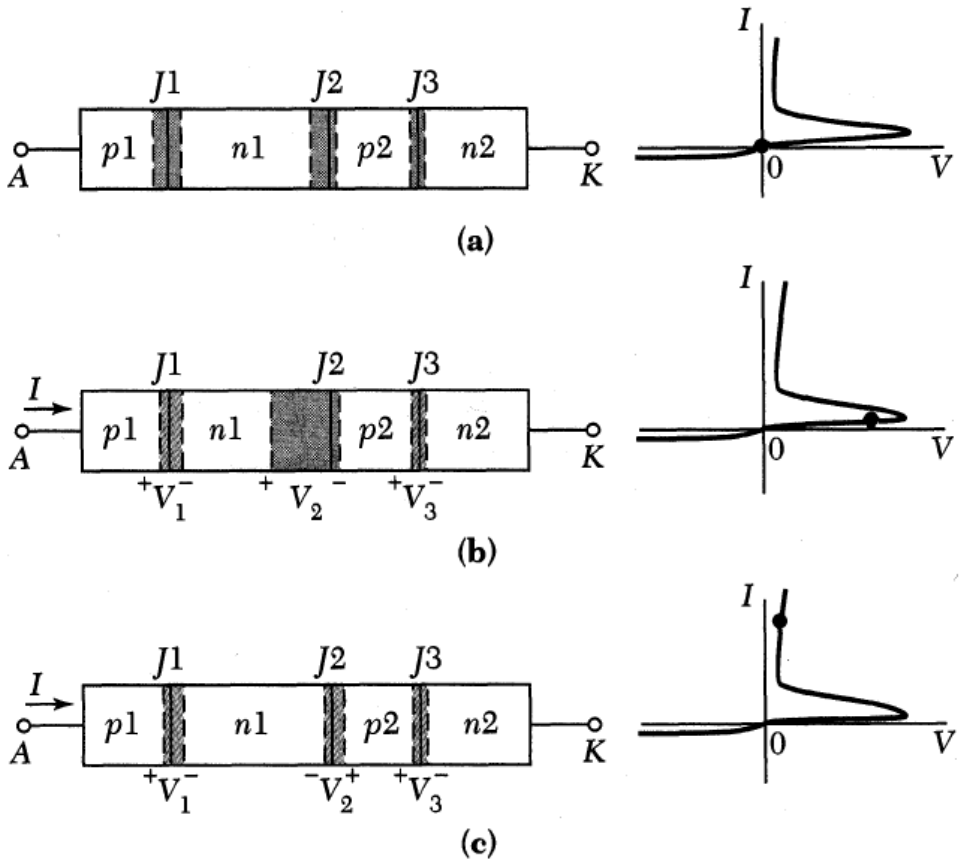

Fig. 2.3 Depletion layer width and voltage drop of a thyristor operated under

(a) Equilibrium (b) Forward OFF-state and (c) Forward On-state [17] .

2. 2 DEVICE OPERATION IN NEURON CIRCUIT

The device initially remain in OFF-state where the middle junction J_2 is reverse biased while the two outer junction of the device, J_1 and J_3 are forward biased. The device is provided integrated input at the anode. The schematic band diagram and charge accumulation in the thyristor just below switching voltage (in the OFF-state) is shown in Fig. 2.4. As the voltage across the device increases to approach its switching voltage, the injection of electrons and holes into the middle reverse biased p-n junction by the outer forward biased p-n junction rapidly increases. The injected carriers sweep across the middle p-n junction and accumulate in the potential wells formed near the outer two p-n junctions. These accumulated charges tends to attract additional charge carriers with opposite polarity from two outermost layers and the

process quickly become regenerative. The accumulation of charges generates an increasing electric field in the middle p-n junction opposite to that of applied field causing it to forward bias and sending thyristor in high current ON-state. This characteristics of the device is utilized in mimicking threshold triggering and depolarization characteristics.

Switching the device back from ON-state to OFF-state causes certain time delay for the junction J_2 to become reverse bias again due to finite recombination time of excess minority carriers in N_1 and P_2 layers of the thyristor, which has been utilized to generate characteristics similar to hyperpolarization state of the action potential.

In order to verify the device operation in neuron circuit, the anode of the device is subjected to integrated or ramp like input and the voltage at the

cathode is sensed. As the voltage reaches the threshold of the device, to turn it ON the voltage at the cathode increases to generate depolarization like characteristics. Then the input at the anode is bring to zero which causes the voltage at the cathode to fall below zero to maintain all the junctions of the device forward-biased due to finite recombination time of the carriers thus generating hyperpolarization like characteristics. Fig 2.5 shows the simulated characteristics at cathode of the thyristor under ramp input to its anode. Fig 2.6 shows the simulated characteristics at the cathode of the thyristor at different temperature showing decrease in threshold voltage of the device by elevating its temperature. The increase in diffusion rate of the carriers from P_1 and N_2 layers of the device by elevating the temperature causes the junction J_2 to get forward biased at the voltage below its room temperature value hence

decreasing its threshold voltage. Fig 2.7 shows the simulated characteristics at the cathode of the thyristor at different recombination time of the carrier showing increase in hyperpolarization duration and slight decrease in turn-on voltage of the thyristor due to increase in carrier recombination time. All the simulations are performed using Atlas Silvaco TCAD simulator.

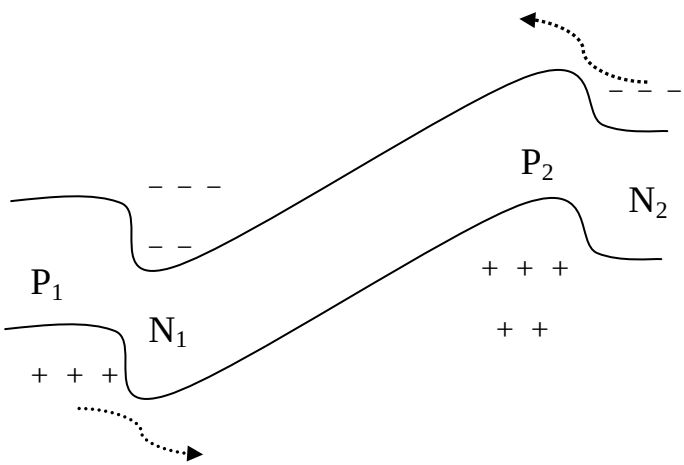

Fig. 2.4 The schematic band diagram and charge accumulation in the thyristor just below switching voltage (in the OFF-state).

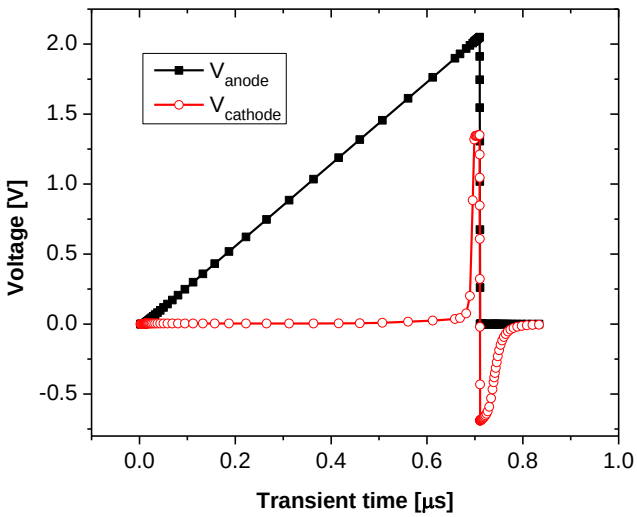

Fig. 2.5 Simulated transient characteristics at cathode of the thyristor device under ramp input to its anode.

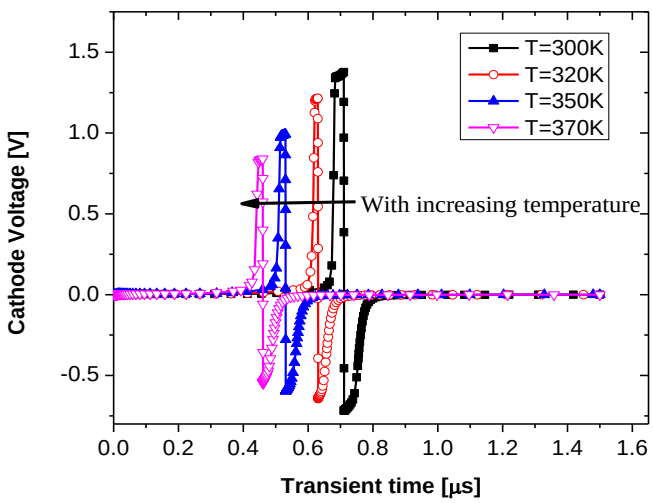

Fig. 2.6 Simulated transient characteristics at the cathode of the device at different temperature.

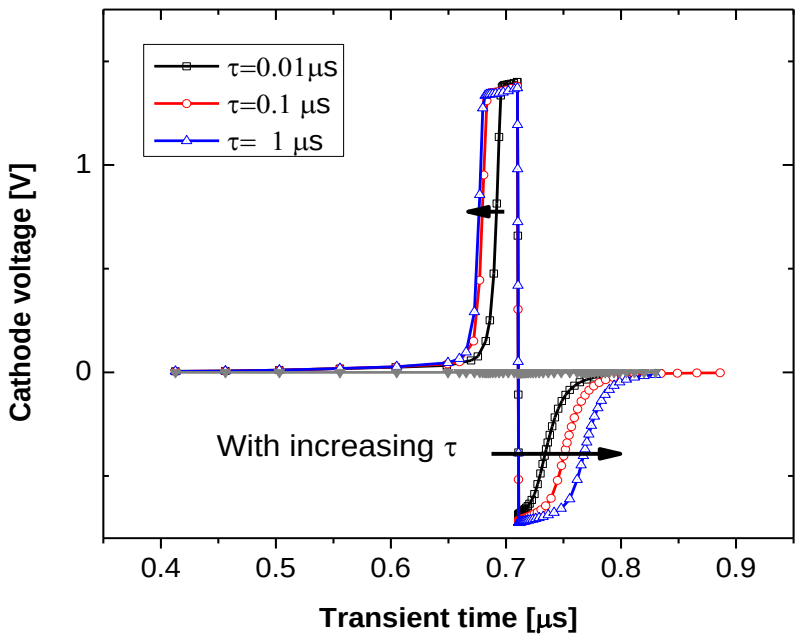

Fig. 2.7 Simulated transient characteristics at the cathode of the device at different carrier recombination time.

3. Neuron Circuit Using a Thyristor

3. 1 CIRCUIT IMPLEMENTATION AND DESCRIPTION

The schematic diagram of the proposed neuron circuit is shown in Fig. 3.1 where the thyristor is used as a two-terminal device with the gate electrode open. The temporal integration of the input current pulse to the neuron occurs on the capacitor C_{mem} to produce the 'membrane potential' V_{mem}. There is a source follower stage comprising of transistors M_1-and-M_2. This source follower stage is deliberately used in the circuit so that it transfers only integrated voltage V_{mem} to the voltage V_2. When the voltage V_2 approaches the switching voltage of the thyristor, it triggers the device into the high current ON-state from the low current OFF-state. As a result of this

triggering at the threshold voltage, the current through the device increases rapidly which is sensed by the transistor M_6 causing voltage V_{out} also to increase rapidly. Thus it mimics the temporal integration and depolarization characteristics of the action potential.

Another source follower stage comprising of transistors M_3-and-M_4 transfers the voltage V_{out} to the voltage V_5 . Increase in the voltage V_5 turn-on the transistor M_5 causing the capacitor C_{mem} to discharge through it, hence bringing the voltage V_{mem} as well as V_2 rapidly to the ground. In-spite of the voltage V_2 which represents the anode voltage of the thyristor dropping to zero, the device does not turn-off simultaneously. As discussed in the previous section, switching the thyristor back into the OFF-state from the ON-state causes a certain time delay for its junction J_2 to become reverse bias again due

to finite recombination time of excess minority carriers in N_1 and P_2 layer of the device. Until these excess minority carriers decay by recombination, the device will remain in ON-state with all its junction forward biased. As a result of this property, the voltage V_{out} drops below zero to maintain all the junctions of the device forward biased and then rises to zero till the excess minority carriers in N_1 and P_2 layers are recombined to bring the thyristor back to OFF-state. Hence it mimics the repolarization and hyperpolarization characteristics of the action potential.

As voltage V_{out} falls, the voltage V_5 is also discharged through transistor M_4 at a rate set by parasitic capacitance at this node and the voltage V_{b2}, which is applied to the gate of the transistor M_4. The fall rate of V_5 is deliberately kept high enough so that the voltage at this node falls relatively

slow as compared to the voltage V_{mem}, V_2 and V_{out}. As long as the voltage V_5 is higher than the threshold voltage of the transistor M_5 , the voltage V_{mem} and V2 are clamped to ground and the neuron cannot spike, as all the input pulse I_{in} is absorbed by the transistor M_5. In this way the circuit is capable of providing refractory period for the generated action potential as well.

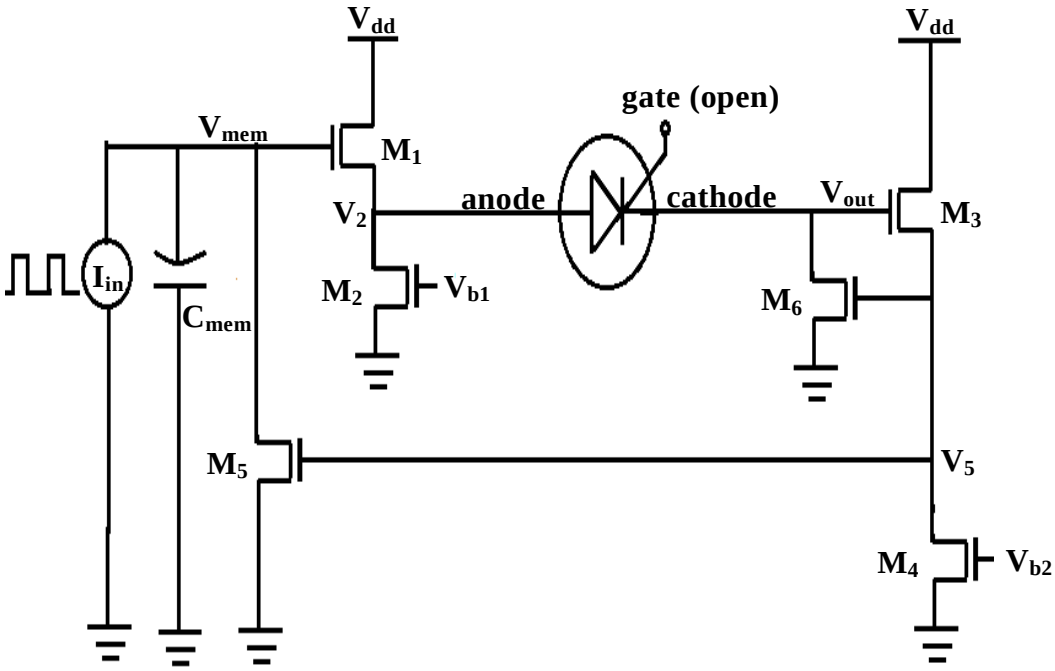

Fig. 3.1 Schematic diagram of the proposed neuron circuit using a thyristor.

3.2 SIMULATION RESULTS

To verify the circuit operation, the proposed circuit in Fig. 3.1 is simulated with ATLAS MIXED-MODE simulator of SILVACO Inc.(ver. Atlas 5.18.3.R). The parameters used for the simulation are: V_{dd} = 2.5V, V_{b1}= 0.4V, V_{b2} = 0.25V, C_{mem}= 20fF with transistors of 0.3 µm-long channel. Fig. 3.2 shows the simulated transient node voltages at all nodes of the circuit where the voltage V_{mem} rises followed by the rise in the voltage V_2 with the input current pulse till it reaches the threshold where the neuron fires. The firing of the neuron voltage pulse V_{out} causes the voltage V_5 to rise due to M_3-and-M_4 source follower stage which turn-on the transistor M_5 causing both V_{mem} and V_2 to drop to ground due to discharge of the capacitor C_{mem}. This causes V_{out} to return back to its resting membrane potential (ground here) after

its hyperpolarization state. But as shown in Fig. 3.2 the voltage V_5 falls relatively slow as compared to V_{mem}, V_2 and V_{out} to provide refractory period for the neuron. Fig. 3.3 shows the detailed transient characteristics of V_{out} which resembles the temporal characteristics of action potential of a biological neuron.

Fig. 3.4 shows the hole concentration in N_1 layer of the thyristor at pre-threshold, depolarized and hyperpolarized and refractory states of the generated action potential where the higher hole concentration in depolarized and hyperpolarized state than pre-threshold and refractory state confirms the finite recombination time for the minority carrier in the device. Similarly Fig. 3.5 shows the electron concentration in P_2 layer of the device at different transient states of the generated action potential. Fig. 3.6 shows the potential

profile in N_1 layer of the thyristor at pre-threshold, depolarized, hyperpolarized and refractory states of the generated action potential. The lower potential barrier in depolarized and hyperpolarized state confirms the device being in ON in these temporal state while higher potential barrier in pre-threshold and refractory state shows the device being OFF in these state.

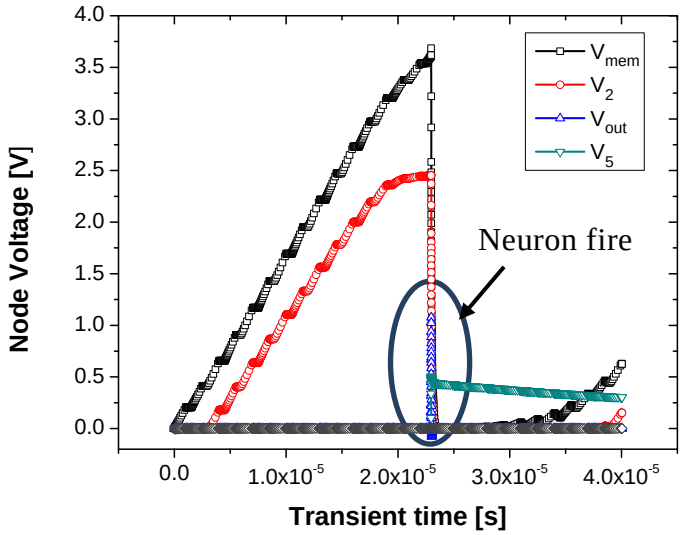

Fig. 3.2 Simulated voltages V_{mem} ,V_2, V_{out} and V_5 as a function of time.

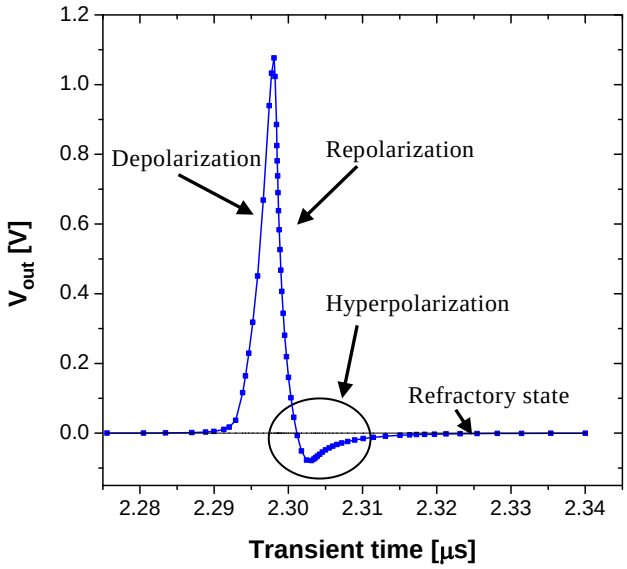

Fig. 3.3 Simulated V_{out} as a function of time where it is mimicking the action potential of a biological neuron.

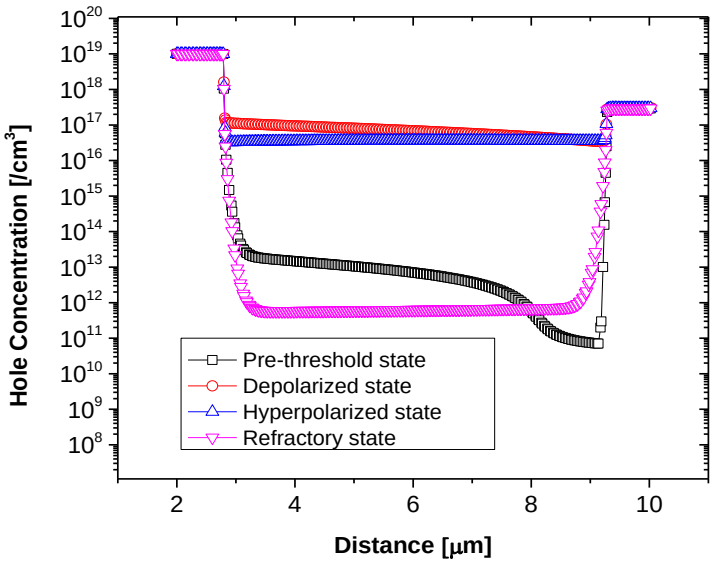

Fig. 3.4 Hole concentration in N_1 layer of the device at different temporal state.

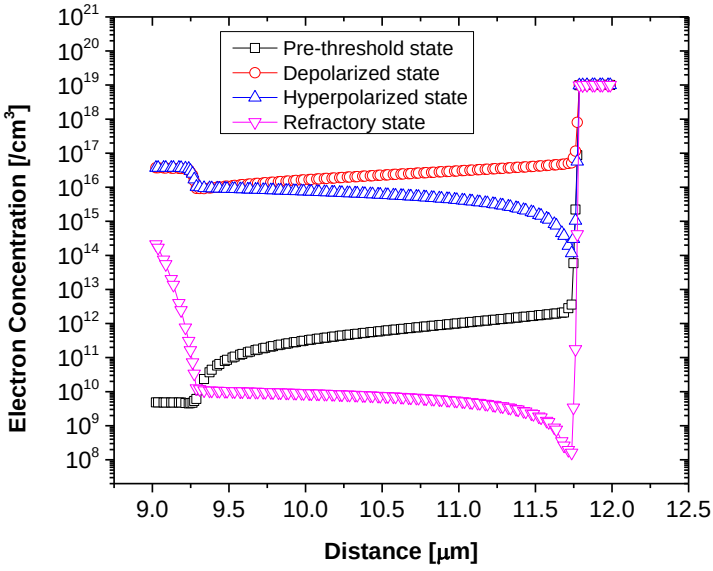

Fig. 3.4 Electron concentration in P_2 layer of the device at different temporal state

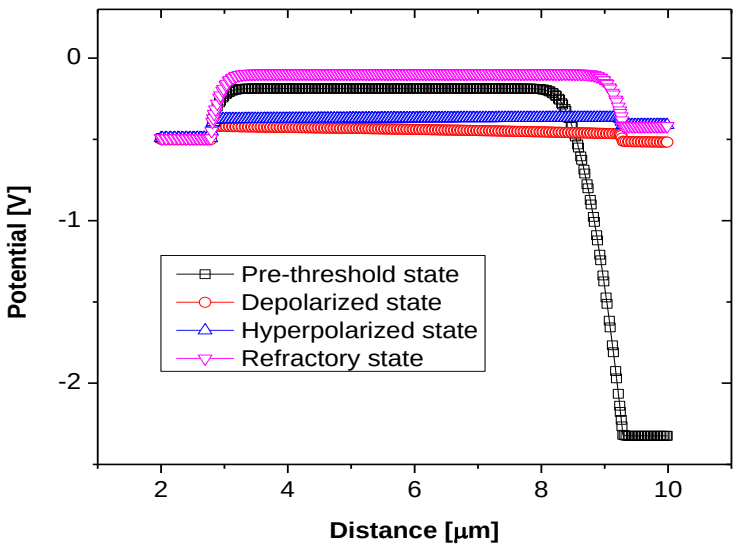

Fig. 3.6 Potential profile in N_1 layer of the device at different temporal state.

3.3 CONCLUSION

In this chapter a neuron circuit using a thyristor has been proposed. The capacitor in the circuit acts as an integrator for the input pulses. The circuit utilizes the bi-stable characteristics of a thyristor to emulate many of the essential temporal characteristics of the biological neuron with very simple and compact circuit, making it area efficient when implemented on the chip.

4. Inter-neuron Connection With Synaptic Device

4. 1 INTRODUCTION OF SYNAPTIC DEVICE

Recent development in neuroscience computation provide evidences that the synapses are not simple interfacing elements for transmitting signal between neurons, but play an important computation role in biological neural network [10]. One of the key properties of biological synapses is their ability to exhibit both short- and long-term plasticity. Short-term plasticity is achieved through the temporal enhancement of a synaptic connection, which then quickly decays to its initial state. However, repeated stimulation causes a permanent change in the connection to achieve long-term plasticity. Fig 4.1

shows the processing flow of Hebbian learning with short-term plasticity (STP) and long-term plasticity (LTP).

There have been various approaches to realize “electrical synapses” with microelectronics technology. The single transistor synapse using floating gate transistor has been proposed [11] but it can mimic only long-term plasticity. The Ag_2S inorganic synapse mimics short- and long-term memories successfully by the incomplete or complete formation of Ag atomic bridge between nanogap [12] as shown in fig 4.2 has also been proposed. But being a non-silicon device it poses difficulty in co-integration with conventional silicon technology. Recently a novel device called “Silicon based Floating-body Synaptic Transistor (SFST) ” [9] has been proposed . Fig 4.3 shows the structure of SFST. It is based on capacitor-less DRAM except the backside

part. By locating the floating gate at backside, SFST is intended to have LTP characteristics as well. When right after the input signal is applied, the excess hole are generated by impact ionization near the surface because of negative V_{cg} which makes potential barrier between source and body. These excess holes are pulled to bottom of silicon and the accumulation of holes results in short-term reinforcement of synaptic weight, which is short-term potentiation (STP) as shown in fig. 4.4 [9] which is similar to the capacitor-less DRAM. The excess hole lowers the potential barrier by the negative V_{cg} causing positive feedback to increase the excess hole generation rate. As a result of the dramatic increase in impact ionization and body hole concentration causes the hot hole injection in floating gate to occur, thus results in long-term potentiation (LTP) as shown in fig. 4.5 [9]. Apart from that the transition from

short-term memory to long-term memory is achieved without any change of bias condition as shown in term of transient body hole concentration in fig 4.6 [9]. Thus SFST is one of the potential synaptic devices for high efficiency, low power consumption and can be fabricated with existing Si technology.

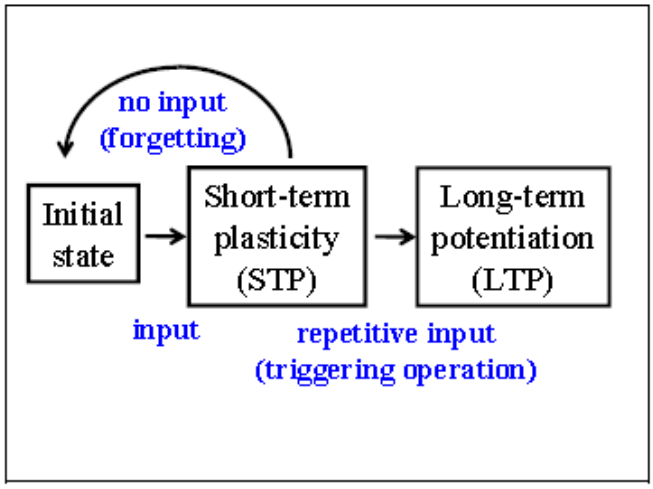

Fig. 4.1 Processing flow of Hebbian learning with STP and LTP.

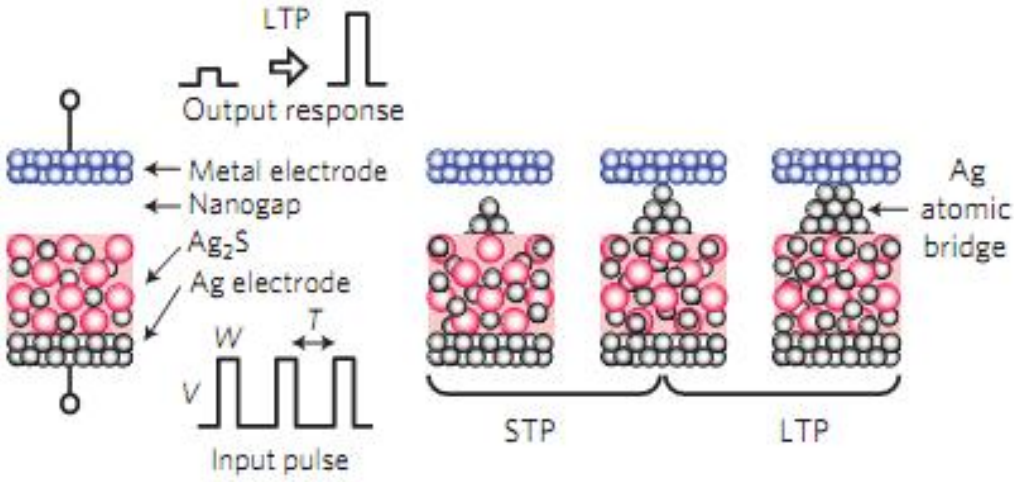

Fig. 4.2 Short- and long-term memory operation of the single inorganic synapses from [12].

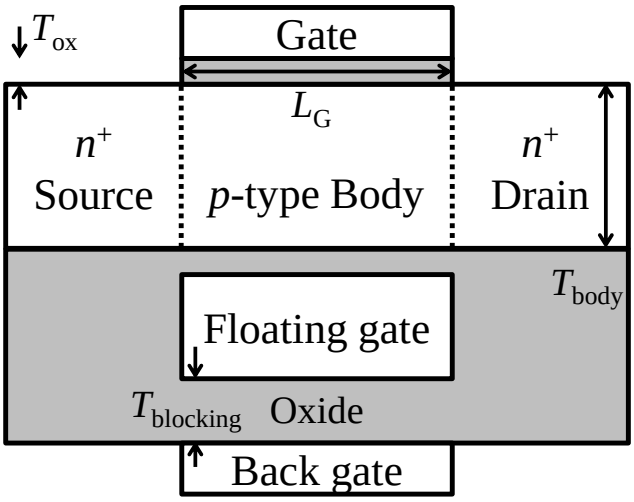

Fig. 4.3 Structure of Silicon-based Floating-body Synaptic Transistor [9]

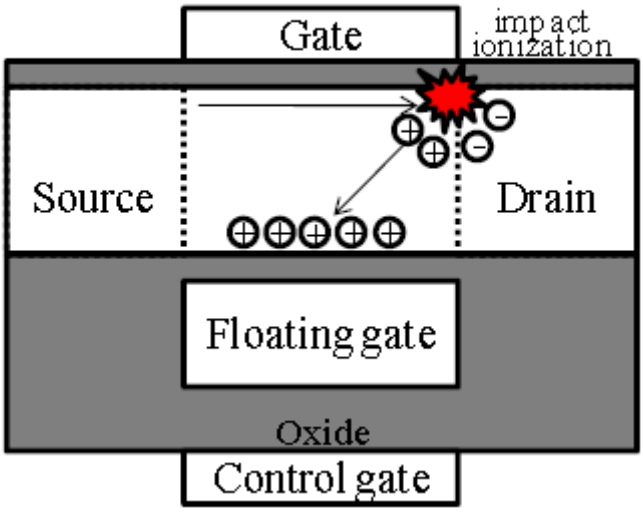

Fig. 4.4 Schematic view of short-term potentiation formation mehanism.[9]

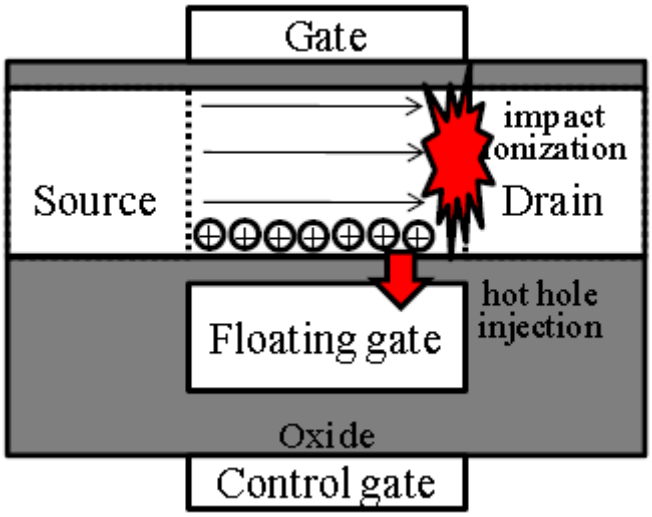

Fig. 4.5 Schematic view of long-term potentiation formation mehanism.[9]

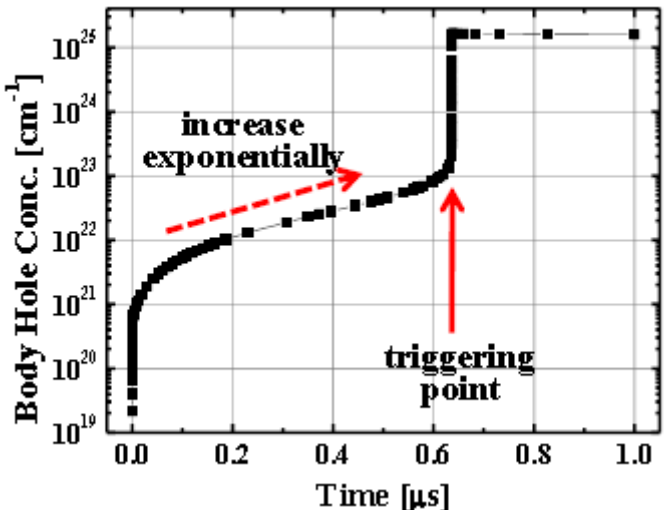

Fig. 4.6 Transient characteristics of body hole concentration.[9]

4. 2 CIRCUIT IMPLEMENTATION AND DESCRIPTION

The schematic diagram for the proposed inter-connect circuit between neurons is shown in fig. 4.7. The silicon-based floating-body synaptic transistor (SFST) is used as synaptic device in the circuit. The pre-synaptic signal V_{pre} is applied at the gate and drain of the synaptic device. The back control gate of the device is connected to negative bias $-V_{ss}$. The synaptic weight is set by the current flowing through the synaptic device to transfer it to the post-synaptic neuron. The generated current pulse from the device is transferred as current pulse input I_{in} to the post-synaptic neuron with the help of intermediate current mirror circuit comprising of transistor M_1-M_2 and M_3-M_4.

The holes are accumulated in the floating body of the synaptic transistor with the subsequent pre-synaptic input to it which decreases its threshold voltage and increases its current drivability. This temporal enhancement of the synaptic weight is similar to the short-term potentiation property of the biological synapse [13].

With further input to the synaptic device, the hot-holes are injected in the floating gate of the synaptic transistor with back control gate bias -Vss which dramatically increases the body-hole concentration resulting in the transition from short-term potentiation to long-term potentiation in the synaptic device.

One of the significant aspect of the intermediate current mirror circuit should be to keep the conductance of the synaptic device independent of post-

synaptic neuron ‘membrane potential’ V_{mem}. This intermediate circuit comprising of double current mirror circuit. The aspect ratio of the transistor M_1 is kept high enough to keep the change in the source voltage V_p of the synaptic device inconsiderable while transition from STP to LTP so that it does not hamper operation of synaptic device. Along with that the intermediate circuit can shield the pre-synaptic neuron from post-synaptic neuron while transferring signal through the same thus maintaining the synaptic conductance independent of V_{mem}.

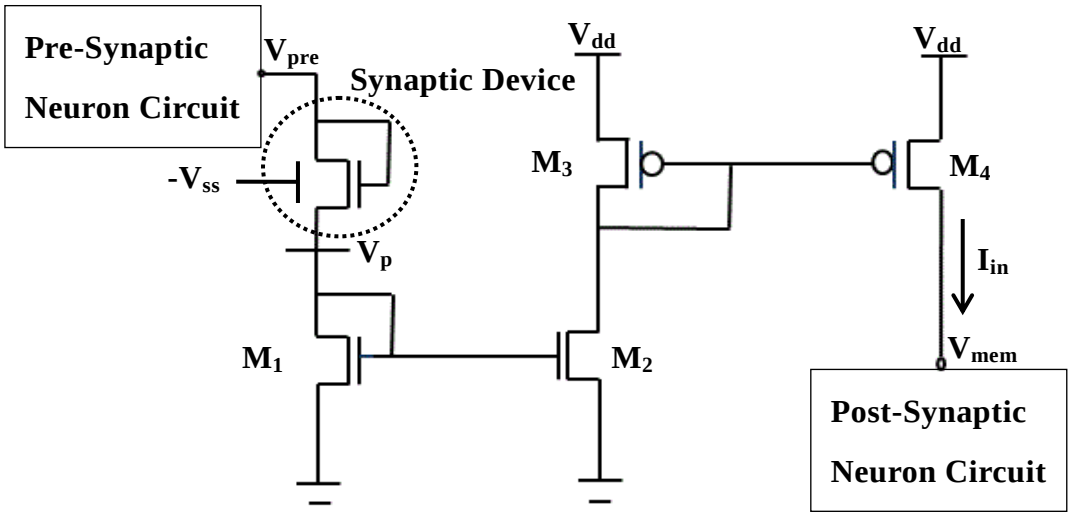

Fig. 4.7 Schematic diagram of the inter-neuron connection circuit with SFST as synaptic device.

4. 3 SIMULATION RESULTS

To verify the circuit operation the proposed circuit in fig. 4.7 is simulated with MIXED-MODE simulator of SILVACO Inc.(ver. Atlas 5.18.3.R) having parameters as: Vdd = 2.5V with transistors of 0.3 µm-long channel. Fig. 4.8 shows the simulated I_{in} as a function of time, showing enhancement in synaptic conductance in the presence of pre-synaptic input V_{pre} , while returning to the same conductance level in its absence, which is similar to short-term learning (potentiation) characteristics of the biological synapse. Fig 4.9 shows the simulated I_{in} as a function of time when pre-synaptic input is continuously applied to the synaptic device where the device undergoes transition from short-term potentiation to long-term term potentiation. The current through the device also shows similar transition

which is transferred to the post-synaptic neuron. Fig. 4.10 shows the charge stored in the floating gate of the synaptic device as a function of time. The hole injection in the floating gate of the device which causes its transition from STP to LTP is evident from this graph. Fig 4.11 shows the transient characteristics of the source voltage V_p of synaptic device having change inconsiderable to effect device operation. Fig 4.12 shows the transient characteristics of V_p and V_{mem} with different value of C_{mem} : 5fF, 10fF and 20fF in which V_p shows no change with the change of V_{mem} at different C_{mem} values hence showing the capability of the intermediate circuit to keep synaptic conductance unaffected by the change in post-synaptic neuron circuit.

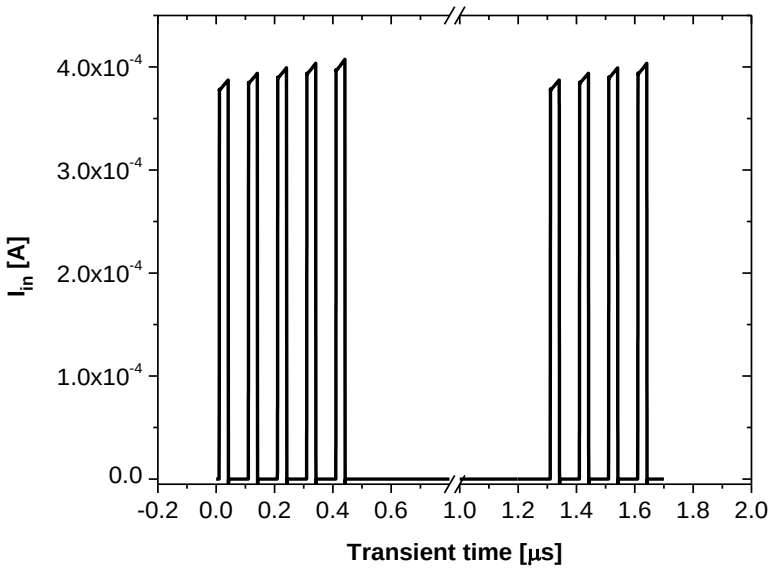

Fig. 4.8 Simulated I_{in} as a function of time showing temporal enhancement due to synaptic device.

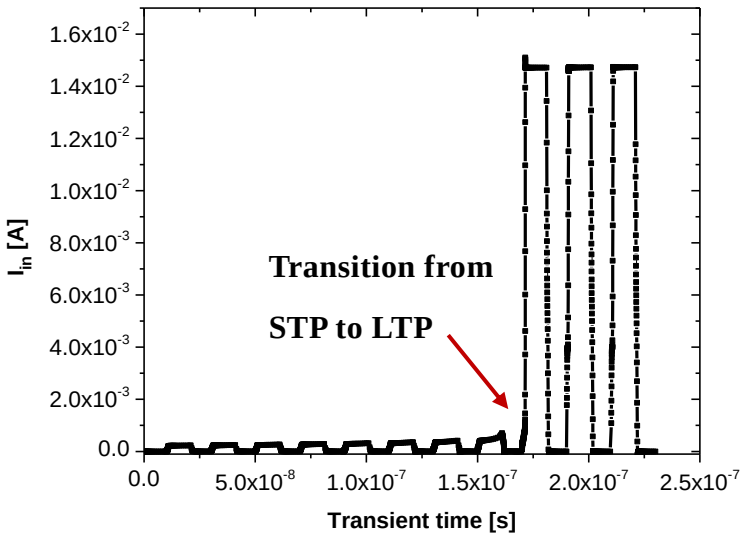

Fig. 4.9 Simulated I_{in} as a function of time showing transition from STP to LTP.

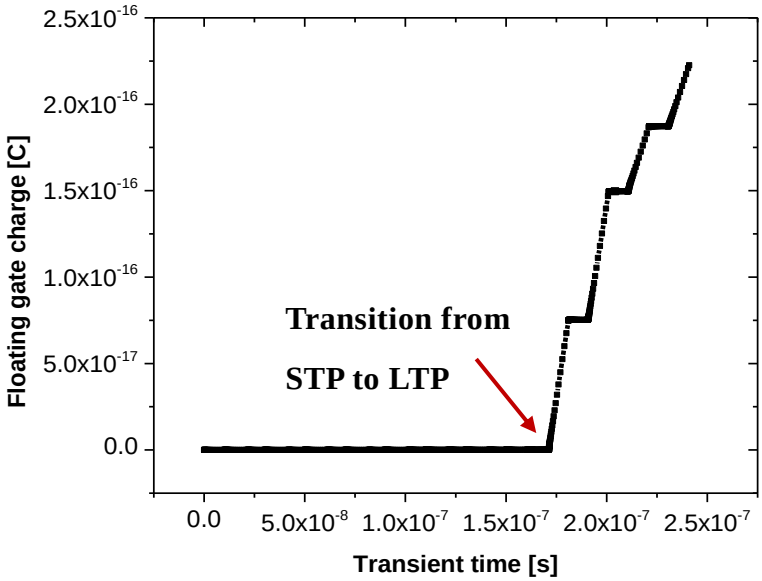

Fig. 4.10 Floating gate charge of the synaptic device as a function of time showing transition from STP to LTP due to hole injection in it.

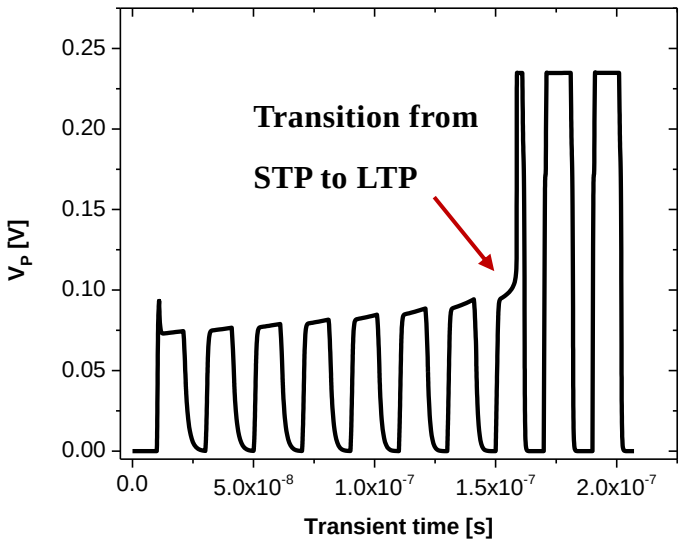

Fig. 4.11 Source voltage of the synaptic device as a function of time showing inconsiderable change while transition from STP to LTP.

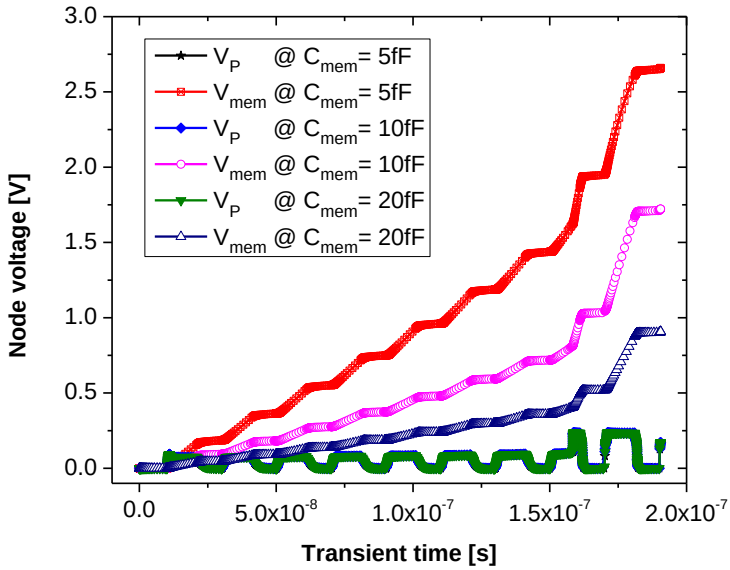

Fig. 4.12 Node voltage V_p and V_{mem} as a function of time at different C_{mem} value showing no change in V_p with the change in V_{mem}

4. 4 CONCLUSION

In this chapter the inter-neuron connection circuit using SFST as synaptic device has been proposed. The short-term plasticity by hole accumulation in the floating body of the device and long-term plasticity by the hole injection in floating gate of the device has been utilized by the inter-connect circuit. The circuit transfers current from pre-synaptic to post-synaptic neuron through the intermediate current mirror which keep the conductance of the synaptic device unaffected by the change in 'membrane potential' V_{mem} of the post-synaptic neuron. Thus the intermediate circuit is capable to keep synaptic conductance unaffected by it.

5. Conclusion

As conventional electronic system from Von Neumann has reveled limitations in terms of cost and efficiency, the need to introduce the new paradigm in information processing evolves the area of neuromorphic system. The neuromorphic system based on neurons enable parallel and adaptable information processing with high efficiency and low power consumption. But there has always been a trade-off between how closely the biological neural elements can be mimicked and number of components to be used in the electronic system.

This work successfully implemented a neuron circuit by utilizing the bi-stable characteristics of a thyristor device to emulate many of the essential temporal characteristics of the biological neuron with very simple and compact circuit, making it area efficient when implemented on the chip.

In addition the inter-connect circuit between neurons using SFST as synaptic device has also been implemented. The circuit utilizes both short-term and long-term potentiation characteristics of the synaptic device and keep the conductance of the synaptic device unaffected by the change in the ‘membrane potential’ of the post-synaptic neuron.

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초 록

지난 이십여 년 동안 뉴로모픽 공학은 아날로그/디지털 VLSI 시스템의 전자 소자들의 동작원리를 직접적으로 활용하여, 생물학적인 뇌의 원리와 동작을 모방한 실질적인 뉴로-컴퓨팅 소자를 개발하기 위한 노력을 해왔다. 그러나 이러한 뉴런 네트워크를 실제와 최대한 가깝게 모사한 간결한 전자 시스템의 개발에 있어서는 항상 여러 의견들이 있어왔다.

본 논문에서는, 사이리스터를 이용한 간결한 뉴런 회로가 제시되었다. 본 논문에 사용된 사이리스터는 높은 임피던스 및 낮은 전류의 꺼짐 상태와 낮은 임피던스 및 높은 전류의 켜짐 상태를 번갈아가며, 주변 보조 회로들의 도움을 받아 생물학적인 뉴런의 활동전위를 모방하였다. 뉴런 회로는 칩 위에 제작되었을 때의 공간상의 효율을 고려하여 총 6개의 트랜지스터 및 한 개의 축전기로 구성되었다

추가적으로 본 논문에서는, 뉴런과 시냅스 소자와의 내부 연결회로가 제시되었다. 실리콘 기반의 플로팅-바디 시냅스 소자가 시냅스의 역할을 수행하였으며,

연결 회로는 시냅스 소자의 단기, 장기 가소성이 반영된 소자 내부 전류를 다음의 후-시냅스 뉴런으로 전달하였다. 연결 회로는 시냅스 소자의 전도성이 후-시냅스 뉴런의 입력전압이 변화하는 것에 영향을 받지 않도록 설계되었다.

주요어 : 뉴로모픽 시스템, 뉴런 회로, 사이리스터, 시냅스 소자, 실리콘 기반의 플로팅-바디 시냅스 소자

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