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이학박사학위논문

**Carrier modulation of BaSnO₃ via field effect
with various gate oxides and their interfaces**

전계 효과를 통한 BaSnO₃의 운송자 변조와
인터페이스에 대한 연구

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Carrier modulation of BaSnO₃ via field effect with various gate oxides and their interfaces

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“Ask and it will be given to you; seek and you will find; knock and the door will be opened to you. For everyone who asks receives; he who seeks finds; and to him who knocks, the door will be opened.”

[Matthew 7:7-8]

SEOUL NATIONAL UNIVERSITY

Abstract

Department of Physics and Astronomy

Doctor of Philosophy

Carrier modulation of BaSnO_3 via field effect with various gate oxides and their interfaces

By Chulkwon Park

The oxide materials were generally believed as one of the most promising materials for the electronic industry due to its exceptional novel characteristics such as high optical transparency and high electrical conductivity compared to conventional materials such as metals or ceramics. In fact, $\text{Sn:In}_2\text{O}_3$, Cu_2O , ZnO , $\text{In}_2\text{O}_3\text{-ZnO}$, $\text{In}_2\text{O}_3\text{-Ga}_2\text{O}_3$, $\text{In}_2\text{O}_3\text{-Ga}_2\text{O}_3\text{-ZnO}$ have been widely investigated and used as transparent conducting oxides and transparent oxide semiconductors.

Additionally, during the past few decades, perovskite oxides such as $\text{YBa}_2\text{Cu}_3\text{O}_7$, $\text{Pb}(\text{Zr}_x\text{Ti}_{1-x})\text{O}_3$, and SrTiO_3 with ABO_3 formula have received a large amount of attention due to their diverse properties such as superconductivity, high-k dielectrics, ferromagnetic, photoconductivity and ferroelectricity. Many researchers have already demonstrated field effect transistors based on perovskite oxide materials in a metal-insulator-semiconductor heterostructure, which is a most fundamental component in oxide

electronics. But even though the field effect transistor devices based on SrTiO₃ and KTaO₃ were already demonstrated, it was impossible to achieve the high performance shown in devices based on binary oxides, due to their poor electron transport properties. Moreover, their lack of oxygen stability limited their applications.

Recently, BaSnO₃ has attracted large attention for many researchers due to its excellent properties compared with the materials mentioned above: the oxygen stability even at high temperatures, and the high electrical mobility at room temperature. BaSnO₃ has a wide band gap with an optical band gap of 3.1 eV. La-doped BaSnO₃ single crystals and thin films have a mobility value of about 300 cm²V⁻¹s⁻¹ and 70 cm²V⁻¹s⁻¹, respectively. It is known that the origin of the difference in mobility between single crystals and thin films is due to the existence of dislocation scatterings or grain boundaries in thin films. The oxygen diffusion constant of BaSnO₃, evaluated by high temperature conductivity measurements, is determined to be 10⁻¹⁵ cm²s⁻¹. Its value is lower than manganites, cuprates, and titanates by 3 ~ 10 orders-of-magnitude. By using these novel properties, the author performed carrier modulations of BaSnO₃ via field effect with amorphous and epitaxial gate dielectrics.

To obtain the appropriate channel layer properties, the author firstly investigated the influence of buffer layers, which is known to be able to reduce the dislocation density on La-doped BaSnO₃ and improve the electrical transport. This is because the dislocations act as a defect (the source of charge traps or scattering centers) on the interface between BaSnO₃ and the dielectric gate oxide. The author chose Al₂O₃ and HfO₂ as gate dielectrics among the many amorphous gate dielectric candidates such as ZrO₂, Y₂O₃, Ta₂O₅, TiO₂. The author also investigated the dielectric properties of Al₂O₃ and HfO₂, namely the breakdown field and dielectric constant. Furthermore, the author demonstrated a field effect transistor made with an undoped buffer layer of BaSnO₃ on a SrTiO₃ substrate using a lightly La-doped BaSnO₃ channel, with the gate dielectrics as Al₂O₃ and HfO₂. The performances of these devices, such as field effect mobility

and $I_{\text{on}}/I_{\text{off}}$ ratio are consistent with the known material parameters of La-doped BaSnO_3 , Al_2O_3 and HfO_2 . And they also provided further evidence for the perfect surface quality of La-doped BaSnO_3 and its stability. Through comparison with SrTiO_3 or KTaO_3 based field effect transistor devices, the author concluded again that these performances are evidences of the superior material properties of BaSnO_3 , and show the potential of BaSnO_3 as a core material in a transparent, high-mobility field effect transistor device.

To further enhance the performance of the device, the author used epitaxial gate dielectrics. Among the epitaxial gate dielectric candidates, such as SrZrO_3 , BaZrO_3 , SrHfO_3 , SrSnO_3 , the author chose LaInO_3 and BaHfO_3 . Also, the author investigated the crystallinity and dielectric properties of these materials by X-ray diffraction and electrical measurements. Then, the author demonstrated field effect transistors using the chosen materials. Overall, the performance of the devices was improved by using epitaxial gate dielectrics. Especially, a remarkable performance was achieved in $\text{LaInO}_3/\text{La-doped BaSnO}_3$ devices. It is comparable with the performance of devices using binary oxides such as ZnO , In-Ga-Zn-O and SnO_2 . Additionally, during the fabrication of the devices, the author observed the sheet conductance enhancement of the La-doped BSO active layer in the $\text{LaInO}_3/\text{La-doped BaSnO}_3$ interface. The author believes a 2-dimensional electron gas is formed at its interface. To explain the origin of this phenomenon, the author investigated the La concentration dependence of BSO, the thickness dependence of LaInO_3 , the possibility of La diffusion, and the oxygen vacancy on the $\text{LaInO}_3/\text{La-doped BaSnO}_3$ interface. The author believes that these investigations on the $\text{LaInO}_3/\text{BaSnO}_3$ interface provide a better understanding of the origin of the 2DEG phenomena at the interface between two-band insulators.

Keywords: Transparent conducting oxide, Transparent semiconductor oxide, Perovskite oxide, BaSnO₃, Wide band gap, Oxygen stability, High electrical mobility, Field effect transistor, Oxide interface

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Chapter 1

Introduction

1.1 Oxide electronics

The oxide materials have gained a large amount attention during the past decade due to their exceptional properties such as high transparency in the visible spectrum region and high electrical conductivity compared to existing materials such as metals and ceramics. Based on these novel properties, oxide materials have been widely investigated and used as transparent conducting oxides (TCO) and transparent oxide semiconductors (TOS) in applications such as flat panel displays, transparent displays, light emitting diodes, touch panels, and solar cells. The names and properties of typical TCO and TOS materials are shown in the table 1. Sn doped Indium Oxide (ITO) is the most famous and widely used TCO in the semiconductor industry. However, the scarcity of Indium compounds demands an effort to find alternative materials. ZnO and SnO₂, the most well-known alternatives, have been investigated as candidate

materials. These two materials have been investigated as TOS candidate materials as well. Based on their superior electrical properties, many researchers have tried to demonstrate electronic devices such as FETs and p-n junctions using these materials. Many examples of FET devices based on various active layers such as ZnO, SnO₂, TiO₂, and Zn-Sn-O have been previously reported [13-21]

Material	E_{gap} (eV)	σ ($\Omega \text{ cm}$) ⁻¹	n (cm ⁻³)	μ (cm ² V ⁻¹ s ⁻¹)	Reference
ZnO:Al	3.2 – 3.4	3.3×10^3	$2.0\text{--}8.0 \times 10^{20}$	35	[1]
ZnO:Ga		25–800	$0.13\text{--}9.53 \times 10^{19}$	120.5–51.1	[2]
ZnO:Mg		0.63	9×10^{15}	440	[3]
ZnO		0.43	2.7×10^{16}	100	[4]
		1.15×10^3	5×10^{20}	36	[5]
ZnO:N		0.025	9×10^{16}	2	[6]
ZnO:As		2	4×10^{17}	35	[7]
SnO ₂ :Ta	3.6 – 4.3	$\sim 6 \times 10^3$	5.7×10^{20}	60	[8]
SnO ₂ :W		$\sim 3 \times 10^3$	2.1×10^{20}	84	[9]
SnO ₂ :F		2×10^3	5×10^{20}	23	[10]
In ₂ O ₃ :Sn	3.75	5×10^3	6.6×10^{20}	47	[11]
In ₂ O ₃ :W		3.1×10^3	2.9×10^{20}	66	[12]

Table 1. Typical optical and electrical properties such as energy band gap (E_{gap}), conductivity (σ), carrier density (n), electron/hole mobility (μ) for TCO and/or TOS candidate materials such as ZnO, In₂O₃, and SnO₂ measured at room temperature. [1-12]

Especially, Hosono group reported results on flexible transparent thin film transistors (TFTs) based on single crystalline In-Ga-Zn-O(IGZO) and amorphous IGZO. With the publication of other backing articles, these results have gained a significant amount of interest from both academia and industries for their possible application to active matrix liquid crystal displays (AMLCDs). [22-25] However, ZnO-related IGZO shows poor oxygen stability. Considering the reliability of device, we need to find an oxygen-stable material. In the next

section (1.2), the author will show an alternative candidate material, perovskite BaSnO_3 (BSO).

Additionally, oxide materials such as Al_2O_3 , HfO_2 , ZrO_2 , La_2O_3 , Y_2O_3 , have been investigated as gate dielectric materials instead of silicon oxide in the conventional silicon-based industries. In Chapter 4 and 5, oxide gate dielectrics will be mentioned in more details.

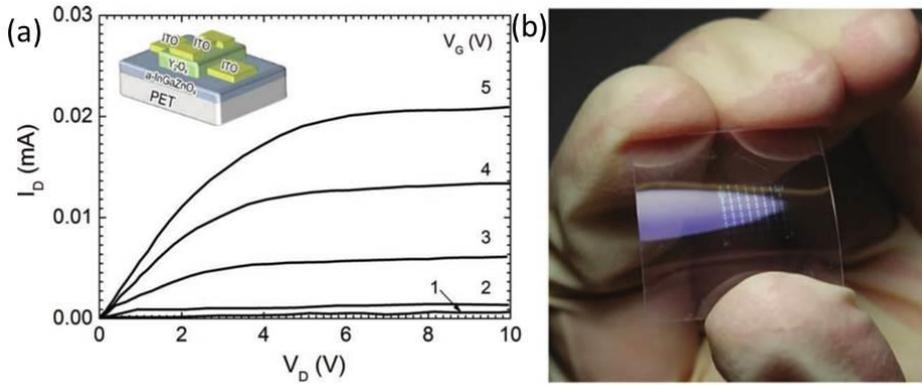


Figure 1. 1. (a) Output characteristics of a flexible substrate with transparent a-IGZO TFTs (b) photograph of the flexible TFT. [23]

1.2 Perovskite oxide

An ideal perovskite oxide has a cubic structure, and has the ABO_3 stoichiometry, where “A” and “B” are cations and “O” is an anion. As shown in Fig. 1. 2., its crystal structure can be described as consisting of corner-sharing BO_6 octahedrons (small cation B within oxygen octahedral) with 12-fold coordinated larger A cations with oxygen. The variety of charges of A and B cations can be represented in three ways, $\text{A}^{1+}\text{B}^{5+}\text{O}_3$, $\text{A}^{2+}\text{B}^{4+}\text{O}_3$, and $\text{A}^{3+}\text{B}^{3+}\text{O}_3$.

The perovskite oxides have received a large amount of attention from many researchers due to their diverse and interesting properties such as

superconductivity, high-k dielectric constant, ferroelectricity, ferromagnetism, photoconductivity, nonlinear optical properties and many more, over a wide range of temperatures. For example, YBCO($\text{YBa}_2\text{Cu}_3\text{O}_7$) plays a dominant role in the high- T_c -superconductor research field.[27-30] To replace magnetic core memory, magnetic bubble memory, and electrically erasable read-only memory, titanates such as BaTiO_3 and $\text{Pb}(\text{Zr}_x\text{Ti}_{1-x})\text{O}_3$ have been investigated for their ferroelectric and/or piezoelectric properties, and have been successfully used in ferroelectric field effect transistor (FeFET)s devices.[31-35] Doped rare-earth manganites such as $A_{b_x}\text{Ca}_{1-x}\text{MnO}_3$ ($A_{b_x} = \text{La}, \text{Nd}, \text{Y}, \text{and Gd}$) are investigated for their colossal magnetoresistance. [36-38]

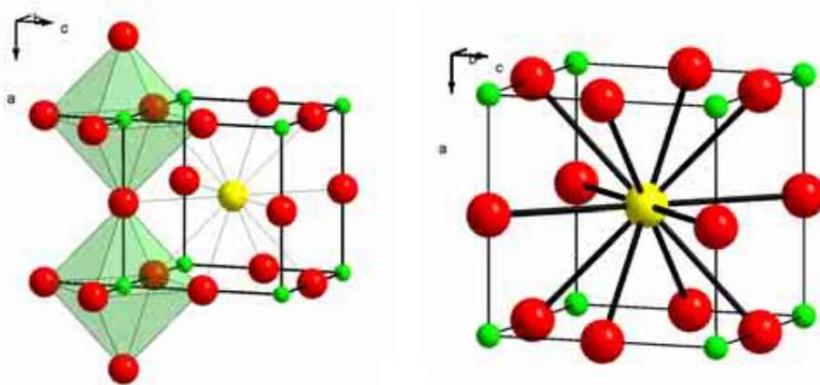


Figure 1. 2. Ideal cubic perovskite structure of ABO_3 . Ideal cubic perovskite has (a) a net corner sharing BO_6 octahedron with (b) 12-fold coordinated A cation with oxygen.[26]

Beside them, LiNbO_3 and $(\text{Li};\text{La})\text{TiO}_3$ are investigated in optical switch and battery material researches, respectively. [39-40] SrTiO_3 and KATiO_3 have been investigated as candidate TOS materials. The demonstration of FETs devices have been pursued using various gate oxide such as Al_2O_3 , CaHfO_3 , and DyScO_3 [41-45]. Although the researchers have made efforts to enhance the interface properties between the active layer and gate dielectric by changing the gate dielectric and/or using epitaxial gate dielectric/amorphous gate dielectric stacks, the devices still showed low field effect mobility, even though a sufficient

carrier modulation of the active layer was possible. These results are related to poor electrical transport properties and oxygen instability of the active layer materials. Recently, BSO was discovered as candidate material corresponding to a demand of a new TOS material, due to its noble properties such as its superior electrical properties and oxygen stability. During the last few decades, BSO has been investigated for its use in thermally stable capacitors, gas sensors, high-k dielectrics, and more. [46-52] It is well-known that BSO has a wide band gap with an optical band gap of 3.1 eV. Recently, the possibility of electron-doped BSO was predicted as a TCO and/or TOS material. The predicted effective mass of BSO was in the range of 0.05 to 1.463 (m^*/m_0) depending on calculation methods.[54, 134-137] When we consider the relation between the mobility, effective mass, and average relaxation time, we can expect high electrical transport properties in BSO.

$$\mu = e\bar{\tau}/m^* \dots\dots\dots(1)$$

where e , $\bar{\tau}$, and m^* are the elementary charge, average relaxation time, and carrier effective mass, respectively. In fact, H. J. Kim *et al.* reported the superior electrical transport property of La-doped BSO in 2012. [53-54] In the range of $10^{19}\sim 10^{20}/\text{cm}^{-3}$ carrier density, BLSO single crystals and thin films show mobility values of about $300\text{cm}^2\text{V}^{-1}\text{s}^{-1}$ and $70\text{cm}^2\text{V}^{-1}\text{s}^{-1}$, respectively. Especially, BLSO single crystals have higher electron mobility than other semiconductors in the degenerate region. Readers can confirm this fact in section 3. 1. Furthermore, the oxygen stability of BSO is confirmed by high temperature thermal annealing in O_2 , Ar, and Air environments. The oxygen diffusion constant is evaluated to be about $10^{-15}\text{cm}^2\text{s}^{-1}$ at $530\text{ }^\circ\text{C}$. This value is 2~8 orders of magnitude lower than titanates, cuprates, and manganites.[53, 62-66] Recently, owing to these two superior properties of BSO, the published articles on the transport and transport mechanisms of BSO are consistently increasing. [55-61] Based on these two noble properties and with dopability in two different cation sites, we can expand the research field as shown in Fig 1. 3. The author strongly believes

that they are remarkable works in oxide electronics, if the demonstrations of a FET, p-n junction, and 2-dimensional electron gas (2DEG) based on BSO is possible.

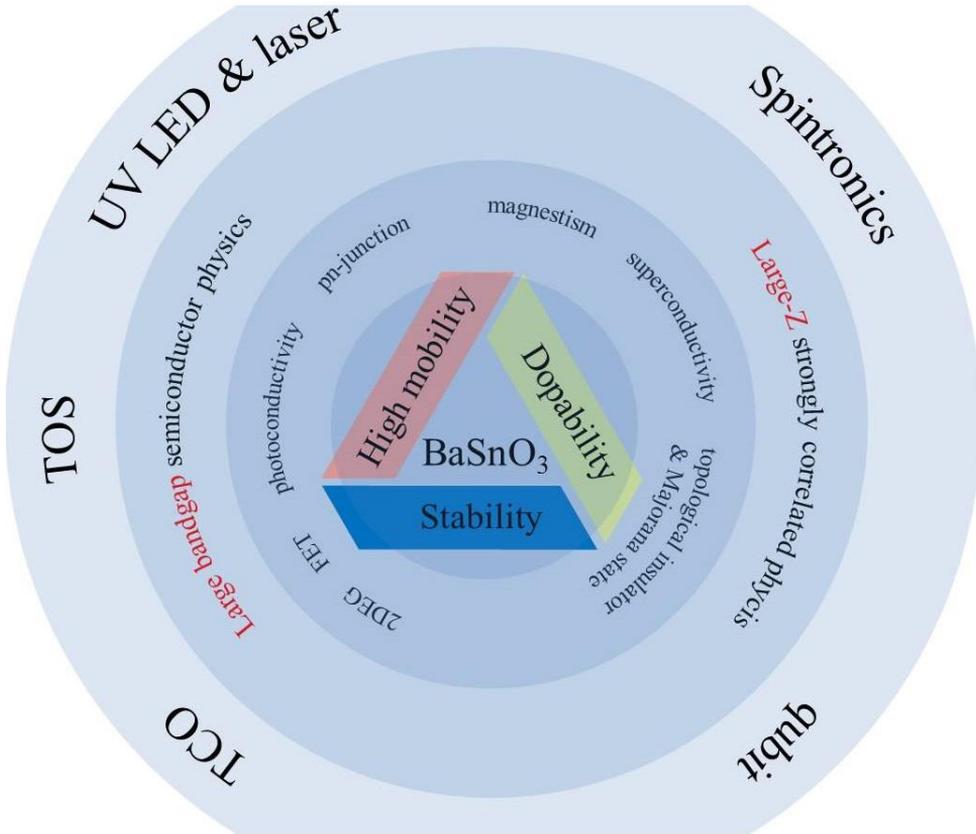


Figure 1. 3. Prospects of BSO

This thesis is organized as follows. In chapter 2, the results on the epitaxial growth of BSO including the crystallinity and surface morphology is presented. Chapter 3 is devoted to electrical properties of electron-doped BSO. Then based on Chapter 3, the performance of field effect devices based on BSO with amorphous and epitaxial gate oxides are presented throughout Chapter 4 and Chapter 5. In Chapter 6, we offer the results that show an interesting phenomenon in the $\text{LaInO}_3/\text{BaSnO}_3$ interface. Finally, the author will summarize these works in chapter 7.

Chapter 2

Epitaxial growth of

BaSnO₃

2.1 Epitaxial growth and structural properties of BaSnO₃ thin films

The lattice constants of commercially used substrates and widely investigated perovskite oxides were shown in Fig 2. 1. The LaAlO₃ substrate is commonly used in measuring the optical band gap for BSO and LIO. The author has fabricated BLSO thin films on KTaO₃, MgO, PrScO₃, and SrTiO₃ substrates to measure the electrical properties. Among them, the author obtained the best results when using SrTiO₃ substrates. Recently, Waderkar *et al.* and Ganguly *et al.* reported the electrical transport results of BLSO thin films by using MgO and

SmScO₃ substrates, respectively.[59, 72] A commonly used method to enhance electrical transport in said materials is to use a buffer layer. In the early days of BLSO research, many materials have been investigated for use as buffer layers [73-75]. A typical material for the buffer layer is LaInO₃. LaInO₃ was also used as a gate dielectric for carrier modulation of the BLSO active layer, as mentioned in chapter 5. BaHfO₃, SrZrO₃, SrHfO₃, and BaZrO₃ will also be mentioned in chapter 5 as an epitaxial gate dielectric material. First, we fabricated 100 nm thick BSO films with various La concentrations on BSO to confirm the crystallinity of BSO. The thin films were grown by PLD.

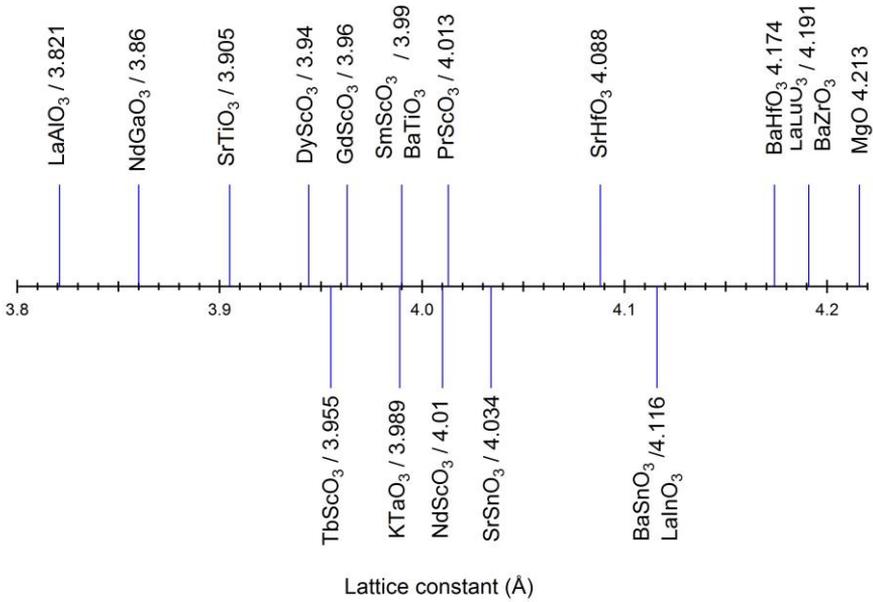


Figure 2. 1. Lattice constant of commercially used substrates and widely investigated perovskite oxides.[67-71]

The fabrication conditions are as follows: We used a KrF excimer laser ($\lambda = 248$ nm) with a repetition rate of 10 Hz and the laser energy density in the range of 1 ~1.5 J/cm², in an oxygen environment with 100 mTorr partial pressure, at a substrate temperature of 750 °C. Then, the crystal structural properties of BSO

thin films were investigated by noting the θ - 2θ curves and ω -rocking curves obtained from X-Ray diffraction (XRD). As seen in Fig 2. 2., secondary phases such as SnO_2 , BaO , and $\text{La}_2\text{Sn}_2\text{O}_7$ are not detected in the BSO or BLSO thin films. Only the (00 l) diffraction peaks were observed, suggesting that a completely (00 l)-oriented BSO thin film has been deposited on the STO substrate. The inset shows the ω -rocking curve of BSO at the lattice position around (002). The full width half maximum (FWHM) value of the ω -rocking curve is 0.112° . The θ - 2θ curves and ω -rocking curves for other La doped BSO thin films were obtained, and their FWHM values were 0.088° , 0.084° , 0.092° for BSO, 1 % BLSO, 4 % BLSO, 7 % BLSO, respectively. These small values suggest the high crystallinity of BSO and/or BLSO thin films.

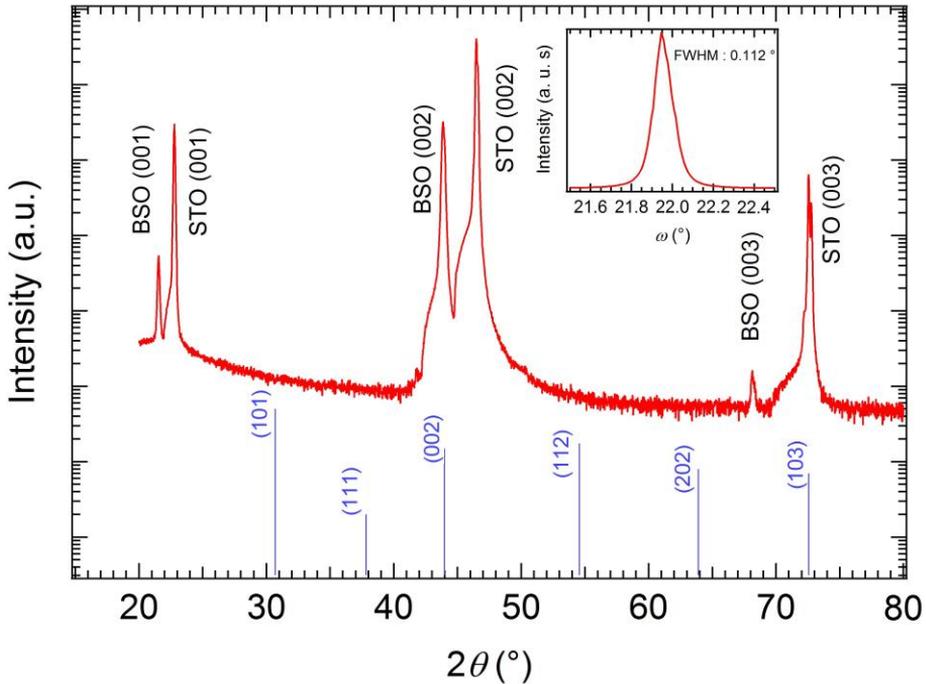


Figure 2. 2. XRD θ - 2θ measurement of BSO film. Inset denotes the ω -rocking curves of the BSO film. The diffraction pattern of BSO refers to BSO powder sample. [76]

2.2 Surface morphology before and after Rapid Thermal Annealing (RTA) treatment

The author investigated the surface morphology with an atomic force microscope (AFM) as shown in Fig 2. 3. The presented area size is $2 \times 2 \text{ }\mu\text{m}^2$. As seen in (a), as-grown thin film has a lower roughness value, root-mean-square roughness (R_{RMS}), than a half unit cell of BSO. The R_{RMS} value of a thin film shows a little change after rapid thermal annealing (RTA).

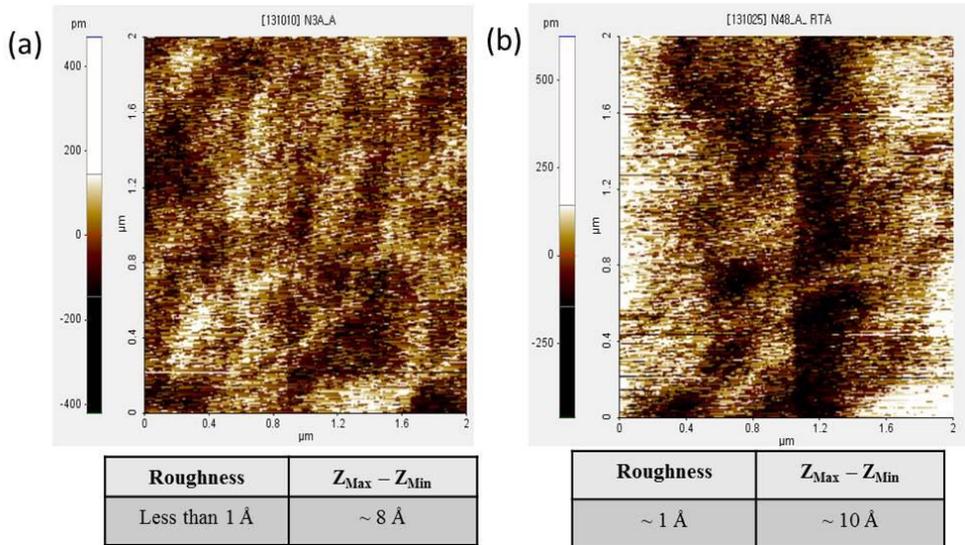


Figure 2. 3. AFM image of BSO thin films, indicating that the surfaces of thin films are very smooth. (a) and (b) show surface morphology of before and after RTA treatment.

This result indirectly indicates that the BSO thin film is thermally stable. Generally, the field effect mobility is much smaller than the corresponding bulk electron/hole mobility, since more scattering occurs at the interface. This atomically flat surface and thermally stable property of BSO is a very important

advantage in demonstrating electronic devices such as p-n diodes, FETs, and so on. Additionally, the author will present the surface morphology of BSO films with varying thickness and dilute nitric etching conditions in **Appendix A**. Able to achieve a flat atomic surface; this may be the best technique for enhancing the electrical transport properties of BLSO thin films for application to high-temperature thermally stable electronics industries.

Chapter 3

Electrical properties of electron doped BaSnO₃

The author has investigated the electrical transport of not only La-doped BSO but also Sb doped BSO systems.[133] The Sb-doped BSO system was a very interesting material to study, because we could understand the dopant site dependence of electron doped BSO systems. However, the author will just refer to articles on this subject since this thesis focuses more on the demonstration of high-mobility FET devices and their interface properties. This chapter will present the electrical transport properties of La-doped BSO. The author tried to demonstrate an all-epitaxial FET device using LIO/BLSO, until the Al₂O₃/BLSO FET device was reported. In the initial work of demonstrating the LIO/BSO FET, the author has achieved only a small carrier modulation of BSO by field effect, even though a full modulation is expected from calculation of modulation capacity, as shown in the equations in chapter 4. The results are presented in

Appendix B. The author presumes that this behavior is caused by the large density of threading dislocation in the BLSO channel layer, where the threading dislocation acts as a leakage path in the dielectric/BLSO interface and suppresses the electric field. The author will also present the various efforts made to overcome this issue by reduce the number of threading dislocations.

3.1 Electrical transport of La doped BaSnO₃ thin Films

The electrical transport properties such as electrical resistivity, electron mobility, and free carrier concentration, were measured using the Vander-Pauw method. The results compared with other famous semiconductors are shown in Fig 3. 1. As can be seen Fig 3. 1., the BLSO single crystal has higher electron mobility than other semiconductors in the degenerate region. In the author's knowledge, the electron mobility of BLSO was predicted to increase as the carrier density decreases in the non-degenerate region under consideration of Eq. (1.1). But although BLSO single crystals obeyed our prediction, BLSO thin films showed the opposite behavior. This behavior in BLSO thin films was observed and well-explained in GaN systems. In a GaN system, the transport behavior was explained by a limited transport mechanism due to threading dislocation scattering. [82,83] As free carriers increase, the transport is increased by the screening of charged threading dislocations. Hence, we can simply assume that the dominant scattering mechanism in BLSO single crystals is impurity scattering. However, both the impurity scattering by ionized impurities and the threading dislocation scattering caused by the lattice mismatch between the BSO and the STO substrate has an effect on the transport properties of BLSO thin films. Therefore, the author tried to understand and investigate the threading dislocations, which will be mentioned in section 3. 2.

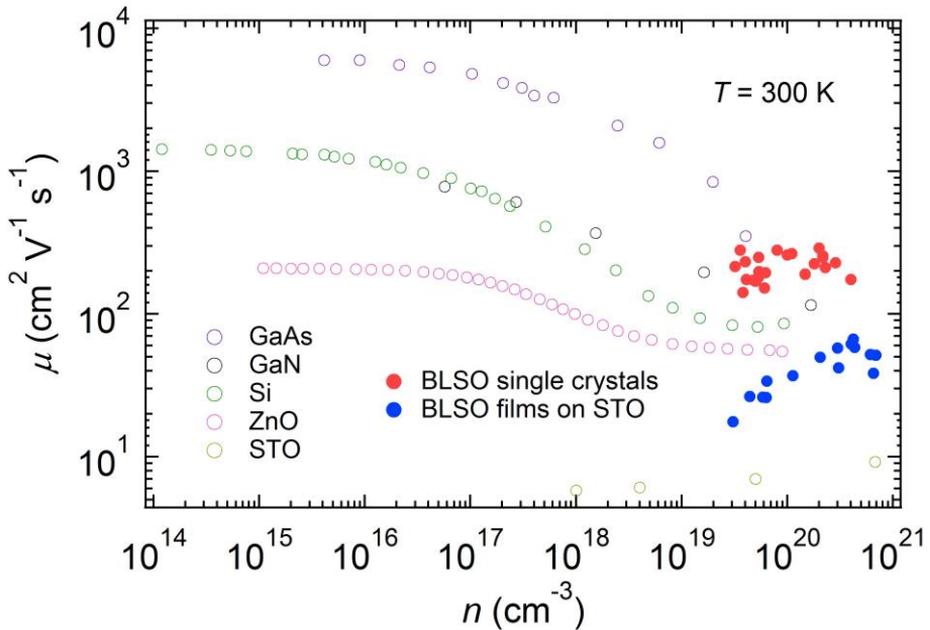


Figure 3. 1. The electrical mobility vs carrier density plots. The electrical transport of single crystals and thin films of La-doped BSO is shown in comparison with other well-known semiconductors such as GaAs, GaN, Si, ZnO, and STO. The same articles were cited in these plots. [53,54,77-81]

When considering the high electrical mobility, even with the free threading dislocations in the non-degenerate region, the author could easily expect the potential of BLSO materials to various applications. Recently, many articles on electron-doped BSO thin films were published as shown in Fig. 3. 2, after the high electrical transport was reported by our group. Filled black and red circles show our results. Especially, BLSO/BSO/STO samples showed results consistent with impurity-scattering dominant transport. As time passed, many groups have reported transport results for electron doped BSO. As seen in the figure, the results of other researches are consistent with ours. Our group also recognized the necessity of demonstrating fundamental devices such FETs before these results were published. Of course, most following results were reported after our successful fabrication of FETs based on BSO.

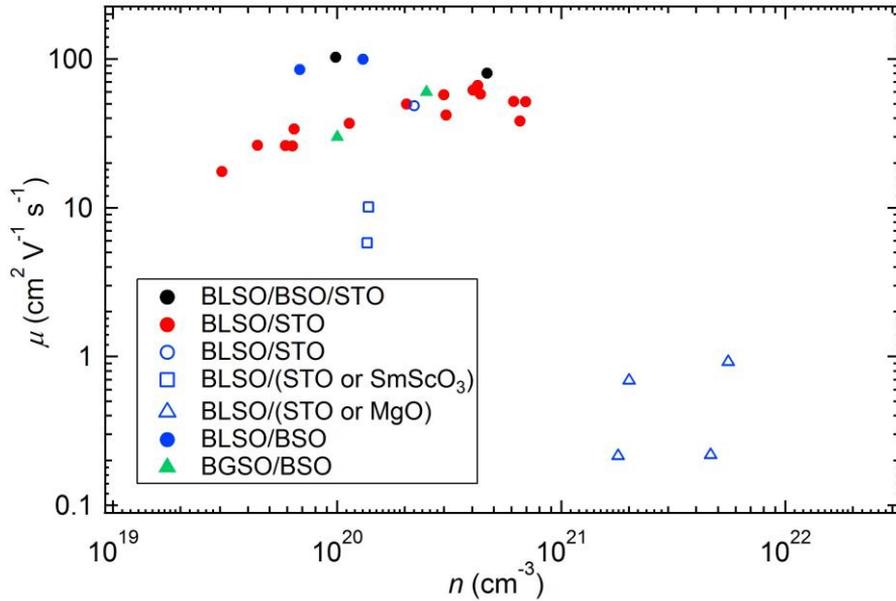


Figure 3. 2. Recently reported study of La-doped BSO and Gd-doped BSO. Some articles were cited in these plots.[53, 55, 57, 59, 84-86]

3.2 The Origin of transport limitations in the low doping Region

As seen in Fig 2. 1., the lattice mismatch between BSO and STO is about 5.4 %. This rather large lattice mismatch and difference of thermal expansion coefficients between BSO and STO substrates can lead to the formation of a large number of misfit dislocations (MDs) at the interface between the two. Furthermore, these MDs cause the formation of threading dislocations (TDs) when the BSO film is relaxed by increasing the thickness of the layer. To directly confirm the density of threading dislocations, we employed two methods. One is the investigation of the cross-sectional image obtained by transmittance electron microscopy (TEM). Another is the surface morphology obtained by AFM after etching the surface with a dilute nitric acid. It is well-known that the

dilute nitric acid etching process can produce dislocation etch pits on the surface of thin films. [87]

The cross-sectional image of a BLSO film and the surface morphology of an as-grown and etched BLSO film are shown in Fig 3. 3. In (a), we can observe two or more threading dislocations every 50 nm range of in-planes. (b) and (c) show the surface morphology before and after etching the surface with diluted nitric acid for about 10 secs. We can count about 200 ~ 300 etch pits. From these results, the 2-dimensional density of TDs was calculated as $10^{10} \sim 10^{11} \text{ cm}^{-2}$ in both measurement methods.

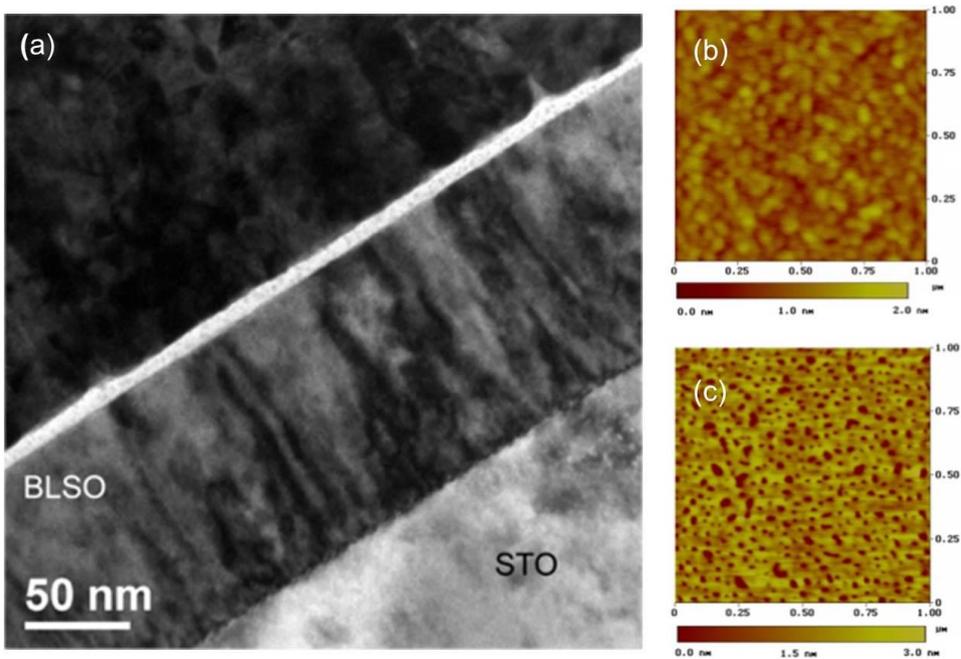


Figure 3. 3. Cross-sectional image of a BLSO film and the surface morphology of an as-grown and etched BLSO film. (a) shows the cross-sectional TEM bright-field images of a BLSO film by using a tow beam condition. (b) and (c) show the surface morphology of BLSO films both before and after etching with diluted nitric acid.[88,89]

3.3 Overcoming threading dislocations

The large density of TDs will act as limitation factor on the electrical transport of BLSO, as mentioned in the above section. The use of a buffer layer is a well-known method for decreasing TDs and improving the electrical properties when the lack of a lattice-matched single crystal for use as a substrate is an issue. The effect of a buffer layer on electrical transport was mentioned in many articles. Some articles present cross-sectional images to confirm that fact. In Fig. 3. 4., (a) and (b) show the images of thick SnO₂ and GaN.

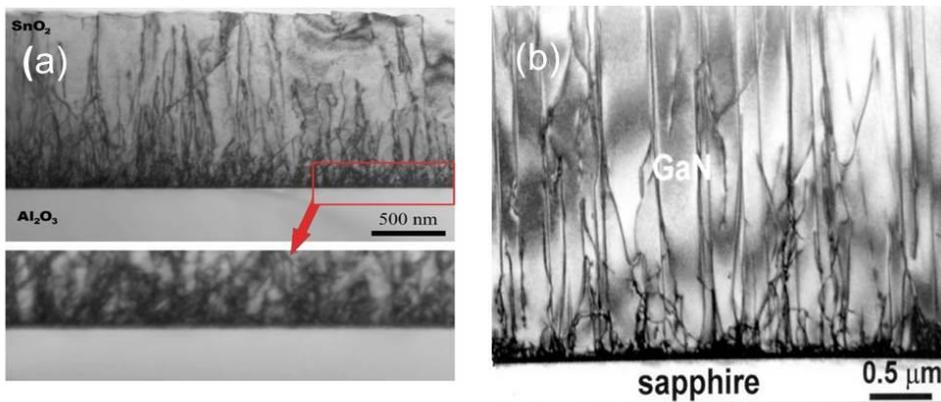


Figure 3. 4. Cross-sectional TEM images of (a) MBE-grown SnO₂/r-sapphire and GaN/sapphire. [74,75]

As can be seen, the threading dislocation density decreases as film thickness increases, since some dislocations disappear during growth. From these articles, the author has tried to study the effect of buffer thickness on BLSO transport.

First, 100 nm and 300 nm thick BLSO films with different La-doping rates (1 %, 4 %, 7 %) are prepared on $5 \times 5 \times 0.5 \text{ mm}^3$ STO (001) substrates by PLD technique to confirm the buffer layer effect on the transport of BLSO films. The results of Hall-effect measurements on BLSO films are presented in figure 3. 5. As we can see in this graph, in the doping range of less than 7 %, the carrier density and mobility of 300 nm thick BLSO films are higher than 100 nm thick

BLSO films. These results can be explained by the reduction of threading dislocation (TD) density, which acts as a charge traps source. As the mobile charge carrier is increased, the shielding of dislocation scattering centers is increased. In short, buffer layers will increase not only the average relaxation time but also the free carrier concentration. From this point, it is clear why the carrier density and mobility increases as the buffer layer becomes thicker. Therefore, the author deduces that using a buffer layer is critical to increasing the mobility in the low-doping region. Also, the author again concludes that the dominant scattering mechanism crosses over from the scattering by TDs in the low-doping region to scattering by La impurities in the more high-doping region.

Based on these conclusions, we prepared 100 nm films of 1 % La-doped BSO with BSO buffer layers of different thickness on STO substrates, in order to decide the appropriate BSO buffer layer thickness.

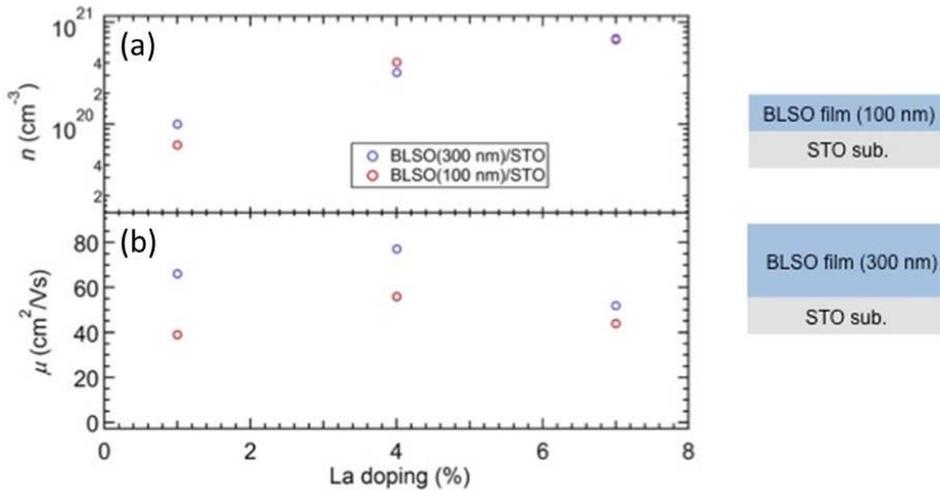


Figure 3. 5. (a) n and (b) μ of 100 nm and 300 nm thick BLSO thin films are presented as a function of La-doping percentage. The right figure represents the cross-sectional schematic of BLSO/BSO films on STO substrates.[90]

In Fig 3.6., the electron mobility, carrier density, and root-mean square (RMS) roughness of 100 nm thick BLSO thin films are presented for various BSO buffer layer thickness. As we can expect, the mobility and the carrier

concentration values of BLSO thin films increase. However, the R_{RMS} roughness of BLSO thin films increases as the whole thickness increases (BSO Buffer layer + BLSO thin films).

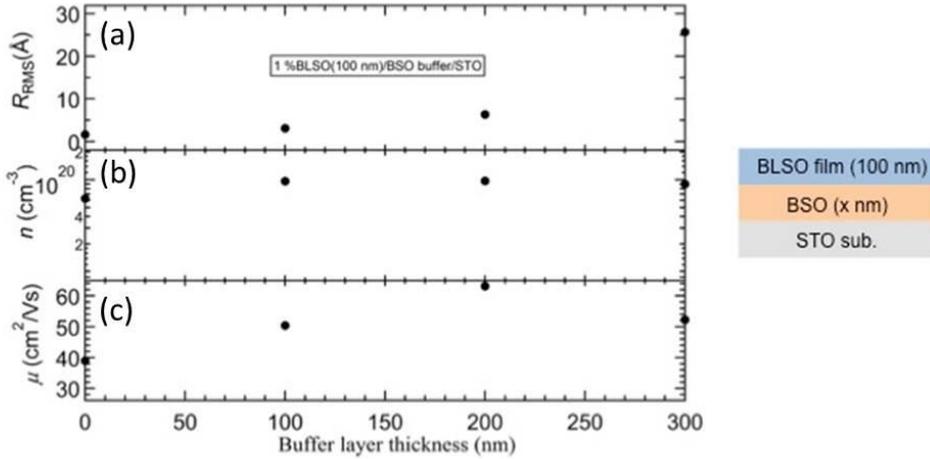


Figure 3. 6. (a) R_{RMS} roughness, (b) n , (c) μ are plotted for various thickness of BSO buffer layer. Right figure represents the cross-sectional schematic of BLSO/BSO films on STO substrate.[90]

Especially, the mobility value and the carrier density of BLSO thin films decreases at 300 nm thick buffer layers, which is probably due to the effect of the RMS roughness of the surface. Therefore, it was necessary to determine the appropriate thickness of the BSO buffer layer to optimize the mobility and the R_{RMS} roughness at the same time.

Chapter 4

Field effect transistor based on BaSnO₃ with amorphous gate oxides

Well-defined FET devices fabricated by dry and/or wet etching techniques will show high performances. But the chemical stability of SnO₂ is well-known. In fact, SnO₂ and cation doped SnO₂ have attracted the interest of many researchers as a protecting layer. [126, 127] Hence, during the fabrication of FET devices based on BSO, the wet etching process is impossible because BSO is based on SnO₂. Also, the dry etching process is impossible due to the thermal oxygen stability of BSO as mentioned in Chapter 1. The author was able to overcome these difficulties using stencil masks made of Si and SUS. The author

could achieve devices of sufficient performance, despite the large dimension of the fabricated FET devices. In this chapter, the author will present the performance of FET devices based on BSO with amorphous gate oxides. First, in section 4.1, the author describes a simple, conventional field effect theory including field effect mobility, subthreshold current/swing, and more, to help readers get a grasp on the research. In section 4.2 and 4.3, the amorphous gate oxide candidates and the dielectric properties of selected gate dielectric materials are presented. Finally, in section 4.4., device performances such as output and transfer characteristics are presented. Especially, the ambient aging experiment results performed on the fabricated FET device shows the stability of BSO. The author believes that these demonstrations will be the cornerstone for the application of oxide electronics.

4.1 Metal-insulator-semiconductor field effect transistors

The metal-insulator-semiconductor field effect transistor consists of a layer of metal, a layer of insulating material and a layer of semiconducting material as shown in Fig. 4.1. The current density in the active layer can be written as:

$$J = \sigma E \dots\dots\dots(4.1)$$

where σ and E are the electrical conductivity and electric field, respectively.

From the known equation $\sigma = nq\mu$, we can write the Eq. (4.1) as:

$$J = nq\mu E \dots\dots\dots(4.2)$$

The I_{DS} can be written as:

$$I = nq\mu AE \dots\dots\dots(4.3)$$

Where A (penetrated area by electron) = Wt . W and t denote the channel width and the channel thickness, respectively.

A substitution of $n = \frac{N}{LA}$ gives

$$I_{DS} = WC_{ox}(V_{GS} - V_{th})\mu E \dots\dots\dots(4.4)$$

Considering the potential $\phi(x)$ in an arbitrary point, if we apply both V_{GS} and V_{DS} to the device, the I_{DS} can be expressed as:

$$I_{DS} = WC_{ox}(V_{GS} - V_{th} - \phi(x))\mu \frac{d\phi}{dx} \dots\dots\dots(4.5)$$

By integrating from 0 to L, under the boundary condition $\phi(x = 0) = 0$ and $\phi(x = L) = V_{DS}$, we can calculate the I_{DS} as:

$$I_{DS} = \frac{W}{L} \mu C_{ox} (V_{GS} - V_{th} - \frac{V_{DS}}{2}) V_{DS} \dots\dots\dots(4.6)$$

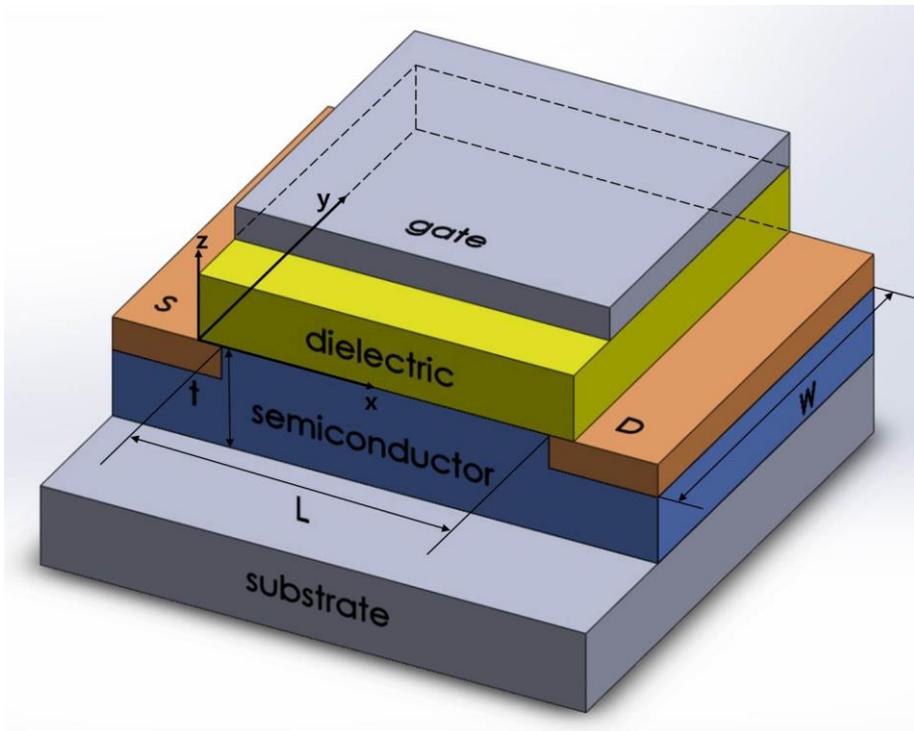


Figure 4. 1. Schematics of conventional FETs

At small V_{DS} ($V_{DS} \ll V_{GS} - V_{th}$), I_{DS} is proportional to V_{DS} . We call this region the “linear region”. As V_{DS} increases, I_{DS} deviates from its linear behavior. And then finally, at high V_{DS} , the current is saturated. We can evaluate the saturated current condition by calculating the derivative of I_{DS} to V_{DS} . We can obtain the V_{DS} needed to saturate I_{DS} as:

$$V_{DS} = V_{GS} - V_{th} \dots \dots \dots (4.7)$$

This V_{DS} is denoted as $V_{DS_{sat}}$.

Substitution of Eq. (4.7) into Eq. (4.6) gives

$$I_{DS_{sat}} = \frac{W}{2L} \mu C_{ox} (V_{GS} - V_{th})^2 \dots \dots \dots (4.8)$$

From Eq. (4.6) and Eq. (4.8), the field effect mobility can be obtained by calculating the transconductance ($g_m \equiv \frac{\partial I_{DS}}{\partial V_{GS}}$).

In the linear region,

$$\frac{\partial I_{DS}}{\partial V_{GS}} = \frac{W}{L} \mu C_{ox} V_{DS} \dots \dots \dots (4.9)$$

In the saturation region,

$$\left(\frac{\partial \sqrt{I_{DS}}}{\partial V_{GS}} \right)^2 = \frac{W}{2L} \mu C_{ox} \dots \dots \dots (4.10).$$

In real device measurements, the field effect mobility values evaluated from equations (4.9) and (4.10) increases dramatically when above threshold voltage, since the accumulated carriers screened the electric field created by defects such as bulk traps, interface traps, vacancies, and more. So in the appropriate high level of electric field, the field effect mobility approaches the bulk mobility of the active layer. If a high electric field is applied, electrons are gradually accumulated near the surface. Therefore, the field effect mobility doesn't increase and is restricted by the surface roughness and interface quality. For this reason the value of the field effect mobility is generally smaller than the bulk mobility of the active layer and depends on the surface quality. So an atomically

flat active layer surface and a high quality interface between the gate dielectric and the active layer are needed for high performance FET devices. Furthermore, from equation 4.7 and 4.8, we can evaluate the threshold voltage from the experiment results by using the extrapolation of $I_{DS}-V_{GS}$ and $I_{DS}^{1/2} - V_{GS}$ in both linear and saturated regions, respectively. Generally, as shown in Fig 4.2.(a), the I_{DS} is not zero below V_{th} . Below V_{th} , I_{DS} decreases exponentially with decreasing gate voltage. This non-zero current is known as the subthreshold current, originating from the diffusion of carriers due to thermal energy. We can divide the transfer characteristic curve into two regions known as diffusion and drift regions, as shown in Fig 4. 2. (b). In the carrier diffusion region, the I_{DS} is proportional to $\exp(qV_s/kT)$. In the carrier drift region, the I_{DS} is proportional to $V_{GS} - V_{th}$ and $(V_{GS} - V_{th})^2$ for the linear and saturation region, respectively. In the subthreshold region, we define an important parameter, the subthreshold swing (S), which is the necessary V_{GS} to increase the I_{DS} by one order.

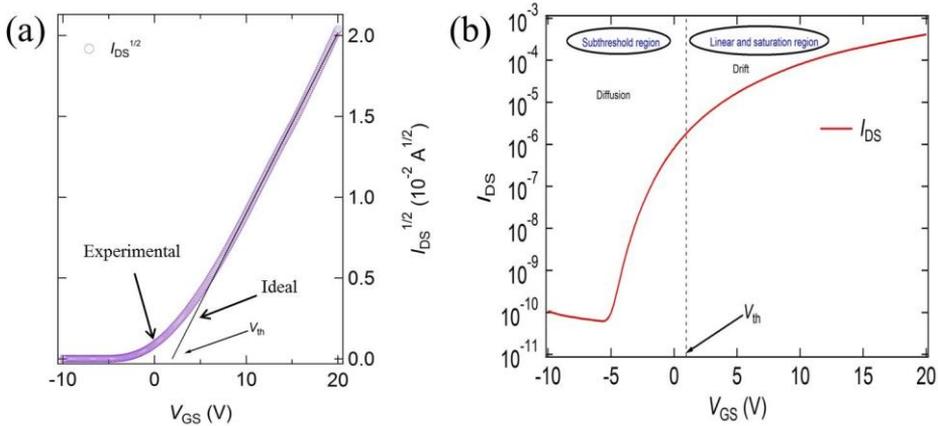


Figure 4. 2. (a) Plot of $I_{DS}^{1/2} - V_{GS}$ characteristic (b) $I_{DS} - V_{GS}$ characteristic. [91]

$$S = 1/\left(\frac{d \ln(I_{DS})}{dV_{GS}}\right) \dots \dots \dots (4.11)$$

This value can be the standard for evaluating device performance in low-voltage, low-power applications. Additionally, we can roughly calculate the interface trap density with the value of the subthreshold current. If the interface

trap is not present, the equivalent circuit can be represented as Fig 4. 3. (a). The S can be written as

$$S = \ln 10 / \left(\frac{d \ln(I_{DS})}{dV_S} \frac{dV_S}{dV_{GS}} \right) \dots \dots \dots (4.12)$$

Then we can obtain Eq. (4.13) by derivation from Eq. (4.12)

$$S = \frac{kT}{q} \ln 10 \left(1 + \frac{C_{dep}}{C_{ox}} \right) \dots \dots \dots (4.13)$$

where k , T , and q are Boltzman's constant, temperature, and electron charge, respectively. So theoretically, we can estimate the minimum value of S as 60 mV/dec at room temperature.

If any traps are present between the active layer and the gate oxide, the equivalent circuit can be expressed as Fig 4. 3. (b). And Eq. (4. 13) can be modified as:

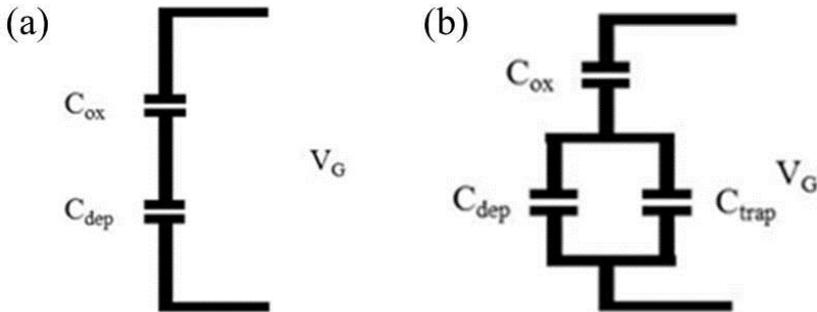


Figure 4. 3. Equivalent circuits for (a) ideal and (b) including trap effects were shown.

$$S = \frac{kT}{q} \ln 10 / \left(1 + \frac{C_{dep} + C_{trap}}{C_{ox}} \right) \dots \dots \dots (4.14)$$

where $C_{trap} = q \sqrt{\epsilon_{sc} D_{bulk}} + q^2 D_{it}$.

This equation can be rewritten as:

$$S \cong \frac{kT}{q} \ln 10 / (1 + \frac{q^2 D_{it}}{C_{ox}}) \dots \dots \dots (4.15)$$

Of course, these values may be over-estimated since we calculate the trap density assuming the absence of bulk traps.

➤ Modulation capacity of dielectrics

When we choose the gate dielectric to demonstrate FET devices, we should consider some material parameters such as the breakdown field, dielectric constant, and modulation capacity (see Section 4.2). In this section, the author will discuss the carrier modulation capacity using the dielectric material. In fact, the induced carrier density in the active layer from the gate dielectric is defined by a function of V_{GS} , V_T , and V_{DS} . Fortunately, we can estimate the modulation capacity by the simple relation;

$$Q \approx CV \dots \dots \dots (4.16)$$

where $Q = Nq$, $C = \epsilon A/d$, and $V = Ed$. This is possible since we generally consider high V_{GS} conditions to calculate the maximum modulation carrier density. We can simplify equation (4.1) as

$$n_{2D} = \frac{\epsilon E}{q} \dots \dots \dots (4.17)$$

Where q , ϵ , and E are the electron charge, permittivity of the gate dielectric, and applied electric field, respectively.

➤ Dielectric breakdown

It is known that catastrophic breakdowns occur when random defects form a chain between the gate dielectric and the semiconductor as described in the percolation theory. Via a tunneling current on the MOS device, the carriers will pass through the dielectric insulator. The energetic carrier causes random distribution of the defects in dielectric insulator. As increased the defect density

by passage of energetic carrier, the continuous chain of defects is formed, which is the leakage current path. Finally, the catastrophic breakdown occurs as shown in Fig. 4. 3. Except defect, which is generated by the passage of energetic carriers, we could think another defect such as fixed charge traps, interface charge trap, threading dislocations as the source of leakage current and catastrophic breakdown in an insulator.

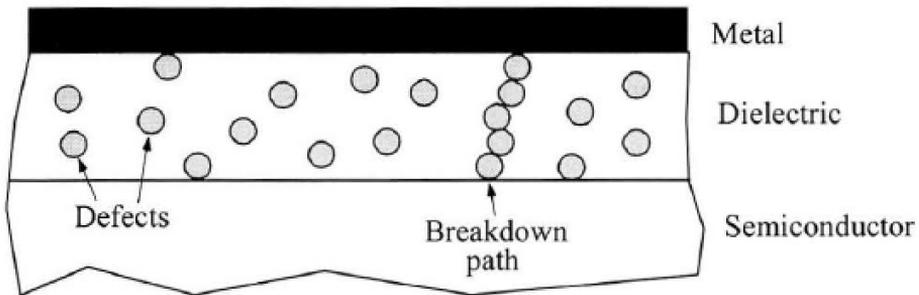


Figure 4. 3. Percolation theory: breakdown occurs when random defects form a chain between the gate and the semiconductor.[92]

In this point of view, the clear interface between active layer and gate dielectric might be needed in our investigation.

4.2 Amorphous gate oxide candidate

When we demonstrated the FETs, the choice of appropriate gate dielectric is very important since the interface between active layer and gate dielectric, electrically active defect, and the conduction band offset with active layer affect the performance such as field effect mobility, I_{on}/I_{off} ratio, and subthreshold swing (S) of FETs device.

So our choice of gate dielectric is based on follows.

1. The conduction band offsets with BSO has to be over 1 eV in order to minimize the effect of carrier injection of its band.
2. The dielectric constant (K) and the breakdown field (E_{BD}) must be high to have higher modulation capacity of carrier of BSO active layer.
3. Gate dielectric must have few bulk electrically active defects, the origin of increasing the off current of FETs device.
4. Gate dielectric must be matching with BSO active layer to minimize the interface state, the origin of increasing the off current and the degradation of FETs device.

The candidates for amorphous gate dielectrics such as SiO_2 , Al_2O_3 , Ta_2O_3 , TiO_2 , ZrO_2 , HfO_2 , La_2O_3 , Y_2O_3 are shown in Fig 4. 4. These materials have been also investigated as candidates for high-k dielectrics in conventional Si industries, and hence their dielectric properties are well-known.[93, 94] As can be seen in Fig. 4.4., most candidate oxides satisfy criterion 1 except Ta_2O_3 and TiO_2 . In order to choose the suitable gate dielectric to demonstrate the FET device based on BLSO, the author evaluated the modulation capacity by using the known parameters of each gate dielectric, such as the dielectric constant and breakdown field. The results are shown in table 2. The author assumed that the thickness of the gate dielectrics to be 100 nm for easy comparison with each other. Since we need to modulate the lightly-doped BLSO active layer, we must consider the 2-dimensional free electron carrier density (n_{2D}) of BLSO. Although the free carrier activation rate did not reach the ideal value due to the charge trapping at threading dislocations, we calculated n_{2D} under the assumption that the free electron carrier is activated by a substitution of a La^{3+} into a Ba^{2+} site.

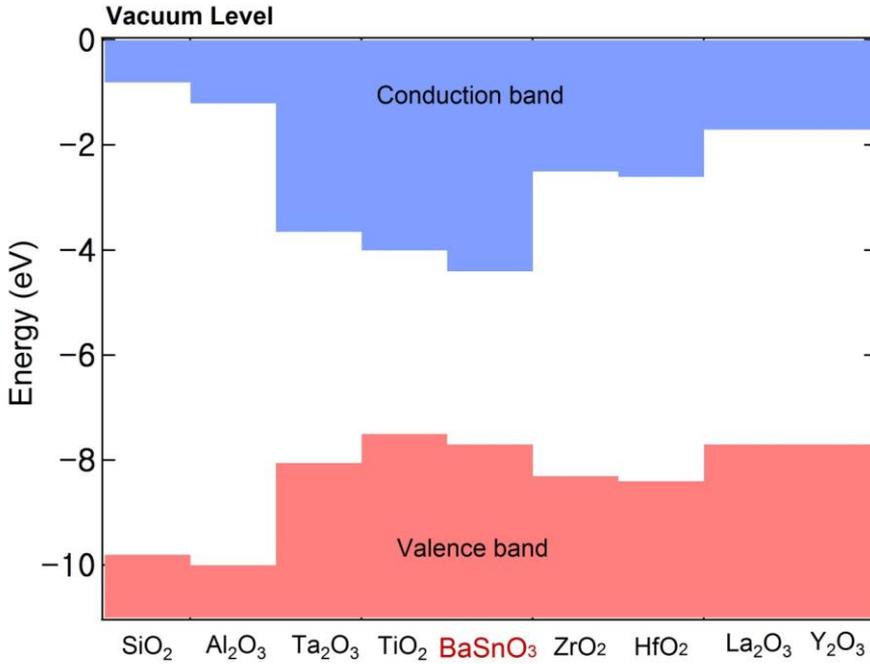


Figure 4. 4. The band alignment between SiO₂, Al₂O₃, Ta₂O₃, BaSnO₃, ZrO₂, HfO₂, La₂O₃, and Y₂O₃. [93,125]

Materials	Dielectric Constant	Band gap (eV)	CB offset With BaSnO ₃ (eV)	Breakdown Field (MVcm ⁻¹)	Modulation Capacity (cm ⁻²) (t _{oxide} = 100 nm)
SiO ₂	3.9	9	3.6	13	2.8 × 10 ¹³
Al ₂ O ₃	9	8.8	3.2	6.2	3.08 × 10 ¹³
Ta ₂ O ₃	22	4.4	0.75	3.2	3.9 × 10 ¹³
TiO ₂	80	3.5	0.4	3.0	1.33 × 10 ¹³
ZrO ₂	25	5.8	1.9	3.8	5.26 × 10 ¹³
HfO ₂	25	5.8	1.8	4.0	5.53 × 10 ¹³
La ₂ O ₃	30	6	2.7	4.2	6.98 × 10 ¹³
Y ₂ O ₃	15	6	2.7	2.0	1.66 × 10 ¹³

Table 2. Static dielectric constant, experimental band gap, calculated conduction band (CB) offsets with BSO, breakdown strength, and calculated modulation capacity of the candidate gate dielectrics. [93-102]

The evaluated value of n_{2D} is about $1.4 \sim 4.2 \times 10^{13} \text{ cm}^{-3}$ in the range of 0.1 % ~ 0.3 % La-doping, where the lattice constant of BSO and the active layer thickness in the FET device is 4.116 Å and 10 nm, respectively. The author chose Al_2O_3 and HfO_2 as gate dielectric oxides for the FET device based on BLSO after considering the parameters discussed above.

4.3 Investigation of Al_2O_3 and HfO_2 gate dielectrics

To confirm the reliability of Al_2O_3 and HfO_2 , the author needed to check their dielectric properties, such as E_{BD} and K . The author first fabricated capacitor devices as follows. An ITO line as a contact layer was grown by the PLD method using a Si stencil mask, then Al_2O_3 and HfO_2 was each deposited as a dielectric layer by the atomic layer deposition (ALD) method. Finally, an ITO line as a contact layer was grown again above the Al_2O_3 and HfO_2 layers.

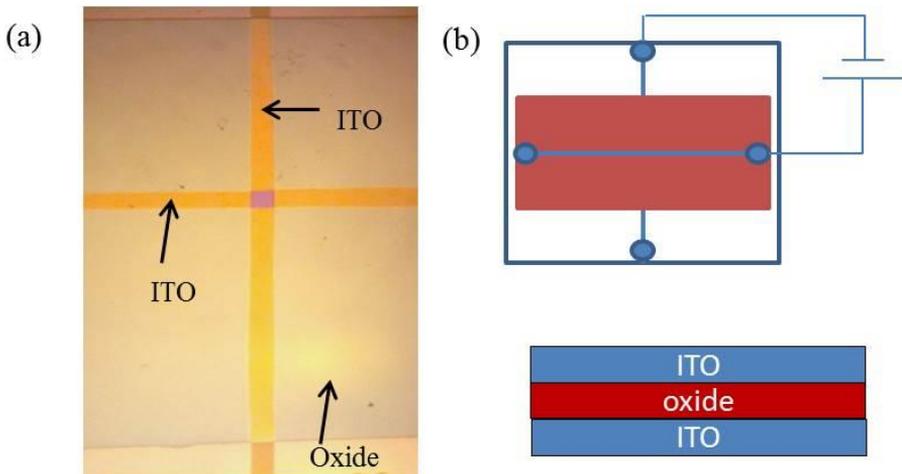


Figure 4. 5. Optical microscope image and measurement schematic of ITO/oxide dielectric/ITO capacitor.

The cross-sectional diagram and optical microscope image of ITO/oxide dielectric/ITO capacitor is shown in Fig 4. 5. After the fabrication of ITO/Al₂O₃/ITO and ITO/HfO₂/ITO capacitors, the author investigated the dielectric constant and breakdown strength by measuring capacitance (C) – frequency (F) and leakage current (J) - electric field (E) characteristics, respectively.

➤ Breakdown field and dielectric constant of Al₂O₃ and HfO₂

The breakdown strength characteristics of Al₂O₃ and HfO₂ are shown in Fig 4. 6. The inset denotes the device junction of the capacitors. As can be seen, the breakdown strength of Al₂O₃ and HfO₂ appears to be 5.1 MVcm⁻¹ and 3.4 MVcm⁻¹, respectively.

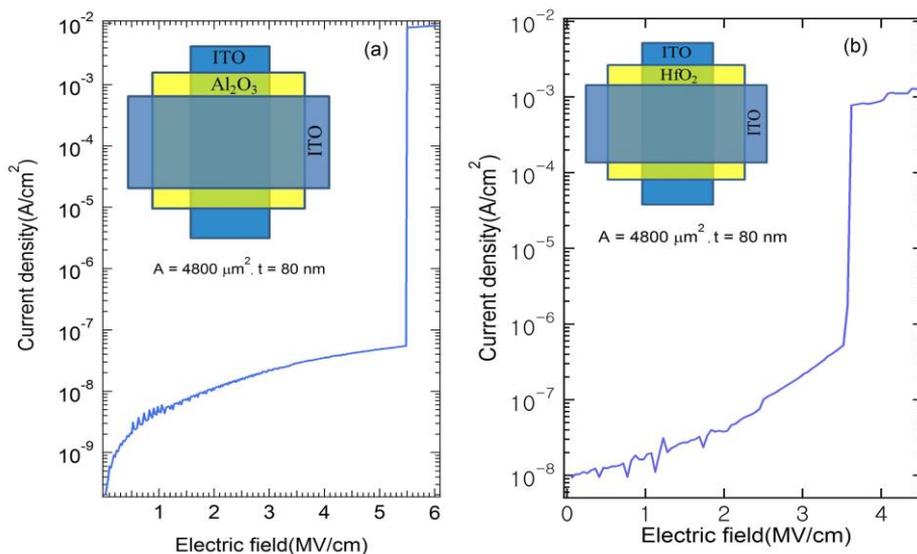


Figure 4. 6. *J-E* characterization of an ITO/Al₂O₃/ITO and ITO/HfO₂/ITO capacitor is shown in (a) and (b). Insets denote the structure and dimension of the capacitors. The gated area and thickness of both capacitors are 4800 μm² and 80 nm, respectively. [103]

They also have a low leakage current density of about $10^{-8} \sim 10^{-9}$ A/cm², which is consistent with known values. The capacitance (C) – Frequency (F) characteristics are presented Fig 4. 7. From this measurement, the dielectric constant of Al₂O₃ and HfO₂ have been calculated by the fundamental relation,

$$K = C \frac{A}{d} \dots \dots \dots (4.18)$$

where C , d , A are the measured capacitance, thickness, and area of junction, respectively. The calculated dielectric constants are 8.8 and 23.7 for Al₂O₃ and HfO₂, respectively. These values are very consistent with known properties in previous articles. [93,94] From these material parameters, the author has demonstrated an FET device based on BSO with amorphous Al₂O₃ and HfO₂.

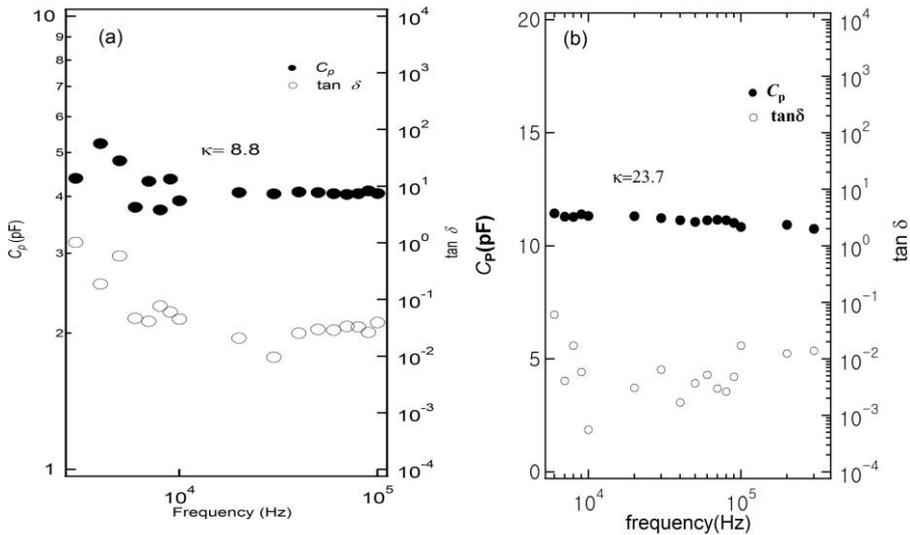


Figure 4. 7. C - F curves for an ITO/Al₂O₃/ITO and ITO/HfO₂/ITO capacitor. (a) C - F characteristic of an ITO/Al₂O₃/ITO capacitor and (b) C - F characteristic of an ITO/HfO₂/ITO capacitor are shown. Filled and unfilled markers denote the capacitance and dissipation factor, respectively. [103]

4.4 Devices utilizing Al_2O_3 and HfO_2 gate dielectrics

4.4.1 Device fabrication process

The TFT devices using an Al_2O_3 or HfO_2 /BLSO structure on a STO substrate are fabricated as follows. The FET device using Al_2O_3 /BLSO is fabricated in two different doping concentrations such as 0.14 % and 0.5 % La-doping in the active layer to compare the effect of carrier concentration on the output and transfer characteristics. First the 110 nm BSO buffer layer, which is the selected buffer layer thickness to achieve optimal electrical and surface properties of the active layer, is deposited on a STO substrate by PLD with the previous conditions. Then, the author deposits the lightly-doped semiconducting channel layer through a Si stencil mask with the same conditions. As the source and drain contacts, ITO is deposited with a P_{O_2} of 10 mTorr and a temperature of 150 °C by PLD using a stainless steel mask. Then an Al_2O_3 or HfO_2 gate dielectric layer is deposited by ALD on the channel layer. After the gate dielectric layer deposition, the author monitors the conductance of the BSO active layer and observed that the conductance generally increases by more than one order of magnitude. The author is able to obtain the original conductance value of BSO by annealing at 400 °C in an oxygen atmosphere. The author believes that the conductance increase in the BLSO active layer may be due to hydrogen absorption on the surface during the ALD process. Finally, ITO is deposited on the device as a gate electrode with a small overlap to the source and drain contact layer to minimize the leakage current and maximize the possible applied bias. The cross sectional diagram and an optical microscope image of an Al_2O_3 /BLSO FET device are presented in Fig 4. 9.

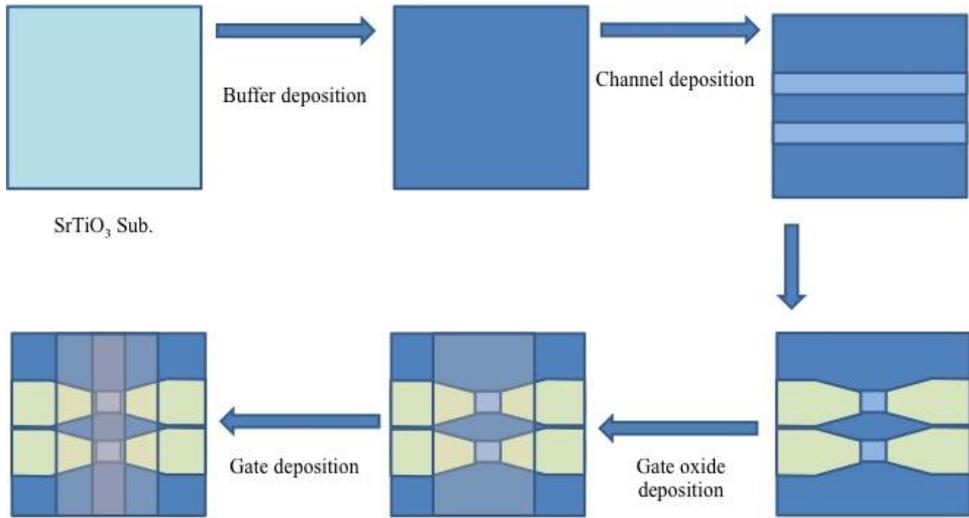


Figure 4.8. The fabrication process of $\text{Al}_2\text{O}_3/\text{BLSO}$ and HfO_2/BLSO devices.

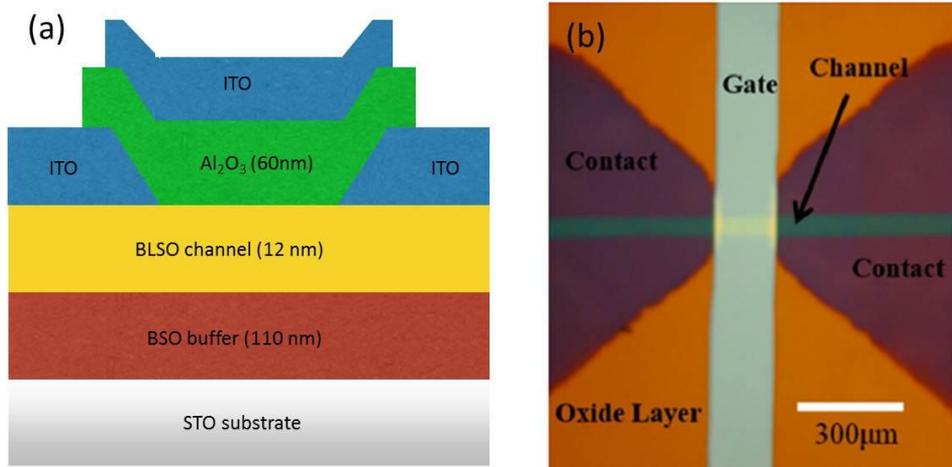


Figure 4. 9. (a) The cross-sectional diagram and (b) an optical microscope image of an $\text{Al}_2\text{O}_3/\text{BLSO}$ FET device. [90]

The channel length and width of the $\text{Al}_2\text{O}_3/\text{BLSO}$ FET are 140 and 60 μm , respectively. Thickness of the Al_2O_3 layer on the 0.14 % BLSO active layer is 60 nm and is 40 nm on the 0.5 % BLSO active layer. The channel length and width of the HfO_2/BLSO FET are 140 and 100 μm , respectively. And the

thickness of the HfO_2 layer on the 0.25 % BLSO active layer is 126 nm. As can be seen, both devices have a well-defined image.

4.4.2 Output characteristics of $\text{Al}_2\text{O}_3/\text{BLSO}$ and HfO_2/BLSO FETs

The output characteristics of $\text{Al}_2\text{O}_3/\text{BLSO}$ and HfO_2/BLSO FETs are shown in Fig. 4. 10. (a), (b), and (c), where the drain-source current (I_{DS}) is plotted against the drain-source voltage (V_{DS}) for various fixed gate-source voltages (V_{GS}). As seen above, I_{DS} is proportional to V_{DS} in the region where V_{DS} is smaller than $V_{\text{GS}} - V_{\text{th}}$ in the linear region. I_{DS} deviates from linear behavior as V_{DS} increases. The current is saturated in the region of $V_{\text{GS}} - V_{\text{th}} < V_{\text{DS}}$.

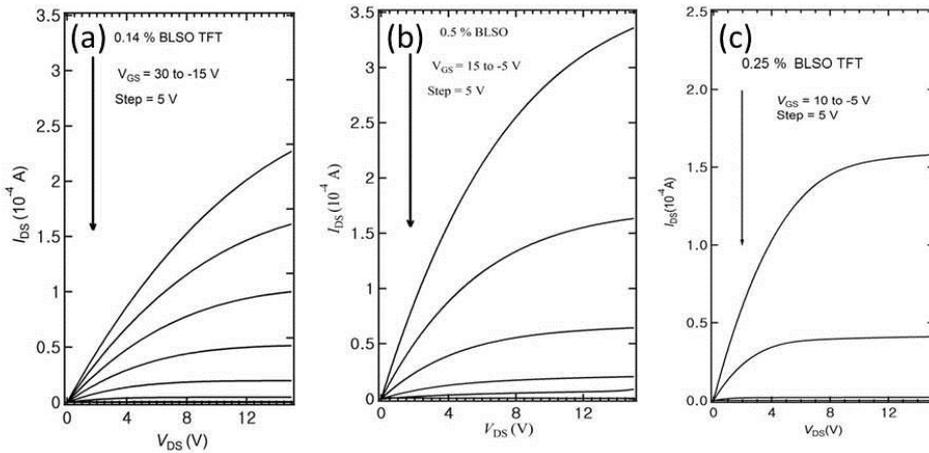


Figure 4.10. The output characteristics, $I_{\text{DS}}-V_{\text{DS}}$ curves, of $\text{Al}_2\text{O}_3/\text{BLSO}$ and HfO_2/BLSO TFTs for various gate bias V_{GS} at room temperature. The output characteristics of (a) $\text{Al}_2\text{O}_3/0.14\%$ BLSO, (b) $\text{Al}_2\text{O}_3/0.5\%$ BLSO, and (c) HfO_2/BLSO TFTs are presented. Gate voltages of (a) and (b) are varied from -15 V to 30 V, from -5 V to 15 V, from -5 V to 10 V in 5 V steps, respectively. [90,103]

Of course, these behaviors are parallel to the ideal output characteristics (I_{DS} vs. V_{DS}) of a MOSFET which are described by the linear region, non-linear region, and current saturation region. The output characteristics, the I_{DS} - V_{DS} curves, of $\text{Al}_2\text{O}_3/\text{BLSO}$ and HfO_2/BLSO TFTs for various gate bias V_{GS} at room temperature are shown. The output characteristics of (a) $\text{Al}_2\text{O}_3/0.14\%$ BLSO, (b) $\text{Al}_2\text{O}_3/0.5\%$ BLSO, and (c) HfO_2/BLSO TFTs are presented. The devices clearly show the behavior of a n-type accumulation mode FET; under positive and negative V_{GS} , I_{DS} increases and decreases, because positively increasing and negatively increasing V_{GS} accumulates and depletes the carriers in the active layer as commented above, respectively. Finally, as we can see in (c), a lower V_{GS} is required to accumulate the carriers in the active layer since the dielectric constant of HfO_2 is higher than Al_2O_3 .

4.4.3 Transfer characteristic of $\text{Al}_2\text{O}_3/\text{BLSO}$ and HfO_2/BLSO FETs

The transfer characteristic, such as I_{ds} - V_{gs} , μ_{FE} , I_{on}/I_{off} ratio, and subthreshold swing (S), are shown in Fig 4. 11. (a) represents the transfer characteristics of the both $\text{Al}_2\text{O}_3/0.14\%$ BLSO and $\text{Al}_2\text{O}_3/0.5\%$ BLSO FETs. As expected results by consideration of results shown in Fig 4. 8., sufficient current enhancement due to carrier accumulation in an active layer could be achieved by applied positive gate bias in both devices. However, author couldn't see the full depletion of active layer by applied negative gate bias in $\text{Al}_2\text{O}_3/0.5\%$ BLSO FET. The author believes that this behavior comes from both high concentration of carrier on BLSO active layer and electric field cancel by interface trap charges. And the author calculates the field effect mobility of devices by using the general relation as commented in chapter 4.1. The calculated maximum mobility of 0.14 % and 0.5 % BLSO active layer are 17.8 and 14.73 $\text{cm}^2\text{V}^{-1}\text{s}^{-1}$, respectively, for $V_{DS} = 1$ V.

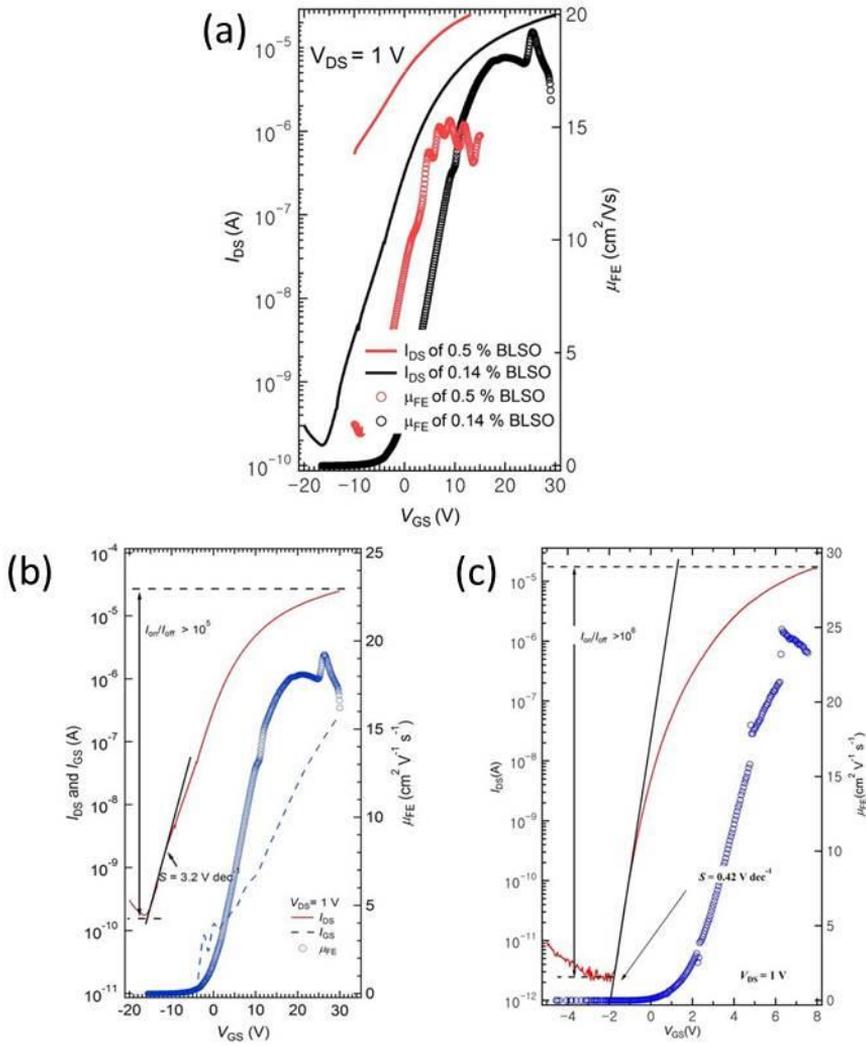


Figure 4. 11. (a) The transfer characteristics, $I_{DS}-V_{GS}$ and $\mu_{FE}-V_{GS}$, of the FET devices for $\text{Al}_2\text{O}_3/0.14\%$ BLSO and the $\text{Al}_2\text{O}_3/0.5\%$ BLSO are represented as the solid line and the symbols, respectively. (b) Transfer characteristic of the FET device with 0.14 % BLSO active layer was represented. The I_{on}/I_{off} ratio at V_{GS} of -15 and 30V exceeds 10^5 for 0.14% BLSO. (c) Transfer characteristic of the FET device for $\text{HfO}_2/0.25\%$ BLSO. The I_{on}/I_{off} ratio at V_{GS} of -5 and 8V exceeds 10^6 . [90,103]

(b) and (c) show the transfer characteristic of $\text{Al}_2\text{O}_3/0.14\%$ BLSO and $\text{HfO}_2/0.25\%$ BLSO FETs to compare their performance. One of most important parameter in FET $I_{\text{on}}/I_{\text{off}}$ ratio, which is defined as the ratio of the maximum to minimum I_{DS} , is higher than 10^5 and 10^6 for $\text{Al}_2\text{O}_3/0.14\%$ BLSO and $\text{HfO}_2/0.25\%$ BLSO FETs, respectively. The field effect mobility of HfO_2/BLSO device is better than $\text{Al}_2\text{O}_3/\text{BLSO}$ device. Also the subthreshold swing (S), is found to be 3.2 Vdec^{-1} and 0.65 Vdec^{-1} for $\text{Al}_2\text{O}_3/0.14\%$ BLSO and $\text{HfO}_2/0.25\%$ BLSO FETs, respectively. From these values, we could evaluate the trap density (D_{it}) as 4.38×10^{13} and $9.99 \times 10^{12} \text{ cm}^{-2}\text{eV}^{-1}$ for each. This poor value for $\text{Al}_2\text{O}_3/0.14\%$ BLSO FET explains why mobility of the 0.14% BLSO active layer is not so large value compared with the mobility of 0.5% BLSO active layer though it has small impurity scattering than 0.5% BLSO active layer. By comparison of $\text{Al}_2\text{O}_3/0.14\%$ BLSO and $\text{HfO}_2/0.25\%$ BLSO FETs we can conclude that the use of higher dielectric materials could decrease S and the operating voltage since the high capacitance with high dielectric constant could compensate the higher density of interface traps. Of course many groups have found Al_2O_3 by ALD retains a large density of charge traps.[104-106] The calculated values such as mobility, $I_{\text{on}}/I_{\text{off}}$ ratio, subthreshold swing, and interface trap density with previous reported performance of FET device results based on perovskite oxide are represented Table 3. As seen, these devices show obviously higher performance than the previous reported FET device results based on perovskite oxide. It is provided evidence of superior material properties of BSO such as high mobility and atomically flat surface with oxygen stability and shows the potential of application of BSO to transparent high mobility FET device. So the development of alternative gate dielectric with free charge traps at the interface is needed. The device fabrication based on all-perovskite, which is perfect match with active layer and gate dielectric, will be good approach. So we demonstrate the FET device with all-epitaxial heterostructure and its results are shown in Chapter 5.

Device	$\mu_{FE}(\text{cm}^2\text{V}^{-1}\text{s}^{-1})$	$I_{\text{On}}/I_{\text{off}}$ ratio	$S(\text{V dec}^{-1})$	$D_{\text{it}}(\text{eV}^{-1}\text{cm}^{-2})$
$\text{Al}_2\text{O}_3/\text{KtTiO}_3$	0.4	10^4		
$\text{Al}_2\text{O}_3/\text{SrTiO}_3$	0.1	10^2		
$\text{CaHfO}_3/\text{SrTiO}_3$	0.4-0.5	$\sim 10^5$		
$\text{CaHfO}_3/\text{SrTiO}_3$	0.4	$\sim 10^5$		
$\text{DyScO}_3/\text{SrTiO}_3$	2.1-2.5	$\sim 10^6$		
$\text{Al}_2\text{O}_3/\text{BaSnO}_3$	17.8	$>10^5$	3.2	4.38×10^{13}
$\text{HfO}_2/\text{BaSnO}_3$	24.9	$>10^6$	0.42	9.89×10^{12}

Table 3. The device performances such as μ_{FE} , $I_{\text{on}}/I_{\text{off}}$ ratio, S , D_{it} were represented with previous reported results based on STO and KTO. [41-45, 90, 103]

4.4.4 Ambient aging

To check the durability of FETs based on BLSO, author investigates the ambient aging of $\text{Al}_2\text{O}_3/\text{BLSO}$ FET device.

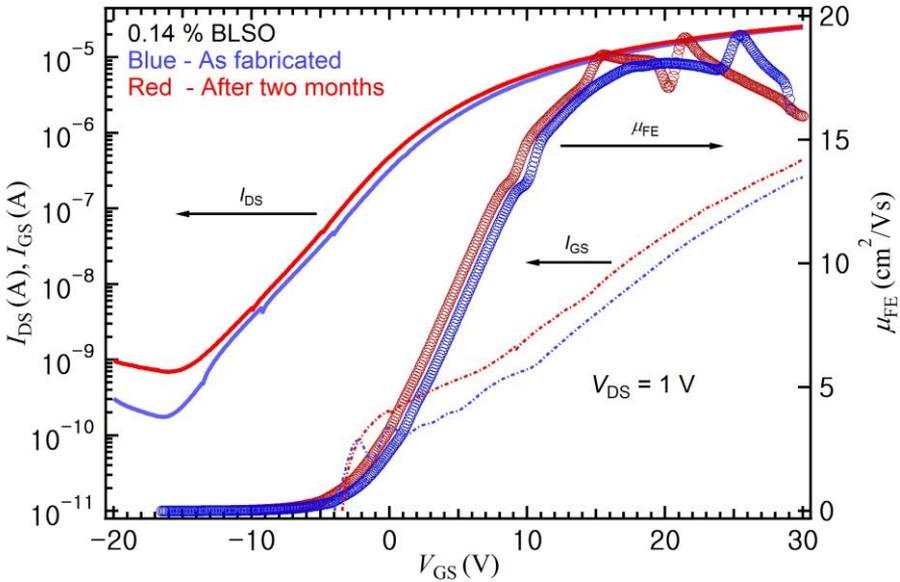


Figure 4. 12. $I_{\text{DS}}-V_{\text{GS}}$, $\mu_{\text{FE}}-V_{\text{GS}}$, and $I_{\text{GS}}-V_{\text{GS}}$ plots for the as fabricated and two months-aged FET device of 0.14 % BLSO were shown. [90]

To that, author measures again the transfer characteristics after two months. In Fig 4. 12., the transfer characteristics, such as μ_{FE} - V_{GS} plots, and gate leakage current (I_{GS} - V_{GS}) of the as-fabricated and the aged FET devices based on BSO, are represented. As seen, author couldn't see the noticeable change in transfer characteristics in FET device based on BSO active layer. Also author believes that the slight increase of the off current in subthreshold region might come from the large photoconductivity of the BSO material. [107] In previous research, by contrast, other FET devices such as SnO₂ and IGZO FETs have been reported V_{th} shifts and degradation of the current level in active layer by ambient aging. [108,109] It is known that the origin of this phenomenon is the absorption of oxygen on the surface. In this result, author could confirm the special material properties of BSO again.

Chapter 5

Field effect transistor based on BaSnO₃ with epitaxial gate oxide

In order to obtain a better performance than amorphous gate dielectric/BLSO FET devices, the author demonstrated FET devices using epitaxial gate dielectrics. Of the criteria for choosing a gate dielectric, the dielectric parameters of dielectrics such as SSO, SZO, BZO, SHO, BHO, and LIO were considered. Then, the dielectric properties of LIO and BHO were explored. After this, the all-epitaxial FET device was fabricated and its device performance was measured. In the author's knowledge, this demonstration of an all-epitaxial FET device is the first in the history of conventional FETs. The detailed process, from

choosing the gate dielectric to measuring the performance of the device, is as follows.

5.1 Epitaxial gate oxide candidate

To demonstrate the all-epitaxial perovskite FET, the author has first tried to find an appropriate perovskite oxide. The candidate materials are shown in Figure 5.1. LIO was used as a buffer layer to enhance the electrical properties, since the pseudo-cubic lattice constant of LIO is ideally matched to that of BSO with a value of 4.116 \AA , as mentioned in Chapter 2. However, previous studies on LIO are relatively scarce. So in the next section, we will present its dielectric properties.

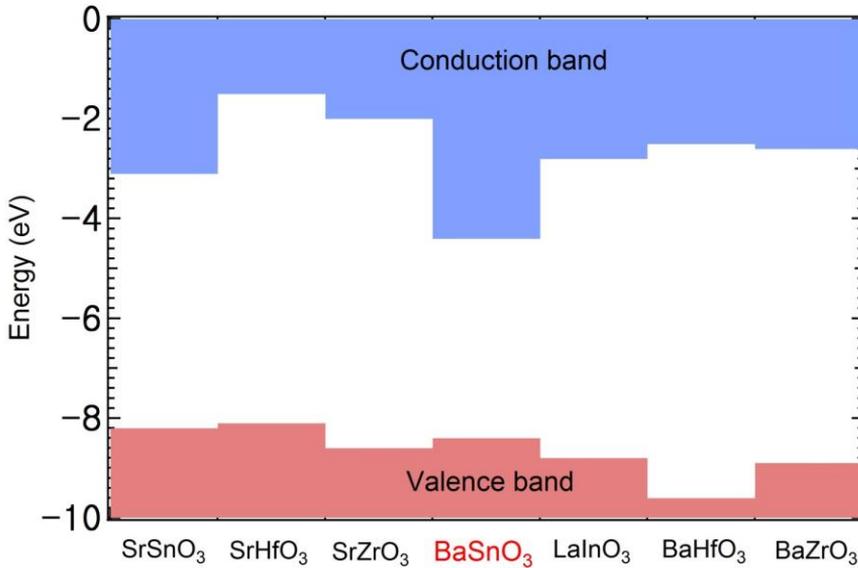


Figure 5.1. The band alignment between SrSnO₃, SrHfO₃, SrZrO₃, BaSnO₃, LaInO₃, BaHfO₃, and BaZrO₃. [91, 93, 122-125]

SHO, SZO, BHO, BZO, and SSO have been investigated as high-k dielectric materials in conventional Si industries. The dielectric properties of amorphous and polycrystalline SHO and BHO were reported by Lupina *et al.* [111, 112,

115-117] In the epitaxial growth of SrHfO₃, the cubic crystal structure demanded a strict control over the deposition condition. It is consistent with previous reports. [117] The results are shown in Appendix C. Not only is SSO a dielectric candidate, but a high electrical transport of SSO as a semiconductor was predicted and its transport properties were reported. [118-120] Some theorists presumed that this high transport property was due to its small effective mass compared with BSO, since the value is much smaller than in BLSO thin films. [118, 120, 121] However, the author thought that the origin of this result might be the structural difference, in particular, the bonding angle of the O-Sn-O conduction channel, and the large band gap.

Materials	Breakdown field (MV cm ⁻¹)	Dielectric constant	Modulation capacity(cm ⁻²) (oxide thickness 100 nm)
SrSnO ₃	—	12	
SrZrO ₃	0.4	60	1.33×10 ¹³
BaZrO ₃	0.4	40	8.85×10 ¹²
SrHfO ₃	—	35	
BaHfO ₃	2.7	23–45	3.47–5.27×10 ¹³
LaInO ₃	3.13	38.7	6.70×10 ¹³

Table 4. Breakdown field, static dielectric constant, and calculated modulation capacity of gate dielectric candidates such as SSO, SZO, BZO, SHO, BHO, and LIO. [91,110-117,122]

Here, the author evaluated the modulation capacity by using known parameters of each gate dielectric such as dielectric constant and breakdown field. The results are shown in table 4. SZO and BZO have a small modulation capacity due to their weak breakdown strength, even though they have a large dielectric constant. In fact, the author deposited epitaxial SZO thin films and fabricated a BLSO/SZO/BLSO capacitor to measure its dielectric properties. Unfortunately, the results were not consistent with the characteristics in previous reports, due to the high leakage current in the SZO dielectric. However, SZO

was used on a SZO/BLSO interface to compare with the interface of LIO/BSO in chapter 6. The author has attached the results on the crystallinity of SZO in Appendix C, too. LIO and BHO were chosen as epitaxial gate dielectrics from considering overall conditions such as lattice matching with BSO and their dielectric properties.

5.2 Investigation of LaInO_3 and BaHfO_3 gate dielectrics

No one has tried to fabricate epitaxial LIOs and BHOs because they need high temperature to form an epitaxial crystal. The author grew epitaxial thin films of LIO and BHO to demonstrate all-epitaxial FETs based on BSO. The fabrication conditions are as follows: The author used a KrF excimer laser ($\lambda = 248 \text{ nm}$) with a repetition rate of 10 Hz and the laser energy density in the range of 1 ~1.5 J/cm^2 , in an oxygen environment with 100 mTorr partial pressure, at a substrate temperature of 750 °C.

5.2.1 Crystallinity of LaInO_3 and BaHfO_3

The author prepared a 100 nm thick BSO, and 100 nm thick LIO with a 10 nm of BSO under layer, a 100 nm thick BHO, a 100 nm thick BHO thin films with a 10 nm of BSO under layer on STO substrates. The θ - 2θ curves and ω -rocking curves are shown in Fig 5. 2. As we can see, only reflections from the (00 l) plane of LIO, BHO, BSO, and STO substrates were observed without a secondary phase or randomly oriented grains. It implies that all films exhibit preferred orientation along the c-axis, and we confirm the epitaxial growth of the thin films.

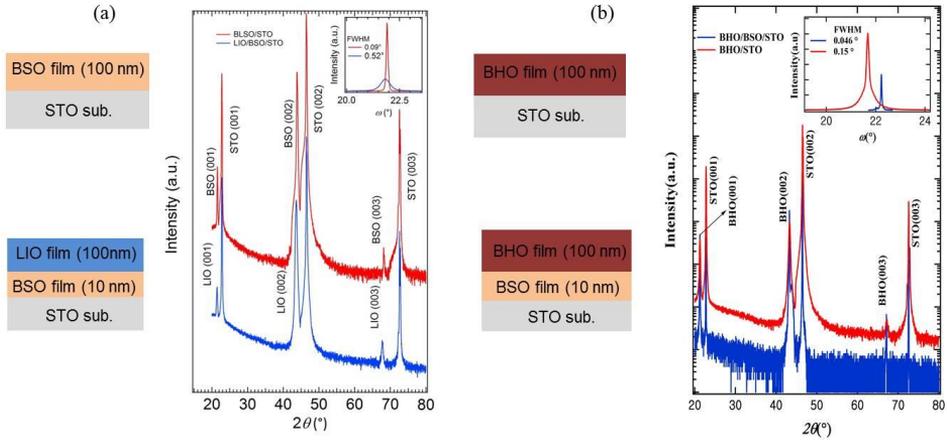


Figure 5. 2. XRD $\theta - 2\theta$ and ω -rocking curves of BSO, LIO, BHO. (a) The $\theta - 2\theta$ for a 100 nm thick BSO and a 100 nm thick LIO with 10 nm BSO under layer on STO substrates were plotted. (b) The $\theta - 2\theta$ for a 100 nm thick BHO and a 100 nm thick BHO with 10 nm BSO under layer on STO substrates were plotted. Insets in (a) and (b) denote the ω -rocking curves of each thin film. [91]

5.2.2 Optical band gap of LaInO_3 and BaHfO_3

Due to their large band gap, we used LAO ($E_g = 5.3$ eV) and $r\text{-Al}_2\text{O}_3$ ($E_g \sim 9$ eV) substrates to measure the optical band gap of LIO and BHO. Additionally, in the film growth of the BHO, a MgO ($E_g \sim 8$ eV) thin layer, which is known to be an acceptable buffer layer, was grown on a $r\text{-Al}_2\text{O}_3$ substrate, and then a BHO layer was deposited for epitaxial growth. It is known that it is possible to grow MgO (001)/ $r\text{-Al}_2\text{O}_3$ films epitaxially[1120]. [128] The results of the optical absorption measurements of LIO and BHO are presented in Figure 5. 3. The optical absorption coefficient (α) was evaluated using the formula: [129]

$$\alpha = \frac{1}{d} \ln \frac{(1-R)}{T} \dots\dots\dots(5.1)$$

Where d , T , and R are the thickness, the transmittance, and reflectance of the films, respectively. Here, we assumed that $R = 0$. The band gap of LIO and BHO, which is evaluated by using a linear extrapolation of the $(\alpha\hbar\omega)^2 - \hbar\omega$ curves, were obtained as 5.0 eV and 6.1 eV, respectively.

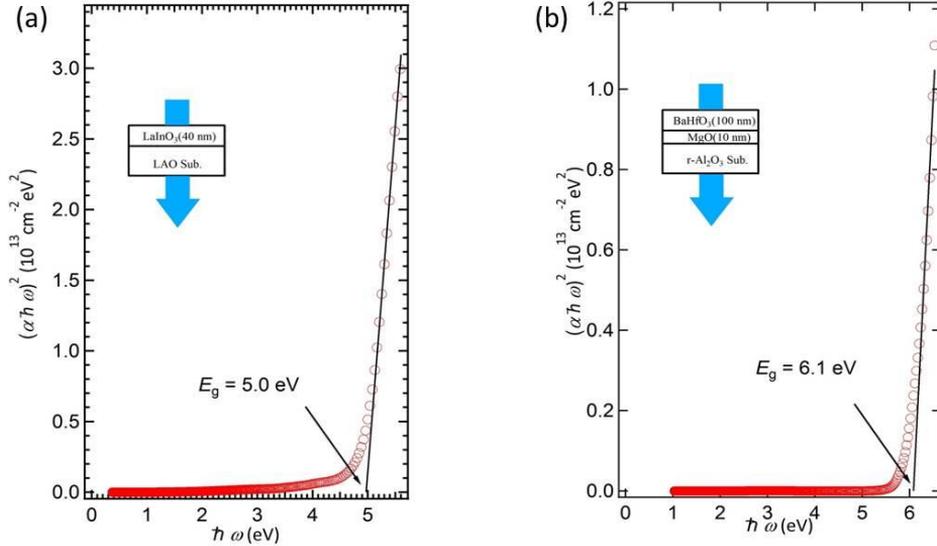


Figure 5. 3. Optical absorption of LIO and BHO. The absorbance of (a) LIO (40 nm)/LAO substrate and (b) BHO (100 nm)/MgO (10 nm)/ r-Al₂O₃ substrate is measured. $\alpha^2\hbar\omega$ versus $\hbar\omega$ plots of LIO and BHO films. [91]

5.2.3 Breakdown field of LaInO₃ and BaHfO₃

The results of the breakdown field measurement of LIO and BHO are shown in Fig x. Their breakdown strengths were found to be 3.13 and 2.9 MVcm⁻¹ for LIO and BHO, respectively. These values are consistent with previous results in table 4.

➤ Conduction process in gate dielectrics

The most prominent conduction mechanism in dielectric materials is the tunneling under a high field. The wave function can transmit through the

potential barrier, and this causes a tunneling emission. This most famous conduction mechanism is shown in figure 5. 4.

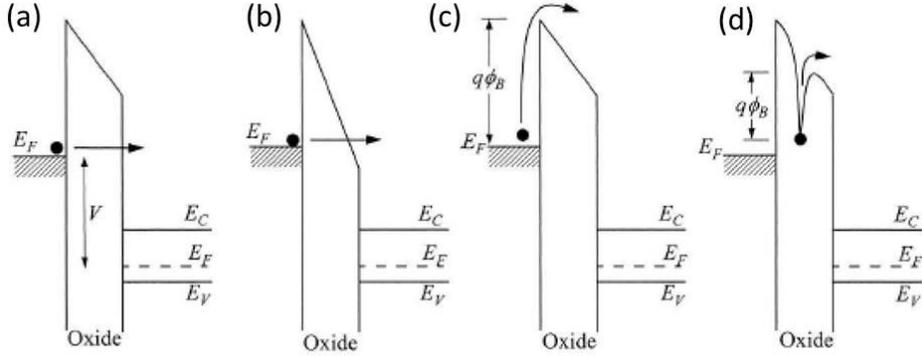


Figure 5. 4. Conduction process in gate dielectrics. Energy-band diagrams showing conduction mechanisms of (a) direct tunneling, (b) F-N tunneling, (c) thermionic emission, and (d) Frenkel-Poole emission were shown. [92]

The CB offsets with BSO were calculated by leakage analysis as shown in Table 5. Insets denote the characteristic plot of the Fowler-Nordheim (F-N) tunneling used to calculate the barrier height between BSO and the two dielectrics, LIO and BHO. The barrier height can be calculated by the given equation

$$J = AE^2 e^{-\frac{B}{E}} \dots \dots \dots (5.1)$$

Where $A = \frac{q^3 m_{semi}^*}{16\pi^2 \hbar m_{diel}^* q\Phi}$ and $B = \frac{4 \sqrt{2m_{diel}^* (q\Phi)^3}}{3\hbar q}$.

The calculated barrier heights were 1.15 eV and 0.51 eV, using $m_{LIO} = 0.46 m_0$ and $m_{BHO} = 0.6 m_0$, respectively. The Fermi level offset for the conduction band of BSO must also be considered, because 4 % BLSO is in the degenerate doping region. The difference of energy in BSO was calculated by a given relation, assuming that the BSO band resembles a parabolic band.

Processes	Fomulae	A	B
Direct Tunneling	$\frac{A}{C_1} E^2 e^{-C_2 B/E}$	C_1 and C_2 are functions of E , ϕ , and t_{diel}	
Ford-Nordheim Tunneling	$A E^2 e^{-B/E}$	$\frac{q^3 m_{semi}^*}{16\pi^2 \hbar m_{diel}^* q \phi}$	$\frac{4\sqrt{2m_{diel}^* (q\phi)^3}}{3\hbar q}$
Thermionic Emission	$A T^2 e^{-q(\phi - B\sqrt{E})/kT}$	$\frac{qm^* k^2}{2\pi^2 \hbar^3}$	$\frac{\sqrt{q}}{\sqrt{4\pi\epsilon}}$
Poole-Frenkel Emission	$A E e^{-q(\phi - B\sqrt{E})/kT}$	$q\mu \sqrt{\frac{N_c N_D}{2}}$	$\frac{\sqrt{q}}{\sqrt{\pi\epsilon}}$

Table 5. The basic conduction processes in gate dielectric. m_{semi}^* , m_{diel}^* , and Φ means effective mass of semiconductor, effective mass of dielectric, and barrier height, respectively.

$$E_F - E_{CB,BLSO} = \frac{\hbar(3\pi^2 n)^{2/3}}{2m_{BLSO}^*} \dots\dots\dots (5.2)$$

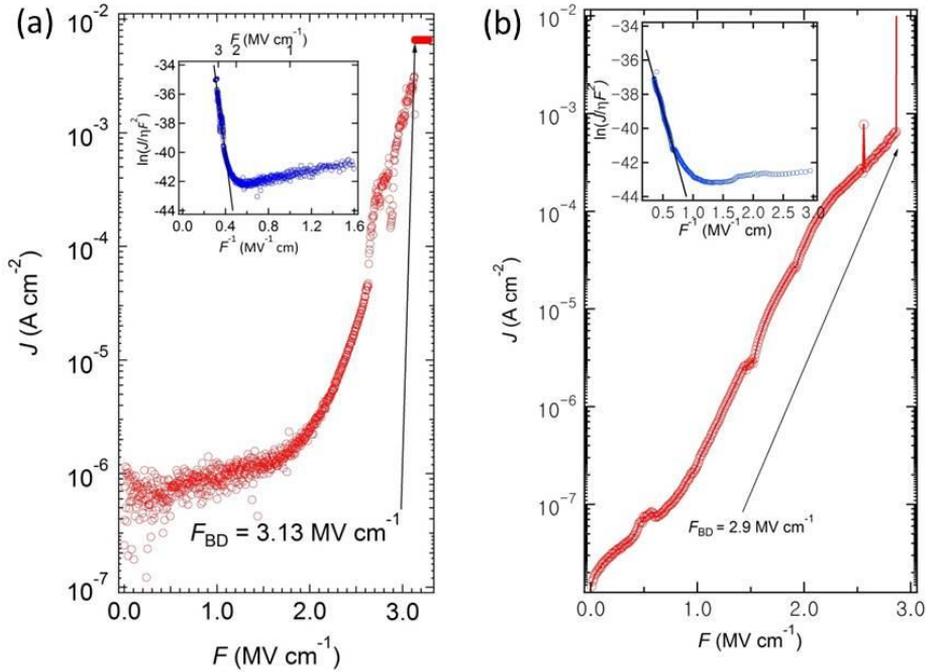


Figure 5. 5. J - E characterization of BLSO/LIO/BLSO and BLSO/BHO/BLSO capacitor is shown in (a) and (b). Insets denote the characteristic plot of the F-N tunneling process. [91]

Where $n = 3.7 \times 10^{20} \text{ cm}^{-3}$ and $n = 5.0 \times 10^{20} \text{ cm}^{-3}$ for LIO and BHO, respectively. The conduction band offset between BSO and the two dielectrics was found to be 1.6 eV and 1.1 eV for LIO and BHO, respectively. Especially, the band offset between BSO and BHO showed a smaller value than previously reported results. If the dielectric had some defects, the lower value of the barrier height could be explained, since we calculated the barrier height assuming that the dielectric is a perfect bulk with no defects.

5.2.4 Dielectric constant of LaInO_3 and BaHfO_3

The K value was evaluated by the equation described in (4. 18). From C - F measurements, the dielectric constants of LIO and BHO have been found to be 38.7 and 37.8.

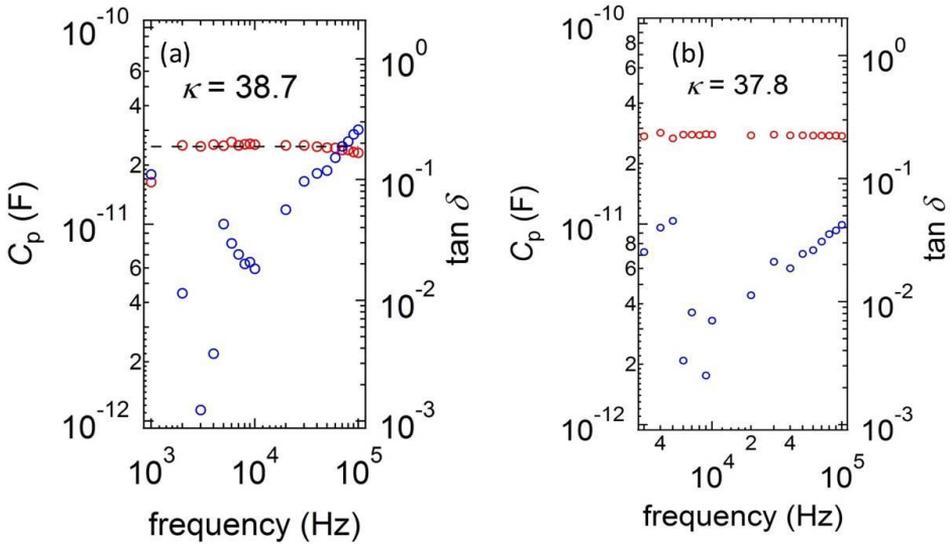


Figure 5. 6. C - F curves for BLSO/LIO/BLSO and BLSO/BHO/BLSO capacitor. (a) C - F characteristic of BLSO/LIO/BLSO capacitor and (b) C - F characteristic of BLSO/BHO/BLSO capacitor are shown. Filled and unfilled makers denote the capacitance and dissipation factor, respectively. [91]

This high value of K may come from the high crystallinity of LIO and BHO. Once more, based on these material parameters, in addition to the lattice match with BSO, we fabricated the all-epitaxial FETs device.

5.3 Device utilizing LaInO_3 and BaHfO_3 gate dielectrics

The device fabrication process is mostly the same with the process for amorphous gate dielectric/BLSO FETs, except that the growth of the source-drain and gate electrode. We fabricated BLSO as the source-drain and gate electrode by using a SUS and Si stencil mask, respectively, with the PLD technique in an oxygen partial pressure of 100 mTorr at a substrate temperature of 750 °C. A more detailed process of fabricating TFT devices of LaInO_3 or BaHfO_3 /BLSO on a STO substrate are as follows. First, a 110 nm BSO buffer layer, the selected buffer layer thickness for the optimization of the active layer properties such as electrical and surface properties, was deposited on a STO substrate by PLD with previous conditions. After then, the author deposited the lightly-doped semiconducting channel layer through a Si stencil mask with the same condition. As the source and drain contacts, BLSO was deposited with a P_{O_2} of 100 mTorr and a temperature of 750 °C by PLD using a stainless steel mask. Then the LaInO_3 or BaHfO_3 gate dielectric layer was deposited by PLD on the channel layer. And finally, BLSO was deposited again on the device as a gate electrode in a small overlap with the source and drain contact layer to minimize the leakage current and to maximize the possible applied bias. The cross-sectional diagram and an optical microscope image of LIO/BLSO FET device are presented in Fig 5. 7.

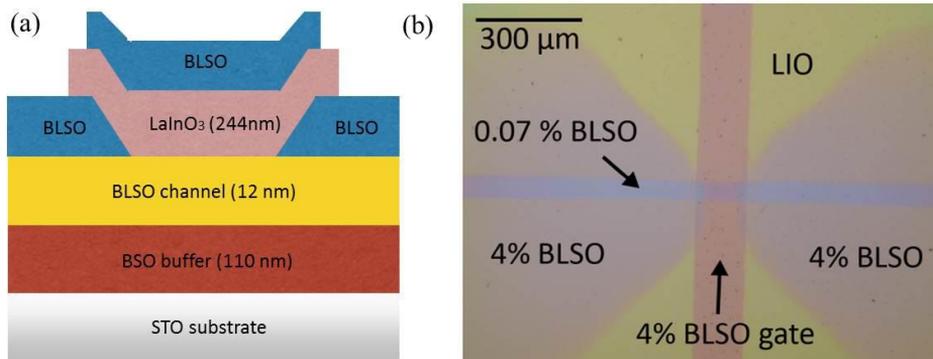


Figure 5. 7. (a) The cross-sectional diagram and (b) an optical microscope image of LIO/BLSO FET device. [91]

The channel length and width of LIO/0.07 % BLSO TFTs were 118 and 56 μm , respectively. The thickness of LIO on the 0.07 % BLSO active layer was 244 nm. The channel length and width of BHO/BLSO FET were 140 and 100 μm , respectively. The thickness of BHfO_3 on the 0.5 % BLSO active layer was 126 μm . As can be seen, the results show a well-defined image of the device. This fivefold high temperature thermal process in demonstrating BSO FETs are possible because BSO is a thermally stable material with an atomically flat surface. Moreover, this demonstration of a conventional all-epitaxial FET device is the first of its kind in the world and provides an interesting challenge to demonstrate a high temperature electronic device.

5.3.1 Output characteristics of $\text{LaInO}_3/\text{BLSO}$ and $\text{BaHfO}_3/\text{BLSO}$ FETs

The output characteristics of the LIO/ 0.07 % BLSO and BHO/0.5 % BLSO are shown in Fig. 5. 8. The two devices show clear output characteristics which are the same with amorphous gate dielectric/BLSO FET as shown in Chapter 4. In (a) and (b), the I_{DS} is plotted against the V_{DS} for various fixed valued of V_{GS} .

As seen, I_{DS} is proportional to V_{DS} where V_{DS} is smaller than $V_{GS}-V_{th}$ in the linear region.

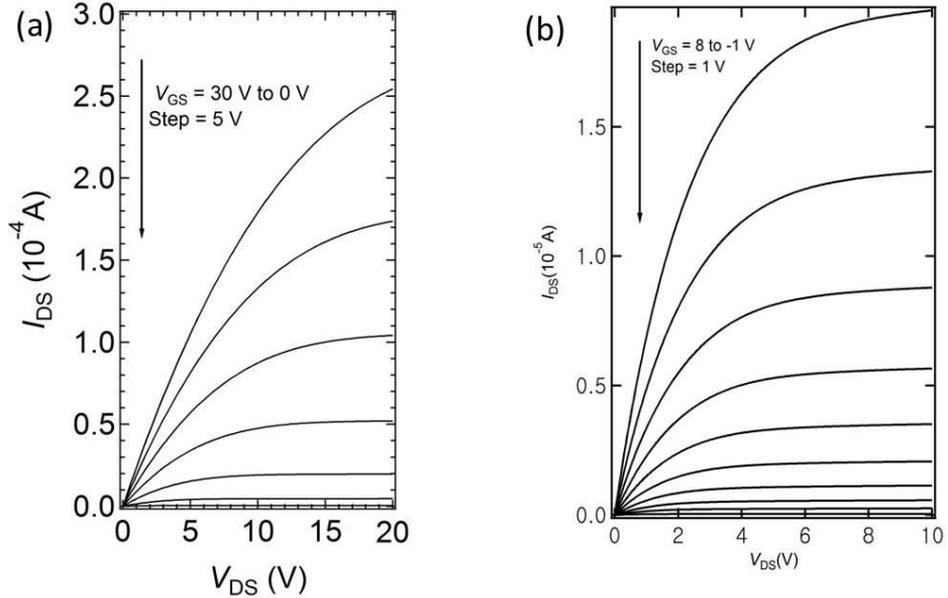


Figure 5. 8. Output characteristic of (a) LIO/BLSO and (b) BHO/BLSO TFTs. Gate voltages of (a) and (b) are varied from 0 V to 30 V in 5 V steps and from -1 V to 8 V in 1 V steps, respectively.[91]

I_{DS} deviates from linear behavior as V_{DS} increases. Finally, the current is saturated in the region where $V_{GS}-V_{th} < V_{DS}$. Of course, these behaviors are parallel to the fundamental output characteristics (I_{DS} vs. V_{DS}) of a MOSFET device as described by the linear region, non-linear region, and the current saturation region. The devices again clearly show the behavior of an n-type accumulation mode FETs; under positive and negative V_{GS} , I_{DS} is increased and decreased as V_{GS} positively and negatively increases, since the carriers are accumulated and depleted in the active layer by V_{GS} as commented in Chapter 4, respectively. Finally, as we can see that in (b), compared to LIO/BLSO, a lower V_{GS} is required to accumulate the carriers of the active layer. This change might

originate from the difference in modulation capacity from using a thinner layer of BHO while the two gate dielectrics have the almost same dielectric constants.

5.3.2 Transfer characteristics of LaInO₃/BLSO and BaHfO₃/BLSO FETs

The transfer characteristics, such as $I_{ds}-V_{gs}$, μ_{FE} , I_{on}/I_{off} ratio and subthreshold swing (S), are shown in Fig 5. 9. (a) and (b) represent the transfer characteristics of the both LIO/0.07% BLSO and BHO/0.5% BLSO FETs.

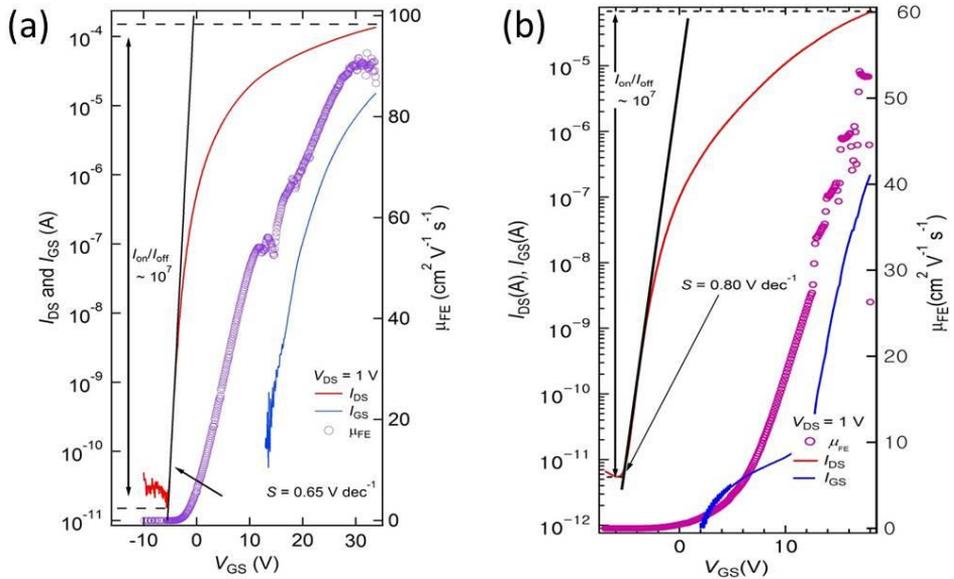


Figure 5. 9. The transfer characteristic of FETs devices. (a) $I_{DS}-V_{GS}$ and $\mu_{FE}-V_{GS}$ of the FET devices for LIO/0.07 % BLSO were represented. The I_{on}/I_{off} ratio at V_{GS} of -10 and 30V exceeds 10^7 . (b) $I_{DS}-V_{GS}$ and $\mu_{FE}-V_{GS}$ of the FET device for BHO/0.5 % BLSO were plotted. The I_{on}/I_{off} ratio at V_{GS} of -4 and 14V exceeds 10^7 . [91]

As we can see, sufficient current enhancement due to carrier accumulation in the active layer can be achieved by applying a positive gate bias in both devices.

The mobility of the devices was calculated by using the general relationship shown in chapter 4.1. The calculated maximum mobility of LIO/0.07 % BLSO and BHO/0.5 % BLSO are 90 and 53.7 $\text{cm}^2\text{V}^{-1}\text{s}^{-1}$, respectively, for $V_{\text{DS}} = 1 \text{ V}$. The $I_{\text{on}}/I_{\text{off}}$ ratios are about 10^7 and 10^7 for LIO/0.07 % BLSO and BHO/0.5 % BLSO FETs, respectively. Also, the value of S was found to be 0.65 Vdec^{-1} and 0.8 Vdec^{-1} for LIO/0.07% BLSO and BHO/0.5 % BLSO FETs, respectively. From these values, we can evaluate D_{it} as 8.67×10^{12} and $2.06 \times 10^{13} \text{ cm}^{-2}\text{eV}^{-1}$ for each device. These small values explain why the performances of these epitaxial gate dielectric/BLSO FET devices are better than amorphous gate dielectric/BLSO FET devices. The calculated values such as mobility, $I_{\text{on}}/I_{\text{off}}$ ratio, subthreshold swing, and interface trap density compared with previously reported performances of FET devices based on perovskite oxides are presented in table 6.

Device	$\mu_{\text{FE}}(\text{cm}^2/\text{Vs})$	$I_{\text{on}}/I_{\text{off}}$ ratio	$S(\text{V dec}^{-1})$	$D_{\text{it}}(\text{eV}^{-1} \text{ cm}^{-2})$
$\text{Al}_2\text{O}_3/\text{KaTiO}_3$	0.4	10^4		
$\text{Al}_2\text{O}_3/\text{SrTiO}_3$	0.1	10^2		
$\text{CaHfO}_3/\text{SrTiO}_3$	0.4-0.5	$\sim 10^5$		
$\text{CaHfO}_3/\text{SrTiO}_3$	0.4	$\sim 10^5$		
$\text{DyScO}_3/\text{SrTiO}_3$	2.1~2.5	$\sim 10^6$		
$\text{Al}_2\text{O}_3/\text{BaSnO}_3$	17.8	$>10^5$	3.2	4.38×10^{13}
$\text{HfO}_2/\text{BaSnO}_3$	24.9	$>10^6$	0.42	9.89×10^{12}
$\text{LaInO}_3/\text{BaSnO}_3$	90	10^7	0.65	8.67×10^{12}
$\text{BaHfO}_3/\text{BaSnO}_3$	53.7	10^7	0.8	2.06×10^{13}

Table 6. The device performances such as μ_{FE} , $I_{\text{on}}/I_{\text{off}}$ ratio, S , D_{it} were represented with previous reported results based on STO and KTO. [41-45, 90, 91, 103]

As expected, these devices obviously show higher performance than previously reported FET devices based on perovskite oxides. This again provides evidence to the superior material properties of BSO, such as high mobility, atomically flat surface, and oxygen stability, and also shows the potential for the application of BSO to transparent high-mobility FET devices.

Especially, the LIO/BLSO device shows superior performance compared with previously reported devices based on binary or well-known semiconductor oxides such as ZnO, SnO₂, and IGZO. The author concluded that this result originates not only from the epitaxial lattice matching, but also the special interface properties between LIO and BSO. In an appendix **D**, the cross-sectional TEM image of a LIO/BSO interface is shown to confirm the perfect lattice matching between LIO and BSO. In fact, the author was able to observe the conductance enhancement of the BLSO active layer after a LIO/BLSO interface was formed. This interesting phenomenon will be presented in the next chapter.

Chapter 6

LaInO₃/BaSnO₃

interface

In this chapter, the author shows the some experimental results to understand and to explain the interesting phenomena in LIO/BSO interface. The origin isn't clearly explained yet. However the author strongly believes that these experimental results provide the understanding and explanation of LIO/BSO interface. The conductance enhancement behavior is measured during fabrication of LIO/BSO FET devices compared with our BHO/BLSO FET device through the monitoring the conductance before and after interface formed. Of course, in fabrication of Al₂O₃/BLSO and HfO₂/BLSO devices, the conductance enhancements of active layers are observed after interface formed between BSO and gate dielectrics and these enhancements could be eliminated by thermal annealing in O₂ atmosphere. So the author thinks that the origin of these phenomena is hydrogen effect during ALD process as mentioned in section

4.4.1. First time, the author thought that the origin of this phenomenon in LIO/BSO is same with LAO/STO polar interface, well-known interface in many articles, because LIO is the polar material.[130-132] However, the result of La doping dependence on the enhancement of LIO/BSO interface shows that it couldn't be explained easily by well-known $\text{LaAlO}_3/\text{SrTiO}_3$ (LAO/STO) polar interface theories. The author sincerely hopes that these experiments could be a help to understand this behavior.

6.1 Conductance enhancement on $\text{LaInO}_3/\text{BaSnO}_3$ interface and La doping dependence

When the author fabricated the devices, the author and co-worker could see the conductance enhancement in LIO/BLSO interface. Because the author demonstrates totally four LIO/BLSO devices, the three data points of La concentration on BSO are represented. But the author thinks that it is suitable to see and confirm the La concentration dependence of sheet conductance enhancement on LIO/BLSO interface. The results are shown in Figure 6. 1. (a) and (b) show the microscope image and schematic of LIO/BLSO devices, respectively. In (c), the red and blue symbols denote the initial conductance by La doping on BSO layer and final conductance after LIO/BLSO interface formed, respectively. As we can clearly see, the sheet conductance enhancements were obtained after LIO/BLSO interface formed except the LIO/undoped BSO interface. About two or three orders of magnitude enhancements were observed. And it depends on La concentration in BLSO layer. This result is very important because the LAO/STO interface experiment is investigated for bare STO layer, generally. All measurements are investigated

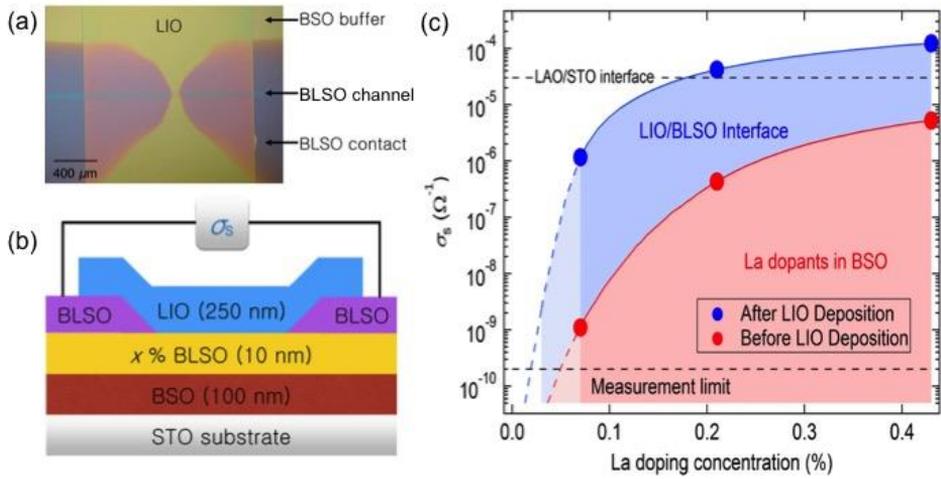


Figure 6.1. Device structure and results of conductance measurements. (a) and (b) denote the microscope image and schematic of LIO/BSO device. (c) represents the results of conductance measurements for before and after LIO/BSO interface formed.

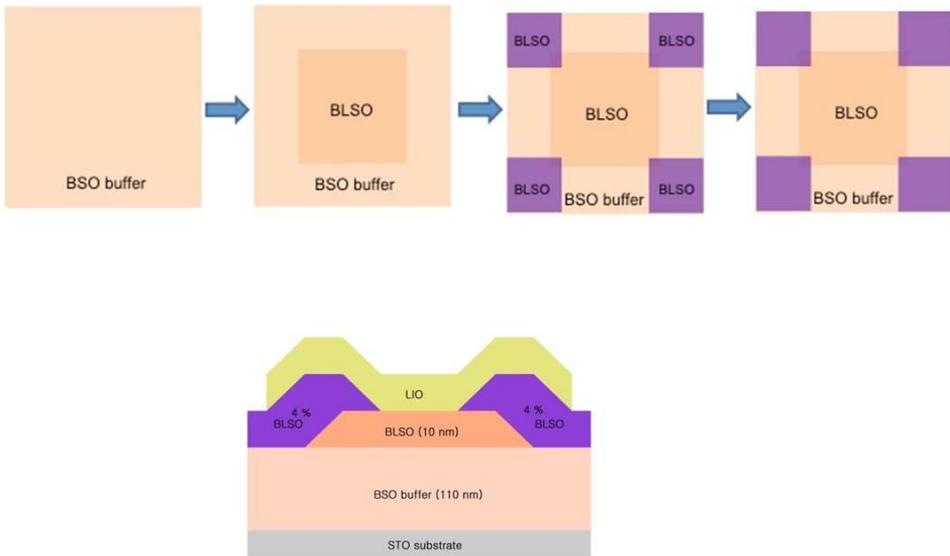


Figure 6.2. Fabrication process to measure LIO/BSO interface transport properties.

by 2 probe measurement. So, in order to minimize the effect of contact resistance and to obtain more detail parameters such as carrier density and mobility, the devices are prepared in Vander-Pauw geometries using Si stencil mask. The new approach is as follows and shown in Fig 6. 2.

First, 110 nm thick undoped BSO buffer layer is deposited on a STO substrate. Second, 10 nm thick $\text{Ba}_{1-x}\text{La}_x\text{SnO}_3$ layers are deposited in a $2 \times 2 \text{ mm}^2$ square shape using a Si stencil mask. Third, 50 nm thick 4 % BLSO contact layers are deposited using another Si mask at the four corners of the BLSO layer with overlapped areas of $0.2 \times 0.2 \text{ mm}^2$. After growth, the sheet conductance and/or Hall measurements depending on conductivity of BSO or BLSO layers are performed. Then, 10 nm thick LIO layer is deposited over the area of $3 \times 3 \text{ mm}^2$ to completely cover the BLSO layer. Finally, the sheet conductance and/or Hall measurement is performed again. The results are shown in Fig 6. 3. Before LIO/BLSO interface formed, the author couldn't investigate the Hall effect measurement of BLSO layers due to their high resistance below 1% La concentration while it could be possible above 1% La concentrations. After interface formed, the author could measure the mobility and carrier density by Hall effect measurement from 0.2 % La doped BSO. As we can see, the values sheet conductance of BLSO layers are increasing as the La concentration is increasing and the maximum enhancement of sheet conductance exceeds 10^4 . In the higher doping region the enhancement of sheet conductance is decreased. When we calculate, the difference of carrier density between before and after interface formation of LIO/BSO interfaces is about $4.5 \times 10^{13} \text{ cm}^{-2}$. This value is approximately same with induced carrier density in LAO/STO interface. However, this doping dependence on LIO/BSO interface can't simply explain using theories of LAO/STO.

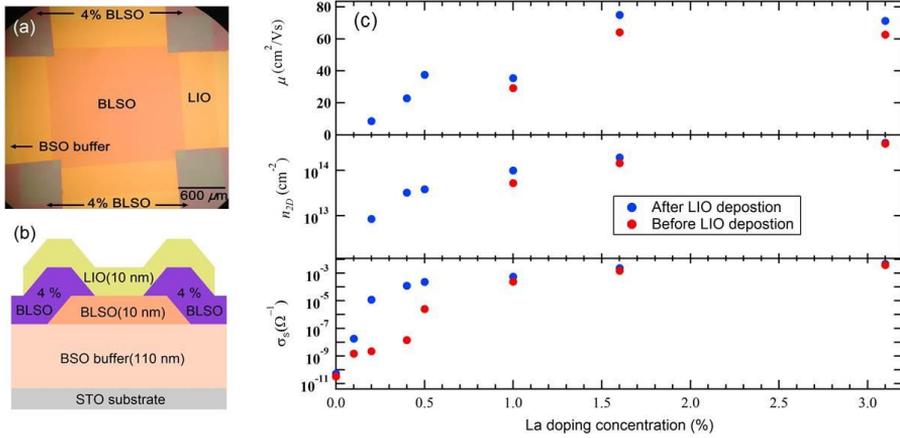


Figure 6.3. (a) A top view of a LIO/BLSO interface. (b) The schematics of LIO/BLSO interfaces. (c) The sheet conductance changes, the mobility, and n_{2D} as a function of the La concentration in the LIO/BLSO interfaces.

6.2 LaInO_3 thickness dependence of $\text{LaInO}_3/\text{BaSnO}_3$ interface

Owing to understand these phenomena, additionally, the author explores the LIO thickness dependence on LIO/BSO interface. The author investigates the transport properties for LIO/0.2 % BLSO interface because the distinguishable enhancement of transports on LIO/BSO interfaces in La concentration between 0.2% and 0.4%. The results are shown in Fig 6. 4. The fabrication process is mentioned in section 6.2. Just only the LIO thickness is varied. As we can see, the sheet conductance is enhanced as increasing LIO thickness and crosses over at special thickness. The sheet conductance reaches the maximum value just in 2 or 3 unit cells. Even the sheet conductance is slightly increased in 1 unit cell of LIO. It seems that the critical thickness isn't in this system compared with LAO/STO interface. And it is maintained in some thickness, and then slowly

decreases as increasing the LIO thickness. In thick LIO region, both the carrier density and the mobility are decreased as increasing the LIO thickness. The author believes that the dislocation effect maintains in this system even though the author has tried to minimize the dislocation effect. So the study and/or method of limitation of dislocations in this system are needed in order to investigate more complete research. From results, the author thinks that any polarization, such as spontaneous polarization in LIO layer, piezoelectric polarization due to epitaxial stress, and/or flexoelectric polarization due to the strain gradient near the interface, might exist in LIO/BSO interface.

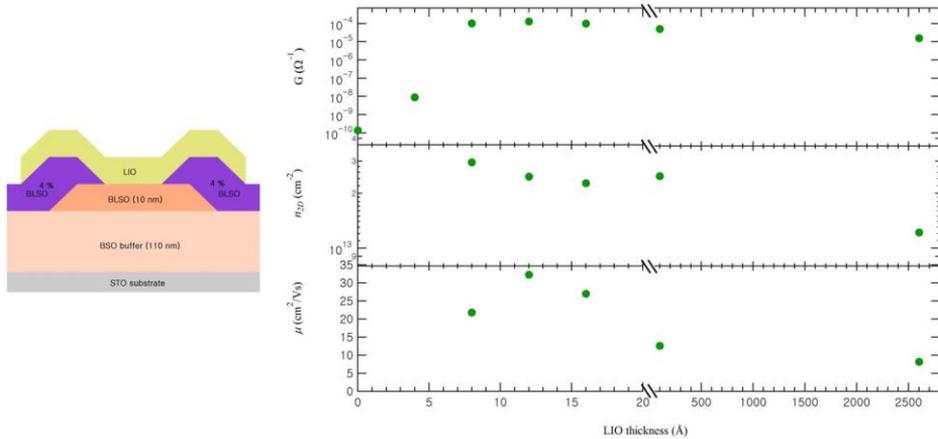


Figure 6. 4. Variation of the sheet conductance, the 2D carrier density, and the electron mobility as a function of LIO thickness in the LIO/BLSO interface.

Next, the author could confirm the polarization effect on LIO/BLSO interface by comparison LIO/BLSO and LIO/BSO/BLSO interfaces. The author demonstrates the new structure using undoped BSO layer on the top of 1 % BLSO layer. These results are shown in Fig 6. 5.

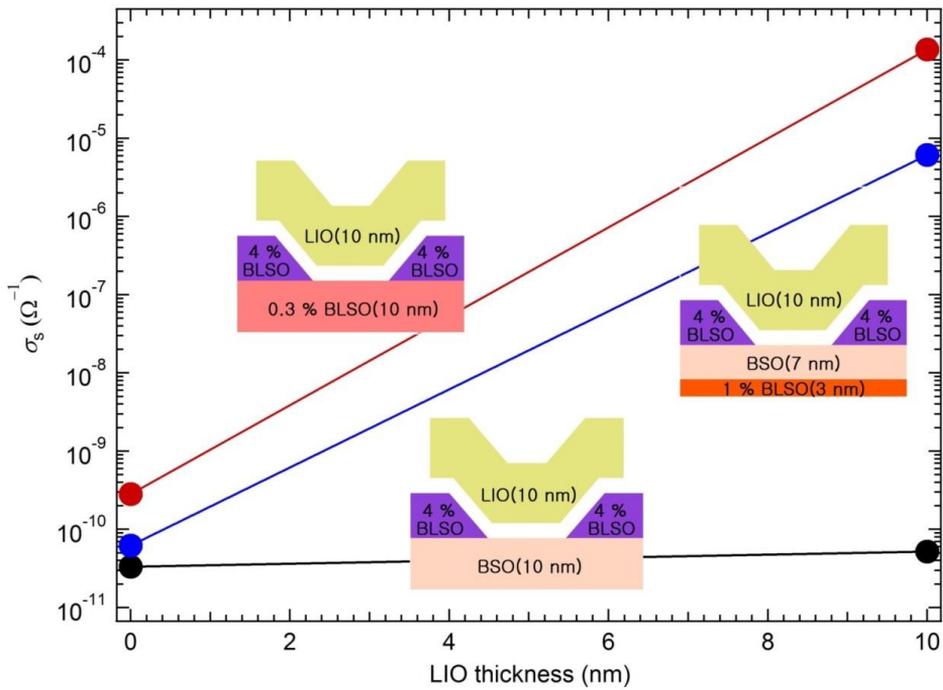


Figure 6. 5. The sheet conductance change measurement after the interface formation with LIO for different three different structures.

As expected, there isn't observed any change in sheet conductance after LIO/undoped BSO interface formed, while the large enhancement of sheet conductance is monitored after LIO/0.3 % BLSO interface formed which is consistent with result in Fig 6. 3. (c). However the significant enhancement of sheet conductance is obtained in LIO/BSO/1 % BLSO interface. Of course, any change of sheet conductance wasn't observed before LIO/BSO/1 % BLSO interface formed. However, the sheet conductance enhancement is a little smaller than LIO/0.3 % BLSO. It seems that the sheet conductance enhancement might be caused by any polarization on LIO/BLSO interface. Moreover, the author thinks that this result can support not only evidence of any polarization in LIO/BSO interface but also the evidence for absence of La cation diffusion.

6.3 polar vs non-polar interface

Finally, the author investigates the enhancement of sheet conductance in the polar interface such as LIO/BLSO and the non-polar interface such SZO/BLSO and BHO/BLSO. Through these investigations, the author expects to know the fact that polar interface is needed to enhance the interface conductance or not.

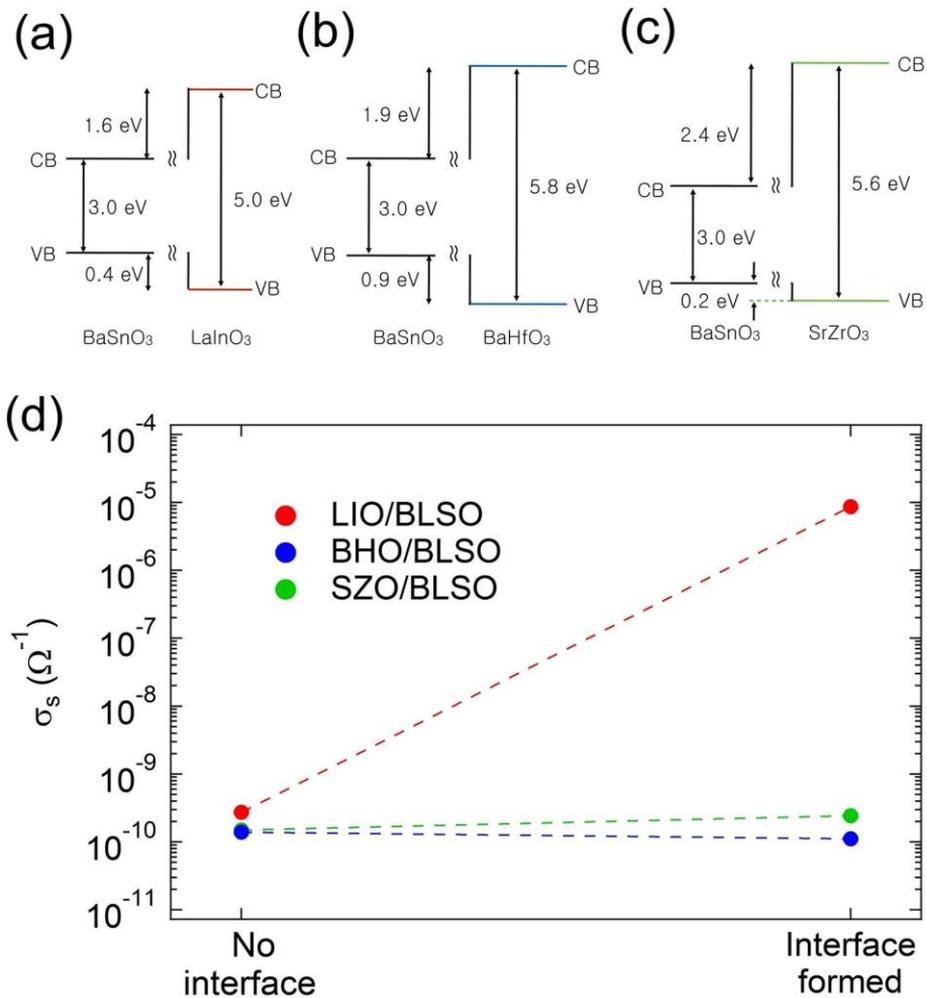


Figure 6. 6. Band alignment and result of sheet conductance measurement before and after interface formed.

The results are shown in Fig. 6. 6. In (a), (b), and (c), the band alignment of LIO/BLSO, SZO/BLSO, and BHO/BLSO are represented. In chapter 5, the author gets the conduction band offset between BSO and BHO as 1.1 eV. However, in this figure the author uses 1.9 eV since the offset can underestimate by effect of defects in oxide as mentioned in section 5. 2. 3. As seen in figure, these three interfaces are in similar band alignment. So these comparisons are reasonable approach to understand and judge polar interface effect on LIO/BLSO interface. In (d), the measured sheet conductance values of each interface are plotted for the two different conditions, the no interface and the interface formed. As seen in graph, the enhancement of sheet conductance is observed in LIO/BLSO polar interface while it isn't shown in non-polar interfaces. This result proves the necessity of polar interface.

7. Summary

In these works, based on high mobility, oxygen stability, and atomically flat surface of BSO the author mainly has demonstrated the FETs based on BSO with various gate oxides such as Al_2O_3 , HfO_2 , LaInO_3 , and BaHfO_3 . It is well-known that BLSO transport is limited by threading dislocations, generated by large lattice lattice mismatch between BSO and STO. The author tried to find an appropriate buffer layer thickness to demonstrate FET devices because the surface roughness could increase as increasing the buffer layer thickness though the buffer layer could reduce the density of threading dislocations. Judging from transport investigations of BLSO/BSO buffer layer/STO, the author could determine the thickness of buffer layer. Next, the author demonstrates the FETs based on BSO with amorphous and epitaxial gate dielectrics under the criterions as mentioned in chapter 4. In both demonstration of amorphous gate dielectric/BLSO FETs and epitaxial gate dielectric/BLSO FETs, the author shows the dielectric properties such as dielectric constant and breakdown field. Especially, the epitaxial growth of LIO and BHO gate dielectrics are the first work in the knowledge of the author. All devices have shown the sufficient performance due to the novel characteristic of BSO. Especially, the superior performance is achieved in LIO/BLSO FET. This performance could be comparable with famous FET devices based on ZnO and IGZO. Additionally,

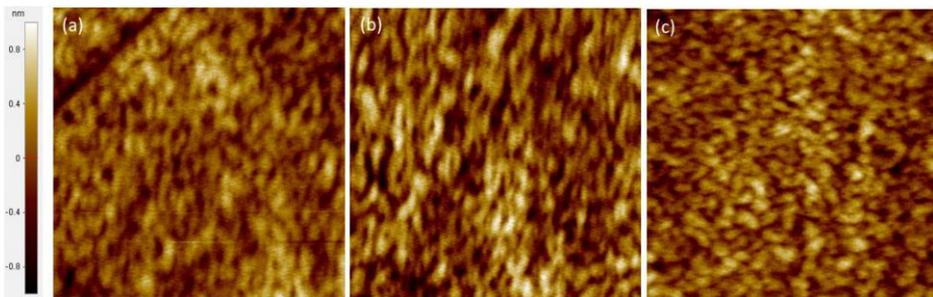
the 2DEG-like behavior has been observed after LIO/BLSO interface formed in LIO/BLSO FETs. After LIO/BLSO interface formed, the sheet conductance of LIO/BLSO interface is enhanced. The enhancement sheet conductance exceeds 10^4 . Of course, the similar behaviors are shown in amorphous gate dielectric/BLSO FETs. However, these enhancements could be removed using thermal annealing in oxygen atmosphere while the enhancement of sheet conductance couldn't be removed in LIO/BLSO interface. So these phenomena could be caused by hydrogen absorption in the BLSO surface since the H_2O is used as oxidant in ALD process. First time, the author thinks that this behavior is originated by LIO/BLSO polar interface formed as same with well-investigated LAO/STO polar interface. However, the theories of LAO/STO interface couldn't explain completely the La concentration dependence of the sheet conductance enhancement of LIO/BLSO interface. To understand this phenomenon, the author investigated the LIO thickness dependence of LIO/BLSO interface. By this investigation, the author could conclude that any polarization such as spontaneous, piezo-electric, and flexco-electric polarization could be formed in LIO/BLSO interface. Also the author confirmed the existence of polarization and the absence of La-diffusion in LIO/BLSO interface through investigation of sheet conductance enhancement by using undoped BSO layer between LIO and BLSO layer. Finally, the author could conclude that the polar interface is necessary to form the 2DEG by comparison between polar interface and non-polar interface. The author can't completely understand why the any polarization is induced in LIO/BSO interface. However, the author strongly believes that these investigations of LIO/BLSO interface can be landmark of application to oxide electronics and to academic researches, if the origin of polarization in LIO/BSO interface is clearly understood.

Appendix A

BaSnO₃ surface treatment by dilute HNO₃

The buffer layer effects on transport of BLSO were described in chapter 3. Additionally, the author investigated the surface morphologies after surface etching by dilute nitric acid. The author uses 0.34 vol % HNO₃ acid. The results were shown in Fig A. 1, 2, and 3.

As mentioned in chapter 3, the author chooses the buffer layer thickness as 110 nm under consideration of transport and surface roughness while the transport of BLSO is enhanced in the thicker buffer layer. As we can see, the roughness values of films are generally decreased as increasing etching time. The author believes that these results can support the usefulness of thicker BSO buffer layer. If then, the device demonstration is possible with low density of threading dislocations. Furthermore, these investigations might support the fabrication of pseudo BSO substrate in the absence of large BSO single crystal.



Time	0 s	30 s	60 s
Roughness	2.0 Å	3.3 Å	2.6 Å
ΔZ	16.4 Å	21.9 Å	18.5 Å

Figure A. 1. AFM image of before and after etched BaSnO₃ (100 nm) film surface by dilute HNO₃ is shown.

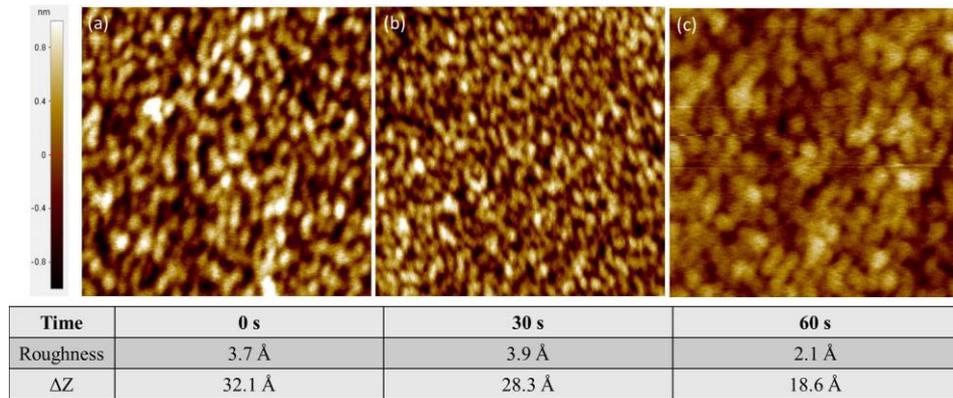


Figure A. 2. AFM image of before and after etched BaSnO₃ (200 nm) film surface by dilute HNO₃ is shown.

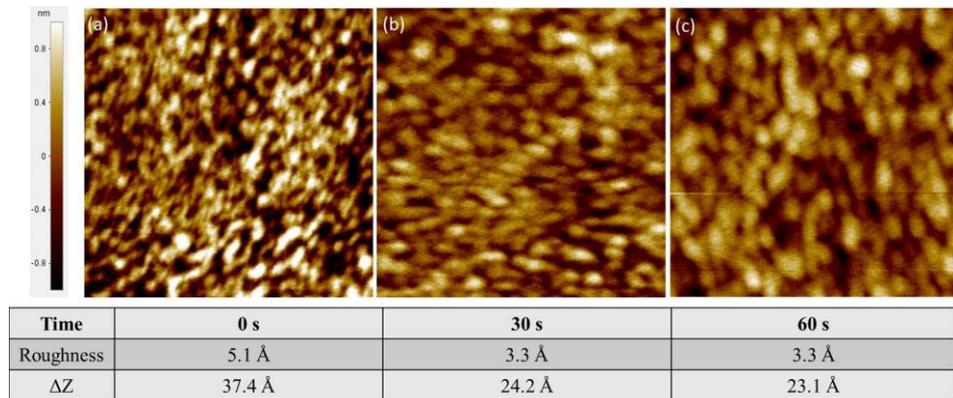
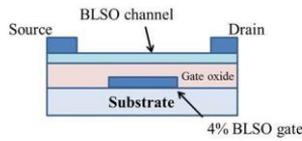


Figure A. 3. AFM image of before and after etched BaSnO₃ (300 nm) film surface by dilute HNO₃ is shown.

Appendix B

Initial works of all-epitaxial LaInO₃/BaSnO₃ field effect transistors

In initial works, the author investigated the dielectric properties of LIO such as breakdown field and dielectric constant to demonstrate all-epitaxial conventional FETs as mentioned in chapter 3. Since the suitable carrier modulation of BLSO active layer using LIO gate dielectric is expected by calculation, the author tried to find an appropriate growth temperature of LIO. The author could determine the growth temperature of LIO by comparison the device performances indirectly. The three samples are prepared in the form of bottom gated FETs. The fabrication process is as follows.



Specification	Sample #1	Sample #2	Sample #3
LaInO ₃ Growth Temperature	650 °C	700 °C	750 °C
Channel Length	3 mm	0.6 mm	0.4 mm
Channel Thickness	10 nm	5 nm	5 nm
Channel Material	4% La-doped BaSnO ₃	4% La-doped BaSnO ₃	2% La-doped BaSnO ₃
Channel Carrier Concentration	$\sim 3 \times 10^{20} \text{ cm}^{-3}$	$\sim 1.5 \times 10^{20} \text{ cm}^{-3}$	$\sim 1 \times 10^{20} \text{ cm}^{-3}$
Gated Area	$2.25 \times 10^{-4} \text{ cm}^2$	$2.25 \times 10^{-4} \text{ cm}^2$	$2.25 \times 10^{-4} \text{ cm}^2$

Table B. 1. Specification of devices.

First the 4 % BLSO lines are fabricated on STO substrate by Si stencil mask as gate electrode. Next LIO is deposited as gate dielectric. After then, BLSO channel layer is deposited by using Si stencil mask again. Finally, the author and co-worker make the source-drain contacts by indium because the SUS stencil mask isn't made at that time. The details and results of devices were shown in table B. 1. and Fig. B. 1. As we can see, the sufficient modulation of active layer was observed in third sample. So the growth temperature of LIO are determined as 750 °C. Of course, someone can claim that these results can't compare completely since the devices have different carrier concentration and channel length.

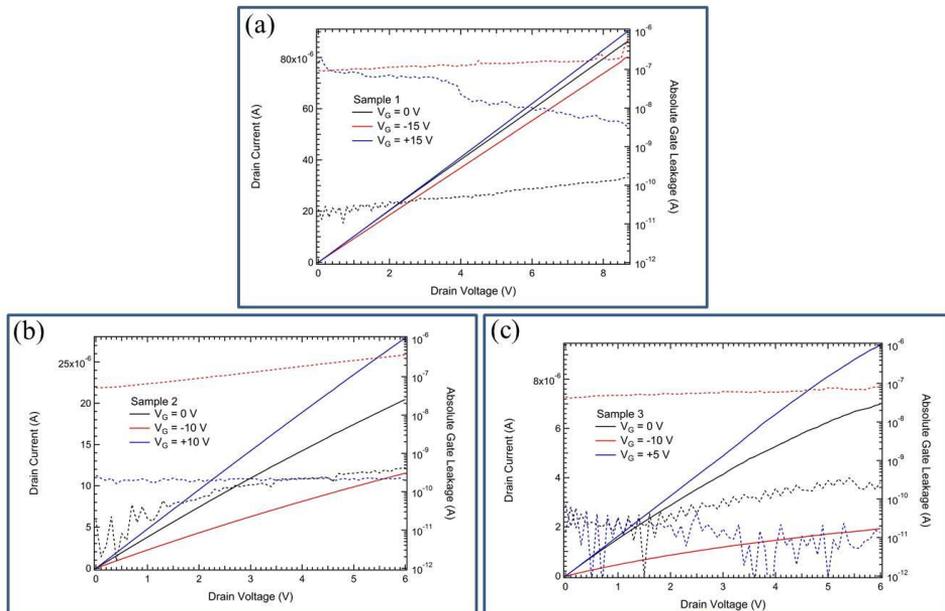


Figure B. 1. Output characteristics of (a) sample #1, (b) sample #2, and (c) sample #3.

However these devices are fabricated as depletion mode FETs because the active layers have high conductivity and high electron carrier density. So the comparable depletion behavior is expected in sample 1 or 2. So the author could

conclude that the dielectric properties of LIO and the quality of LIO/BLSO interface is the best at 750 °C.

After these investigations, the author tries to demonstrate the top gated FETs. Except the BSO buffer layer deposition sequence, its process is all most same with fabrication process of FETs as described in chapter 4. At first time, the author thought simply that the carrier modulation could obtain using thinner active layer under consideration of modulation capacity. Of course this assumption can satisfy for amorphous channel layer and defect free systems. However, It is not easy as shown in Figure B. 2. The author could see just a little carrier modulation while the high electric field, which is suitable electric field to modulate the carrier in active layer, is applied on LIO gate dielectric. Though the author expected the full depletion of active layer at high negative electric field, the author couldn't achieve the sufficient I_{on}/I_{off} ratio. The I_{on}/I_{off} ratio is smaller than 10. The author thought that some factors might affect on increasing the off current on active layer.

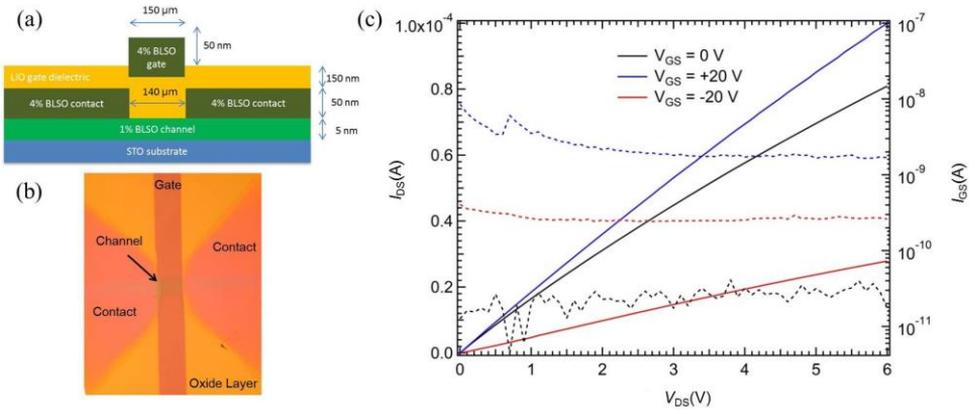


Figure B. 2. (a) Schematics of device, (b) optical top view image, and (c) output characteristic of $\text{LaInO}_3/\text{BaSnO}_3$ FET were represented.

It is well-known fact that leakage source of current such as the trap charge (interface trap, bulk trap) and gate-source leakage could contribute to increasing the off current on active layer. In this system, the author thought the threading

dislocations might be dominant since author reduced the active layer thickness to minimize the n_2d of active layer. As mentioned in chapter 3, the large density of threading dislocations maintained in BLSO thin layer due to the larger lattice mismatch between BSO and STO. So the trapped charges in these threading dislocations act as leakage source on source-drain current. Moreover, these threading dislocations can cancel the electric field when author applied the electric field on LIO gate dielectric. From these considerations, the author felt the necessity of BSO buffer layer between BSO and STO to reduce the threading dislocations in BLSO.

Appendix C

Epitaxial growth of SrHfO₃, LaInO₃, and SrZrO₃

The author described the successful LIO/BLSO and BHO/BLSO FETs in chapter 5. However, the author investigated other epitaxial gate dielectrics such as SHO and SZO until the successful FETs are demonstrated using BSO buffer layer. Additionally, the studies of LIO in various oxygen partial pressures are investigated. Lupina *et al.* investigates SHO as a candidate dielectric of high- k material. The lattice mismatch between BSO (4.116 Å) and SHO (4.088 Å) is about 0.7 %. These properties of SHO such as high dielectric constant ($K=35$) and small lattice mismatch (0.7 %) with BSO attracted the author's interesting.

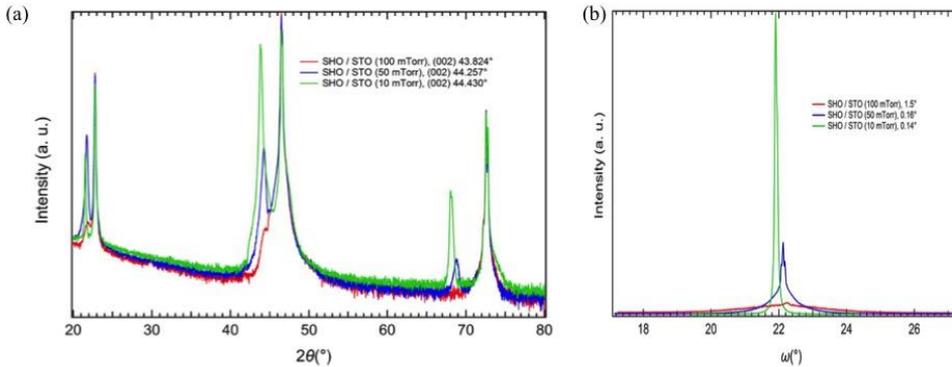


Figure C. 1. XRD $\theta - 2\theta$ and ω -rocking curves of SHO. (a) The $\theta - 2\theta$ curves of 100 nm thick SHO films on STO substrates are plotted for various P_{O_2} . (b) denotes the ω -rocking curves of each thin films.

As mentioned in chapter 5, the cubic crystal structure of SHO demanded the strict control over deposition condition. So the author investigates crystallinity of

SHO in the various laser energy fluences under fixed oxygen partial pressure and distance from target to substrate. In the special energy fluence, the author could achieve cubic phase of SHO with no secondary phase. Additionally, the author deposits SHO films on STO substrate in various oxygen partial pressures to confirm the oxygen partial pressure effect on crystallinity. The results are shown in Figure C. 1. As seen, the author could fabricate epitaxial SHO films with no phase separation and high crystallinity. However, the author couldn't measure the dielectric properties such as breakdown field and dielectric constant of SHO because the BLSO contact electrode on SHO dielectric layer is insulating. It means that the demonstration of all-epitaxial FETs is impossible. Based on the results of SHO, the author investigates oxygen partial pressure effect on crystallinity of LIO. Because the author thinks that the high dielectric properties is induced by high crystallinity of LIO. The results are shown in Figure C. 2. As we can see, the high crystallinity is achieved in the low oxygen partial pressure and the author could see the lattice expansion of LIO as decreasing the oxygen partial pressure. This expansion might be regarded as the result of repulsive interaction by induced electrons in oxygen vacancies.

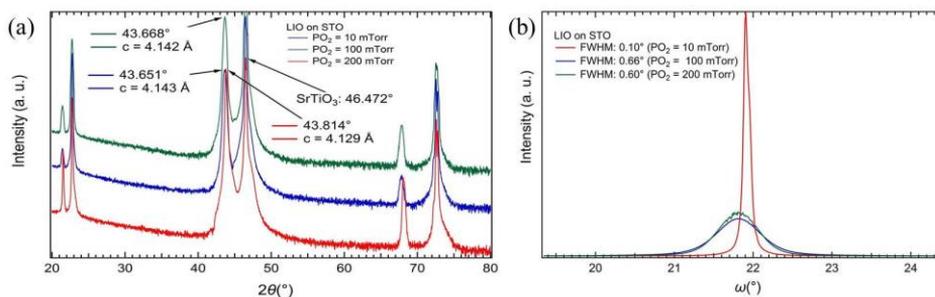


Figure C. 2. XRD θ - 2θ and ω -rocking curves of LIO. (a) The θ - 2θ curves of 100 nm thick LIO films on STO substrates are plotted for various P_{O_2} . (b) denotes the ω -rocking curves of each thin films. Especially, the high crystalline thin film is achieved in low P_{O_2} .

However, the dielectric properties of LIO, deposited in low P_{O_2} , are very leaky and poor. Maybe, the oxygen vacancies might act leakage source. Finally, the author deposited SZO thin film on STO substrate with the oxygen partial of 100 mTorr and substrate temperature of 750 °C. The results are shown in Figure C. 3. As seen, the epitaxial film of SZO is grown. As mentioned in Chapter 5, the author prepares BLSO/SZO/BLSO capacitor. Also the author investigates the dielectric stack with LIO due to its high dielectric constant. However, the satisfactory results aren't achieved. So SZO couldn't be used as gate dielectric and just used in the investigation of polar interface versus non-polar interface as shown in Chapter 6.

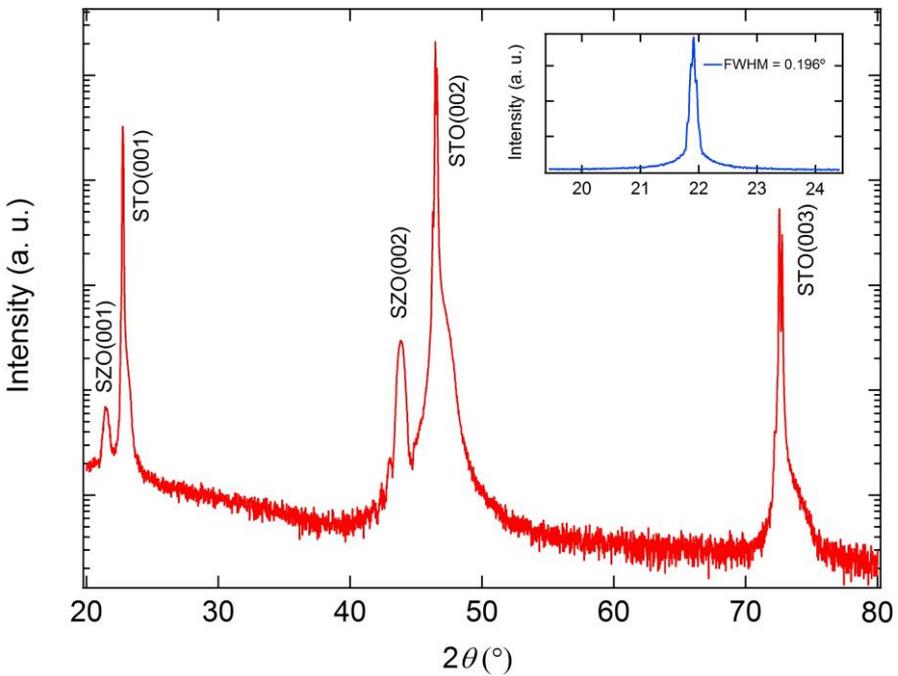


Figure C. 3. XRD $\theta - 2\theta$ and ω -rocking curves of SZO. The $\theta - 2\theta$ curve of 100 nm thick SZO is plotted. Inset denotes the ω -rocking curve of SZO film.

Appendix D

Interface quality study by Cross-sectional TEM measurement

As mentioned in Chapter 3, the author could confirm and count dislocations using investigation of cross-sectional TEM of BSO thin film on STO substrate. The cross-sectional TEM measurement is useful technic to study on interface quality, too. One of the devices of LIO/BLSO interface formed shown in section 6.1 is measured. Its cross-sectional images were shown in Fig D. In (a), as expected and seen in chapter 3, we can see again the existence of the misfit dislocations between BSO and STO and threading dislocations in LIO/BLSO/BSO. However, we can't see the generation of threading dislocations and/or misfit dislocations in LIO/BLSO interface. The author thinks that it might come from perfectly lattice matching between BSO and LIO. It is clearly seen in (b) and (c). Especially, in (c) defects such as point defects and stacking fault can't be observed. And in (d), we can see the perfectly matched LIO/BLSO interface as expected. In fact, anyone can't distinguish the boundary of BSO and LIO layer directly. This perfect interface can explain the superior performance of LIO/BLSO FETs shown in Chapter 5. Moreover, this image seems that the interface layer is deposited in a layer-by-layer growth mode. This is very surprising result because the ex-situ device fabrication is carried out as described in section 6. 1. This result may strongly support the superiority of our growth system and experience.

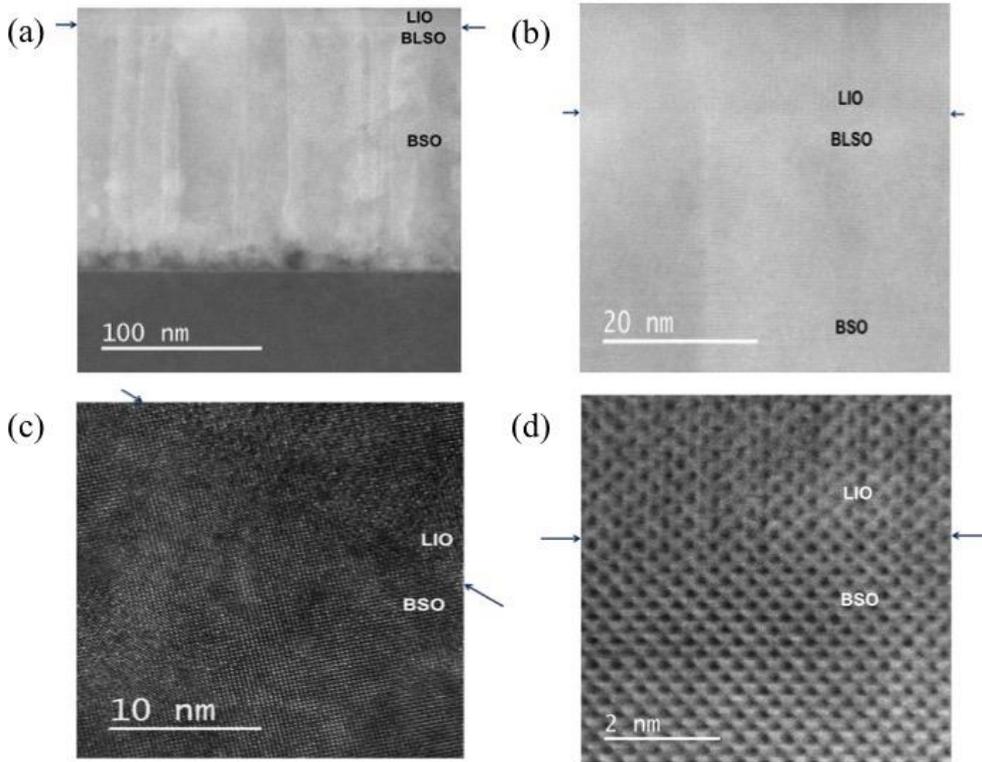


Figure D. The cross-sectional TEM images of LIO/BLSO interfaces. (a), (b), (c), and (d) represent the cross-sectional TEM images of LIO/BLSO interfaces for various scales. Arrows in each image denote the interface boundary of LIO/BLSO interface.

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국문 초록

일반적으로 산화물이 종래의 금속 또는 세라믹과 같은 물질들과 비교하여 이례적인 광학적 투명도와 높은 전기 전도도로 보임으로 인해 전자공업 분야에서 가장 전도 유망한 물질로 여겨지고 있다. 실재로, Sn:In₂O₃, Cu₂O, ZnO, In₂O₃-ZnO, In₂O₃-Ga₂O₃, In₂O₃-Ga₂O₃-ZnO 등의 물질들이 투명 전도성 산화물 과 투명 산화물 반도체로 많이 연구가 되어왔다.

추가적으로 지난 몇 십 년간, YBa₂Cu₃O₇, Pb(Zr_xTi_{1-x})O₃, SrTiO₃ 와 같은 ABO₃ 구조의 페로브스카이트 산화물이 superconductivity, high-k dielectrics, ferromagnetic, photoconductivity, ferroelectricity 등의 흥미로운 특성들로 인해 많은 관심을 받아 왔다. 실재로, 많은 연구자들이 산화물 전자 소자로의 적용의 초석이라고 할 수 있는 전계 효과 트랜지스터(Field effect transistor)를 구현하기 위하여 많은 노력을 기울였었다. SrTiO₃ 와 KaTaO₃를 기반으로 하는 전계효과 트랜지스터가 구현 되었음에도 불구하고, 이 물질들의 낮은 전자 이동도로 인해 이원화 산화물을 기반으로 하는 디바이스 보다 뛰어난 성능을 얻을 수가 없었다. 더욱이, 산소 안정성의 결여는 이 물질들의 응용에 있어서 제한 요소로 작용하였다.

최근 높은 온도에서의 산소 안정성과 상온에서의 높은 전기 이동도를 가지는 BaSnO₃ 가 많은 관심을 받고 있다. BaSnO₃가 3.1 eV 의 넓은 광학적 띠틈(optical band gap) 을 가지며, 특히 La 도핑된 단결정과 박막 같은 경우, 각각 300 cm²V⁻¹s⁻¹과 70 cm²V⁻¹s⁻¹의 전자 이동도를 가진다는 것이 알려졌다. 단결정(single crystal)과 박막(thin films)에서의 이동도 차이는 박막내의 어긋나기(dislocation)와 낱알 경계(grain boundary)의 영향으로 여겨지고 있다. 또한 10⁻¹⁵ cm²s⁻¹의 산소 퍼짐 상수(diffusion constant)가 얻어 졌으며, 이 값은 magnate, cupprate, titanate 등의 기존의 많이 연구된 perovskite들과

비교하여 적게는 3 오더 많게는 10오더정도가 작은 값이다. 이러한 우수한 특성을 이용하여 비결정(amorphous)과 켄쌓기 게이트(epitaxial gate) 물질로 전계효과를 통해 BaSnO₃의 운송자(carrier) 변조(modulation)를 하였다.

우선적으로 적절한 채널층의 특성을 얻기 위해서 채널의 특성뿐만 아니라, BaSnO₃와 게이트 유전체 사이의 결합으로 작용할 수 있는 어긋나기를 줄이기 위해서 완충층의 효과를 조사하였다. 게이트 유전체로 Al₂O₃와 HfO₂를 선택 하였으며, 이들의 절연 파괴장과 유전상수와 같은 유전 특성을 연구 하였다. 또한 이러한 물질 인자들을 기반으로 하여 SrTiO₃기판에 BaSnO₃ 완충층을 증착 한 후, 미량의 La가 도핑된 BaSnO₃ 채널을 게이트 유전체 Al₂O₃와 HfO₂를 이용하여 전계 효과 트랜지스터를 구현하였다. 이 장치의 BaSnO₃, Al₂O₃, HfO₂의 알려진 물질 변수와 일관된 전계 효과 이동도(field effect mobility), I_{on}/I_{off} 비율과 같은 성능은 더 나아가서 BaSnO₃의 표면질(Surface quality)와 안정성을 방증한다 할 수 있을 것이다. 더욱이 동일한 구조의 SrTiO₃ 또는 KaTaO₃를 기반으로 하는 전계 효과 트랜지스터 장치들과 비교하여 볼 때, 이러한 성능은 BaSnO₃ 물질의 우수성을 제공함과 동시에 높은 이동도 투명 전계 효과 트랜지스터 장치로의 적용에 잠재성을 보인다 할 수 있겠다.

이 후 장치의 성능을 향상시키기 위해서 켄쌓기 게이트 유전체를 사용하였다. 여러 후보군중 LaInO₃, BaHfO₃를 선택하였다. 또한 이 둘의 결정화도(crystallinity)와 유전 특성을 X-ray diffraction과 전기적 측정을 통하여 각각 연구 하였다. 이를 기반으로 하여 전계 효과 트랜지스터를 구현 하였으며 ZnO, In-Ga-Zn-O, SnO₂를 기반으로 하는 전계 효과 트랜지스터의 성능과 비교하여볼 때 주목할만한 성능이 보여졌다.

특별히 LaInO₃/La-doped BSO 장치를 제작하는 과정에서 채널 층의 판전도도(sheet conductance)가 증가하는 현상이 관찰되었으며, 이 현상이 두 물질의 계면에 2차원 전자 가스가 형성되었을 것이라 생각한다. 이 현상의

원인을 설명하기 위해서 계면 전도도의 La 도핑, LaInO_3 두께 의존성을 연구 하였으며, 추가적으로 제기될 수 있는 계면에서의 La 확산과 산소 결핍등의 효과를 조사하였다. 이러한 조사들이 $\text{LaInO}_3/\text{BaSnO}_3$ 계면에서 일어나는 2차원 전자 가스의 원인을 이해하는데 도움이 될 수 있을 것이다.

Keywords : 투명 전도성 산화물, 투명 산화물 반도체, 페로브스카이트 산화물, BaSnO_3 , 넓은 띠타, 산소 안정성, 높은 전자 이동도, 전계 효과 트랜지스터, 산화물 계면

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