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공학박사 학위논문

Enhancement of Injection and Transport in Organic Field-Effect Transistors and Light-Emitting Transistors with Multilayers

다층 유기 전계 효과 트랜지스터 및 유기 발광 트랜지스터의 전하 주입 및 거동 능력의 향상

2017 년 8 월

서울대학교 대학원

공과대학 전기·컴퓨터공학부

이 규 정

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지도 교수 이 신 두

이 논문을 공학박사 학위논문으로 제출함

2017 년 8 월

서울대학교 대학원

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Abstract

Enhancement of injection and transport in organic field-effect transistors and light-emitting transistors with multilayers

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The organic electronics have drawn great attention for their potential of application in advanced electronic device. The intrinsic advantages of organic materials, such as flexibility, light-weight, and low-cost and large-area processability, give organic electronics superior merit compared to the silicon-based materials. Moreover, the chemical versatility of organic materials opens new fields of light-emission, charge-transport, photovoltaicity, and sensing properties in organic electronics. In this regards, the detailed investigation to physical mechanism of organic electronics enables the successful introduction of organic semiconductors to various opto-electronic devices including organic light-emitting diodes (OLEDs), organic field-effect transistors (OFETs), and organic photovoltics (OPVs). Among the organic electronic devices, the OFETs have been considered as a main candidate for the various fields of flexible electronics, integrated circuits, organic-based

sensors, and radio frequency identification tags.

In recent years, the extensive researches in material level have led to the development of high performance organic materials having field-effect mobility (up to 10 cm^2/Vs). For realization of OFETs as a practical application of advanced electronics, however, the enhancement of charge injection and transport in device level is strongly required. In order to fully utilize the capability of improved electric performance of organic material, the multi-layers structures of OFETs have been adopted to improve electrical characteristics. For example, the interlayer between the source/drain electrode and the organic semiconductor (OSC) was placed to improve the injection characteristics, and the ambipolar-type OFETs was introduced to balance the transport of holes and electrons in same device. Moreover, the light-emitting transistors was extensively studied for its light-emitting property together with the switching capability of transistor in single device.

The main purpose of this thesis is to demonstrate the enhancement of charge injection and transport of OFETs and OLETs with multi-layers by the optimization of device structures. At first, an ambipolar-type OFET with two-stacked OSCs in dual gate configuration was proposed. Two stacked OSCs, directly contacted with the source/drain electrodes, form the separated channels for holes and electrons, respectively. These individual channels can be effectively and independently controlled by corresponding gate bias voltage, so the ambipolar-type transport in a single device can be obtained. Next, the introduction of semiconducting organic buffer layer between the source/drain electrodes and the OSC layer is described. The semiconducting organic buffer layer greatly reduces the potential loss at the contact region (interface of source/OSC) so the injection properties of OFETs can be improved. And lastly, the vertical configuration of OLETs (VOLETs) having high on/off ratio is demonstrated by dielectric encapsulation of source electrode. The dielectric encapsulation of source electrode governs the effective charge pathway in

VOLETs by blocking excessive electric fields from the drain voltage. As a result, the gate voltage can successfully control the accumulation and transport of charges, which results in the high on/off ratio of VOLETs.

The novel device architectures of OFETs with multi-layers demonstrated in this thesis would pave the way towards the enhancement of electrical characteristics in OFETs, the precise control of effective charge flow in OFETs, the ambipolar-type operation in single device, the integration of light-emitting capability in switching OFETs, and further application of advanced, flexible and multi-functional organic electronics.

Keyword : Organic field-effect transistors, Organic light-emitting transistors, Device configuration, Numerical simulation, Charge injection and transport, Dielectric encapsulation

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Chapter 1. Introduction

1.1. Overview of organic electronics

Organic electronics has been attracted a great attention due to its potentials for the application of novel class of electronic devices. For example, organic electronic devices have been widely investigated in the fields of integrated circuits, bendable/flexible electronic devices, chemical-/or bio- sensors, photovoltaic devices, and optoelectronic devices. [1] In addition, organic electronics have potential to be fabricated by low-cost, easy and high-throughput process and large-area production method. Among the various organic electronic devices, optoelectronic devices including organic field-effect transistors (OFETs), organic light-emitting diodes (OLEDs), and organic photovoltaic cells (OPVs) are in the center of interest. More excitingly, the optimization of organic semiconductor material design at the molecular level as well as structural innovation of organic devices allow organic electronic devices to exhibit excellent electrical characteristics with high mobility, low threshold voltage and stability and different functional properties simultaneously or under different operating conditions in a single device. Therefore, the multi-functional organic devices are considered as one of the hot topics in organic electronics.

In this regards, several ways to enhance the electrical performance of OFETs and organic light-emitting transistors (OLETs) by employing multi-layer organic semiconductors in a single device have been presented. The introduction of the multi-layer OSCs helps to accomplish the improvement of charge injection and charge transport in OFETs and OLETs. In this thesis, the structural optimization of the ambipolar-type OFETs in dual gate configuration and that of the vertical-type

OLETs via numerical simulation together with experimental data will be presented, which will provide the multi-functional integration in a single OFETs.

In this **Chapter 1**, two different organic electronic devices will be briefly introduced. One is the OFETs mainly used for the application of switching and driving transistors in integrated circuits and/or active matrix display component. The other is the OLETs for the integration of OFETs and OLEDs in a single device having both electrical switching performance and light-emitting characterisitcs, which can be controlled by applying the voltage for corresponding electrodes.

1.2. Organic field-effect Transistors

OFETs have been considered as one of the attractive candidates for a broad range of low-cost, flexible electronic applications, including electronic papers, radio frequency identification (RFID) tags, and chemical-/bio-sensors [1-3]. Due to the extensive development of organic electronics, great progresses have been made towards the high performance organic devices with field-effect mobility well over 1 cm^2/Vs [4, 5]. Moreover, the systemic investigation of the relationship between the molecular structure and device performances, the novel patterning technique of organic materials, and the innovative architectures such as vertical-type OFETs or dual-gate configuration of OFETs enable the construction of integrated circuits, and the exploration of novel applications with OFETs [6, 7]. Among these important progresses, the development of multi-functional OFETs, which combine two or more types of physical properties in a single device, has attracted particular attention. Recently, numerous studies on OFET based sensors, photodetectors, and organic light-emitting transistors (OLETs) have been demonstrated by various research groups [8-10], which clearly demonstrate the rapid developments of multi-functional OFETs. To achieve the multi-functional characteristics in a single OFETs, multi-layer organic semiconductors (OSCs) are often used. In those OFETs with multi-layer OSCs, it is essential to precisely control the charge injection and charge transport [11]. Especially, the advent of novel device configuration with multi-layer OSCs strongly requires the optimization of the charge injection and transport based on the systemically investigated physical mechanism.

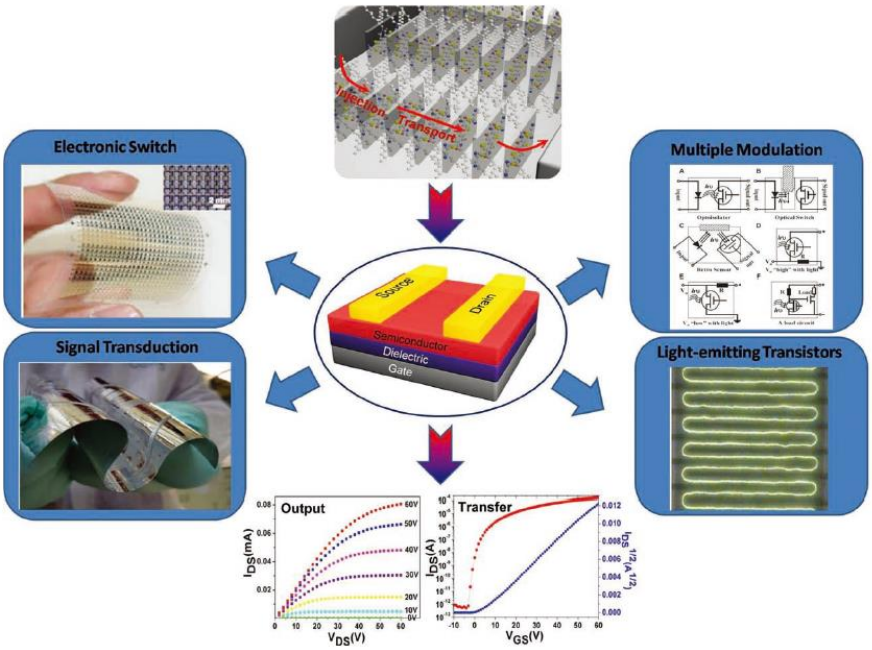

Figure 1.1. Illustration of device structure, electrical characteristics, and applications of OFETs (Ref. [1]).

1.3. Organic light-emitting transistors

Tremendous interest in organic optoelectronics has been drawn as the emergence of OLETs [8, 9]. An OLET has three electrodes with same role as those of an OFET, which determines degree of the injected charges, the accumulation of injected charges at the channel region, and the transport of accumulated charges. In addition, by governing the process of exciton recombination in the channel region, the feature of light-emission can be also accomplished in OLETs [8-11]. That is, OLETs offer the possibility to combine the electrical switching capability with the light-emission function in a single device, thereby less complex circuit design is required in realization of next-generation display circuit.

Moreover, OLETs are considered as excellent opto-electronic devices to investigate physical mechanism via observation of light-emission properties. For instance, the processes of charge-carrier injection, transport, recombination, and light-emission in organic semiconductors can be directly observed by the location of light-emission in terms of the applied voltage for each electrode. In this regard, the use of the high-resolution (up to nanometer scale) microscopic observation devices offers more detailed and easy access for physical mechanism.

The nature of the semiconductor and the chemical and dielectric properties of the insulator as well as the materials for each electrode, the device architecture and the processing conditions are fundamental in optimizing the optoelectronic parameters (charge carrier mobility, brightness, voltage threshold, quantum efficiency, etc.) of OLETs. Therefore, there have been various approaches toward the improvement of OLET such as (i) multi-layer OSCs for better charge transport and light-emission [12, 13]; (ii) modified electrodes for better charge injection [14-16]; (iii) increase of out-coupling efficiency by same techniques in OLEDs.

Still, more specific and detailed investigations on the physical mechanisms of

OLETs from the viewpoint of the injection, transport and recombination of charges as well as the light emission processes in organic light-emitting field-effect transistors are strongly required. Moreover, multi-layer OLETs should be optimized not just from the viewpoint of materials used, but also in the perspective of the device structure and geometrical level. Therefore, the novel device architecture of OLET is discussed in **Chapter 5**.

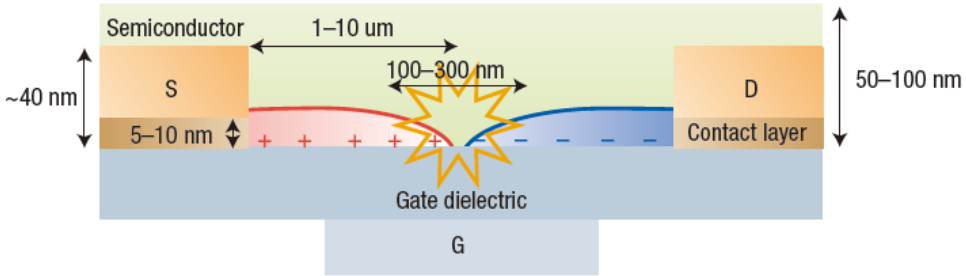

Figure 1.2. Schematic representation of the device structures and the main optoelectronic processes occurring in an OLET (Ref. [9]).

1.4. Outline of thesis

This thesis is organized into the following **Chapters of 1-6**, including the **Introduction** and **Concluding Remarks**. In **Chapter 1**, the introduction of organic electronics, especially about the OFETs and OLETs with multi-layer structure for application of the advanced organic electronic circuits and/or the active matrix display component. In **Chapter 2**, I mainly discuss on the introduction and basic theoretical principals of OFETs. Moreover, advanced configurations such as multi-layer OFETs, ambipolar-type OFETs, and OLETs with vertical configuration will be shown briefly. In **Chapter 3**, I present on the specific concept for enhancement of the charge transport mechanism via OFETs with multi-layers. The enhancement of transport characteristics of both charges (electrons and holes) in ambipolar-type OFETs will be demonstrated by introducing the dual-gate configuration with two-stacked OSCs. The two-stacked OSCs in ambipolar-type OFETs form the separate channels for the electrons and the holes, respectively. The separate channels can be individually controlled by corresponding gate electrode while the counter gate electrode effectively suppresses the accumulation and transport of courter charge. The improvement of injection transport in terms of energy barrier height is discussed in the **Chapter 4**. With numerical simulations, the scientific investigation of physical mechanism in injection of OFETs was conducted in terms of the effect of the injection barrier height together with the mobility of buffer layer on the electrical characteristics of OFETs. Based on simulation results, the semiconducting organic buffer layer (SOBL) was inserted in typical bottom gate top contact OFET configuration. The SOBL enables the improvement of injection mechaism by tailoring injection barrier height as well as the increase of overall mobility by transporting the injected charges toward the channel region. In **Chapter 5**, vertical OLETs having high on/off ratio will be shown. The achievement of high on/off ratio

is accomplished by dielectric encapsulation of source electrode. The dielectrically encapsulating source insulator can successfully reduce the off-current current (leakage current between source-drain electrode) injected from the top and side of source electrode. Moreover, the injected charges can be accumulated at the interface of gate-inulsator/OSC, resulting increased gate-controllability. The degree of on/off ratio in terms of device configuration was investigated by 2-D numerical simulation tools. In addition, the effect of interfacial defect at the OSC/source-insulator on the on/off ratio was also studied. Finally, the concise summaries and some concluding remarks are presented in **Chapter 6**.

Chapter 2. Theoretical Backgrounds

2.1. Operation principle of organic field-effect transistors

In this section, the basic structures, the current-voltage characteristics, and working principles of organic field-effect transistors will be introduced. In addition, this section will also briefly describe the basic component of OFETs, most common charge transport models, some important parameters, and the various device configuration of OFETs.

An organic field-effect transistor mainly consists of the parts of three electrodes, gate insulator, and an organic semiconductor (OSC). In detail, a gate insulator covers gate electrode. The source and drain electrodes with channel width W and the semiconducting layer with a channel length of L plays important role on carrier transport (shown in Figure 2.1). The OSC layer of an OFET is formed by vacuum deposition, drop-cast, or spin-cast method. The gate electrode can be a metal or a conducting polymer. As gate insulator, inorganic insulator or polymeric insulators are commonly used. The source electrode injects charges into the active layer and the drain electrode collects the transported charges. The metals and solution-processable conducting polymers have been used for the source and drain electrodes.

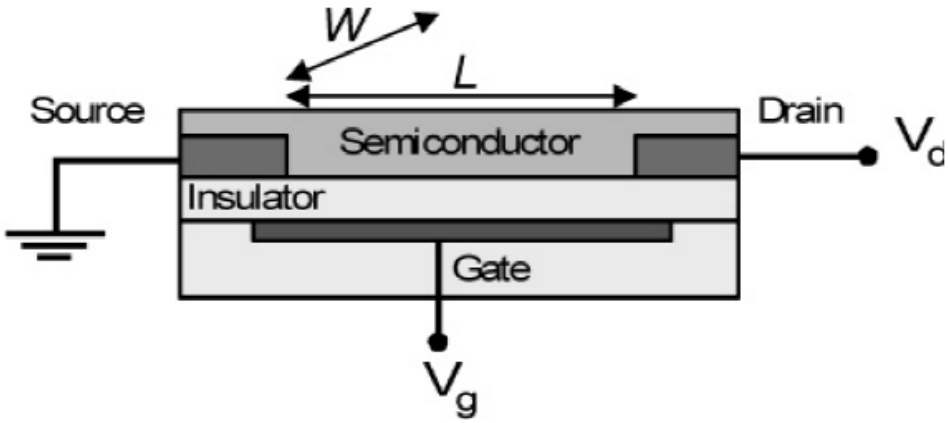

Figure 2.1. Structure of an OFET. *L* represents channel length, *W* the channel width, V_d the drain voltage, and *V*g the gate voltage (Ref. [18]).

Figure 2.2 illustrates the basic operating regimes and associated current-voltage characteristics of a field-effect transistor. When $V_G > 0$, the electrons will be injected from the source electrode and then accumulated at the interface of insulator/semiconductor (the channel region). For negative V_G, the holes will be injected and accumulated at the channel region. The degree of accumulation at the interface is proportional to V_G and the capacitance C_i of the gate insulator. Those accumulated charges will be transported to the drain electrode by electric fields induced by the drain voltage, which contribute to the drain current.

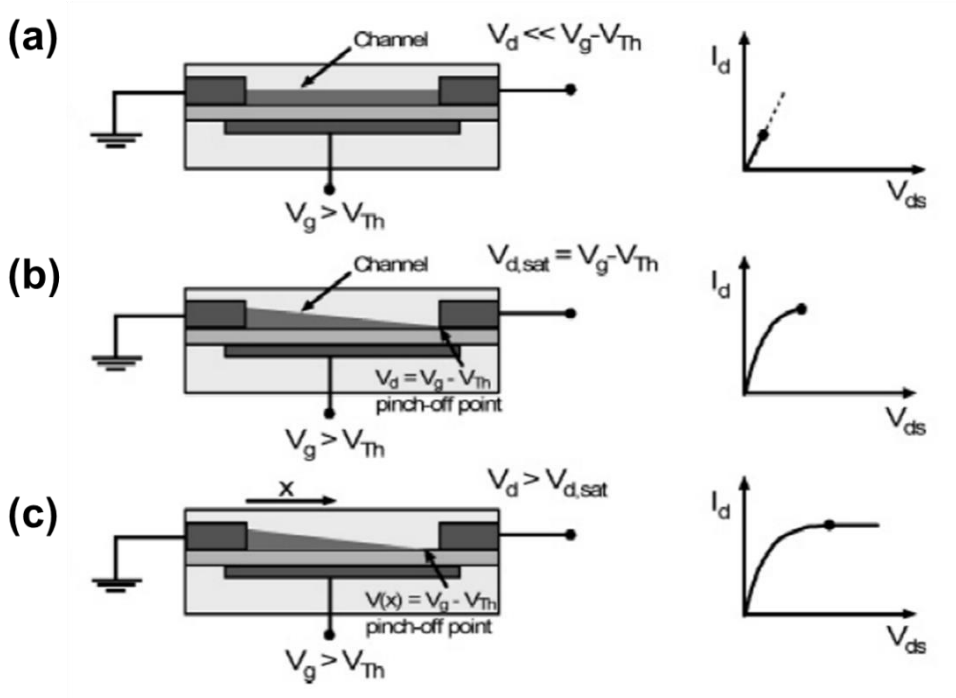

Figure 2.2. Illustrations of operating regimes of OFETs: (a) linear regime; (b) start of saturation regime at pinch-off, (c) saturation regime and corresponding current-voltage characteristics (Ref. [18]).

However, due to the defects of OSC and gate insulator, not all injected charges can be transported to the drain electrode. At first, the deep traps in the OSC absorb the injected charges. That is, a gate voltage has to be applied that is higher than a threshold voltage V_{th}, and thus the effective gate voltage is reduced to $V_G - V_{th}$. On the other hand, donor (for n-channel) or acceptor (for p-channel) states and interface dipoles can create an internal potential at the interface and thus cause accumulation of charges in the channel even when $V_G = 0$ V. [19, 20]

When zero source-drain bias (V_{DS}) is applied, the carrier concentration in the transistor channel is uniform. A linear gradient of charge density from the carrier-injecting source to the extracting drain forms when a negligible small source-drain voltage is applied ($V_{DS} << V_G$, Figure 2.2(a). This regime is called as the linear regime, in which the degree of current flowing through channel is directly proportional to

V_{DS}. In the linear regime, the drain current (I_D) can be simplified to

$$I_D = (W/L)\mu_{lin}C_i(V_G - V_{th} - 0.5V_{Ds})V_{Ds} \quad (1)$$

The drain current is directly proportional to V_G, and the field-effect mobility in the linear regime (μ_{lin}) can thus be extracted from the gradient of I_D versus V_G at constant V_{DS} (applicable for gate voltage dependent mobility).

When V_{DS} is further increased to a point of $V_{DS} = V_G - V_{th}$, the channel becomes "pinched off" (Figure 2.2(b)). Here, a depletion region is formed next to the drain electrode because the difference between the local potential and the gate voltage is now below the threshold voltage. A space-charge-limited saturation current $I_{DS,sat}$ can flow across this narrow depletion zone as carriers are swept from the pinch-off point to the drain by the comparatively high electric field in the depletion region. Further increasing the source-drain voltage will not substantially increase the current but will lead to an expansion of the depletion region. Since the potential at the pinch-off point remains $V_G - V_{th}$ and thus the potential drop between that point and the source electrode stays approximately the same, the current saturates at a level $I_{DS,sat}$ (Figure 2.2(c)). Here, the saturation current can be obtained by substituting V_{DS} with $V_G - V_{th}$, yielding

$$I_D = (W/2L)\mu_{sat}C_i(V_G - V_{th})^2 \quad (2)$$

Note that transistors with short channel lengths require thin gate dielectrics, typically $L > 10d_{dielectric}$ [21, 22], in order to ensure that the field created by the gate voltage determines the charge distribution within the channel (gradual channel approximation) and is not dominated by the lateral field due to the source-drain voltage. Otherwise, a space-charge-limited bulk current will prevent saturation and the gate voltage will not determine the "on" or "off" state of the transistor [23-27].

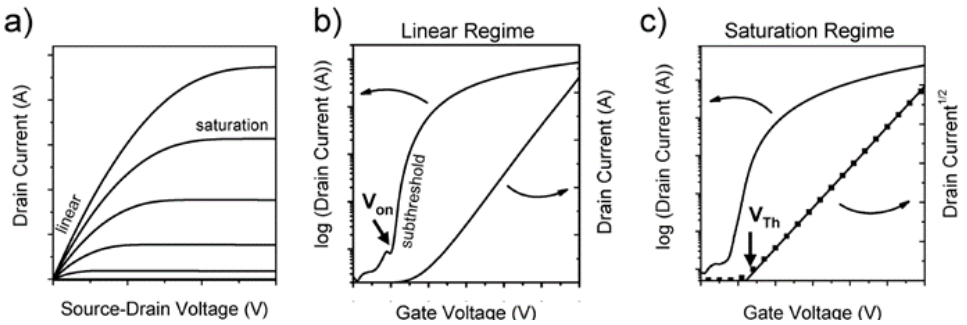

Figure 2.3. Representative current-voltage characteristics of an n-type OFET. (a) Output characteristics showing the linear and saturation regimes. (b) Transfer characteristics in the linear regime and the onset voltage (V_{on}). (c) Transfer characteristics in the saturation regime and the threshold voltage V_{th} (Ref. [18]).

Figure 2.3(a) shows typical output characteristics (the drain current versus source-drain voltage for various constant gate voltages) of an n-channel OFET with a channel length of 200 μm. From the output characteristics, the linear regime at low V_{DS} and the saturation regime at high V_{DS} are evident.

Figure 2.3(b) shows the transfer characteristics (the drain current versus gate voltage at constant V_{DS}) of the same transistor in the linear regime by both as a semi-log plot and as a linear plot. From the semi-log plot, the onset voltage (V_{on}, the voltage at which the drain current abruptly increases above a defined low off-current level) can be easily extracted and the subthreshold swing ($S = dV_G/d(\log I_{ds})$), which depend on the gate dielectric capacitance and the trap states at the interface, can be also calculated. The gradient of the current increase in the linear regime is directly proportional to the mobility if the mobility is gate voltage independent. Most semiconductors, however, show gate-voltage-dependent mobility, and thus, the curve shape may deviate from being linear.

Figure 2.3(c) shows a transfer curve in the saturation regime. Here the square root of the drain current should be linearly dependent on the gate voltage, and its gradient is proportional to the mobility. Extrapolating the linear fit to zero yields the threshold voltage V_{th}. Threshold voltage is originated from several effects and

strongly dependent on the OSC and dielectric used. Built-in dipoles, impurities, interface states, and, in particular, charge traps contribute to the threshold voltage [28]. Note that V_{th} can be reduced by increasing the gate capacitance and thus inducing more charges at lower applied voltages. The threshold voltage is not necessarily constant for a given device. When OFETs are operated for long time, V_{th} tends to increase. This bias stress behavior has a significant effect on the applicability of OFETs in circuits and is presently under intense investigation [29-34]. A shift of the threshold voltage on the time scale of current-voltage measurements causes current hysteresis (usually the forward scan shows higher currents than the reverse scan), stable threshold shifts, for example, induced by polarization of a ferroelectric gate dielectric, can be used in organic memory devices [35, 36].

Another important parameter of OFETs is the on/off ratio, which is the ratio of the drain current in the on-state at a particular gate voltage and the drain current in the off-state (I_{on}/I_{off}). For excellent switching behavior, this value should be as large as possible. The on-current mainly depends on the mobility of the OSC and the capacitance of the gate dielectric. The magnitude of the off-current is determined by gate leakage and by the bulk conductivity of the semiconductor, which can increase due to unintentional doping, as for example often observed in P3HT transistors [37-39].

The difference of geometry has also great impact on the electrical characteristics even in case of OFETs with identical materials. The device configuration can be categorized in four-ways based on the position of gate electrode and contact between source/drain electrode and OSC. The four different device structures of the bottom-gate bottom-contact (BCBG, Figure 2.4(a)), top-gate bottom-contact (TGBC, Figure 2.4(b)), bottom-gate bottom-contact (BGBC, Figure 2.4(c)), and top-gate top-contact (TCTG) and top contact/bottom gate (TCBG, Figure 2.4(d)) structures are shown in Figure 2.4. One of the major differences

between these device geometries arises from the position of the injecting electrodes in relation to the gate. In the bottom contact/bottom gate structure, the charges are directly injected into the channel of accumulated charges at the semiconductor-dielectric interface. In the other structures, the source/drain electrodes and the channel are separated by the semiconducting layer. Thus, charges first have to travel through several tens of nanometers of undoped semiconductor before they reach the channel. Other differences among the transistor structures arise from the dielectric/semiconductor and electrode/semiconductor interfaces, such as different morphologies at the top and bottom surfaces of a semiconductor film (molecular orientation, roughness) [40] or introduction of trap states during metal evaporation on organic semiconductors for top contact transistors [41, 42].

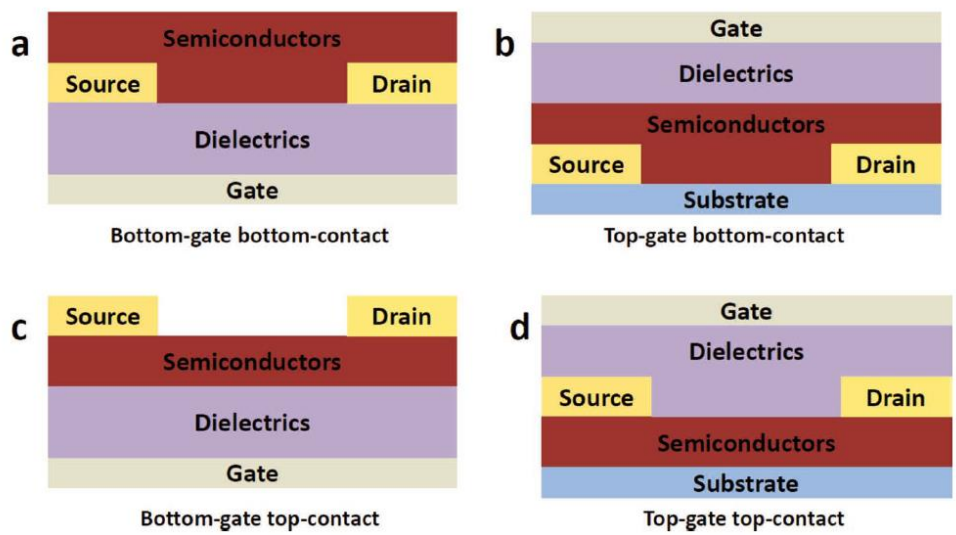

Figure 2.4 Device structures of typical OFETs: (a) bottom-gate bottom-contact (BGBC), (b) top-gate bottom-contact (TGBC), (c) bottom-gate topcontact configurations (BGTC), and (d) top-gate top-contact (TGTC) (Ref. [1]).

2.2. Charge transport in ambipolar-type organic field-effect transistors

The performance of OFETs has improved immensely over the past decades, with OFET mobility in some cases exceeding those of amorphous silicon FETs [43-45]. Most of the OFETs have shown only unipolar behavior (either holes or electrons). However, the fabrication of devices exhibiting ambipolar-type behavior that can provide both n- and p-channel performance in single device is very important due to their application in large-area manufacturing of complementary integrated circuits without requiring micro-patterning of the individual p- and n-channel semiconductors [46]. Another advantage of ambipolar-type OFETs is that the light emission can be achieved in ambipolar-type OFETs by recombination of holes and electrons within the transistor channel. The ambipolar-type feature associated with light-emission will be discussed in **Section 2.5.** In this section, only electrical characteristics of ambipolar-type OFETs will be discussed.

For an ambipolar-type OFET, both electrons and holes are accumulated depending on the applied voltages. To understand ambipolar-type operation in OFET, let us assume an OFET at a given positive drain voltage V_D (the source potential is held at ground, Vs = 0 V) and start with a positive gate voltage of $V_G > V_D$. Like a typical n-type OFET, the gate electrode is more positive than the source electrode and thus electrons are injected from the source into the accumulation layer and drift toward the drain, given that $V_g > V_{th,e}$ ($V_{th,e}$ is threshold for electron accumulation). Only one polarity of carriers is present, and we call this the unipolar regime. On the other hand, if V_G is smaller than V_D, the gate potential is more negative than that of the drain electrode by V_G - V_D. While, for $V_G < V_{th,e}$, the source will not inject electrons, the drain electrode in an ambipolar transistor will inject holes into the channel if V_G - $V_D < V_{th,h}$ ($V_{th,h}$ is threshold for hole accumulation). Thus, one should

actually now speak of the drain electrode as a hole source. A hole current will flow, and thus, the measured drain current will be high, not like in a unipolar, n-channel transistor, which would now be in an off-state. If the gate potential is somewhere between V_D and V_S so that it is bigger than $V_{Th,e}$ but also V_G - V_D < $V_{Th,h}$ (Figure 2.5(a)), both the source and drain electrode will inject the respective charge carriers and thus both electrons and holes are present in the channel. This regime is called the ambipolar regime, in contrast to the unipolar regime, where only one polarity of charges is present in the channel for any particular biasing condition.

In an ideal ambipolar transistor with just one semiconducting layer, the ambipolar regime is characterized by a hole and an electron accumulation layer next to the respective electrode that meet at some point within the transistor channel (inset of Figure 2.5(b)). There, oppositely charged carriers recombine. In electroluminescent materials, this leads to light emission from within the channel, which will be discussed in **Section 2.5**.

The length of each channel and thus the meeting point and position of the recombination zone depend on the applied gate and source-drain voltage and mobility ratio. The potential of the transistor channel in the ambipolar regime can roughly be imagined as that of a saturated hole and electron channel in series, resulting in an S-shaped transition region (Figure 2.5(b)), as shown in previous studies [47-49]. The transfer curves of ambipolar transistors exhibit a characteristic V-shape with one arm indicating electron transport and the other indicating hole transport (see Figure 2.5(c)). For positive (negative) applied voltages, the effective gate voltage for holes (electrons) depends on the applied source-drain voltage, which gives rise to the characteristic dependence of the transfer characteristics on the source-drain voltage. The output curves are characterized by a superposition of standard saturated behavior for one carrier at high V_G and a super-linear current increase at low V_G and high V_{DS} due to injection of the opposite carrier (Figure 2.5(d)).

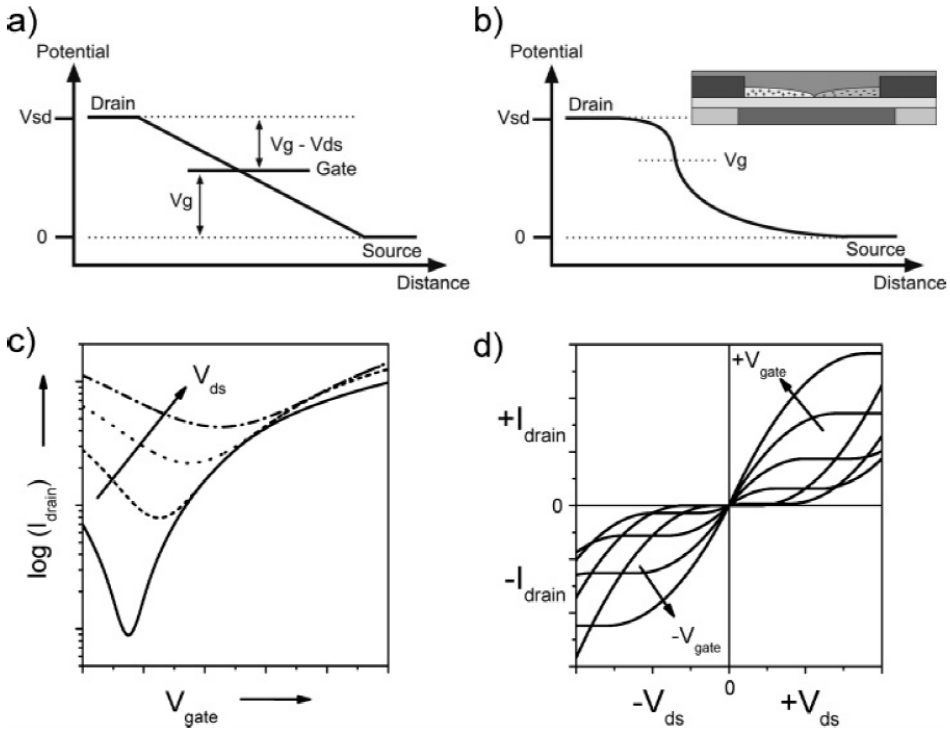

Figure 2.5 (a) Illustration of the electrode potentials in an OFET. (b) Channel potential in an OFET in the ambipolar-type with two separate channels of holes and electrons that meet in the channel where opposite charge carriers recombine (inset). (c) Transfer characteristics of an ambipolar transistor. (d) Output characteristics of various values of V_G and V_{DS}. (Ref. [18])

There are three major groups of ambipolar transport OFETs, which can be classified by the semiconducting layer: single ambipolar OSC, blended OSCs, and bilayer OSC(s) [43].

One of the challenges of fabricating ambipolar transistors with single OSC lies in the efficient injection of both charge carriers. Optimal charge injection takes place when the work function of the metal electrode lines up with the HOMO level of the semiconductor for hole injection and with the LUMO level for electron injection. Since most of the standard organic semiconductors have band gaps of 2-3 eV, the injection of at least one carrier must be contact limited for any given electrode

material. Another challenge is trapping of one or both carrier types. We have seen that especially electrons are likely to be trapped by impurities or certain chemical moieties at the dielectric/semiconductor interface. This can be prevented by using appropriate dielectrics, using pure materials, and processing in an inert atmosphere. The stability of hole and electron transport under ambient conditions, and thus exposure to moisture and oxygen, is another issue.

An alternative method of using blends of n- and p-channel materials is suggested to realize ambipolar-type transport in a single OSC layer. For the blend approach, both co-evaporated and solution-processed films are possible. Those results show good ambipolar characteristics but mobility of each carrier is smaller than that of the pure materials [50]. This can be understood in terms of interpenetrating networks of n-channel and p-channel materials, which predominantly conduct one or the other carrier due to their different electron affinities and ionization potentials, and thus, the effective mobilities of both electrons and holes in a percolating network are lower compared to that of a neat film. Some studies reveal that the ambipolar characteristics of these blend films depend strongly on the nature of the dielectric they are spun upon and the resulting film morphology [51]. Inverters fabricated with such blends show high gain [52] and thus could be suitable for integrated circuits. However, those OSC film formed by blends of two material have experienced poor surface properties such as non-uniform grains, high surface roughness, and high grain boundary resistance.

Another way to achieve the balanced ambipolar-type electrical characteristics is suggested as an OFET with bilayer configuration. A lot of bilayer structures such as pentacene/PTCDI-$C_{13}H_{27}$, pentacene/C_{60}, and DH4T/PTCDI-$C_{13}H_{27}$ have been found to exhibit ambipolar behavior [53, 54].

However, there are some major issues of bilayer structure. First, few case of ambipolar bilayer OFETs based on solution-processed semiconductors have been

demonstrated up to now, due to the problem of degradation of bottom OSC from the solvent of top OSC. Second problem is that the one OSC is not directly contact with source/drain electrode, so injection is not balanced. Moreover, one OSC layer screens the electrical field from the gate electrode toward the other OSC layer, so the gate-controllability is greatly reduced for one-type of charges. As a result, the mobility of each charge carrier in bilayer is lower than that of OFET with single layer.

2.3. Role of injection barrier height in in organic field-effect transistors

In recent decades, the development of OSCs have demonstrated carrier mobility of over 10 cm^2/Vs in organic field-effect transistors [1, 18, 43]. This value is comparable or even exceeding the mobility of amorphous/polycrystalline silicon-based FETs. In spite of this surprisingly high charge transport in OSCs, the need for improvement in contact injection properties in OFETs remains. That is, before a current flow through the transistor channel, the charges have to be injected from the source electrode into the semiconductor. For charges to be injected, electrons should be injected into the LUMO level in case of n-type OFET and holes should be injected into the HOMO level of the semiconductor in case of p-type OFETs, For injection of charges from electrode to OSC, injection barrier height plays critical role on determining the amount of injected charges at same bias condition. The injection barrier can be defined as difference between the work-function of electrode and the HOMO/LUMO level of OSC for holes/electrons. When the work function of the injecting metal is close to the HOMO or LUMO level of the semiconductor, an ohmic contact is expected [55]. In ohmic contact cases, the charges are easily injected from the electrode to OSC without potential loss. Otherwise, the charges have to overcome the injection barrier so the loss of potential at the contact exist. The amount of potential loss is expressed as an additional resistance (contact resistance) in the OFET. Contact resistance can be measured as the voltage drop at the electrodes by means of Kelvin probe, four-point probe measurements, or by transfer line method [18]. In a short-channel OFET with high OSC material, contact resistance can be significant or even larger than the channel resistance and effective mobility is greatly reduced than that of OSC material itself [56]. In particular, the linear regime of field-effect transistors is more affected by contact resistance because a large part of the

source-drain voltage already drops at the contacts and not across the channel. High non-ohmic contact resistance can be indirectly observed in the output curve as an initially suppressed and then super-linear current (S-shape) in the linear region. Adjusting the work function of the injecting metal with the HOMO/LUMO levels of an OSC is simple and good way to achieve the low contact resistance. However, the simple matching of the electrode work-function and the HOMO/LUMO of an OSC is sometimes insufficient to decrease the contact resistance. An additional dipole barrier at the interface tends to change the metal work function [57], and thereby the interface barrier height is increased. In this regard, the formation of dipoles at the metal/OSC interface through self-assembled monolayers have been proven to useful approach for enhancing the injection properties of OFETs [58].

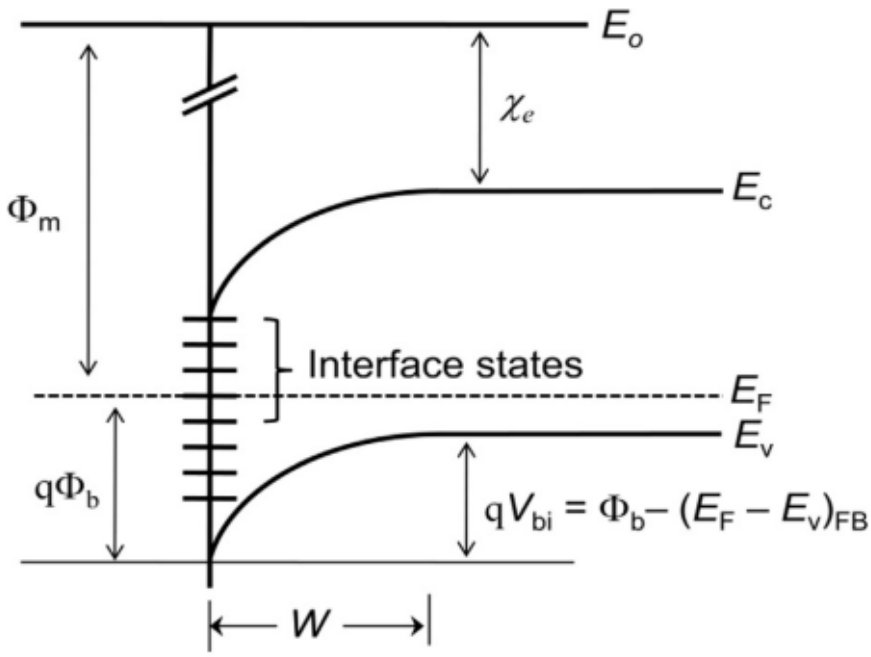

Figure 2.6. The energy band diagram of Schottky barrier with interface states: Φ_m is the metal work function, Φ_b is the Schottky barrier height, χ_e is the electron affinity of semiconductor, V_{bi} is the built-in potential, and W is the depletion width (Ref. [25]).

Additionally, the device structure has influence on the contact resistance. As mentioned in **Section 2.1.**, in a geometry of TGBC and BGTC, the charges are injected over a relatively larger area than in a BGBC configuration. This phenomena, called current crowding, reduces a contact resistance in given materials [59]. Furthermore, while bottom contacts can be modified to alter their work function, evaporated metals may introduce surface states in the semiconductor that help or hamper charge injection [41]. And during the OSC formation, OSC experience different surface energy in the regions of metal and gate-insulator. Those different surface condition leads to the poor morphology of OSC film, for example, non-uniform and smaller grain size. Therefore, non-uniformity of OSC film in bottom contact degrades the transport of charges in the OSC layer.

2.4. Organic light-emitting transistors

2.4.1. General description of organic light-emitting transistors

Recently, organic light-emitting transistors (OLETs) have been attracted a lot of attention for their potential of combining the electrical switching functionality of an OFET and the light generation capability of OLED in a single device [8-11]. OLETs represent a novel class of organic devices, and could pave the way towards nanoscale light sources and highly integrated organic optoelectronics. In addition, it is worth mentioning that OLETs offer an ideal structure for improving the lifetime and efficiency of organic light-emitting materials due to different driving conditions with respect to standard OLED architectures, and to optimized charge-carrier balances. Here, several recent advances in the use of field-effect transistor architectures to achieve light generation from a variety of organic materials are described. The advantages in terms of low fabrication costs and ease of integration on virtually any substrate are highlighted in the discussion of OLETs based on organic thin films. Some possible directions of development and opportunities that could be offered by this new class of devices are also discussed.

Organic light-emitting field-effect transistors were first demonstrated [60] using a device structure with interdigitated gold source and drain electrodes with a charge transport and emitting layer of a tetracene. The electrical device characteristics are typical of a unipolar p-type field-effect transistor, whereas observation of light emission from tetracene proves that electrons and holes are simultaneously injected into the active layer. After this study, many researches have been reported and some the enhancement in luminescence efficiency was demonstrated by scaling down the channel length in unipolar devices. However, the external quantum efficiency has been still very low and needs to be improved for

practical applications. For this purpose, it is necessary to use organic materials with both efficient electroluminescence and transistor characteristics. A promising approach to combine high emission efficiency and good transistor characteristics in OLETs has been reported [61]. In this work, it was shown that by doping active layer, the field-effect characteristics of the OLETs are maintained and the electroluminescence quantum efficiency of the OLET reached 0.8%. In addition, using metals for source and drain electrodes that have a work-function more suitable for holes and electrons injection showed [62, 63] a clear increase of the light-emission efficiency.

Ambipolar transport is a desirable feature for organic semiconductors as it enables the fabrication of complementary logic circuits such as CMOS transistors with in a single device with a single active layer [64]. Moreover, the ambipolar transport can maximize the exciton recombination through electron–hole balance. In ambipolar active layer, the position of the recombination region and resulting emission zone can be tuned by the gate voltage [65]. As a consequent, the exciton quenching is minimized and therefore it will lead to improved internal and external quantum efficiency of the OLETs. However, few materials possesses the high electroluminescence characteristics with high and balanced ambipolar mobility. As alternative approaches, therefore, the methods of the bilayer structure and the use of heterojunction have been suggested to achieve the high ambipolar transport in OLETs.

The bulk heterojunction approach, commonly applied to to LEDs, solar cells and FETs, was adopted for ambipolar OLETs by blending two materials of n-type and p-type. The most important requirement for the two materials used for heterojunction is that the relative positions of their highest occupied molecular orbitals (HOMO) and the LUMO must allow exciton formation and recombination in the material with the smaller energy gap.

The bilayer approach have exhibited the highest balanced mobility values in ambipolar OLET devices so far. Particularly, two groups have shown that in a polymer-based ambipolar light-emitting transistor the emission zone can be moved across the transistor channel on changing the gate bias [66]. In those cases with high opto-electrical performances, a low work-function metal for the electron injection electrode and of a high work-function metal for the hole-injection electrode is used. In addition, the dielectrics with less trap density were selected as the gate insulator to avoid the charge trapping at the interfaces. The observation of a spatially resolved recombination zone, whose location in the transistor channel is controlled by the gate voltage, suggests that the coexistence of electron and hole channels, and therefore the ambipolar transport of both charges actually occurs. The recombination zone is located at the center of the channel when the current of electrons and that of holes are balanced.

However, the spatial separation of the electron-transport layer and the hole-transport layer drastically reduces the probability of electrons and holes meeting to form excitons inside the device channel. In addition, the low mobility values and unbalanced mobility for holes/electrons is remains as the drawback of the ambipolar polymer-based light-emitting transistors.

Very recently, a tri-layer structure consisting of an emission layer sandwiched between an electron- and hole- transporting layer, similar to the conventional OFET configuration, is appeared (Figure 2.7) [67]. Trilayer OLET devices have demonstrated EQE values as large as 5%, outperforming the OLED with the same emission layer and optimized transport layers (2.2%). According to that research, the high value of EQE is achieved by the tri-layers of active layer structure, which enables the effective suppression of essential losses such as the the metal-exciton quenching, the charge-exiction quenching, and the charge-metal quenchings in the channels. Moreover, in the ambipolar operation mode (V_{DS} = -100 V and V_{GS} = -30

V) the light-emitting region is located far from the drain electrodes at a distance of 8 μm, thus preventing photon losses due to exciton-metal quenching. For the transported charges to be effectively transported into the central emission layer, the LUMO level of the n-type transport layer should be similar to the LUMO level of the emission layer and the HOMO level of the p-type transport layer should be aligned with the HOMO level of the emission layer. That is, it is essential for the tri-layer structure to enable to transport the injected charges into the central emission layer. Moreover, in order to accomplish the high field-effect mobility in the transport layers together with the high recombination rate and internal quantum efficiency, the optimization of the interface morphology between the organic layers is strongly required. However, all of above mentioned OLETs constructed in planar geometry have experienced narrow light-emission zone.

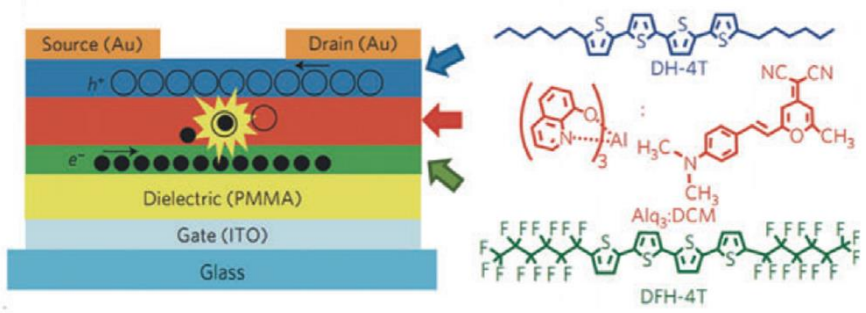

Figure 2.7. Schematic of the trilayer OLET with the chemical structure of each OSC, and the processes of charge transport and light-generation. (Ref. [67])

2.4.2. Vertical organic light-emitting transistors

As discussed in previous section, the planar geometry of OLETs exhibits line- or band-type light-emission, which significantly reduces aperture ratio of OLETs. Therefore, from the viewpoint of expanding the area of light-emission in device with improved electrical characteristics, vertical OLETs have attracted great attention. In the vertical OLETs, the source electrode and the drain electrode is vertically located and the layers of OSCs are located between the two electrodes. Therefore, the short channel length can be easily achieved without additional patterning techniques, resulting in the high speed operation at low voltage. In a vertical architecture, typically a source electrode with periodic vacancies or perforated electrodes [68] and interdigitated electrodes [69] have been used. In those cases, the electric field should be precisely controlled through the vacancies of the source electrode by the gate electrode. As shown in Figure. 2.8, the flow of charge transport can be categorized in two flows: the first flow is lateral charge flow (q_L), which the injected charges from the source electrode flow laterally along the channel area by the gate voltage. The second flow is the vertical charge flow (q_V), which the injected charges moves into the emission layer by the drain voltage. Here, the degree of q_V is governed by the space-charge limited current [70] and is directly propositional to the degree of charge recombination in emission layer for light emission. Since the charge recombination and the resultant light emission are primarily governed by the pathway as well as the magnitude of q_L and q_V from each side of the aperture, the geometrical dimension of the aperture and the thickness of each layer play critical roles on the light emission characteristics including the emission zone and the spatial distribution around the aperture boundary.

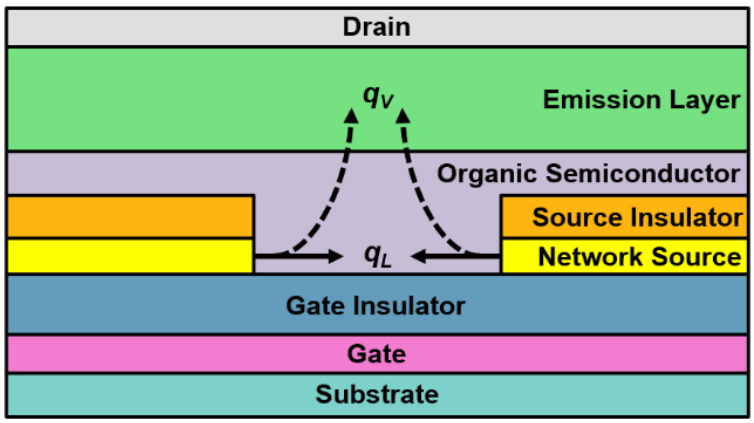

Figure 2.8. Cross-sectional view of a VOLET with a network source electrode having periodic apertures. The lateral charge flow (q_L) and the vertical charge flow (q_V) are depicted as solid and dashed arrows, respectively. (Ref. [68])

Chapter 3. Ambipolar-type Charge Transport of Organic Field-Effect Transistors in Dual-Gate Configuration

3.1. Introduction

Ambipolar-type organic field-effect transistors (OFETs) have been extensively studied for understanding the charge transport phenomena [18] and developing organic electronic devices such as light-emitting devices [71] and complementary integrated circuits [72]. An active, organic semiconductor (OSC) layer is one of the most critical ingredients in ambipolar-type OFETs, and generally consists of a single OSC (Figure 3.1 (a)) [71, 73] or a blend of two different OSCs (Figure 3.1. (b)) [74, 75]. The two cases often encounter with the unbalanced energy barrier and/or high channel resistance from the viewpoints of the charge injection and transport.

To simultaneously improve the injection and the transport of charges in the ambipolar OFETs by structural approach other than the OSC materials used, the device architectures using two stacked OSC layers in single gate configuration, as shown in Figure 3.1 (c), have been demonstrated to balance the carrier mobility and to improve the crystalline structure of each OSC layer [76, 77]. However, in a single gate configuration, the charge control scheme is still limited. For example, for the current flow from one of two OSCs either in the n-type or the p-type operation, the other OSC acts as an additional insulator or a channel of undesired charge carriers. This leads directly to a low on/off current ratio of an ambipolar-type OFET.

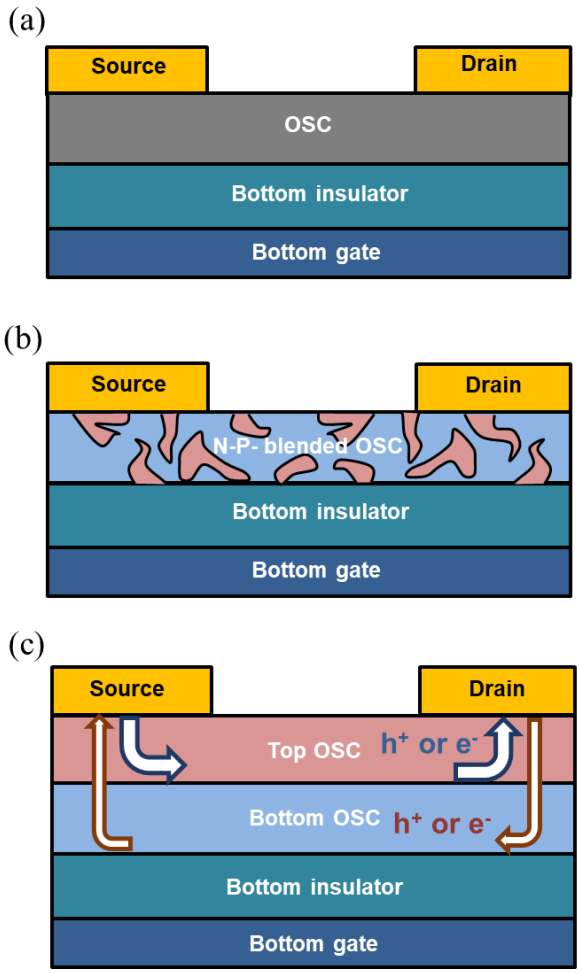

Figure 3.1. Device structures of various ambipolar OFETs with (a) single OSC (b) blended OSC, and (c) bilayer OSCs.

In this work, I present the ambipolar properties of a dual-gate OFET with two OSC-insulator interfaces stacked together [78]. Two active layers of an n-type and a p-type OSCs were stacked between two gate insulator-electrode pairs. In my ambipolar-type OFET structure, the bottom gate insulator-bottom OSC interface was involved in the channel for the p-type operation and the top gate insulator-top OSC interface in the channel for the n-type operation. A combination of two gate voltages from two separated, bottom and top electrodes enables to efficiently control the corresponding charge carriers for the enhancement of the mobility and the on/off current ratio in the ambipolar operation.

3.2. Fabrication of ambipolar-type organic field-effect transistors

A schematic diagram of my ambipolar dual-gate OFET is shown in Figure 3.2. A heavily doped p-type Si substrate was used as a bottom gate electrode and a 300 nm-thick SiO_2 layer was served as the bottom gate insulator. The Si/SiO_2 substrate was cleaned with acetone, isopropyl alcohol, methanol, and deionized water in series for 10 min each under ultra-sonication. The cleaned Si/SiO_2 substrate was subsequently exposed to UV-ozone for 10 min and then spin-coated with hexamethyldisilazane (HMDS) as a buffer layer at 3000 rpm for 30 sec and rinsed to obtain a monolayer. A p-type OSC, poly(4,4-di-n-hexyldithienosilole-alt-(bi)thiophene) (DS6T1 or P1200) dissolved in dichlorobenzene (DCB) in 1 wt.%, was spin-coated at 2000 rpm for 30 sec, followed by annealing at 70°C for the removal of the solvent and thickness was measured as 60 nm [79]. The source and drain electrode were prepared with 50-nm-thick Au which was thermally deposited. Using a shadow mask, the channel length and the channel width were defined to be 150 μm and 1 mm, respectively. An n-type OSC, poly{[N,N9-bis(2-octyldodecyl)-naphthalene-1,4,5,8-bis(dicarboximide)-2,6-diyl]-alt-5,5-(2,29-bithiophene)} [P(NDI2OD-T2) or N2200] dissolved in p-xylene in 1 wt.%, was spin-coated at 2000 rpm for 30 sec and subsequently baked at 110°C for 6 hr in a vacuum dry oven, of which thickness was 60 nm. The top gate insulator was prepared using poly(methyl methacrylate) (PMMA), dissolved in ethyl acetate in 8 wt.%, by spin-coating at 3000 rpm for 30 sec and annealed at 100°C for 1 hr. The thickness of the PMMA film was about 1.8 μm. The top gate electrode was made of 50-nm-thick Al. All the electrical characteristics of my ambipolar OFET were measured using a semiconductor analyzer (HP 4155A) at room temperature under ambient condition.

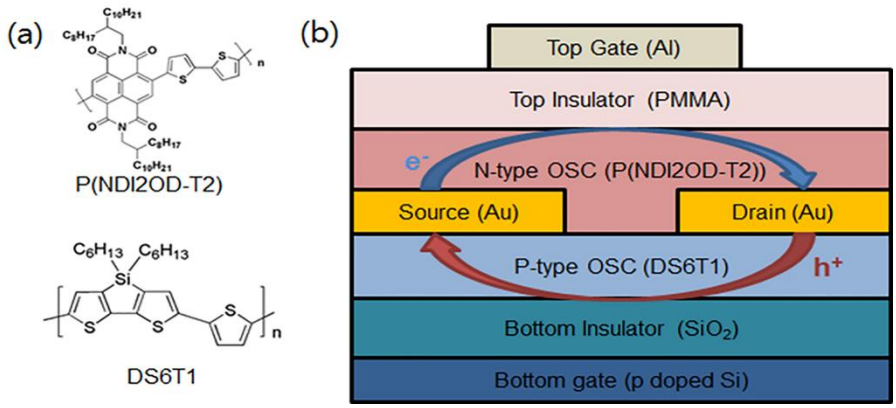

Figure 3.2. Device structure of an ambipolar-type OFET with dual-gate, two-stacked OSCs, which has two OSC/metal interfaces for corresponding two separate channels.

3.3. Experimental results and discussions

3.3.1. Electrical characteristics in single gate configuration

I first measure the unipolar characteristics of both the n-type and the p-type OSCs in conventional top- and bottom-gate OFETs with single OSC-insulator interfaces (SIs) to optimize the stacking sequence of two OSC-insulator pairs. Figure 3.3 show the transfer characteristics of the OFETs with P1200 and Figure 3.4 show those with N2200 in the top- and bottom-gate geometries, respectively.

The measured mobility of the SI-OFET with P1200 was about 4.7×10^{-4} cm^2/Vs in the top-gate geometry from Figure 3.3(a) and 1.3×10^{-3} cm^2/Vs in the bottom-gate geometry from Figure 3.3(b). The mobility for the N2200 case was 6.4×10^{-2} cm^2/Vs in the top-gate geometry from Figure 3.4(a) and 1.7×10^{-2} cm^2/Vs in the bottom-gate geometry from Figure 3.4(b). As a consequence, a bottom-gate geometry for the p-type operation (P1200) and a top-gate geometry for the n-type operation (N2200) are desirable in an ambipolar OFET. This is also hinted by the facts that for the p-type operation, less charge traps are produced at the P1200-SiO_2 interface than the P1200-PMMA interface and N2200 shows the high molecular regioregularity as well as the electronic structure suitable for the n-type operation [80, 81].

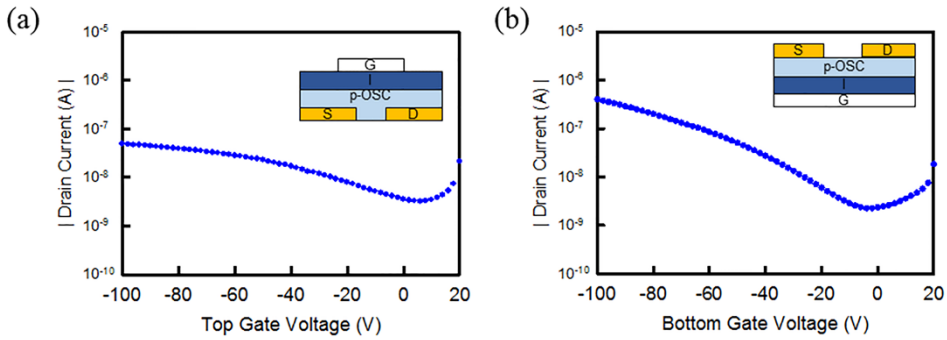

Figure 3.3. Transfer curves of SI-OFETs having OSC layer of P1200 in the (a) top gate configuration and (b) bottom gate configuration with single gate electrode. (Ref. [78])

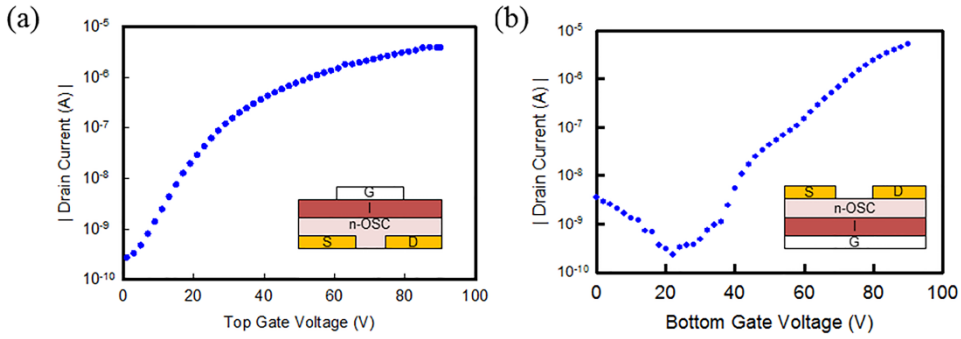

Figure 3.4. Transfer curves of SI-OFETs having OSC layer of N2200 in the (a) top gate configuration and (b) bottom gate configuration with single gate electrode.

3.3.2. Electrical characteristics in dual-gate configuration

Based on the above results, specifically from Figures of 3.3(b) and 3.4(a), P1200 and N2200 were used in the bottom-gate and the top-gate geometries, respectively, for constructing an ambipolar-type OFET as depicted in Figure 3.2(b). The unipolar and ambipolar electrical characteristics of my OFETs with dual OSC-insulator interfaces (DI) were investigated under the condition that a single gate voltage was swept (Figure 3.5) or two gates were swept (Figure 3.6), respectively.

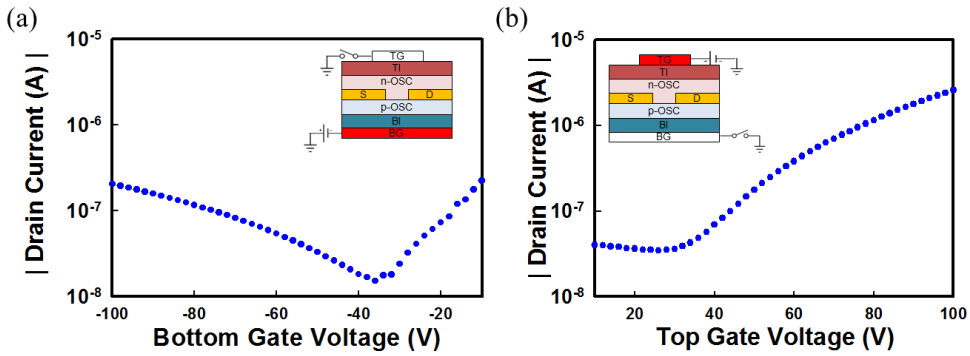

Figure 3.5. Transfer curves of an ambipolar OFET with dual-gate: (a) p-type operation (sweeping bottom gate) with floated top gate, and (b) n-type operation (sweeping top gate) with floated bottom gate (Ref. [78]).

First, I discuss the single gate operation of the DI-OFET when one of two gates is floated. For the p-type operation of the DI-OFET when the bottom gate was swept while the top gate was floated, the mobility was measured to be 6.2×10^{-4} cm^2/Vs from Figure 3.5(a) and the off-current was substantially increased compared to the SI-OFET case in Figure 3.3(b). This is attributed to the formation of a virtual n-channel in the top n-type OSC. Although the hole-channel is turned-off when V_{GS} = 0 V and V_{DS} = – 80 V, the electrons would feel as if V_{GS} = 80 V and V_{DS} = 80 V. In other words, due to the presence of the top n-type OSC, a virtual electron-channel can be formed during the suppression of the hole-channel under the condition that the bottom gate voltage is swept toward the negative direction. Consequently, the

on/off ratio is significantly decreased due to formation of n-channel in the DI-OFET even in the turn-off voltage region of the p-type SI-OFET. For the n-type operation of the DI-OFET when the top gate was swept while the bottom gate was floated, the mobility was about 5.0×10^{-2} cm^2/Vs, determined from Figure 3.5(b), which is nearly slightly decreased from the SI-OFET case in Figure 3.4(a). Similar to the formation of electron-channel in the p-type operation in Figure 3.5(a), the high off-current and low on/off ratio are observed in this case, which results from the formation of a virtual hole-channel in the bottom p-type OSC layer. This low on/off ratio induced by the formation of virtual counter channel is commonly observed phenomena in ambipolar-type OFETs, which should be avoided to achieve good electrical properties by means of an electrically controllable scheme such as a dual-gate configuration [82].

I now describe the relative roles of the bottom and top gate voltages on the off-current and the output characteristics of my DI-OFETs for the ambipolar-type operation. As shown in Figure 3.6(a), for the p-type operation, the off-current as a function of the bottom gate voltage ($V_{G\text{-}B}$) was greatly decreased with increasing a bias voltage at the top gate ($V_{G\text{-}T}$) above a certain value (about – 40 V) in the negative direction. It is noted that under zero bias voltage at the top gate ($V_{G\text{-}T}$ = 0 V), the virtual electron-channel is not suppressed at all in my case (black dotted line) irrespective of the bottom gate voltage. The drain current is the sum of the currents in the hole-channel and the electron-channel. Since the drain current flowing in the electron-channel is 10 times greater than that in the hole-channel as shown in Figures of 3.3(b) and 3.4(a), the total drain current does not seem to be modulated by the bottom gate voltage whether the suppression of the hole-channel is occurred or not. For the n-type operation, similar suppression of the off-current was observed with increasing the top gate voltage as shown in Figure 3.6(b). The only difference is that the modulation of the drain current is observed even under zero bias voltage at the

counter gate ($V_{G\text{-}B}$ = 0) compared to the case of Figure 3.6(a). This is because even though the virtual hole-channel is formed, the drain current flowing in the hole-channel is much lower than that in the electron-channel.

The on/off current ratio of my ambipolar-type DI-OFET remains still quite low (only on the order of 10^2) even though off-current was decreased with suppression of virtual-channel. However, the on/off ratio can be much improved by increasing on-current through the proper interfacial modification and the optimized channel dimension for given OSC materials.

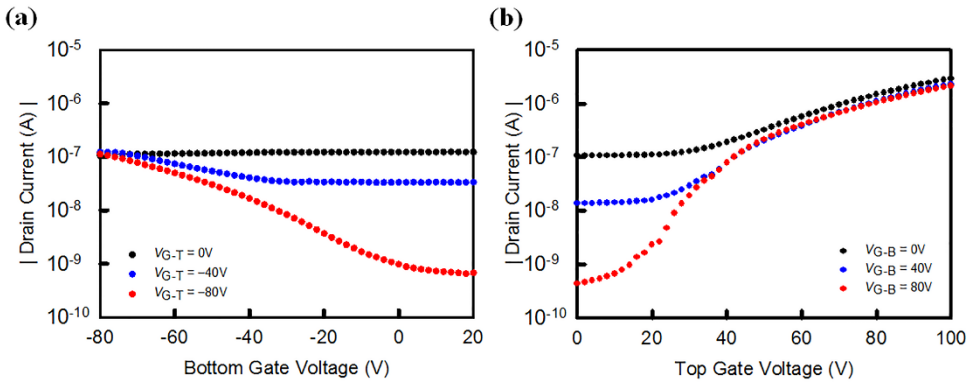

Figure 3.6. Transfer curves of an ambipolar OFET with dual-gate: (a) p-type operation (sweeping bottom gate) with negatively biased top gate, and (b) n-type operation (sweeping top gate) with positively biased bottom gate (Ref. [78]).

Figure 3.7 shows the output characteristics of the DI-OFET as a function of the sweeping drain voltage at several different bias voltages for the p-type operation and the n-type operation, respectively. Clearly, the ambipolar-type operation was observed. The saturated drain current in the p-type operation is almost ten times less than that in the n-type operation, which is due to the intrinsic property of the p-type OSC I used. The mobility of the dual-gate OFET was measured to be 5.7×10^{-4} cm^2/Vs for the p-type operation and 6.9×10^{-2} cm^2/Vs for the n-type operation. The dual-gate OFET enables to individually control the degree of accumulation and transport of charges in the p-channel or that in the n-channel, allowing the use of two

different OSCs in a stacked manner.

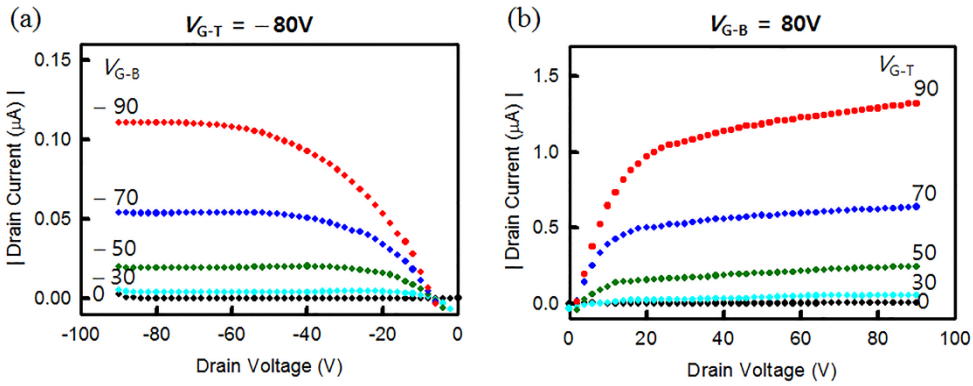

Figure 3.7. Output curves of ambipolar OFET with dual gate: (a) p-type operation at the V_{G-T} = – 80 V while V_{G-B} was varied from 0 V to – 90 V, and (b) n-type operation at the V_{G-B} = 80 V while V_{G-T} was varied from 0 V to 90 V (Ref. [78]).

3.4. Conclusions

I demonstrated a dual-gate configuration of an ambipolar-type OFET with two different OSC-insulator interfaces. The combination of two individual gate voltage is capable of controlling the charge transport in a two stacked organic semiconductors. My approach may offer one of the solutions to eliminate the disparity of the electrical properties between the p-type operation and the n-type operation in the ambipolar-type OFET. However, the improvement of the device performance through the use of the OSC materials having excellent electrical properties, the precise control of the interfaces, and the optimization of the device architecture remains to be pursued for practical applications as integrated organic circuits.

Chapter 4. Enhancement of Charge Injection in Organic Field-Effect Transistors by Semiconducting Organic Buffer Layer

4.1. Introduction

Recently, organic field-effect-transistors have been extensively investigated for the application of high-speed integrated circuits. [1, 18, 43] Due to the rapid development of the novel OSCs and/or the various coating technique [1, 18, 43], the mobility of OFETs reaches up to the 10 cm^2/Vs. [18, 43] In such OFETs having high mobility, however, the overall electrical performance was greatly hampered by a high injection barrier at the organo-metal interface. [83] The injection barrier ($\Delta\phi_B$), defined as the difference of energy level between the work-function of source electrode ($\Delta\phi_S$) and the highest occupied molecular orbital (HOMO) energy level of the OSC layer, is one of the key factors governing the injection mechanism at the heterogeneous interface of metal and OSCs. According to the degree of $\Delta\phi_B$, the different injection mechanism is applied to corresponding OFETs. In specific, the quasi-ohmic injection occurs in small $\Delta\phi_B$ ($0 \leq \Delta\phi_B < 0.3$ eV), the thermionic injection in intermediate $\Delta\phi_B$ ($0.3 \leq \Delta\phi_B < 0.6$ eV), and the tunneling injection in high $\Delta\phi_B$ ($0.6 \leq \Delta\phi_B$). [84] Therefore, the potential drop at the interface and resultant contact resistance is increased at high $\Delta\phi_B$. As a consequence, the overall mobility of OFET is greatly decreased by the high contact resistance [83, 84].

In this regard, the reduction of $\Delta\phi_B$ is critical issue to improve injection properties of OFETs. One of the simple approaches is adopting high work-function metals as source/drain electrodes in order to match $\Delta\phi_S$ and the HOMO level of

active layer ($HOMO_{OSC}$) [85-87]. In cases of high mobility OSCs, the value of $HOMO_{OSC}$ is usually higher than 5 eV and only few metals exhibits $\Delta\phi_S$ over 5 eV. In addition, the unexpected energy shift induced by the surface dipoles strongly depend on the process conditions [86] or the push-back effect [87] can deteriorate the injection properties even though $\Delta\phi_S$ and $HOMO_{OSC}$ is well-matched. As an alternative, the introduction of buffer layer such as the surface modification of self-assembled monolayer [88], an oxide layer [89], and a doped layer [90] has been proposed. Among them, a contact-area-limited oxide buffer layer [89] or doped buffer layer [90] has been successfully demonstrated to improve the electrical characteristics in top contact configuration. However, the diffusion of buffer layer into the active layer hampers the long-term stability of OFETs. In addition, those previous studies covered only the reduction of injection barrier, and thus a comprehensive picture of the relationship between the energy level as well as the mobility of the buffer layer and the electrical performance of the OFET is remains to be solved.

In this work, I introduced the semiconducting organic buffer layer (SOBL) to enhance the charge injection and transport of the OFETs. For the efficient injection, the amount of the injected charges should be increased and the injected charges should be transported to the channel area [83]. In this regard, I extensively investigated the effect of SOBL from the viewpoint of two parameters: (i) the HOMO level of SOBL ($HOMO_{SOBL}$) which would reduce the injection barrier and increase the number of the injected charges from the source electrode by tailoring injection mechanism, and (ii) the mobility of SOBL (μ_{SOBL}) which is directly related to the transport of injected charges to the active layer. The typical OFET in the top contact configuration together with its energy diagram is shown in Figure 4.1(a) and that having SOBL is shown in Figure 4.1(b). For the typical OFET, the injection barrier is denoted as $\Delta\phi_B$. In the OFET with SOBL, the injection barrier can be characterized

by sum of $\Delta\phi_{M\text{-}S}$ (difference of energy level between the metal and SOBL) and $\Delta\phi_{S\text{-}O}$ (difference of energy level between the SOBL and active OSC layer). Here, two types of the injection barrier in case of intermediate height ($\Delta\phi_B$ = 0.4 eV, thermionic injection barrier) and that of high height ($\Delta\phi_B$ = 0.6 eV, tunneling injection barrier) were studied in OFETs with top contact configuration. In our numerical simulations, the ratio of $\Delta\phi_{M\text{-}S}$ versus $\Delta\phi_{S\text{-}O}$ ($\Delta\phi_{M\text{-}S}$: $\Delta\phi_{S\text{-}O}$) and μ_{SOBL} were varied and the injection properties were investigated at the interface in terms of the degree of potential drop at the contact (V_C). In addition, the effective mobility of OFET was extracted from the simulated transfer curves of OFET. Finally, in the basis of our simulation, the materials for the source/drain electrodes, the active layer, and SOBL were selected. The fabricated OFETs with SOBL exhibit the improved electric characteristics, which was well agree with the simulation results. This work provides a scientific basis for unravelling the mechanism for the charge injection in the OFET by the introduction of semiconducting organic buffer layer.

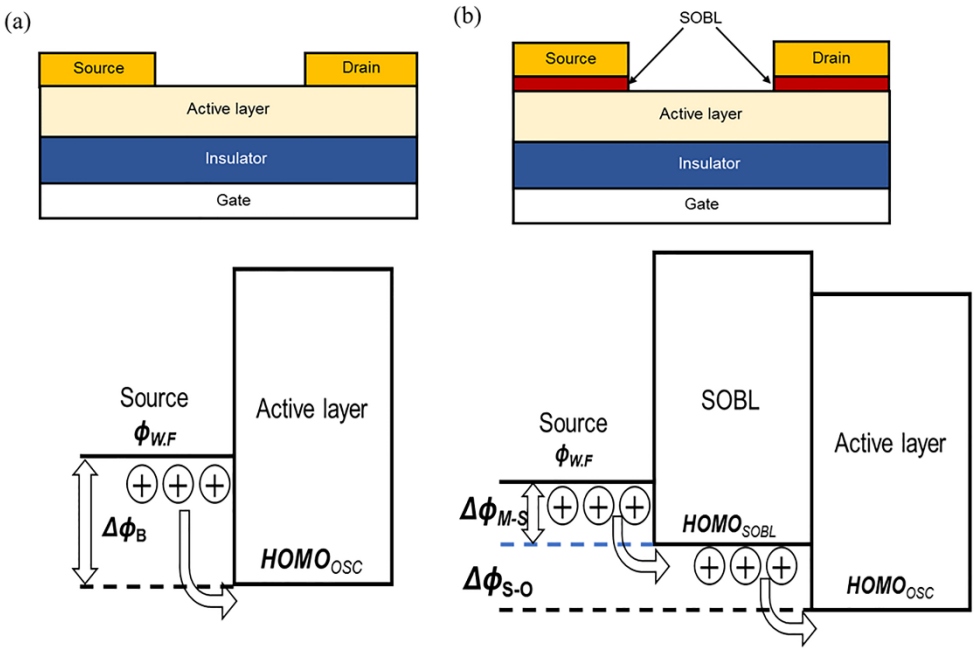

Figure 4.1. Device structures and corresponding energy diagram of (a) an OFET without semiconducting organic buffer layer (SOBL) and (b) an OFET with SOBL, respectively.

4.2. Numerical simulations

4.2.1. Simulation model and device parameters

Numerical simulations of the electrical characteristics of our OFET were performed using a commercial two-dimensional (2-D) device tool (Atlas, Silvaco). This simulator can obtain the electrical characteristics of a device under the bias conditions by solving Poisson's equation together with the continuity equation. The electrostatic potential ψ related to the space charge density in Poisson's equation is given as follows

$$\varepsilon\nabla^2\psi = -\ q(p - n + N_D - N_A) \tag{4.1}$$

where ε is the dielectric constant, q represents the fundamental charge, and N_D and N_A denote the concentration of donors and that of acceptors, respectively. For the boundary condition, the surface potential ψ_s at the Schottky contact is given by

$$\psi = V_o - \ E_g/2q + \Delta\phi_B \tag{4.2}$$

where V_o denotes the applied bias to the source or drain electrode. E_g represents the energy gap between the highest occupied molecular orbital (HOMO) and the lowest unoccupied molecular orbital (LUMO) energy level of the OSC, given by E_{HOMO} - E_{LUMO} where E_{LUMO} and E_{LUMO} are the energy levels of HOMO and LUMO, respectively. $\Delta\phi_B$ denotes the Schottky barrier height between the electrode and the OSC. Here, $\Delta\phi_B$ can be expressed as $E_{HOMO} - \phi_M$ for holes or ϕ_M - E_{LUMO} for electrons where ϕ_M is the work-function of the electrode.

Our device is a p-type OFET, so the current density of holes was considered. The current density of holes (J) is gained from the equation (4.3)

$$J = qp\mu F + qD\nabla p \tag{4.3}$$

where F denotes the electric field extracted from the gradient of the electrostatic potential ψ, namely, $F = -\nabla\psi$. The potential ψ was determined from equations of (1)

and (2). The concentrations of holes are p, and the intrinsic carrier mobility and the diffusion coefficient are denoted by μ and D. The material parameters of μ was taken from the literature values and D is given by $D = (kT/q)\mu$.

The effective mobility of OFET in saturation region(μ_{eff}) can be extracted from the transfer curve and calculated from the Eq. (4.4)

$$I_D = \mu_{eff} C_i (W/2L)(V_{GS} - V_{th})^2 \quad (4.4)$$

where I_D is the drain current, W and L denote width and length of channel, C_i is the capacitance of gate insulator layer, V_{GS} is the voltage difference between the gate electrode and the source electrode, and V_{th} is the threshold voltage of an OFET. As conventional operation conditions for OFETs, the bias condition of the V_{GS} = - 50V with the drain voltage (V_D) of – 50 V is applied for obtaining transfer curves. The material parameters such as E_{HOMO}, E_{LUMO}, μ, and C_i used in our simulation were summarized in Table 4.1.

For analyze the effect of SOBL in OFETs, the simulation was performed with varying two parameters: one is the ratio of $\Delta\phi_{M\text{-}S}$: $\Delta\phi_{S\text{-}O}$ which is determined by the location of $HOMO_{SOBL}$ between the ϕ_S and the E_{HOMO} of the OSC, and the other is μ_{SOBL}. Here, two OFETs having different $\Delta\phi_B$ were compared. One is an OFET with $\Delta\phi_B$ = 0.4 eV in which thermionic injection is dominant. The other is an OFET with $\Delta\phi_B$ = 0.6 eV in which tunneling injection mechanism is dominant.

Table 4.1. The electrical parameters of materials used in simulation

Layer	Material	E_{HOMO} or ϕ (eV)	μ_{eff} (cm^2/Vs)	Thickness (nm)
SOBL	Pentacene	4.9 – 5.2	0.001 - 0.8	10
OSC	TIPS-Pentacene	5.3	0.4	100
Source/ Drain	Ag or Au	4.7 or 4.9	-	50

4.2.2. Potential distribution in the channel

The shape of the potential in the contact region mainly determines on the amount of charges injected from the electrode. The voltage available across the channel ψ ($\psi = V_D - V_C$) is closely correlated with the degree of current flowing in the channel region, as expressed in equation (4.1). It is commonly known that when the high injection barrier height is present at the interface of OSC/source electrode, the large V_C at the interface leading to the high contact resistance and hampering the injection properties [83, 85]. Therefore, the insertion of SOBL between the source electrode and active layer can divide single barrier $\Delta\phi_B$ into two barrier ($\Delta\phi_{M\text{-}S} : \Delta\phi_{S\text{-}O}$) to change the injection mechanism. In addition, the high mobility of SOBL will enhance the transport of injected charges to the channel area. In this regard, the numerical simulations of OFETs with/without SOBL in terms of potential distribution were performed. I would more extensively discuss the effective injection at the contact area of both OFETs in terms of the potential loss V_c.

At first, the ratio of $\Delta\phi_{M\text{-}S} : \Delta\phi_{S\text{-}O}$ is varied while μ_{SOBL} is fixed as 0.2 cm^2/Vs. Figures 4.2(a) and 4.2(b) represent the calculated cross-sectional profiles of potential at channel region (1 nm above the interface between OSC and the gate insulator) in the OFET having $\Delta\phi_B$ = 0.4 eV and that having $\Delta\phi_B$ = 0.6 eV, respectively. The potential distribution of OFET without SOBL is drawn in black solid line. Each potential distribution of OFETs with SOBL having value of $\Delta\phi_{M\text{-}S} : \Delta\phi_{S\text{-}O}$ = 2 : 1, 1 : 1, and 2 : 1 is depicted in green dash-dots, red dashes, and blue dash-dot-dot patterns, respectively.

In the case of OFET having $\Delta\phi_B$ = 0.4 eV without SOBL, V_C at the source-channel interface was – 12.2 V. However, the introduction of SOBL greatly decreases V_C. Specifically, the value of V_c is – 2.5 V for $\Delta\phi_{M\text{-}S} : \Delta\phi_{S\text{-}O}$ = 1 : 1, – 3.1 V for $\Delta\phi_{M\text{-}S} : \Delta\phi_{S\text{-}O}$ = 2 : 1 and – 4.1 V for $\Delta\phi_{M\text{-}S} : \Delta\phi_{S\text{-}O}$ = 1 : 2. That is, when $\Delta\phi_{M\text{-}S} : \Delta\phi_{S\text{-}O}$ =

1 : 1, the $\Delta\phi_{M\text{-}S} = \Delta\phi_{S\text{-}O} = 0.2$ eV so the quasi-ohimic injection is occurred in two barriers. On the other hand, when $\Delta\phi_{M\text{-}S} : \Delta\phi_{S\text{-}O} = 2 : 1$ or $1 : 2$, the two barriers are divided unequally, and in larger barrier, the thermionic injection is happened so the amount of injected charges are decreased. Therefore, the introduction of SOBL can effectively enhance the current of OFET.

In the case of OFET having $\Delta\phi_B = 0.6$ eV without SOBL, V_C at the source-channel interface was – 44.9 V, which makes little voltage (around 5 V) is applied for the transport of charges along the channel. However, if SOBL is inserted, V_C was significantly decreased. For instance, $V_C = -4.7$ V for $\Delta\phi_{M\text{-}S} : \Delta\phi_{S\text{-}O} = 1 : 1$, $V_C = -12.3$ V for $\Delta\phi_{M\text{-}S} : \Delta\phi_{S\text{-}O} = 2 : 1$, and $V_C = -16.3$ V for $\Delta\phi_{M\text{-}S} : \Delta\phi_{S\text{-}O} = 1 : 2$. Consequently, the voltage across the channel is increased and effective transport along the channel is happened. From the results, the loss of potential at the interfaces was greatly reduced by the dividing single barrier in two small barriers by SOBL, which leads to the transport of accumulated charges can be effectively happened in the channel region. Moreover, when $\Delta\phi_{M\text{-}S} : \Delta\phi_{S\text{-}O} = 1 : 1$, V_C was minimized so effective current density and following mobility can be enhanced. Again, when $\Delta\phi_{M\text{-}S} : \Delta\phi_{S\text{-}O} = 1 : 1$, the $\Delta\phi_{M\text{-}S} = \Delta\phi_{S\text{-}O} = 0.3$ eV so the thermionic injection is occurred in two barriers. On the other hand, when $\Delta\phi_{M\text{-}S} : \Delta\phi_{S\text{-}O} = 2 : 1$ or $1 : 2$, at the larger barrier, the tunneling injection is happened so the amount of injected charges are greatly decreased.

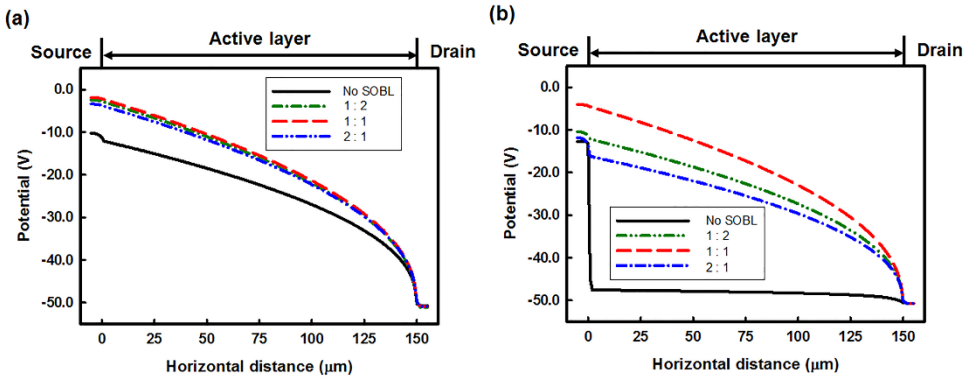

Figure 4.2. Spatial distribution of potential in the channel at various $\Delta\phi_{M\text{-}S} : \Delta\phi_{S\text{-}O}$ ratio with (a) $\Delta\phi_B$ = 0.4 eV and (b) $\Delta\phi_B$ = 0.6 eV. Black line represents the potential distribution in OFET without SOBL, the green dot-dashes represent that in OFET with $\Delta\phi_{M\text{-}S} : \Delta\phi_{S\text{-}O}$ = 1 : 2, the red dashes represent that in OFET with $\Delta\phi_{M\text{-}S} : \Delta\phi_{S\text{-}O}$ = 1 : 1, and the blue dash-dot-dot patterns represent that that in OFET with $\Delta\phi_{M\text{-}S} : \Delta\phi_{S\text{-}O}$ = 2 : 1.

The μ_{SOBL} also affects on the V_C. To observe sole effect of μ_{SOBL}, $\Delta\phi_{M\text{-}S} : \Delta\phi_{S\text{-}O}$ was fixed to 1 : 1 and μ_{active} to 0.4 cm^2/Vs. As shown in Figure 4.3, the increase of μ_{SOBL} greatly reduces the loss of potential at the source/channel interface. For the case of $\Delta\phi_B$ = 0.4 eV, V_C = – 12.2 V without SOBL, V_C = – 4.9 for μ_{SOBL} = 0.001 cm^2/Vs, and V_C = – 2.5 V for μ_{SOBL} = 0.2 cm^2/Vs. The impact of μ_{SOBL} is more evident in case of high injection barrier. V_C = – 44.9 V without SOBL, V_C = – 29.5 for μ_{SOBL} = 0.001 cm^2/Vs, and V_C = – 4.7 V for μ_{SOBL} = 0.2 cm^2/Vs.

From above simulation results, it is clear that higher μ_{SOBL} can successfully reduce the V_C by transporting more charges to channel area. As a result, the effective mobility of OFET is increased with the higher mobility of SOBL.

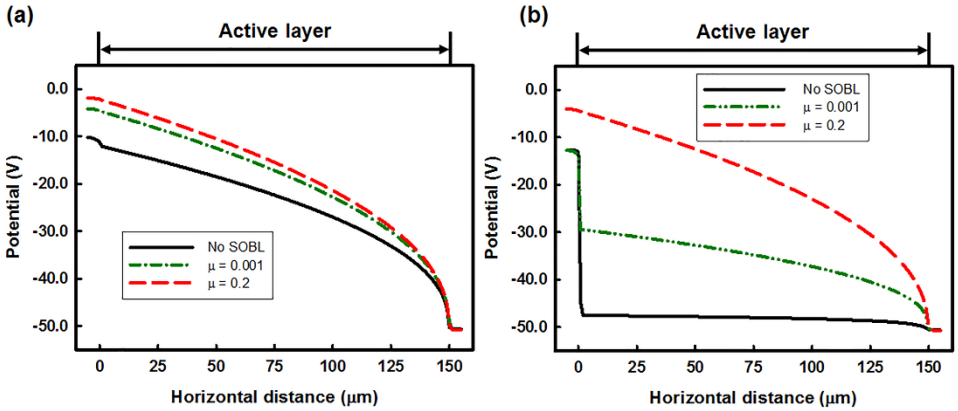

Figure 4.3. Spatial distribution of potential in the channel at different mobility of SOBL having (a) $\Delta\phi_B$ = 0.4 eV and (b) $\Delta\phi_B$ = 0.6 eV. Black line represents the potential distribution in OFET without SOBL, the green dot-dashes represent that in OFET with the mobility of SOBL as 0.001 cm^2/Vs and the red dashes represent that in OFET with with the mobility of SOBL as 0.2 cm^2/Vs.

4.2.3. Effect of semiconducting organic buffer layer on the effective mobility

In Figure 4.4, the calculated effective mobility of OFET in terms of various ratio of $\Delta\phi_{M\text{-}S}$ to $\Delta\phi_{S\text{-}O}$ ($\Delta\phi_{M\text{-}S} : \Delta\phi_{S\text{-}O}$) and E_{SOBL} is presented. The relation of μ_{SOBL} and effective mobility of OFET is shown in the Figure 4.2(a) when the $HOMO_{SOBL}$ is close to ϕ_S ($\Delta\phi_{M\text{-}S} : \Delta\phi_{S\text{-}O} = 2 : 1$), in Figure 4.2(b) when the E_{SOBL} is located in the middle of ϕ_S and $HOMO_{OSC}$ ($\Delta\phi_{M\text{-}S} : \Delta\phi_{S\text{-}O} = 1 : 1$), and in Figure 4.2(c) when $HOMO_{SOBL}$ is rather close to $HOMO_{OSC}$ ($\Delta\phi_{M\text{-}S} : \Delta\phi_{S\text{-}O} = 1 : 2$). The simulation results for the $\Delta\phi_B = 0.4$ eV is plotted as red line, and those for the $\Delta\phi_B = 0.6$ eV is drawn in black line in Figure 4.4.

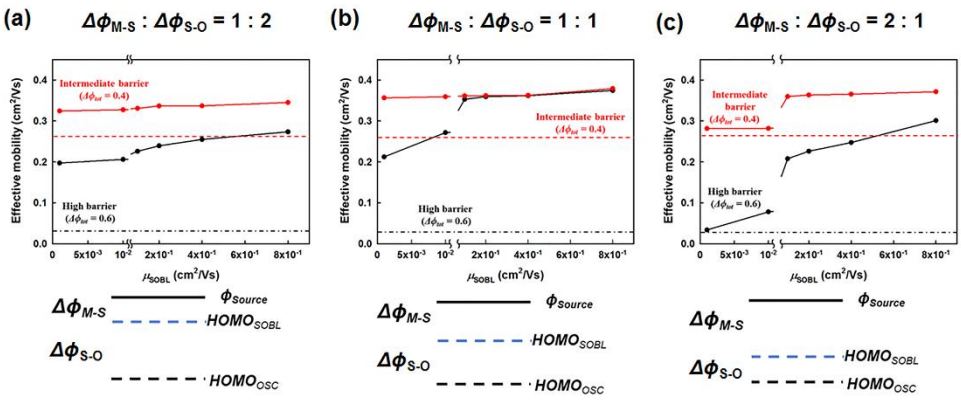

Figure 4.4. Simulation results of the effective mobility in conditions of (a) $\Delta\phi_{M\text{-}S} : \Delta\phi_{S\text{-}O} = 1 : 2$, (b) $\Delta\phi_{M\text{-}S} : \Delta\phi_{S\text{-}O} = 1 : 1$, and (c) $\Delta\phi_{M\text{-}S} : \Delta\phi_{S\text{-}O} = 2 : 1$. Black dots represent the mobility of an OFET with $\Delta\phi_B = 0.6$ eV and red black dots represent that with $\Delta\phi_B = 0.4$ eV. The black dot-dashes show the effective mobility of an OFET with $\Delta\phi_B = 0.6$ eV and the red show that with $\Delta\phi_B = 0.4$ eV without SOBL, respectively.

From Figure 4.4, the introduction of SOBL indeed greatly enhances the effective mobility of OFET in all cases. We first will discuss for the case of $\Delta\phi_B = 0.4$ eV. When $HOMO_{SOBL}$ is close to the ϕ_S ($\Delta\phi_{M\text{-}S} : \Delta\phi_{S\text{-}O} = 2 : 1$, Figure 4.4(a)), the low value of μ_{SOBL} (0.001 cm^2/Vs) has little effect on the enhancement of the mobility

(0.27 cm^2/Vs to 0.28 cm^2/Vs). However, as μ_{SOBL} is increased from the 0.001 cm^2/Vs to 0.1 cm^2/Vs, the effective mobility is also increased from 0.28 cm^2/Vs to the 0.35 cm^2/Vs, and the further increase of μ_{SOBL} as 0.8 cm^2/Vs induces the effective mobility of OFET reaches to 0.37 cm^2/Vs. When $\Delta\phi_{M\text{-}S} : \Delta\phi_{S\text{-}O} = 1 : 1$ ($HOMO_{SOBL}$ is located in the middle, Figure. 4.4(b)), even at the low value of μ_{SOBL} can greatly increase the effective mobility to 0.35 cm^2/Vs and maximum mobility reaches to 0.37 cm^2/Vs. When $\Delta\phi_{M\text{-}S} : \Delta\phi_{S\text{-}O} = 1 : 2$ ($HOMO_{SOBL}$ is close to $HOMO_{OSC}$, Figure 4.4(c)), the similar trend of the effective mobility in terms of μ_{SOBL} to the Figure 4.4(b) is observed, but the maximum effective mobility is reduced to the 0.34 cm^2/Vs. From the results, it can be concluded that the ratio of $\Delta\phi_{M\text{-}S} : \Delta\phi_{S\text{-}O}$ mainly governs the enhancement of effective mobility and when $\Delta\phi_{M\text{-}S} : \Delta\phi_{S\text{-}O} = 1 : 1$, the effective mobility was maximized even for the small value of μ_{SOBL}. That is, when $\Delta\phi_{M\text{-}S} : \Delta\phi_{S\text{-}O} = 1 : 1$, the $\Delta\phi_{M\text{-}S} = \Delta\phi_{S\text{-}O} = 0.2$ eV so the quasi-ohimic injection is occurred in two barriers. On the other hand, when $\Delta\phi_{M\text{-}S} : \Delta\phi_{S\text{-}O} = 2 : 1$ or $1 : 2$, the two barriers are divided unequally, and in larger barrier, the thermionic injection is happened so the amount of injected charges are decreased.

The effect of SOBL is more evident when $\Delta\phi_B$ is increased to 0.6 eV. Comparison of Figures of 4.4(a)-(c) reveals that when $\Delta\phi_{M\text{-}S} : \Delta\phi_{S\text{-}O} = 1 : 1$, the maximum effective mobility is increased from 0.03 cm^2/Vs to 0.37 cm^2/Vs, which is comparable to that of OFET having $\Delta\phi_B = 0.4$ eV. On the contrary, when E_{SOBL} deviates from the middle of ϕ_S and E_{HOMO}, the maximum mobility is rather decreased to 0.27 cm^2/Vs for $\Delta\phi_{M\text{-}S} : \Delta\phi_{S\text{-}O} = 2 : 1$ and 0.30 cm^2/Vs for $\Delta\phi_{M\text{-}S} : \Delta\phi_{S\text{-}O} = 1 : 2$. Again, when $\Delta\phi_{M\text{-}S} : \Delta\phi_{S\text{-}O} = 1 : 1$, the $\Delta\phi_{M\text{-}S} = \Delta\phi_{S\text{-}O} = 0.3$ eV so the thermionic injection is occurred in two barriers. On the other hand, when $\Delta\phi_{M\text{-}S} : \Delta\phi_{S\text{-}O} = 2 : 1$ or $1 : 2$, at the larger barrier, the tunneling injection is happened so the amount of injected charges are greatly decreased. Those results indicate that the dividing high injection barrier into two small barrier by introduction of SOBL is indeed beneficial

approach for improvement of injection properties. That is, in OFET without the SOBL, $\Delta\phi_B$ of typical OFET is entirely imposed to single interface (source/active layer). On the other hand, in our case with SOBL, the high barrier is divided to the two small barriers at two interfaces (source/SOBL and SOBL/active layer). Therefore, owing to the reduction of energy barrier at the each interface [84], the amount of injected the charges through the active layer is increased. In this regard, when the two barriers at the source/SOBL and at the SOBL/active layer is equal, the effective mobility of OFET is maximized because of the balanced injection barrier in both interfaces. Furthermore, when μ_{SOBL} is increased, the injected charges can be transported and accumulated along the channel, so the effective mobility is increased for the fixed energy barriers.

4.3. Experimental results and discussions

4.3.1 Fabrication of organic field-effect transistors with semiconducting organic buffer layer

A heavily p-type Si substrate was prepared as a gate electrode and a thermally grown 300 nm-thick SiO_2 layer was served as the gate insulator. The Si/SiO_2 substrate was cleaned with acetone, isopropyl alcohol, methanol, and deionized water for 10 min each under ultra-sonication in sequence. As a buffer layer of the gate insulator for the active layer, poly(4-vinylphenol) (PVP) together with methylated poly(melamine-co-formaldehyde) dissolved in propylene glycol methyl ether acetate in 2 wt.% was spin-coated on the SiO_2 layer at the rate of 3000 rpm for 30 sec. The PVP layer was subsequently annealed at 100°C for 10 min and at 200°C for 30 min in sequence. A p-type OSC, 6,13-bis(triisopopylsilylethynyl) pentacene (TIPS-PEN) together with the poly(alpha) methylstyrene dissolved in Tetralins in 1.5 wt.%, was spin-coated at 1000 rpm for 30 sec, followed by annealing at 70°C for the removal of the solvent. The SOBL layer of pentacene was thermally evaporated with thickness of 10 nm through a shadow mask at the deposition rate of 0.05 nm/s under about 10^{-6} Torr. The source and drain electrode were prepared with 50-nm-thick Au which was thermally deposited. The channel length and the channel width were defined to be 150 μm and 1.5 mm, respectively.

The electrical transfer curves and the output curves of our VOLET were measured using a source meter (4155A, Keithley) in an ambient condition.

4.3.2. Electrical characteristics

The electrical characteristics of OFET from the viewpoint of SOBL will be discussed in this section. As already mentioned in **Section. 4.2.**, the cases of $\Delta\phi_B$ = 0.4 eV (corresponding to Au source/drain electrode) and $\Delta\phi_B$ = 0.6 eV (corresponding to Ag source/drain electrode) was tested in experiment.

In Figure 4.5, the transfer curves at the bias condition of V_D = – 50 V when $\Delta\phi_B$ = 0.4 eV and $\Delta\phi_B$ = 0.6 eV are presented. The black symbols represent the transfer curve of an OFET without SOBL and the red symbols represent that of an OFET with SOBL. As clearly seen from the Figure 4.5, as predicted in **Section. 4.2.,** the effective mobility of OFETs, extracted from the transfer curve, is 0.36 cm^2/Vs for OFET with SOBL and 0.27 cm^2/Vs for OFET without SOBL. That is, the effective mobility is increased almost 33 % by introduction of SOBL.

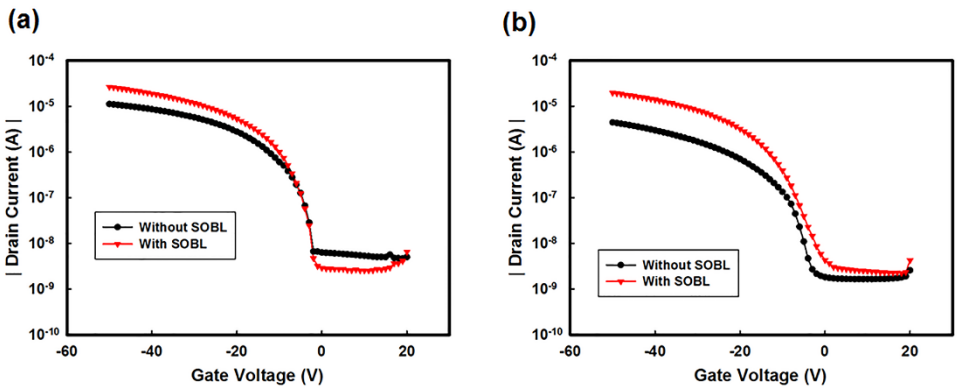

Figure 4.5. Transfer curves of the OFETs at V_D = - 50 V having (a) $\Delta\phi_B$ = 0.4 eV (Au electrode) and (b) $\Delta\phi_B$ = 0.6 eV (Ag electrode), respectively. The black circles represent the transfer curve of an OFET without SOBL and the red triangles represent that of an OFET with SOBL.

This trend is more evident in case of OFET having $\Delta\phi_B$ = 0.6 eV. In Figure 4.5(b), the transfer curves at the bias condition of V_D = - 50 V when $\Delta\phi_B$ = 0.6 eV is shown. The effective mobility of OFETs, extracted from the transfer curve, is 0.31 cm^2/Vs for OFET with SOBL and 0.05 cm^2/Vs for OFET without SOBL. When case

without SOBL, due the high injection barrier up to 0.6 eV, the tunneling injection happens at the interface, which greatly decreases the amount of injected charges. Meanwhile, for the case with SOBL, the effective mobility of OFETs having $\Delta\phi_B$ = 0.4 eV and $\Delta\phi_B$ = 0.6 eV is almost comparably same range. That is, the SOBL can actually alleviates the energy difference between the source electrode and active layer. These results strongly suggest that the introduction of SOBL has merit of increasing the window of material selection in fabrication of OFET without concerning the degradation of electrical performance.

The output characteristics of OFET with/without SOBL in the cases of $\Delta\phi_B$ = 0.4 eV and $\Delta\phi_B$ = 0.6 eV were surmerized in Figure 4.6 and Figure 4.7. As shown, the maximum current of OFETs with SOBL is increased to four-times of those without SOBL. Those results clearly verify the simulation result in **Section. 4.2** that the introduction of SOBL indeed lowers the potential loss at the contact region.

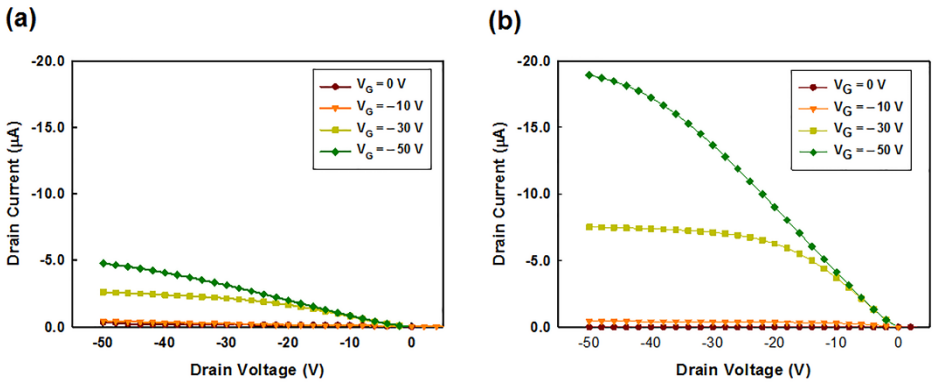

Figure 4.6. Output curves of OFETs having $\Delta\phi_B$ = 0.4 eV (a) without SOBL and (b) with SOBL at various V_G.

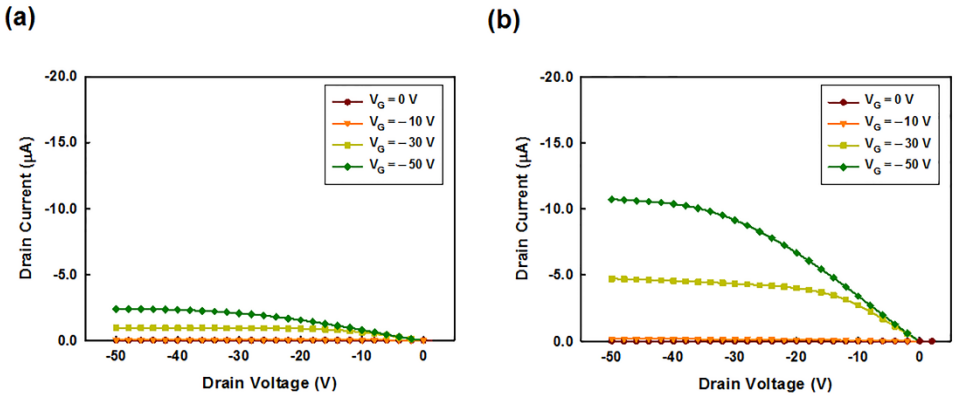

Figure 4.7. Output curves of OFETs having $\Delta\phi_B$ = 0.6 eV (a) without SOBL and (b) with SOBL at various V_G.

4.4. Conclusions

In this work, I investigated how the energy level of the semiconducting organic buffer layer (SOBL) influences the charge injection and transport of the OFET with the help of numerical simulations. For fixed energy level difference of 0.4 eV and 0.6 eV between the active layer and the source electrode, the energy level of SOBL (E_{SOBL}) was varied. As shown in simulations and experiments, the maximum mobility was obtained when E_{SOBL} was located in the middle of the injection barrier height between the source electrode and the OSC layer. The mobility improvement was attributed to the decrease of the potential difference at the interface between the source electrode and the OSC layer. Specifically, it was found that for $\Delta\phi_{M\text{-}S} : \Delta\phi_{S\text{-}O} = 1 : 1$, the potential difference at the interface was greatly decreased from - 12.2 V to - 2.5 V. As a result, the effective mobility was increased to 0.27 from 0.36 when $\Delta\phi_B = 0.4$ eV and increased to 0.05 from 0.31 when $\Delta\phi_B = 0.6$ eV. The output curves with SOBL shows linear increase while those without SOBL show poor S-shape curve. From those results, it is demonstrated that SOBL can simultaneously enhances the injection properties and the transport properties of OFETs. My work provides a scientific basis for unravelling the mechanism for the charge injection in the OFET in terms of the injection energy barrier.

Chapter 5. Vertical Organic Light-Emitting Transistors with Dielectric Encapsulated Source electrode

5.1. Introduction

Recently, the organic light-emitting transistors (OLETs) have been paid much attention owing to functional integration of the electrical switching characteristics and the light emitting capabilities in a single device architecture. [8, 9, 91] Moreover, the OLET has several advantages over an organic light emitting diode (OLED) in the external quantum efficiency and the aperture ratio for active matrix display applications. [9, 16, 92] So far, most of OLETs have been constructed in planar geometry where the source electrode and the drain electrode were laterally located. However, those planar-type OLETs have been confronted with the line- or band-type of light emission since the recombination of transported holes and electrons occurred in limited area within channel. [8, 13, 92]

Thus, vertical OLETs (VOLETs) have been suggested as one of the promising approaches toward the achievement of the quasi-surface emission characteristic by introducing the source electrode of closed topology with periodic vacancies. [93] In this regard, various types of source electrode with vacancies such as quasi-discontinuous [94] or periodically perforated metallic film, [95-98] and the network of randomly distributed carbon nanotubes (CNTs) [99, 100] or silver nanowires [101] have been investigated in a vertical architecture. In those cases, the accumulation and transport of charges at the vacancies of the source electrode should be precisely governed by the electric field from the gate electrode for the switching operation.

However, except for the few cases of CNT-based VOLETs, the short channel length in the VOLETs greatly hampers the transistor-type switching performance since the flow of charges largely passes along the direct vertical path from the source electrode to the drain electrode rather than through an interface between the organic semiconductor (OSC) and the gate insulator before the charge recombination in the active layer. Thus, the large amount of leakage current exists at off-state of VOLETs, decreasing the on/off ratio. Even though the CNT-based VOLETs have demonstrated good switching ability with low leakage current, they may suffer from the poor uniformity and the long-term stability arising from the random distribution and the poor connectivity of the CNTs used for the source electrode. [99, 101] To suppress the direct vertical charge flow, the metal-insulator-semiconductor-type VOLETs (MIS-VOLETs) with a source insulator layer on the source electrode [93, 102] (Device I, Figure 5.1(a)) or above the source electrode [103] (Device II, Figure 5.1(b)) were proposed. In particular, MIS-VOLETs with the source insulator layer above the source electrode show substantially higher on/off current ratio than those with a source insulator layer on the source electrode. [102, 103] Nonetheless, the on/off ratio of the MIS-VOLETs are still insufficient for practical switching applications because the charges injected from the side of the source electrode are considerably governed by the electric field between the drain electrode and the source electrode rather than that from the gate electrode.

In this work, I demonstrated VOLET with a high current on/off ratio by employing source electrode whose top and side parts are encapsulated by an insulator (Device III, Figure 5.1(c)). In my proposed novel device configuration, the charge injection occurs only at the bottom part of source electrode where the direction of electric fields is toward the interface between the gate insulator and the OSC. Consequently, the injected charges are transported and accumulated along the interface of gate insulator and OSC rather than the direct vertical path, enabling the

efficient control by gate voltage. In **Section 5.2.**, the concept and fabrication details of my VOLET with dielectrically encapsulated source electrode will be presented. In **Section 5.3.**, with help of numerical simulation, the effect of dielectric encapsulation of VOLET on the switching performance was investigated and compared with other previously reported structures of VOLETs with a source insulator layer [93, 102, 103]. The influence of the interface traps at the source insulator on the electrical characteristics of VOLET will be also analyzed. The opto-electrical characteristics of my encapsulated VOLET are measured and discussed in **Section 5.4**. The enhancement of switching capability by structural optimization of VOLET would lead to the increased on/off ratio of current and luminance in VOLET, which are essential features for the development of high-performance OLET-based displays.

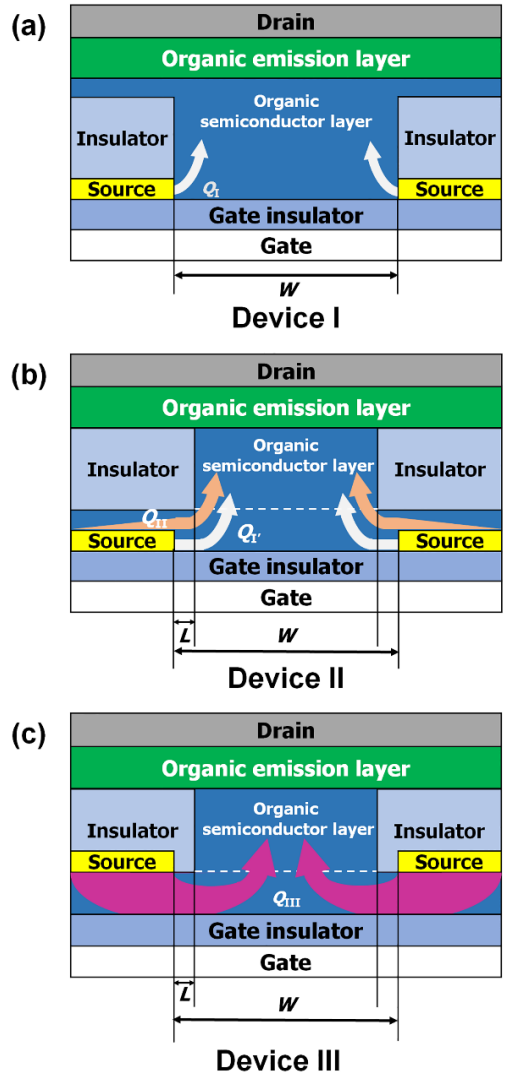

Figure 5.1. Three different configurations of the VOLET; (a) Device I with no OSC above or below the source electrode, (b) Device II with the OSC between the source insulator and the source electrode, and (c) Device III with the OSC between the source electrode and the gate insulator. Q_I, $Q_{I'}$, Q_{II}, and Q_{III} represent the flow of charges in the three VOLET structures, respectively. W denotes the width of a single aperture region between two adjacent stripes of the finger-like source electrode and L represents an extended length of dielectric encapsulation of the source insulator (Ref. [97]).

5.2. Device structure and fabrication

The three dimensional (3-D) schematic illustration of my VOLET is depicted in Figure 5.2.

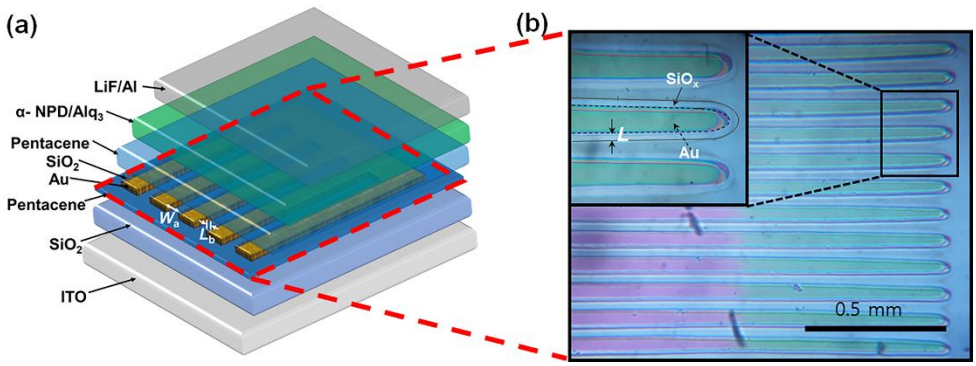

Figure 5.2. (a) 3-D schematic of a VOLET with a dielectrically encapsulated source electrode. Dielectrically encapsulated source electrode is highlighted in red dashes. (b) Microscopic image of dielectrically encapsulated source electrode with blocking length (L) of 10 μm (Ref. [97]).

For the fabrication of the VOLET, I used same materials for the all electrodes and organic layers as previous studies of Device I [93, 102] and Device II [103] to distinguish the effect of device structure on the electrical characteristics of VOLET from other factors. A glass substrate with a pre-patterned gate electrode of 70 nm-thick indium-tin-oxide (ITO) was prepared. For the gate insulator, silicon dioxide (SiO_2) of 300 nm thick was evaporated over the gate electrode by plasma-enhanced chemical vapor deposition. To improve the surface characteristics of gate insulator, poly(4-vinylphenol) (PVP) together with methylated poly(melamine-co-formaldehyde) dissolved in propylene glycol methyl ether acetate in 2 wt.% was spin-coated at the rate of 3000 rpm for 30 sec. The PVP layer was then annealed at 100°C for 10 min and at 200°C for 30 min in sequence. For restricting charge

injection only to occur in the bottom part of source electrode, the 20 nm-thick bottom OSC layer of p-type semiconductor, pentacene, was deposited by vacuum evaporation at the rate of 0.05 nm/s under about 10^{-6} Torr.

The detailed fabrication process for realization of the source electrode and encapsulating source insulator was described in Figure 5.3. For the source electrode, gold (Au) of 15 nm was deposited by vacuum evaporation through the shadow mask at the deposition rate of 0.1 nm/s under about 10^{-6} Torr, as depicted in Figure 5.3.(a). To completely encapsulate the top and side parts of source electrode, 300 nm-thick SiO_x was sequentially deposited while the substrate was rotated for the oblique deposition of SiO through the shadow mask [104] in same condition above, as depicted in Figure 5.3.(b). The microscopic image of fabricated source electrode with a source insulator layer is presented in Figure 5.2.(b), showing that the source electrode is well-covered by the source insulator. In my device, the blocking length of encapsulating source insulator (L) was measured as around 10 μm, the width of single aperture (W_a) as 25 μm, and the effective total channel width (W) as 56 mm with 16 apertures.

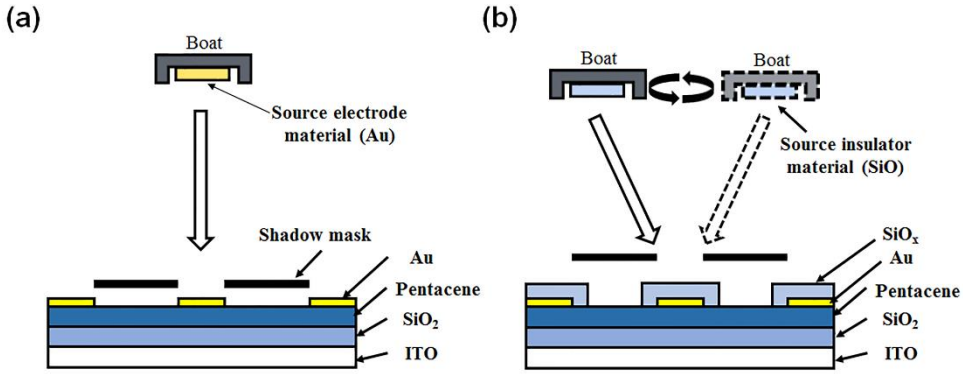

Figure 5.3. Illustration describing fabrication method for deposition of dielectrically encapsulated source electrode by oblique deposition of source insulator. (a) The process of depositing source electrode and (b) the oblique deposition of source insulator covering the top and side part of the source electrode (Ref. [97]).

After deposition of the source insulator, a 100 nm-thick OSC layer of pentacene, a 50 nm-thick hole transport layer (HTL) of N,N'-di(1-naphthyl)-N,N'-diphenylbenzidine (α-NPD), a 50 nm-thick emission layer (EML) of tri-(8-hydroxyquinoline)aluminum (Alq3), and the drain electrode of lithium fluoride/aluminum (LiF/Al, 0.5 nm/60 nm thick) were subsequently deposited by vacuum evaporation at the deposition rate of 0.05 nm/s under about 10^{-7} Torr.

The electrical characteristics of transfer curves and output curves were measured by a source meter (4155A, Keithley). The light emission characteristics of my VOLET were observed with an optical microscope (Eclipse E600, Nikon). The transfer curves of luminance in my VOLET as a function of the gate voltage were measured by a spectrometer (CS-2000, Konica Minolta).

5.3. Numerical simulations in three-type of vertical organic light-emitting transistors

5.3.1 Simulation models and device parameters

The numerical device simulation was conducted by a commercial two-dimensional (2-D) device tool (Atlas, Silvaco). The simulator predicts the electrical characteristics of a device at specified bias conditions by solving systems of Poisson's equation and continuity equation given for holes and electrons. [105]

The electrostatic potential is related to the space charge density in Poisson's equation of Equation (1)

$$\varepsilon\nabla^2\psi = -\ q(p - n + N_D - N_A) + Q_{\mathrm{T}} \quad (1)$$

where ε, ψ, and q are the dielectric constant, the electrostatic potential, and fundamental electronic charge, respectively. The p and n are the concentration of holes and electrons, N_{D} and N_{A} are the concentration of donors and acceptors, and Q_{T} is the charges induced by the presence of impurities.

Assuming that the boundary conditions at the Schottky contact are imposed at two interfaces of the source/OSC and the OSC/drain, the surface potential at the Schottky contact [106] is given by Equation (2)

$$\psi = V_{\mathrm{o}} -\ E_g/2q + \phi_{\mathrm{B}} \quad (2)$$

where V_{o} denotes the applied bias to the source electrode. E_{g} denotes the energy gap between the highest occupied molecular orbital (HOMO) and the lowest unoccupied molecular orbital (LUMO) energy level of the OSC, given by E_{HOMO} - E_{LUMO} where E_{HOMO} and E_{LUMO} are energy level of HOMO and LUMO. ϕ_{B} denotes the Schottky barrier height between the electrode and the OSC. Here, ϕ_{B} can be expressed by E_{HOMO} - ϕ_{M} or ϕ_{M} - E_{LUMO} for holes or electrons, where ϕM denotes the

work-function of electrode.

The current density for holes and electrons, J_p and J_n, can be obtained by considering their drift and diffusion components, described as Equations of (3a) and (3b)

$$J_p = qp\mu_p F + qD_p \nabla p \quad (3a)$$

$$J_n = qn\mu_n F + qD_n \nabla \mathrm{n} \quad (3b)$$

where F denotes the electric field, μ denotes the mobility of material, and D denotes the diffusion coefficient. The electric field (F) is extracted from the gradient of the potential ($F = -\nabla\psi$). The subscript of p is used in the values for holes and that of n is used in the values for electrons.

Here, I applied electric field-dependent Poole-Frenkel model to determine the effective mobility of organic materials, given by $\mu = \mu_0 \exp(\gamma\sqrt{F})$, where μ_0 represents the zero-field mobility of organic materials and γ represents the characteristic parameter for the field-dependence.

The charges induced by the interface defects between the source insulator and OSC, Q_T in Equation (1), were also investigated in simulation. Particularly, in my VOLET with encapsulating source insulator, the acceptor-like interface traps at the surface of source insulator can greatly influence the switching performance of transistors. [107, 108] Therefore, the exponential distribution of interface trap states, g(E), was assumed at interface between the source insulator and OSC. The states of interface traps based on the characteristic temperature and the density with exponential distribution are given by Equation (4)

$$\mathrm{g}(E) = N_\mathrm{T}/kT_\mathrm{int} \times \exp[(E - E_\mathrm{C})/kT_\mathrm{int}] \quad (4)$$

where E refers to the energy level, EC refers to the energy level of conduction band, k refers to the Boltzmann's constant, N_T and T_{int} refer to the density of interface trap states and the characteristic temperature of interface traps, respectively. Then, the value of Q_T in Equation (1) can be calculated as $Q_\mathrm{T} = q\int_{E_\mathrm{v}}^{E_\mathrm{c}} \mathrm{g}(E) f(E) dE$

where $f(E)$ is probability of occupation from the Fermi-Dirac statistics. The $f(E)$ is expressed in equation of $f(E) = 1/(1 + \exp[(E - E_F)/kT])$ where E_F is the Fermi-level energy.

The 2-D cross-sectional schematics of VOLETs used in simulations are illustrated in Table 5.1 and 5.2 To distinguish the effect of device structure on the electrical characteristics of VOLET by comparison with other configurations, I used same organic materials for OSC of pentacene, HTL of α-NPD, and EML of Alq_3 as previous studies of Device I [93, 102] and Device II [103]. For the electrodes, the source electrode of Au, the drain electrode of LiF/Al and the gate electrode of ITO were selected for the efficient injection between the electrodes and organic layers. The layers of gate insulator and source insulator were considered as perfect insulator without leakage current in simulation. The materials and geometric parameters were fixed and applied in all the simulations of VOLET throughout this study. The material parameters are taken from the literatures [105, 107-113] and detailed material parameters used in the simulation are summarized in Table 5.1 and 5.2. The E_{HOMO} of pentacene was adjusted to 5.25 eV, taking account of the energy alignment between the pentacene and Au by formation of interfacial dipoles [114]. The density of states in the valance band and those in the conduction band are taken as $2 \times 10^{21}/cm^3$ for all organic layers in this work. [105] The characteristic parameter for the field-dependence of γ is assumed to be 1×10^{-3} $(cm/V)^{1/2}$. The value of L_b was assumed as 10 μm, W_a as 25 μm, and the total channel width of W as 56 mm, same as fabricated VOLETs (described in **Section 5.2.**).

Table 5.1. The electrical parameters of materials for organic layers used in simulation.

Layer	Material	E_{LUMO}[a] (eV)	E_{HOMO}[b] (eV)	Dielectric constant	μ_{p0}[c] (cm^2/Vs)	μ_{n0}[d] (cm^2/Vs)	Thickness (nm)
OSC	Pentacene[19]	3.2	5.25	4	0.2	5×10^{-5}	20/100[e]
HTL	α-NPD[24]	2.4	5.4	3	3×10^{-4}	1×10^{-9}	50
EML	Alq_3[25, 26]	3.1	5.8	3	1×10^{-9}	3×10^{-4}	50

[a] E_{LUMO} is the energy level of the lowest unoccupied molecular orbital.

[b] E_{HOMO} is the energy level of the highest occupied molecular orbital.

[c] μ_{p0} is the zero-field mobility for holes.

[d] μ_{n0} is the zero-field mobility for electrons.

[e] An additional layer of 20 nm-thick OSC was placed below the source electrode for Device II and Device III.

Table 5.2. The electrical parameters of materials for the electrodes and insulators used in simulation.

Layer	Material	Work-function (eV)	Dielectric constant	Thickness (nm)
Source electrode	Au	4.9	-	15
Drain electrode	LiF/Al	3.2	-	0.5/100
Gate electrode	ITO	4.7	-	75
Source insulator	SiO_x	-	3.9	300
Gate insulator	SiO_2	-	3.9	300

5.3.2 Current density distributions

The mechanism of charge flow in VOLET plays an important role on determining switching performance. For example, the Device I exhibits insufficient on/off ratio in order of 10^1 in previous studies, which was originated from its structure [93]. In other words, in Device I (Figure 5.1(a)), the charges are injected at the side of source electrode, and then transported in direct passage between the drain electrode and the source electrode (Q_I) rather than through the interface of the gate insulator and OSC because of the stronger electric field between the source electrode and the drain electrode than the electric field induced by the gate electrode. As for Device II (Figure 5.1(b)), the source insulator was laterally extended so as to the increase horizontal charge pathway OSC for the flow of charges injected from the source electrode ($Q_{I'}$) along the interface between the gate insulator and OSC. Compared to the flow of Q_I in Device I, the longer horizontal charge pathway of $Q_{I'}$ along the interface substantially increases the controllability over injected charges by the gate voltage (V_G). However, since the top part of source electrode is interfaced with OSC, the flow of charges injected from the top part of the source electrode toward the drain electrode (Q_{II}) happens and acts as a leakage current. As depicted in Figure 5.1.(b), the flow of Q_{II} does not pass through the interface between gate insulator and OSC, hence the overall switching capability of Device II is diminished. On the other hand, in case of the Device III (Figure 5.1(c)), the encapsulating source insulator induces the charge injection to be occurred in the bottom of source electrode while blocking the injection at the top and side parts of source electrode. Then, the flow of injected charges is transported and accumulated at the interface of the gate insulator and OSC. The accumulated charges can be moved horizontally along the interface (Q_{III}) before the recombination process. The degree of accumulation and lateral extension of charges at the interface can be controlled by

applying V_G, giving the effective transistor-type switching ability to Device III. In this respect, I investigated how the architecture of VOLET affects the current flow and the switching operation of VOLETs by numerical simulation focusing on the Device II and III in ideal condition without interface traps. The VOLETs presented in the Refs. 93, 102, 103 exhibit light emission under the bias condition of drain voltage (V_D) of – 10 V, so my simulation was also conducted under the same bias condition of V_D = – 10 V.

The simulation results for the profiles of the current density distributions in Device II and III are shown in Figure 5.4. and Figure 5.5, respectively. The profiles are obtained when both devices are turned-on at the V_G of – 50 V and turned-off at V_G of + 50 V at the fixed V_D of – 10 V under zero source voltage. The current density distributions in the off-state (V_G = – 50 V, V_D = – 10 V) of Device II and Device III are shown in Figures of 5.4(b) and 5.5(b), and those in the on-state (V_G = + 50 V, V_D = – 10 V) of Device II and Device III are shown in Figures of 5.4(b) and 5.5(b), respectively.

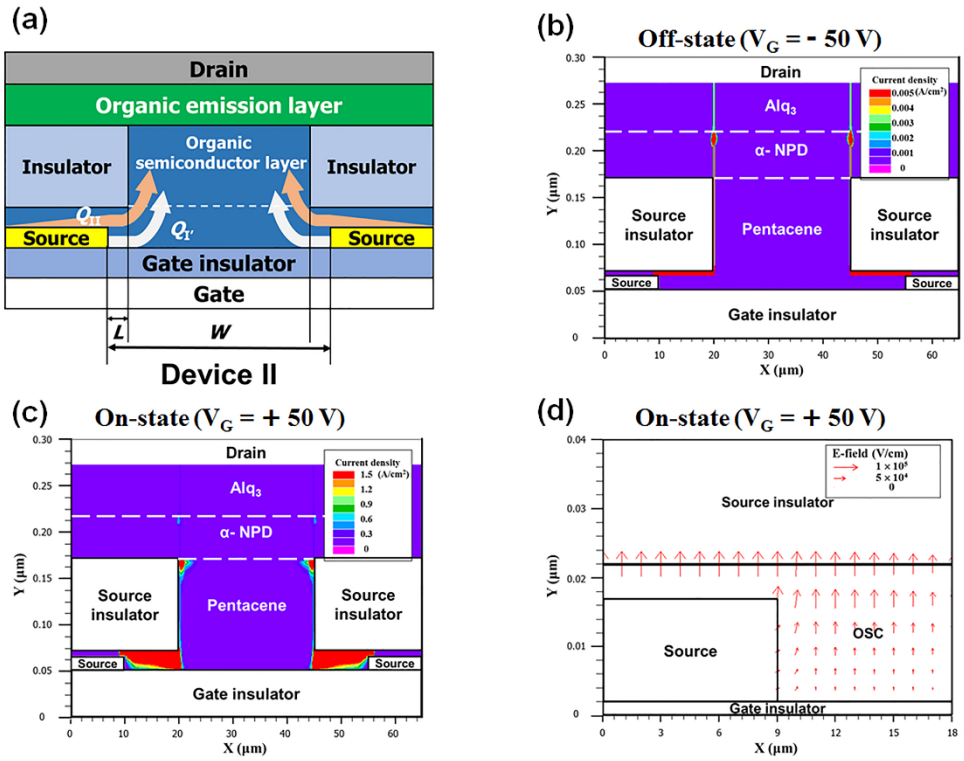

Figure 5.4. (a) The schematic and charge flow of Device II. The current density distributions of Device II (b) in the off-state ($V_G = -50$ V, $V_D = -10$ V) and (c) in the on-state ($V_G = -50$ V, $V_D = -10$ V). (d) Electric field lines in the OSC layer near the source electrode of Device II and in the on-state. In a color code from blue to red, the low density is shown in blue and the high density in red except for zero density (in purple) (Ref. [97].

Interestingly, the significant reduction of off-current in the Device III was observed. Comparison of the current densities in the off-state between Device II and Device III, shown in Figures of 5.4(b) and 5.5(b), reveals that the off-current density of the Device III was reduced to one-thousandth of that of the Device II. As described above, in case of the Device II, the controllability over the charges in the flow of Q_{II} by the gate voltage is not enough to suppress the off-current, disrupting the complete turn-off operation. On the contrary, in case of the Device III, the flow of Q_{III} can be effectively blocked by the positive V_G with the help of the enhanced gate-controllability of Device III. Besides, the positive V_G can suppress the accumulation

of charges at the interface between gate insulator and organic semiconductor, leading to the further decrease of off-state current density.

In addition to the increased on-current, as shown in Figures of 5.4(c) and 5.5(c), the current density of Device III in the on-state is higher than that of Device II in the on-state. The increased current density in the on-state could be attributed to the direction of electric fields in bottom OSC layer near the source electrode, which mainly determines the flow of injected charges. The electric fields of Device II in OSC layer near the source electrode in the on-state are shown in Figure 5.4(d) and those of Device III are shown in Figure 5.5(d). For the Device II, the direction of electric fields in bottom OSC layer near the top and side parts of source electrode are toward the drain electrode so most of the injected charges are transported in upper part of bottom OSC layer rather than accumulated at the interface of the gate insulator. On the contrary, for the Device III, the direction of electric field in bottom OSC layer near the bottom part of source electrode is toward the gate electrode so more charges can be accumulated at the interface of gate insulator. The more accumulated charges at the interface give rise to the higher on-current in Device III. Furthermore, the accumulated charges at the interface are expanded in horizontal direction by the negative V_G so that the wide light emission zone in aperture region can be provided.

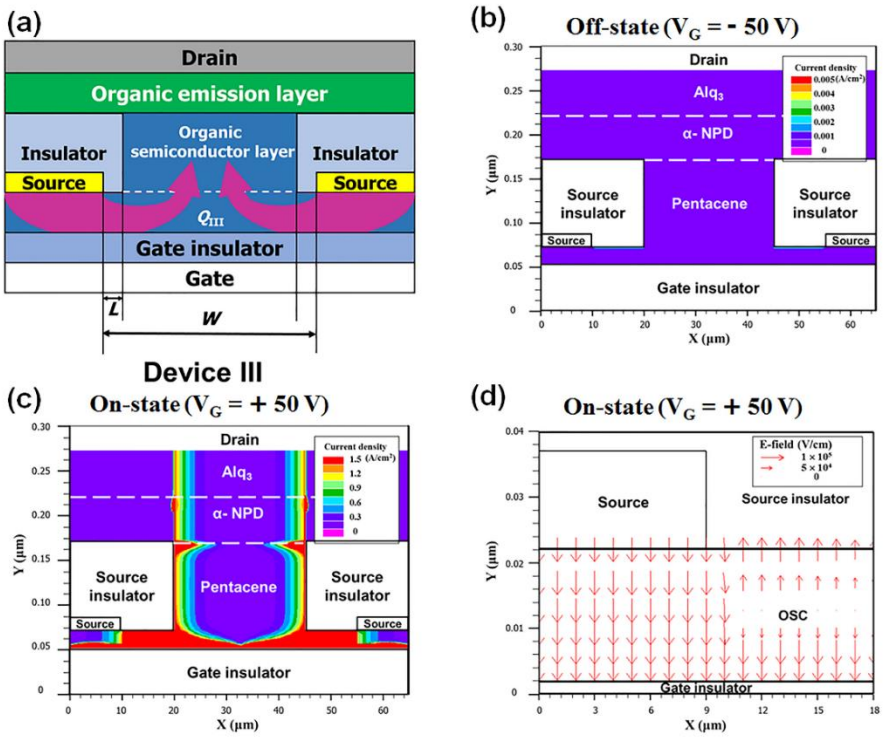

Figure 5.5. (a) The schematic and charge flow of Device III. The current density distributions of Device III (b) in the off-state and (c) in the on-state. (d) Electric field lines in the OSC layer near the source electrode of Device III and in the on-state. In a color code from blue to red, the low density is shown in blue and the high density in red except for zero density (in purple) (Ref. [97]).

The numerical simulation successfully demonstrated that the dielectric encapsulation of source electrode in VOLET can be useful approach for reinforcing the switching performance.

5.3.3 Electrical characteristics

The numerically simulated transfer curves of Device I, Device II, and Device III were summarized in Figure 5.6(a) (the case without interface traps) and Figure 5.6(b) (the case with interface traps between the source insulator layer and OSC layer). The interfacial defects of traps and fixed charges at the interface between the source insulator of SiO_x and OSC layer of pentacene were considered, which may arise from the moisture, oxygen and/or mobile charges in the insulator layer. [107, 108] The interface defects should be taken into account, because they interrupt the shift of Fermi level by the gate voltage and result in the poor subthreshold slope and decreased I_D. The simulated values of interface traps are taken as N_T of $6 \times 10^{12}/cm^2$ with T_{int} of 1900°C and the fixed interface charges of $-2.5 \times 10^{11}/cm^2$, which are comparable values with previous studies. [105, 107, 108]

At first, I simulated the transfer characteristics as a function of VG for the each type of VOLET (Device I, II and III) in condition without interface defects. The transfer curves obtained by simulation were plotted in Figure 5.6.(a). The on/off current ratio of Device I is around 10^1, that of Device II is around 10^2, and that of Device III is around 10^7. The calculated maximum on-current of Device III (2.6 mA) is about five-times larger than that of Device II (0.5 mA) and about 70-times larger than that of Device I (36 μA) in the on-state. Those results indicate that the encapsulating source insulator indeed reinforces the injection and accumulation of charges in the on-state of VOLET in given materials as discussed in **Section 5.3.2.** Note that the hump-effect is observed at V_G in range of 0 V to – 20 V, which may originated from enhanced electric field from the sharp edge of source electrode. [115] When the interface traps to the source insulator was inserted in simulation, the subthreshold slope and I_D is diminished in Fig. 5.6(b). The comparison of Figure 5.6(a) and Figure 5.6(b) in terms of interface traps reveals that those at the source

insulator plays important role on sub-threshold region, so interfacial traps should be reduced by surface treatment such as self-assembled monolayer. [116] Nevertheless, the numerically extracted on/off current ratio of Device III is still more than 100-times higher than that of Device II even after interface traps were considered. From the simulation results, it can be concluded that my approach of dielectric encapsulation of source electrode greatly improves the switching performance of VOLET.

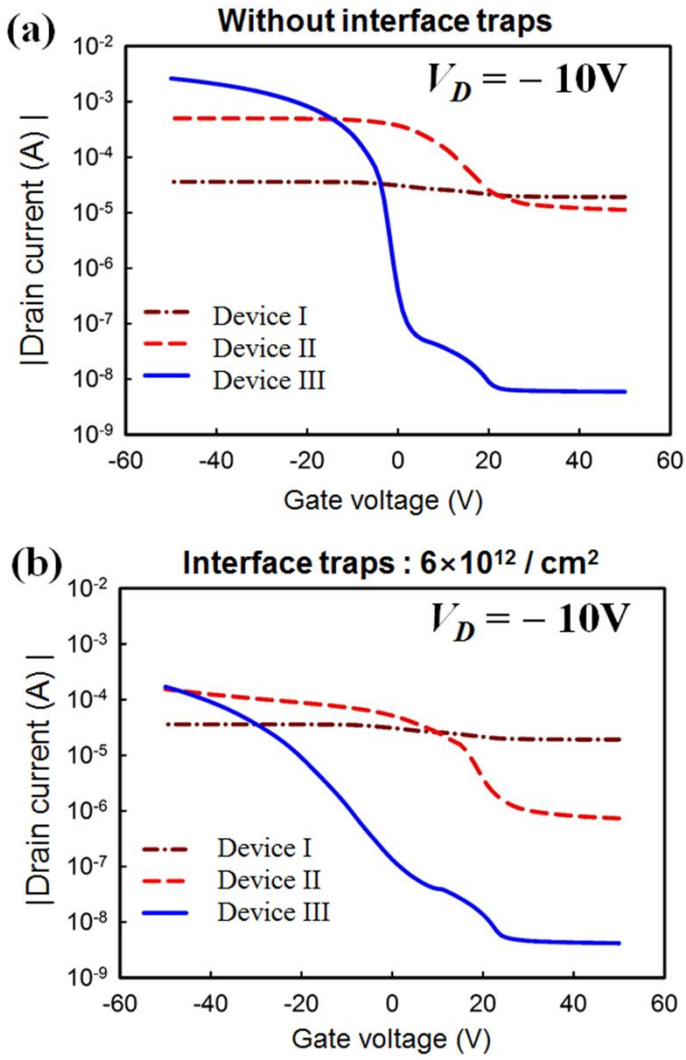

Figure 5.6. The simulated transfer curves of different VOLETs as a function of V_G at V_D = – 10 V; (a) one with no interface trap and (b) the other with interface trap density of 6 × 10^{12}/cm^2. The results for Device I, II and III are shown in a brown dash-dot line, a red dash line, and blue solid line, respectively (Ref. [97]).

5.3.4 Opto-electrical characteristics

The opto-electrical characteristics of Device II and Device III were compared. In specific, I carried out the simulations on the processes of the exciton formation and the exciton recombination rate in Device II and Device III. The simulation parameters used were in Table 5.3. The spatial distribution of the exciton density in on-state of Device II and Device III were shown in Figure 5.7. It is clear that the exciton density of Device III is much higher thn that of Device II. Moreover, the exciton density is more laterally extended in Device III than Device II. As already shown in distribution of current density (Figure. 5.4 and Figure 5.5), the enhanced gate-controllability over accumulated charges at the channel region indeed leads to the increase of effective light emission zone.

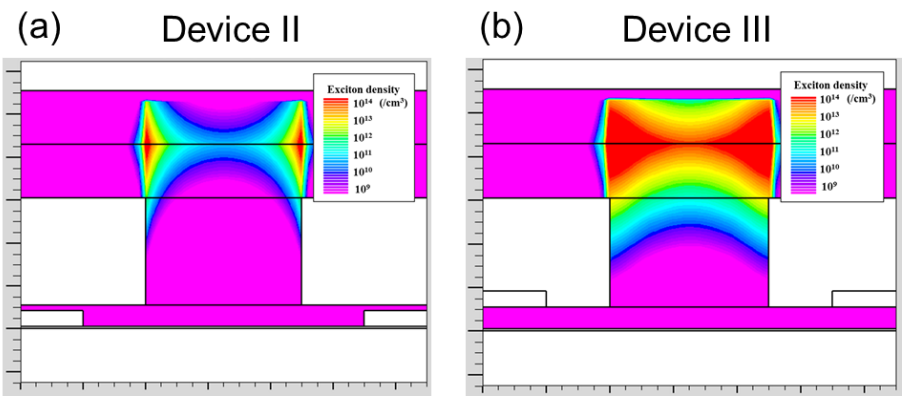

Figure 5.7. Spatial distribution of the exciton density in the on-state of Device II and that of Device III obtained in numerical simulations.

The spatial distribution of the recombination rate in the on-state of Device II and that of Device III obtained in numerical simulations was described in Figure 5.8. It is evident that recombination rate is also higher and the width of recombination region is wider in Device III than those in Device II. Combined opto-electrical characteristics with Figure 5.7 and Figure 5.8 directly imply that the emission zone in Device III would be much wider than that in Device II. In addition, as the exciton

density and recombination rate is higher in Device III, so the higher luminance is expected in Device III under the same geometrical conditions.

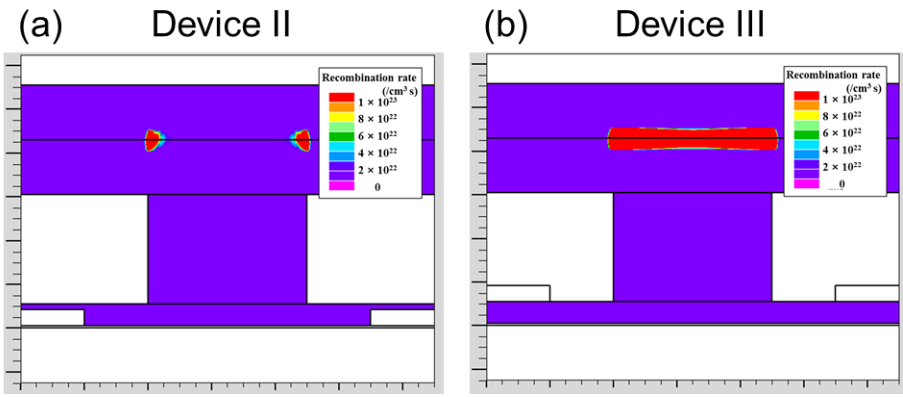

Figure 5.8. Spatial distribution of the recombination rate in the on-state of Device II and that of Device III obtained in numerical simulations.

Table 5.3. The opto-electrical parameters of material for emission layer used in simulation.

Simulation parameter	**Value**
fraction of singlets formed during Langevin recombination	0.25
radiative decay lifetime	10^{-9} s
exciton diffusion length	0.01 μm
singlet-singlet constant	2×10^{-10} cm^3/s
intersystem crossing constant	10^{-7} /s
non-radiative decay constant	2×10^{-9} cm^3/s
host photoluminescence quantum efficiency	1

5.4. Experimental results and discussions

5.4.1 Electrical characteristics

In Figure 5.9, experimental data of Device III are presented. The transfer curves as a function of V_G at different V_D are plotted in Figure 5.9(a) and the output curves as a function of V_D at various V_G are plotted in Figure 5.9(b). The Figure 5.9(a) shows the typical transistor-type operation of VOLET. My VOLET starts to function as the electrical switching device at V_D of – 2.5 V with the on/off ratio of 10^3 and on-current of 466 nA. As V_D is varied from – 5.0 V to – 10.0 V, the magnitude of on-current also increases from – 22.9 μA to – 102.7 μA. The on/off current ratio of my VOLET at V_D = – 10 V is around 5×10^3, sufficient for switching performance. The reported current on/off ratio of Device II was in order of 10^2 when the L_b of Device II is around 10 μm in Ref. 103 under the same condition of my experiment. Therefore, my VOLET has advantage of wide aperture ratio with sufficiently high on/off current ratio in given materials and geometric parameters. The maximum on/off ratio of Device II reached to around 5×10^3 when lateral length of L_b becomes around 40 μm in Ref. 103. However, it should be noted that the increase of L_b would reduce the aperture ratio of VOLET so the length of L_b should be decreased for display application.

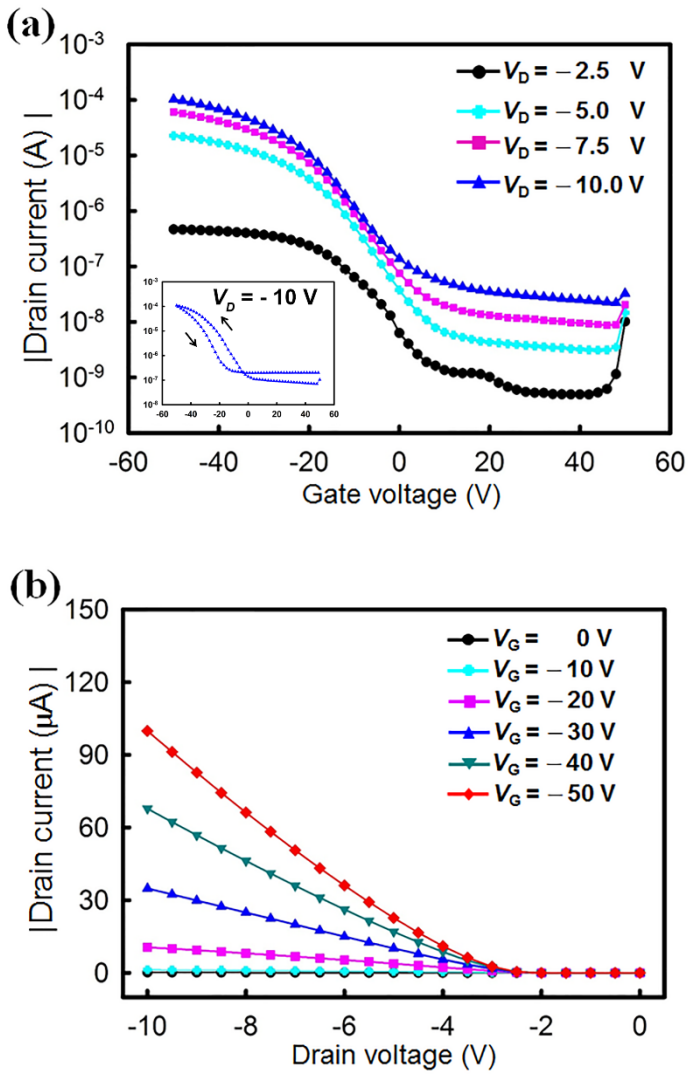

Figure 5.9. Experimental results for the electrical characteristics of my VOLET. (a) The transfer curves as a function of V_G at different values of V_D. (Inset: Hysteresis curve at V_D = – 10 V. V_G was swept from + 50 V to – 50 V and then – 50 V to + 50 V.) (b) The output curves as a function of V_D at different values of V_G (Ref. [97]).

Compared with simulated transfer curves of Figure 5.6 (**Section 5.3.3.**), the experimental transfer curves are well agree with the simulated curves in the on-state. The mismatch between the experimental data and simulated data in the off-state could be attributed to the leakage current in source insulator layer. That is, the source insulator was assumed as a perfect insulator in simulation but it actually conducts

small amount of leakage current owing to the poor crystallinity and uniformity of thermally evaporated SiO_x, and therefore the measured off-current is slightly larger than simulated off-current. However, if better insulating material is adopted for the source insulator, the leakage current can be easily reduced. Note that the on-current can be further increased by reducing the interface defects and the off-current can be further decreased by using better insulating materials for source insulator. In Fig. 5.9(b), the output curves with typical dependency of I_D on V_D are plotted. Particularly, as V_G varied in negative direction from 0 V to – 50 V at fixed V_D of – 10 V, I_D is also increased from – 49.4 nA to – 99.9 μA. As described before, V_G controls the injection and the accumulation of the charges, thereby modulation of I_D can be accomplished.

5.4.2 Light emission properties

The microscopic images of the light emission at different V_G of 0 V, – 20 V, and – 50 V at fixed V_D of – 10 V were shown in Figure 5.10. A little amount of light emission near the right-side edge of the source electrode is observed even at V_G of 0 V in Figure 5.10(a). It implies that the imperfect encapsulation of source electrode at the right-side of edge, which results in the presence of charge injection by the electric field between the drain electrode and the source electrode. That means the potential barrier between the OSC layer of pentacene and the source electrode of Au (about 0.4 eV) is not high enough to perfectly suppress the charge injection. [93, 114] By applying more negative V_G, more charges can be injected, accumulated, and recombined to emit the light. When V_G is – 20 V, I_D reaches to around 10 μA and the light begins to be emitted in Figure 5.10(b). At the high negative bias of V_G = – 50 V, the width of emission area as well as the intensity of emitted light are increased, and the light emission is occurred in full aperture region as shown in Figure 5.10(c). The transfer curve of luminance at V_D of – 10 V is plotted in Figure 5.10(d). When VOLET is turned-off by positive V_G of + 50 V, negligibly small luminance of 0.003 cd/m^2 (minimum observation limit of my measurement machine) is measured. At V_G = – 20 V, luminance exceeds 1 cd/m^2 and emitted light begins to fill the aperture region. At V_G = – 50 V, maximum luminance reaches to 29.4 cd/m^2 with light emission over the full aperture region. As shown in the inset of Figure 5.10(d), my VOLET emits light over the whole device area of 2.0 mm × 2.5 mm (highlighted in red dashed-lines). It should be noted that the better emission characteristics can be achieved by the use of doped emission layer [113, 117] or the reduction of the interface defects with proper interface treatment [116]. It should be emphasized that my fabricated VOLET has good luminance contrast ratio of more than 5×10^3.

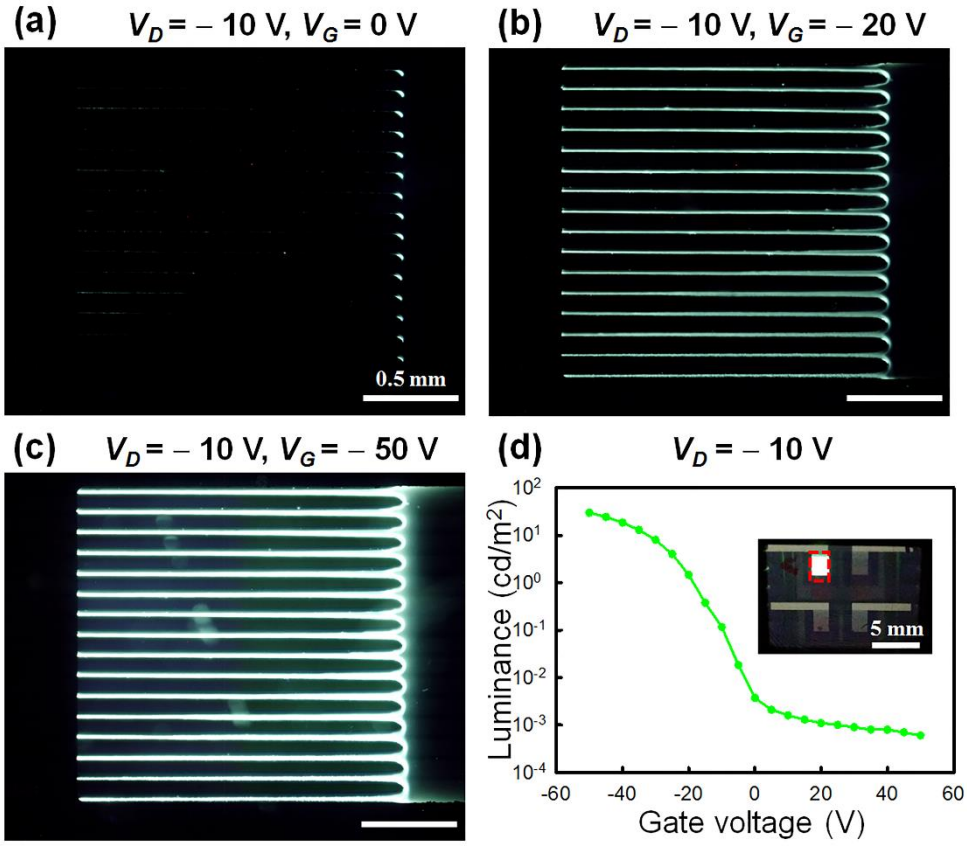

Figure 5.10. Light emission properties of our VOLET. The microscopic images showing the light emission in area of 2.0 mm × 2.5 mm under the bias conditions of (a) V_G = 0 V, (b) V_G = – 20 V, and (c) V_G = – 50 V at fixed V_D = – 10 V. (d) The luminance transfer curve as a function of V_G at V_D = – 10 V. (Inset: the microscopic image showing the light emission covering the whole device area (indicated by a red dash rectangle) at V_G = – 50 V). (Ref. [97]).

5.5. Conclusions

In this **Chapter 5**, VOLET with a high current on/off ratio was demonstrated by dielectric encapsulation of source electrode. In my VOLET configuration where the electric fields near the source electrode flow in direction toward the gate insulator, the injected charges are accumulated along the interface between OSC/gate-insulator so they can be effectively controlled by gate voltage. In addition, the dielectric encapsulation blocks the injection from the side part of source electrode, so the off-current is greatly reduced. From numerical simulation, the concept of dielectric encapsulation enhances switching performance in vertical configuration by comparison of the profiles of current density of previous studies. Due to the increased controllability over injected charges and the decreased off-current, the simulated on/off current ratio of my VOLET is about 100 times higher than that of previously reported VOLETs for given materials. The effect of interface traps at the source-insulator/OSC on switching performance was studied in simulation, which would give the insight into the optimization of sub-threshold slope in VOLET with a source insulator. The experimental results were well agreed with the simulations, showing the on/off current ratio and the luminance contrast ratio of 5×10^3. The dielectric encapsulated VOLET presented in my work would give viable platform for developing a high-performance OLET displays.

Chapter 6. Concluding Remarks

In this thesis, the enhancement of charge injection and transport in OFETs and OLETs with multi-layers have been demonstrated in terms of physical mechanism for the development of advanced OFETs and OLETs in the practical applications. The extensive, scientific investigations of electrical performances in OFETs and OLETs with the multi-layer OSCs have been conducted via numerical simulations. Particularly, the structural modification of device can be easily performed by simulation without tedious and difficult experiments. From the basis of simulation results, the multi-layer engineering of OFETs and OLETs can be fabricated, showing the improved the charge injection and transport characteristics; (i) the ambipolar-type OFETs with dual gate, two stacked OSCs, (ii) the enhanced injection properties of OFETs by the introduction of semiconducting buffer layer, and (iii) the achievement of high on/off current ratio in vertical OLETs through the dielectric encapsulation of source electrode.

In **Chapter 1**, the brief introduction and review of recent emergence of organic electronics were described. In **Chapter 2**, the theoretical backgrounds for the OFETs and OLETs were discussed, especially focused on the those with multi-layer OSCs.

In **Chapter 3**, the novel OFET architecture having dual gate with two-stacked OSCs interfacing with source/drain electrode was demonstrated. The separation of each channel for holes and electrons, together with the dual gate corresponding to each channel, leads to the highly effective control over each charges. Therefore, the operation of one carrier channel while the suppression of the opposite carrier channel can be accomplished by biasing counter-gate electrode. Moreover, the formation of two stacked OSCs via solution-process was realized by using the orthogonal solvent for two OSCs. The further optimization of materials used for OSCs, device geometry,

and bias condition should be demonstrated for balanced electric characteristics of p-type and n-type operations. Our new architecture of ambipolar-type OFET devices allows the low-cost, easy fabrication of integrated circuits with single ambipolar-type OFETs.

In **Chapter 4**, I investigated the effect of using organic semiconductor as a buffer layer in terms of injection properties of OFETs. Numerical simulation reveals that SOBL have indeed increased effective mobility of OFETs by reducing the potential loss at the interface of OSC/source electrode, resulting in the improved injection characteristics of OFET with SOBL. In specific, the simulation results found that the high mobility of SOBL can tailoring injection mechanism of OFETs. The high mobility of SOBL as well as reduced injection barrier height between electrode/OSC greatly attribute to the decrease of potential loss, which leads to smaller contact resistance and higher mobility of OFETs. The experimental results were also coincident with numerical simulations. The introduction of SOBL having high-mobility in OFETs would further widen the selection window of materials.

In **Chapter 5**, the vertical OLETs with high current on/off ratio were demonstrated by the dielectric encapsulation of source electrode. I demonstrated the enhancement of the gate-voltage controllability in the VOLET by the encapsulation of both the top and the side of the source electrode with an insulator. In my proposed vertical OLET configuration where the charges are injected only from the bottom of source electrode into the organic semiconductor layer, the injected charges are mainly transported along the interface with the gate insulator before the charge recombination in the active layer. Numerical simulations and experimental results show that the on/off current ratio of my VOLET is about 100 times higher than that of a conventional VOLET. Further enhancement of my VOLET will be accomplished by following approaches: (i) The reduction of interfacial traps at the source insulator will increase on/off ratio up to 10^6 and improve subthreshold swing

curve. (ii) The decrease of encapsulating length will lead to higher aperture ratio. (iii) Use of better emission layer, the opto-electrical characteristics of VOLETs will be further improved to those of OLEDs. Still, my dielectric encapsulation approach will play an essential role in developing a new class of high-performance OLET displays.

The various new device structures proposed in this thesis would pave a way toward realization of advanced organic-based electronic devices. The detailed numerical investigations conducted in this thesis would provide essential physical mechanism on the charge flow of OFETs and OLETs with multi-layers. The electrical performances of fabricated devices are well agree with simulation predictions. As a consequent, the OFETs and OLETs with multi-layers having superior electrical characteristics will be applied in the various fields from integrated circuits to the active matrix display systems.

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국문 초록

오늘날 유기 전자 공학은 차세대 전자 소자에 적용 가능하다는 큰 잠재력을 보유하고 있어 크게 주목받고 있다. 유기물의 본연의 성질인 유연성, 가벼움과 더불어 저가격에서 대면적 공정이 가능하기에 유기 물질들은 실리콘 기반 물질들에 비해 우수한 물질적 특성을 보유하고 있다. 또한, 화학적으로 유기물의 특성을 조절할 수 있기에, 유기물 반도체는 전하 수송을 통한 전통적인 전자 소자에 제한되지 않고, 발광 소자, 태양 전지, 그리고 다양한 화학/바이오 센서등 여러 분야에 넓게 응용이 가능하다. 위와 같은 다양한 장점을 갖고 있는 유기 전자 재료는 급격한 분자적 조립 기술에 의한 새로운 재료 개발에 힘입어 전기적 성능이 크게 증가하고 있다. 또한 유기 재료 물성에 대한 과학적 분석을 통해 유기물을 다양한 분야에 적용하려는 시도가 활발히 이루어지고 있다. 다양한 유기 전자 소자 중에서는, 광전자 소자 분야의 대표적인 소자인 유기 발광 다이오드와 유기 전계 효과 트랜지스터, 그리고 유기 태양전지의 발전이 돋보인다. 그 중에서도 유기 전계 효과 트랜지스터는 유연 소자, 집적 회로, 유기물 기반 센서 및 무선인식 (radio frequency identification tag, RFID) 소자에 다양하게 활용이 가능하기에 유기 광전자 소자의 응용에 핵심 요소로 자리잡고 있다.

최근 활발히 진행되고 있는 유기 반도체 물질의 물성에 대한 재료적 연구에 힘입어 유기 반도체의 전하 이동도가 10 cm^2/Vs 이상을 보이고 있으며, 이는 현재 디스플레이 회로에 사용되는 비결정질 실리콘 기반 소자의 전기적 성능에 필적하거나 넘어서는 수준이다. 하지만, 유기

반도체 물질이 갖고 있는 본연의 특성을 소자 적용 및 구동시에도 최대로 활용하도록 구성하는 것이 중요하며, 이를 위해서 소자 수준에서의 전하 주입 및 거동 능력의 향상에 대한 연구가 필수적이다. 소자 수준의 전하 주입 및 거동 능력을 향상시키기 위해, 다층 물질을 적층한 유기 전계 효과 트랜지스터 구조가 적용되어 왔다. 다층의 유기물을 적층한 연구로는, 1) 소스/드레인 전극과 유기 반도체 물질 사이에 중간층을 삽입하여 전하 주입 능력을 향상시킨 연구 2) 양극성 반도체 물질을 사용하여 전자와 정공을 단일 소자에서 동시에 수송하도록 하는 연구 3) 유기 트랜지스터와 유기 발광 다이오드를 한 소자에 집적하여 트랜지스터의 스위칭 능력과 발광 다이오드의 발광 능력을 한 소자에서 발현할 수 있는 유기 발광 트랜지스터 등이 있다.

본 논문은 다층의 물질이 적층된 유기 전계 효과 트랜지스터 및 유기 발광 트랜지스터의 전하 주입 및 거동 능력을 향상한 연구들을 제시한다. 이를 위해 유기 전계 효과 트랜지스터에서 전하 주입과 전하 거동 능력을 개선한 연구를 각각 제시하며, 이 결과를 유기 발광 트랜지스터에 적용하여 높은 점멸비를 가지면서 소자의 전 영역에서 발광하도록 한다.

우선, 이중 게이트 구조에서 두 유기 반도체를 적층한 구조를 갖는 양극성 유기 전계 효과 트랜지스터를 제안한다. 두 유기 반도체 모두 소스/드레인 전극과 직접적으로 접촉시켜 적층한 구조를 통해, 전자와 정공에 대한 독립적인 두개의 채널을 형성할 수 있다. 또한 이렇게 형성된 두개의 독립적 채널은, 서로 다른 게이트 전극에 의해 효율적으로 제어가 가능하다. 이를 통해, 양극성 소자를 단일 소자에

집적할 수 있을 뿐만 아니라, 전자와 정공에 대한 수송 능력의 균형을 전기적으로 달성할 수 있다.

두번째로는 유기 반도체 물질 기반 중간층을 소스/드레인 전극과 활성층 (active layer) 사이에 도입하여 전하의 수송 능력을 향상시킨 연구를 구현한다. 유기 반도체 물질 기반 중간층은 소스 전극과 활성층 사이에서 손실되는 전압의 크기를 줄이고, 이를 통해 소자의 유효 전하 이동도를 대폭 상승시킬 수 있다. 이 연구에서는 수치 해석 시뮬레이션 프로그램을 통해, 전하 주입 능력에 대한 심층적인 해석을 가능하게 할 뿐만 아니라 다양한 전극에서의 실제 소자 구현을 통해 시뮬레이션 결과를 검증하였다.

마지막으로 수직 구조의 유기 발광 트랜지스터에서 소스 전극을 절연막으로 완전히 덮어 전하의 이동경로를 조절하고, 이를 통해 높은 점멸비를 달성한 연구를 제시한다. 소스 전극의 상단부 뿐만 아니라 측면부를 완전히 덮어, 드레인 전극에서 과대하게 인가되는 전기장의 세기를 줄일 뿐만 아니라 소스 전극 하단부에서 주입된 전하가 게이트 절연막과 유기 반도체 층의 계면에 축적되도록 한다. 축적된 전하는 게이트 전압에 의해 효율적으로 제어되며 수평적으로 확장될 수 있어, 게이트 전압에 의한 점멸비 향상 뿐만 아니라 발광 영역의 확대에도 기여한다. 시뮬레이션과 실험 결과를 통해 본 연구의 효율성을 검증하였으며, 이를 통해 유기 전계 효과 트랜지스터를 차세대 전자 소자, 특히 디스플레이 소자 분야로 적용할 수 있는 잠재력을 극대화했다.

본 논문에서 구현된 새로운 다층 적층 구조의 소자 구조들은 유기

전계 효과 트랜지스터의 전기적 능력 향상의 밑바탕이 될 것이다. 또한 수치 해석 프로그램을 통한 체계적인 물리적 매커니즘 분석과 그에 기반한 실험결과는 본 논문에서 제안한 소자 구조의 유효성을 입증한다. 본 논문에서 제시된 이중 게이트 구조의 양극성 트랜지스터, 중간층을 도입한 전하 주입 능력 향상 및 전하 경로 조절을 통한 높은 점멸비를 갖는 수직 구조의 유기 발광 트랜지스터는 유기 전자 소자의 집적 뿐만 아니라 차세대 다기능 유기 전자 소자의 개발에 중요한 방향을 제시할 것으로 기대된다.

핵심어 : 유기 전계 효과 트랜지스터, 유기 발광 트랜지스터, 소자 구조, 수치 해석 시뮬레이션, 전하 주입 및 거동

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