공학박사학위논문

A Study on Fabrication of High Performance Polycrystalline Silicon Thin Film Transistors

고성능 다결정 실리콘 박막 트랜지스터의 제작에 관한 연구

2018 년 2 월

서울대학교 대학원
재료공학부
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by

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A dissertation submitted to the Faculty of Seoul National University in partial fulfillment of the requirements for the degree of Doctor of Philosophy

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ABSTRACT

A Study on Fabrication of High Performance Polycrystalline Silicon Thin Film Transistors

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The emergence of liquid crystal display (LCD) devices is due to the development of thin film transistor (TFT) integration technology in which amorphous silicon (a-Si) is deposited on a glass substrate. As a result, the LCD and plasma display panel (PDP) replaced the cathode ray tube (CRT) after 2000s. The usage of PDP with high power consumption begun to gradually decrease, and the LCD has become common and now it is an essential element in many electronic devices. Recently, however, the display industry is in the period of transition due to the development of active-matrix organic light emitting diode (AMOLED) display, providing higher color gamut, wider viewing angle, and lower power consumption. Since the light source of the active matrix display is driven by the TFT formed in the pixel circuit, the characteristics of the TFT determine the performance of the display. Unlike the LCD, which uses voltage driving circuits, the AMOLED display utilizes current driving circuit resulting in the TFTs with a high field-effect mobility. Therefore, research on an active layer

material to replace the a-Si TFT having a low field-effect mobility and poor reliability has become imperative. Polycrystalline silicon (poly-Si) is the most proper material for this purpose, and various low temperature crystallization methods have been studied for producing poly-Si such as solid phase transformation, laser crystallization and metal-induced lateral crystallization (MILC). Among many crystallization methods, MILC has attracted attention from the industry as the low temperature polycrystalline silicon (LTPS) technology for the next generation of display fabrication because it has advantages in field-effect mobility, uniformity in crystallization, grain size, thermal damage on device, and large area process. Displays are also evolving from the AMOLED display, aiming for higher resolution, wider panel area, and higher performance display such as 3D display. Therefore, in this study, the research was focused on the development of high performance poly-Si through the MILC process applicable to the next generation of display. As a result, the following experiments were conducted.

In the first study, a planarized copper gate MILC poly-Si TFT has been fabricated and characterized. As displays have been developed to the need for the continuously increasing panel area, higher resolution, and higher performance compared with conventional displays, high-frequency addressing is required. Therefore, it becomes important to reduce the RC propagation delay, caused by electrical resistance of the interconnection line, has become a significant issue. The planarized copper structure using the trench was possible to fabricate interconnects for fast signal addressing. The MILC poly-Si TFT fabricated on this planarized interconnect and this structure solved problems such as adhesion to the glass substrate in the device, fast diffusion, and etching problems. In addition, the effect of suppressing the leakage current was confirmed by applying a combination of a planarized gate and an overlap/ off-set at the

source-gate/ drain-gate structure. This is because the suggested structure reduces the lateral electric field applied between the source and the drain, and also effectively reduces the gate leakage current generated between the gate and drain regions.

The second research investigated surface treatments for the improved interface between the gate dielectric and the poly-Si layer by reducing the defects for the high performance MILC TFT fabrication. Several surface passivation techniques, including oxidizing silicon surface with HNO_3, H_2SO_4, and HCl, as well as N_2O plasma treatment, were investigated. Strong acids showed surface cleaning effect of removing heavy metals while forming a thin oxide layer on the surface of the poly-Si. The N_2O plasma reduced the defects and stabilized the interface by forming oxynitride films. Among them, the MILC poly-Si TFT fabricated with the N_2O plasma showed the best performance in the electrical characteristics and reliability.

In the third study, a novel LTPS TFTs using a nickel (II) nitrate hexahydrate ($Ni(NO_3)_2 \cdot 6H_2O$) solution was developed. The solution process simplifies the Ni deposition process for MILC. By the solution process, the problem of nickel contamination in the conventional MILC poly-Si can be greatly reduced. Solution-processed MILC poly-Si exhibits high field-effect mobility from elongated crystal grains and shows a large reduction in leakage current due to low defect concentration in the channel area. Moreover, using the advantages of the solution process, poly-Si TFT could be fabricated with a simplified two-step mask process. TFTs fabricated using this method could prevent threshold voltage shift by using a low concentration nickel solution process and achieve performance as TFTs of conventional MILC process.

Therefore, in this thesis, experiments on the fabrication of high performance poly-Si TFTs using MILC process have been carried out, and it will be possible to make next generation display beyond the limit of current fabrication technology.

Keywords: active matrix organic light remitting diode (AMOLED), low-temperature polycrystalline silicon (LTPS), metal-induced lateral crystallization (MILC), thin-film transistor (TFT), copper interconnect, leakage current, solution process, polycrystalline silicon grain

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CHAPTER 1

Introduction

1.1 Flat Panel Displays

Recently, the electronic display has become indispensable technology for everyday life. The displays, including cathode-ray tubes (CRTs), plasma display panel (PDP), liquid crystal display (LCD), and organic light-emitting diode (OLED), have been developing in a rapid pace with various structures, advantages, and operation principles.

Display technologies started from the CRT, which was widely used in televisions (TVs) and personal computer (PC) monitors. The CRT occupied the display market for a long time due to the competitive price and quality such as high resolution, fast response time, and wide viewing angle. However, it had certain weaknesses such as the large volume, heavy weight, and high power consumption as it was operated with vacuum tubes consisting of electron guns and phosphorescent screen. Thus, CRTs gradually disappeared because of these drawbacks and eventually it was superseded by the emerging technology of flat-panel displays (FPDs).

The FPD has become an essential part of the display technology due to the recent trends of light and small applications and the convergence of digital technologies. Moreover, the importance of the large panel area and high resolution is emphasized, opening the era of FPD, led by the PDP and LCD. A PDP is relatively thin with a wide color gamut, and a fast response time, which can be produced much cheaper than the initial LCD. However, the intrinsic problems such high heat generation and power consumption are not solved, because a PDP is composed of millions of cells between two glass panels and uses the principle of emitting light from a plasma discharge of an inert gas mixture inside the cell.

The LCD technology began with the passive-matrix (PM) LCDs in small electronic devices. PM is a method of controlling the liquid crystal by addressing a driving voltage from integrated circuits to a row and a column intersecting at the designated pixel. Therefore, PM operates with a slow response time and inaccurate voltage adjustment, which cause problems in contrast and afterimages in display. Due to the characteristics of the PM, PMLCD is only applied to small electronic applications and unable to provide high resolution and fast response time. The development of thin film transistor (TFT) and peripheral circuits integration technology that is fabricated by deposition of amorphous silicon (a-Si) on a glass substrate, resulted in active-matrix (AM) LCD replacing PMLCD. AM is capable of driving each pixel independently with a switch consisting of a transistor and a storage capacitor. When the transistor in individual pixel of the AMILCD is turned on by electrical signal from the data line and the addressing line, the charge become stored in the storage capacitor, and the hold voltage signal controls the polarization state of the liquid crystal molecule. Since AM can drive each pixel individually, it is able to provide a high resolution and fast response time onto the display. As a result, with the emergence of

AMLCD, it has become a popular medium for transmitting visual information to small devices such as smart phones as well as the conventional TVs.

The active-matrix organic light emitting diode (AMOLED) display has been commercialized lately due to the challenges faced in OLEDs such as lifespan and the high quality active layers in driving circuits. Unlike the AMLCD, which uses liquid crystal and a filter to change the color of the white backlight, the AMOLED display offers higher resolution, faster response time and better viewing angle by providing a direct light source for red, green, and blue OLEDs. Although its high manufacturing price is a problem, it is positioned as the highest quality display due to its advantages. The circuit inside the OLED display pixel requires more than two transistors, one configured as a switch and the other as a current supplier, and one or more capacitors. A switching TFT fabricated from a new active layer material having high field-effect mobility is required to perform a current driven switching operation.

	AMLCD	**AMOLED**
Active Materials	a-Si	poly-Si
Mobility	Low mobility (0.5~1 cm^2/Vs)	High mobility (50~300 cm^2/Vs)
Driving	Voltage Driving	Current Driving
Problem	Low resolution Contrast ratio Viewing angle	Crystallization Process Lifespan of OLED
Flexibility	Bad - Cell-gap change -Backlight unit	Good
Transparency	Bad -Color Filter, Back Light Unit	Good

Table 1.1 Comparison of characteristics between AMLCD and AMOLED.

1.2 Thin Film Transistors for Display

A transistor is a semiconductor device that is used to amplify or switch an electrical signal with at least three terminals. It is consisted of one pair of terminals to determine which current or voltage is applied that is controlled by the other terminal. Transistors are the main element of integrated circuits and the basis of the modern electronic systems.

Various types of transistors have been developed, but the invention of Lilienfeld's field-effect transistor in 1933 initiated the revolution of electronic devices [1.1-1.3]. Miniaturized transistors enable smaller electronic devices that had been ubiquitous in everyday life by being embedded into integrated circuits. Furthermore, the metal-oxide-semiconductor field-effect transistor (MOSFET) played a significant role in the computer industry improving the modern civilization [1.4]. However, in addition to the technology for producing chips on silicon wafers, the fabrication of transistors on substrates with different functions became necessary.

A TFT is one of the field-effect transistors, which is made by the deposition of a thin film of active material, dielectric, and metallic material on a non-conducting substrate [1.5]. In 1979, hydrogenated a-Si (a-Si:H) was discovered, which could be doped with donors or acceptors unlike pure a-Si [1.6, 1.7]. a-Si:H was the first active layer material of TFTs and widely used in the display industry due to its low temperature deposition process (below 300°C), capability of wide-area deposition, and high uniformity of deposited layer. The discovery enabled the AM display technology and the commercialization AMLCD.

1.3 Low Temperature Polycrystalline Silicon (LTPS)

As the display technology is developing to the stage where pixels of higher aperture ratio and higher resolution are needed, higher field-effect mobility and stability are required for the TFT. Although a-Si:H has many advantages, its low field-effect mobility (~1cm^2/Vs) and poor stability can not meet the demand [1.8-1.13]. Therefore, polycrystalline silicon (poly-Si) is proposed as an effective alternative active layer for a-Si. Poly-Si exhibits high field-effect mobility (50~300 cm^2/Vs) and high reliability due to the low defect content. Thus, many low temperature polycrystalline silicon (LTPS) processes have been researched at below 600°C to prevent a thermal damage on the glass substrate [1.14, 1.15]. The LTPS process is basically divided into the laser crystallization process and the non-laser crystallization process. Excimer laser annealing (ELA), which is commonly used in the FPD industry, is a method of melting a-Si with the excimer laser and solidifying with crystallite [1.16, 1.17]. The regions involved in the liquid-solid phase transformation become one crystallite, and this process can produce the largest poly-Si grain. However, it has many disadvantages such as expensive cost and high surface roughness which occurs during the liquid-solid phase transformation. Non-laser crystallization methods are largely categorized in solid phase crystallization (SPC) and metal-induced lateral crystallization (MILC). The SPC is a simple and low cost process with the long time heat process at over 600°C [1.18, 1.19]. However, since the poly-Si grains, which are produced in the SPC are very small, induce frequent scattering of the carriers at the grain boundaries resulting in a relatively low field-effect mobility. In

addition, the prolonged high temperature annealing process causes shrinkage of the glass substrate, which lacks reliability [1.20].

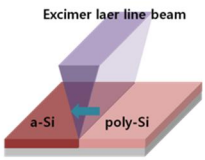
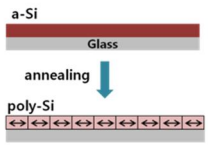
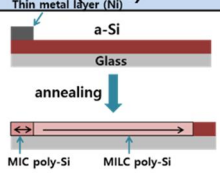
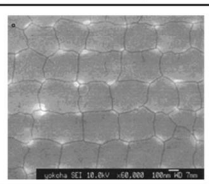
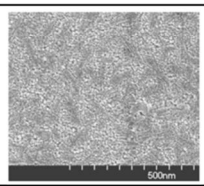
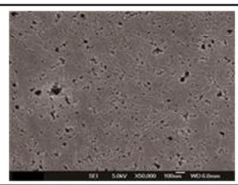
Method	Excimer Laser Annealing (ELA)	Solid Phase Crystallization (SPC)	Metal Induced Lateral Crystallization (MILC)
Process			
Micro-Structure			
Remarks	-Good Crystallinity -Surface Roughness -Expensive Process -Large Area Limit	-Simple Process -High Temperature (600°C~750°C) -Substrate Shrinkage	-Good Crystallinity -Ni Contamination -Add. Mask -Leakage Current

Table 1.2 Crystallization methods for low-temperature polycrystalline silicon [1.21-1.23].

1.4 Metal-Induced Lateral Crystallization (MILC)

Specific metals such as Ni, Pd, Ti etc. act as a catalyst when it contacted with a-Si, thereby lowering the crystallization temperature of a-Si down to 500 °C [1.24-1.26]. The region where the metal contacts with the a-Si forms a silicide, and a metal-induced crystallization (MIC) occurs vertically. Various forms of the silicide compounds are transformed into MSi_2, and the nucleation takes place at the 500 ^{o}C annealing condition [1.27-1.31]. The MSi_2 diffused into Si and form poly-Si. Poly-Si generated by MIC has small crystal grains and is not suitable for use as an active layer

of TFT, because it forms many defects due to metal impurities in grain boundaries which cause trap state in band gap [1.32, 1.33]. However, other crystallization methods using Ni and Pd have been found, and this crystallization proceeds after MIC [1.34, 1.35]. Among the metal catalysts, Ni is widely used due to its faster crystallization. MILC diffuses again from the MIC region where the metal contacts, crystallizing a-Si. The lateral growth is mediated by the Ni silicide that acts as the nuclei due to the lattice mismatch between the crystallized Si and $NiSi_2$ [1.36]. Then, from the nuclei, 1~2 μm sized needle-shaped crystalline-Si grains proceed toward the a-Si region with the migration of the $NiSi_2$ at the front that leaves the crystalline-Si behind the trace [1.37]. MILC poly-Si grains grow by spreading around from the nuclei as forming crystallite network as shown in Fig. 1.1.

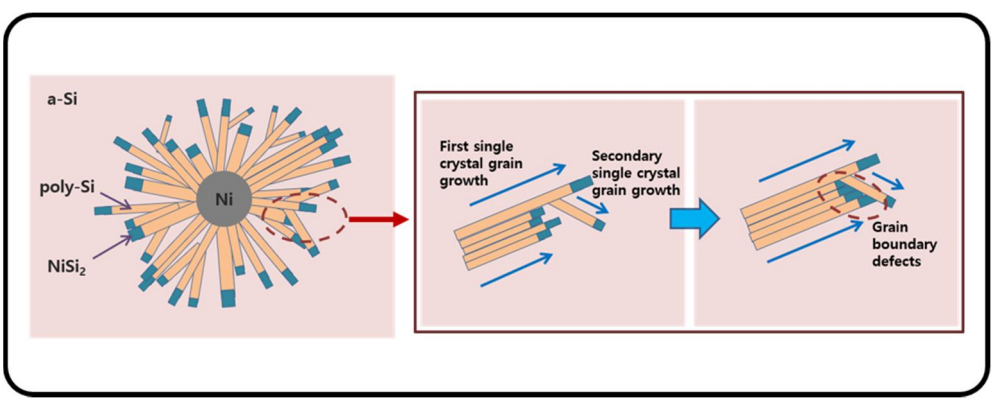


Figure 1.1 Schematic images for the phenomenon of grain growth and defect generation during MILC process.

When the in-progress $NiSi_2$ collides with the already crystallized Si grains, the progress is stopped and the $NiSi_2$ silicide becomes trapped at the boundary of the

grains [1.36]. MILC shows many advantages including low cost batch process, smoother surface, and higher degree of crystalline uniformity [1.38-1.41]. Although it has many advantages, MILC suffers from defects in the active layer resulting from its catalytic process using silicide. The defects acting as a trap state induce a relatively high leakage current, due to the trapped carriers, which is easily activated from the defect energy level existing in the forbidden region. This could induce a leakage current such as field-enhanced thermal excitation of trapped carriers, field-enhanced tunneling, and leakage current between the gate and the drain.

CHAPTER 2

Application of the Metal-Induced Lateral Crystallization Thin-Film Transistors to the Planarized Interconnect

2.1 Polycrystalline-Silicon Thin-Film Transistor Fabricated with Copper Gate Controlled Morphology by Plating Mode

As displays have been developed to the need for a continuously increasing panel area, higher resolution, and higher performance compared with conventional displays, high-frequency addressing is required. Therefore, reducing RC propagation delay ($\tau = RC$), caused by electrical resistance of the interconnection line, has become a significant issue [2.1–2.3]. Copper can be an appropriate substituent for aluminum and its alloys, which are the most preferred materials in conventional metallization in the display industry due to copper's low electrical resistivity (1.7 μΩ-cm) and high resistance in electromigration [2.4]. However, copper typically suffers from high diffusivity in

dielectrics, easy surface oxidation, poor adhesion with glass substrate, and difficulty in wet etching process, rendering it difficult to apply to the device [2.3, 2.5]. As a solution to these obstacles, we proposed a novel planarized copper gate structure of a polycrystalline-silicon thin-film transistor (poly-Si TFTs). In this structure of the TFT, copper is used as the gate metal and is filled into a deep silicon oxide trench. This structure could alleviate problems related to the use of copper in micro devices. If the TFT can be stably fabricated in the copper interconnection of this planarized structure, the process of separately depositing the gate layer can be simplified, and the crosstalk between the interconnections due to parasitic capacitance can be reduced because of the reduction of the contact area of the planar lines. Moreover, fabricating a thick copper gate with a high-aspect ratio trench can ensure an excellent, lower resistance gate without reducing the aperture ratio that affects the transmittance of the display.

Copper was deposited by electroplating in acidic sulphate-plating baths. In modern electroplating practice of filling a high aspect ratio trench, the effects of some additives on the surface quality and growth phenomena of copper have been studied intensively [2.6, 2.7]. Among the additives, a leveling agent, which alters the Cu^{2+} reduction mode, provides a bright and smooth surface for the product. Thus, thiourea (TU), known to act as a leveler, was included in the solution with chloride, reported to enhance the effect of TU, and the combined effect of TU and chloride markedly improved the surface quality of the copper gate [2.8–2.10]. Poly-Si was used as an active layer, which has a higher mobility than that of amorphous-silicon (a-Si), and combined with metal-induced lateral crystallization (MILC) [2.11-2.13]. The MILC method was proper to fabricate poly-Si in inverted staggered TFT than other processes due to its less thermal damages on gate metal and substrate showing a high degree of uniform crystallinity and a smoother surface of poly-Si [2.14-2.16]. With careful

consideration of the structure used for the copper gate and the need to improve the electrical characteristic of the TFT with the gate surface condition, we successfully fabricated high performance planarized copper gate MILC poly-Si TFT.

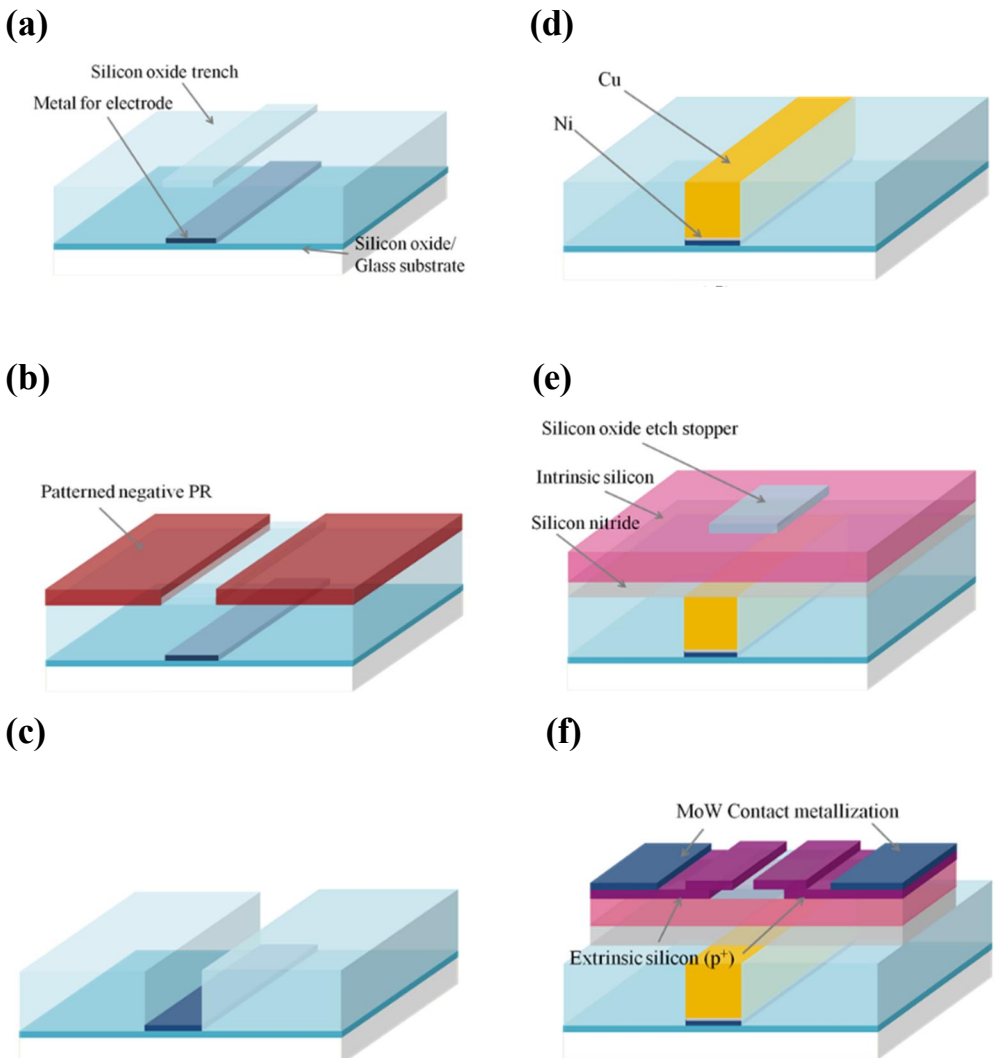


Figure 2.1. Configuration of planarized copper gate MILC TFT process flow on glass substrate. (a) Deposition of buffer layer, metal electrode, and trench silicon oxide. (b) Self-aligned back-side exposure using negative photoresist by copying the bottom electrode. (c) Etching by RIE.

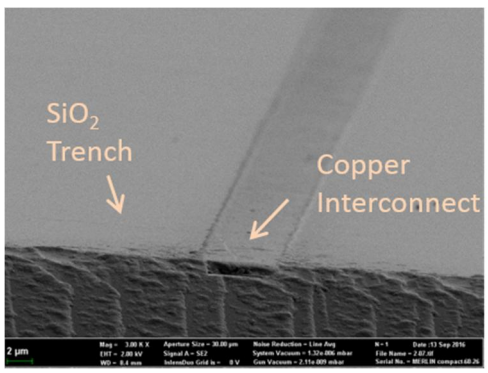
(d) Filling trench with Ni and Cu by electroplating. (e) Deposition of the silicon nitride/a-Si/silicon oxide and silicon oxide layer is etched as an etch stopper. (f) Deposition of extrinsic silicon layer and contact metal. After that, completion of planarized copper gate TFT with MILC process and hydrogen passivation was carried out.

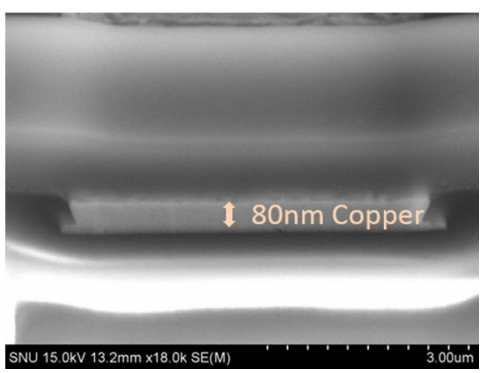
We analyzed the deposited quality of copper surface using atomic force microscopy (AFM) and scanning electron microscopy (SEM). We also characterized the effect of acidic sulphate plating solution using voltammetry and investigated the electrical performance of the TFT from transfer curve.

2.1.1 Experiment

The proposed TFT is basically an inverted staggered type poly-Si TFT with a planarized gate applying a trench structure. The trench is fabricated with a thickness of 500nm and copper was filled in the trench to the same thickness. The planarized copper structure provides many advantages in reducing the copper diffusion area for the gate dielectric, especially at the edge of the gate metal, while it eliminates the need for the wet etching process and inhibits the direct contact with the glass substrate. Fig 2.1 shows schematic illustration of fabrication process of planarized copper gate TFT. The detailed manufacturing process is as follows. First, a 100nm-thick buffer silicon oxide layer was deposited on glass substrate (Corning eagle XG, $10^5 \times 10^5$ mm^2) in plasma-enhanced chemical vapor deposition (PECVD) system. A 100 nm-thick $Mo_{0.9}W_{0.1}$ as a metal line for the electrode was deposited by direct-current (DC) magnetron sputtering system and the metal line is then patterned in an aluminum etchant solution (H_3PO_4+ CH_3COOH + H_2O). Then, 500 nm-thick silicon oxide was deposited on the metal by PECVD. To fabricate the trench structure, self-aligned back-

side exposure was carried out to copy the bottom electrode pattern with the negative photo resist. The thick silicon oxide was then dry etched with a reactive ion etching (RIE) process.





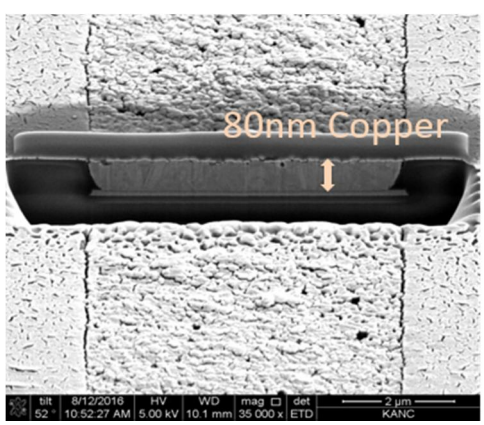


Figure 2.2. SEM images of the trench structure filled with copper

A 50 nm-thick nickel adhesion layer was deposited on the $Mo_{0.9}W_{0.1}$ by DC electroplating and 350 nm-thick copper was deposited on nickel by DC electroplating. Acidic sulphate-plating baths were used, consisting of a bath with 0.1M $CuSO_4$ and 1M H_2SO_4 of normal solution and a bath with 0.1M $CuSO_4$, 1M H_2SO_4, 20μM TU, and 300μM HCl with additives (Fig 2.2). A 80 nm-thick silicon nitride, known to have high resistance in copper diffusion, was then deposited as the gate insulator in PECVD system. Then, a 70 nm-thick a-Si was deposited by PECVD and, silicon oxide as an etch stopper was then deposited on the a-Si layer, sequentially. The etch-stopper was patterned by wet etching in a buffer oxide etchant (BOE) solution as a same size of overlapping area of gate and channel region. After depositing a 100 nm-thick extrinsic silicon layer (p^+) by PECVD, a separate mask was used to separate the source/drain regions on the extrinsic layer. The active layer pattern was also etched by RIE on the intrinsic and extrinsic silicon layer simultaneously. Then, a 5 nm-thick Ni layer was sputter-deposited on source and drain region. The MILC process and hydrogen passivation at 550 ^oC were carried out in a tube furnace in vacuum and hydrogen ambient, respectively. Finally, contact source and drain were fabricated.

2.1.2 Result & Discussion

TU and chloride is generally used in acid sulfuric-plating baths for copper electroplating. However, TU in the plating bath can sensitively alter the mode of

electrocrystallization and deposition kinetics in low concentration by adsorption on the cathodic electrode surface producing a thin interface layer. Chloride improves the

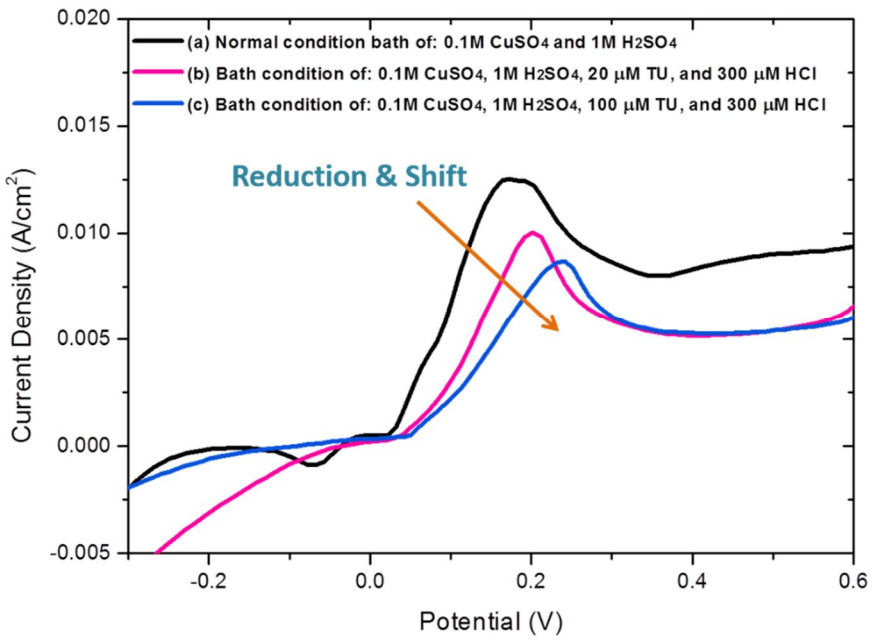


Figure 2.3. Comparison of voltammetry variation for Cu^{2+} reduction with and without additives in acidic sulphate-plating baths: (a) normal condition bath of: 0.1M $CuSO_4$ and 1M H_2SO_4, (b) bath condition of: 0.1M $CuSO_4$, 1M H_2SO_4, 20μM TU, and 300μM HCl, (c) bath condition of: 0.1M $CuSO_4$, 1M H_2SO_4, 100μM TU, and 300μM HCl.

deposit quality compared to the sole use of TU by complexing agents with electrolytes [2.17]. Amount of coverage of the additive molecules on the electrode attribute to the changing degree of cathodic polarization due to the adsorption. As it increases, the total electrode potential polarize toward more positive potential. Fig 2.3 denotes the current suppression by TU, which inhibits Cu^{2+} reduction by coverage on the surface.

Thus, the current density against cathodic potential reduces and the polarization curve shifts as the TU concentration increases.

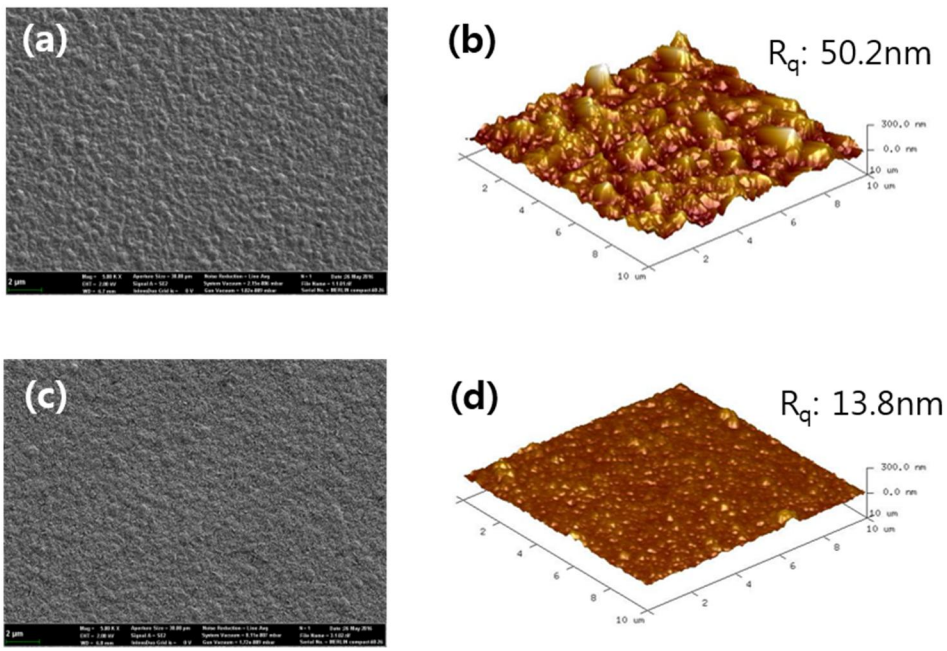


Figure 2.4. SEM images and AFM topographic images of the copper film surface by different plating modes. The conditions include (a), (b): 0.1M $CuSO_4$ and 1M H_2SO_4 bath on 5mA cm^{-2}, (c), (d): 0.1M $CuSO_4$, 1M H_2SO_4, 20μM TU, and 300μM bath on 5mA cm^{-2}

Fig 2.4 (a) and (b) show the dull and poorer quality surface formed in the additive-free acid sulphate-plating bath with relatively large macroscopic nodules. The surface is dendritic and powdery. As expected, microscopically bright and reflective deposits are generated with relatively smaller nodule in the bath with the additives. Fig 2.4 (c) and (d) reveal that TU and chloride can promote a smooth and fine grained structure. The root mean square roughness (Rq) is 50.2 nm at additive involved solution and 13.8 nm at normal solution respectively. Electroplating with TU added solution generates a

macroscopically bright and fine surface, while electroplating in a normal plating bath creates a dull and milky surface. In the nucleation phenomena, TU adsorbed at the

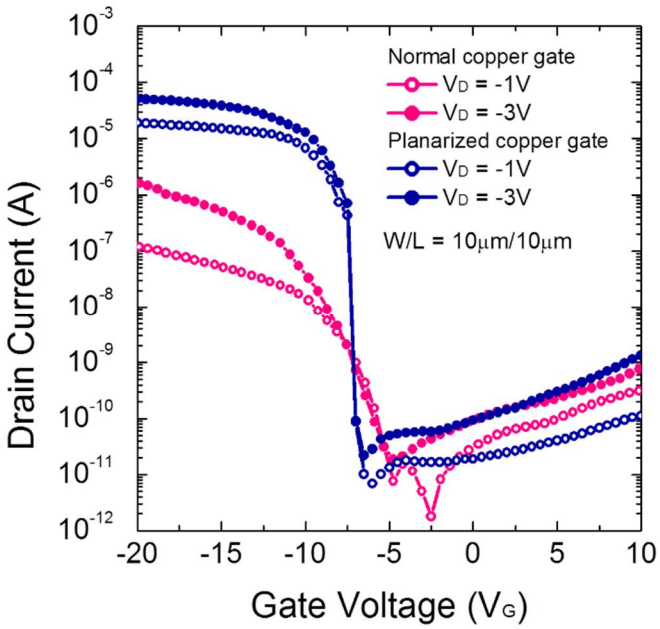


Figure 2.5. Comparison of I_D-V_G transfer characteristics of planarized copper gate MILC TFT electrodeposited in normal acidic sulphate-plating baths (red curves) and with additives (blue curves).

Sample	Normal electroplating	Electroplating with additives
V_{TH} (V)	-18.6	-7.2
μ_{FE} (cm^2/Vs)	0.304	106.968
S.S (V/dec)	0. 86	0. 21
Max. I_{ON} ($\times 10^{-7}A$)	1.2	188
Min. I_{OFF} ($\times 10^{-12}A$)	1.8	16.5

Table 2.1. Key device parameters for TFTs I_D-V_G characteristics at -1V of drain bias of planarized copper gate poly-Si for controlled surface morphology by plating mode.

surface inhibits the adatoms incorporated with the nuclei and blocks the growth of the individual crystal. These functions generate high density of the nucleation site and grain precursor before the growth of grains, resulting in producing smaller crystallites with grain refinement. The presence of leveling agents increases the density of nuclei by blocking the surface diffusion; thus, the surface diffusion-controlled electroplating increases the nucleation rate and the deposits will have a smaller grain structure and finer surface [2.8, 2.9].

The enhanced gate deposit morphology is confirmed to be advantageous for creating a more stable channel and markedly improves the electrical performance of the TFT, as revealed in the transfer curve of the planarized copper gate MILC TFT shown in Fig 2.5 As revealed from table 2.1, reducing the dimension of the surface inhomogeneity enhanced key parameters such as mobility, on current, threshold voltage, and subthreshold slope. The subthreshold slope was defined as the voltage required to raise the drain current by a factor of 10. The maximum on/off current ratio was determined at a drain voltage of -1 V in the gate voltage range of −20 to 10 V. The field-effect mobility was extracted from the peak linear transconductance (g_m) at a drain voltage of −1V. A rougher gate surface generates an unstable channel on the active layer, which induces irregular transport properties of the carrier. Moreover, in the case of an inverted staggered type TFT, the morphology of the gate deposit influences the condition of the silicon nitride film and the poly-Si/ silicon nitride interface condition is directly affected by the roughness of the silicon nitride surface as well [2.18]. Therefore, the conditions that impact on the channel not only influence the

morphology of the copper gate, but also the interface condition of poly-Si/silicon nitride which closely associated with surface roughness scattering. The extent of surface deviation modifies the charge carrier transport properties by interfacial disorder which causes fluctuations of the energy levels at the interface and limits the life time of the drifting carriers [2.19–2.21]. The planarized copper gate TFT with smoother surface morphology exhibited more well-defined saturation and electrical characteristics including subthreshold slope, threshold voltage, field-effect mobility, and high on/off current ratio.

2.1.3 Conclusion

In summary, planarized copper gate MILC poly-Si TFT was successfully fabricated, overcoming problems of copper with novel structure. Moreover, the electrical characteristics were enhanced by high quality surface morphology of copper gate when modifying the plating mode with the additives. The electrical characteristics of TFT were enhanced such as field-effect mobility, on/off current ratio, and subthreshold slope. Thus, it is expected to fabricate a display with a high-frequency addressing using planarized interconnections and safely apply the copper gate transistor simplifying the process.

2.2 Leakage Current Suppression with a Combination of Planarized Gate and Overlap / Off-set Structure in Metal-Induced Laterally Crystallized Polycrystalline-Silicon Thin-Film Transistors

A great deal of attention has been given to research on poly-Si TFTs, with investigations on the use of AMOLED and liquid crystal display LCD technology in the construction of peripheral circuits. The poly-Si reveals relatively higher field-effect mobility than that of a-Si which is sufficiently high to operate as a driving and switching transistor in active matrix flat-panel display devices [2.16, 2.22]. Thus, methods of crystallizing a-Si at low temperature have been widely applied such as solid phase crystallization (SPC), excimer laser annealing (ELA), metal-induced lateral crystallization (MILC), etc. However, the ELA, which has been widely used in the flat panel display industry using XeCl laser, is expensive and causes thermal damages to gate metal during its liquid-solid phase transformation [2.23, 2.24]. SPC silicon shows relatively low field-effect mobility due to the small size and high density of grains [2.25, 2.26]. Also, its high crystallization temperature and long process time could cause thermal damage on the glass substrate. Both ELA and SPC have critical problems for fabricating inverted staggered type poly-Si TFTs, while the MILC could overcome these limits due to its low process temperature of around 500 ℃, high mobility from good crystallinity silicon and large grains, and less thermal damage to

the gate metal and substrate [2.11, 2.27]. However, the MILC TFT suffers from a relatively high off-state leakage current caused by defects in the active layer resulting from its catalytic process using Ni silicide. It has been reported that the leakage current in poly-Si TFTs arises from the high electric field between the channel and drain regions, which results in the activation of free carriers from the trap states within the grain boundary itself, although Ni-mediated crystallized poly-Si causes more trap states from Ni contamination. After the completion of the lateral growth of crystallization, the Ni silicide generally captured in the grain boundary remains in poly-Si. [2.26, 2.28, 2.29] The defects acting as a trap state induce a relatively high leakage current, due to the trapped carriers, which is easily activated from the defect energy level existing in the forbidden region [2.30]. This could induce a leakage current such as field-enhanced thermal excitation of trapped carriers, field-enhanced tunneling, and leakage current between the gate and the drain (Fig 2.6) [2.31-2.33].

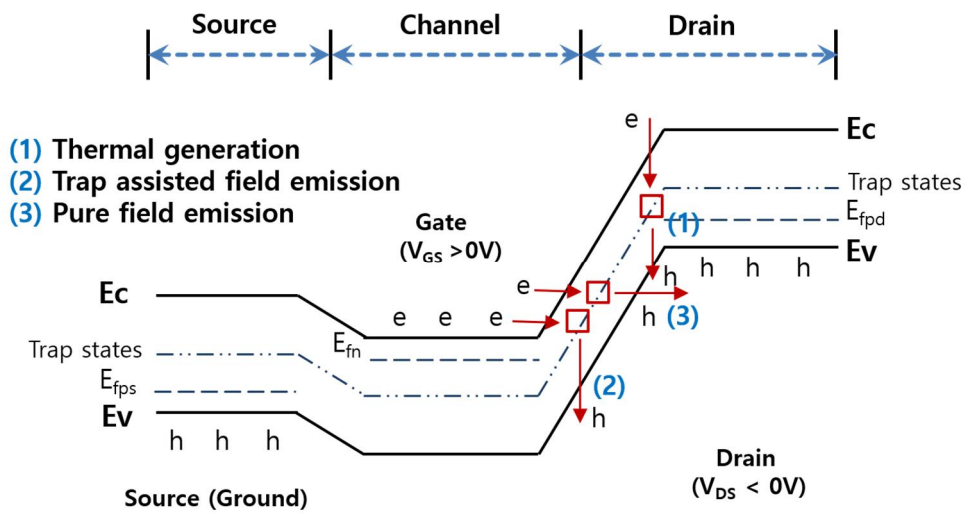


Figure 2.6. The leakage current mechanisms at the off-state regime of the p-type poly-Si.

In this study, we examined a novel inverted staggered structure to alleviate this drawback. A combination of a planarized gate and an overlap/off-set structure was applied to an inverted staggered TFT that was sourced from the mechanism of a lightly doped drain (LDD) and field-induced drain (FID) structure, reported to be effective for reducing leakage current [2.34-2.36]. Shifting the position of the etch-stopper to the direction of the drain side could create an undoped Si area between the channel and drain that does not on the influence of gate bias. Moreover, the planarized gate structure provides thicker gate dielectric to reduce the space-charge limited current (SCLC) than inverted staggered structure of protruded gate when the position of the etch-stopper is modified. Therefore, the suggested TFT could reduce the activation of the carrier from the lowered lateral electric field on the drain side and the leakage current from the gate to the drain. This chapter contains the contents of accepted paper in solid-state electronics.

2.2.1 Experiment

In this work, we produced a novel structure of TFT modified from an inverted staggered TFT widely used in industry. First, we deposited a 100 nm-thick buffer silicon oxide on a glass substrate (Corning eagle XG, $10^5 \times 10^5$ mm^2) in a plasma-enhanced chemical vapor deposition (PECVD) system. A 100 nm-thick $Mo_{0.9}W_{0.1}$ as

an electrode layer was deposited on buffer oxide by a direct current magnetron sputtering system and etched in an aluminum etchant (H_3PO_4+ CH_3COOH + H_2O). Then, a 500 nm-thick silicon oxide was deposited on the electrode layer.

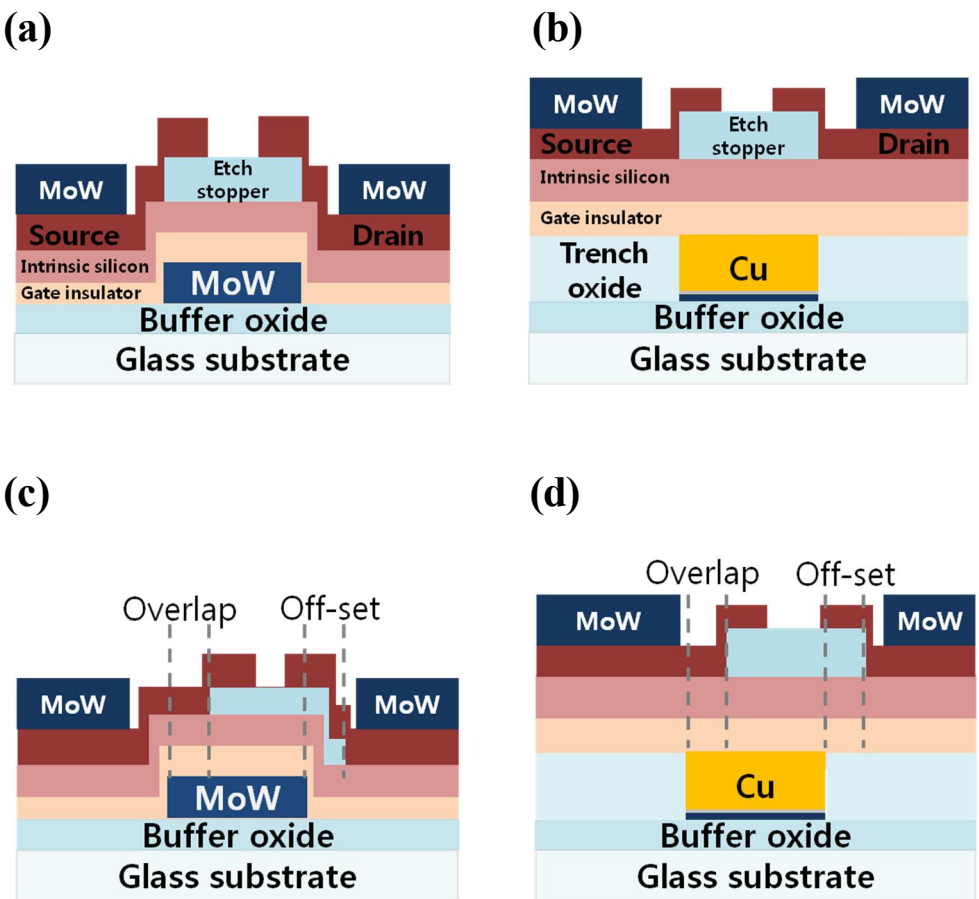


Figure 2.7. Schematic cross-sectional view of (a) inverted staggered TFT, (b) planarized gate TFT, (c) inverted staggered TFT with drain off-set structure was applied, and (d) planarized gate TFT with drain off-set structure was applied.

To make silicon oxide trench, the thick silicon oxide layer was patterned to form the same shape as that of the electrode layer using self-aligned back-side exposure with negative photo-resist (PR) and etched using reactive ion etching (RIE) system. The trench was filled with Ni and Cu. Ni as an adhesion layer of 50 nm-thick was electroplated in 1M $NiSO_4$, 0.2M $NiCl_2$, and 0.5M H_3BO_3 of plating bath. Cu for a gate metal by DC electroplating with acidic sulphate-plating baths, consisting of 0.1M $CuSO_4$ and 1M H_2SO_4. In addition, 20μM thiourea and 300μM HCl were used as additives for a smooth surface [2.8, 2.37]. The electroplating process was advantageous for filling the trench and fabricating the planarized gate structure. After completion of the fabricated planarized gate structure, a 80 nm-thick silicon nitride was deposited in the PECVD to act as a gate dielectric with a diffusion barrier of Cu. Then, a 70 nm-thick a-Si was deposited in the PECVD system. Subsequently, silicon oxide was deposited and patterned in a buffer oxide etchant of the same size as the perpendicularly overlapping region of the channel and gate to act as an etch-stopper to prevent the damage on channel during seperation of the source and drain through RIE. To investigate the influence of the overlap/off-set structure, four other samples are fabricated by shifting the etch stopper by 1μm and 2μm in the direction of the source and drain, respectively. Fig 2.7 (a) and (b) show schematic illustrations of the planarized gate TFT and inverted staggered TFT, respectively, comparing the transformed features as the etch-stopper was shifted to the drain region from the channel area shown in Fig 2.7 (c) and (d). As the position of the etch-stopper was shifted to the drain region, the source region was overlapped and the drain became off-set perpendicularly with the gate. Therefore, the influence of the gate bias decrease near the drain region, and increase at the source region. Then, extrinsic silicon (p^+) was

deposited by PECVD and etched to segregate the source and the drain region by RIE. After the completion of all deposition processes, the extrinsic and intrinsic silicon layers were defined to the source, channel, and drain in the RIE system. Then, the gate dielectric was etched by in-situ RIE process. After that, MILC process was carried out in vacuum ambient to generate poly-Si [2.38]. Finally, dopants were activated and dangling bonds were passivated simultaneously during furnace annealing in H_2 ambient for 2.5 hours. For comparison, the conventional inverted staggered TFTs were also processed under the same conditions, except the process fabricating the gate structure.

2.2.2 Result & Discussion

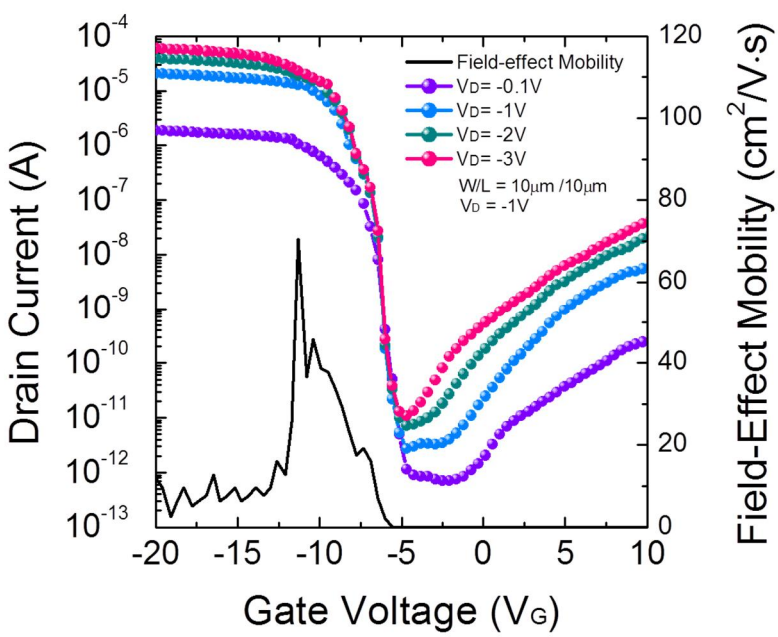


Figure 2.8. Transfer characteristics of the planarized gate TFT in the range of gate bias from 10V to -20V at various drain bias.

The transfer characteristics (I_D-V_G curves) of normal planarized gate MILC TFT were examined with the gate bias swept in the gate voltage range from -20 to 10V at the -1V of fixed drain bias (Fig 2.8). These curves reveal that the TFT exhibits good electrical characteristics including high on-current, low off-current, low subthreshold slope and a high field-effect mobility of 69.3 $cm^2V^{-1}s^{-1}$. However, the planarized gate TFT still denotes a sharp increase of current in the positive gate bias region related to the trapped carriers in the high electric field due to Ni silicide defects in channel/ drain junction. In the MILC process, $NiSi_2$ migrates toward the a-Si region, leaving crystallized silicon behind the trace. When the $NiSi_2$ moving forward at the front collides with the already crystallized silicon, the $NiSi_2$ becomes captured between the poly-Si grains. Then, Ni silicide captured at the grain boundary generates high density of charge trapping states in the forbidden band-gap region [2.29, 2.30]. These charge trap states are related to leakage current resulting from the thermionic emission due to the thermal excitation of trapped carriers occurring in the low gate bias region as well as to the field-enhanced tunneling of the trapped carriers in the high reverse gate bias region. When the reverse voltage increases, a phenomenon called a 'pinning' occurs in which the leakage current increases.

Fig 2.9 (a) shows a comparison of the transfer characteristics of the proposed TFTs with the planarized gate and the off-set/overlap structure are applied. The measured and extracted parameters are also summarized in table 2.2. The threshold voltage was defined at a normalized drain current ($I_D \times W/L$) of 0.1 μA at a drain bias of -1V. The

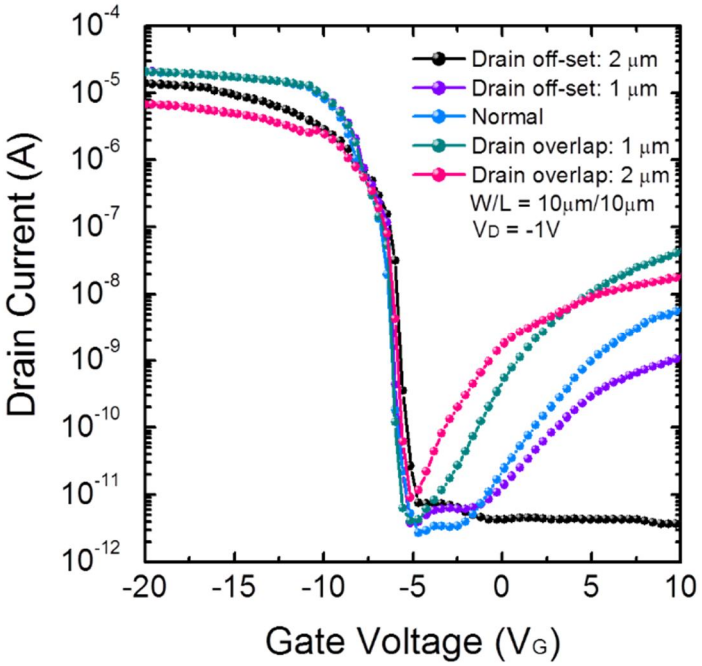
subthreshold slope was extracted from the curve as the voltage required for the drain current to increase by a factor of 10.

$$S = \frac{dV_g}{d(\log I_d)}$$

The field-effect mobility was calculated by applying the following equation from a maximum value of transconductance (g_m) in the linear region at a drain voltage of -0.1V.

$$\mu_h = \frac{L}{WC_iV_D} g_m = \frac{L}{WC_iV_D} \frac{\partial I_d}{\partial V_g}\bigg|_{Vg=const.} \quad (V_d < V_{dsat})$$

(a)


Drain Current (A)
Gate Voltage (VG)
Drain off-set: 2 μm
Drain off-set: 1 μm
Normal
Drain overlap: 1 μm
Drain overlap: 2 μm
W/L = 10μm/10μm
VD = -1V

(b)

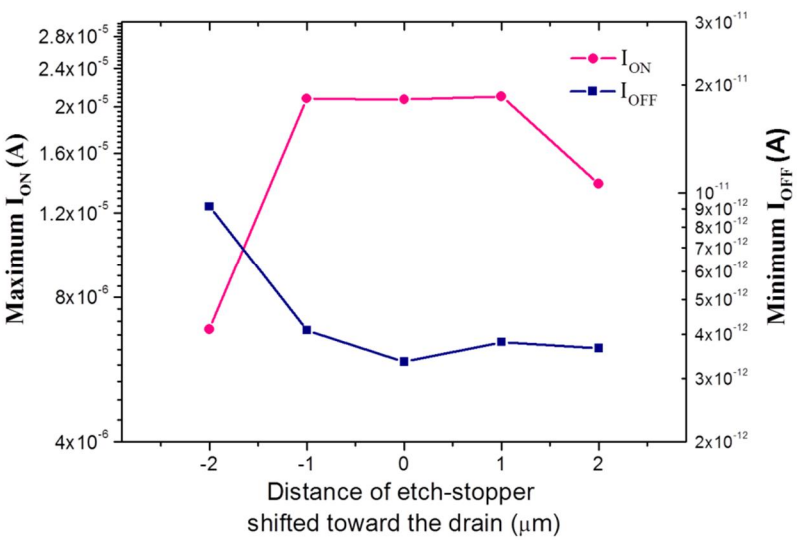

Maximum ION (A)
Minimum IOFF (A)
ION
IOFF
Distance of etch-stopper
shifted toward the drain (μm)

Figure 2.9. (a) The comparison of transfer characteristics of the planarized Cu gate TFT from different overlap/ off-set stage in the range of gate bias from 10V to -20V at a -1V of drain bias. (b) Effect of the overlap/ off-set lengths on minimum off-current and maximum on-current at V_G = -20 V and V_D = -1 V.

Planarized gate TFT					
Distance of etch-stopper shifted to the drain(μm)	**-2**	**-1**	**0**	**1**	**2**
V_{TH} (V)	-6.40	-6.74	-6.58	-6.53	-6.38
Subthreshold Slope (V/dec)	0.24	0.16	0.13	0.18	0.25
Field Effect Mobility (cm^2/Vs)	44.29	60.26	70.43	65.09	53.03
On Current (10^{-6}A)	6.85	20.8	20.7	21	13.8
Off Current (10^{-12}A)	9.15	4.1	3.35	3.8	3.65
Leakage current at 10V of gate voltage (10^{-10}A)	189	448	58.9	11.5	0.38

Table 2.2. Electrical properties of the planarized gate TFTs with different overlap/off-set length.

The leakage current of the TFTs was drastically suppressed as the position of the etch-stopper shifted to the drain side. On the other hand, the leakage current sharply increases when the drain overlaps the gate perpendicularly. The off-set structure is evidently effective to reduce leakage current by restricting the high electric field between the channel and drain regions. When the 2μm off-set to drain side is applied, no pinning phenomenon is observed. The leakage current model in poly-Si TFT, according to the trap assisted field-emission model, can be explained by [2.39]

$$I_L \approx qWx_eN_T\left(\frac{1}{\tau_{TC}+\tau_{TV}}\right)\left(\frac{|V_D|}{E_x}\right)$$

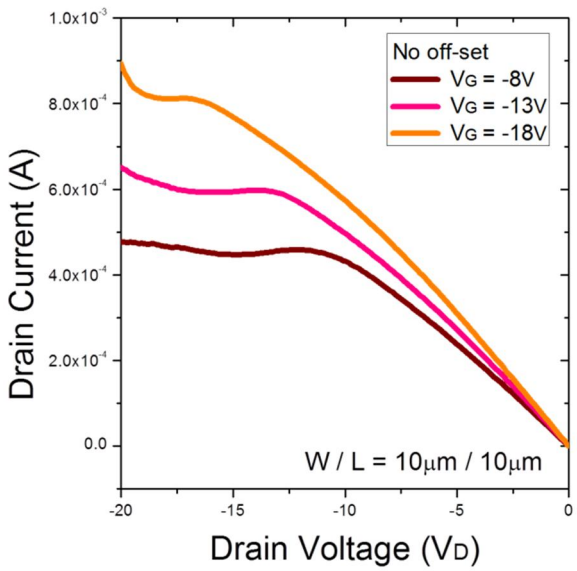
where W, x_e, and N_T are the effective channel width, effective depth of the junction region, and the trap density, respectively, the values of which are dependent on the reverse gate bias regime. The time constants, τ_{TC} and τ_{TV}, are for hole and electron tunneling which are in inverse proportion to the electric field. From this model, it can be considered that the lateral electric field plays the most important role and the leakage current can be reduced by decreasing the lateral electric field at the channel and drain junction regions. By the shifting the position of the etch-stopper, the leakage current of TFT can be lowered by reducing the lateral electric field. The maximum on- and minimum off-current show a different tendency as the performance is degraded as the off-set and overlap structures are applied (Fig 2.9 (b)).

It could be assumed that the shifting of the etch-stopper modifies the position of the extrinsic region (p^+) and this structure also induces a reduction of channel area affected by the gate bias. When gate bias is applied, an undoped Si area between the channel and drain is generated in the active layer and the density of the carrier is reduced as the lateral electric field is decreased, so that the mobility and on-current of the TFTs become degraded. Moreover, the drain off-set structure shows a higher on-current than that of the drain overlap structure. Carriers with high energy that are accelerated from the source can move more through the hot carrier or tunneling effect in the drain off-set structure.

The minimum off-current is reduced as the position of the etch-stopper moves toward the drain region. The shift of the etch-stopper position to drain side could reduce the minimum off-current that restricts the flow of the carrier. However, the minimum off-current is also affected by the formation of the accumulation area. This implies the result of a slight increase in the minimum off-current in the drain off-set state.

Therefore, when drain off-set structure is applied, the leakage current can be effectively reduced without considerable reduction in the on-off current ratio.

(a)



(b)

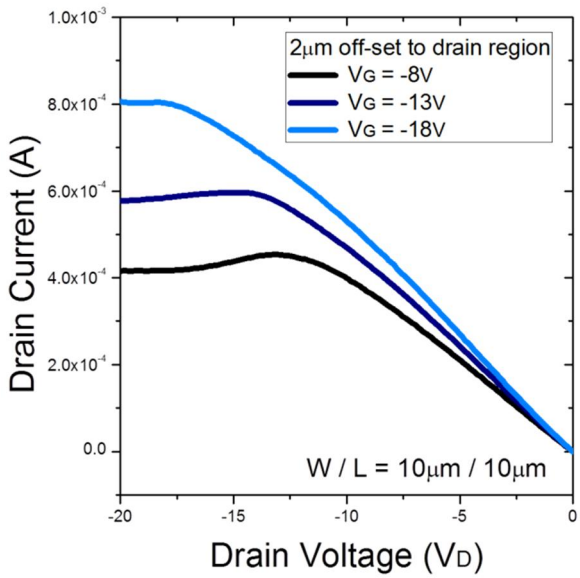


Figure 2.10. Output characteristics of (a) normal planarized gate TFT and (b) planarized gate TFT with the 2μm drain off-set.

Fig 2.10 shows a comparison of the output characteristics (I_D-V_D curves) of the normal planarized gate TFT and the planarized gate TFT with 2μm drain off-set in high gate bias. The drain current increment appears at the normal planarized TFT after saturation and the planarized gate TFT with off-set structure exhibits kink-free I_D-V_D characteristics. The kink effect is related to the drain junction trap sites and the junction area [2.40-2.42]. This phenomenon implies that the drain off-set structure could effectively reduce the lateral electric field at the channel/drain junction region, which results in reducing the impact of the ionization rate and thermal excitation of the trapped carrier.

(a)

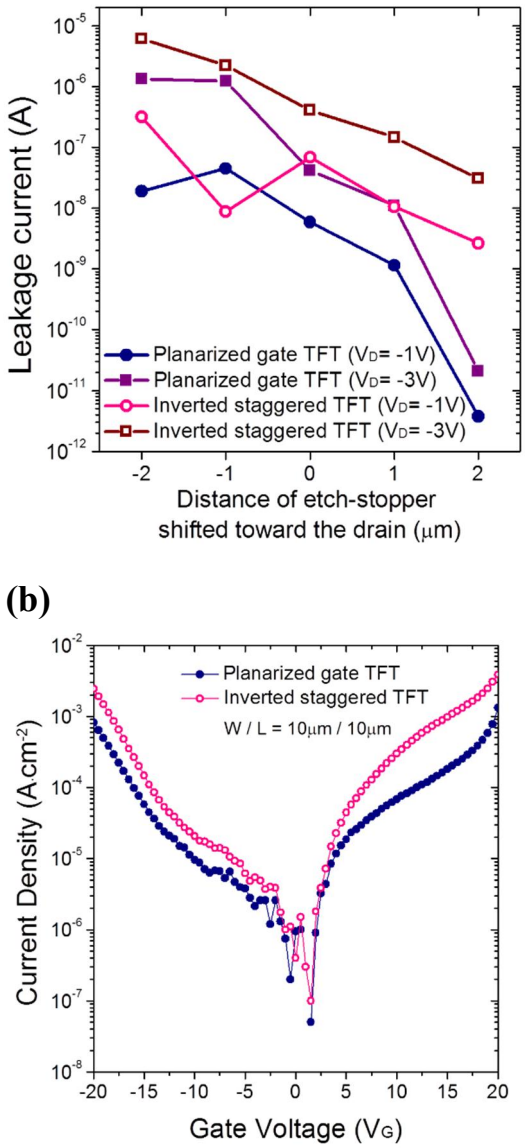


Figure 2.11. (a) Comparison of the drain leakage current at the 10V of gate bias from different position of the etch-stopper. (b) Gate leakage current densities as a function of V_G at the 0V of drain bias between the planarized gate TFT and the inverted staggered TFT with 2μm drain off-set.

Fig 2.11 (a) denotes a comparison of the effect on leakage current for the different positions of etch-stopper lengths in the planarized gate and the inverted staggered TFT respectively. Considering both TFTs fabricated under the same condition except for gate structure, the planarized gate TFT shows a more significant reduction in leakage current than that of the inverted staggered TFT. This phenomenon could be considered to the result from gate leakage current as shown in Fig 2.11 (b). In the MILC process, the gate dielectric could also be contaminated by the diffusion of Ni compound and it generates the interface defect state or fixed charge within the gate dielectric. The defects in the gate dielectric can generate SCLC from the gate to the drain [2.43]. The planarized gate TFT could provide a thicker gate dielectric to reduce the leakage current from the drain than that of the conventional gate. Since the side wall of the gate is relatively thinly deposited along the aspect ratio of the film deposited in the PECVD system, more leakage current is generated in the inverted staggered TFT as shown in Fig 2.7. The thick gate dielectric for the SCLC in the planarized gate TFT effectively decreases the gate leakage current and modified the position of etch-stopper make less than that of the lateral electric field, which reduces the generation of hot carriers and tunneling current. Therefore, the low leakage current of MILC TFT is attributed to a combination of the planarized gate and the drain off-set structure.

2.2.3 Conclusion

In summary, we successfully fabricated a novel structure of poly-Si TFT with a planarized gate and an overlap/ off-set structure. The modified position of the etch-stopper to the drain position could create an undoped active area that is not affected by

the gate bias; this reduces the lateral electrical field near the drain region. The planarized gate structure renders this phenomenon more effective by extending the SCLC path. Compared with the normal inverted staggered TFT, the novel TFT could reduce more leakage and pinning current effectively. Therefore, the proposed TFT can be easily applicable to high-density and reliable-performance displays.

CHAPTER 3

Interface Improvement for the Metal-Induced Lateral Crystallization Thin-Film Transistors

3.1 Effect of Ultrathin Silicon Oxide Film for Enhanced Performance and Reliability of Metal-Induced Laterally Crystallized Thin-Film Transistors

Polycrystalline silicon (poly-Si) has been widely used in active-matrix flat panel displays (AMFPDs) as an important material for thin-film transistor (TFT) because of its higher mobility and driving current than those of amorphous Si (a-Si) [3.1, 3.2]. Thus, methods of crystallizing a-Si at low temperature have been widely applied. Among the various low-temperature polycrystalline silicon (LTPS) methods, metal-induced lateral crystallization (MILC) has many advantages such as a low-cost batch process and smooth film surface. However, the MILC method causes many defects in channel during the process due to the Ni silicide residue and its randomly formed grain boundary which degrade the electrical characteristic of the poly-Si TFT by creation of potential barrier [3.3-3.5]. When a gate dielectric is directly deposited on a MILC poly-Si surface, the high interface trap-states and grain-boundary trap states in

the band-gap region which induce a high subthreshold slope and high leakage currents including the Poole-Frankel (P-F) emissive current and gate leakage current through gate dielectric [3.6] Also as gate dielectric, silicon nitride exhibit good electrical performance due to its higher permittivity than that of silicon oxide, while it has a number of electrical stability problems caused by interface quality and the fixed charge within the dielectric [3.7-3.9]. Silicon nitride on the MILC poly-Si surface generates high density of trap states. Therefore, surface treatment was proposed to overcome these problems. However, for a display substrate such as glass and plastics, they are not able to withstand high temperature and high pressure, and growing stable thick silicon oxide using thermal oxidation or wet oxidation in high pressure is not possible [3.10]. Thus, forming a thin layer by oxidation to stabilize the poly-Si surface before depositing the gate dielectric was considered. Strong oxidizing agents of silicon such as HNO_3, H_2SO_4, and HCl were proposed due to the effect of oxidation and removing the heavy metals on the poly-Si surface [3.11-3.14]. Wet oxidation was performed in atmospheric pressure and 75 ^oC in a stable condition for glass substrate. Moreover, to accelerate the oxidation process in low temperature, H_2O_2 was blended with acid for strong oxidation and cleaning effect. We also investigated N_2O plasma as a surface stabilizing method. It was effective because the insertion of nitrogen, forming an oxynitride and Si≡N bond at the surface of the silicon was found to have a positive impact, reducing the charge traps and stabilizing the interface [3.15]. We confirmed the poly-Si surface condition by X-ray Photoelectron Spectroscopy (XPS) to obtain useful information about the silicon/oxygen compounds and the surface condition. And finally, we also confirmed the performance variation of the surface treated MILC poly-Si TFTs through the I_D-V_G characteristics and the reliability of each surface treated sample from mechanism of hot carrier stress. This chapter

contains the contents of published paper in ECS Journal of Solid State Science and Technology [3.16].

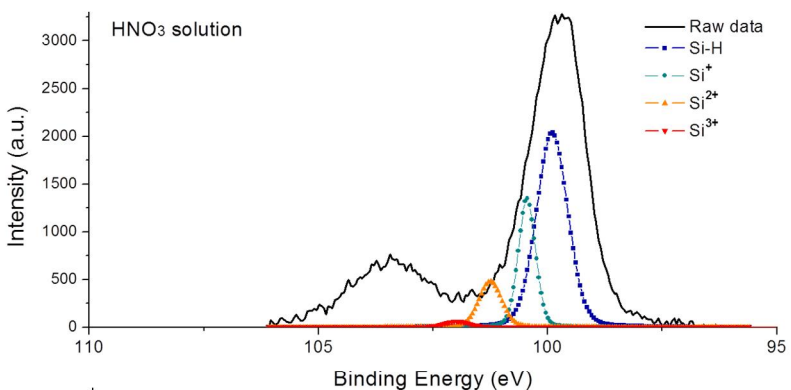
3.1.1 Experiment

The same MILC poly-Si was produced on glass substrate prior to surface treatment to fabricate conventional coplanar poly-Si TFT. First, a 200 nm-thick silicon oxide as a buffer layer and a 50 nm-thick intrinsic a-Si channel layer were deposited by plasma-enhanced chemical vapor deposition (PECVD) on a glass substrate sequentially. After patterning an a-Si active region, a 5 nm-thick Ni film was deposited on a same dimension with the metal contact area for source/ drain using a direct-current (DC) magnetron sputtering system, and the Ni film was then removed with sulfuric acid. Heat processing was then carried out in hydrogen ambient at a temperature of 550^{o}C for 2hours to make MILC poly-Si using the mechanism of seed induced lateral crystallization [3.4]. RCA cleaning was then performed to remove impurities. Surface treatment was carried out by using two different procedures. Wet oxidation was the first treatment which is generating a thin oxide layer on poly-Si by immersing in acids. To make thin silicon oxide layer, three samples were oxidized in 75°C HNO_3, H_2SO_4, and HCl solution, respectively. Each solution was blended with H_2O_2 of 1:1 ratio to make accelerate oxidizing reaction. The second treatment was using N_2O Plasma within the PECVD in 350^{o}C. The gas condition was N_2O gas 20sccm, Ar gas 10sccm under 100W of radio-frequency (RF) power for 600 seconds. A 50-nm-thick silicon nitride was then deposited after surface treatment and $Mo_{0.9}W_{0.1}$ alloy metal was deposited thereon as the gate metal by DC magnetron sputtering. The gate metal was

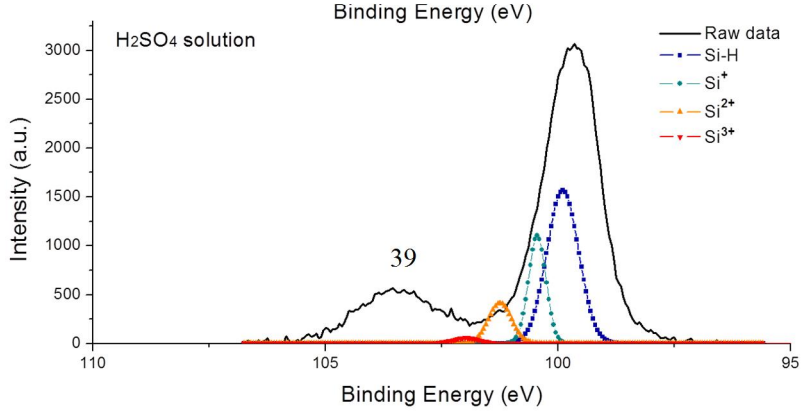
patterned by a gate mask and wet etching was performed. Then, the gate insulator was dry etched using the self aligned gate metal. In order to make the source/drain junction, the sample was doped by ion shower system using B_2H_6 source gas. After that the contact layer was deposited with $Mo_{0.9}W_{0.1}$. In the final process, furnace annealing was performed in H_2 ambient at a temperature of 550°C for 2hours to electrically activate the dopants. And surface treated MILC samples, fabricated with the same method on Si wafer, were characterized by XPS spectra.

3.1.2 Result & Discussion

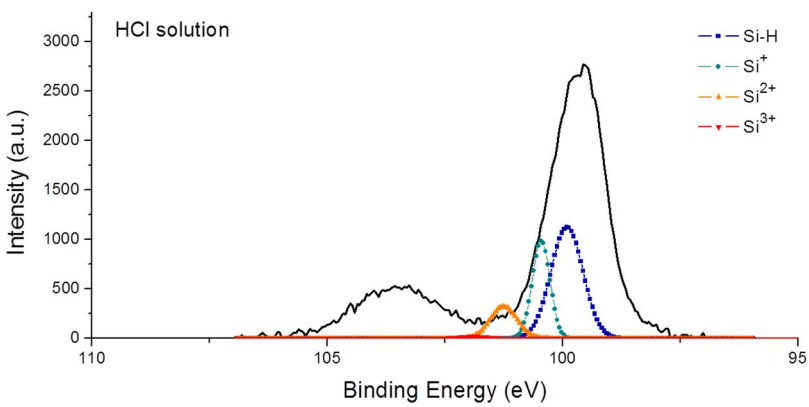
(a)



(b)

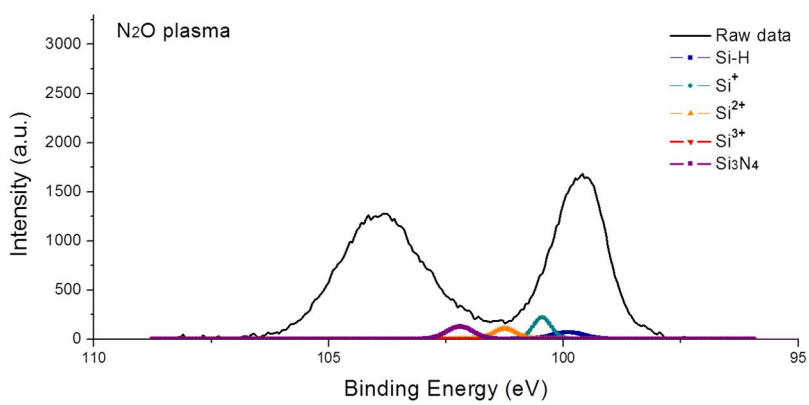


(c)


HCl solution
Si-H
Si+
Si2+
Si3+
Intensity (a.u.)
3000
2500
2000
1500
1000
500
0
110
105
100
95
Binding Energy (eV)

(

d)


N2O plasma
Raw data
Si-H
Si+
Si2+
Si3+
Si3N4
Intensity (a.u.)
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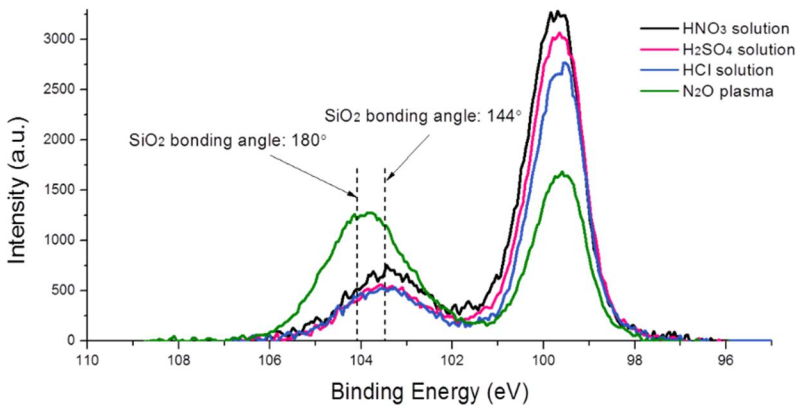
2500
2000
1500
1000
500
0
110
105
100
95
Binding Energy (eV)

(e)



(f)

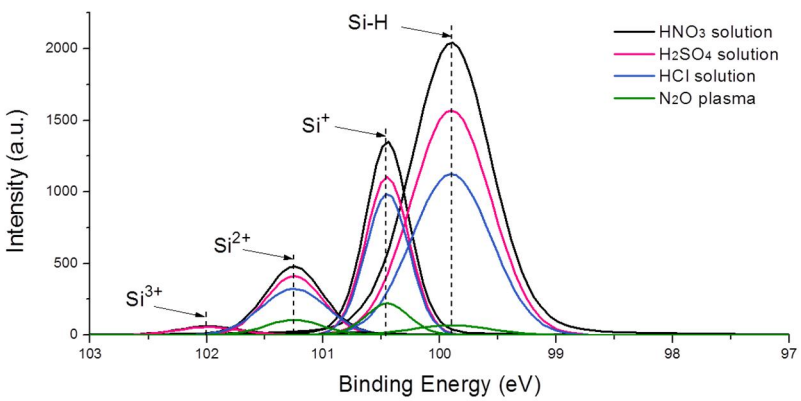


Figure 3.1. XPS spectra in the *Si 2p* region for the chemical oxide-covered Si surfaces. The chemical treatments for the formation of the oxide layers are as follows: (a) MILC poly-Si in HNO_3:H_2O_2= 1:1 at 75°C for 15min, (b) MILC poly-Si in H_2SO_4:H_2O_2= 1:1 at 75°C for 15min, (c) MILC poly-Si in HCl:H_2O_2= 1:1 at 75°C for 15min, (d) MILC poly-Si treated with N_2O plasma and comparison of (e) raw data peaks, and (f) sub peaks.

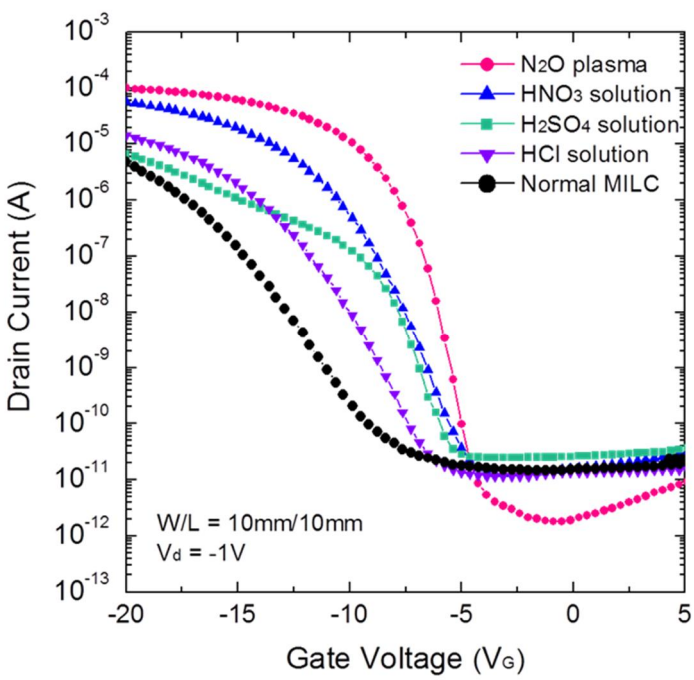
Fig 3.1 shows the XPS spectra in the Si 2*p* region of the oxide-covered MILC poly-Si surfaces. Grown oxide layers in HNO_3 solution, H_2SO_4 solution, and HCl solution are shown in Fig. 1(a), 1(b), and 1(c), respectively, and Fig. 1(d) is for silicon oxide layer

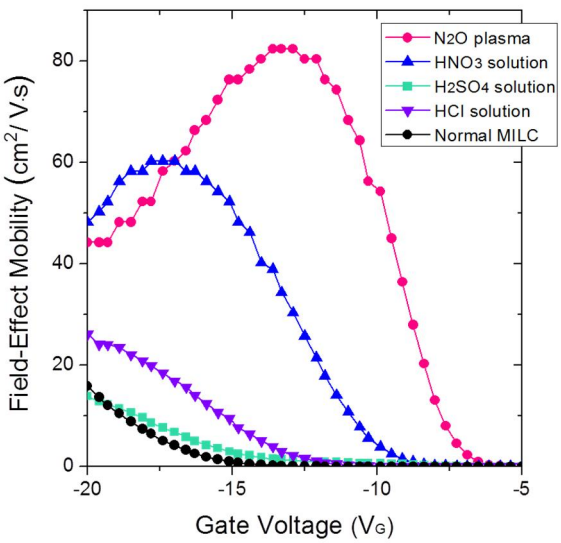
generated by N_2O plasma. The two main peaks indicate silicon oxide and Si bonding located at 103.4 eV and 99.5 eV, respectively. The thickness of the oxide grown film can be identified from the intensity of the Si 2*p* peak, which indicates the increment in the thickness of bonding. The peaks of intermediate oxidation states, i.e., Si^{+}, Si^{2+}, and Si^{3+}, denote Si atoms, each bound with one, two, and three oxygen atoms, are assumed to be located at 0.95, 1.75, and 2.50eV, respectively, shifted from the Si *2p* peak [3.11, 3.12, 3.17]. They easily become interface trap-states when the Si-O bond of the species is ruptured due to its weak and unstable bonds [3.18].

The generated oxide film was 2~3-nm-thick for wet oxidations, 4~5-nm-thick for N_2O plasma. The oxidizing power of HNO_3 solution was more effective than other acids, while intermediate oxidation states are increased simultaneously. The peak of the Si-H species in the HNO_3-grown oxide layer is the highest because more of the Si dangling bond was passivated by the proton to form a Si-H bond. In the case of the H_2SO_4 and HCl solutions, the amount of increased silicon oxide was similar to that of the HNO_3 solution, but the capability of forming oxide was slightly lower. H_2SO_4 and HCl solution also have low amounts of Si-H species as well and are therefore expected to show a lower grade active layer property. From these results, HNO_3 is the strongest oxidizer, implying that it is also the most appropriate candidate for fabricating MILC TFT within wet oxidation processes. N_2O plasma is also able to generate a thin oxide film on a silicon surface. It shows the generation of a considerably large oxide layer in short time and a markedly reduced amount of Si. It also shows the lowest intermediate oxidation states among surface treated samples. The major difference between the N_2O plasma and the wet oxidation is that the shift of silicon oxide bonding Si 2*p* peak because of the insertion of oxygen and nitrogen together on the MILC poly-Si surface forms not only Si-O bonding but also Si≡N bonding. It stabilizes the charge trap states

by the interface passivation effect of the nitrogen and generates oxide film containing Si≡N bonding which has less carrier trapping site and smoother film interface than that of oxide film [3.19]. Moreover, the insertion of nitrogen induces changing bond angle of Si-O which results in reducing strain of the interfacial surface originated from the MILC process. It leads to a substantial improvement in the surface quality [3.20-3.22].

(a)





(b)

Figure 3.2. (a) Transfer characteristics and (b) field-effect mobilities of MILC poly-Si TFTs fabricated with surface treatment and normal MILC TFT in the range of gate voltage −20 to 5 V.

Sample	N_2O plasma	HNO_3 solution	H_2SO_4 solution	HCl solution	Normal MILC
V_{TH} (V)	-6.5	-9.0	-9.8	-11.8	-14.8
μ_{FE} (cm^2/Vs)	-82.36	-60.26	-13.86	-26.11	-15.87
S.S (V/dec)	0.5	0.9	0.8	1.1	1.5
Max. I_{ON} ($\times 10^{-6}$A)	99.6	56.5	6.71	14.4	4.8
Min. I_{off} ($\times 10^{-12}$A)	1.8	12.9	25.1	11.6	15.0

Table 3.1. Key device parameters for MILC poly-Si TFTs with and without surface treatment.

Fig 3.2 demonstrates a comparison of the effects of various acids and N_2O plasma on the surface of MILC poly-Si from the I_D-V_G transfer curve and field-effect mobility. Device parameters are summarized in Table 3.1 as well. The transfer characteristics are improved in high mobility, low threshold slope, and high on/off current ratio as a result of surface treatments. All samples show electrical characteristic enhancement by the following tendencies as shown in XPS spectra. MILC TFT treated with HNO_3 solution exhibits the best characteristics within the surface oxidation by acid. The H_2SO_4 solution has an enhanced subthreshold slope and threshold voltage, but the minor progress in hydrogen adsorption induces the negative defect of the dangling bond, degrading on-current. The HCl solution also exhibits an improvement in the characteristics with the cleaning process as well. However, it shows less variation compared with normal MILC TFT because of the lower passivation in which few dangling bonds could be filled with the hydrogen atoms and the remaining dangling

bonds act as trap states. The N_2O plasma treated on the active layer exhibits the highest performance in carrier mobility, low subthreshold slope, and a high on/off current ratio as the concentration of Ni silicides reduced. The unnecessary interaction can therefore be reduced at the interface between the gate dielectric and the active layer surface to reduce the leakage current due to the stress and the tunneling site. In addition, it shows better performance than that of wet oxidation as well.

As is well known, the electrical characteristic of TFT is mainly affected by the microstructure quality of its active layer. The mobility of carriers strongly depends on the size of grains, texture of grains, and intragrain microdefects [3.3]. In the case of the MILC method, crystallization was induced by the migration of Ni silicide. The Ni silicide triggers phase transformation and moves toward a-Si region leaving a trace of needle-like structured epitaxially crystallized grain. If the front side of the Ni silicide in crystallization progress and another poly-Si grain already produced by the MILC process make contact together, the prior will be captured in the side wall of the grain and will then become trap-states. Also, residual Ni silicide on the surface of the generated poly-Si then act as interface-trap states. Therefore, many traps generated by Ni silicide could exist in MILC poly-Si surface, degrading the electrical property of the TFTs [3.4, 3.5, 3.23-3.26].

To measure the lowered grain-boundary trap-densities (N_{gt}) by the effect of surface treatment, the Levinson plot was used and values were extracted from the transfer curve of Fig 3.2 (a) [3.26, 3.27]. Fig 3.3 shows the ln $[I_D/(V_G-V_{FB})]$ versus $1/(V_G-V_{FB})^2$ curves at V_D= -1V and the high gate voltage region above the threshold voltage. The grain boundary density N_{gt} value was obtained from the slopes of the following equation.

$$I_D = \mu_{FE}\, C_i\, \frac{\mathrm{W}}{\mathrm{L}}\, (\mathrm{V_G} - \mathrm{V_{FB}})\, \mathrm{V_D} \exp\left(-\frac{q^2\, N_{gt}^2 \sqrt{\varepsilon_i}/\varepsilon_{\mathrm{Si}}}{C_i^2\, (\mathrm{V_G} - \mathrm{V_{FB}})^2}\right)$$

$$N_{gt} = \frac{C_i}{q}\sqrt{|\mathrm{slope}|}$$

Where the ε_i and $\varepsilon_{\mathrm{Si}}$ values were dielectric constants of the gate dielectric and silicon, respectively. C_i is the capacitance of the gate dielectric, q is the electron charge. The flat band voltages V_{FB} were defined at the gate voltage that yields the minimum drain current at a drain voltage of -1V. As shown in Fig 3.3, as the strength of the surface treated effect increases, the slope becomes steeper.

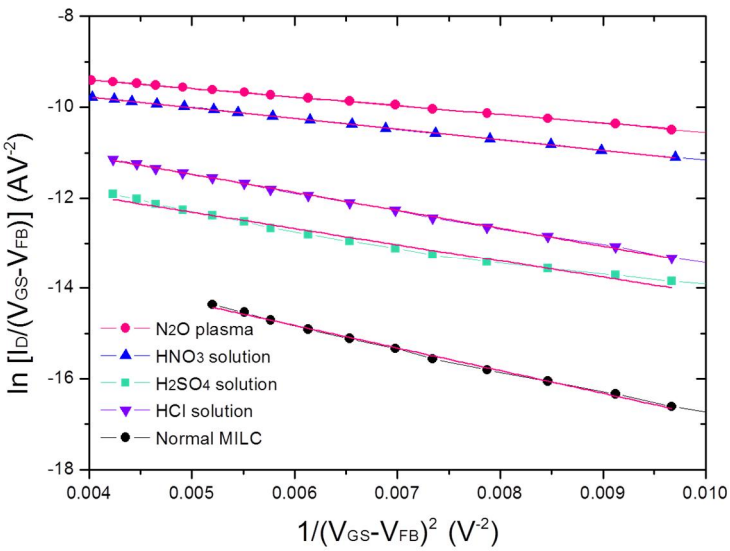


Figure 3.3. Levinson plot of MILC poly-Si TFTs with and without surface treatment at V_D = -1V.

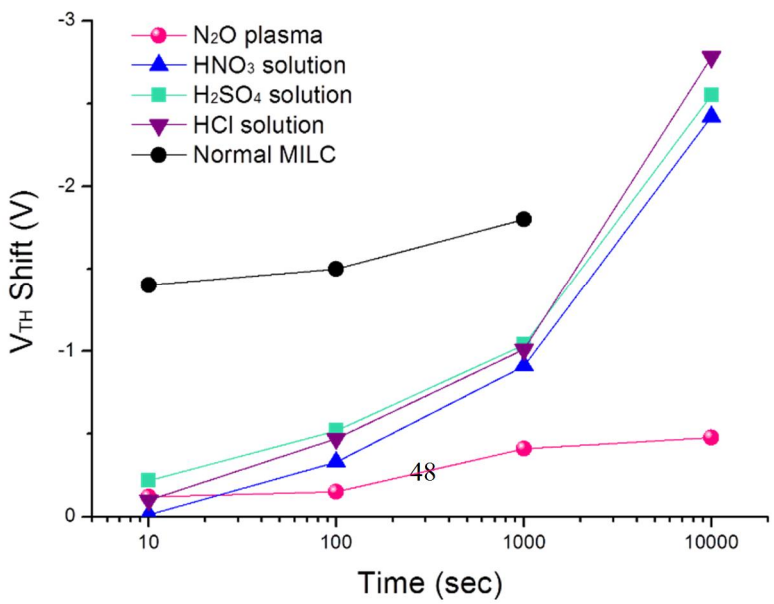
The effective trap-state densities (N_{it}) at the interface were also calculated from the subthreshold slope by applying the Dimitriadis model [3.28].

$$N_{it} = \left(\frac{\mathrm{SS}}{\ln 10}\frac{q}{kT} - 1\right)\frac{C_i}{q}$$

Sample	N_2O plasma	HNO_3 solution	H_2SO_4 solution	HCl solution	Normal MILC
N_{gb} $(\times 10^{+12}\,cm^{-2})$	6.13	11.7	10.3	14.5	20.0
N_{it} $(\times 10^{+13}\,cm^{-2})$	1.14	12.7	15.8	16.5	18.5

Table 3.2. Grain-boundary trap-density and interface trap-density extracted from Levinson plot and Dimitriadis model, respectively.

Where k is the Boltzmann constant. The total grain boundary and interface trap-densities are summarized in table 3.2. The calculated results reveal that wet oxidation shows good enhancement in reducing the trap states in the grain-boundary and interface, and that N_2O plasma was the most effective solution for reducing trap states.



(a)

(b)

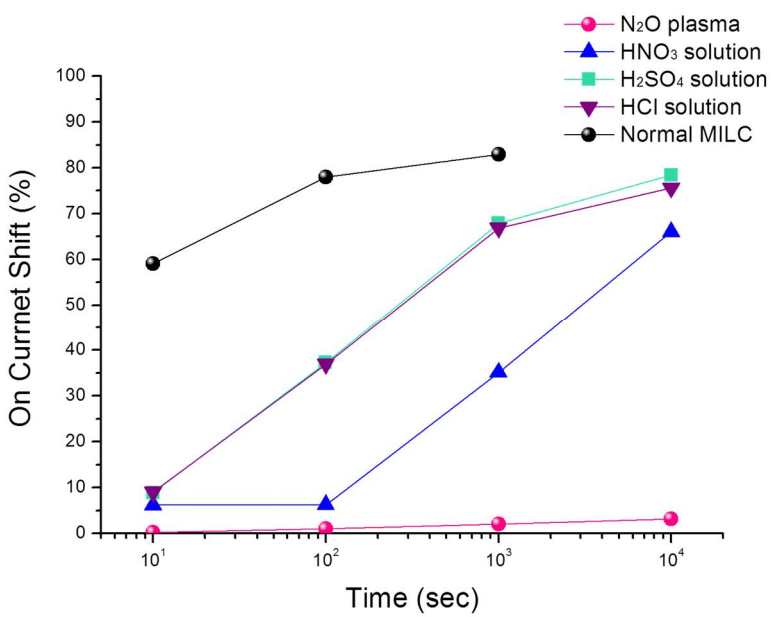


Figure 3.4. (a) V_{TH} shift and (b) on current degradation versus stress time of surface treated MILC poly-Si TFTs and normal MILC TFT.

Generally, the electrical performance and reliability of TFTs can be easily degraded in high electrical stress. High stress causes a threshold voltage shift and a decrease in the

driving current. The main mechanisms of high electrical stress are hot carrier stress for self-heating, which are attributed to the metastable creation of the trap states at the interface and charge trapping to the deep-state level [3.29-3.33]. Therefore, to identify the reliability enhancement in the surface treatment, high stress (V_G = -15V, V_D = -20V) was applied at room temperature. As identified from Fig 3.4, electrical characteristic degradation was highly related to properties like strength and quantity of bonding shown in XPS analysis. The normal MILC TFT undergoes breakdown after 10^4 seconds, because high trap density induces large amount of P-F tunneling current. In the case of wet oxidation, a high amount of intermediate oxidation bonding, which is a weak and unstable bonding rather than that of stoichiometric silicon oxide, can be easily broken by high stress. They show enhanced electrical performance in the transfer curve, while more characteristic degradation was revealed under high electrical stress as a result of breaking large amount of intermediate oxidation states of Si atoms, and the variations of threshold voltage and driving current of each sample were similar. However, since N_2O plasma exhibits slight variation in subthreshold slope and driving current, which results in a better trap density property at the interface and grain-boundary.

3.1.3 Conclusion

The MILC poly-Si TFTs manufactured with surface treatments exhibited superior carrier mobility, lower subthreshold slope, and a higher on/off current ratio with the reduction of the interface and grain-boundary trap-density to represent characteristics and reliability improvement. Every surface treatment methods exhibited electrical

characteristic enhancement, although some degree of difference was revealed by XPS analysis. Wet oxidation shows good electrical characteristic enhancement, while the intermediate oxidation state was easily degraded under high stress. Among the various surface treatment methods, N_2O plasma was the most effective shown from in electrical characteristic and reliability among various surface treatment methods. The MILC poly-Si TFT fabricated with N_2O plasma showed excellent electrical performance by stabilizing poly-Si surface and reducing strain, charge traps. Therefore, the surface treatment using N_2O plasma is recommended for the device fabrication.

CHAPTER 4

Application of Extra Low Amount of Nickel to the Metal-Induced Lateral Crystallization Thin-Film Transistors

4.1 Application of Extra Low Amount of Nickel to the Metal-Induced Lateral Crystallization Thin-Film Transistors

Low-temperature polycrystalline silicon (LTPS) thin-film transistors (TFTs) are an attractive technology for the realization of a wide range of micro- and nano-scale electronic applications, because they can be integrated in the peripheral circuits on a glass substrate showing high electrical properties. [4.1, 4.2] Among the many types of LTPS techniques, metal-induced lateral crystallization (MILC) comprises many advantages including a low cost batch process, smoother surface, higher degree of crystalline uniformity, etc [4.3-4.5]. Although it is capable of outstanding characteristics, the MILC requires additional equipment, like a sputtering or ion-implantation system, resulting in a high process complexity; furthermore, the equipment could cause plasma radiation damage on the deposition layer. Several of the previous researches on the Ni-mediated LTPS process involved the use of

solutions instead of deposition of Ni on amorphous Si (a-Si). However, the focus of those studies is the crystallization method for which a Ni solution is used as a precursor, while the lateral-crystallization process for which a solution is used has not been reported yet. [4.6, 4.7] Since the metal-induced crystallization (MIC) leads to a vertical grain growth, the grain size is small and numerous defects are generated at the boundaries of the small and high density grains. Thus, it is difficult to expect that the quality of the MIC poly-Si will be better than that of the lateral crystallization method. [4.3] Although capable of the high quality, the MILC poly-Si also suffers from the Ni contamination after crystallization. The Ni silicide ($NiSi_2$) defect that remain after the crystallization induces high leakage currents from trapped carriers of the poly-Si TFTs, including the thermionic emission that is due to a thermal excitation and a Poole-Frankel emissive tunneling current through the potential barrier. [4.8-4.10] For this study, a method for a solution-processed MILC (SMILC) process was developed. The solution-based spin-coating process provided a low-cost and simplified fabrication on a large-area glass substrate for the LTPS. Moreover, the SMILC could enhance the quality of the poly-Si by reducing the concentration of the Ni silicide residues, acting as a catalyst of crystallization, through controlling the preannealing reaction time. It was advantageous not only for the reduction of the Ni silicide defects, but also the decrease of the large Ni silicide amount that could affect the morphology of grains. Therefore, high quality poly-Si with long and stretched grain and a low Ni concentration level was obtained, and the TFTs that were fabricated using the SMILC process showed high electrical characteristics.

4.1.1 Experiment

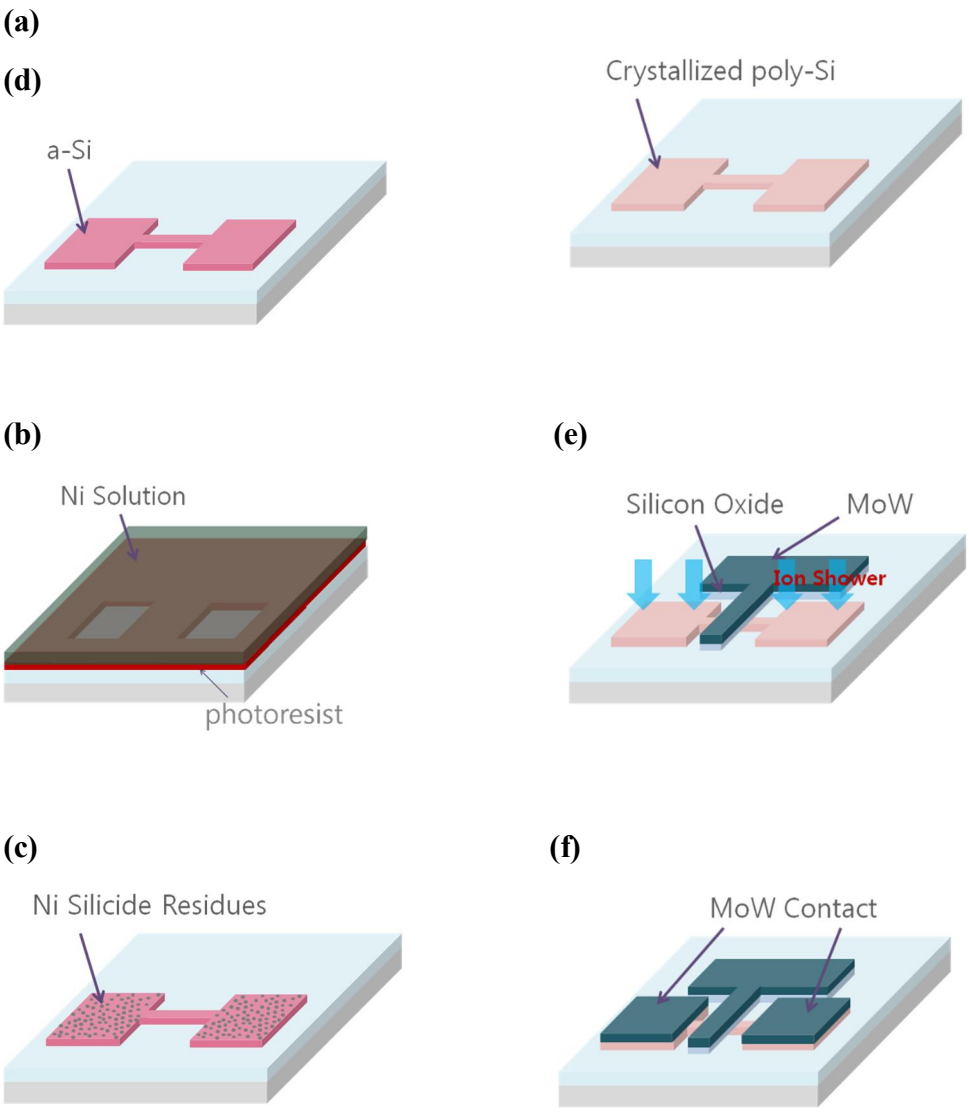


Figure 4.1. Schematic fabrication process flow of the SMILC TFT.

The schematic fabrication process of the SMILC poly-Si TFT is shown in Fig 4.1. The fabrication was commenced with a 2000-Å-thick silicon oxide buffer-layer deposition on the Corning Eagle XG glass substrate, and this was followed by the deposition and patterning of a 700-Å-thick a-Si into an active layer. The photoresist was then coated and developed, leaving only the source/drain regions to react with the Ni solution. The high viscosity of Ni solution was prepared from 180g of nickel(II) nitrate hexahydrate ($Ni(NO_3)_2 \cdot 6H_2O$) that was obtained by a dissolution of Ni in 60% of nitric acid (HNO_3), followed by a drying, and then a dissolution in 30ml of deionized water at 70°C. The solution was spin-coated at the speed of 300 rpm on the photoresist-patterned active layer, and the thick solution could be coated effectively on the hydrophobic Si surface. The initial stage of the interfacial reaction between the a-Si and the Ni solution was examined using Fourier transform infrared (FT-IR) spectroscopy, as shown in Fig 4.2.

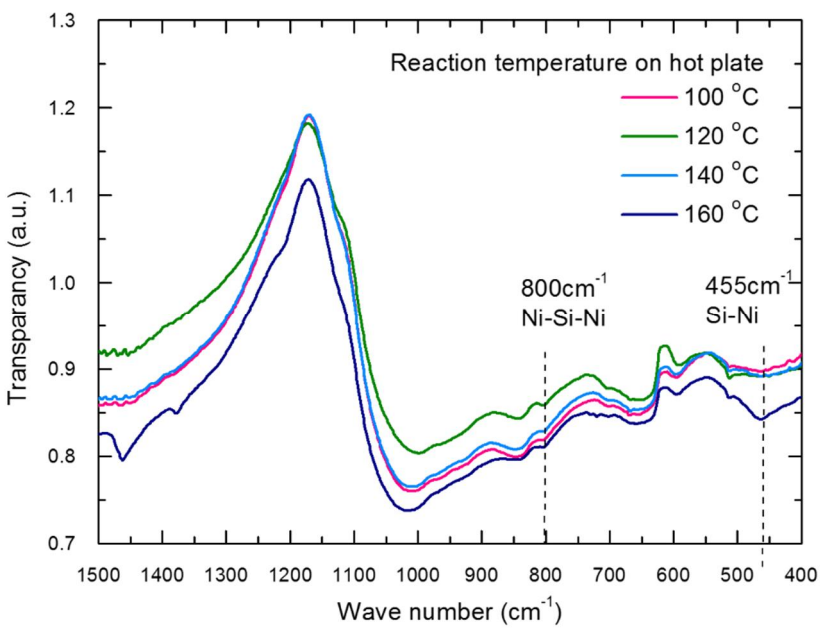
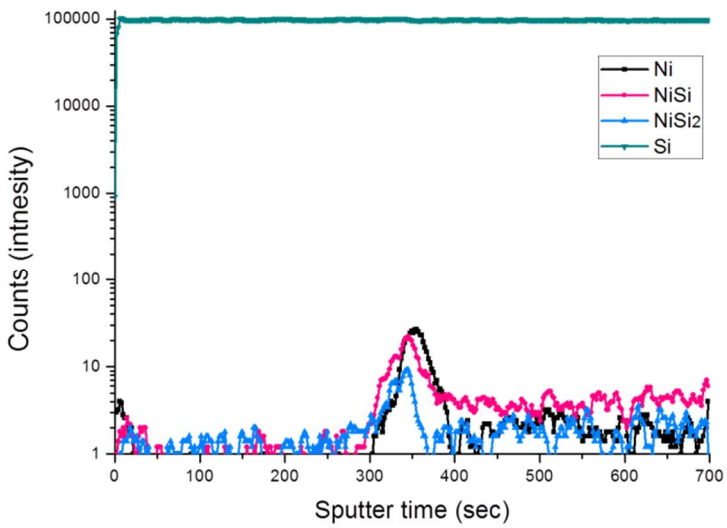


Figure 4.2. Fourier transform infrared (FT-IR) patterns for the Ni solution that was preannealed for 1min on a-Si samples at the different respective temperature of 100°C, 120 °C, 140 °C, and 160°C.

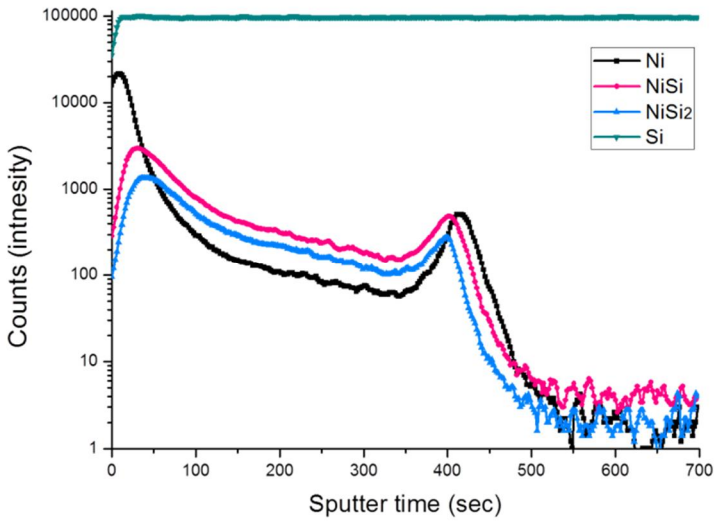
Each sample was heat-treated with the coated Ni solution on a hot plate from 100-160°C with 20°C intervals for 1min. The Si-O and Ni-Si-Ni bonds appeared at over every 100°C temperature conditions, but a low concentration of Ni-Si-Ni bonds does not affect the lateral growth of the nickel silide seeds. The initial reaction for the Ni-Si bond, the available precursor for the MILC mechanism, is located at 450 cm^{-1}, and its generation began at approximately 160 °C. Then, the preannealing was carried out on a hot-plate at 180°C to produce the compounds of Ni and a-Si in a short time frame. The sample was cleaned with the photoresist stripper for 10min using sonication and was then rinsed in de-ionized water. After that, only the Ni-Si compounds remained on the source/drain surface. Then, the SMILC poly-Si was annealed at 550 °C in a vacuum furnace for 2 hr. The Ni-Si compound was transformed to the $NiSi_2$ that triggers the lateral growth of poly-Si as a catalyst. After the fabrication of the SMILC poly-Si, a 700-Å-thick silicon oxide and a 2000-Å-thick $Mo_{0.9}W_{0.1}$ were deposited sequentially. The $Mo_{0.9}W_{0.1}$ was etched in an aluminum etchant (H_3PO_4+ CH_3COOH + H_2O) using a gate mask and the silicon oxide was dry-etched in a reactive ion-etching system. Then, the boron was doped using an ion-shower system with a diborane (B_2H_6) source gas diluted with 80% of hydrogen (H_2) gas. Finally, the dopant activation and hydrogen passivation were carried out simultaneously in 550 °C of hydrogen ambient for 2 hr. Conventional MILC TFTs were also fabricated for a comparison, and the electrical properties of the TFTs were measured by Agilent System.

4.1.2 Result & Discussion

(a)



(b)


Counts (intnesity)
Sputter time (sec)
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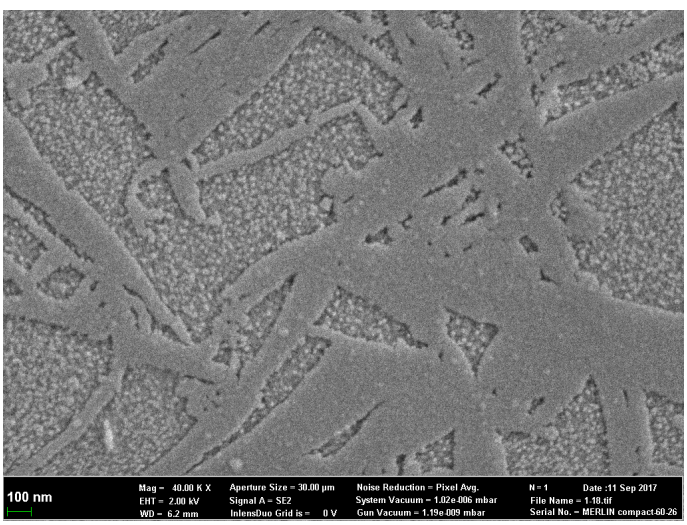
NiSi
NiSi2
Si
100000
10000
1000
100
10
1
0
100
200
300
400
500
600
700

(c)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EHT = 2.00 kV
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(d)

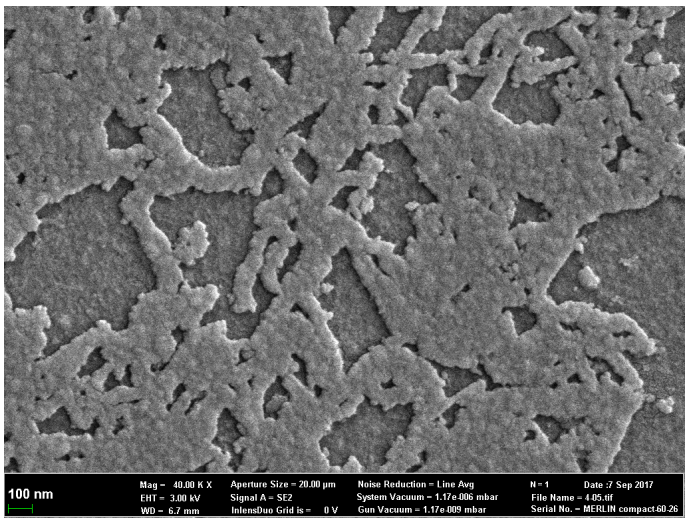
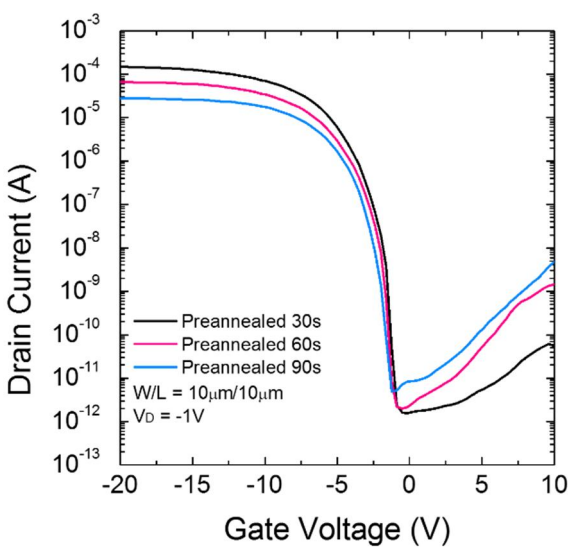


Figure 4.3. SIMS depth profiles for concentration of Si, Ni, and Ni silicide in (a) SMILC and (b) MILC poly-Si thin-film. SEM micrographs for grain growth of (c) SMILC and (d) MILC poly-Si after Secco etchant treatment.

The concentration variations of Ni, Si atoms, and their compounds in the solution-processed MIC and MIC poly-Si region were investigated with the secondary ion mass spectroscopy (SIMS) as shown in Fig 4.3 (a), (b). The concentrations of Ni atom and Ni-Si compounds in the SMIC poly-Si was greatly lower than that of the MIC poly-Si across the sputtered thickness of 700 Å. Moreover, the SMIC poly-Si denotes approximately 1000 times lower amounts of the Ni and Ni silicide than the MIC poly-Si at the surface where the carrier mainly moves. It shows that the chemical reaction using the solution process was advantageous for reacting a low amount of Ni uniformly with Si rather than using the deposition process. Fig 4.3 (c) and (d) show the micrographs of scanning electron microscope (SEM) for the longitudinal grains at the border of poly-Si growth that was fabricated using the SMILC and MILC methods, respectively. In comparison, the individual crystalline-Si grains of the SMILC poly-Si

revealed long and stretched morphology, while the grains of conventional MILC poly-Si was small and had many curves. This phenomenon is thought to be caused by the MILC process with the small amount of Ni contents. The lateral growth is mediated by the Ni silicide that acts as the nuclei due to the lattice mismatch between the crystallized Si and $NiSi_2$. Various forms of the Ni-Si compounds are transformed into $NiSi_2$, and the nucleation takes place at the above 500°C annealing condition. Then, from the nuclei, needle-shaped crystalline-Si grains proceed toward the a-Si region with the migration of the $NiSi_2$ at the front that leaves the crystalline-Si behind the trace. When the in-progress $NiSi_2$ collides with the already crystallized Si grains, the progress is stopped and the $NiSi_2$ silicide becomes trapped at the boundary of the grains. [4.5, 4.11]

(a)



(b)

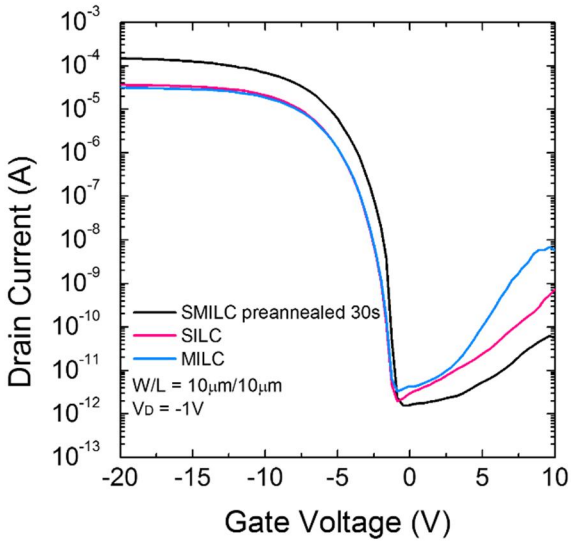


Figure 4.4. (a) Comparison of the transfer characteristics of SMILC TFTs for the different preannealing times after the solution was coated on the source/drain region. (b) Transfer characteristics of the poly-Si TFTs fabricated by SMILC, MILC, and SILC process.

	SMILC preannealed: 30s	**SMILC preannealed: 60s**	**SMILC preannealed: 90s**	**SILC**	**MILC**
V_{TH} (V)	-2.8	-3.0	-3.3	-3.5	-3.5
Subthreshold Slope (V/dec)	0.20	0.20	0.20	0.26	0.27
Field Effect Mobility (cm^2/Vs)	274.1	128.1	68.96	101.4	93.18
On-State Current (10^{-5}A)	14.8	6.65	2.80	3.61	3.15
Off-State Current (10^{-12}A)	1.55	2.00	4.90	2.81	3.75

Table 4.1. Device parameters of the TFTs using solution-processed MILC and conventional MILC methods.

From the lateral-crystallization mechanism, it can be inferred that the MILC poly-Si with the low concentration of crystallization site could produce long and stretched grains without the occurrence of an intergranular collision that is generated by the growth of numerous grains. As the concentration of Ni and Ni silicide in the SMILC poly-Si was drastically lower than that of the MILC poly-Si as shown in SIMS profile, the poly-Si with high quality crystalline grains could be grown without collisions of grains in the SMILC process. Using SMILC poly-Si, coplanar structured TFTs of 10μm channel width and 10μm channel length were fabricated. The measurement was in the gate-bias range from 10V to -15V at a drain bias of -1V. Fig 4.4 (a) shows the transfer characteristics of the SMILC TFTs that were fabricated from different preannealing times after the solution was coated on the source/drain region. The TFTs revealed outstanding performance, showing a low subthreshold slope, a high on/off current ratio. In comparison, the characteristics of TFTs improved as the reaction time of the Ni solution and the a-Si becomes shorter. This is thought to be the difference in preannealing time affects the density of Ni silicide on the a-Si surface which cause changes in microstructural quality of the poly-Si active layer such as the morphology of grains and the Ni silicide defect level.

In Fig 4.4 (b), the electrical performance of the SMILC poly-Si TFT is compared with that of the conventional MILC poly-Si TFTs, using the MILC and the seed-induced lateral crystallization (SILC) processes. [4.12] Also, the key device parameters of the TFTs are summarized in Table I. The field-effect mobility was extracted from maximum value of linear transconductance (*gm*) by the following equation at drain voltage of -0.1V. In case of the MILC and SILC poly-Si TFTs, they showed only a slight difference in the off-state current. That is result from the relative trap density level generated from Ni silicide defects in the poly-Si, while the density is not large

enough to affect the morphology of grains. However, in comparison with the SMILC, the driving characteristics of the SMILC TFT is significantly high, and the off-state current is low. The electrical property of TFTs mainly depends on the microstructural quality of its active layer, such as the size, and texture of the grains, and the intragrain microdefects. The Ni silicide defects present in the grain boundaries that are mainly responsible for the carrier trapping and the formation of the potential barrier results in a scattering of the carriers that interferes with the intragrain carrier movement. [4.13-4.15] Moreover, activation of free carriers from the trap state existing in the forbidden band gap induces high off-state leakage current caused by field-enhanced thermal excitation, field-enhanced tunneling [4.8-4.10]. In this case, the device performance improvements, including the threshold voltage, on-state current, and the field-effect mobility, mainly arise due to the enhanced morphology of the poly-Si active layer as shown in Fig 4.3 which attribute to reduce the carrier mobility scattering. Further, due to low level of Ni contamination in the SMILC poly-Si, the leakage current caused by trapped carrier is also reduced.

4.1.3 Conclusion

The low-cost and simplified fabrication method for an LTPS was investigated using a solution-based process. Moreover, the poly-Si films that were created using the SMILC process showed long grains and low of Ni contamination level. The long grains provided high field-effect mobility for the reduction of the scattering site in the movement of the carriers, and the reduction defect level in the channel area improved off-current and leakage current, which is the main problem of the MILC poly-Si. The fabricated SMILC TFTs showed superior electrical characteristics with a high field-effect mobility, low threshold voltage, low subthreshold slope, and high on/off current

ratio than conventional MILC and SILC TFTs. The SMILC process can be adopted easily on a large area substrate without additional equipment, and the plasma radiation damage on the Si layer that is caused by the sputtering system can be avoided. Therefore, the SMILC represents an inexpensive and efficient alternative for the fabrication of LTPS applications.

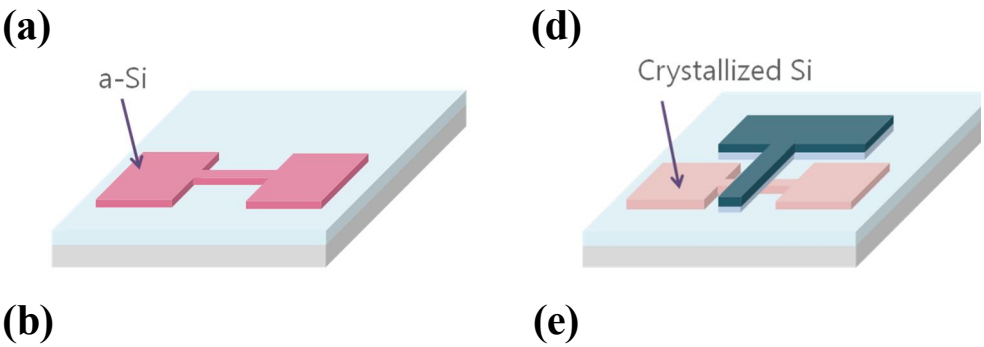
4.2 Two Mask Step Self-Aligned Solution-Processed Metal-Induced Lateral Crystallization Thin-Film Transistors

The simplified fabrication method for LTPS was investigated using a solution-based process. MILC poly-Si has good properties but requires complex and expensive equipment such as sputtering or ion-implantation system. Therefore, a simplified and easy solution method has been studied with the two mask step self-aligned process. The solution process was applied to self-aligned TFT structure because of the low Ni contamination. The solution was made differently according to the concentration of Ni ion, and TFT characteristics were changed according to the concentration of the

solution. High-quality TFT could be fabricated with a solution of low nickel content, and it was confirmed that the MILC TFT can be fabricated with a simplified two-step mask process using the solution.

4.2.1 Experiment

The schematic fabrication process of the two mask step self-aligned SMILC poly-Si TFT is shown in Fig 4.5. At first, a 2000-Å-thick silicon oxide buffer-layer was deposited on the glass substrate. A 700-Å-thick a-Si was deposited and patterned into an active layer. After that, a 700-Å-thick silicon oxide and a 2000-Å-thick $Mo_{0.9}W_{0.1}$ were deposited sequentially without crystallization process. The $Mo_{0.9}W_{0.1}$ was etched in an aluminum etchant and the silicon oxide was dry etched in a reactive ion etching system. Each sample was heated at 150 °C on a hot plate, and then sprayed with 0.2 ml of Ni ion solution uniformly. The concentrations of the solution were prepared from 10^{-2} M, 10^{-3} M, 10^{-4} M, 10^{-5} M of nickel(II) nitrate hexahydrate ($Ni(NO_3)_2 \cdot 6H_2O$) dissolved in deionized water.



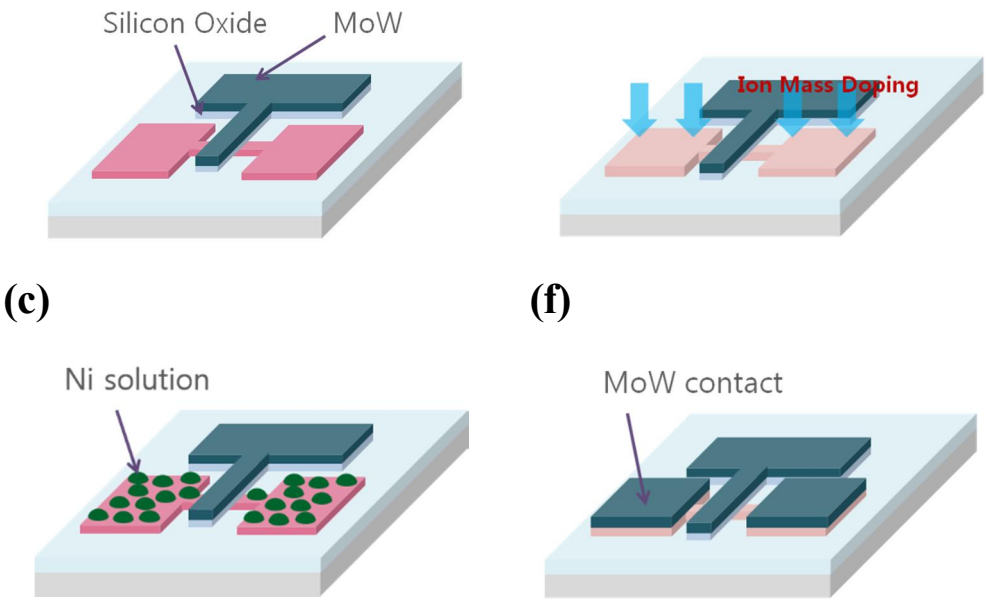


Figure 4.5. Fabrication steps for two-mask process self-aligned SMILC TFT.

As the sample was entirely sprayed by Ni ion solution, the solution comes into contact with the entire region of the TFTs. Then, the heat process at 550 ºC was carried out in a vacuum furnace for MILC crystallization process. Then, the boron was doped in the source/drain region using an ion-shower system to make p-type TFT. Finally, the hydrogen passivation and dopant activation were performed in 550 ºC of hydrogen ambient furnace for 2 hr. Conventional self-aligned MILC TFTs were also fabricated for a comparison.

4.2.2 Result & Discussion

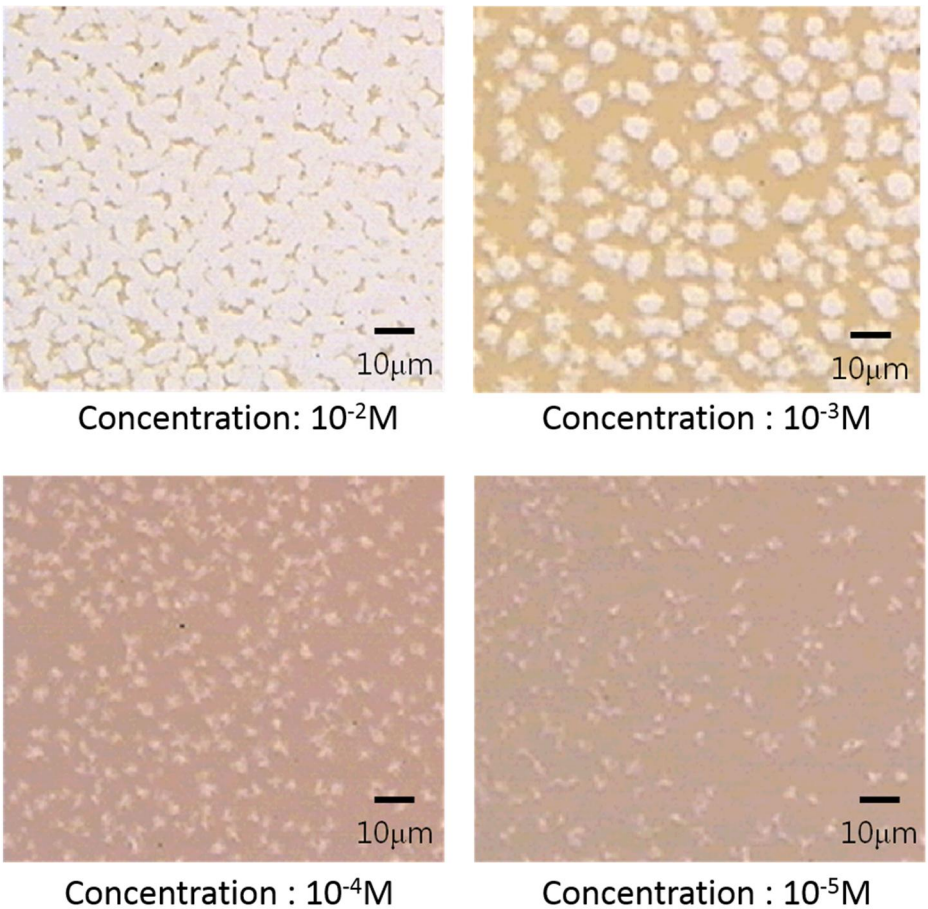
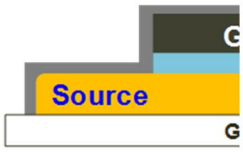


Figure 4.6. Optical microscope images of partially crystallized a-Si surface after 30min 550°C heat process in vacuum furnace.

Figure 4.6 shows the optical-microscopy images of the partially crystallized area on the a-Si after a 30 min heat treatment in a vacuum furnace at 550 °C. The difference in the concentration of Ni ion generates the degree of density for Ni silicide seeds on the a-Si surface. Since the lateral growth begins with the formation of the nuclei of Ni silicide, it denotes that the short range of crystallization occurs from Ni silicide seeds,

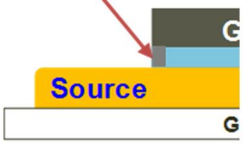
(a)

Prepare

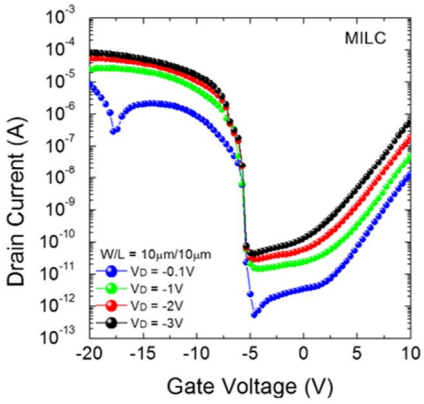


Ni Dep

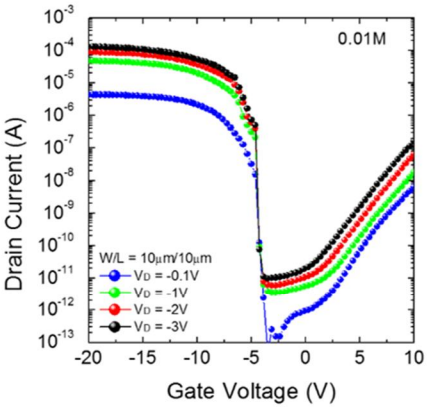
Ni contamina



After Cry



(b)



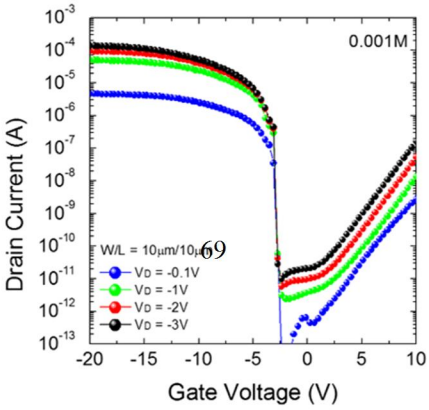


Figure 4.7. (a) Schematic images of self-aligned MILC process. (b) Comparison of transfer characteristics of the SAMILC and SASMILC TFTs.

Self-Aligned TFTs	MILC	0.01M	0.001M
V_{TH} (V)	-6.2	-3.1	-3.0
Subthreshold Slope (V/dec)	0.224	0.156	0.155
Field Effect Mobility (cm^2/Vs)	74.093	116.278	118.997
On-State Current (10^{-5}A)	-2.50	-4.89	-5.05
Off-State Current (10^{-12}A)	-14.8	-4.00	-2.45

Table 4.2. Key parameters extracted from the transfer curves.

and the low density of the crystallized poly-Si from the nuclei becomes evident as the Ni ion concentration in solution becomes shorter. Although solution of low concentration could result in a low level of Ni contamination, it increases the annealing time for the crystallization. For instance, solution-processed MILC poly-Si using under 10^{-4} M of solution consumes 3 hr of annealing time for a 15μm length of crystallized active layer, and it could not fabricate fully crystallized MILC poly-Si. In Fig 4.7 (b), the transfer characteristics of the self-aligned MILC and SMILC poly-Si TFTs are compared. Also, the extracted and estimated parameters of the TFTs are plotted in Table I. The proposed TFTs fabricated under the same conditions, except for the nickel content, showed good characteristics, but showed especially a large shift of the threshold voltage. The reason for the large shift of the threshold voltage is due to the structural characteristics of the self-aligned MILC TFT. As shown in Fig 4.7 (a), the self-aligned structure is exposed not only to the active layer but also to the gate and the dielectric at the same time. Therefore, contaminations occur in the dielectric, and it affects the properties of the dielectric from generating fixed charges. It can be seen that the contamination level of the solution process is smaller than that of the conventional MILC process and thus the threshold voltage shift is small. In addition, this measurement shows that the improvement of the driving characteristic and the off current induced by the decrease of the Ni content.

4.2.3 Conclusion

In conclusion, the two mask step self-aligned MILC TFTs were successfully fabricated and compared with conventional self-aligned MILC TFT. It is confirmed that the properties of TFT improved as the concentration of the Ni ion solution become reduced and the limit of the concentration of the Ni ion solution for MILC process to fabricate the fully crystallized poly-Si was 0.001M. The solution process was more advantageous than the conventional MILC process showing a lower threshold voltage shift.

CHAPTER 5

Conclusion

5.1 Summary of Results

In this thesis, novel approaches for fabrication of TFT were studied to meet the demand of evolving display. MILC is an attractive process to fabricate poly-Si for higher resolution, wider panel area, and higher performance display. Compared to ELA, which is the most widely used but difficult to apply to large area, and SPC, which causes high thermal damage on the substrate, MILC has outstanding characteristics to be applied to next generation displays because it has advantages in field-effect mobility, uniformity in crystallization, grain size, thermal damage on device, and large area process. The proposed experiments using MILC process have been effectively applied by maximizing the merits of MILC and complementing its drawbacks.

Due to the need for the continuously increasing panel area, higher resolution, and higher performance, high-frequency addressing is required in display. Therefore, it becomes significant issue to reduce the RC propagation delay and usage of low resistance material for interconnect line is demanded. Thus, the thick planarized

copper gate MILC thin film transistor, which can manufacture the gate and interconnection line in a single process, was fabricated. This attributes to simplify interconnection and transistor fabrication processes with high performance device. The planarized copper gate could structurally alleviate the drawbacks of copper and enhanced stability to adapt in TFTs. Moreover, the surface of copper was systematically investigated by electroplating process involving leveling additives such as thiourea and chloride in acidic sulphate-plating baths to improve surface morphology and ensure a smoother surface of the copper gate. The surface morphology influenced the electrical property of poly-Si TFT by also reducing the surface roughness scattering effect. As the gate surface morphology was enhanced, the device exhibited superior electrical characteristics in driving characteristics such as field-effect mobility, on/off current ratio, and subthreshold slope. Moreover, through structural modification, leakage current of the planarized copper gate transistor was effectively suppressed. A novel inverted staggered MILC poly-Si thin-film transistors TFTs with a combination of a planarized gate and an overlap/ off-set at the source-gate/ drain-gate structure were fabricated and characterized. While the MILC process is advantageous for fabricating inverted staggered poly-Si TFTs, MILC TFTs reveal higher leakage current than TFTs crystallized by other processes due to their high trap density of Ni contamination. Due to this drawback, the planarized gate and overlap/ off-set structure were applied to inverted staggered MILC TFTs. The proposed device shows drastic suppression of leakage current and pinning phenomenon by reducing the lateral electric field and the space-charge limited current from the gate to the drain.

A method for enhanced electrical characteristics of MILC TFTs have been devised by improving the interface between poly-Si and gate insulator. The MILC process exposes problems due to defect inherent in the poly-Si and the MILC poly-Si TFTs

using Si_3N_4 as a gate dielectric shows high grain-boundary and interface trap-density with the MILC poly-Si film. In order to reduce this problem, passivation have been carried out to stabilize the interface of the MILC poly-Si through oxide passivation to obtain high driving characteristics. The MILC poly-Si TFT was successfully fabricated showing high performance and excellent reliability with various surface treatments. Several surface treatment techniques, including oxidizing silicon surface with HNO_3, H_2SO_4, and HCl, as well as N_2O plasma treatment, were investigated. Acids have a surface cleaning effect of removing the heavy metals at the same time of forming the SiO_2 on the surface of the poly-Si. Comparing the characteristics of the proposed MILC poly-Si TFTs, the N_2O plasma treated was the most effective, showing superior electrical performance and reliability to the other surface treatment methods. The role of the N_2O plasma is to insert nitrogen into the poly-Si surface, which causes a relaxation and passivation of the trap states by producing Si≡N strong bonds, while the surface treatments using acids simply oxidize Si atoms. Due to N_2O plasma process, stabilized MILC poly-Si could be obtained and the TFT shows enhanced electrical properties.

The simplified fabrication process for reducing extra amount of nickel for MILC poly-Si was investigated using a nickel (II) nitrate hexahydrate ($Ni(NO_3)_2 \cdot 6H_2O$) solution. The nickel-silicon compounds were formed on the source/drain region of the TFT devices by the preannealing of a spin-coated solution on a-Si at 180°C. The a-Si channel was laterally crystallized from the source/drain area by the low concentration of Ni silicide that was used as a catalytic component for the MILC at 550°C. By controlling the reaction time for generating the Ni silicide, the Ni contamination level in poly-Si could be reduced, and it affected the formation of long and stretched grains. The fabricated TFTs showed superior electrical characteristics such as a high field-

effect mobility, threshold voltage, subthreshold slope, on-off current ratio, and low leakage current compared with the TFTs that were fabricated by the conventional MILC methods. Moreover, SMILC poly-Si TFT could be fabricated only by simplified two steps of mask process. By using a solution with a low nickel content, V_{TH} shift can be prevented and the self-aligned SMILC TFT has characteristics comparable to those of a conventional MILC process.

Therefore, in this thesis, various approaches for the fabrication of high performance poly-Si TFTs using MILC process have been studied, and they will be possible to be a new alternative for LTPS technology.

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요약(국문초록)

고성능 다결정 실리콘 박막 트랜지스터의 제작에 관한 연구

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유리 기판 위에 비정질 실리콘을 증착하여 제작한 박막 트랜지스터의 집적 기술이 개발됨에 따라 능동형 액정표시장치가 등장하게 되었고, 2000 년대 이후 액정 표시장치는 플라즈마 디스플레이 패널과 함께 디스플레이 시장을 점유하며 음극선관 디스플레이를 대체하기 시작하였다. 이후, 높은 소비 전력의 플라즈마 디스플레이 패널은 소비가 점차 줄어들기 시작하였고, 액정표시장치는 널리 보급되어 많은 전자기기에 필수적인 요소가 되었다. 하지만 최근 액정 표시장치보다 높은 색 구현도, 넓은 시야각, 낮은 소비 전력의 능동형 유기 발광 디스플레이의 개발로 인해 디스플레이 산업은 과도기를 맞이하고 있다. 능동형 디스플레이의 광원은 픽셀 내부 회로에 구성되어 있는 박막 트랜지스터로 구동되기 때문에 박막 트랜지스터의 특성은 디스플레이의 성능을 좌우하게 된다. 특히 유기 발광 디스플레이는 전압 구동 방식의 액정 표시장치와는 다르게 전류 구동 방식 트랜지스터의 사용으로 높은 전계 이동도를 요구한다. 따라서 낮은 전계 이동도와 신뢰성의 한계를 갖는 비정질 실리콘을 대체할 활성층 물질에 대한 연구가 절실해졌다. 다결정 실리콘은 이에 가장 적합한 물질로서, 고체상 변형법, 레이저 결정화법, 금속 유도

측면 결정화법 등의 다결정 실리콘을 제작하기 위한 다양한 저온 결정화 방식이 연구되었다. 많은 결정화 방식 중에서 금속 유도 측면 결정화법은 전계 이동도, 결정화도, 결정립의 크기, 소자의 열적 손상, 그리고 대면적 디스플레이의 제작에 이점을 갖고 있어 차세대 디스플레이 제작을 위한 저온 다결정 실리콘 기술로 주목받고 있다. 또한 디스플레이는 유기 발광 디스플레이를 기반으로 더 높은 해상도, 넓은 패널 면적, 그리고 3 차원 디스플레이와 같은 고성능 디스플레이를 지향하며 발전하고 있다. 따라서 본 연구에서는 차세대 디스플레이에 적용 가능한 금속 유도 측면 결정화법을 통하여 높은 성능의 다결정 실리콘 박막 트랜지스터의 개발을 중점으로 연구가 진행되었고, 그 결과 다음과 같은 연구들이 진행되었다.

첫번째 연구에서는 배선의 RC 전달 지연을 줄이기 위해서 낮은 저항을 갖는 구리 배선에 금속 유도 측면 결정화 다결정 실리콘 박막 트랜지스터를 적용하는 연구가 수행되었다. 디스플레이 패널의 면적이 증가할수록 능동형 패널 배선에 고주파 전달이 요구됨에 따라 상호 연결 라인의 전기적 저항에 의한 RC 전달 지연을 줄이는 것이 중요한 문제가 되었다. 도랑형 구조를 이용한 평탄화된 구리 게이트는 빠른 전기적 신호 전달을 위한 배선을 제작할 수 있었고, 이 배선 구조와 함께 제작한 금속 유도 측면 결정화 다결정 실리콘 박막 트랜지스터는 소자 내에서 유리 기판과의 접착력 문제, 표면 산화, 빠른 확산, 식각 문제를 해결할 수 있었다. 또한 저농도로 도핑된 드레인을 적용하기 어려운 하부 게이트 구조 박막 트랜지스터에서 평탄화된 게이트와 드레인 오프셋을 이용한 구조의 변형을 적용하여 누설 전류를 억제하는 효과를 확인하였다. 이는 소스와 드레인 사이에 인가되는 전기장을 감소시키고 게이트와 드레인 영역 사이에 발생하는 게이트 누설 전류 또한 효과적으로 감소시키기 때문인 것을 확인하였다.

두번째 연구는 고성능 박막 트랜지스터 제작을 위해 금속 유도 측면 결정화법으로 제작된 다결정 실리콘과 게이트 유전층 사이의 계면을 패시베이션하여 결함들을 감소시키는 표면처리법을 연구하였다. 표면처리에는 실리콘 표면을 산소로 패시베이션 할 수 있는 방법들이 사용되었다. 강산은 다결정 실리콘의 표면에 산화막을 형성하는 동시에 중금속을 제거하는 표면 세정 효과를 나타냈다. 아산화질소 플라즈마는 산질화막을 형성함으로써 결함들을 감소시키고, 계면을 안정화시켰다. 이 중에서 아산화질소 플라즈마 처리는 표면 처리 방법 중 다결정 실리콘은 박막 트랜지스터로 제작하였을 경우, 전기적 특성 및 신뢰성 면에서 가장 우수한 성능을 나타내었고 그 효과를 입증하였다.

세번째 연구는 저농도의 니켈 함량을 갖는 금속 유도 측면 결정화 다결정 실리콘 제작에 관한 연구로서, 용액 기반 공정의 적용에 대해 연구하였다. 용액 공정을 통하여 기존의 금속 유도 측면 결정화 다결정 실리콘이 갖는 니켈 오염 문제를 크게 줄일 수 있었다. 용액 공정 금속 유도 측면 결정화 다결정 실리콘은 길게 뻗은 결정립으로부터 높은 전계 효과 이동도를 나타내며, 채널 영역의 낮은 결함의 농도로 인해 누설 전류의 큰 감소 효과를 보였다. 또 낮은 니켈 농도의 금속 유도 측면 결정화 다결정 실리콘을 제작할 수 있는 용액 공정의 장점을 이용하여, 단순화된 두 단계의 마스크 공정만으로 다결정 실리콘 박막 트랜지스터 제작이 가능하였다. 이 박막 트랜지스터는 낮은 농도의 니켈 용액 공정을 이용하여 문턱 전압의 이동을 방지 할 수 있으며, 기존 금속 유도 측면 결정화 다결정 실리콘 공정의 박막 트랜지스터만큼의 성능을 이끌어낼 수 있었다.

따라서 본 연구에서는 금속 유도 측면 결정화법을 이용한 고성능 다결정 실리콘 박막 트랜지스터 제작에 관한 실험들이 진행되었고, 이는 현재

생산 기술의 한계를 넘어 차세대 디스플레이 제작을 가능하게 할 것으로 생각된다.

Keywords: 능동형 유기 발광 다이오드, 저온 다결정 실리콘, 금속 유도 측면 결정화, 박막 트랜지스터, 구리 배선, 누설 전류, 계면 패시베이션, 용액 공정, 다결정 실리콘 결정립

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