Ph.D. DISSERTATION

Homoepitaxial growth on on-axis 4H-SiC substrate using BTMSM source

by

Hyunwoo Kim

February 2018

DEPARTMENT OF MATERIALS SCIENCE AND ENGINEERING
COLLEGE OF ENGINEERING
SEOUL NATIONAL UNIVERSITY

ABSTRACT

Silicon Carbide (SiC) is a wide bandgap semiconductor with high melting point, large breakdown field, high thermal conductivity and high saturation electron mobility, and is being studied as a next generation semiconductor material to replace Si. SiC power devices are expected to be very powerful when applied to industrial transportation systems such as aerospace systems, electric vehicles, or next generation power plants due to their superior characteristics. However, this positive effect of applying SiC can only be expected when a SiC device is successfully fabricated. For this, epitaxial growth, which is an essential process in device fabrication, is very important. The performance of the SiC device depends largely on the quality of the epitaxial layer, so that the productivity, reproducibility and quality of the epitaxial layer have a great influence on the improvement of the device. For growth of high quality SiC epitaxial layers, many techniques such as molecular-beam epitaxy (MBE), liquid-phase epitaxy (LPE), and vapor-phase epitaxy (VPE) have been tried but problems to be solved are still remained. To solve this problem, the author focuses on the homoepitaxial growth of a 4H-SiC epilayer by metal-organic chemical vapor deposition (MOCVD) using bis-trimethylsilylmethane (BTMSM, $C_7H_{20}Si_2$).

Currently, for enhancing the polytype stability of SiC homoepitaxy, an off-axis substrate with several degrees off-cut toward the $[11\bar{2}0]$ direction is commonly used. However, even though the polytype stability is enhanced in this case, other numerous issues still exist. First, the basal plane dislocations (BPDs) are transferred into the epilayer from the substrate. BPDs are known

as “killer defects,” which, when present within the epilayer, largely degrade the forward voltage of the bipolar device. Second, the number of wafers obtained decreases when the substrate is cut along the off-cut direction in the SiC ingot. In order to solve these issues, it is essential to study epitaxy on on-axis substrates. However, because of the low step density on on-axis substrates, there is a possibility of creating unintended polytypes on epitaxial layers. In this study, we investigated the etching characteristics of Si-face and C-face on-axis substrates and report on the effect of these characteristics on the polytype stability of the epilayer grown using bis(trimethylsilyl)methane (BTMSM) source with a high C/Si ratio of 3.5. By understanding the correlation between the etching characteristics and the epilayer qualilty, we controlled the micro-steps of the etched substrates and improved the polytype stability of 4H-SiC up to 99% for Si-face. And we also discussed how to increase polytype stability at C-face by considering factors that affect polytype stability of on-axis epitaxial growth of SiC.

After in-situ H_2 etching of the on-axis substrate, micro-steps generated by selective etching of the threading screw dislocations (TSDs) were observed on the surface of the substrate. The micro-steps formed during etching process enhance 4H stability of the grown epilayer by exposing the stacking sequence of 4H-SiC at the side wall and providing sites for step flow growth. However, the step-bunching phenomenon caused by the high-temperature (above 1500 ℃) etching process partially eliminates the micro-steps and increases the probability of nucleation of 3C-SiC. In order to solve this problem, we increased the etching duration at the low etching temperature, spreading the

micro-steps on the substrate without step-bunching and greatly increased the stability of the 4H-SiC polytype in the epilayer. Improved polytype stability of 4H-SiC up to 99% was finally achieved for Si-face on-axis substrates using BTMSM source.

In case of C-face, it has etching characteristic similar to that of Si-face. Micro-steps were created by selective etching of TSDs and step-bunching phenomenon less occurred at high temperature than Si-face due to low surface energy of C-face. However, the polytype stability of the grown SiC layer on C-face after spreading micro-steps without step-bunching was not improved and was much lower than that of Si-face. This is because high nucleation density of C-face due to the low critical supersaturation ratio. We discussed the factors affecting polytype stability of SiC layer from the viewpoint of competition of step-flow growth and nucleation. In addition, experimental data on silicon carbide epitaxy were considered. By reducing the source flow rate, the stability of the polytype on the C-face on-axis substrate was improved.

Keywords : 4H-SiC, homoepitaxial growth, BTMSM, on-axis epitaxy, polytype stability
Student Number : 2011-23315
Hyunwoo Kim

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Chapter 1. Introduction

1.1 Overview

In recent decades, the semiconductor industry has developed dramatically, and there has been a growing demand for next-generation materials for devices with better performance. While Si-based semiconductor devices are still dominant in market (over 90%) and continue growing, there have been a lot of efforts in the development of compound semiconductor devices for electrical and optical devices, especially in the full range of wavelength, and for electronic devices operating at high frequency, high power, high temperatures, and harsh environments. In most cases, these devices involve growing epitaxial layers by molecular beam Epitaxy (MBE), chemical vapor deposition (CVD), and vapor phase epitaxy (VPE). Among them, the silicon carbide (SiC) is likely candidate to replace Si in the near future due to their superior electrical, mechanical properties which will be discussed in detail in chapter 2. During recent years, great progress has been made in the growth of SiC single crystals and epitaxial films. However, the quality of the grown crystals and epilayer still needs further improvement, because the crystals still contain a number of various structural defects, such as micropipes, dislocations, inclusions, and mosaic structure, etc., of which the formation is strongly related to the key parameters of epitaxial growth process. So, in order to exploit the promising potential of SiC material, first, it

is essential to obtain the high quality epitaxial films with precise doping controls. It has been well known that the heteroepitaxial growth with silicon substrate causes the resulting epilayer to have a high defect level because of the large differences in the crystal lattice constants and the thermal expansion coefficients of Si and 3C-SiC. Therefore, homoepitaxy that, in principle, eliminates the lattice constant and the thermal expansion mismatches is preferable for the structurally perfect epilayer. However, a reduction of the growth temperature, improvement of crystallinity, and precise doping control are still required. To solve these problems, an organo-silicon precursor, bis-trimethylsilylmethane (BTMSM, $C_7H_{20}Si_2$) was used. BTMSM is an organo-silicon source which has a nontoxic and nonflammable nature, thus giving it certain advantages in comparison with the normal process using silane (SiH_4). Moreover, because BTMSM has a Si-C bonding structure, low temperature epitaxial growth is also possible. Another problem to be solved in the homoepitaxial growth of SiC is to reduce the off-cut angle. Unlike heteroepitaxy of 3C-SiC, it is common to use off-axis substrates for homoepitaxy to enhance polytype stability. However, the introduction of off-cut angles has the problem of transferring BPD (Basal Plane Dislocation) from the substrate to the epilayer. These BPDs are known as killer defects which greatly degrade the performance of devices. Also, as the size of the substrate increases, the amount of ingot that is discarded when fabricating the off-axis substrate increases, thereby increasing the cost. To solve this problem, it is necessary to use a substrate with an off-cut angle reduced or an on-axis substrate.

1.2. Dissertation Outline

The literature review and the background of SiC semiconductor material and its applications will be presented in Chapter 2. In Chapter 3, the experimental procedure will be shown. Chapter 4 discusses the results of the 4H-SiC homoepitaxial growth on on-axis substrate using BTMSM for both Si-face and C-face. Finally, chapter 5 presents a brief summary, including the conclusion.

Chapter 2. Literature Review

2.1. Properties of SiC

2.1.1. Phase equilibrium and polytypism

The AFM scan was performed after the removal of thermal oxide layer, as Silicon carbide is the only compound species in the Si-C binary system that exists in the solid state, as shown in Fig. 2.1. [1] However, it is difficult to grow from a stoichiometric melt due to the peritectic nature of the material. The solubility of carbon in molten silicon is very low at temperatures below 2270 K, for example, the solubility is only 0.1% at 2073 K.

Silicon carbide was one of the first semiconductors discovered and its large cohesive energy made people mistake it for an element. SiC is the only known binary compound of silicon and carbon. The basic structural unit of SiC consists of a primarily covalently bonded tetrahedron of four carbon atoms with a silicon atom positioned at the center of mass of the tetragonal structure (or vice versa), as shown in Fig. 2.2. The approximate bond length between the Si-Si or C-C atoms is 3.08 Å whereas the distance between Si and C is approximately 1.89 Å. [2] The SiC crystals are constructed with these tetrahedral joined to each other at the corners. When the same chemical compound exists in two or more crystallographic forms, these forms are called polymorphs and the phenomenon is called polymorphism. In certain close-

packed structures, there exists a special one-dimensional type of polymorphism called polytypism. Polytypes are alike in the two dimension of the close-packed plane but differ in the stacking sequence in the dimension perpendicular to the close-packed plane.

In a polytypic compound, similar sheets of atoms or symmetrical variants are stacked atop each other and related according to a symmetry operator. The differences among the polytypes arise only in the direction perpendicular to the sheets (along the c-axis). In SiC, the sheets can be represented as a close-packed array of spheres forming a two-dimensional pattern with six-fold symmetry. Each sheet represents a bilayer compound of one layer of Si atoms and one layer of C atoms. Using the notations from hexagonal crystal structures, the first sheet can be defined as the basal or c-plane with Miller-indexed directions according to Fig. 2.3. The most stable way to stack an identical second sheet of close-packed spheres is to place the spheres atop the "valleys" in the first sheet. There are two possibilities for arranging the second sheet relative to the first sheet in this way. The second sheet may be displaced along, for example, $[1\bar{1}00]$ until the spheres lie in the valleys denoted "B" in Fig. 2.3, or the sheet may be displaced along, for example, $[1\bar{1}00]$ until the spheres lie in the valleys denoted "C" in Fig. 2.3. Thus, a sheet can be denoted A, B, or C, depending on the positions of its spheres. All polytypes can be described as different stackings of A, B, and C sheets, with the restriction that sheets with the same notation cannot be stacked upon each other. A large number of SiC polytypes exist, with some having stacking sequences of several hundreds of bilayers. The crystal structures of the SiC polytypes are

cubic, hexagonal, or rhombohedral. The only cubic polytype is referred to as β-SiC, whereas the hexagonal and rhombohedral polytypes are referred to collectively as α-SiC. Due to the increasing number of discovered polytypes of α-SiC, it was suggested that each polytype could be named with a number according to the periodicity in the stacking direction and the letter H, for hexagonal, or R, for rhombohedral. [4] Subsequently, it became common to refer to β-SiC as 3C-SiC.

The purely wurtzite ABAB... stacking sequence (with the stacking along the [0001] direction) is denoted as 2H-SiC reflecting its two bilayer stacking periodicity and hexagonal symmetry. Another simple stacking sequence of ABCABC… produces the zincblende 3C structure (with the stacking along the [111] direction), which is the only possible cubic polytype. All of the other polytypes are mixtures of the fundamental zincblende and wurtzite structures. Some common hexagonal polytypes with more complex stacking sequences are 4H- and 6H-SiC. 4H-SiC is composed equally of cubic and hexagonal structures, while 6H-SiC is two thirds cubic. Despite the cubic elements, each has overall hexagonal crystal symmetry. The stacking sequences for 4H and 6H are ABACABAC… and ABCACBABCACB… respectively. Fig. 2.4 illustrates most common polytypes of SiC: 3C, 4H, and 6H.

The extent to which a real crystal structure approximates a close packing can be determined by its lattice constants. Any close packing can be conveniently referred to the hexagonal axes. If c denotes the height of the hexagonal unit cell, n the identity period, and h the separation between successive layers, then c = nh. Simple calculation gives:

$$c/a=nh/a=0.8165\times n \quad \text{(Eq. 2.1)}$$

The axial ratio c/a for an ideally close packed structures must be an integral multiple of 0.8165. However, in the case of α-SiC, the value of c/na deviates from 0.8165 due to the local relaxation as shown in Table 2.1. [10] This difference of the lattice constant can be utilized to identify the polytype of SiC by high resolution X-ray diffraction (HRXRD).

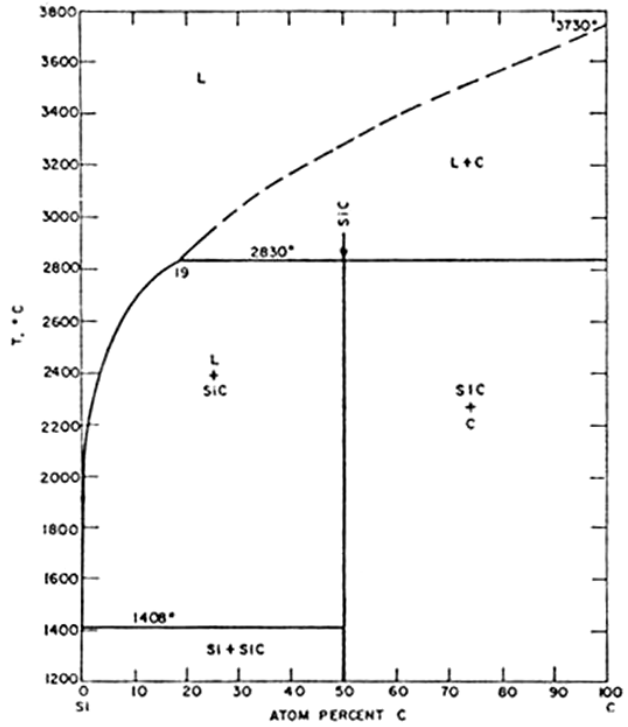

Figure 2.1 Phase diagram of the binary system Si-C. [1]

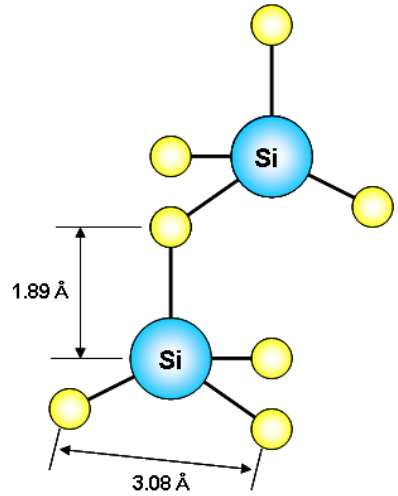

Figure 2.2 The tetragonal bonding of a carbon atom with the four nearest silicon neighbors. The distance a is approximately 3.08 Å. [2]

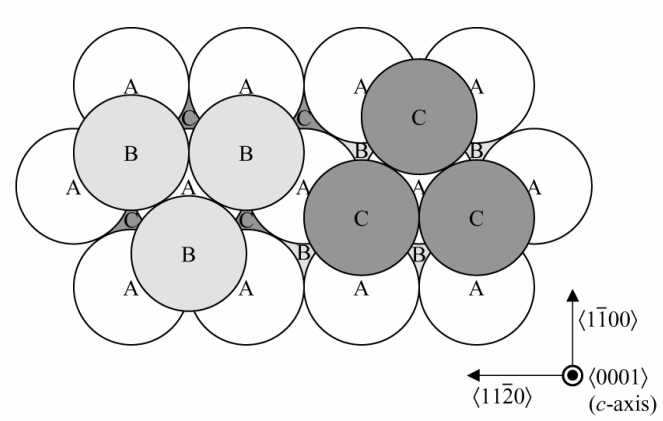

Figure 2.3 The close packing of spheres. There are three possible position for a layer (A, B, and C). [3]

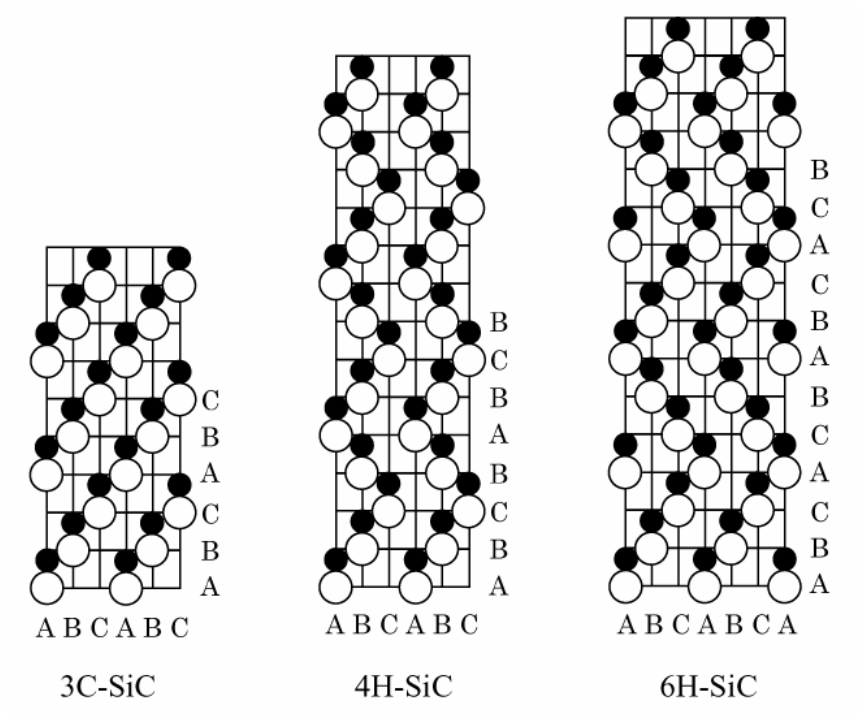

Figure 2.4 Illustration of different polytypes of SiC. Open circle and closed circle represent Si and C atoms, respectively. [3]

Table 2.1 Lattice constants of different SiC polytypes. Theoretical values are taken from [5] or have been calculated recently. [10] Experimental values have been taken from [7] (2H), [8] (3C), and [9] (4H and 6H).

polytype	ref.	a(Å)	c/n (Å)	c/(na)
3C	[5]	3.034	2.477	0.8165
	[6]	3.063	2.501	0.8165
	[8]	3.083	2.517	0.8165
6H	[5]	3.033	2.480	0.8177
	[6]	3.062	2.502	0.8172
	[9]	3.081	2.520	0.8178
4H	[5]	3.032	2.482	0.8185
	[6]	3.061	2.503	0.8179
	[9]	3.081	2.521	0.8184
2H	[5]	3.031	2.480	0.8185
	[6]	3.057	2.508	0.8201
	[7]	3.076	2.524	0.8205

2.1.2. Physical properties of SiC

2.1.2.1. Mechanical properties

SiC has robust mechanical property and chemical stability which are presented in Table 2.2. [11] Its favorable mechanical properties such as high elastic modulus and toughness, in combination with its large band gap, make SiC an excellent material for high temperature applications. Compared to Si, SiC has demonstrated higher chemical inertness and radiation resistance which also increase its potential for sensors operating in adverse environments. Such applications are in instrumentation and control of nuclear power systems which require high temperature transducers capable of operating in radiation environment. In comparison to diamond, attractive features of SiC are that it can be easily doped both p- and n-type using well-known p-type dopants of aluminum and n-type dopants of nitrogen. In addition, SiC has a natural oxide to be grown on its surface.

2.1.2.2. Thermal properties

The excellent high-temperature properties make SiC very suitable for high high-temperature electronic applications. The high elastic modulus of SiC and the relatively low atomic weights of Si and C promote harmonic lattice vibrations, giving SiC a high thermal conductivity. The values at room temperature for some polytypes are given in Table 2.3. [12] The 3~10 times

high thermal conductivity compared to the conventional semiconductors such as Si and GaAs makes SiC a promising material for high power and high frequency device applications.

2.1.2.3. Optical properties

SiC polytypes have relatively high band gap energies, ranging from 2.39 to 3.33 eV at 0K. These different band gap energies originate from the different polytypes structures that cause changes in the configurations of the valence and conduction bands. With the exception of 2H- and 3C-SiC, there are a limited number of band-structure calculations, mainly due to the rather large number of atoms in the unit cells. All polytypes have the indirect band gaps. In general, the band gap values increase with the degree of hexagonality. The values of the optical band gaps and exciton energy gaps for SiC polytypes are shown in Table 2.4. [13]

2.1.2.4. Electrical properties

The electrical properties of SiC are different for each polytype, as shown in Table 2.5. The table also shows the electrical properties for Si, gallium arsenide (GaAs), and gallium nitride (GaN). The electron and hole mobilities in SiC are a function of carrier concentration, polytype, structural perfection, and temperature. There has been a tendency towards increasing mobilities and

decreasing residual carrier concentration for unintentionally doped epitaxial layers. The electron mobility of 3C-SiC was predicted from theoretical calculations to be significantly greater than can be obtained from 6H-SiC, due to reduced phonon scattering in the cubic material. For this reason, there was early interest in the growth of thin film of 3C-SiC for device applications. However, most recent work has concentrated on the use of 4H-SiC, which has a theoretical electron mobility essentially the same as 3C-SiC and much greater than 6H-SiC. In addition, 4H-SiC has identical mobilities along the vertical and horizontal directions, whereas 6H-SiC has anisotropic mobilities. The breakdown field of 3 MV/cm is one order of magnitude larger than Si and GaAs. This parameter is important in order to reduce on-resistance in power devices. The high saturation drift velocity (2×10^7 cm/s) also enables SiC to operate in devices at high frequencies.

Table 2.2 Mechanical Properties of 3C-, 4H-, and 6H-SiC. [11]

Polytype	Young's modulus (GPa)	Mohs hardness	Acoustic velocity (ms^{-1})
3C	392-448	~9	12600
6H		~9	13730
4H		~9	13260

Table 2.3 Thermal properties of SiC polytypes. [99]

	3C-SiC	4H-SiC	6H-SiC
Thermal conductivity ($Wcm^{-1}K^{-1}$)	4.9	4.9	4.9
Thermal expansion coefficient (K^{-1})	2.9×10^{-6}		4.2×10^{-6} (∥ a-axis)[a] 4.68×10^{-6} (∥ c-axis)[a]
Decomposition temperature (^{o}C)	2839±40		

[a] measured at 700 K

Table 2.4 Optical band gaps and exciton energy gaps for SiC polytypes. [13]

	3C-SiC	6H-SiC	15R-SiC	4H-SiC	2H-SiC
Hexagonality	0	33	40	50	100
Optical bandgap (eV, room T)	2.2	2.86	-	3.26	-
Exciton energy gap (eV, 0 K)	2.39	3.023	2.986	3.265	3.33

Table 2.5 The electrical properties of SiC polytypes, Si, GaAs, and GaN. [99]

	3C-SiC	4H-SiC	6H-SiC	Si	GaAs	GaN
Electron mobility ($cm^2V^{-1}s^{-1}$)	1000	900	450	1500	8500	900
Hole mobility ($cm^2V^{-1}s^{-1}$)	50	100	50	450	400	20
Breakdown electric field ($\times 10^6$ Vcm^{-1})	2	3	3	0.3	0.4	3
Thermal conductivity ($Wcm^{-1}K^{-1}$)	4.9	4.9	4.9	1.5	0.46	1.3
Saturated electron drift velocity ($\times 10^7$ cm^{-1})	2.7	2.2	1.9	1	2	2
Relative dielectric constant (ε_r)	9.7	10.03	10.03	11.9	12.8	10.4
Band gap (eV)	2.39	3.26	3.02	1.12	1.42	3.42

2.1.3. Potential applications of SiC

The high breakdown field and high thermal conductivity of SiC coupled with high operational junction temperatures theoretically permit extremely high power densities and efficiencies to be realized. The high breakdown field of SiC relative to Si or GaAs enables the blocking voltage region of a power device to be roughly 10 times thinner and 10 times more heavily doped, permitting roughly a 100-fold decrease in the blocking region resistance. In addition, the high breakdown field and wide energy band gap of SiC also enable much faster power switching than is possible in comparably volt-amp rated Si power-switching devices, resulting in SiC based power converters which can operate at higher switching frequencies with much greater efficiency (i.e., less switching energy loss). Higher switching frequency in power converters is highly desirable because it permits use of smaller capacitors, inductors, and transformers, which in turn can reduce overall system size and weight. While the smaller on-resistance and faster switching of SiC help minimize energy loss and heat generation, the higher thermal conductivity enables more efficient removal of waste heat from the active device. Waste heat radiation efficiency increases greatly with increasing temperature difference between the device and the cooling ambient. Thus, the ability of SiC to operate at high junction temperatures permits much more efficient cooling to take place, so that heat-sinks and other device-cooling hardware (i.e., fan cooling, liquid cooling, air conditioning, etc.) typically needed to keep high-power devices from overheating can be made much

smaller or even eliminated.

Uncooled operation of high-temperature or high-power SiC electronics would enable revolutionary improvements in aerospace systems. Replacement of hydraulic controls and auxiliary power units with distributed “smart” electromechanical controls and sensors capable of harsh-ambient operation will lead to substantial jet-aircraft weight savings, reduced maintenance, reduced pollution, higher fuel efficiency, and increased operational reliability. SiC high-power solid-state switches will also afford large efficiency gains in electric power management and control. Performance gains from SiC electronics could enable the public power grid to meet the increased consumer electricity demand without building additional generation plants, and improve power quality and operational reliability through ``smart'' power management. More efficient electric motor drives, enabled by improved SiC power devices, will benefit industrial production systems as well as transportation systems such as diesel-electric railroad locomotives, electric mass-transit systems, nuclear-powered ships, and electric automobiles and buses.

Table 2.6 shows the different figures of merit (FOM) characterizing a relative advantage of a given material for various device applications. Johnson's figure of merit (JFM) [14] estimates the potential of a material for high-frequency and high-power applications:

$$\mathrm{JFM} = \frac{E_B^2 v_S^2}{4\pi^2} \quad \text{(Eq. 2.2)}$$

where E_B is the breakdown electric field and vs is the electron saturation velocity. In terms of this figure of merit, SiC is 260 times better than Si and is inferior only to diamond.

Keyes' figure of merit (KFM) [15] is relevant to the application in integrated circuits:

$$\mathrm{KFM} = \kappa\sqrt{\frac{cv_s}{4\pi\varepsilon_r}} \quad \text{(Eq. 2.3)}$$

where c is the velocity of light, ε0 is the relative static dielectric constant, and κ is the thermal conductivity.

Baliga's figure of merit (BFOM) characterize material properties for application in high-power switches:

$$\mathrm{BFOM} = \varepsilon_r \mu E_B^3 \quad \text{(Eq. 2.4)}$$

where, μ is the electron mobility. Since all of these FOM give the different assessment of material properties, a combined dimensionless figure of merit (CFOM) was proposed by Shur et al. [16]

$$\mathrm{CFOM} = \frac{\kappa\epsilon_r\mu v_s E_B^2}{\kappa(\varepsilon_r\mu v_s E_B^2)_{Si}} \quad \text{(Eq. 2.5)}$$

Although these FOMs of diamond is better than that of SiC, it is important to note that it is nearly impossible to obtain the single crystal and epitaxial film of diamond. Therefore, FOM may overestimate the potential of diamond for device application. Among wide band-gap semiconductor materials, 4H-SiC has come closer to practical applications than any other material. [17] Also GaN shows excellent physical properties. Since GaN-based blue light-emitting diodes were developed in the early 1990s, research work on GaN has been received strong efforts to realize short-wavelength laser diodes and high-frequency devices. However, some difficulties in crystal growth remained unsolved, such as a narrow doping range (especially in p-type), high density of defects in grown layers, and the lack of suitable

techniques for large-area bulk growth.

Table 2.6 Figure of merits for selected semiconductors. [99]

	$(E_B v_s)/2\pi$ ($\times 10^{11}$ Vs^{-1})	$(v_s/\varepsilon_r)^{1/2}$ (Wcm$^{-1/2}$ s$^{-1/2}$K^{-1})	JFM	KFM	BFOM	CFOM
Si	9.5	13.8	1.0	1.0	1.0	1.0
GaAs	25.0	6.3	6.9	0.456	15.7	7.36
InP	38.0	8.4	16.0	0.608		
GaN	159.2	24.3	281.6	1.76	24.6	404
6H-SiC	250.0	70.7	695.4	5.12		393
4H-SiC	289.0	76.1	932.3	5.51		404
3C-SiC	320.0	80.3	1137.8	5.81	4.4	
Diamond	859.4	444.0	8206.0	32.2	101	30080

2.2. SiC epitaxial growth

Epitaxy comes from the Greek words epi meaning on, to or above and taxis meaning order or ordering. The translation describes the growth process rather well: On top of a substrate, there are atoms placed in an ordered fashion. To improve the quality of bulk material and produce complicated device structures, epitaxial techniques are necessary. As with other semiconductor material systems, LPE techniques and CVD were used early in the development of SiC to produce device structures. Although the crystal grown by LPE was of high quality, difficulties with molten Si used as the melt prompted the development of vapor phase techniques such as sublimation epitaxy and CVD. CVD is presently the most widely used epitaxial technique for the growth of SiC devices structures.

2.2.1 Chemical Vapor Deposition (CVD)

CVD has been a successful and reliable method for epitaxial growth of SiC films on SiC and Si substrate, because CVD has the advantage of large area capability, precise interface and doping control. 6H-SiC epitaxial growth on 6H-SiC {0001} substrates by CVD has been reported since the late 1960s in the temperature range from 1500 to 1850 ℃. [18-22] A significant lowering of the growth temperature and improvement of material quality have been achieved by using substrates that are misoriented a few degrees off the {0001}

plane toward the [11-20] direction. [23,24] This growth on misoriented substrate has been termed "step-controlled epitaxy" and has the added advantage of stabilizing the polytype structure. Homoepitaxial CVD growth has been reported for 6H, 4H, and 3C-SiC, while heteroepitaxial growth of 3C-SiC has been reported on silicon. [25,26] Several reactor configurations have been successfully developed for the growth of SiC epitaxy. All are constructed with high temperature tolerant materials such as quartz, graphite, and SiC. Most require active water cooling. Hydrogen carrier gas along with silane and propane reagents are typically employed at atmospheric and reduced pressure and temperatures ranging from 1450 to 1600 ℃. To reach these high temperatures inductively heated SiC coated graphite susceptors are employed. The most basic configuration is a cold-wall horizontal reactor, which was utilized in this thesis. The group of Davis [27] have developed the multi-wafer barrel reactor. Kordina et al. [28] have developed a hot-wall reactor for the purpose of reducing the large (20~40 kW) power requirement of the other reactors by using a hollow susceptor in an otherwise basic horizontal reactor. Most recently Rupp et al. [29] developed the single wafer rapidly rotating vertical reactor.

Karmann et al. [30] reported the unintentional incorporation of contaminants from the susceptor during SiC CVD. In these experiments, 6H-SiC layers were grown in an atmospheric pressure reactor with a growth rate of 0.7 ㎛/hr. Uncoated and SiC-coated (100 to 120 ㎛ thick) graphite susceptors were used for comparison. For the uncoated susceptors, the layers were found to be contaminated with aluminum, boron, and nitrogen.

Conversely, using a SiC-coated graphite susceptor in the same system, SiC layers with a concentration ND-NA of 4×10^{15} cm^{-3} could be grown. In a low pressure vertical reactor with high-speed substrate rotation, SiC with background concentrations in the 10^{14} cm^{-3} range was demonstrated without use of SiC-coated parts. This low amount of contamination is attributed to the favorable gas-flow patterns generated in this reactor.

The principle of the CVD process is to transport reactive compounds (precursors) by a carrier gas to a hot zone where the precursors will thermally decompose into atoms or radicals of two or more atoms which may diffuse down onto a substrate and produce an epitaxial film. In this process there are several complications that need to be understood or investigated. The precursors and carrier gas must be correctly chosen, the flow of the gases must be laminar and the material used for the hot parts of the reactor must be chosen with great care in order not to contaminate the system. In addition, there are gas phase and surface reactions taking proper place.

The hydro-dynamics needs to be investigated so that the transport of the precursors is made in an accurate way. The flow must be laminar of two reasons: First, to avoid intermixing between gas compositions of two types i.e. when abrupt pn-junctions or hetero-junctions are required, fast switching between different gas compositions are needed and the intermixing in the gas phase must be kept low. Second, a turbulent flow is an efficient heat exchanger in contrast to a laminar flow. In a laminar flow the heat transport is governed by heat conduction and convection. One may picture it as "sheets" of gas with a specific velocity that are heated or cooled by the adjacent sheets,

having a different velocity. The turbulent flow does not have these sheets and a gas molecule close to a hot surface may at the next moment be in the center of the flow. The whole volume of gas will thus be uniformly heated until it reaches the temperature of the walls (if these are at the same temperature). Efficient heat exchangers always try to maintain a turbulent flow on account of the quick heat transfer. The type of flow through the reactor is largely determined by the dimensionless Reynolds number (Re):

$$\mathrm{Re} = \frac{\bar{u} d_h}{\nu} \quad \text{(Eq. 2.6)}$$

where $\bar{\mu}$ is the mean velocity, dh is the hydraulic diameter (4 times the area divided by the perimeter) and υ is the kinematic viscosity. The hydraulic diameter dh of a circular tube is, thus, its diameter. The relationship between the kinematic viscosity υ, the dynamic viscosity m and the density r is given as:

$$\nu = \frac{\mu}{\rho} \quad \text{(Eq. 2.7)}$$

Typically, the Re number is below 100 for the CVD process. The cross-over to turbulent flow is known to occur for a Re number at approximately 2300. [31] The roughness of the tube surfaces and the shape of the tube have some influence and may give a cross-over point at lower Re numbers. It is, however, unlikely that turbulent flow would occur at the low Re numbers used in the CVD process. So, it is reasonable that the flow in a CVD reactor normally is assumed laminar. Mass transfer of the reactive species in the gas down on to the substrate will thus be taken care of by diffusion.

When the flow is laminar the velocity profile can easily be calculated for simple geometries such as a flow between parallel plates or flow in a circular

pipe. The forces acting on a small element are viscous forces and forces due to the pressure gradient. These forces will balance since at fully developed laminar flow the velocity profile will look exactly the same at different places downstream. A particle will thus at all time travel at the same distance from the walls and at a constant speed. The pressure gradient (pressure force per unit volume) is constant along the length of the pipe or parallel plates.

In the case of CVD, the complexity increases since one or more of the walls are hot and will heat the gas passing through the tube. The physical properties of the gas will thereby change. For gases, the dynamic viscosity increases and the density decreases as the temperature increases, which means that the kinematic viscosity increases with increasing temperature. This will provide more suitable conditions for laminar flow, however, exact calculations of the flow profile will become very difficult to do manually.

It is convenient to discuss the flow close to a wall in terms of a boundary layer. The boundary layer can be illustrated as a layer over which all velocity changes occur. For a laminar flow past a semi-infinite plate the evolution of the boundary layer or the velocity profile is described by the Blasius profile:

$$\delta(x) = 4.99\left(\frac{vx}{u_0}\right)^{\frac{1}{2}} \quad \text{(Eq. 2.8)}$$

The next question is the temperature distribution of the gas phase. This problem is of considerable importance for the growth of SiC on account of the large difference in dissociation energies between the precursors. Accurate estimations of the temperature distribution involve complicated calculations and a great deal of approximations. It can, however, be expressed by the Prandtl number (Pr):

$$P_r = \frac{\nu}{\kappa} \quad \text{(Eq. 2.9)}$$

which is the ratio between the kinematic viscosity and the thermal diffusivity. The Prandtl number is thus a property of the fluid. The thermal diffusivity is expressed as :

$$\kappa = \frac{k}{\rho C_p} \quad \text{(Eq. 2.10)}$$

where k is the thermal conductivity and C_p is the specific heat at constant pressure. For a gaseous medium the Prandtl number is roughly equal to unity. This implies that the thermal and velocity boundary layers are approximately the same. The question of the temperature distribution remains, however, still unanswered since it is hard to calculate the velocity boundary layer accurately.

2.2.1.1. Heteroepitaxial growth of 3C-SiC

Heteroepitaxial growth of SiC is initially motivated by lack of large inexpensive SiC substrate for homoepitaxy. Silicon wafer having a large area diameter has been mainly used as a substrate for SiC epitaxial growth. CVD growth on Si Substrates results in growth of 3C-SiC. The quality of the films depends critically on the substrate structure, orientation, and surface quality. 3C-SiC epitaxial films on (001) Si substrates, the most widely utilized substrate material, contain a variety of defects, including misfit dislocations, threading dislocations, twins, stacking faults, and antiphase boundaries (APB's). [32] The formation of these defects can be attributed to the following factors, including the large difference (0.08%) of the thermal expansion

coefficients and lattice parameters (~20%) between 3C-SiC and Si. Despite intense research of 3C-SiC growth on Si and significant improvement in material properties, the quality of the grown 3C-SiC film is not good enough for most electronic devices. In order to improve the crystalline quality of 3C-SiC films, titanium carbide (TiC) and α-SiC have been developed as an alternative substrate material. Ingots of TiC 18 mm in diameter have been successfully grown and used for SiC growth, although substrate within the ingots is difficult to remove. [33] The use of TiC substrate can result in 3C-SiC films superior in quality to films on Si substrates. [34]

Growth of 3C-SiC on α-SiC substrates greatly reduces problems of lattice mismatch and chemical incompatibility, resulting in lower defect densities. For example, the density of defects in 3C-SiC films can be dramatically reduced by depositing films on basal orientation substrate of 6H-SiC. [35, 36] However, defects such as DPB's generally persist because of island growth and surface defects, and it is not always possible to achieve 3C-SiC growth devoid of α-SiC polytypes.

2.2.1.2. Homoepitaxial growth of α-SiC

Homoepitaxial growth of α-SiC (6H-SiC, 4H-SiC, 15R-SiC) by CVD has been advanced at Kyoto University using off-oriented SiC substrates. This technique is called step-controlled epitaxy because the growth process is determined by the lateral growth rate of the terraces. The growth rate, substrate misorientation, and growth temperature determine whether growth

will occur via the step-controlled mechanism. Step-flow growth has been one of the very interesting subjects from a viewpoint of crystal growth. Since Burton, Cabrera, and Frank (BCF) laid the theoretical foundation on dynamics of atomic steps [37], several modifications of the BCF theory [38-40] and applications to MBE of Si [41] and GaAs [42] have been investigated. Kimoto et al. [43] reported the surface kinetics of adatoms in epitaxial growth of SiC on off-axis 6H-SiC {0001} substrates based on BCF theory.

Let's consider a simple surface diffusion model, where steps with a height h are separated by an equal distance λ_0 as shown in Fig. 2.5. Thermally decomposed molecules in the reactor are absorbed and these adatoms diffuse on terraces toward steps. Some of the adatoms can reach steps and are incorporated into the crystal, and the others re-evaporate to vapor. Some adatoms will coalesce to form nuclei if supersaturation on terrace is high enough.

If it is assumed that the nucleation on terraces does not occur, the effective incoming flux onto the surface should be equal to the diffusion flux toward steps. Then, the continuity equation of adatoms is expressed by [43]

$$-D_s \frac{d^2 n_s(y)}{dy^2} = J - \frac{n_s}{\tau_s} \quad \text{(Eq. 2.11)}$$

where $n_s(y)$ is the number of adatoms per unit area on the surface, J the flux of reactants arriving at the surface, τ_s the mean residence time of adatoms, and Ds the surface diffusion coefficient. Let's assume that the steps are uniform and perfect sinks for the incoming adatoms, that is, the capture probability of adatoms at steps is unity. Under the boundary condition that the supersaturation ratio α (n_s/n_{s0}) equals unity at steps: $n_s = n_{s0}$ at $y=\pm\lambda_0/2$, the

adatom concentration on the terraces can be given as a solution of Eq. 2.11:

$$n_s(y) = J\tau_s + (n_{s0} - J\tau_s)\frac{\cosh(\frac{y}{\lambda_s})}{\cosh(\frac{\lambda_0}{2\lambda_s})} \quad \text{(Eq. 2.12)}$$

where n_{s0} is the adatom concentration at equilibrium and λ_s is the surface diffusion length of adatoms, which is given by the following equation [37]:

$$\lambda_s = (D_s\tau_{s)})^{1/2} = \exp(\frac{E_{des}-E_{diff}}{2kT}) \quad \text{(Eq. 2.13)}$$

where a, k and T are jump distance (interatomic distance), Boltzmann constant, and absolute temperature, respectively. E_{des} and E_{diff} are the activation energies for desorption and surface diffusion. This λ_s is an average length for adatoms to migrate on a "step-free" surface before desorption.

The flow of adatoms in the y direction $J_s(y)$ is given by [37]

$$J_s(y) = -D_s\frac{dn_s(y)}{dy} = \lambda_s\left(J - \frac{n_{s0}}{\tau_s}\right)\frac{\sinh\left(\frac{y}{\lambda_s}\right)}{\cosh\left(\frac{\lambda_0}{2\lambda_s}\right)} \quad \text{(Eq. 2.14)}$$

Since the capture probability of migrating adatoms at steps is assumed to be unit, the step velocity υ_{step} is given by the following equation using the $J_s(y)$ at steps ($y= \lambda_{s0}/2$):

$$v_{step} = 2\frac{J_s(y)}{n_0}\Big|_{y=\lambda_0/2} = \frac{2\lambda_s}{n_0}\left(J - \frac{n_{s0}}{\tau_s}\right)\tanh(\frac{y}{2\lambda_s}) \quad \text{(Eq. 2.15)}$$

Here, n_0 is the density of adatom sites on the surface, and migrating adatoms from both the left and right sides of steps are considered. In step-flow growth, the growth rate (R) is calculated by the product of the step velocity and $\tan\theta$ ($=h/\lambda_0$), where θ is the off-angle of a substrate. Thus, the following equation is satisfied:

$$R = \frac{2h\lambda_s}{n_0\lambda_o}\left(J - \frac{n_{s0}}{\tau_s}\right)\tanh(\frac{\lambda_0}{2\lambda_s}) \quad \text{(Eq. 2.16)}$$

Fig. 2.6 shows the distribution of adatom concentration and the supersaturation ratio (α) on a surface. Since α has a maximum value α_{max} at the center of a terrace, nucleation occurs most easily at this position. Based on Eqs. (2.14) and (2.16), α_{max} can be expressed by

$$\alpha_{max} = 1 + \frac{\lambda_0 n_0 R}{2\lambda_0 h}\frac{\tau_0}{n_{s0}}\tanh\left(\frac{\lambda_0}{4\lambda_s}\right) \quad \text{(Eq. 2.17)}$$

The α_{max} depends on experimental conditions such as growth rate, growth temperature, and terrace width. This α_{max} is an essential parameter that determines whether the growth mode is step-flow or two-dimensional nucleation. Since a two-dimensional nucleation rate J_{nuc} increases exponentially with the supersaturation ratio on a surface, nucleation becomes significant when α_{max} exceeds a critical value α_{crit}. Thus, the growth modes are determined according to the relationship between α_{max} and α_{crit} as follows:

$\alpha_{max} > \alpha_{crit}$: two-dimensional nucleation,

$\alpha_{max} < \alpha_{crit}$: step-flow.

Under the critical condition, the following equation is satisfied:

$\alpha_{max} < \alpha_{crit}$

Using Eq. 2.17, the above equation can be rearranged as

$$\frac{\lambda_0}{4\lambda_s}\tanh\left(\frac{\lambda_0}{4\lambda_s}\right) = \frac{(\alpha_{crit}-1)}{2n_0 R}\frac{n_{s0}}{\tau_s} \quad \text{(Eq. 2.18)}$$

In Eq. 2.18, R and λ_0 are determined by growth condition, and n_0 and h are inherent parameters of a material. If the values of n_{s0}/τ_s and α_{crit} are known, λ_s can be calculated from Eq. 2.18. Then, by finding out the critical condition experimentally, the surface diffusion length can be estimated. A critical growth rate can be calculated by Eq. 2.16 if the growth temperature

and off-angle of substrates are fixed. Kimoto et al. [42] calculated critical growth conditions for various off-angle of substrate as shown in Fig. 2.7. As shown, the higher growth rate and lower off-angle are available for step-flow growth at higher growth temperatures.

In 1986 to 1987, Matsunami group [24] and Davis group [25] reported the 6H-SiC epitaxial growth on off-axis 6H-SiC {0001} substrate at low temperatures of 1500 ℃, independently. This technique is named "step-controlled epitaxy", because the polytype of epilayer can be controlled by the exposed step sequence of off-axis substrate Hence, the polytype mixing problem in CVD growth was solved by using off-axis substrate. Today, device-quality SiC epitaxial films have been produced by this technique.

In SiC growth, the step flow results in homoepitaxial growth while the two-dimensional nucleation leads to growth of twinned crystalline 3C-SiC, which is stable at low temperature (< 1500 ℃). In the case of two-dimensional nucleation, the growing 3C-SiC can take two possible stacking sequence of ABCABC... and ACBACB...., leading to double positioning boundary (DPB). To enhance step flow, the step density and terrace width should be large and small, respectively. This is the reason why several degree off-axis substrate is used for homoepitaxy of SiC. The technique of step-controlled epitaxy is utilized for growth of 6H-SiC, 4H-SiC, and 15R-SiC.

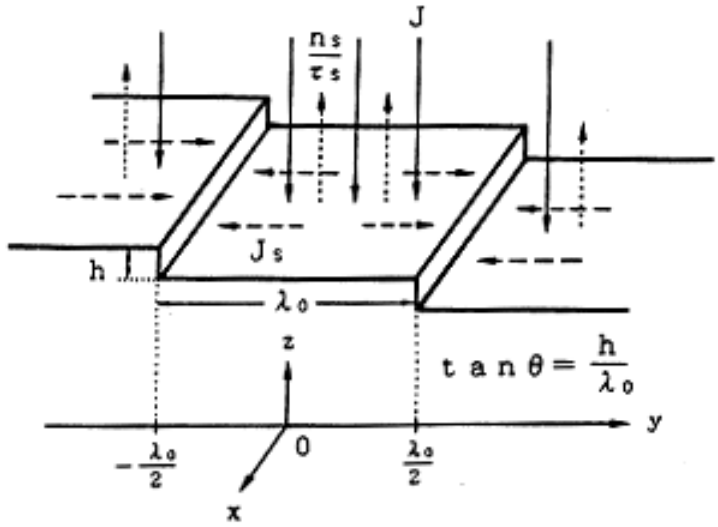

Figure 2.5 Schematic illustration of simple surface diffusion model, where steps with a height h are separated by an equal distance. [42]

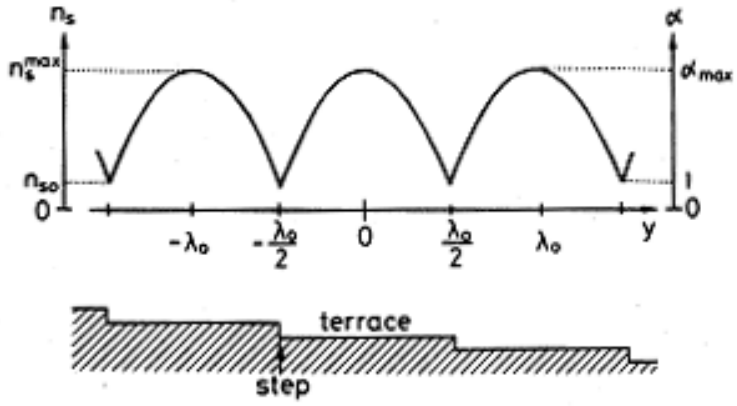

Figure 2.6 The distribution of adatom concentration and supersaturation ratio α (= ns/ns0) on off-axis surface. [42]

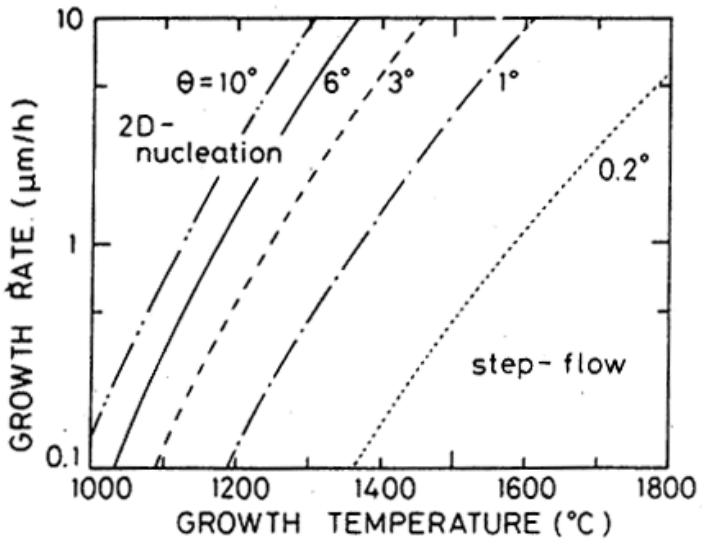

Figure 2.7 Critical growth conditions as a function of growth temperature, growth rate, and off-angles of the substrate (θ= 0.2°, 1°, 3°, 6°, and 10°). The top-left and bottom-left regions from the curves correspond to two-dimensional nucleation and step-flow growth conditions respectively. [42]

2.2.1.3. Precursor materials for CVD

A number of precursors have been used for the growth of SiC. For transport of the Si species, the most popular choice is SiH_4, along with Si_2H_6 and $SiCl_4$ which have also been used. For growth of SiC, the hydrocarbon species most reported is C_3H_8. However, there are also reports of SiC growth using C_2H_2, CH_3Cl, CH_4 as carbon sources. In the case of 3C-SiC heteroepitaxial growth on silicon, single precursor materials such as methyltrichlorosilane (MTS) [44], silacyclobutane (SCB) [45], hexamethyldisilane (HMDS) [46], methylsilane [47], and BTMSM [48] to reduce the deposition temperature. However, in the case of homoepitaxial growth for 4H-SiC and 6H-SiC, there is no systematic investigation using single precursor material. In this thesis, BTMSM source material was used for the SiC deposition. It is important to note the similarity between HMDS [$(CH_3)_3$-Si-Si-$(CH_3)_3$] and BTMSM [$(CH_3)_3$-Si-CH_2-Si-$(CH_3)_3$] precursor. Takahashi et al. [46] reported that HMDS decomposed in the form $(CH_3)_n$-Si-H_{4-n} (n=1~3) species below 1300 ℃ and the intensity of $(CH_3)_n$-Si-H_{4-n} have maxima at around 1100 ℃. Hence, the dominant process at temperature between 1100 and 1300 ℃ is

$$(\mathrm{CH_3})_\mathrm{n} - \mathrm{Si} - \mathrm{H}_{4-\mathrm{n}}(\mathrm{n} = 1 - 3) + \mathrm{H_2} \rightarrow \mathrm{SiC}(solid) + \mathrm{C_nH_m} + \mathrm{H_2}$$

At temperature higher than 1300 ℃, $(CH_3)_n$-Si-H_{4-n} species are expected to undergo second-order decomposition as follows

$$(\mathrm{CH_3})_\mathrm{n} - \mathrm{Si} - \mathrm{H}_{4-\mathrm{n}}(\mathrm{n} = 1 - 3) + \mathrm{H_2} \rightarrow \mathrm{C_nH_m} + \mathrm{or\ Si}\ (radical)\ \mathrm{or\ etc.}$$

2.2.1.4. Growth equipment for CVD

The chemical vapor deposition of silicon carbide can be classified into various types according to the structure and the shape of the reactor. In this section, we describe the structure and characteristics of a horizontal cold-wall reactor and a horizontal hot-wall reactor.

The horizontal cold wall reactor has been used for a long time, and the schematic structure of the equipment is shown in Fig. 2.8. Since this type of reactor has been used for epitaxial growth of compound semiconductors for a long time, it has been applied to silicon carbide epitaxial growth relatively easily at the beginning. The horizontal cold wall reactor consists of a double quartz tube in which water is circulated between the walls of the reactor as shown. The substrate or specimen is placed on an induction heated graphite susceptor. The water circulating between the walls serves to cool down and the susceptor is placed on the insulation to maintain a cool wall condition. As shown, the susceptor is tilted to maintain uniformity of the epitaxial layer being grown. These horizontal cold wall reactors are widely used due to the simple structure of the reactor and the convenience of application, but they have limitations in terms of industrialization such as limited substrate size and low temperature uniformity or low growth rate of epitaxial layer.

The industrial limitations of this horizontal cold wall reactor can be solved in a hot wall reactor. Most of the drawbacks of cold wall reactors are related to the fact that the bottom of the substrate is heated but the top of the

substrate is not heated. That is, the temperature gradient between the upper part of the specimen and the reactor wall is very large. Most of the hot wall reactors have the structure shown in Fig. 2.9, and the heated susceptor wraps the substrate, thereby achieving thermal uniformity not only in the horizontal direction but also in the vertical direction. In the figure, the graphite susceptor has a rectangular hole through the susceptor and the top of the hole is tilted. The geometry of such a susceptor reduces the depletion effect to increase the velocity of the passing gas and to grow a uniform epitaxial layer. The susceptor is surrounded by a heat-insulating material, which reduces heat loss due to radiant heat, resulting in much lower power consumption than a cold-walled reactor. The excellent thermal uniformity of the hot wall reactor increases the efficiency of the precursor decomposition and leads to an increase in the growth rate. In fact, the growth rate of the hot wall reactor is very high, about 25 ~ 50μm / h, compared with the growth rate of 5 ~ 10μm / h of the cold wall reactor. Besides the improvement of the growth rate, there is an advantage of eliminating the supersaturation of the silicon due to the temperature gradient in the vertical direction, thereby improving the uniformity of the epitaxial layer. That is, the gas phase Si aggregation is minimized in the hot wall reactor as compared to the cold wall reactor. Finally, in a hot wall reactor, it is possible to provide a very stable environment for long-term growth and continuous growth of more than several hours without deterioration of the silicon carbide surface. Such industrial advantages of hot wall reactors have been applied in a variety of improved ways.

One of them is a vertical hot wall reactor designed for very high

deposition rates. [49] This structure, called a chimney reactor, is shown in Fig. 2.10. The structure of the symmetric susceptor enables symmetrical temperature gradients and distribution of gas flow over the substrates placed opposite the susceptor. Generally, the gas is injected from the bottom to the top of the reactor. Epitaxial growth at a doping concentration of 10^{14} cm^{-3} was reported at a growth rate of 30μm/h.

High temperatures in SiC epitaxial reactors can be obtained with rf heating. In most systems, the susceptor is made from graphite and coated with SiC because of the reaction between graphite and H_2 at temperatures in excess of 1300 ℃. Unintentional incorporation of contaminants from the susceptor during SiC CVD was studied by Karmann and co-workers. [50] In a low-pressure vertical reactor with high-speed substrate rotation, SiC with background concentration in the 10^{14} cm^{-3} range was demonstrated without use of SiC-coated parts. This low amount of contamination is attributed to the favorable gas-flow patterns generated in this reactor.

Temperature measurement is a major equipment issue for CVD growth at high temperatures. During growth, substrate temperature is usually measured by optical pyrometer calibrated by melting of Si of Ge. The temperature of the susceptor typically is found to be 50 to 100 ℃ higher than that of the SiC substrate.

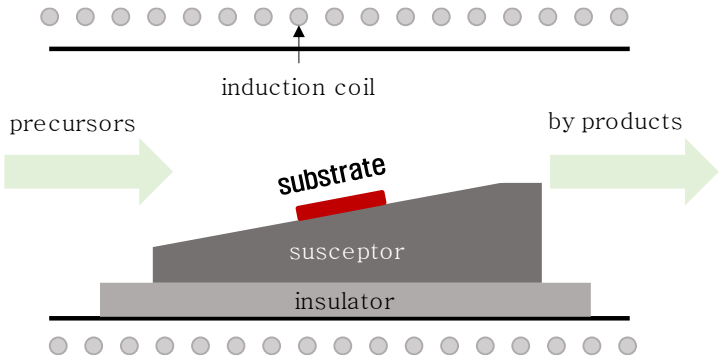

Figure 2.8 Schematic structure of horizontal cold wall reactor.

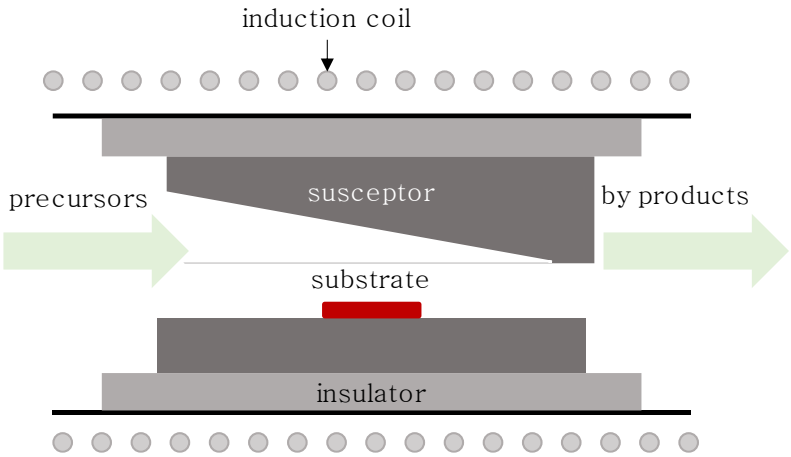

Figure 2.9 Schematic structure of horizontal hot wall reactor.

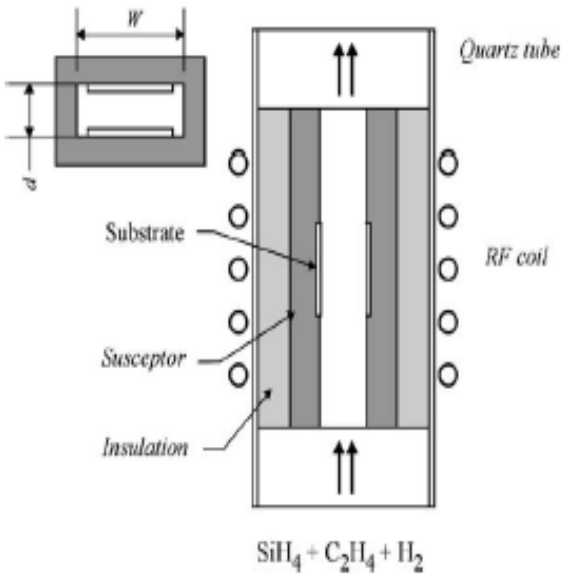

Figure 2.10 Schematic structure of vertical hot wall reactor. [49]

2.2.2. Liquid phase epitaxy

SiC LPE growth is performed from a supersaturated solution of Si and C in a melt solvent. The growing films are in equilibrium with the liquid phase during LPE growth. The endpoint of the process is determined by the phase diagrams for Si, C, and the solvent material. LPE was used early in the development of SiC technology. Growth from Si melt as well as alloy melts was demonstrated. LPE has been performed in graphite boats by vertical dipping and by a novel levitation process called container-free epitaxy. Doping of SiC was accomplished in LPE over a large range of concentrations. Due to the difficulty in control of surface morphology, LPE techniques have lost ground in favor of CVD approaches. However, recently discovered unique properties of LPE [51] such as micropipe closing and the ability to produce very heavily doped p-type film with a carrier concentration of 5×10^{20} cm^{-3}, may secure a future role for this technology.

2.2.3. Sublimation epitaxy

The growth mechanism of SiC sublimation epitaxy are similar to those for bulk SiC sublimation growth. However, sublimation epitaxy is usually performed at lower temperatures with smaller growth rates and for shorter time periods than bulk SiC sublimation growth. Growth of epitaxial SiC using the sublimation process had been the subject of many early investigations. The breakthrough in sublimation epitaxial technology was achieved with the

development of "sublimation sandwich method" by Vodakov et al. [52] They employed a nearly flat source positioned close to the substrate and performed the growth under near equilibrium conditions. This method allowed for the vapor equilibrium to be constant over the substrate. The sublimation sandwich method made it possible to grow high-quality SiC films in the temperature range of 1600 to 2100 ℃. [53]

2.2.4. Molecular beam epitaxy

Molecular beam epitaxy (MBE) has attracted more interest because of lower deposition temperature (<1100 ℃) and the clean ambient. Additionally, the superlattice of SiC polytypes having a slightly different band-gap that can be grown, which may be used in quantum well devices. Solid- and gas-source (GS) MBE techniques have been employed for the deposition of SiC films. [54, 55] Kaneda et al. [54] used on-axis α(6H)-SiC {0001} substrates and electron-beam evaporated Si and C sources. Epitaxial 3C-SiC (111) films were obtained at a particular Si-to-C flux ratio in the temperature range of 1150~1400 ℃. By contrast, Yoshinobu et al. [55] employed the periodic introduction of Si_2H_6 and C_2H_2 to achieve 3C-SiC growth on vicinal 6H-SiC $(000\bar{1})$and 6H-SiC $(0\bar{1}1\bar{4})$ substrates at 850~1160 ℃. Films grown on vicinal 6H-SiC $(000\bar{1})$contained DPB's while those grown on 6H-SiC $(0\bar{1}1\bar{4})$were free of these defects. Rowland et al. [56] reported the deposition of monocrystalline 3C-SiC on 6H-SiC(0001) at 1050 ℃ using a simultaneous supply of C_2H_4 and Si_2H_6 which shows the very slow growth rate of 10 nm/hr.

Taneka et al. [57] investigated the effects of gas flow ratio on SiC film growth mode and polytype formation during GSMBE. Island formation occurred under carbon rich condition, while step flow was achieved using the gas flow ration of 1. Hence, 6H-SiC films on 6H-SiC substrate was grown at 1050 ℃ using a simultaneous supply of source gases and $C_2H_4/Si_2H_6 = 1$. Recently, Fissel et al. [58] reported the controlled growth of SiC heteropolytypic structures consisting of hexagonal and cubic polytypes by SSMBE. On on-axis substrates, 4H/3C/4H-SiC (0001) and 6H/3C/6H-SiC (0001) structures were obtained by first growing the 3C-SiC film some nanometer thick at lower temperature of 1277 ℃ and Si-rich conditions and a subsequent growth of α-SiC on top of 3C-SiC film at higher temperature of 1327 ℃ under more C-rich conditions. Nevertheless, MBE technology for SiC growth is in its fancy, and material with competitive performance parameter is yet to be produced.

2.3. SiC doping

Wide band-gap materials are difficult to dope due to the large ionization energies and self-compensation effects of most substitutional impurities. Fortunately, in the case of SiC, an excellent donor atom (nitrogen) exists and a workable acceptor atom (aluminum) also exists. Progress in SiC technology has resulted in a wide doping range for both n- and p-type conductivity. The three doping techniques are doping during growth, diffusion, and ion implantation.

Impurities for SiC doping have been found for: (1) donors (mainly nitrogen), (2) acceptors (mainly aluminum), and (3) deep-level impurities to form semi-insulating material (practically vanadium). Recently, Er was introduced in SiC and preliminary results for IR emission [59] look promising. There have been few attempts to study isoelectronic traps in SiC, but the subject requires further investigation. The doping development for SiC is complicated because the doping process depends not only on the surface orientation, doping technology, and doping concentration, but also on polytype structure. So, the information on impurity properties in SiC is limited even for impurities such as nitrogen and aluminum.

2.3.1. In-situ doping during epitaxial growth

In order to obtain the wide range doping concentration, unintentional doping level should be small. 6H-SiC epitaxial layers having a low

background doping concentration were grown and characterized. [60] It was shown that, using propane as a carbon precursor, uncompensated SiC films with donor concentration less than 10^{15} cm^{-3} may be grown, whereas with methane, uncompensated layers can be produced with electron concentrations in the mid $10^{14}cm^{-3}$ range. The optimal growth temperatures for these films were found to vary between 1550 and 1600 ℃. At higher temperatures, contamination from graphite parts become noticeable, and bake-out of the growth system had a significant impact on the background doping. The effect of unintentional hydrogen doping by CVD was studied by Clemen et al. [61] 4H-SiC layers with electron concentrations as low as 2×10^{14} cm^{-3} were reported. [62] Kimoto et al. [63] reported electrical and optical measurements on high-quality 4H-SiC layers. The background doping concentration in the SiC films was determined to be 3×10^{15} to 2×10^{16} cm^{-3}, and electron mobility in the {0001} basal plane was 600 to 720 cm^2/Vs (300K). Deep-level transient spectroscopy (DLTS) measurements on these films showed that the concentration of electron traps was approximately 10^{13} cm^{-3} independently of substrate polarity. Minority carrier lifetimes have been measured on 6H-SiC layers with N_D-N_A ranging from 10^{14} to 10^{17} cm^{-3}. Lifetimes as high as 0.45us (300K) have been achieved for thick low-doped epi-layers. [64] However, the maximum reported values of minority carrier diffusion length for CVD-grown SiC pn structure do not exceed 3um.

In-situ n-type doping can easily be achieved by the introduction of N_2 during epitaxial growth. The donor concentration is proportional to the N_2 flow rate in the wide range (10^{16} to 10^{19} cm^{-3}) on both Si and C faces. [65]

P-type doping has been achieved by using Al as a dopant. [66] Epitaxial films in this study were grown using SiH_4-C_3H_8-H_2-TMA (trimethylaluminum) precursor at a C/Si ratio of 2.5. The reactor pressure was 800mbar and growth temperature was 1550 ℃. A growth rate was about 2um/hr. The atomic Al concentration in 6H-SiC was controlled from 10^{17} to 10^{21} cm^{-3}. When the Al concentration exceeded 2×10^{20} cm^{-3}, impurity banding occurred and the Al acceptors were completely ionized, while 1% ionization was observed at lower doping levels with the Al ionization energy of 0.25 eV. Schoner et al. [67] found that the Al ionization energy varied with doping concentration as well as the degree of compensation. As expected, at high doping levels, crystal quality was deteriorated.

In 1993, Larkin et al. [68] demonstrated a dependence of dopant incorporation efficiency on input Si/C ratio (analogous to the impact of III/V ratio in that compound semiconductor family [69]) helping to both reduce background doping density and extend the range of intentional doping into epilayers. So-called site-competition epitaxy has been used for the control of nitrogen, phosphorus, aluminum, and boron incorporation in 6H-SiC and 4H-SiC films. For example, in the case of nitrogen doping, the growth under a higher C/Si ratio leads to the lower N concentration in the epilayers. This phenomenon can be explained by the fact that the higher C atom coverage on a growing surface prevents the incorporation of N atom, which substitute at the C site, into crystal.

Impurity memory effect on dopant concentration profiles in 4H- and 6H-SiC were investigated by SIMS. [70] It was found that dopants were absorbed

by the reactor walls and re-evaporated after the dopant precursor flow was switch off. These memory effects limit the doping control range to about three orders of magnitude for aluminum and two orders of magnitude for boron. The dynamic range for Al doping was increased up to five orders of magnitude by controlling the Si/C ratio and using HCl etching during the 10 min growth interruption after gas switching. For boron, a dynamic range of more than three orders of magnitude was obtained. Doping spikes between the substrate and epi-layer were also reduced by an in situ HCl etch. [71]

2.3.2. Diffusion of Impurities in SiC

Impurities diffusion is one of the principal methods of doping. Although the effective diffusion coefficients for most of the major impurities in SiC is too small for practical applications, it is nevertheless important to understand diffusion process in SiC, as these processes may take place during bulk and epitaxial growth, as well as during heat treatments. Diffusion coefficients for different impurities in 6H-SiC are shown in Fig. 2.11. [72] Boron and aluminum diffusion has been used for SiC device fabrication. Boron diffusion has produced yellow and green [73] light-emitting diodes, while field effect transistors were fabricated by aluminum diffusion. [74]

2.3.3. Ion Implantation

Ion implantation is a materials engineering process by which ions of a

material can be implanted into another solid, thereby changing the physical properties of the solid. Ion implantation is used in semiconductor device fabrication and in metal finishing, as well as various applications. Especially, Ion implantation is the only technique for the selective doping and is widely used in SiC device technology. Ion implantation has been used for: (1) p-n junction formation [75], (2) light emitting diode fabrication [76], (3) highly doped contact layers [77, 78], (4) field effect transistor channels [79], and (5) device isolation and termination. [80] Ion-implanted dopant activation is achieved by thermal annealing using resistively or rf-heated furnaces. [81] Excimer laser activation has also been reported. [82] Simulation of implantation profiles in SiC and their comparison with experimental results have been performed. [83]

N-type doping by ion implantation has been developed into a production process. Annealing of nitrogen implantation has, in general, resulted in low residual damage due to the small size of nitrogen atom. Nitrogen ion implantation is usually performed in 6H-SiC at elevated temperatures. Annealing at 1500 and 1600 ℃ for 15 min, performed in SiC crucibles, results in Rutherford back-scattering yields at the virgin crystal level, indicating a good recovery of the crystalline quality. Recently, activation process of high-dose (3.8×10^{15} and 7.1×10^{15} cm^{-2}) nitrogen implants into 6H-SiC have been investigated. [84] It was shown that low resistivity of the implanted material can be obtained after long-time (2000 min) anneals at 900 ℃.

One of the current problem in ion implantation technology is activation

of the p-type dopants. Because Al is a large atom, higher annealing temperatures and times are required to produce device-quality p-type layers. [85] Amorphization and recrystallization of Al-implanted 6H-SiC were investigated. [86] Ion implantation was performed in n-type 6H-SiC in the temperature range of room temperature to 1000 ℃. Aluminum ions were implanted with a dose range of 5×10^{13} to 5×10^{16} cm^{-2} and implant energies of 180 and 360 keV into 6H-SiC epitaxial layers having doping concentration of 1×10^{16} cm^{-3}. After implantation, the samples were annealed between 800 and 1600 ℃ for 30 min in an Ar flow. It was shown that density of defects induced by implantation decreased exponentially with increasing implantation temperature. However, residual defects were detected even after annealing at 1600 ℃. At a 1600 ℃ anneal temperature sublimation of SiC was observed. Carrier concentration and mobility were found to be independent of the implantation temperature, and the carrier concentrations at room temperature were measured to be about 5% of implanted dopant. The measured hole mobility was less than 1 cm^2/Vs (300 K). Annealing p-type implants at lower temperatures has proven ineffective. For example, annealing at 1400 ℃ [87] resulted in a hole concentration of 5×10^{17} cm^{-3}. Also, C or Si co-implantation also did not improve Al activation efficiency. [88] Experimental data on ion implantation in other than the 6H polytype are limited.

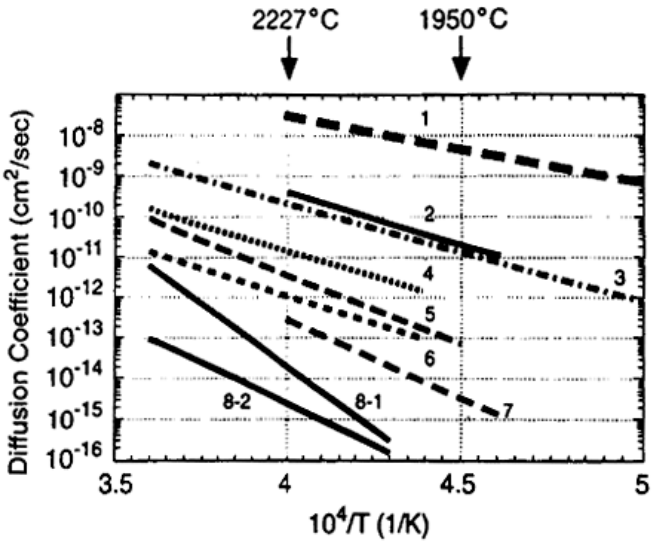

Figure 2.11 Diffusion coefficients for different impurities in 6H-SiC. [1: Be (bulk diffusion), 2: Be (diffusion in the surface region), 3: B (Bulk diffusion), 4: B (diffusion in the surface region), 5: Al, 6: Ga, 7: oxygen, 8-1 and 8-2: nitrogen]. [75]

2.4. Step kinetics on vicinal surface

Step bunching in 4H-SiC homoepitaxial growth is widely investigated because the use of off-axis substrate in 4H-SiC epitaxy. Micro-step bunching is well explained by surface energy minimization by Kimoto et al. [42], but macro-step bunching is still not well explained. Here the step kinetics during film growth could be a clue for the behavior of macro-step bunching because macro-step bunching during 4H-SiC epitaxy is affected by process parameters. The step kinetics on vicinal surface is quoted from Ki-Ha Hong's Ph. D. Thesis. [89] Step bunching is famous unstable step structure appeared during growth of vicinal surface. Though many origins, the lattice strain effects and diffusion asymmetric kinetics at step-edge is introduced.

The theory of the growth of a stepped surface by molecular beam epitaxy (MBE) was devised by Burton, Cabrera and Frank. [37] Considering the growth by MBE of an infinite vicinal surface, formed by terraces of high-symmetry orientation separated by parallel, equidistance steps, following diffusion equation can be obtained.

$$\frac{\partial \eta}{\partial t} = D\frac{\mathrm{d}}{\mathrm{d}x^2}\eta + F \quad \text{(Eq. 2.19)}$$

η is adatom density per unit site, D is adatom diffusion coefficient, and F is adatom flux. In this study, we consider step flow growth mode and the atom diffusion is generally much faster than step motion in this case. Therefore, it is a good approximation to neglect time derivative of η. This is called quasi-static approximation. [90]

At region 1 in Fig. 2.12, the governing equation for adatom concentration is

$$D\frac{\mathrm{d}}{\mathrm{d}x^2}\eta + F = 0$$

and the boundary conditions are: $D\frac{d\eta}{dx}\Big|_{x_{m-1}^{+0}} = K^{-}(\eta - \eta_0(x_{m-1}))$ at x_{m-1} and $-D\frac{d\eta}{dx}\Big|_{x_m^{-0}} = K^{+}(\eta - \eta_0(x_m))$ at x_m, which comes from assumption of that diffusion flux at step-edge is proportional to difference between adatom density η and equilibrium density η_0 at step-edge. K^- and K^+ is kinetic coefficient influencing asymmetric kinetics at step edge. In the absence of ES barrier, $K^- = K^+ = \infty$, and this is also assumed by Tersoff et al. [91]

At region 2, the governing equation is also

$$D\frac{\mathrm{d}}{\mathrm{d}x^2}\eta + F = 0$$

And the boundary conditions are: $D\frac{d\eta}{dx}\Big|_{x_m^{+0}} = K^{-}(\eta - \eta_0(x_m))$ at x_m and at x_{m+1}.

Then, the velocity of the mth step becomes

$$v_m = D\left[\frac{d\eta}{dx}|x_m^{+0} - \frac{d\eta}{dx}|x_m^{-0}\right] \quad \text{(Eq. 2. 20)}$$

If one knows the adatom density at the mth step, velocity of each step can be determined by the Eq. 2.20. There are two factors to affect the adatom density at mth step. One is the adatom formation energy at step (E_1) and the

other is elastic force exerted on a step (f_m). There are two kinds of elastic interactions between steps. [92] The one is monopole force induced by bulk stress. In a strained layer, the lateral force forms the strained material on one side of the step is not balanced by and equal force from the other side. This force attracting steps of which direction normal is same. The other is dipole force induced by the intrinsic strain due to asymmetric neighborhood at step edge. Dipole force repels steps with each other. Elastic force exerted on step m is expressed as follows:

$$f_m = \sum_{n \neq m} \left(\frac{\alpha_1}{(x_n - x_m)} - \frac{\alpha_2}{(x_n - x_m)^3} \right) \quad \text{(Eq. 2. 21)}$$

Where $\alpha_1 = \sigma_2 h_2 / M$, M being an elastic constant and α_2 is the strength of dipole, x_m is the position of the m_{th} step in the direction perpendicular to the steps. The first term represents monopole-monopole interaction induced by lattice strain and this term generates attractive force between steps of which direction normal is same. The second term makes repulsion force between steps. Then equilibrium adatom concentration can be expressed as follows [91]:

$$\eta_0(x_m) = \eta_e e^{-f_m A / kT} \quad \text{(Eq. 2. 22)}$$

E_1 is the formation energy of an adatom (the energy to dissociate an adatom from a step) and A is the area per surface site. Inserting Eq. 2.22 and boundary condition into Eq. 2.20, one can obtain following step velocity equation.

$$v_m = v_m^k + v_m^E \quad \text{(Eq. 2.23)}$$

Where

$$v_m^k = \frac{F\left\{\frac{D}{K^+}x_{m+1}+\frac{D}{K^-}x_m+\frac{1}{2}(x_{m+1}^2-x_m^2)\right\}}{\frac{D}{K^+}+\frac{D}{K^-}+(x_{m+1}-x_m)} - \frac{F\left\{\frac{D}{K^+}x_m+\frac{D}{K^-}x_{m-1}+\frac{1}{2}(x_m^2-x_{m-1}^2)\right\}}{\frac{D}{K^+}+\frac{D}{K^-}+(x_m-x_{m-1})}$$

(Eq. 2.24)

And

$$v_m^E = -\frac{D\eta_o A}{kT}\left\{\frac{f_{m+1}-f_m}{P+(x_{m+1}-x_m)} - \frac{f_m-f_{m-1}}{P+(x_m-x_{m-1})}\right\} \quad \text{(Eq. 2.25)}$$

Where

$$P = \frac{D}{K^+} + \frac{D}{K^-} \quad \text{(Eq. 2.26)}$$

With Eq. 2.23, we can analyze step dynamics under stress within step flow regime and the step structure change during step flow growth will be shown.

The existence of bunching instability can be determined by linear stability analysis that perturbing the steps from their initial equidistant positions and calculating the linear response. Let $u_m(t)$ denote the deviation of the step from the position it would have under ideal step flow, i.e.,

$$u_m(t) = x_m(t) - L_{av}(m + Ft) \quad \text{(Eq. 2.27)}$$

where L_{av} is the average step separations. For a perturbation of amplitude Δ and period N steps, we substitute $u_m(t=0) = \Delta\cos(2\pi m/N)$ into Eq. 2.23 and integrate the velocity. Resulted fluctuation for small intervals within first order in Δ is

$$u_m(t) \approx e^{rt}\Delta cos(km + \Xi(t)) \quad \text{(Eq. 2.28)}$$

where $\Xi(t) = Ft\,[P^2 + L_{av}\,(2P + L_{av})]\,\sin k/\,(P + Lav)^2$.

r is defined as follows within linear stability.

$$r = \left(1 - cos\frac{2\pi}{N}\right)\left[B\frac{\alpha_1}{L_{av}^3}\frac{4\pi^2}{N^2}(N-1) - B\frac{4\alpha_2\pi^4}{L_{av}^5 N^4}(N-1)^2 - \frac{F\left[\left(\frac{D}{K^+}\right)^2 - \left(\frac{D}{K^-}\right)^2\right]}{(P+L_{av})^2}\right] \quad \text{(Eq. 2.29)}$$

where, $B = \frac{DA}{2kT}e^{-E_1/kT}$N is period of the sinusoidal perturbation. If r>0, the perturbation will be amplified and it means that there are step bunching instability. Though Tersoff et al's model [91] is only valid in the condition that N is very large, this model is valid for whole range of N and moreover, this model contains the effect of surface kinetics. The first term within a brace in Eq. 2.29 cannot be minus value, only second term surrounded with bracket determines the sign of r. There are three terms determining step bunching instability in the bracket. The first term in the bracket is related with the monopole interaction and this promotes bunching instability. The second is related with dipole interaction and this stabilizes equidistant step structure. The third is originated from ES barrier and this can make several interesting phenomena. For normal ES barrier, D / K^+ has finite value because it needs excess energy for interstep diffusion and D / K^- becomes almost '0'. In this case, the third term has positive value and hinders step bunching instability. This term is closely related with flux which is expected to stabilize step flow growth in this case. But there was a report on a possibility of inverse ES barrier for homoepitaxy on Si (0001). Inverse ES barrier means that there is excess energy barrier of adatom attachment to step edge from terrace. [95] In the case of inverse ES barrier, the third term has negative value and adatom flux can promotes step bunching which are

opposite with normal ES barrier condition. This model has important physical meaning in points of that it can analyze competition between elastic interaction and interstep diffusion kinetics and also predicts the kinetic bunching induced by inverse ES barrier.

There are so many factors to determine the growth characteristics. Eq. 2.29 says that step bunching can be affected by step-step interaction, average step distance (miscut angle), flux, ES barrier and temperature. Energy configuration of normal ES barrier and inverse ES barrier is plotted in Fig. 2.13.

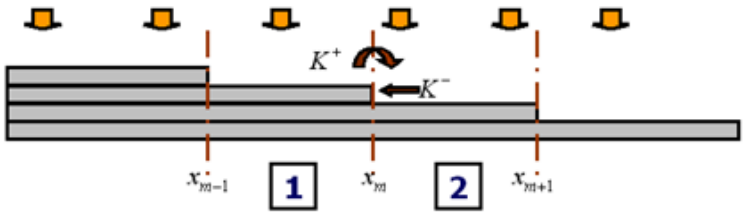

Figure 2.12 One dimensional picture of the step flow growth. Region 1 indicate upper terrace region and region 2 indicates lower terrace region. K^- and K^+ is kinetic coefficient influencing asymmetric kinetics at step edge. [91]

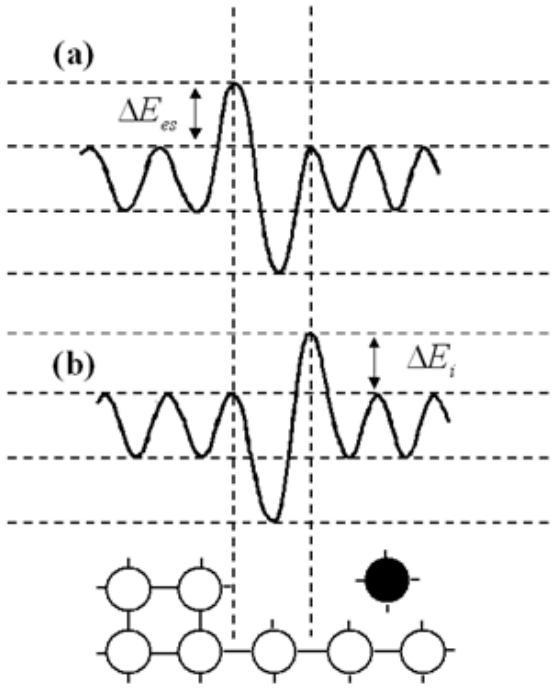

Figure 2.13 Model potential for adatoms near a step edge. (a) Normal and (b) inverse ES barrier. [92]

2.5. SiC Power Device Application

SiC can withstand a voltage gradient (or electric field) over eight times greater than Si or GaAs without undergoing avalanche breakdown. This high breakdown electric field enables the fabrication of very high voltage, high-power devices such as diode, power transistors, power thyristors and surge suppressors, as well as high power microwave devices. [13,14] Additionally, it allows the devices to be placed very close together, providing high device packaging density for integrated circuits. SiC is an excellent thermal conductor (SiC possess high thermal conductivity). Heat will flow more readily through SiC than other semiconductor materials. In fact, at room temperature, SiC has a higher thermal conductivity than any metal. This property enables SiC devices to operate at extremely high power levels and still dissipate the large amounts of excess heat generated. The high saturated electron drift velocity explain why SiC devices can operate at high frequencies (RF and microwave).

Power semiconductor devices are a critical element of smart power electronics technology. Today, utilities generate on average 20% more electricity than is consumed at any given time. This excess power reserve is needed to ensure that electric service is reliably immune to everyday load changes and component failures that cause electrical glitches throughout the power grid. The incorporation of solid state smart power electronics into the power grid should significantly reduce the power reserve margin necessary for compensate for local glitches. It has been estimated that a mere 5% reduction

in power reserve margin would eliminate the need for $ 50 billion worth of new power plants within the next 25 years. This same smart power technology would also enable as much as 50% larger power capacities to be carried over existing power lines. Presently, these devices are all implemented in conventional silicon based semiconductor technology. The faster switching speed not only increases conversion efficiency of power system, but it also enables the use of smaller transformers and capacitors to greatly shrink the overall size and weight of the system. Furthermore, the high temperature capability of SiC greatly reduces cooling requirements that are also a substantial portion of the total size and cost of a power conversion and distribution system (Fig. 2.14). [93] Recent developments in SiC device technology have opened up the hybrid electric vehicles or the fuel cell electric vehicle for SiC based power electronics, where these devices could be utilized for substantial weight savings and enhanced electric vehicles performance (Fig. 2.12). [94] SiC devices are therefore expected to drastically improve the distribution and efficient usage of electric power in the 21st century.

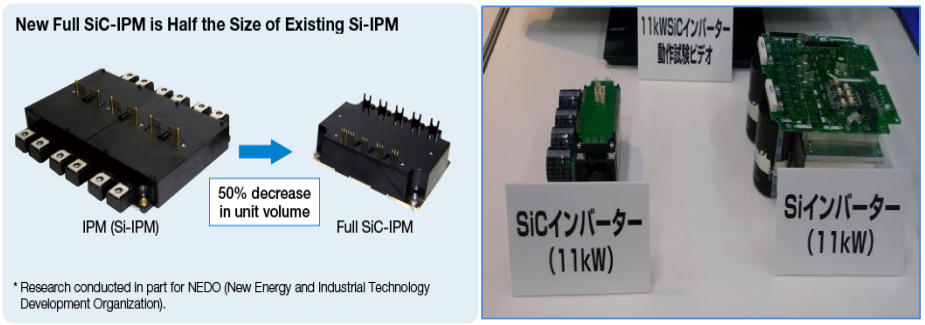

Figure 2.14 Comparison SiC-IPM with Si IPM. [93]

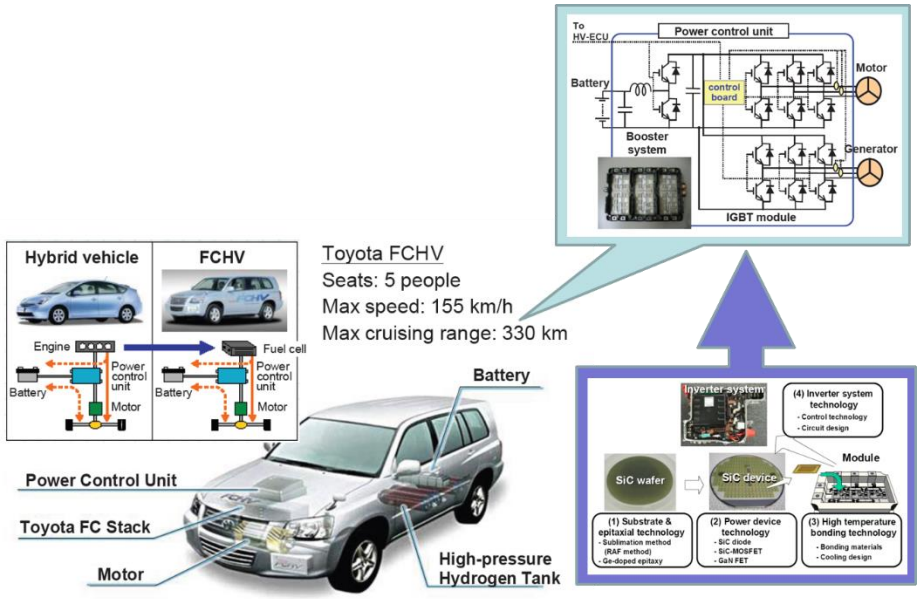

Figure 2.15 Schematic of SiC high power electronics devices for Toyota's HEV (Hybrid electric Vehicle), FCEV (Fuel Cell Hybrid Vehicle). [94]

Chapter 3. Experimental procedure

3.1. Sample preparation

3.1.1. 4H-SiC wafer

Research grade on-axis 4H-SiC (0001) substrates were purchased from Cree Inc. Unlike other off-axis wafers that are available in product grade, only research grade is available for on-axis substrates. 8 × 8 mm^2 specimens cut from a 100 mm diameter 4H-SiC Si-face on-axis chemical mechanical polishing (CMP) polished wafer were used for the experiment. Nominal off-cut angle of the substrates measured by the supplier was 0 – 0.04 degree.

3.1.2. Surface cleaning

Several steps of cleaning were deliberated to minimize the formation of oxide layer and contaminants. As a surface treatment, cleaning steps consist of largely two parts, organic cleaning and RCA (Radio Corporation of America) cleaning. As an organic cleaning, acetone, methanol and isoprophyl alcohol (IPA) were used for 10min, 1min and 1min respectively. As a RCA cleaning, firstly, H_2O_2 : H_2SO_4 = 1 : 4 solution (SPM) was used for 10 min at 100 ^oC. Then, H_2O_2 : NH_4OH : Deionized (D.I) water = 1 : 1 : 5 solution (SC1) was used for 10 min ant 70 ^oC, and H_2O_2 : HCl : D.I water = 1 : 1: 6 solution (SC2)

was used for 10 min at 70 ^{o}C. Between each step, Hydrogen fluoride (HF) : D.I water = 1 : 9 solution was used to remove the native oxide layer.

3.2. CVD system modification

The CVD system consist of (1) the reaction chamber made in quartz, (2) the vacuum system which includes two mechanical pump and one turbo molecular pump, (3) the gas inlet and exhaust lines, and (4) the control panel including the pressure control system. Fig. 3.1 shows the schematic diagram of cold-wall, horizontal-type CVD system. Fig. 3.2 shows the schematic diagram of the SiC-coated graphite susceptor and quartz boat. This system is almost the same as that described in detail by W. Bhang. [95]

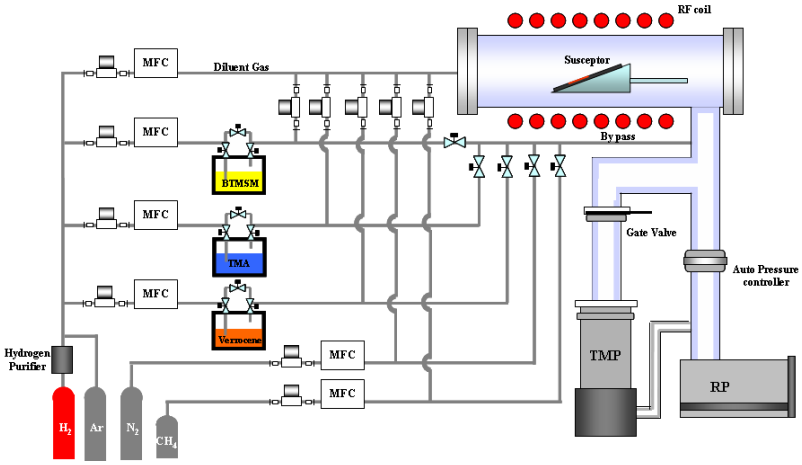

Figure 3.1 Schematic diagram of MOCVD system

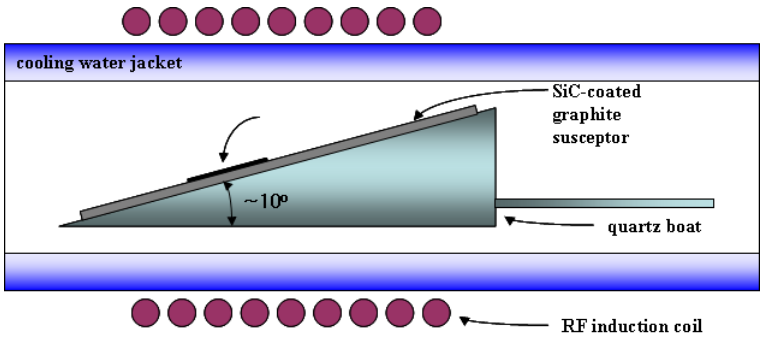

Figure 3.2 The schematic diagram of the reactor chamber of CVD system.

3.3. Procedure for the Growth of 4H-SiC Epitaxial Layer

The 4H-SiC epitaxial films were deposited on the n-type 4° off-axis 4H-SiC Si-face, C-face, and on-axis substrates by low-pressure chemical vapor deposition (CVD). A horizontal cold wall system with a SiC coated graphite susceptor was used, which was inductively heated by an RF generator. The substrates were double-side polished n-type 4H-SiC Si-face and C-face wafers with 4° off-orientation toward the $[11\bar{2}0]$ direction. The substrate temperature was measured using an optical pyrometer which was calibrated with the melting temperature of Si (1418 ℃). Prior to the growth, the substrates were sequentially cleaned with acetone, methanol, H_2SO_4/H_2O_2 = 4:1 at 130 ℃, and diluted HF, and then rinsed with deionized water in order to remove the surface contamination and native oxide layer. Before the epitaxial growth, *in situ* H_2 pre-etching was done for 10 min to remove the damaged scratches and substrate imperfections such as voids and dislocations. The H2 pre-etching temperature and pressure were 1450–1500 ℃ and 180 Torr, respectively. The growth temperature and the bubbling gas flow rate of BTMSM source ranged between 1240 ℃ and 1550 ℃ and 5 sccm to 20 sccm, respectively. The BTMSM canister was immersed into a water bath and maintained at 24 ℃, which was controlled by a thermostat device with a circulation pump (LAUDA E100, temperature control ±0.02 ℃). The vapor pressure of BTMSM source at 24 ℃ was roughly estimated to be 13.55 torr by using Clausius-Clapeyron equation. The actual flow rates of BTMSM with

H_2 bubbling gas flow rate of 5–20 sccm were also calculated to be 0.41–1.63 sccm, respectively. The input flow rate of the diluent gas, H_2, was maintained at 3000 sccm and the pressure in the growth chamber was fixed at 180 Torr. The epitaxial growth was performed for 1-2 hr.

3.3. Characterization Method

3.3.1. Surface Morphology

The surface morphology of *in situ* H_2-etched substrates and epitaxial films was observed using a Nomarski microscope (NMS; Nicon, Eclipse LV100D), atomic force microscopy (AFM; JEOL, JSPM-5200)

3.3.2 Thickness Evaluation

The thickness of SiC epilayer is very important parameter because it is essential parameter in various SiC based devices. The thickness of epilayers was observed by the scanning electron microscopy.

3.3.3. Structure and Defect Analysis

X-ray diffraction (XRD) analysis was conducted by a PANalytical high resolution X-ray diffractometer with a 2 kW Cu radiation source. Double-axis crystal XRD was used to evaluate the crystallinity. The chemical structure of

the hydrogen etched SiC layers was evaluated by X-ray photoelectron spectroscopy (XPS; Sigma Probe, ThermoVG, U.K.). Micro-Raman spectroscopy was performed to determine the existence of polytype conversion using a Horiba Jobin-Yvon LabRam HR spectrometer and detected with a liquid-nitrogen-cooled CCD detector. The 514.5-nm line of an Ar-ion laser was used as an excitation source, and the laser power on the sample was maintained at around 100 μW to avoid heating of the sample by the measuring laser beam. The laser spot diameter was about 1 μm. The Raman signal was collected in a backscattering geometry using a ×100 microscope objective lens. The film uniformity was examined by electron back scattering diffraction pattern (EBSP, Oxford instruments Ltd.), which is a map of the angular variations (Kikuchi lines) in intensity of electrons back-scattered from a crystalline specimen after incident electron beam has been diffracted. The crystallographic relationships between domains were also examined by EBSD. Because EBSD is an add-on package to SEM, it has the capability of diffraction and imaging in real time with a spatial resolution of 0.5um. Because the escape depth of the electron beam is approximately 10 nm, it was used to determine whether the very thin layer is amorphous or crystalline.

3.4. Precursor for Homoepitaxial Growth of 4H-SiC

The precursor for homoepitaxial growth of SiC is bis-trimethylsilylmethane [$((CH_3)_3Si)_2CH_2$, BTMSM], which is purchased from United Chemical Inc. The boiling temperature and freezing temperature of BTMSM were 137 ℃ (410 K) and -71 ℃ (202 K), respectively. Therefore, the BTMSM is liquid phase at room temperature. The source material is feed into the reaction chamber by the carrier gas, H_2, which flows through liquid BTMSM source in the bubbler. The BTMSM source bubbler was immersed into water bath. The bubbler bath maintained a constant temperature of 24 ℃ by thermostat device with circulation pump. This material has the advantage of non-toxic and non-flammable source, compared to SiH_4, which is conventional gas for Si supply.

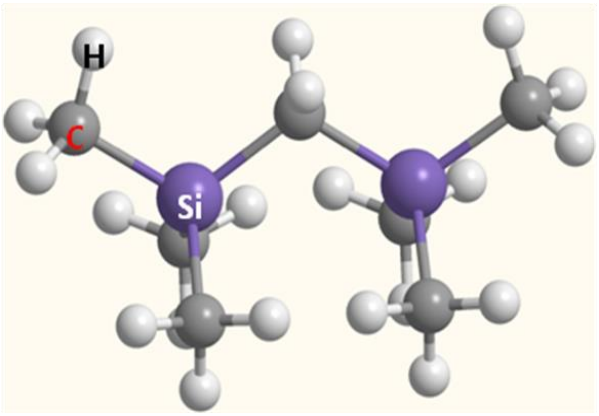

Figure 3.3 The structure of bis-trimethylsilylmethane. Silicon atoms bonded tetrahedrally with carbon atoms, which is the same structure of SiC crystal.

Chapter 4. Results and Discussions

4.1. Homoepitaxial growth of 4H-SiC on Si-face on-axis substrate

4.1.1. Introduction

Silicon carbide (SiC) is a wide bandgap semiconductor possessing properties such as a high decomposition temperature, large breakdown electric field, good thermal conductivity, and high saturation velocity. Because of these unique properties, SiC has been actively studied as the material of choice for high temperature, high voltage, and high frequency applications. [96-98] Different stacking sequences of the Si-C bilayers lead to different polytypes of SiC. As a result, numerous studies on polytypes such as 3C-SiC, 4H-SiC, and 6H-SiC have been reported. [99-101] Such polytypes exhibit different characteristics [102], and it is important to control the formation of polytypes in the crystal growth of SiC. [103]

Currently, for enhancing the polytype stability of SiC homoepitaxy, an off-axis substrate with several degrees off-cut toward the [$11\bar{2}0$] direction is commonly used. [104, 105] However, even though the polytype stability is enhanced in this case, numerous other issues exist. First, the basal plane dislocations (BPDs) are transferred into the epilayer from the substrate. BPDs

are known as “killer defects,” which when present within the epilayer, largely degrade the forward voltage of the bipolar device. [106, 107] Second, the number of wafers obtained decreases when the substrate is cut along the off-cut direction in the SiC ingot. In recent years, there has been an alarming increase in the amount of discarded SiC ingots as the sizes of wafers have increased. Third, anisotropies of the epilayers can appear along the step-flow direction because of the off-cut angle. These include not only structural anisotropies [108], but also anisotropies in the channel mobility or the threshold voltage in trench metal-oxide-semiconductor field-effect transistors because of the dependence of the metal-oxide-semiconductor interface on the face polarity. [109-111]

Hence, in order to solve these issues, it is essential to study epitaxy in nominally on-axis substrates. However, because of the low step density in nominally on-axis substrates, there is a possibility of creating unintended polytypes on epitaxial layers. [112-114] This polytype instability has been the biggest problem faced in the study of on-axis epitaxy. Currently, hydrogen etching prior to the deposition of the epilayer is considered to be a crucial step for achieving homoepitaxial growth in epitaxy with nominally on-axis substrates. [115-118] Hassan et al. reported that hydrogen etching in a Si-rich environment increases the polytype stability of the epilayer. [115] Kojima et al. reported the enhanced morphology and polytype stability of the epilayer on the C-face substrate after etching when compared to the Si-face substrate. [116]

However, it is not clear which characteristics of the etched substrate

actually enhance the polytype stability of the epilayer. Moreover, most of the on-axis epitaxy studies use source materials that have C/Si ratios of less than 1.0. [115-117] If the source with low C/Si ratio is used, the surface diffusion length becomes longer, which is advantageous for improving the polytype stability on the on-axis substrate. [119] However, a major disadvantage in such low C/Si ratio sources is that it becomes difficult to control the doping concentration because of the increased carbon vacancy. [120]

In this study, we investigated the etching characteristics of Si-face on-axis substrates and report on the effect of these characteristics on the polytype stability of the epilayer grown using bis(trimethylsilyl)methane (BTMSM) source with a high C/Si ratio of 3.5. By understanding the correlation between the etching characteristics and the epilayer, we controlled the micro-steps of the etched substrates and improved the polytype stability of 4H-SiC up to 99%.

4.1.2. Etching characteristics of on-axis substrates

Prior to epilayer deposition, it is essential to etch the substrate with hydrogen to remove the damage due to polishing. [122, 123] In order to optimize the experimental conditions for hydrogen etching of on-axis substrates, we varied the etching temperature from 1300 ℃ to 1600 ℃. Fig. 4.1(a)–4.1(d) illustrate the optical images of the hydrogen-etched specimens at 1300 ℃, 1400 ℃, 1500 ℃, and 1600 ℃, respectively, for 10 min. Though

no special feature is observed at 1300 ℃ (Fig. 4.1(a)), it can be seen that hexagonal etch pits appear at 1400 ℃, like in region 1 in Fig. 4.1(b). The inset in Fig. 4.1(b) is a magnified image of the etch pit. In addition, wavy step-like structures appear at 1500 ℃ (Fig. 4.1(c)) and 1600 ℃ (Fig. 4.1(d)). Degradation of the nominally off-axis substrates is frequently observed because of step-bunching, which is the direct result of high-temperature hydrogen etching. However, the behavior of the on-axis substrates appears to be quite different from the case of the off-axis substrates. The evolution of the etch pit occurred at a relatively low temperature of 1400 ℃ and step-bunching started at and above 1500 ℃. In contrast, no significant change was observed after etching at 1500 ℃ for 4° off-axis or at 1600 ℃ for 8° off-axis substrates in our system. This result implies that the on-axis substrates degraded even at low temperatures because of etching when compared to off-axis substrates. There have been several reports that state that step-bunching increases at smaller tilt angles of the substrates. [124-126] The exact mechanism for this observation is not well understood, but step bunching phenomenon in the low angle off-axis substrates may be related to the stepped structure of the vicinal faces with low inclination angle for the ideal (0001) plane.

To investigate the surface of specimens microscopically, $5 \times 5\ \mu m^2$ AFM images and root-mean-square (RMS) roughness of the substrates etched at temperatures ranging from 1300 ℃ to 1600 ℃ and of the bare wafer (unetched) are shown in Fig. 4.2. For specimens etched at temperatures between 1400 ℃ and 1600 ℃, the morphology may vary depending on where

the AFM measurements are performed. Fig. 4.2 shows a general area without the specific morphologies (etch pits for 1400 ℃, bunched steps for 1500 ℃ and 1600 ℃). AFM images of such specific regions are shown in Fig. 4.3. The RMS roughness of the bare wafer is 1.02 nm, and it is slightly larger than those of other commercial product grade off-axis substrates (< 0.75 nm). Scratches due to rough mechanical polishing were not observed. Though the macroscopic morphologies degraded because of etching at high temperatures (Fig. 4.1), microscopic RMS roughness values of the etched substrates are lower than that of the bare wafer, irrespective of the temperature. This implies that any damage to the wafer because of polishing is effectively removed during the hydrogen etching process. From the AFM images, we observe that uniform steps are formed on the surface at etching temperatures of 1500 ℃ and 1600 ℃. Such uniform steps were unexpected, as they did not exist prior to the high temperature etching process. In general, while steps of several nanometers are created because of step-bunching at high temperature [127-129], in our case, the on-axis substrates exhibited regular steps with uniform height. The heights of these micro-steps were 1 nm, which is consistent with the unit-cell height of 4H-SiC. Regular micro-steps of unit-cell height have been reported in several studies for both on-axis 4H- and 6H-SiC. [115, 125, 130, 131] There are several explanations for the origin of the micro-steps. Some researchers suggested that micro-steps originate from the etching of screw dislocations. Hassan et al. investigated the etched surface of 4H-SiC and reported that regular micro-steps form from elementary screw dislocations, and then spread over the entire surface. [125] Another

explanation is that micro-steps arise from the unintentional miscut of the wafers, which is related to the stacking sequences of the Si-C bilayers. Nakajima et al. claimed that the anisotropic etching rate of vicinal surfaces leads to the step structures of the 6H-SiC surface. [130] Interestingly, the generation of steps because of the etching of the screw dislocations was also reported in the same study.

In our case, the etching of threading screw dislocation (TSD) appears to influence the formation of the micro-steps. In order to understand the origin of the micro-steps, it is important to note that etch pits first appeared at 1400 ℃. The AFM image of the etch pit at 1400 ℃ is shown in Fig. 4.3(a) (region 1 in Fig. 4.1(b)). From Fig. 4.3(a), it can be seen that uniform steps were created at the center of the etch pit, while no micro-steps were observed at the periphery of the etch pit in Fig. 4.3(b) (region 2 in Fig. 4.1(b)). Steps in the etch pit have a height of 1 nm, as shown in the profile with an arrow in Fig. 4.3(a), and this is consistent with the lattice parameter (*c*) of 4H-SiC. In addition, the density of the etch pit is approximately 5×10^3 cm^{-2}, determined from the optical microscope image. The average concentration of TSDs on the substrate was determined to be 3.8×10^3 cm^{-2} using molten KOH etching of six different areas, which is similar to the density of the etch pits. Here, the density of the measured TSDs is a little higher than that of other commercially available off-axis wafers ($< 1 \times 10^3$ cm^{-2}). When the height of the step and the concentration of the etch pits are considered, it appears that this etch pit arises because of selective etching of TSD.

On closer observation of the specimen surface, it can be seen that etching

at a high temperature (1500 ℃), as shown in Fig. 4.3(c) (region 3 in Fig. 4.1(c)), results in micro-steps created throughout the entire specimen, unlike etching at low temperature. Notably, the direction of the steps was always perpendicular to the <$1\bar{1}00$> direction group, and step height corresponds to the strength of the Burgers vector of the screw dislocation (1 nm). Other than these regular micro-steps, bunched steps were observed in some parts of the specimen, as representatively shown in Fig. 4.3(d) (region 4 in Fig. 4.1(c)). These bunched steps had a step height of several nanometers to tens of nanometers. The bunched steps can be formed from the merging of micro-steps because of the high etching temperature, or step-bunching of an unintentional off-cut. [131] Their exact origin is unclear currently, but it is evident that more bunched steps with a larger height form at increased etching temperatures. Notably, the micro-steps disappear at the peripheral part of a bunched step, as seen in Fig. 4.3(d). It is important to understand how these micro-steps created during the etching process affect the epitaxial growth, as discussed later.

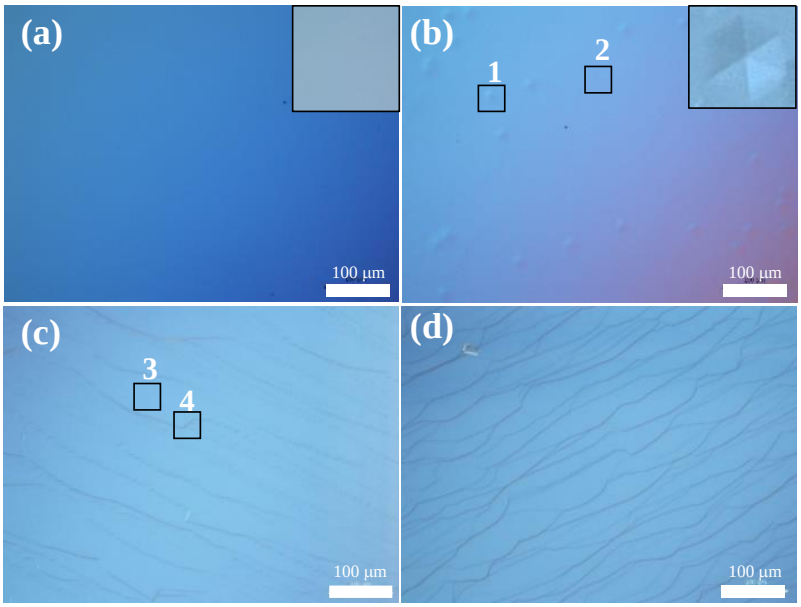

Figure 4.1 Optical images of the surface of the substrates etched at temperatures of (a) 1300 ℃, (b) 1400 ℃, (c) 1500 ℃, and (d) 1600 ℃ for 10 min. The surface of the bare wafer is shown as inset in (a) with the same scale. Regions marked 1 and 2 in (b) are etch pit (1) and the periphery of etch pit (2) of the etched substrate. Regions marked 3 and 4 in (c) are the micro-steps (3) and the bunched step (4) of the etched substrate. The inset in (b) is a magnified image of the etch pit.

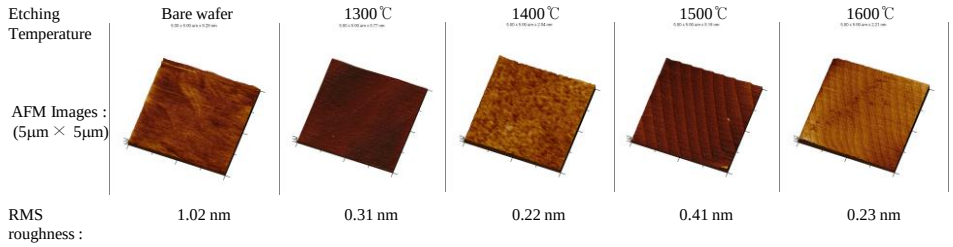

Figure 4.2 AFM images (5 × 5 μm^2) and RMS values of bare wafer and specimens that were etched at temperatures from 1300 ℃ to 1600 ℃ for 10 min.

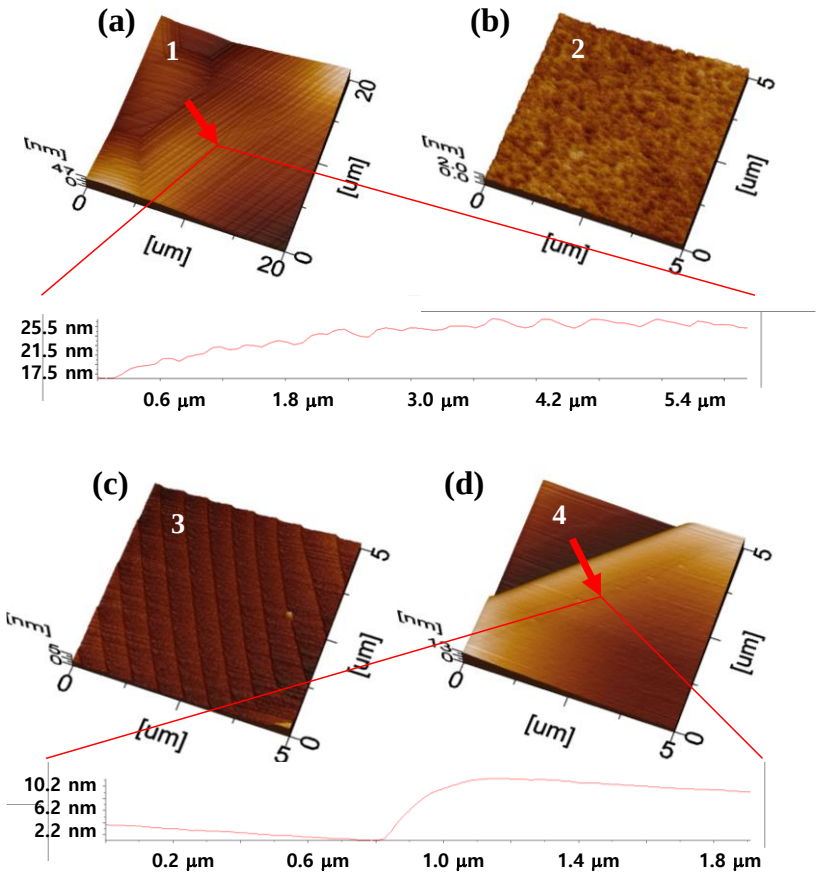

Figure 4.3 AFM images of (a) etch pit (20 × 20 µm^2, region 1 in Fig. 1) and (b) peripheral part of the etch pit (5 × 5 µm^2, region 2 in Fig. 1) of the substrate etched at 1400 ℃ for 10 min. 5 × 5 µm^2 AFM images of (c) micro-step (region 3 in Fig. 1) and (d) bunched step (region 4 in Fig. 1) of the substrate etched at 1500 ℃ for 10 min.

4.1.3. Epitaxial growth on on-axis substrates with various etching temperature

Fig. 4.4(a)–(d) illustrate the top-view optical micrographs of the epilayers grown for 1 h at a deposition temperature of 1550 ℃ after hydrogen etching at various temperatures between 1300 ℃ and 1600 ℃ for 10 min, respectively. Notably, large hillocks can be seen in the optical microscope images of the grown specimen (dotted lines and triangles). Hillocks in Fig. 4.4 may look concave compared to the surroundings, though it is actually convex. It's because pseudo 3D appearance of the DIC imaged specimens is affected by translation of the objective Nomarski prism. The growth mechanism of SiC layers can be classified into three types. Hillocks are formed from the spiral growth with TSD in the center, and they are common for various on-axis substrates (not only in SiC). [132-134] The second mechanism is step-flow growth through the step of the substrate. This step-flow growth may occur at micro-steps generated during the etching process. The third mechanism is growth by nucleation on the terrace and it shows a high probability of growth of other polytypes. [135] Other regions observed in Fig. 4.4, except hillocks, may form following the second and/or third mechanisms. These two mechanisms are indistinguishable in the optical microscope images.

We can observe the polytype through EBSD mapping of the surface of the epilayers grown after etching at temperatures of 1400 ℃ and 1500 ℃, as shown in Fig. 4.5. The red area in the mapping image shows an area with 4H-SiC polytype, whereas the black area shows an area with other polytypes. The

polytype of the black area was not identified from the EBSD mapping, but it was revealed to be 3C-SiC by Raman analysis as discussed in the following paragraph. All the hillocks seen in the optical image are 4H-SiC (dotted regions). This can be attributed to the fact that the screw dislocation acts as a growth site in the on-axis substrate and it supplies a step with a 1c (unit cell height) Burgers vector, transferring the 4H polytype stacking sequence to the layer. In other areas, we can observe a mixture of 4H-SiC and other polytypes. They are probably grown by step-flow mode to 4H, and by nucleation to form other polytypes.

Raman analysis confirms the polytypes of the deposited layer. Fig. 4.6 shows the results of Raman analysis on several regions of the epitaxial layers grown at 1550 °C for 1 h. Etching was performed at 1500 °C for 10 min before growth. As in the case of EBSD mapping, shown in Fig. 4.5(b), it is seen that only the 4H-SiC-related peaks were detected in the hillocks ($4H_h$ in Fig. 4.6(a)). Regions other than hillocks can be divided into 3C-SiC ($3C_1$ and $3C_2$) and 4H-SiC ($4H_1$ and $4H_2$) domains using the Raman spectra. As shown in Fig. 4.6(b), the FLO peak of 3C-SiC at 971 cm^{-1} is observed in the 3C domains. On the other hand, only the FLO peak of 4H-SiC at 964 cm^{-1} is observed in the 4H domains. Notably, some of the 4H domains have a small FLO peak of 3C-SiC at 971 cm^{-1} because of 3C inclusion, as shown in a representative $4H_1$-2 region in Fig. 4.6(c). The intensity of the FLO peak of 3C because of the inclusions is weaker than that in the 3C domains such as $3C_1$ and $3C_2$. Generation of different polytypes within the same crystal bulk and specific mechanism, which is very similar to our case, is reported for

proteins by Aquilano et al. [136]

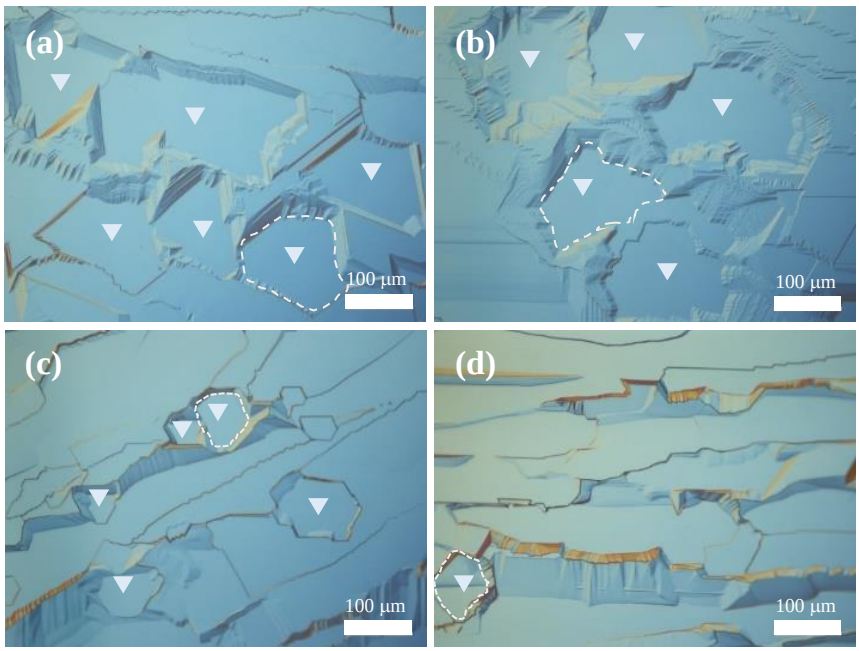

Figure 4.4 Optical images of the surface of epitaxial layers grown for 1 h at 1550 ℃. Specimens are etched before the growth process at (a) 1300 ℃, (b) 1400 ℃, (c) 1500 ℃, (d) 1600 ℃ for 10 min. Triangles and dotted lines indicate the hillocks grown by screw dislocation.

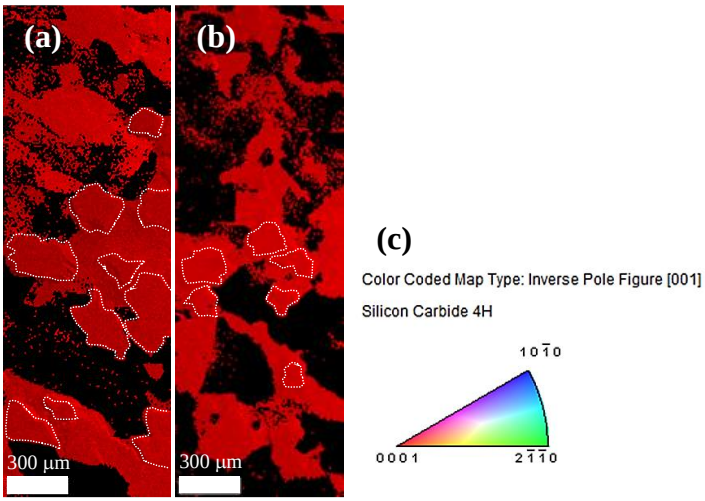

Figure 4.5 (a), (b) EBSD maps of epitaxial layers grown for 1 h at 1550 ℃ and (c) inverse pole figure triangle. Specimens are etched before the growth process at (a) 1400 ℃ and (b) 1500 ℃ for 10 min. Dotted lines indicate the hillocks. All the hillocks are 4H-SiC.

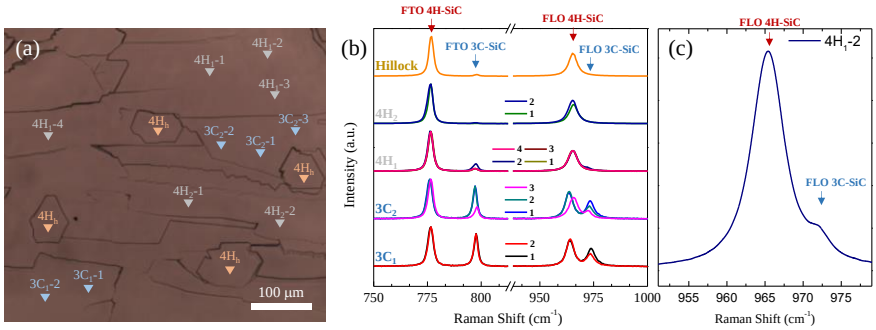

Figure 4.6 Raman analysis results of epitaxial layers grown for 1 h at 1550 ℃. The specimen was etched for 10 min at 1500 ℃ before the growth process. (a) Optical microscope image with hillocks, 3C, and 4H regions. (b) Raman spectra of hillocks, 3C, and 4H regions in the epitaxial layers. (c) Magnified Raman spectra of the $4H_1$-2 region.

4.1.4. Dependence of epilayer characteristics on etched surface

The role of screw dislocation and micro-steps is more evident when we look at the specimen at the beginning of growth. Fig. 4.7 shows optical micrographs of the surface of the layer grown at 1550 ° C for 10 minutes after etching for 10 minutes at 1300, 1400, and 1500 ℃. The optical microscopic image shows that the surface of the layer deposited for 10 minutes after etching at low temperature differs from the surface of the layer deposited for 10 minutes after etching at high temperature. Hillock was formed from the initial stage of deposition on the surface of the deposited layer after etching at low temperature. In steps other than hillock, wavy step-like structures are observed. The surface with these wavy step-like structures is similar to the etched surface at high temperatures. As a result of the SEM measurement to be shown later, it can be seen that in the case of the sample after the etching at low temperature, the deposition is not performed in the region other than the hillock. Therefore, wavy step-like structures are formed by being deteriorated due to the high temperature deposition temperature. On the other hand, for the specimens deposited for 10 minutes after etching at high temperature, as shown in the optical image, it has a surface that seems to be deposited entirely. And hillock is not observed.

The EBSD measurement results of the above samples are shown in Fig. 4.8. The ratio of 4H-SiC was much higher in the specimens deposited after etching at low temperature compared with the specimens etched at high temperatures. However, this is not because of the high ratio of 4H-SiC in the

deposited layer, but because there are many unexposed portions except the hillock region, the substrate is exposed. Therefore, the 4H-SiC of the substrate was measured in the EBSD result, and the red part was increased. On the other hand, in the layer deposited after etching at high temperature, 3C-SiC was included according to EBSD measurement result. It can be seen that 3C has already been generated from the beginning of the deposition.

The cross-sectional SEM images of the specimen with the layer grown for 10 minutes after etching for 10 minutes at 1500 ° and 1400 ° are shown in Fig. 4.9. In the case of the specimen after the etching at 1500 ° C, it was confirmed from the SEM measurement that the layer about 200nm thick was uniformly grown. That is, a uniform layer was grown throughout the specimen from the initial stage of the deposition. On the other hand, in the case of the specimens after etching at 1400 ° C, the hillock region has grown to a thickness of 400 nm or more, but no layer has grown in the other regions. That is layer was selectively deposited only in the hillock region at the early stage of the deposition. These results are similar to the results of the above-mentioned optical image, in which regions other than hillock are similar to etched surfaces at high temperature. The difference in layer growth at the initial stage of deposition with the etch temperature further explains the effect of micro-steps on layer growth. In the case of low-temperature etching, a micro-step is formed only around the etch-pit, and at the initial stage of the deposition, the micro-steps provide a growth site so that the layer is selectively deposited in the hillock region. In the rest of the area, there is no micro-steps and the deposition does not proceed, which is related to the

increased size of the hillock when the deposition time is increased. On the other hand, in the case of the sample after the high-temperature etching, the micro-steps were spread over the entire sample, and the SiC layer of uniform thickness was deposited on the entire sample at the early stage of the deposition. We can once again confirm that micro-steps provide a site where the layer can grow. In the case of the specimen etched at a high temperature, it was confirmed from the result of EBSD measurement that 3C-SiC was generated from the initial stage of deposition. 3C-SiC is nucleated in the bunched-step produced during the high-temperature etching process.

Micro-steps created by etching can act on the epilayers as follows: 1) the micro-steps provide a growth site for step-flow growth on an on-axis substrate that initially did not have a step site. 2) As the stacking sequence of 4H-SiC (ABAC) is revealed on the side walls of the micro-steps, it enhances the polytype stability of the deposited layer. Schematic illustration of the micro-steps exhibiting the stacking sequence of 4H-SiC is shown in Fig. 4.10.

Although micro-steps are present on the entire specimen when etched at high temperature, they cannot explain the growth of other polytypes such as 3C-SiC. Low polytype stability at high-temperature-etched specimens may be affected by the bunched steps observed from the AFM image of the specimen etched at high temperature (Fig. 4.3(d)). Micro-steps disappeared in the peripheral part of a bunched step so that step-flow growth should be weakened. In such a case, other polytypes of 3C-SiC can nucleate. There was a similar report that growth of 3C is promoted by step-bunching, which generates a longer terrace. [135]

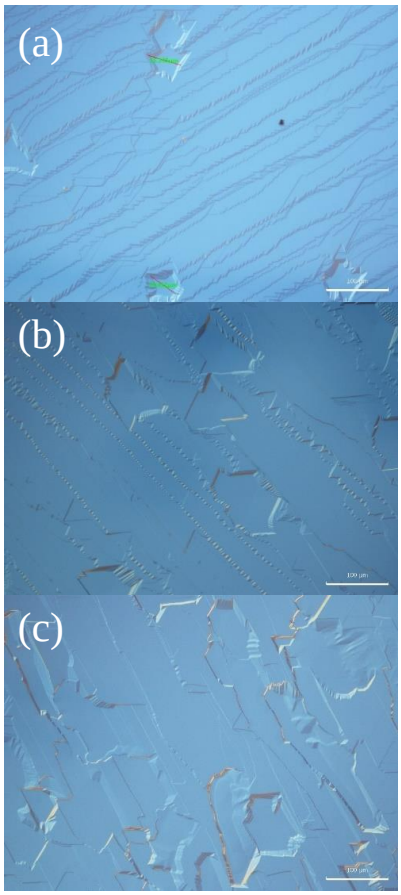

Figure 4.7 Optical microscope images of epitaxial layers grown for 10 min at 1550 ℃. Specimens are etched before the growth process at (a)1300 ℃, (b)1400 ℃ and (c) 1500 ℃.

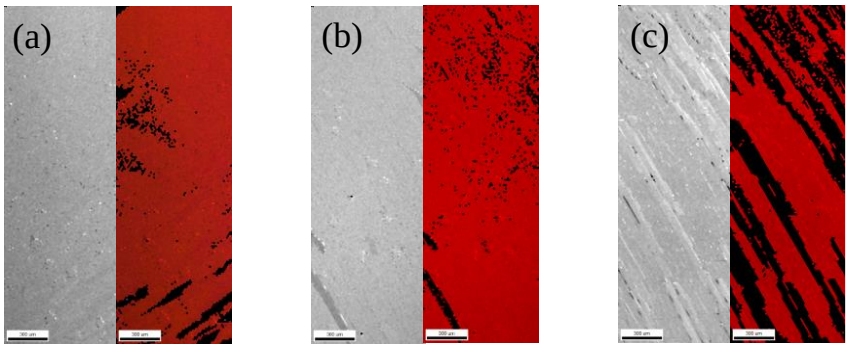

Figure 4.8 EBSD mapping images of epitaxial layers grown for 10 min at 1550 ℃. Specimens are etched before the growth process at (a)1300 ℃, (b)1400 ℃ and (c) 1500 ℃.

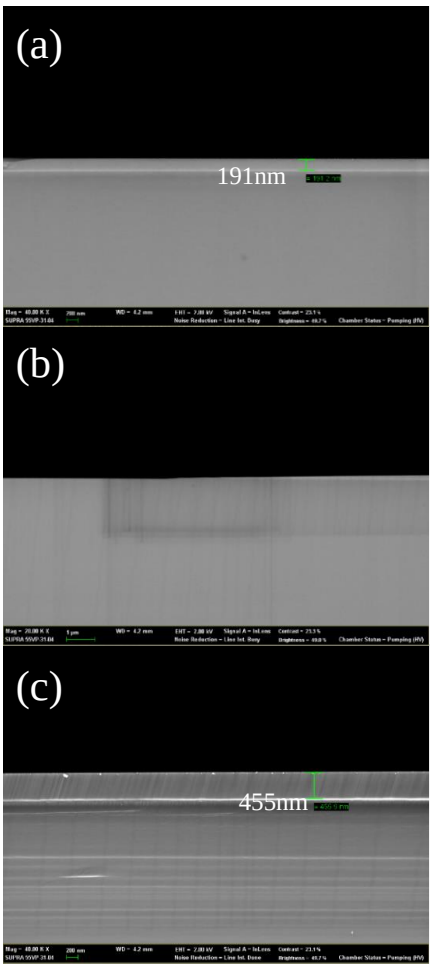

Figure 4.9 Cross sectional SEM images of epitaxial layers grown for 10 min at 1550 ℃. Specimens are etched before the growth process at (a)1500 ℃, (b), (c)1400 ℃. Epitaxial layer was not deposited in other parts except the hillocks in (b). A magnified image of the hillock is shown in (c).

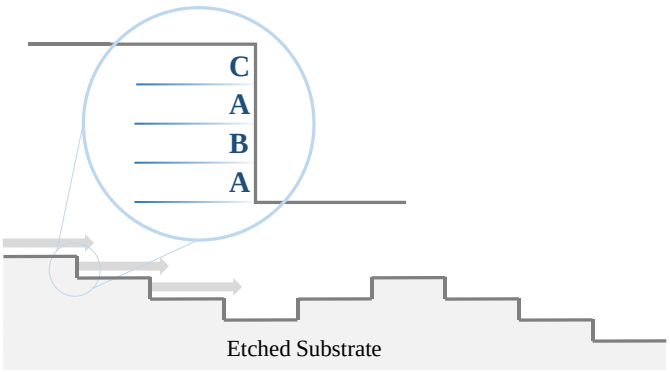

Figure 4.10 Schematic diagram of the generated micro-steps. Stacking sequence of 4H-SiC (ABAC) is revealed on the side wall of the micro-steps.

4.1.5. Enhancing polytype stability of on-axis epitaxy by controlling micro-steps

If a micro-step with a height of 1 nm can provide sites for epilayer growth and improve the stability of the 4H polytype, it is important to make sure that the micro-steps are present in the specimen without step-bunching. At an etching temperature of 1400 ℃, etch pits appeared with selective etching of TSD; however, when etched for 10 min, only micro-steps were formed around the etch pit part. On the other hand, though micro-steps were spread throughout the specimen because of TSD at high temperature, step-bunching occurred. Based on this observation, we attempted to realize micro-steps spread throughout the specimen without step-bunching, by increasing the etching duration at a temperature of 1400 ℃.

Fig. 4.11(a) shows the optical image obtained using a Nomarski microscope of the surface of the specimen in which we increased the etching duration to 90 min at a temperature of 1400 ℃. It is shown that the etch pit disappeared compared to the case for the 10-min-etching (Fig. 4.1(b)). In addition, it shows a better surface morphology than the specimen etched for 10 min at 1500 ℃ (Fig. 4.1(c)). Formation of uniform steps throughout the surface was observed from the AFM image in Fig. 4.11(b). For the specimen etched for 90 min at 1400 ℃, we found that there are regions with step-bunching, as shown in Fig. 4.11(c) and the bunched step had a height of about 3 nm maximum. However, this step bunching was very rare compared to the etching at high temperature.

In the case of the specimen with the layer deposited after revised etching process, the difference can be seen at the initial stage of the deposition. Fig. 4.12 shows the optical micrographs and cross-sectional SEM measurement of the surface of the SiC layer at the initial deposition after being etched at 1400 ° C for 90 minutes and then deposited at 1550 ° C for 10 minutes. In the optical image, it seems that layer is deposited on the entire specimen as compared with the surface of the specimen deposited 10minutes after etching for 10 minutes at 1400 ℃. Compared with Fig. 4.7(b), the surface is not divided into hillocks and areas with wavy step-like structures. In the modified etching conditions, a uniform layer of about 200 nm was deposited on the entire specimen. This can be attributed to the fact that by increasing the etching time, the micro-steps spread over the entire specimen and the layer was grown through the step-growth in the entire specimen.

Fig. 4.13 shows the EBSD mapping of the epilayers deposited for 1 h after etching for 10–120 min at a temperature of 1400 ℃. The stability of the 4H-SiC polytype improved with increasing etching duration and almost 99% of the 4H-SiC polytype was achieved at 90 min. As the etching duration is increased, the micro-steps spread throughout the specimen and the micro-steps would provide sites for step-flow growth. As a result, the polytype stability is enhanced. The temperature ramp from 1400 ℃ for etching to 1550 ℃ for growth took 30 s. and it is believed that the surface degradation occurring because of step-bunching is insignificant.

Our results demonstrate that it is possible to improve polytype stability using precursors, even with high C/Si ratio, such as BTMSM, in on-axis Si-

face epitaxy and it will provide more control on background doping of the grown epilayers. As mentioned earlier, if C/Si becomes higher, the surface diffusion length becomes smaller. Therefore, it is difficult for adatoms to reach a step because of the short surface diffusion length in the on-axis substrate with low step density compared to an off-axis substrate. Thus, it is highly disadvantageous for step-flow growth. That is, it is difficult to maintain the polytype stability, as nucleation of 3C-SiC is likely to occur. However, by increasing the etching duration at a low temperature and realizing micro-steps spread throughout without step-bunching, we could provide a site for step-flow growth despite this short surface diffusion length, and therefore, we could increase the stability of 4H-SiC.

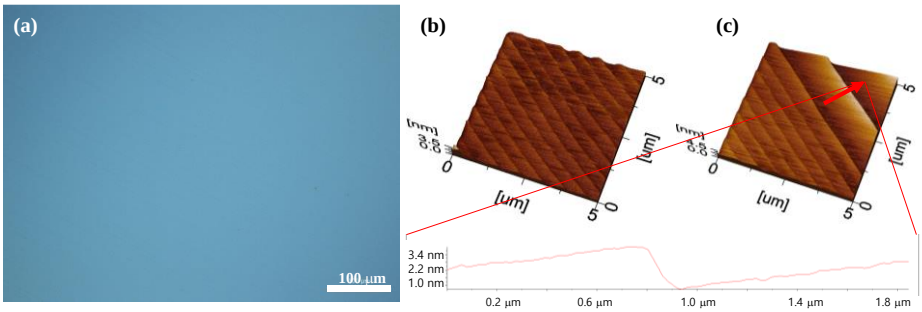

Figure 4.11 (a) Optical image, and 5 × 5 μm^2 AFM images of (b) micro-step and (c) bunched step of a substrate etched at 1400 ℃ for 90 min.

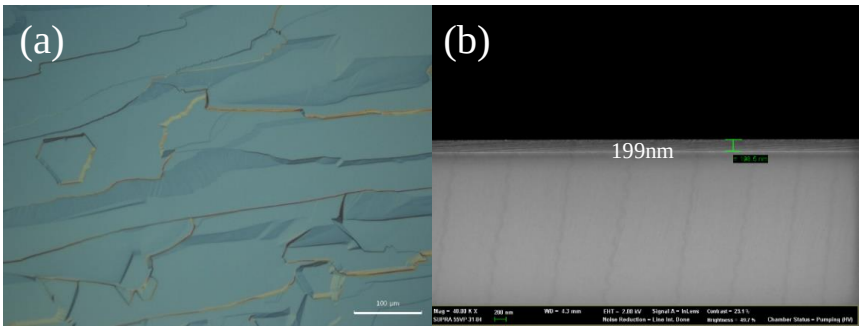

Figure 4.12 (a) Optical and (b) cross-sectional SEM images of epitaxial layers grown for 10 min at 1550 ℃ after etching at 1400 ℃ for 90 min.

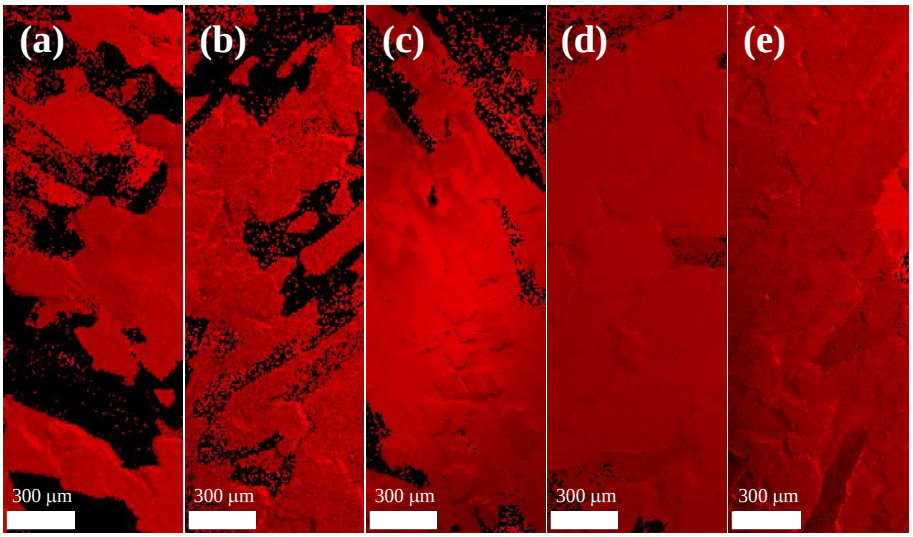

Figure 4.13 EBSD maps of epitaxial layers grown for 1 h at 1550 ℃ after etching by increasing the etching duration. Specimens are etched before the growth process at 1400 ℃ for (a) 10 min, (b) 30 min, (c) 60 min, (d) 90 min, and (e) 120 min.

4.1.6. Considerations on device fabrication

As mentioned in introduction, SiC epitaxial growth is an essential step for device fabrication. In other words, the SiC epitaxial layer must meet the conditions for operating the device. For the on-axis epitaxial growth, it is also an important issue to apply the grown SiC layer to device fabrication. For that, we have enhanced the polytype stability within the epitaxial layer, which is the biggest problem of on-axis epitaxial growth. There are many other considerations in fabricating devices, but investigating all of them is outside the scope of this paper, so we have conducted two additional experiments with an emphasis on application to devices. The first is an experiment on whether polytype stability is maintained even when the thickness of the epitaxial layer is increased, and the second is the experiment of fabricating the diode with on-axis epitaxial layer.

The SiC device has the greatest advantage of being able to operate at high voltage and thus is the most utilized as a high voltage power device. The thickness of the epitaxial layer required for it is about 10 to 15 μm. The thickness of the SiC layer grown in this study is about 1 μm and thinner than that. It is important that the polytype stability is maintained even if the SiC layer becomes thick. However, as a system used in this study, it is practically difficult to directly grow an epilayer of 10 μm or more. This is due to the low growth rate (1 um / h) and thus the long process time and equipment degradation at high temperatures. Therefore, we have examined the surface of the epilayer more closely to determine whether the polytype stability in the

thicker epilayer is maintained indirectly. If the micro-steps that were formed at etching process were to be maintained during epitaxial growth, the sites for step-flow growth would be maintained and the stability of 4H-SiC would be maintained even if the epilayer is thick. Fig. 4.14 shows AFM images of the surface of the epilayer grown for 1h after hydrogen etching at 1500 ℃ for 10 minutes. AFM images show the surface of the layer grown with 4H-SiC and the surface of layer grown with 3C-SiC. Looking more closely at the surface of the 4H-SiC region, regular micro-steps are observed on the surface. In other words, it was confirmed that the micro-steps were maintained during the growth of the epilayer, and it can be deduced that 4H-SiC can grow to thicker thickness through the step-flow growth. On the other hand, no micro-steps were observed in the 3C-SiC region. This is because 3C-SiC has grown through nucleation rather than step-flow growth.

Although the thickness is not sufficient, the diode was fabricated on the grown on-axis epitaxial layer and the electrical properties were investigated. The structure of the Schottky barrier diode (SBD) is shown in Fig. 4.15. The SBDs were fabricated by using 32%, 83%, and 99% of 4H-SiC in the SiC layer, respectively. I-V measurement results of the fabricated diode are shown in Fig. 4.16. As the ratio of 3C-SiC in the epitaxial layer increased, the leakage current of the diode increased. The forward characteristics of the device also depend on the polytype stability and the better the polytype stability, the better the characteristics. The performance of the device is not good compared to devices that use off-axis substrates, because the surface quality of the on-axis epitaxial layer is poor. If the surface of the SiC layer is

controlled by mechanical polishing and then device is fabricated, the device with better characteristics can be fabricated.

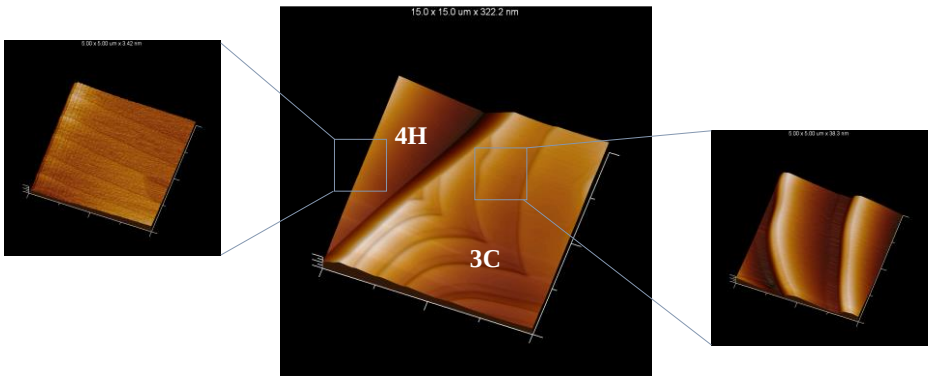

Figure 4.14 AFM images of the surface of the epilayer grown for 1h after hydrogen etching at 1500 for 10 minutes.

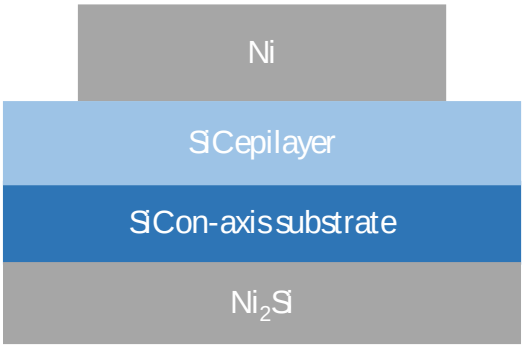

Figure 4.15 Schematic structure of fabricated Schottky barrier diode.

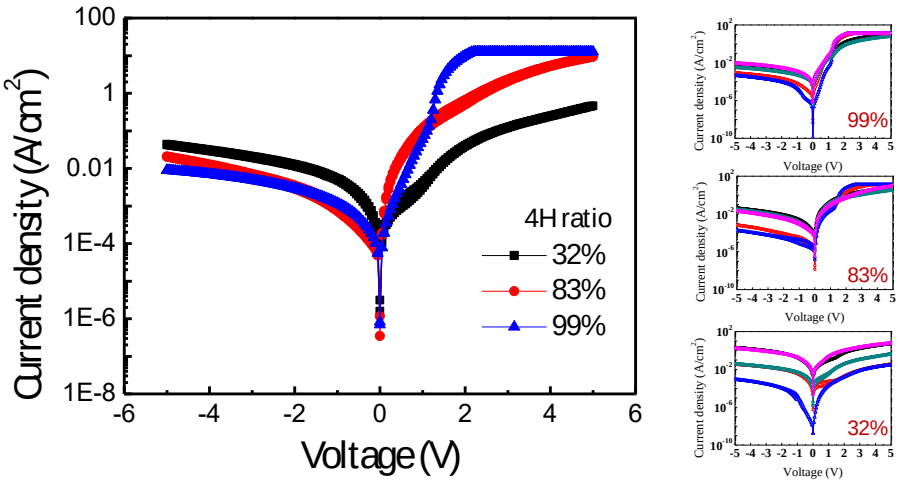

Figure 4.16 I-V Characteristic measurement results for fabricated diodes.

4.2. Homoepitaxial growth of 4H-SiC on C-face on-axis substrate

4.2.1. Introduction

As mentioned in Chapter 2, silicon carbide epitaxy can be achieved in many growth planes. The existence of these multiple growth planes is attributed to the crystal structure of silicon carbide, and the characteristics and growth conditions of the epilayer may vary from one growth plane to the other. At present, Si-face and C-face are mostly used for epitaxial growth of homoepitaxy of α-SiC and many studies have been made. Industrially, Si-face growth is mainly used because deposition is relatively easy due to the wide window of layer growth, and it is easy to control the background doping concentration. On the other hand, C-face has been relatively less used than Si-face. The biggest problem of C-face epitaxy is that it is difficult to control background doping concentration due to auto-doping of nitrogen atoms. However, there are also advantages to be gained by using C-face. First, there is an advantage that the channel mobility in the device is higher and the oxidation rate is faster than the Si-face. [104, 137] Especially, in the homoepitaxy on the on-axis substrate, the C-face growth surface has an advantage compared to the Si-face. This is because the low surface energy of the C-face makes it easy to control the surface morphology during the high temperature process. It has been reported that using C-face for on-axis epitaxy

enhances the stability of polytype in epilayer and has a good surface compared to Si-face. Kojima et al. reported successful homoepitaxial growth on a C-face on-axis 6H-SiC substrate. [116] In this literature, epitaxial growth on Si-face and C-face on-axis was conducted and showed that the epitaxial layer with a better polytype stability was grown on the C-face substrate. This is explained by the low surface energy of C-face as mentioned above.

In this study, we report the results of epitaxial growth on a C-face 4H-SiC on-axis substrate using a BTMSM source. We investigated the etching characteristics and epitaxial growth characteristics of C-face on-axis substrate and analysed the factors affecting polytype stability compared with Si-face. Based on this, we will discuss how to improve polytype stability for C-face on-axis epitaxy. In particular, high C/Si can be a solution to the problem of background doping control in C-face mentioned above. The C/Si ratio of the BTMSM source used in this study is as high as 3.5, which is considered to be a great help in solving the background doping problem compared with the case of the on-axis C-face epitaxy reported so far.

4.2.2. Epitaxial growth on C-face on-axis substrates with conventional etching process

At first, in-situ hydrogen etching and layer growth were performed in the same conditions as those of the off-axis substrate prior to the full-scale experiments on the etching condition and growth mechanism of C-face on-

axis epitaxial growth. Fig. 4.17 shows the EBSD measurement results and optical micrographs of the surface of the SiC layer grown for 1h at 1550 ℃ after 1 hour of hydrogen etching at 1500 ℃ on the on-axis C-face 4H-SiC substrate, same as the condition of epitaxial growth on 4° off-axis. Optical images show very poor surfaces. As a result of the EBSD measurement, the ratio of 4H-SiC is very low, that is polytype stability is very low. In comparison with the on-axis Si-face deposited under the same conditions, the surface morphology of the deposited layer was not good compared to the Si-face. At the same time, it was confirmed that the polytype stability is lower than that of Si-face. The black areas in the EBSD measurement were identified as 3C-SiC by Raman measurements shown in Fig. 4.18. These results are in contrast to those reported earlier, in which polytype stability is higher than Si-face in C-Face for on-axis epitaxial growth. In this paper, we analyze the etching characteristics of C-face and results of C-face on-axis epitaxial growth using the BTMSM source, and compare the growth mechanism of the two growth planes. In addition, we will analyze the factors affecting the stability of the polytype on C-face on-axis to investigate how to improve the polytype stability.

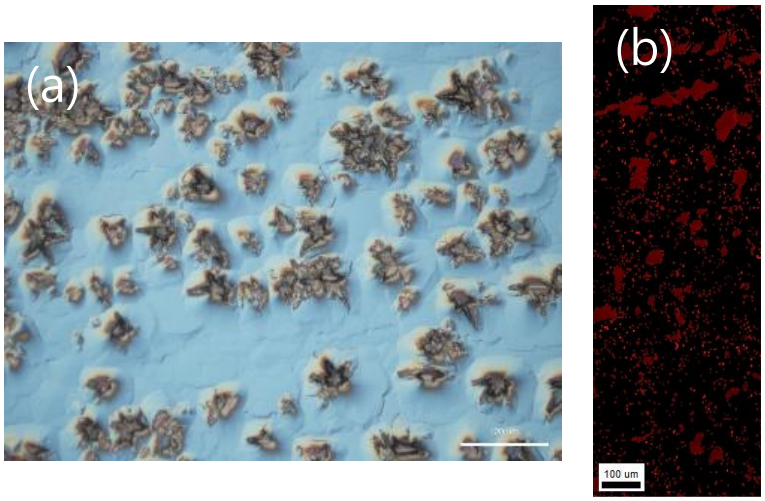

Figure 4.17 (a) Optical image (b) EBSD maps (b) of SiC layers grown for 1 h at 1550 ℃ with conventional etching condition.

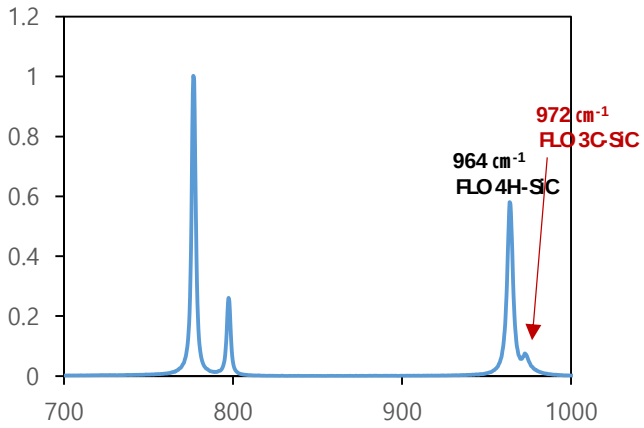

Figure 4.18 Raman analysis results of SiC layers grown for 1 h at 1550 ℃ with conventional etching condition.

4.2.3. Epitaxial growth on C-face on-axis substrates with revised etching process

As can be seen from previous Si-face experimental results and other literature, hydrogen etching conditions and properties have a large influence on the polytype stability of the epilayer on the on-axis substrate. Therefore, the etching characteristics of C-face on-axis substrate were investigated with various etching temperature before the epitaxial growth. Fig. 4.19 is an image of the surface of the sample etched for 10 minutes with the etching temperature varying from 1300 to 1600 ℃. Looking at the optical images, the tendency of the etching characteristics for the temperature is very similar to the Si-face, which shows a surface with no characteristic at the etching temperature of 1300 ℃. A hexagonal etch pit appears when the etching temperature reaches 1400 ℃. When the temperature is higher than 1500 ℃, the surface is deteriorated due to the high temperature. It is more severely deteriorated at 1600 ℃ than at 1500 ℃. This overall trend is the same as for Si-face, but there is a clear difference between the surfaces of etched specimens at high temperatures. In the case of C-face, it can be seen from the images that the surface deterioration of the specimen etched at a temperature of 1500 ℃ or higher is not so severe as compared with the Si-face. This is because the surface energy of the C-face is smaller than that of the Si-face as mentioned above, and the advantage of the C-face under the high-temperature process is as it is.

Fig. 4.20 shows the results of AFM measurement of the bare wafer and

the surface of the etched specimen by temperature. The RMS value of the hydrogen-etched specimen is smaller than that of the bare wafer because the wafer's polishing-related scratch was removed by hydrogen etching. At an etching temperature of 1500 ° C or higher, a uniform step on the surface can be seen, which is seen as the creation of micro-steps like Si-face.

Fig. 4.21 (a) shows the AFM image of the surface of etched sample at 1400 ° C. It can be seen that a hexagon shaped etch pit and the internal height profile to confirm that there are micro-steps inside the etch pit. As shown in Fig. 4.21 (b), there is no micro-step in the region other than the etch pit because the micro-steps do not spread over the entire specimen due to the low etching temperature as in Si-face. In the hydrogen etching process of the C-face on-axis substrate, micro-steps spread out from the screw dislocation of the substrate like the Si-face. At low temperature, the etch rate was not fast, so micro-steps exist only in the etch pits centered on screw dislocation. At higher temperatures, the etch rate is faster, indicating that micro-steps have spread throughout the specimen.

Although there is less deterioration of the surface at the high temperature compared to the Si-face due to the small surface energy of the C-face, a step-bunching phenomenon during the high-temperature etching process is observed. Fig. 4.22 shows the bunched-step from AFM measurements of the etched samples at 1600 ° C. Although the height is smaller than that of the Si-face, it can be seen that the micro-steps also disappeared around the bunched step.

In this bunched step, 3C-nucelation is likely to occur, so we used a

method of spreading the micro-steps throughout the specimen without step bunching by increasing the etch time at the low temperature. Fig. 4.23 shows the Nomarski image and AFM image of the hydrogen-etched specimen at 1400 ° C for 120 min. Comparing this with the measurement results of the samples etched for 10 minutes at the same temperature, we can see that the etch pits disappeared because the micro-steps spread throughout the specimen by increasing the etching time. Also, AFM image shows micro-steps of uniform height throughout the specimen, which is different from the case where no step was found elsewhere except inside the etch-pit in a 10-minute etched specimen. In other words, at C-face, by increasing the etching time at the low temperature, micro-steps could be spread throughout the specimen without step-bunching.

The optical micrograph and the EBSD measurement results of the layer grown for 1h using BTMSM source on the C-face on-axis substrate after etching at 1400 ℃ for 120 mins are shown in Fig. 4.24. The optical image shows that the surface of the specimen is not very good, and the EBSD measurement shows that the ratio of 4H in the SiC layer is 17 percent. This is very low compared to Si-face. In the case of Si-face, the 4H ratio of 99% can be achieved by depositing SiC layer on the etched specimen for the same condition. It is surprising that the C-face has a low polytype stability of the deposited SiC layer even though micro-steps are found throughout the specimen without step-bunching before the deposition. In order to explain this, theoretical considerations on step-growth and terrace nucleation in the step, together with the existing experiments on SiC epitaxial growth, will be

discussed to investigate the factors affecting 3C-SiC nucleation.

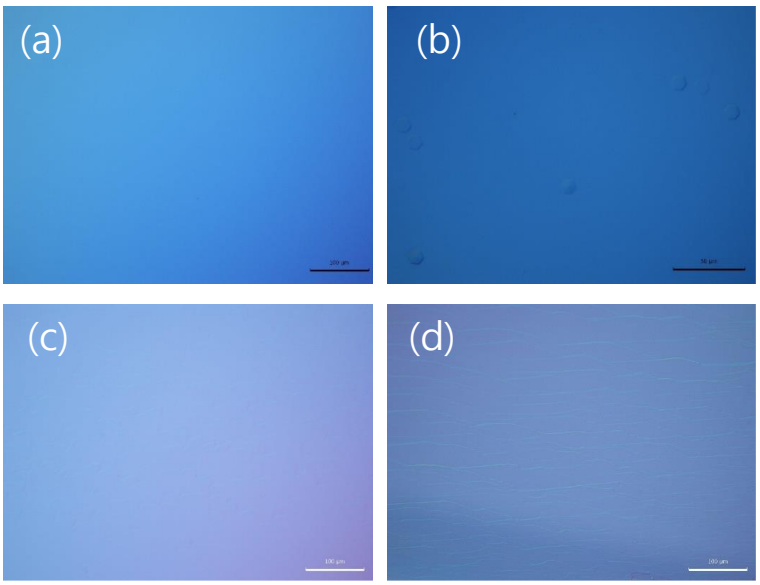

Figure 4.19 Optical images of the surface of the substrates etched at temperatures of (a) 1300 ℃, (b) 1400 ℃, (c) 1500 ℃, and (d) 1600 ℃ for 10 min.

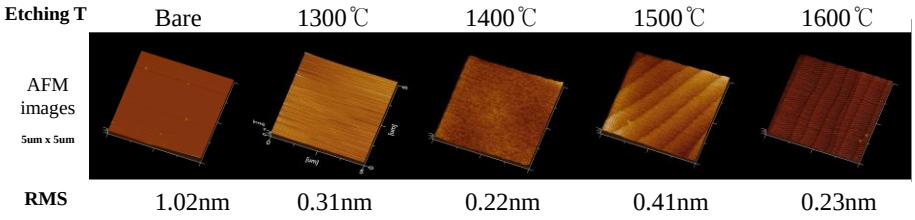

Figure 4.20 AFM images (5 × 5 μm2) and RMS values of bare wafer and specimens that were etched at temperatures from 1300 ℃ to 1600 ℃ for 10 min.

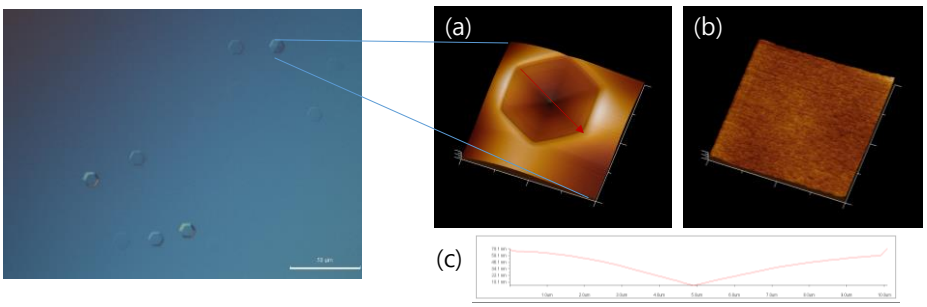

Figure 4.21 AFM images of sample etched at temperatures of 1400 ℃. (a) etch pit, (b) peripheral part of the etch pit (c) height profile of arrow in (a).

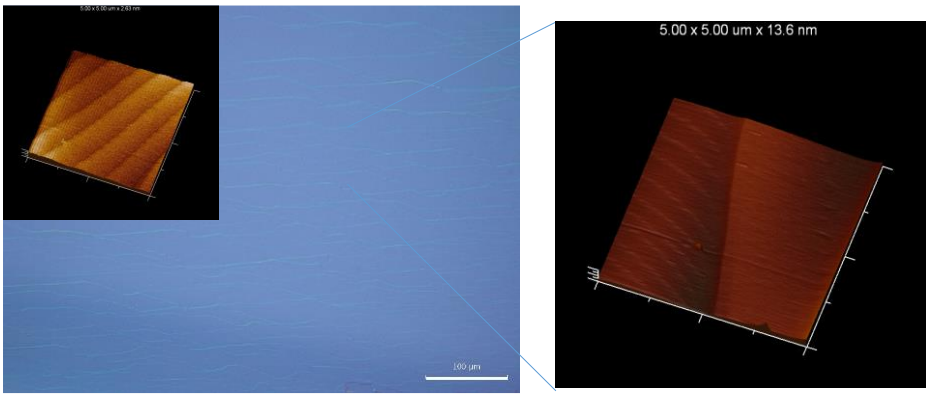

Figure 4.22 bunched-step from AFM measurements of the etched samples at 1600 ℃.

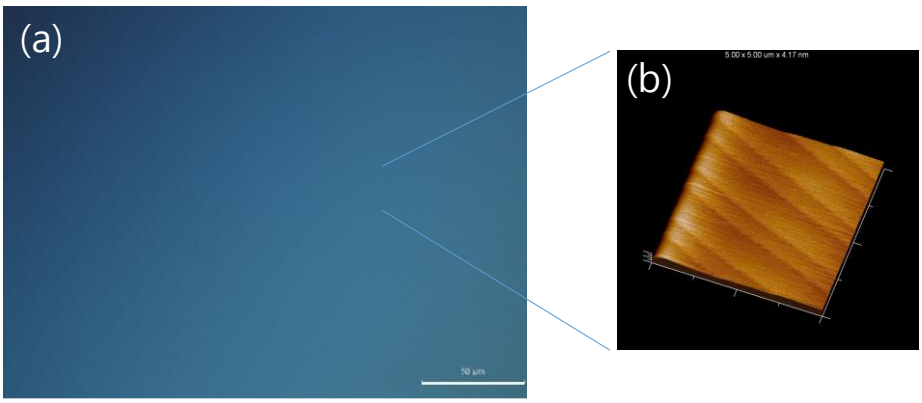

Figure 4.23 (a) Optical image and (b) AFM image of the surface of the substrates etched at temperatures of 1400 ℃ for 120 min.

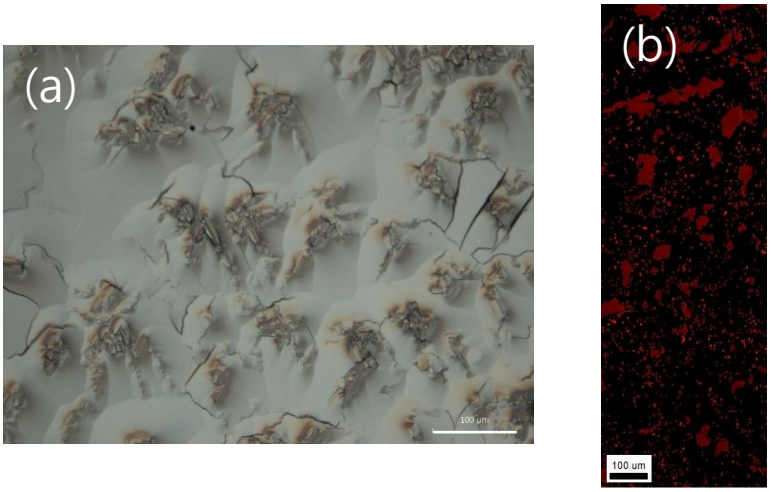

Figure 4.24 (a) Optical image (b) EBSD maps (b) of SiC layers grown for 1 h at 1550 ℃. This sample was etched at 1400 ℃ for 120min before layer growth.

4.2.4. Factors affecting polytype stability of SiC epilayer: theoretical discussion

In order to investigate the factors affecting the 4H stability in the layer in 4H-SiC homoepitaxy on on-axis substrate, BCF (Burton, Cabrera, and Frank) theory [37] and experimental results on SiC epitaxial growth should be considered together. The BCF theory is a common simple surface diffusion model for adatom on step and terrace, but it cannot account for a specific part of the SiC epitaxy, so other experimental results are needed. By combining the above information, it is possible to predict under what conditions the layer will grow through step-flow growth or grow through nucleation. If layer is grown through step-flow growth, it will be grown as 4H-SiC, which has the stacking sequence of the substrate. Or not, 3C-SiC will be nucleated if layer is grown through nucleation.

As shown in the literature review (2.2.1.2), the simple diffusion model in BCF theory shows that the supersaturation ratio α ($\alpha = n_s / n_{s0}$) is distributed as shown in Fig. 4.25. The supersaturation ratio α has the largest α_{max} value at the center of the terrace. If α_{max} is greater than α_{crit}, nucleation occurs. Under these conditions, nucleation will lead to layer growth. In other words,

$\alpha_{max} > \alpha_{crit}$ nucleation occurs

$\alpha_{max} < \alpha_{crit}$ step-flow growth

If α_{max} is larger than α_{crit} and grows through nucleation, the probability of inclusion of 3C increases. Therefore, if we examine how α_{max} and α_{crit} form under certain conditions, i.e., the conditions under which nucleation occurs,

the stability of 4H in the SiC layer can be predicted.

Based on the above theory, we have examined four factors that affect the nucleation density, that is, the stability of 4H polytype.

The first is the terrace length. The longer the terrace length, the greater the α_{max} is. [37]

$$\alpha_{max} = 1 + \frac{\lambda_0 n_0 R \tau_s}{2\lambda_s h n_{s0}} \tanh\left(\frac{\lambda_0}{4\lambda_s}\right) \quad \text{(Eq. 4.1)}$$

In the above equation, α_{max} becomes larger when λ_0 becomes longer. In other words, for longer terrace α_{max} can exceed α_{crit}, so nucleation is more likely to occur. This is shown in Fig. 4.26.

The second factor is the source flow rate. If the source flow rate at the inlet increases, the flux of reactants reaching the substrate increases, which also leads to an increase in α_{max}. Conversely, a decrease in the source flow rate leads to a decrease in α_{max}. This appears in the equation as follows.

$$\alpha_{max} = 1 + \frac{\lambda_0 n_0 R \tau_s}{2\lambda_s h n_{s0}} \tanh\left(\frac{\lambda_0}{4\lambda_s}\right) \quad \text{(Eq. 4.2)}$$

$$R = v_{step} \ \tan\theta = \frac{2h\lambda_s}{n_0\lambda_0}\left(J - \frac{n_{s0}}{\tau_s}\right) \tanh\left(\frac{\lambda_0}{2\lambda_s}\right) \quad \text{(Eq. 4.3)}$$

In other words, if the source flow rate increases beyond a certain threshold value, then the probability of 3C-SiC generation through nucleation increases. This is shown in Fig. 4.27.

The third factor to consider is the C/Si ratio. This factor is considered only in the SiC epitaxy, and the degree of nucleation varies according to the C/Si ratio of the reactants. When the C/Si ratio of the source is increased, it is

generally known that the supersaturation ratio of the adatom increases, because the mobility decreases at the SiC surface. It can be deduced that the energy barrier for an adatom transition of Si atoms in SiC crystal surface is 0.16 eV, while that of carbon is 2.34 eV [138] It has also been experimentally reported that nucleation occurs frequently at high C/Si ratios. Kimoto found that the nucleation density increased with increasing C/Si ratio in the SiC layer growth on the 6H-SiC substrate in 1995. [119] The C/Si ratio of the BTMSM source used in this experiment has a very high value of 3.5. In other literature, the C/Si ratio used for epitaxial growth on on-axis substrates is 1 or less. High C/Si ratio of BTMSM is a disadvantage in terms of lowering the nucleation density and strengthening step-flow growth. However, it is not always good to use low C/Si, because there is a disadvantage that it is not easy to control the background doping concentration. Especially in C-face, as mentioned above, the control of background doping concentration is not easy compared with Si-face, so using high C/Si ratio can help solve the problem. In other words, it is important to determine the appropriate C/Si ratio considering both the nucleation density and the background doping concentration.

The last factor to consider is growth face. Due to differences in the growth surface at which the SiC layer grows, differences in nucleation density may occur even under the same experimental conditions. It is experimentally reported that nucleation occurs more frequently in the C-face than in the Si-face for the SiC layer grown on the 6H-SiC substrate. [119] This is because the α_{crit} value changes due to the difference in the surface energy of the growth

surface. It is reported that C-face with low surface energy has a low α_{crit} value [119], so nucleation is easy even with the same α_{max} under the same experimental conditions, and 3C-SiC is easily produced. Low surface energy of C-face facilitates on-axis epitaxy by making surface morphology control easy at high temperature as mentioned above, but on the contrary, it causes disadvantage in terms of nucleation density. Fig. 4.28 shows the difference in α_{crit} due to face difference.

Taking all of the above factors into consideration, it is possible to explain how the polytype stability in Si-face reported in Chapter 4.1 has enhanced. Si-face has a higher α_{crit} than C-face, so nucleation is not easy, but surface energy is high and step bunching occurs at high temperature. In the bunched-step due to this step-bunching phenomenon, the micro-steps disappear and thus the long terrace is formed. This leads to an increase of α_{max}, which results in 3C-SiC nucleation in the terrace. This is a factor that lowers the stability of polytypes in on-axis Si-face 4H-SiC homoepitaxy. On the other hand, if the etching temperature is lowered and the etching time is increased to spread the micro-steps without step bunching, the terrace length is shortened without the bunched step, and the polytype stability can be improved. This is shown in Fig. 4.29.

On the other hand, C-face has lower surface energy than Si-face, and step-bunching phenomenon is not so severe, so it has uniform terrace length. On the other hand, since α_{crit} value is low, nucleation can easily occur even in small α_{max}. In particular, the BTMSM source used in this experiment can be expected to cause a high nucleation density due to a high C/Si ratio of 3.5. As

shown in Fig. 4.30, 3C-SiC nucleation occurred frequently even though micro-steps were spread without step-bunching because α_{max} value is higher than α_{crit}. Therefore, to change the situation shown in the dotted line in Fig. 6, finding the method of suppressing nucleation during growth is a solution to enhance polytype stability in C-face on-axis epitaxy. The four factors considered above are: 1. the terrace length cannot be reduced more because of the nature of the C-face, which has no severe step-bunching phenomenon already. 2. The source flow rate can be reduced. 3. C/Si ratio is fixed at 3.5 for BTMSM and cannot be changed. Especially, C-face requires high C/Si to control background doping concentration. 4. α_{crit} due to the difference in growth face cannot be changed because it is inherent characteristic. So, experiments were conducted to achieve suppression of nucleation by reducing the source flow rate.

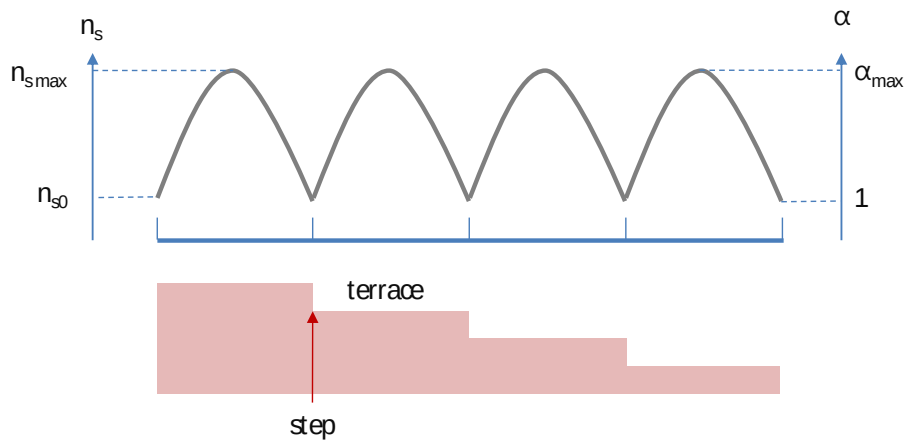

Figure 4.25 Schematic diagram of supersaturation of adatom at step structure.

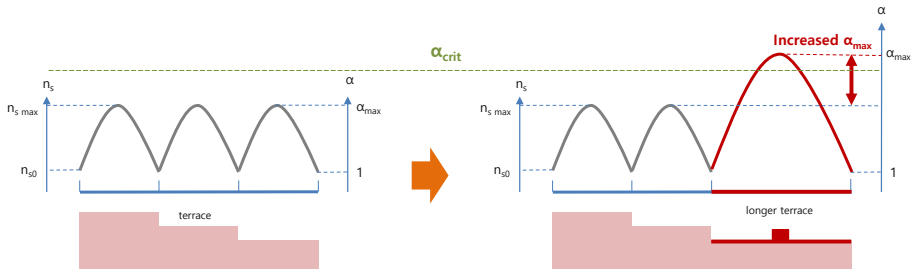

Figure 4.26 Schematic diagram of the effect of terrace length on nucleation density.

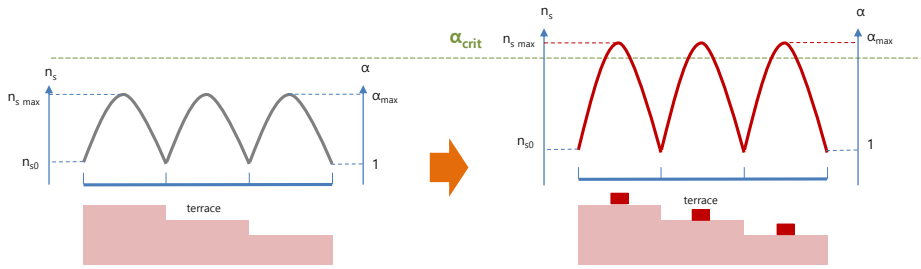

Figure 4.27 Schematic diagram of the effect of source flow rates on nucleation density.

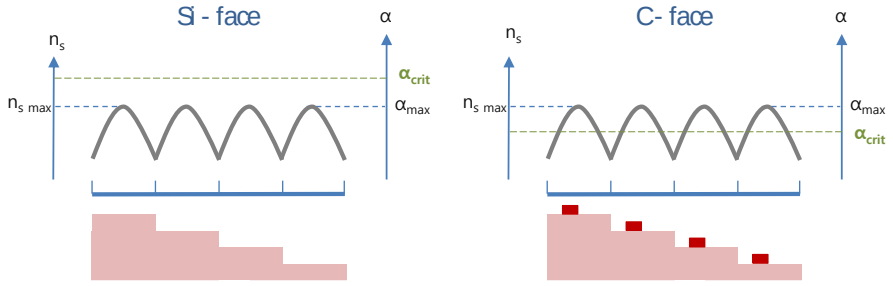

Figure 4.28 Schematic diagram of the effect of face difference on nucleation density.

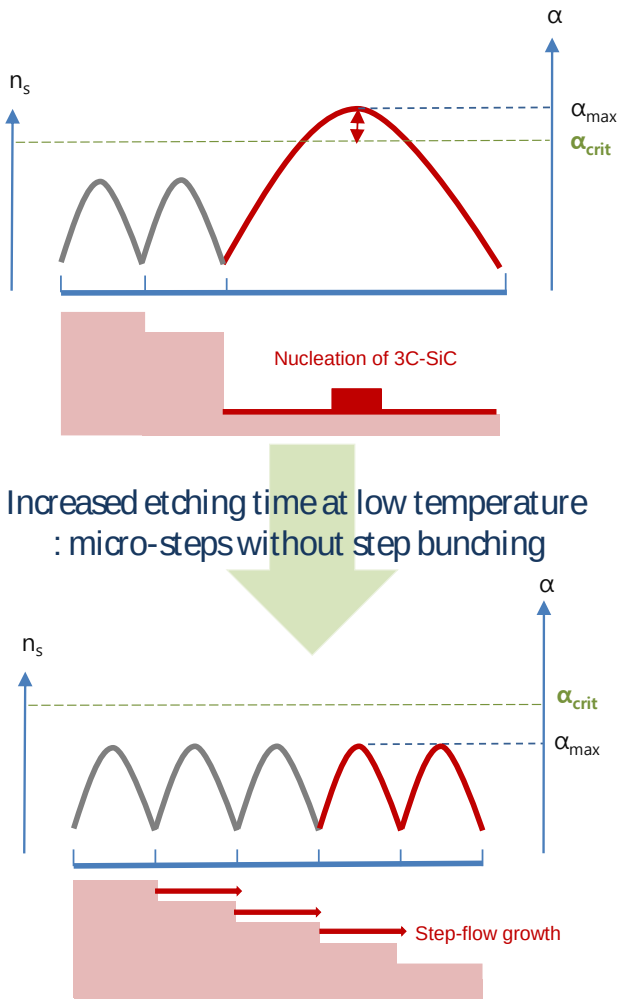

Figure 4.29 Schematic diagram of how the polytype stability in Si-face has enhanced.

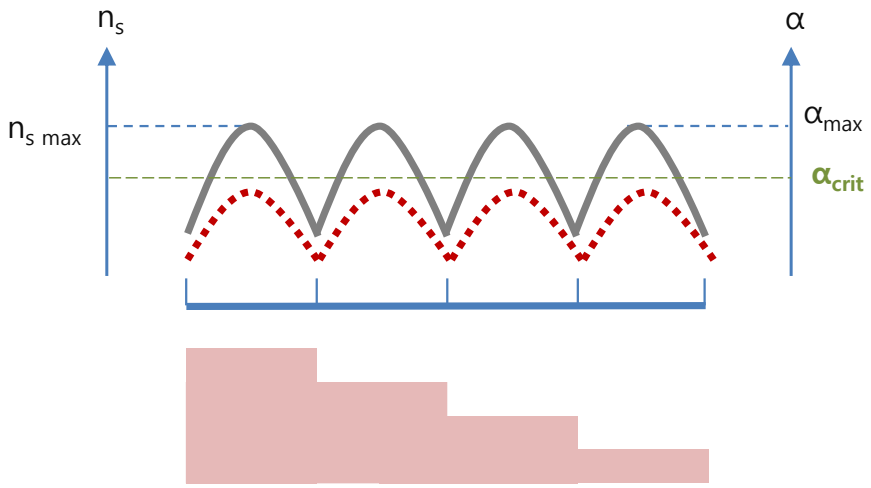

Figure 4.30 Schematic diagram of α_{max} and α_{crit} of C-face on-axis epitaxy.

4.2.5. Enhancing polytype stability of C-face on-axis epitaxy

Fig. 4.31 shows the optical mircographs and EBSD measurements of the specimens grown by hydrogen etched at 1400° C for 120 min and then changing the BTMSM source flow rate from 2.5 sccm to 10 sccm at 1550 ° C. When the flow rate of the source is 7.5 sccm or more, 4H ratio in deposited layer is very low. This is because the α_{max} value at the source flow rate is larger than the low α_{crit} value of the C-face, resulting in frequent nucleation. On the other hand, it can be seen that the stability of 4H is much higher at source flow rate of 5 sccm or less. The reason why the ratio of 4H in the layer is increased is because α_{max} has fallen below α_{crit} because the source flow rate has decreased. However, it still did not achieve high stability compared to Si-face. The reason for this is as follows. If the terrace length is changed, the α_{max} value is affected sensitively, and if the terrace length is shortened, the α_{max} value is greatly decreased and can be decreased below α_{crit} value. Therefore, the Si-face with a high α_{crit} value may have suppressed the nucleation very effectively if the terrace length is shortened by using revised hydrogen etching process. On the other hand, the change in the source flow rate does not affect the α_{max} value not so sensitively, so that the α_{max} value may not be reduced to a large value. Thus, even if the source flow rate is reduced, there is often a case where the α_{max} exceeds α_{crit} on a C-face with a low α_{crit} if there is a bit long terrace. This can be deduced from the fact that even if the source flow rate is reduced, Si-face has no effect on improving the polytype stability. If higher polytype stability is to be achieved on homoepitaxy of 4H-SiC on an on-axis

C-face substrate, adjustment of C/Si may be necessary and additional experiments and discussions are needed.

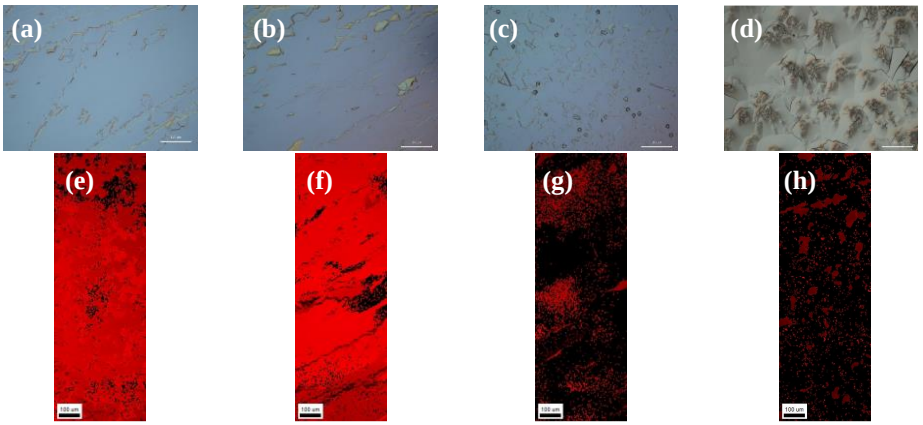

Figure 4.31 Optical image of surface of samples grown for 1h at 1550 ℃ with source flow rate of (a) 2.5sccm, (b) 5sccm, (c) 7.5sccm, (d) 10sccm. EBSD maps of samples grown with source flow rate of (d) 2.5sccm, (e) 5sccm, (f) 7.5sccm, (g) 10sccm.

Chapter 5. Conclusion

In-situ H_2 etching and homoepitaxial growth of 4H-SiC were performed on on-axis Si-face substrates using low-pressure chemical vapor deposition. We investigated the effect of various etching temperatures and durations on the surface of the on-axis substrates and adopted the optimized etching characteristics to enhance the polytype stability of the epitaxial layer.

For the on-axis substrates, micro-steps were generated on the surface of the substrates after H_2 etching because of selective etching of TSDs. These micro-steps at the etched surface contribute to the growth of the 4H polytype because they provide sites for step-flow growth at the side walls. However, for a high etching temperature (above 1500 ℃), step-bunching occurred and micro-steps disappeared around a bunched step. Since other polytypes such as 3C easily nucleate at bunched steps with a larger terrace, the formation of regular micro-steps without step-bunching on an etched surface is vital for enhancing the polytype stability. To spread out the micro-steps without step-bunching during the etching process, an increase in the etching duration at a temperature lower than the conventional etching temperature was required. Improved polytype stability of 4H-SiC up to 99% was finally achieved for Si-face on-axis substrates. This result is meaningful in that it solves the deposition problem that the value of C/Si ratio should be lower than 1.0 in the previously reported literature for the high polytype stability of on-axis epitaxial growth. BTMSM source used in this experiment has a C/Si ratio

value of 3.5, and 4H-SiC homoepitaxial layer can be grown on the on-axis substrate using a source having such a high C/Si ratio. This is because step-flow growth can be enhanced despite the short diffusion length by spreading the micro-step on the substrate without step-bunching during etching process.

The C-face on-axis substrate has similar etching characteristics to Si-face. Micro-steps were created on the substrate from the etching of the TSDs after the etching process. The step-bunching phenomenon at high temperature occurred less than the Si-face, which is due to the low surface energy of the C-face. However, despite the good surface morphology after the etching process, the stability of 4H-SiC on the grown epilayer was much lower at the C-face on-axis substrate. In order to analyze the reason, the BCF theory and reported experimental results for SiC epitaxial growth were considered together. As a result, the growth of the epilayer can be explained by the competition of the step-flow growth and the nucleation, and the factors influencing it are 1. terrace length, 2. the source flow rate, 3. C/Si ratio of source, and 4. difference in growth face. By lowering the source flow rate, it was possible to enhance the polytype stability in C-face on-axis epitaxial growth. In order to achieve higher polytype stability in C-face on-axis epitaxial growth, it is important to set the appropriate C/Si ratio and flow rate of the source considering the growth rate of the layer, control of the background doping concentration, and surface diffusion length of adatoms.

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2. Proceeding

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레이기술학회 2012년 춘계학술대회 및 제2회 반디 제주포럼, 18 may 2012, Jeju, Korea

국문 초록

탄화규소는 고온의 융점, 높은 파괴 전계, 큰 열전도성 및 큰 포화전자 이동도를 갖는 와이드-밴드갭 반도체로써 기존의 실리콘을 대체할 차세대 반도체 재료로 많은 연구가 진행되고 있다. 특히 탄화 규소를 이용한 전력 소자는 그 우수한 특성으로 항공 우주 시스템, 전기 자동차 또는 차세대 발전소와 같은 산업 운송 시스템에 적용된다면 큰 발전을 야기할 것으로 기대된다. 하지만 이러한 탄화규소를 적용함으로써 얻을 수 있는 긍정적인 효과는 탄화규소 소자를 성공적으로 제작할 수 있을 때에 비로서 실현될 수 있다. 그것을 위해서는 소자 제작을 위한 필수적인 단계인 에피택셜 성장(epitaxial growth) 공정이 매우 중요하다. 탄화 규소 소자의 성능은 에피택셜층(epitaxial layer)의 품질에 크게 의존하므로, 에피택셜 층의 생산성, 재현성 및 품질이 소자 성능의 개선에 큰 영향을 미친다. 고품질의 탄화규소 에피택셜 층의 성장을 위해서 분자 빔 에피택시(MBE), 액상 에피택시(LPE) 및 기상 에피택시(VPE)와 같은 많은 방법이 시도

되었지만 여전히 몇 가지 문제가 남아있다. 이 문제를 해결하기 위해 본 저자는 bis-trimethylsilylmethane (BTMSM, $C_7H_{20}Si_2$)을 이용한 유기-금속 화학증착기 (MOCVD)에 의한 4H-SiC 에피 층의 동종 에피택셜 성장에 관한 연구를 진행하였다.

현재로서는 탄화규소 동종에피탁시(homoepitaxy)의 폴리타입(polytype) 안정성을 향상시키기 위해 [11$\bar{2}$0] 방향으로 오프-컷(off-cut)된 오프-엑시스(off-axis) 기판이 일반적으로 사용된다. 그러나 이러한 경우 폴리타입 안정성이 향상 되더라도 다른 많은 문제가 존재한다. 먼저, 기저면 전위(BPD)가 기판으로부터 에피택셜 층으로 전달될 수 있다. BPD는 "킬러 결함(killer defects)"으로 알려져 있으며, 이는 에피택셜 층 내에 존재할 때 바이폴라 소자의 순방향 전압을 크게 저하시킨다. 둘째로, 탄화규소 잉곳에서 오프-컷 방향을 따라 기판이 절단 될 때 얻어지는 웨이퍼의 수가 감소한다. 위와 같은 오프-엑시스 기판을 사용함으로써 생기는 문제를 해결하려면 온-엑시스(on-axis) 기판에의 에피택셜 성장을 연구하는 것이 필수적이다. 그러나, 온-엑시스 기판의 낮은 스텝(step) 밀도 때문에, 에피택셜 성장 중, 에피택

셜 층 내에 의도하지 않은 폴리타입이 생성 될 가능성이 매우 높다. 본 연구에서는 규소 성장면(Si-face)과 탄소 성장면(C-face) 온-엑시스 기판의 수소 에칭 특성을 조사하고, 이 특성이 성장한 에피택셜 층의 폴리타입 안정성에 미치는 영향에 대해 3.5의 C/Si 비를 갖고 있는 BTMSM 전구체를 사용하여 보고하였다. 본 연구에서는 에칭 특성과 에피택셜 층의 상관 관계를 이해함으로써 에칭된 기판의 마이크로 스텝을 제어하고 규소 성장면에 대해 4H-SiC의 폴리 타입 안정성을 99%까지 향상시켰다. 또한, 탄화규소 온-엑시스 에피택셜 성장의 폴리타입 안정성에 영향을 미치는 요인을 고찰하여 탄소 성장면에서 폴리타입 안정성을 증가시키는 방법에 대하여 논의하였다.

온-엑시스 기판의 경우, 쓰레딩 스크루 전위 (TSD)의 선택적 에칭으로 인해 수소 에칭 후 마이크로-스텝(micro-step)이 기판 표면에 생성되었다. 에칭 된 표면에서의 이러한 마이크로-스텝은 4H 폴리타입의 성장에 기여하는데, 그 이유는 스텝의 측면에서 스텝-플로우 (step-flow) 성장을 위한 적층 순서를 노출시켜 제공하기 때문이다. 그러나, 높은 에칭 온도 (1500 ℃ 이상)에서는 스텝-번칭(step-

bunching)이 발생하고 번칭된 스텝 주위에서 마이크로-스텝이 사라진 것을 관찰하였다. 3C와 같은 다른 폴리타입이 이렇게 번칭된 스텝의 긴 테라스에서 쉽게 핵 생성될 수 있기 때문에, 에칭 된 표면에 스텝-번칭 현상 없이 규칙적인 마이크로-스텝을 형성하는 것이 폴리타입 안정성을 향상시키는 데 중요하다. 에칭 공정에서 스텝-번칭 현상 없이 마이크로-스텝을 시편에 퍼뜨리기 위해서는 종래의 에칭 온도보다 낮은 온도에서 에칭 지속 시간의 증가가 필요하다. 이러한 개선된 에칭 공정을 통해 99% 수준의 4H-SiC로 성장된 에피택셜 층을 규소 성장면 온-엑시스 기판에서 성공적으로 성장시켰다.

탄소 성장면의 경우, 규소 성장면과 유사한 에칭 특성을 가지고 있다. TSD의 선택적 에칭에 의해 마이크로-스텝이 만들어졌고 탄소 성장면의 낮은 표면 에너지로 인해 규소 성장면보다 높은 온도에서 스텝-번칭 현상이 거의 발생하지 않았다. 그러나, 스텝-번칭 현상 없이 마이크로-스텝을 퍼뜨린 후에 탄소 성장면에서 성장한 탄화규소층의 폴리타입 안정성은 개선되지 않았고, 규소 선장면의 경우보다 훨씬 낮았다. 이것은 낮은 임계 과포화 비율(critical supersaturation

ratio)로 인해 탄소 성장면의 핵 생성 밀도가 높기 때문이다. 따라서 본 저자는 스텝-플로우 성장과 핵 생성의 경쟁의 관점에서 탄화규소 층의 폴리타입 안정성에 영향을 미치는 요인에 대하여 이론적으로 고찰하는 동시에 탄화규소 에피택시에 대해 기존에 보고된 실험 데이터를 검토했다. 전구체의 유량을 감소시킴으로써, 탄소 성장면 온-엑시스 기판상의 에피택셜 층의 폴리타입 안정성이 향상되었다.

Keywords : 4H-탄화규소, 동종 에피택셜 성장, BTMSM, 온-엑시스 에피택시, 폴리타입 안정성

Student Number : 2011-23315

김현우

Acknowledgement

저의 박사 학위논문에 도움을 주신 분들께 지면을 빌려 글로써 감사의 말씀을 전합니다.

우선 6년이 넘는 시간 동안 저를 지도해주신 김형준 교수님께 가장 먼저 감사하다는 말씀 드립니다. 박사과정 기간 동안 가르쳐 주신 학문적 지식뿐만 아니라 교수님께서 보여주신 훌륭하신 인품, 그리고 저에게 해주신 조언들을 항상 마음속에 기억하고 살아가겠습니다. 그리고 저의 논문 심사위원장을 맡아주신 황철성 교수님께 감사드립니다. 교수님께서 보여주신 학문적인 통찰력과 날카로움에 항상 감탄했고, 조금이나마 배울 수 있어서 영광이었습니다. 또한 바쁘신 시간에도 저의 논문심사를 허락해주시고 많은 조언을 해주신 홍성현 교수님, 허재영 교수님, 이훈희 박사님께도 깊은 감사의 말씀을 전합니다.

이번에 같이 졸업하는 박막재료연구실 구성원 에게도 감사한 점이 많습니다. 항상 도움을 주기보다는 많이 받았었던 것 같은데, 앞으로 갚을 기회가 있기를 바랍니다. 우선 같은 SiC 팀이였던 수형이와 홍전이형. 박막재료연구실의 마지막 방장 수형이는 처음 들어온 후배가 자기보다 나이가 많아서 참 애매했을 텐데 6년동안 정말 많은 도움을 받은 것 같아 고맙다. 양복을 받지 않는 걸로 고마움을 대신한다. 홍전이형, 형하고 학회 갔을 때가 참 기억에 많이 남아요. 과제 같이 할 때, 그리고 평소에도 도움을 많이 받은 것 같아서 감

사해요. 영석이는 똘똘하고 운도 좋으니 어딜 가서도 잘 할 수 있을 것 같아. 여러 방면으로 잡다한 지식이 많아서 유용했고, 앞으로도 종종 물어볼게. 성민아, 똑똑하고 부지런한 네가 우리 연구실의 마지막 총무라서 다행이다. 총무일 하느라 수고했고 고마워. 인아야, 같이 필라테스 같이 다녀줘서 고맙고, 마지막에 같은 방을 써서 재미있었다. 지민아, 내가 장난을 많이 쳤었는데, 혹시 기분이 좋지 않았을 까봐 걱정된다. 다 친밀감의 표현이었으니까 이해해주고, 준비하고 있는 것 잘 되기를 바란다.

먼저 졸업하셨던 박막재료연구실 선배님들께도 감사의 말씀을 전합니다. 우선 제 사수였던 훈희형, 형께서 졸업하실 때 정말 보내드리기 싫고 나는 이제 어떻게 해야하지라고 생각했던 기억이 나는데 어느새 저도 졸업을 했네요. 형은 도움을 많이 안 주셨다고 하지만 저에게는 정말 최고의 사수이셨고 많은 도움을 받았어요. 같이 생활할 때에도, 그리고 졸업 후에도 항상 무언가를 물어보면 귀찮은 내색 없이 설명해주시고 같이 고민해 주셔서 감사합니다. 같은 SiC 팀이였던 창현이형과 도현이형. 마찬가지로 학교에서나 졸업 후에도 많은 도움을 받았고, 또 동생처럼 챙겨주셔서 감사합니다. 또한 같이 생활하며 정말 많은 도움을 주셨던 상현이형, 종호형, 봉섭이형, 영배형, 명숙누나, 유진누나, 성인이형, 승하형, 지운이형, 준래형에게도 감사드립니다. 회사에서 오셔서 같이 생활했던 윤장이형, 종식이형, 웅수형, 혁진이형, 은길이형, 민호형, 상진이형에게도 감사하다

는 말씀 드립니다. SiC연구를 계속 하시며 학술적으로 많은 조언을 해주신 전기연구원의 방욱 박사님과 문정현 박사님, 그리고 RIST의 서한석 박사님께도 감사드립니다. 논문 작업을 지도해 주시며 부족한 저를 이끌어주신 허재영 교수님께도 다시 한번 감사드립니다.

마지막으로 학교 밖에서 아낌없는 지원을 해 주신 가족 분들께 감사의 말씀을 전합니다. 가장 먼저 부족한 손자를 항상 최고라고 생각해주시고 많이 걱정해 주셨던 할아버지 할머니, 감사드립니다. 그리고 뒤에서 응원해 주셨던 중앙무선 식구들과 친척분들께 감사드립니다. 항상 미안한 점이 많은 내 동생 수영아 고마워. 끝으로 말없이 저를 믿어주시고 살아오는 동안 넘치는 사랑을 느낄 수 있게 해 주신 부모님께 이 논문을 바칩니다.

그 외에도 여기에 말씀드리지 못한 많은 분들께도 감사한 점이 많습니다. 저 혼자만의 능력으로는 여기까지 올 수 없었다는 것을 잘 알고 있습니다. 제가 받은 모든 것을 잊지 않고, 항상 겸손하고 감사한 마음을 가지고 살아가겠습니다.

2018년 1월

김현우 올림