**Ph.D. DISSERTATION**

# InGaZnO based charge trap device for NAND flash memory application

**by**

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**DEPARTMENT OF MATERIALS SCIENCE AND ENGINEERING**

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# Abstract

Current information technology industry requires faster, smaller, less power consuming and cost effective memory devices, which is the fundament of the computer system. Out of many memory devices, NAND flash memory technology one of the promising candidate for next generation storage system. Planar technology is at its roadblocks due to the fundamental limitation of the density per available wafer area. Hence, vertical NAND flash (VNAND) is the solution, which can overcome the density limitation. Current industry use three major types of V-NAND (i.e. BiCs, TCAT and Pipe-BiCs). These major architectures of V-NAND all require “Etch hole”, where ONO, channel and oxide is deposited. Due to limitation on wafer area, etch hole and spacer between etch holes have limitations, often called as the “critical diameter or dimension”. In case of etch hole itself, each packing density has different critical diameter of hole (CD). Currently, a-Si or poly-Si channels are used as the channel material. However, as etch hole depth elongates, to increase cell density, Si based channel suffer from low on current, which can be very problematic in achieving constant device uniformity. To increase on current, Si based channel requires thickening, but again, limited by the CD. Hence, new channel material that can guarantee tunable electrical characteristic is ideal. Out of many candidates, amorphous oxide is one of the promising candidate.

InGaZnO (α-IGZO or IGZO) has been well studied to be applied on V-NAND technology.

Professor Hosono first proposed IGZO in the year 2004. Since then, IGZO has been intensely studied for its application on display devices. With most common deposition technique, sputtering. Large area, fast deposition rate, and relatively uniform film quality had lead such popularity. In primitive stage of the IGZO research, most problematic characteristic was material's instability against light illumination under negative bias (NBIS). When light wavelength of 550nm (or shorter) is induced on IGZO (held at negative gate bias), negative shift of the transfer curve was observed. Numerous arguments have been proposed as a possible cause, but most agreed that it was the ionization of the oxygen vacancy. When light is induced, the oxygen vacancy (naturally occurring from amorphous large band gap nature of the material) begins to ionize, changing its valance state from neutron to two (creating two extra electron). Previous research from our group has shown that NBIS is geometry dependent (NBIS worsen as channel length increase), hence, smaller channel dimension may solve the issue. Other possible solutions were to doping and use passivation layer.

Despite its intensive study for display application, IGZO's application on V-NAND still requires major challenge, to change deposition technique. Despite fast and low temperature merits of the sputtering process, its low step

coverage hinders IGZO for the memory applications. In this sense, this research proposes relatively new deposition technique to deposit IGZO: metal-organic chemical vapor deposition (MOCVD).

First part of this research compares program and erase characteristics of MOCVD and sputter deposited a-IGZO. Both deposition methods have shown to have similar atomic percent (stoichiometry), density and thickness. Despite, slightly higher saturation mobility from sputter IGZO, the program and erase characteristics showed much faster operation in case for the MOCVD IGZO (PGM 3.12V @ $V_{PGM}$=20V,$t_{PGM}$=100ms for MOCVD and PGM 1.63V @ $V_{PGM}$=20V, $t_{PGM}$=100ms). In depth analysis of such behavior were studied.

Second part concerns the composition variation of the IGZO. MOCVD processed IGZO were studied with different Ga/Zn ratio, keeping the In content at constant (40 atomic percent). Previous research has indicated Ga as the carrier sink, allowing the stable off current of the TFT, due to strong bonding between Ga and O. However, study on different Ga/Zn ratio has indicated while highest field effective channel mobility was observed at max Zn content (of the study), highest saturation mobility was observed when Ga/Zn ratio was at maximum (of the study). Analysis to understand the role of Ga/Zn within the IGZO thin film is further investigated

**Keywords:** amorphous oxide semiconductor, IGZO, TFT, planar NAND, MOCVD

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# List of Abbreviations

| | |
|---|---|
| DRAM | Dynamic random access memory |
| V-NAND | Vertical NAND (not and) memory |
| AOS | Amorhous oxide semiconductor |
| $V_{th}$ (VTH) | Threshold voltage |
| ALD | Atomic Layer Deposition |
| CVD | Chemical vapor deposition |
| MOCVD | Metal Organic Chemical vapor deposition |
| XRF | X-ray fluorescence |
| TFT | Thin Film Transistor |
| XPS | X-ray photoelectron spectroscopy |
| AES | Auger electron spectroscopy |
| XRD | X-ray diffraction |
| XRR | X-ray reflectivity |
| TOF-SIMS | Time of Flight Secondary Ion Mass Spectroscopy |
| UPS | Ultraviolet Photoelectron spectroscopy |
| CTF | Charge Trap Flash |
| DADI | [3-(Dimethylamino)propyl](dimethyl)indium |
| DEZ | Diethyl Zinc |
| TMGA | Trimethyl Gallium |
| PDA | Post Deposition Annealing |
| $E_G$ | Band-gap energy |
| GAXRD | Glancing Angle X-ray Diffraction |
| IGZO | Indium Gallium Zinc Oxide |
| LPCVD | Low pressure chemical vapor deposition |

| | |
|---|---|
| ITO | Sn-doped Indium Oxide |
| NBIS | Negative Bias illumination Stability |
| NBS | Negative Bias Stability |
| PBIS | Positive Bias illumination Stability |
| PBS | Positive Bias Stability |
| SE | Spectroscopic Ellipsometry |
| SS | Sub-threshold Swing |
| TFT | Thin Film Transistor |
| VB | Valence Band |
| CB | Conduction Band |
| $V_{OX}$ (VOX) | Oxygen Vacancy |
| μ | Mobility |
| ONO | T.O.-C.T.L.-B.O. ($SiO_2$-$Si_3N_4$-$SiO_2$) |
| T.O. | Tunneling Oxide |
| C.T.L. (CTL) | Charge Trap Layer |
| B.O. | Blocking Oxide. |
| CD | Critical Diameter (in VNAND) |

# 1. Introduction

## 1.1. Amorphous Oxide Semiconductor

Amorphous oxide semiconductors (AOSs) have been widely researched for thin-film transistors (TFTs) in high performance display devices due to its transparency and superior carrier transport properties. Since the AOSs are composed of post-transition-metal cations which have a large wave function overlap with neighboring atoms in the s-orbitals, the electrical properties are not significantly altered from the atomically regular crystalline material even when in the amorphous structure. As a result, a high carrier density and mobility care obtained [1].

Since the report of Hosono in 2004 on transparent and flexible TFTs using amorphous indium gallium zinc oxide (a-IGZO), a-IGZO have received considerable attention in display applications, such as active-matrix liquid crystal displays, active matrix organic light-emitting diodes, and flexible displays. Such was due to their superior electrical performance compared with conventional AOSs TFTs. Recently, it was reported that AOSs can be potentially utilized in low-voltage logic devices, as well as memory applications [2-4].

The amorphous nature and high carrier mobility of a-IGZO, which can be achieved by simple sputtering processes at room temperature, attract a great deal of attention for this approach [5, 6]. In addition, the high performance of AOS TFTs also allows them to be easily integrated with Si-based devices even at low processing temperature [6-8]. However, despite these promising factors, research on applications for AOS has mostly been focused on the development of thin film transistors for display or planar-type devices. Furthermore, while there have been many efforts to improve the electrical performance of AOS, only a few results have been reported about the device scaling or novel device applications. Although the issues related with scaling have not been highlighted for display devices, a proper understanding of the overall conduction mechanism is very important for new applications such as logic and memory devices. Therefore, it is very important to establish a concrete understanding of the device performance variation in terms of device scaling and contact characteristics. Furthermore, to be implemented in novel devices applications, various device structures should be suggested and their electrical characteristics should be investigated..

## 1.2. Empirical Background

The very first planar a-IGZO charge trap flash is shown in figure 1-1. On top of the $P^{++}$ Si substrate (which acts as a gate electrode) 100nm PECVD $SiO_2$, 20nm LPCVD $Si_3N_4$ and 4nm PECVD $SiO_2$ was deposited from ISRC. On such ONO structure, a-IGZO was deposited via sputtering method at power 150W, pressure 5.1mTorr and Ar plasma gas. The very first device shows poor program characteristic, where it required around 1000 programming time to shift $V_{TH}$ by 4V. Considering the fact that current industry uses flash devices under 10 micro programming second at 20V with 4V $V_{th}$ shift, such device fabricated from DTFL was not suitable, which requires future improvement.

There are two major aspect to consider in programming charge trap flash device. One is the amount of charge injected via channel (from electronds) and the other is the quality of the tunneling oxide. To verify that the amount of charge injected from the channel was sufficient in first flash device, the displacement relation was used to calculation the electrical field on tunneling oxide, figure 1-2.

As can be seen from the figure 1-2, the amount of field induced on tunneling oxide was around 1.75MV/cm. The next step was to compare such value with the theoretical value. The method to find the amount of

charge needed for the change in $V_{th}$ is shown in figure 1-3, from such relation, the current necessary to shift $V_{TH}$ by 1V at program time of 1second was found to be around $3.45 \times 10^{-8}$ A/m$^2$.

Considering the fact that the major programming current is the fowler Nordhiem tunneling (F.N. tunneling), F.N. tunneling equation was used to found the theoretical electronic field necessary to cause $V_{th}$ shift by 1V at 1 second programming time. (Figure 1-4). The result indicated that the first planar structure induced too small electric field on the tunneling oxide, which was not enough to cause $V_{th}$ shift, hence the resulting programming operation of the device was very poor.

Hence, new ONO structure was necessary. The new ONO was composed by thermal $SiO_2$ (20nm), LPCVD $Si_3N_4$ (5nm) and LPCVD $SiO_2$ (5nm) on same substrate. The much thinner ONO structure can induce around 7.25 MV/cm, where it is much closer to the theoretical value. The resulting device operation is shown in figure 1-5, Although the programming characteristics has improved, it still has a room for the enhancement, compared to the flash devices used in the industry.

Atomic layer deposition (ALD) is well known as the deposition method that can lead most defect free thin film. Hence, the ALD was considered to be used to deposit tunneling oxide. Although TMA $Al_2O_3$ may have higher dielectric constant than $SiO_2$, DTFL ALD system could

not deposit ALD $SiO_2$ during the research period; hence, alterative had to be used. Despite the higher dielectric constant, leading smaller electronic field induced on the tunneling oxide ($4.14x10^8$V/m), the $Al_2O_3$ has lower work function than $SiO_2$, which may compromise the smaller electronic field induced during the F.N. tunneling operation. The final charge trap characteristic, using $Al_2O_3$ tunneling oxide is shown in figure 1-6. Although the result may still be much slower than the industry, the programming operation was fast enough to measure $V_{th}$ shift from the pulse programming voltage. Hence, such ONO structure will be used from here on.

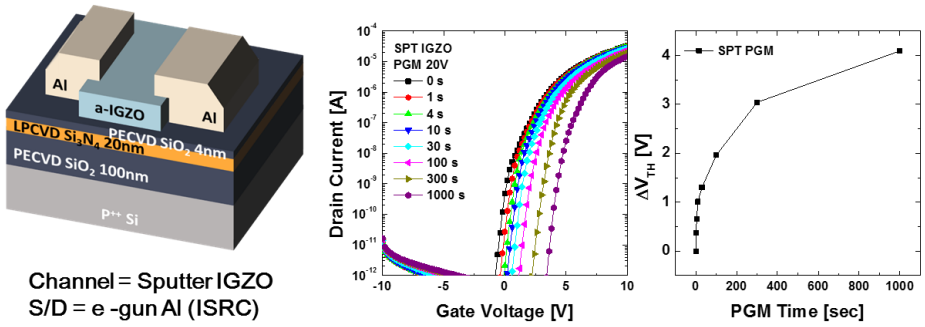



Figure 1-1 schematic diagram of 1st IGZO charge trap device from DTFL, and its programming characteristics

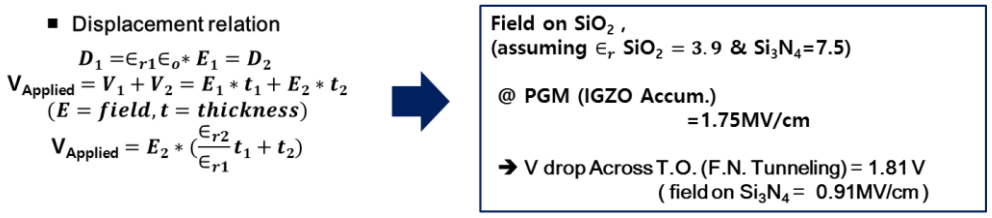



Figure1-2 Displacement relation of the very first IGZO flash device and amount of electrical field induced on tunneling oxide.

$\Delta V_{TH} = \frac{\Delta Q_{trapped}}{C_{Oxide(B.O.)}}$ , **$SiO_2$ THK=100nm, A= 1m²**

$\Delta V_{TH} = 1V = \frac{\Delta Q_{trapped}}{C_{Oxide}}, \Delta Q_{trapped} = 3.45\ x\ 10^{-8}$ **[C/m²]**

**→ ~ 3.45 x $10^{-8}$ C/m² needed to cause $V_{TH}$ to shift 1V**

**→ Since J=Q/(t*A),**

**→ @ $t_{PGM}$ =1sec, $J_{PGM}$ to cause 1V $V_{TH}$ shift ~ 3.45 x$10^{-8}$ [C/s m² ] [A/m²]**

Figure 1-3 amount of charge needed for change in Vth.

$$J_{F.N.} = \frac{A}{4\Phi_B} * E^2 * e^{\frac{-2B\Phi_B^{\frac{3}{2}}}{3E}}, A = \frac{q^2}{2\pi h}, B = \frac{4\pi\sqrt{2m^* q}}{h} \text{ (from Hori p.45)}$$

$$J_{F.N.} = \frac{\Delta Q_{trapped}}{t\,(1sec)} = 3.45x10^{-8}\left[\frac{C}{s * m^2}\right]$$

$$= \frac{(1.6 * 10^{-19})^2 [C^2]}{\frac{2\pi(6.626 * 10^{-34})\,[J * s]}{4(3.26/(1.6 * 10^{-19}))\,[V]}} * (E)^2 \left[\frac{V^2}{m^2}\right] * e^{\frac{-2^{\frac{4\pi\sqrt{2(9.109*10^{-31}\,[kg]1.6*10^{-19}\,[C]}}{6.626*10^{-34}\,[J*s]}(3.26eV/(1.6*10^{-19}))^{\frac{3}{2}}}}{3(E)\left[\frac{V}{m}\right]}}$$

$$3.45x10^{-8}\left[\frac{C}{s*m^2}\right] = 3.01x10^{12}(E)^2\left[\frac{V}{m}\right] * e^{\frac{-1.172x10^{10}}{(E)\left[\frac{V}{m}\right]}}, E = 7.42\,x\,10^8\left[\frac{V}{m}\right] = 7.42\,\left[\frac{MV}{cm}\right]$$

Figure 1-4 F.N. Tunneling equation and resulitng electronic field necessary to cause Vth shift of 1V at programming time of 1second.

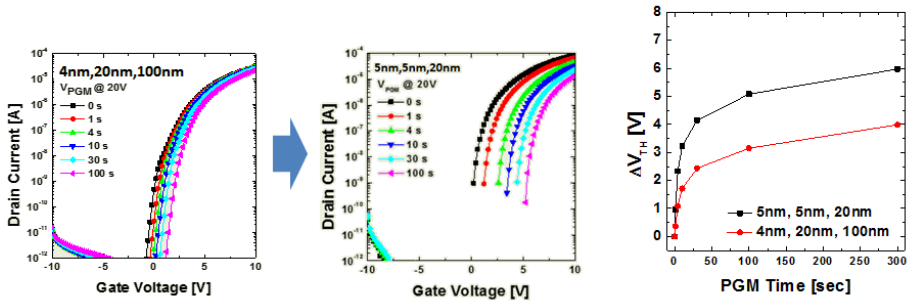



Figure 1-5 PGM operation comparison between 1st and 2nd ONO structured a-IGZO charge trap flash

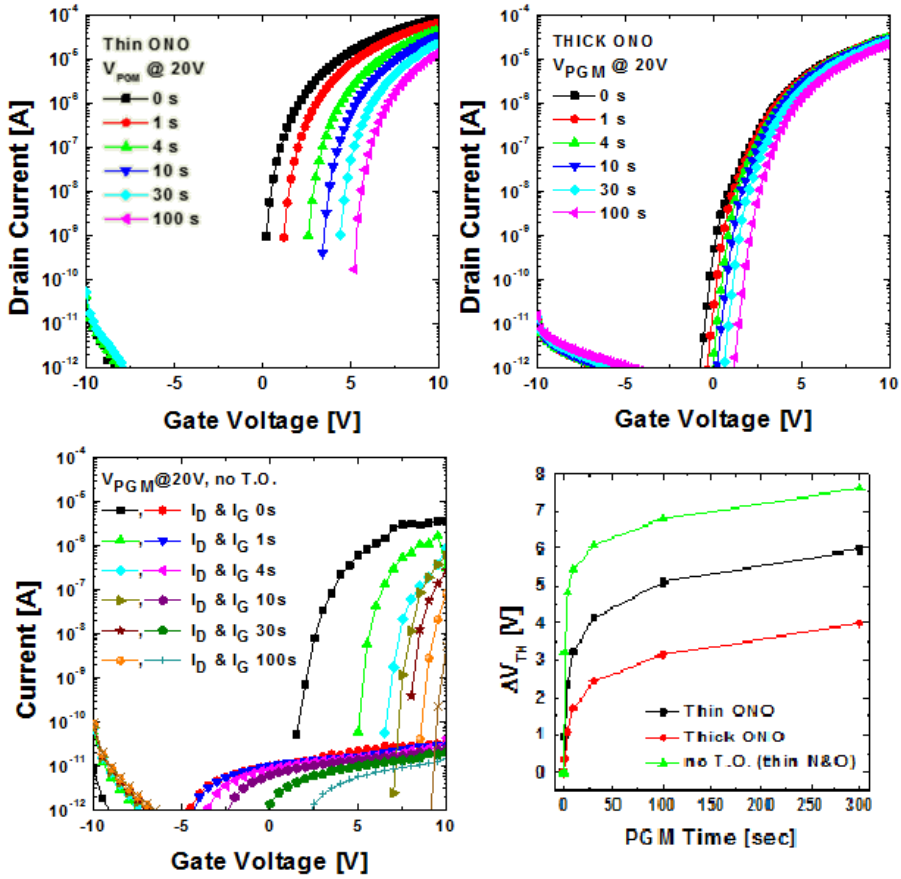



Figure 1-5.1 Effect of tunneling oxide on PGM characteristics.

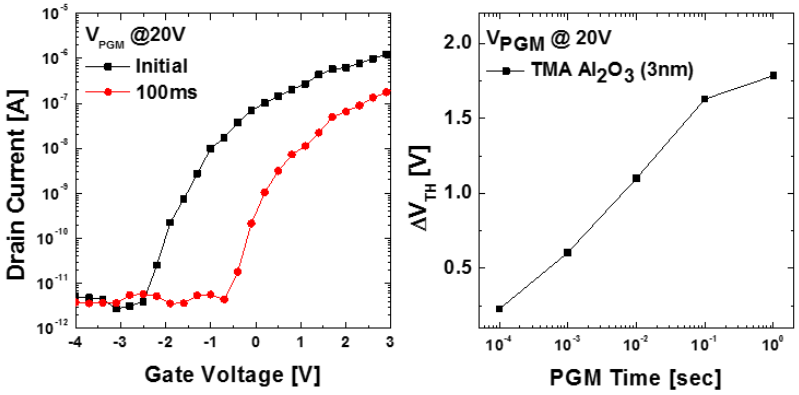
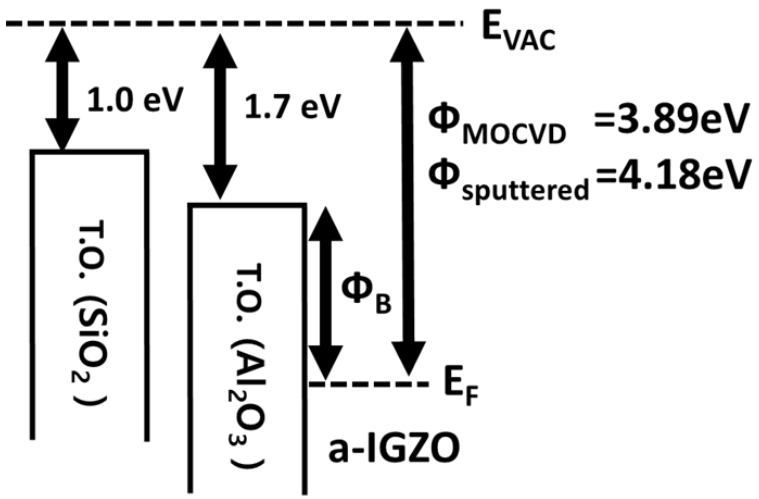
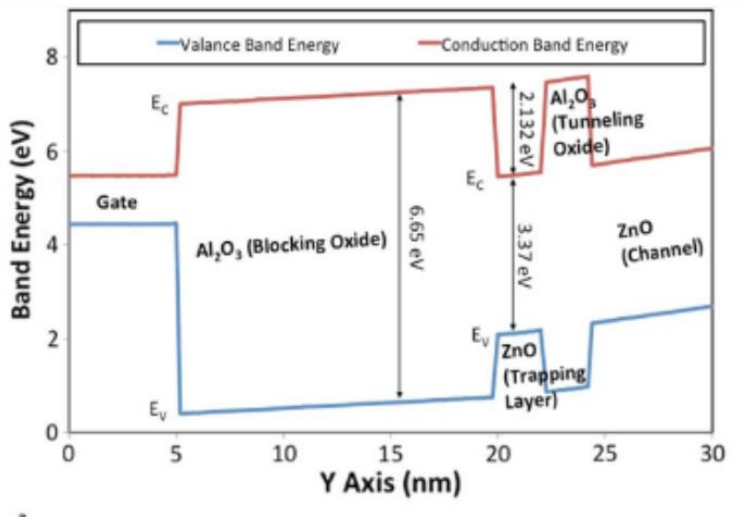



Figure 1-6 PGM operation of a-IGZO CTF with TMA Al2O3 tunneling Oxide




$SiO_2$ and $Al_2O_3$ information taken from
Robertson J., J.Vac.Sci.Technol.A31,2013

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## 1.3. Objective and Chapter Overview

The objective of this dissertation is to show possibility of amorphous oxide semiconductor (AOS), amorphous-InGaZnO (a-IGZO), as a channel material for the next generation charge trap memory, vertical, even Fin-Fet structured, NAND flash memory, by introducing fairly new technique, in a-IGZO, metal-organic chemical vapor deposition (MOCVD). ..

Chapter 2 present the background studies needed to understand and development of a-IGZO charge trap memory.

Chapter 3 covers comparison between sputtering, most widely used deposition method to deposit a-IGZO, and MOCVD a-IGZO. Detailed thin film characteristic analysis were performed to understand the different program and erase speed/ characteristic of MOCVD and sputtered a-IGZO charge trap memory..

Chapter 4 covers effect of Ga/Zn ratio within the MOCVD IGZO and its effect on devices, TFT and Charge Trap memory..

Finally, in chapter 5, the conclusion of the dissertation is made.

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# 2. Literature

## 2.1. Amorphous Oxide Semiconductor: IGZO

AOS, especially a-IGZO, are promising channel materials for TFTs used mainly in the display industry. Ever since Professor Hosono first presented in the year 2004, a-IGZO has been a hot prospect for channel materials owing to its high electron mobility (>10 cm2/Vs), good optical transparency, and tunable electrical conductivity. The comparison of a-IGZO with a-Si and poly-Si is listed in Table 2.1.3.

The a-IGZO holds n-type semiconductor property due to its native oxygen vacancies and zinc interstitials. It has been reported and widely accepted that the native donor is the oxygen vacancy, which is one of the predominant defects by calculation of reaction reacts and diffusion experiments [6,16-18].

Three possible charge state of oxygen vacancies exists in the ZnO based oxide semiconductors; Vo $0^{+}$, Vo $1^{+}$, and Vo $2^{+}$ for neutral, singly, or doubly ionized states, varying with the electronic chemical potential of the semiconductor [18, 19]. The oxygen vacancy state may also vary by the relative cations around the vacancies.

The a-IGZO is composed of post-transition-metal cations (In, Ga and Zn). Therefore, the a-IGZO has conduction path composed of extended spherical s orbitals of heavy metal cations [6, 15, 20], while a covalent amorphous semiconductor, for example, a-Si:H, consists of sp3 orbitals.

In a-IGZO, the direct overlap between neighboring metal s orbitals is rather large, and it is not significantly affected even at the amorphous structures, as shown in Figure 2.1.1. The conduction paths of a-Si can be significantly be altered by the bond angle distribution, and this structural randomness greatly degrades the magnitude of bond overlap, resulting in the decreased carrier mobility in a-Si [6, 20]. Hence a-IGZO is more suitable for the next generation display and memory devices.

Table 2.1.1 Comparison of a-Si, poly-Si, and a-IGZO channel layer [6]

| | **a-Si** | **poly-Si** | **a-IGZO** |
|---|---|---|---|
| Mobility ($cm^2/Vs$) | < 1 | 30 ~ 100 | 1 ~ 20 |
| TFT uniformity | Good | Poor | Good |
| TFT polarity | n-type | COMS | n-type |
| Cost/Yield | Low/High | High/Low | Low/High |
| $V_{th}$ shift | > 10 V | < 0.5 V | < 1 V |
| Process Temp. (°C) | 150 ~ 350 | 250 ~ 550 | RT ~ 400 |

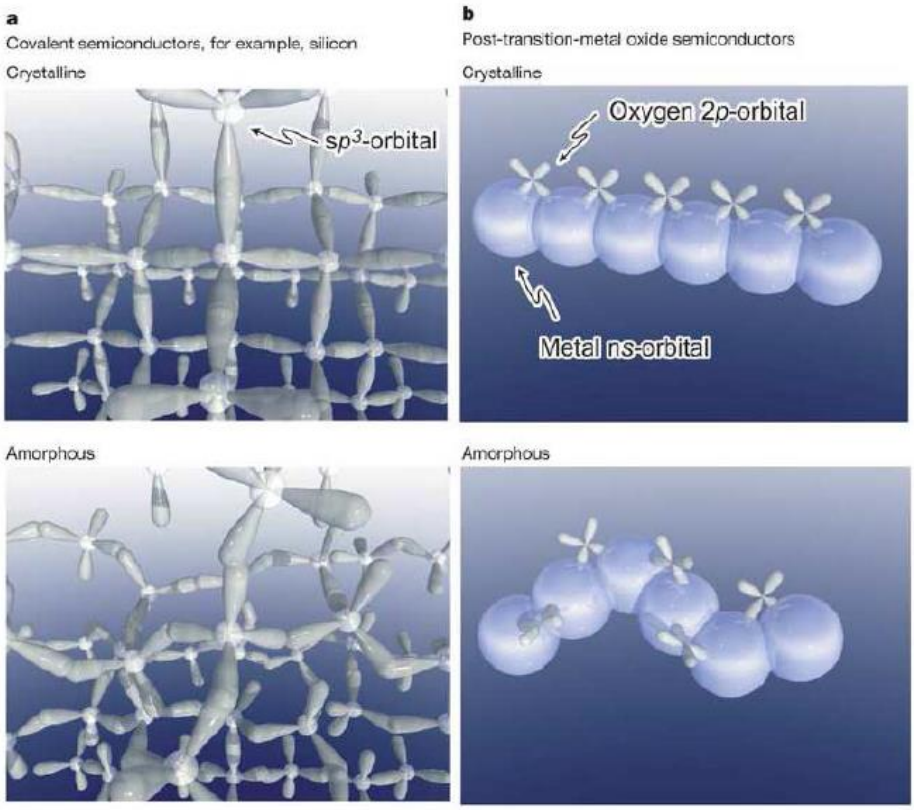


Figure 2.1.1 Schematic orbital drawing for the carrier transport paths in (a) amorphous Si (b) amorphous oxide semiconductors composed of post transition metal cations [20]

## 2.2. Oxide Semiconductor thin-film transistors

Thin film Transistors (TFTs) is similar to the SOI (Silicon on Insulator) devices, but has been mostly been compared with more conventional Metal Oxide Semiconductor Field Effective Transistors (MOSFETs). However, they are very different, since MOSFET is based on Si bulk substrate (which acts as a channel). The TFTs are composed of numerous deposited thin films with thickness in range of nanometers. However, for the electrical characterization of TFTs and to understand its operation, MOSFET theory is used. In MOSFET, the semiconductor (Si substrate) is connected to the source/ drain electrodes by forming p-n junction. However, there is no p-n junction between the semiconductor and source/drain electrodes in case of the TFTs.

Figure 2.2.1 shows the most conventional structures of TFTs [21, 22]. In staggered inverted structure, the source/drain (S/D) are on opposite side of the semiconductor in coplanar structure, the S/D are place on the same level with the semiconductor. The staggered structure has been used for the a-Si:H TFT. The staggered bottom gate structure has been used for the poly-Si TFTs and a-Si:H TFT in LCD devices. Due to the gate metal electrodes screening the channel layer from the back light of the LCD, staggered bottom gate structure is more suitable. Structures shown in figure 2.2.1 are selected by its advantages

depending on the device characteristics and process integration, processing and properties [23, 24] In this section, the bottom gate structure will be dealt, since it is widely used for the AOS industry, where back channel is exposed to an air, and can be easily modified by the subsequent processes (chemical absorption/desorption during annealing and post treatments).

Etch stopper, or passivation, layer is often used in the staggered bottom gate structure. Such etch stopping layer is usually an insulating film, and can improve the processing by allowing accurate etching of the channel layer, without damaging the semiconductor surface [25]. The etch stopper is also an effective protective layer which can protect channel from chemical absorption/desorption, and moistures in air. Such defects may alter the conductivity and other electrical properties of the device by acting as various electron source or sinks [26, 27]

TFTs are similar with the MOSFET in sense that they are both used in microprocessors or memory devices, but also very different. MOSFET is based on silicon wafer, which acts as the substrate and the semiconductor layer. In TFTs, insulating substrate is often used, e.g. glass, and channel deposition process is sequentially followed. Also, MOSFETs have p-n junction between the S/D and channel, but not in TFTs. Such relates the another importance difference in device characteristics. When TFTs and MOSFETs rely on the field effect to

modulate the conductivity of the channel layer, at on state, the on state of TFTs is achieved by the accumulation of the charge at the interface. In MOSFETs, the gate bias induces inversion region in the channel, where carrier transports. Thus is MOSFET, an n-type conductive layer is formed in case of the p-type silicon wafer substrate (and vice versa for the n-type wafer).

In TFTs, depending on the carrier concentration, un-like MOSFET, current may flow from the source to drain without any gate bias applied (normally on-state, depletion mode TFT). In such case, negative bias should be applied at the gate electrode to deplete the channel layer to achieve off state. THE TFT operation is depicted in Figure 2.2.3. For ideal TFT operation, the channel should be fully depleted for off-state and saturation accumulation for on state [28].

Like MOSFETs, the analysis of TFT device characterization typically follows the MOSFET equations. Drain current on/off ratio, channel mobility (saturation, $\mu_{sat}$, and field effective, $\mu_{FE}$), threshold voltage ($V_{TH}$), subthreshold swing (S.S.) are often used to evaluate the device. Channel mobility is related with the carrier transportation in the channel, may be hopping, band to band or scattering assisted band to band conduction. Scattering mechanisms, such as lattice vibration, ionized impurities, grain boundaries and other structural defects [29]. Due to the

The equations for thin film transistors are as follows:

@ $V_{DS} < V_{GS}-V_{TH,}$ saturation mobility is given by

$$I_{DS,linear} = \frac{W}{L}\mu_{FE}C_{ox}(V_{GS} - V_{th})V_{DS}$$

& Field effective mobility is given by,

$$g_m = \left.\frac{\partial I_{DS}}{\partial V_{GS}}\right|_{V_{DS}=const.} = \frac{W}{L}\mu_{FE}C_{ox}V_{DS}$$

$$\therefore \mu_{FE} = \frac{Lg_m}{WC_{ox}V_{DS}}$$

@ $V_{DS} > V_{GS} - V_{TH}$,

$$I_{DS,sat.} = \frac{W}{2L}\mu_{sat}C_{ox}(V_{GS} - V_{th})^2$$

$$\therefore \mu_{sat} = \frac{2Lm^2}{WC_{ox}}$$

$$(m \text{ is slope of } \sqrt{I_{DS,sat.}} - (V_{GS} - V_{th}))$$

Also, the subthreshold swing (S.S.) are usually extracted from the maximum slop from transfer curve ($V_G$-$I_{DS}$ curve).

$$SS \equiv \ln(10)\frac{\partial V_{GS}}{\partial \ln(I_{DS})}$$

$$= \frac{V_{GS,2} - V_{GS,1}}{\log(I_{DS,2} - I_{DS,1})}$$

In TFTs, threshold voltage has different physical meaning than conventional MOSFET. In conventional MOSFET, threshold voltage is defined as the gate voltage equal to the double of semiconductor surface potential. In TFT, threshold voltage is usually defined as the gate voltage which induces a drain current of 10 nA.

TFTs has been used as a pixel driver for the LCD and OLED displays and may also be used for the next generation flexible display. Especially for the amorphous oxide semiconductors (AOS), the higher mobility, excellent uniformity and good transparency to visible light

than conventional a-Si and poly-Si allows it to be the most promising candidate [30]. However, in AOS, the device stability against photon (light) and bias stress still remains a critical issues for them to be used in the industry [20, 30]. Out of various stability issues, stability against negative bias at light emitted condition holds most concern. Figure 2.2.4 shows the evolution of the transfer characteristics of ZnO TFTs under positive or negative gate bias stress with and without light [31]. Since the operation of conventional LCD and any other light emitting devices inevitably suffers from the stress induced by the photon energy, from back light unit and/ or the external visible light, the negative bias illumination stress needs to be addressed before its commercial use. In this regard, intensive efforts has been made to understand the origin of the negative bias illumination instability. Mainly three models has been reported, which can be considered as plausible origins. Photo-induced hole trapping [32-35], photon induced transition of oxygen vacancies from neutral to 2+ states [36] and photo-desorption of ambient gas molecules on the back surface of the channel [37]. First is based on the electron hole pair generation in oxide in oxide semiconductor under light illumination. Such electron hole pairs generated from photon may overcome the bandgap by the photo-excitation. Figure 2.2.5 depicts the band diagram to explain such phenomenon. The photo-induced hole trapping model assumes that photo-generated holes drift towards the

gate insulators by the negative gate voltage and trapped at the gate oxide/ channel interface or at the bulk of gate oxide [33]. Therefore, the hole trapping depends more strongly on the quality of the gate insulator. Also, oxygen vacancy may work as a defect center and source of hole carriers [38]. The transition of neutral oxygen vacancies to $2^{+}$ valence state makes such phenomena possible. The neutral state forms deep state and the two plus state donates two electrons into the conduction band as shown in figure 2.2.6. Hence, under illumination, ionization of oxygen vacancy can create two extra electrons, leading higher channel conductivity. Such will result negative $V_{TH}$ shift in the transfer curve [39-41]

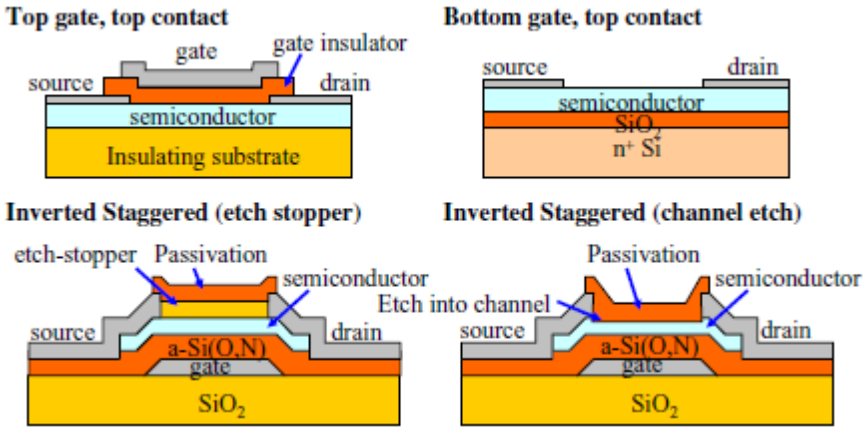


Figure 2.2.1 Schematic diagrams of most conventional TFT structures [22]

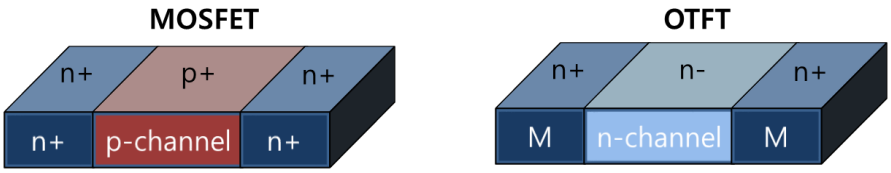


Figure 2.2.2. Schematic diagram comparison between MOSFET and OTFT.

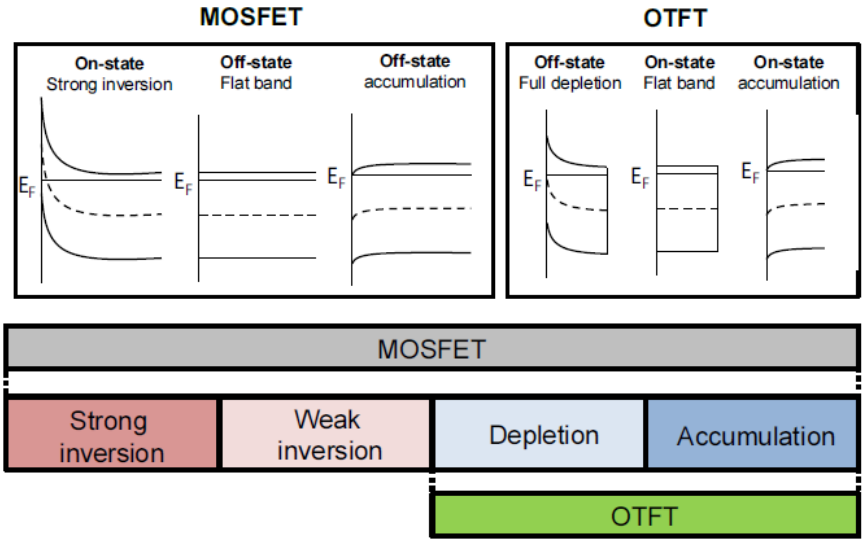


Figure 2.2.3 Comparison of TFT operation with MOSFET operation [28].

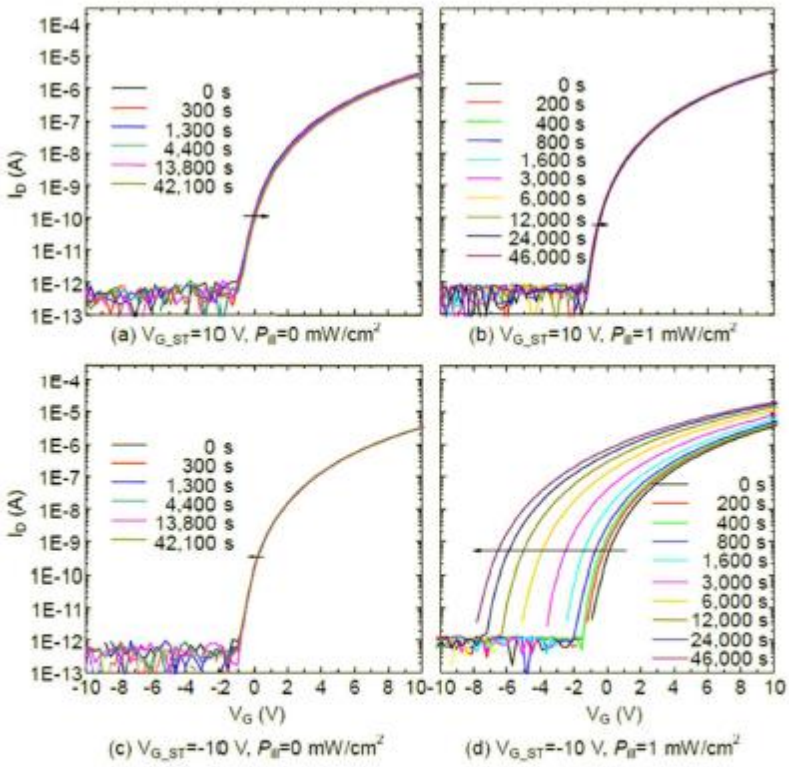


Figure 2.2.4 Evolution of the transfer characteristics of ZnO TFTs under positive or negative gate bias stress with/without light [31].

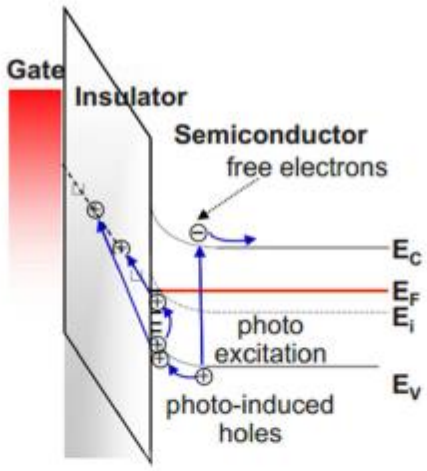


Figure 2.2.5 Schematic band diagram, which is based on trapping or/and injection of a photo induced hole carrier [30].

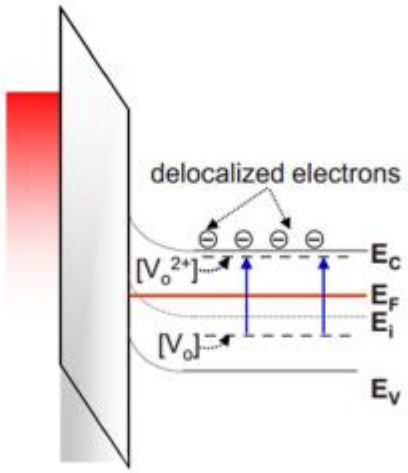


Figure 2.2.6 Schematic band diagram, which is based on transition of neutral oxygen vacancy [$V_O$] to [$V_O^{2+}$] charged state by photon irradiation [30].

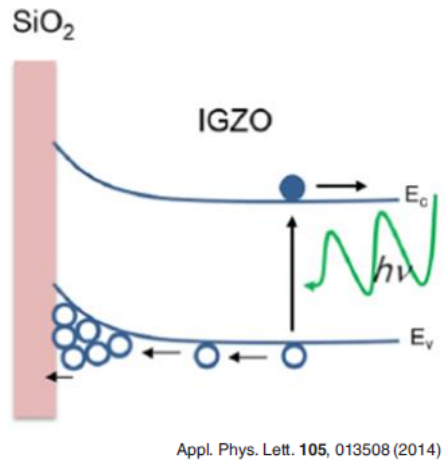


Figure 2.2.7 Effect of photon energy on IGZO at negative gate bias

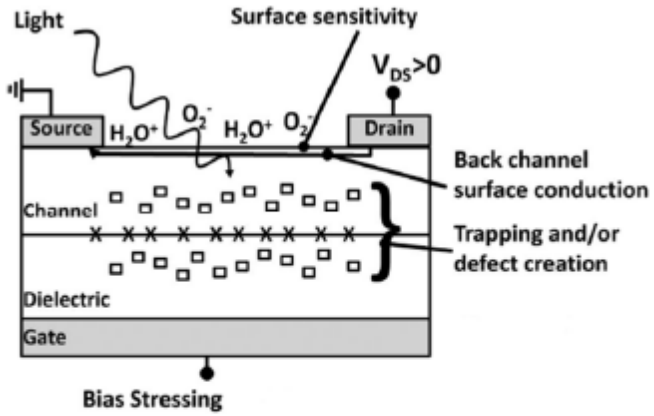


Figure 2.2.8 Schematic summary of the potential instabilities in the AOS TFTs [36].

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# 3. $In_2Ga_2ZnO_7$ oxide semiconductor based charge trap device for NAND flash memory

## 3.1. Abstract

The programming characteristics of charge trap flash memory device adopting amorphous $In_2Ga_2ZnO_7$ (a-IGZO) oxide semiconductors as channel layer were evaluated. Metal-organic chemical vapor deposition (MOCVD) and RF-sputtering processes were used to grow 45nm-thick a-IGZO layer on 20nm-thick $SiO_2$ (blocking oxide)/$p^{++}$-Si (control gate) substrate, where 3nm-thick atomic layer deposited (ALD) $Al_2O_3$ (tunneling oxide) and 5nm-thick low-pressure CVD (LPCVD) $Si_3N_4$ (charge trap) layers were intervened between the a-IGZO and substrate. Despite the identical stoichiometry and other physicochemical properties of MOCVD and sputtered a-IGZO, faster programming speed of MOCVD a-IGZO was observed. A comparable amount of oxygen vacancies was found in both MOCVD and sputtered a-IGZO, confirmed by X-ray photoelectron spectroscopy and bias-illumination-instability test measurements. Ultraviolet photoelectron spectroscopy analysis revealed the higher Fermi level ($E_F$) of the MOCVD a-IGZO (~0.3eV) film than that of the sputtered a-IGZO, which could be ascribed to the higher hydrogen concentration in the

MOCVD a-IGZO film. Since the programming in flash memory device is governed by the tunneling of electrons from channel to charge trapping layer, the faster programming performance could be the result of higher $E_F$ of MOCVD a-IGZO.

## 3.2. Introduction

Amorphous indium gallium zinc oxide (a-IGZO) has been widely investigated as the channel material for the display applications due to its high mobility, uniformity, and transparency [1-4]. Recently, a-IGZO has attracted attention as a new channel material for the semiconductor memory applications, such as the vertically integrated NAND (V-NAND) flash memory devices [5-10]. The present V-NAND adopts thin and poorly crystallized Si as the channel layer to minimize the cell-to-cell and device-to-device variability [8, 9]. However, the very low carrier (electron) mobility of such channel (<1 $cm^2/V \cdot sec$) deteriorates the device performance, which will eventually limit the maximum stackable number of device layers [1, 11,12]. Also, the limited critical dimension of the channel hole of the current V-NAND technology requires an alternative channel material that can improve its electrical characteristics without increasing its thickness [13]. In this regard, ZnO- and carbon-based channel have been attempted by other groups [14-18]. However,

ZnO channel suffers from the too high concentration of free carriers that requires carbon or other impurities as a carrier suppressor [14, 15]. The flash memory device using the ZnO channel showed very slow programming speed: ~2V of threshold voltage shift required a programming time of 3 sec even at a very high voltage of 30V [14]. Carbon-based devices show too low on/off ratio making its adoption to the V-NAND technology challenging [16, 17, 18]. In addition, previous work with ZnO from other group showed relatively slow program behavior, around 2V $V_{TH}$ shift after program time of 3 seconds at 30V [14]. Hence, a-IGZO with higher mobility and uniformity may be the viable solution for the next generation V-NAND technology. The authors' group has reported several works for the application of a-IGZO thin film as the semiconductor channel layer of charge trap flash (CTF) device, where the prototypical device structure is of thin film transistor (TFT) [4, 8, 9]. In such prototypical TFT devices, heavily-doped $p^{++}$-Si substrate serves as the control gate, and the thermally oxidized $SiO_2$ (20 nm), low-pressure chemical vapor deposited (LPCVD) $Si_3N_4$ (15nm) and LPCVD $SiO_2$ (5nm) layers were adopted as the blocking oxide, charge trap layer, and tunneling oxide layer, respectively. After these layers were fabricated on the $p^{++}$-Si substrate, the a-IGZO layer was sputter-deposited and patterned into the channel region. Then, metals with low work function, such as Ti and Al, were deposited and patterned to form

the source and drains. After the elaborate process optimization, the CFT-TFT showed feasible memory characteristics, where the threshold voltage ($V_{th}$) shift by the electron trap and detrap as high as several volts could be achieved [8, 9]. However, there were several critical problems: First, while the programming (positive $V_{th}$ shift) could be readily achieved by the electron trapping, erasing (negative $V_{th}$ shift) was almost impossible due to the almost complete lack of holes in the a-IGZO channel [2]. However, this problem can be mitigated when the pristine (or electron detrapped) state is taken as the data 0 whereas the programmed state represents data 1. Second, the program time was too long (several secs – hundred sec), which is probably due to too low tunneling current or too high blocking oxide leakage current [8, 9]. Third, the sputtering process of a-IGZO can hardly be adopted for the V-NAND structure fabrication due to the low step coverage. Also, the inherent involvement of physical damage effect by the energetic particle bombardment of the sputtering process may impose an adverse effect on the a-IGZO layer. Previous works from other groups on a-IGZO as a channel layer of charge trap device have been performed by varying the charge trapping, or tunneling oxides with the sputtered a-IGZO channel layer [19, 20]. However, due to the low step coverage of the sputtering process, an alternative deposition method with high step coverage is necessary.

To solve the problems mentioned above, in this work, thin (3nm) atomic layer deposited (ALD) $Al_2O_3$ thin film was adopted as the tunneling oxide to increase the tunneling current. Also, the metal-organic chemical vapor deposition (MOCVD), which is one of the efficient methods to deposit thin films with high uniformity with decent step coverage, was used to deposit the a-IGZO thin films. For comparison, the CTF-TFT devices adopting the conventional sputter-deposited a-IGZO thin films with identical remaining factors were also fabricated. The thin ALD $Al_2O_3$ film provided the device with much higher tunneling current than the previously adopted 5nm-thick LPCVD $SiO_2$ tunneling oxide [4, 8], which increases the programming speed by ~$10^6$ times while maintaining the reasonable retention time due to the decreased leakage current at low field. The sufficiently thick blocking oxide (thermally-grown 20nm $SiO_2$) revealed leakage current level below the detection limit of the test equipment, so the adverse effect of the blocking oxide leakage could be disregarded. Fermi level ($E_F$) of MOCVD a-IGZO film was higher than that of the sputtered film by ~0.3 eV, which also contributed to the much faster programming time. The detailed physical and chemical properties of the MOCVD and sputtered a-IGZO were compared by X-ray photoelectron spectroscopy (XPS) and ultraviolet photoelectron spectroscopy (UPS). The film reliability test results, such as the negative bias illumination stability (NBIS)

measurements, supplement the conclusion about the improved performance of the device using the MOCVD film.

## 3.3. Experimental Procedures

Bottom gated planar flash memory devices with MOCVD and sputtered amorphous $In_2Ga_2ZnO_7$ channels (~45nm thickness) were fabricated as shown in figure 1 (a). On top of the underlying heavily doped $p^{++}$ Si substrate (resistivity <0.005Ω cm), a thermal oxide (20nm $SiO_2$) was grown, which acts as a blocking oxide for the flash memory device. For the charge trapping layer and the tunneling oxide, 5nm-thick LPCVD $Si_3N_4$ and 3nm-thick ALD $Al_2O_3$ films were used, respectively. After the ALD $Al_2O_3$ film growth, the dielectric film stack was annealed at 1000 $^oC$ in the $O_2$ atmosphere for 60 min to decrease the charge loss at low electric field region and increase the charge transport at high electric field region through the $Al_2O_3$. Then, the a-IGZO was deposited as the channel layer via RF-magnetron sputtering or MOCVD. The sputtering and MOCVD were performed at substrate temperatures of 25$^oC$ and 370$^oC$, respectively, and were post-deposition annealed at 350$^oC$ for 60 min under air atmosphere. The precursors for In, Ga, and Zn were [3-(dimethylamino)propyl](dimethyl)Indium, trimethyl

Gallium, and diethyl Zinc, respectively, and the $O_2$ gas was used as the oxygen source during the MOCVD. The MOCVD reactor was of shower-head type optimized for very large scale substrates (760 x 920 mm, Jusung Engineering). The measured thickness of the two types of a-IGZO thin films was examined by the X-ray reflectivity (XRR, PANalytical, X'pert Pro). The amorphous structure of a-IGZO with two different deposition methods was confirmed by the X-ray diffraction, using Cu Kα X-ray radiation (XRD, PANalytical, X'pert Pro). The a-IGZO channel layer was patterned by photolithography and wet-etching with a diluted hydrofluoric acid solution. The channel width and length were 20 μm and 5 μm, respectively. The Al (100nm thickness) source/drain electrodes were deposited via electron-beam evaporation and patterned using the conventional lift-off method. Figure 1 (a) shows the schematic diagram of the flash memory device. Figure 1 (b) shows the top view optical microscopy image of the complete flash device. After the device fabrication, the samples were annealed at 350$^{o}$C for 60 min at the atmorphere condition to improve the contact between the Al metal and channel. The stoichiometry of MOCVD and sputtered a-IGZO films was confirmed by X-ray fluorescence spectroscopy (XRF, Thermoscientific, ARL Quant'X) and secondary ion mass spectroscopy (SIMS, Cameca, IMS-6F). Depth profile of the fabricated device structures were examined by the Auger electron spectroscopy (AES,

ULVAC-PHI, PHI-700). The physical and chemical properties of the MOCVD and sputtered a-IGZO films were examined by the atomic force microscopy (AFM, JEOL, JSPM-5200), XPS (AXIS-His, KRATOS) and UPS (AXIS-His, KRATOS). Charge trapping properties and other electrical characteristics were examined using an HP 4155A semiconductor parameter analyzer and AFG3101C pulse generator (Tektronix).

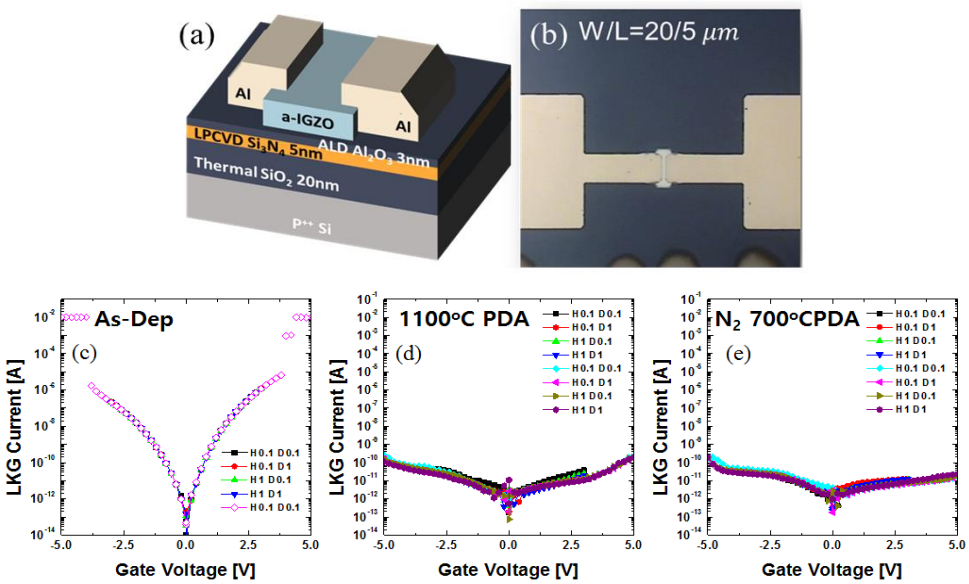



Figure3- 1. (a) Schematic diagram of the planar flash device. (b) top view of the planar flash device with width/length = 20/5 μm. (c)~(e) shows leakage current of TMA $Al_2O_3$ at various post deposition conditions

## 3.4. Results and Discussions

Thin film properties of MOCVD and sputtered a-IGZO

First, the cation stoichiometry of the MOCVD and sputtered a-IGZO was confirmed by the XRF, and the results are summarized in table 1. The molar ratio of In, Ga, and Zn content in the film was 2:2:1 which was identical for both MOCVD and sputtered (a-$In_2Ga_2ZnO_7$). The density and thickness of each film were confirmed by the XRR measurements, as shown in figure 2 (a). The thickness of the two films was ~45nm, and the density was 4.99 g/cm$^3$ for MOCVD and 5.12 g/cm$^3$ for sputter a-IGZO. No significant change in density was observed for both films after post-deposition annealing (PDA) at 350$^o$C for 1hour. The higher density of the sputtered a-IGZO film may be due to the strong ion bombardment effect on the substrate during the sputtering process. Figure 2 (b) shows the XRD patterns of the two types of films before and after PDA. All the films did not show any notable diffraction peaks suggesting the amorphous structure of the films. Figures 3 (a) and (b) show the AFM topographic images of the as-deposited samples, and figures 3 (c) and (d) show the same for the annealed samples. Surface roughness was higher in case of the MOCVD a-IGZO, before and after annealing, compared with the sputtered film, and such observation is consistent with the higher density of the latter film resulting smoother surface roughness. PDA slightly improved the surface smoothness, which may

contribute to the improved electrical performance of the fabricated devic e. Since MOCVD uses carbon containing precursors, contamination of t he film with the residual carbon is concerned, whereas the sputtered fil m has a low chance of involving carbon. To address this potential issu e, SIMS depth profile was performed before and after the PDA of both MOCVD and sputtered films which can be seen in figure 4. The MO CVD film showed slightly higher carbon-related signals than the sputter ed film, but the overall intensity was quite low suggesting that the resi dual carbon concentration could be disregarded in further analysis. The annealing did not induce any notable change in any of the film compo nents. The films showed uniform composition along the depth direction except for the slight gradual decrease in Zn concentration near the film surface for the MOCVD film, which might be related with the rather h igher vapor-pressure of Zn-containing species during the MOCVD due t o the higher MOCVD temperature of 370 $^{o}$C.

**TABLE 3-I.** XRF results of MOCVD and Sputter a-$In_4Ga_4Zn_2O$ [at %]

| | In | Ga | Zn |
|---|---|---|---|
| **MOCVD** | **41.1** | **40.8** | **18.1** |
| **SPUTTER** | **41.4** | **40.2** | **18.4** |

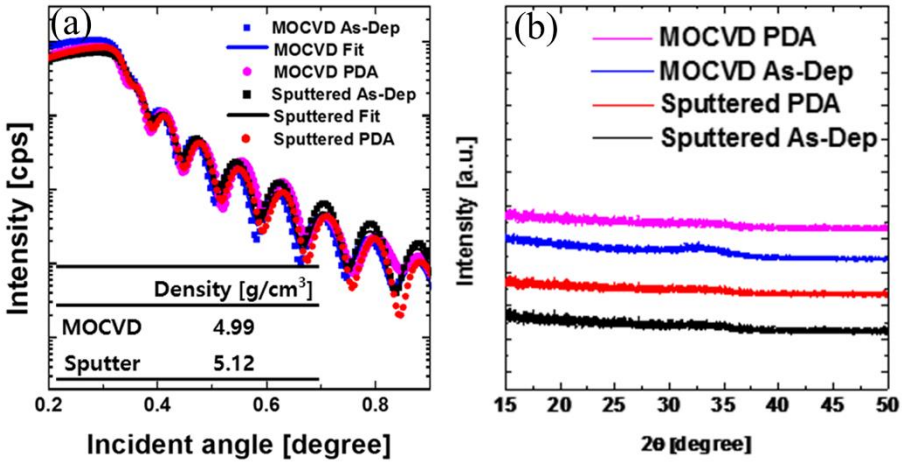



Figure3- 2. (a) XRR and (b) XRD spe ctra of MOCVD and Sputtered a-IGZO.

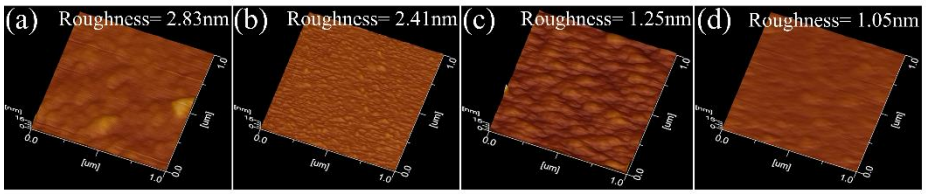



Figure3- 3. AFM topographic images of a-IGZO films. As deposited (a) MOCVD, (b) Sputtered a-IGZO and annealed (c) MOCVD, (d) Sputtered a-IGZO

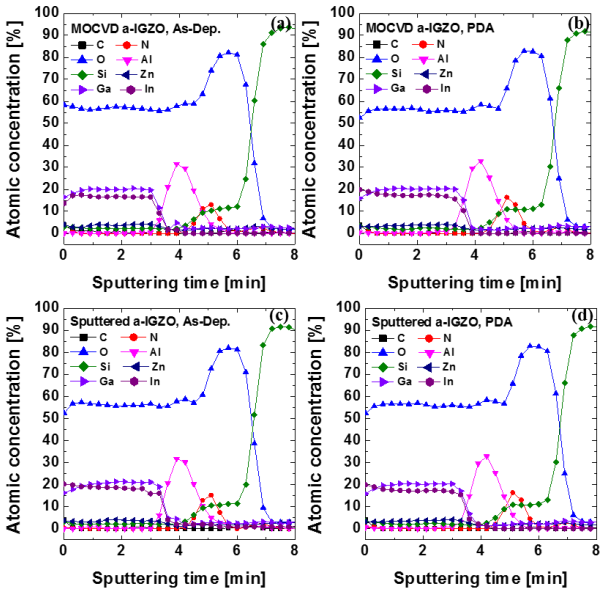



Figure3- 4.2. AES depth profile results of as-deposited and annealed MOCVD ((a) and (b)) and sputtered a-IGZO ((c) and (d)).

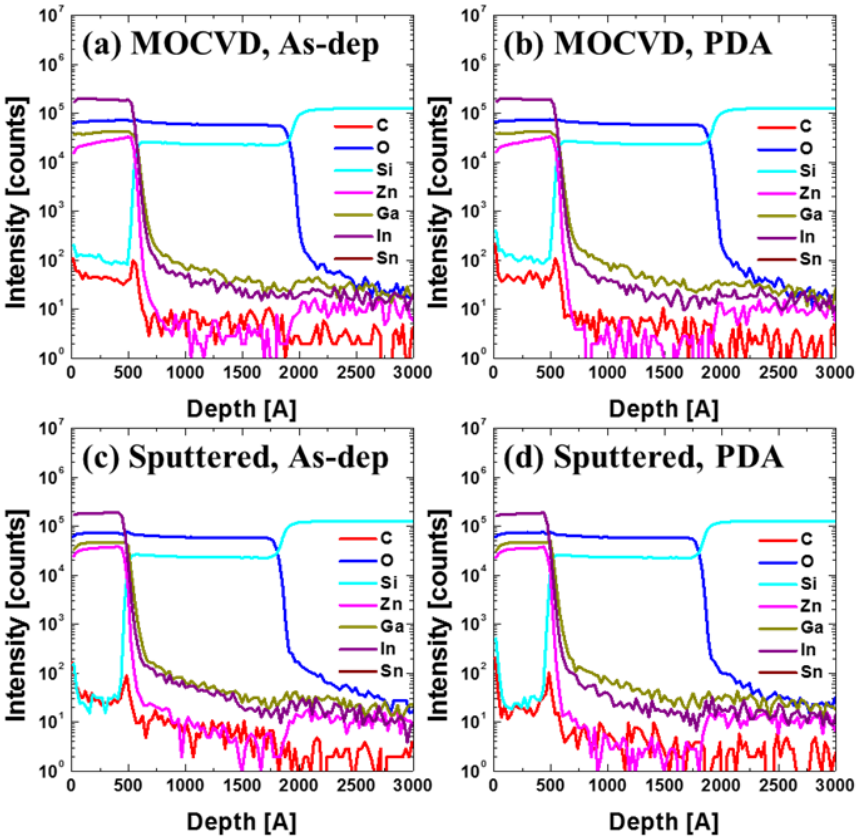
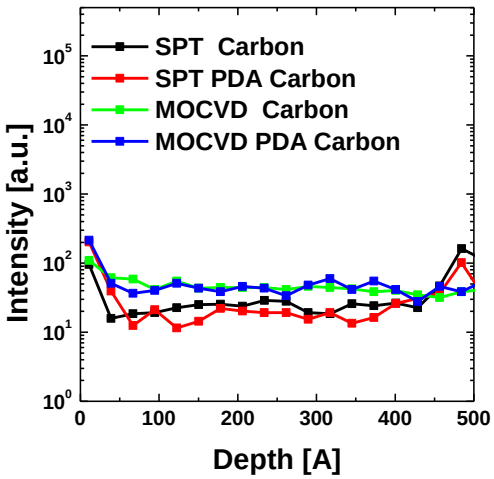



Figure3- 5. SIMS depth profile results of as-deposited and annealed MOCVD ((a) and (b)) and sputtered a-IGZO ((c) and (d)).



Program characteristics of MOCVD and sputtered a-IGZO planar flash device

Figure 5 shows well-behaving transfer characteristics (drain current – gate voltage (Id – Vg)) of the control TFT devices, where the tunneling oxide and charge trap layers were omitted, and the only 100nm-thick SiO2 layer was used as the gate oxide. The same PDA was performed after the a-IGZO film deposition. The ratio between on- and off-current was as high as ~107. The estimated basic device parameters from these Id-Vg curves are summarized in table 2, where the subthreshold swing (SS) and saturation mobility values (μsat) were almost identical for the two devices suggesting the similar interface quality. However, the Vth, defined as the Vg at which Id of 1nA flows, of the TFT with MOCVD film was much lower (-2.71 V) than that of the device with the sputtered film (0.21 V). The latter value coincides with the previous reports [9], but the much lower Vth of the former device indicates that the carrier (electron) concentration of the MOCVD a-IGZO film was much higher than that of the other film. This factor is quite beneficial in achieving the high programming speed in the CFT-TFT device as shown below, and favorable to set the read voltage to 0V for the CTF TFT memory, which is a standard method of Si-based NAND flash.

Figures 3-6 (a) and (b) show the $I_d$-$V_g$ curves of the CTF-TFT with MOCVD and sputtered films, respectively, at the pristine state (black

square symbol), programmed state (red circle symbol), and erased state (green triangle symbol). In these cases, the program and erase operations were performed by applying +20 V and -20 V, respectively to the $p^{++}$-Si gate for 100 ms. The pristine devices show degraded SS values (0.225 V/dec.) compared with the control devices in figure 3-5, due to the involvement of $Si_3N_4$ CTL and $Al_2O_3$ layers, which is also the case for standard Si-based CTF flash devices [9]. The programming operation induced the positive $V_{th}$ shift in the MOCVD (3.12 V) and sputtered (1.63 V) film devices suggesting the fluent electron trapping at the CTL. The almost doubled $V_{th}$ shift for the former case compared with the latter case suggests that the charge transfer during the high $V_g$ application was much faster in this case. Considering the thickness of the blocking oxide (20 nm) and assuming that the electrons are uniformly trapped across the 5nm-thick $Si_3N_4$ layer, the trapped electron density was ~$1.68 \times 10^{18}$ $cm^{-3}$ and ~$8.74 \times 10^{17}$ $cm^{-3}$ for the MOCVD and sputtered film devices, respectively. The programmed state did not show any notable degradation in SS. The -20 V application induced the detrapping of the carriers from the CTL to a-IGZO channel, recovering the $V_{th}$ values (erase operation). In standard Si-based CTF flash device, the erase operation also induces hole trapping making the $V_{th}$ shifted more toward the negative bias direction compared with the pristine state [10-12]. However, in these cases, such a fluent erase cannot be achieved due to

the almost complete lack of holes in the a-IGZO channel [2, 13]. In fact, the erased state also involves the $V_{th}$ values slightly higher than that of the pristine state, suggesting that the complete detrapping of the trapped carriers did not occur during the -20 V of $V_g$ application. Nevertheless, a voltage margin of 2.39 V was obtained between the two states for the case of the MOCVD film, and thus, the two states could be clearly discerned when the read voltage was set to 0V. In contrast, the sputtered a-IGZO device showed a much inferior separation between the programmed and erased states, only 1.19 V of $V_{th}$ margin, which does not allow the full on-off current ratio. Another problem is that the read voltage cannot be set to 0 V since the $V_{th}$ of programmed state is not sufficiently positive. These device features clearly demonstrate the superior performance of the MOCVD a-IGZO film as the channel layer in IGZO CTF-TFT compared with the same device adopting the sputtered film. Next, programming and erase performances were further examined under the different voltage and times.

Figures 3-6 (c) and (d) show the shift in $V_{th}$ ($\Delta V_{th}$) during the programming and erasing, respectively, of the MOCVD and sputtered film devices for the three different voltage amplitudes of 16, 18, and 20 V. As can be expected, the higher the voltages the shorter the programming and erasing time for both types of devices. For the case of the MOCVD device, a $\Delta V_{th}$ of ~1.8 V and ~3.0V can be achieved at the

program time of 1 ms, and 10 ms, when the program voltage was 20 V, but $\Delta V_{th}$ of only ~1.9 V could be achieved at a time as long as 1 s for the case of the sputtered device. The erasing performance was generally much faster than the programming case, where an abrupt change in $\Delta V_{th}$ could be observed only after the erase time of 0.1 ms, and a further increase in the erase time induced an only marginal increase in $\Delta V_{th}$ for all cases. While the maximum erasing $\Delta V_{th}$ for the sputtered device was limited to ~1.2 V even at 1s, it could be as high as ~2.4 V for the MOCVD device after the same erasing time.

Figures 3-7 (a) and (b) show the retention estimated at room temperature and 85 $^{o}$C, respectively, for the two types of devices. To make the comparison fair, devices with similar programmed $V_{th}$ were chosen when they have programmed with 20 V and 100 ms. The erasing was performed using a -20 V and 100 ms long pulse. Both devices show stable operation at room temperature up to $10^4$ s, but showed decay at 85 $^{o}$C due to the thermally activated charge detrapping. Extrapolation of the data indicates that the 10-year-lifetime of the written data cannot be guaranteed especially for the sputtered device, which must be supplemented by further study. Figure 3-7 (c) shows the switching endurance performance of the two types of devices. Both devices demonstrate stable cycling up to $10^4$ cycles, which is already sufficient number as a NAND flash memory element, considering the current wear-

leveling technique. All these features demonstrate clearly the superior performance of the CTF-TFT adopting the MOCVD a-IGZO film as the channel layer compared with the other cases.

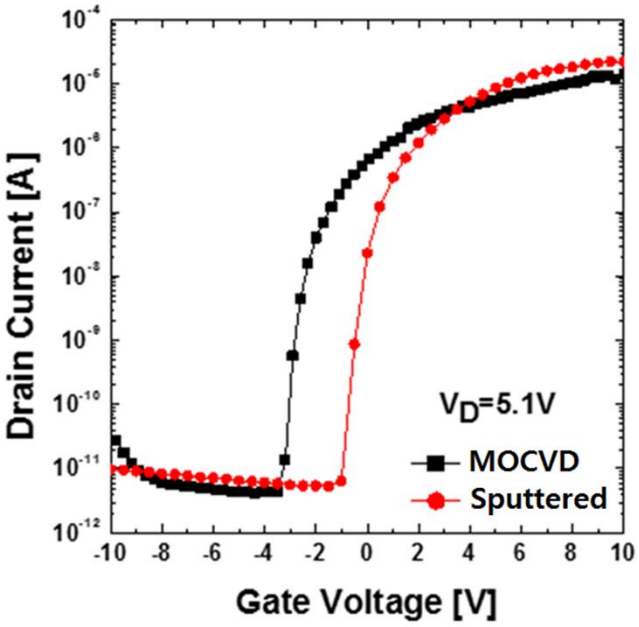



Figure3- 6. Transfer characteristics of MOCVD and Sputtered a- IGZO control TFT devices.

Table 3-2. Basic device parameters of MOCVD and Sputtered a-IGZO TFT.

| | $V_{th}$ [V] | S.S. [V/dec] | $\mu_{sat}$. [$cm^2$/Vs] |
|---|---|---|---|
| MOCVD | -2.71 | 0.182 | 19.3 |
| Sputtered | 0.21 | 0.189 | 22.1 |

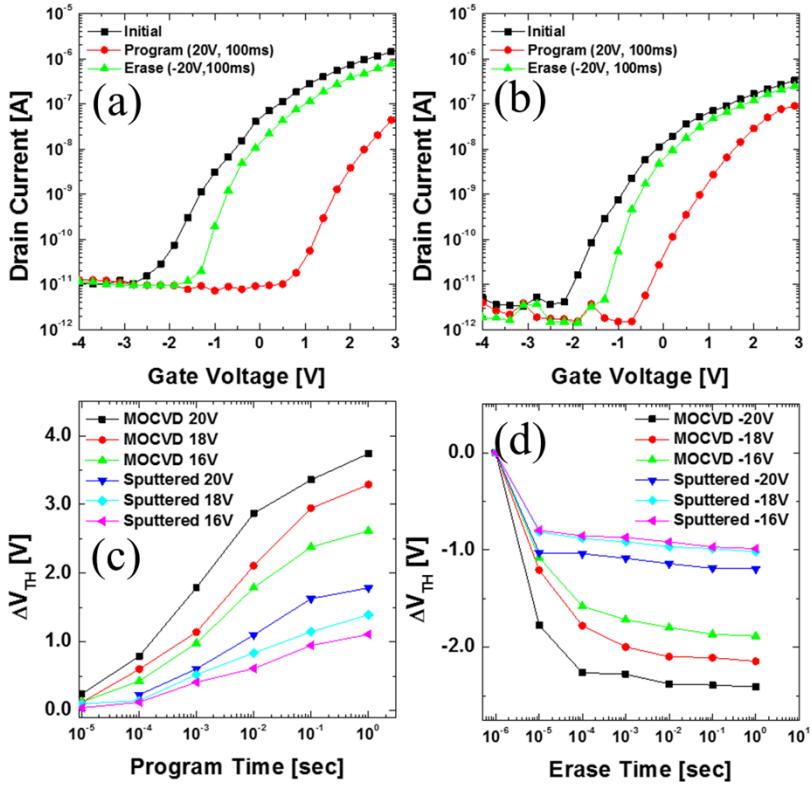



Figure3- 7. Program and Erase characteristics of MOCVD and sputtered a-IGZO flash memory devices ((a) and (b)). Threshold voltage shift of MOCVD and sputtered a-IGZO at various (c) program voltage and time and (d) erase voltage and time.

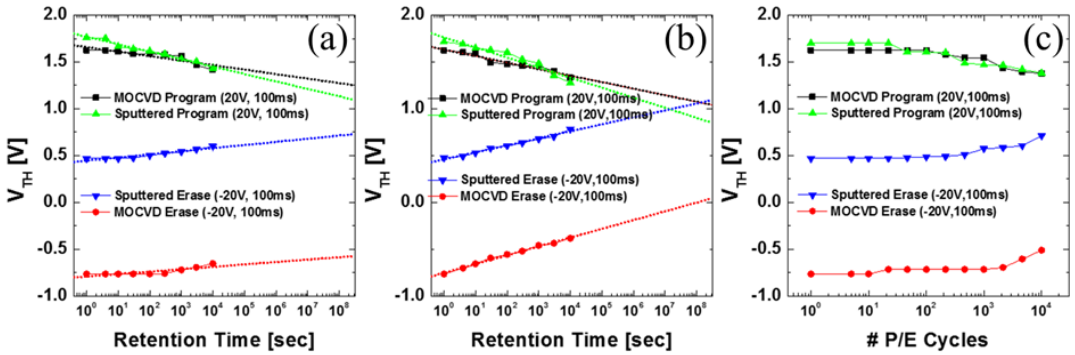



Figure3- 8. Retention characteristics at (a) 25ºC, (b) 85ºC and (c) endurance characteristics of MOCVD and sputtered a-IGZO

Analysis of the different programming behavior of MOCVD and sputtered IGZO

Next step is to examine the potential reasons for the better performance of the MOCVD film. These could be achieved by electrical reliability tests and further physical-chemical analysis to compare the electronic energy structures of the two a-IGZO films. To verify that the different programming behavior was only from the electron trapping at the $Si_3N_4$ layer, without any assistance from the possible bulk traps of the a-IGZO, positive bias stability (PBS) measurements were conducted as shown in figure 3-8. The same MOCVD and sputtered a-IGZO channel and Al source/drain layers were deposited on the $SiO_2$ (thickness of 100nm), which was thermally grown on a $p^{++}$Si substrate (no charge trapping layer). After positive 20V stress for 300 seconds, MOCVD a-IGZO showed only 0.2V $V_{th}$ shift while sputtered a-IGZO showed 1.18V $V_{th}$ shift. No change in the SS value was observed, which indicates no additional interfacial traps were generated during PBS. It is well known that such shift in $V_{th}$ of a-IGZO devices is due to the electron trapping at or near the interface without the creation of new defects [2, 13]. Due to the strong bombardment of cations to the surface, an increase in interface trap can be expected for the sputtered a-IGZO device. The higher shift in $V_{th}$ of the sputtered device after the PBS test also corroborates the lower

recovery of $V_{th}$ after the erase voltage application shown in in figures. 3-6 and 3-7. From the PBS results, therefore, it can be understood that the faster program behavior of MOCVD a-IGZO flash was owing to the faster charge trapping at the $Si_3N_4$ layer without the assist from the bulk or interface traps.

From the authors' previous research, it has been elucidated that the amount of oxygen vacancy in the amorphous oxide semiconductor can be estimated from the NBIS measurements [15]. Therefore, the NBIS of MOCVD and sputtered a-IGZO were measured under the negative bias of 20V with a light source with wavelength 450nm, and the results are summarized in figure 3-9, which shows almost identical NBIS performances. Since the change in Vth from NBIS is mainly caused by the ionization of the oxygen vacancies, the similar results between MOCVD and sputtered a-IGZO reveal that both films contain a comparable amount of oxygen vacancies [16, 17]. Therefore, oxygen vacancy effect on the different programming performance can be neglected.

The faster programming speed for the given tunneling oxide and CTL conditions could be inferred from the lower Schottky barrier for electron tunneling from the channel layer (a-IGZO) and tunneling oxide ($Al_2O_3$). Therefore, the energy level of $E_F$ of the MOCVD and sputtered a-IGZO films were further scrutinized as follows [18].

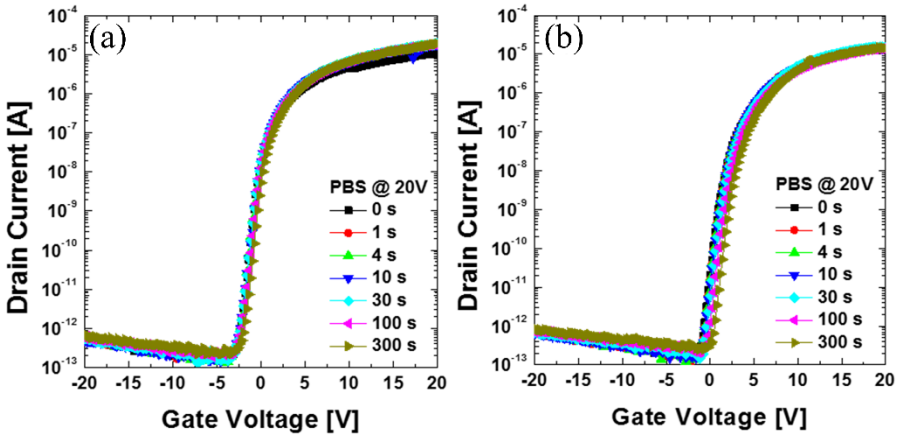



Figure3- 9. Positive Bias Stability (PBS) results for (a) MOCVD and (b) sputtered a-IGZO. After 300 sec, MOCVD a-IGZO showed 0.2V Vth shift while sputtered a-IGZO showed 1.18V $V_{th}$ shift

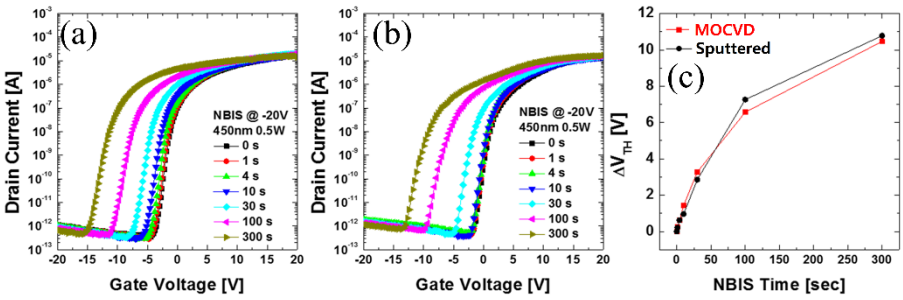



Figure3- 10. Negative Bias Stability results for (a) MOCVD, (b) sputtered a-IGZO and (c) $\Delta V_{th}$ comparison

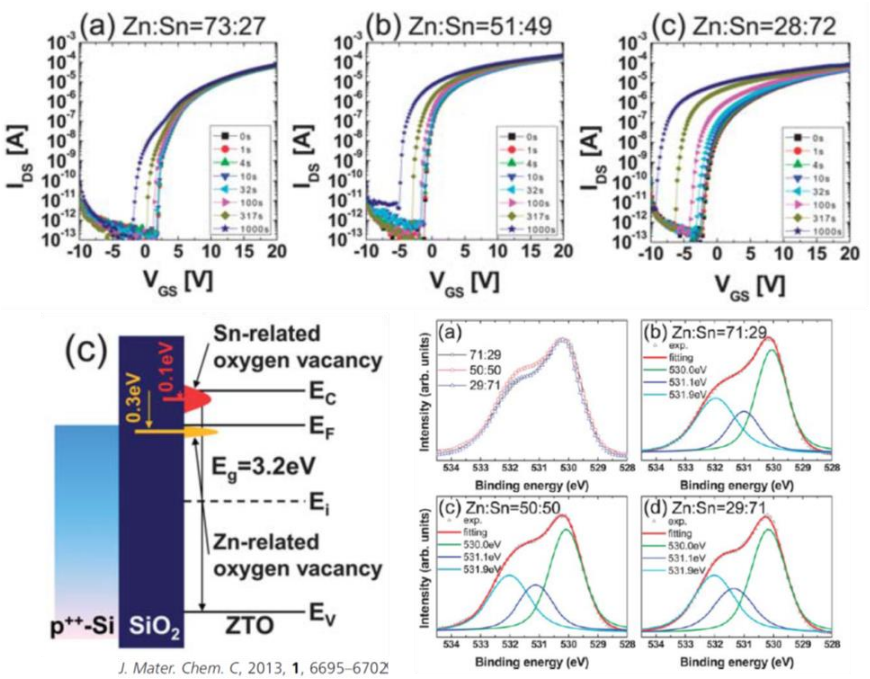



Figure 3-9.2. NBIS of ZTO with various Zn:Sn composition [20]

Investigation on the chemical state of MOCVD and sputtered a-IGZO

The chemical states of the two types of the a-IGZO films were investigated through the XPS, as shown in figure 3-10. The a-IGZO and many of the ZnO-based amorphous oxide semiconductors are known to have a large number of oxygen vacancies, which produces electrons as majority carriers [19]. Figure 3-10 (a) shows the oxygen 1s peak for the MOCVD and sputtered a-IGZO. The bonding energy of the O1s peak in IGZO is known to have three sub-peaks: O lattice (~529.1eV), O deficient (~529.7eV) and OH impurity related (~530.9eV) [20, 21]. However, the O1s peaks shown in figure 10 demonstrate similar full width at half-maximum (FWHM) and peak intensity making it difficult to state that there was a significant difference in oxygen stoichiometry. Hence, the results from the metal cations have to be considered as well, as shown in figures 3-10 (b), (c) and (d). No discernable differences in the FWHM and peak intensity of the metal species peak, suggesting that the overall chemical environments are quite similar. For the sputtered a-IGZO, nonetheless, all peaks shifted towards the lower binding energy compared to the MOCVD a-IGZO, suggesting that the $E_F$ of the two samples are different.

The binding energy (BE) in XPS is governed by the equation (3-1):

$$BE = h\nu - E_{kin} - (E_{vac} - E_F) \qquad (3\text{-}1)$$

, where hv, $E_{kin}$, and $E_{vac}$ are the incident X-ray energy, the kinetic energy of the electron, and vacuum level, respectively. Therefore, the uniform shift of BE in the XPS spectra indicates that the $E_F$ of MOCVD film is higher than that of the sputtered film, which may have influenced the program efficiency.

UPS analysis was used to estimate the $E_F$ values of the two films, as shown in figure 3-11 (a). By definition, the work function of the material can be found by subtracting cutoff energy from the UPS result from the energy of the light source (21.22 eV for UPS instrument used in this study) [22]. From the linear extrapolation of the result, the $E_F$ of MOCVD IGZO was found to be ~0.3eV higher than that of the sputtered a-IGZO.

For the programming in flash memory device, the electrons must be transferred from the channel region to charge trapping layer via tunneling through the tunneling oxide. Therefore, the higher $E_F$ of the MOCVD film suggests a lower barrier for tunneling under the programming condition, which can explain the faster programming performance of the MOCVD a-IGZO device compared with the sputtered a-IGZO device. The time-of-flight SIMS (ToF-SIMS) profile data of hydrogen atoms of the two types of the films before and after the PDA are included in figure 3-11 (b). Due to the lack of appropriate references for the ToF-SIMS data

quantization, estimation of absolute H-concentration is difficult. However, it is obvious that the H-concentration in the MOCVD film is higher than that of the sputtered film, of which concentration does not vary after the PDA. The higher H-concentration of the MOCVD film could be induced by the thermal cracking of the ligands of the MO-precursors.

It has been reported that the incorporated hydrogen atoms in the IGZO easily ionized to H+ ions generating electron carriers [23, 24]. This is consistent with the lower $V_{th}$ of the control TFT shown in figure 4, which indicates a higher carrier concentration in the MOCVD a-IGZO channel. The increased carrier concentration increases the $E_F$ level and decreases the tunneling barrier height at the interface with the $Al_2O_3$ tunneling oxide.

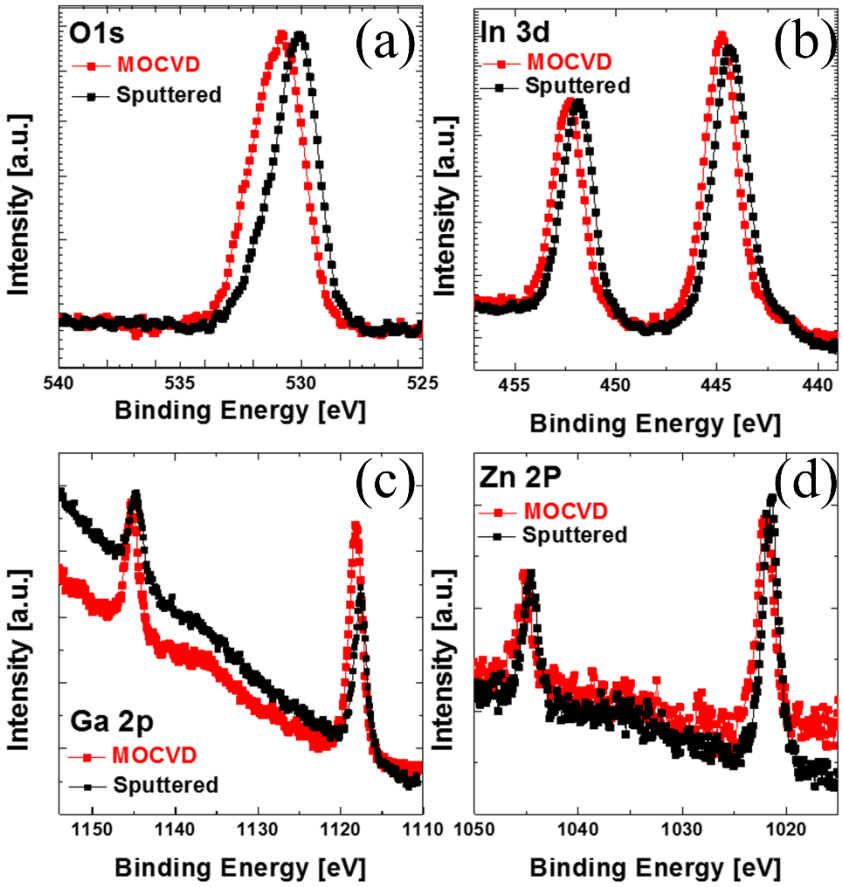



Figure3- 11. XPS for MOCVD and sputtered a-IGZO

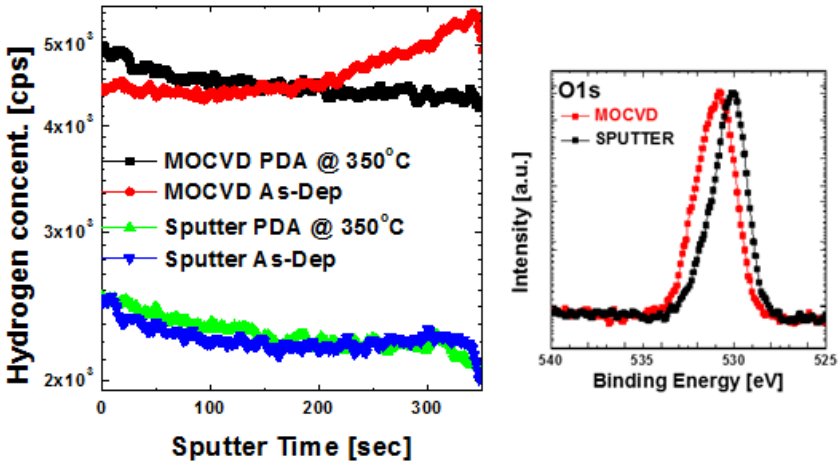



Figure 3-11. TOF-SIMS results of Hydrogen concentration in MOCVD and sputter a-IGZO for before and after PDA of 350oC for 60min and XPS binding energy spectra of O1s for MOCVD and Sputter a-IGZO,(O lattice (~529.1eV), O deficient (~529.7eV), OH impurity related (~530.9eV))

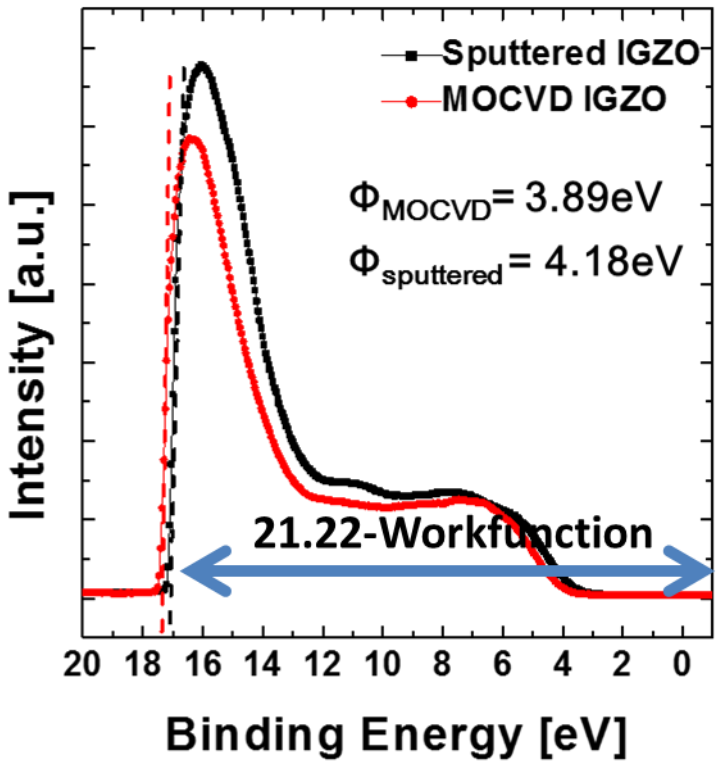
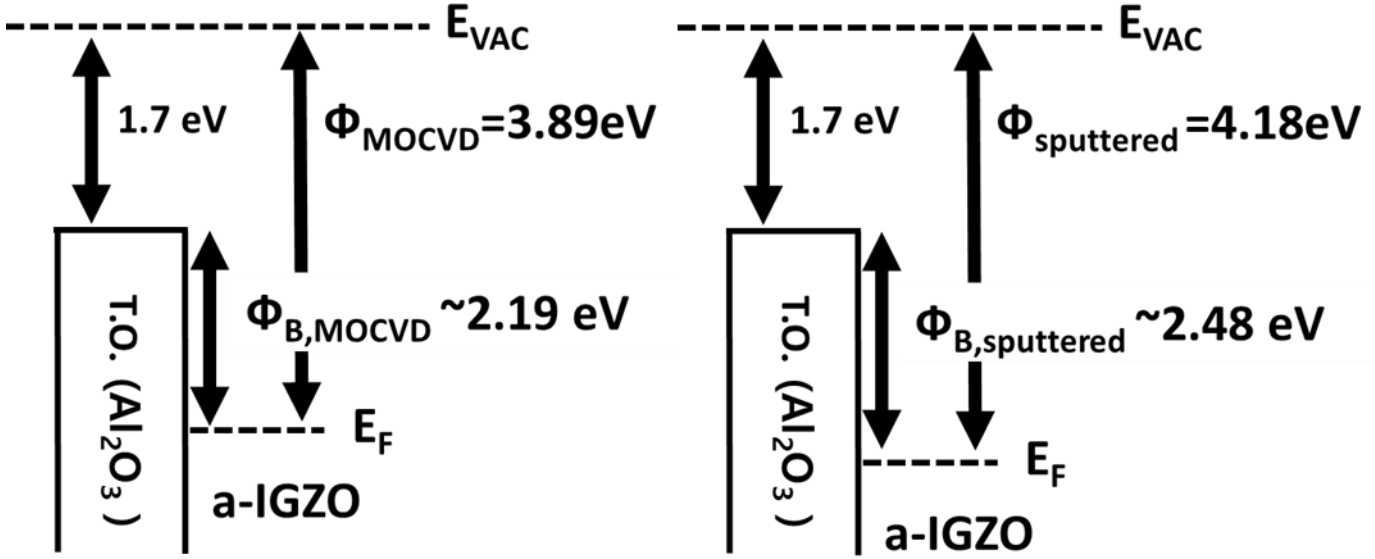



Figure 3-12 UPS comparison of Sputtered and MOCVD IGZO


E_VAC
1.7 eV
Φ_MOCVD=3.89eV
Φ_B,MOCVD ~2.19 eV
E_F
T.O. (Al2O3)
a-IGZO
E_VAC
1.7 eV
Φ_sputtered=4.18eV
Φ_B,sputtered ~2.48 eV
E_F
T.O. (Al2O3)
a-IGZO

## 3.5. Conclusion

The programming characteristics of charge trap flash memory device adopting a-IGZO oxide semiconductors as channel layer were evaluated. Despite the identical stoichiometry of MOCVD and sputtered a-IGZO, confirmed by the XRF and SIMS profile, faster programming speed of MOCVD a-IGZO was observed. The effect of oxygen vacancy as the cause of the different programming performance can be neglected because the comparable amounts of oxygen vacancies were estimated to be present in both MOCVD and sputtered a-IGZO, using XPS and NIBS analysis. UPS analysis has revealed the higher $E_F$ in the case of the MOCVD IGZO (~0.3 eV) than the sputtered a-IGZO, which could be the cause for such faster programming performance. The incorporation of hydrogen atoms in the MOCVD a-IGZO film appears to constitute the main reason for the higher carrier concentration which induced, the higher $E_F$ and consequently lower Schottky barrier between the a-IGZO channel and $Al_2O_3$ tunneling oxide layer. The programming threshold voltage shift of ~1.8 V and ~3.0 V could be achieved by applying the 20 V of $V_g$ for 1 ms and 10 ms, respectively, to the MOCVD CTF TFT. The erase voltage (-20 V) application for as short as 1 ms was sufficient to recover more than 70% of the shift $V_{th}$, which allowed the fluent NAND type device application with the standard read voltage of 0 V. Feasible

retention and endurance performances were also confirmed. Sputtered a-IGZO film, despite with identical thickness, cation composition, and even higher density, did not permit such high performance due to the higher carrier trapping within the channel or interface with the dielectric layers.

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# 4. Investigation on the composition dependence of InGaZnO (Ga/Zn ratio)

## 4.1. Introduction

To date, charge trapping devices are shifting its paradigm from planar to vertically NAND (VNAND). In fabrication, there are three major structures of VNAND which are; BiCs, piped-BiCs, TCAT [1]. All three of these devices structures use Fowler Nordhiem tunneling (F.N. tunneling) to program its cells and either GIDL or F.N. tunneling for the erase operation. Other than programming mechanism, these devices structures share the same facts that they all require uniform etch hole with relatively limited diameter to fill-in the blocking oxide, charge trapping, blocking oxide, and channel [2]. So called macaroni structure is fabricated by depositing layers if $Si_3N_4$ and $SiO_2$ in sequence. Then etch hole process is followed, which requires uniform hole diameter along the depth. Within the etch hole, ONO is deposited by chemical vapor deposition process or atomic layer deposition process to ensure step coverage. Polycrystalline Si (or a-Si:H) is filled in as the channel layer. At this date, current density of the cell has no problem, but as the depth of etch hole gets deeper (string in final structure), uniform channel on current emerges as an issue. Estimated on current with respect to the

stacking layers for poly-Si is listed on table 4-1. As indicated on the table, the saturation current will decrease as the stacking layer increases, causing an un-readable saturation current (On current) of the cell,

Amorphous oxide semiconductors (AOSs) have been widely researched for thin-film transistors (TFTs) in high performance display devices due to its transparency and superior carrier transport properties. Since the AOSs are composed of post-transition-metal cations which have a large wave function overlap with neighboring atoms in the s-orbitals, the electrical properties are not significantly altered from the atomically regular crystalline material even when in the amorphous structure. As a result, a high carrier density and mobility care obtained [3].

Since the report of Hosono in 2004 on transparent and flexible TFTs using amorphous indium gallium zinc oxide (a-IGZO), a-IGZO have received considerable attention in display applications, such as active-matrix liquid crystal displays, active matrix organic light-emitting diodes, and flexible displays. Such was due to their superior electrical performance compared with conventional AOSs TFTs. Recently, it was reported that AOSs can be potentially utilized in low-voltage logic devices, as well as memory applications [4-5]

There has been numerous reports on effect of composition of IGZO [6-10]. In general, electrical properties of IGZO vary depending on the composition of the cations. [11,12] abundance of Ga results in a low carrier concentration because of the high oxygen binding energy, which is essential for use as a semiconductor. However, it also causes low electron mobility. [13] Indium, however, is known to cause high n-type carrier concentration and high electron mobility due to its large overlap of the In 5s orbitals [14,15, 16]. Zn can either stabilize the amorphous structure to its preferential tetrahedral structure. Both In and Zn may contribute to the carrier concentration (n-type) density, due to donor like trap generated near conduction band minima [17]. In such sense, change in the stoichiometry may alter the electron conductivity of the IGZO film, which may be suitable for limited hole sized VNAND technology.

In this experiment, ratio of Ga to Zn in IGZO thin film is varied, while keeping the atomic percent of In to be nearly constant. With three types of IGZO films with different Ga to Zn ratio, its growth-rate, density and crystallinity were examined by the X-ray reflectivity (XRR, PANalytical, X'pert Pro). Then, samples were fabricated to thin film transistors by photo-lithography process, where its basic electrical characteristics and stabilities were examined.

**TABLE 4-I. Estimated On current for Poly-Si & IGZO**

| Thickness 110Å $V_{READ}$ = 7V | Poly-Si | a-IGZO |
|---|---|---|
| $I_{D,SAT}$ @ 24stack ($L_{CH}$~1.3μm) | 600 nA | 0.902 mA |
| $I_{D,SAT}$ @ 48stack ($L_{CH}$~2.6μm) | 300 nA | 0.451 mA |
| $I_{D,SAT}$ @ 96stack ($L_{CH}$~3.9μm) | 150 nA | 0.226 mA |

$$I_{D,SAT} = \mu_{SAT} C_{ox} \frac{W}{2L} (V_G - V_T)^2$$

## 4.2. Experimental Procedures

Bottom gated thin film transistor (TFT) and planar flash memory devices with various a-InGaZnO thin films with various Ga to Zn ratio, with same amount of In content, were fabricated (Jusung Eng.) as shown in figure 4-1 (a) and (b). In case of the planar flash memory device, heavily doped $p^{++}$ Si substrate (resistivity <0.005Ω cm) substrate with thermal oxide ($SiO_2$ 20nm), which acts as a blocking oxide for the flash device, charge trapping layer and the tunneling oxide, LPCVD $Si_3N_4$ (15nm) and ALD $Al_2O_3$ (3nm, TMA 250$^oC$), respectively, were used. To overcome the poor leakage characteristics of TMA $Al_2O_3$, post deposition annealing (PDA) was conducted at 1,000 $^oC$ under vacuum. In case of thin film transistor, thermal oxide ($SiO_2$, 100nm) on heavily doped $p^{++}$Si substrate was used.

Various MOCVD IGZO with different Ga to Zn ratio were deposited by three different precursors, which were injected at the same time. Out of these three Ga showed fastest deposition rate, hence to control the composition of the final IGZO thin film, the flow amount had to be carefully controlled. The process temperature of MOCVD IGZO was 370$^oC$, and ozone and $N_2$ were used as the Oxidant and purge gas, respectively.

To fabricate planar charge trap memory, ant TFT, both types of IGZO were subject to the photo-lithography process. Wet-etching of each IGZO under diluted HF solution (500:1) was followed by the source drain pattering. Then, source and drain electrodes were deposited by electron beam gun evaporator, with al crucible with rotation speed of 12.8 rpm for final thickness of 100nm Al source and drain. Excess aluminum on un-wanted area was then removed by the lift off process with Acetone as the removing agent. The channel width and length were 20 μm and 5 μm, respectively. Figure 4-1 (a) shows the schematic diagram of the flash memory device and Fig. 4-1 (b) shows the top view optical microscopy image of the completed flash device.

To be safe from any damage caused during both deposition and patterning of the sample, post-deposition annealing was performed at 350$^{o}$C for 60 min under air atmosphere.

The Stoichiometry of MOCVD IGZO films were confirmed by X-ray fluorescent spectroscopy ((XRF, Thermoscientific, ARL Quant'X), which is listed on Table 4-2.

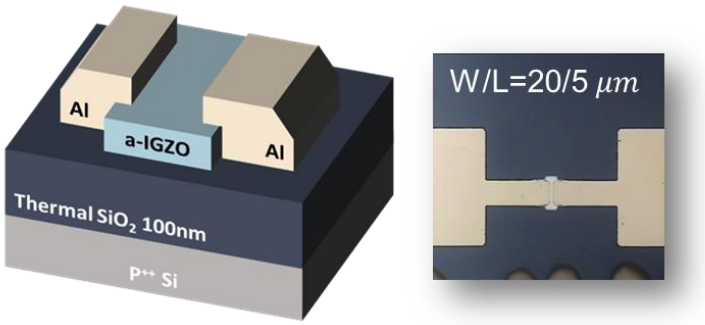



Figure 4-1. Figure 1. (a) Schematic diagram of the planar flash device. (b) top view of the planar flash device with width/length = 20/5 μm.

**TABLE 4-2. XRF results of MOCVD a-In4Ga x Zn 0.6- x O [at %]**

| | In | Ga | Zn | Ga/Zn | Dep Rate [A/s] |
|---|---|---|---|---|---|
| **MOCVD (REF)** | **41.1** | **40.8** | **18.1** | **2.3** | **3.91** |
| | **40.5** | **35.2** | **25.3** | **1.4** | **3.92** |
| | **40.5** | **47.4** | **12.1** | **3.9** | **3.8** |

## 4.3. Results and Discussions

### 4.3.1 Basic Thin Film Characteristics

Table 4-2 shows the stoichiometry and growth-rate of the IGZO thin films with different Ga to Zn ratios. The maximum Ga to Zn ratio was 3.9 and minimum was 1.4 atomic percent. Deposition rate varied as Ga to Zn ratio differed, which showed reasonable CVD deposition rate.

Figure 4-2 shows the XRR image of Ga:Zn 2.3,3.9, and 1.4. All three films had thickness around 50nm and relatively same density (inset to show the critical angle of the XRR image, which represents the density).

Figure 4-3 shows the XRD image of each IGZO. Despite the gradual increase in Ga content, the purely amorphous nature was observed only when Ga to Zn ratio was 2.3 (In:Ga:Zn = 4:4:2). Such is in contrary to previously known phenomenon where Ga is known to cause amorphous nature of the film. Such behavior was observed from various other compositions, which is shown in Figure 4-3 (b).

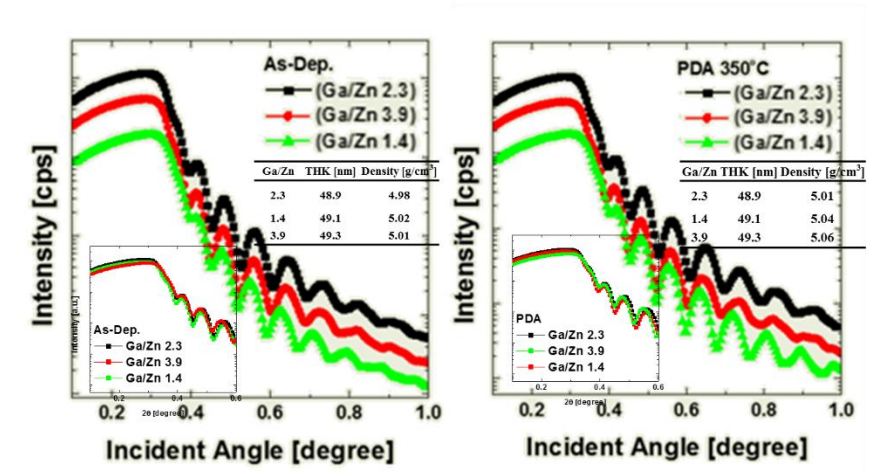



Figure 4-2.XRR Results of three IGZO thin films with different Ga to Zn ratio , before and after PDA of 350°C

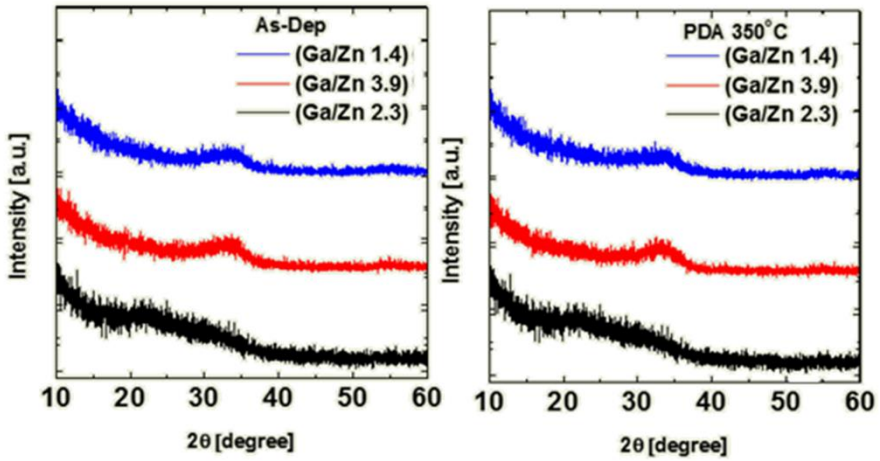



Figure 4-3.XRD Results of three IGZO thin films with different Ga to Zn ratio , before and after PDA of 350°C

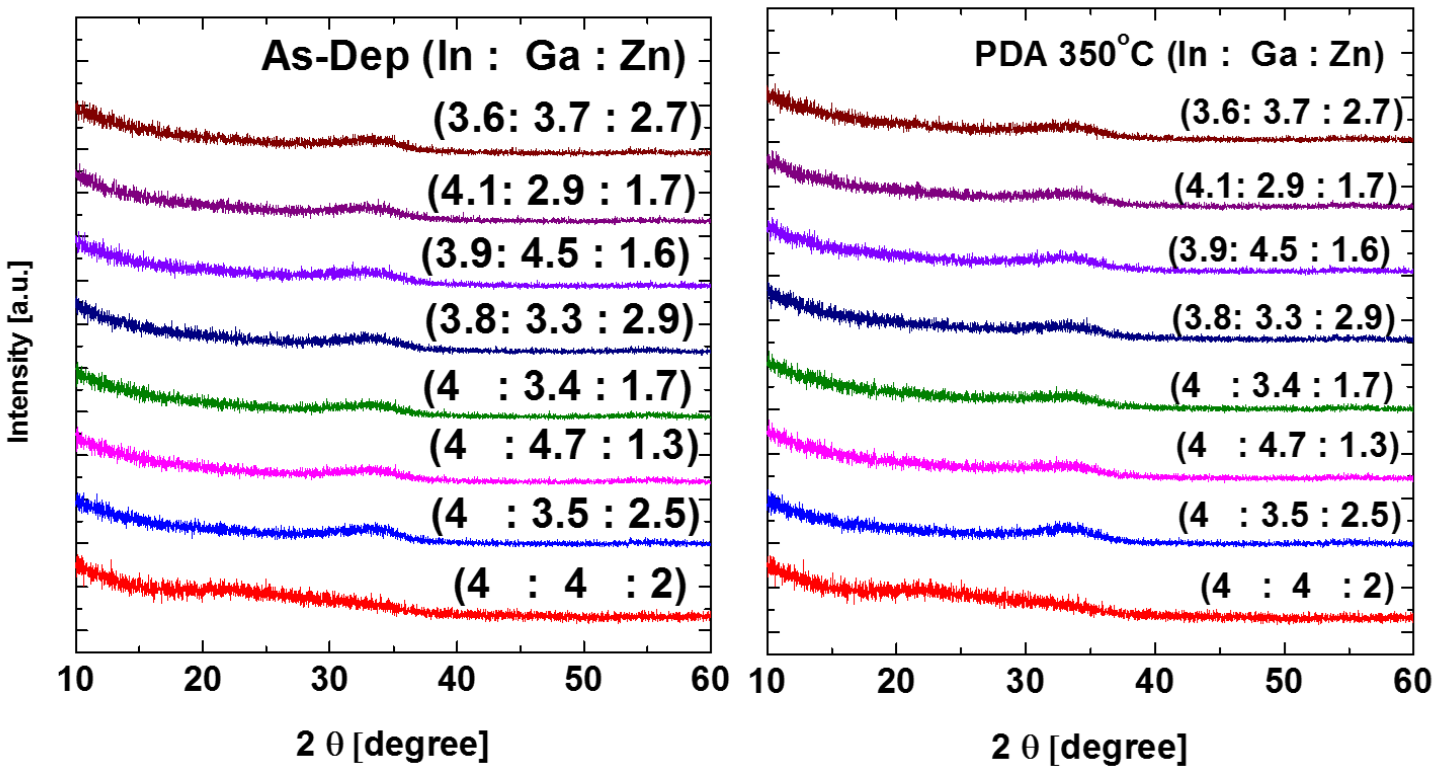



Figure 4-3 (b) .XRD Results of three IGZO thin films with different Ga to Zn ratio , before and after PDA of 350°C

### 4.3.2. TFT Characteristics

Figure 4-4 shows the transfer curves of various Ga:Zn IGZO TFTs. Figure 4-3 and 4-3(b) has shown that other than the Ga:Zn 2.3, all sampels showed nano crystalline like phase. If such nano crystalline phase may act as a trap site for TFT, hysteresis in the transfer curve has to be shown, which was the case. The characteristics from the transfer curves are summarized in table 4-3. Despite the previous consensus that Ga causes low electron mobility was contradicted in the saturation region. Despite the highest field effective mobility with minimum Ga amount, questions on highest saturation mobility of Ga still remains to be answers. Secondary ion mass spectroscopy might be give the answer to such phenomenon if non-uniform composition of Ga along depth was found.

To understand abnormally on mobility by TFT, ToF-SIMS depth profile was conducted to confirm the various cation composition along the depth of the film. As can be seen from the figure 4-5, uniform composition along the depth was found. Relative amount of In, Ga, Zn were indistinguishable among the three IGZOs with different Ga/Zn ratio. However, Zn showed significant change, smaller cps of Zn with respect to the Ga/Zn ratio, hence the ratio indicated in this work is verified. ToF-SIMS has wide M/Z [amount of molecule/ charge amount], but it has low resolution. Hence, measuring the amount of hydrogen by ToF-SIMS has to be conducted with care. The figure 4-5 indicates that there are no

significant change in the amount of hydrogen. Further characterization of thin film characteristics was conducted by XPS analysis. (Figure 4-6). Slight shift in Oxygen peak was observed with similar peak shift in other cations. Such may indicate that the fermi level has shifted. In part 3 of this work, it was indicated that the fermi level shift can be concluded from the XPS shift. Hence, such has to be considered again for the IGZO with various Ga/Zn ratio. With results from part 3, the shift in the fermi level (i.e. the work function) of IGZO with various Ga/Zn ratio were estimated. The result is shown in table 4-4. Correlation with the O1s peak shift, the Ga/Zn ratio of 3.9 would be the most likely candidate for the fastest programming characteristics. Figure 4-7 shows that the programming characteristics of the Ga/Zn 3.9 was indeed the fastest. Hence the previous approximation may be validated. The detailed reasoning for such reaction may be from the loss feature peak shown in Ga, but cannot be concluded.

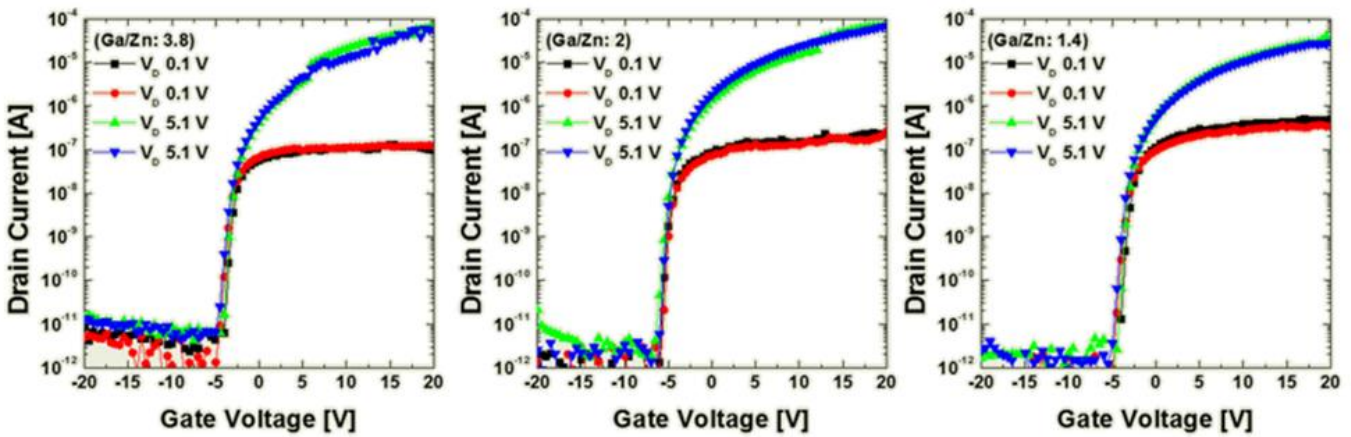



Figure 4-4.Transfer curves of IGZO with different Ga/Zn ratio

TABLE 4-3. Electrical characteristics of IGZO TFTs with different Ga/Zn ratio

| Ga/Zn | $V_{TH}$ [V] | $\mu_{F.E.}$ [$cm^2/Vs$] | $\mu_{sat.}$ [cm2/Vs] | S.S. [V/dec] | $\Delta V_{TH}$ @ $V_G$= 1nA [V] |
|---|---|---|---|---|---|
| 3.9 | -3.0 | 4.04 | 34.36 | 0.24 | 0.35 |
| 2.3 | -3.8 | 4.87 | 30.29 | 0.27 | 0.06 |
| 1.4 | -3.0 | 5.30 | 18.12 | 0.24 | 0.36 |

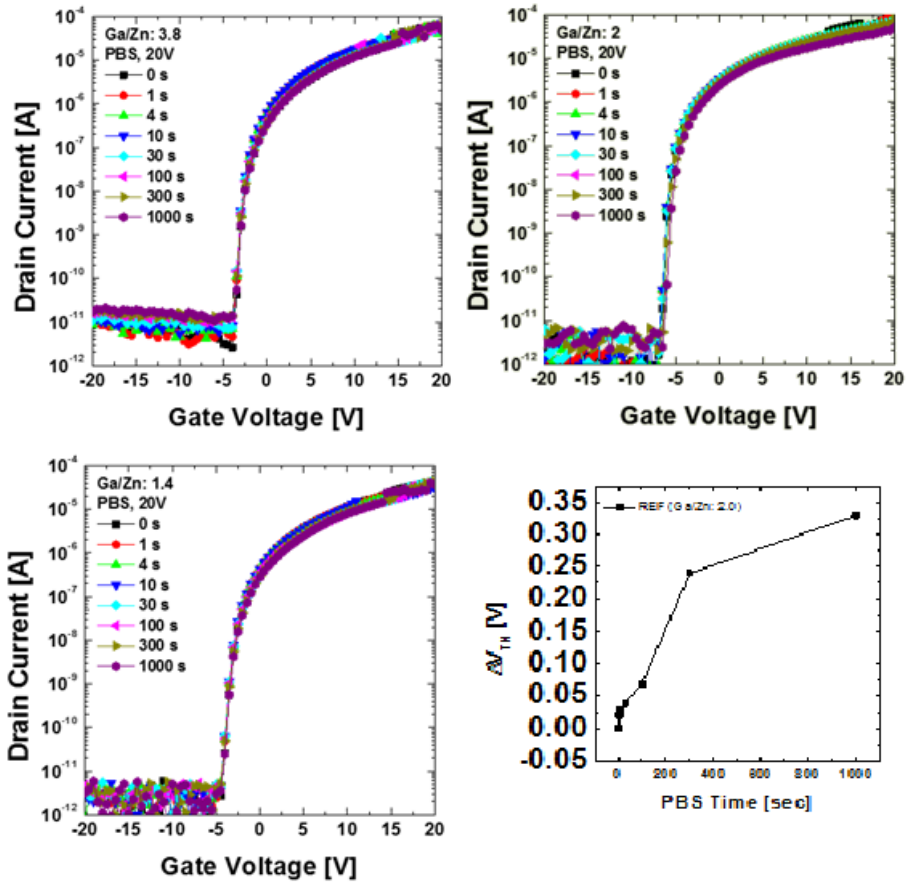



Figure 4-4.1 PBS Results of a-IGZO TFT with various Ga/Zn ratio

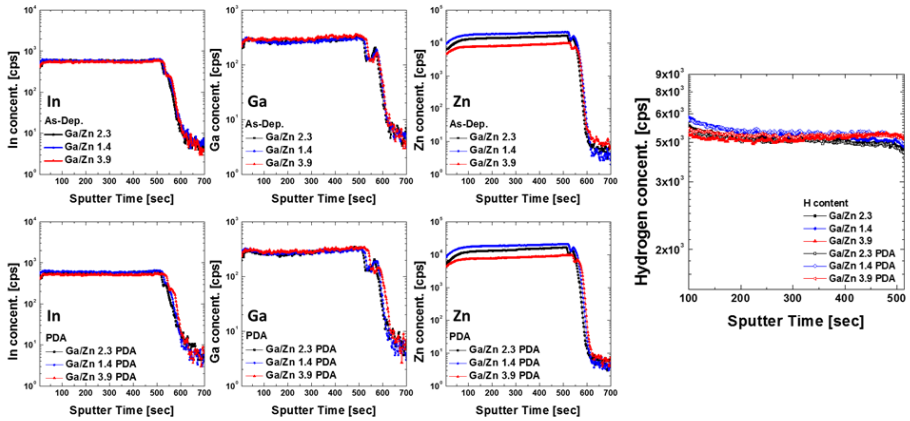



Figure 4-5. ToF-SIMS results of various IGZO with different Ga/Zn ratio at before and after PDA under 350°C.

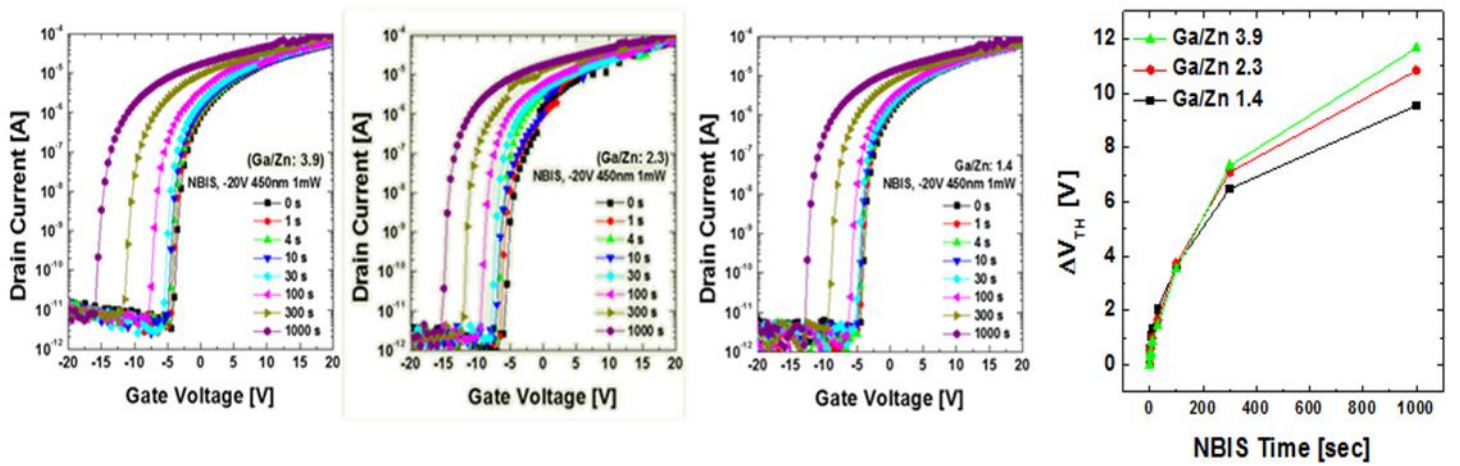



Figure 4.5.1 NBIS results of a-IGZO TFTs with various Ga/Zn ratio

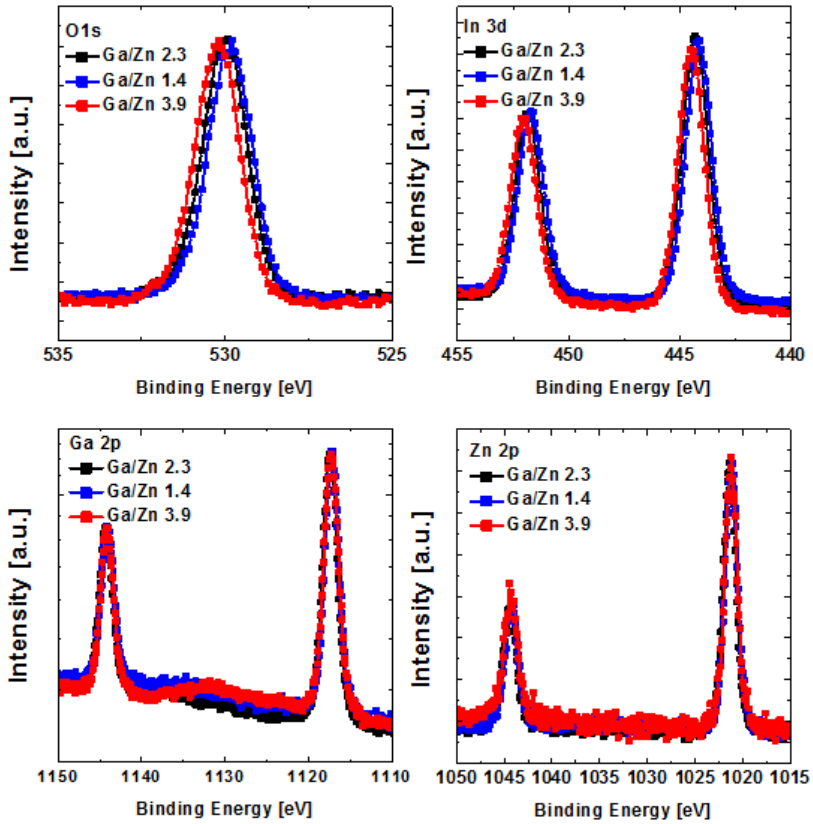



Figure 4-6. XPS analysis of IGZO with various Ga/Zn ratio

**Table 4-4**

| sample | ΔB.E. (O1s) | Δwork function | work function | ΦB |
|---|---|---|---|---|
| Ga/Zn 2.3 | - | - | 3.89 eV (measured) | 2.19eV |
| Sputtered | - 0.76eV | + 0.29 eV (measured) | 4.18 eV (measured) | 2.48eV |
| Ga/Zn 1.4 | - 0.16eV | + 0.06 eV (estimate) | 3.95 eV (estimated) | 2.25eV |
| Ga/Zn 3.9 | + 0.22eV | - 0.09 eV (estimate) | 3.80 eV (estimated) | 2.10eV |

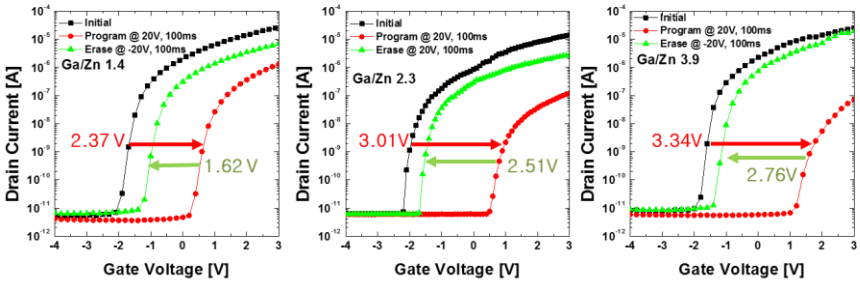



Figure 4-7. PGM char. Of IGZO with var Ga/Zn ratio.

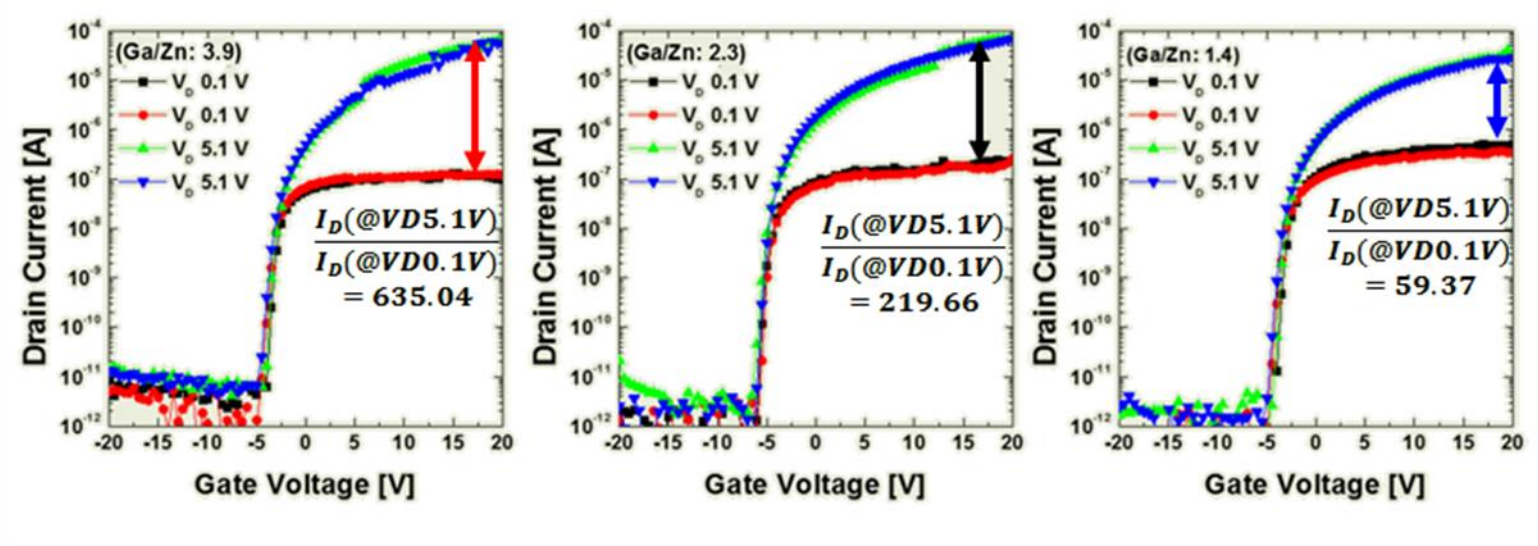



Figure 4.7.1 $I_{DS}$ ratio comparison at different Ga/Zn ratio

$$J_{F.N.} = \frac{A}{4\Phi_B} * E^2 * e^{\frac{-2B\Phi_B^{\frac{3}{2}}}{3E}}, A = \frac{q^2}{2\pi h}, B = \frac{4\pi\sqrt{2m^* q}}{h}$$ (from Hori p.45)

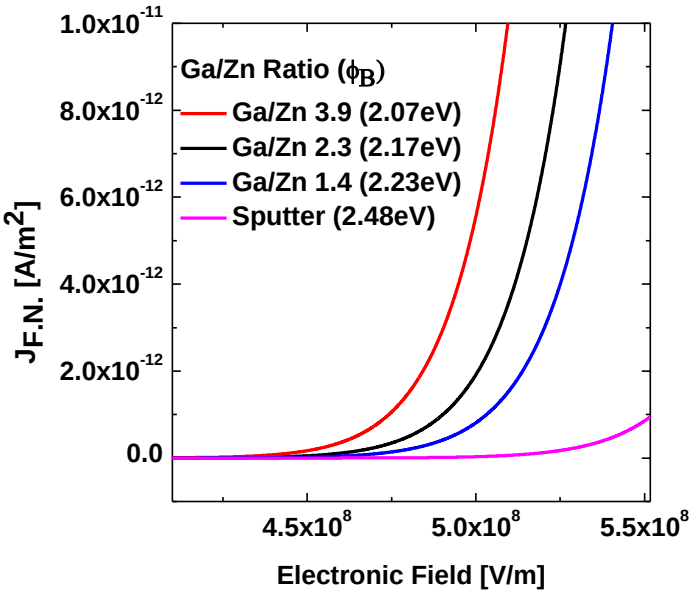
$$D_1 = \in_{r1} \in_o * E_1 = D_2 = D_3$$

$$V_{Applied} = V_1 + V_2 + V_3 = E_{1_{(Al_2O_3)}} * t_{1_{(Al_2O_3)}} + E_{2_{(SiO_2)}} * t_{2_{(SiO_2)}} + E_{3_{(Si_3N_4)}} * t_{3_{(Si_3N_4)}}$$

$$(E = field, t = thickness)$$

$$V_{Applied}(VPGM = 20V) = E_1 * \left( t_1 + \frac{\in_{r1}}{\in_{r2}} t_2 + \frac{\in_{r1}}{\in_{r3}} t_3 \right),$$

$E_1$ (Field on $Al_2O_3$ T.O.) = 4.14 x $10^8$ V/m



## 4.4. Conclusion

The programming characteristics of charge trap flash memory device adopting a-IGZO oxide semiconductors with various Ga/Zn ratio as channel layer were evaluated. Despite the previous reports from other groups, the saturation mobility increased with respect to the increase in relative amount of Ga in the film. ToF-SIMS indicated that only Zn was varied, leaving the similar amount of In and Ga. XPS indicated IGZO with highest relative amount of Ga may have fermi level shift, which will lead to lowering of the potential barrier between channel and the tunneling oxide, which was confirmed by the programming characteristics were fasterst, most heighst binding identical stoichiometry of MOCVD and sputtered a-IGZO, confirmed by the XRF and SIMS profile, faster programming speed of MOCVD a-IGZO was observed. The effect of oxygen vacancy as the cause of the different programming performance can be neglected because the comparable amounts of oxygen vacancies were estimated to be present in both MOCVD and sputtered a-IGZO, using XPS and NIBS analysis. UPS analysis has revealed the higher $E_F$ in the case of the MOCVD IGZO (~0.3 eV) than the sputtered a-IGZO, which could be the cause for such faster programming performance. The incorporation of hydrogen atoms in the MOCVD a-IGZO film appears to constitute the main reason for

the higher carrier concentration which induced, the higher $E_F$ and consequently lower Schottky barrier between the a-IGZO channel and $Al_2O_3$ tunneling oxide layer. The programming threshold voltage shift of ~1.8 V and ~3.0 V could be achieved by applying the 20 V of $V_g$ for 1 ms and 10 ms, respectively, to the MOCVD CTF TFT. The erase voltage (-20 V) application for as short as 1 ms was sufficient to recover more than 70% of the shift $V_{th}$, which allowed the fluent NAND type device application with the standard read voltage of 0 V. Feasible retention and endurance performances were also confirmed. Sputtered a-IGZO film, despite with identical thickness, cation composition, and even higher density, did not permit such high performance due to the higher carrier trapping within the channel or interface with the dielectric layers.

in the saturation region. Despite the highest field effective mobility with minimum Ga amount, questions on highest saturation mobility of Ga still remains to be answers. Secondary ion mass spectroscopy might be give the answer to such phenomenon if non-uniform composition of Ga along depth was found.

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# 5. Conclusion

The programming characteristics of charge trap flash memory device adopting a-IGZO oxide semiconductors as channel layer were evaluated. Despite the identical stoichiometry of MOCVD and sputtered a-IGZO, confirmed by the XRF and SIMS profile, faster programming speed of MOCVD a-IGZO was observed. The effect of oxygen vacancy as the cause for the different programming performance can be overlooked as comparable amounts of oxygen vacancies were found in both MOCVD and sputtered a-IGZO, using XPS and NIBS analysis. UPS analysis has revealed the higher EF in the case of the MOCVD IGZO (~0.5eV) than the sputtered a-IGZO, which could be the cause for such faster programming performance. The reason for the different values of EF from the two films is not clearly understood at this moment. Further research will be performed to test the device performance in a manner comparable to the standard NAND device

MOCVD has shown to be the successful way to vary the stoichiometry of the IGZO. However, resulting crystallinity and electrical measurements did not agree with the previously known characteristics of Ga and Zn in IGZO system. Further analysis is required for these questions to be answered.

# Curriculum Vitae

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## I. Educations

**2005. 9. - 2010. 2.** B.S.

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University of Illinois at Urbana-Champaign

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Seoul National University, Seoul, Korea

## II. Research Areas

**1. Developing Metal Organic Chemical Vapor Deposition process**

- MOCVD process of multi-component films

**2. Thin film deposition for amorphous oxide materials**

- Binary InSnO and ternary InGaZnO process

**3. Mechanism studies on chemical reactions in deposition process**

- Chemical analysis through spectroscopies

**4. Planar Charge trapping memory device fabrication**

- Deposition/etching/lithography/Analyzing electrical propeties

## III. Experimental Skills

**1. Deposition methods**

- DC & RF magnetron sputtering
- MOCVD & ALD
- E-beam evaporation for electrode
- Handling and maintenance of high vacuum equipment

**2. Sample preparation**

- Photo-lithography
- Conventional furnace annealing for ambient and vacuum annealing

- Rapid thermal annealing
- TEM sampling

**3. Analysis methods**

- X-Ray Fluorescence Analyzer (XRF, Thermo scientific, ART Quant'X EDXRF) for analysis of composition and layer density of film
- X-ray Diffractometer (PANalytical, X'Pert PRO MPD) for measurement of X-ray diffraction and X-ray reflection.
- Atomic Force Microscopy (AFM, JEOL, JSPM-5200) for analysis of the topography
- Spectroscopic Ellipsometer (SE, J.A. Woollam, M-2000) for analysis of optical properties and thicknesses of thin films
- Four point probe for resistivity measurement of metals and conducting materials
- Pulse/pattern generator (Tektronix AFG 3110C) and digital oscilloscope
- HP4155B for I-V measurement of oxide semiconductor thin film transistor
- HP XXXX for C-V measurement of oxide semiconductor based capacitor
- Characterizing and analysis of thin films by XPS, UPS, AES, TEM

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11. **Eun Suk Hwang**, Jun Shik Kim, Seok Min Jeon, Seung Jun Lee, Younjin Jang, Deok-Yong Cho and CHeol Seong Hwang “In2Ga2ZnO7 oxide semiconductor based charge trap device for NAND flash memory” *IOP Nanotechnology*, in process

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## Abstract (in Korean)

현재의 정보 기술 산업은 컴퓨터 시스템의 기본 요소인 빠르고, 그 사이즈가 작으며, 전력소모가 작으며, 효율적인 비용을 요하는 메모리 장치를 필요로 한다. 많은 메모리 디바이스 중에서 NAND Flash 메모리 기술은 차세대 스토리지 시스템을 위한 유망한 후보 중 하나이다. 기존의 평면 NAND flash 메모리 기술은 사용 가능한 웨이퍼 영역 당 밀도의 근본적인 한계로 인해 고집적도를 위한 한계에 직면한다. 따라서 Vertical NAND (V-NAND) flash 가 밀도 제한에 대한 해결책으로 대두되고 있다. 현재 산업에서는 세가지 주요 유형의 V-NAND 가 사용되고 있다 (Bic, TCAT and Pipe-BiC). V-NAND의 이러한 주요 아키텍처들은 모두 ONO 채널 및 산화물이 증착되는 "Etch hole"이 필요하다. 웨이퍼 면적에 대한 제한 때문에, Etch hole 사이의 스페이서와 etch-hole 은 "임계 직경 또는 치수" (Critical diameter or dimension)로 제한이 된다. 에치 홀 자체의 경우 각 패킹 밀도는 이 임계 직경에 따라 제한된다. 현재 V-NAND 기술에는 a-Si 또는 poly-Si 채널이 채널 재료로 사용된다. 그러나, 에치 홀 깊이가 길어짐에 따라 셀 밀도가 증가하고 이에 따라 Si 기반 채

널은 낮은 On current 를 겪게 되고, 이는 일정한 디바이스 균일 성을 달성하는데 매우 큰 문제로 직면이 된다. 현재 Si 기술에서는 전류를 늘리기 위해 더 두꺼운 채널의 두께가 필요하지만, 이는 다시 critical dimension 으로 제한이 된다. 따라서, 두께에 상관없이 전기적 특성을 조정 가능한 (tunable) 새로운 채널 재료가 필요하다. 많은 후보군 중, 비정질 산화물 반도체는 매우 유망한 후보자 중 하나이다.

여러 비정질 산화물 반도체 중, 2004년 도코 대학교의 호소노 교수가 처음 제안한 비정질 InGaZnO (a-IGZO)가 가장 유력한 새로운 채널 물질로 거론 된다. 비정질 InGaZnO는 metal cation 의 s-orbital 간의 overlap 으로 인해 비정질 상을 유지 하면서도 Si 기반 채널 물질 보다 매우 높은 이동도를 갖는 다는 이점이 가장 큰 이점으로 인해 주로 디스플레이 장치에 대한 응용으로 집중적으로 연구가 되어 왔다. 현재 a-IGZO를 증착하기 위한 가장 일반적인 스퍼터링 증착 방법은 빠른 증착 속도와 상대적으로 균일 한 박막 품질로 인해 이러한 인기를 이끌었다. 초창기 IGZO는 네거티브 바이어스 하에서 빛에 의해 발생되는 전자-공공 페어 (electron-hole pair)

로 인해 문제가 되어왔다 (NBIS). 550nm 이하의 파장의 광 파장과 음의 바이어스가 유도 될 때, IGZO를 채널로 사용한 트랜지스터의 transfer curve 는 음의 방향으로 이동 하였는데, 이에 대한 가장 대중적인 원인은 산소 결손 의 이온화 (ionization of oxygen vacancy) 라고 수렴되어 왔다. 본 연구실 에서는 NBIS 가 기하g 구조 의존적이라는 것을 보여주고 (NBIS는 채널 길이가 늘어남에 따라 약화됨), 따라서 채널의 사이즈가 작은 경우 그 문제가 해결될 수 있다는 것을 발표하였다. 따라서 이러한 신뢰성 문제는 소자의 치수가 작아짐에 따라 자연적으로 해결 될 수 있다.

디스플레이 응용 분야에 대한 집중적인 연구에도 불구하고 IGZO의 증착법은 스퍼터링에 집중되어 왔다. 스퍼터링의 증착법은 낮은 step-coverage 와 타겟의 사용 시간에 따른 타겟 조성의 변형 등으로 메모리 산업에 적합하지 않은 증착 방법이다. 따라서 본 연구에서는 a-IGZO 박막을 Metal Organic Chemical Vapor Deposition (MOCVD) 으로 증착하고자 한다.

본 논문의 첫 번째 파트에서는 MOCVD 와 스퍼터링 증착방법으로 증착 한 a-IGZO 를 채널로 사용하는 planar flash memory의

program 과 erase 특성을 비교 하였다. 두 종류의 (MOCVD & Sputtered) a-IGZO 박막은 동일한 chemical stoichiometry와 두께, 밀도를 갖지만 그 메모리 특성은 큰 차이를 보였다. 동일한 program 전압과 시간에서 MOCVD a-IGZO의 경우 sputtered a-IGZO보다 약 2.5배 빠른 program 특성을 보였고, 이를 분석 하기 위해 다양한 전기적, 화학적 분석 기법이 사용되었다.

두 번째 파트에서는 MOCVD 로 증착한 a-IGZO 박막의 Ga/Zn 비율에 따른 전기적 특성에 대해 분석 하였다. 이전 연구들에서는 Ga과 O 사이의 강한 결합으로 인해 a-IGZO TFT의 안정된 오프 전류를 허용하는 캐리어 싱크로서 Ga을 설명 하였다. 하지만 본 실험에서는 이와 상반되게 Ga의 함량이 가장 많을 때 가장 높은 이동도를 보였고 이를 접촉저항, 상분리 등으로 설명 하였다.

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**Keywords:** amorphous oxide semiconductor, IGZO, TFT, planar NAND, MOCVD

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