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Ph. D. DISSERTATION

Characterization of Trapping Charges and Contact Properties in Carbon Nanotube Transistors

탄소 나노 튜브 트랜지스터의
트랩핑 전하 및 접촉 저항 특성 연구

BY

HYEONWOO SHIN

FEBRUARY 2018

DEPARTMENT OF ELECTRICAL ENGINEERING AND
COMPUTUER SCIENCE
COLLEGE OF ENGINEERING
SEOUL NATIONAL UNIVERSITY

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이 논문을 공학박사 학위논문으로 제출함

2018 년 2 월

서울대학교 대학원

전기컴퓨터공학부

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Abstract

Characterization of Trapping Charges and Contact Properties in Carbon Nanotube Transistors

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Carbon nanotubes (CNTs) have received tremendous attention due to unique electrical properties because of their one-dimensional (1D) material nature. Owing to extraordinary thermal conductivity, mechanical, and electrical properties, CNTs have been considered as the candidate material for next-generation electronics. Among various applications, CNTs as semiconducting layers in transistors are the most promising, since silicon technology is expected to reach its performance limits soon, and the demand for flexible/transparent electronics is high. Although the unique 1D feature of CNTs is beneficial in terms of flexibility and tuning electrical properties for the required device operation, this 1D feature also yields some issues. (i) transistor operation could largely be influenced by charge diffusion from the CNTs to the surrounding dielectric. This causes the electrical performance of CNT transistors to

be largely influenced by the trapping of charges. (ii) The effective contact area is smaller than the geometrically defined channel to the source/drain (S/D) contact region, since the diameter of a CNT is typically only 1–3 nm. Thus, in this thesis, two important interfaces, the CNT/gate insulator and the CNT/S/D contact, are discussed.

First, the correlation between charge trapping and the charge transport properties in random-network single-walled carbon nanotube (SWCNT) transistors was investigated using direct current (DC) and transient analysis. DC analysis was conducted throughout the temperature-dependent forward (12 V to -12 V) and reverse (- 12 V to 12 V) gate sweep. The activated energy (E_a) extracted from the temperature-dependent mobility showed that the charge transport in our SWCNTs is not governed by the residual ions or the defects in the gate dielectric layer. Further investigation was conducted by extracting the temperature-dependent charge carrier density (n) and trap density (N_t). The charge carrier density (n) and trap density (N_t) showed similar temperature-dependent behavior, which indicates that the charge trapping and hysteric behavior in SWCNT transistors is primarily from the charge injection from the CNTs to the surrounding dielectric. Subsequently, transient measurement was carried out for further investigation. The transient measurement was performed with a small load resistor (R_{load}), such that the measurement circuit was small enough to extract the intrinsic RC time constant (τ) value of the SWCNTs channel. To investigate the effect of charge trapping on the transient response, an empirical equation was developed based on the theoretical trapping model. The transient mobility (μ_{tr}) showed similar temperature-dependent trends with the mobility (μ) extracted from the DC analysis, which further supports that the main factor of charge trapping in SWCNTs is not the residual ions, or the defects in the gate dielectric layer. Throughout the empirical equation, the charge velocity distribution in SWCNTs was successfully explained by the trapping of charges. The correlation between charge carrier density (n) and intrinsic time constant difference ($\Delta\tau$) was also investigated. Throughout this analysis, we confirmed that the transient

response is significantly influenced by charge trapping. We also found that the charge transport in the SWCNTs channel is largely influenced by the shallow traps rather than the deep traps. The trapping and detrapping rates were also extracted from the transient analysis.

Second, the effect of the graphene S/D contact on the electrical performance of the SWCNT transistor was investigated. The contact resistance between SWCNTs and the S/D electrode can be improved by forming a large number of junctions between the SWCNTs and the S/D electrode. Thus, forming a dense SWCNT film is an effective way to increase the junctions between the SWCNT film and the S/D electrode. However, too dense an SWCNT film can cause the CNTs to form bundles and results in the decrease in the on/off current ratio (I_{on}/I_{off}). Thus, a trade-off relationship exists between the contact resistance and the I_{on}/I_{off}. To overcome this trade-off relationship, we employed graphene as the S/D electrode for the SWCNT transistor. The bottom-gate bottom-contact (BGBC) geometry was selected for the graphene S/D contact SWCNTs (Gr-SWCNTs) transistor such that the drain current (I_D) could additionally be modulated by the graphene layer. A palladium (Pd) S/D contact SWCNTs (Pd-SWCNTs) transistor with the same device geometry was also fabricated for comparison. To determine whether graphene formed by chemical vapor deposition (CVD) is suitable for the S/D electrode, our graphene film was characterized thoroughly by the optical microscopic image, atomic forced microscopic (AFM) image, scanning electron microscope (SEM), and the Raman spectra. Throughout the graphene film analysis, we found that our monolayer graphene sheet consists of the combination of large-sized grains (diameter of grain ~100 μm) and small-sized grains (~1 μm). The transmission line method (TLM) results show that the resistivity of graphene was small enough to be used as the S/D

electrode in a single transistor device. The effective work function investigation result indicates that the work function of graphene is well aligned to the work function of Pd. Since the surface energy of the underlying films could influence the deposition of the SWCNTs film, contact angle measurements were performed to acquire the surface energy of each layer. The resulting surface energy was then systematically compared with the AFM image of SWNCTs in the channel. The results showed that the graphene S/D contact is favorable for the SWCNTs to be densely formed in the channel, presumably due to the selective wetting properties that led the SWCNTs to be well confined in the channel. The transfer characteristics of the Gr-SWCNT transistor showed that high mobility (μ) with good I_{on}/I_{off} could be achieved by employing the graphene S/D contact. The conducting behavior and the influence of the contact resistance to the electrical performance of the transistor were further investigated using the stick percolating system and the TLM method. Both Gr-SWCNT and Pd-SWCNT transistors showed the exponent of the stick percolating system near 1 (m = 1). The TLM results showed that the contact resistance of Gr-SWCNTs was lower than that of Pd-SWCNTs.

Keywords: random-network carbon nanotube, transient measurement, empirical equation, graphene, source-drain contact

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Chapter 1

Introduction

Since the first reports on multi-walled carbon nanotubes (MWCNTs) and single-walled carbon nanotubes (SWCNTs) in 1991 and 1993, carbon nanotubes (CNTs) have received tremendous attention, because of the uniqueness in their material and corresponding physical properties. [1–4] The nature of the one-dimensional (1D) geometry that consists of carbon atoms bonded together through the Van der Waals force leads to excellent electronic and mechanical properties with extreme flexibility. Moreover, it takes advantage in terms of electrical tunability for the required device operation because the electrical properties of CNTs can be modified from metallic to semiconducting depending on the chirality and diameter. All of these interesting properties in CNTs have led many researchers to study their fundamental aspects, such that they can be applied in various devices such as the bio-sensor, gas sensor, and flexible/transparent electrodes and transistors (Fig. 1.1) [5–8].

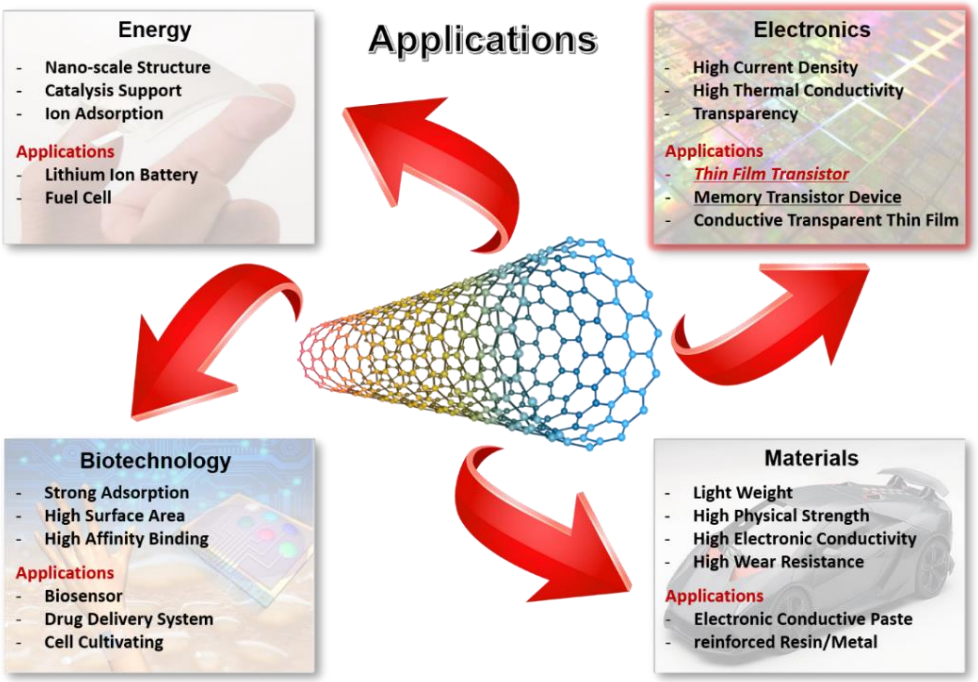

Figure 1.1 Application area of carbon nanotubes.

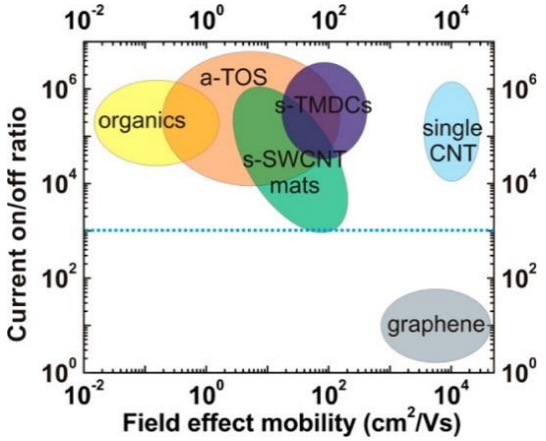

Figure 1.2 Comparison of candidate semiconducting materials in terms of on/off current ratio and mobility [5].

Among those application areas, CNT transistors for circuit applications are the most promising, since the silicon complementary metal-oxide semiconductor (CMOS) technology and poly-silicon transistors are expected to reach their performance limits and the demand for the flexible/transparent or even stretchable electronic devices is high [8–12]. Fig. 1.2 shows the comparison of candidate semiconducting materials in terms of mobility (μ) and on/off current ratio (I_{on}/I_{off}). As in Fig. 1.2, the CNT shows relatively good electrical performance compared with other candidate materials and marks a wide range of spots in the map because of the various material geometries and device structures.

Despite the promising physical properties of the CNT, researchers still fail to meet the requirements for industrialization. Although many studies have been made to understand the fundamentals of charge transport mechanisms of the CNT, it is still unclear and further studies are necessary. The synthesis of high-purity CNT samples and the improvement in device geometry are also necessary. Very recently, G. J. Brady and coworkers reported the current density of CNT transistors that exceeded that of silicon and Ga-As transistors by a combination of CNT purification, solution-based assembly, and CNT treatment [3]. C. Qiu and coworker reported a complementary CNT transistor that shows superior electric characteristics to a silicon transistor (made by Intel's methodology) by employing graphene source/drain (S/D) electrodes [4]. Although these results are from the aligned CNTs, it indicates that CNT transistors can outperform the electrical characteristics of the silicon-based transistor even if the lattice mismatch between the CNT and gate insulator interface could limit the electric performance of the CNT transistors. By expanding this concept to larger-

sized transistors such as thin-film transistors (TFTs) for the display backplane applications, the advantages become more predominant. When the transistor arrays are on a glass or plastic substrate, it is difficult to fabricate a single crystalline silicon transistor on top of these amorphous substrates; thus, amorphous or poly-crystalline silicon transistors are currently commercialized in the industry. The attractive aspect of the CNT transistor is that a single crystalline transistor can be fabricated, or a similar outcome can be expected as long as the CNT strands are connected from the source to drain electrode [3,13]. The random-network CNT transistor is also attractive for TFT applications when the channel length of the device is much longer than the length of the CNT, since this could lead to the large area uniformity.

Whether the CNT is aligned or is in a random network, the CNT is interfaced with the gate insulator and source/drain (S/D) electrode. Thus, two important issues need to be addressed: i) The existence of the void area (where the gate insulator is not covered with CNTs) within the channel could lead to additional diffusion of charges from the CNT to the gate insulator surface [14,15]. This leads to charge trapping from the CNT to the surrounding gate dielectric and influences the charge transport property of the CNT transistors. Thus, understanding the charge trapping effect on the charge transport system in CNT transistors is necessary. ii) The electrical characteristics of the CNT could dramatically change with respect to the S/D contact [16,17]. To reduce the contact resistance between the CNT and S/D electrode, the number of CNT strands to the S/D junction should be large and the highest occupied molecular orbital (HOMO) or the lowest unoccupied molecular orbital (LUMO) level of the CNT should be well matched with the work function of the S/D electrode. Thus,

understanding the effect of charge trapping on the charge transport system and improving the contact properties of the CNT transistor are important for the CNT transistors to be used in industrial areas.

1.1 Charge Trapping Sites in Carbon Nanotube Transistors

The electrical performance of transistors is largely affected by charge trapping in various locations such as the insulator, insulator/semiconductor interface, or within the semiconductor. Fig 1.3 gives an example of various trapped charges in the transistor: the oxide trapped charge (Q_{ot}), fixed oxide charge (Q_f), and mobile ionic charge (Q_m) within the gate insulator. The oxide trapped charge (Q_{ot}) is due to the defects within the gate insulators. This charge can be created from high-energy light irradiation. The fixed charge (Q_f) is located approximately 3–5 nm below the insulator/semiconductor interface [18]. This fixed charge (Q_f) is generally dependent on the oxidation and annealing conditions. The mobile ionic charge (Q_m) is due to the contamination from sodium or other alkali ions. Because the mobile ionic charge (Q_m) is mobile during device operation, special attention needs to be made to eliminate the mobile ions from the devices. The aforementioned trapping charges generally exist in most cases and this can be improved by employing a high-quality gate insulator. The interface trapped charge (Q_{it}) exists in the insulator/semiconductor interface. This trapped charge is generally due to the insulator/semiconductor interface properties and depends on the lattice mismatch or chemical affinity between the insulator and semiconductor [18]. Since a channel forms within a few nanometers above this interface, it is important to improve the interface characteristics in all types of transistors such that the oxygen or water molecule that could act as an additional trapping site does not intrude into the interfaces [19–21]. The surface trapped charge (Q_s) lies between the semiconductor and air (passivation layer). Although the surface trapped charge (Q_s) does not significantly influence the device characteristics when the semiconductor layer is sufficiently thicker than the charge accumulation layer, it

greatly influences the device operation when CNTs and dichalcogenide monolayers (TMDC) are used as a semiconductor layer [14,15,22,23]. A. Vijayaraghavan and coworkers [14] showed the experimental evidence that charge trapping in CNT transistors is largely due to the charges that are injected from the CNT to the surrounding dielectric and not from the ions or mobile charges already present in the gate dielectric. R. S. Park and coworkers [15] discovered a source of traps that are unique in 1D channels such as CNTs and nanowires. They found that charge trapping in the CNT transistors are largely affected by the surface traps (Q_s) rather than the interface traps (Q_{it}).

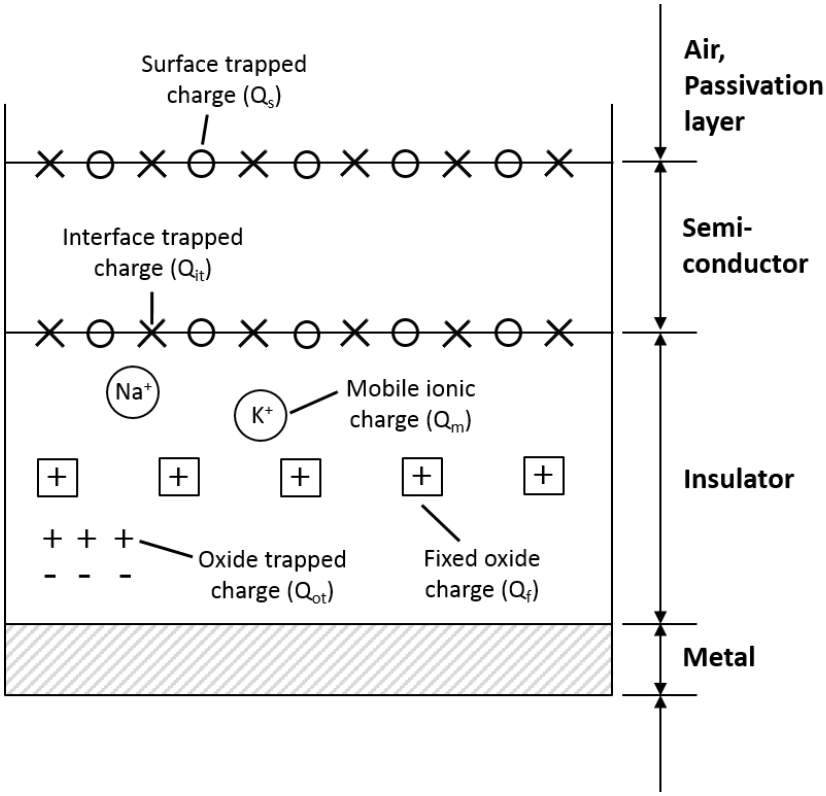

Figure 1.3 Various trapping sites within the transistor.

1.2 Contact Property in Carbon Nanotube Transistors

Since all semiconductor devices have contacts such as metal-semiconductor contact or semiconductor-semiconductor contact, it is important to characterize the contact property to understand the origin of the resulting electrical performance and to improve the electrical performance of the devices. The contact resistance between the semiconductor and S/D electrode is generally due to the dipole moment near the interface (organic/metal interface) or the Schottky barrier (inorganic/metal interface) due to the energy level difference between two materials. A structural disorder near the contact or contaminated surfaces could also lead to defect-assisted transport, which impacts the contact properties [24,25].

In the case of the CNT devices, the contact properties dramatically influence the device performance. Although CNT transistors generally show p-type characteristics, it could also become an n-type transistor when a low work function metal or a chemically doped contact is used [26,27]. In the case of the random-network CNTs, some CNTs are connected to the S/D electrode and some CNTs are not directly in contact with the S/D electrode, which could limit the effective contact area and yield a relatively larger contact resistance [28,29]. Thus, the contact resistance can be reduced by increasing the junctions between the CNTs and S/D electrode by forming a dense SWCNT film. However, too dense an SWCNT film causes the CNTs to form bundles and results in the drain current (I_{DS}) to be less likely modulated by the gate (decrease the I_{on}/I_{off}).

1.3 Outline of Thesis

This thesis consists of five chapters. In **Chapter 1**, a brief history of the CNT and future applications are discussed. Since the CNT has two direct interfaces with other layers (CNT/gate insulator and CNT/S/D electrode), which could influence the device characteristics significantly, the important issues in each interface is discussed accordingly. In **Chapter 2**, the structure and electrical property of the CNT is first discussed. The device fabrication methods and characterization methods are discussed afterwards. **Chapter 3** focuses on the interface between the single-walled CNTs (SWCNTs)/gate insulator where the trapping/detrapping of charges influence the charge transport property of the SWCNT transistor. The trapping/detrapping behaviors were first analyzed throughout the temperature-dependent transfer characteristics. To further analyze the effect of trapping/detrapping on the charge transport property of the SWCNT transistor, transient measurements were performed and the corresponding empirical equation was developed. By using the parameters extracted from the empirical equation that fit to the experimental results, we investigated the effect of trapping/detrapping of charges on the charge transport property of the SWCNT transistor. **Chapter 4** discusses a method of improving device performance by employing the graphene S/D electrode. A chemical vapor deposition (CVD) graphene film was first characterized to determine whether the CVD graphene is suitable to be used as the S/D electrode. Subsequently, the surface energy of the underlying layer (where the SWCNTs will be deposited) and the corresponding SWCNT film characteristics were discussed. The I–V characteristics of the graphene S/D contact SWCNT transistor was systematically compared with the palladium (Pd) S/D contact SWCNT transistor. The applications of the graphene S/D

contact SWCNT transistor in transparent electronics was also briefly discussed. Finally, the summary and concluding remarks of this thesis are highlighted in **Chapter 5**.

Chapter 2

Materials and Methods

2.1 Materials

2.1.1 Structure and Electrical Property of Carbon Nanotubes

The CNT is defined as a cylindrical nanostructure material formed by the sp^2 hybridization of carbon atoms. It is also simply described as a graphene sheet rolled up in a cylindrical form. These unique features of the CNT allow the 1D confinement of electronic charges and results in the van Hove singularities, yielding a unique shape of the density of states (DoS). **[Appendix I]** In the case of the SWCNTs, their electrical characteristic varies from semiconducting to metallic with respect to the diameter and chiral angle (helicity). A simple method to specify each CNT is by adopting the concept of the chiral vector ($\mathbf{C}_h$). A chiral vector ($\mathbf{C}_h$) is a vector along the circumference of the CNTs and is perpendicular to the translation vector (**T**) (tube

axis) as depicted in Fig. 2.1(a). The chiral vector ($\mathbf{C}_h$) is generally described as pair of indices (n, m) (Eq. 2.1).

$$\mathbf{C}_h = n\mathbf{a}_1 + m\mathbf{a}_2 \equiv (n, m) \tag{2.1}$$

Here, $\mathbf{a}_1$ and $\mathbf{a}_2$ each denotes the unit vectors in the hexagonal honeycomb lattice. The (n, m) indices provide almost all the necessary information of the CNTs from their physical shape to their electrical characteristics. Most importantly, the (n, m) indices enable us to distinguish the semiconducting CNTs from the metallic CNTs. |m-n| = 3k + 1 imply semiconducting CNTs and |m-n| = 3k imply metallic CNTs, where k is an integer. When the CNTs are in distinctive (n, m) indices such as zigzag (n, 0) or armchair (n, n) as described in Fig. 2.1(b), the zigzag CNTs are semiconducting whereas the armchair CNTs are metallic. Other than the zigzag (n, 0) or armchair (n, n) CNTs, the other CNTs are all chiral CNTs.

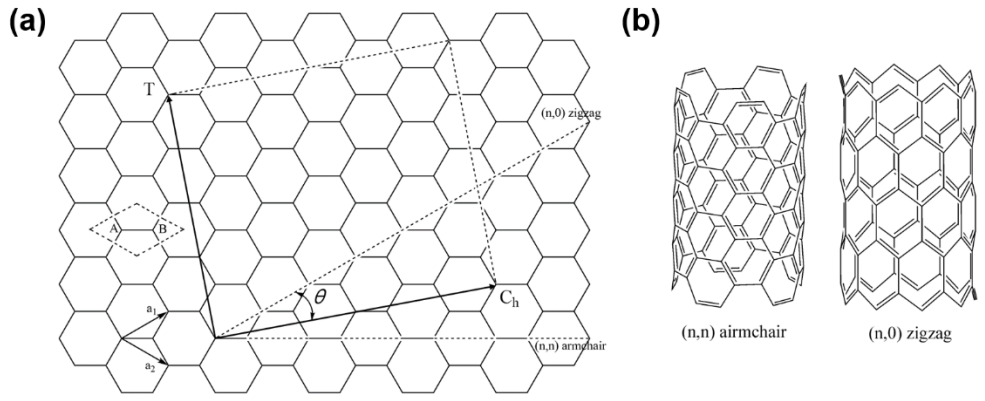

Figure 2.1 (a) Unrolled honeycomb lattice of a CNT, where T is the translation vector and C_h is the chiral vector. a_1 a_2 are the unit vectors, and the dotted rhombus is the unit cell. (b) Two representative CNTs: armchair and zigzag.

The CNTs can be further examined using additional parameters such as the CNT diameter (d_t) and chiral angle (θ). The CNT diameter (d_t) in terms of (n, m) indices can be expressed as in Eq. 2.2.

$$d_t = \frac{C_h}{\pi} = \sqrt{3}a_{cc}(m^2 + mn + n^2)^{1/2}/\pi, \quad (2.2)$$

Where C_h is the length of the chiral vector ($\mathbf{C_h}$) and a_{cc} is the nearest-neighbor carbon-to-carbon distance (1.421 Å). The chiral angle (θ) can be expressed as in Eq. 2.3.

$$\theta = \tan^{-1}\left[\sqrt{3}m/(m + 2n)\right] \quad (2.3)$$

Hence, the diameter (d_t) and chiral angle (θ) of the CNT can be acquired from the (n, m) indices. Since the optical gap of the CNT depends on the CNT diameter (d_t) and chiral angle (θ), the (n, m) indices also enable us to extract the approximate value of the CNT bandgap (E_g). The Kataura plot is one of the representative methods of extracting the bandgap (E_g) of the CNT [30,31]. Fig. 2.2 is an example of an empirical Kataura plot calculated from the fixed value of chiral angle (θ) as in Fig. 2.1 (a). Although Fig. 2.2 only describes the diameter-dependent optical gap with a fixed chiral angle (θ) value as an example, both the diameter (d_t) and chiral angle (θ) are important parameters that determine the optical gap.

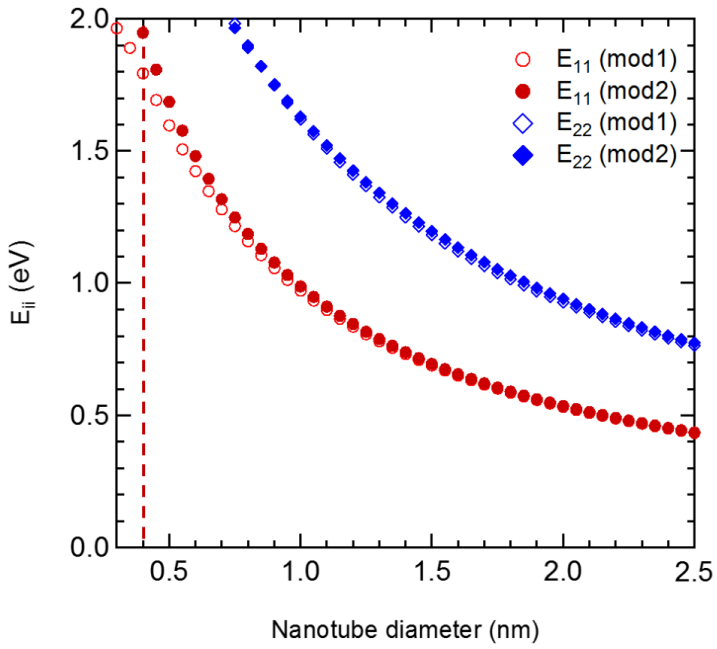

Figure 2.2 Empirical Kataura plot calculated from the fixed value of chiral angle (θ) as in Fig 2.1(a)

2.1.2 Carbon Nanotube Film Deposition

Prior to the SWCNTs deposition, the substrate was dipped in a Poly L-Lysine solution (Sigma Aldrich, 0.1% (w/V) H_2O) for 10 min and gently rinsed with deionized (DI) water to modify the surface of SiO_2, favorable for the SWCNTs deposition. The SWCNTs (Nano Integris, IsoCNTs-S (99%)) solution was drop-casted for some time and gently rinsed with the DI water.

2.1.3 Raman Spectroscopy of Carbon Nanotubes

Raman spectroscopy is an exceedingly powerful tool for CNT characterization. Thus, the Raman spectra characterization method is briefly discussed in this section. The main focus of this section is CNT characterization using Raman spectra rather than the fundamental mechanisms of Raman spectroscopy. Fig. 2.3 shows the Raman spectrum of the SWCNTs (Nano Integris, IsoCNTs-S(99%)) acquired with an Ar-Ion laser (514 nm). Two distinguishable peaks in the G-band is a unique feature of the SWCNT. Each G^+ (1592.5 cm^{-1}) and G^- (1570.3 cm^{-1}) band is associated with the carbon atoms vibrating along the tube axis, and along the circumference of the SWCNT, respectively. The D-band generally originates from structural defects. The structural quality of a carbon-based material can be investigated through the G/D ratio. The Raman spectra in Fig. 2.3 shows that the integration value of the G/D peak is much higher than 100, indicating that the SWCNT film consists of high quality of SWCNTs. The diameter of the SWCNT (d_t) can be extracted from the radial breathing-mode (RBM) frequency (Eq. 2.4) [32,33].

$$\omega_{rbm} = A/d_t + B \tag{2.4}$$

For typical SWCNTs, A = 234 cm^{-1} nm and B = 10 cm^{-1}, whereas A = 248 cm^{-1} nm and B = 0 for the isolated SWCNT on an oxidized silicon substrate. As a result, the diameter of the SWCNT (d_t) was extracted to be 1.5–2 nm. The band gap (E_g) can be estimated from the diameter of the SWCNT (d_t) (Eq. 2.4) [34].

$$E_g = 2 \cdot a_{cc} \cdot \gamma / d_{t,} \tag{2.5}$$

Where a_{cc} is the C-C bond length (~ 0.142 nm), γ is the hopping length (2.5 – 3.2 eV) and d_t is the diameter of the SWCNT. The band gap (E_g) of the SWCNT was extracted to be ~ 0.46 eV.

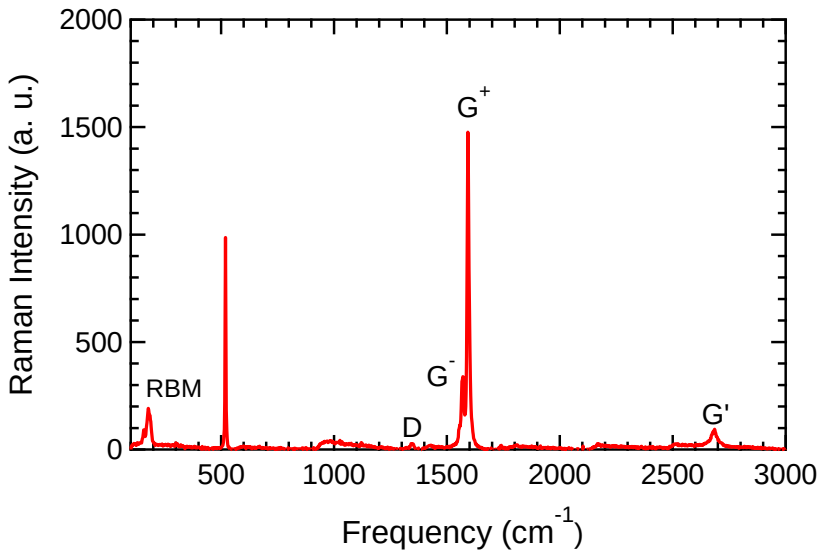

Figure 2.3 Raman spectrum of SWCNTs (Nano Integris, IsoCNTs-S (99%)) on SiO_2.

2.1.4 Synthesis of Graphene and Transfer Process

Graphene was grown by a low-pressure CVD process on a thin Cu foil (25 μm, Alfa Aesar). The Cu foil was ultra-sonicated in 5% nitric acid for 2 min and rinsed with DI water, methanol, and IPA sequentially. Subsequently, the Cu foil was put into a furnace and annealed at 1000 °C for 30 min with 100 sccm flow of H_2 gas. By infusing 100 sccm of CH_4 and 40 sccm of H_2 into the furnace followed by a quenching process, a monolayer graphene was grown. To transfer the graphene to the target substrate, poly(methyl methacrylate) (PMMA, Sigma Aldrich, M_w ~350,000) was first spin coated on the graphene/Cu foil. Cu was etched by immersing the Cu foil in a 114 g/L of ammonium persulfate ($(NH_4)_2S_2O_8$) aqueous solution for 1 hour. Subsequently, the PMMA/graphene film floating on the Cu etchant ($(NH_4)_2S_2O_8$) was washed by DI water for several times. The transfer process was performed by scooping up the PMMA/graphene film to the substrate and dried at 60 °C. The substrate was then put into a jar with 9.7 ml of acetone and sealed with a controlled vent for an hour to construct a fine-quality graphene monolayer, followed by a thorough spreading of the graphene film to the substrate. After the solvent annealing process, PMMA was removed by dipping the substrate into acetone for 30 min followed by methanol and IPA rinsing [35–38].

2.2 Device Fabrication Methods

2.2.1 Carbon Nanotube Transistors for Transient Measurement

The glass substrate was ultra-sonicated with acetone, isopropyl alcohol (IPA), and deionized (DI) water for 10 minutes each and the substrate was dried with N_2 gun, and was the put into an N_2 atmosphere oven at 120 °C subsequently to completely remove the remaining moisture. A palladium (Pd) gate electrode was deposited using electron-beam (E-beam) evaporation. Subsequently, 100 nm of silicon nitride (SiN_x) and 100 nm of silicon (SiO_2) bilayer gate dielectric were formed using plasma-enhanced chemical vapor deposition (PECVD). After the gate dielectric deposition, the Pd S/D electrode was formed using standard photolithography and E-beam evaporation, followed by the lift-off process. The device fabrication was completed after the SWCNT deposition followed by photolithography and the reactive ion etching (RIE) process. The resulting channel length (L) and width (W) of the device was 250 μm and 1200 μm, respectively.

2.2.2 Graphene S/D contact Carbon Nanotube Transistors

ITO/glass was used as the substrate. Here, ITO served as the gate electrode. The bilayer SiN_x (150 nm)/SiO_2 (300 nm) dielectric was deposited throughout the PECVD process. The Pd contact pad (S/D electrode in case of reference samples) deposition was performed using standard photolithography followed by E-beam evaporation and the lift-off process. Subsequently, the graphene S/D electrode was transfer printed on the substrate. The graphene monolayer was patterned using photolithography and O_2 plasma etching. Finally, the SWCNTs were deposited on the substrate and patterned with photolithography followed by O_2 plasma etching. The resulting channel length (L) of the device was between 30 μm to 150 μm (channel width (W) was 600 μm). A schematic of the graphene S/D contact SWCNT transistors fabrication process is shown in Fig. 2.4.

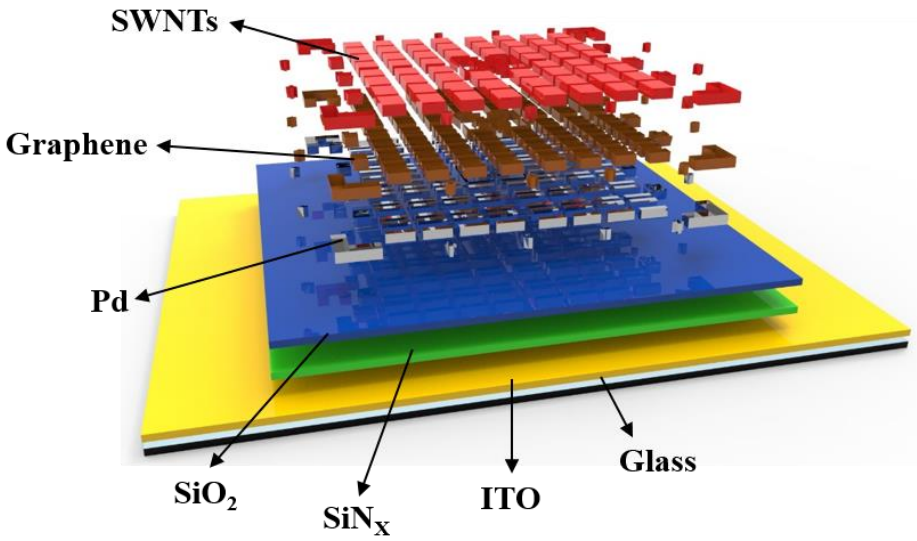

Figure 2.4 Schematic of graphene S/D contact SWCNT transistor fabrication process.

2.3 Device Characterization Methods

2.3.1 Measurement Setup for Carbon Nanotube Transistors

The Agilent 4155C parameter analyzer was used to measure the DC characteristics of the SWCNT transistor as shown in Fig. 2.5 (a). The transient response of the SWCNT transistor was measured as depicted in Fig. 2.5 (b). The gate electrode was grounded, and the drain electrode was connected to the variable resistor (R_{Load}). A step impulse of 12 V was applied to the source electrode using the Tektronix AFG 3101 arbitrary function generator. The period of the pulse cycle was 3 m·sec and the duty cycle was 3%. The Tektronix TDS5054B oscilloscope was connected to each source and drain electrode to detect the transient response signal. The temperature-dependent measurement was performed in a vacuum atmosphere (under 10^{-3} torr) chamber and the temperature was controlled with liquid nitrogen (N_2).

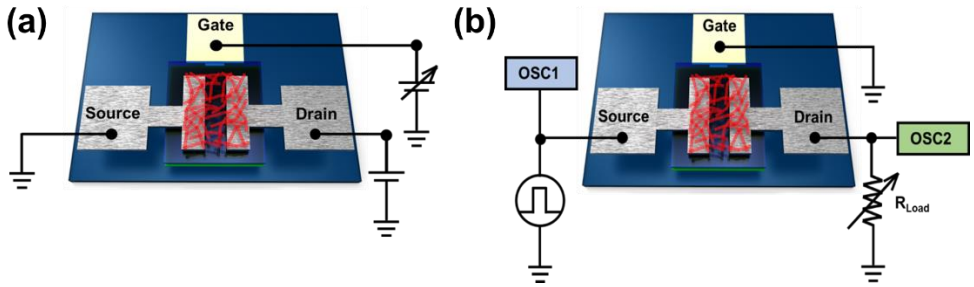

Figure 2.5 Measurement setup for the SWCNT transistor in (a) DC and (b) transient analysis.

2.3.2 Direct Current (DC) Sweep Characterization

When the external bias is applied to the gate electrode (V_G) and the drain-source voltage (V_{DS}) is swept from 0 to a certain voltage, we can plot the drain-source current (I_{DS}) as a function of V_{DS} (output curve). When V_{DS} = 0, the electric potential difference between the drain and source electrode is 0, thus current (I_{DS}) cannot flow between these two electrodes and it is in the off state. When V_{GS}-V_T $\geq$ V_{DS}, I_{DS} is linearly dependent on V_{DS}. In this case, the transistor is operating in the linear region and I_{DS} can be expressed as in Eq. 2.6.

$$I_{DS} = \frac{W}{L} \cdot C_{ox} \cdot \mu_{lin} \cdot \left(V_{GS} - V_T - \frac{V_{DS}}{2}\right) \cdot V_{DS}, \quad (2.6)$$

Where W and L are the channel width and length of the device, C_{ox} is the gate oxide capacitance, and μ is the mobility of the device. Other than mobility, all other parameters are dimensionality factors or corresponding voltages that need to be applied in order to operate the device. Thus, mobility is an important factor that indicates the electrical performance of the transistor. When V_{GS}-V_T $\leq$ V_{DS}, the transistor is in the saturation region and I_{DS} is expressed as in Eq. 2.7.

$$I_{DS} = \frac{W}{2L} \cdot C_{ox} \cdot \mu_{sat} \cdot (V_{GS} - V_T)^2 \quad (2.7)$$

Eq. 2.7 shows that when a transistor is operating in the saturation region, I_{DS} is no longer a function of V_{DS} and it is proportional to the $\sqrt{V_{GS}}$. Assuming that the parallel plate model is valid, the field effect mobility in the linear region can be extracted from the slope of I_{DS} ($g_m = \partial I_{DS} / \partial V_{GS}$) and the mobility in the saturation region can be extracted from the slope of $\sqrt{I_{DS}}$.

2.3.3 Transient Response Characterization

When the transistors are in their circuit application, they generally operate under a pulse or sinusoidal input and would output the corresponding transient response. Thus, understanding the transient response of the transistor is as important as understanding the DC operation characteristics. To understand transient response characteristics, we first need to approximate the carrier density distribution p(x,t) at the channel (Eq. 2.8) [39].

$$p(x,t) \approx p_0\left[1-\frac{x}{\alpha t^{\gamma}}\right] \tag{2.8}$$

Where p_0 is the time-invariant carrier density, x is the distance, t is time, α is a pre-factor, and γ is a power factor that represents a distance extrapolated from the linear part of the carrier density to where the density is 0. Substituting Eq. 2.8 into the drift-diffusion equation yields Eq. 2.9 [39].

$$\frac{\gamma h x}{\alpha t^{\gamma+1}} \approx -\frac{\partial}{\partial x}[\mu E_x(x)]p(x,t) + \mu E_x(x)\frac{h}{\alpha t^{\gamma}} \tag{2.9}$$

Since most of the charge carriers are primarily distributed in the gate oxide/semiconductor interface, the current component vertical to the interface is neglected. Let $\bar{x}$ be the peak position of the electric field. Then $\partial_x E_x(x) = 0$. Therefore, the first term in the right-hand side vanishes at $\bar{x}$. Assuming that the electric field along the channel is linearly dependent on the applied external voltage, then $E_x(x) \approx V/x$. If we solve Eq. 2.9 for mobility, we can acquire Eq. 2.10.

$$\mu \approx \frac{\gamma}{|V|}\frac{L^2}{t} \tag{2.10}$$

Because the signal can only be detected at the source or drain electrode, $\bar{x}$ becomes the channel length (L) of the device (the detailed derivation of Eq. 2.10 is in **[Appendix 2 (i)]**). The fastest charge exits the drain while the channel is still forming. Thus, an additional pre-factor γ should be added in the equation, and was previously determined from the experimental and simulation results from other groups ($\gamma \sim 0.3 - 0.5$) [39–41]. It is noteworthy that unlike the mobility, which can be extracted from the DC curve, the transient mobility (μ_{tr}) is independent of the gate capacitance (Eq. 2.10). This is because transient mobility (μ_{tr}) is a parameter that is extracted from the transient time (t_{tr}), which is the time it takes for the fastest charge carriers to arrive at the counter electrode. Although t_{tr} is independent value to the gate capacitance, the capacitance of the devices significantly influences the overall transient response shape. This will be further discussed in detail in Chapter 3. Note that we minimized overlapping area of the gate to S/D electrode (A_{SD}) using standard photolithography (gate and S/D overlap length was less than 3 μm). Since the sharp rising time and falling time was necessary for the accurate transient analysis, only effective way of reducing the displacement current was reducing A_{SD} **[Appendix 2 (ii)]**.

2.3.4 Transmission Line Method

Since the contact resistance is an important factor that determines the device characteristics, various contact resistance (R_c) extraction methods had been proposed, such as the transmission line method (TLM), four-probe measurement, Kelvin probe microscopy, and the Y-function method [42–45]. Among these methods, the transmission line method (TLM) is the most straightforward and reliable method to extract the contact resistance (R_c) or channel resistance (R_{ch}) of the devices. Because the electrical performance is sensitive to R_c when the charges are starting to be injected from the external voltage, R_c is generally extracted from the linear region of the output curve near $V_{DS} = 0$. The total resistance (R_{tot}) of the device is the sum of R_c and R_{ch} as described in Eq 2.11.

$$R_{tot} = \frac{L}{WC_{ox}\mu(V_G - V_T)} + R_c \quad (2.11)$$

By plotting R_{tot} as a function of channel length (L), R_{ch} can be extracted from the slope of the curve and R_c can be extracted from the y-intercept. Because this method is valid when the transistors are operating in the linear region, the voltage drop between the drain to source affects the I–V characteristics. Thus, R_c becomes the sum of the contact resistances of the drain and source electrodes ($R_c = R_d + R_s$). When the transistor is in the saturation region, the drain current (I_D) is no longer a function of the drain voltage (V_D), but is only a function of the gate-to-source voltage (V_{GS}). Thus, the voltage drop between the gate and source is only valid in this case and the contact resistance in the source electrode becomes the overall contact resistance ($R_c = R_s$) [46].

The TLM method can also be used to investigate the contact properties between the conductive material/metal contacts. Since the conductive material does not require an additional voltage source from the third electrode, such as the gate electrode in a transistor (applying a certain voltage to the gate is necessary to form a channel such that the current can flow from the source to drain electrode), the equation simplifies to $R_{tot} = R_{sh} \cdot L/W + R_c$ [47]. Here, the current is only a function of the electric field between two counter electrodes, thus R_c is the summation of the two contacts ($R_c = R_d + R_s$).

2.3.5 Other Characterization Methods

Atomic forced microscopy (AFM) : Non-contact mode AFM (XE-100, Park system) measurement was used to inspect the surface morphology of the random-network CNT films.

Ultraviolet photoelectron spectroscopy (UPS) : Au was used as a reference sample to calibrate the Micro-XPS (Kraos, AXIS-NOVA) device. He I (21.2 eV) photon source was used to acquire the work function of the metal and graphene.

UV-visible absorption measurement : Transmittance spectra was obtained using a UV-Vis absorption spectrometer (CARY5000, Agilent).

Contact angle measurement : Contact angle was measured by drop-casting 1 μL of de-ionized (DI) water and diiodomethane (DIM) on the target substrate.

Appendix 1

The volume in the k-space per state (V) can be described as $(2\pi/L)^n$, where n is a dimensionality factor. In 1D materials such as CNTs or nanowires, n = 1 (n = 2 for two-dimensional (2D) materials such as transition metal dichalcogenide monolayers (TMDC), and n = 3 for a typical three-dimensional (3D) material such as silicon). The volume in the k-space occupied by states with energies less than E(V_k) is k ($V_k = k$) in 1D materials ($V_k = \pi k^2$ in 2D, $V_k = 4\pi/3 \cdot k^3$ in 3D), where $k = \sqrt{2m(E - E_c)}/\hbar$. The number of electron states (N(E)) can be described as $N(E) = 2 \cdot V_k/V$, where the pre-factor 2 indicates an electron that spins up and spins down. The DoS (g(E)) can now be acquired from the following equation, $g(E) = 1/L^n \cdot \partial N(E)/\partial E$ [48]. Fig. A.1 shows the DoS of each 1D, 2D, and 3D material.

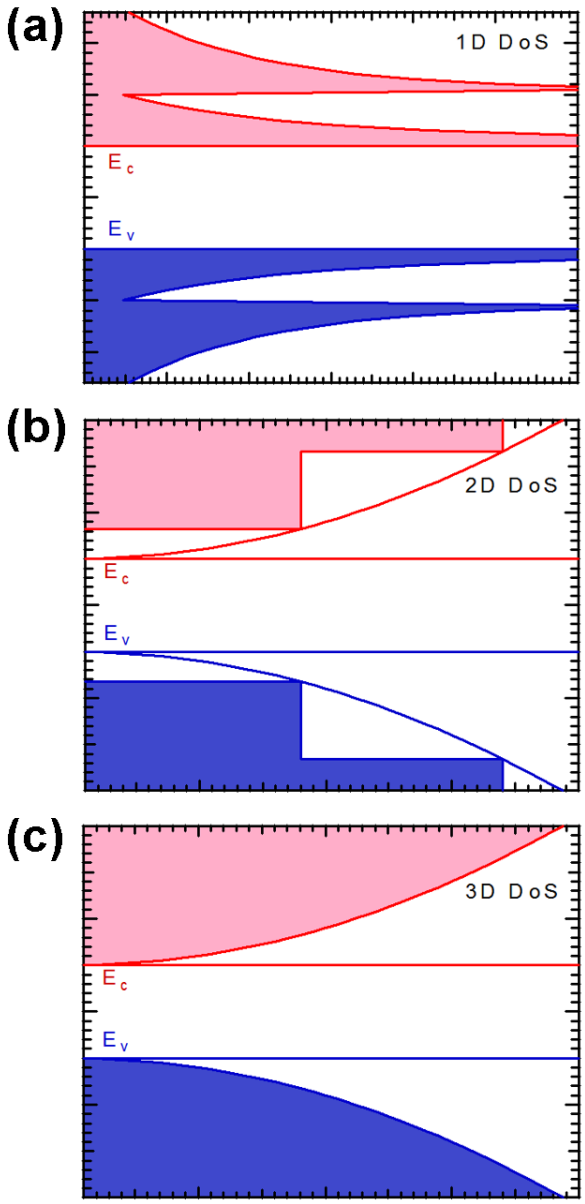

Figure A.1 Density of state in (a) 1- (b) 2- (c) 3-dimensional materials.

Appendix 2

i) Transient Mobility Derivation [39]

Charge carrier density in the channel : $p(x,t) \approx p_0\left[1-\frac{x}{\alpha t^{\gamma}}\right]$

Drift-diffusion equation : $J(t) = q \cdot p(x,t) \cdot \mu \cdot E_x(x) - q \cdot D\frac{dp(x,t)}{dx}$

(The first term in the right-hand side is drift current component; the second term is the diffusion current component)

Continuity equation : $\frac{\partial p(x,t)}{\partial t} = -\frac{1}{q}\nabla J$

Drift-diffusion & continuity equation :

$$\frac{\partial P(x,t)}{\partial t} = -\frac{\partial}{\partial x}[p(x,t)\mu E_x(x)] + D\frac{\partial^2}{\partial x^2}p(x,t)$$

(Substituting charge carrier density term in the drift-diffusion & continuity equation)

$$\frac{\partial p}{\partial t} = \frac{\gamma h x}{\alpha t^{(\gamma+1)}}$$

$$\frac{\partial p}{\partial x} = -\frac{h}{\alpha t^{\gamma}}\ ,\ \frac{\partial^2 p}{\partial x^2} = 0$$

$$\frac{\partial}{\partial x}[p(x,t)\cdot\mu\cdot E_x(x)] = -\frac{h}{\alpha t^{\gamma}}\cdot\mu\cdot E_x(x) + \frac{\partial}{\partial x}[\mu\cdot E_x(x)]\cdot p(x,t)$$

$$\frac{\gamma h x}{\alpha t^{(\gamma+1)}} = \frac{\partial}{\partial x}[\mu E_x(x)]p(x,t) + \mu\cdot E_x(x)\cdot\frac{h}{\alpha t^{\gamma}}$$

Assume that $\frac{\partial}{\partial x}E_x(x) = 0, E_x(x) = \frac{V}{x},\ x \leq \alpha t^{\gamma}$, and x is substituted by L.

Thus, $\mu \approx \frac{\gamma}{|V|}\frac{L^2}{t}$.

ii) Displacement Current Derivation [40]

Displacement of charge q along the transistor:

$\delta q_D = -\frac{q}{\pi(L-x)}\delta x$; where L is the channel length, x is the distance of the mobile electron charge in the channel

Using $\gamma = \frac{1}{2}$ for simplicity, α and υ becomes

$$\alpha = [2\mu V]^{1/2} \text{ , velocity } \upsilon = [\frac{\mu V}{2t}]^{1/2}$$

$$L = \int_0^{t_{tr}} v\ dt = \int_0^{t_{tr}} \left[\frac{\mu V}{2t}\right]^{\frac{1}{2}} dt = \left[\sqrt{\frac{\mu V}{2}} \cdot 2t^{\frac{1}{2}}\right]_0^{t_{tr}} = \sqrt{2 \cdot \mu \cdot V} \cdot \sqrt{t_{tr}} = \alpha\sqrt{t_{tr}}$$

$$\rightarrow \alpha = \frac{L}{\sqrt{t_{tr}}}$$

$$q_D = \int_0^L p(x,t)\ dx = p_0\left[-\frac{1}{2}\frac{\sqrt{t_{tr}}}{\sqrt{t}}\frac{x^2}{L}\right]_0^L = p_0 \cdot L \cdot \left[1 - \frac{1}{2}\sqrt{\frac{t_{tr}}{t}}\right]$$

$$I_D = \frac{\partial q_D}{\partial t} \cdot A_{SD} = \frac{\partial q_D}{\partial x} \cdot \frac{\partial x}{\partial t} \cdot A_{SD} = \frac{-q}{\pi(L-x)} \cdot \frac{L}{2\sqrt{t \cdot t_{tr}}} \cdot A_{SD}$$

$$= \frac{-p_0 \cdot L^2}{2\sqrt{t \cdot t_{tr}}} \cdot \frac{A_{SD}}{\pi(L-x)} \cdot \left[1 - \frac{1}{2}\sqrt{\frac{t_{tr}}{t}}\right] = \frac{-p_0 L}{2\sqrt{t \cdot t_{tr}}} \cdot \frac{A_{SD}}{\pi\left[1 - \sqrt{\frac{t}{t_{tr}}}\right]} \cdot \left[1 - \frac{1}{2}\sqrt{\frac{t_{tr}}{t}}\right]$$

Chapter 3

Effects of Trapping/detrapping Charge Carriers in SWCNT transistors

For decades, the SWCNTs that exhibit excellent electronic properties have encouraged researchers to study their charge transport mechanisms such that they can be applied in the industry [49–52]. Although high on-state current density and highly uniform transistors were achieved very recently [3,12], the relatively large hysteresis in SWCNT transistors is still a limitation factor that hampers the replacement of the silicon technology [53–55]. Despite the importance of understanding the effects of charge trapping on the charge transport system in SWCNT transistors, only a few have studied the sources of trapping and how it is related to the charge transport properties of the SWCNT transistor [14,15,22,56]. As depicted in Fig. 3.1, the trapping of charge not only influences the hysteresis, but it could also influence the

electric field from the gate to the semiconductor. Thus, understanding the effect of trapping to the electrical performance of the CNT transistor is important to reduce hysteresis and to improve device performance. Vijayaraghavan and co-workers [14] found that hysteresis occurs from charges that are injected from the SWCNTs to the surrounding dielectrics, and the hysteresis depends on the charge carrier density of the CNTs. Recent work from Park and co-workers found that the surface traps in SWCNTs play a crucial role to the charge trapping in the SWCNT transistor [15]. These studies and previous other studies mainly focused on the origin of charge trapping in the SWCNT transistors [14,15,56]. However, it is also important to understand the correlation between the charge trapping and the charge transport properties in the SWCNT transistor for the deeper understanding [22]. Since the transistors generally operate under a square pulse input when the transistors are in their circuit application, understanding the trapping effect to the transient response is also necessary. Therefore, we investigated the effect of charge trapping/detrapping on the electrical performance of the SWCNT transistor using the DC and transient analysis. Since charge trapping in the SWCNT transistor mostly occurs on the surface or the interface between the gate insulator and CNTs, a transient analysis was performed by applying a step impulse signal to the source electrodes such that the charge carriers can be directly injected into the CNTs to the surrounding dielectrics. For a deeper understanding of charge trapping/detrapping and charge transport properties in SWCNTs, an empirical equation was developed and systematically analyzed to understand how the trapping/detrapping of charges influences the charge transport properties of SWCNT transistors.

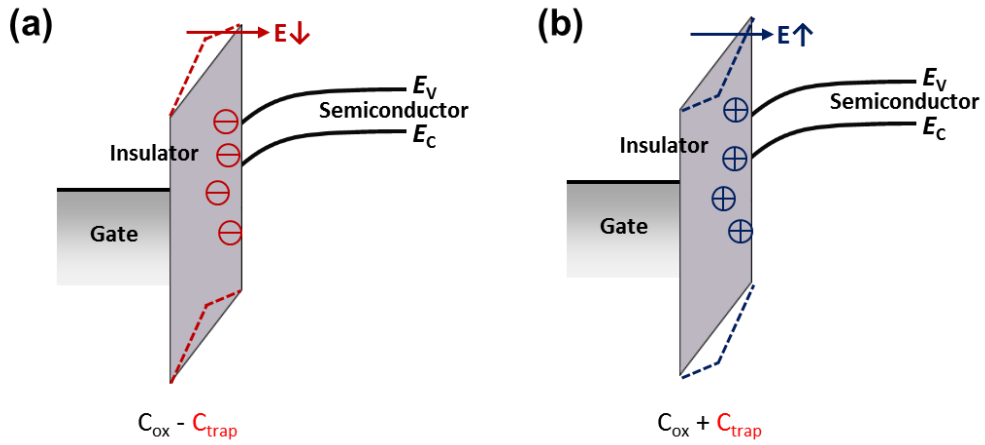

Figure 3.1 Influence of (a) negative (b) positive trapped charges on the electric field from the gate to semiconductor.

3.1 I-V Characteristics of SWCNT Transistors

3.1.1 SWCNT Film Characterization

As in the AFM image of the random-network SWCNTs in Fig. 3.2, the length of the SWCNT (~ 1 – 1.5 μm) was much shorter than that of the channel length (250 μm) of the device. Thus, we optimized the density of the SWCNTs to form a large number of inter-tube junctions without significant bundling. As a result, a well-interdigitated SWCNT film was acquired, indicating that the random-network SWCNT film can successfully transport charges from the source to the drain electrode.

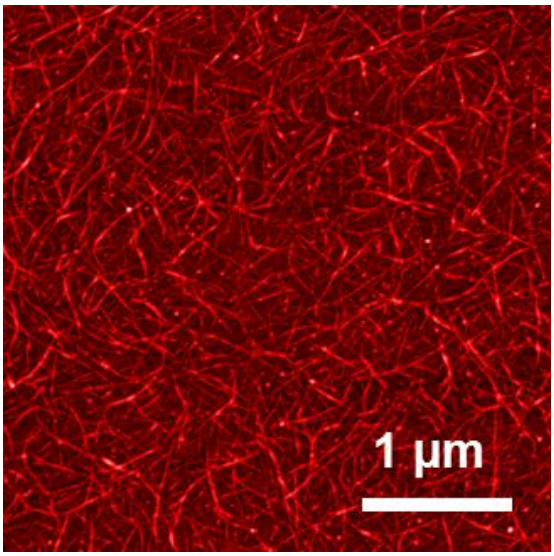

Figure 3.2 AFM image of random-network SWCNTs on SiO_2.

3.1.2 Analytical Equation

Since the SWCNT film does not fully cover the gate dielectric and electrostatic coupling could occur between the gate and the SWCNTs, an effective gate capacitance was acquired using an analytical equation (Eq. 3.1) [9,57,58].

$$C_G = \left\{ C_Q^{-1} + \frac{1}{2\pi\varepsilon_0\varepsilon_r} \ln\left[\frac{\Lambda_0}{R} \frac{\sinh\left(\frac{2\pi t_{ox}}{\Lambda_0}\right)}{\pi} \right] \right\}^{-1} \Lambda_0^{-1}, \quad (3.1)$$

Where the quantum capacitance (C_Q^{-1}) value of the SWCNTs was taken from the previous results ($C_Q = 4$ pF/cm). The $\varepsilon_0 = 8.854 \times 10^{-14}$ F/cm, the relative dielectric constant (ε_r) of the bilayer gate dielectric was extracted to be 7.79 (Fig. 3.3(a)), and the effective thickness of the gate dielectric was 200 nm. The radius of the CNTs was extracted from the Raman spectrum in Fig. 2.3. Λ_0^{-1} is the density of the SWCNTs (/μm) and this value was taken from the average value of more than 10 different line profile in the AFM image. Fig. 3.3(b) is the example of a line profile extracted using an image processing tool (Image J). Fig. 3.3(c) shows the effective gate capacitance value extracted from the analytical equation. As the density of the SWCNTs increased, the effective gate capacitance becomes saturated. This result is in accordance with previous results from other groups [9,57]. Since the SWCNTs are densely formed in our case, the capacitance value extracted from the analytical equation was slightly smaller than that from the parallel-plate model (34.1 nF/cm^2 to 29.5 nF/cm^2).

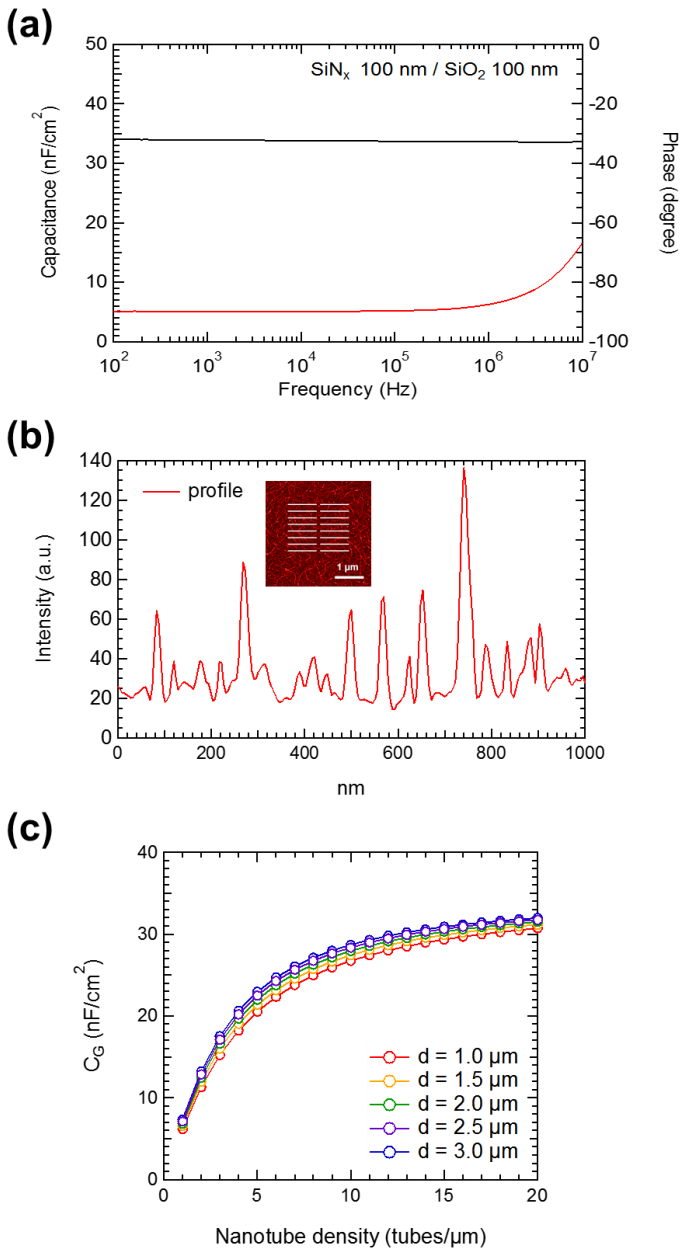

Figure 3.3 (a) Capacitance of gate insulator (SiN_x/SiO_2) as a function of frequency. (b) Example of SWCNT film profile for SWCNT density extraction. (c) Effective capacitance as a function of SWCNT density.

3.1.3 Charge Transport and Trapping Analysis in SWCNT Transistors

Fig. 3.4(a) shows the temperature-dependent transfer characteristics of the SWCNT transistor. The gate voltage was swept forward and backward while a constant voltage of - 12 V was applied to the drain electrodes. As depicted in Fig. 3.4(a), the on current (I_{on}) and off current (I_{off}) increase as the temperature increases. This implies that the thermally-assisted transport dictates the charge transport in our devices. The field effect mobility (μ) was extracted using $\mu = g_m L \times (C_i W V_D)^{-1}$, where, g_m is the trans-conductance, V_D is the applied drain voltage and C_i is the gate capacitance. The extracted mobility was Arrhenius plotted using the parallel-plate model and the analytical equation (Fig. 3.4(b)). Assuming the thermally activated transport,$\mu \sim \mu_0 \exp(-E_a/kT)$ [59–61] is valid, the activation energy (E_a) in the high-temperature range was extracted to be 8.20 – 9.21 meV, which is an order of magnitude lower than the E_a of mobile ions (80 – 320 meV) [62], the defect sites in insulators (250 – 500 meV) [63]. It is noteworthy that the measurements were performed under a vacuum atmosphere (under 10^{-3} torr), where the residual water molecules are continually expelled from the chamber. This result indicates that the charge transport in our SWCNT transistor is not dictated by the mobile ions, or the defect sites in the insulator. The activation energy (E_a) is a parameter that is strongly related with the trapping/detrapping of charges. Thus, the field-dependent activation energy (E_a) and trap density of state (DoS) were further investigated from the temperature-dependent conductance (σ), where $\sigma(V_g) \sim \sigma_0 \exp(-E_a/kT)$ [64,65]. Fig 3.5(c) shows the activation energy (E_a) as a function of V_{GS}. We observed a decrease in activation energy (E_a) as the gate voltage is increased toward the negative value, which indicates that the Fermi level moves towards the band-edge as the

applied gate voltage was increased. Since the change in the gate voltage leads to a shift in the activation energy (E_a), the density of trap states in the bandgap of the SWCNTs were calculated using Eq. 3.2 [65–67].

$$N(E) = \frac{C_i}{q \cdot d}\left[\frac{\partial E_a}{\partial V_G}\right]^{-1}, \tag{3.2}$$

Where C_i is the capacitance of the dielectric, and d is the effective accumulation-layer thickness. Note that the Eq. 3.2 is valid under the assumption that the charge density is constant up to the effective accumulation-layer thickness [65]. Fig. 3.5(d) shows the density of trap states in the band-gap of SWCNTs. As shown in Fig. 3.5(d), we found that a large number of traps are located at a few meV above the valence band of the SWCNTs. This result further supports that the activation energy (E_a) of the SWCNT transistor is smaller than that of the general thermally activated charge transport transistors and that the trapping and detrapping of charges dominantly occur at the valance band above ~ 8.20 – 9.21 meV.

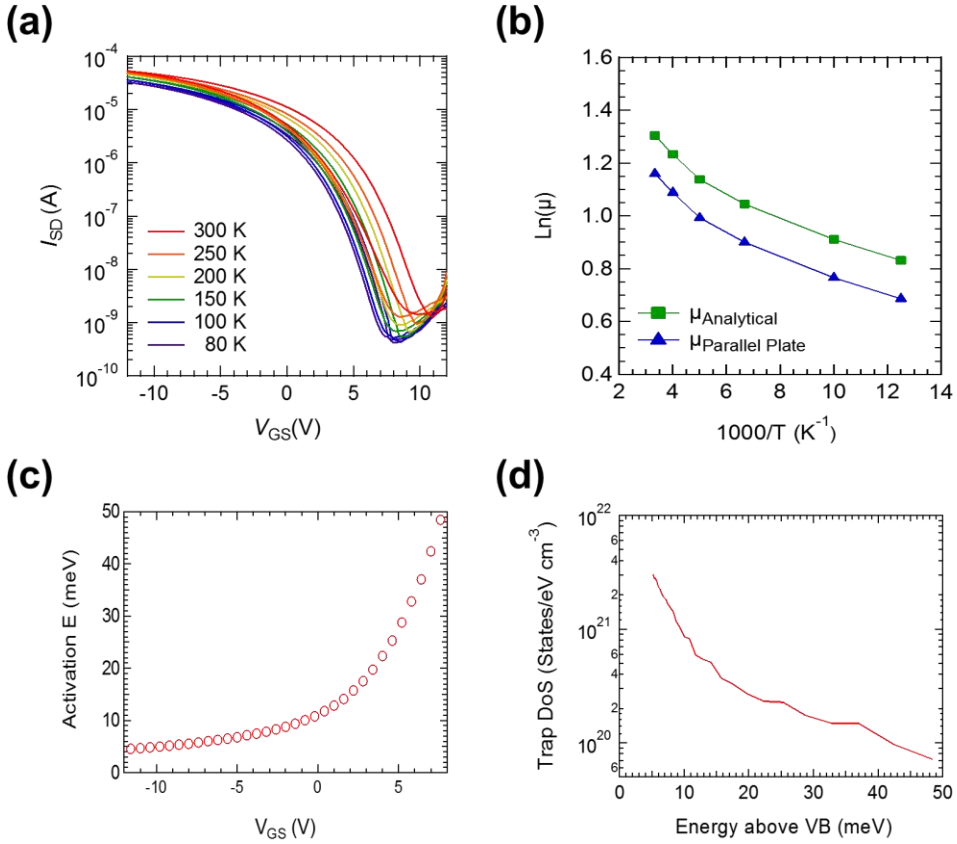

Figure 3.4 (a) Temperature-dependent transfer characteristics of the SWCNT transistor. (b) Arrhenius plot of mobility extracted from the parallel-plate model and analytical equation. (c) Activation energy (E_a) as a function of V_{GS}. (d) Density of trap states in the band-gap of SWCNTs.

To further investigate the trapping mechanism in the SWCNT transistors, we extracted the charge carrier density (n) and trap density (N_t) as a function of temperature. Assuming that the drift-diffusion equation is valid in our transistor, the charge carrier density (n) was extracted from $n = G/(q \cdot \mu)$, where G is the channel conductance, q is the elementary charge, and μ is the mobility. The trap density (N_t) was extracted from $N_t = (C_i \Delta V)/q$ [68,69], where ΔV is the device's hysteresis. As in Fig. 3.5(a), the trap density (N_t) increased as the charge carrier density (n) increased with respect to temperature. This similar temperature-dependent trend between charge carrier density (n) and trap density (N_t) becomes more clear by plotting the ratio of the charge carrier density (n) to the trap density (N_t) as a function of temperature (Fig. 3.5(b)). The ratio of the charge carrier density (n) to the trap density (N_t) was invariant in entire temperature range, which is a strong evidence that the charge trapping in the SWCNT transistor occurs from the charge injection from the SWCNTs to the surrounding dielectric. This result is consistent with previous studies that showed that the charge carriers' density (n) is closely related to the trapping/detrapping of charges in SWCNT transistors [14,22].

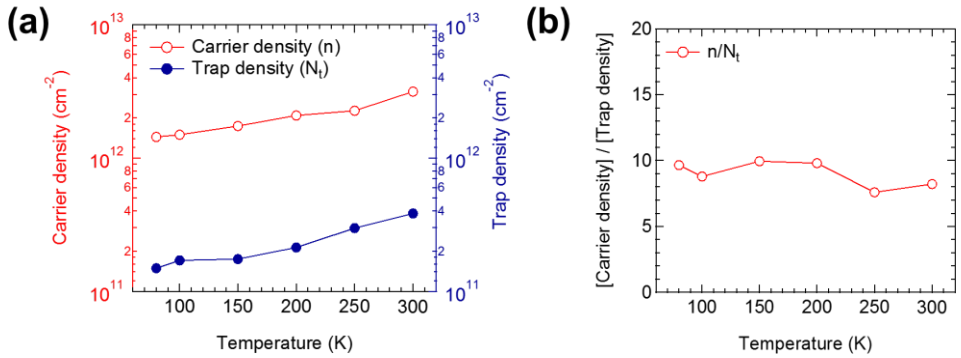

Figure 3.5 (a) Charge carrier density (n) and trap density (N_t) with temperature. (b) The ratio of charge carrier density (n) to trap density (N_t) with temperature.

3.2 Transient Response of SWCNT Transistors

3.2.1 Intrinsic RC in SWCNT Transistors

Fig. 3.6(a) shows the equivalent circuit for the transient measurement. Since the charge carriers in the SWCNTs can be trapped in the surrounding dielectric and this could affect the RC network of the transistor channel, the C_{trap} term was added in the equivalent circuit. As in Fig. 3.6(b), because the t_{tr} is the time it takes for the fastest charge carriers generated from the source electrode to drift to the drain electrode, the transient time (t_{tr}) is independent of R_{Load} [41]. However, R_{Load} could influence the RC time constant (τ) value, which is related to the overall transient response signal that reaches the quasi-equilibrium state. Thus, we plotted the normalized transient response as a function of different R_{Load} values to find the optimum value that does not distort the intrinsic transient response signal. We found no significant changes in the transient response shape when the value of R_{Load} is less than 1 KΩ, indicating that our measurement circuit is small enough to observe the intrinsic transient response in the SWCNT transistor.

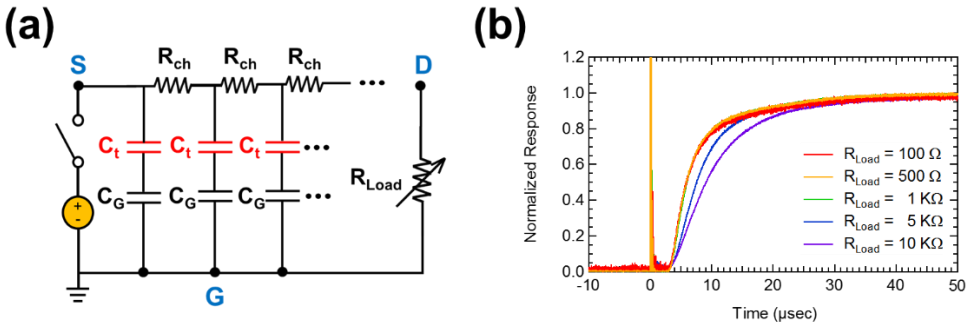

Figure 3.6 (a) Equivalent circuit model of transient measurement scheme. (b) Normalized transient response as a function of R_{load}.

3.2.2 Trapping/detrapping Model

Recently, Juska *et al.*[41] developed a numerical equation to explain the transient response of organic transistors. Their experimentally obtained transient response characteristics were in good agreement with their proposed equation. However, their equation did not consider the effects of charge trapping/detrapping, which is an important, factor especially in materials such as organic semiconductors or random-network CNTs, where trap-assisted transport primarily occurs in the grain boundary or inter-tube junctions [70–72]. Dost *et al.* [73] showed the effect of traps on the transient response by comparing the discrepancy in transient time (t_{tr}) extracted from the time when the step impulse is applied and removed. This method provides insight into the charge trapping effect on the transient response but only gives limited information. Thus, a more accurate analysis method is necessary to understand the relationship between transient response and the trapping/detrapping mechanism. Based on previous results that argue that trapping/detrapping influences the transient response [40,73,74] and that charge trapping/detrapping is closely related to the presence of charge carriers in the SWCNTs [14,22], we used the trapping model proposed by Chen *et al* [75]

$$n(t) = \frac{\gamma_1 N_1}{\gamma_1+\kappa_1}[1-\exp\{-(\gamma_1+\kappa_1)t\}] + \frac{\gamma_2 N_2}{\gamma_2+\kappa_2}[1-\exp\{-(\gamma_2+\kappa_2)t\}] \quad (3.3)$$

$$n(t) = n_{10}\cdot\exp[-\kappa_1 t] + n_{20}\cdot\exp[-\kappa_2 t] \quad (3.4)$$

Eq. 3.3 and Eq. 3.4 denote the density of total trapped charges when the electric field is applied (trapping) and removed (detrapping), respectively. n_{10} and n_{20} are the initial conditions of the shallow-trapped charges and deep-trapped charges, respectively. $N_{1,2}$ is the total number of traps, $\kappa_{1,2}$ is the thermal detrapping rate

constant, and the subscripts 1 and 2 each denotes the shallow traps and deep traps, respectively. The thermal trapping rate is described as $\gamma_{1,2} = J_0\sigma_{1,2}/q \cdot \exp(E/E_0)$, where J_0 is the current density when the initial electric field E_0 is applied. σ is the trapping cross section, E is the electric field, and q is the charge amount. To simplify the equation, the charging and discharging from the shallow traps to deep traps or from the deep traps to shallow traps were not considered. The empirical equation was derived by substituting boundary conditions into the previously proposed equation. (i) Before the step impulse signal is applied to the source electrode, we assumed that the trapping sites at the semiconductor/insulator interface or the trapping sites within the semiconductor layer is void. Thus, we assumed that the total trapped charges are 0 ($n(0) = 0$) for convenience. (ii) Immediately after the fastest charge carriers have arrived ($t = t_{tr}$), relatively slow charge carriers also start to arrive at the drain electrode. Because the transistor channel can be considered as an RC network, the transient response is an exponential function and this is the stage where the charge carriers fill the remaining trapping sites in the channel. (iii) When the step impulse is applied for a certain time, the response signal reaches a quasi-equilibrium state and the charge carriers can now freely drift to the drain electrode without significant interference from the trapping sites. Since we normalized the transient response signal, the total trapped charges (n) in the quasi-equilibrium state equals to 1. Thus, the sum of the pre-factors in Eq. 3.3 and Eq. 3.4 becomes 1 ($\frac{\gamma_1 N_1}{\gamma_1+\kappa_1} + \frac{\gamma_2 N_2}{\gamma_1+\kappa_2} = 1$, $n_{10} + n_{20} = 1$). Note that our SWCNT transistor operates in the depletion mode, thus some amount of the charge could already present in the channel

even if the step impulse is not applied to the source electrode. Strictly speaking, the trap charge difference between the two boundary conditions is Δn.

From these boundary conditions and the drift-diffusion equation combined with the continuity equation that give the transient time (t_{tr}) term in the equation, the resulting empirical equation for the transient response is as shown in Eq. 3.5 and 3.6:

$$n(t) = 1 - A \cdot \exp\left[\frac{-(t-t_{tr})}{\tau_1}\right] - (1 - A) \cdot \exp\left[\frac{-(t-t_{tr})}{\tau_2}\right] \quad (3.5)$$

$$n(t) = B \cdot \exp\left[\frac{-(t-t_{tr\prime})}{\tau_{1\prime}}\right] - (1 - A) \cdot \exp\left[\frac{-(t-t_{tr\prime})}{\tau_{2\prime}}\right] \quad (3.6)$$

It is noteworthy that the second term disappears if A or B equals to 1, which indicates that only the shallow trap is effective in transient response. Fig. 3.9 shows the temperature-dependent transient response and the empirical equation fitting result when the time pulse is applied and removed. As in Fig.3.7, the empirical equation fits well to the experimental results with an average error deviation of less than 1.15%. This indicates that the transient response in the SWCNT transistor is a superimposed value of two exponential function terms, which is related to the shallow traps and deep traps. The extracted parameters are summarized in Table 3.1 (a) and (b). The RC time constant ($\tau_{1,2}$) values extracted from the time when the step impulse was applied were smaller than the time constant ($\tau_{1,2}$) value extracted when the step impulse was removed, which is in accordance with Eq. 3.3 and 3.4, where the time constant value ($\tau_{1,2}$) is smaller at the time the electric field was applied than when it was removed.

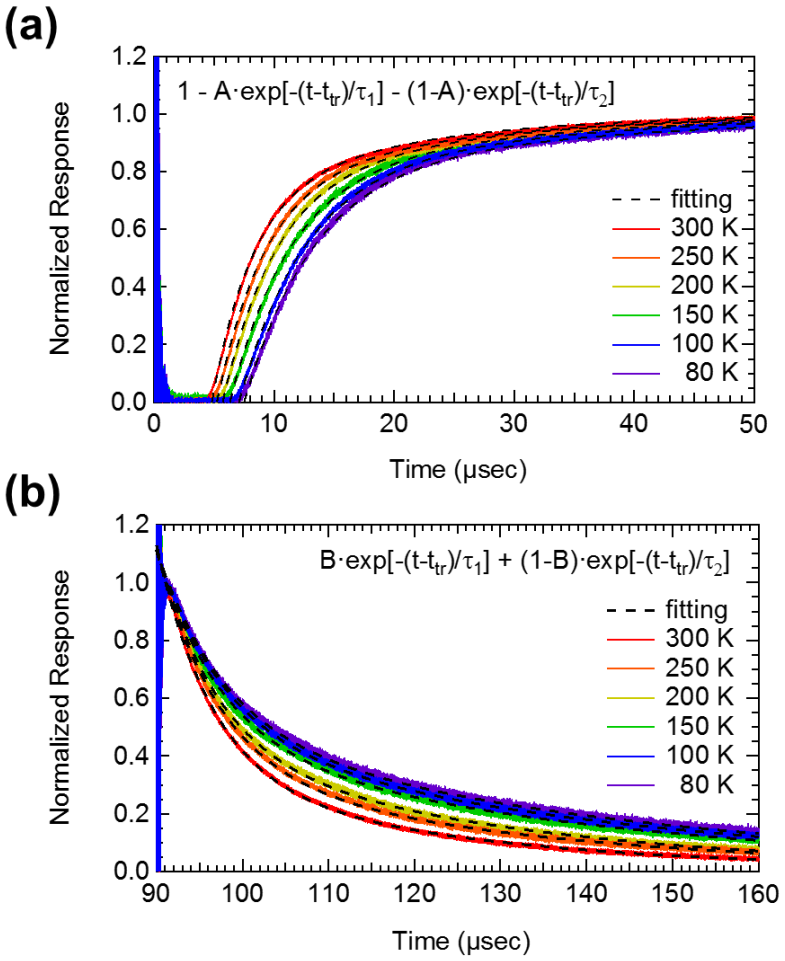

Figure 3.7 Temperature-dependent transient response and the empirical equation fitting result when pulse is (a) applied and (b) removed.

Table 3.1 (a) Extracted parameters from transient response when pulse is applied.

Temp. (K)	t_{tr}	τ_1 $(Shallow\ traps)$	τ_2 $(deep\ traps)$	A
300 K	4.81×10^{-6}	3.34×10^{-6}	1.47×10^{-5}	0.69
250 K	5.26×10^{-6}	3.91×10^{-6}	1.69×10^{-5}	0.73
200 K	5.71×10^{-6}	4.30×10^{-6}	1.72×10^{-5}	0.72
150 K	6.31×10^{-6}	4.89×10^{-6}	1.96×10^{-5}	0.74
100 K	7.08×10^{-6}	5.25×10^{-6}	2.09×10^{-5}	0.74
80 K	7.50×10^{-6}	5.72×10^{-6}	2.65×10^{-5}	0.78

Table 3.1 (b) Extracted parameters from transient response when pulse is removed.

Temp. (K)	$t_{tr'}$	$\tau_{1'}$ $(Shallow\ traps)$	$\tau_{2'}$ $(deep\ traps)$	B
300 K	1.04×10^{-6}	6.46×10^{-6}	3.32×10^{-5}	0.67
250 K	1.06×10^{-6}	7.12×10^{-6}	4.04×10^{-5}	0.65
200 K	1.17×10^{-6}	6.81×10^{-6}	3.87×10^{-5}	0.58
150 K	1.19×10^{-6}	7.35×10^{-6}	4.83×10^{-5}	0.55
100 K	1.29×10^{-6}	7.69×10^{-6}	5.07×10^{-5}	0.53
80 K	1.35×10^{-6}	7.69×10^{-6}	5.21×10^{-5}	0.51

3.2.3 Temperature-dependent Transient Mobility

The transient mobility (μ_{tr}) was extracted by substituting transient time (t_{tr}) in Table 3.1(a) to Eq. 2.10. The mobility extracted from the transient response and the DC characteristics are Arrhenius plotted in Fig. 3.8. The mobility extracted from the transient response and the transfer curve showed similar temperature-dependent characteristics. Comparing the transient mobility (μ_{tr}) with the mobility extracted from the transfer curve, the transient mobility (μ_{tr}) showed a relatively large mobility with a larger temperature-dependent behavior. This is presumably due to the fact that μ_{tr} is the mobility extracted from the fastest charge carrier that arrives at the drain electrode. The activation energy (E_a) extracted from the temperature-dependent transient mobility (μ_{tr}) was 6.9 – 18.1 meV, which is also an order of magnitude lower than the activation energy (E_a) of the mobile ions, or the defect sites in the insulator.[62,63].

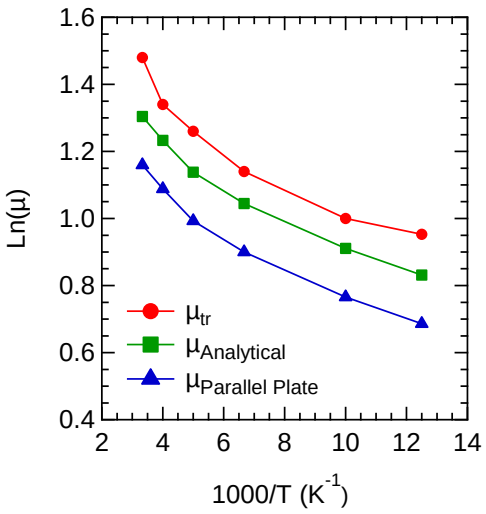

Figure 3.8 Arrhenius plot of extracted mobility from transient response and transfer curve.

3.2.4 Temperature-dependent Charge Velocity Distribution

A strong advantage of acquiring the intrinsic RC time constant value of the transistor channel is that it enables the charge velocity distribution to be extracted, which provides an insight into the charge carrier propagation through the channel. Fig. 3.9 shows the temperature-dependent normalized velocity distribution plotted by differentiating the transient response as a function of time. Our velocity distribution coincides well with the previously reported velocity distributions and the image of the electric field distribution from the time-resolved microscopic optical second-harmonic generation (TRM-SHG) technique [39,74,76]. The velocity distributions of the charge carriers were widely distributed in the $10^3 - 10^4$ cm/sec range, where the fast charge carriers are influenced by the shallow traps (first term in Eq. 3.5, pink-colored area in Fig. 3.9) and the relatively slow charge carriers are influenced by the deep traps (second term in Eq. 3.5, blue-colored area in Fig. 3.9). No significant changes in the velocity distribution shape with respect to temperature, indicates that our SWCNT transistor's charge transport system is similar in all temperature ranges.

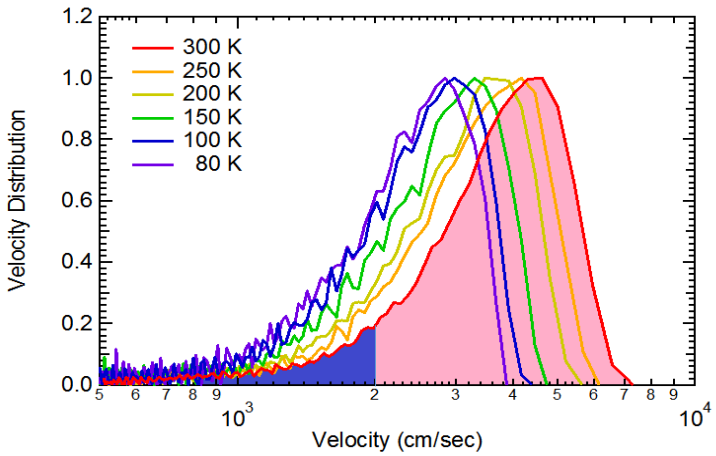

Figure 3.9 Temperature-dependent velocity distribution of SWCNT transistor.

3.2.5 Charge Trapping/detrapping Analysis

As the relationship between charge carrier density (n) and charge trapping/detrapping was investigated from the transfer characteristics, it was also investigated in the same manner from the transient response signal. Leveraging the empirical equation developed based on the trapping/detrapping of charge carriers, we further investigated the relationship between charge carrier density (n) and $\Delta\tau$ ($\Delta\tau_{1,2} = \tau_{1',2'} - \tau_{1,2}$). Since R_{Load} is small enough to allow the intrinsic transient response to be observed, the response signal in the quasi-equilibrium state should be proportional to the channel conductance (G) (Fig. 3.10 (a)). Thus, the ratio of the transient response in the quasi-equilibrium state to the transient mobility (μ_{tr}) should be proportional to the charge carrier density (n) [14,22]. $\Delta\tau$ was deduced from the extracted parameters summarized in Table 3.1(a), (b). For comparison, the ratios of conductance (G), mobility (μ), and hysteresis (ΔV) extracted from the transfer characteristics were also plotted in Fig. 3.10(b). As in Fig. 3.10(b), both $G/(\mu\Delta V)$ and $G/(\mu\Delta\tau_1)$ show a strikingly similar temperature-independent trend. However, $G/(\mu\Delta\tau_2)$ deviates from this trend, indicating that the deep traps are less likely influenced by the carrier density (n) of the SWCNTs. Thus, the charge carrier density (n) of SWCNTs largely influences the trapping and the detrapping of charges in shallow traps rather than the deep traps. This result is also consistent with the velocity distribution result, where the integral domain of velocity distribution influenced by the shallow traps (pink-colored area in Fig. 3.9) is much larger than that from the deep traps (blue-colored area in Fig. 3.9).

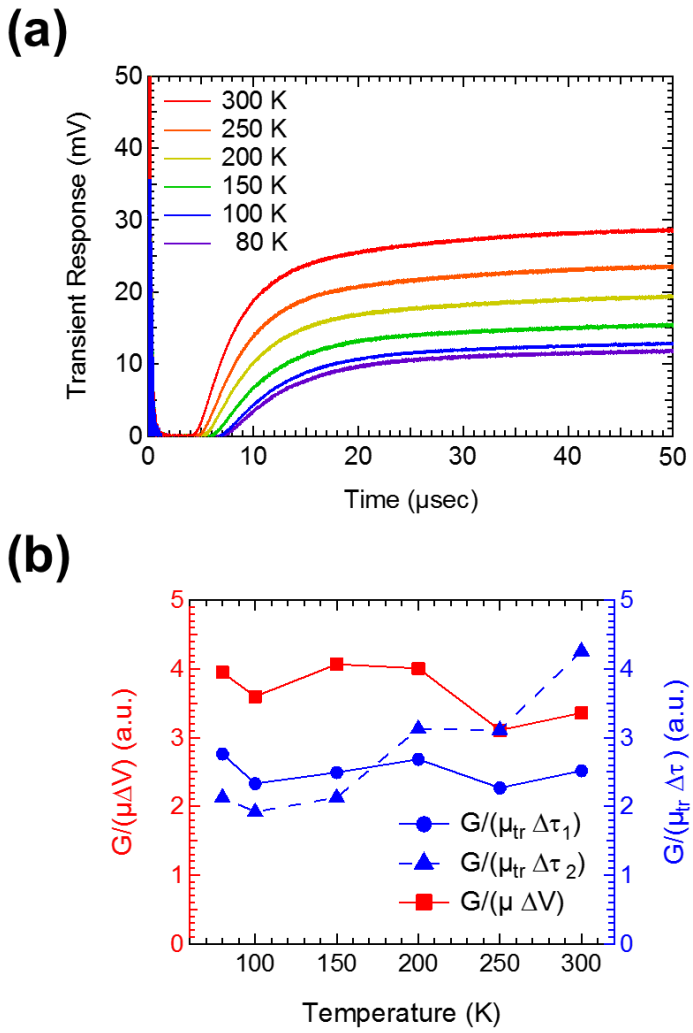

Figure 3.10 (a) Transient response of SWCNT transistor before normalization. (b) Variation in the ratio of conductance (G), mobility (u) and time constant (Δτ) in SWCNT transistor with temperature.

Finally, the trapping and detrapping rates were investigated. The rapping and detrapping rates of the shallow and deep traps with respect to temperature are plotted in Fig. 3.11. The trapping and detrapping rates were deduced by substituting the extracted parameters in Table 3.1(a), (b) to Eq. 3.3 and 3.4 (the extracted parameters are summarized in Table 3.2). The trapping and detrapping rates extracted from Table 3.2 are the average values of 5 different samples, to account for reliability. Since the time constant (τ) value does not change regardless of whether the transient response signal is normalized, the extracted value from the empirical equation gives the quantitative values of the trapping and detrapping rates. Fig. 3.11 shows that the trapping and detrapping rates of shallow traps are larger than those of deep traps. This is because the energy barrier in a shallow trap is smaller than the one in a deep trap [75,77]. Since the trapping and detrapping rates of the shallow trap is larger than those of the deep trap, the trapping and detrapping of shallow traps contribute more to the overall charge transport in the SWCNTs than the trapping and detrapping of deep traps. The trapping rate of the shallow traps showed a stronger temperature-dependent behavior than the trapping rate of the deep traps. From these results, we conclude that the increase in charge carrier density (n) and the proportional increase in hysteresis (ΔV) are due to the large increase in the shallow trap (κ_1). trapping rate.

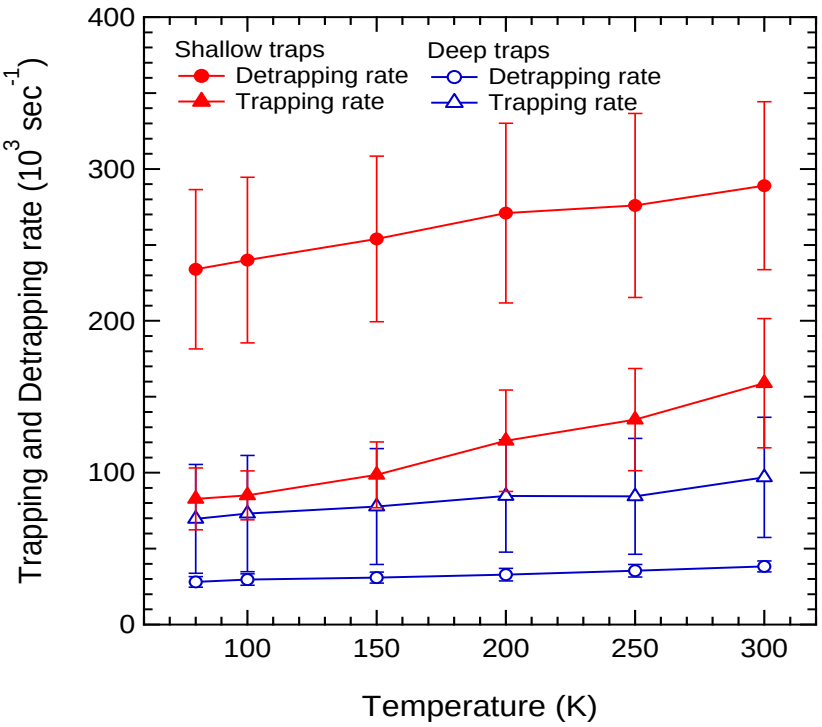

Figure 3.11 Temperature-dependent trapping and detrapping rate.

Table 3.2 Trapping rate and detrapping rate extracted from Eq. 3.2, Eq. 3.3.

Temp. (K)	κ_1	κ_2	γ_1	γ_2
300 K	2.89×10^5	3.83×10^4	1.59×10^5	9.70×10^4
250 K	2.79×10^5	3.54×10^4	1.35×10^5	8.44×10^4
200 K	2.71×10^4	3.29×10^4	1.21×10^4	8.47×10^4
150 K	2.54×10^4	3.10×10^4	9.86×10^4	7.77×10^4
100 K	2.40×10^4	2.96×10^4	8.51×10^4	7.31×10^4
80 K	2.34×10^4	2.81×10^4	8.28×10^4	6.96×10^4

3.3 Summary

In summary, we investigated the relationship between the trapping of charge carriers and the charge transport properties of the SWCNT transistor using both DC and transient analysis. Throughout the DC analysis, we found that the origin of charge trapping in the SWCNT transistor is the charge injection from the CNTs to the surrounding dielectrics. Transient analysis was also performed for a more detailed analysis. We began the transient analysis by verifying that the empirical equation developed from the trapping model is well fitted to the experimentally obtained transient response. Leveraging the empirical equation, the effects of the shallow traps and deep traps on the charge velocity distribution was successfully investigated. The correlation between the trapping of charge and the charge carrier density (n) was also performed using transient analysis. Our results showed that the shallow traps significantly contributed to the charge transport properties in the SWCNT transistor compared to the deep traps.

Chapter 4

Improvement of Contact Properties of SWCNT Transistors

Although the unique feature of the carbon nanotube (CNT) takes advantage in terms of the electrical tuning property for the required device operation, this unique 1D feature also yields issues in the contact between the S/D electrode and the CNT. Since the diameter of a single-walled carbon nanotube (SWCNT) is typically in the 1–3 nm range, the effective contact area between the SWCNT and S/D electrode reduces to the diameter of the SWCNT [16,28,29]. This leads to the effective channel width of the device being smaller than the device with the general 3D materials and results in the increase in contact resistance. Thus, various studies have been made to investigate the contact property in the CNT transistor [16,17,28,80,81]. J. Xia and coworkers [16] found that the CNT-metal contact could form a Schottky contact and this could

significantly influence the electrical performance of the random-network SWCNT transistors. C. Cao and coworkers [17] have investigated the effect of device geometry on contact resistance in a random-network SWCNT transistor by employing three different types of device geometry (top contact, bottom contact, and double contact). They found that the bottom contact takes advantage of the top contact in terms of the electrical performance of the SWCNT transistor. Moreover, they showed that the double contact (bottom contact metal/semiconductor/top contact metal) offers a significant decrease in contact resistance regardless of contact material (Ag nanoparticles, Au nanoparticles, and metallic CNTs). However, the double contact presumably has disadvantages in terms of fabrication process time and device yield. Thus, improving the contact property of a random-network SWCNT transistor by modifying the device geometry or employing the S/D electrode that is favorable for the SWCNTs to the S/D contact is necessary to enhance the electrical performance of the SWCNT transistor.

Graphene is considered as an excellent contact material for the CNT device because it provides homogeneous carbon junction [81,82], and good electro-physical compatibility between graphene and CNT [83]. Thus, many research groups have employed graphene as the S/D contact or as the gate electrode in a CNT transistor for better electrical performance, flexibility, and transparency [83–85]. P. R. Yasasvi Gangavarapu and coworkers [86] performed temperature-dependent measurements to extract the barrier height between the CNTs and graphene, and they found that the graphene electrodes formed almost no barrier between the CNTs regardless of graphene thickness.

Very recently, C. Qiu and coworkers [4] reported a graphene S/D contact CNT transistor with a 5-nm gate length having superior electrical performance to the

silicon transistor (fabricated using Intel's technology). They attributed such an improvement in mobility and I_{on}/I_{off} to the CNTs/graphene/insulator/gate stacked structure and the nanometer thin nature of the graphene layer that enhanced the gate controllability. Although graphene S/D electrode was found to be effective for the aligned CNT transistors with 5-nm gate length, less attention had been made to improve the electrical performance of the random network CNT transistor by employing the graphene S/D electrode [84,86]. Inspired by previous results showing that the graphene S/D electrode could lead to homogeneous carbon junction and barrier-free contact to the CNT, we investigated the effect of the graphene S/D contact on the random-network SWCNT transistor in bottom-gate bottom-contact (BGBC) geometry.

4.1 Advantages of Proposed Device Geometry

We fabricated our devices in BGBC geometry using graphene as the S/D electrode and palladium (Pd) as the contact pad (Fig. 4.1). For convenience, an indium-tin-oxide (ITO) gate electrode was deposited in the entire area of the substrate such that the electrical characteristics of the graphene electrode could also be modulated by the gate [4]. The detailed fabrication process was discussed earlier in Chapter 2. We expect three main advantages throughout this device geometry: (i) The Pd contact pad acts not only as the contact pad but could also be used as an alignment key for photolithography patterning. Thus, the stacking of transparent layers such as graphene or CNTs becomes easier (Fig.4.2). This method also enables us to use highly transparent monolayer graphene as the S/D contact electrode for the fabrication of the SWCNT transistor. (ii) Since the graphene layer is stacked before the SWCNTs deposition, the electric field from the gate could largely influence the graphene S/D electrode [4]. Thus, the drain current can be additionally modulated by the graphene electrodes. (iii) Because the CNTs deposition is the last step of the fabrication, the CNT has less chance to be damaged during the fabrication process, which is advantageous for the electrical properties of carbon-based devices, as was consistently argued from other research groups [17,87]. Since the graphene film deposition step is before the CNT deposition, the graphene film characteristics is an important factor that determines the SWCNT film and the electrical performance of the SWCNT transistor. Thus, the film characteristics and the I–V characteristics of graphene will be discussed in the following section.

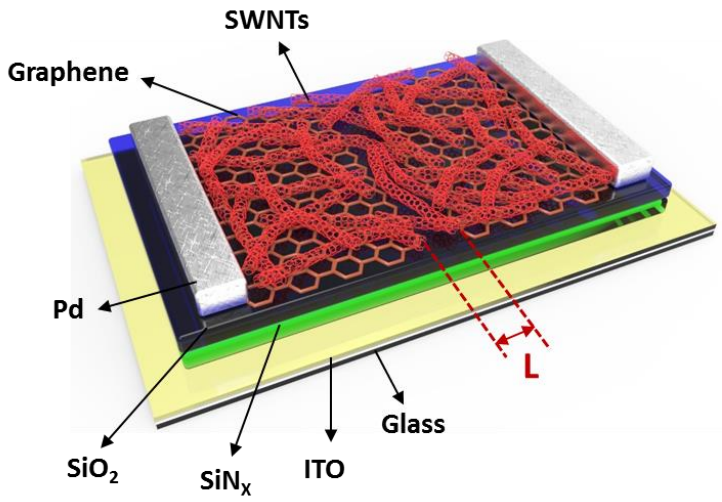

Figure 4.1 Schematic of graphene S/D contact SWCNT transistors.

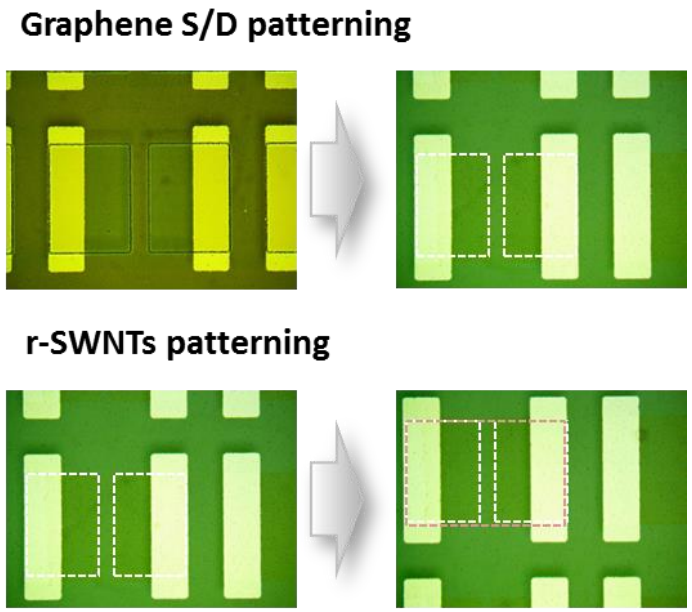

Figure 4.2 Optical microscopic image of graphene S/D patterning and SWCNTs patterning.

4.2 Graphene Characterization

4.2.1 Graphene Film Characterization

Although many methods of forming graphene monolayer exist, such as the mechanical exfoliation method, and solution process method, chemically prepared graphene is advantageous in terms of being able to form good-quality single-layer graphene in a large area. [35–38] Thus, chemical vapor deposition (CVD) graphene was used as the S/D electrode in this study. The film characteristics of the CVD-grown graphene was investigated using optical microscopy, scanning electron microscopy (SEM), AFM, and the Raman spectra as in Fig. 4.3. The schematic of the CVD graphene grown on Cu foil is described in Fig. 4.3 (a). The morphology of the graphene film was measured when the CVD graphene is on the Cu foil. The optical microscopic image reveals that our graphene sheet consists of large-sized grains (diameter of grain ~100 μm), whereas the SEM and AFM images show that the graphene films consist of small-sized grain (~1 μm). From these results, we found that our graphene sheet consists of a combination of large-sized and small-sized grains. The line trace of the graphene layer in the inset of Fig. 4.3 (d) shows that graphene has a very smooth surface, with a root mean square (RMS) value of 0.3 nm. Two prominent peaks at ~1588 cm^{-1} and 2650 cm^{-1} in the Raman spectra correspond to the characteristics of the G and 2D bands of graphene, respectively (Fig. 4.3 (e)). The intensity ratio between the G and 2D peaks (I_G/I_{2D}) indicate the number of graphene layers. The I_G/I_{2D} was extracted to be 0.44, which implies that our graphene is a monolayer graphene [88,89]. The I_G/I_D was relatively large in our graphene, indicating that our CVD-grown graphene consists of high-quality carbon atoms without significant structural defects.

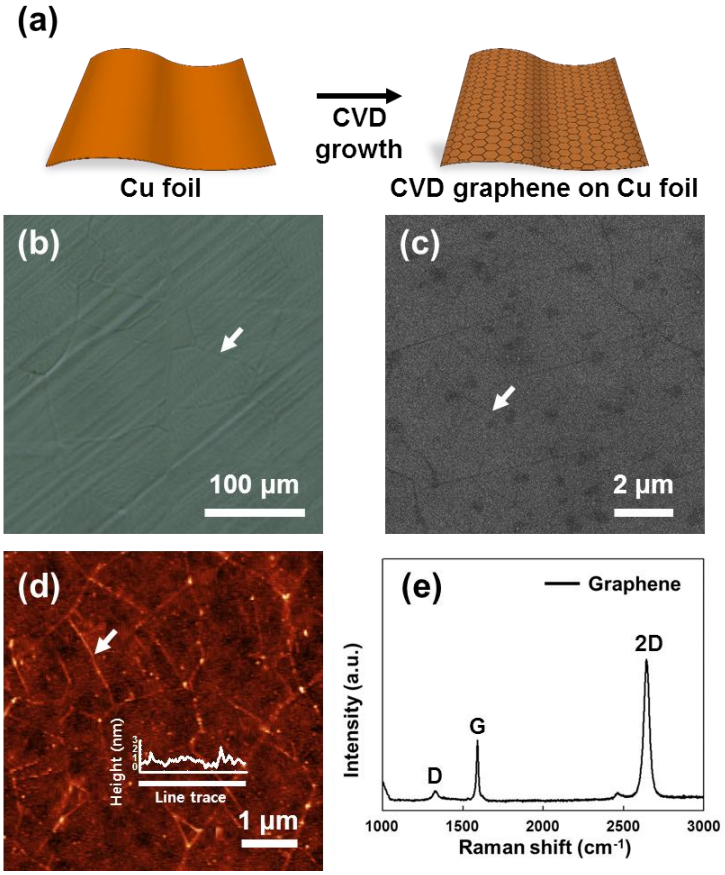

Figure 4.3 (a) Schematic of CVD graphene grown on Cu foil. (b) Optical image, (c) SEM image, (d) AFM image of graphene on Cu foil (white arrows indicate grain boundary of graphene). (e) Raman spectra of graphene on silicon wafer.

4.2.2 I–V Characteristics of Graphene

To use the CVD graphene sheet as the S/D electrode, the resistivity of the graphene sheet and the contact resistances in Pd and the graphene interface should be sufficiently small. Thus, the resistivity of graphene and the contact resistance between Pd and graphene were investigated using the transmission line method (TLM). The graphene sheet that forms contact with the two Pd counter electrodes was used for the I–V characterization of graphene. The distances between the two Pd electrodes (channel length) were 30, 50, 75, 100, and 150 μm. The current–voltage (I–V) characteristics were measured in more than 5 different samples (Fig. 4.4(a)). From these I–V curves, we were able to extract the contact resistance in Pd/graphene and the sheet resistance of graphene. The contact resistivity in Pd/graphene is the y-intercept of the plot in Fig. 4.4(b) and it was extracted to be 28.63 kΩ·μm, which is similar to the previously published results [47,90,91]. The sheet resistivity of graphene is extracted from the slope of the plot in Fig. 4.4(b). The resistivity of graphene sheet was extracted based on the assumption that our graphene sheet is a monolayer, as previously confirmed by the Raman spectra. The resistivity of graphene was extracted to be 0.95 Ω·μm. Table 4.1 compares the resistivity of graphene with metals. As in Table 4.1, the resistivity of our CVD graphene was much larger than the metals, probably due to the grain boundary in the graphene sheet that hinders charge transport. Thus, using the monolayer CVD graphene as an electrode for the large area application seems inappropriate. Multilayers of CVD graphene or an additional conductive metal for the electrical wiring between the transistors could be candidate methods of using CVD graphene for the large area application. Although the resistivity of the CVD graphene was relatively large compared with typical metals,

we concluded that this value is small enough to be used as the S/D electrode in a single transistor device, since the sheet resistance of the SWCNT film was much larger. The sheet resistance of the SWCNTs and the contact resistance of SWCNT/graphene will be discussed in detail in a later section.

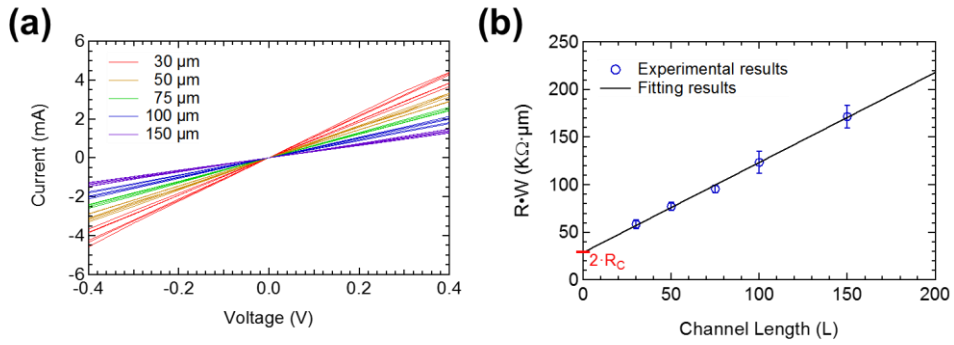

Figure 4.4 (a) I–V characteristics of graphene sheet as a function of channel length. (b) Channel-length-dependent total resistance.

Table 4.1 Comparison of resistivity of graphene sheet with other materials.

Materials	ρ (Ω · μm) at 20 ℃
Our results	**0.95**
Carbon(graphene)	0.01
Silver (Ag)	0.0159
Copper (Cu)	0.0168
Gold (Au)	0.0244

4.2.3 Effective Work Function of Graphene

Since the contact resistance could be caused by the dipole moment near the interface or the Schottky barrier between Pd and graphene, we investigated the work function of Pd, graphene, and the SWCNTs using photoelectron spectrometer measurements. The work function was extracted from the middle point of the first slope as depicted in Fig. 4.3 [92,93]. Since the electrical performance of the device was measured in the ambient air condition, the work function measurement was also performed in the same manner such that it is deliberately contaminated by oxygen or carbon-based molecules for the direct comparison of both data. The work function of Pd, graphene, and SWCNTs was extracted to be 4.45, 4.4, and 4.42 eV. From these results, we assumed that neither the dipole moment nor the Schottky contact is formed between Pd and graphene or between Pd and the SWCNTs interface. Thus, we concluded that the work functions of graphene and CNT are well aligned to Pd, and that this is not the dominant factor that influences the electrical performance of the device.

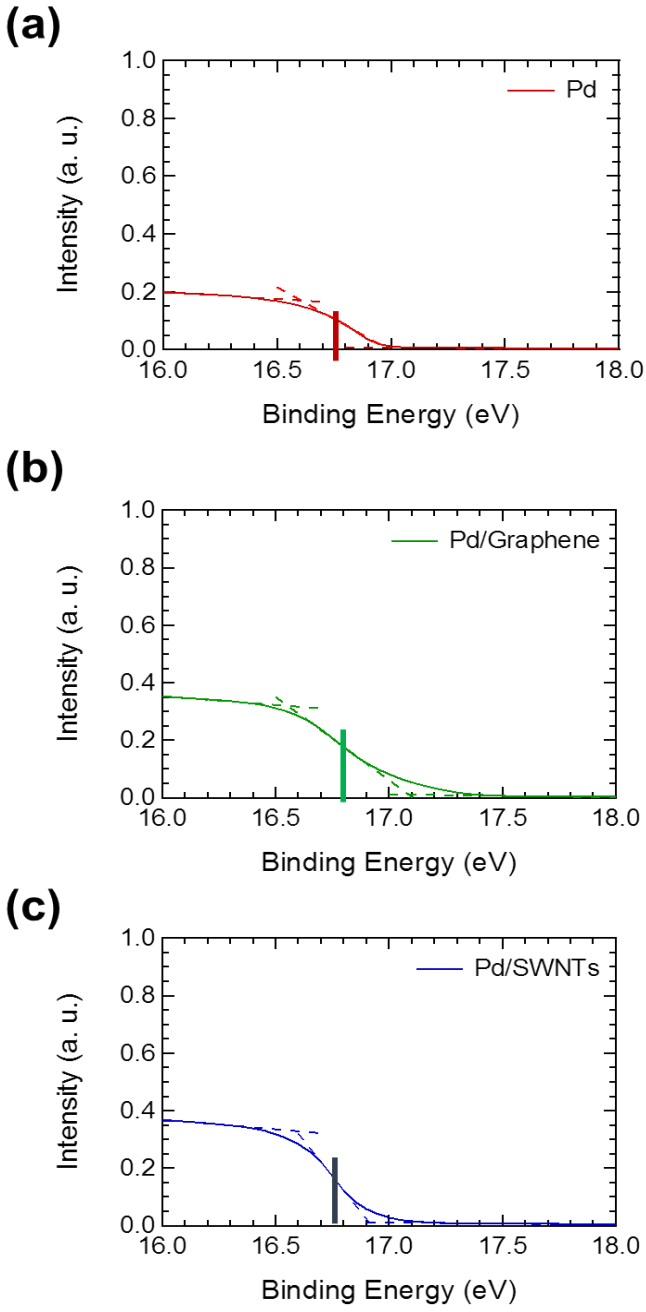

Figure 4.5 Effective work function of (a) palladium (b) graphene on palladium (c) SWCNTs on palladium.

4.3 Characteristics of Graphene Contact SWCNT Transistors

4.3.1 Investigation of Surface Energy for SWCNT Deposition

Since the deposition of SWCNTs was performed using the drop-casting method, the surface energy of the underlying layer could largely influence the SWCNTs deposition characteristics. Thus, the surface energy of graphene, Pd, and SiO_2 was investigated by measuring the contact angle of the polar solvent (DI water) and non-polar solvent (diiodomethane) as in Fig. 4.6. By substituting the contact angle in the Good Van Oss model (Eq. 4.1), we were able to extract the surface energy of each layer [94,95].

$$(1+\cos\theta_t)\gamma_t = 2\left\{\left(\gamma_t^d\gamma_s^d\right)^{\frac{1}{2}} + \left(\gamma_t^p\gamma_s^p\right)^{\frac{1}{2}}\right\}, \quad (4.1)$$

Where θ_t is the contact angle of liquid on the dielectric layer, γ_s^d and γ_s^p are the dispersive component and non-dispersive component, respectively, and γ_t^d and γ_t^p are the energy components of typical liquids. The average surface energy of each layer is summarized in Table 4.2. It is noteworthy that the surface energy of graphene can be influenced by surface defects and π-hydrogen bonding. Since the initially deposited graphene attracts airborne hydrocarbons and shields the polar surface sites, the surface energy of graphene decreases as it is exposed to air for a long time [96]. Thus, the surface energy of graphene can be modified with respect to the film's grain boundary and the exposure time in air. In our case, the surface energy of graphene was lower than the surface energy of SiO_2, whereas the surface energy of Pd was higher than that of SiO_2.

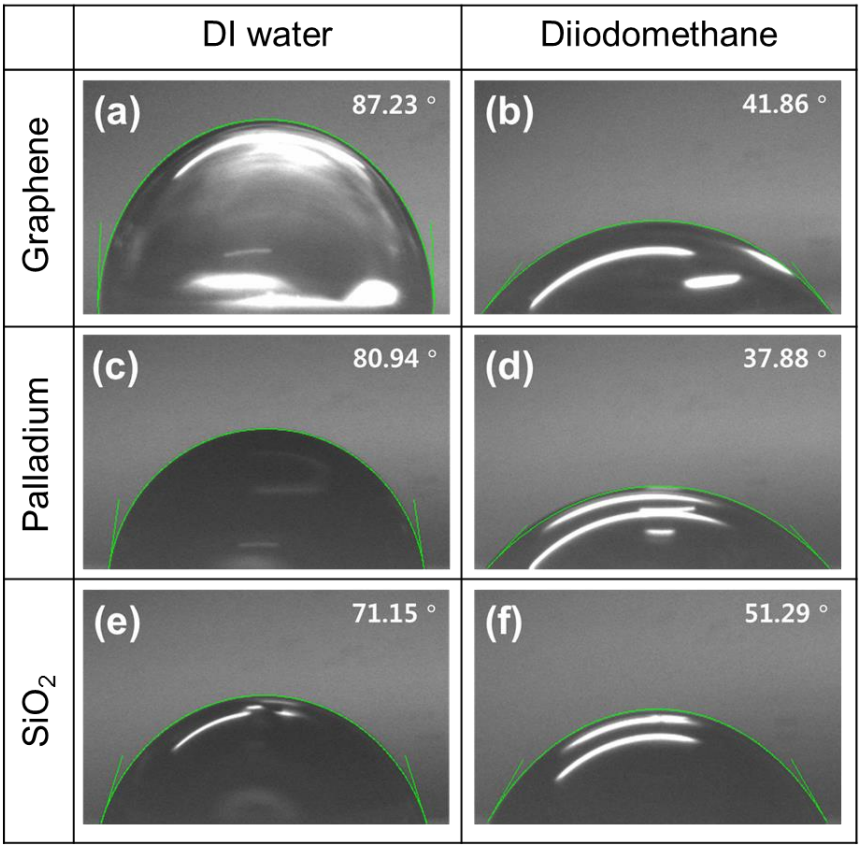

Figure 4.6 Contact angle of DI water and diiodomethane on (a),(b) graphene, (c),(d) palladium and (e),(f) SiO_2.

Table 4.2 Average surface energy of each layer.

Materials	Surface energy (mJ/m^2)
Graphene	39.81
Palladium	44.19
SiO_2	41.82

4.3.2 SWCNT Film Characterization

The SWCNT film density was then investigated using an AFM image because the SWCNTs film density is an important factor that determines the overall electrical performance of the SWCNT transistor. For the reference devices, the SWCNTs with Pd S/D contact were also fabricated. Since the CNT film density is a function of the CNT deposition time, the SWCNT transistors were fabricated with respect to two different CNT deposition times (1t, 2t). Fig. 4.7 shows the AFM image of the graphene S/D contact SWCNT (Gr-SWCNT) film with (a) 1t and (b) 2t deposition times, and Pd S/D contact SWCNT (Pd-SWCNT) film with (c) 1t and (d) 2t deposition times. It is noteworthy that the AFM image was acquired at the channel of each device. Both the Gr-SWCNT and Pd-SWCNT film densities increased as deposition time increased. The SWCNT film with 2t deposition time has a larger SWCNT diameter than the SWCNT film with 1t deposition time. This is probably due to the fact that the CNTs are entangled with each other and formed a bundle of SWCNTs. The SWCNT film with graphene contact showed a denser film formation than that with the Pd contact. We attribute such results to the surface energy difference between each layer. In our graphene contact device, SiO_2 is located between the graphene (hydrophobic part). Thus, the drop-casted CNTs would form a dense film on the channel (on top of SiO_2) with the graphene contact, presumably due to the selective wetting properties that led the SWCNTs to accumulate towards the channel [97–100].

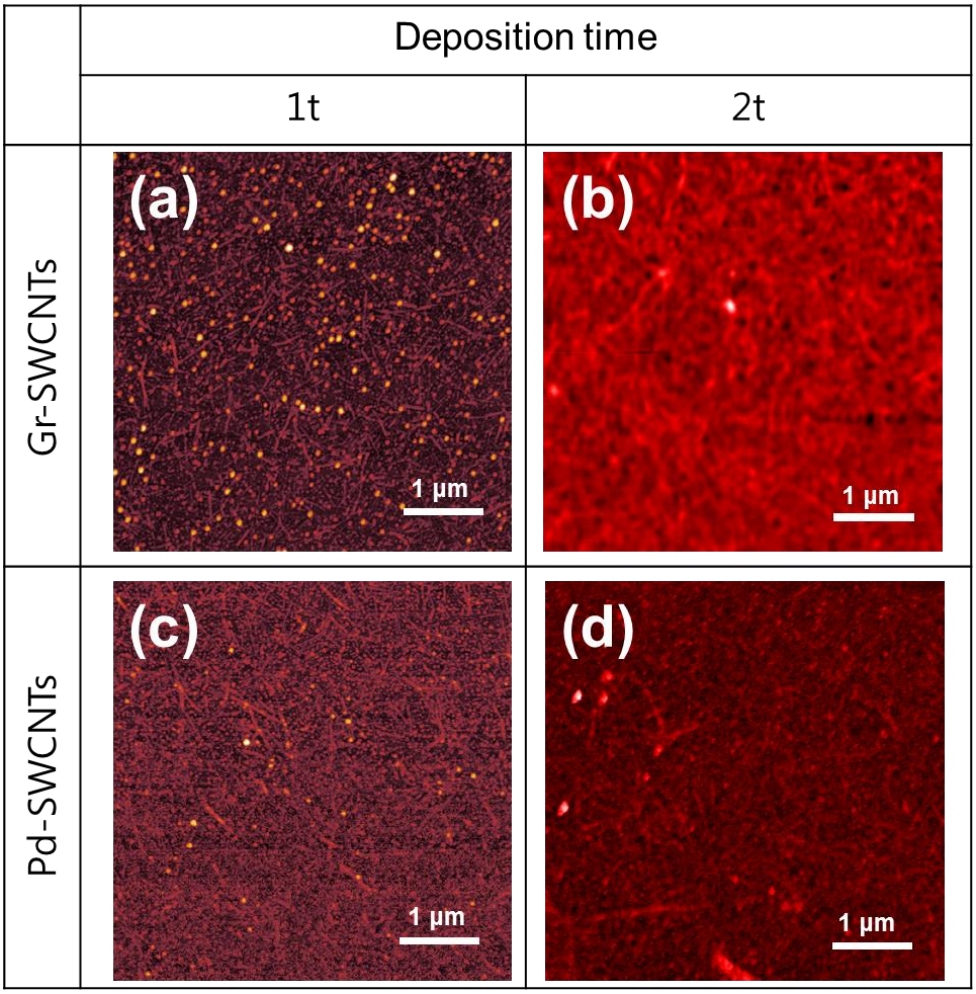

Figure 4.7 AFM image of graphene S/D contact SWCNT film with (a) 1t and (b) 2t deposition times and palladium S/D contact SWCNT film with (c) 1t and (d) 2t deposition times.

4.3.3 I-V Characterization in Graphene S/D Contact SWCNT Transistors

Fig. 4.8 shows the transfer characteristics of the Gr-SWCNTs transistor and the Pd-SWCNTs transistor with two different CNT deposition times. More than 10 different samples were measured to acquire reliable data. The I_{on}/I_{off} and mobility of each device are summarized in Table 3.3. For simplicity, the mobility was extracted using the parallel-plate model. As summarized in Table 3.3, both the Pd and graphene S/D contact SWCNT transistor showed an increase in current density and a decrease in I_{on}/I_{off} when the deposition time was increased. This is largely due to the CNT bundles, which could act as a conducting path that is less sensitive to gate modulation. Thus, there is trade-off relationship between current density and I_{on}/I_{off} [28]. Since the SWCNT film with graphene S/D contact has a denser CNT film than that with the Pd S/D contact, the electrical performance of the Gr-SWCNT transistor should have a higher current density with lower I_{on}/I_{off}. However, the Gr-SWCNT showed improved current density and mobility with no significant decrease in I_{on}/I_{off}. This trend becomes more clear when we compare the Gr-SWCNT transistor and the Pd-SWCNT transistor at 2t deposition time, where the Gr-SWCNT transistor has a higher current density and a higher value of I_{on}/I_{off}. Although it is not desirable, the improvement in I_{on}/I_{off} in Gr-SWCNTs could be due to the Schottky contact in graphene/SWCNTs, where the Schottky barrier height could additionally modulate the charge injection property [101–104]. Thus, we further investigated the contact property between the graphene and SWCNTs.

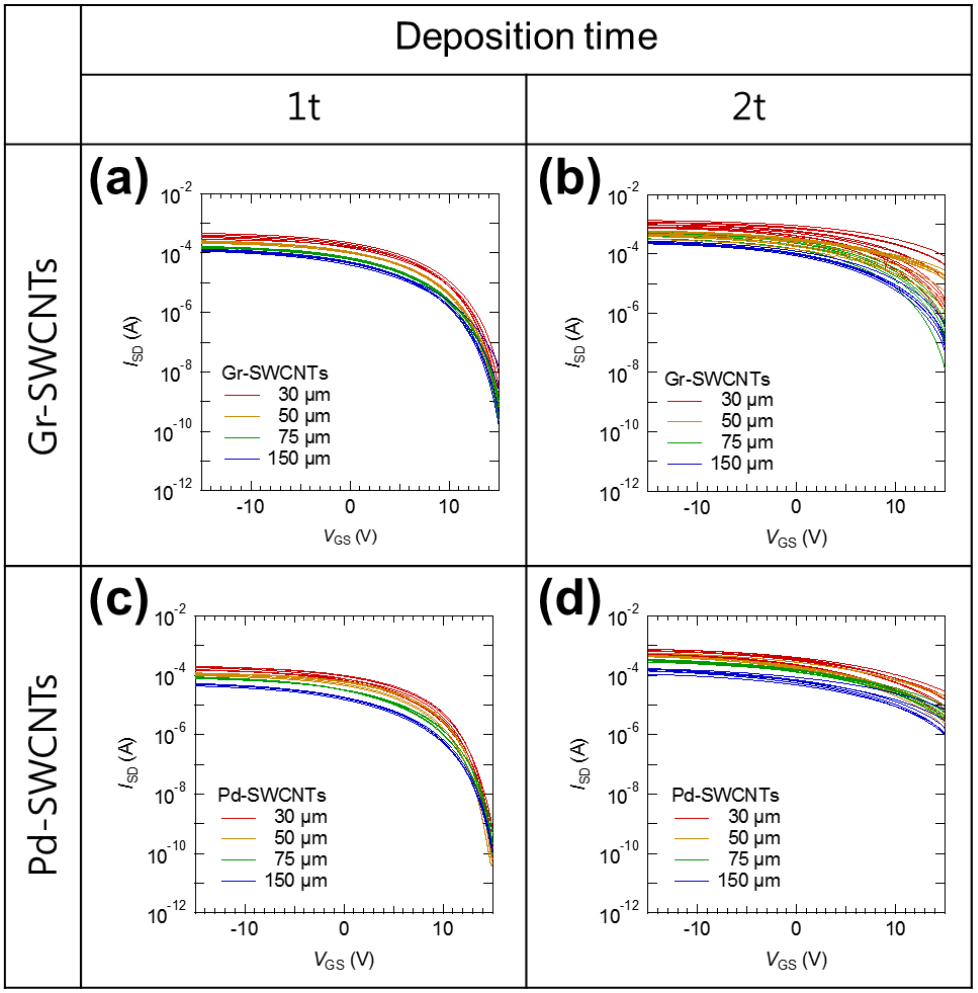

Figure 4.8 Transfer characteristics of graphene and palladium S/D contact SWCNT transistors with respect to two different SWCNTs deposition times, where (a) and (b) are the graphene contact SWCNT transistors with 1t and 2t SWCNTs deposition times, respectively, and (c) and (d) are the palladium S/D contact SWCNT transistors with 1t and 2t SWCNTs deposition times, respectively.

Table 4.3 Average I_{on}/I_{off} and mobility from the transfer curve.

	I_{on}/I_{off}	Mobility ($cm^2/V{\cdot}s$)
Gr-SWCNTs (1t)	7.36×10^5	8.14
Pd-SWCNTs (1t)	1.13×10^6	4.43
Gr-SWCNTs (2t)	1.18×10^4	13.31
Pd-SWCNTs (2t)	1.91×10^2	7.36

The Schottky barrier between the S/D electrode and the channel can be generally investigated by varying the temperature, but such a method is not applicable to SWCNT transistor since many inter-tube junctions are in the channel and the conductivity of the SWCNT film could also change with respect to temperature [16]. Thus, we investigated the contact property between graphene and the SWCNTs using the stick percolation frame work. J. Xia *et al.* recently showed that the value of *m* (exponent of the stick percolating) can be smaller than 1 in the Schottky-type contact SWCNT transistors (generally, the exponent *m* is equal to 1 or larger than 1) [16]. Inspired by these previous results, we investigated the effect of contact resistance on the conducting behavior of the SWCNT transistors using Eq. 4.2 [16,105].

$$\frac{I}{W} = \frac{\sigma V}{L^m} \tag{4.2}$$

Where I is the current; L and W are the channel length and width of the device, respectively; σ is the conductivity; V is the voltage; m is the exponent of the stick percolating system. For a long channel device ($L \gg L_S$), the current through the SWCNTs can be described as in Eq. 4.3 [16,105].

$$I \sim f(V_G, V_D)\left(\frac{L_s}{L}\right)^{m(\rho_s L_s^2)} \tag{4.3}$$

Where L_S is the tube length, L is the channel length, and ρ_s is the tube density. Fig. 4.9 shows the length scaling of the calibrated current at (a) high V_D (- 15 V) and (b) low V_D (- 1 V). As in Fig. 4.9, the current level was independent of the channel length of the device (m = 1), indicating that the transistor behaves as an ohmic conductor. Thus, the Schottky contact behavior was not observed in the Gr-SWCNT transistor. Fig. 4.10 shows the output characteristics of both the graphene and Pd S/D contact SWCNTs with 2 different SWCNTs deposition times. As in Fig.4.8, all the transistor showed no significant Schottky current behavior near 0 V, which indicates that the electrical characteristics of the device do not suffer from the contact resistance. This result is in good agreement with the photoelectron spectrometer measurement result and previously published results from the other group [86,106], where the work function of graphene was well aligned with that of Pd and the SWCNTs.

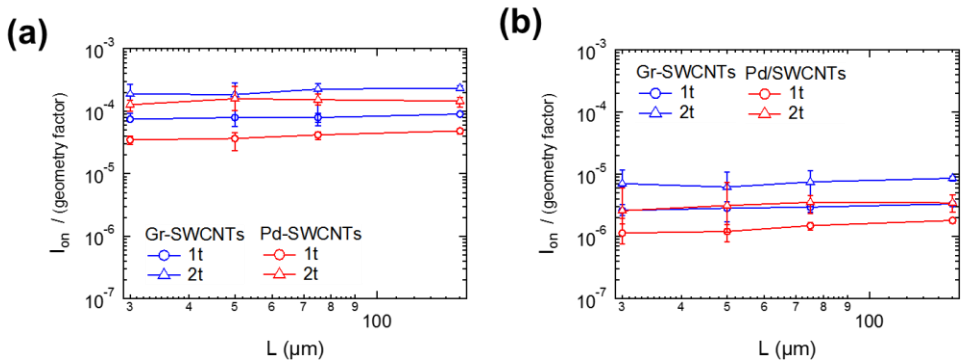

Figure 4.9 The length scaling of calibrated current at (a) high V_D (- 15 V) and (b) low V_D (- 1 V)

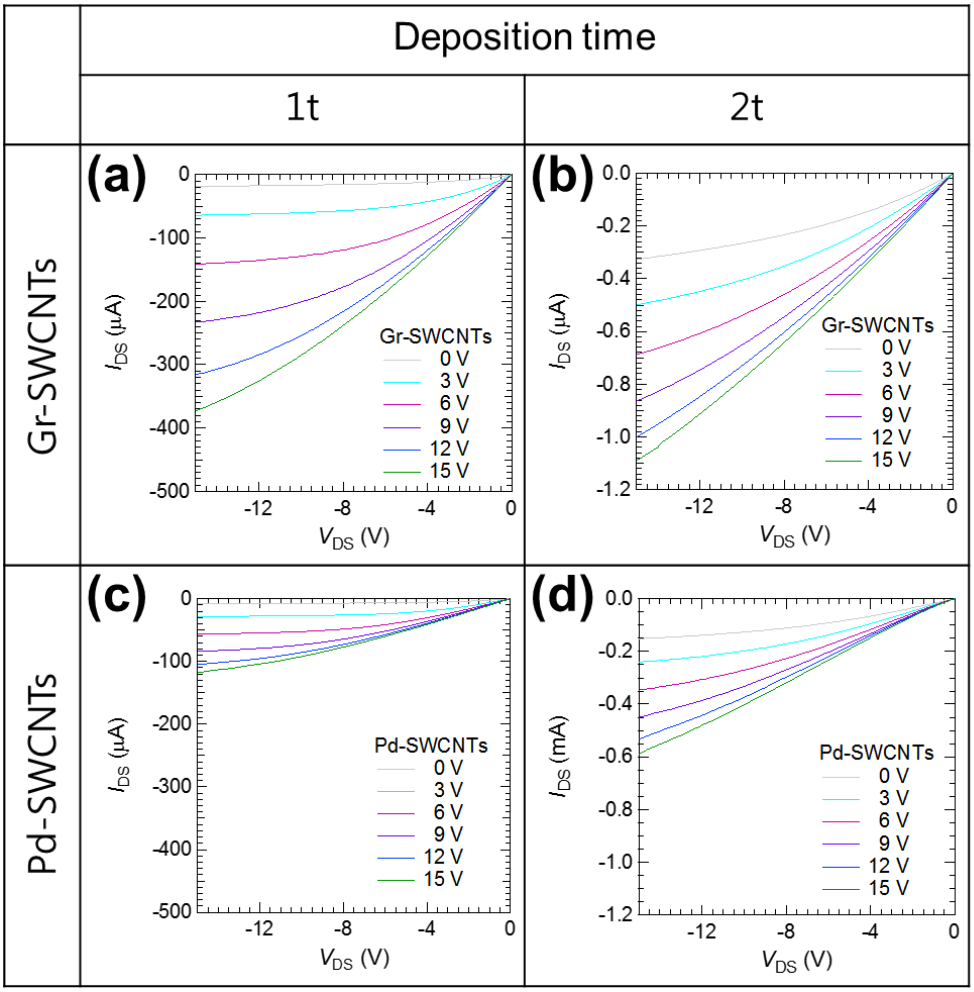

Figure 4.10 Output curve characteristics of graphene and palladium S/D contact SWCNT transistor with two different SWCNT deposition times, where (a) and (c) are the graphene S/D contact SWCNT transistor with 1t and 2t SWCNTs deposition times, respectively, and (b) and (d) are the palladium S/D contact SWCNT transistor with 1t and 2t SWCNTs deposition times, respectively.

4.3.4 Contact Resistance of Graphene S/D Contact SWCNT Transistors

In previous section, the influence of the S/D contact to the electrical performance of the transistor was investigated using the stick percolating system. The Gr-SWCNT transistor showed the exponent of the stick percolating system near 1 (m = 1) which indicates that there is no significant Schottky barrier in S/D contact region. However, this result could be due to the fact that the measurement was performed in the device with relatively long channel (the effect of the contact resistance to the overall electrical performance of the device becomes smaller as the channel length is increased). Thus the further investigation was necessary.

The contact property of Gr-SWCNTs was further investigated using the transmission line method (TLM) as depicted in Fig. 4.11. Extracted parameters are summarized in Table 4.4. Since a larger number of CNTs in the channel could increase the junction between the CNT and the S/D electrode, both the Gr-SWCNT and Pd-SWCNT transistors showed less contact resistance at 2t deposition time than at 1t deposition time. The sheet resistance of the device with 2t deposition time was almost independent of the applied gate voltage, whereas the sheet resistance of the device with 1t deposition time is strongly influenced by the applied gate voltage. This is consistent with the transfer curve results where the gate is less likely to modulate the drain current when the deposition time of the CNT is longer. It is noteworthy that the contact resistivity between Pd and graphene was extracted to be 28.63 kΩ·μm, which is a far lower value than the contact resistivity in Pd/SWCNT or graphene/SWCNT (Table 4.4).

Finally, the contact property of the Gr-SWCNT transistor was investigated by comparing the contact resistance and sheet resistance of the Gr-SWCNT transistor

with those of the Pd-SWCNT transistor. Since the contact resistance of the device is related to the sheet resistance of the SWCNT film (film density), a fair comparison of contact resistance between the Gr-SWCNTs and Pd-SWCNTs could not be made by simply comparing the contact resistance of each device. Thus, we divided the contact resistance with the sheet resistance to acquire a value that is independent of the CNT film density, such that a fair comparison can be made. As summarized in Table 4.4, the graphene contact had a smaller R_c/R_S value compared to the Pd contact, which reveals that the graphene/SWCNTs contact is more favorable for the charge injection than the Pd/SWNCNTs contact. This improvement in the Gr-SWCNT transistor could be due to the thin layer of graphene that enables the junction between the SWCNTs and S/D electrode favorable for the charge injection [86]. The electrochemical compatibility between the SWCNTs and graphene might also be more favorable than that of the Pd/SWCNTs, because both graphene and CNTs are material derived from carbon [83]. Since the contact property was improved by employing the graphene/SWCNT contact in our device geometry, Schottky contact does not seem to be the reason for the such improvement in I_{on}/I_{off}. Since the band-gap of graphene can be modulated depending on the hydrogen adsorption (during the RIE etching process) or surface characteristics of the underlying SiO_2 [107–109], such improvement in the high current density with the good I_{on}/I_{off} could be due to the additional gate modulation from the graphene.

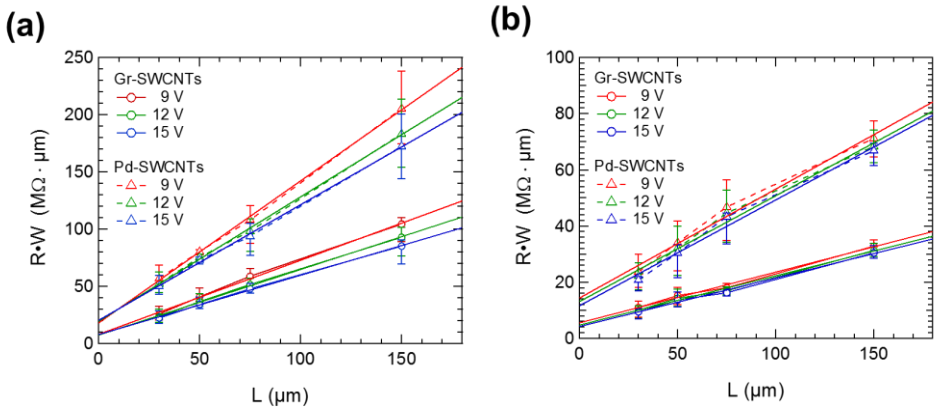

Figure 4.11 Total resistance of the graphene S/D contact SWCNTs and palladium S/D contact SWCNT transistor with respect to channel length in (a) 1t and (b) 2t deposition time.

Table 4.4 Contact resistance and sheet resistance of graphene S/D contact SWCNT and Pd S/D contact SWCNT transistors.

	R_c (KΩ)	R_S (MΩ)	R_c / R_S ($\times 10^{-3}$)
Gr-SWCNTs (1t)	12.53	0.362	0.346
Pd-SWCNTs (1t)	34.45	0.613	0.562
Gr-SWCNTs (2t)	6.97	0.243	0.287
Pd-SWCNTs (2t)	22.42	0.355	0.631

4.4 Transparent SWCNT Transistors

CVD graphene and SWCNTs are advantageous in terms of their transparency. This advantage could lead to the fabrication of transparent electrical circuits or bottom-emission display modules. Fig. 4.12 shows the transmittance of the device with respect to layer deposition. Since the glass substrate could absorb some amount of UV light, the transmittance data was acquired from the light source in a visible range. As in Fig. 4.12, the transmittance of the device was higher than 80% in the entire visible wavelength. It is noteworthy that the transmittance data is acquired without the Pd contact pad and the observation of the wavy transmittance data is due to the high transmittance of the device. Our transparent graphene contact transistor is demonstrated in Fig. 4.13.

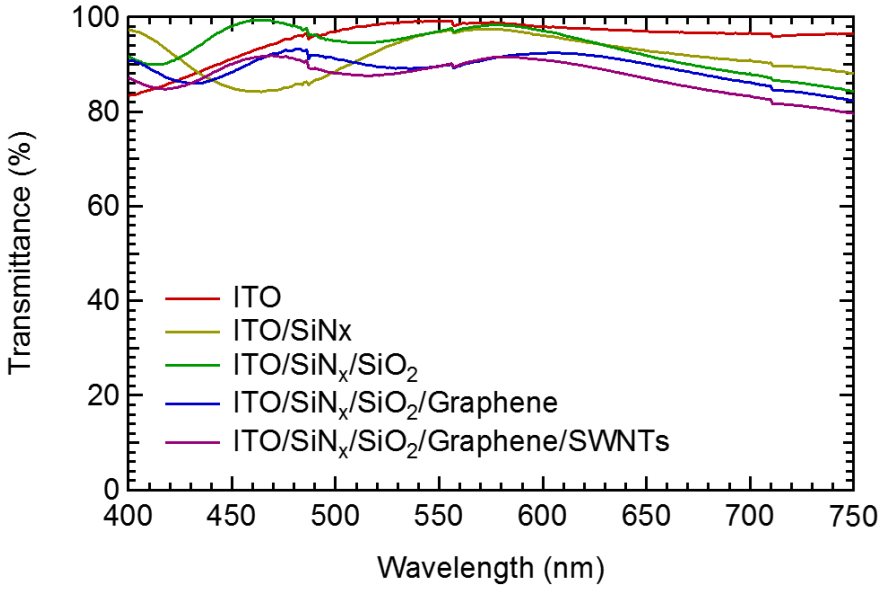

Figure 4.12 Transmittance of the device in each layer.

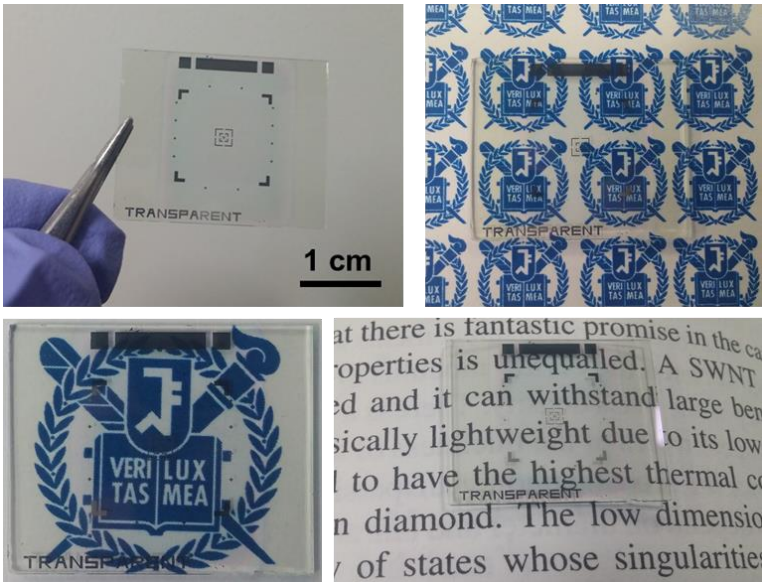

Figure 4.13 Real size image of the transparent device.

4.5 Summary

In summary, we improved the electrical performance of the SWCNT transistor by using graphene as the S/D electrode. Our fabrication scheme enabled the good electrical performance with ease of fabrication. By employing the graphene S/D electrode, we were able to form a dense CNT film, presumably due to the selective wetting properties that led the SWCNTs to accumulate towards the channel. Our results indicate that the BGBC geometry and the thin layer of graphene (~1 nm) good mobility without significant sacrifice in I_{on}/I_{off}. With the ohmic conducting behavior in the Gr-SWCNT transistors, the contact resistance of the Gr-SWCNT transistors were extracted to be lower than that of the Pd-SWCNT transistors. Thus, we believe that using the CVD graphene as the S/D electrode in a proposed BGBC device configuration is a good method of improving the electrical performance of the SWCNT transistor.

Chapter 5

Conclusion

In this thesis, we investigated two important interfaces in the random-network single-walled carbon nanotube (SWCNT) transistors: (i) CNTs to gate insulator, and (ii) CNTs to source/drain (S/D) electrodes.

First, we investigated the trapping/detrapping of charge carriers in the SWCNT film, where the SWCNTs were deposited on top of the gate insulator (SiO_2). The SWCNT film was characterized first since the SWCNTs should be well interdigitated with each other, such that the SWCNT film can successfully transport charges from the source to the drain electrodes. Because the SWCNTs do not fully cover the gate insulator and the CNT-to-CNT inter-coupling could occur in the SWCNT films, we also extracted the effective capacitance of the device using an analytical equation. Following the SWCNT film characterization and the effective capacitance extraction, we investigated the temperature-dependent activation energy (E_a). The activation

energy (E_a) was extracted to be a much lower value than that from the defect sites in the gate insulator or residual ions. We also studied the correlation between charge carrier density (n) and charge trapping using the temperature-dependent transfer characteristics (from 80 K to 300 K). From the temperature-dependent carrier density (n) and trap density (N_t), we confirmed that charge trapping in the SWCNT transistor channel is primarily due to the charge carrier injection from the SWCNTs to the surrounding dielectric layer in the device. The trapping behavior in the SWCNT film was further characterized by employing the temperature-dependent transient measurement by applying a step impulse signal to the source electrode. The measurement circuit was kept small to extract the intrinsic RC time constant (τ) value within the SWCNTs channel. An empirical equation was developed from the theoretical equation to further study the trapping effect in the SWCNTs channel. We started out our transient analysis by extracting the activation energy (E_a) from the temperature-dependent transient mobility. The activation energy (E_a) extracted from the transient analysis supports that the trapping of charges is not from the defect sites in the gate insulator or residual ions. A charge velocity distribution was also plotted as a function of temperature, and the integrated value of the velocity distribution showed that the velocity distribution in the high velocity part (where it is largely influenced by the shallow traps) consumes a large portion of the velocity distribution, implying that charge velocity is largely influenced by the shallow traps. The relationship between charge carrier density (n) and the RC time constant value deviation ($\Delta\tau$) was characterized as it was done in the DC analysis. The quantitative values of the trapping and detrapping rates were also extracted and the results showed that the shallow traps significantly influenced the charge transport property of the device.

Second, we investigated the contact behavior in the SWCNT transistor and improved the electrical performance of the device by employing the graphene S/D electrode. We applied the bottom-gate bottom-contact geometry to ease device fabrication and for good electrical performance. The chemical vapor deposition (CVD) graphene film was investigated to determine whether it is suitable to be used as a S/D electrode. The atomic forced microscopic image (AFM) and the scanning electron microscope (SEM) image of the graphene film showed that our monolayer graphene sheet consists of a combination of large-sized grains (diameter of grain ~100 μm range) and small-sized grains (~1 μm). By employing the transmission line method (TLM) to the graphene sandwiched between two counter electrodes in parallel, the resistivity of graphene was extracted to be 0.95 Ω·μm, which was suitable to be used as the S/D electrode for the transistor. The effective work function of graphene was in a range of the palladium (Pd) work function due to the Fermi level alignment in graphene. The combination of the surface energy and the SWCNTs film investigation result showed that the graphene contact is favorable for the SWCNTs to be densely formed in the channel. The I–V characteristics of the graphene S/D contact SWCNT (Gr-SWCNT) transistor showed better electrical performance than the Pd S/D contact SWCNT (Pd-SWCNT) transistor in terms of mobility (μ) and on-off current ratio (I_{on}/I_{off}). The TLM result showed that the Gr-SWCNT transistors has smaller contact resistance than the Pd-SWCNT transistors, presumably due to the thin graphene layer. The stick percolation system analysis and the TLM analysis indicate that the graphene form good contact with the SWCNTs.

In summary, this thesis provides an insight into a method of improving the CNT transistor performance by investigating the CNT/gate insulator interface (channel) and the CNT/ S/D contact. For the SWCNTs channel investigation, DC measurements

and transient measurements were performed and a corresponding empirical equation was developed based on the trapping theory. Our results showed that charge trapping occurs from charge injection from the SWCNTs to the surrounding dielectrics and that the shallow trap largely influences the charge transport properties in the SWCNT transistor. For the contact studies, we employed the CVD graphene as the S/D electrode. We found that the employing the graphene contact to SWCNT transistor is good way to improve the electrical performance of the SWCNT transistor. By using a thin layer of graphene (~1 nm) as the S/D electrode in the BGBS geometry, we achieved good mobility (μ) without significant sacrifice in I_{on}/I_{off} .

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[1] SCI Journal Papers

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8. C.-M. Kang, **H. Shin**, C. Lee, "High –Frequency Organic Rectifiers Through Interface Engineering", MRS communications **7**, 755 (2017)
9. **H. Shin**, C.-M. Kang, K.-H. Baek, L.-M. Do, C. Lee, "Low Temperature Solution-Processed Zinc Oxide Field Effect Transistor by Blending Zinc Hydroxide ($Zn(OH)_2$) and Zinc Oxide Nanoparticle (ZnO) in Aqueous Solutions" Japanese Journal of Applied Physics **(Under Revision)**

[2] International Conferences

1. **H. Shin**, J. Song, J. Roh, M. Park, C. Lee, “Organic field effect transistors based on performed poly (3-hexylthiophene) nanowires via solubility-induced crystallization”, International workshop on flexible & printed electronics (IWFPE), Muju, Korea (Nov, 2012).
2. C.-M. Kang, J. Roh, **H. Shin**, C. Lee, “Electrical and Morphological Properties of Pentacene Films on Surface-modified Gold”, Materials Research Society (MRS) spring meeting, San Francisco, USA (Apr, 2013).
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[3] Domestic Conferences

H. Shin, S.-Y. Park, T.-J. Ha, C. Lee, “Non-quasistatic Measurement for Charge Transport Properties of Single-walled Carbon Nanotube Thin Film Transistors”, 한국봄물리학회, Daejeon, Korea (Apr, 2015).

한글 초록

탄소나노튜브는 우수한 기계적, 전기적 특성을 가지며 이로 인해 차세대 전자 소자로 각광받고 있다. 유연하고 투명한 전자소자의 수요가 증가하고, 실리콘 트랜지스터의 전기적 특성 향상이 한계점에 다다르고 있으므로 탄소나노튜브를 반도체 층으로 이용한 트랜지스터 연구가 현재 활발히 진행중에 있다. 탄소나노튜브의 1 차원적 구조는 유연 소자 제작 및 전기적 특성을 바꾸기 용이하다는 장점을 낳지만, 이러한 독특한 1 차원 구조로 인해 다음과 같은 문제점을 야기하기도 한다. (i) 탄소나노튜브 트랜지스터는 탄소나노튜브에서 주변 절연체 층으로의 전하 확산 작용에 많은 영향을 받는다. 이로 인해 탄소나노튜브 트랜지스터의 전기적 특성은 박막 표면에서의 전하 트랩핑 효과에 상대적으로 많은 영향을 받게 된다. (ii) 단일 벽 탄소나노튜브의 지름이 일반적으로 1 - 3 nm 인 점을 고려해볼 때 탄소나노튜브 트랜지스터는 구조적으로 정의한 채널 넓이만큼의 소스/드레인 (S/D) 접촉 영역에 비해 적은 면적의 접촉이 일어나고 이는 접촉 저항 값을 상대적으로 크게 만드는 효과를 낳는다. 따라서 본 연구에서는 탄소나노튜브가 트랜지스터로 제작되었을 시 탄소나노튜브와 다른 층 사이 (탄소나노튜브/절연체, 탄소나노튜브 /전극) 계면에서 일어나는 특성에 관한 연구를 진행하였다.

첫번째로 트랜지스터 채널 내에서의 전하 이동 특성과 전하 트랩핑 특성의 연관관계 분석을 진행하였다. 먼저 온도에 따른 탄소나노튜브 트랜지스터의 전달 곡선 분석을 통하여 활성화 에너지 (E_a)를 추출해 보았고, 그 결과 탄소나노튜브 트랜지스터의 전하 이동 특성은 제작 공정 중에 생긴 잔여 이온이나 절연 막 결함에 큰 영향을 받지 않는다는 사실을 알 수 있었다. 추가 분석을 위해 온도에 따른 탄소나노튜브 전하 농도 (n) 및 트랩 농도 (N_t)를 추출하였는데, 온도에 따른 전하 농도 (n)와 트랩 농도 (N_t) 변화 추이가 아주 유사하다는 사실에 기반하여 탄소나노튜브 트랜지스터에서 트랩핑이 일어나는 주된 원인은 탄소나노튜브에서 주변 절연층으로의 전하 주입이라는 것을 알 수 있었다. 조금 더 심도 있는 분석을 위해 과도 상태 분석이 이루어 졌다. 먼저 측정 회로에 의한 신호 왜곡이 없도록 가변 저항 값을 최소화 하여 탄소나노튜브 채널 내의 고유한 저항-커패시터 시 상수 (τ) 값을 추출했다. 다음으로, 탄소나노튜브의 트랩핑 효과가 탄소나노튜브 트랜지스터의 과도 상태 신호에 어떠한 영향을 주는지 분석하기 위해 실험식을 유도 했다. 실험식을 과도 상태 신호에 피팅 함으로써 과도 상태 시간 (t_{tr})을 추출할 수 있었으며, 이를 이용하여 온도에 따른 전하이동도를 추출하였다. 과도 상태 분석을 통해 추출된 온도에 따른 전하 이동도 (μ) 변화 추이는 트랜지스터 전달 곡선에서 추출한 전하 이동도 변화 추이와 유사한 경향을 보였으며, 이는 탄소나노튜브 트랜지스터의 전하 이동 특성이 잔여 이온이나 절연층에 존재하는 결함에 큰 영향을 받지 않는다는 사실을 뒷받침

해줬다. 다음으로, 탄소나노튜브 트랜지스터 채널 고유의 저항-커패시터 시 상수(τ) 값을 이용하여 속도 분포도를 추출하였다. 추출된 속도 분포도는 실험식에 의해 성공적으로 설명될 수 있었다. 전하 농도 (n)와 시 상수 차이 값 ($\Delta\tau$)의 상관관계 또한 밝혀냈으며, 이를 통해 탄소나소튜브에서 주변 절연층으로의 전하 트래핑 효과가 전기적 특성에 큰 영향을 준다는 사실을 확인할 수 있었다. 이와 같은 과도 상태 분석을 통해 각 파라미터 간의 연관 관계를 알 수 있었고, 더 나아가 얕은 트랩이 탄소나노튜브 트랜지스터의 전기적 특성에 지배적인 역할을 한다는 것을 밝혀냈다. 마지막으로 실험식에 의해 추출된 매개변수를 이론식에 대입함으로써 트랩핑 속도 또한 추출할 수 있었다.

두번째로 탄소나노튜브 트랜지스터의 S/D 접촉 특성 (탄소나노튜브/전극)이 트랜지스터의 전기적 특성에 미치는 영향에 대한 연구를 진행하였다. 탄소나노튜브 박막의 탄소나노튜브 밀도를 높이게 되면 S/D 전극 간의 접촉 영역을 높일 수 있으므로 탄소나노튜브 트랜지스터의 접촉 저항 값을 줄일 수 있다. 하지만 너무 높은 밀도를 가지는 탄소나노튜브 박막은 탄소나노튜브 간의 엉킴을 야기하게 되며 이렇게 엉킨 탄소나노튜브는 탄소나노튜브 박막의 전도도를 너무 높게 만들어 트랜지스터의 점멸 비 (I_{on}/I_{off}) 특성을 좋지 않게 만든다. 따라서 탄소나노튜브 트랜지스터의 접촉 저항 특성은 점멸 비 (I_{on}/I_{off}) 특성과 트레이드-오프 (trade-off) 관계에 있다. 이를 개선시키기 위하여 그래핀 S/D 전극을 도입하여 탄소나노튜브 트랜지스터를 제작해 보았으며, 그에 대한 비교 군으로

팔라듐을 S/D 전극으로 이용한 탄소나노튜브 트랜지스터를 제작하였다. 먼저 그래핀이 S/D 전극으로 사용되기에 적합한지 판단하기 위해 그래핀의 박막 특성 분석이 이루어졌다. 광학 현미경, 원자 현미경, 전자현미경, 라만 분석이 이루어 졌으며, 이를 통해 우리가 제작한 그래핀 박막은 지름 ~ 100 μm 의 그레인과 지름 ~ 1 μm 그레인이 혼합된 형태로 존재함을 알 수 있었다. 스케일링 분석을 통해 그래핀이 낮은 면저항을 가짐을 확인하였으며, 탄소나노튜브 트랜지스터의 S/D 전극으로 사용되기에 적합하다는 사실을 확인하였다. 또한 그래핀과 팔라듐의 일 함수 추출을 통해 그래핀의 일 함수가 팔라듐의 일 함수에 잘 맞춰 짐을 추가로 확인하였다. 탄소나노튜브가 증착되어지는 박막의 표면 에너지는 탄소나노튜브의 증착 특성에 큰 영향을 줄 수 있으므로 탄소나노튜브가 증착되어지는 박막의 표면 에너지 특성 분석과 그에 따른 탄소나노튜브 박막 분석이 이루어졌다. 그 결과, 그래핀을 전극으로 사용함으로써 트랜지스터 채널 내의 탄소나노튜브 농도를 증가 시킬 수 있음을 확인하였다. 마지막으로 탄소나노튜브 트랜지스터의 전기적 특성 분석이 이루어졌다. 전달 곡선 분석을 통해 그래핀을 S/D 전극으로 이용하여 탄소나노튜브 트랜지스터를 제작할 시 대조 군에 비하여 높은 전하 이동도 (μ)와 점멸 비 (I_{on}/I_{off})를 가짐을 확인할 수 있었다. 추가적인 전하 이동 특성과 접촉 저항 특성 분석을 위해 스틱 퍼콜레이팅 시스템 분석과 스케일링 분석이 이루어졌다. 스틱 퍼콜레이팅 시스템 분석을 통해 그래핀을 S/D 전극으로 사용한 탄소나노튜브 트랜지스터는 오믹(ohmic) 도체

특성을 가짐을 확인 할 수 있었다 (m = 1). 하지만 이러한 결과는 채널이 상대적으로 긴 트랜지스터 상에서의 전기적 특성 분석이므로 접촉 저항이 트랜지스터의 전기적 특성에 미치는 영향이 작았기 때문일 수 있다. 따라서 스케일링 분석법을 이용하여 추가적으로 접촉 저항 및 채널 저항에 대한 분석이 이루어졌으며, 그래핀을 S/D 전극으로 사용할 경우 상대적으로 작은 접촉 저항을 가지는 탄소나노튜브 트랜지스터를 제작 할 수 있음을 확인하였다.

주요어: 탄소나노튜브, 트랩핑, 과도 상태 분석, 실험식, 그래핀, 소스/드레인 접촉

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