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Control of Charge Pathways for Performance Improvement of Organic Photo-Transistors

유기 광트랜지스터의 광반응 향상을 위한 전하 이동 경로 제어

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공과대학 전기·컴퓨터공학부

박 혜 림

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Abstract

Control of Charge Pathways for Performance Improvement of Organic Photo-Transistors

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Organic photo-transistors (OPTs) have attracted the growth of interest as fundamental building blocks for optoelectronic systems adopting light as an information carrier. The OPT is a type of optical transducer where the functions of light detection, switching, and signal amplification are integrated into a single device. In addition to the intrinsic advantages of organic materials such as low cost, mechanical flexibility, and chemical versatility, the OPTs exhibit higher photosensitivity and signal-to-noise ratio than two-terminal organic photodiodes owing to the signal amplification capability by the field effect. Due to the advantages, they have widespread technological applications, from telecommunications to sensors in industrial, medical, and

civil environments such as information processing, X-ray medical imaging, and position detection.

In terms of the operation of the OPTs, charges are accumulated and transported within the first few monolayers of the organic semiconductor (OSC) films adjacent to the gate dielectric surface due to the bias of the third terminal and then extracted to the drain, contributing to the output signal. As flowing in the channel, the charges interact with surrounding conditions and all of the interactions are reflected in output signals. In this regard, the charge pathways play a critical role in determining the performance of the OPTs. Especially for the planar type OPTs, since the charges laterally transport along the OSC/gate insulator interface from the source to the drain electrodes, the performance of the device is highly affected by the interfacial characteristics at OSC/gate insulator. It is important to obtain understanding of the relationship between the interfacial characteristics of the gate insulator and the charge carrier dynamics of the OPTs under light illumination. Another issue is on the restriction of unnecessary charge path to reduce the leakage current in the OPTs. The leakage current is regarded as noise which deteriorates the photoresponse of the OPTs. In this regard, patterning processes of OSC layers are required. Particularly for the vertical-type OPTs, the devices suffer from high leakage current from the source to the drain which cannot be controlled by the gate bias and exhibit considerable current flow even in off state.

This thesis primarily aims to demonstrate control of charge pathways for improvement of photoresponse in OPTs which are categorized into the planar and the vertical types.

Firstly, the enhanced optical memory effect of OPTs based on polymer gate insulator is demonstrated by investigating the effect of the interfacial properties between a polymer dielectric and an OSC layers on the photoresponse properties of OPTs. The type and the density of functional group of the dielectric material were found to more dominantly govern the optical memory effect of the OPT than the morphological effect. They can be properly tailored for specific applications of the OPTs ranging from optical memory to optical sensing devices.

Secondly, photosensitivity was improved through the solution-based patterning of OSC layers. The OPTs based on small-molecule OSC/polymer blends suffer from relatively high off current and thus low photosensitivity due to undesirable current pathways over a whole substrate. By using selective contact evaporation printing based on wetting difference, high-fidelity patterns were obtained and the patterned OPTs exhibited the improved photosensitivity due to the reduction of parasitic leakage current.

Lastly, vertical OPTs with reduced off current was developed using a self-aligned source insulator on the source electrode. The protruded part of the self-aligned source insulator blocked the considerable current flowing from the edge of the source to the drain in the off state and thus the optimized OPTs exhibited high photosensitivity. In addition, the devices showed higher photoresponsivity in comparison with the planar types due to the short channel length of the thickness of the OSC layer. With the fabrication method demonstrated here, source insulator coverage can be precisely controlled and thus the devices can be highly integrated.

In summary, control of charge pathways is investigated for improvement of photoresponse in the OPTs within the framework of the interfacial phenomena involved in different layers and the development of the novel structure. The work presented in thesis is expected to open a new route to the delicate interfacial modification of multi-layers and the integration of basic building blocks for constructing advanced optoelectronic systems.

Keywords: Organic photo-transistor, Photosensitivity, Optical memory, Leakage current, Vertical structure, Dielectric/organic semiconductor interface

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Chapter 1. Introduction

1.1. Organic field-effect transistors

Organic field-effect-transistors (OFETs) have attracted enormous attention due to low cost, light weight, flexibility, and versatile modification of material properties via molecular design [1, 2]. For commercialization of OFETs, considerable research efforts to satisfy the industrial figures of merit have been performed over the past decades, including the synthesis of organic semiconductors with high mobility and stability, the modification of interfaces, and the development of fabrication processes [3]. In addition, there have been other attempts to seek unique applications of OFETs which are irreplaceable by other electronics. The functional OFETs such as phototransistors, light-emitting transistors [4], bio-sensors [5], and memories [6] are considered as pomising candidates in that they can take full advantages of the simple modification of material properties through molecular deisgn. They are commonly achieved through the incorporation of organic functional materials into the OFETs to give specific functionalities [7].

As shown in Fig. 1.1, typical OFETs are composed of several stacks of layers including gate electrodes, gate dielectric layers, organic semiconductor (OSC) layers, and source/drain electrodes [8]. In the OFETs, there are several interfaces between two different stacking layers such as dielectric/OSC and electrode/OSC interfaces. The contacting interfaces as well as the intrinsic

properties of each layer highly affect the performance of OFETs. In the functional OFETs, the materials that are able to emit light or sense the change of environmental conditions are used in the intrinsic layers, blended in certain layers, or inserted at the interfaces [9].

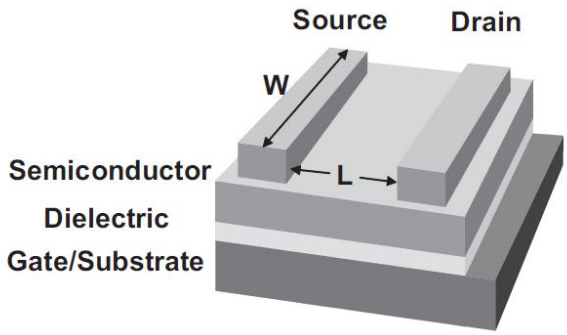

Figure 1.1. Schematic structure of a typical OFET. *L* and *W* denote the channel length and width, respectively.

The operation principle of OFETs is as follows. Depending on the gate voltage, OFETs can be modulated between on and off states. In the case of p-type OSCs, when the negative gate voltage is applied for on state, holes are injected from the source electrode into the OSC layer and accumulated within the first few monolayers of the OSC films adjacent to the gate dielectric surface. With the source-drain voltage, holes in the channel transport from the source to the drain electrodes, generating the current flow. For the n-type OSCs, electrons are majority carriers and the positive gate voltage should be applied for on state [10]. From the charge path, it can be implied that, in the

process, the properties of the dielectric/OSC and electrode/OSC interfaces play a critical role in the electrical characteristics of the OFETs.

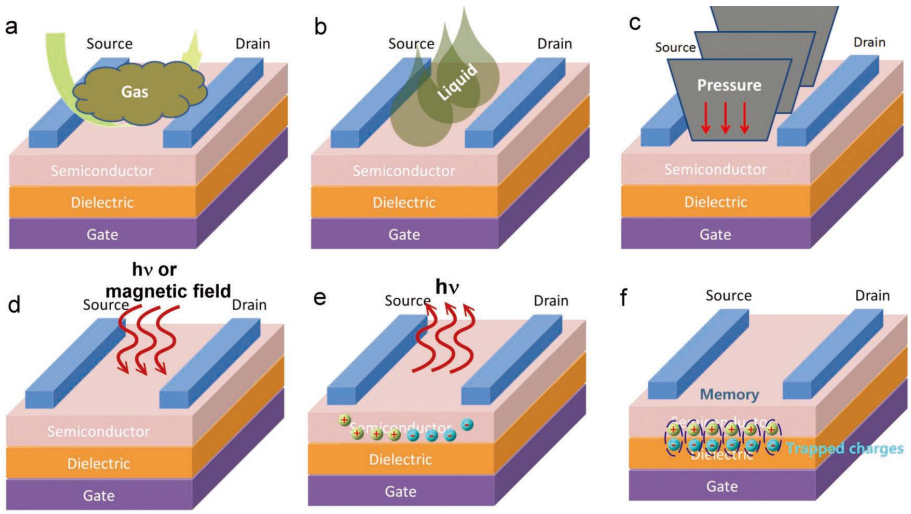

Figure 1.2. Schematic diagrams of functional OFETs. (a) Gas sensor, (b) liquid sensor, (c) pressure sensor, (d) phototransistor and magnetic field-effect OFETs, (e) light-emitting transistors, and (f) memory cell (Ref. [11]).

Among various kinds of functional OFETs, this thesis is focused on phototransistors where optical functionalities are incorporated into conventional transistors.

1.2. Organic photo-transistors

Organic photo-transistors (OPTs) are three-terminal organic optoelectronics where the incident light acts as the external electrode to tune the electrical signal. In a single device, the functions of light detection, switching, and signal amplification are integrated. In addition to the advantages of organic electronics such as low cost and flexibility, the OPTs exhibit higher photosensitivity and signal-to-noise ratio than two-terminal organic photodiodes since the gate electrode, being the third terminal, enables to accumulate charge carriers at the dielectric/OSC interfaces, resulting in the amplification of output signals [12, 13].

Operating principles of the OPTs under the dark condition are the same with the OFETs, because the structures are based on the OFETs. Under the light exposure, in p-type OPTs, electron-hole pairs are created and immediately divided into electrons and holes by the external electric field. The photo-generated electrons remain in the channel and photo-generated holes are extracted to the drain, contributing to the output signal [14]. As flowing in the channel, the charges interact with surrounding conditions and all of the interactions are reflected in output signals. For example, the characteristics at the dielectric/OS interface determine the amount of trapped charges at the interface under light illumination so that they should be properly tailored for specific applications of the OPTs ranging from optical memory to optical sensing devices [15]. In this regard, control of charge path

control plays a significant role in obtaining the desired performance of the OPTs and this is covered in Section 2.2, 2.3, and 2.4 in detail.

1.3. Outline of thesis

This thesis contains six chapters including this **Introduction** and **Concluding Remarks**. In **Chapter 1**, OFETs and, as one of the functional OFETs, OPTs are briefly introduced and simple operating principles largely affected by the surrounding environments are addressed. **Chapter 2** explains the background information with regard to the OFETs. At first, basic structures based on the lateral-type OFETs and the various sorts of operation parameters are demonstrated for the evaluation of the OFET performance. In order to understand the operation of OPTs demonstrated in this thesis, the basic photoresponse mechanisms, that is, the photoconductive and the photovoltaic modes are explained briefly. After that, the underlying mechanism which is related to the interfacial properties and the charge transport in organic electronics, especially the OFETs and the OPTs, are discussed. The fabrication method focusing on the solution-based patterning including transfer printing, selective contact evaporation printing (SCEP), micromolding in capillary (MIMIC), and ink-jet printing are introduced with the related fundamental physics. Lastly, the basics of vertical OFETs (VOFETs) such as the advantages and general operating principles are described. Based on fabrication methods of sources and source insulators, VOFETs are divided into two categories of photolithography and shadow mask and then each of them is explained. The scientific and engineering approaches for improving the photoresponse of OFETs are demonstrated by dividing into two major categories, one of which is focusing on the planar-

type OFETs in Chapter 3 and Chapter 4 and the other is self-aligned source insulator structure (SSIS) VOFETs in Chapter 5 which show higher photoresponse than previous structures. In **Chapter 3**, the effect of the interfacial properties between polymer dielectric and OSC layers on the photoresponses of OPTs was investigated. Three different polymer materials having different interfacial properties, poly(methyl methacrylate) (PMMA), amorphous fluoropolymer CYTOP, and poly(4-vinylphenol) (PVP), were used as gate insulators for the OPTs. For the trapping and detrapping processes of minority carriers, the physicochemical nature and the density of functional group of the dielectric material were found to more dominantly govern the photoresponsive properties of the OPT than the morphological effect. In **Chapter 4**, we demonstrated the effect of ultraviolet ozone (UVO) treatment of a polydimethylsiloxane (PDMS) stamp on the pattern fidelity of a 6,13-bis(triisopropylsilylethynyl) pentacene (TIPS-PEN) film when using selective contact evaporation printing where parts of a TIPS-PEN film in contact with a patterned PDMS stamp were absorbed into the nanoporous PDMS, generating patterns complementary to PDMS patterns. In addition, through the formation of OSC patterns, the photosensitivity was improved due to the reduction of the off-current level. For the case of the untreated, hydrophobic PDMS surface, the TIPS-PEN patterns developed initially were shrunken and eventually disappeared after 24 h due to the steady absorption of the TIPS-PEN in time. In contrast, UVO-treated PDMS stamps for 30 min were our best optimized point of UVO treatment for high pattern fidelity. They produced best-replicated patterns in both height and width as desired and,

interestingly, maintained the initial patterns even after 24 h, since the absorption of the TIPS-PEN was limited by the hydrophilic nature of the UVO-treated PDMS. The patterned TIPS-PEN layer by the SCE was implemented into the OPTs to demonstrate the viability of the SCEP combined with the UVO treatment for solution-processed organic electronic devices. As a result, we obtained the device with the improved photosensitivity through UVO-aided SCEP patterning method. **Chapter 5** consists of a novel structure of vertical OPTs based on the self-aligned source insulator on the source electrode. Here, the structure was optimized by controlling the duration of wet-etching time and thus changing the length between the source and the source insulator. The protruded part of the self-aligned source insulator blocked the considerable current flowing from the edge of the source to the drain in the off state and thus greatly reduced the off-current level. Besides, the optimized device had the short channel length which is the intrinsic properties of vertical type devices. For the reasons, the optimized OPTs exhibited high photosensitivity which was originally difficult to achieve in vertical-type OPTs due to intrinsic high-off current. In addition, the devices showed higher photoresponsivity in comparison with the planar types. The optimized structure of OPTs is applicable for constructing highly photosensitive devices. Finally, **Chapter 6** provides the summary and the concluding remarks.

Chapter 2. Background Information

2.1. Basics of organic field-effect transistors

In this section, the basic structures, the operation, and the photoresponse mechanism of OFETs are covered. The basic structures are only focused on the lateral-type OFETs and the four types of structures are introduced in **Section 2.1.2.** For the evaluation of the OFET performance, the various sorts of operation parameters are represented in **Section 2.1.2**. Lastly, the photoresponse mechanisms of the OFETs are categorized into two, that is, the photoconductive and the photovoltaic modes and they are explained in **Section 2.1.3**. In addition, the parameters related to the photoresponse such as photoresponsivity and photosensitivity are introduced.

2.1.1. Structures

As shown in Fig. 2.1, the structures of lateral OFETs are classified into four types based on the relative position among multilayers [16]. If the gate is positioned on the top of the OSC layer, it is called top gate structures and if the gate is in the bottom, it is called bottom gate structures. In addition, based on the contacts of the source/drain electrodes with the OSC layers, structures are categorized into two types: the top contact and the bottom contact structures. The electrodes contacting on the top of the OSC layers correspond

to top contact structures and the structures with the electrodes in the bottom of the OSC layer are called the bottom contact.

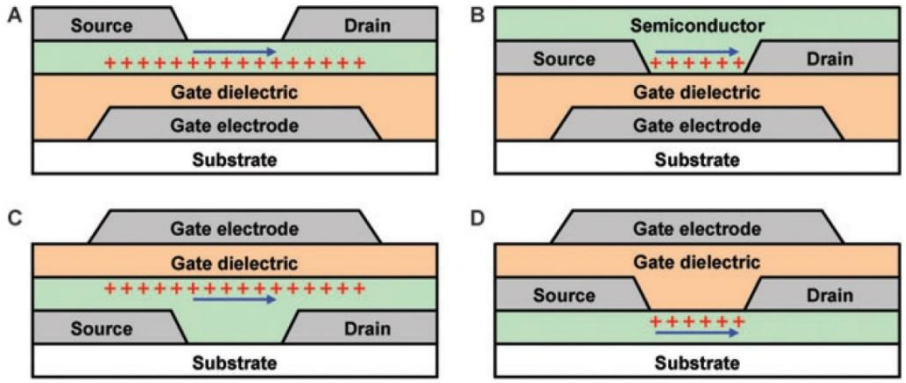

Figure 2.1. Device structures of lateral OFETs. (a) Bottom-gate top-contact, (b) bottom-gate bottom-contact, (c) top-gate bottom-contact, and (d) top-gate top-contact configuration (Ref. [16]).

All of structures have their own cons and pros. In Figs.1(c) and (d), the top gate structures show more stable operation due to self-encapsulation of the OSC layer with the gate insulators but the OSC layers usually suffer from the contaminations and defects due to depositing gate metal at the high temperature. On the other hand, the bottom gate structures are easily fabricated with the deposition of the OSC material on the insulator without creating any impairment in the OSC layer. In this regard, the bottom gate structures are preferred to the top gate structures. As for the bottom and top contacts, the source and drain electrodes are easily patterned through typical photolithography in the bottom structures. However, this process cannot be

applied to the top contact structures since the OSC layers are damaged by the photoresist and ultra-violet (UV) light during the photolithography process. Usually, patterning by shadow mask is used for the top contact structures, resulting in the relatively large channel length. In the viewpoint of contact resistance, the top contact structures show lower resistance than bottom contact structures [17].

2.1.2. Operation

Silicon metal-oxide-semiconductor field-effect transistors (MOSFETs) are operated in inversion mode where the drain current is caused by the transport of minority carriers, while the OFETs are operated in accumulation mode where the majority carriers make current flow in the devices. Like this, although the transport physics in OFETs is different from that in silicon MOSFETs, the current–voltage characteristics are described with the same formalism. The drain current (I_D) in the linear regime where $|V_{GS}\text{-}V_{th}| > |V_{DS}|$ is given by [16]

$$I_D = \frac{\mu C_i W}{L}\left\{(V_{GS} - V_{th})V_{DS} - \frac{{V_{DS}}^2}{2}\right\} \quad (2.1)$$

where μ is the field-effect mobility, C_i the capacitance of a gate insulator per unit area, L and W the length and the width of channel, respectively, V_{GS} the gate voltage, V_{th} the threshold voltage, and V_{DS} the drain voltage. The drain current in the saturation regime where $|V_{DS}| > |V_{GS}\text{-}V_{th}| > 0$ is given by [16]

$$I_D = \frac{\mu C_i W}{2L}(V_{GS} - V_{th})^2 \quad (2.2)$$

To improve the value of I_D, the value of L is required to be short, W to be large, and C_i to be high. From the equation of $C_i = \varepsilon/d$ where ε is the dielectric constant and d is the thickness of an gate insulator, insulating materials with high value of ε are used for forming the thin films (the small value of d) of gate insulator layer without any detrimental effect on leakage current.

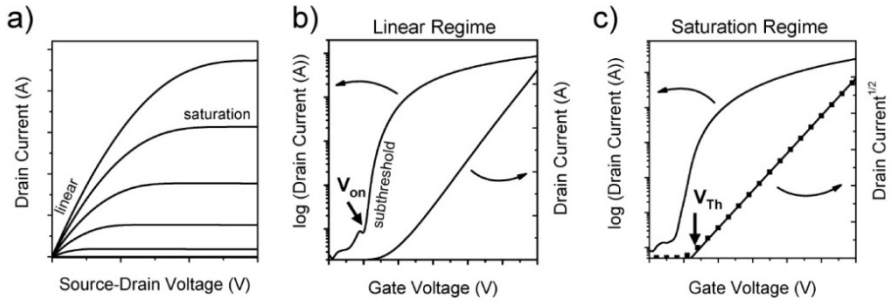

Figure 2.2. Current-voltage characteristics of n-type OFETs. (a) Output curves indicating the linear and saturation regimes. (b) Transfer curves in the linear regime, indicating the onset voltage (V_{on}) when the drain current increases abruptly. (c) Transfer curves in the saturation regime, indicating the threshold voltage (V_{Th}), where the linear fit to the square root of the drain current intersects with the x-axis. (Ref. [18]).

In Figure 2.2, the output curves and the transfer curves of n-type OFETs are represented. The transfer curves and the output curves show the drain current as a function of the gate voltage and drain voltage, respectively. Operation parameters including V_{on}, V_{th}, on/off current ratio (I_{on}/I_{off}), subthreshold swing (SS), and μ are extracted from the transfer curves to evaluate the electrical performance of the OFETs. From Fig. 2.2(b), V_{on} is the

gate voltage where the drain current begins to increase abruptly. V_{th} is the intersection of the extrapolating line of the square root of the drain current and the gate voltage axis as in Fig. 2.2(c). I_{on}/I_{off} is the ratio of the maximum drain current (I_{on}) and the minimum drain current (I_{off}). *SS* is the inverse value of slope of the logarithmic drain current. From Eqs. (2.1) and (2.2), μ in the linear and the saturation regimes can be derived by the following equation [19].

$$\mu = \frac{L}{WC_i V_{DS}} \frac{\partial I_D}{\partial V_G} \quad \text{(for the linear regime)} \tag{2.3}$$

$$\mu = \frac{2L}{WC_i} \left(\frac{\partial \sqrt{I_D}}{\partial V_G} \right)^2 \quad \text{(for the saturation regime)} \tag{2.4}$$

2.1.3. Photoresponse mechanism

During the light exposure, two effects are observed in the OFETs: the photovoltaic and the photoconductive effects [20].

For p-type OFETs, under the light, the electric field by the gate electrode facilitates the spatial separation of photo-generated electron–hole pairs. Since both source and drain contacts are hole-selective, the photo-generated electrons remain in the channel while the photo-generated holes are extracted at the drain. The electrons in the channel are accumulated and trapped at the dielectric/OSC interfaces by electron capturing sites such as hydroxyl groups of silicon dioxide (SiO_2) and other sources. The trapped electrons at the interfaces result in a shift in threshold voltage. This is called photovoltaic effect which is dominant when the devices operate in accumulation ($V_{GS} < V_{th}$).

Here, the trapped electrons cause more holes to be injected even after the light illumination stops. The lifetime of these trap states may be as long as days. These electrons can be de-trapped through the negative gate bias resetting the OFETs. Thus, the OFETs dominantly exhibiting photovoltaic effect with exceptionally long trap state lifetimes are considered as optical memory devices [14, 20].

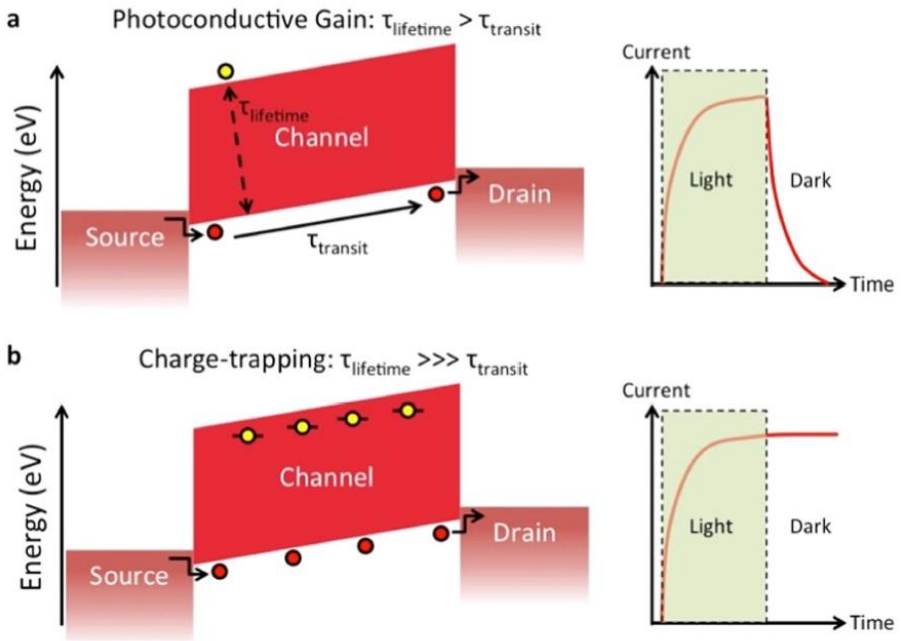

Figure 2.3. Energy band diagrams (left) and dynamic response curves (right) of OFETs with (a) photoconductive and (b) photovoltaic mode. Holes are red and electrons are yellow dots (Ref. [14]).

When the devices operate in the depletion ($V_{GS} > V_{th}$), I_D increases proportionally to the optical power due to the increased carrier mobility or the

carrier density. The situation is similar to two-terminal devices, but with the additional gate terminal enhancing photogeneration. This is called photoconductive effect. The OFETs often operate both in the photoconductive and the photovoltaic effects because both of them are related to the lifetime of minority carriers with different time scales [14, 20].

In addition to the typical parameters of the OFETs such as μ, V_{th}, and SS, photosensitivity (P) and photoresponsivity (R) are used to evaluate the photoresponse of the OFETs. They are defined as follows [21].

$$P = \frac{I_{ph}}{I_{d,dark}} = \frac{I_{d,ph} - I_{d,dark}}{I_{d,dark}} \tag{2.5}$$

$$R = \frac{I_{ph}}{P_{opt}} = \frac{I_{d,ph} - I_{d,dark}}{P_{opt}} \tag{2.6}$$

where I_{ph} is the source-drain photocurrent, $I_{d,ph}$ and $I_{d,dark}$ are the drain current in the dark and under the illumination, respectively, and P_{opt} the incident optical power.

2.2. Interfaces in organic photo-transistors

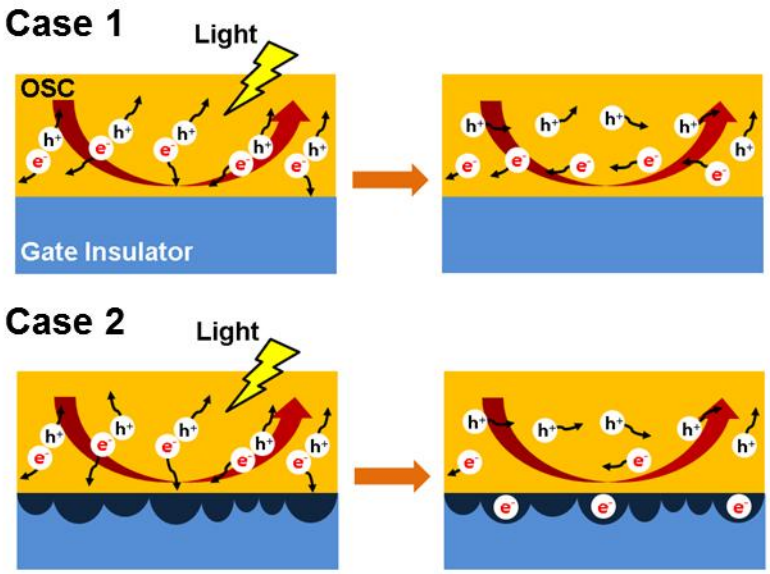

Figure 2.4. Schematic diagram of photo-response in the OPT with low trap density (Case 1) and high trap density (Case 2) at dielectric/OSC interfaces.

As shown in **Chapter 1**, electrical performances of OFETs are closely related to the interfacial characteristics of dielectric/OSC and electrode/OSC layers. Especially, the interfacial properties of dielectric/OSC layer influence gate bias stress effects such as the decrease of current with operation time and the hysteresis of device characteristics. A large number of studies have been conducted on the relationship between the gate bias stress effect and the interfacial properties. The interfacial affecting factors at the dielectric/OSC layers were found to be the molecular weight and chain end group of dielectric material, the surface roughness, the surface energy, and so on [22,

23]. Similarly, in the OPTs, there have been many previous studies about the relationship between the interfacial characteristics of dielectric/OSC layers and the responses of OPTs under the light irradiation [12, 13, 15, 24-27]. As schematized in Fig. 2.4, it was reported that the OPTs with relatively low trap density at the dielectric/OSC interface represented the increase of current level related to the photo-induced electron-hole pair generation with negligible trapping behavior under the light (Case 1). On the other hand, the OPTs with relatively high trap density at the interface showed trapping of photo-induced electrons which changed the performances of the OPTs such as photoswitching speed, photoresponsivity, photosensitivity, retention time of optical memory effect, and so on (Case 2). For example, D. Ma et al. improved the photoresponsivity of OPTs through the insertion of low trap density of poly(methyl methacrylate-co-glycidyl methacrylate) on SiO_2 dielectric layer [26]. Y. Qiu et al. demonstrated that introduction of low trap density of PVP and PMMA to tantalum oxide (Ta_2O_5) or adjusting the oxygen content in Ta_2O_5 changed the photoresponsivity, photosensitivity, and retention time of OPTs for the optical memory applications [24, 25]. In addition, S. Pyo et al. investigated and compared the photo-sensing properties such as photoswitching speed and the retention time of memory effect in the polymeric gate dielectrics of PVP and poly(4-phenosy methylstyrene) [28]. Like this, to design the OPTs for certain applications such as the optical switching and the optical memory, the sensing properties of OPTs depending on various kinds of interfacial characteristics should be systematically identified. However, most of the systematic investigations about the influence

of interfacial characteristics at dielectric/OSC layers on sensing properties of OPTs were targeted at the inorganic dielectric materials which were far from the advantages of OPTs including flexibility and low cost. In this regard, systematic and comprehensive studies about the relationship between the interfacial characteristics of dielectric/OSC layer and the photo-response in the polymer dielectric-based OPTs are required.

2.3. Solution-based patterning processes

For fabricating integrated circuits, patterning elements over a desired area is necessarily required. Except for the dielectric layers, all layers must be patterned. To define the channel length and width, the patterning of source and drain electrodes is essential. Because devices with short channel length exhibit high operating speed, reducing the pattern size is an important factor toward enhancing the performance of circuits [29]. The formation of gate electrode patterns can reduce the gate leakage current. During the patterning process, delicate control of alignment among different layers should be ensured for proper device function. That is, the deposition of source and drain electrodes should be placed in-line with the gate electrodes and the OSC layers. Especially, OSC layers are required to be patterned since the isolation of each element through patterning eliminates crosstalk between neighboring devices and reduces the off-current in the devices [30]. Therefore, much effort has been made toward the development of patterning methods. Among various kinds of patterning process, solution-based patterning methods have attracted much attention since they enable the mass production of devices at high throughput. Transfer printing [31, 32], SCEP [33, 34], MIMIC [35], and ink-jet printing [36] are the typical examples of solution-based approaches. However, many of them often suffer from incidental errors in patterns or inevitably involve complicated processes such as the fabrication of banks and selectively wetting regions in defining precise patterns through the photolithography and the self-assembly monolayer treatment [36-39].

2.3.1. Transfer printing

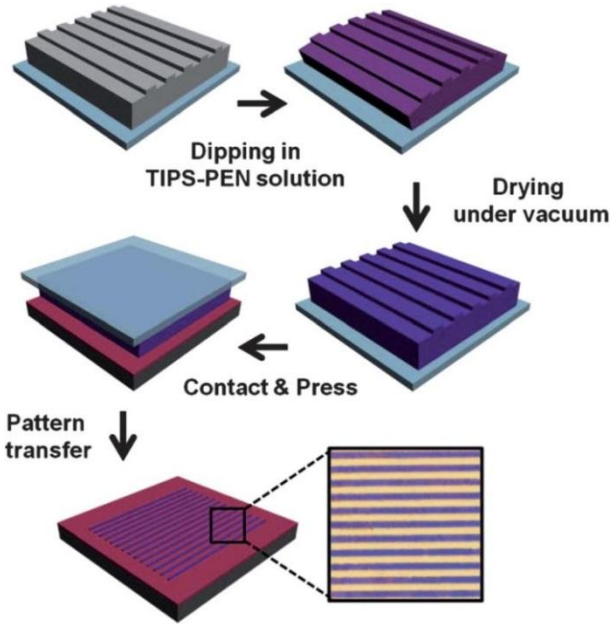

Figure 2.5. Schematic diagrams of transfer printing processes (Ref. [31]).

Transfer printing generates patterns with submicrometer lateral dimensions over macroscopic areas. The technique uses a transfer medium, usually made of PDMS, which helps transfer materials via direct contact between the material and the target substrate [40]. As stamps, elastomeric materials are commonly used to ensure conformal contact between the stamp and the receiving substrate, but rigid materials such as silicon wafers or glass can also be used. The chemical characteristics of stamps and adhesion between the transferred materials and the receiving substrate should be optimized to obtain desired patterns. For the fabrication of the stamps, PDMS

is casted onto a pre-patterned mold that is patterned by photolithography or e-beam lithography. After that, curing of the PDMS is performed at elevated temperatures. The PDMS stamp is then removed from the mold and contacted with the targeting materials. The adsorbed materials can be transferred from the stamp to the receiving substrate via contacting to the substrate, thereby reproducing the patterns encoded in the stamp.

2.3.2. Selective contact evaporation printing

At first, the pre-patterned PDMS stamps are prepared as described in **Section 2.3.1** and fully-dried thin films are formed. With conformal contact of PDMS under an appropriate pressure, the thin film is annealed at am elevated temperature. The molecules of thin films in contact with the patterned PDMS stamp are absorbed into nanoporous PDMS, generating patterns complementary to the PDMS patterns. During the process, a stamp should be in conformal contact with the thin film surface for effective heat accumulation at the contact regions, which ensures maximum temperature difference between the films exposed to air and in contact with the stamp. In addition, a mold should have sufficient free volume to allow the target molecules to diffuse into the stamps efficiently. In this regard, elastomeric PDMS is an excellent stamp material [33, 34]. From this, it can be inferred that the films with monomers or oligomers which have small volume can be patterned through this patterning method, while polymer patterns are difficult to obtain through this process.

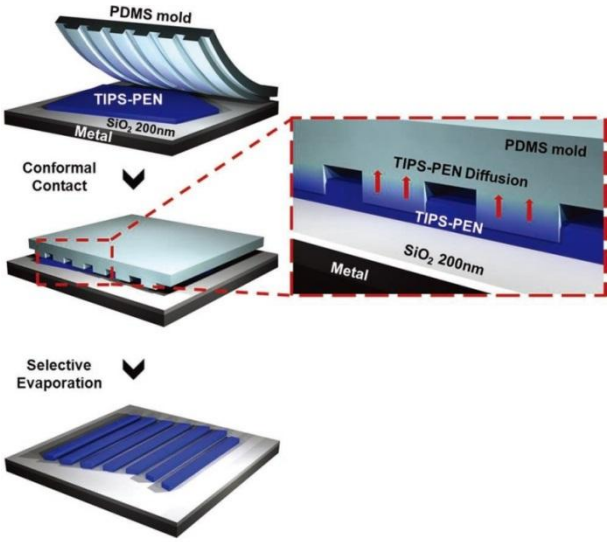

Figure 2.6. Schematic diagrams of SCEP processes (Ref. [33]).

2.3.3. Micromolding in capillary

MIMIC method is widely used to pattern soluble materials. The elastomeric stamp is usually made of PDMS and is prepared as depicted in **Section 2.3.1**. When the stamp is placed on a substrate as shown in Fig. 2.7, the grooves in the stamp form the channels. When a solution is poured at the open end of the stamp, the solution immediately fills the channels due to the capillary effect [35]. Note that the solvent should not swell the polymeric stamps. After the evaporation of the solvent, the stamp is removed, leaving the patterns on the substrate. The channel size, the concentration of the solution, and the self-organizing properties of the solute are key factors which determine the length scale achieved during the process. In addition, the rate of

infilling depends on the ratio between surface tension and the viscosity of the solution, the size of the channel, the length of the filled section of the channel, and the surface tension and friction between the solvent and the channel walls [41]. Due to the self-organization of the solute, spatially organized nanodots, wires, or crystallites can be fabricated. However, this method has drawbacks of low throughput and relatively difficult control of patterning dimension.

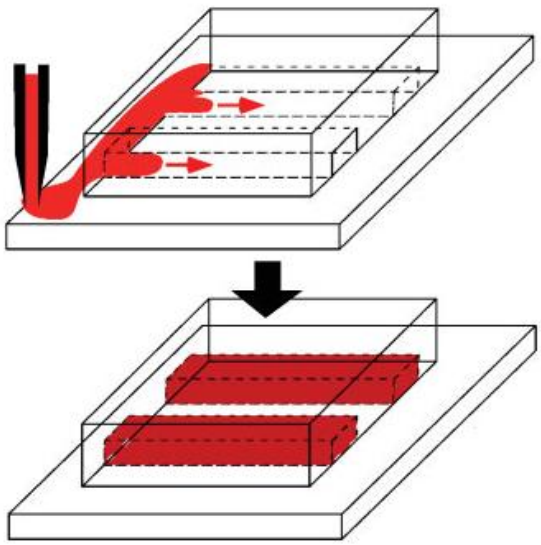

Figure 2.7. Schematic diagrams of micromolding in capillary processes (Ref. [41]).

2.3.4. Ink-jet printing

Ink-jet printing is a noncontact, additive, direct-write patterning process and regarded as an attractive patterning technique for the emerging printable electronics on a variety of substrates, being flexible and stretchable [42, 43]. It

can dramatically reduce the material waste and the production cost by ejecting ink droplets at desired areas. In ink-jet printing system, ink droplets are ejected through the nozzle orifice by vapor bubbles formed by heating a resistive element or piezoelectric transducer deformed by applying a voltage [29].

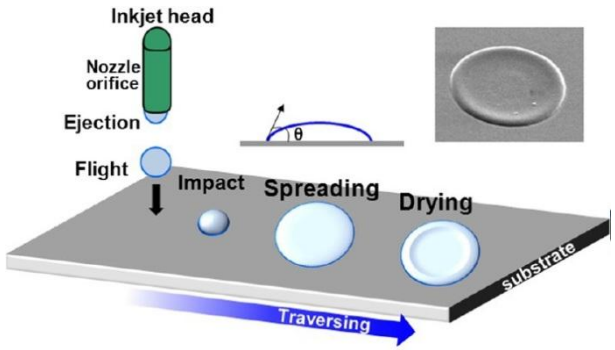

Figure 2.8. Schematic diagrams of ink-jet printing processes (Ref. [29]).

In Fig.2.8, the ink-jet printing processes are illustrated, consisting of ink ejection, flight, impact, spreading, and drying [44]. During the printing processes, it is inherently difficult to control the printed features such as morphology, edge shape, line width, and thickness due to the nature of liquid. Particularly, during the drying process, this coffee ring effect inevitably arises due to the outward convective flow within the droplets, interrupting the formation of uniform films [44, 45]. Since the printed features are highly affected by the substrate surface properties and the ink properties, the overall process should be optimized to obtain a desired pattern via ink-jet printing. Besides, ink-jet printing produces wavy patterns and has difficulty in forming

sharp and short channel length for the typical OFETs [46]. In this communication, self-alignment approaches exploiting surface wettability or bank structure has been demonstrated to achieve the high resolution and pattern fidelity. However, they involve complicated processes such as photolithography and the self-assembly monolayer treatment, which dilute the advantages of the solution-based patterning processes [36-39].

2.4. Basics of vertical organic field-effect transistors

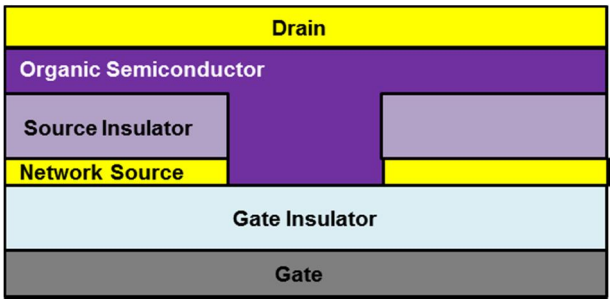

Figure 2.9. Schematic diagram of a VOFET.

It has been known that the OFETs are still very limited by low-speed, low-current level, and relatively high operational voltage mainly due to the low-mobility and high-resistivity of organic materials [47]. Especially for photoresponse which is one of the important parameters, conventional OFETs exhibit relatively low performance (photosensitivity, photoresponsivity, and response time), impeding practical use for optical sensing devices [48]. To overcome such drawbacks, much effort has been made toward the reduction of the channel length, the increase of the channel width, the fabrication of a highly-organized OSC film, and so on. However, most of existing solutions inevitably involve critical problems such as a small detection area, a complicated process, and the difficulty in integration. Finally, to solve both the low output current and the high operating voltage at once, the OFETs based on vertical configurations have been suggested [49]. In the planar configuration, the channel length is determined by the distance between

source and drain electrodes in the same plane, usually tens or hundreds of micrometer scale. Meanwhile, the channel length of the VOFET reduces down to the nanometer scale of thickness of the OSC layer, which enables a high current output at low operating voltage without any high-resolution patterning processes.

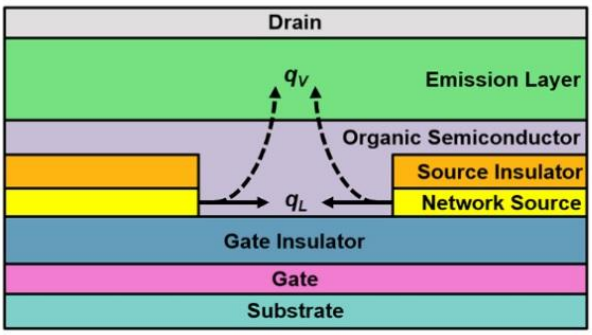

Figure 2.10. Charge flows in a VOFET. The lateral charge transport (q_L) and the vertical charge transport (q_V) are depicted as solid and dashed arrows, respectively (Ref. [50]).

As shown in Fig. 2.10, the flow of charge transport in the VOFETs is categorized into two: q_L and q_V. Like the planar OFETs, operation is based on accumulation mode. For q_L, charge carriers are injected from the source and transported within a certain horizontal distance adjacent to the gate dielectric layer near the source electrode before entering the vertical channel. After that, charges are flowed in the vertical direction, that is, perpendicular to the substrate (q_V) by the applied bias between the source and the drain [50]. Typically a source electrode with periodic vacancies, perforated electrodes, or

interdigitated electrodes have been used for the gate bias not to be shielded by source electrodes [49-51]. It should be noted that the spatial distribution of charges in the lateral direction is primarily governed by charge transport properties from each edge of the apertures in the source electrodes. Thus, the apertures of the source electrodes should be optimized in order to maximize the use of the light and obtain the high photoresponse of the VOFETs. In addition, since the charge carriers can be easily injected from the source electrode to the OSC layer, the VOFETs suffer from high leakage current from the source to the drain irrespective of the gate voltage and eventually deteriorate the on/off current ratio [52-54]. In this regard, the solutions such as the selection of the source and the OSC materials with high energy barrier and the implementation of the insulator on the source electrode are suggested. Particularly, the investigation based on the fabrication technique and the arrangement of the source/insulator structure are carried out to comprehensively understand the charge carrier behaviors and to optimize the geometrical parameters of the devices. The concept and the characteristics of the fabrication methods are explained below.

2.4.1. Photolithography

As schematized in Fig. 2.11, Kudo's group fabricated and compared two types of vertical structures in this study [53, 55]. The structure of device I has the same width between the source and the source insulators. In device II, the source electrode is separated from the insulating layer and the source

electrode is fabricated to be narrower than the source insulator. The overhang length denoted by Δ in device II represents the length from the edge of the source electrode to the edge of the source insulating layer. Note that, in the figure, the source insulating layer is named as the charge restriction layer. To fabricate the device, photoresist is used as source insulators on pre-patterned source electrodes, since it should be formed accurately at the correct position against the source electrode position. As a result, the modified device (the device II) improved the on/off ratios by over two orders of magnitude by reducing the leakage current. However, the device dimension is around a hundred of micrometer scale which is relatively high and low density, since the precise alignment of the insulator on the source electrode is difficult. In addition, as reported, the performance of the device is degraded during the resist formation because the organic materials are very sensitive to most types of solvents.

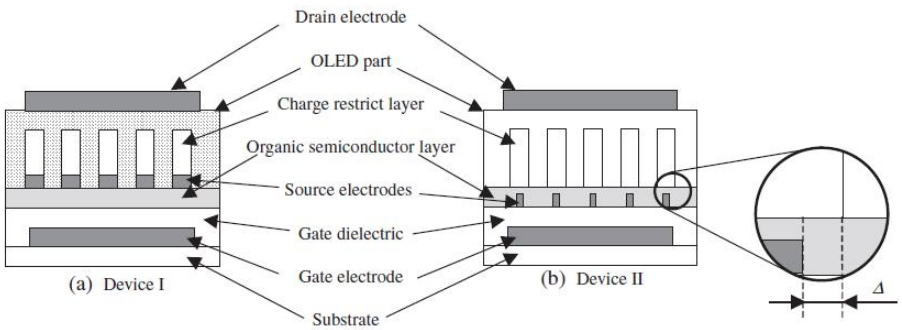

Figure 2.11. Schematic diagrams of two different vertical structures (Ref. [53]).

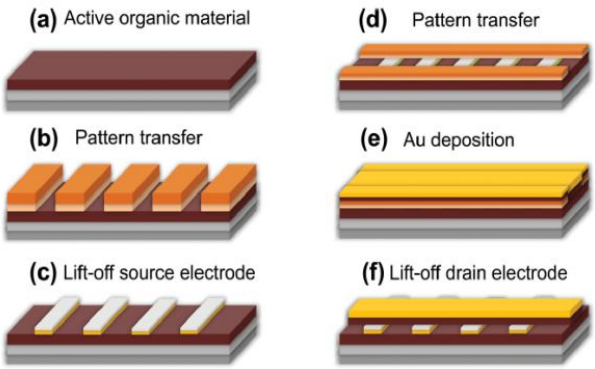

Figure 2.12. Schematic diagram of VOTFT fabrication: (a) deposition of the OSC (dark red) on the substrate (dark gray) with the gate insulator (gray), (b) pattern formation of the photoresist, (c) deposition of the source electrode (Au, yellow) and the source insulator (SiO_2, light gray) followed by lift-off of the spare material, (d) coating, exposure, development, and etching of the photoresist for the drain electrode, (e) deposition of the OSC and the drain electrode (Au), and (f) the final VOTFT device after lift-off (Ref. [51]).

To solve the problem of solvent orthogonality with the OSC layer, Hans et al., fabricated the VOFETs by photolithography using fluorinated photoresist and solvent compounds in Fig. 2.12. The materials allow photolithographical patterning directly onto the OSC layer without any detrimental effect, simplifying the fabrication protocol and enabling precisely control of important geometrical parameters of the device which is required for systematic study about the underlying physical effects of operation. Besides, it offers a new route towards a high density integration of organic electronics [51]. In spite of the advantages, it is difficult to control the arrangement of the source/insulator with various Δ, unlike the previous study

and the effect of the relative position between the source and the source insulator was not covered.

2.4.2. Shadow mask

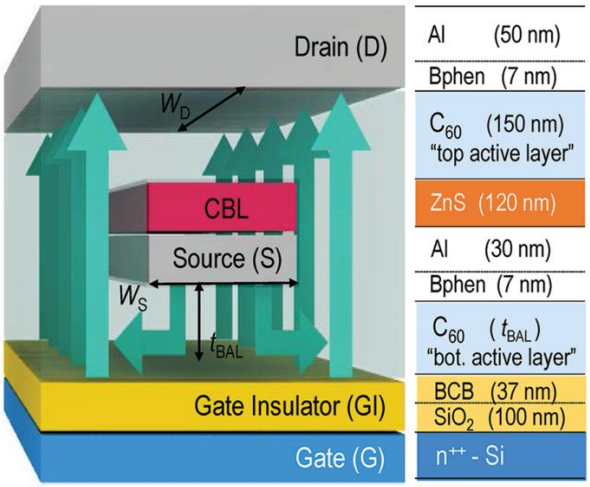

Figure 2.13. Schematic diagram of the VOFETs fabricated in Ref. [52].

In some studies, the source insulators of the VOFETs were patterned by shadow masks.

Kwon et al., as shown in Fig. 2.13, fabricated the device with the same shadow mask for both the source electrode and the source insulator (denoted by CBL in the figure). Here, they mentioned that covering not only the top side but also the edge of the source electrode with the insulator is important since the Ohmic contact between the source and the OSC makes considerable current flowing from the edge of the source to the drain even in the off state.

Thus, they recommended using a shadow mask for the source insulator with a slightly larger opening than that of the source electrode. However, it wasn't ensured that the high performance, especially on/off current ratio, of the fabricated device is due to the natural coverage during the thermal evaporation process even with the same shadow mask between the source and the insulator [52]. Moreover, through the shadow mask patterning, it is difficult to obtain the high-density integration and the precise control of insulator arrangement on the source electrode. In this study, the pattern dimension is hundreds of micro-scale.

Lee et al. suggested the vertical structure with full-covered edge of the source electrode for significant reduction of off current. For full coverage of the top and two edges of each source, oblique deposition of insulator material was performed twice to form insulator patterns on the source in such a way that the substrate was rotated by the angle of 180^{o} during the subsequent deposition as shown in Fig. 2.14 [54]. Due to the shadow mask patterning of the source insulator through oblique deposition, it has the limitation of low-density integration with hundreds of micrometer scale. Besides, oblique deposition cannot guarantee pattern fidelity and stability as designed.

At present, the research of the VOFET is still in its infancy as described previously. Thus, it is highly required to obtain a rather complete picture of the relationship between the source and the source insulator and the charge carrier dynamics. Together, effort should be poured to develop simple fabrication processes suitable for mass manufacturing overcoming disadvantages and experimental difficulties in the previous studies.

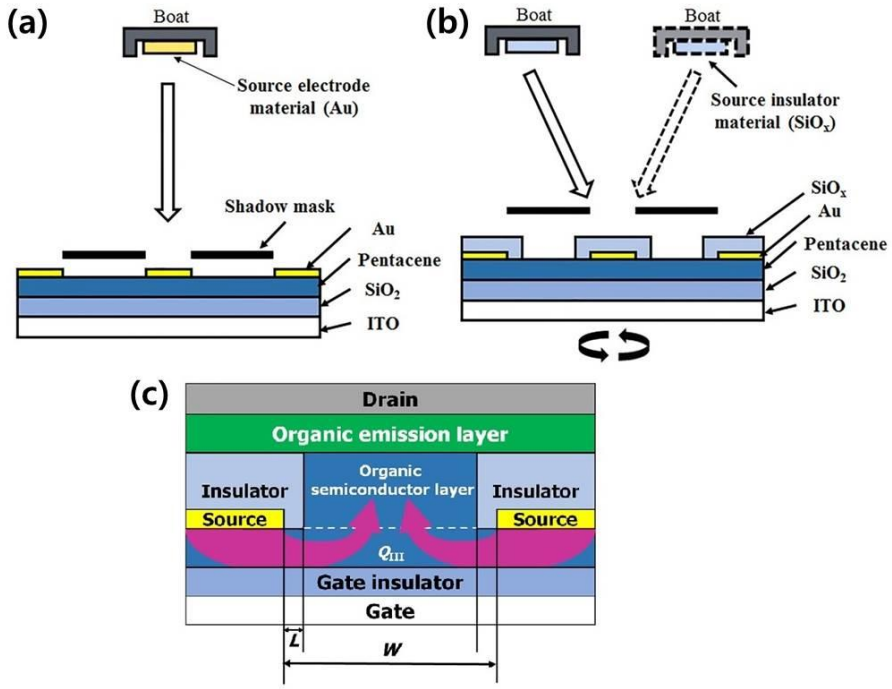

Figure 2.14. Schematic diagrams of fabrication process of (a) sources and (b) source insulators patterning and (c) the structure of the VOFET fabricated in Ref. [54].

Chapter 3. Enhanced Optical Memory Effect by Physicochemical Modification of Gate Insulator

3.1. Introduction

In OPTs, the interfacial properties of the dielectric/OSC play a critical role in the photoresponse since the transport of photo-generated charges primarily takes place within the first few monolayers of the OSC films adjacent to the interface with a gate dielectric layer as described in **Section 2.2**. In particular, the interfacial characteristics determine the amount of trapped charges at the dielectric/OSC interface under light illumination so that they should be properly tailored for specific applications of the OPTs ranging from optical memory to optical sensing devices [15, 56]. Thus, the effect of interfacial properties of dielectric/OSC layers on charge transport has been extensively investigated to understand the photoresponse of OPTs [12, 13, 15, 24-27]. Although most studies so far have focused on the OPTs based on inorganic insulators such as SiO_2 and Ta_2O_5, the effect of the interfacial properties of a polymer insulator, allowing the mechanical flexibility and low-cost fabrication process, on the photoresponse of a polymer insulator-based OPT (p-OPT) has not been fully addressed from the viewpoint of the charge trapping mechanisms involved in OFETs [57]. Therefore, the p-OPTs having different polymer insulators should be systematically investigated to

understand the delicate interplay between the interface and charge carrier dynamics.

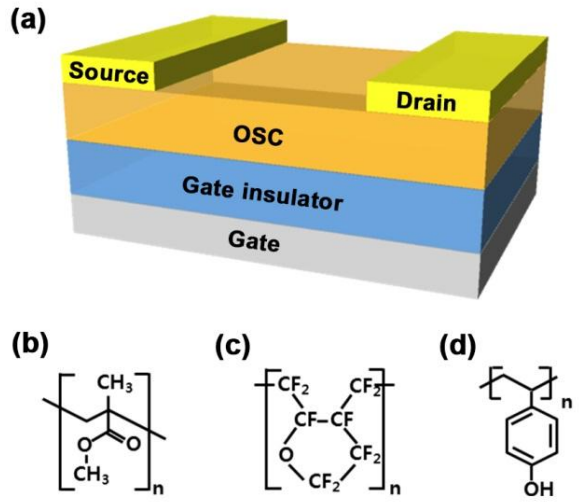

Figure 3.1. Schematic diagram of the p-OPT configuration. Chemical structures of (b) PMMA, (c) CYTOP, and (d) PVP (Ref. [58]).

In this chapter, we systematically investigated the photoresponse of the p-OPTs in terms of the morphological and the physicochemical properties at the dielectric/OSC layer including the surface roughness, the surface energy, and the functional group of the polymer insulator. Note that the surface properties are largely divided into morphological and physicochemical properties. The surface roughness is categorized into the morphological properties. The surface energy and the functional groups of dielectric layers attracting specific charges by coulombic forces are related to the physicochemical properties. In determining the effect of the dielectric/OSC interfacial characteristics on the photoresponse of the p-OPT, we used three

different polymer dielectric materials of PMMA, CYTOP, and PVP for gate insulators. The schematic diagram of our p-OPT is shown in Fig. 3.1(a). The three polymer gate insulators we used have been widely employed in organic electronic devices due to their excellent dielectric properties [59, 60]. As seen from the chemical structures in Figs. 3.1(b)-(d), PMMA has the ester group acting as a trapping site for holes [61, 62] and PVP has the hydroxyl group which dominantly traps the electrons by the electrostatic interaction [1, 23]. In contrast, CYTOP has no specific chemical group for electrical traps [63].

3.2. Fabrication of organic photo-transistors with different gate insulators

The p-OPTs were fabricated on the glass substrates with patterned indium-tin-oxide (ITO) of 165 nm thickness, being as a gate electrode. The substrates were cleaned with acetone, isopropyl alcohol, methanol and deionized water in sequence. For gate insulators, the PMMA (M_w = 996,000 g/mol, Sigma-Aldrich Korea) was dissolved in anisole at 8 wt. % concentration and the CYTOP (CTL-809M, Asahi Glass) was used as received with the concentration of 9 wt. %. Also, the PVP (M_w = 25,000 g/mol, Sigma-Aldrich Korea) mixed with poly(melamine-co-formaldehyde) (PMF) (100 wt. % of the PVP) in propylene glycol methyl ether acetate in 10 wt. % was used. To form a gate insulator of 500 nm-thick, the PMMA, the CYTOP and the PVP solutions were spin-coated at 3000 rpm for 60 s, 5000 rpm 60 s, and 3000 rpm for 30 s, respectively. After that, the PMMA and the CYTOP were annealed at 110 ^{o}C for 2 h and 100 ^{o}C for 1 h, respectively, in ambient condition to remove the residual solvent. Also, the PVP film was soft baked at 100 ^{o}C for 30 min and cross-linked at 200 ^{o}C for 50 min in ambient condition. On top of three different dielectric layers, the 50 nm thickness of pentacene was evaporated at the rate of 0.5 Å/s under the pressure of 1 × 10^{-5} Torr. Note that the mobility of pentacene (about 1 cm^2/Vs) is comparable to that of hydrogenated amorphous silicon [64, 65]. Subsequently, Au was thermally deposited through shadow mask at the rate of 1.0 Å/s under the pressure of 1

$\times 10^{-5}$ Torr to define the source and drain electrodes with the channel length of 150 μm and the channel width of 1 mm.

For the experiment of two different concentration of the PMF in the PVP dielectric layer, heavily doped p-type silicon wafers with 300-nm-thick thermally grown silicon dioxide were cleaned and coated with the concentration of 2 wt. % PVP under the same conditions for the gate insulators described above. After that, the organic semiconductor layer and the source-drain electrode were formed in the same manner as described before.

The electrical characterization of the p-OPTs was carried out using a semiconductor parameter analyzer (HP4155A, Hewlett–Packard Co.) under ambient condition. For the measurement of photoresponse, the devices were illuminated from the top side using the 365nm wavelength of UV light source (GL-155, UVSMT) at the intensity of 9 mW/cm^2. Note that pentacene-based OPTs have been widely used for detection of UV light [66-68]. The surface morphologies of dielectric layers and pentacene films were characterized by using an atomic force microscopy (AFM) (XE-100, PSIA) and the water contact angles of dielectric layers were observed through optical microscopy (Optiphot-Pol, Nikon). For the PVP films with the different ratio of the PMF, Fourier transform infrared spectroscopy (FT-IR) equipment (Tensor 27, Bruker) was used to observe the amount of hydroxyl group in the PVP film with or without PMF.

3.3. Effect of modified gate insulators on photoresponse

3.3.1. Different polymer dielectrics

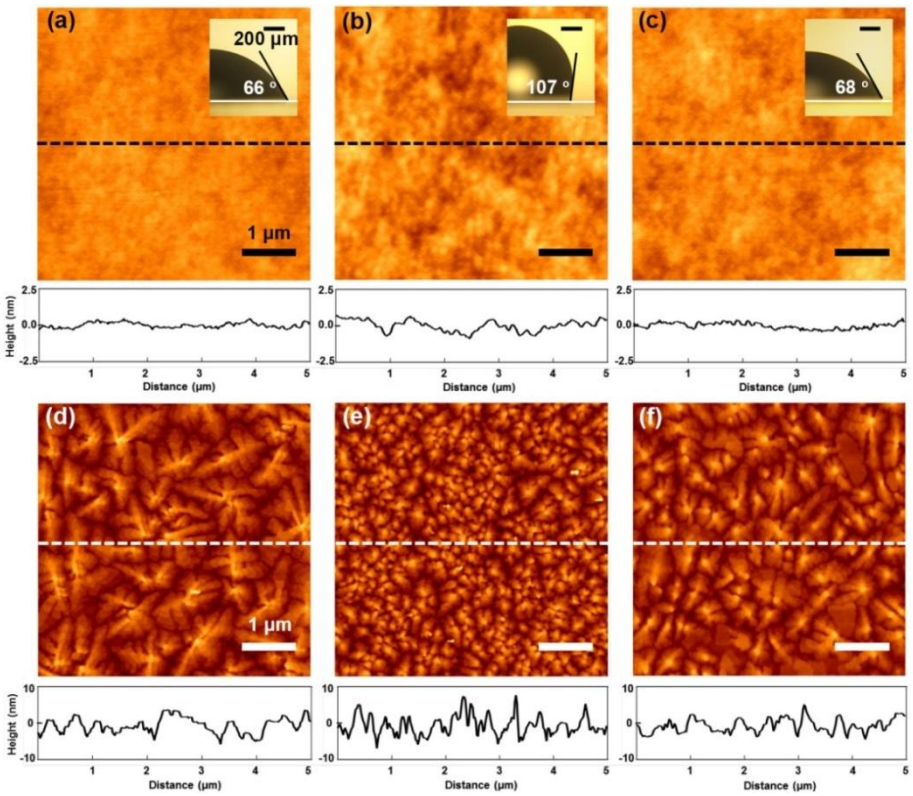

Figure 3.2. The AFM images and morphological profiles of (a) PMMA, (b) CYTOP, and (c) PVP. The contact angles of water were shown in insets. The AFM images and morphological profiles of 10-nm-thick pentacene layers on (d) PMMA, (e) CYTOP, and (f) PVP (Ref. [58]).

Before the analysis of photoresponse in three different p-OPTs, We first characterize the morphological and physicochemical properties of three different dielectric/OSC layers. Figs. 3.2(a)-(c) show the AFM images and the corresponding morphological profiles of PMMA, CYTOP, and PVP layers, respectively. From the AFM images, the values of the root mean square roughness of the PMMA, the CYTOP, and the PVP were 0.17, 0.32, and 0.24 nm, respectively. In this range of values, the roughness is known to have essentially no effect on the charge transport [61, 69]. For investigating the physicochemical properties, the surface energies of the dielectric/OSC interfaces were analyzed by the contact angle of each dielectric layer. As shown in the top insets of Fig. 3.2(a)-(c), the contact angles were 66 ^{o} on the PMMA, 107 ^{o} on the CYTOP, and 68 ^{o} on the PVP. From the contact angles, it is clear that the surface energy of the PVP and the PMMA is similar and rather hydrophilic while that of the CYTOP is relatively hydrophobic [70, 71]. Note that the surface energy of dielectric layer affects the charge transport, since the hydrophilic surfaces of the dielectric layers induce donor- and acceptor-like traps at the dielectric/OSC interfaces through the diffusion of water molecules [72]. In addition, the difference of surface energy between the OSCs and the dielectric layers will strongly influence the morphology of the OSC films grown on the polymer dielectric layers [23]. The morphologies of pentacene layers on each dielectric layer were analyzed through the AFM images of 10-nm-thick pentacene layers as shown in Fig. 3.2(d)-(f). Since the charge transport occurs only in the first few monolayers of molecules on the dielectric surface, we deposited only 10-nm-thick layers of pentacene on the

various dielectric surfaces [73]. Due to lower surface energy of the CYTOP than that of pentacene, the grain size of the OSC film on the CYTOP layer was smaller than other dielectric materials to minimize the total surface energy [17, 23]. The values of the average grain size of pentacene on the PMMA, CYTOP, and PVP layers were 0.92, 0.30, and 0.72 μm, respectively. Note that the average grain size of pentacene on the CYTOP layer was smaller than those in the other two cases. In terms of the surface energy of the dielectric layers, the CYTOP was expected to have different influence on the charge transport, compared to other two dielectric layers.

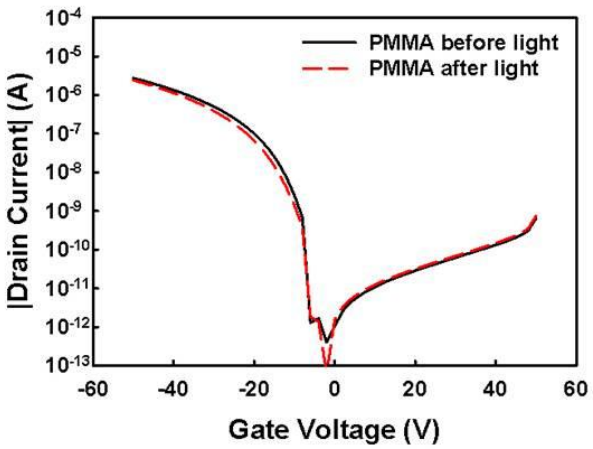

Figure 3.3. Transfer curves of the p-OPTs with the PMMA dielectric layer before (solid line) and after (dashed line) 1 min duration of light exposure at the V_D of -50 V (Ref. [58]).

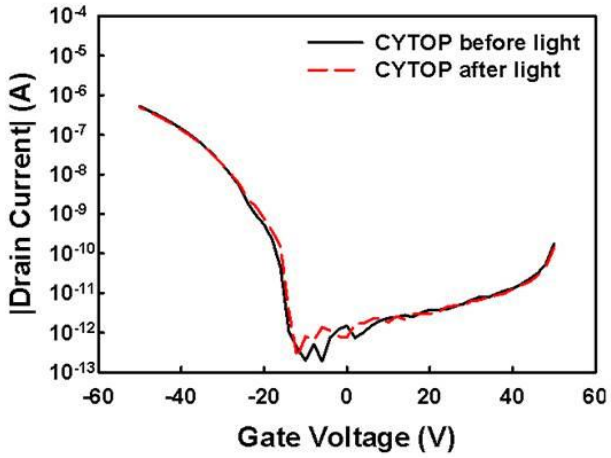

Figure 3.4. Transfer curves of the p-OPTs with the CYTOP dielectric layer before (solid line) and after (dashed line) 1 min duration of light exposure at the V_D of -50 V (Ref. [58]).

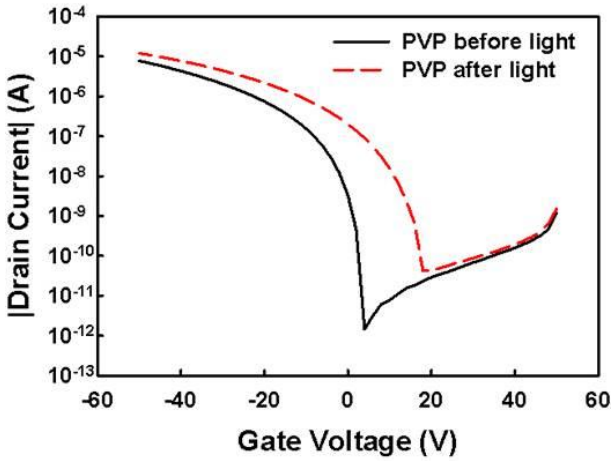

Figure 3.5. Transfer curves of the p-OPTs with the PVP dielectric layer before (solid line) and after (dashed line) 1 min duration of light exposure at the V_D of -50 V (Ref. [58]).

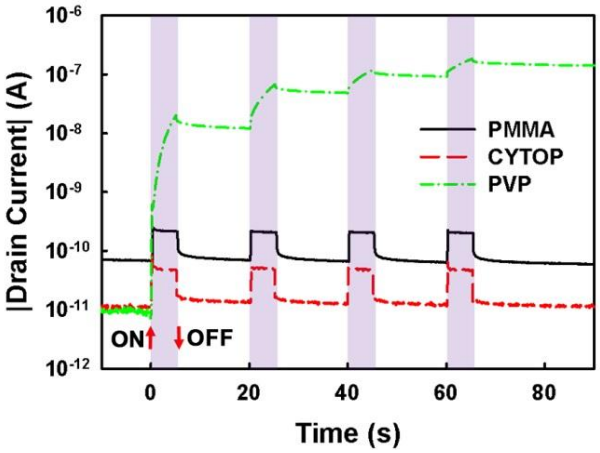

Figure 3.6. Dynamic photoresponse behaviors of three p-OPTs with PMMA, CYTOP, and PVP under periodic light illumination for 5 s during the period of every 20 s at V_D = -50 V and at $V_G = V_{on}$ (-6 V for PMMA, -12 V for CYTOP, and 4 V for PVP). The shaded areas indicate the duration of the light illumination (Ref. [58]).

We now investigate the static and the dynamic photoresponse of three types of p-OPTs. In order to observe static responses, the transfer curves of the p-OPTs with dielectric layers of PMMA, CYTOP, and PVP before and after the light exposure for one minute were represented in Figs. 3.3-3.5. Note that, in Fig. 3.4, the p-OPT with CYTOP showed a lower current level than those with PMMA and PVP, which resulted from a relatively high density of grain boundaries of the pentacene film on the CYTOP layer as clearly seen in Fig. 3.2(e). In addition, before the light illumination, the transfer curve in the PVP case exhibited a positive onset voltage (V_{on}) in contrast to the PMMA and the CYTOP cases. This is attributed to the building up of negative charges captured by hydroxyl groups at the PVP/OS interface in the presence of

oxygen and moisture [74, 75]. In Figs. 3.3-3.5, the threshold voltage shifts (ΔV_{th}) of the p-OPTs with the PMMA and the CYTOP after the light exposure were negligible values of 0.24 V and 0.02 V in the negative direction while the ΔV_{th} of the p-OPT with the PVP was a significantly large value of 10.55 V toward the positive direction. The ΔV_{th} to the positive (negative) direction under the illumination is proportional to the amount of trapped electrons (holes) at the dielectric/OSC interface [15, 22, 57]. For the PVP case, a large amount of electrons were trapped at the interface under light illumination whereas for the PMMA and the CYTOP cases, the values of ΔV_{th} were so small that the amount of trapped charges could be ignored. Here, it is implied that the amount of trapped charges under the light illumination is one of most important factors in static photoresponse.

The dynamic photoresponse of each of the three cases was measured from I_D as a function of time with the light exposure of 5 s in every 20 s period. Fig. 3.6 represents the dynamic photoresponse of the p-OPTs at the V_G of the V_{on} where the effective V_G in the three different p-OPTs is identical to zero. Here, the values of V_{on} for the PMMA, CYTOP, and PVP cases were -6, -12, and 4 V, respectively. Let us focus on the one period of light illumination. For all of the p-OPTs, the drain current immediately increases right after light exposure, which is mostly attributed to the photo-generated electron hole pairs. After that, during the light exposure (shaded areas), the drain current for the PVP device obviously increases with time while those for the others kept constant current level. It was implied that electrons were not remarkably trapped at the PMMA/OSC or CYTOP/OSC interface but largely trapped at

the PVP/OSC interface during the light exposure as in the static case. Under no light illumination, the p-OPTs with the PMMA and the CYTOP exhibited immediate recovery processes of I_D from the latest state to the initial states with the decay time on the order of hundreds of milliseconds. In contrast, the PVP device showed the persistent photo-generated current level, so called memory effect, since the long-lived electrons occupied at the interfaces built up the additional negative gate voltage [76]. This tells us that depending on the physicochemical properties of the dielectric polymer surface, the p-OPT will exhibit the persistent or reversible photocurrent. Thus, appropriate dielectric layers should be selected for desired applications. For example, the p-OPTs with the PMMA and the CYTOP, especially the CYTOP, can be applied to the optical sensors due to their reliable on-off characteristics with the periodic light exposure. On the other hand, as the photo-generated current was persistent (memory effect) as long as the voltage was applied in the p-OPT with the PVP, this can be utilized as volatile memory.

As for the surface energy, the previous studies insisted that the hydrophilicity of dielectric layers was one of the plausible causes for the different photoresponse of p-OPTs, which was not clearly verified [28]. In addition, the large difference of surface energy between the OSCs and the dielectric layers resulted in the high density of grain boundaries in OSC layers interrupting the transport of the charges as trap sites. However, in our study, the PVP and the PMMA with the large difference in the photoresponse represented the similar level of water contact angles. This leads directly to the conclusion that except for the surface roughness and the surface energy, the

functional groups of the dielectric polymers should play a significant role in the photoresponse of the p-OPT, particularly, at the interface between the OSC and the dielectric surface.

3.3.2. Functional group density

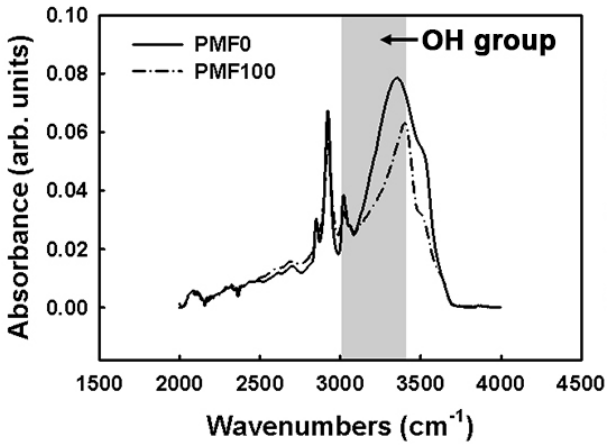

Figure 3.7. FT-IR spectra of the p-OPTs with PMF0 and PMF100 (Ref. [58]).

Lastly, the relationship between the density of hydroxyl groups and the photoresponse behaviors of the p-OPTs was investigated. The p-OPTs using PVP mixed at different concentrations of PMF were fabricated. Note that the number of the hydroxyl groups of PVP decreases with increasing PMF because the PVP molecules chemically react with hydrogen or methyl groups of PMF during annealing [77]. In the experiment, no PMF (PMF0) and PMF at the concentration of 1:1 in weight with respect to PVP (PMF100) were used

for examining the difference in the photoresponse between them. Besides, the p-OPTs with 60nm PVP coated on 300nm SiO_2 dielectric layer were examined since the PVP with the PMF0 without blocking layer of SiO_2 exhibited significant increase of off current so the dynamic photoresponse of p-OPTs could be influenced by the intrinsic current-voltage characteristics as well as the characteristics of dielectric/OSC interface.

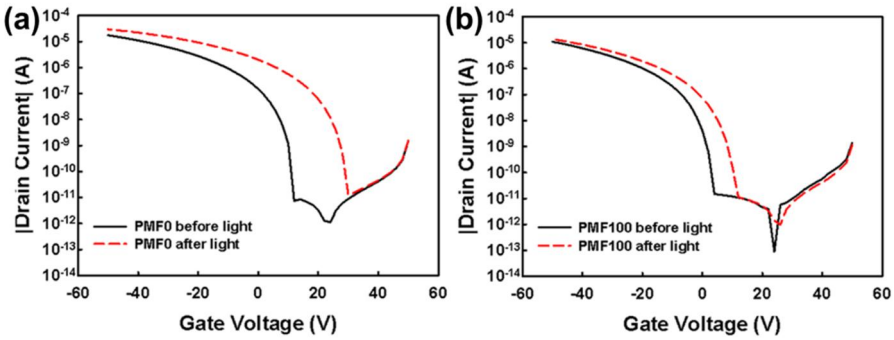

Figure 3.8. Transfer curves of p-OPTs with (a) PMF0 and (b) PMF100 before (black and solid line) and after (red and dashed line) the light illumination for 1 min at V_D = -50 V (Ref. [58]).

As we can see in Fig. 3.7, higher peaks of the PMF0 around 3000~3400 cm^{-1} in the FT-IR spectra indicated the existence of more hydroxyl groups than the PMF100. Fig. 3.8 demonstrated the transfer curves of the PMF0 and the PMF100 before and after the light illumination. After the light exposure, larger value of ΔV_{th} around 17.74 V was exhibited in the PMF0 when it compared with the PMF100 (ΔV_{th} = 6.16 V). Of course, this was caused by more hydroxyl groups in the PMF0 than that in the PMF100 as demonstrated

in Fig. 3.7. In addition, in the case of the PMF100 (60-nm thick PVP), the values of ΔV_{th} are different from the single layer of 300-nm-thick PVP (Fig. 3.5), which means the PVP bulk as well as the interface may influence on the photoresponses of the p-OPTs. As the dynamic photoresponse of the p-OPTs, Fig. 3.9 represented I_D as a function of time in the PMF0 and the PMF100 at the V_G of V_{on} with the periodic light irradiation. Note that, for the PMF0 and PMF100, the values of V_{on} were 4 and 12 V, respectively. As shown in Fig. 3.9, the graphs of I_D in linear scale during the first light exposure period were inserted to show the significant difference of increased I_D between in the PMF0 and in the PMF100 (about five times). Note that the current of the p-OPT with no PMF gradually increases with the successive light illumination in time due to the accumulative trapping of the electrons in the presence of the hydroxyl groups [75]. When the p-OPT with the PVP is utilized as the optical memory, the performance of the memory such as on-off ratio and retention time can be modulated simply by changing the amount of the PMF. Therefore, the density of the functional groups at the dielectric/OSC interface was identified as the dominant factor determining the photoresponse of the p-OPT through the trapping and detrapping processes of minority carriers. Although the charge trapping-detrapping results in the deterioration of the operational stability in the OFET case, it leads to the persistence of the photocurrent in the OPT case. In fact, the nature of the carrier dynamics of the OPT is different from that of the OFET. In other words, in the OPT, excessively photo-generated minority carriers together with the majority carriers contribute to the output current under light illumination.

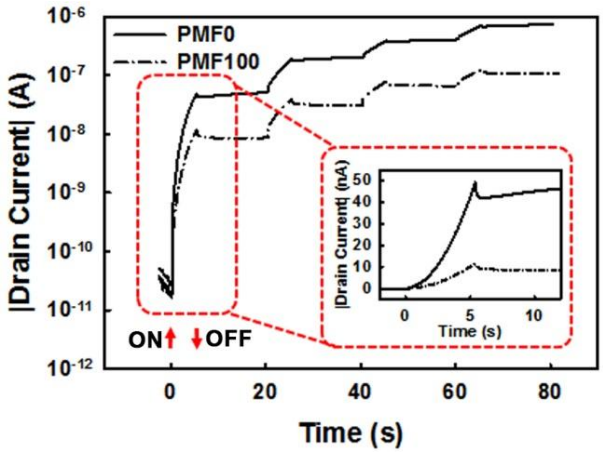

Figure 3.9. Dynamic photoresponse behaviors of p-OPTs with PMF0 (solid line) and PMF100 (dash-dotted line) at V_D = -50 V when V_G = V_{on} under periodic illumination of light. Inset shows a linear-scale plot during the first period of light illumination (Ref. [58]).

3.4. Summary

In summary, we presented a comprehensive picture of how the morphological and physicochemical properties of dielectric/OS interfaces influence on the photoresponse behaviors of the p-OPTs using three different types of polymer dielectric layers. Among the dielectric/OSC interfacial characteristics, the type and the density of functional groups of the dielectric layers is a dominant factor determining the photoresponses performance of the p-OPTs. More specifically, the hydroxyl group of the PVP trapping the electrons play a major role in the persistent photo-induced current in the PVP devices after the light whereas the PMMA and the CYTOP devices showing reliable on-off characteristics with the periodic light exposure also resulted from the functional groups of the dielectric surface not trapping the minority carriers of electrons. The molecular level approach presented here will provide a useful guideline for the selection of a suitable dielectric material, being used as a gate dielectric layer, for the desired optical applications of the p-OPTs such as an optical memory or an optical sensor.

Chapter 4. Improvement of Photosensitivity by Solution-Based Patterning of Active Layer

4.1. Introduction

Solution-processed OFETs have been extensively studied because of the printing capability over large area in simple and cost-effect ways. Particularly, among various kinds of solution-processed OSC materials, TIPS-PEN/polymer blends have attracted enormous attention due to the combined characteristics of the relatively high mobility of TIPS-PEN and the device uniformity of polymers which are prerequisites for the commercialization of the OSC-based devices [78, 79]. However, the OFETs based on TIPS-PEN/polymer blends suffer from relatively high off current and thus low photosensitivity due to undesirable current pathways over a whole substrate. In addition, to fabricate integrated circuits for practical devices, production of a patterned OSC film over a desired area is particularly essential since perfect isolation of each element through patterning eliminates the undesirable current pathways [29, 34, 80]. Therefore, there has been much effort toward the development of reliable and cost-effective methods of patterning the OSC films, for example, transfer printing [29, 31], SCEP [33, 34], MIMIC [35], and ink-jet printing [36]. However, they produce the patterns in a distorted manner or, to acquire the desired patterns, the complicated processes such as the fabrication of bank and selectively wetting region through the

photolithography and the self-assembly monolayer treatment should be involved [29, 34, 81]. Thus, investigation about the formation of high-fidelity patterns in a simple and cost-effective way is greatly required to facilitate the commercialization of OSC-based devices.

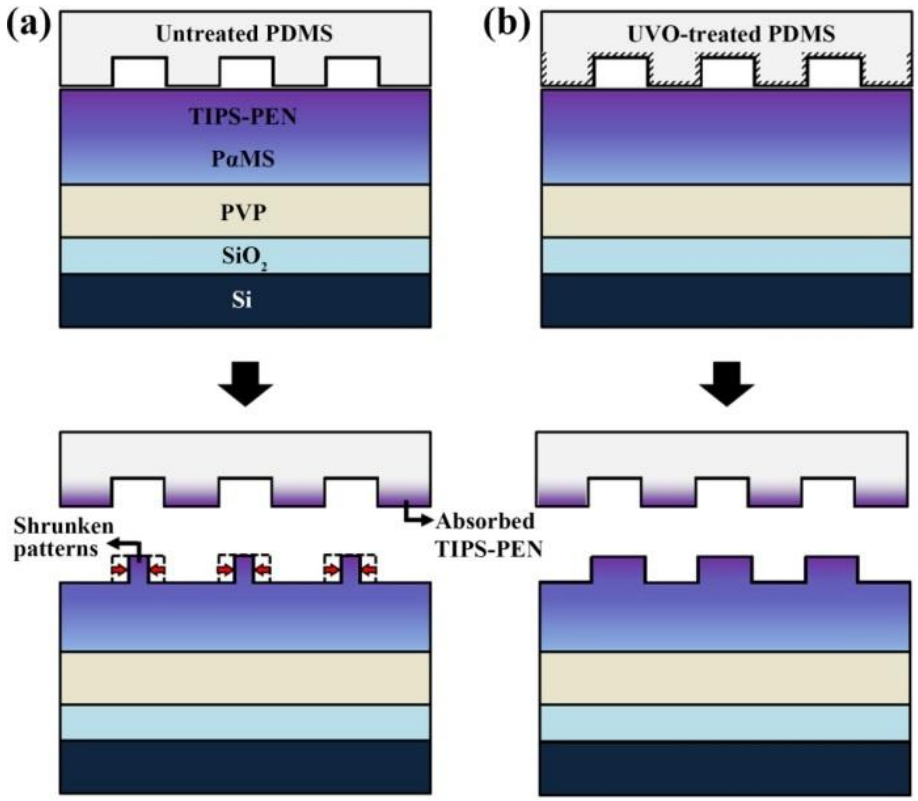

Figure 4.1. Schematic diagram showing the patterning process and the resultant patterns of the TIPS-PEN through the absorption of the TIPS-PEN monomers into (a) the untreated PDMS stamp and (b) the UVO-treated PDMS stamp. PαMS and Si denote poly(alpha-methylstyrene) and silicon, respectively. The hatched region in (b) represents the UVO-treated surface of the PDMS (Ref. [82]).

In this work, we investigated the relationship between the UVO treatment time of PDMS stamps and the degree of distortion in pattern dimension using one of the patterning methods, SCEP. In addition, through the formation of OSC patterns, the photosensitivity was improved due to the reduction of the off-current level. As for the conventional SCEP, an OSC/polymer blend, TIP-PEN/PαMS in our case, is used for producing the OSC patterns. In a film of the TIPS-PEN/PαMS blend, the TIPS-PEN molecules are usually phase-separated from the PαMS molecules and mostly located above the PαMS layer, that is, at the air-polymer interface. In fact, the PαMS layer serves as an additional dielectric layer in an organic electronic device such as an OFET. Here, for patterning the OSC films, the UVO-treated PDMS stamp having micrometer-scale patterns was contacted with the thin film of TIPS-PEN/polymer blend uniformly coated on a substrate. During this process, the nanoporous PDMS stamp absorbed the TIPS-PEN monomers through the contact area, generating the complementary patterns of TIPS-PEN. It should be noted that for the SCEP, the amount of the absorption of the TIPS-PEN molecules by the patterned PDMS stamp in the contact regions is critical for defining the TIPS-PEN patterns. In other words, the surface properties of the PDMS stamp play an essential role in both the fidelity and the stability of the TIPS-PEN patterns. We investigate how the UVO treatment for the modification of the PDMS surface affects the TIPS-PEN patterns produced in the SCEP using the PDMS stamp. Figure 1 shows the schematic diagram of the patterning processes of the SCEP and the resultant patterns of the TIPS-PEN obtained using the untreated and the UVO-treated PDMS

stamps. For the case of the untreated PDMS stamp as shown in Fig. 1(a), shrunken patterns were observed previously in the SCEP [33]. However, the introduction of UVO treatment on PDMS stamps greatly improved the pattern fidelity as shown in Fig. 1(b), since the hydrophilic nature of the modified surface of the PDMS by the UVO tends to limit the absorption of the TIPS-PEN beyond a certain amount, as explained below.

4.2. Fabrication of active layer patterns

4.2.1. Materials

TIPS-PEN with purity greater than 98% (Tokyo Chemical Industry Co., Ltd.) and PαMS (M_w = 437 k, Sigma-Aldrich Korea) with the concentration of 3 wt. % at 1:1 blending ratio were dissolved in 1,2,3,4-tetrahydronaphthalene. PVP (M_w = 25 k, Sigma-Aldrich Korea) was dissolved in propylene glycol methyl ether acetate with the concentration of 5 wt. % and the same weight amount of poly(melamine-co-formaldehyde) with the PVP was additionally put in the solution. A pre-patterned mold with 10 μm width of line and space was fabricated with the height of 1.2 μm using conventional photolithography on Si substrate. The PDMS base and a curing agent (Sylgard 184) were purchased from Dow Corning corporation. A mixture of the base and the curing agent at 10:1 by weight was poured on the pre-patterned mold in vacuum condition for 30 min to eliminate air bubbles inside the PDMS mixture and annealed at 70 ^{o}C for 2 h.

4.2.2. Formation of active layer patterns

The pre-patterned PDMS stamps were exposed to the UVO at the intensity of 28 mW/cm^2 for the duration from 0 to 90 min using the UVO-cleaner (AH-1700, Ahtech LTS Co., Ltd.). Note that the UVO-cleaner uses

ultraviolet light with the wavelength of 184.0 and 253.7 nm in the ambient condition [83]. Subsequently, the UVO-treated PDMS stamps were attached on TIPS-PEN films with the pressure of 1 kPa by placing the weight of 40 g in the area of 4 cm^2. The PDMS stamps on the TIPS-PEN films were thermally cured at 70 ^oC for the duration from 1 to 24 h under the vacuum condition of 6 Torr. Note that we fabricated the OSC patterns at the curing temperature of 70 ^oC (just above a typical annealing temperature of 60 ^oC) to prevent any harmful effect from thermal energy [84].

4.2.3. Fabrication processes

Firstly, a heavily doped p-type Si wafer was used as a substrate as well as the gate electrode. A thermally grown SiO_2 layer of 300 nm thick on the Si wafer served as the primary gate insulator. The substrate was cleaned with acetone, isopropyl alcohol, methanol, and deionized water in sequence. In order to achieve a uniform film of TIPS-PEN/ PαMS blend through the improved wetting, the 200 nm thickness of PVP layer was additionally formed on the SiO_2 layer via spin-coating at 3000 rpm 30 s. The film was then annealed at 110 ^oC for 10 min to remove any residual solvent and cross-linked at 200 ^oC for 20 min in ambient air. As an OSC layer, a solution of the TIPS-PEN/PαMS blend was spin-coated on the gate insulator at 1000 rpm for 30 s to obtain the thickness of about 80 nm. The annealing process was performed at 70 ^oC for 30 min in ambient condition. After that, 50 nm thickness of Au layer was thermally deposited through a shadow mask at the rate of 1.0 Å/s

under the pressure of 1×10^{-5} Torr to define the source and drain electrodes. The channel length and the channel width were 150 μm and 1 mm, respectively.

4.2.4. Measurements

The surface morphologies and geometrical profiles of the patterned TIPS-PEN film were characterized by using an AFM (XE-100, PSIA). The patterned TIPS-PEN films were observed through optical microscopy (OM) (Optiphot-Pol, Nikon). The electrical characterization of the OFETs was carried out using a semiconductor parameter analyzer (HP4155A, Hewlett–Packard Co.) under ambient pressure at room temperature. To measure photoresponse, the non-patterned and the patterned devices were illuminated from the top side using the 365nm wavelength of UV light source (GL-155, UVSMT) at the intensity of 3 mW/cm^2.

4.3. Wetting difference-based patterning

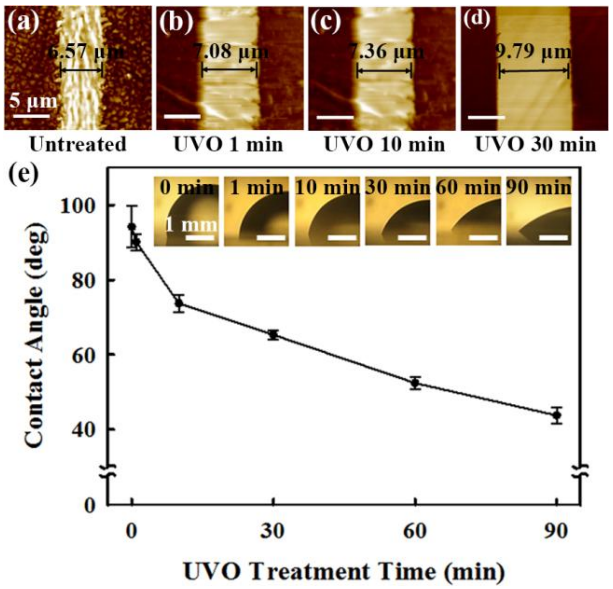

Figure 4.2. The AFM images of the TIPS-PEN patterns observed at 5 h after the SCEP using the PDMS stamps with the UVO treatment for (a) 0, (b) 1, (c) 10, and (d) 30 min, respectively. (e) The contact angle of water on the PDMS stamp treated with the UVO as a function of the duration time from 0 to 90 min (Ref. [82]).

We first examined how the UVO treatment for the modification of the PDMS surface influenced on the pattern formation of the TIPS-PEN observed at 5 h after the SCEP. Fig. 4.2 shows AFM images of the patterned TIPS-PEN films produced by SCEP using the PDMS stamps with the UVO treatment time of 0, 1, 10, and 30 min, respectively. As the duration of the UVO treatment increased, the width of the TIPS-PEN patterns greatly increased from 6.57 to 9.79 μm. Note that an ideal width of the TIPS-PEN pattern was

10 μm which is exactly the physical dimension of the patterned PDMS stamp in line width and space. In consideration of the ideal width of the TIPS-PEN pattern, the UVO-treated PDMS stamp for 30 min (PDMS 30) was found to exhibit the highest fidelity of the TIPS-PEN pattern, giving the shrinkage in width of about 2.1%. Note that the severe exposure of the PDMS stamps to UVO such as 60 and 90 min rather interrupted the patterning of TIPS-PEN films even after 48 h of annealing (not shown here). This may be caused by excessive amount of conversion of polysiloxane to SiO_x in the PDMS surface and makes the PDMS surface be less porous [85]. As shown in Fig. 4.2(e), the contact angle of water on the untreated PDMS stamp was 97.5° and it was decreased down to 43.7° with increasing the duration of the UVO treatment. This means that the PDMS surface becomes relatively hydrophilic by the UVO treatment. As a result, the hydrophilic PDMS surface tends to absorb the hydrophilic TIPS-PEN molecules into the nanoporous PDMS until it limits the further absorption due to the hydrophilic-hydrophilic interactions that hinder the penetration of the TIPS-PEN into the nanopores in the PDMS stamp. Thus, further adjustment to an appropriate UVO treatment time will obtain the pattern much closer to ideal one.

To clarify the effect of UVO treatment on the pattern formation, patterning processes of TIPS-PEN film with the untreated PDMS and the PDMS 30 were closely observed depending on time. Fig. 4.3(a) and (b) represent OM images of the time-evolution patterns of TIPS-PEN from 1 to 24 h produced using the untreated PDMS and the PDMS 30, respectively. As we can see in the figures, TIPS-PEN molecules contacted with PDMS was

selectively etched out through the evaporation and absorption of the molecules into the nanoporous PDMS. In figures of 1 h and 3 h, both the untreated PDMS and the PDMS 30 were completely patterned between 1 and 3 h. At the early stage of 1 h, the absorption into the PDMS 30 was more pronounced than that into the untreated PDMS until the absorption was limited due to the hydrophilic-hydrophilic interactions between the TIPS-PEN and the UVO-treated PDMS surface. More precisely, for the PDMS 30, the TIPS-PEN molecules were accumulated on the surface of the nanopores in the PDMS to some extent in an early stage and the molecules were no longer allowed to diffuse deeply into the PDMS in a later stage due to the strong adhesion. In contrast, for the untreated PDMS, the TIPS-PEN molecules were steadily diffused into the nanopores in the PDMS due to the weak adhesion of the TIPS-PEN molecules on hydrophobic nanopores in the PDMS. This is why the initial TIPS-PEN pattern for the case of the PDMS 30 was well-preserved compared to that for the case of the untreated PDMS, whereas the PDMS 30 maintained the pattern after 24 h. The geometrical profiles across the TIPS-PEN patterns for the untreated PDMS and those for the PDMS 30 were seen in Fig. 4.3(c) and (d). In both figures, the red and dashed line represented the geometrical profile of the ideal pattern in cross section. As mentioned before, at 1 h, the TIPS-PEN molecules in contact with the PDMS stamps were not fully eliminated in both cases, resulting in the residue of TIPS-PEN in undesirable regions. For the case of the untreated PDMS, in spite of incomplete patterning of TIPS-PEN film in 1 h, the film already had shrunken width of pattern around 8.63 μm and increasingly diminished in

width of the patterns over time, as shown in Fig. 4.3(c). On the other hadn, the PDMS 30 in Fig. 4.3(d) maintained the initial TIPS-PEN patterns in both the height and the width over time.

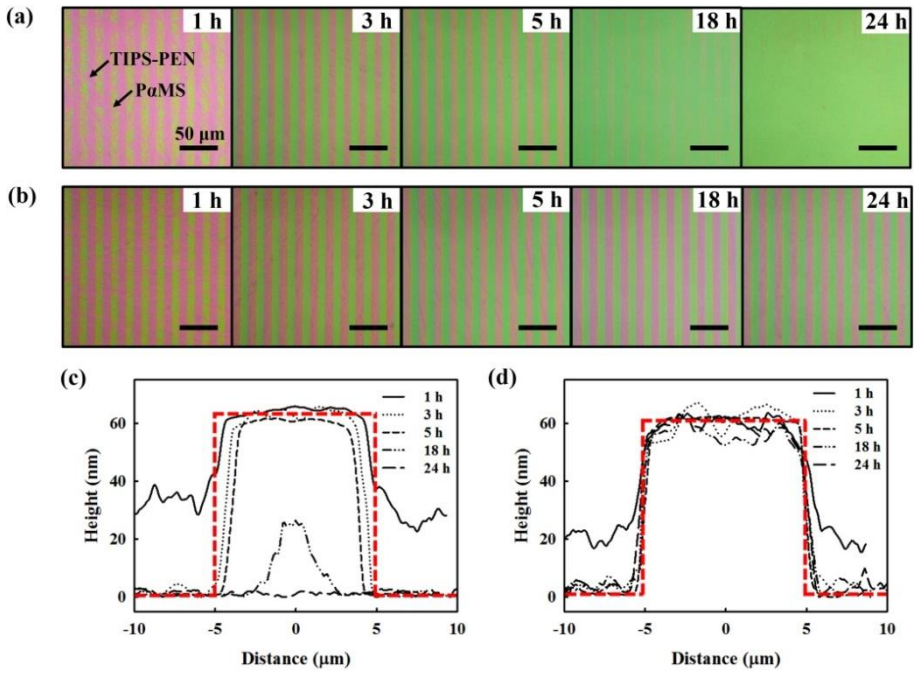

Figure 4.3. The OM images of the time-evolution patterns of TIPS-PEN using (a) the untreated PDMS and (b) the PDMS 30. The geometrical profiles of cross-sectional TIPS-PEN patterns in (a) and those in (b) were shown in (c) and (d), respectively. The red dashed lines are the ideal patterns of TIPS-PEN (Ref. [82]).

4.4. Transfer characteristics and photoresponse

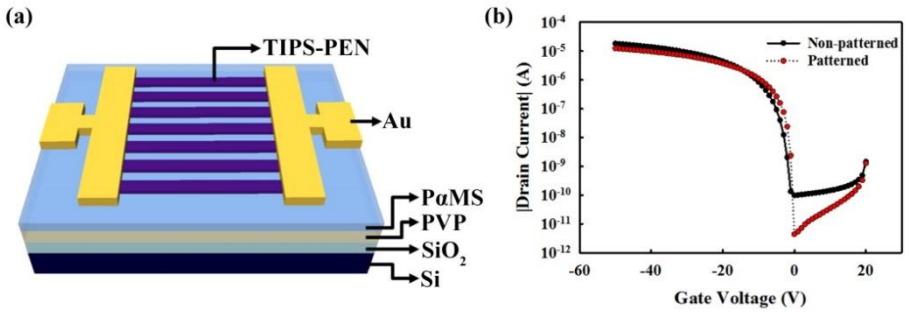

Figure 4.4. (a) Schematic diagram showing the OFET with the TIPS-PEN patterns. (b) Transfer curves of the OFETs with the non-patterned (solid line) and the patterned (dotted line) TIPS-PEN layers at the drain voltage of -50 V (Ref. [82]).

Finally, to ensure the implementation of the patterned TIPS-PEN layer by the SCEP into an OFET, we fabricated and compared OFETs with a non-patterned TIPS-PEN film and those with the patterned film through the PDMS 30. The structure of the OFETs with the TIPS-PEN patterns in this study is schematized in Fig. 4.4(a) and transfer curves of OFETs with non-patterned and patterned TIPS-PEN are plotted in Fig. 4.4(b). The non-patterned and the patterned OFETs showed similar values of mobility of 0.33 and 0.34 cm^2/Vs, respectively and the onset voltage is around 0 V in both OFETs, demonstrating that the patterning process didn't have any detrimental effect on the electrical performance of the devices. In addition, perfect isolation of each OFET enabled significant reduction of the off-current in the patterned OFET through eliminating the unnecessary current pathway. For the non-

patterned case, the on-current and the off-current were 1.81×10^{-5} and 9.85×10^{-11} A, respectively, yielding the on-off current ratio of 1.84×10^{5}. For the patterned one, the on-current and off-current were 1.23×10^{-5} and 4.44×10^{-12} A, respectively. The on-off current ratio in this case is 2.77×10^{6}, which is at least one order of magnitude higher than the non-patterned case.

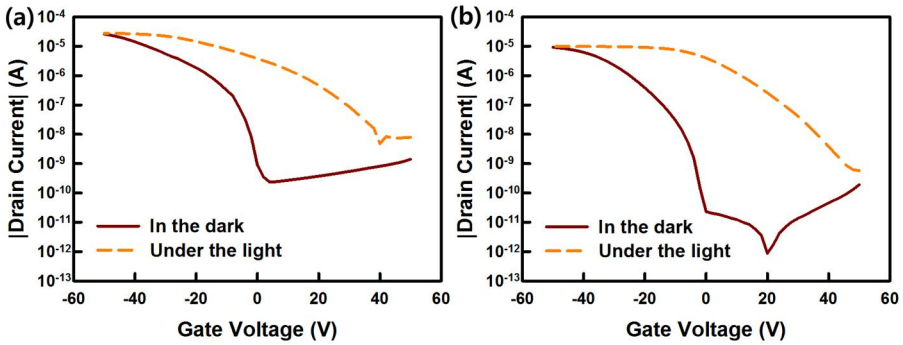

Figure 4.5. Transfer curves of (a) the non-patterned OFET and (b) the patterned OFET in the dark (solid line) and under the light (dashed line) at the drain voltage of -50 V.

For the photoresponse, we compared the transfer curves of the non-patterned OFET and the patterned OFET in the dark and under the light illumination at the drain voltage of -50 V as shown in Fig. 4.5. With the curves, the values of photosensitivity and the photoresponsivity were extracted in Fig. 4.6. It was found that the patterned OPT showed a higher photosensitivity value than the non-patterned device at the gate voltage from 50 to -50 V, resulting from the reduction of the dark current by the elimination of parasitic current paths. The max values of photosensitivity in non-patterned

and patterned devices are 1.17×10^4 and 1.73×10^5, respectively. However, the max photoresponsivity values, determined from Fig. 4.6(b), were 3.73×10^3 for the non-patterned case and 3.91×10^3 mA/W for the patterned case and the magnitude of the photoresponsivity is not essentially different from each other.

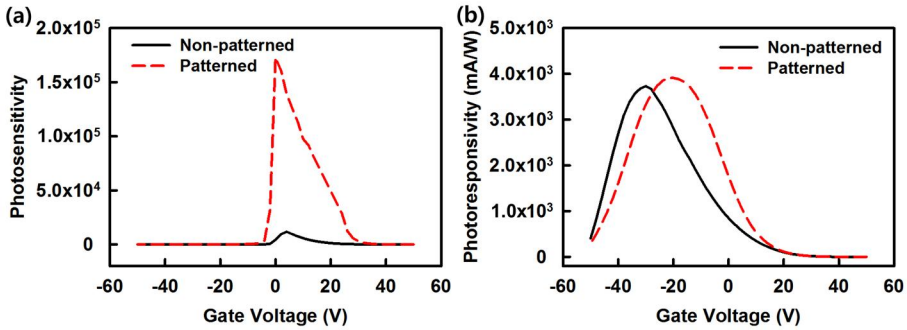

Figure 4.6. The graphs of (a) photosensitivity and (b) photoresponsivity of the non-patterned (solid line) and the patterned (dashed line) OFET at various gate voltage from 50 to -50 V at the drain voltage of -50 V.

4.5. Summary

In conclusion, we demonstrated the effect of the UVO treatment of the PDMS stamp on the fidelity of the TIPS-PEN patterns produced through the absorption of the TIPS-PEN monomers in contact with the PDMS surface during the SCEP. Here, the UVO-treated PDMS for 30 min was the best optimized condition for the highest pattern fidelity of TIPS-PEN. At the pattern size of 10 μm in line width and space, the pattern shrinkage of only 2.1% was observed at an early stage and the pattern was well-preserved over 24 h while the untreated PDMS patterned the films with at least 14% distortion due to early formation of the significantly shrunken pattern prior to complete patterning. This is mainly attributed to the fact that the absorption of the TIPS-PEN is limited due to the hindrance of the molecular diffusion into the nanopores in the PDMS at a later stage. Through patterning of OSC layers, the OFETs with lower off current and higher photosensitivity were fabricated. Our approach to achieving high pattern fidelity through the simple and low-cost patterning technique is expected to open a new route to the construction of advanced flexible optoelectronic systems and highly integrated organic optoelectronic circuits based on solution-processed OSCs.

Chapter 5. Reduction of Leakage Current of Vertical-Type Photo-Transistors

5.1. Introduction

The typical OPTs have limitations of low speed, low current level, and relatively high operational voltage mainly due to the low mobility and high resistivity of organic materials as described in **Section 2.4**. In addition, for photoresponse which is one of the important parameters, the OPTs exhibit relatively low photoresponse, impeding commercialization [48]. To overcome such drawbacks, much effort has been made toward the reduction of the channel length, the increase of the channel width, the fabrication of a highly-organized OSC film, and so on. However, most of existing solutions inevitably involve critical problems such as a small detection area, a complicated process, and the difficulty in integration. To pursue the devices with high current level, low operating voltage, and high detection area at once, the OPTs based on vertical configurations have been suggested [86-88]. Since the channel length of the VOFET reduces down to the nanometer scale of thickness of the OSC layer, it has the advantage that the photoexcited carriers only have to travel a short distance before reaching a contact.

The VOFETs suffer from high leakage current from the source to the drain irrespective of the gate voltage and eventually deteriorate the on/off current ratio and photosensitivity as demonstrated in Section.2.4. To solve this,

implementation of the insulator on the source electrode has been widely investigated. Particularly, the researches have been focused on the fabrication technique and the arrangement of the source/insulator structure. However, they still have difficulty in the precise control of source insulator arrangement on the source electrode, high-density integration, solvent orthogonality, and scalability [51-54].

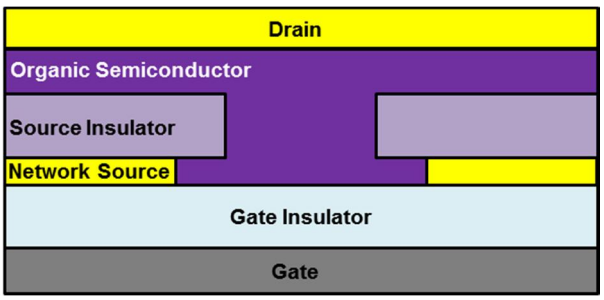

Figure 5.1. Schematic diagram of the vertical-type OPT based on SSIS.

In this work, we demonstrated the new configuration of vertical-type OPTs called SSIS (see Fig. 5.1.) and a simple fabrication process of the SSIS. During wet-etching process, the SSIS was obtained through control of wet-etching time. We optimized the electrical characteristics of SSIS device through controlling the length of the charge blocking coverage. The optimized device showed higher photosensitivity than the lateral type and the previous vertical type of OPTs at low operating voltages of 10 V. In contrast to other two devices (the lateral and the previous vertical types), the optimized device had the ability to detect the weak light intensity of 1 $\mu W/cm^2$ due to the reduction of off-current and intrinsic short channel length of vertical types.

5.2. Fabrication process

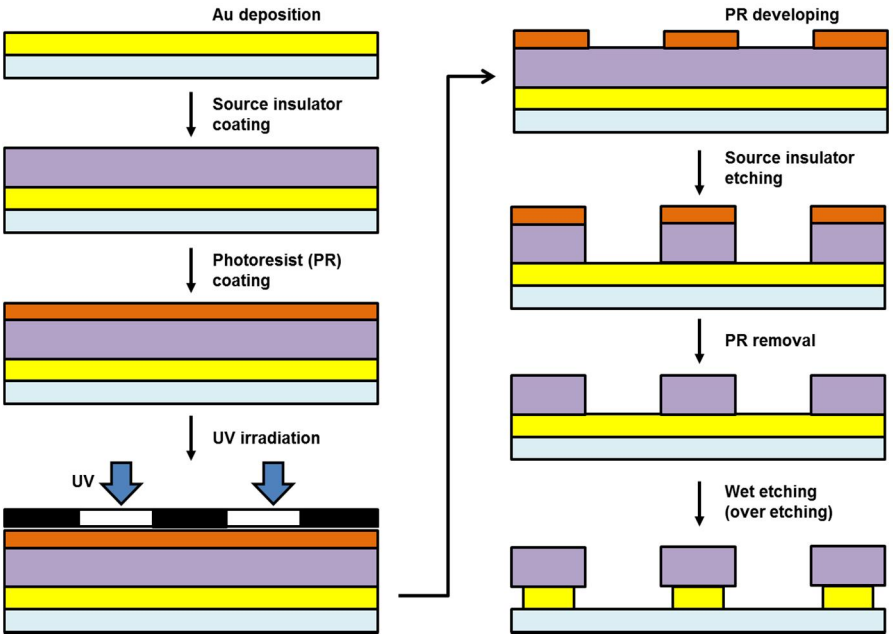

Figure 5.2. Fabrication processes of the SSIS. PR denotes photoresist.

OPTs were fabricated on glass substrates with a 165 nm-thick ITO layers serving as gate electrodes. The substrate was cleaned with acetone, isopropyl alcohol, methanol, and deionized water in sequence. PVP (M_w = 25,000 g/mol, Sigma-Aldrich Korea) mixed with PMF (100 wt. % of PVP) in propylene glycol methyl ether acetate at 10 wt. % were used for fabricating gate insulators and source insulators. To prepare a gate insulator of 500 nm thick, a solution of the PVP was spin-coated at 3000 rpm for 30 s. The film was then annealed at 110 ^{o}C for 10 min to remove any residual solvent and cross-linked at 200 ^{o}C for 20 min in ambient environment. For the fabrication of SSIS, a

45nm-thick Au layer was thermally deposited at the rate of 1.0 Å/s under the pressure of about 2.5×10^{-5} Torr to fabricate the source electrode. Here, the vertical-type OPT with network source electrodes was used. As the source insulator, the 500 nm-thick PVP layer was spin-coated and baked under the same condition for the gate insulator. The source insulator was patterned using a PR (AZ 5214, AZ electronic materials) through conventional photolithographic and dry-etching processes. After the removal of the PR, the network source electrode of 20 μm in the size of each aperture and the separation between two adjacent apertures was produced by wet-etching in an etchant (TFA, Transene) for Au. Here, the patterned PVP source insulator was served as a mask and length from the edge of the source electrode to the edge of the source insulating layer (L_s) is controlled based on wet-etching time (see Fig. 5.3(a)). That is, as the wet-etching time increased, then the L_s was also increased. For the fabrication of the OSC layer, the TIPS-PEN with purity greater than 98% (Tokyo Chemical Industry Co., Ltd.) was dissolved in anisole with the concentration of 1 wt. %. The solution of the TIPS-PEN was dropped over the SSIS and baked subsequently at 60 ^{o}C for 30 min. A 50 nm-thick Au layer was thermally deposited through a shadow mask at the rate of 1.0 Å/s under the pressure of 2.5×10^{-5} Torr to prepare the drain electrodes.

The SSIS was observed with scanning electron microscope (SEM, S-4800, Hitach). The electrical characterization of the VOFET was carried out using a semiconductor parameter analyzer (HP4155A, Hewlett–Packard Co.) under ambient condition. The photoresponse of the devices was measured using a UV light source (LLS-365, Ocean Optics, Inc.) with the intensity

about from 1 to 210 $\mu W/cm^2$ at the peak wavelength of 365 nm. For higher intensity of the light, we used a UV light source (GL-155, UVSMT) with the intensity of 3 mW/cm^2 at the same peak wavelength of 365 nm. Note that OFETs based on TIPS-PEN have been widely used for detection of UV light [89]. The UV light was illuminated from the bottom side where the substrate and the gate electrode were located.

5.3. Effects of length of charge blocking coverage

5.3.1. Fabricated structures

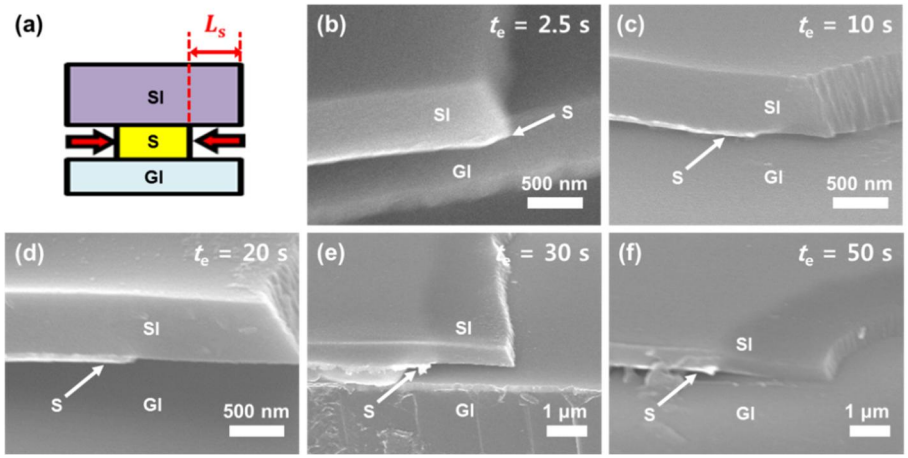

Figure 5.3. (a) Schematic diagram of SSIS. Increment of wet-etching time increases the value of L_s. SEM images of SSIS with wet-etching time (t_e) of (b) 2.5, (c) 10, (d) 20, (e) 30, and (f) 50 s. S, SI, and GI denote source, source insulator, and gate insulator, respectively.

As shown in Fig. 5.3(a), the value of L_s can be controlled depending on the t_e. In Figs. 5.3(b)-(f), as the wet-etching time increased, the value of L_s was increased. The values of L_s at t_e of 2.5, 10, 20 s were about 0.07, 0.6, and 1.2 μm, respectively. From this, the average rate of wet etching is assumed to be 60 nm/s. Note that the device with t_e = 2.5 s can be regarded as the previous vertical types because it showed negligible value of L_s between the source and the source insulator. However, after t_e = 20 s, collapse of source

insulator was shown and, at t_e = 50 s, the source insulator completely collapsed, reaching the surface of the gate insulators.

5.3.2. Transfer characteristics

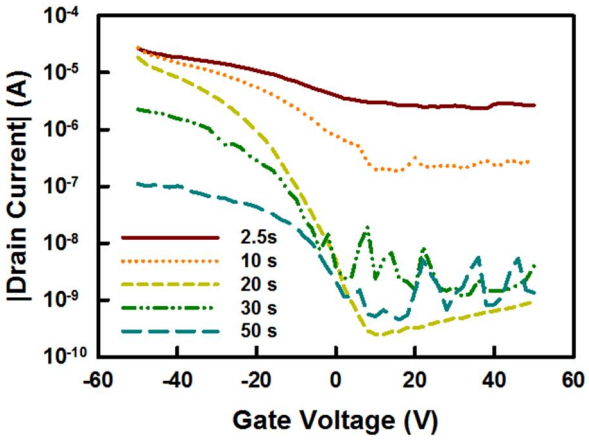

Figure 5.4. Transfer curves of the OPTs based on SSIS with different t_e of 2.5, 10, 20, 30, and 50 s at the V_D of -10 V.

From Figs. 5.3(b)-(f), it can be assumed that after t_e = 20 s, the performance of the devices is degraded. The devices with t_e of 2.5, 10, and 20 s exhibited comparable on-current level about 10^{-5} A as shown in Fig 5.4. In contrast to the on-current level, the devices showed different aspects in terms of off-current level. That is, with the increment of t_e, the off-current level was decreased from 2.49×10^{-6} to 2.49×10^{-10}, resulting in the improvement of on-off current ratio from 10^1 to 10^5. Highly reduced off current resulted from the

fact that protruded parts of source insulator layers sufficiently block leakage current from the source to the drain electrode which cannot be easily controlled by the gates bias. At t_e of 30 and 50 s, on-current level was reduced and the devices showed unstable off-current due to the collapse of the source insulators. Thus, at t_e = 20 s, we obtained the optimized performance of the devices based on SSIS.

5.3.3. Photoresponse

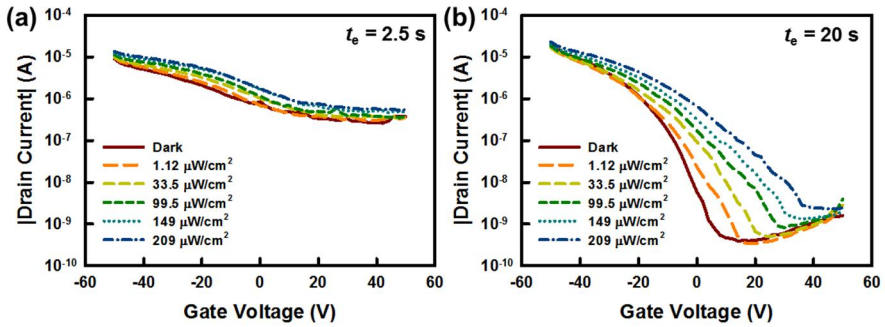

Figure 5.5. Transfer curves of the OPTs with wet-etching time of (a) 2.5 and (b) 20 s in the dark and under the different light intensity of 1.12, 33.5, 99.5, 149, and 209 μW/cm^2 and at the V_D of -10 V.

To understand the influence of the SSIS on the photoresponse, the transfer curves of the OPTs with t_e = 2.5 and 20 s in the dark and under the different light intensity were investigated as shown in Fig. 5.5. The device with t_e = 20 s exhibited the change in transfer curves even at the weak light intensity of 1.12 μW/cm^2, while the change of the transfer curve of the device

with t_e = 2.5 s was negligible at the same condition. This is mainly attributed to the reduction of off-current of the optimized device (t_e = 20 s). In addition, at higher light intensity, the OPTs with t_e = 20 s showed more change in transfer curves than those with t_e = 2.5 s.

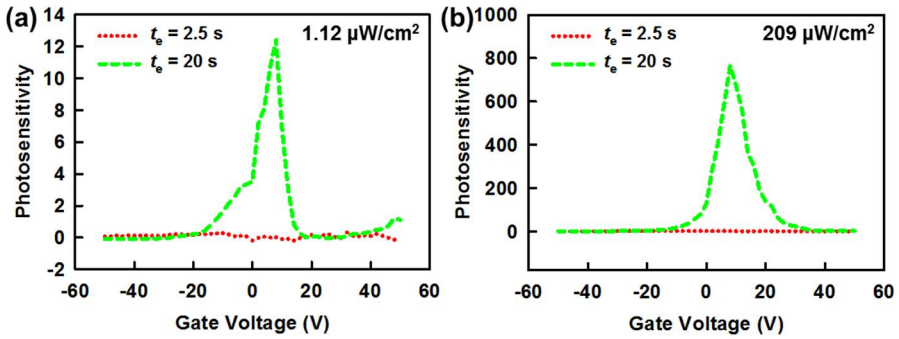

Figure 5.6. Photosensitivity-gate voltage graphs of the OPTs with t_e of 2.5 (dotted line) and 20 s (dashed line) at the light intensity of (a) 1.12 and (b) 209 μW/cm^2.

For comparison of photoresponse in both devices, the values of photosensitivity with gate voltage were extracted from the transfer curves in Fig. 5.5. The graphs of photosensitivity-gate voltage at the light intensity of 1.12 and 209 μW/cm^2 were shown in Fig. 5.6. It indicates that, at both light intensities, the OPTs with t_e = 20 s showed much higher photosensitivity. At the light intensity of 1.12 μW/cm^2, the values of max photosensitivity of t_e = 2.5 and 20 s cases were 3.11×10^{-1} and 1.24×10^{1}, respectively. At the light intensity of 209 μW/cm^2, the values were 1.96 and 7.65×10^{2}, respectively. Note that the highest values of photosensitivity were usually around at onset voltage.

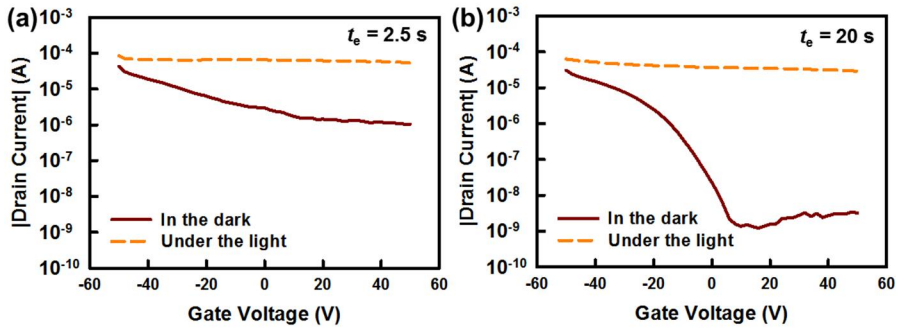

Figure 5.7. Transfer curves of the OPTs with t_e of (a) 2.5 and (b) 20 s in the dark (solid line) and under the light (dashed line) at the light intensity of 2.97×10^3 μW/cm^2 at the V_D of -10 V.

The photoresponse of both devices under relatively high light intensity of 2.97×10^3 μW/cm^2 was examined. The transfer curves of t_e = 2.5 and t_e = 20 s cases in the dark and under the light were shown in Figs 5.7 (a) and (b), respectively. As we can see from the figures, under the light, both devices showed nearly constant current level over entire gate voltages in the transfer curves. That is, the OPTs with t_e = 2.5 s and 20 s exhibited high photoresponse with the photosensitivity of 5.16×10^1 and 2.86×10^4, respectively. Here, the optimized OPT (t_e = 20 s) showed higher photosensitivity.

For the dynamic photoresponse, the drain current level with time was measured in both OPTs. As shown in Fig. 5.8, at the higher light intensity of 2.97×10^3 μW/cm^2 (the same light intensity in Fig. 5.7), both devices enabled to detect the light exposure and showed memory effects where the current level after light exposure was persistent since the photo-generated electrons were strongly trapped so that an additional negative gate voltage was built up

[76]. In contrast, at the light intensity of 209 μW/cm^2, the OPT with t_e = 2.5 s couldn't detect the light exposure while the OPT with t_e = 20 s enabled to detect the light due to much lower current level in the dark. In this regard, it can be concluded that the photosensitivity was improved through the introduction of SSIS in the vertical-type OPTs.

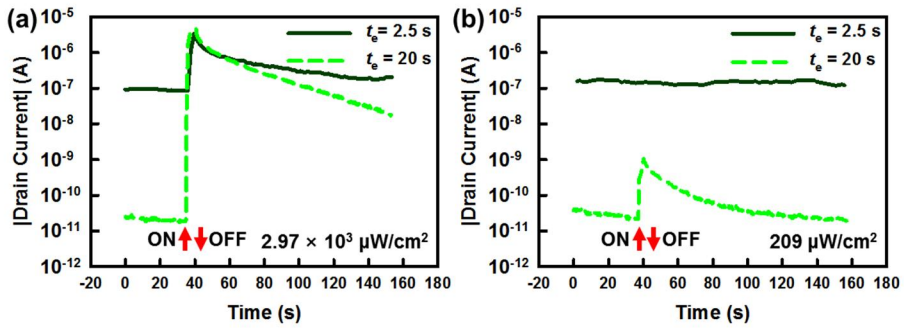

Figure 5.8. Dynamic graphs of the OPTs with the t_e of 2.5 (solid line) and 20 s (dashed line) at the light intensity of (a) 2.97 × 10^3 and (b) 209 μW/cm^2.

5.4. Conclusions and summary

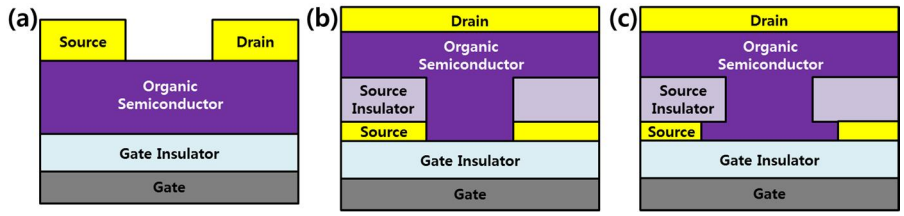

Figure 5.9. Schematic diagrams of (a) planar-type, (b) previous vertical-type (t_e = 2.5 s), and (c) optimized vertical-type OPTs (t_e = 20 s) based on SSIS.

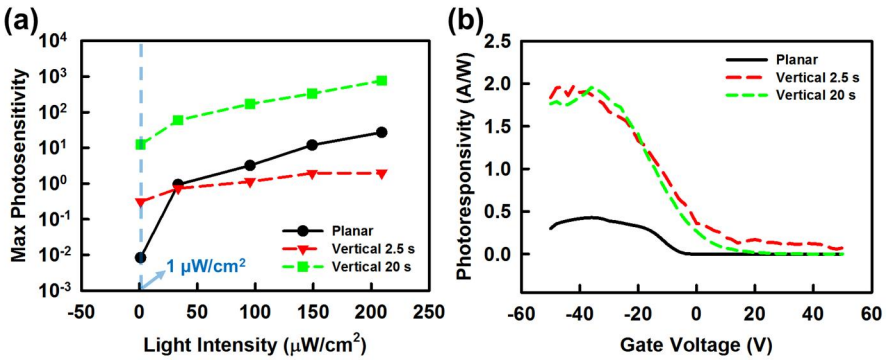

Figure 5.10. Graphs of (a) one maximum photosensitivity vs the light intensity and (b) photoresponsivity vs the gate voltage of three-type OPTs (one planar type and two vertical types with t_e = 2.5 and 20 s) at the light intensity of 209 μW/cm^2.

Lastly, three different structures of OPTs were compared as shown in Fig. 5.9. Typically, at the same operating voltage, planar OPTs had lower current level than previous vertical type, while the vertical type showed higher off-current than the planar one. Due to the high off-current, vertical type showed lower photosensitivity in spite of higher photoresponsivity caused by its

intrinsic short channel length. Through the introduction of optimized SSIS in the vertical-type OPTs, the lower photosensitivity causing from high off-current level could be solved. As shown in Fig. 5.10, previous vertical type corresponding to 'Vertical 2.5 s' in the figure exhibited lower photosensitivity than the planar type except at the light intensity of 1 $\mu W/cm^2$. Note that the higher photosensitivity of previous vertical type at the light intensity of 1 $\mu W/cm^2$ was mainly due to the short channel length in which photo-induced charges transport into the electrodes without recombination, while the planar one was unable to detect the weak light due to the relatively large channel length. However, the OPTs based on optimized SSIS (t_e = 20 s) have higher photosensitivity even in comparison with the lateral one. In terms of photoresponsivity, both vertical-type OPTs showed the same values with gate voltage but the planar OPT showed lower photoresponsivity due to the large channel length.

In summary, we presented a novel structure of vertical OPTs based on the self-aligned source insulator on the source electrode. Here, the structure was optimized by controlling the duration of wet-etching time and thus changing the length of charge blocking coverage. The optimized OPTs exhibited high photosensitivity which was originally difficult to achieve in vertical-type OPTs due to intrinsic high off current. In addition, the devices showed higher photoresponsivity in comparison with the planar types. The higher photoresponse than previous devices was mainly attributed to the fact that the protruded part of the self-aligned source insulator blocked the considerable current flowing from the edge of the source to the drain in the off state and the

devices had the short channel length of the thickness of the OSC layer. Our OPTs in the new vertical configuration will open a new route for constructing highly photosensitive devices.

Chapter 6. Concluding Remarks

In this thesis, control approaches of charge pathway were demonstrated in the scientific and technological viewpoints towards the improvement of photoresponse in OPTs. The enhancement of optical memory effect and the improvement of photosensitivity were achieved through the interfacial modification and the restriction of unnecessary charge paths. During the operation of the OPTs, since charges are accumulated and transported within the first few monolayers of the OSC films adjacent to the gate dielectric surface due to the bias of the third terminal, it is important to obtain understanding of the relationship between the interfacial characteristics of the gate insulator and the charge carrier dynamics of the OPTs under light illumination. Besides, for the improvement of photosensitivity, the reduction of the leakage current deteriorating the photoresponse of the OPTs is required.

Firstly, the effect of the interfacial characteristics at polymer dielectric/OSC layers on the photoresponse was investigated to develop the p-OPTs with the enhanced optical memory effect. The origin of the charge carrier dynamics, especially trapping/detrapping ratio related to the memory effect, under light illumination was systematically analyzed in terms of morphological and physicochemical characteristics at the dielectric/OSC interfaces. The physicochemical properties of the dielectric material were found to more dominantly govern the optical memory effect of the OPT than the morphological effect.

Next, for the improvement of photosensitivity, reduction of leakage current both in the planar and the vertical types was investigated.

For the planar type, the parasitic leakage current was reduced by the solution-based patterning of OSC layers. The OPTs based on small-molecule OSC/polymer blends suffer from relatively high off current and thus low photosensitivity due to undesirable current pathways over a whole substrate. Through the introduction of wetting difference-based SCEP, high-fidelity patterns were developed and the patterned OPTs exhibited the improved photosensitivity due to the reduced leakage current.

On the other hand, for the vertical case, vertical OPTs based on SSIS were introduced to improve photosensitivity. Since the protruded part of the self-aligned source insulator obstructed the unnecessary current flowing from the edge of the source to the drain which cannot be controlled by gate bias, the vertical OPTs exhibited high photosensitivity in comparison with previous vertical types. When it compared with the planar type, the devices showed higher photoresponsivity due to the intrinsic short channel length. In addition, with the fabrication method demonstrated here, source insulator arrangement on the source electrode can be precisely controlled and the devices can be highly integrated.

In conclusion, control of charge pathways was investigated for the improvement of photoresponse in the OPTs within the framework of the interfacial phenomena involved in different layers and the development of the novel structure. The work presented in thesis is expected to open a new route

to the delicate interfacial modification of multi-layers and the integration of basic building blocks for constructing advanced optoelectronic systems.

Appendix (acronyms)

AFM: atomic force microscopy

FT-IR: Fourier transform infrared spectroscopy

ITO: indium-tin-oxide

MIMIC: micromolding in capillary

MOSFET: metal-oxide-semiconductor field-effect transistors

OFET: organic field-effect transistor

OM: optical microscopy

OPT: organic photo-transistor

OSC: organic semiconductor

PDMS: polydimethylsiloxane

PDMS 30: PDMS stamp treated with ultra-violet light for 30 min

PMF: poly(melamine-co-formaldehyde)

PMF0: poly(4-vinylphenol) without PMF

PMF100: poly(4-vinylphenol) with PMF at the concentration of 1:1 in weight with respect to poly(4-vinylphenol)

PMMA: poly(methyl methacrylate)

p-OPT: polymer insulator-based organic photo-transistor

PR: photoresist

PVP: poly(4-vinylphenol)

SCEP: selective contact evaporation printing

SEM: scanning electron microscope

SiO_2: silicon dioxide

SSIS: self-aligned source insulator structure

Ta_2O_5: tantalum oxide

TIPS-PEN: 6,13-bis(triisopropylsilylethynyl) pentacene

UV: ultra-violet

UVO: ultraviolet ozone

VOFET: vertical organic field-effect transistor

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Abstract (Korean)

유기 광트랜지스터(transistor)는 빛을 정보 전달 매개로 이용하는 광전자 시스템(system)의 기본적인 구성요소로서 큰 관심을 받고 있다. 유기 광트랜지스터는 빛 감지, 스위칭(switching), 그리고 신호 증폭의 기능이 단일 소자에 집적 되어있는 광변환장치의 한 종류이다. 유기 광트랜지스터는 저가격, 기계적 유연성 및 화학적 다기능성과 같은 유기 물질 고유의 장점뿐 아니라, 전계 효과에 의한 신호 증폭 효과를 통해 2 단자 유기 광다이오드보다 높은 광감성 및 신호 대 잡음 비를 갖는다. 이러한 장점들 때문에, 유기 광트랜지스터는 전기 통신 장비, 정보처리 기기, 위치 감지 시스템 등의 각종 산업 군에서부터 의료용 X 선 영상 기기 및 센서와 같은 의학 분야에 이르기까지 다양한 기술분야에서 응용되고 있다.

유기 광트랜지스터의 구동은 3 단자의 전압으로 인해 전하들이 게이트(gate) 절연체 부근의 유기 반도체 층에 쌓이고 드레인(drain)으로 흐르며, 이를 통해 출력 신호를 내보내는 과정들로 이루어진다. 전하들이 채널(channel) 내부를 흐르면서 주변 환경과 상호 작용하고 이들의 영향은 모두 출력 신호에 반영 된다. 이러한 점에서, 전하 이동 경로는 유기 광트랜지스터의 성능을 결정하는 가장 중요한 요소 중 하나라고 할 수 있다. 특히 수평 구조의 유기 광트랜지스터에서는, 전하들이 수평적으로 유기 반도체

층과 게이트 절연층 계면을 따라 소스에서 드레인으로 이동하기 때문에, 소자의 성능이 그 계면 성질에 크게 영향을 받는다. 따라서, 게이트 절연체의 계면 성질과 빛에 따른 전하 동역학 사이의 관계에 대한 이해가 중요하다. 또한 유기 광트랜지스터에서는 누설 전류가 광반응을 저해시키는 노이즈(noise)로 작용하기 때문에, 누설 전류 저감을 위해 불필요한 전하 경로를 제한하는 것이 필요하다. 수평 구조의 유기 광트랜지스터에서는 불필요한 전하 경로를 제한하기 위한 방법으로, 유기 반도체층 패터닝(patterning)을 들 수 있다. 수직 구조의 유기 광트랜지스터의 경우에는, 게이트 전압에 의해 조절되지 않고 소스(source)에서 드레인으로 흐르는 누설 전류가 상당히 크고, 이로 인해 오프 상태 (off state)에서의 전류 값이 크다는 문제점을 가지고 있어 이를 해결하기 위한 새로운 기술 개발이 필요하다.

본 논문에서는 기본적으로 수평 구조와 수직 구조로 분류되는 유기 광트랜지스터의 광반응을 향상시키기 위한 전하 경로 제어 기술들을 제시한다.

첫 번째로는, 고분자 게이트 절연층 기반의 유기 광트랜지스터에서 광반응에 대한 고분자 절연층과 유기 반도체층 사이의 계면 성질의 효과를 연구하고, 그 결과를 이용하여 광메모리(memory) 효과를 증대시켰다. 광메모리 효과는 절연 물질의 작용기의 종류와 밀도에 따라 제어 가능하다는 것을 알 수 있었다.

이러한 성질은 광메모리 뿐만 아니라 광스위치(switch)와 같은 특정 응용처에 적합한 소자를 개발하기 위해 활용될 수 있다.

두 번째로는, 용액 공정 기반 패터닝 기술을 이용하여 유기 반도체층의 패턴(pattern)을 형성하고 이를 통해 소자의 광감도를 향상 시켰다. 저분자/고분자 혼합물 기반 유기 광트랜지스터는 주로 스핀 코팅(spin-coating) 공정을 통해 유기 반도체 층을 형성하며, 기판 전면에 도포된다. 따라서, 불필요한 전류 경로로 인해 오프 전류 값이 크고, 필연적으로 광감도가 낮은 문제점이 있었다. 젖음성 변화에 기반한 선택적 흡착 증발 프린팅(selective contact evaporation printing) 기술을 이용함으로써, 높은 신뢰도로 유기 반도체층 패턴을 형성하였고, 해당 기술이 적용된 유기 광트랜지스터는 기생 누설 전류의 저감에 따라 광감도가 증가하였다.

마지막으로, 수직 구조 유기 광트랜지스터의 광감도 향상을 위해 소스 전극 상부에 자기배열 소스 절연층을 형성했다. 소스 절연층의 돌출된 부분이 소스의 가장자리에서 드레인으로 흐르는 불필요한 전류 흐름을 효과적으로 차단함에 따라 높은 광감도를 얻을 수 있었다. 또한, 본 소자는 수직 구조에서 기인한, 반도체층 두께에 해당하는 짧은 채널 길이로 인해 수평 구조에 비해 높은 광반응을 보인다. 해당 연구에서 사용한 제작 방법은 소스 전극 위에 소스 절연층의 배열을 미세하게 조절 할 수 있으며 이에 따라

고집적이 가능하다는 장점이 있다. 이는 기존 연구에서는 불가능하였었다.

요약하자면, 소자 내 서로 다른 물질 층 사이에 일어나는 계면 현상과 구조적 관점에서의 전하 경로 조절 기술을 통해 유기 광트랜지스터의 광반응성을 향상시켰다. 본 논문에서 제시된 연구는 광유기전자 시스템 발전을 위해, 기본 구성 요소를 집적하고 다층 구조에서의 계면을 조절하는 데 있어 새로운 길을 열어 줄 것으로 기대된다.

주요어: 유기 광트랜지스터, 광감도, 광메모리, 누설 전류, 수직 구조, 절연체/유기물 계면