M.S. DISSERTATION

SPICE Simulation of the Neuromorphic System Composed of Neuron Circuit and Synaptic Device

뉴런 회로 및 시냅스 소자로 구성된 뉴로모픽 시스템 전자회로 시뮬레이션

by

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DEPARTMENT OF ELECTRICAL ENGINEERING AND
COMPUTER SCIENCE
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Confirming the master's thesis written by

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ABSTRACT

Artificial intelligence, such as voice recognition, face recognition, and autonomous motion that can artificially replace the human brain has caused a big issue, and the artificial intelligence industry in the future will bring about a big change in the global trend. However, computing system based on the existing von Neumann structure and artificial intelligence implementation through it show problems in terms of power consumption and efficiency. Especially, when performing higher-order operations, von Neumann bottleneck appears when processing large amounts of data due to the large power consumption and inefficiency which caused the emergence of a new artificial intelligence system. To confirm the efficiency of the neuromorphic system, Spiking-Neural-Network system is closely investigated by using synaptic device and neuron circuit. In the SPICE simulation, neuromorphic system features equivalent output with artificial neural network MATLAB simulation when performing MNIST pattern recognition test. This means any software-based artificial intelligence can be implemented in hardware. Furthermore, in order to enhance accuracy of the MNIST pattern recognition, overflow retaining neuron circuit is proposed. Through a simple circuit structure change, virtual membrane node is properly operated with minimizing the wasted signals differently from conventional

integrate and fire neuron circuit. It is confirmed by comparing the raster plot extracted from the MATLAB simulation and SPICE simulation output which implicit the hardware implementation of all other artificial neural network.

Keywords: Neuromorphic, Spiking-Neural-Network, Neuron, Synapse, Overflow retaining

Student number: 2016-20956

CONTENTS

Chapter 1

Introduction

Artificial intelligence, such as voice recognition, face recognition, and autonomous motion that can artificially replace the human brain has caused a big issue, and the artificial intelligence industry in the future will bring about a big change in the global trend [1-3]. However, computing system based on the conventional von Neumann structure and artificial intelligence implementation through it show problems in terms of power consumption and efficiency [4,5]. When performing higher-order operations, such as cognition and reasoning, von Neumann bottleneck appears and many multiplication iterations required in the process for weight updating are inevitable [6,7]. Therefore, the large power consumption and inefficiency of the conventional system requires the emergence of a new artificial intelligence system [8-10]. Unlike conventional computing system, the human brain consists of only neurons and synapses, and event-driven operation efficiently perform the higher-order operation in a large parallel

structure with relatively low power consumption [11-13]. Thus, the neuromorphic system, an artificial intelligence implementation based on brain-inspired hardware, is a strong candidate for a new systematic configuration [14-15]. And there have been various attempts to construct such a novel Spiking-Neural-Network (SNN) by using RRAM and PCRAM and floating body device together with a neuron circuit [16-20].

Numerous researches have been focusing their efforts to make a breakthrough by implementing hardware based neural network system, such as Spiking-Neural-Network (SNN). However, although many novel systems have been proposed, the effectiveness of those systems are not yet clear when the actual system is implemented in hardware. Therefore, it is necessary to confirm whether the system that implement the whole system in hardware actually have learning and recognition functions such as Modified National Institute of Standards and Technology database (MNIST) pattern recognition through SPICE simulation.

In this thesis, neuromorphic system using synaptic device, neuron circuit

and weight transfer method is implemented by SILVACO SMARTSPICE simulation tool. In addition, we propose and confirm the overflow retaining neuron circuit which can improve the accuracy of MNIST pattern recognition. The hardware-based recognition system has advantages in terms of power consumption and efficiency as mentioned above, and it is meaningful to have the same capability as the software-based artificial intelligence system.

Chapter 2

Building Blocks and Methods for Neuromorphic System

2.1 Neuron Circuit

Biological neurons integrate the signals of the pre-neurons coming through the synapse into the soma. When the integrated signal goes above a certain threshold, it generates an action potential spike through the axon. This integrate & fire characteristic also applies to the neuron circuit in the neuromorphic system which imitates the biological nervous system [1,2]. In the neuron-synapse multilayer, signals coming from the synaptic device are integrated in the capacitor of the neuron circuit. When the signal is generated from the neuron, the generated signal is transferred to the post-synapses. At the same time, signal is fed back to the pre-synapses, and the weight of the pre-synapses can be changed through the characteristics of Spike-Timing-

Dependent-Plasticity (STDP) or Spike-Rate-Dependent-Plasticity (SRDP).

A proposed neuron circuit is shown in Fig. 2.1., which generates asymmetric output spikes that can drive the synaptic device. The proposed neuron circuit has integrate & fire characteristics like biological neurons, and uses only NMOS, PMOS, and capacitors, and has simple structure such as inverter and current mirror. First, the capacitor labeled C_1 integrates signal comes from the pre-synapses like the soma of the biological neuron. When the signal integrated in the capacitor goes above a certain level and exceeds the threshold, the NMOS connected with $-V_{DD}$ indicated by N_6 operates first and pulls the output node

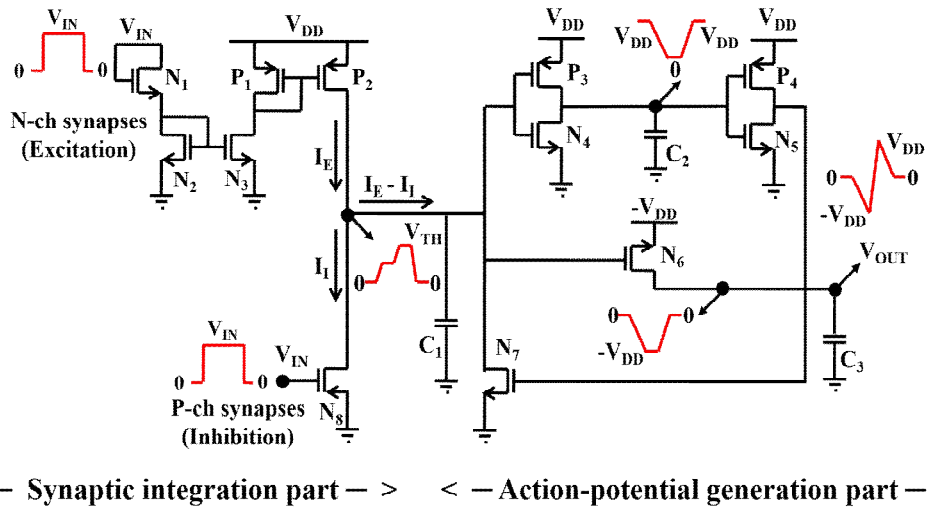

Figure 2.1. Integrate & Fire Neuron circuit having an asymmetric output characteristic.

voltage to $-V_{DD.}$ At the same time, at the two inverter stages connected in series, the output node is pulled back to $+V_{DD}$ when the second inverter operates, ensuring a sufficient delay to be pulled to $-V_{DD}$. Finally, the output node voltage pulled to $+V_{DD}$ again drives the NMOS labeled N_7 to return the output node voltage to its original state by discharging capacitor $C_{1.}$ The fabricated circuit diagram is shown in Fig 2.2.

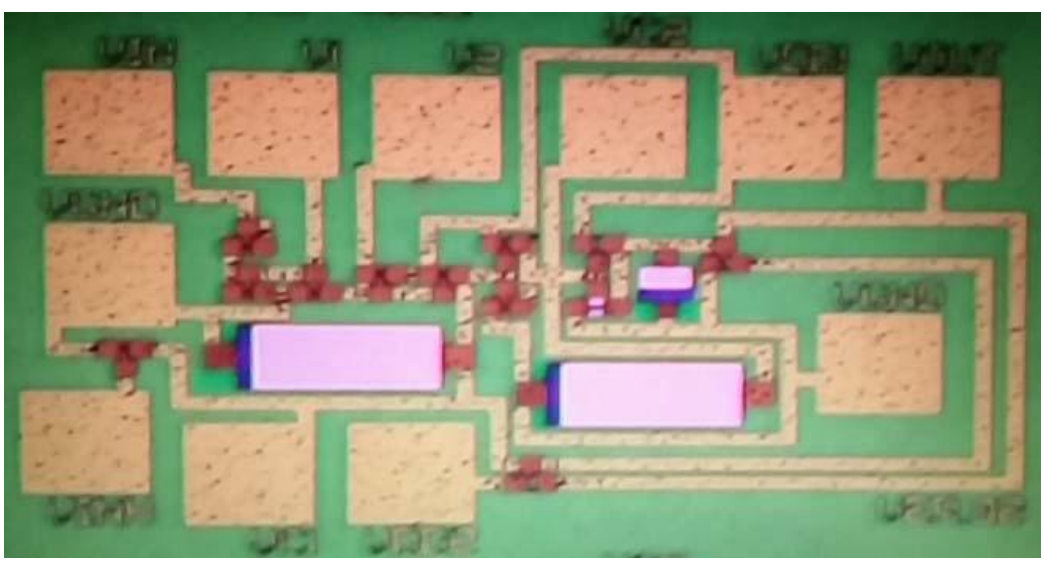

Figure 2.2. Top view of the fabricated neuron circuit.

2.2 Synaptic Device

The above-mentioned neuron circuit with asymmetric output spike characteristic circuit is designed to drive the previously proposed 4-terminal silicon based floating body synaptic transistor (SFST) [3,4]. As shown in Fig 2.3., there is an ONO stack with a double gate structure that can store charge at the 'gate2' side. If excess carriers are generated by impact-ionization when the device is operating, carriers can be stored in the charge storage layer. Therefore, it is possible to change the weight of the synaptic device according to the degree of a presence of carriers in the ONO stack by the timing difference between pre-neuron and post-neuron signals coming into gate1 and gate2 respectively [5].

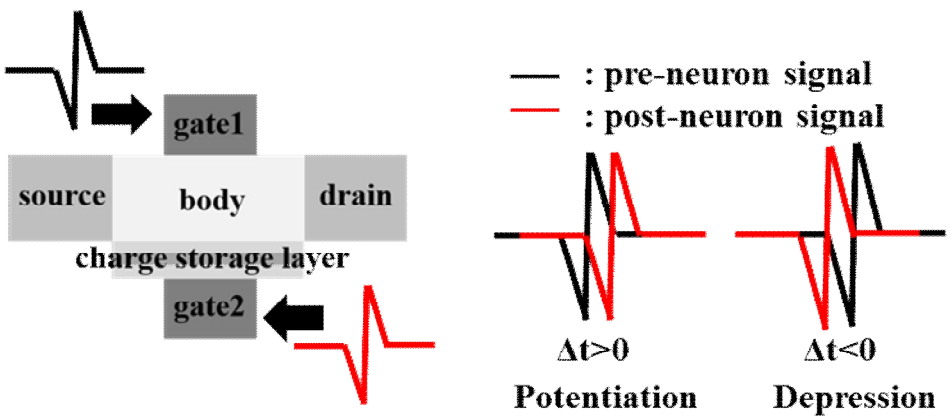

Figure 2.3. Structure and learning mechanism of the SFST.

2.3 Weight Transfer Method

In Fig 2.4, simple neuromorphic system with neuron-synapse connection is shown. Just like biological neural system, signals from pre-neuron is transferred to post-neuron by synaptic device, which can store appropriate weight. Weight of the synaptic device can be modulated with timing difference of pre-synaptic neuron and post-synaptic neuron by mimicking biological STDP characteristics. When square input pulse is applied to the pre-synapse which is replaced to simple NMOS, pre-neuron integrates the signal and finally generates output spike as mentioned above. In this situation, the output spike of the neuron circuit which is measured value and characteristics of the synaptic device is modeled and verified using SILVACO SMART SPICE simulation tool. In the case of $\Delta t > 0$, where Δt is a timing difference of the post-neuron and the pre-neuron spike applied into the synapse, a positive bias is applied to the top gate of the synaptic device and a negative bias is applied to the bottom gate. After this learning process, synaptic device flows more current when the same input is applied again. Similarly, in the case of $\Delta t < 0$, a negative bias is applied to the top gate

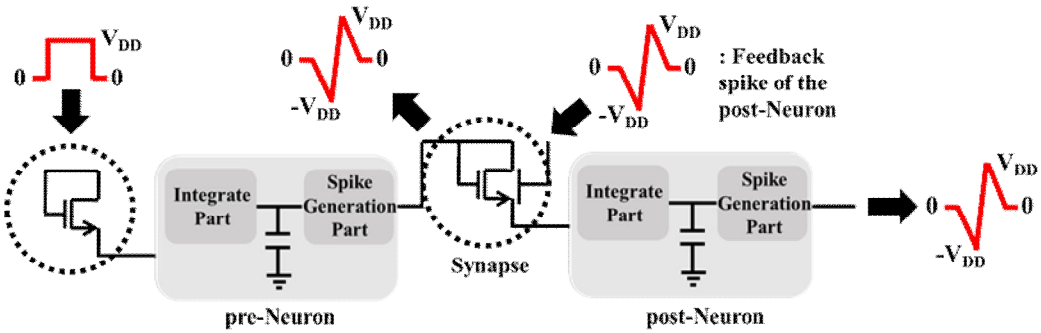

Figure 2.4. Simple neuromorphic system configuration with connection of the neuron and synapse.

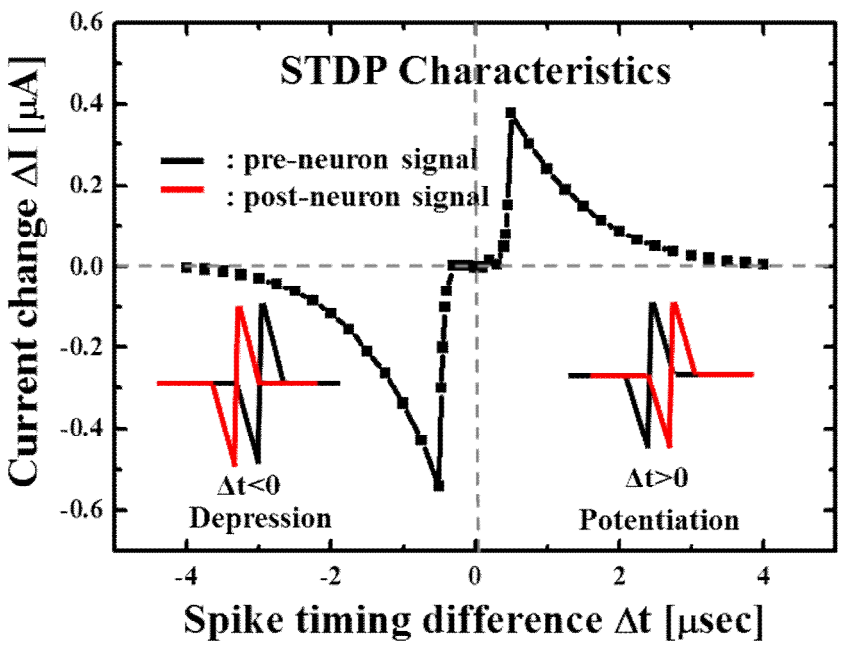

Figure 2.5. STDP characteristics of the neuromorphic system in Fig. 2.4.

and a negative bias is applied to the bottom gate causing less current to flow when the same input is applied after learning. STDP characteristics of the neuromorphic system constructed in Fig. 2.4 is shown in Fig. 2.5. By applying feedback spike into the bottom gate of the synapse with various timing difference, the weight change of the intermediate synapse is verified with well-known STDP characteristics in biological neural systems [6]. Therefore, we know that the weight of the synapse can be changed according to the STDP characteristics. As shown in Fig 2.6, and Fig 2.7, charging speed of the capacitor varies. In the case of $\Delta t > 0$, capacitor charges faster because of the holes in ONO stack of the SFST. On the other hand, in the case of $\Delta t < 0$, capacitor charges more slowly due to the electrons in ONO stack. As a result, it can be seen that the weight of the synaptic device can be changed by the timing difference between the pre-synaptic neuron and post-synaptic neuron. This also means that weights can be appropriately assigned in the weight transfer method.

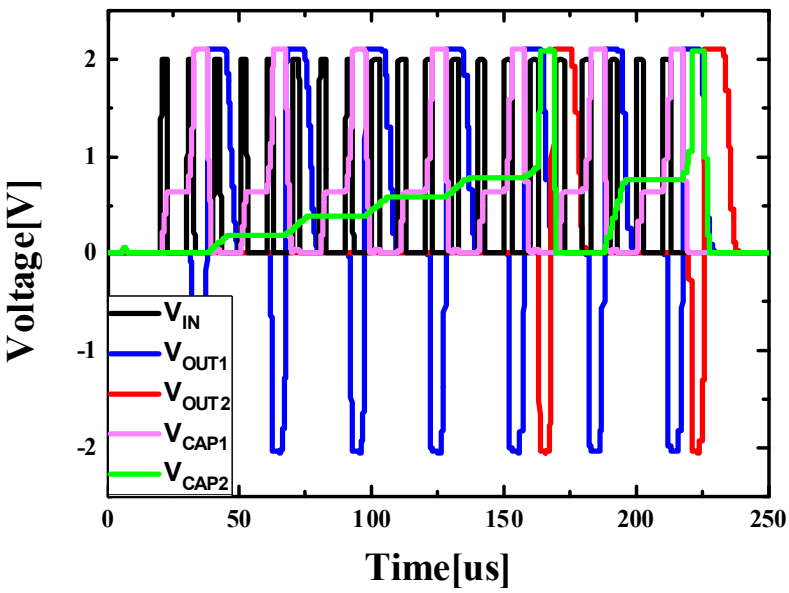

Figure 2.6. Potentiation of the synaptic device.

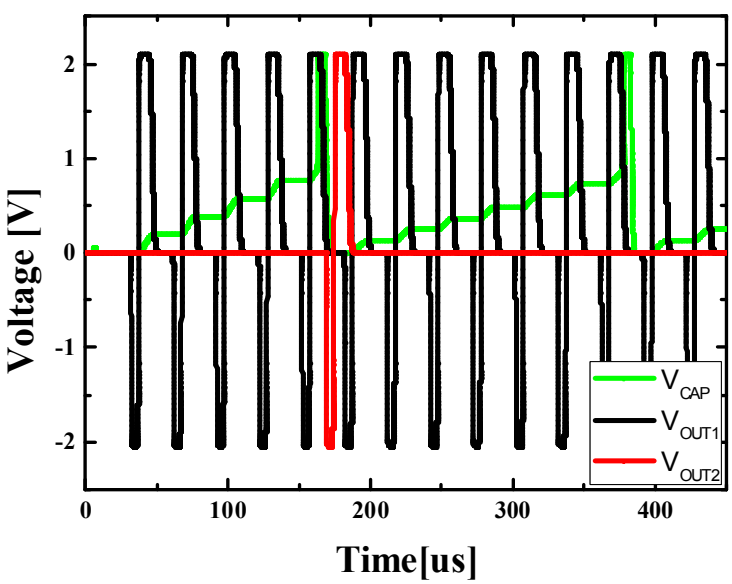

Figure 2.7. Depression of the synaptic device.

As shown in Fig 2.8, the weight from a well-established non-SNN can be transferred to SNN. If the non-SNN system, learned through the activation function of RELU, Sigmoid, etc., can be applied directly in the hardware based SNN, it has a great advantage in terms of power consumption and efficiency. By using two stage synapse as a synaptic integration part and changing only the weight of excitatory synapse, it is possible to implement +, – weight as in non-SNN. In Fig 2.9, it is shown how + and – weight can be implemented. First, the graph indicated by *Q(exc)* shows how much charge is accumulated in the membrane capacitor in one pulse by changing V_T of excitatory synapse. Secondly, using inhibitory synapse as a set with excitatory synapse, the charge accumulated on the membrane capacitor can be set to zero when there is no V_T change in excitatory synapse. Finally, if ΔV_T is positive, excitatory synapse will flow less current than inhibitory synapse, discharging the membrane cap. In the opposite case, if ΔV_T is negative, excitatory synapse will flow larger current than inhibitory synapse, charging the membrane capacitor.

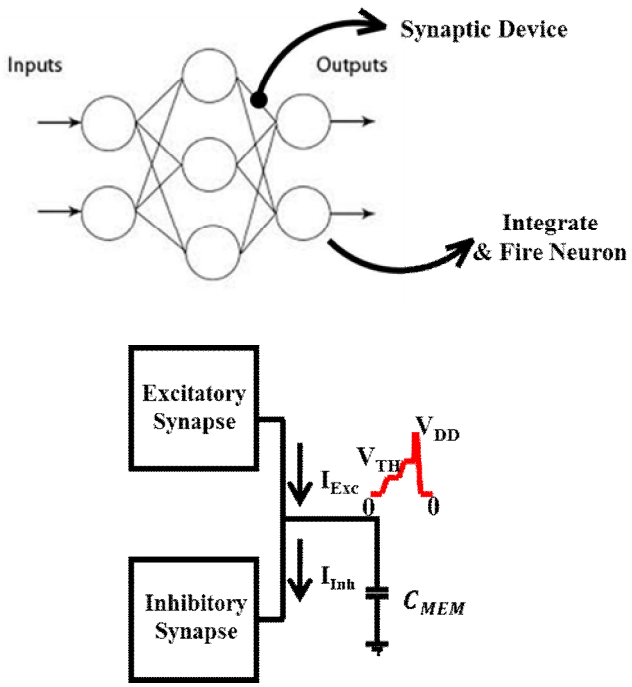

Figure 2.8 Schematic view of signal integration part to implement +, - weight.

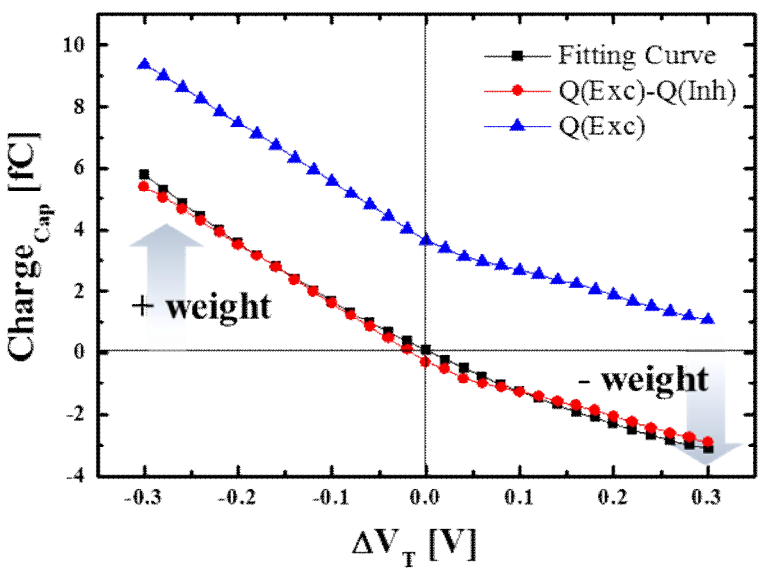

Figure 2.9 Weight transfer from software-based simulation

Weight map of 1-layer MNIST simulation in non-SNN is shown in Fig 2.10. The 1-layer MNIST pattern recognition simulation using MATLAB showed error rate of 7.33%, which means 733 of 10000 test samples were determined as errors. The Rectified Linear Unit(ReLU) is used as an activation function.

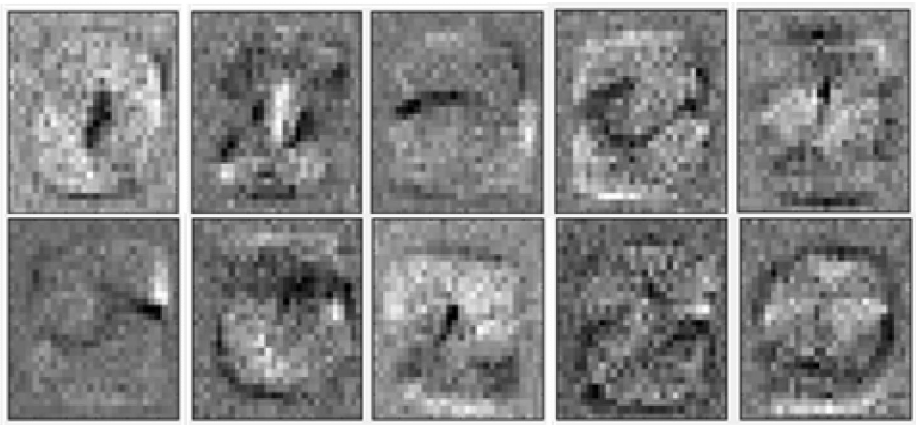

Figure 2.10. Weight map of non-SNN based 1-layer MNIST simulation (Error rate: 7.33%).

2.4. System Configuration

Synaptic device, neuron circuit, system configuration for +, – weight and weight transfer method can be used to form an overall neuromorphic system using SNN. In particular, for the + and – weight implementations, inhibitory synapse must flow the same amount of current as the excitatory synapse with $\Delta V_T=0$ when the signal is received. In order to construct inhibitory part serving as a constant current source, we composed pseudo-current source that can constantly discharge the membrane capacitor which is shown in Fig 2.11. By using synaptic device and simple current mirror, it can mimic the characteristics of the voltage controlled current source.

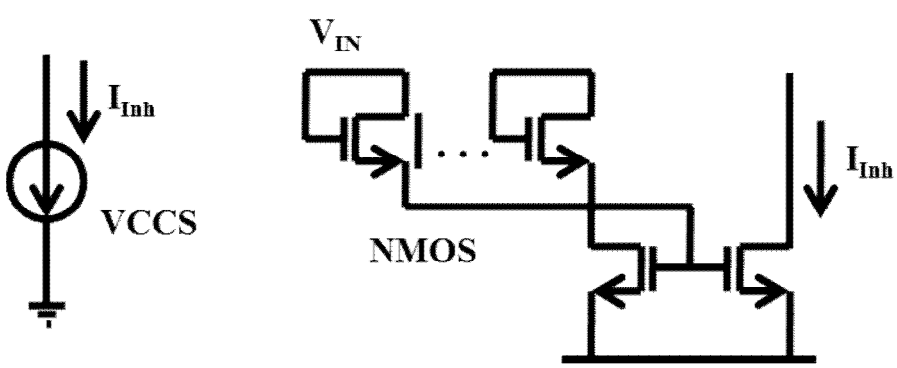

Figure 2.11. Inhibitory synapse connection to flow constant current.

In Fig 2.12, using the MNIST test sample, it is shown that the currents are same with VCCS and the pseudo-current source using the current mirror. With constant inhibitory current, V_T map of excitatory synapse which is shown in Fig 2.10 can be exactly given in SNN. Therefore, regardless of the spike generation part, the weight between layers can be determined in the integration part of the circuit. A comparison of MNIST pattern recognition test sample '0' using VCCS and the pseudo-current source in the neuron corresponding to the digit '4' is shown in Fig 2.13.

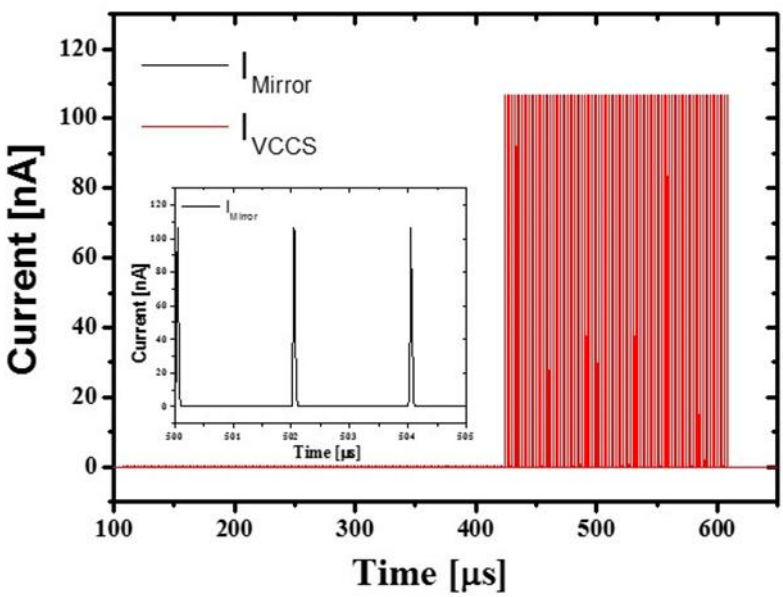

Figure 2.12. Compared I_{Inhitory}-T curves of Voltage Controlled Current Source and inhibitory part using current mirror.

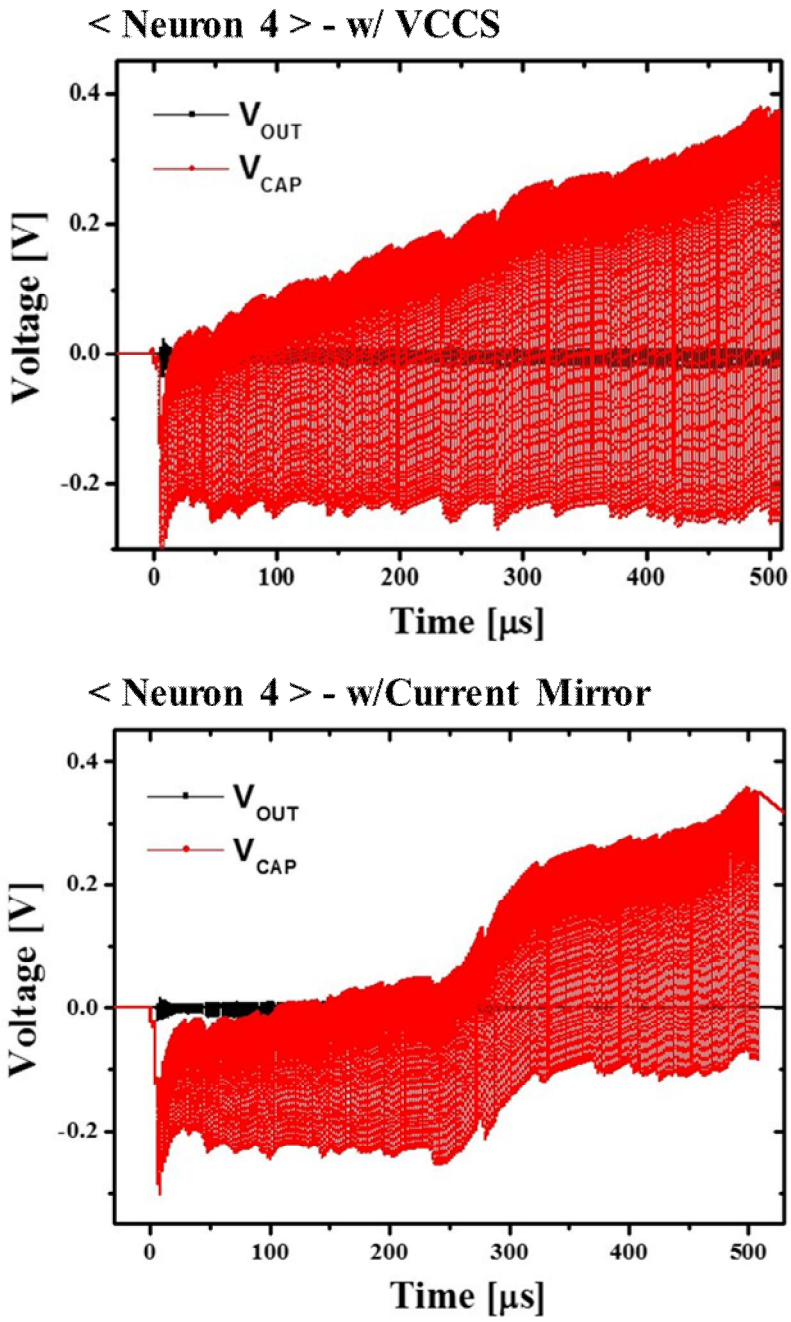

Figure 2.13. Comparison of membrane capacitor voltage of the MNIST test sample '0' using VCCS and pseudo-current source.

Chapter 3

Implementation of Neuromorphic System

3.1 1-Layer MNIST Pattern Recognition

Integrate and fire neuron circuit consists of integration part and spike generating part is used to implement neuromorphic system as mentioned above. In Fig 3.1, overall system construction is shown. Integration part receives input signal and integrate the current at membrane capacitor which consists of excitatory part and inhibitory part. In spike generating part, when the capacitor voltage is above threshold, a

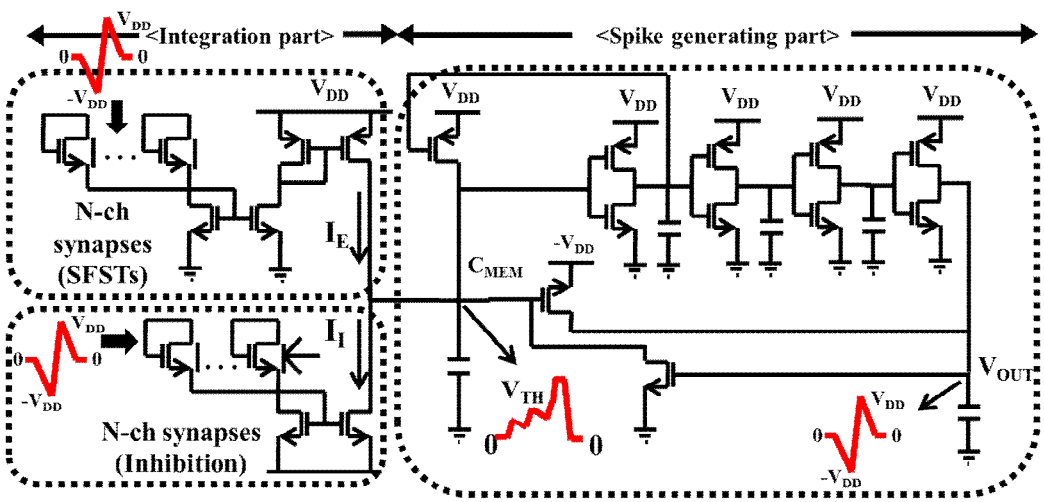

Figure 3.1. Integrate & Fire neuron circuit consists of integration part and spike generating part.

pMOS pulls up the capacitor voltage and series of inverter, nMOS, pMOS generate asymmetric output pulse. The MNIST is large database of handwritten digits which is commonly used for training image processing systems. In order to test 28 x 28 MNIST pattern recognition, input stage consists of 784 excitatory synapses. As shown in Fig 3.2, same number of inhibitory synapses are used to match excitatory synapse each. The pair of excitatory and inhibitory synapse represent one pixel of 28 x 28 MNIST pattern. The output stage consists of 10 equivalent neuron, each represent digit 0 to 9. By identifying the most frequently firing neurons among the 10 neurons, we can assert what digit the input is recognized as.

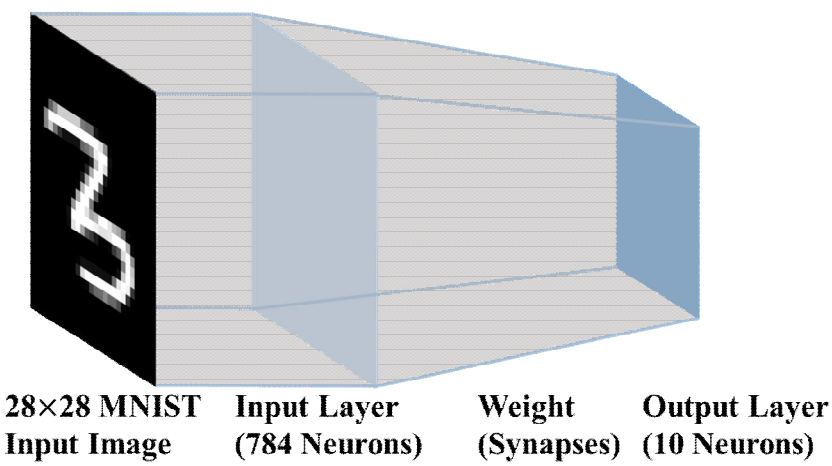

Figure 3.2. Schematic view of 1-layer MNIST pattern recognition simulation. Input stage consists of 784 synapses and output stage is constructed with 10 neurons.

3.1.1. Right-justified Rate Coding

By using spike rate coding, MNIST pattern recognition is conducted. Right-justified rate coding, which is also called frequency coding, is a traditional coding scheme assuming that stimulus is contained in the firing rate of the neuron as shown in Fig 3.3. Therefore, the stronger the signal intensity within a certain time scale, the greater the number of fires. Since it is proceeded with 256 gray scale, in the case of right justified rate coding, the signal comes in at regular intervals, and as the intensity of the signal increases, the signal starts to come in first. For example, the signal with the highest intensity produces 255 spikes, while the signal with the lowest intensity does not produce spikes. To ensure MNIST is implemented correctly at SNN, 14th MNIST test

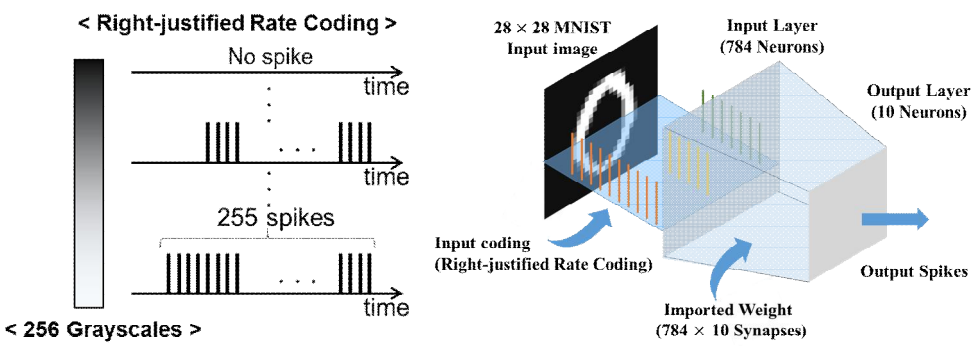

Figure 3.3. Schematic view of right justified rate coding and overall system configuration using synaptic device, neuron circuit, weight transfer method.

sample is verified. For the time scale, the process was performed from 255 times to 510us with 2us intervals per signal. In Fig 3.4, raster plot of MNIST test sample '0' is shown. Since right justified rate coding is used, more neurons tend to fire as they go to 510us. In the case of the 14th test sample, digit '0' enters as an input and the system correctly recognizes '0' as shown in Fig 3.4. MATLAB simulation of the SNN system shows that the neuron corresponding to '0' is the most likely to be fired compared to other neurons. Fig 3.5 and Fig 3.6 shows SPICE simulation result of the 14th test sample in neurons which represent digit '0', '2', '5', and '9'.

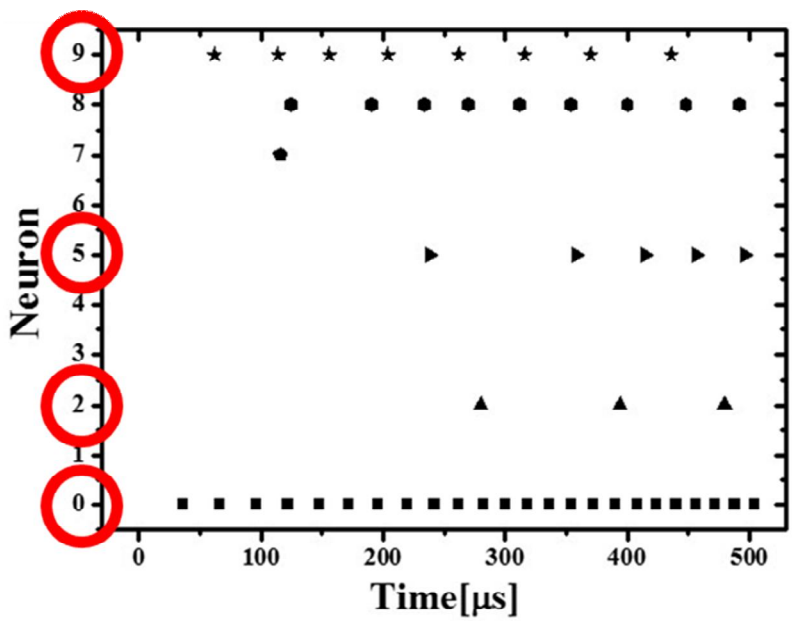

Figure 3.4. Raster plot of MNIST test sample '0' using right justified rate coding.

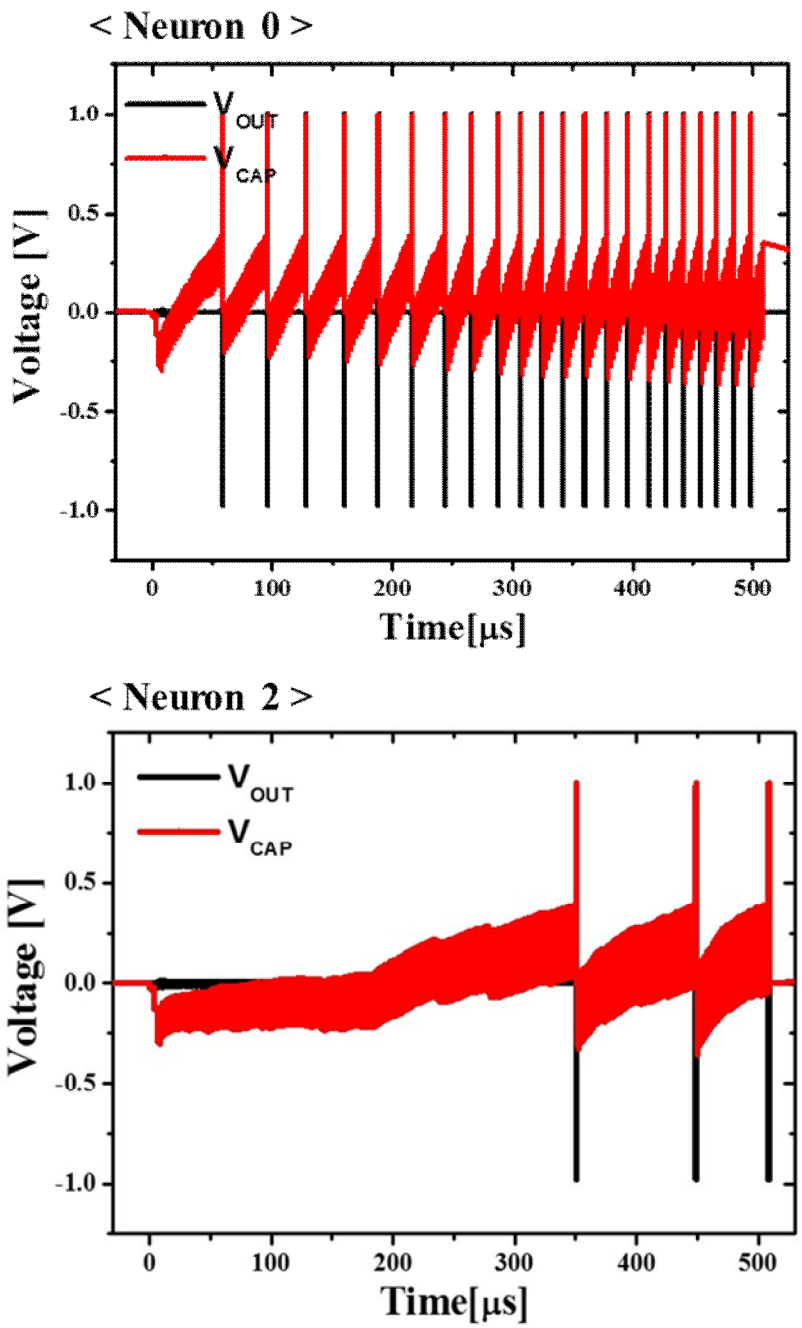

Figure 3.5. Membrane capacitor voltage of neuron 0 and neuron 2 with the MNIST test sample '0'. Right justified rate coding is used for input.

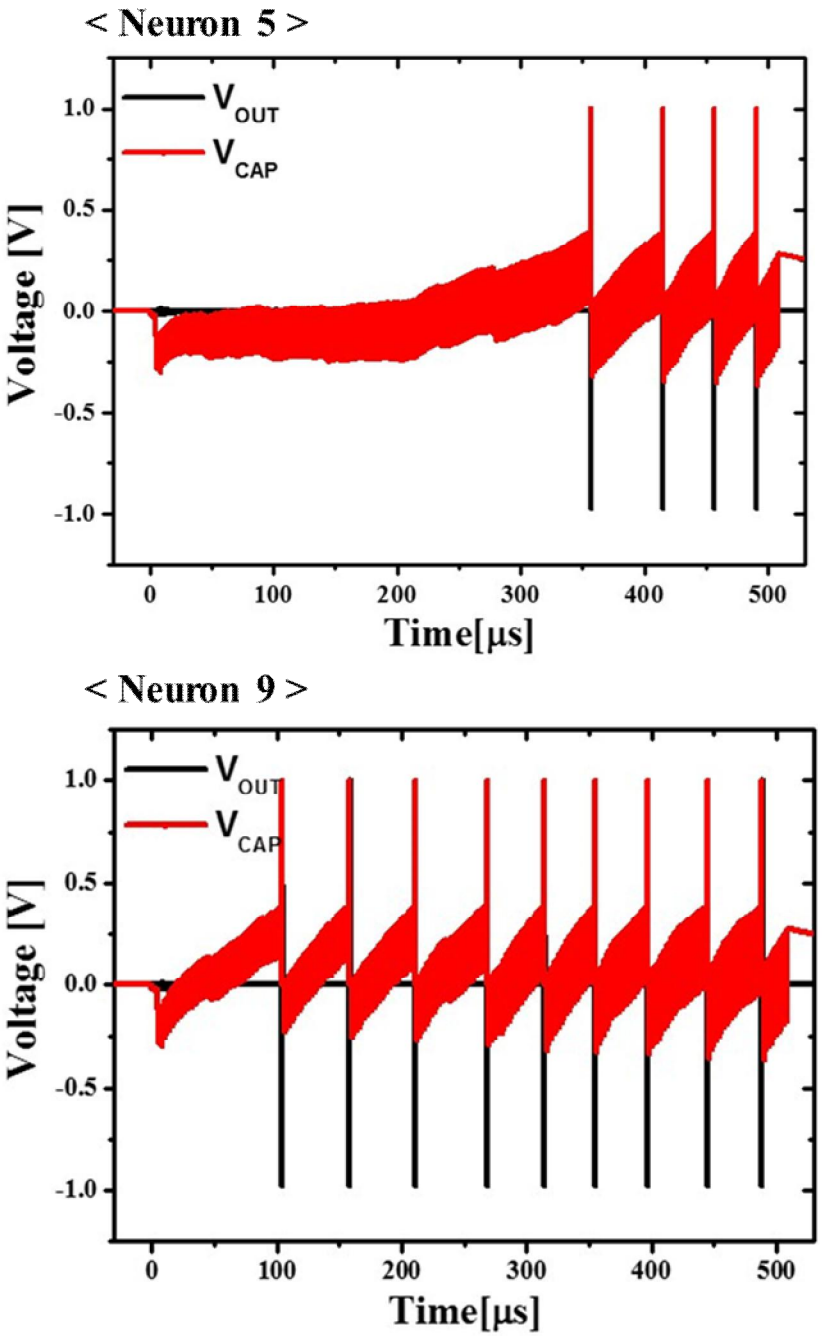

Figure 3.6. Membrane capacitor voltage of neuron 5 and neuron 9 with the MNIST test sample '0'. Right justified rate coding is used for input.

3.1.2. Left-justified Rate Coding

As with right-justified rate coding, the interval between signals is constant even with left-justified rate coding and multiple spikes begin to come out from the beginning as the signal becomes stronger. For example, in the case of the strong signal, spikes start to generate from 0us, and continue for as long as the intensity of the signal as shown in Fig 3.7. In Fig 3.8, raster plot of the 14th test sample when using left-justified rate coding is shown. Unlike Fig 3.4, since left-justified rate coding is used, it is shown that neurons are less fired as they go to 510us.

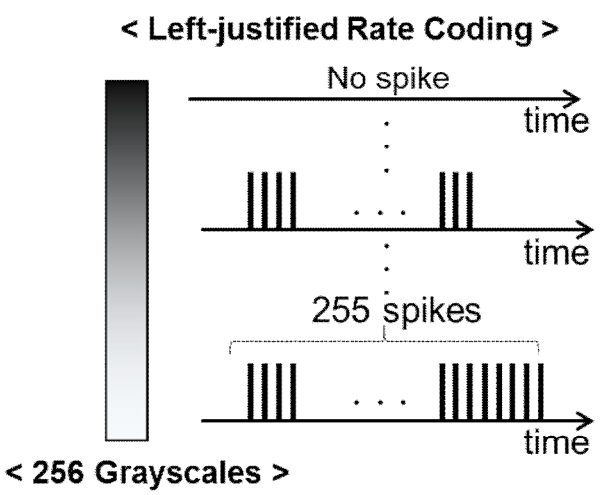

Figure 3.7. Schematic view of left justified rate coding.

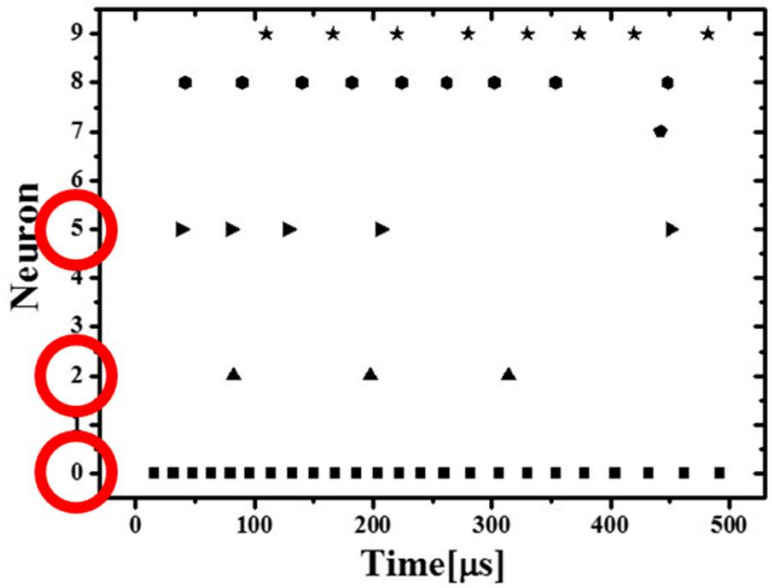

Figure 3.8. Raster plot of MNIST test sample '0' using left justified rate coding.

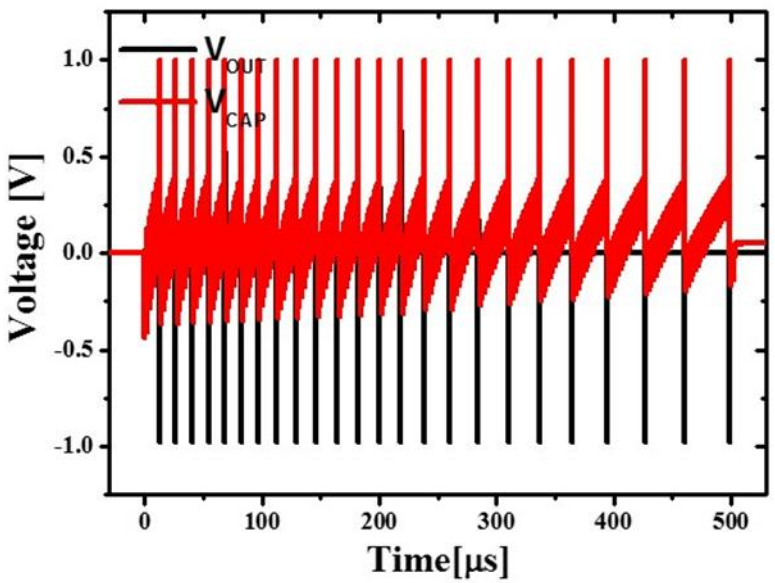

Figure 3.9 Membrane capacitor voltage of neuron 0 with the MNIST test sample '0'. Left justified rate coding is used for input.

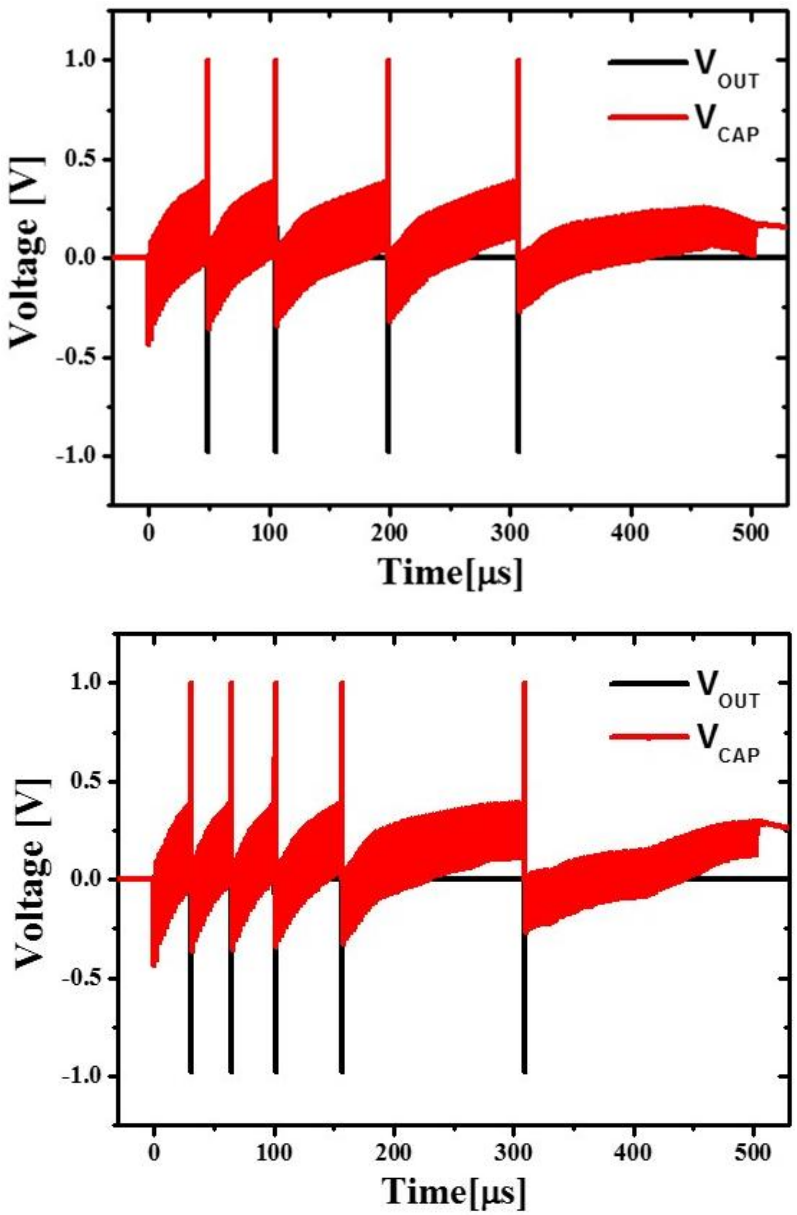

Figure 3.10 Membrane capacitor voltage of neuron 2 and neuron 5 with the MNIST test sample '0'. Left justified rate coding is used for input.

In Fig 3.9 and Fig 3.10, it is verified that the simulated neuromorphic system can equivalently reflect the software based non-SNN simulation which used RELU as a activation function. Compared with Fig 3.8, although the number of firing is not exactly the same, circuit simulations show that the neurons fire at almost the same rate as the non-SNN, recognizing handwritten digit '0' correctly. As with right-justified rate coding, the most frequent firing occurred in the case of neuron 0, and the 14^{th} test sample corresponding to '0' was confirmed to be well-checked by the system.

SNN-based SPICE simulations and non-SNN based MATLAB simulations show equivalent results, which means that weights in well-established non-SNNs using back-propagation can be appropriately transferred to the SNN.

3.2 Overflow Retaining Neuron Circuit

In Fig 3.11, overflow retaining neuron circuit with different structure of spike generating part from the conventional neuron circuit is shown. By setting virtual membrane node differently from conventional neuron circuit, spikes can be generated independently of the membrane capacitor voltage. In the overflow retaining circuit, the membrane capacitor merely integrates the signal coming from the integration part, and when the neuron fires, the capacitor discharges only by V_T. Also, even though the value of the membrane capacitor is near V_T through the inverter stage, the voltage is pulled up to V_{DD} at virtual membrane node, so no separate feedback device is needed.

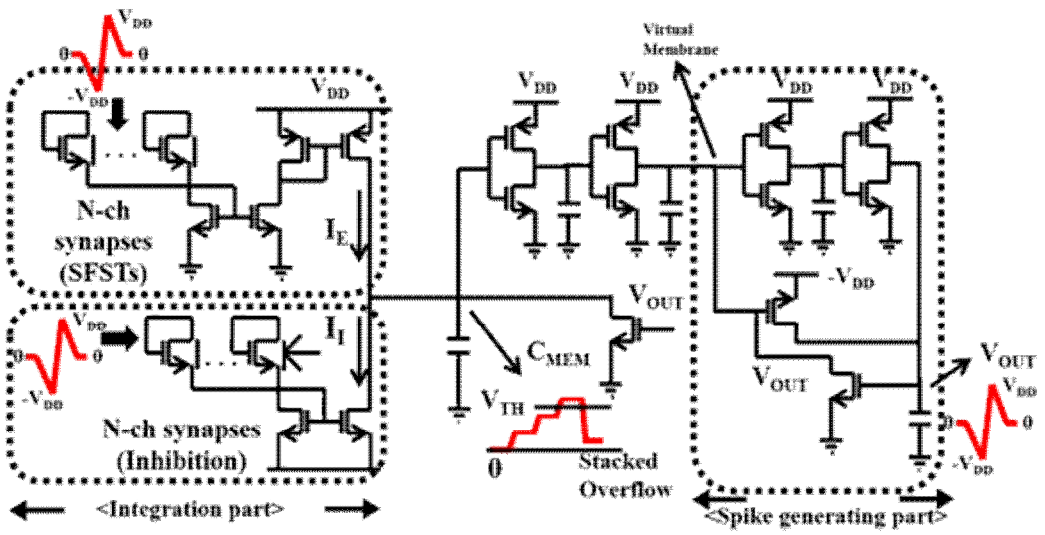

Figure 3.11. Overflow retaining neuron circuit.

For the rest of the operation, it operates in the same way as the circuit shown in Fig 2.1. Through the two cascaded inverter stages, virtual membrane node can be defined, which can produce the same output pulse as the previous neuron circuit. At the same time, in the case of the membrane capacitor node, the integration of the signal and the discharge of capacitor can proceed independently. The reason why the discharge must occur in the capacitor only by V_T is shown in Fig 3.12. When the neuron fires, if the incoming signal exceeds V_T, the remaining signal is wasted. In the case of conventional neuron circuit, if V_T is exceeded, membrane capacitor node will be unconditionally pulled up to V_{DD} so there will be a wasted signal every time neuron is fired. However, in the case of

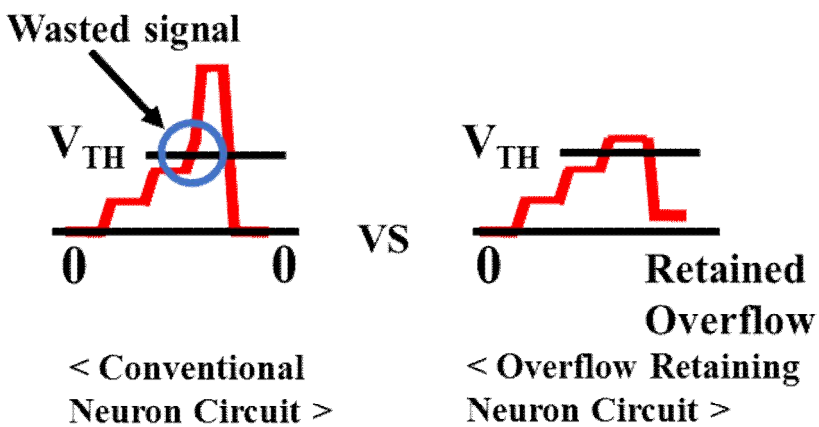

Figure 3.12. Comparison of membrane capacitor voltage of conventional neuron circuit and overflow retaining neuron circuit.

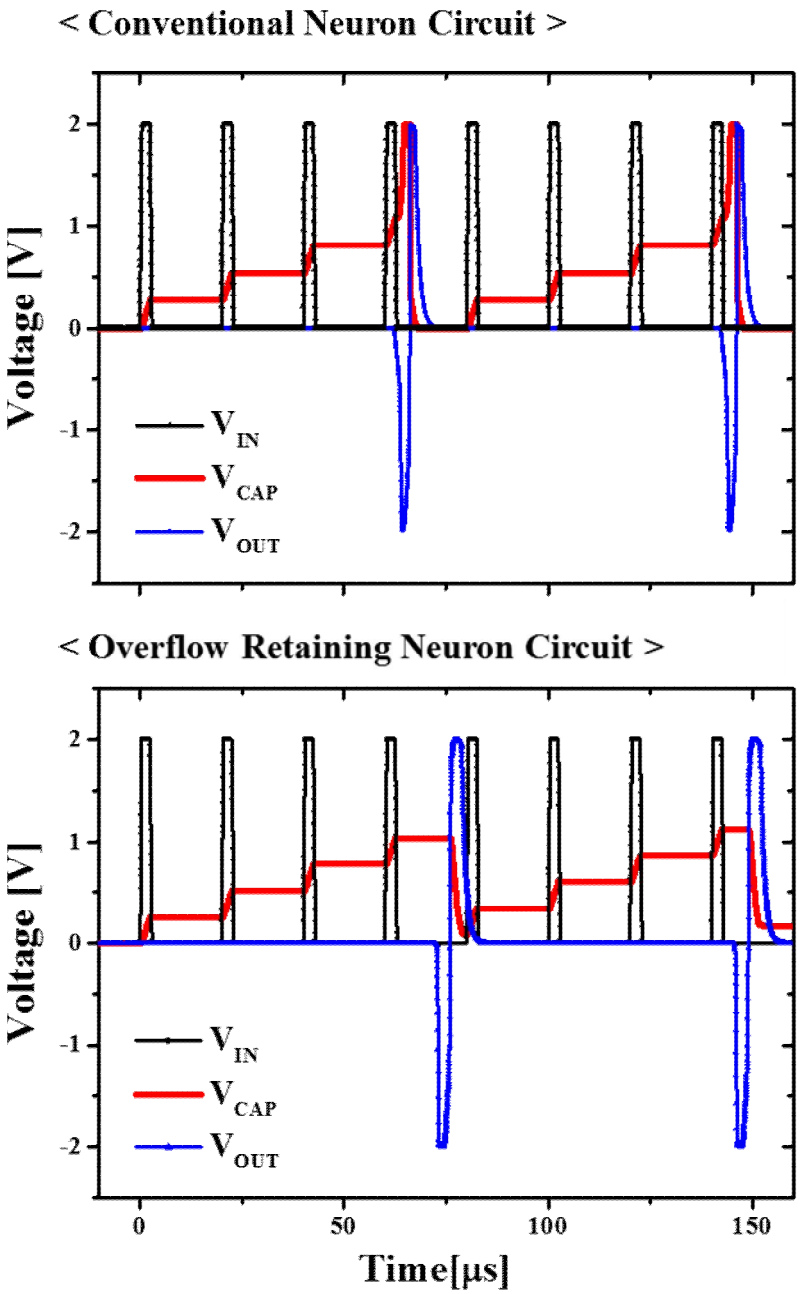

Figure 3.13. Comparison of simulated membrane capacitor voltage of conventional neuron circuit and overflow retaining neuron circuit.

overflow retaining neuron circuit, the virtual membrane can replace the membrane of the conventional neuron circuit, allowing the membrane capacitor node to be discharged only at V_T when neuron is fired. In Fig 3.13, comparison of the simulated membrane capacitor voltage of conventional neuron circuit and overflow retaining neuron circuit is shown. Since the overflow retaining circuit discharges exactly VT, the overflow can be stably maintained without the wasted signal. At the same time, it can be confirmed that asymmetric output pulse is generated as well as conventional neuron circuit.

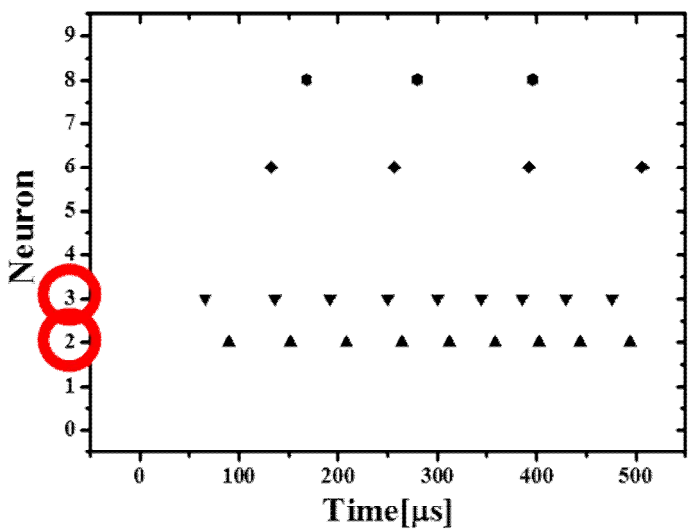

Figure 3.14. Raster plot of MNIST test sample '3' using right justified rate coding and conventional integrate and fire neuron circuit.

From Fig 3.14 to Fig 3.17, 529th test sample is used which is handwritten digit '3', but '2' or '3' is determined by a very fine difference. In Fig 3.14, raster plot of the MNIST test sample '3' is shown. Right-justified rate coding is used with conventional integrate and fire neuron circuit. However, this test sample concludes that the neuron 2 and neuron 3 fired the same number of times, which turns out to be an error. On the other hand, when overflow retaining circuit is used, it can be seen from the Fig 3.15 that the neuron 3 is fired once more than the neuron 2, so that it is recognized correctly.

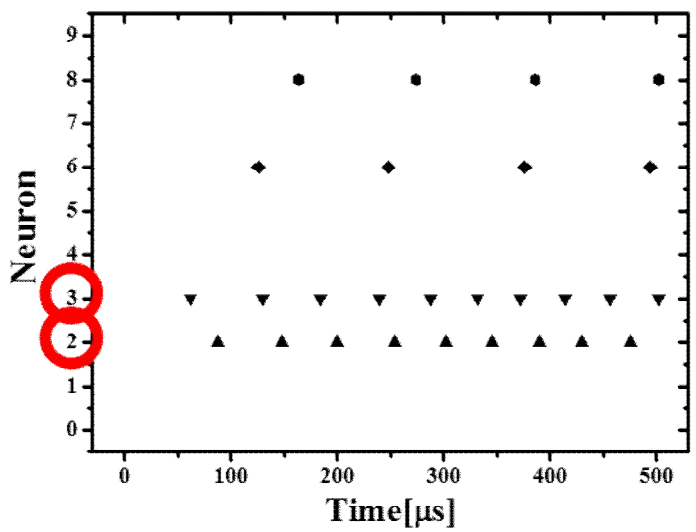

Figure 3.15. Raster plot of 529th test sample using right justified rate coding and overflow retaining neuron circuit

As in the previous 14^{th} test sample, it is shown in Fig 3.16 and Fig 3.17 whether the same result as the raster plot is obtained in the actual SPICE simulation. In Fig 3.16, as in Fig 3.14 which uses conventional integrate and fire neuron circuit, the neuron 2 and neuron 3 fired the same number of times and recognized as an error. On the other hand with overflow retaining neuron circuit, it is verified in Fig 3.17 that it recognizes the digit '3' correctly like raster plot in Fig 3.15 by keeping the overflow.

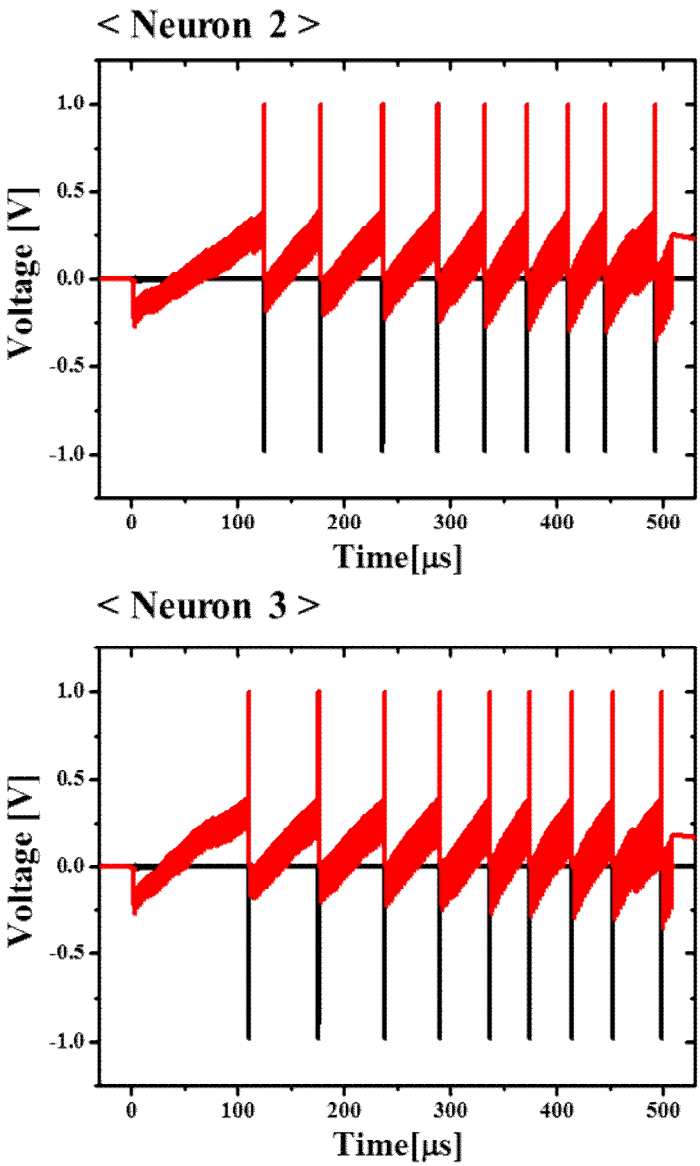

Figure 3.16. Membrane capacitor voltage of neuron 2 and neuron 3 with MNIST test sample '3'. Right justified rate coding is used for input.

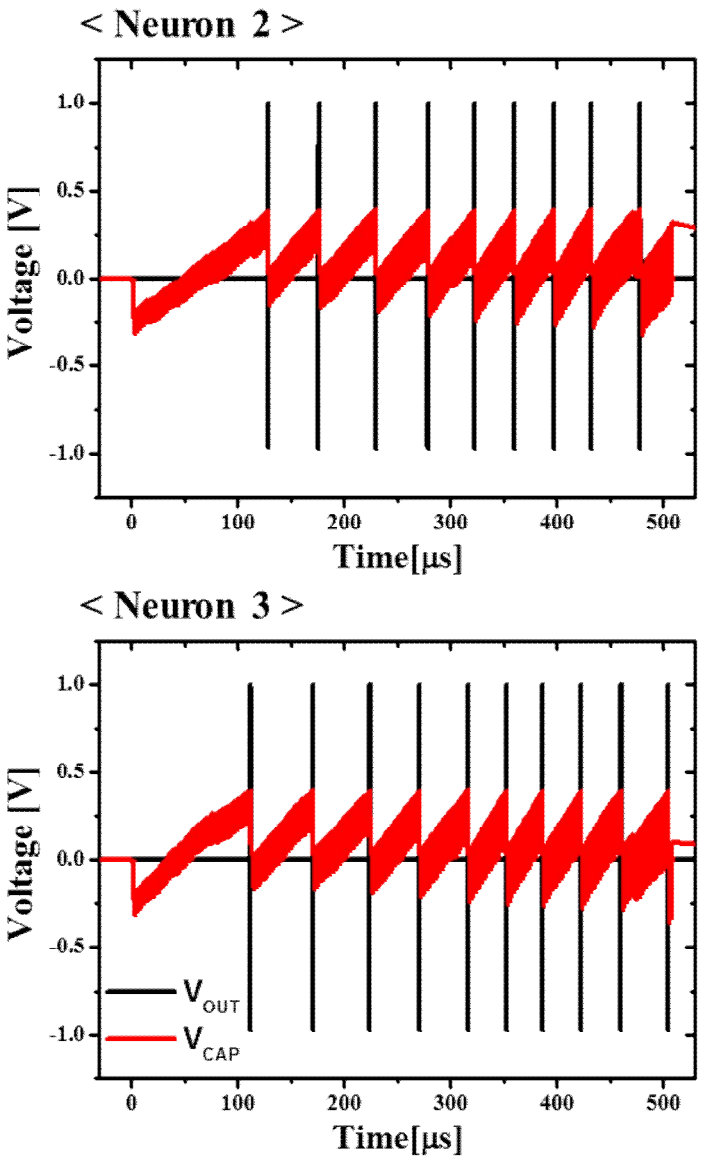

Figure 3.17. Membrane capacitor voltage of neuron 2 and neuron 3 with MNIST test sample '3'. Right justified rate coding is used for input.

Chapter 4

Conclusions

In this thesis, neuromorphic system has been introduced which can perform MNIST pattern recognition. In addition, the overflow retaining neuron circuit which can improve the accuracy more easily through simple structure change have been demonstrated. This system implemented by SPICE simulation can be used not only for MNIST pattern recognition but also for all kinds of artificial neural network related systems such as voice recognition, face recognition at hardware level instead of software. The STDP characteristics that can modulate synaptic weight, are analyzed in SPICE simulation by connecting previously proposed synaptic device and neuron circuit. The weight can be determined by V_T of the synaptic device and it is confirmed that + and – weight in the software can be equivalently implemented in SNN system, through inhibitory part of the neuron circuit. Also, 1-layer artificial neural network is specifically investigated by implementing 1-layer SNN neuromorphic system using SILVACO SMARTSPICE simulation tool. In the simulation result, the result of MATLAB

simulation and SPICE simulation are almost the same. In order to increase the accuracy, the operation of the overflow retaining neuron circuit to minimize the wasted signal is confirmed. Case study shows that overflow retaining neuron circuit improves the accuracy MNIST pattern recognition.

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초 록

인간을 대신할 수 있는 음성 인식, 얼굴 인식, 자율 작업과 같은 인공 지능 기술은 큰 화제를 불러 일으켜왔고, 세계적인 추세에서 미래의 산업 시장을 바꿀 것이다. 하지만 폰 노이만 구조에 기인한 현재의 컴퓨팅 시스템의 경우에는 파워 소모와 효율성 측면에서 문제점을 보여왔다. 특히 고차원적인 연산을 수행할 때 많은 양의 정보를 처리하면서 비효율성과 큰 전력 소모로 일어나게 되는 폰 노이만 병목 현상은 새로운 인공지능 시스템을 야기하였다. 뉴로모픽 시스템의 효용성을 확인하기 위해 시냅스 소자와 뉴런 회로로 구성된 스파이킹-뉴럴-네트워크에 대해 면밀하게 연구하였다. 전자회로 시뮬레이션을 통해 손글씨패턴인식을 진행하였을 때, 뉴로모픽 시스템이 MATLAB을 통해 구현한 인공신경망과 같은 결과를 보임을 확인하였다. 이것은 소프트웨어 기반으로 구현된 모든 인공지능 시스템을 하드웨어적으로 그대로 옮겨와서 구현할 수 있음을 의미한다. 또한, 손글씨패턴인식의 정확도를 개선하기 위해, overflow retaining 뉴런 회로를 제안하였다. 간단한 회로 구조의 변화를 통해 가상의 노드가 적절하게 동작하였으며, 기존의 integrate and fire 뉴런 회로와 다르게 낭비되는 신호를 최소화 하였다. 이러한 사실은 MATLAB 시뮬레이션에서 추출한

raster plot과 전자회로 시뮬레이션의 결과를 비교함으로써 확인되었고 다른 인공신경망 구조가 하드웨어적으로 구현될 수 있음을 의미한다.

주요어 : 뉴로모픽 시스템, 스파이킹 뉴럴 네트워크, 뉴런, 시냅스, 과도신호 유지.

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