이학석사학위논문

Quantum dot qubit devices implemented in semiconductor heterostructures

반도체 적층구조에 구현한 양자점 큐비트 소자 연구

2018 년 2 월

서울대학교 대학원

물리천문학부

이 명 원

Contents

Abstract

To realize the universal quantum computation, it is necessary to achieve the called quantum bit or qubit in a physical system. Semiconductor heterostructure with 2-dimesional electron gas(2DEG) are possible candidates for the qubit system. In this thesis, AlGaAs/GaAs and Si/SiGe heterostructures are investigated for qubit implementation. Apparatus for low-temperature experiment and measurement electronics are demonstrated. Electromagnetic field simulation

using Finite Element Method(FEM) is done for high frequency measurement circuit and sample design. Procedures for sample fabrication are also illustrated. Finally, Characteristics of the sample was analyzed through high frequency and quantum hall measurement in low temperature. Measurement result showed that single electron control in quantum dot and future qubit application of the device are possible in AlGaAs/GaAs system. Quantum hall measurement on Si/SiGe structures confirmed 2-dimentional transport in the structure and possibility of the wafers for the future quantum dot qubit devices.

Introduction

Advances in nanotechnology and quantum manipulation make it possible to realize quantum bit (qubit) in physical systems. In this these, we use semiconductor heterostructures to

realize qubit. In the semiconductor system, the state of single is manipulated to implement the qubit. The quantum dot system realized in this way can be applicable to quantum computing [1] and quantum simulation for artificial physical system [2].

The background for readers to understand quantum dot qubits is presented in Chapter 1. Chapter 2 covers the experimental setup for low temperature experiment and sample preparation. The measurement results are explained separately for GaAs and SiGe systems. Chapter 3 deals with details of methods for quantum dot measurement and results in GaAs systems. In chapter 4, quantum hall experiment in SiGe systems are discussed. Finally, chapter 5 summarizes the results and experiences from the experiment. Highlighting the problems and challenges the experiment, future works are also suggested.

Chapter 1

Background for quantum dot qubit

This chapter gives brief introduction to qubit especially implemented in semiconductor platform. The principle of 2-dimensional electron gas is presented and quantum dot qubit structure in it is covered

1.1 Quantum computing with quantum object

Quantum mechanical two level systems that fulfill the requirement for qubit can be found in various fields of physics. Recent advances in superconducting qubit [3] [4] reveals that it is robust platform for quantum computing, for its long coherence time and scalability. Qubit using nitrogen vacancy center(NV) in diamond is an attractive candidate for quantum computing[5] because it can operate at room temperature.

Semiconductor quantum dot qubit, which is the main subject of this thesis, is also a promising candidate for qubit though it has relatively short history. [6, 7]

1.2 Qubit implementations in semiconductor heterostructures

1.2.1 2DEG in semiconductor heterostructures

2-dimensional electron gas(2DEG) is an experimentally realized 2D system in semiconductor. 2DEG is a thin layer of electrons which can move freely in a 2-dimensional direction. Electrons in 2DEG encounter no hard-scattering events, so it has high carrier mobility up to $3 \times 10^7 cm^2/Vs$ for AlGaAs/GaAs wafer at cryogenic temperature[8]. This high mobility corresponds to mean free path of 0.3mm, which is long enough for transport in 2DEG to be considered ballistic. This fact is very important because quantum dot experiment measures the quantum

phenomena which can be seen at quantum regime that transport considered ballistic. 2DEG wafers are grown using Molecular Beam Epitaxy(MBE) for GaAs or PECVD for SiGe to make clean crystal structures. Figure shows the band structure of GaAs/AlGaAs heterostructure. The GaAs and AlGaAs are joined about 100nm below the surface, with conduction band of AlGaAs is much high than that of GaAs. Doping layer in AlGaAs gives the free electrons into the structure. The diffused electrons from the delta-doped layer fall into the band gap and become trapped by the band gap ΔE between the heterojunction. By this mechanism, electrons are confined in the GaAs conduction band. Having lost electrons by diffusion into the structure, Si donor layer forms a sheet of positive charge, making no further diffusing back to the surface direction. This forms the 2-dimensionally confined electron layers, that its electrons can move freely in 2-dimensional direction but trapped in vertical way. At low temperature, only the lowest mode in potential occupied and

electrons form a 2D Sheet. Although donors are the main scattering source in semiconductor, with 2DEG structure that having the donor layer far away from the conduction channel can have very high mobility.

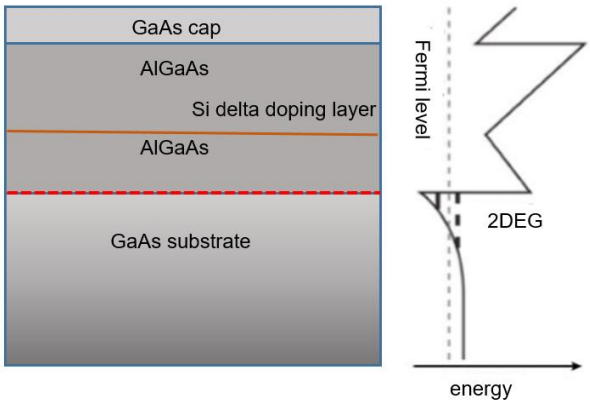


Figure 1.1 band diagram of AlGaAs/GaAs system

To confine the electrons in 2DEG for forming a quantum dot, lateral depletion gates are fabricated on top of the heterostructure. Gate sizes range down to tens of nanometer, to making the any artificial structure to form quantum dots.

1.2.2 Lateral quantum dots in 2DEG

By applying voltages to the depletions gates which are on top of the device, quantum dot can be formed within the 2DEG. Quantum dot means a small island of 2DEG with discrete energy levels. The energy levels of quantum dot become discrete if the size of the dot is of the order of the de Broglie wavelength $\lambda = h / 2m_c^* E$ of electron, E is for energy and m_c^* stands for effective mass. The figure illustrates the schematic picture of the quantum dot devices.

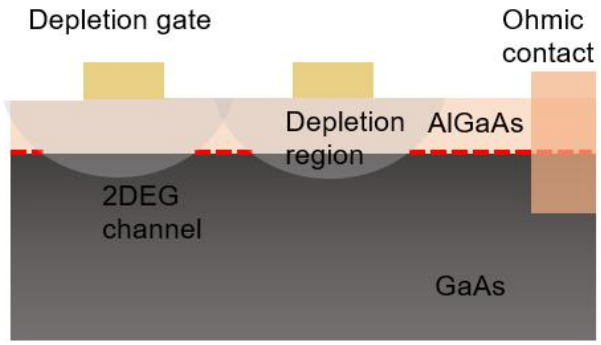


Figure 1.2 Schematics of lateral gate structure

Because of Coulomb repulsion of the electrons inside the dots, the energy needed to add an additional electron to the dot become relatively high, so it results the phenomenon called 'coulomb blockade'

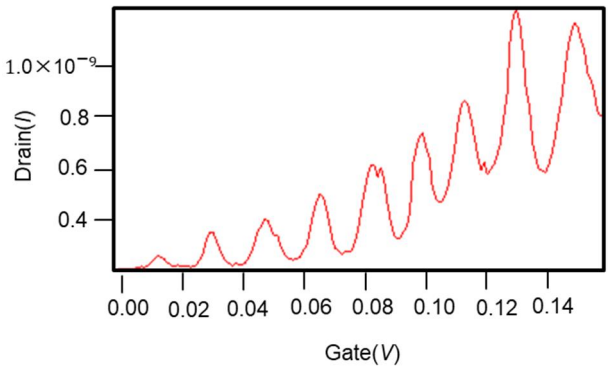


Figure 1.3 Coulomb Blockade in quantum dot

Chapter 2

Preparations for the experiment

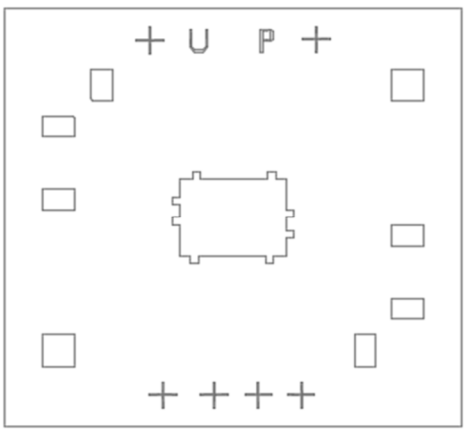
This chapter covers overall preparations for quantum dot measurement at low temperature. Procedures from sample design to fabrications are discussed. Hardware setup for the experiment and protocol for sample preparations are also presented.

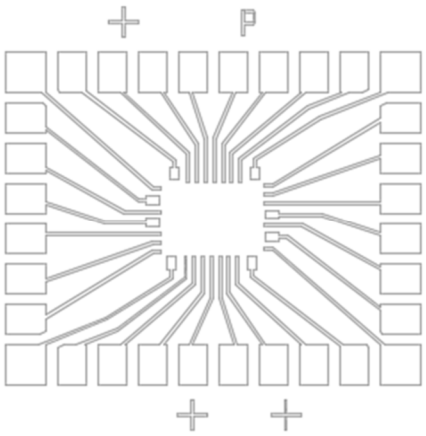
2.1 Sample design and simulation

2.1.1 Sample design

Designing the sample structure consists of two parts; one for the patterns large enough to be done with photolithography, and the other for e-beam gate. Firstly, the overall structure of the sample need to be designed to make a photomask for fabrication.

In this step, the number of the ohmic contact and depletion gate is determined. Once ohmic contacts are positioned and photomask is made, the number of contact pad for wire bonding is fixed.





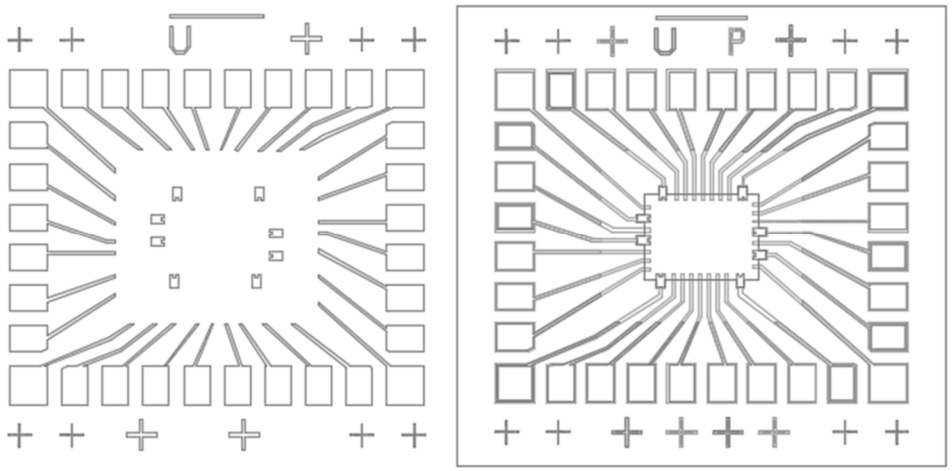


Figure 2.1 Mask design for Photolithography

The next thing is to design the depletion gates geometries. Gate layout is crucial for successful experiment. The shapes and size, distances between gates should be designed properly.

The best layout uses the as few as possible gates to form a quantum dot. Although complicated structure can control the dot more sophistically, it

To sum all these factors, designing the structure with trial and error is not the best solution. The FEM tool for simulating the electrostatical environment can help design the gate structure.

2.1.2 Finite Element Method (FEM) simulation

Finite element method is a numerical method to find the solution of deferential equations in engineering and physics. To solve the problems, FEM divides the structure into small and simple parts called finite elements. The relatively simple equation for finite element are then assembled into the larger equation for entire systems. FEM typically deals with heat transfer, strain, mass flow and electromagnetic potential. In the quantum dot experiment, FEM can also tribute to find out the numerical solutions for electrostatic potential in semiconductor heterostructure [9]. In this experiment, the commercial program named COMSOL Multiphysics are used. It has powerful numerical solver for complexed multi-physics problem which

has more than two equations to solve for the system. The FEM is used to get a solution for Maxwell's equation for gate structure. However, the information needed for designing the structure is not a potential landscape but charge distribution. To get information for charge distribution in heterostructure, Thomas-Fermi approximation is applied. By converting the potential into charge density, it provides reasonable prediction for the system. For simulation, 2DEG heterostructure is modeled and physical property like dielectric constant for each material is set. Numerical solver finds the solution for applied gate voltage then convert into the charge density using Thomas-Fermi equation [10].

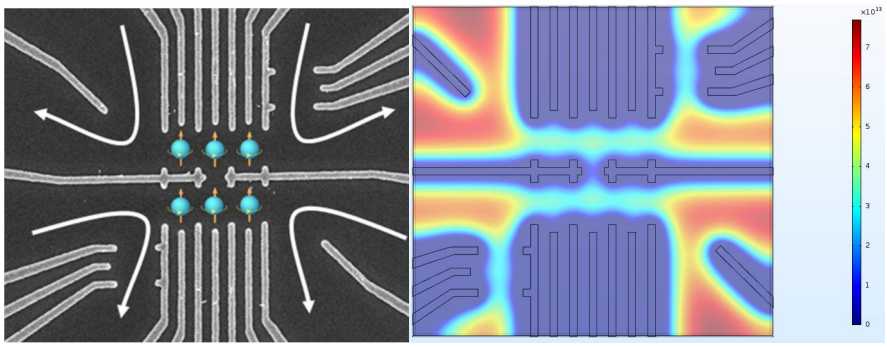


Figure 2.2 Simulated potential profile in quantum dot

Figure shows the simulated charge distribution with SEM image of real device. By controlled the gate size, distance between the gates and voltage applied to each gate, optimal structure for quantum dots could be estimated.

2.2 Fabrication on semiconductor heterostructures

To make quantum dot devices, fabrication process including nano-size patterning in required. This chapter describes the general fabrication process for GaAs sample. The fabrication of

quantum dot devices consists mainly three parts: mesa etching, making ohmic contact, and e-beam gate lithography. The process for SiGe is not that different except it uses oxide as gate dielectric. The additional parts for SiGe are presented in Chapter 4.2

2.2.1 Mesa etching

The defined 2DEG region called 'Mesa' is form using wet etching. Making mesa pattern restricts the conduction through the 2DEG by remove the other uninterested part of the wafer. It can reduce the noise of the sample by removing the channel's capacitive coupling to entire wafer and confining the conduction.

The etching process is done by wet etching process. Dry etching could be also used, but for GaAs sample it is much

Mesa pattern is made by photolithography.

2.2.2 Ohmic contact formation

Making the Ohmic contact is the crucial step because it connects the sample to macroscopic world to measure the sample electrically. It is important to not degrade the 2DEG quality during the process for it uses annealing at high temperature to make ohmic contact.

The process is executed in three steps. Firstly, the pattern is made by photolithography, then metal layers for contact are evaporated on it. Finally, by diffusing the metals into the wafer using rapid thermal annealing is done.

2.2.3 E-beam gates

E-beam gates are made for the last step. It uses e-beam lithography for pattering the fine gate. E-beam lithography has a similar process with photolithography while it uses electron beam to change the structure of resist. Figure depicts the general e-beam lithography process.

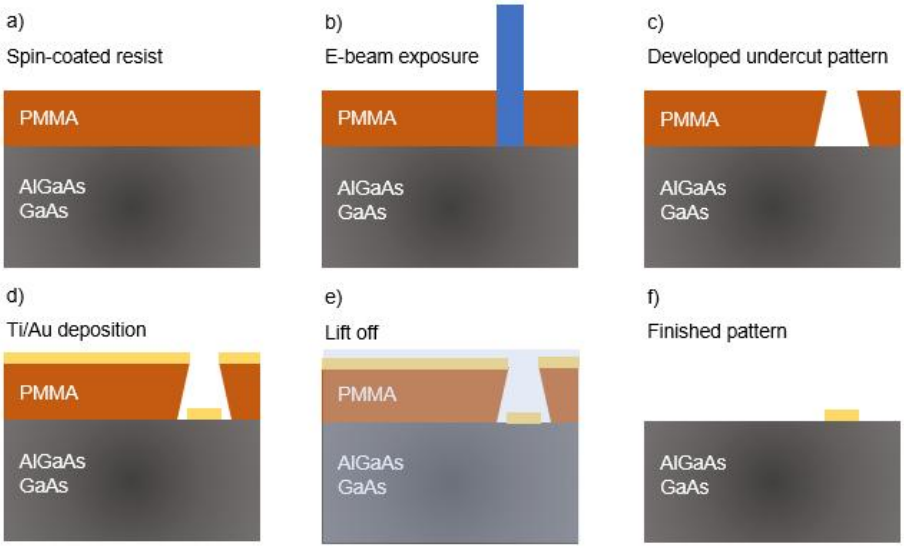


Figure 2.3 Procedure of E-beam lithography

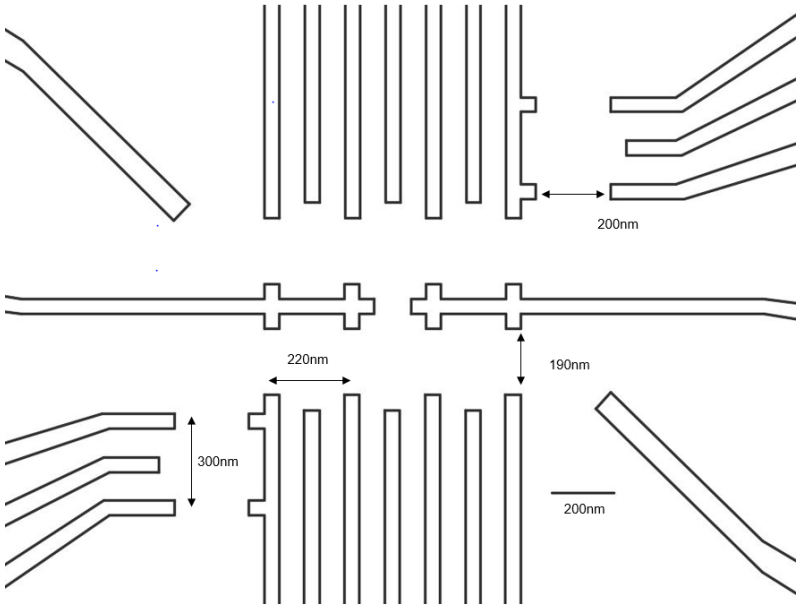


Figure 2.4 Fine Gate design for quantum dot

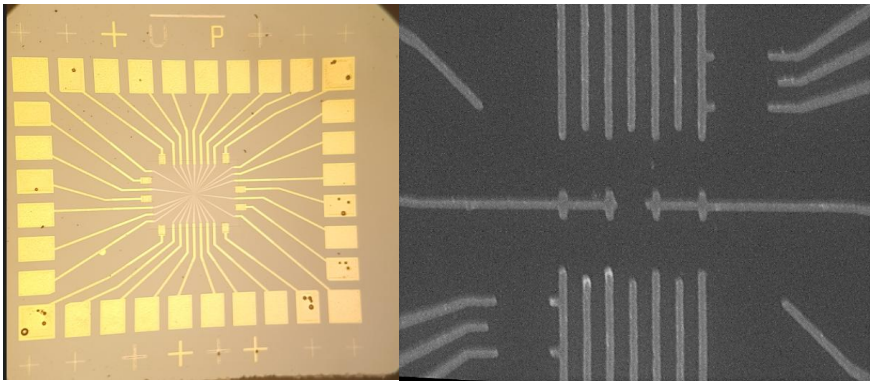


Figure 2.5 Optical and SEM image of the completed sample

2.3 Sample preparation and wire bonding

2.3.1 Sample preparation

The devices were mounted on the sample PCB using GE varnish. Ge Varnish is epoxy for low temperature applications. It has high thermal conductivity and stability even at millikelvin. To make thermal contact between sample and PCB as good as possible, varnish is mixed with acetone or isopropanol(IPA). The mixed varnish applied on PCB and forms a very thin layer on PCB. Sample is then carefully mounted on it because GaAs sample is extremely fragile. The Sample should be horizontally flat, for easy wire bonding. Finally, the sample is inspected for dirt or contaminations.

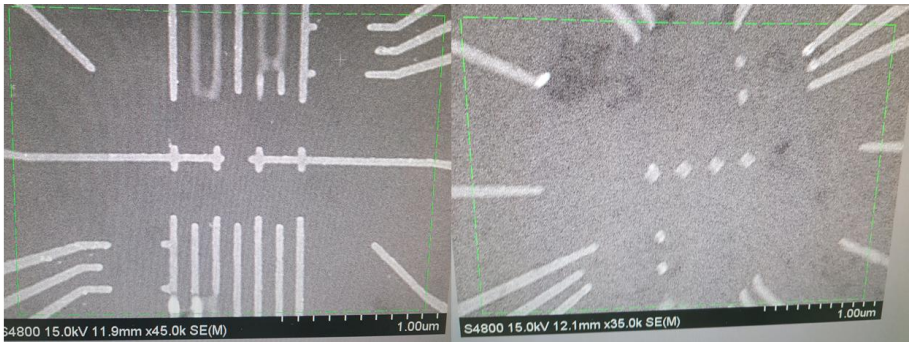


Figure 2.6 SEM image of damaged fine gate

Quantum dot devices are likely to be damaged by electrostatic discharge because of densely distributed metal structure. It is one of the common failure modes in the experiment. To avoid these, Extreme care must be taken when wire bonding, handling and loading. Ground straps need to be worn and lab's humidity should be maintained properly. Figure show the SEM image of the samples which are damaged during handling or loading.

2.3.2 Wire bonding

Wire bonding is the process that connecting the nanostructure of the sample to the PCB. As mentioned previous chapter,

quantum dot devices could be easily damaged by static. Additional care needed to protect the sample during bonding. Ground line that connect all the gates to the same electrical ground with wire bonder itself was used for safety. Wedge bonder is used because it uses ultrasonic to bond the material so safer in static issue than ball bonder which uses electrical discharging during process.

Wire bonding for the quantum dot sample has several rules. The one major issue is that RF line is already fixed in PCB so in some configuration, the bonding across the other lines is inevitable. These cross lines could be the noise source during measurement. Bonding pads are very small size, so it is needed to bond the rightly on pad's middle site. Failure in bonding is showed in Fig. For successful measurement, the right boding map should be made with these factors considered. The detailed description is in Appendix B. Once the sample is done with bonding, it is ready to be loaded on dilution refrigerator.

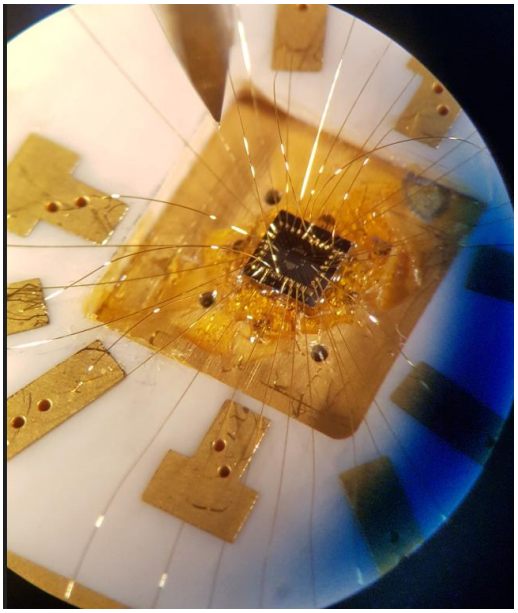


Figure 2.7 Optical image of wire-bonded sample

2.4 low temperature measurement setup

Low temperature is the most important factor to realize quantum system in laboratory. Quantum object reveals its quantum characteristics well at low temperature because energy scale of the quantum phenomena is so small that it is hard to

measure the quantum effects in room temperature. Advances in theory of refrigeration in early 20th century brought many scientific discoveries like superconductivity and quantum hall effect. Recent commercialization of refrigeration technology enabled qubit experiment in a laboratory.

2.4.1 Theory of dilution refrigeration

Dilution refrigerator uses mixture of ^4He and ^3He which is a liquid in cryogenic temperature. If the mixture is cooled down below the critical temperature at 0.87K, it starts to separate into two phases. In mixing chamber, ^4He sinks to the bottom because it is much dense than ^3He with bigger atom number. As the temperature goes down, the top site of mixture is filled with pure ^3He. However, it is discovered that even at the zero kelvin the concentration of the mixture does not completely separated into two parts but 6.6% of residual ^3He are stay in ^4He. This

separated state cause entropy transfer between the two states, make the temperature drop to milikelvin.

2.4.2 Tritron 300- dilution refrigerator

Triron 300 is a commercial dilution refrigerator provided by Oxford Instrument. It has a closed loop with cryogen-free system. It means that precooling of the mixture is done by pulse tube. it can cool down the sample plate to about 15mK and has a superconducting magnet which can apply magnetic field up to 5T in the vertical direction.

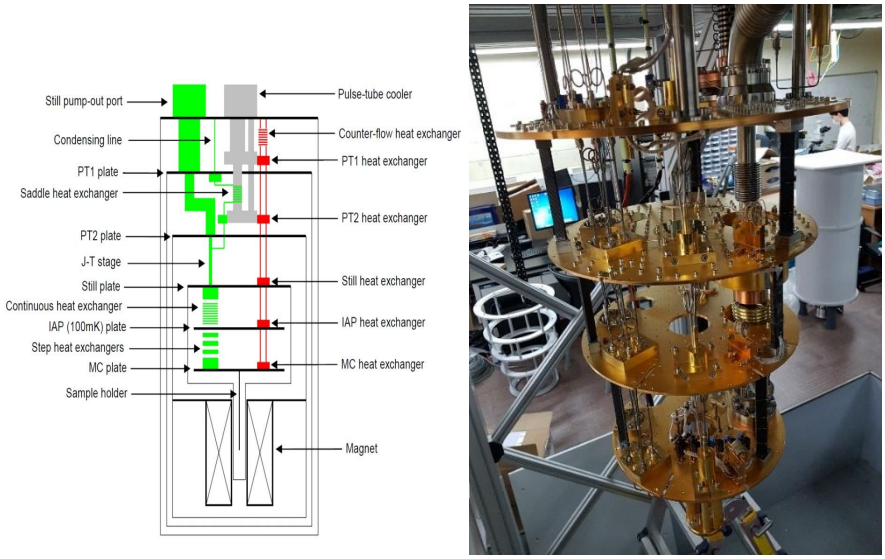


Figure 2.8 Schematics of Dilution unit and real image, the figure is adapted from oxford instrument manual

2.4.3 Cold traps

The cold traps are the partial setup for the dilution fridge. Although helium circulation system in the fridge is closed loop, small contaminations can still exist in it. Metal and plastic parts of the fridge can release many particles, molecules, and oils during cool-down and warm-up process. To get rid of these, cold traps are installed inside the circulation loop. Two of the

cold traps are located on the PT1, PT2 plates, and one is installed outside of the fridge. The principle of the cold trap is freezing the molecules that pass through the traps. The traps in the dilution units are cooled down and stay at low temperature by pulse tube of the system. The one which is outside of the dilution units need regular maintenance by refiling liquid nitrogen.

2.4.4 1.5K helium refrigerator

Although the dilution fridge is fancy apparatus for low temperature experiment, it takes much time to cooled down and magnetic field can be exerted to only to 5T (Tesla). So, it is not suitable for sample test which should be done fast and some experiments that need higher magnetic field, like quantum hall measurement. For that kinds of applications, helium refrigerator which can reach at 1.5K is used. Teslatron from Oxford Instrument is the fridge which can cool down to 1.4K and apply

magnetic field up to 8T. The detailed explanations on measurement setup are in Chapter 4.3.

Chapter 3

GaAs/AlGaAs Quantum dot measurement

3.1 Bias cooling and stability test for devices

3.1.1 Bias cooling

Bias Cooling is the process to reduce noise of the sample by applying small positive voltage (100-600mV) to all gates when it is cooled down. By doing this technique, it has been observed that gate stability is enhanced and noise is notably suppressed. The principle of bias cooling is that preventing charge tunneling

through the Schottky barrier in GaAs. At base temperature, 2DEG is formed and charges are frozen.

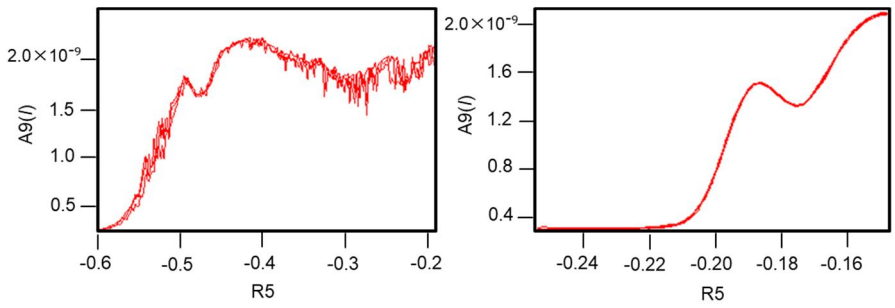


Figure 3.1 Measured current before and after bias cooling

During the experiment, different bias voltages are tested to determine the best condition for the wafer. For our devices, +500mV is proved to be the optimal voltage.

3.1.2 Device test methodology

The first test for the samples loaded via bias cooling is ohmic contact test to obtain the resistance of the wafer itself. The resistance of a good ohmic contact ranges typically few hundreds of ohms, but measured resistance could be several

kilo ohms because resistance of the measurement setup, such as breakout box and connectors, is added. If the ohmic contact does not work, test is over and the other sample is loaded. The next all gates are checked for proper operation. The gate operation is tested by applying voltage to the gate while allowing small current (-5nA) to flow between the ohmic contacts and pinch off curve is examined. If the gate does not work, there is no significant change in the current between the contacts.

3.2 Quantum dot transport

DC transport measurement is the first method to test and form quantum dots. It is done by using the DAC channel attached to one of ohmic contact and other ohmic contact via home-built amplifier. Applying a bias voltage to source line make the current pass through the 2DEG channel and this current can be read with drain line.

3.3 Charge sensing

Charge sensing is the technique to detect the changes in the electrostatic environment of the quantum dot by using the transport measurement through the adjacent quantum structure. Unlike ordinary transport measurement of which current pass through the quantum dot itself, charge sensing uses Quantum Point Contact(QPC) [11] or some other quantum dot as a sensor[12].

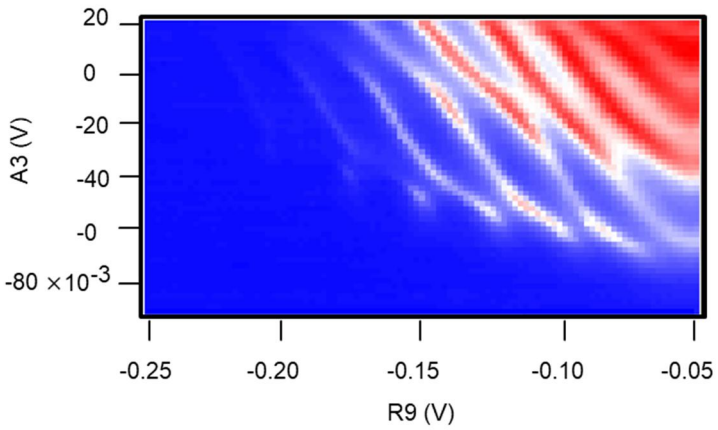


Figure 3.2 Charge stability diagram by transport

3.4 RF reflectometry

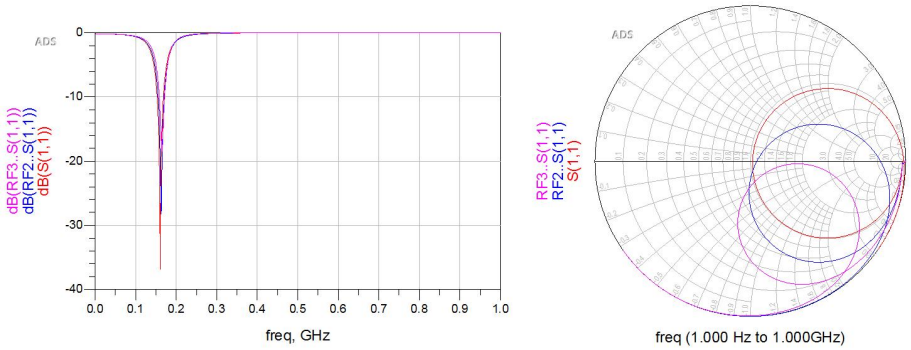


Figure 3.3 RF matching simulation

Figure 3.3 shows the RF simulation for matching circuit. About 150MHz the LC matching is done and near this point the measurement is done for RF reflectometry.

3.5 Results and discussion

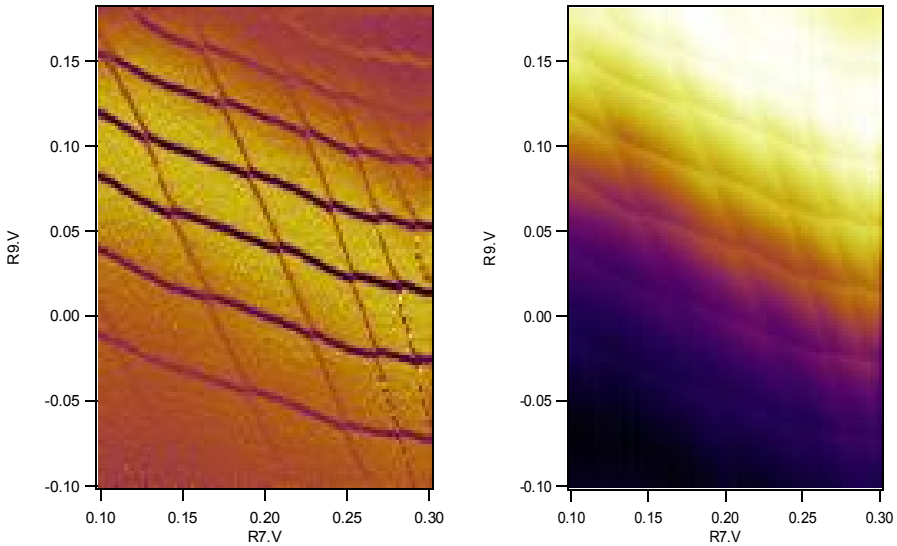


Figure 3.4 Charge stability diagram by QPC (left: derivative plot, right: QPC date)

Figure 4 show the measured stability diagram for quantum dot. By sweeping the gate between the nearest dots, one can get the 2D scan mapping of coulomb blockade. The signal is obtain using lock-in amplifier. The derivative plot in figure 3.4 show the vivid charge number profile of the quantum dot

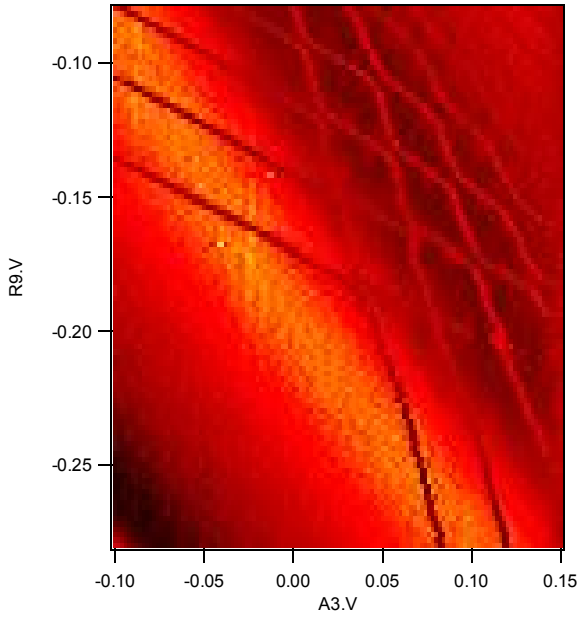


Figure 3.5 Charge stability diagram down to single electron regime

Figure 3.5 shows the charge stability diagram down to single electron regime. As the gate voltage approaches to the minus, no more coulomb peak is appeared. At that regime, no electron is present and one can say the quantum dot is completely empty. Right front the empty line, there is single electron regime. In this regime, one can control the single electron to use it as a qubit.

Chapter 4

Si/SiGe Hall measurement

Fabrication quantum dot devices on Si/SiGe heterostructure especially undoped one takes much time and effort.

This chapter deals with quantum hall measurement of Si/SiGe hall bar at low temperature. The theory of quantum hall effect and measurement technique for hall measurement are presented. The detailed fabrication process for Si/SiGe hall bar is covered and result of measurement are discussed.

4.1 Quantum Hall measurement

Quantum hall effect is first discovered by Klaus von Klitzing who is the Nobel Prize laureate in 1985 for its discovery [13]. Quantum hall effect is an attractive phenomenon both for fields of theoretical and experimental physics because it shows distinct

quantum effect which can be explained by well-established theory. In early 2000's, quantum hall effect was brought back into the front line of quantum experiment with advances in 2-dimensional materials like graphene [14] [15]. For semiconductor heterostructure system, it can be used to determine the characteristics of 2DEG for instance carrier type, charge density and mobility. Quantum hall measurement are done on Si/SiGe wafer with specified structure for hall measurement called 'Hall bar'.

4.2 Fabrication process for Si/SiGe heterostructures

Fabrication of hall bar on Si/SiGe heterostructure has similar steps that of quantum dot devices except making nano-size gates using e-beam lithography. The GaAs structure mentioned previous chapter has delta doping profile and there was no need to make top gate structure to accumulate charge carriers at low temperature. For undoped Si/SiGe structure, global

accumulation gate is inevitable and gate oxide also must be deposited. Cross-sectional schematics are illustrated in Fig 4.1.

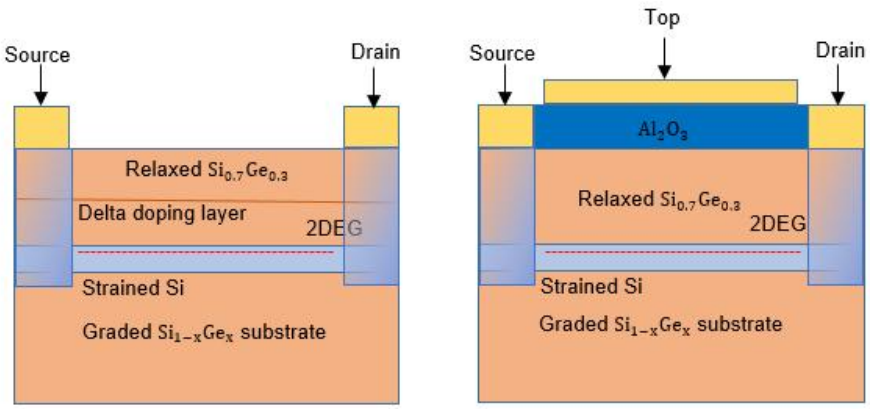


Figure 4.1 Schematic of Si/SiGe structure

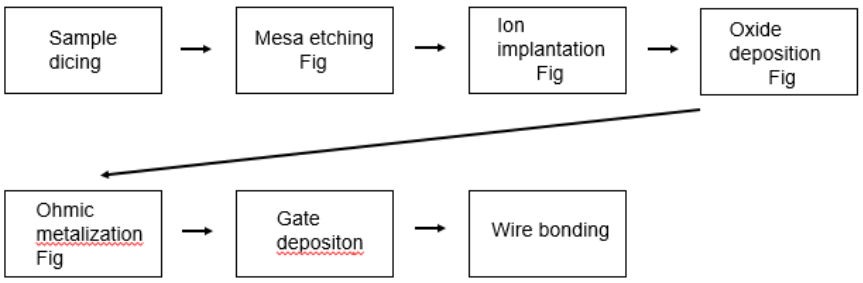


Figure 4.2 Procedure of sample fabrication

4.2.1 Dry etching

Dry etching process is done with RIE(reactive ion etch) etcher system. Using SF_6 gas with photolithography mask, it was possible to selectively etch the sample and make mesa structure. Once the etching process is finished, it is hard to remove the photoresist with solvent cleaning. Additional oxygen plasma cleaning could completely remove the residue.

4.2.2 Ion implantation

To make ohmic contacts for Si/SiGe structure, ion implantation with +P ion is tested.

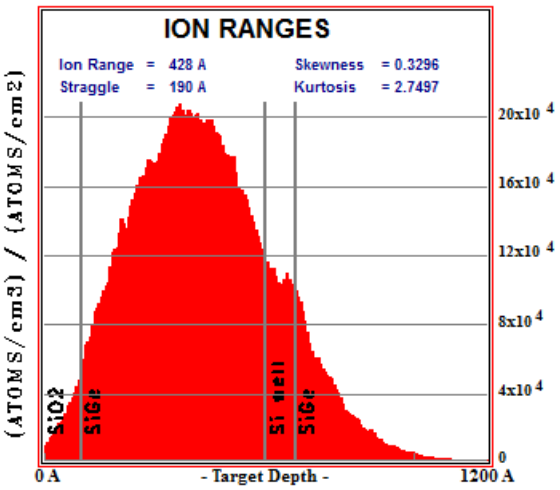


Figure 4.3 SRIM simulation

The implantation energy is determined by Stopping and Range of Ions in Matter (SRIM) simulation. This Free software get the solution by performing Monte Carlo algorithm to atom's collision in the semiconductor. Once the depth and material for the heterostructure is set, SRIM gives the depth profile of atoms

under certain energy. Figure 4.3 shows the result for 30keV implantation.

Implanted ions make defects to crystal structure of Si. It is required that reconstruct the crystal to make doped ions act as donors. Rapid thermal annealing is performed about 30 seconds for 5×10^{14} dose. It is reported that too much heat energy gives thermal budget for the structure and degrades the 2DEG quality.

4.2.3 Oxide deposition

To accumulate charges in Si/SiGe wafer, MOS structure with top gate is required. In this work, aluminum oxide (Al_2O_3) are used as gate dielectric. Al_2O_3 has high dielectric constant, which the value of κ reported as 9.1. With this high κ, it is possible to deposited thick oxide layer up to 90nm to prevent possible leakage current, while exerting sufficient electric field to accumulate charges. Oxide layer is deposited using atomic layer

deposition (ALD) to maintain clean layer interface with stacking layers one by one.

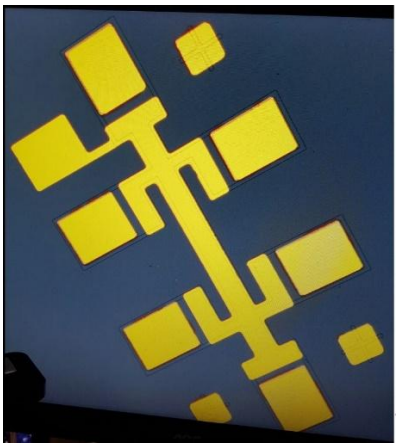


Figure 4.4 Completed hall bar sample

4.3 Hall measurement method

The Fabricated hall bar is prepared in similar way as mentioned previously in chapter 2.3. The sample is then loaded to Tealatron and checked for electrical connections. Once the

sample is cooled down, the first thing to do is accumulating the carrier. Two sourecemeter (Keithley 2400) are used to turn the devices on. The compliance for the gate is set very low (-10nA) for measurement with low leakage. If the Leakage goes up to compliance, the sample need to be replaced. This gate test, unfortunately, can be done only at low temperature because accumulating charges at room temperature can make the fixed charge at oxide-semiconductor interface. The current compliance for source-drain can be set higher (-50nA).

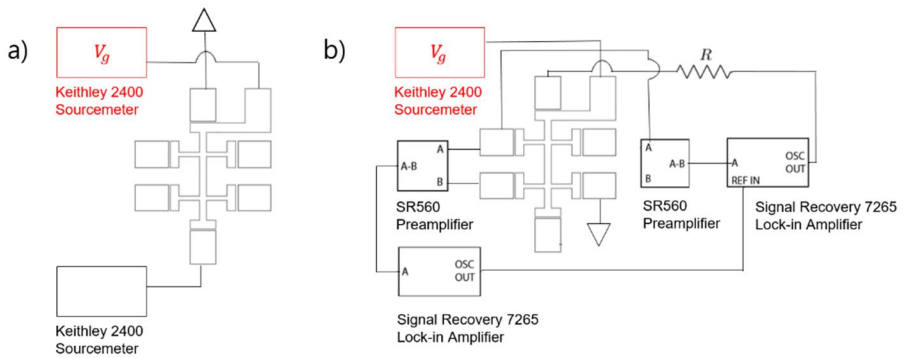


Figure 4.5 Circuit diagram for hall measurement

4.4 Results on Si/SiGe hall bar

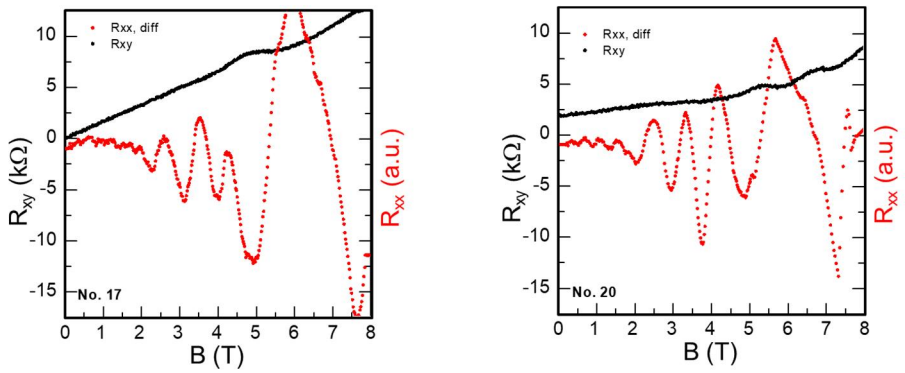


Figure 4.6 Quantum hall measurement result

Figure 4.6 shows the measured quantum hall effect with two different wafers. Shubinikov de haas oscillation is shown and from this phenomenon, it is clear that two dimensional transport is presented. Mobility is calculated from the zero field resistance and Hall voltage at 1T [16]. Calculated mobility for two wafer is both about 30,000cm^2/Vs at charge carrier density $6 \times 10^{11} cm^{-3}$.

Chapter 5. Summary and future work

5.1 Summary of the results

In this research, gate-defined quantum dot devices in GaAs systems are investigated. It is verified that multiple quantum dots can be formed and few electrons in the quantum dot can be operated with our experimental setup. Single electron control was possible using transport and sensing technique

The measurement using rf reflectometry revealed that reliable sensing using rf sensor is possible.

For Si/SiGe wafer, the possibility to build quantum dot devices are shown. 2-dimensional transport is confirmed by quantum hall effect and mobility is calculated from the data for wafers.

5.2 Future Works

For scalability of quantum dot qubit devices, making a 3D sensor structure on top of the devices could be a possible solution. Another 2D channel beside the 2DEG is required for 3D sensing, and combination with traditional quantum dot devices and 2D material like graphene is a candidate to implement 3D sensing structure.

For Si/SiGe devices, attempt to use 2D material as a gate dielectric is ongoing. Hexagonal boron nitride(h-BN) is an insulating 2D material with band gap higher than 6.1eV[17]. It also used as a buffer material for graphene to preserve the high mobility of the graphene channel after fabrication. It is reported that with hBN-graphene-hBN structure, mobility of the graphene channel reaches as hig1h as 100,000cm^2/Vs. [18] Using these properties of hBN, it is possible to make high-mobility graphene channel as a vertical charge sensor while hBN serves as gate dielectric.

Appendix A

Devices list

Sample No.	Date.	Bias	Result
No.1	19.10.2017	250mV	5 dots are formed
No.2	23.10.2017	300mV	Stability is bad
No.3	24.10.2017	300mV	C9 gate is broken
No.4	25.10.2017	200mV	Bias cooling is not sufficient

No.5	27.10.2017	0mV	Bias condition test
No.6	28.10.2017	250mV	Double dot formed
No.7	30.10.2017	230mV	Problems with ohmic
No.8	01.11.2017	230mV	Stability is bad
No.9	07.11.2017	300mV	Some gates are not working
No.10	19.11.2017	500mV	Some gates are broken
No.11	20.11.2017	500mV	Some lines are not working
No.12	25.11.2017	500mV	Stability is bad
No.13	30.11.2017	300mV	Double dot formed
No.14	02.12.2017	300mV	6 dots are formed

Appendix B

Wire bonding

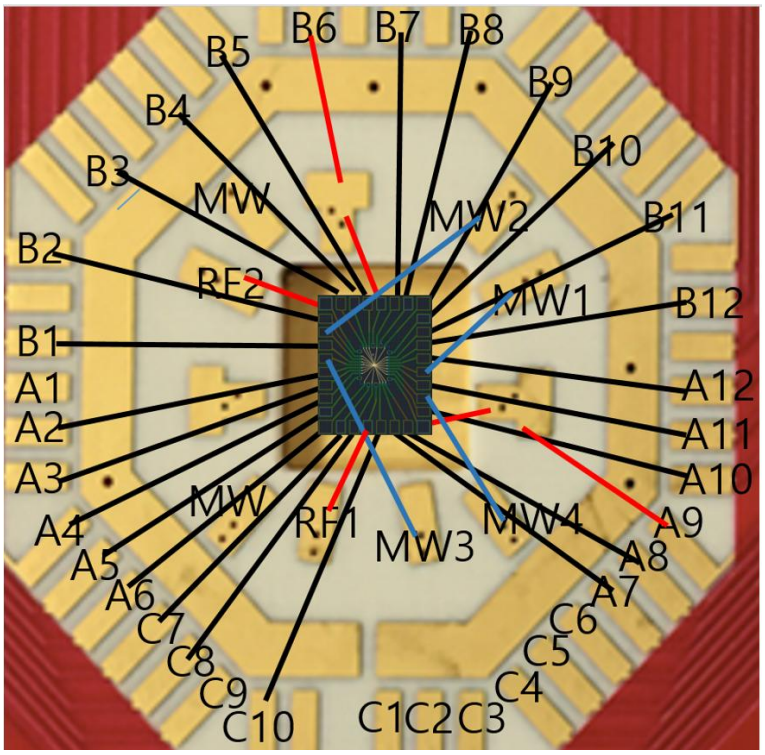
Wire bonding the sample to PCB is the final step of sample preparation before loading to dilution fridge. In this chapter,

wire bonding map for cool down sample are presented. Bonding map is designed following some constraints.

1. RF readout lines(red) are taken as short as possible to reduce stray capacitance and noise.

2. Crossing other lines are avoided except microwave lines(blue)

3. Because of noise issue in fridge line, some lines in C labels are avoided



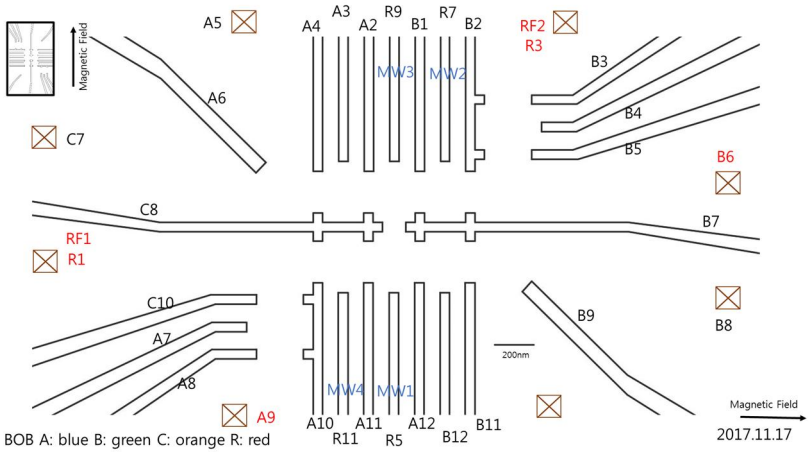


Figure app.1 bonding map for quantum dot sample

Appendix C

Fabrication recipe

Quantum dot fabrication on semiconductor heterostructures are consist of series of general semiconductor fabrication steps including lithography pattering and metal deposition. Process for Quantum dot and hall bar sample are almost the same except nano-size gate patterning using E-beam lithography(EBL). This Chapter contains the fabrication recipe for Si/SiGe hall bar mainly. Fabrication of GaAs sample is collaborated with Dr. Chang-ki Hong, Busan national university.

Fabrication process described here is done mainly in cleanroom of physics department, and Inter-university Semiconductor Research Center (ISRC). For E-beam lithography

under 100nm pattern, JEOL JBX 9300 is used in Korea Advanced Nanofab Center (KANC)

Sample dicing

Objective: Dice the wafer into 5mm × 5mm square

1. Dice the wafer into 5 × 5 mm square using DAD3350 in ISRC
2. Remove Blue tape and soak in acetone for 5 minutes
3. IPA rinse
4. Dry using N_2 gun

Trench and align marker formation

Objective: etch trench lines to define the 2DEG conduction area. Align markers are also made in the step.

1. Spin photoresist AZ5214 with 3000 rpm, 1 minute.
2. Photolithography.
3. Develop resist using MIF 500.
4. Remove native oxide with 20 : 1 BOE for 15 seconds.
5. Rinse in DI water.
6. N_2 dry
7. Load the RIE vacuum chamber immediately. Using Oxford RIE etcher in ISRC, the recipe is 25 sccm SF_6 and 2 sccm O_2, 25W power at 16mT for 80 seconds.
8. Measure the etched depth of dummy sample using AFM, Repeat the process if necessary
9. Soak sample in acetone for an hour and lightly sonicate
10. Rinse in IPA.
11. Inspect the sample with optical microscope.
12. Clean the samples using O_2 plasma.

Ion implantation

Objective: implant P+ ion into the wafer to allow the conduction between surface metal contact and the 2DEG

1. Spin photoresist AZ5214 with 3000 rpm, 1 minute
2. Photolithography.
3. Develop resist using MIF 500.
4. Remove native oxide with 20 : 1 BOE for 15 seconds.
5. Rinse in DI water.
6. N_2 dry.
7. Implant sample with P+ (phosphorus) at 20keV and 75keV twice with does 5×10^{14} ions/ cm^2 , 7° tilt, room temperature.
8. Soak in acetone for hours, then sonicate lightly.
9. Rinse in IPA.

10. Clean the samples using O_2 plasma.

11. Anneal the samples at 625℃ for 30 seconds in ISRC

12. Inspect the implanted region with optical microscopy.

Oxide deposition

Objective: make the oxide layer between top metal gate and semiconductor.

1. Remove native oxide on the samples with 20 : 1 BOE dip for 15 seconds.
2. Rinse in DI water.
3. N_2 dry.
4. Deposit 850 cycles (90nm) Al_2O_3 at 250 ℃

Ohmic contact

Objective: Create metal contact over the ion-implanted region to allow electrical connection to the 2DEG

1. Spin photoresist AZ5214 with 3000 rpm, 1 minute.
2. Photolithography.
3. Develop resist using MIF 500.
4. Remove native oxide and underlying Al_2O_3 with 20 : 1 BOE for 3 minutes.
5. Rinse in DI water
6. N_2 dry
7. Place the sample in evaporator chamber.
8. 5 nm Ti at 0.5 Å/s
9. 100nm Au 1 Å/s
10. Liftoff using acetone and rinse in IPA

Top gate deposition

Objective: Make Au top gate over the oxide layer

1. Spin photoresist AZ5214 with 3000 rpm, 1 minute.
2. Photolithography.
3. Develop resist using MIF 500.
4. Rinse in DI water
5. N_2 dry
6. Place the sample in evaporator chamber.
7. 5 nm Ti at 0.5 Å/s
8. 70nm Au at 1 Å/s
9. Liftoff using acetone and rinse in IPA

MIF 500 in develop process dissolves Al_2O_3 with very slow etching rate. E-beam lithography could be the better choice for this step if possible.

국문 초록

보편적 양자계산을 실현하기 위해서는 계산의 가장 작은 단위인 양자 비트, 즉 큐비트를 물리적인 시스템에 구현하는 것이 필요하다. 높은 전자이동도의 이차원 전자가스를 가지는 반도체 적층 구조는 큐비트 시스템에 적합한 후보 중 하나이다. 반도체 위에 형성된 나노사이즈의 게이트를 이용하여 2 차원에서 양자점을 인위적으로 구현할 수 있다. 밀리 켈빈 영역의 저온 수송 측정을 통해 양자점 내부의 전자 개수를 단일 전하 수준에서 제어할 수 있으며 전자의 개수와 스핀 상태를 양자계산을 위한 큐비트로 이용할 수 있다. 본 학위논문에서는 갈륨비소(AlGaAs/GaAs)와 실리콘/저마늄(Si/SiGe) 반도체 적층 구조를 양자점 기반 큐비트 구현을 위해 연구하였다. 저온 실험을 위한 냉각장치와 측정에 필요한 장비들의 준비과정과 각각의 특성을 설명하였다. 소자와 고주파 측정 회로 디자인을 위해 유한요소법을 이용한 전자기장 시뮬레이션이 연구되었다. 또한 반도체 구조에 나노 공정을 통하여

양자점 소자를 구현하는 과정을 다루었다. 마지막으로 저온에서의 고주파 측정과 양자 홀 측정을 통해 소자의 특성이 분석되었다. 실험 결과 갈륨 비소 구조에서 구현한 양자점 내부의 전자를 단일 전하 수준에서 제어할 수 있었으며 본 연구에서 사용한 소자 구조를 통해 큐비트를 구현할 수 있는 가능성을 확인했다. 실리콘/저마늄 반도체에 이루어진 양자 홀 측정을 통해 이차원 전도가 발생하는 것을 확인했으며 전하 이동도 분석 등을 통해 향후 양자점 소자의 재료로써 가능성을 입증했다.

1. Zwanenburg, F.A., et al., *Silicon quantum electronics.* Reviews of Modern Physics, 2013. **85**(3): p. 961-1019.

2. Jeong, H., A.M. Chang, and M.R. Melloch, *The Kondo effect in an artificial quantum dot molecule.* Science, 2001. **293**(5538): p. 2221-2223.

3. Schuster, D.I., et al., *Resolving photon number states in a superconducting circuit.* Nature, 2007. **445**(7127): p. 515-518.

4. Oliver, W.D., et al., *Mach-Zehnder interferometry in a strongly driven superconducting qubit.* Science, 2005. **310**(5754): p. 1653-1657.

5. Dutt, M.V.G., et al., *Quantum register based on individual electronic and nuclear spin qubits in diamond.* Science, 2007. **316**(5829): p. 1312-1316.

6. Loss, D. and D.P. DiVincenzo, *Quantum computation with quantum dots.* Physical Review A, 1998. **57**(1): p. 120-126.

7. Kim, D., et al., *Quantum control and process tomography of a semiconductor quantum dot hybrid qubit.* Nature, 2014. **511**(7507): p. 70-74.

8. Manfra, M.J., *Molecular Beam Epitaxy of Ultra-High-Quality AlGaAs/GaAs Heterostructures: Enabling Physics in Low-Dimensional Electronic Systems*, in *Annual Review of Condensed Matter Physics, Vol 5*, J.S. Langer, Editor. 2014. p. 347-373.

9. Zajac, D.M., et al., *A reconfigurable gate architecture for Si/SiGe quantum dots.* Applied Physics Letters, 2015. **106**(22).

10. Kane, E.O., *THOMAS-FERMI APPROACH TO IMPURE SEMICONDUCTOR BAND STRUCTURE.* Physical Review, 1963. **131**(1): p. 79-&.

11. Field, M., et al., *MEASUREMENTS OF COULOMB BLOCKADE WITH A NONINVASIVE VOLTAGE PROBE.* Physical Review Letters, 1993. **70**(9): p. 1311-1314.

12. Barthel, C., et al., *Fast sensing of double-dot charge arrangement and spin state with a radio-frequency sensor quantum dot.* Physical Review B, 2010. **81**(16).

13. Laughlin, R.B., *ANOMALOUS QUANTUM HALL-EFFECT - AN INCOMPRESSIBLE QUANTUM FLUID WITH FRACTIONALLY CHARGED EXCITATIONS.* Physical Review Letters, 1983. **50**(18): p. 1395-1398.

14. Zhang, Y.B., et al., *Experimental observation of the quantum Hall effect and Berry's phase in graphene.* Nature, 2005. **438**(7065): p. 201-204.

15. Du, X., et al., *Fractional quantum Hall effect and insulating phase of Dirac electrons in graphene.* Nature, 2009. **462**(7270): p. 192-195.

16. Mi, X., et al., *Magnetotransport studies of mobility limiting mechanisms in undoped Si/SiGe heterostructures.* Physical Review B, 2015. **92**(3).

17. Watanabe, K., T. Taniguchi, and H. Kanda, *Direct-bandgap properties and evidence for ultraviolet lasing of hexagonal boron nitride single crystal.* Nature Materials, 2004. **3**(6): p. 404-409.

18. Zomer, P.J., et al., *A transfer technique for high mobility graphene devices on commercially available hexagonal boron nitride.* Applied Physics Letters, 2011. **99**(23).