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A High-Speed Link Transmitter for Emulating Channel Attenuation with Logarithmic and Exponential Function

대수함수와 지수함수를 통한 전송선로 손실을 모사한 고속신호 전송회로

2018 년 8 월

서울대학교 대학원

전기 · 컴퓨터 공학부

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Abstract

This paper describes a transmitter that can emulate a wide variety of frequency-dependent loss characteristics of high-speed DRAM channels, with an aim to facilitate an automated test procedure for DRAM interface that does not require physical reconfiguration of channels. Specifically, the proposed transmitter can generate the waveform of an NRZ data stream that experienced the adjustable amounts of skin-effect loss and dielectric loss of electrical channels. To save the hardware cost of implementing a high-speed, high-resolution digital-to-analog converter, the transmitter constructs the waveform using a set of logarithmic and exponential basis functions, each of which is implemented using a pseudo-logarithmic amplifier and low-bandwidth amplifier with adjustable gain and bandwidth, respectively. The prototype chip fabricated in 65um CMOS consumes 52,000um2 and operates over 1.4~7Gbps while dissipating 38mW at 7Gbps. It is demonstrated that the implemented transmitter can emulate 10~40”-long microstrip lines on FR4 material with the peak error less than 6.25% in the pulse response.

Keywords : channel-emulating transmitter, built-in self-test, skin-effect, dielectric loss, mixed-signal IC.

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Chapter 1

Introduction

Integrated circuits(ICs) have been growing steadily in accordance with Moore's Law, and semiconductor process, represented by CMOS, increased by 50% per year [2]. The speed of CMOS logic gates, which has been accelerated 13% per year, enables the 56Gbps electrical interface standard CEI-56G and 802.3bs-400GbE [3]. The trends are also applied to memory systems, which accounts for 50% of the semiconductor market. The DRAM chip is increasing capacity by 1.3-times per year, and the speed of data transfer rates is increasing by 1.25-times per year [4]. Fig. 1.1 DRAM data bandwidth trends. [3] represents the DRAM trend.

The development of DRAM has been proceeding in two directions, one is the evolution of the memory generation, and the other is the diversification of the memory type. In case of the computing memory uses in personal computer and server, it started form the DDR1 SDRAM that operates 100-200Mbps. And it is ahead of the DDR5 SDRAM that operates up to 6400Mbps. Each generation of the

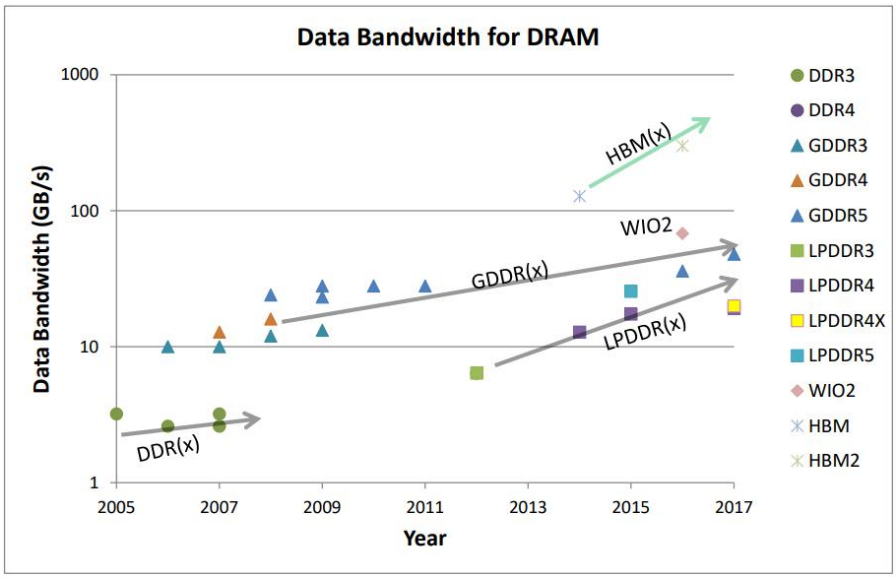


Fig. 1.1 DRAM data bandwidth trends. [3]

DDR memory has increased the speed of twice, and most systems were developed based on the DDR SDRAM memory. But recent systems use various memory type to optimize the system instead of using the computing memory in the past. Therefore, many memory types are developed in the Joint Electron Device Engineering Council(JEDEC). As an example, the graphics memory GDDR is developing for high-speed and high-resolution graphics processor unit(GPU) and mobile memory LPDDR is developing for low-power and high-speed application processor(AP). Recently, high bandwidth memory(HBM) is introduced for big data processing and artificial intelligence(AI). During the development of the DRAM, interface issues appear due to the constant increase in the DRAM operation speed. In this chapter, we will look specifically at why this problem occurred and what difficulties it has.

1.1 DRAM Interface

The memory interfaces have continually increases for supporting high-performance and low-power operation. As a result, the DDR1 SDRAM, which started at the speed of 200Mbps in 2000, evolves into the DDR5 SDRAM with 6400Mbps. And the graphics memory GDDR6 introduces 16Gbps speed at ISSCC [5]. In case of the HBM2, the HBM2 is able to transfer 341GB/s memory bandwidth per die [6].

During the evolution of the memory interface, the DRAM interfaces maintain the single-ended signaling and use parallel bus. The single-ended signaling, which requires fewer channels for signal transmission, is the simplest way to transmit data and is a cost-effective solution. It is even more attractive for the DRAM that uses parallel IO from 64bit to 2048bit per package. Therefore, the system is able to achieve low-cost and low-power performance with the high bandwidth memory.

The parallel single-ended interface, which is the considerable difference from the other ICs, induces many problems. The other interface chips have switched to a serial interface with differential signaling to speed up. The PCI and ATA are started with single-ended signaling, but it adopts differential signaling for increasing the data rate. Because the singled-ended signaling has a weakness in channel noise. In case of differential signaling, the common mode noise can be rejected by the differential receive, but the single-ended signaling is unable to reject it. And the receiver compares the input signal with internal reference voltage, and it would have

less gain than the differential signal receiver. Therefore, the DRAM interface would pay heed to the attenuation of the signal amplitude by the channel loss. For this reason, the memory interface get more sensitive to the channel.

Even with the difficulties, the memory interface has continued to increase the speed, and achieves 16Gbps per pin in the GDDR6. But the interface failure occurs more frequently in the system, and the most common reason is the channel. Various systems have been developed and the failure in systems designed with bad channel characteristics. If we cannot filter out the failure, the advantage of the DRAM interface will disappear. Because, the failure and debugging increases system development costs.

In next sub-chapter, more detail problems is explained with the type of memories.

1.1.1. Interface of the computing memory

The problem of computing memory interface starts with versatility. From the DDR SDRAM to DDR5 SDRAM is a kind of computing memory. It is used in the most general computer systems, from personal computers used by individuals to servers used by data centers. Because it has high convenience for capacity expansion and connection by using a Dual In-line Memory Module(DIMM). The multiple DRAM packages are mounted to the DIMM, which has 64bit parallel data bus using a shared command and address. Because the memory system uses shared data bus and command address, the system can easily expand the memory density. But the

shared bus makes problem.

It is difficult to increase the bus speed due the structure in which a plurality of DIMMs are connected to a single channel. Such a connection structure is called a multi-drop bus scheme. A mismatch in channel impedance at the point where each DIMM is connected creates reflected noise, and it causes signal distortion and degrades the interface margin. To solve the problem, the multi-drop channel is designed with different impedances at the branches to minimize the reflection [7].

The channel impedance value is different for each type of memory vendor and system board. In other words, the interface margins may decrease or fail due to the different channel conditions of the computing systems that mainly use in personal computer and server. The failure is difficult to screen at the package level because it occurs at the system level. To overcome this difficulty, the CPU manufacturer provides a tool to quantify interface margins in each system by using Built-in Self-Test(BIST). Testing in an application-based environment called application test. It insures validity of the system, but this manual validation procedure need higher cost and time, therefore, only sampling test is available. The sampling test is difficult to represent the worst case, or test cost is increased for representing the worst case.

1.1.2. Interface of the mobile memory

Low-power and high-speed operation are the most important factors in the mobile memory. and the mobile system needs highly integrated memory. In other to satisfy

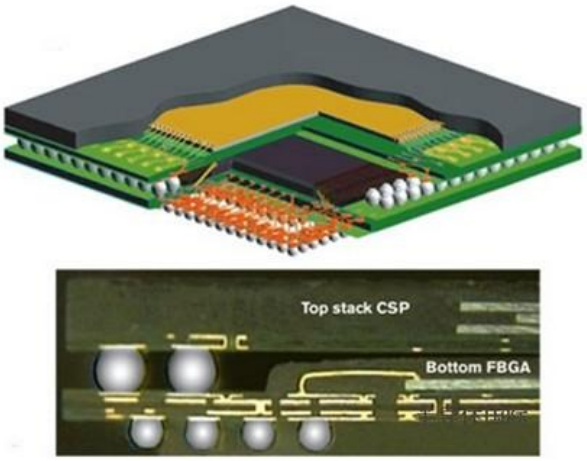


Fig. 1.2 The configuration of Package over Package in mobile memory.

these conditions, the mobile DRAM has focused on developing System in Package (SiP). A Package over Package (PoP) is a typical example of SiP in the high-

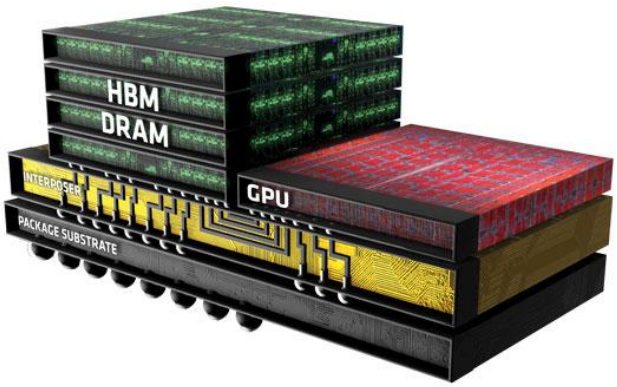


Fig. 1.3 The configuration of the HBM.

performance mobile system. As shown in the Fig. 1.2, memory package is directly mounted on a mobile AP package. This configuration is able to build highly integrated system, because it can eliminate the command address and data bus that occupy a large area of the system when implemented on the Printed Circuit Board (PCB). And the PoP has short channel length between memory and AP. The mobile system channel is defined by memory package substrate and application package substrate [4]. This configuration has the advantage of increasing the operation speed and the advantage of configuring the low-power IO. Therefore, the mobile DRAM interface achieves 4266Mbps faster than computing memory and reduces interface power by adopting low voltage-swing terminated logic (LVSTL) driver [8]. But the PoP has problem on debugging the channel.

The PoP does not expose channels to the outside, and there are so many kinds of package. The only point exposed to the outside in the PoP is the bump ball which joins between the application processor package and the DRAM package. The

difficulty of debugging is caused from the characteristics of channels that are not exposed to the outside. And the channel is too diverse due to many different packages. The channel is decided by combination between application processor package and DRAM package. There are various application processors, and each application processor has a different package. And the mobile DRAM has more package type than application processor. The package design depends on company, density, die configuration, and DRAM technology node. Therefore, the debugging difficult is increased due to the unexposed characteristics and diversity. Also, it is hard to verify the interface characteristics only by testing with mobile dram packages. The characteristics of mobile system channel is not reflected at the test.

1.1.3. High bandwidth memory

The computing system requires high-density and high-bandwidth memory for supporting big data processing, in-memory computing, and artificial intelligence (AI). The HBM is specialized in these applications due to high-bandwidth prosperity of 341GB/s [6]. And the stacked dies are able to support high density DRAM with small area. The HBM is connected to the SoC through a 1024bit parallel data bus per die operating at 2.4Gbps speed.

The highly integrated HBM has problem with interface such as the mobile system. The HBM operates 2.4Gbps per pin, which is slower than the mobile interface, but it uses unterminated single-ended signaling for achieving low-power operation. Furthermore, the silicon interposer has higher resistance value than the PCB channel. The channel characteristic makes signal attenuation and signal to noise ratio(SRN)

that is able to cause interface margin failed by combining the unterminated single-ended signaling and poor channel environments.

The direct process of HBM is performed by attaching SoC and DRAM on a silicon interposer. It means that the channel is not exposed to the outside and each component cannot be tested by alone. Unexposed channel makes hard to debugging signal integrity for measuring the interface margin in HBM system. Therefore, to test interface margins, it uses the BIST instead of ATE, which causes problems of increasing system building cost because it cannot screen the fault DIE.

1.2 Memory Test

The memory companies should ensure stable operation at the various systems. The memory operating speed is continuously increased, and it is being developed for various applications. The memory operates reliably at high speed in various environments, and the companies need testing environment for ensuring the stable operation. To this end, memory companies are developing various methods. Through Automatic Test Equipment(ATE), various tests are performed to ensure memory operation. and build typical application environment for testing the memories. Although the memory companies try to guarantee stable operation of memory through the various tests, but memory operating failures still happen due to the various environments.

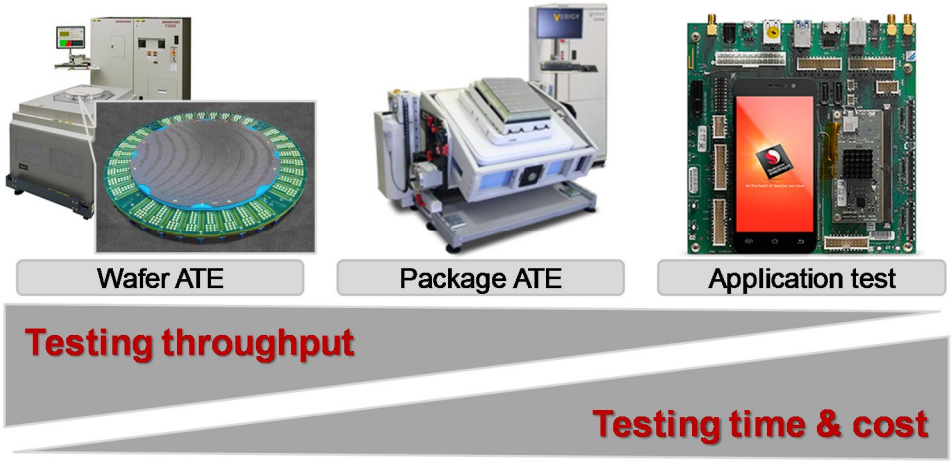


Fig. 1.4 Procedures of DRAM testing and properties of each stages.

This chapter explains in detail the reason why it is difficult to guarantee the memory operation. Then it discusses what methods have been proposed and the limitations for solving the problems.

The traditional DRAM test environment lags the DRAM evolution in the high-speed interface and the diversified DRAM. The evolution of DRAM decreases interface margin and it causes failure in some systems, but the traditional test methodology cannot find the weak point of the systems. Because, the ATE is uncorrelated to the system at the channel view point.

1.2.1. DRAM test sequence

The DRAM test sequence aligns to the property of DRAM product, which one has mass quantities than the other IC chips. The test cost is about 10 ~ 20% of the DRAM cost, and the main fact of test cost is testing time. The ATE is able to reduce testing time by automated the all testing sequence, even including test handler automatically places test DUTs to the ATE sockets. And the test uses multi-site and compression test [9]. The multi-site test shares the common interface like command bus and tests multiple devices at once, therefore, the low-speed test has more advantage on the multi-site test.

The DRAM test consists of wafer level test, package level test, and application test as Fig. 1.4. The first test sequence is the wafer test that has the highest test throughput in the test sequences. The test is performed at low-frequency operation, but it can test multiple die with shared connection. It means that the wafer test is the best stage to screen fault DRAMs in terms of test cost.

The next test step is package test with ATE that tests the DRAM passed in the wafer test sequence. It has aim to screen fault that relates to timing parameter, so it uses various clock frequency, a hundred MHz to higher frequencies than normal operation, to screen parametric fault DRAMs. It also uses multi-site test with lower clock frequency to reduce testing time, but at speed test has the lowest test throughput due to the limited sharing channel. The interface margin can be measured at this stage because the operating frequency is same as the real operation condition. But the package ATE channel is fixed and it is designed to have low noise. The traditional ATE is designed to prevent the DRAM from over screen due to the noise of the device, so the test environment of ATE is almost noise less condition [10] [11].

The last test procedure is application test. It uses the real system as the Fig. 1.4,

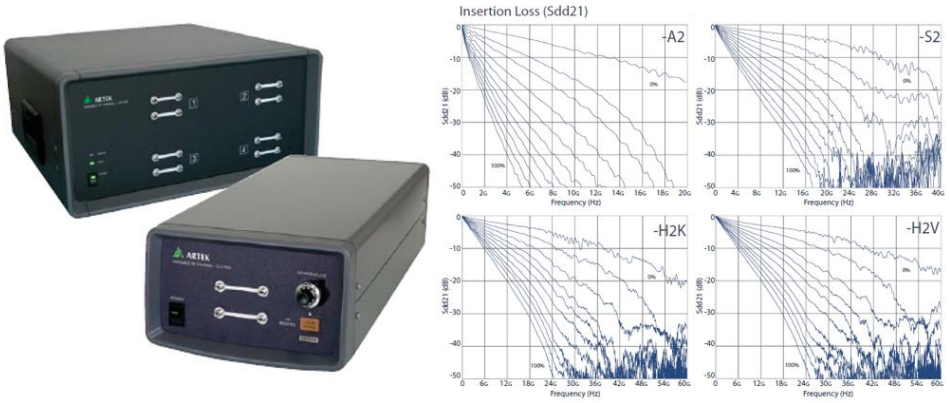


Fig. 1.5 Ace unitech CLE100, variable Inter-Symbol-Interference (ISI) channel tester for high-speed serial interface [12].

but the difference is that the DRAM is mounted by the socket, not by soldering. The test environment is most same as the real application environment, and it is more accurate than the other testing environments. Therefore, the interface margin is tested on this test, but there are some problems. First, it requires the highest test cost than other sequence. The testing time is long and full test process would be handled by manually. Second, a large amount of system is needed to build the test environment, and it cannot reuse for long time due to reliability of the system. The introduction of new systems annually limits the effectiveness of older systems. Third, there are many system manufacture, the implemented system does not represent the products of all manufacturers.

As reviewed in the chapter, the traditional DRAM test sequence does not provide adequate testing method for interface margins. The ATE can reduce test cost but the

Fig. 1.6 Keysight Technology, J-BERT that can emulate ISI [13].

fixed channel condition limits screen ability, and the application test needs a large cost and cannot represent the worst case.

1.3 Channel Testing Environment in High-Speed Serial Link

The channel emulation test equipment had been developed for using to the high-speed serial link area [12][13]. This is faster than the development of DRAM tester,

probably because the serial link device operates at a higher speed than the DRAM. Therefore, high-speed operated serial link device shows more sensitivity to the channel, and it would have created a consensus on the need for testing variable channels.

There are two ways to support the channel verification in electrical test equipment. First, the test equipment emulates channel by physically, as it implements variable channels in the tester or it changes channels characteristic by controlling electromagnetic flied [12]. The real channel-based operation is merit of the tester as Fig. 1.5, but the programmable range is limited because all the channel characteristics are decided by the implemented channels. Second, the test equipment emulates channel by electrical IC. An example is finite impulse response (FIR) filter as Fig. 1.6, it shows high pass transfer function by de-emphasis output signal in the HSL device, but it uses low pass transfer function in tester to make the artificial inter symbol interference without using channel. The FIR filter is easily implemented and has flexibility on changing the tap coefficient, therefore the most source generator in the Bit Error Ratio Tester(BERT) adopts it. But the limited tap number and discrete-time based FIR filter is hard to emulate the channel loss accurately.

The channel emulation tester in serial link device is useful to test the interface margin with considering the channel, but it has some problems to adopt in the memory. It is commonly used in the serial link standard like MPHY to test variable channel. The difference between serial link and the DRAM is number of interface channel. The memory has more than 8 to 1024 per package, and it is much larger than the serial link channel. The number of channel depends on the tester cost, and

the total cost is too high to build the tester system for the DRAM.

Chapter 2

Channel Attenuation and Modeling

2.1 Channel Noise

Fig. 2.1 shows noise and interference that occur on the interface [14]. Among these components, the noise associated with the channel is attenuation, crosstalk, and reflection. This work mainly focuses to the attenuation than other noise factors among the channel noise components represented by attenuation, crosstalk, and reflection. Because the attenuation is decided by the intrinsic properties of the channel constituent material, and it is the most key factor that determines the

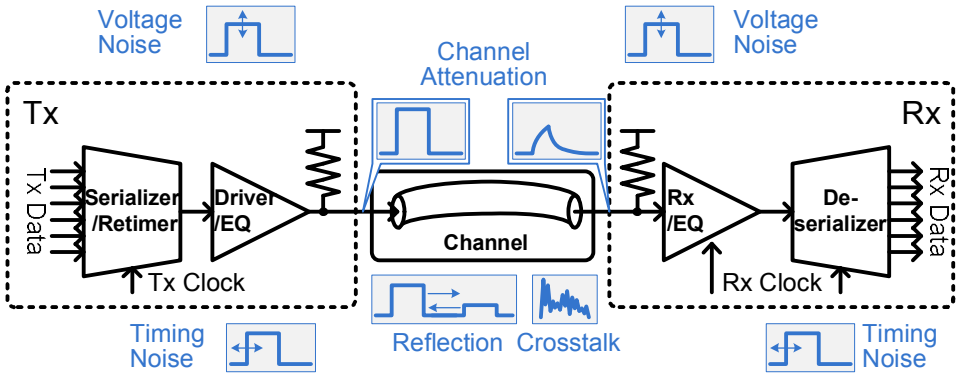


Fig. 2.1 The operating environment of high speed link and the noise sources.

maximum operating frequency of the interface system. The attenuation decides a signal amplitude reduction and propagation delay, and the reduced signal makes smaller voltage and timing margin of an interface circuits. Therefore, the circuit techniques are developed to compensate the attenuation loss in the channel that uses equalization method in transceiver systems. And also the improvement material that uses for fabricating channel reduces the attenuation loss and the operating speed of network and memory interface speed to 30% per year [3]. But still the many works focus to increases speed of interface system that limited by the channel noise by attenuation loss wall. Attenuation loss in the micro strip channel in PCB consists with skin-effect, dielectric loss, and radiation loss, and those loss have effective frequency band.

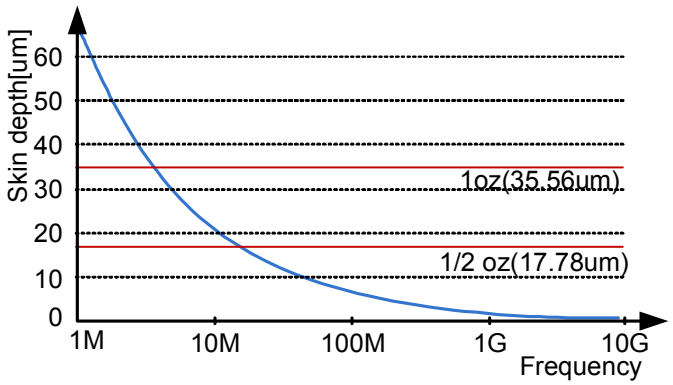


Fig. 2.2 Skin depth of transmission line vs. frequency.

2.1.1. Skin-effect

Skin-effect is the conduction loss that the alternating electric current (AC) density flows a conductor with nonuniform distributed [15] [16]. As the electric field is caught between the transmission line and the ground, the current is concentrated and concentrated on the area where the electric field is strong. It causes more current to flow to the outside of the transmission line, and this phenonium changes the depth of the effective conductor. The depth of the actual surface through which the current flows is called skin depth, which becomes smaller in proportion to the frequency component of the current. As a result, when the frequency increases, the effective resistance of the transmission line increases as shown in the Fig. 2.2. The skin-effect depends on square root of the frequency as shown in a following Eq. (2.1.1), therefore, the skin-effect is mainly affected by the low-frequency component of the transmission signal. The skin depth of conductor can be expressed as (2.1.1):

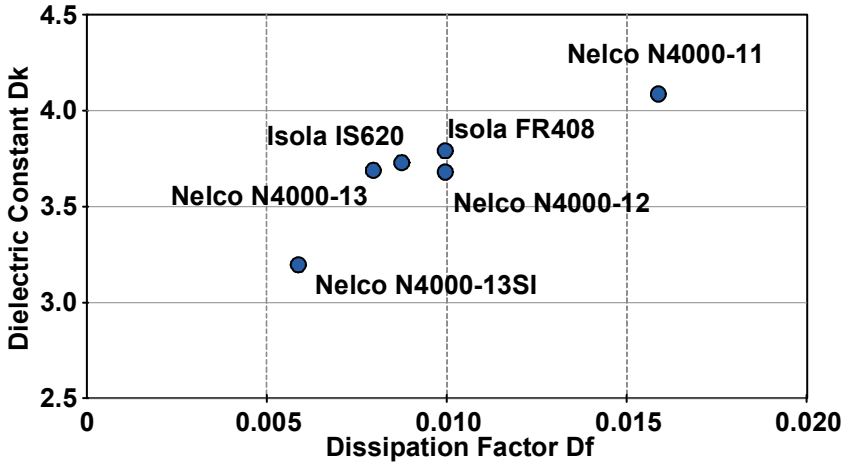


Fig. 2.3 Material properties of improved FR4 [17].

$$\delta = \sqrt{\frac{2\rho}{2\pi f \mu}} \tag{2.1.1}$$

where ρ is the resistivity of the conductor, f is the frequency, μ is the magnetic permeability. As an example, 1-ounce copper transmission line has geometrical thickness of 35um at the PCB, the skin depth is less than 35um when the signal frequency is higher than 10MHz. This is illustrated in Fig. 2.2. The equation is based on a formula that best represents result of skin-effect measurement, not the formula derived from the theoretical interpretation. However, the experimental result and the expressions show the skin-effect that increases with signal frequency, and that the signal attenuation is limited at frequencies above a certain frequency, because the skin-effect is proportional to square root.

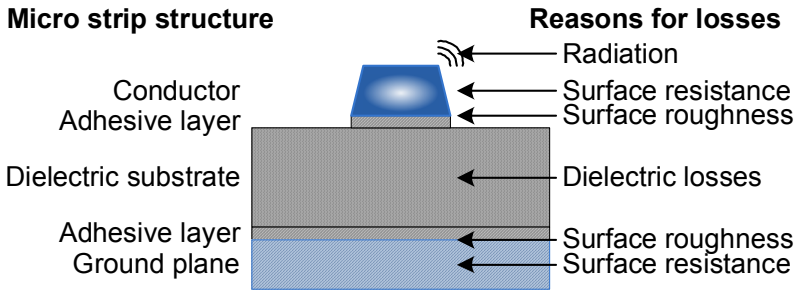


Fig. 2.4 Micro strip line structure and loss mechanism.

2.1.2. Dielectric loss

Dielectric material has inherent dissipation of electromagnetic energy, and the dielectric loss quantifies the material properties. In case of the transmission line, the dielectric loss causes from material's inherent dissipation between signal line and ground. The dielectric loss is expressed by the dissipation factor loss tangent as:

$$\alpha_D = 0.91 \cdot \tan\delta_\varepsilon \cdot f \cdot \sqrt{\frac{\varepsilon_r(1+F)}{2}\left\{\frac{1-F}{\varepsilon_r(1+F)}\right\}^{-1}} \qquad (2.1.2)$$

$$\text{with } F = 1/\sqrt{1+10h/w}$$

Where α_d is dielectric loss, ε_r is the relative permittivity, $\tan\delta_\varepsilon$ is dielectric loss tangent, and f is frequency. The dielectric loss is improved by changing material that

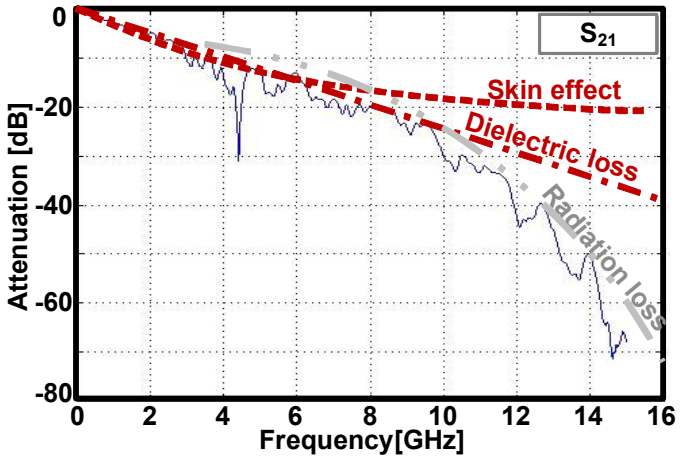


Fig. 2.5 The channel attenuation curve with the dielectric loss and the skin-effect.

has low loss tangent. It depends on the material inheritance, therefore, the higher speed interface adopts lower loss tangent material than the commonly used FR4. The current network standard CEI-56G uses material that has 10-time lower loss tangent than FR4. In case of the memory interface, the improved FR4 still used in the systems the ATE uses the material that has loss tangent less than 0.005 in the Fig. 2.3 [17].

2.1.3. PCB loss mechanism

Fig. 2.4 shows signal attenuation mechanism occurring on the transmission line.

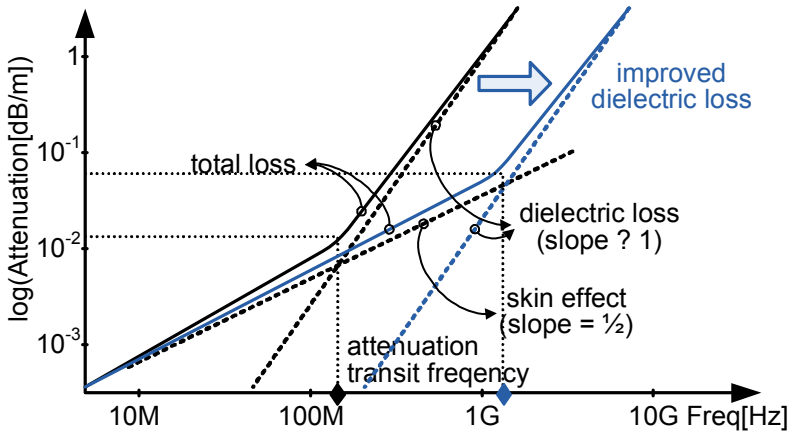


Fig. 2.6 Comparing attenuation transition frequency between two channels.

The attenuation caused by the transmission line on a PCB is divided into conduction loss, dielectric loss, and radiation loss, which are represented by the skin-effect and the dielectric loss describes above. Total attenuation constant α_T is expressed as the sum conduction loss α_C, dielectric loss α_D, and radiation loss as α_R.

$$\alpha_T = \alpha_C + \alpha_D + \alpha_R \tag{2.1.3}$$

Each loss has frequency dependence as shown in Fig. 2.5, and the equation (2.1.2) can be expressed with the frequency as:

$$H(f) = e^{\gamma_0 + \gamma_1 \sqrt{f} + \gamma_2 f + \gamma_3 f^2}$$
$$\gamma_i = \alpha_i + j\beta_i \tag{2.1.4}$$

where the $H(f)$ is transfer function of channel, γ_0 is propagation constant of dc

resistance and surface roughness, γ_1 is propagation constant of skin-effect, γ_2 is propagation constant to relate dielectric loss, and γ_3 is propagation constant of radiation loss. Each propagation constant of γ_i consists of attenuation coefficient α_i and phase-change coefficient of β_i. Fig. 2.5 shows the transmission line attenuation result and each loss components. The skin-effect term depends on root square of frequency and it is predominant on the low frequency band, and the dielectric loss is major loss in the high frequency range within which the HSL operates. The radiation loss depends on square of frequency and it decides high frequency range of the transmission line. In particular, conduction loss and dielectric loss are major loss components on memory transmission lines.

The two losses are partially independent of each other and the transmission line is characterized by the two losses as Fig. 2.6. The frequency at which the two losses are equal to each other is defined as the f_T (attenuation transition frequency) to express the relationship between the two components. However, due to the continuous use of materials capable of improving dielectric loss, the f_T increased, and the loss due to the skin-effect became more important as the dielectric loss was compensated circuit techniques. Those two attenuations express as:

$$H(f) = e^{\gamma x}$$
$$\gamma = \alpha + j\beta = \sqrt{(r + j2\pi fl)(j2\pi fc)} \tag{2.1.5}$$

where α is attenuation constants, β is phase constants of the transmission line that consists with r, l, and c per unit length and the wire length x. Furthermore, we assume that the dielectric loss is included in the capacitance as a complex dielectric

constant, $c(\varepsilon)$, where ε is the complex dielectric constant [33].

In case of skin effect only analysis, the resistive loss can be described as [1]:

$$e^{(-r/2Z_0)} \tag{2.1.6}$$

where r is resistance of channel, and Z_0 is the channel impedance. The resistance in equation (2.1.6) will vary with the frequency as (2.1.7):

$$r = r_s\left(1+j\right)\sqrt{2\pi f} \tag{2.1.7}$$

where r_s is the resistance of the low-frequency band that is not affected by the skin-effect. The Arabi [2] showed that by describing both the resistive and the inductive part of skin effect properly in equation (2.1.5), it was possible to fulfill the constraints above is the resistance value that is not affected by skin-effect. With (2.1.5) and (2.1.7), the skin-effect channel loss is expressed as:

$$H \propto e^{-j2\pi f\sqrt{lc}} \cdot e^{-\left(r_s/\sqrt{2}Z_0\right)\sqrt{j2\pi f}} \tag{2.1.8}$$

where the dominant loss is decided by resistance due to lc is small enough to neglect.

In the case of dielectric loss, a transfer function with multiple dielectric constants is used to express the dielectric loss [34] as:

$$H \propto e^{\left(-a\sqrt{lc_0}\,j2\pi f \ln\left(\frac{\tau_1(1+j2\pi f\tau_2)}{\tau_2(1+j2\pi f\tau_1)}\right)\right)} \tag{2.1.9}$$

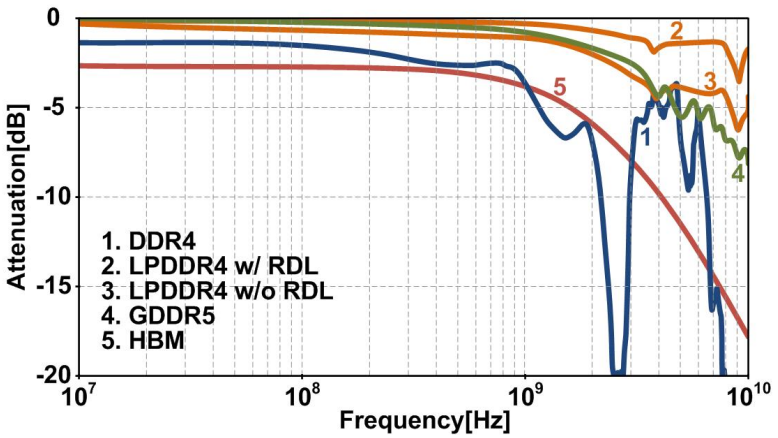


Fig. 2.7 Channel attenuation comparison between memory type.

where τ_1 and τ_2 are the relaxation time of multiple modeled dielectric constants, a is strength of it. Separately from the complex formulas derived by the reference [34], the mathematically expressed formulas for modeling the dielectric loss can identify channel losses that increase in proportion to frequency.

2.2 Memory Channel Characteristics

Memory channel using PCB-based channel is also affected by the channel noise, and reduced signal amplitude by channel loss causes interface margin problems. Although much efforts have been made to detect such problems, there are

difficulties in uncertainty due to many factors that can not be defined in the memory test sequence.

One of the uncertainties is that memory channel is not defined as standard specification. As a result, various channels exist due to the different board design for each company. This can lead to channels with problematic characteristics, and in combination with the characteristics of the DRAM interface, a unexpected fail phenomenon can occur.

Another uncertain element is that there are multiple memory types, like DDR4, LPDDR4, GDDR5, and HBM2. These memory types have different channel layout, channel loss, and channel material. The operating speed of each memory is widely span from 2Gbps to 8Gbps. Therefore, the ATE that has fixed channel characteristics has problems that cannot replicate the channel loss or noise of application specific environments.

The DRAM standards such as DDR4, LPDDR4, GDDR5, and HBM use different I/O channels of which loss characteristics span a wide range as Fig. 2.7. The silicon interposer channel of HBM has 4mm long and has 5dB loss at 2.4Gbps of operation. The major loss is caused from the conduction loss that includes low conductivity of silicon interposer channel and skin-effects. Therefore, it has short channel length than other product and low frequency operation speed, but the attenuation is not negligible. The mobile system has a loss value of 1 to 4dB at 4266Mbps, depending on redistribution layer(RDL) usage. The channel layout of mobile PoP is less than 1cm and the loss of the package substrate channel is small. But the RDL of the DRAM side has low conductivity value, and skin-effect of RDL increases signal attenuation. The GDDR5 has 3cm length and operates at 8Gbps, but the channel loss

doesn't exceed 5dB at operating speed. Because the improved FR4 material is adopted to reduce dielectric loss of channel.

Various memory use various memory channels, and f_T is an appropriate factor to define the characteristics of various kinds of memory channels. Conduction loss is a major loss of LPDDR4 and HBM2, while the GDDR6 is dielectric loss dominant.

Chapter 3

Channel-Emulating Model

In this work, we propose a test that emulates output waveforms through a transmitter, which can replicate various channel outputs. Fig. 3.1 is a HSL system that the work wants to test. In the HSL system, the signal is input to receiver after the signal output from the transmitter is attenuated through the channel. The degree of this attenuation is different for each channel, the previous ATE based test method requires a new board when the channel is changed. In Fig. 3.1, the proposed method uses an emulation driver that outputs an attenuated signal and the signal waveform can be controlled by a user control to replicate various channels. Therefore, it is possible to analyze and verify the desired system even on ATE base where new channel is not implemented. This improvement permit ATE test that correlated the application test, and programmable emulation drivers can be used to perform preliminary verification on the assumption of an arbitrary system.

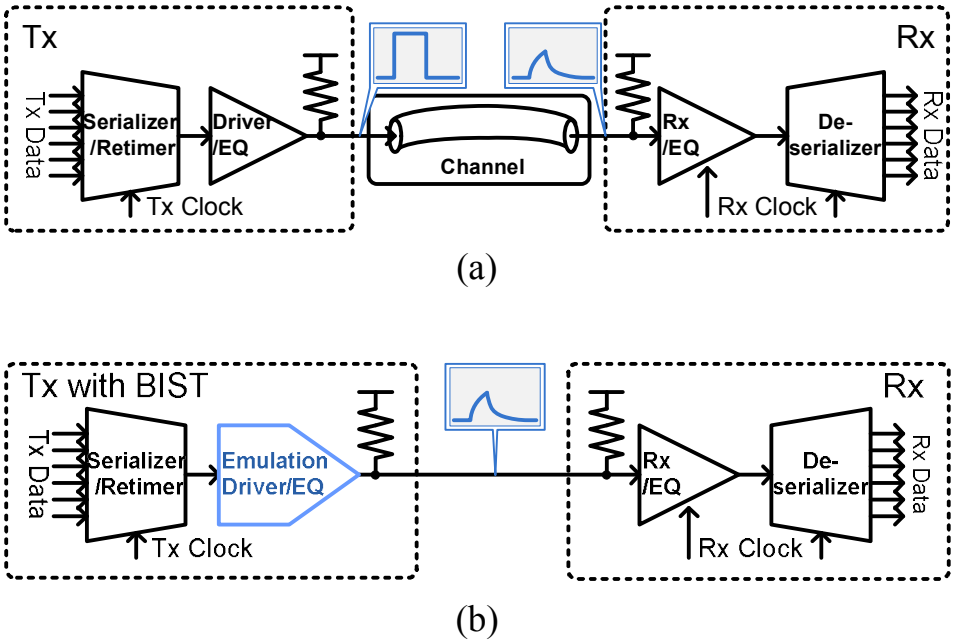


Fig. 3.1 The test environment of high speed link with: (a) the implemented channel on ATE, and (b) the emulation transmitter to remove the channel.

In this section, we will describe the process for finding a model for channel emulation. There are two ways to find the model for channel-emulating. First, we can create a model based on the proposed equation to express it based on the channel loss mechanism. Second, the inverse function of the transfer function that are used in the equalizer for compensating the channel loss in the high-speed serial link. Using these two methods, the suitable model is proposed with the basis function that can be implemented as an actual circuit.

3.1 Channel Loss Model

There have been a number of papers to analyze the waveform by transferring the skin-effect and dielectric loss equation described in the frequency domain to the timing domain [33][34][35]. From these papers, it refers the time domain function to model the channel loss, such as impulse response and step response. However, the problem of not being represented by close-form expression in the inverse Fourier transform of the channel model expressed by the phenomenon had been found in the previous researches, and the approximation method was used to solve this problem.

First, Dr. Schrader solved the impulse response by only modifying the attenuation of the cable channel. An approximation for the cable frequency transfer function (excluding propagation delay) is given as :

$$H(f) = e^{-\sqrt{j2\pi f\tau_1} - j2\pi f\tau_2} \tag{3.1.1}$$

where the skin effect (time constant τ_1) and the dielectric loss (time constant τ_2) cause dispersion and frequency dependent attenuation. The first term expresses skin-effect that degrade attenuation with square root of frequency, and the second term express the dielectric loss. The time domain channel response is get by using inverse Fourier transform, and the impulse response $h_s(t)$ of skin-effect and $h_d(t)$ of dielectric loss are expressed as, respectively.

$$h_s(t) = \frac{\sqrt{\tau_1}}{2t\sqrt{\pi t}} e^{-\tau_1/4t} \tag{3.1.2}$$

$$h_d(t) = \frac{1}{\pi\tau_2} \cdot \frac{1}{1+\left(t/\tau_2\right)^2} \tag{3.1.3}$$

The paper notes that "these impulse responses are theoretical approximations of the real cable impulse response, but nevertheless accurate enough over the frequency range of interest". But, these equations appear to have restrictions on casual conditions and it bases on the channel model without phase information. Even if some of the mathematical formulas have problems, there is a difficulty in defining the model of the emulator based on the mathematical formula. In the case of the skin effect, the $1/t\sqrt{t}$ function combined with the exponential decay function is not suitable as the basis function.

Secondly, Dr. Svensson obtains the transfer function of a transmission line and describes the skin-effect and dielectric loss separately as equation (2.1.8) and (2.19). The solved equations are still contained approximations, but it include the phase information's and solves non-casual problem. The step function of skin-effect and dielectric loss are expressed as:

$$o_s(t) = \operatorname{erfc}\left(\frac{r_s}{2\sqrt{2}Z_0\sqrt{t}}\right) \tag{3.1.4}$$

$$o_d(t) \approx 1 - e^{\sqrt{\left(t/0.27a\sqrt{lc_0}\right)}} \tag{3.1.5}$$

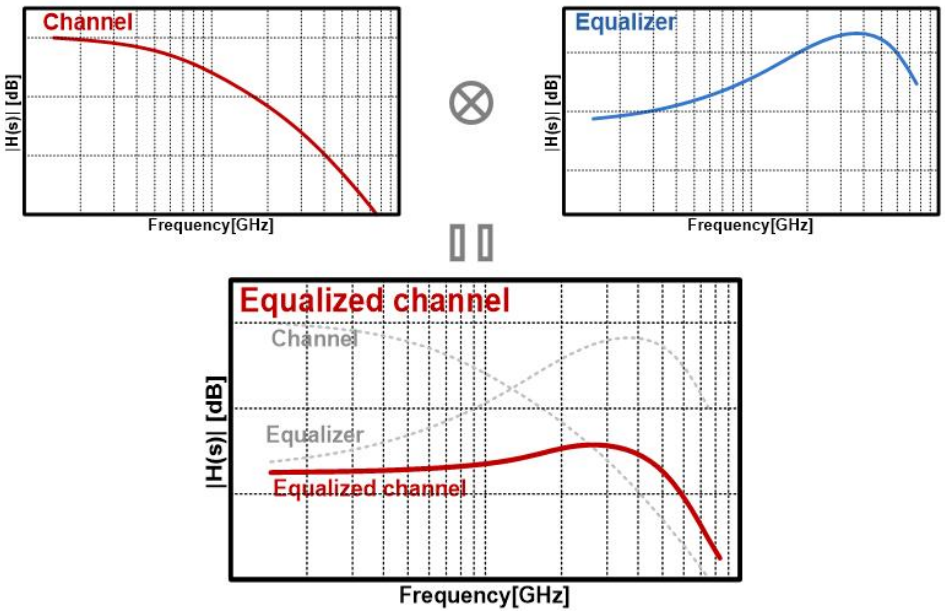


Fig. 3.2 Transfer function analysis of the channel equalization.

where erfc is the complementary error function, r_s is dc resistance value per unit, Z_0 is impedance of the channel, and *lc* is inductance and capacitance per unit length. It includes an error function that can not be implemented, and the dielectric loss is same as the skin-effect. The time domain equations of the channels can be used to represent signal waveforms, but they are not consistent with our goal of emulating the circuit as mentioned above.

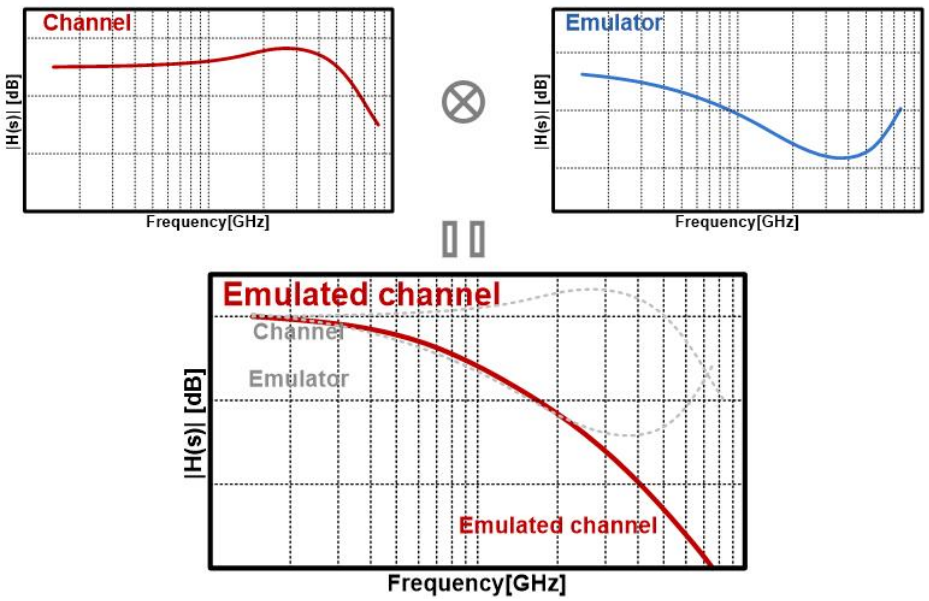


Fig. 3.3 Transfer function analysis of the channel emulation.

3.2 Channel Equalization and Emulation

Channel equalization techniques to compensate channel attenuation can be applicated to the emulating the channel noise. Because the emulation and equalization techniques are based on the same principle. The channel equalization has aim to restore a original signal that inputs to the channel. The frequency response is a good method to achieve the equalization aim as Fig. 3.2 (c). At the Fig.

3.2 (a), the transfer function of the channel is a form in which the gain decreases as the frequency increases like low pass filter. The skin-effects and the dielectric loss are major factors to induce attenuation with the frequency increases. The equalization is performed to get a flat response within operation frequency range by multiplying the transfer function to lossy channel. The optimal equalization is inverse shape of the lossy channel as the Fig. 3.2 (b). As a result, the equalized channel multiplied by the lossy channel and the equalizer has a flat transfer function in the operating domain.

The emulation is similar to equalization, and Fig. 3.3 shows the emulation procedure. The channel emulation wants to generate lossy channel response by using inverse transfer function of equalizer. But the emulation system uses very short channel that has negligible attenuation, and it could be compare as the result of the equalized channel at the Fig. 3.3 (a). The purpose of the channel emulation is to replicate a lossy channel with multiplying the flat channel and the emulator. If the emulation block has inverse of the channel equalizer that uses for channel compensation, the product of the very short channel and emulator will be same as the lossy channel.

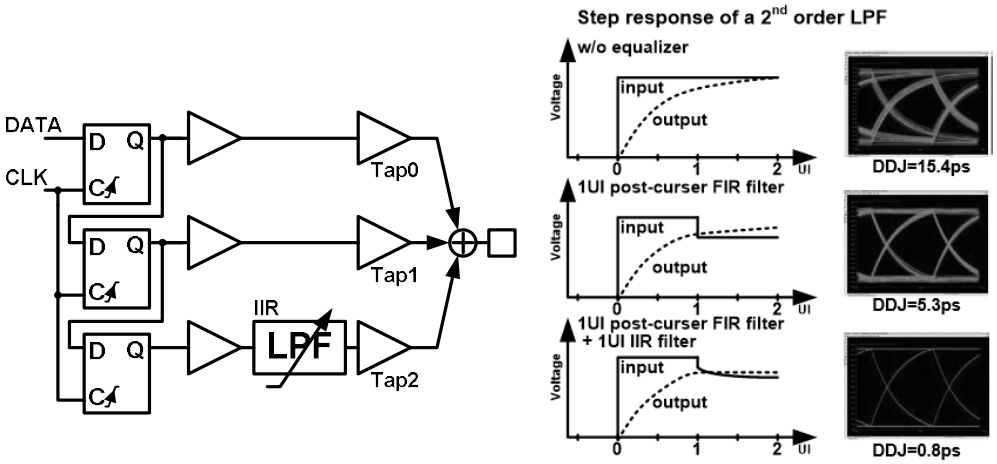
The previous research about the channel equalizer is useful to implement the channel emulator. Because, the inverse transfer function of channel equalizer is same as the emulator. Especially, a lots of equalization techniques are studied to compensate the dielectric loss, and it can be used for dielectric loss emulator. The previous research on the channel equalization will be introduced at the next sub-capture.

3.3 Skin-Effect Emulator

3.3.1. Skin-effect equalizer

The skin-effect is expressed with root square term of frequency as Eq. (2.1.2), and previous equalizer, such as CTLE, with transfer function of exponential function cannot make flat transfer function by compensating loss causes by the skin-effect. Furthermore, the skin-effect is hard to find satisfied transfer function when using the model formula and equalizer. Because, the skin-effect depends on the root square of the signal frequency, which don't have suitable circuit with an inverse function [25]. Therefore, the previous researches have attempted to solve problems through optimal combination of exponential functions.

The skin-effect is getting more important to reduce more channel noise in the higher speed serial link. The previous researches are effective to compensate dielectric loss, but the low frequency channel noise is remained. Therefore, equalizer is getting complex and bigger to compensate the remained noise. A solution is suggested by Crit [20] and Parikh [21]. Each of researches suggested band pass filter that may be suitable for a specific case channel.

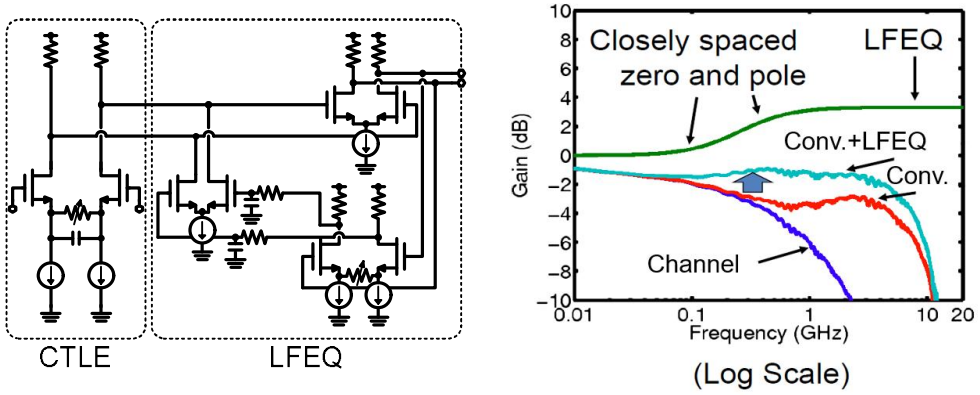


(a) (b)

Fig. 3.4 (a) Tunable LPF architecture and (b) simulation results for an ideal transmitter driving an LPF [20].

Crit proposed transmitter that includes IIR filter to compensate skin-effect as Fig. 3.4. A half-UI post-cursor FIR filter is adopted for compensating dielectric loss of channel, and IIR filtering are purposed to compensate the remained ISI. The remained ISI is caused from the skin-effect of channel. It announced the traditional post-cursor transmit equalizer cannot eliminating the ISI introduced by the 0.35GHz pole form the skin-effect, but it proves the additional curser with IIR filter can reduce it. The IIR filter is a equalizer based on the exponential functions and is limited in its ability to compensate for the skin-effect.

Parikh proposed the CTLE that aims to compensate skin-effect by using IIR filter [21]. It also announced conventional equalizers cannot compensate for the small amount of low-frequency loss, because the skin-effect has different frequency response(3dB/dec) from the dielectric loss(20dB/dec). Therefore, the work proposed



(a) (b)

Fig. 3.5 (a) The CTLE and low-frequency equalizer unit and (b) frequency-domain responses of a backplane channel with and with low frequency equalization [21]오류! 참조 원본을 찾을 수 없습니다..

CTLE with low-frequency equalizer(LFEQ) that implements a small amount of equalization (0 to 4dB) to compensate for the gentle slope of the low frequency loss due to skin-effect. It implements a zero at low frequency (500MHz) through a feedback topology like Fig. 3.5. The proposed IIR filter is effective in removing remaining ISI from the skin-effect, but the mismatch between transfer function of the proposed equalizer and skin-effect remains to be an error. The previous work already discussed about the skin-effect has different response, but the proposed circuits are using the zero at the low frequency area. As a result, the signal of a specific region will be over-boosting and it needs to minimize the distortion. Thus a proper function is required to effectively emulate the skin-effect.

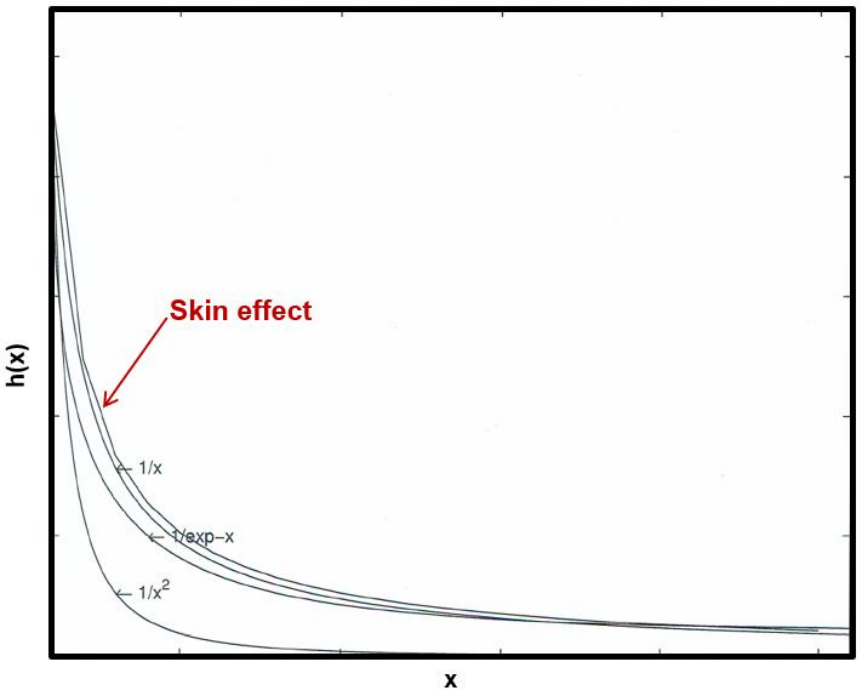
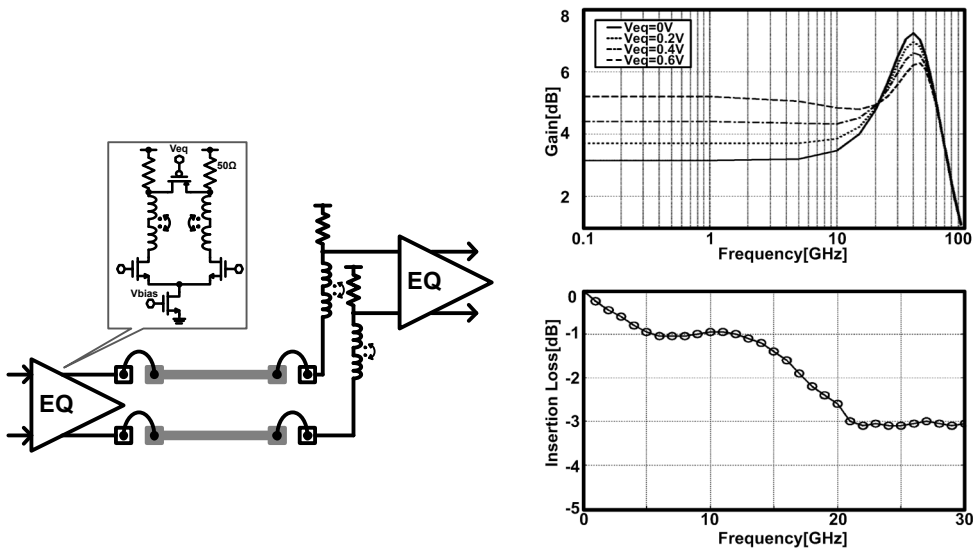


Fig. 3.6 The impulse responses of the skin-effect and various functions.

3.3.2. Skin-effect emulator

This work needs to find a new basis function that can substitute the unrealizable skin-effect modeling function. In the time domain, the skin-effect expression is described as an multiplicative inverse and exponential decay product that is too complex to implement, therefore, Schrader adopts numerical computation rather than mathematically calculation to find ISI residue [25]. To find implementable basis



(a) (b)

Fig. 3.7 (a) The unit analog block (tunable G_m cell) and (b) array composition of the unit block in the field-programmable analog array [23].

function, the impulse responses of known circuit are compared with impulse response of skin-effect. Fig. 3.6 shows the result. The reference curve is the result of fast Furrier transform result of the skin-effect. And it is compared with exponential function, multiplicative inverse, and square of multiplicative inverse. As the result, the multiplicative inverse shows more suitable form than the exponential function. This exhaustive search outputs the interested function as:

$$h_{se}(t) = \frac{\alpha_{cs1}}{\alpha_{cs2}t + 1} \cdot u(t) \qquad (3.3.1)$$

where α_{cs1} and α_{cs2} are the coefficients of time domain basis function.

The step response of multiplicative inverse is logarithm function. And the logarithm function has several examples of implementation. An example is the logarithmic amplifier, and it is widely used in radar systems. The receivers in radar system is needed to limited output range, even if an input signal has high dynamic range [22]. Instead of unrealizable error function, the logarithmic can accurately represent the step response of the skin-effect.

3.4 Dielectric Emulator

In order to emulate the dielectric loss, the exponential decay function is selected to the basis function for expressing the impulse response, which is set with reference to previous channel equalization methods. As the work has analysis in the previous chapter 3.2, the work has not found suitable basis function for dielectric loss in the time do-main. However, based on the recent development of equalizer compensation techniques for dielectric loss, which is a major component of channel loss, a consistent basis function can be established.

3.4.1. Dielectric equalizer

The continuous time linear equalizer (CTLE) is a typical way to compensate the loss caused by a lossy channel. The CTLE transfer function can boost the gain of the

operating frequency range to create a platted output response. Dr. Kim implements the equalizer by using inductive peaking shows effective compensating the channel loss from the 40Gbps channel [24]. Fig. 3.7 shows the equalizer in the paper. The inductively-peaked CML buffer with an MOS device bridging the two resistor loads operates as de-emphasis equalizer. The inductor blocked the high frequency current and connects the low frequency signals. Therefore, the high-frequency gain of the equalizer is fixed by the inductances, and low-frequency gain is determined by the load resistance. The high-frequency gain will properly compensate the channel loss from 10GHz to 20Ghz, and the flat response will be achieved by the equalizer. It contains complex poles in the transmitter to compensate the channel loss, but the zero also has same transfer function of it at the gain perspective. Dr. Srikanth Gondi compares the compensation output between complex pole and real zero and implement the equalizer by merging the both schemes [31]. The capacitive degeneration schemes is efficient way to provide the real zero on the receiver, but the degenerated structure trades this gain-bandwidth product for the boost factor.

3.4.2. Dielectric emulator

Since the dielectric loss has a behavior characteristic that the amount of channel attenuation increases in proportion to the frequency, the exponential decay function is chosen, which is the impulse response of the low pass filter using single pole. The CTLE uses to compensate for the dielectric loss compensates the channel loss by using degeneration capacitive element is a good reference to the selection. The low

pass filter by using RC network is proper solution of the dielectric loss emulator that has inverse characteristic of the CTLE, and the impulse response $h_{de}(t)$ of emulating dielectric loss is expressed as :

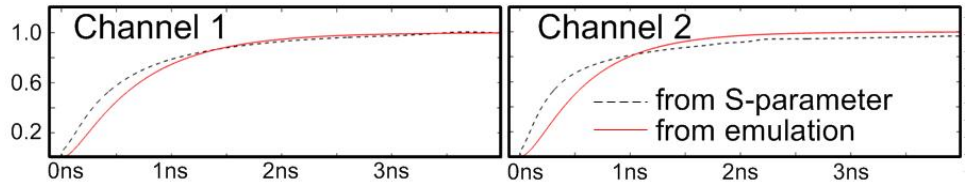
$$h_{de}(t) = e^{-\alpha_{cd}t} \cdot u(t) \tag{3.4.1}$$

where α_{ds} is the coefficient of time domain basis function.

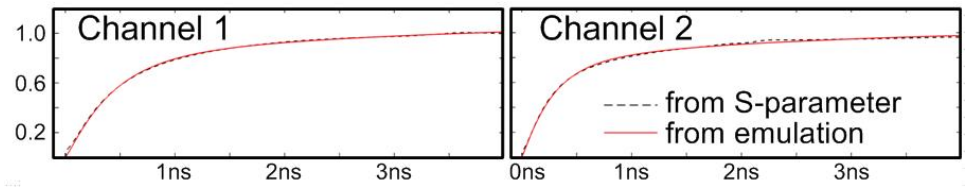
3.5 Emulation Model Proposal

This work suggests the logarithmic function to model the step response of skin-effect and the exponential function to model the impulse response of dielectric loss in time domain. Instead of unrealizable error function, the $1/t$ can accurately represent the impulse response of the skin-effect and it transfers to step response. The exponential function is suitable for emulating dielectric loss, and it has been shown to compensate dielectric loss in previous research. The proposed model equation is expressed as:

$$o(t) = a_0 \log(a_1 t + 1) * e^{-a_2 t} \tag{3.5.1}$$



(a)



(b)

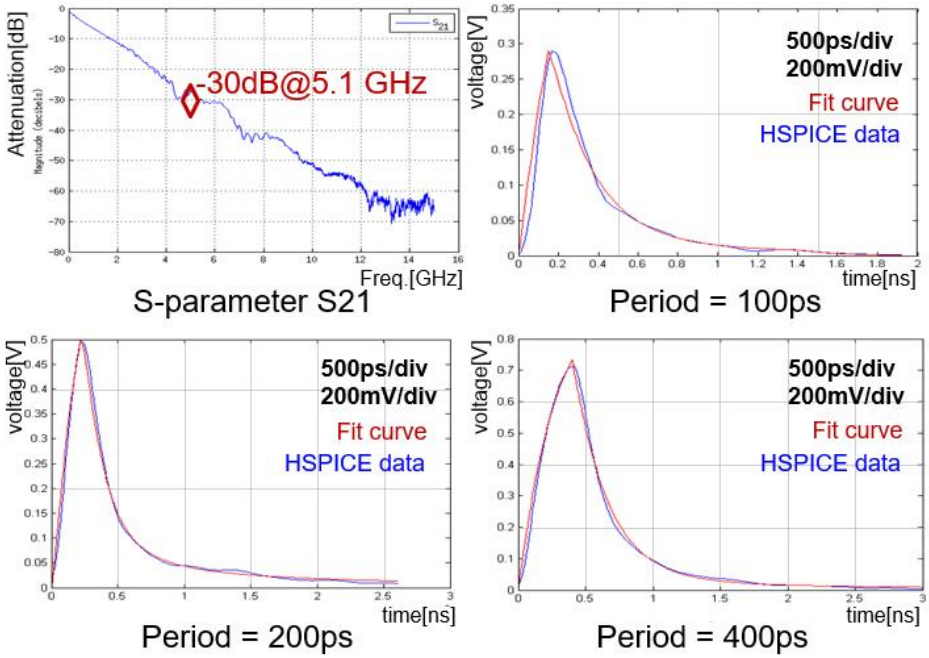
Fig. 3.8 The step responses comparison with S-parameter and: (a) the emulation with two exponential function, (b) the logarithmic and exponential function.

where a_0 is coefficient signal amplitude, a_1 is coefficient parameters for skin-effect modeling, and a_2 is for dielectric loss.

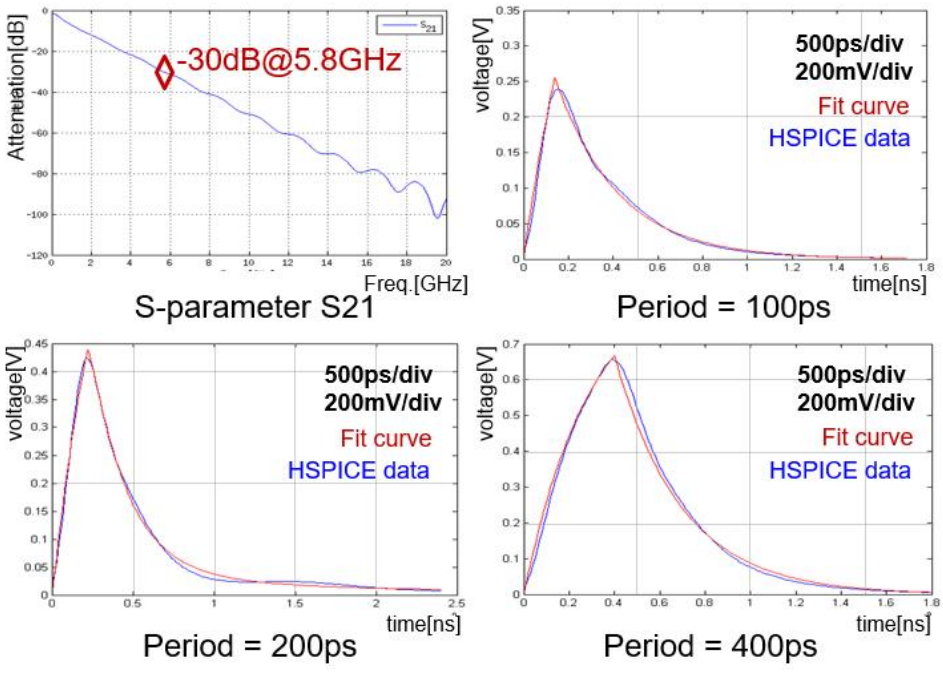
To verify the consistency of the proposed model, the following simulations are performed. Fig. 3.8 shows the step response results comparison between the proposed model and previous approach that uses multiple exponential functions. The dotted line is step response from the channel model with s-parameter, and the solid line is the proposed model and the multiple exponentials. The used channels are downloaded from IEEE802.3 task group website, and it shows dissimilar step response that caused by different skin-effects and dielectric losses. The proposed model results are more similar to s-parameter regardless of the channels, whereas the exponential-only model has certain errors. The first channel has more attenuation

than second channel due to use FR4 material, and the second channel uses advanced FR4 material that has small dielectric loss and large skin-effect. In case of exponential only model, it suffers to fit low frequency loss. It also raises the error in the high frequency range to match the low frequency loss. But the logarithmic function of proposed model replicates the low frequency band and the high frequency band reproduces through the exponential function, therefore, the both channels are precisely matched.

The proposed model confirms the coherence of the emulation results of other channels as Fig. 3.9. It is simulation result of three channels that has different attenuation. First channel has -30dB loss at 5.1GHz, second channel has -30dB at 5.8GHz, and last channel has -30dB at 7.2GHz. In this simulation, we compare the single bit response between HSPICE with s-parameter and the proposed model. The various period, such as 100ps, 200ps, and 400ps, are used. The results show that the proposed model has high consistency. But, there is a problem that the proposed model shows a certain error in the channel where the reflection is observed. Fig. 3.10 shows the matching result when the channel has impedance mismatch. As can be expected without the result, the proposed model does not have a term that emulates the signal reflection form the channel impedance mismatch, therefore, the fitting curve induces modeling error when the channel output waveform is distorted by the reflections.


Attenuation[dB]
-30dB@5.1 GHz
Freq.[GHz]
S-parameter S21
voltage[V]
500ps/div
200mV/div
Fit curve
HSPICE data
time[ns]
Period = 100ps
Period = 200ps
Period = 400ps

(a)


Attenuation[dB]
-30dB@5.8GHz
Freq.[GHz]
S-parameter S21
voltage[V]
500ps/div
200mV/div
Fit curve
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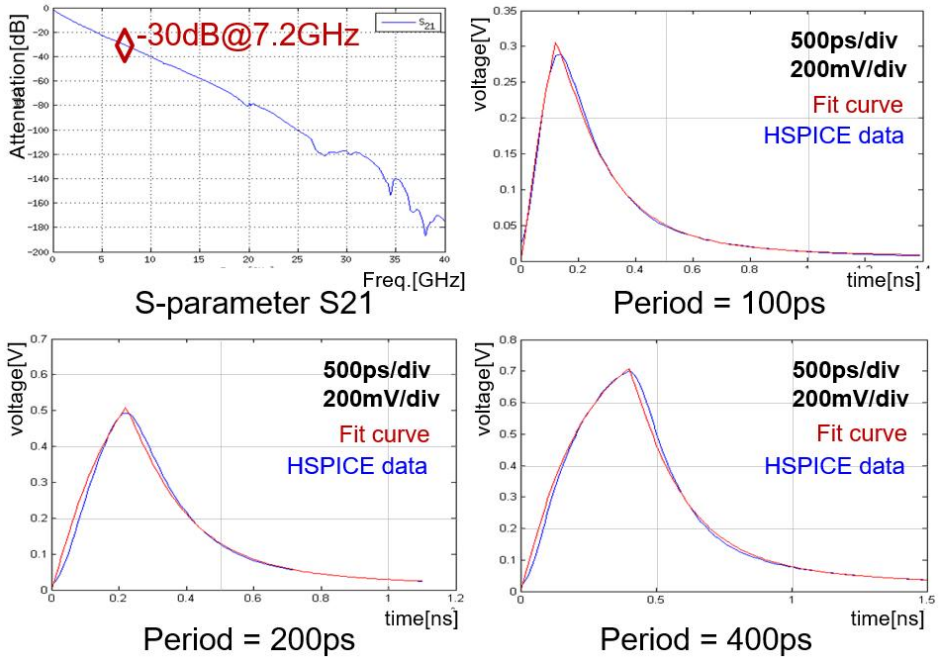
Period = 400ps

(b)



(c)

Fig. 3.9 The single bit responses comparison with S-parameter and various channels: (a) 30dB loss at 5.1GHz, (b) 30dB loss at 5.8GHz, (c) 30dB loss at 7.2GHz.

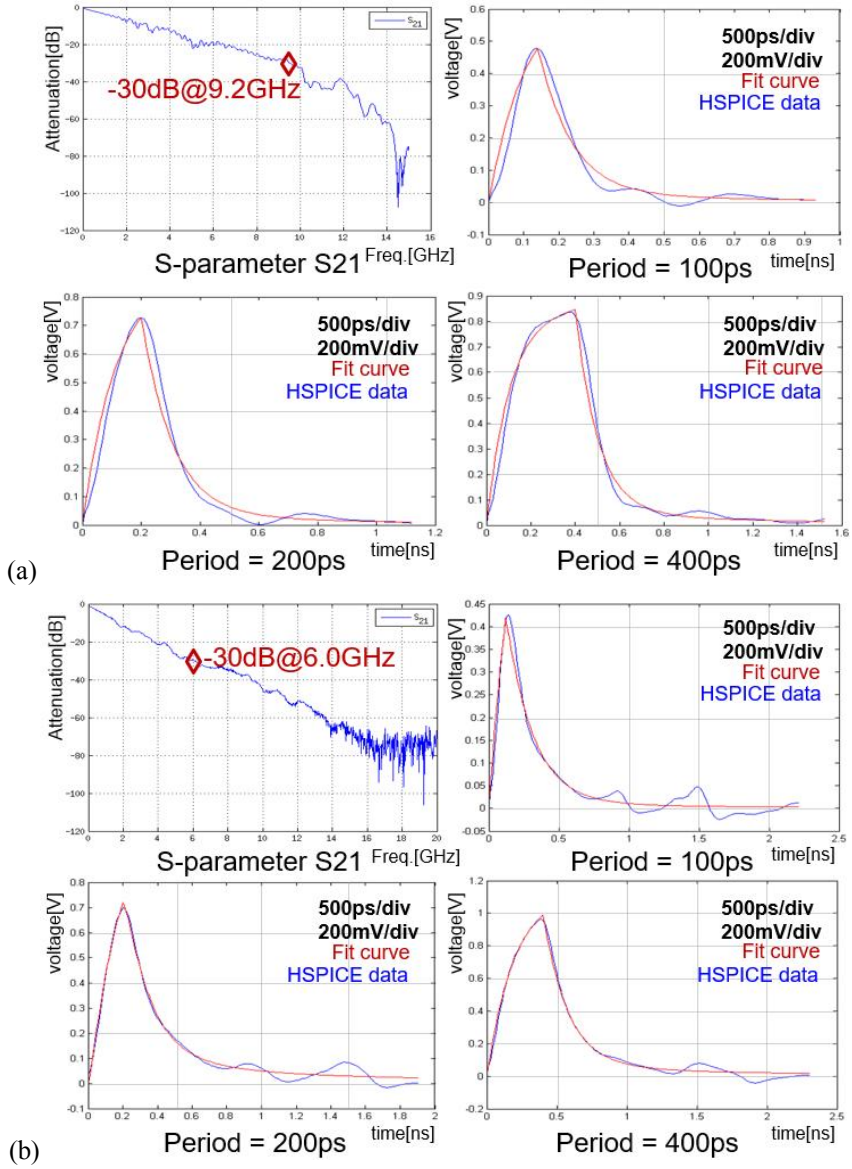


Fig. 3.10 The single bit responses comparison with S-parameter and various channels, which one has reflection noise: (a) 30dB loss at 9.2GHz, (b) 30dB loss at 6.0GHz.

Chapter 4

The Architecture of Channel-Emulating Transmitter

This chapter explains an architecture for embodying the proposed channel emulation model. It tries to present the methods and problems for the architecture that implement the proposed basis function and discusses the importance of the emulation degrees of freedom considered in the architecture. This will explain each of the skin-effect emulator and dielectric emulator previously proposed.

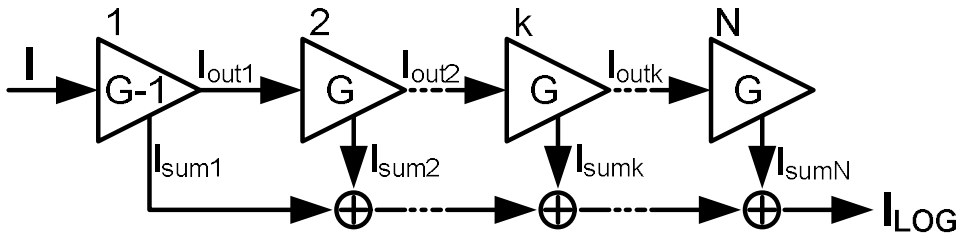


Fig. 4.1 The pseudo logarithmic amplifier that has series connected limiting amplifier.

4.1 Logarithmic Approximation

The proposed skin-effect model, the logarithmic function, is specified by referring to the radar system. The high dynamic input range of logarithmic amplifier is suitable for receiving radar signal that has variations in received input power of over 100dB. This characteristic makes the radar receiver universally adopts logarithmic amplifier [22]. Two basic types of logarithmic amplifiers are commonly used, and we select the true types instead of the demodulating types due to simplification. The demodulating logarithmic amplifiers detects the signal envelope to provide logarithm of the signal, but True logarithmic amplifiers provide the logarithm of the signal without detecting or demodulating the signal.

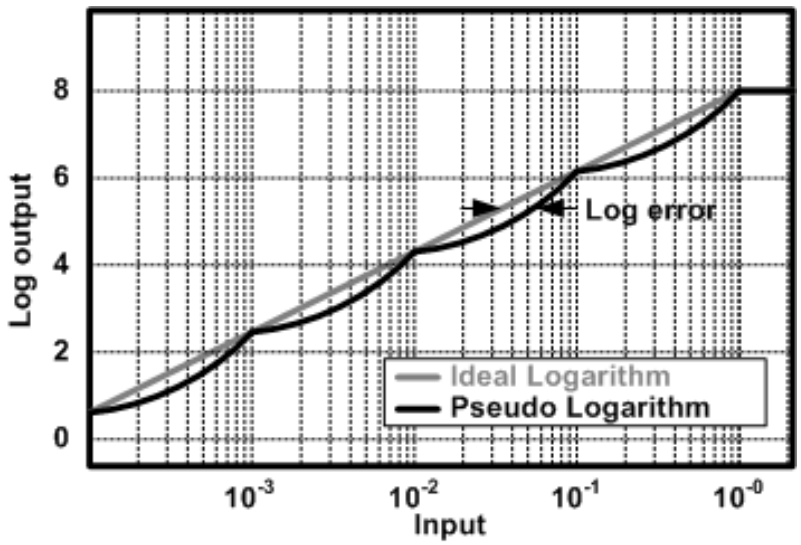


Fig. 4.2 The error between ideal logarithmic function and linear-limit logarithmic function.

4.1.1. Pseudo-logarithmic approximation

The pseudo-logarithmic approximation is efficient way to implement logarithmic amplifier than single-stage logarithmic amplifier that uses complex non-linear feedback amplifier [22] [23]. The non-linear feedback amplifier uses the BJT component for feedback gain stage of amplifier, therefore, it has large variation and design difficulties. The BJT area and DC operating condition are burden to adopts it, and the BJT is larger than other components in CMOS process and also lateral type BJT model has large process variation. Furthermore, the operating condition of DC will reduce design freedom of logarithmic amplifier.

Table. 4.1. Current calculations example of three stage pseudo-logarithmic amplifier

I	I_{SUM1}	I_{SUM2}	I_{SUM3}	I_{LOG}
0.001	0.001	0.009	0.09	0.1
0.01	0.01	0.09	0.9	1
0.1	0.1	0.9	1	2
1	1	1	1	3
10	1	1	1	3

Fig. 4.1 shows the general idea of pseudo-logarithmic approximation. The pseudo-logarithmic amplifier consists of serially connected limiting amplifier. The limiting amplifier consists of a cascade of dual gain cells, with each cell having a high-gain limiting amplifier in parallel with a unity-gain buffer. Each stage will amplify until the signal is smaller than the limiting threshold, and the signal becomes larger, a point will be reached at which the limiting amplifier in the last stage ceases to amplify and provides a constant current. As the input signal becomes larger and the limiting amplifier reaches the threshold level, the second will progressing same operation and it will continuously repeat to last stage. Meanwhile, the buffer amplifiers in all stages will continue to pass the signal. Fig. 4.2 shows the response, approximates a straight line when plotted on a semilogarithmic axis.

As an example, the table 4.1 shows a linear relationship for the input current range of 0.001mA to 10mA. Three stage of pseudo-logarithmic amplifier ability to generate the desired logarithmic characteristic. The linear amplifying operates with the range between 0.01 to 1, but the last input current of 10 result saturated output of 3. This is due to the fact that it has already limited completely, and thus the output

current will always remain constant after the input reaches 1.

This pseudo-logarithmic amplifier has model equation as:

$$I_{LOG} \approx N \cdot \log_G(I) \tag{4.1.1}$$

where N is stage number of limiting amplifiers, and G is the gain value of each stage. The base number of logarithmic function is decided by the gain of the amplifier. In this equation, the current input and output are used to describe the logarithmic function, but it could be changed to voltage.

4.1.2. Pseudo-logarithmic for data input

The in-output pseudo-logarithmic amplifier needs to be changed to the data stream that has time information. The input is the step response waveform and the output is the logarithmic waveform over time axis. The previous radar receiver uses logarithmic function at DC domain, such as DC input to DC output, which one has enough bandwidth to threat the input signal. But the work requires the operation that can handle bit stream input to logarithmic function of time input variable.

The proposed method shows in Fig. 4.3. It is conceptual block diagram to compose the bit stream input to logarithmic waveform output. The input pattern data

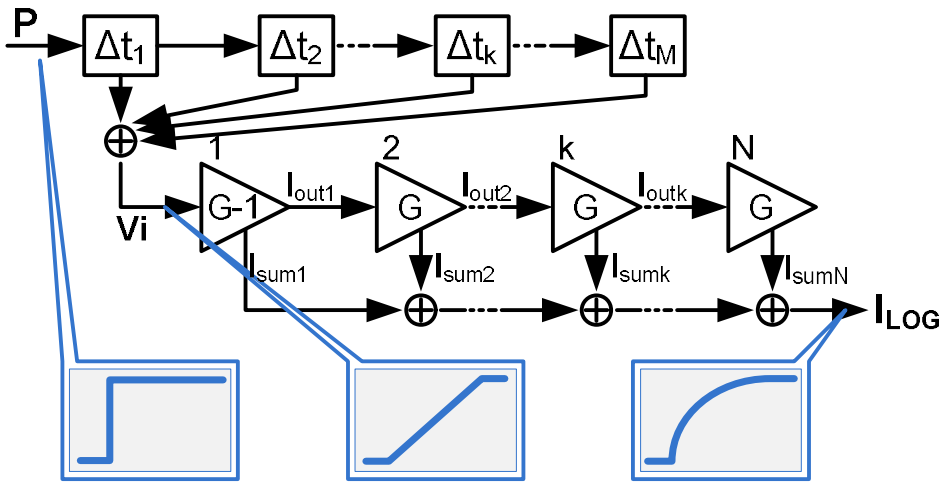


Fig. 4.3 The pseudo logarithmic amplifier that has data input pattern.

goes through M stages of unit delay, which one has the delay Δt_D, and each output of unit delays are added together. This piecewise linear output will have a linear value as the delay unit value is fine. This linearly varying input on the time axis is input to the log amp, it results output waveform of logarithmic function to the time axis through the logarithmic amplifier. At this time, the function of log is changed according to the rising time of the input triangular wave. This conceptual approach provides logarithmic function of bit stream input, but it is difficult to combine the output of delay units, implement small delays, and implement a logarithmic amplifier with a sufficiently large bandwidth. Therefore, the complexity of the conceptual block diagram would be reduced.

Alternative block diagram of logarithmic amplifier of bit stream data is shown at Fig. 4.4. In order to reduce complexity of the previous structure, a linear input by

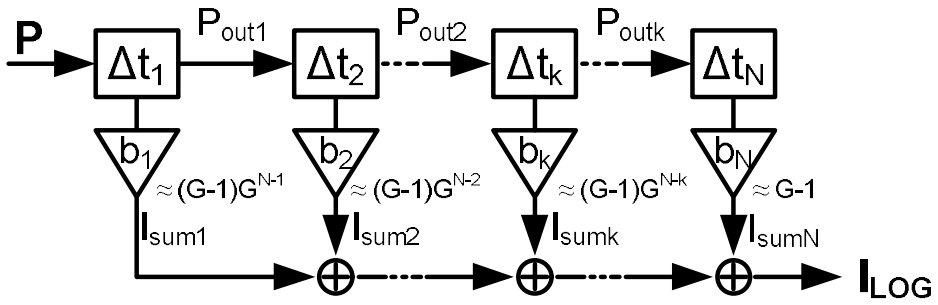
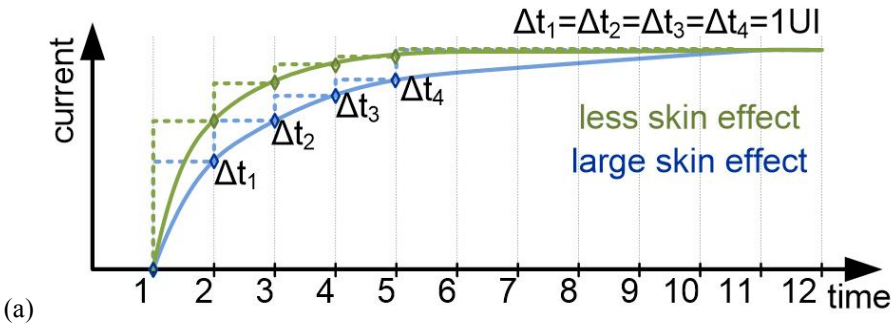


Fig. 4.4 The modified pseudo logarithmic amplifier that has data input pattern.

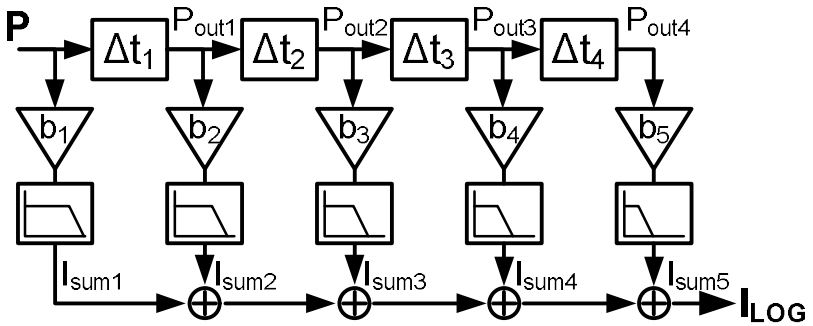
delay units are divided into separate limiting amplifier stages. And the gain of each stage is decided according to the previous pseudo-logarithmic approximate. If the stage number is N, the first stage has gain of $(G-1)G^{N-1}$ that has the largest gain And the gain of remain stages get decreased with the proportional ratio. The all sum of the signal will have the wanted signal amplitude.

Therefore, it provides logarithmic function of time scale. But, the number of stage can make limitation of the function implementation. The purposed of the logarithmic amplifier is implementing skin-effect emulator, and it needs flexibility to replicate various amount of skin-effects. But the fixed conditions of pseudo-logarithmic amplifier loss the freedom of degree as Fig. 4.5. There are two channel conditions, first one has less skin-effect and second one has large skin-effect. If it has fixed delay unit of 1UI, then the first case will have large error at the 1st unit stage and the second case will have large error at the last stage.

Fig. 4.5 (b) shows the proposed solution to increase degrees of freedom by providing the flexible gain and time delay. Both knobs are independently controlled



(a)



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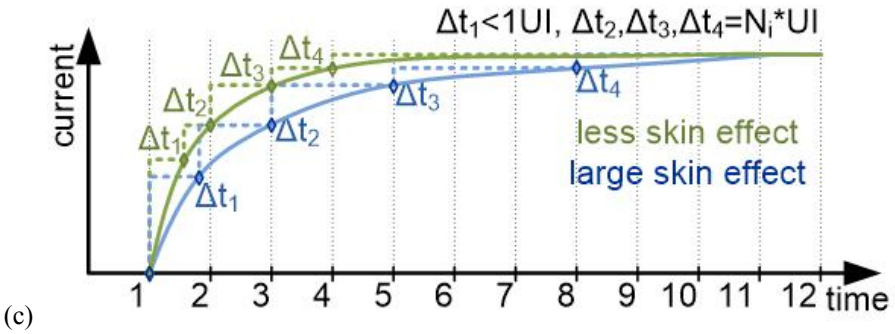


(c)

Fig. 4.5 The pseudo logarithmic amplifier and timing diagram: (a) the error when it has the fixed timing resolution, (b) the modified logarithmic amplifier that has variable delay resolution and gain, (c) the error when it has the modified logarithmic amplifier

and ensure high degrees of freedom. It enables emulation within a small error regardless of the skin depth as shown in Fig. 4.5 (c) by taking the small delay unit at first and the large delay unit at last. The first delay unit is controlled by absolute time, like ps unit, for improving high frequency resolution of step pulse, and the remain delay units are controlled in UI units for reducing low frequency error. And this work suggests adding a low pass filter to each stage, each of which has different cut-off frequency. The current added through the amplifier between each stage has a staircase shape, and this transition increases the quantization error as the delay value increases. The proposed low pass filter can reduce the errors even if the delay is controlled in UI units.

4.2 Dielectric Loss Emulator

Fig. 4.6 shows block diagram of the dielectric loss emulator. The CTLE is a representative equalizer, and it is configured through the high pass filter. The inverse transfer function of equalizer is low pass filter and it is suitable for dielectric loss emulator. A dielectric emulator is configurated by connecting a low pass filter which is designed to adjust the cut-off frequency at the output of the block to emulate the preceding skin-effect. The front side low pass filter can be removed, because the low pass filters are overlapped between the dielectric emulator and the skin-effect emulator. Especially the first and second stage of low pass filter has higher cut-off frequency than the low pass filter of dielectric emulator. However, the quantization

error of the remain stage can be increased by removing the low pass filters that have lower cutoff frequency.

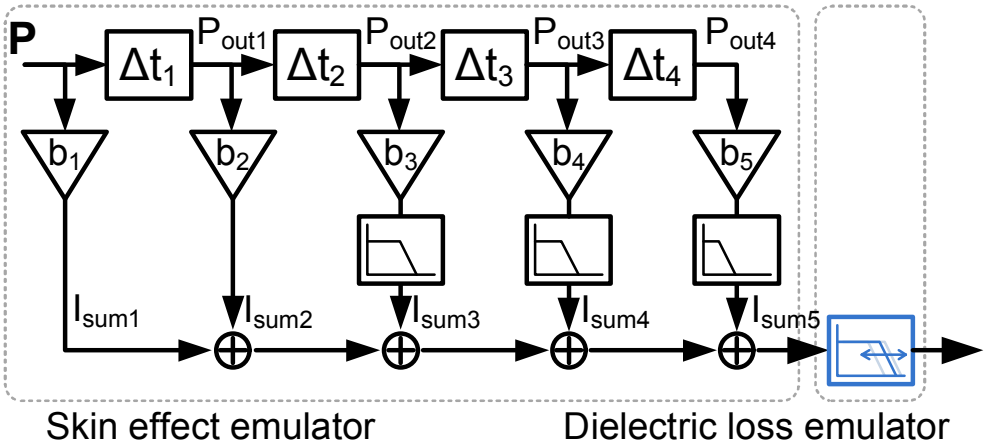


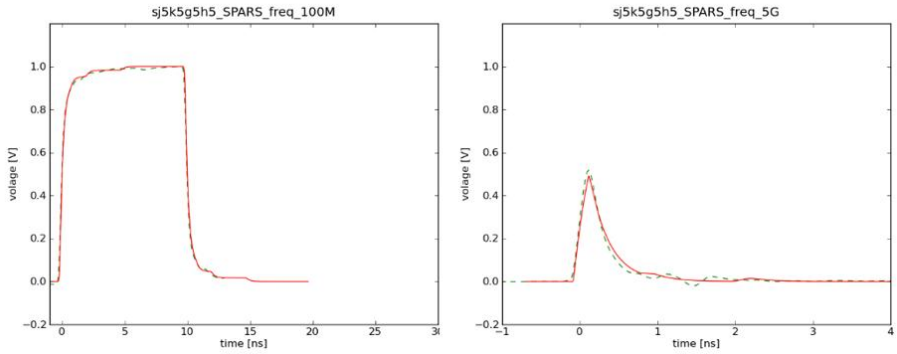
Fig. 4.6 The dielectric loss emulator.

4.3 Emulating Results

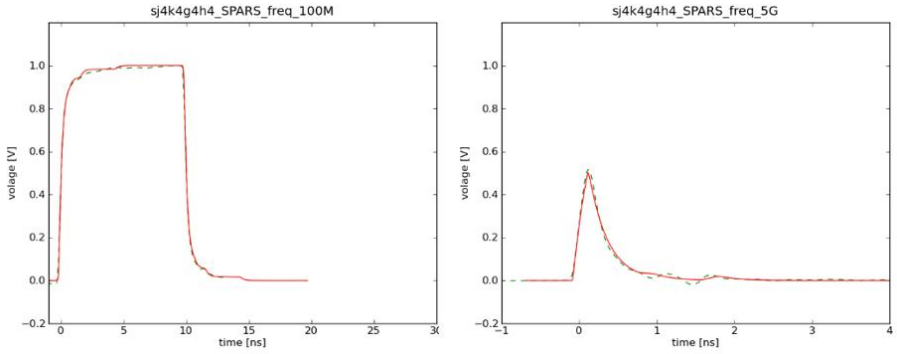
Based on the proposed architecture, we simulate emulator performance by comparing single bit response and step response with S-parameter result. The proposed architecture is composed with MATLAB and finds the optimized coefficients. The project is set up according to delay of delay units, gain of amplifiers, and cut-off frequency of low pass filters as a variable. The green dotted

line in the graph is the result of HSPICE using the S-parameter, and the red solid line is the result of putting the optimal coefficients into the MATLAB architecture. The left side shows the step response and the right side shows the single bit response of 200ps. And four channels are derived from the task group of IEEE 803.2. In order to verify the consistency of the proposed architecture based on the proposed model, which was verified through comparison of the four channels. A pseudo-logarithmic approximation block that reduces the quantization error accurately emulates the skin-effect with a step response and a single bit response. Likewise, the modeling of the dielectric loss and the matching of the architecture configuration can be confirmed.

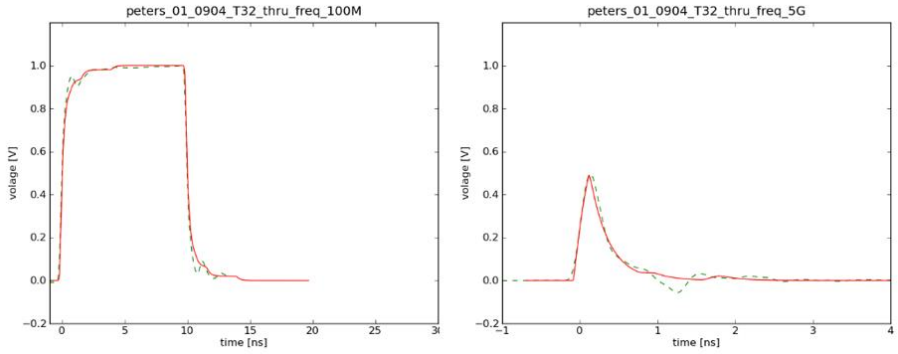
(a)


sj5k5g5h5_SPARS_freq_100M
sj5k5g5h5_SPARS_freq_5G
volage [V]
time [ns]

(b)


sj4k4g4h4_SPARS_freq_100M
sj4k4g4h4_SPARS_freq_5G
volage [V]
time [ns]

(c)



(d)

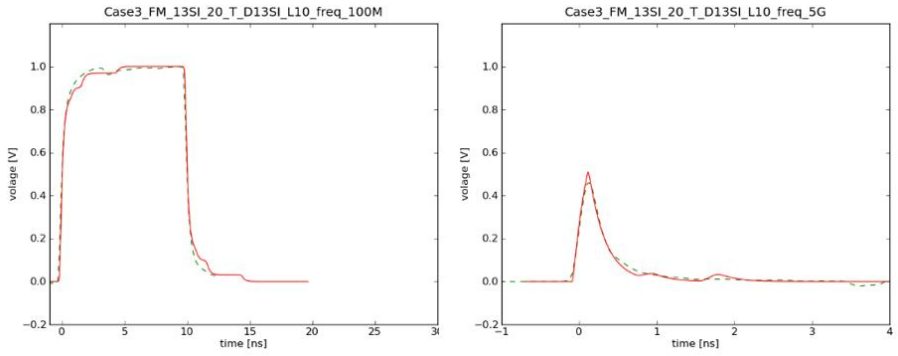


Fig. 4.7 The step response and single bit response comparison between the proposed emulating block and spice results: (a)~(d) various channels from IEEE802.3ab

Chapter 5

Circuit Implementation

This chapter also describe circuits use to describe each proposed architecture and explains key performance indicators that should be taken into account in constructing the emulator circuit for BIST operation. For example, it is hard to increase the degree of freedom without affecting basic performance of transmitter. The CML circuits are used to solve the problem of performance degradation due to the large programmability that has difficulty in circuit implementation. In addition to the CML circuitry, some of the parameters could be handled in a circuit implemented in digital to reduce the burden on speed for damage to the area. And it will be described about the pattern generation and the clock generator is designed for ease of test.

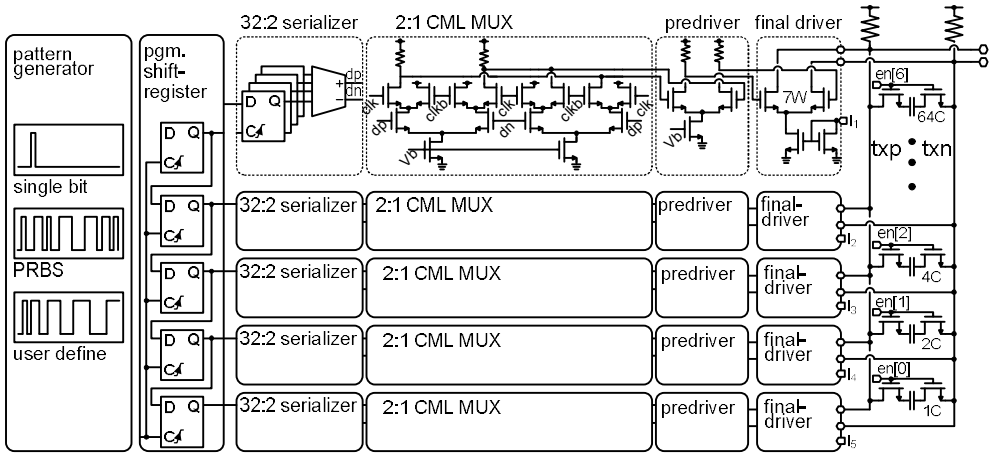


Fig. 5.1 The proposed channel-emulating transmitter architecture.

5.1 Proposed Emulation Architecture

Fig. 5.1 is the block diagram when the proposed architecture is implemented by the circuits. A programmable shift register, serializer, and driver are configured to implement a channel-emulating transmitter. The pattern generator is existed to support testing the channel emulating functions, which one generates single bit pattern, step patterns, pseudo random bit stream patterns, and user defined patterns. After generating test patterns, the shift register shifts the pattern to serializer of 5 tap according to the programmed value. As mentioned earlier, shift registers 3 to 5 are shifted in UI units and shift register 2 is in time scale units. The shift register output is connected to a 32: 2 serializer configured in CMOS. This work has placed the shift register before the serializer to facilitate the implementation of the logarithmic

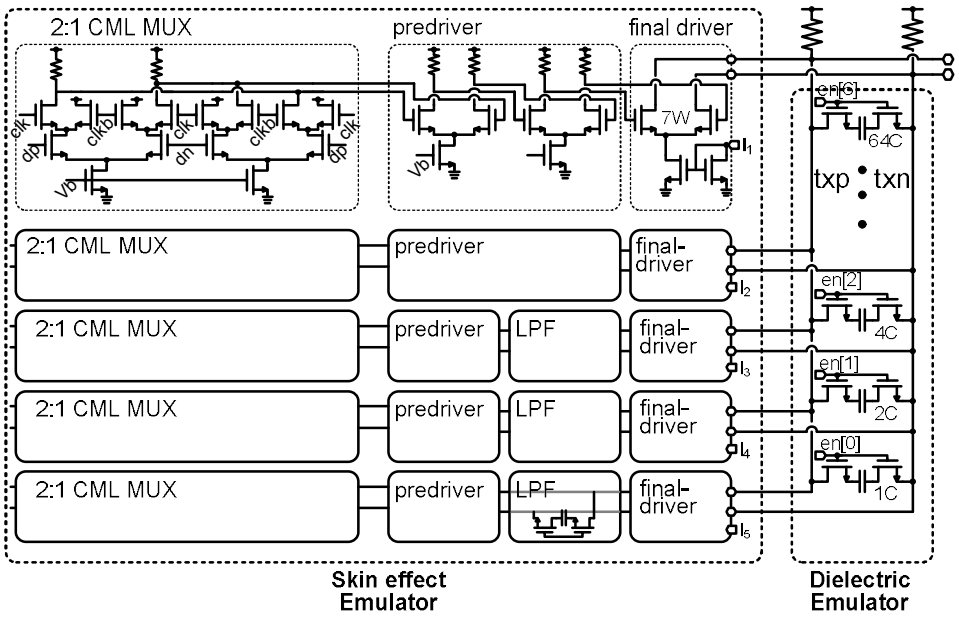


Fig. 5.2 The proposed transmitter to simulate skin-effect and dielectric loss.

function. Even as the number of serializers increases, the speed margin places programmable shift register operates at low-frequency. After that, the current mode logic(CML) is used to configure high speed MUX and amplifier to implement the pseudo-logarithmic amplifier. And the programmable low pass filter locates at the output node of transmitter. The details will be discussed in the sub-chapters.

5.1.1. Transmitter

Fig. 6(a) shows proposed transmitter circuit to emulate skin-effect and dielectric

loss attenuation. The proposed emulating transmitter selects the current mode driver because the transmitter has several advantages in implementing the channel emulator. The output impedance of the transmitter is important to reduce the reflected noise, and the current mode driver ideally has an infinite output impedance so that the line impedance is independent of the line signal level. This makes it more feasible to implement the characteristics that change the output swing level on the test device. For example, the output swing level is controlled by the bias current that doesn't affect the output impedance of transmitter. The current mode driver can isolate signal ground to transmitter ground. It can applicate to change the common mode level of output signal without degrading transmitter performance. And the current mode driver has merit on reducing simultaneous switching noise(SSN) that induces data dependency jitter. Thus, the current mode driver has serval advantages in the implementation of the transmitter except for the disadvantage on current.

The logarithm function is implemented with the 5 tap CML drivers that have variable gain. Each stage of logarithm amplifier needs independent gain control method for flexible emulation. Therefore, each current mode driver owns an independent current steering DAC that can be controlled by programable input. The current steering DAC has two control codes; one controls the coefficient per CML transmitter, and the other code calibrates the common gain of total CML transmitter. The common gain is used to control the output swing amplitude with the fixed coefficient of channel emulator.

To ensure reliable operation, the separation from the 2:1 CML MUX has the advantage of implementing the proposed variable delay unit for flexible channel emulation. This structure can place the proposed low-pass filter between the pre-

Table. 5.1. Weight distribution table per stages by characterizing various channels

	I_1 1st stg current	I_2 2nd stg current	I_3 3rd stg current	I_4 4th stg current	I_5 5th stg current
Min	0.59 * I_{total}	0.06 * I_{total}	0.02 * I_{total}	0.02 * I_{total}	0.01 * I_{total}
Max	0.87 * I_{total}	0.22 * I_{total}	0.09 * I_{total}	0.09 * I_{total}	0.04 * I_{total}
Average	0.79 * I_{total}	0.11 * I_{total}	0.04 * I_{total}	0.04 * I_{total}	0.02 * I_{total}

driver and the final driver inside the 3rd to 5th amplifier stages, and it will reduce the quantization noise. Each low-pass filter is designed to have an independently controlled cut off frequency by external program.

The final driver ratio of the 5-stage logarithmic amplifier is determined based on the data of various channels. Based on the 28 kinds of channel data collected from IEEE 802.3 task group, we find the coefficients of the proposed model and compute the gain min and max of each stage. The final driver sizes are determined based on median value from the gathering data. The table 5.1. shows the value that we evaluate.

The dielectric loss emulation block is implemented with programmable low pass filter that connects to the output node of transmitter. The capacitor array is connected to the output termination resistor by using MOS switch circuits, and the 7 bit binary code controls MOS switches. Because the parasitic capacitance of the MOS switch limits bandwidth of the transmitter, the capacitor needs to be minimized, and an alternative way to achieve the wide tuning range is using an external capacitor. The additional low pass filter is also implemented between pre-

drivers and final-drivers from the third to the fifth taps with the same method. It is used to reduce quantization errors caused by the UI-based delays.

5.1.2. Programmable Shift Register and Serializer

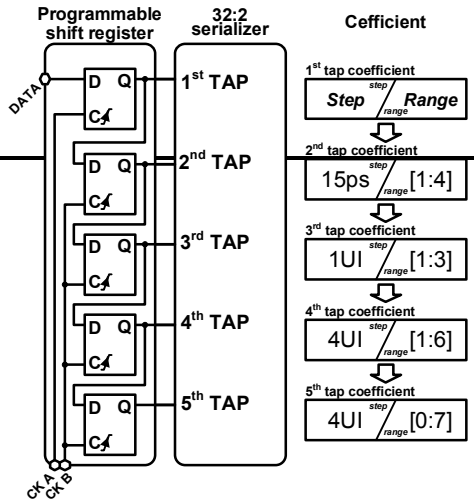


Fig. 5.3 The programmable shift registers and serializer with the variable delay control resolutions.

The programmable shift register and serializer is shown at Fig. 5.4. It receives a parallel data from pattern generator, shifts the parallel data by the clocks, and then serializes the parallel data into serial stream data to the transmitter side. The programmable shift register uses two input clocks, CK A and CK B, with different phases and sequentially feeds the parallel stream data to the five tapes based on these clocks. Each tab of the serializer block consists of a 32:2 ratio serializer configured with CMOS logic, and each tap output is connected to the transmitter of the skin-effect emulator to implement the logarithmic function. The amount of delay controlled by each tap in the programmable shift register is derived by analyzing multiple channels and has the shown values and ranges as in Fig. 5.4. The first tap aligns the parallel data stream by CK A clock domain. The CLK A clock domain is the reference clock domain. The second tap adjusts the amount of delay from one to four in 15ps resolution unit by switching the clock domain from CK A to CK B. The remaining taps shift the data to the delay resolution of the UI unit by using the clock

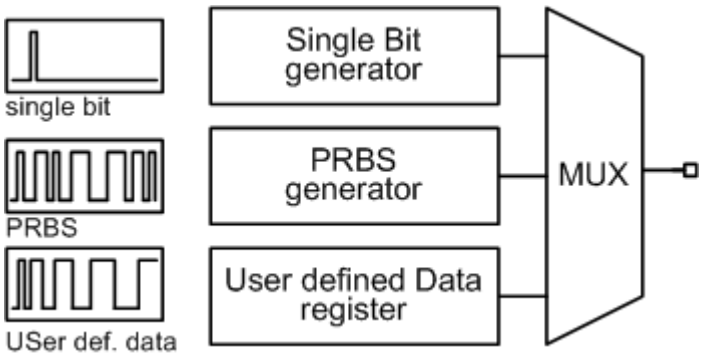


Fig. 5.4 The pattern generator for generating noise source.

domain of CK B. The third tap shifts data from one to three in 1UI units, the fourth tap shifts data from one to six units in 4UI units, the fifth tap delays up to seven in 4UI unit.

5.1.3. Pattern Generator

Fig. 5.4 shows the pattern generator that uses for characterizing channel properties. It generates single bit data with 256bit period, 2^{13}-1 pseudo random bit stream data, and user defined data. The supported patterns are to make patterns such as step response, pseudorandom bit stream (PRBS) data, and random number generator to more easily test the characteristics of the channel. It also has a function to input and output a 256bit stream to support a specific pattern desired by the user. The pattern entered by the user is stored in the pattern generator via I2C. All pattern generators

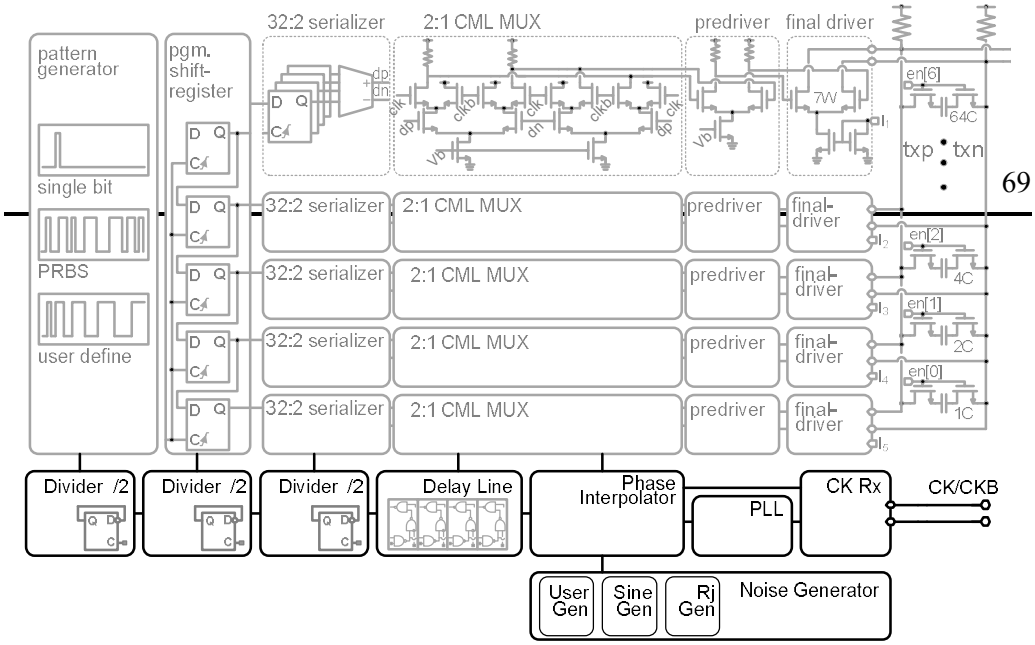


Fig. 5.5 The clock generating unit for the transmitter.

are designed with digital code in Verilog and implemented through synthesis and place and route.

5.1.4. Clock generator

For the operation of the channel emulator, we design a clock generator unit that consists with input clock receiver, all digital phase locked loop, digitally controlled phase interpolator, clock mux, digitally controlled delay line (DCDL), and noise pattern generator. It operates based on an external clock or internally generated clock, and the emulator has been designed to operate up to 8Gbps, and the internal clock has 4GHz period.

The clock generator selects the clock between the PLL output and external clock. Both inputs are intended for operation up to 4 GHz, but for low frequency operation, the PLL is limited to a 3 GHz operating range, so an external input should be used. The phase interpolator is designed to emulate the jitter that can occur in the clock

Table. 5.2.1. Key parameters of the PLL

Kpd [LSBs/rad]	KDCO [Hz/LSB]	Fref [Hz]	N
13	3.9e6	90e6	64
BW [Hz]	PM [`]	Ki	Kp
100e3	80	1/2^10	1/2^1

noise, and tried to generate various types of jitter based on digital code information. The noise pattern generator makes the sinusoid code or random code for generating jitter with the phase interpolator. The DCDL generates CK B domain that uses for 2^{nd} tap of logarithmic amplifier, and the CK A domain is the input clock of DCDL. After DCDL, it provides clocks used for low frequency digital circuit operation through multiple divider.

The PLL is able to support more functions through digital design through cell based design flow rather than full custom. The digitally controlled oscillator (DCO), divider and a time-to-digital converter (TDC) have been custom designed and the loop filter has been digital design. The PLL consists of key parameters such as table 5.1.4. Designed to target a bandwidth of 100KHz, the PLL showed 10ps random jitter in noise simulation using XMODEL, and DCO took the operating range from 3GHz to 5GHz. TDC is implemented using time-domain configurable analog block (TCAB) [30].

The PI is implemented by using TCAB that can have linearity properties of phase

output without complex design, and the design speed is improved by increasing the response speed to input code. PI's digital input controller is implemented to emulate random jitter, sine-wave noise, and user-defined data dependency jitter. This enables emulation of high-speed jitter such as cycle to cycle jitter. Fig. 5.7 shows the simulation result waveform for random noise generated by PI.

The digitally controlled delay line uses a lattice-type digital delay cell which is digitally controlled by a set of thermometer-coded control registers [26][31]. It can create a delay of 15ps with a simple and low-burden. The delay, which consists of digitally controlled delay line (DCDL), is controlled by 4-bit thermometer code with 15ps resolution per a code. The lattice delay line

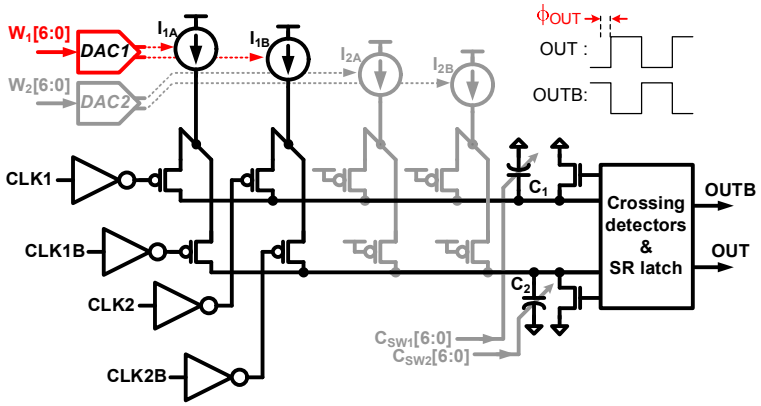


Fig. 5.6 The phase interpolator for generating jitter noise.

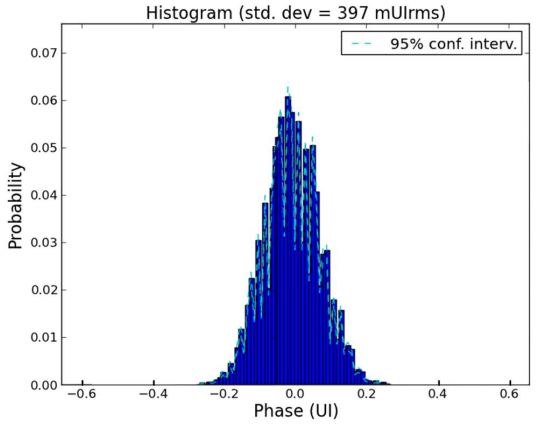
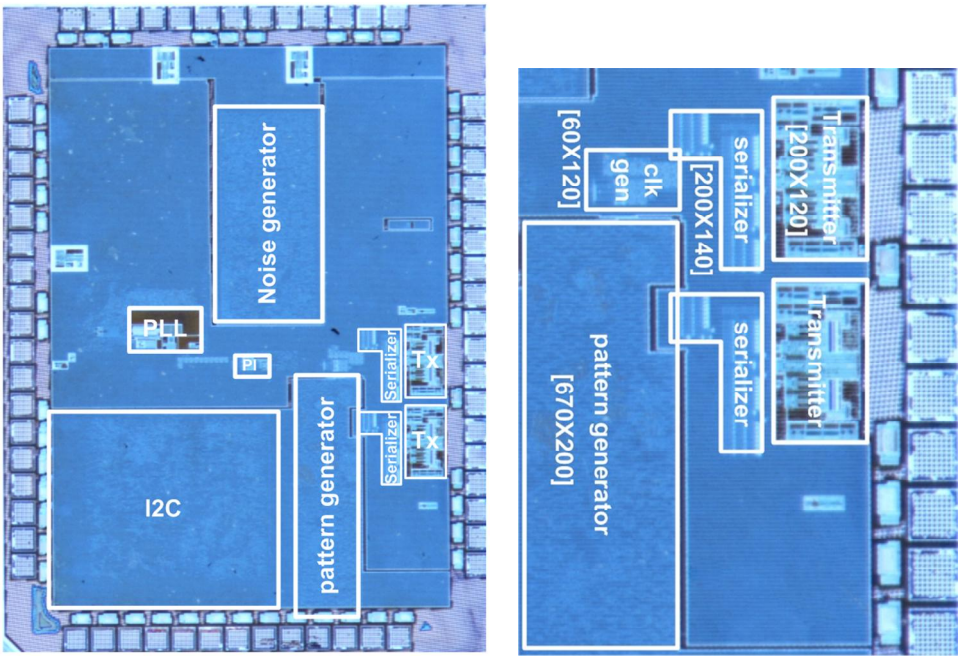


Fig. 5.7 The simulation result of the random noise in the clocking generator.

Chapter 6

Experimental Results

The proposed prototype chip is fabricated based on 65-nm GP process, and a die photograph is shown in Fig. 6.1. Inner 2mm by 3mm die area, the channel emulation transmitter, clock generator, noise generator, pattern generator, and I2C block is implemented with cell-based design flow [27]. The channel emulation transmitter occupies the total active area of 52,000um2 and operates at 1V supply. The target operation frequency is 7Gbps and it consumes 38mW at the 1.4 ~ 7Gbps, of which 7mW is the added power to channel emulation function. Table 6.1.1 summarizes the chip information and performance.



(a) (b)

Fig. 6.1 (a) The full chip photo, and (2) photo of the proposed channel-emulating transmitter.

Table. 6.1.1. Characteristic summary of the prototype IC

Process	CMOS 65 nm GP 1P9M
Supply	1.0 V
Area	52,000um^2
Operation speed	1.4 ~ 7Gbps
Power	38mW @ 7Gbps

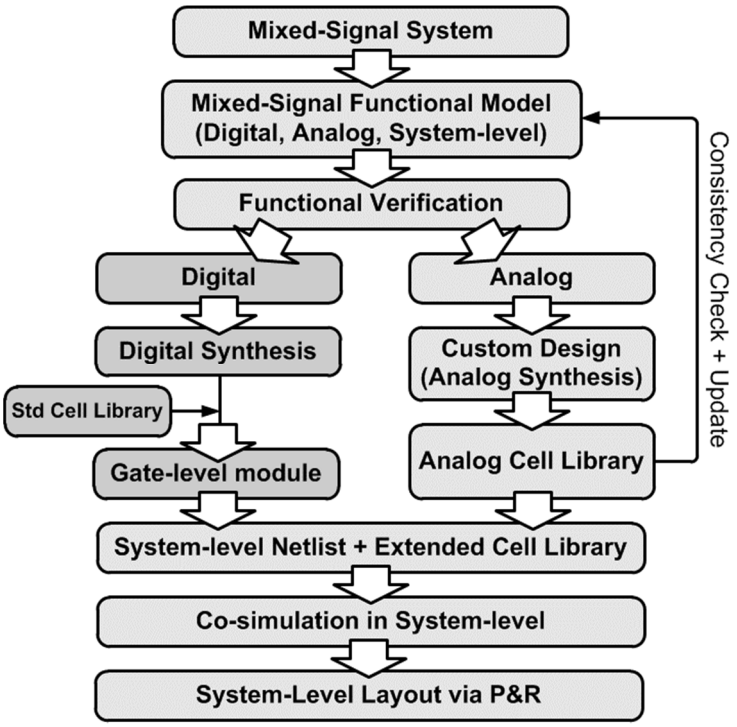


Fig. 6.2 The model-first, cell-based design flow for analog/mixed-signal systems.

This design methodology is highly efficient for implementing full custom design

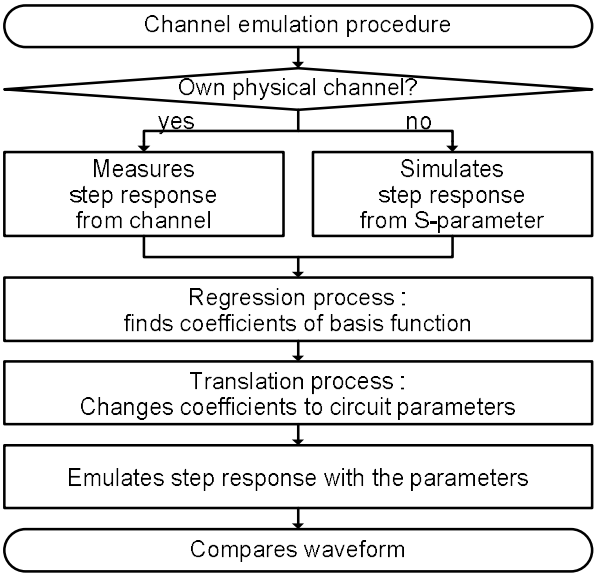


Fig. 6.3 The channel emulation procedure.

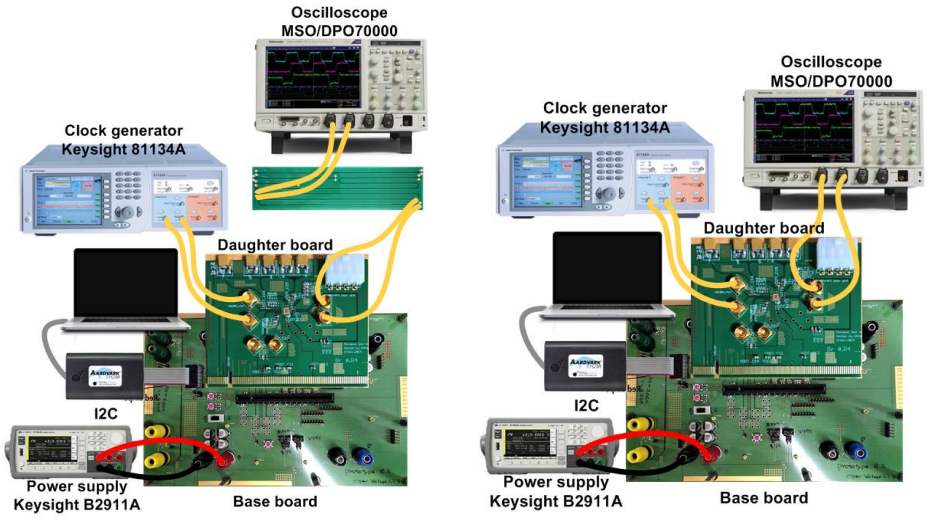
and digital design in a chip, because it shares same concept of a model-first flow. As a digital circuit design flow, the model-first flow proposed in [28] aims to leverage high-level functional models for analog components and improves the design and validation productivity. The full custom design block as transmitter and clock generator blocks are carefully portioned and drawn. Therefore, each custom cell can be laid out in a similar manner to a standard logic cell. As a result, the chip-level layout of analog/mixed-signal systems are utilized the Synopsys IC Compiler and Custom Designer co-design flow for constructing the full chip design.

6.1 Emulation Procedure

The proposed emulation procedure is introduced at Fig. 6.3. The emulator can be applicates both measured data and simulated data of the channel. If the user has the actual channel, then the measured step response can be used for emulation. Even if there is no actual channel, the emulation can be performed if step response can be obtained through simulation. Obtaining the data through simulation has many merits, because it can test multiple cases without additional cost for fabricating the channel. This saves manufacturing costs, and can be used in a variety of cases through channel validation through predictions. Manufacturing PCB board for application test is an extremely complex and expensive work, but its design requires a relatively small amount of resources. This s-parameter channel is used to emulate the channel, and it will reduce iteration to find the optimum channel. The second step is regression analysis by applying the channel information extracted from the first step. It finds optimal coefficients of the basis function (3.5.1) that has the best fit to the step response of the channel data. At this work, the optimization tool box in the MATLAP is used for finding the coefficients. The final step is mapping process in which the coefficients are converted to the circuit parameters such as DAC, delay, and low pass filter codes. At the end of the process, a single bit response, a step response, and a PRBS are output, which will show the channel characteristics.

6.2 Measurement Environments

Fig. 6.4 shows the environment for the measurement. The clock is input from the Keysight 81134A test equipment, and the output waveform is captured by real-time oscilloscope Tektronix MSO/DPO 7000. The Keysight B2911A is used for providing power to the prototype chips and tester board. All the function on the chip is controlled by I2C with the python codes.



(a) (b)

Fig. 6.4 Experiment setup to test the channel-emulating transmitter: (a) test environment for the actual channel and (b) for the emulation transmitter.

The project mounts the channel emulation transmitter chips to the daughter card without using the package. In order to reduce the inductance of the bond wire, two wires are connected to the high-speed signal lines between chip PAD to PCB landing PAD. The daughter board is connected to the base board on the PCI socket for

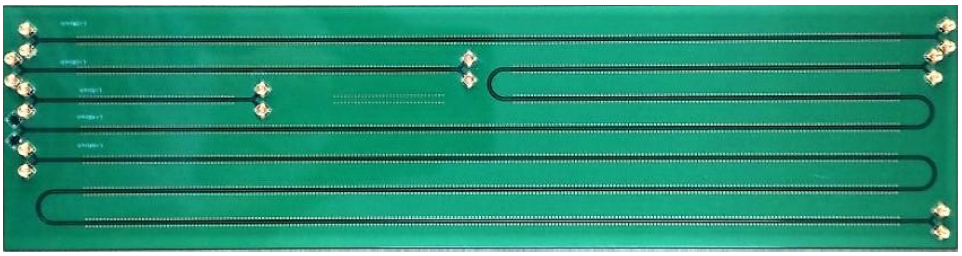


Fig. 6.5 The prototype FR4 board that consists of 10~40 inch channels.

providing power and control signals that operates at lower speed range. The I2C is an example of the lower speed signal. This configuration is advantageous in that the daughter board can focus on the critical signal, like high-frequency I/O. Because the low-frequency signal input connector and power connector is implemented at the base board, and these can be supplied via a PCI connector.

The emulation test proceeds as shown in the Fig. 6.4. In case of the actual channel, a channel connection on the test configured to obtain a step response with oscilloscope. The measurement is performed in a state where all the BIST functions connected to the transmitter are disabled. The emulation parameters are obtained using the waveforms scoped through the process, and the corresponding parameter values are applied to the BIST through I2C. The proposed emulation transmitter then outputs the step response using the function of the channel replica and can compare the difference with the waveform using the actual channel.

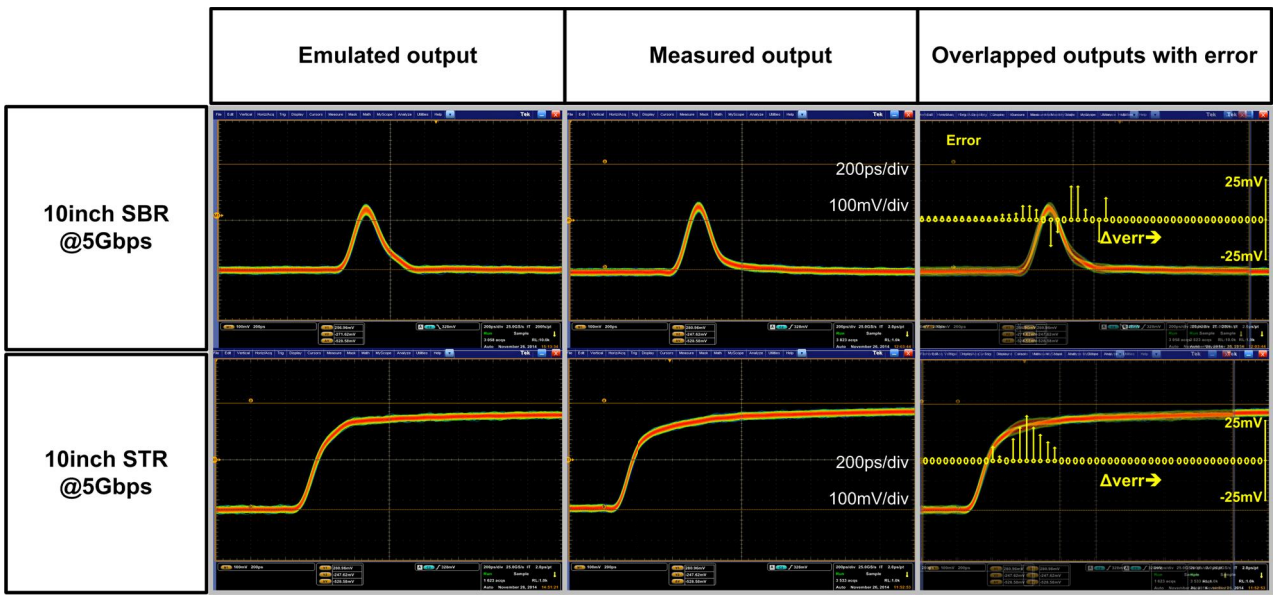


Fig. 6.6 The comparison data between emulated result and 10-inch measured result.

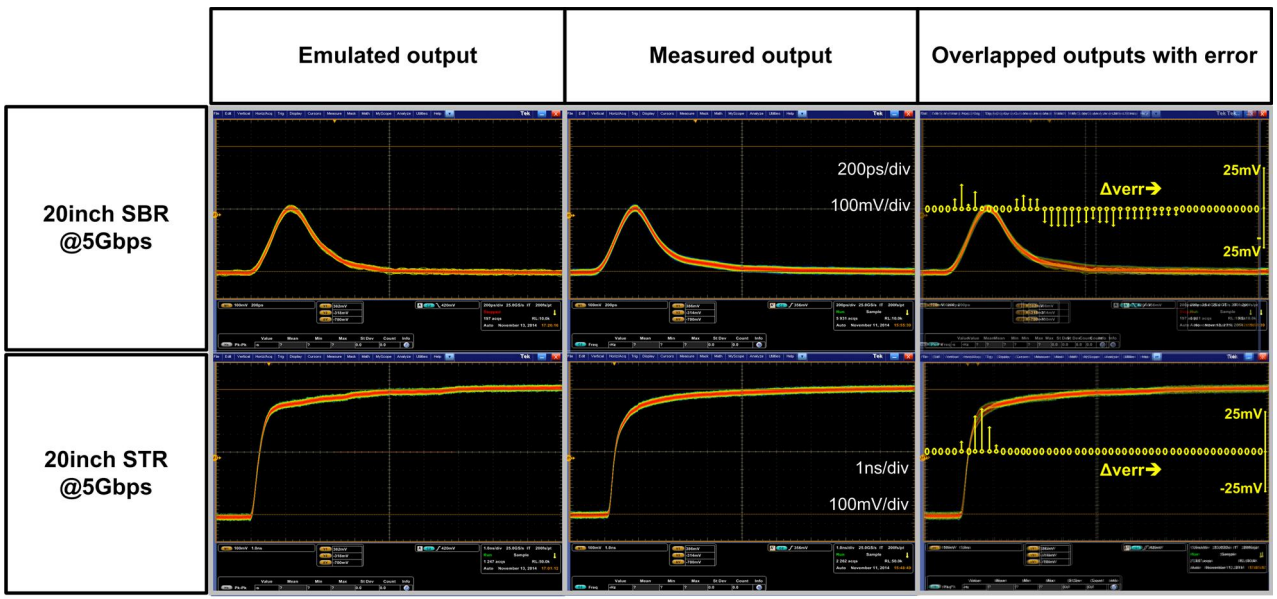


Fig. 6.7 The comparison data between emulated result and 20-inch measured result.

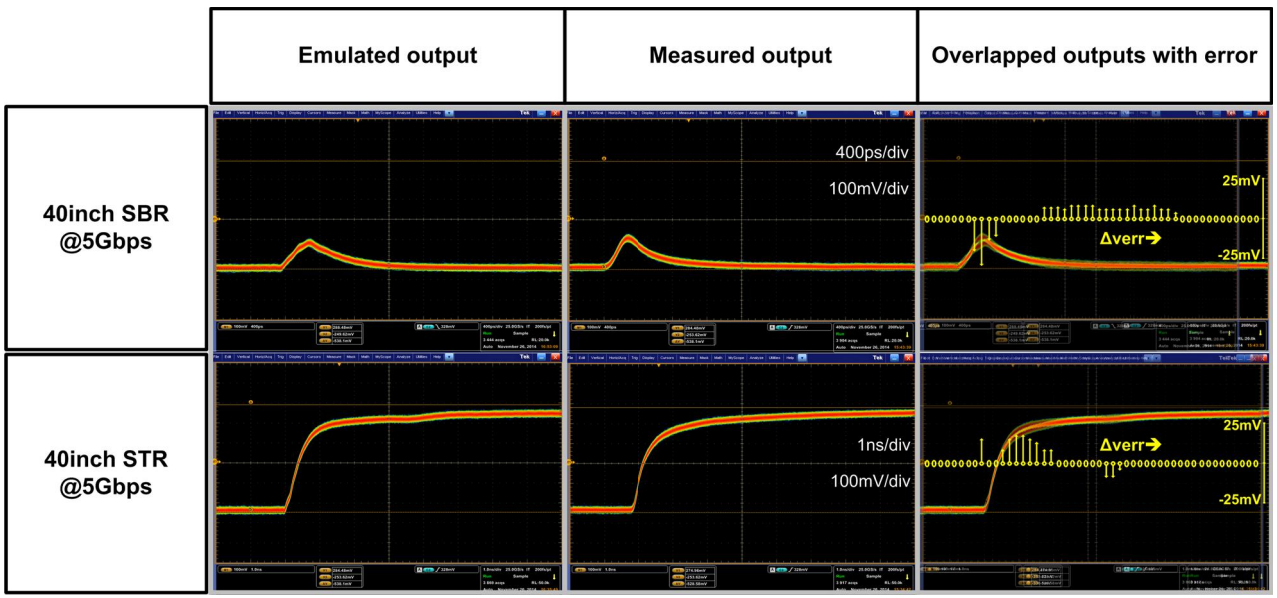


Fig. 6.8 The comparison data between emulated result and 40-inch measured result.

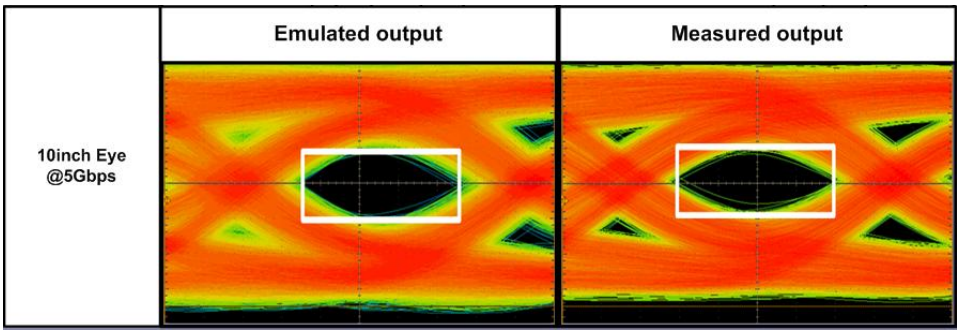


Fig. 6.9 The eye diagram of 10inch channel at 5Gbps

6.3 Emulation with Actual Channels

To validate the emulation transmitter, FR4 channels are fabricated in multiple length (10, 20, 40 inches) as Fig. 6.5. After measuring the step response using these channels, each emulation parameters are obtained and applied to the BIST function to obtain the step response again. And the step response of each channel is measured and emulated in Fig. 6.6 to Fig. 6.8. The first column is measured from emulator output, and the second is measured from actual channel. The last column overlaps with the previous two columns, and plots the magnified difference between the signal from the emulator and the real channel.

For step response comparison of the 10-inch channel, the emulated signal slope is steeper than the actual measurement due to the fitting error in the 3rd tap coefficient. This error factor is also the same in the single bit response result. The source of this

error is considered to be offset in the process of switching parameters from the basis equation to the circuit. The emulated waveform error is less than 25mV (6%) at 400mV total swing voltage. And this error keeps a similar value when the channel length is increased. In the result of 20-inch and 40-inch case, the fitting results are generally matched between emulation results and actual channel results except for the similar errors found in the result of 10-inch.

The FR4 material has a higher dielectric loss than the skin-effect, so the dielectric loss is dominant loss in the short channel length. But the skin-effect is observed more at the long length channel, therefore, the signal is affected by ISI for a long-time period as the measured waveform. The emulated transmitter also well replicates the long-term ISI. The eye diagram is shown at Fig. 6.9, which operates at 5Gbps in the 10inch channel and emulated channel. Comparing the measured results between the physical channel and the emulated output, we can confirm the proposed work.

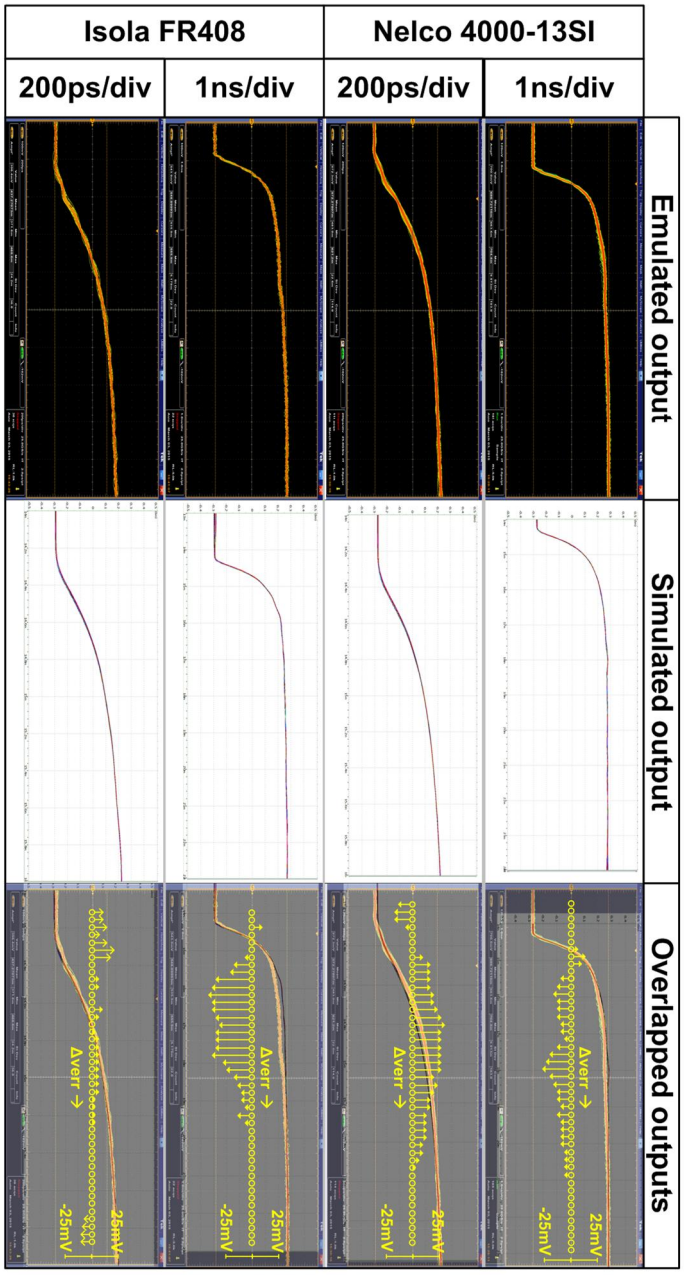


Fig. 6.10 The comparison data between emulated result and simulated result with low dielectric loss channel.

6.4 Simulation with S-Parameters

Fig. 6.10 shows the emulated test results performed by using s-parameter. It emulates s-parameter channel that consists of FR408 and Nelco 4000-13SI. Both material is called advanced FR4, which has much lower loss tangent that decides the dielectric loss. But it has almost the same attenuation to the skin-effects.

The error factor of the third tap is still founded in these results. The error components are also found except the error factor of the third tap, and the factors that can be considered as the cause are the components that are not considered in the simulation. For example, a loss in a cable on a measurement is not considered in the simulation. Especially, it is estimated that the connectors that cause impedance mismatch and the difference between actual and simulation of transmitter are the main components of error in the results. Therefore, the error is little bit larger than FR4 measured data. Despite these errors, a similar signal slope is formed between the emulation waveform and simulated waveform, with an absolute voltage error of about 25mV.

The channel emulation can use s-parameter when physical channels are not available. Manufacturing PCB board for application test is an extremely complex and expensive work, but design itself requires relatively small amount of resources. The s-parameter channel can be used as an emulated channel, reducing dual work in finding the optimum channel.

Chapter 7

Conclusion

This paper describes a transmitter that can emulate a wide variety of frequency-dependent loss characteristics of high-speed DRAM channels, with an aim to facilitate an automated test procedure for DRAM interface that does not require physical reconfiguration of channels. Specifically, the proposed transmitter can generate the waveform of an NRZ data stream that experienced the adjustable amounts of skin-effect loss and dielectric loss of electrical channels.

In order to emulate various channels, the work proposed a basis function consisting of exponential and logarithmic functions. The emulation can be done by using the inverse of the equalization transfer function used to compensate for the loss of the channel. But the previous transfer functions have a problem of modeling efficiency. Especially, the replication of the skin-effect through the logarithmic function has a higher degree of emulation than the previous studies. The proposed function is able to confirm the consistency through a number of channel fitting

results.

The emulation architecture is implemented using a pseudo logarithmic amplifier and a low-pass filter. The pseudo logarithmic amplifier is modified to control both timing and gain parameters in order to increase the degree of freedom of emulation.

For the implementation, the pseudo logarithmic amplifier is implemented by using the CML driver, and the low-pass filter is implemented using a resistor and capacitor, capacitor is varied to MOS switch. Digitally controlled delay line and shift register are used for the timing control, and individual DAC is used for CML bias control for the gain control. And the pattern generator, I2C, and clock generator are implemented to support the channel emulation test.

The prototype chip fabricated in 65um CMOS consumes 52,000um2 and operates over 1.4~7Gbps while dissipating 38mW at 7Gbps. It is demonstrated that the implemented transmitter can emulate 10~40”-long microstrip lines on FR4 material. The single bit response and step response waveform are compared between emulation and actual channels. Based on the result, the maximum error is less than 6.25%, and the error is estimated as the offset of the 3rd stage gain that occurred in the process of switching parameters. In the simulation-based comparison, it shows 12.5% error between waveforms, due to mismatch occurred in the connector not considered in the S-parameter simulation. Nevertheless, we could confirm the high similarity between the two waveforms.

Although the proposed circuit can emulate similar response of real channels with a minimum of additional circuitry, it can still be a burden to use as a BIST. Therefore, it is necessary to improve performance and chip area through continuous improvement in the future. The proposed work is expected to solve the channel test

environment issue in the high seed link with a minimal additional cost.

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초 록

이 논문에서는 다양한 환경에도 구동되는 DRAM 의 송수신 장치의 특성을 측정할 수 있는 채널 모사장치를 논의합니다. 이 모사 장치는 기존의 자동화 된 ATE 에 적용을 통해 물리적 환경 변경이 없는 상황에서도 다양한 전송 신호 채널을 기반으로 DRAM 의 송수신기를 측정 할 수 있는 장점을 가집니다. 특히 제안된 송신 장치는 표면 효과에 의한 손실과 전기적 채널의 유전 손실을 모사하며, 그 손실양을 조절하여 NRZ 데이터 스트림의 파형을 생성 할 수 있다.

채널의 손실을 모사하기 위해 유전률 손실에 대해서는 지수함수를 사용하였으며, 표면 효과로 인한 손실은 대수함수를 이용해 대신하였다. 이를 구현하기 위해서는 고속 고해상도의 디지털-아날로그 변환기를 구현하여 하드웨어의 비용을 절감하였으며, 대수함수의 경우 의사 대수 함수 증폭기를 이용하였다. 이를 통해 가변 이득 및 대역폭을 갖춘 광대역 증폭기. 65um CMOS 로 제작 된 프로토 타입 칩을 제작, 이는 52,000um2 의 면적에 1.4 ~ 7Gbps 이상에서 동작하며, 7Gbps 동작 속도에서 38mW 를 소모합니다. 구현 된 송신기는 FR4 소재의 10 ~ 40 "길이의 마이크로 스트립 라인을 이용하여 측정하였을 때, 계단파형 응답에서 6.25%보다 낮은 오차율을 보였으며, S-parameter 기반의 예측 기반 모사의 경우 12.5%의 오차를 보여 그 사용에 가능성을 확인할 수 있었습니다.

주요어 : 채널 모사 송신장치, 자율 측정 장치, 표면효과, 유전율 손실, 혼성신호 직접회로

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