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Ph.D. DISSERTATION

Transparent, Flexible, and Inkjet-
Printed Thin-Film Transistors
Based on Organic and Nano
Materials

유기 및 나노 재료 기반
투명하고 유연하며 잉크젯 프린팅 공정으로
제작된 박막 트랜지스터에 관한 연구

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COMPUTER SCIENCE
COLLEGE OF ENGINEERING
SEOUL NATIONAL UNIVERSITY

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Transparent, Flexible, and Inkjet- Printed Thin-Film Transistors Based on Organic and Nano Materials

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Abstract

Transparent, Flexible, and Inkjet- Printed Thin-Film Transistors Based on Organic and Nano Materials

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Recently, transparent and flexible thin-film transistors (TFTs) have attracted much attention in the hope that they will underpin the next-generation electronics as there are a variety of applications for transparent thin-film electronics, such as bendable, rollable, foldable, and wearable devices. Meanwhile, inkjet-printing enables low-cost, low-temperature, and large-area fabrication with a simple process. Thus, various solution-processed/inkjet-printed metal oxide layers have been employed for transparent electronic applications because of their high optical transparency and high carrier mobilities and concentrations. However, several issues remain to be addressed to fully utilize flexible metal oxide-based TFTs fabricated via inkjet-

printing, such as the high annealing temperature required, the presence of organic impurities, and film rigidity. To overcome these issues, transparent conducting polymers and intrinsically flexible semiconductor materials should instead be adopted for transparent and flexible device applications.

In this dissertation, we demonstrated the fabrication of inkjet-printed transparent TFTs using poly(3,4-ethylenedioxythiophene):polystyrenesulfonate as transparent electrodes and three types of semiconductor active layers, namely 6,13-bis(triisopropylsilylethynyl)pentacene as an organic semiconductor, single-walled carbon nanotubes (SWCNTs), and molybdenum disulfide (MoS_2). All layers are intrinsically flexible and were formed using a printing process that is compatible with flexible platforms. In addition, we have proposed a facile interface engineering method to improve the electrical performance of transparent organic TFTs (OTFTs) and systematically analyzed the optical characteristics of transparent TFTs based on nano-materials. Through studying the implementation and characterization of transparent and flexible TFTs based on printing techniques using various materials, we propose guidelines for each application field based on the advantages and disadvantages of each material. The results are expected to have a high impact in both the academic and industrial domains.

For printed OTFTs, surface energy matching of the source/drain (S/D) electrodes and the gate dielectric is critical, because unless their surface energies are matched, printing organic semiconductors results in a high contact resistance as well as unfavorable crystal structures of the π -conjugated semiconductors during drying of the solvents near the S/D electrodes, yielding poor electrical performance. To obtain an improved crystal structure of the organic semiconductors, we propose an effective, one-step interface engineering method that can be simultaneously

conducted on transparent organic electrodes and the gate dielectric layer for all-inkjet-printed, all-organic transparent transistors and inverters on flexible substrates. The proposed inkjet-printed organo-compatible polystyrene interlayer delivers better charge injection properties and semiconductor layer crystallinity, while minimizing defect sites on the gate dielectric layer without degrading the transmittance.

For transparent TFTs to be practically used, there should be little change in their operation under illumination. Because common semiconducting materials including organic semiconductors are well known to be sensitive to light, a stable active layer for transparent TFTs under illumination is needed. SWCNT TFTs exhibit an unusual photoresponse because SWCNTs have a high exciton binding energy owing to the enhanced Coulomb interactions in one-dimensional materials. Unlike TFTs are fabricated using other semiconducting materials, SWCNT TFTs exhibit no significant change in electrical properties under low-power light used in practical life, although the current decreases under high-power laser illumination. Utilizing these attributes, the applicability of transparent and flexible SWCNT TFTs to real-life transparent flexible device applications will be discussed.

Unlike SWCNTs, MoS₂ exhibits high photoresponsivity. This characteristic of MoS₂ enables its application as a photosensor, which is an essential element in many proposed wearable devices. However, currently MoS₂ TFTs have been applied in electronics using conventional inorganic electrodes and dielectrics implemented using conventional photolithography or transfer processes that are not compatible with large-area and flexible device applications. To fully exploit the advantages of two-dimensional (2D) MoS₂ in practical applications, novel strategies for realizing flexible and transparent 2D electronics using low-temperature, large-area, and low-cost processes should be developed. Here, fully-printed transparent chemical vapor

deposition-grown monolayer MoS₂ phototransistors fabricated on flexible polymer substrates will be presented. All the electronic components such as the dielectric and the electrodes were directly patterned with mechanically tolerable organic materials using inkjet-printing onto transferred monolayer MoS₂. By integrating these soft organic components with ultra-thin MoS₂, the fully printed MoS₂ phototransistors exhibited excellent transparency and mechanically stable operation.

Keywords: *transparent electronics, flexible electronics, organic thin-film transistors, single-walled carbon nanotube thin-film transistors, MoS₂ thin-film transistors, inkjet printing*

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Chapter 1

Introduction

1.1. Motivation

Since they were first proposed in 1997 [1], transparent electronics have been extensively studied owing to their applicability in various transparent thin-film electronic devices, such as transparent displays [2-4], sensors [5-7], memory devices [8], photodetectors [9], solar cells [10], and smart contact lenses [11]. In particular, the transparent thin-film transistor (TFT) is a key technology used in transparent electronic devices, because it acts as a bridge between passive electrical and active electronic devices. As transparent electronics technology is further improved, the demand for thinner and lighter devices on flexible platforms using low-cost, low-temperature, and simple fabrication processes has increased to enable bendable, rollable, foldable, and wearable device applications. Thus, research on transparent and flexible TFTs fabricated using solution process has attracted significant attention in recent years.

Among the conventional TFT fabrication processes, although vacuum

deposition and photolithography have been widely used to deposit layers and produce the electrode or gate dielectric patterns, the need for high vacuum systems, various shadow masks, and photo-patterning using photoresist (PR) have posed as obstacles in realizing low-cost, large-area electronic applications developed via a simple process. Moreover, these conventional photolithography processes that use multiple photomasks, toxic gases, and organic solvents are considerably complex, time-consuming, and not environmentally friendly, resulting in high-cost products. Therefore, solution processes, especially the direct-printing process is regarded as one of the most promising candidates to substitute the conventional vacuum process owing to its advantages of low-temperature, considerably low-cost, maskless implementation, and easy process capabilities compared with the conventional vacuum deposition fabrication methods; these advantages are important in realizing flexible, low-cost, large-area electronic devices. In addition, the direct-printing process is also compatible with flexible platforms such as plastic, paper, or steel substrates. Various printing technologies, including inkjet printing, screen printing, offset printing, gravure printing, and flexography have been widely used in the printed electronics industry, and eventually, the roll-to-roll process is suitable for high-throughput systems.

As shown in Figure 1.1, among various kinds of large-scale solution printing methods, the inkjet printing technology is considerably simpler in application than conventional photolithography. In addition, inkjet printing avoids wastage of material or contamination because of mask contact or PR deposition/strip [12-14]. Furthermore, the drop-on-demand inkjet-printing method allows easy implementation of arbitrary patterns with various thicknesses without using masks; this is depicted in Figure 1.2. Because of these significant advantages, the inkjet-

printing process is widely used in the fabrication of TFTs to deposit electrodes or active layers. Consequently, simple, low-cost devices on flexible substrates can be realized using it.

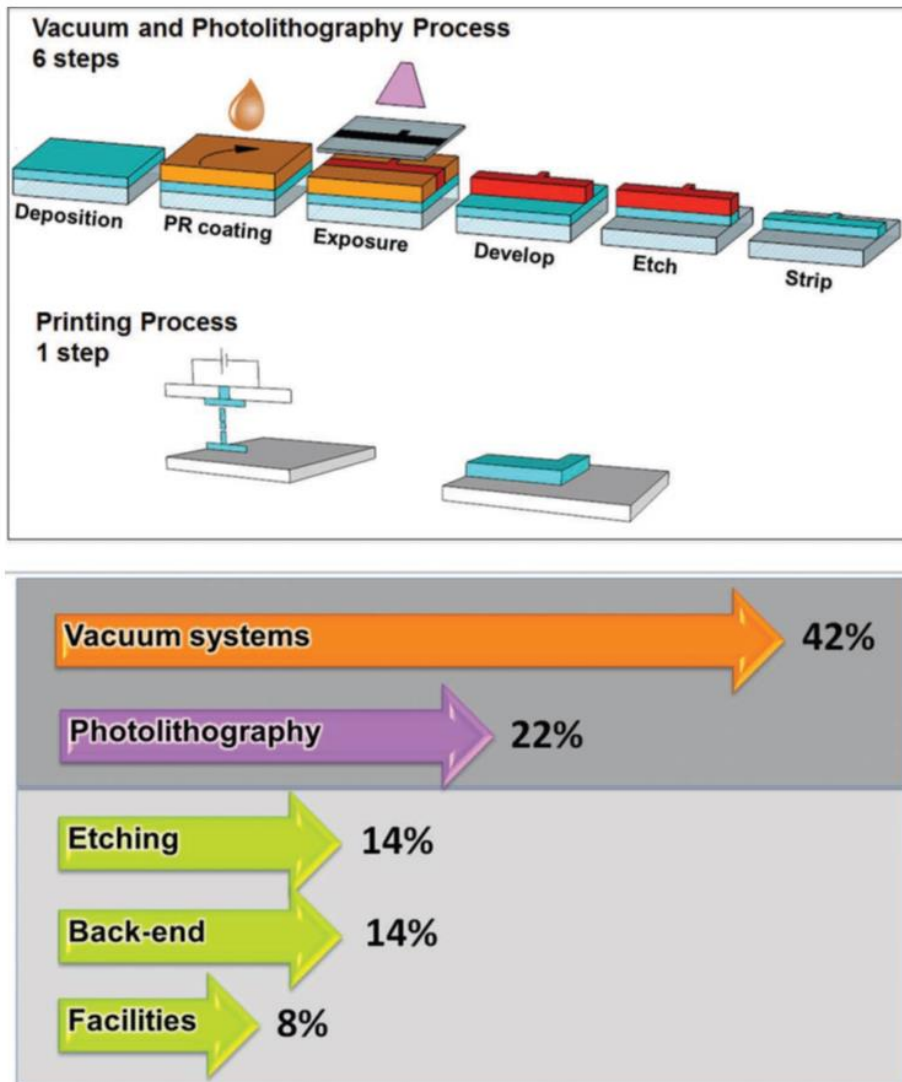


Figure 1.1 | Comparison between the printing and conventional microelectronic technology processes as well as the normalized costs associated with each process [15].

Number of
printing passes

1
2
3
4
5
1cm

been used only for either gate dielectric or bottom electrodes. Furthermore, those methods require a sufficient coupling reaction time under inert conditions, as well as complicated procedures. Therefore, a more acceptable surface treatment is required for high-speed and performance inkjet-printed OTFTs. Conventional solution-processed polystyrene (PS) thin films can provide sufficient hydrophobic and smooth surfaces to induce ordered crystals of organic semiconductors, and prevent water absorption into the gate dielectric layer.^[34,35] However, the PS layers physisorbed on substrates tend to swell and delaminate easily when they are sequentially exposed to organic solvent. In contrast, end-functionalized PS could be chemisorbed to UV/O₃-treated substrates, providing physicochemical stability to SiO₂ or Al₂O₃ dielectrics, by substituting a silane-coupling moiety on either end of PS.^[36] On the PS-chemisorbed organic dielectrics, the solution-processed triethylsilylethynyl thienothiophene and poly (3-hexylthiophene-2,5-diyl) films showed good electrical properties in top-contact OTFTs.^[36] In this paper, we investigated bottom-contact OTFTs with inkjet-printed components and revealed that one-step chemical coupling of dimethylchlorosilane-terminated PS (PS-(H₃)₂Cl) on both gate dielectric and bottom S/D electrodes significantly enhanced the characteristics at the interface between semiconductor and those layers. High-performance inkjet-printed *p*-type organic inverters have been demonstrated on a flexible polymer substrate, using an interdigitated structure for the drive TFT and the chemical coupling method. By introducing end-functionalized PS, the fabrication of OTFTs has been improved by one order.

Figure 1.2 | “SNU”-letter shaped PEDOT:PSS patterns with different thicknesses formed using the drop-on-demand inkjet-printing process with different number of printing passes (1 to 5) [16].

1.2. Organization of This Dissertation

In this dissertation, we study transparent and flexible TFTs fabricated using inkjet printing with poly(3,4-ethylenedioxythiophene):polystyrenesulfonate (PEDOT:PSS) for the gate and source/drain (S/D) electrodes, cross-linked poly(4-vinylphenol) (PVP) as the gate dielectric layer, and three types of semiconductor materials as active layers, namely 6,13-bis(triisopropylsilylethynyl)pentacene (TIPS pentacene) as an organic semiconductor, single-walled carbon nanotubes (SWCNTs), and molybdenum disulfide (MoS_2) (see Figure 1.3). In particular, the use and applicability of these three types of semiconducting materials for different applications was studied based on the corresponding characteristics of each semiconductor material.

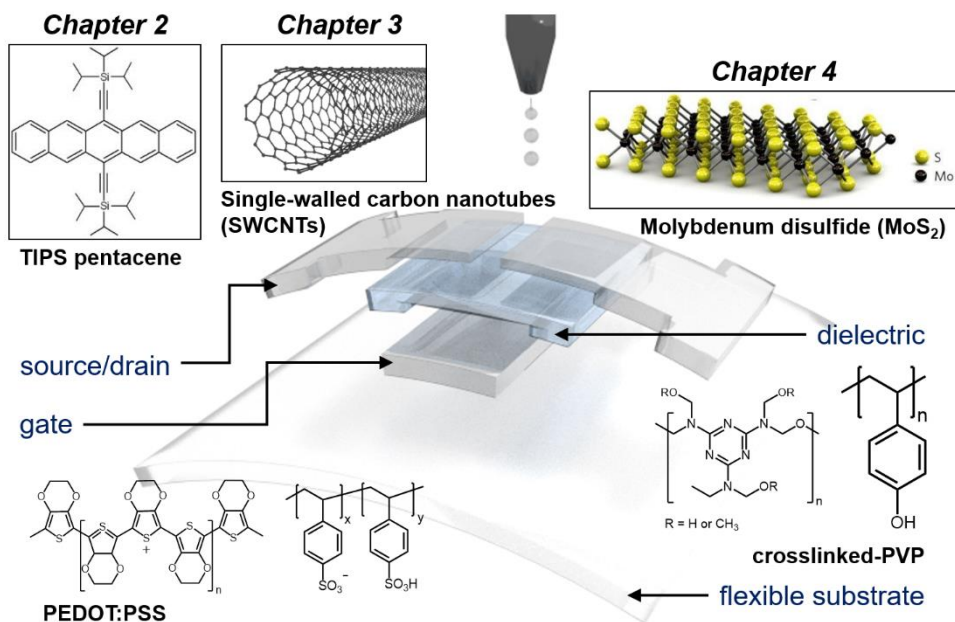


Figure 1.3 | Overview of this dissertation. Transparent and flexible TFTs with three types of semiconducting materials will be fabricated and fully analyzed; the details will be presented in each chapter.

First, in order to enhance the electrical characteristics of transparent organic TFTs (OTFTs), a one-step, effective interface engineering method that can be simultaneously conducted on transparent organic electrodes and gate dielectric layers for all-inkjet-printed, all-organic transparent transistors and inverters on a flexible substrate is performed, which is discussed here. The proposed inkjet-printed organo-compatible polystyrene interlayer yields better charge injection properties and semiconductor layer crystallinity. In addition, it minimizes defect sites on the gate dielectric layer without degrading its transmittance.

Furthermore, because common semiconductor materials including organic semiconductors are photosensitive, it is difficult to use them in several practical

applications without the inclusion of additional structures, such as an encapsulation layer. Therefore, it is essential to use semiconductor materials whose characteristics are not affected by light, i.e., they are not photosensitive in such cases. In contrast, for photosensor devices, which are essential elements in wearable devices, semiconductor materials that exhibit high photoresponsivity are needed. Considering these, in this study, we systematically analyzed the optical properties of transparent, flexible TFTs based on two types of nanomaterials with opposite photoresponse, namely SWCNTs and MoS₂. In particular, because SWCNTs are insensitive to light whereas MoS₂ is highly sensitive to light, SWCNT TFTs and MoS₂ TFTs can be utilized for transparent display/circuit applications and transparent phototransistors/photosensors, respectively.

We analyzed the unusual photoresponse of SWCNT TFTs in our study. Unlike TFTs including other semiconducting materials, in SWCNT TFTs, a decrease in current is observed under high-power laser illumination. However, they do not exhibit any significant change in their electrical properties under low-power light commonly used in daily life. Based on these attributes, the applicability of transparent, flexible SWCNT TFTs for real-life transparent flexible devices will be discussed. Finally, fully-printed transparent chemical vapor deposition (CVD)-grown monolayer MoS₂ phototransistor arrays fabricated on flexible polymer substrates will be presented. All the electronic components, such as dielectrics and electrodes, were directly patterned with mechanically tolerant organic materials using inkjet-printing technology onto a transferred monolayer of MoS₂. By integrating these soft organic components with ultra-thin MoS₂, the fabricated fully printed MoS₂ phototransistors exhibited excellent transparency and mechanically stable operation. Moreover, the responsivity of the fabricated phototransistors

showed good linearity for laser power density, which is an important characteristic for photosensor applications.

This dissertation consists of five chapters, including an Introduction and Conclusion.

Chapter 1 briefly introduces the necessity and importance of transparent flexible TFTs fabricated using inkjet printing techniques, which serves as the motivation for this dissertation. In addition, the materials and equipment used for TFT fabrication are presented.

Chapter 2 describes a one-step interface engineering method, which is simultaneously conducted on transparent PEDOT:PSS electrodes and gate dielectric layers for all-inkjet-printed transparent TFTs and inverters on a flexible substrate.

Chapter 3 discusses the transparent and flexible SWCNT TFTs that are light stable, and can be applied to real-life transparent flexible device applications. In addition, the unusual photoresponse of the SWCNT TFTs under both low-power light and high-power laser illumination is explained.

Chapter 4 describes the fully-printed transparent CVD-grown MoS₂ phototransistors fabricated on flexible polymer substrates, which can be applied to low-cost wearable device applications.

Chapter 5 summarizes the transparent, flexible, and inkjet-printed TFTs based on the organic semiconductor, SWCNTs, and MoS₂. In addition, it highlights the significance of this study and also discusses directions for future research.

1.3. Materials & Equipment

In this chapter, we briefly explain the materials and inkjet-printing systems used for the fabrication of transparent and flexible TFTs.

1.3.1. Transparent Conducting Polymers

Transparent conductive electrodes (TCEs) are essential to realize transparent electronic devices. In this regard, soluble organic-, oxide-, and carbon-based materials have gained significant attention as potential candidates [17-19]. Various solution-processed metal oxide layers are employed for these electronic applications because of their high optical transparency as well as high carrier mobilities and concentrations. However, several obstacles to realizing flexible metal oxide-based TFTs still exist, including high-temperature annealing, the presence of organic impurities, and film rigidity, among others [3, 18, 20, 21]. Flexible carbon nanotubes and graphene have been extensively utilized for soft electronics applications as complementary carbon-based materials [19, 22, 23]. However, the uniformity and patterning capability of solution-processed carbon-based layers needs to be further improved to realize practical soft electronic devices. Thus, in recent times, solution-processed conducting polymers have been widely studied as materials for transparent electrodes in low temperature, simple, large-area, and low-cost printed electronics [24-26]. PEDOT:PSS (Figure 1.4a) is one of the most promising conducting polymers for transparent electrodes having high optical transparency, conductivity, and thermal stability [17, 24, 27]. In particular, as shown in Figure 1.2 [16], PEDOT:PSS electrodes can be easily fabricated using an inkjet-printing method,

without the need for any other dedicated procedures including photolithography [24, 28, 29]. Furthermore, the fluorosurfactant Zonyl FS-300 (Figure 1.4b) is added to PEDOT:PSS ink to improve the conductivity of the film, film's ability to withstand deformation, and render it suitable for multi-layer deposition on various substrates [17].

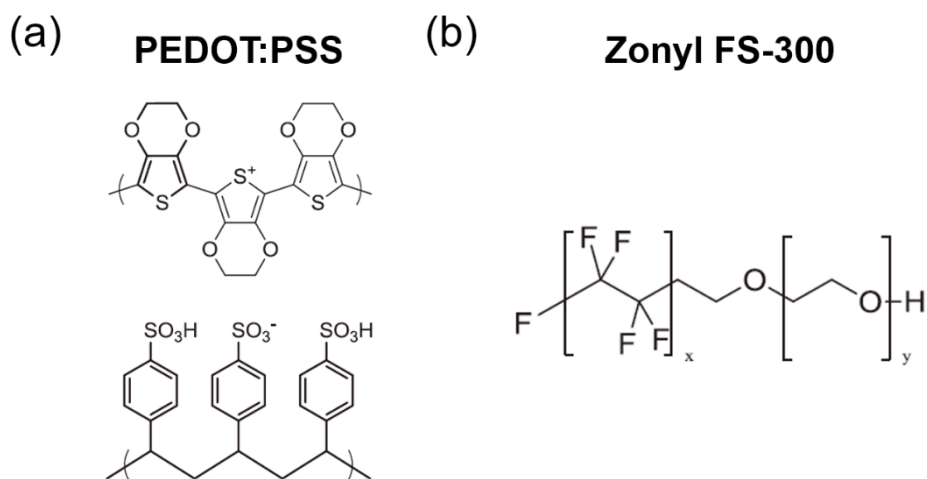


Figure 1.4 | Chemical structures of (a) PEDOT:PSS and (b) Zonyl FS-300 [17].

1.3.2. Transparent Insulators

In general, most insulating materials are transparent owing to their high band-gap. Furthermore, high-quality gate dielectrics in TFTs should guarantee good insulating performance, low undesirable impurities, small number of trapping sites, and smooth surface roughness. Considering this, organic gate dielectric materials are the most promising candidates for printed electronics applications. The most commonly used

soluble organic dielectric materials include PVP, polyvinyl alcohol, poly(methyl methacrylate), and polystyrene (PS), because these require relatively low curing temperatures of under 200 °C, which makes them compatible with flexible substrates; in addition, they exhibit good electrical insulation performance. In particular, PVP is used as a gate dielectric with poly(melamine-*co*-formaldehyde) methylated (PMFM) as a cross-linking agent (Figure 1.5a, b). Moreover, curing conditions critically affect the surface of the gate dielectric layers, thus determining their interfacial properties. Therefore, in order to obtain a high-performance printed gate dielectric layer, the layer should be coffee-ring-free at the edge of the printed area and have good surface roughness without pin holes, which also determine the leakage characteristics [13].

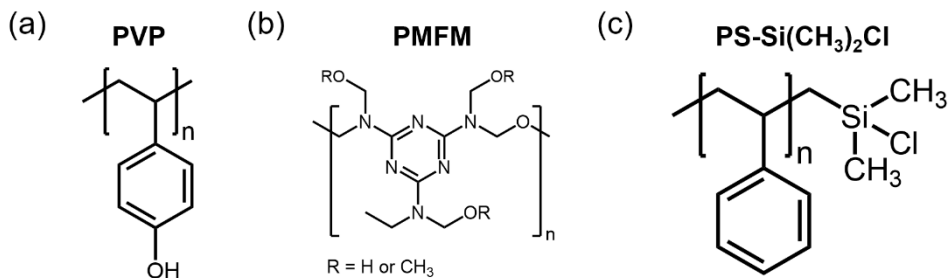


Figure 1.5 | Chemical structures of (a) PVP, (b) PMFM, and (c) dimethylchlorosilane-terminated PS (PS-Si(CH₃)₂Cl).

The surface energy matching of S/D electrodes and gate dielectrics is critical, especially in the case of bottom-gate and bottom-contact TFTs, because dewetting and swelling during upper layer deposition can cause severe degradation of the electrical performance of the TFTs. In Chapter 2, an interface engineering method with chlorosilane-end-terminated PS (Figure 1.5c) grafted on both the transparent

conducting polymer electrodes and organic dielectric will be discussed in detail.

1.3.3. Transparent Semiconductors

1.3.3.1. TIPS Pentacene

In the past few decades, the electrical performances of organic semiconducting materials based on π -conjugated molecules have been improved significantly. Consequently, they have been adopted in e-paper and other electronic display applications. Pentacene is one such organic semiconducting material, which is a promising candidate owing to its high mobility of up to $5 \text{ cm}^2/\text{V}\cdot\text{s}$ [30]. However, pentacene films can only be developed using the high-cost vacuum deposition process because of its insolubility in organic solvents. Therefore, pentacene cannot be used for inkjet printing applications. Considering this, soluble, polymeric organic semiconductors such as P3HT, F8T2, F8BT, and PQT12 conjugated polymers have attracted significant attention as substitutes for pentacene. However, the electrical performances of these polymeric organic semiconductors, especially carrier mobility, is poor, and therefore, they are not suitable for electronic applications. Thus, TIPS pentacene has been developed as a high-performance soluble organic semiconductor [31]. In TIPS pentacene, two bulky functionalized groups are permanently attached to the pentacene backbone that allow the molecules to dissolve in organic solvents. Moreover, the attached functionalized groups also induce strong π -stacking of molecules to enhance intermolecular orbital overlap resulting in high mobility of $> 1 \text{ cm}^2/\text{V}\cdot\text{s}$ (see Figure 1.6). Furthermore, TIPS pentacene is compatible with flexible substrates because of its low annealing and drying temperature. Although soluble pentacene precursor semiconductor, which is a non-functionalized pentacene that readily transforms into pentacene upon heating near $200 \text{ }^\circ\text{C}$, has also attracted much

attention to this end, high-temperature annealing of soluble pentacene precursor semiconductor for >1 h causes film degradation resulting in poor electrical performance. For the fabrication of high-performance OTFTs with a TIPS pentacene active layer, many research groups have attempted to optimize the TIPS pentacene deposition conditions, such as solvent dependence, annealing temperature, and ambient conditions. Although the TIPS pentacene material itself is not completely transparent, thin film deposition can exhibit high transmittance, while still maintaining electrical properties.

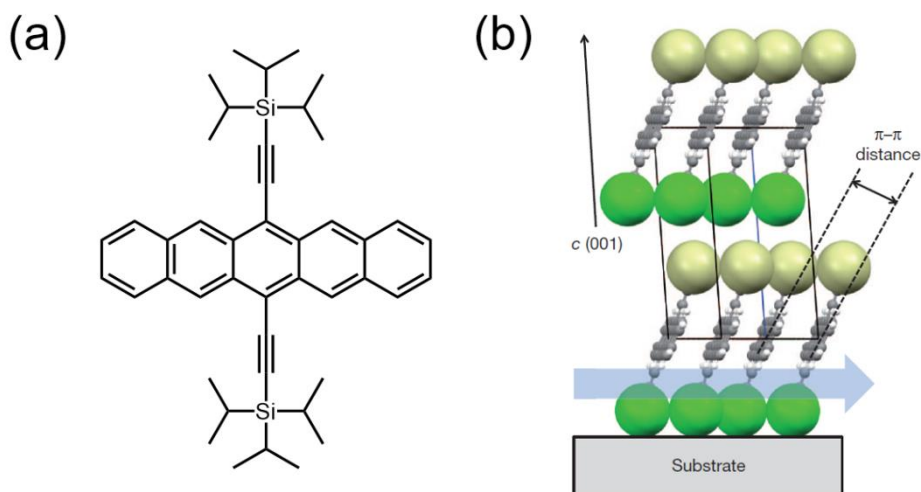


Figure 1.6 | (a) Chemical structure of TIPS pentacene. (b) Molecular packing structure of the TIPS pentacene thin film. The spheres in the figure represent the TIPS groups, where the yellow and green color indicate the front and back of the pentacene moiety, respectively. In addition, the blue arrow represents the high charge transport direction [32].

In addition, various surface treatments, such as octadecyltrichlorosilane and hexamethyldisilazane, have been reported on for a gate dielectric layer and S/D electrodes. However, to the best of our knowledge, a one-step interface engineering method that can be simultaneously introduced to both polymer electrodes and dielectric materials has not been studied yet; however, it should be noted that the sequential processes with two or more steps have been reported in previous studies.

1.3.3.2. SWCNTs

Since they were first reported on multi-walled carbon nanotubes (MWCNTs) and SWCNTs in 1991 [33] and 1993 [34], respectively, carbon nanotubes (CNTs) have received considerable attention owing to their unique physical properties that can potentially be applied to develop next-generation electronics [35, 36].

Atomic carbon is a species with a considerably short life; therefore, carbon is stabilized in the form of a variety of multiatomic structures with different molecular configurations, i.e. as allotropes. Carbon has a wide range of allotropes in various dimensions: zero-dimension (0D) as fullerene, one-dimension (1D) as SWCNT, two-dimension (2D) as graphene, and three-dimension (3D) as graphite (see Figure 1.7a). The electronic structures of SWCNTs can be investigated using the band structure of graphene because the formation of SWCNT involves rolling of a piece of graphene ribbon into a seamless cylinder [37]. Depending on the rolling angle used to form the cylindrical SWCNTs (i.e., chirality), the electronic structure of SWCNT can be metallic or semiconducting. The nanotube structures are specified using a pair of integers (n, m) defining a chiral vector that describes the circumference of the nanotube. In particular, (n, m) SWCNTs with $n - m = 3k$ are metallic, whereas those with $n - m \neq 3k$ are semiconducting, where $k = 0, 1, 2, 3, \dots$ [38]. The spikes in the

density of state (DOS) (see Figure 1.7b) in the SWCNTs are called van Hove singularities and manifest the confinement properties along the circumference of the nanotube.

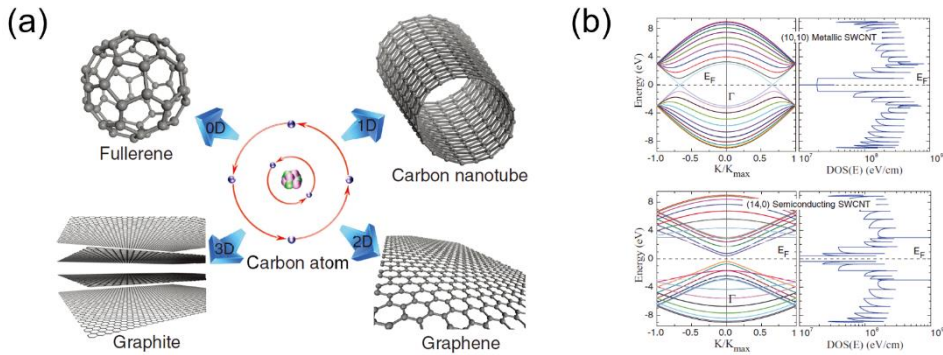


Figure 1.7 | (a) Crystal structures of different carbon allotropes: the carbon atom consists of six protons and neutrons inside the nucleus, and two electrons revolve in the 1s orbital whereas the four other electrons rotate in the next energetic 2s, 2p orbitals (middle). The carbon atoms form 0D fullerene (top left), 1D SWCNT (top right), 2D graphene (bottom right), and 3D graphite structures. (b) Electronic band structure and corresponding DOS of a (10,10) metallic SWCNT (top) and (14,0) semiconducting SWCNT (bottom) [39].

The nature of 1D carbon atoms bound together by Van der Waals forces leads to excellent electronic and mechanical properties with extreme flexibility. Moreover, because the electrical properties of the SWCNTs can be modified from metallic to semiconducting based on its chirality and diameter, this is an advantage because the electrical characteristics can be tuned for the required device operation. All these interesting properties of SWCNTs led many researchers to investigate its use in

various device applications, such as biosensors, gas sensors, transparent/flexible electrodes, and transistors [40, 41]. Among these applications, SWCNT TFTs for circuit applications are the most promising because silicon complementary metal-oxide-semiconductor technology and polysilicon transistors have been expected to reach performance limits and demands the transparent and flexible or even stretchable electronic devices are ever increasing. Moreover, in order to utilize these advantages of SWCNTs in large-area, high-throughput printed electronics, solution-based purification and assembly methods for SWCNT inks to obtain in high-quality SWCNT films, have been extensively studied.

1.3.3.3. MoS₂

Graphene has been highly favored because of its interesting properties, such as high mechanical strength, small thickness, and flexibility, among others. Most of all, primarily because of its extremely high mobility, graphene has been studied for the development of next generation electronic components [42-44]. However, using graphene as a channel layer has a critical drawback because it does not have an intrinsic band gap energy. In order to overcome this problem, researchers have attempted to chemically dope graphene or fabricate nano-ribbon-shaped graphene to create an artificial band gap [45]. Nevertheless, though a band gap in graphene can be obtained by specially treating it, it has been observed that doing so reduces electrical properties, such as mobility, making it difficult to use this modified graphene in electronic devices.

Motivated by the interesting features of 2D materials using graphene, researchers sought to find other 2D materials which can be used in electronics. In this regard, 2D transition-metal dichalcogenides (TMDCs) have received

considerable attention as emerging semiconductors owing to their promising atomic thin film properties with good field-effect mobility and tunable band gap energy [46]. The TMDCs consist of three atoms—one from transition metals, and the other two from the oxygen-group elements (chalcogen) (Figure 1.8a)—and have a covalent bond in the in-plane direction and weak Van der Waals bonds in the out-of-plane direction (Figure 1.8b). Therefore, these materials can be easily exfoliated using adhesive tape to form thin films. Among the various types of TMDCs, MoS₂ has been widely used as channel layer for TFTs. MoS₂ TFTs have several good characteristics such as high mobility, high on/off ratio, and tunable band gap energy based on the layer thickness [47].

Furthermore, in 2016, CVD-synthesized large-area monolayer MoS₂ TFTs with inkjet-printed silver electrodes were reported [48], which raised the expectation of researchers that large-area monolayer MoS₂ could be applied to printed electronics.

(a)

H																	He
Li	Be	MX_2 M = Transition metal X = Chalcogen										B	C	N	O	F	Ne
Na	Mg	3	4	5	6	7	8	9	10	11	12	Al	Si	P	S	Cl	Ar
K	Ca	Sc	Ti	V	Cr	Mn	Fe	Co	Ni	Cu	Zn	Ga	Ge	As	Se	Br	Kr
Rb	Sr	Y	Zr	Nb	Mo	Tc	Ru	Rh	Pd	Ag	Cd	In	Sn	Sb	Te	I	Xe
Cs	Ba	La-Lu	Hf	Ta	W	Re	Os	Ir	Pt	Au	Hg	Tl	Pb	Bi	Po	At	Rn
Fr	Ra	Ac-Lr	Rf	Db	Sg	Bh	Hs	Mt	Ds	Rg	Cn	Uut	Fl	Uup	Lv	Uus	Uuo

(b)

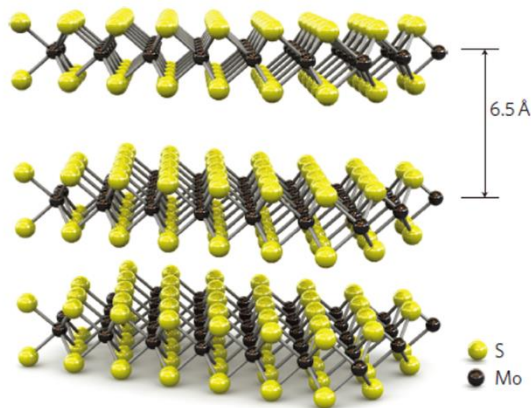


Figure 1.8 | (a) Transition metals and the three chalcogen elements that predominantly crystallize in their layered structures are highlighted in the Periodic table [46]. (b) Three-dimensional representation of the structure of MoS_2 [47].

1.3.4. Inkjet-Printing Systems

The experiments in this study were performed using a piezoelectric drop-on-demand inkjet printer (DMP-2831, Dimatix Corp.) that can allow multiple nozzle printing on various substrates (see Figure 1.9). Ink cartridges were classified as 10 picoliter (pL) and 1 pL cartridges, which are determined by the nozzle diameter. The nozzle

Chapter 2

Organo-Compatible Interface Engineering for Transparent Flexible Organic TFTs/Inverters

In this Chapter, we report a one-step and effective interface engineering with organo-compatible polystyrene (PS) interlayer for organic thin-film transistors (OTFTs). This chapter is composed of two sub-chapters.

In first sub-chapter, we report contact properties of fully inkjet-printed OTFTs with various channel lengths and their improvement by introducing an organo-compatible PS interlayer between the organic channel and inkjet-printed metallic contacts. Especially, because the contact resistance more dominantly affects a carrier injection property as channel length gets short, a short-channel length of 7 μm was formed to investigate effects of the organo-compatible interlayer obviously. To evaluate contact properties of the inkjet-printed short-channel OTFTs, transmission line method and Y -function method analyses were used for various channel lengths and low drain-to-source voltage (V_{DS}) regime, respectively. The contact properties

between inkjet-printed silver source/drain electrodes and 6,13-bis(triisopropylsilylethynyl)pentacene semiconductor were drastically enhanced showing contact resistance lowered by an order of magnitude and a good linearity at low V_{DS} regime after inserting an end-functionalized PS layer.

In second sub-chapter, we report a one-step interface engineering methodology which can be used on both polymer electrodes and gate dielectric for all-inkjet-printed, transparent, flexible OTFTs and inverters. Dimethylchlorosilane-terminated PS was introduced as a surface modifier to cured poly(4-vinylphenol) dielectric and poly(3,4-ethylenedioxythiophene):polystyrenesulfonate (PEDOT:PSS) electrodes without any pretreatment. With the benefit of the PS interlayer, the electrical properties of the OTFTs on a flexible plastic substrate were significantly improved. The all-organic-based thin-film transistors and inverters, including deformable and transparent PEDOT:PSS electrodes exhibited a light transmittance of higher than 70% (at wavelength of 550 nm). Specifically, there was no significant degradation in the electrical performance of the interface engineering-assisted system after 1000 bending cycles at a radius of 5 mm.

2.1. Interface Engineering for Inkjet-Printed Short-Channel Organic TFTs

2.1.1. Introduction

Inkjet-printed organic thin-film transistors (OTFTs) have been widely reported as emerging potential driving components for flexible and large-area electronic applications due to their ability to use low-temperature processing without vacuum processes [12-14, 49-51]. However, owing to the poor organic solvent and thermal resistance of the printed organic semiconductors, bottom-contact structures have been typically adopted instead of top-contact ones [12-14, 49, 51]. Therefore, printing of organic semiconductors onto bottom source and drain (S/D) electrodes and gate dielectrics results in a high contact resistance as well as unfavorable crystal structures of π -conjugated semiconductors during drying of solvents near S/D electrodes, yielding poor electrical performance, even if the devices are fully dedicated and aligned, compared to vacuum-processed systems [52, 53]. Moreover, as demand for short-channel OTFTs has been significantly increased for improvement of on-state current and maximum operating frequency in highly integrated systems [54-56], contact properties between organic semiconductors and inorganic S/D electrodes should be addressed because contact resistance is one of the most critical factors for electrical characteristics of OTFTs by dominantly affecting a carrier injection property as the channel the length gets short [57-59].

In this chapter, we report enhanced contact properties of fully inkjet-printed short-channel OTFTs by introducing a chlorosilane-terminated polystyrene (PS) interlayer between the S/D electrodes and semiconductor layers. The end-

functionalized PS layer allows not only the better contact properties by introducing an organo-compatible interface on the contacts, but uniformly deposited printed organic semiconductor layers by providing a smooth and sufficiently hydrophobic surface [60]. The contact properties were analyzed by using both transmission line method (TLM) and *Y*-function method (YFM).

2.1.2. Experiments

Figure 2.1 illustrates procedure of fabricating all-inkjet-printed OTFTs with various channel lengths in order to examine the contact resistance between the S/D electrodes and organic semiconductor layer using TLM. Onto the cleaned glass (Eagle XG) substrate, a metal-organic precursor type silver ink (Jet-001T, Hisense Electronics Corp.) was inkjet-printed to form a gate electrode, and then sintered at 150 °C for 30 min. The width and height of the gate electrode were 610 μm and 200 nm, respectively. For a gate dielectric layer, a poly(4-vinylphenol) (PVP) solution composed of 10 wt.% of PVP powder and 2 wt.% of poly(melamineco-formaldehyde) (PMFM) as a cross-linking agent dissolved in propylene glycol methyl ether acetate (PGMEA) was inkjet-printed in 2 passes. A ramped curing condition for the PVP dielectric layer was used to eliminate the formation of pin holes, and to allow a smoother surface [13]. For short-channel length and narrow S/D electrodes formation, nozzles with a small diameter of 9 μm that can eject 1 picoliter (pL) volume of ink droplets were used. Note that 2-pass-printed S/D electrodes were used to deliver better conductivity and surface properties. To introduce an organo-compatible PS interlayer, a 0.4 wt.% dimethylchlorosilane-terminated PS (PS-Si(CH₃)₂Cl, $M_n = 8$ kDa, Polymer Source Inc.) solution dissolved in toluene was also

inkjet-printed onto both the S/D electrodes and channel region, followed by being annealed at 100 °C for 1 h to deliver a chemically-stable monolayer coupled with the hydroxyl groups (–OH) on the dielectric. After annealing, the non-coupled residue was rinsed with toluene. Finally, for the formation of semiconductor layer, a 1 wt.% 6,13-bis(triisopropylsilylethynyl)pentacene (TIPS pentacene) (EM-index Corp.) solution dissolved in toluene was inkjet-printed onto the channel and contact region, and then dried at room temperature in ambient air. All layers in the device were inkjet-printed using a piezoelectric inkjet printer (DMP-2831, Dimatix Corp.). All measurements were performed at room temperature in ambient air.

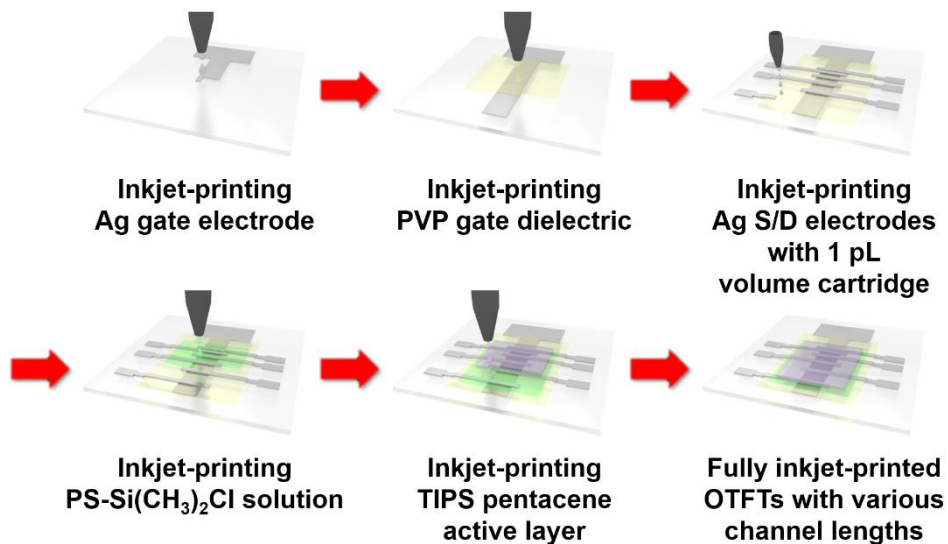


Figure 2.1 | Fabrication procedure of all-inkjet-printed OTFTs with various channel lengths [61].

2.1.3. Results and Discussion

To achieve good contact properties between solution-processed organic semiconductor layers and inorganic contacts, surface energy matching between the gate dielectric layers and S/D electrodes should be guaranteed to form well-crystallized semiconductor layers near the channel-contact boundary. The chemically-coupled PS interlayer allowed an organo-compatible surface on the inkjet-printed silver (Ag) electrodes providing a sufficient hydrophobic surface to produce highly ordered crystal structures of TIPS pentacene. Also, the interlayer delivered an excellent wetting property of TIPS pentacene semiconductor ink on both the gate dielectric layer and the S/D electrodes in a single-step, resulting in uniformly deposited π -conjugated semiconductor layers without discontinuous crystals (Figure 2.2a, b). Figure 2.2c, d show the channel length normalized transfer curves of the OTFTs without and with the PS interlayer, respectively. Because the contact resistance dominantly affects electrical performances of short-channel OTFTs, the length-normalized drain-to-source current (I_{DS}) was lowered as the channel length of the OTFTs shortened. This phenomenon also could be observed from the output characteristics of the OTFTs having a channel length of 7 μm (Figure 2.3a, b) comparing with those of the OTFTs having a channel length of 107 μm (Figure 2.3c, d). Although short-channel OTFTs still show more obvious *S*-shape at low drain-to-source voltage (V_{DS}) regime than those with a longer channel length, carrier injection properties of the OTFTs with the PS interlayer were drastically improved by enhancing the wetting and contact properties of TIPS pentacene near the contacts.

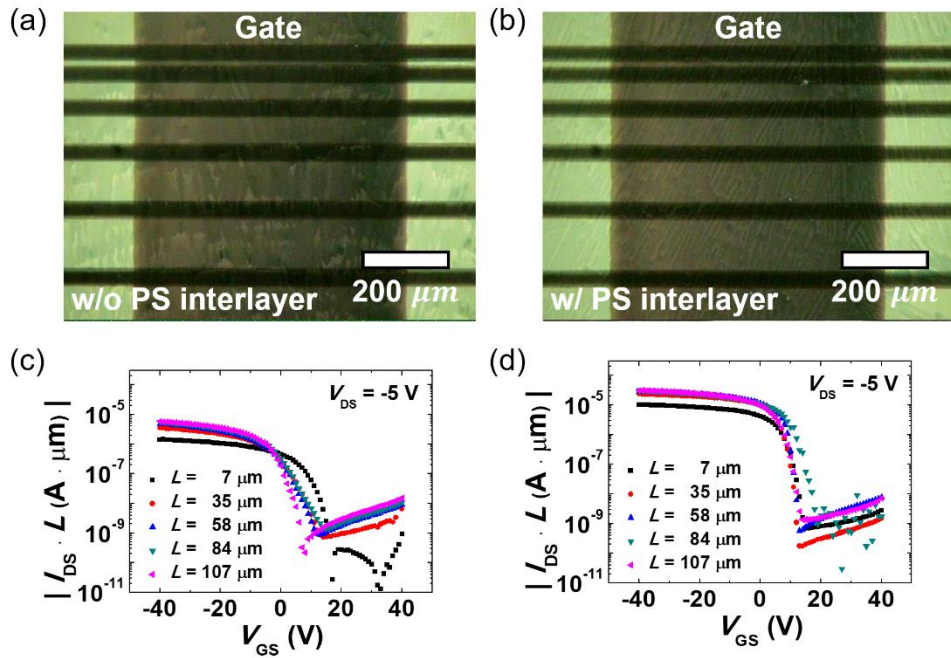


Figure 2.2 | Optical images of the OTFTs (a) without and (b) with the PS interlayer. Channel length normalized transfer curves of the OTFTs (c) without and (d) with a PS interlayer [61].

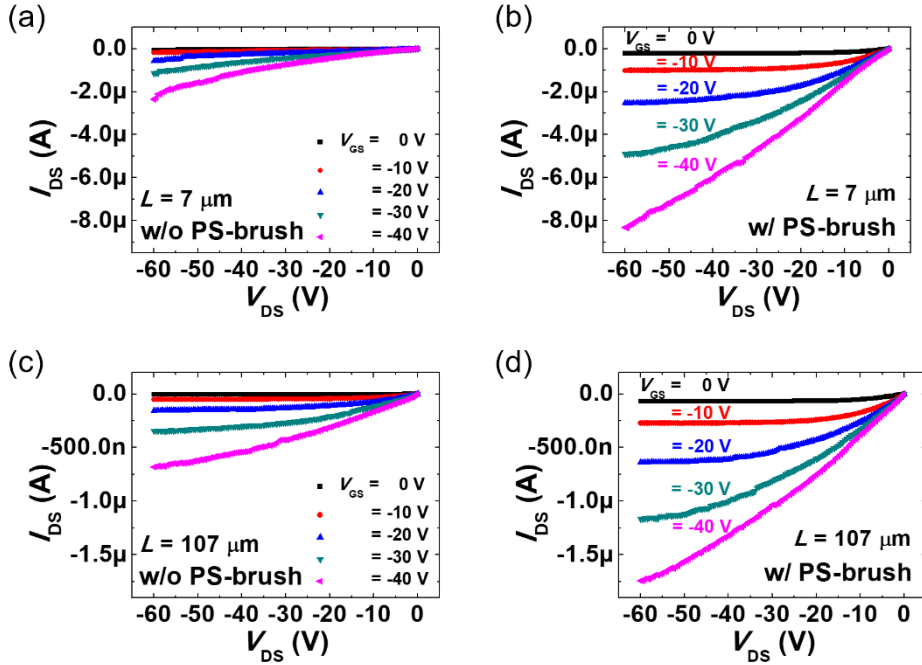


Figure 2.3 | (a–b) Output curves of the OTFT having a channel length of $7 \mu\text{m}$: (a) without (b) with the PS interlayer. (c–d) Output curves of the OTFTs having a channel length of $107 \mu\text{m}$: (c) without and (d) with the PS interlayer [61].

For further investigation of effects of the PS interlayer to the inkjet-printed OTFTs, the contact resistances were extracted by employing two kinds of analyses: TLM and YFM. From the electrical characteristics of the OTFTs with various channel lengths, the contact resistances between the S/D electrodes and semiconductor layer were extracted using TLM. Because the on-state resistance (R_{on}) of the OTFTs is the sum of the channel resistance (R_{ch}) and the contact resistance (R_c) in a linear regime, R_{on} can be expressed as following equation [62–64]:

$$R_{on} = R_{ch} + R_c = \frac{1}{\mu_{FET} W C_{ins} (V_{GS} - V_{th} - V_{DS}/2)} L + R_c \quad (2.1)$$

where L , W , C_{ins} , μ_{FET} , V_{GS} and V_{TH} denote a channel length, a channel width, capacitance per unit area of the gate insulator, a field-effect mobility, a gate-to-source voltage, and a threshold voltage, respectively. From the Equation 2.1, R_c can be assumed as R_{on} when the channel length is equal to 0 because R_{ch} is proportional to the channel length, which means R_c can be extracted from y-intercept of $R_{\text{on}}-L$ graph. From the relationship of R_{on} and the channel length in Figure 2.4a, b, the contact resistance of the OTFTs drastically reduced from 28.2 M Ω (= 1.72 M Ω ·cm) to 3.47 M Ω (= 0.211 M Ω ·cm) after introducing the PS interlayer. The contact resistance of the OTFTs without the PS interlayer is consistent with the previously reported result [53, 65]. Also, the logarithmic plot of the output characteristics as shown in Figure 2.4c supports enhanced carrier injection properties after introducing the PS interlayer due to the lower contact resistance showing a better linearity at low V_{DS} regime.

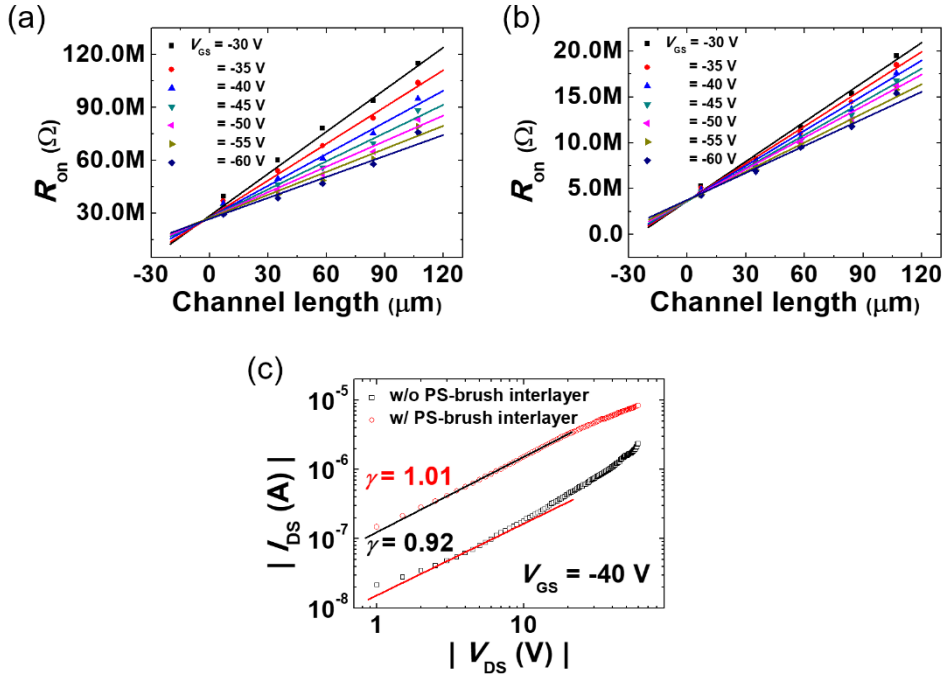


Figure 2.4 | TLM results for the OTFTs (a) before and (b) after introducing the PS interlayer. (c) The I_{DS} – V_{DS} relationship of short-channel OTFTs with and without the PS interlayer in a logarithmic scale (γ value closed to 1 means a good linearity) [61].

The contact resistances were also extracted using YFM which is known as useful method to extract a mobility, a threshold voltage, and a contact resistance [66-69]. Y -function can be expressed as following equation:

$$Y = \frac{I_{DS}}{\sqrt{g_m}} \quad (2.2)$$

where g_m denotes the transconductance. Assuming that V_{DS} is much smaller than $V_{GS} - V_{TH}$, I_{DS} can be approximated as [69]:

$$I_{DS} = \mu_0 C_{ins} \frac{W}{L} (V_{GS} - V_{TH}) (V_{DS} - I_{DS} R_C) \quad (2.3)$$

where μ_0 denotes a low field mobility. From the Equation 2.2 and 2.3, Y-function can be expressed as:

$$Y = \sqrt{\mu_0 C_{ins} V_{DS} \frac{W}{L} (V_{GS} - V_{TH})} \quad (2.4)$$

Therefore, from the Y-function– V_{GS} graph in Figure 2.5a, b, μ_0 and V_{TH} can be extracted from the slope and the x-intercept, respectively.

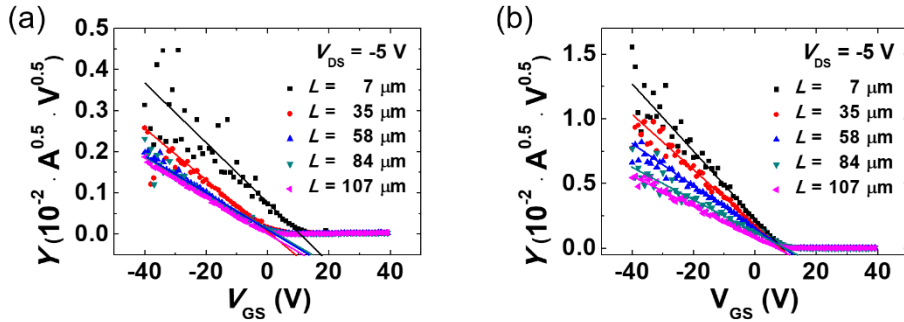


Figure 2.5 | Y-function— V_{GS} graphs of the OTFTs with various channel lengths (a) without and (b) with the PS interlayer [61].

After then, the contact resistance can be calculated from the following equation:

$$R_C = R_{on} - R_{ch} = \left| \frac{V_{DS}}{I_{DS}} \right| - \left| \frac{1}{\mu_0 C_{ins} (W/L) (V_{GS} - V_{TH})} \right| \quad (2.5)$$

Substituting μ_0 and V_{TH} to the acquired values from YFM, the contact resistances could be calculated. The contact resistances without and with the PS interlayer were 27.1 M Ω (= 1.65 M Ω ·cm) to 4.54 M Ω (= 0.277 M Ω ·cm) which are consistent with the extracted contact resistances by TLM. Electrical characteristics of the short-channel OTFTs including the contact resistances extracted from both the TLM and YFM are summarized in Table 2.1. From the extracted contact resistance values, it could be concluded that the PS interlayer delivered improved contact properties between the metallic contacts and organic semiconductor layer resulting in one order of magnitude reduced contact resistance. The rate of this improvement is comparable with those of the previously reported results [70-72]. Also, a facile printing method allowed a low-cost, easy and fast processing on large-area platforms.

Table 2.1 | Summary for electrical properties of the OTFTs without and with the PS interlayer.

	μ_{FET} [cm ² /V·s]	On/off ratio	R_c extracted by TLM [M Ω ·cm]	R_c extracted by YFM [M Ω ·cm]	N_{SS}^{max} [cm ⁻² · eV ⁻¹]
w/o PS interlayer	0.00816	1.08 × 10 ⁴	1.72	1.65	1.74 × 10 ¹²
w/ PS interlayer	0.125	3.73 × 10 ⁴	0.211	0.277	6.93 × 10 ¹¹

2.1.4. Conclusion

In this chapter, enhanced contact properties by conducting organo-compatible interface engineering between silver S/D electrodes and TIPS pentacene organic semiconductor layers for all-inkjet-printed OTFTs with a bottom-contact configuration were reported. The contact properties between the S/D electrodes and organic semiconductors were fully investigated by using both TLM at various carrier concentrations and YFM at various channel lengths, and the contact resistances extracted by two methods were well-agreed. By introducing the organo-compatible PS interlayer, the contact resistance was reduced by an order of magnitude showing a better carrier injection property. Based on these results, we believe this interface engineering approach can be an attractive candidate to solve contact-related issues for realizing low-cost and highly integrated inkjet-printed short-channel OTFTs and their applications.

2.2. One-Step Interface Engineering for Transparent Flexible Organic TFTs/Inverters

2.2.1. Introduction

In a bottom-gate and bottom-contact OTFT, it should be considered that the polar moieties of poly(3,4-ethylenedioxythiophene):polystyrenesulfonate (PEDOT:PSS) electrodes can cause a high contact resistance and a short conducting path of organic semiconductors, which together yield severe degradation in the electrical performance [73, 74]. A large mismatch in the surface energy (γ) between the bottom S/D electrode and gate dielectric materials develops an undesired and inhomogeneous semiconducting layer, particularly when a transverse printing between the predefined electrodes on the gate dielectrics is performed. Accordingly, many studies have been focused on matching the surface properties of the bottom electrode and gate dielectric to enhance not only the charge injection from the electrode to the semiconductor layer but also the charge-carrier transport along the π -overlapped semiconducting domains in OTFTs [75, 76].

Nonpolar self-assembled monolayers (SAMs) or grafted polymer layers may yield organo-compatible dielectric surfaces with fewer charge-trapping sites [60, 77]. As one of the most popular treatment methods, the introduction of proper SAMs onto the S/D electrode and dielectric surfaces is well-known to yield optimized surface properties, as well as achieve better ohmic contact and charge transport paths [78, 79]. However, low molecular weight (M_w) organo-silanes, or -carboxylic acids, -thiols, etc., have been utilized in limited capacities because of the complex processing conditions, originating from these poor environmental stability [80, 81]

and specific surface chemistry (e.g., organothiols for Au [82] and organo-silanes for hydroxyl-rich surfaces [83]). To the best of our knowledge, the one-step interface engineering with a SAM compound, which can simultaneously be introduced to both polymer electrode and dielectric materials, has not been studied yet, while the sequential two or more step processes have been reported elsewhere [71, 84]. End-functionalized polymers have been extensively used as reactive modifiers in the surface and interface-related nanoscience [60, 83, 85, 86]. Yang *et al.* have reported that the organo-compatibility of polar oxide or polymer dielectrics was enhanced through grafting of chlorosilane-end-terminated PS to these surfaces [60, 87]. In this case, the surface-grafted chains forming brush- or pancake type layers (4 ~ 6 nm) could maintain the excellent solvent resistance without any dewetting or delaminating symptoms, even under direct solvent contact.

Here, we report a simple interface engineering method for organic-based transparent electrode and dielectric materials, which can be simultaneously modified with end-silane-terminated PS without any preliminary treatment. The solvent-durable polymer layer bound to the bottom electrode and gate dielectric surfaces could considerably improve the electrical performance of all-inkjet-printed OTFTs and inverters including PEDOT:PSS, TIPS pentacene, and PVP as all-organic electrode, semiconductor, and insulator components, respectively, on a flexible plastic substrate. Optimized OTFTs showed a field-effect mobility (μ_{FET}) of 0.27 $\text{cm}^2/\text{V}\cdot\text{s}$, a threshold voltage (V_{th}) of 2.42 V, a subthreshold swing (SS) of 1.16 V/dec, and an on/off current ratio ($I_{\text{on}}/I_{\text{off}}$) of greater than 10^6 , in comparison to the untreated (no interlayer) systems that demonstrated severely degraded values ($\mu_{\text{FET}} < 0.02 \text{ cm}^2/\text{V}\cdot\text{s}$; $V_{\text{th}} = 4.41 \text{ V}$; $SS = 4.60 \text{ V/dec}$; $I_{\text{on}}/I_{\text{off}} \sim 10^4$). Also, the polymer interlayer-introduced inverters yielded a high voltage gain ($A_v = \partial V_{\text{out}}/\partial V_{\text{in}}$) of 7.17 V/V at

supply voltage (V_{DD}) of -20 V. The OTFTs and inverters including transparent PEDOT:PSS electrodes with a sheet resistance (R_S) of $160 - 240 \Omega/\text{sq}$ exhibited a light transmittance (T_L) of higher than 70% [at wavelength (λ) of 550 nm]. Specifically, there was no significant degradation in the electrical performance of the direct interface engineering-assisted system after 1000 bending–relaxation cycles at a bending radius (R) of 5 mm.

2.2.2. Experiments

2.2.2.1. Materials and Sample Preparation

Isopropyl alcohol (IPA, Daejung Chemicals & Metals Co.), PGMEA ($\geq 99.5\%$, Sigma-Aldrich), and toluene (anhydrous, 99.8%, Sigma-Aldrich) were used as solvents without any purification. PEDOT:PSS (E-157, Contech), PVP ($M_w = 25,000$ g/mol, Sigma-Aldrich), PMFM (number-average molecular weight (M_n) ~ 432 g/mol, Sigma-Aldrich), PS-Si(CH₃)₂Cl ($M_n = 7,800$ g/mol, PDI = 1.06, Polymer Source Inc.), and TIPS pentacene (EM-index Corp.) were purchased and used without any further treatment.

A flexible 200 μm thick Arylite film (A200HC, Ferrania Corp.) was sequentially ultrasonic-cleaned using IPA and deionized water media. First, as a gate material, the PEDOT:PSS solution was inkjet-printed on the Arylite film while at room temperature, using an inkjet printer (DMP-2831, Dimatix Corp.) with multiple piezo-response nozzles. The resulting gate electrodes were annealed at 130°C for 30 min. Then, a PVP layer was inkjet-printed on the patterned gate electrode with a solution containing 10 wt.% PVP and 2 wt.% PMFM dissolved in PGMEA. The layer was thermally cured with a two-step procedure: 100°C for 20 min and 200°C

for 20 min. On the gate dielectric, PEDOT:PSS S/D electrodes were patterned with the same printing and annealing conditions used for forming the gate electrodes: channel length (L) and width (W) were 60 μm and 1,050 μm , respectively. To introduce a polymer interlayer on the bottom S/D electrode and dielectric surfaces, the electrode and channel region were uniformly covered by a dilute PS-Si(CH₃)₂Cl solution inkjet-printed through 16 nozzles. After drying, the sample was cured at 100 °C for 1 h to efficiently bind the PS-Si(CH₃)₂Cl to these surfaces, and the unbound residues were removed via rinsing with an excess of toluene: the sample was sequentially immersed in toluene for 1 min and dried at 100 °C for 10 min in order to remove residual toluene.

Finally, TIPS pentacene OTFTs and inverters were fabricated on the untreated and polymer-treated bottom S/D electrode and dielectrics. A solution ink of TIPS pentacene dissolved in toluene was inkjet-printed on the bottom surfaces to form the drop spacing (see Figure 2.6) of 5 μm and the drop velocity of 5 m/s with a piezoelectric inkjet head, which contains independently controllable nozzles, at room temperature in ambient air. Then, the coating layer of TIPS pentacene was completely dried at room temperature for 1 h in air. The detailed jetting parameters of each layer inkjet-printed are summarized in Table 2.2. Additionally, transparent and flexible TIPS pentacene-based inverters were fabricated, including one diode-connected load OTFT ($W/L = 440 \mu\text{m}/320 \mu\text{m}$) and one driver OTFT ($W/L = 2,050 \mu\text{m}/80 \mu\text{m}$).

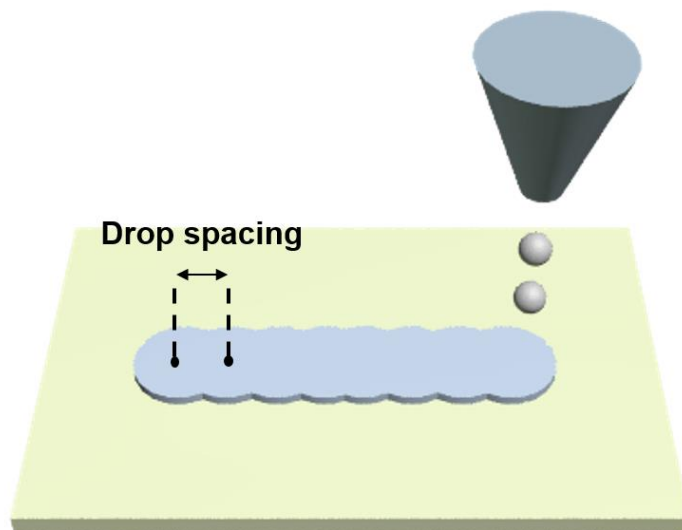


Figure 2.6 | Definition of a drop spacing in the inkjet-printing procedure [16].

Table 2.2 | The detailed jetting parameters to inkjet-print each layer in this study. Note that a piezoelectric inkjet head contains 16 jetting nozzles, with a diameter of 21 μm , which jet individual ink drops of 10 pL volume.

Jetting parameter	Layer			
	PEDOT:PSS	PVP	PS-Si(CH ₃) ₂ Cl	TIPS pentacene
# of nozzles	4	8	16	16
drop velocity [m/s]	12	8	5	5
frequency [kHz]	5	5	5	5
drop spacing [μm]	25	25	5	5
substrate temperature [$^{\circ}\text{C}$]	RT	RT	RT	RT

2.2.2.2. Characterization

The electrical properties of all the OTFTs and inverters were measured using a semiconductor parameter analyzer (4145B, Agilent Technologies) in a dark box. Scanning electron microscopy (SEM) was conducted on TIPS pentacene films inkjet-printed on the S/D electrode and dielectric surfaces using a field emission SEM (FE-SEM, S-4800, Hitachi Corp.). The transmittance measurement was conducted on a bare Arylite film, PEDOT:PSS layers, and all-printed devices on Arylite substrate using a spectrophotometer (DU-70, Beckman). The thicknesses of all printed layers were measured using a surface profiler (Alpha-step 500, Tencor Instruments), and morphologies were measured using an atomic force microscopy instrument (AFM, XE-100, Park Systems Corp.). To determine the surface moieties on the electrodes and dielectrics, X-ray photoelectron spectroscopy (XPS, Axis-HSI, Kratos Inc.) was conducted with an Al monochromator anode and a power of 18 mA and 12 kV. Ultraviolet photoelectron spectroscopy (AXIS Ultra DLD, Kratos Inc.) was performed on printed PEDOT:PSS layer with a He-I photon source. Mechanical properties of PEDOT:PSS and Ag (DGP 40LT-15C, ANP Corp.) layers were measured using a nanoindenter (TI 900TriboIndenter, Hysitron Corp.).

2.2.3. Results and Discussion

2.2.3.1. Inkjet-Printing of TIPS Pentacene OTFTs

Figure 2.7 shows the chemical compounds, scheme, and real image of the all-inkjet-printed, all-organic, transparent TIPS pentacene-based OTFTs on a 200 μm thick flexible Arylite film. All organic components in the device were sequentially printed on the flexible substrate with the following orders: gate, dielectric, S/D electrode,

optionally printed PS-Si(CH₃)₂Cl layer, and semiconductor layer. After two-pass printing, a mixture solution of 10 wt.% PVP and 2 wt.% PMFM as a cross-linker in PGMEA on a PEDOT:PSS gate printed plastic substrate, the printed dielectric was thermally annealed using the curing conditions noted in Chapter 2.2.2.1.

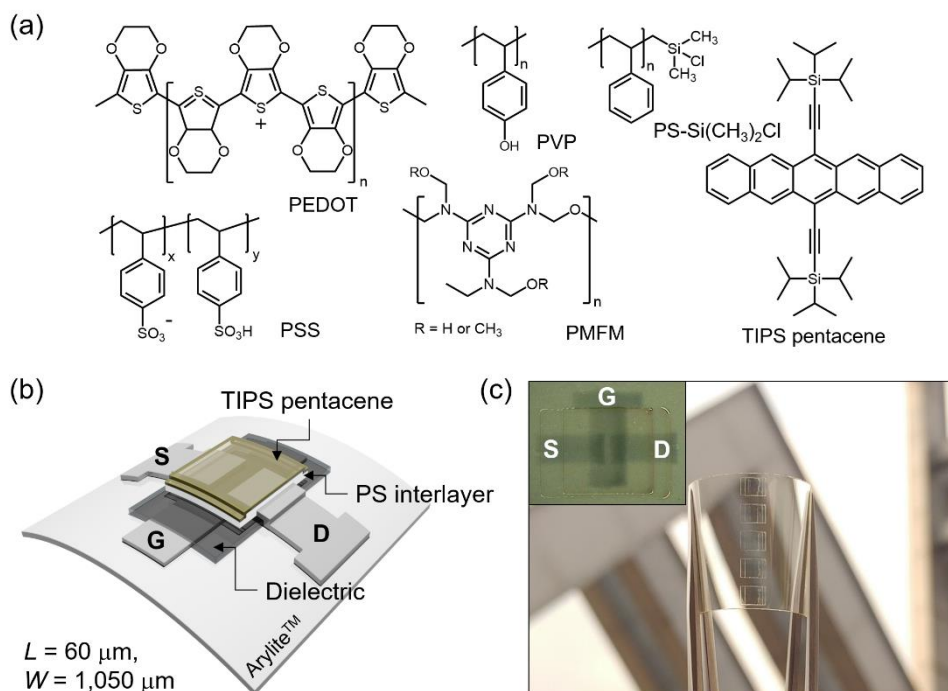


Figure 2.7 | (a) Chemical structures of the materials used in this study. (b) Scheme and (c) digital image of all-inkjet-printed TIPS pentacene OTFTs on an Arylrite substrate (a microscopic image of the device is also included in the inset) [16].

We have found that an appropriate ultraviolet–ozone (UV–O₃) or plasma treatment on Ag and PVP layers could generate active moieties, which could be coupled with silane-terminated polymers, e.g., PS-Si(CH₃)₂Cl [60]. However, it was reported that a UV–O₃ exposed PEDOT:PSS layer yielded severe conductivity

degradation by the decomposition of PEDOT:PSS, as shown in Figure 2.8 [88]. We proposed a direct treatment of PEDOT:PSS and PVP surfaces with PS-Si(CH₃)₂Cl, because sulfonate (–SO₃[–]) moieties on the PEDOT:PSS electrodes and –OH moieties on the PVP gate dielectric can be potential binding sites of the silane-terminated PS (Figure 2.9a) [89]. As an interlayer between the predefined bottom electrode/gate dielectric and top organic semiconductor, a PS-Si(CH₃)₂Cl layer ($M_n = 7,800$ g/mol) that was several tens of nanometers thick was inkjet-printed on both the PEDOT:PSS and PVP surfaces using a 0.4 wt.% solution dissolved in toluene, and then the printed layer was thermally treated to immobilize the chain ends to both surfaces at 100 °C for 1 h. Finally, the polymer-treated electrode and dielectric surfaces were rinsed with an excess of toluene to remove nonimmobilized residue from these surfaces (Figure 2.9a). On the basis of our previous works, it was expected that the immobilized polymer layer was a few nanometers thick [60].

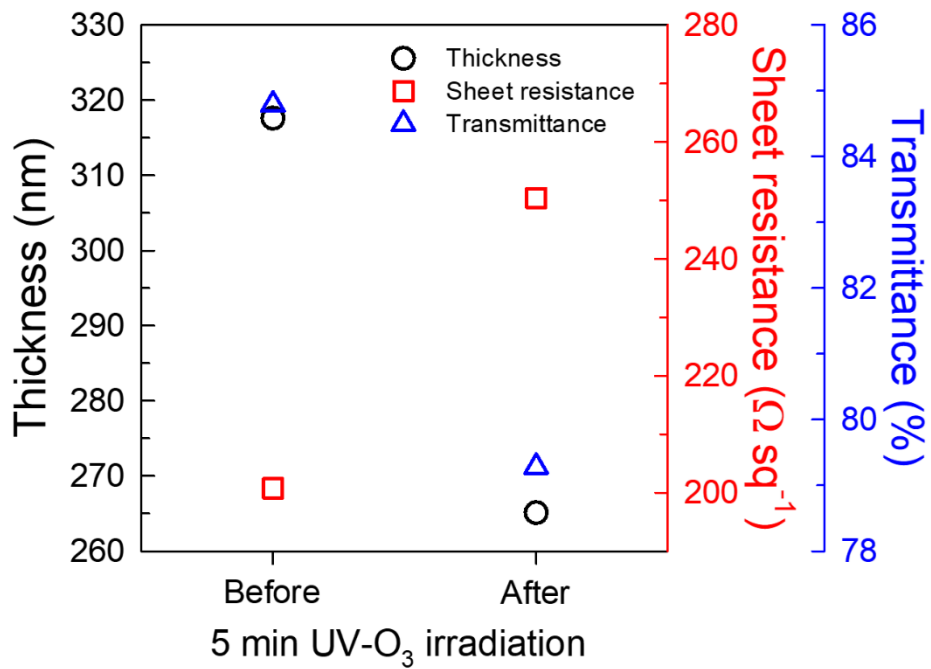


Figure 2.8 | Variations in transmittance and sheet resistance of inkjet-printed PEDOT:PSS layer before and after UV-O₃ irradiation for 5 min [16].

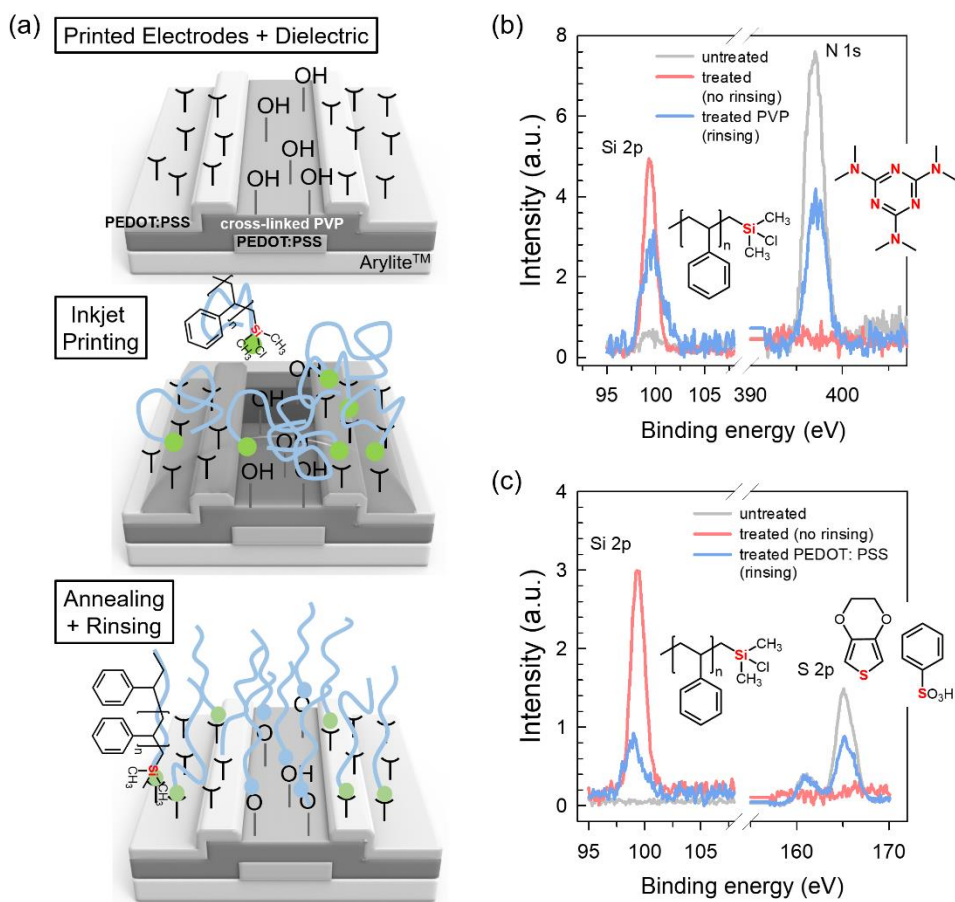


Figure 2.9 | (a) Binding scheme of PS-Si(CH₃)₂Cl to the predefined PEDOT:PSS and PVP surfaces on gate-patterned Arylite substrate. XPS spectra of untreated and PS-Si(CH₃)₂Cl-treated (b) PVP and (c) PEDOT:PSS films on substrates, before and after rinsing with an excess of toluene [16].

To clarify the proposed interface engineering, XPS was conducted on the PS-Si(CH₃)₂Cl-treated PVP and PEDOT:PSS films spun-cast on supporting substrates, before and after toluene rinsing (Figure 2.9b, c). First, XPS spectra of untreated 500 nm thick PVP and 200 nm thick PEDOT:PSS films did not indicate any binding energy for the Si 2p level. However, the XPS spectra showed intense photoelectron

signals at the binding energies of 397.0 and 165.1 eV related to the N 1s and S 2p levels of N and S atoms in PMFM and PSS, respectively (gray lines in Figure 2.9b, c). Interestingly, the XPS spectra of both the PS-Si(CH₃)₂Cl-treated films clearly showed Si 2p peaks at 99.5 eV, irrespective of solvent rinsing. The changes in signal of photoelectrons related to Si 2p, N 1s, and S 2p levels were related to the surface coverage of PS-Si(CH₃)₂Cl. Note that most of the collecting photoelectrons were located near the film surface (less than several nanometers) [90]. Before solvent rinsing, the XPS spectra of the polymer-treated PVP and PEDOT:PSS samples were mostly acquired from the topmost 20 ~ 30 nm thick PS-Si(CH₃)₂Cl coating layers, irrespective of the binding types and strength of the polymer to the surfaces. After rinsing, the treated PVP and PEDOT:PSS films with the topmost ultrathin layer of PS-Si(CH₃)₂Cl showed the relatively weaker XPS signals of the photoelectrons for N 1s and S 2p than those in the untreated films, maintaining the strong Si 2p peaks. This result can suggest that the PS-Si(CH₃)₂Cl chains can sufficiently bind to both PVP and PEDOT:PSS surfaces without any pretreatment.

On untreated and PS interlayer-assisted electrode and dielectric surfaces, approximately 70 nm thick TIPS pentacene layers were inkjet-printed and crystallized from the solution in order to complete flexible OTFTs with *L* of 60 μm and *W* of 1,050 μm (Figure 2.7b). Figure 2.10a, b shows typical optical microscopy (OM) images of TIPS pentacene layers on the predefined surfaces. The untreated system contained the irregular crystal morphologies of TIPS pentacene, which were clearly observed around the alternated PEDOT:PSS/PVP/PEDOT:PSS (i.e., electrode/dielectric/electrode) surface boundaries (Figure 2.10a). The result was mainly related to the discernible wettability of the TIPS pentacene solution inkjet-printed onto these heterogeneous surfaces.

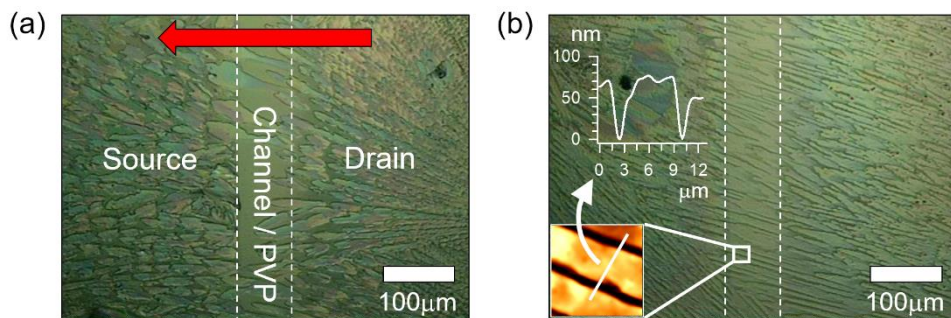


Figure 2.10 | OM images of TIPS pentacene films inkjet-printed on the (a) untreated and (b) polymer-treated PEDOT:PSS and PVP surfaces. The red arrow in panel a represents the inkjet-printing direction of the TIPS pentacene ink from the one electrode to the other, and the insets in panel b represent AFM topography and a cross-sectional profile collected from the white-boxed region in the channel area [16].

Among these materials used to generate core components in OTFTs, the difference in γ tended to induce a preferred wetting of the TIPS pentacene solution ($\gamma_{\text{TIPS pentacene}} = 47.36 \text{ mJ/m}^2$; $\gamma_{\text{toluene}} = 28.52 \text{ mJ/m}^2$) on the untreated PVP dielectric ($\gamma_{\text{PVP}} = 48.41 \text{ mJ/m}^2$), instead of the hydrophilic PEDOT:PSS electrodes ($\gamma_{\text{PEDOT:PSS}} = 67.80 \text{ mJ/m}^2$) [91]. The γ values of each layer were extracted using Owens-Wendt model (Figure 2.11) [92]. The difference of γ between two surfaces could be shown in Figure 2.12. A water droplet was split and preferentially located to hydrophilic PEDOT:PSS sides (Figure 2.12a), while a similar volume of water formed a singular water droplet with a contact angle of approximately 91° on the polymer-treated PEDOT:PSS and PVP surfaces (Figure 2.12b).

Film	Contact angle (DI water)	Contact angle (Diiodomethane)	Surface energy [mJ/m ²]
TIPS pentacene	90.71°	22.34°	47.36
PVP	58.6°	41.7°	48.41
PEDOT:PSS	20.6°	54.2°	67.80

Figure 2.11 | Surface energy values of TIPS pentacene, PVP, and PEDOT:PSS layer extracted using Owens-Wendt model.

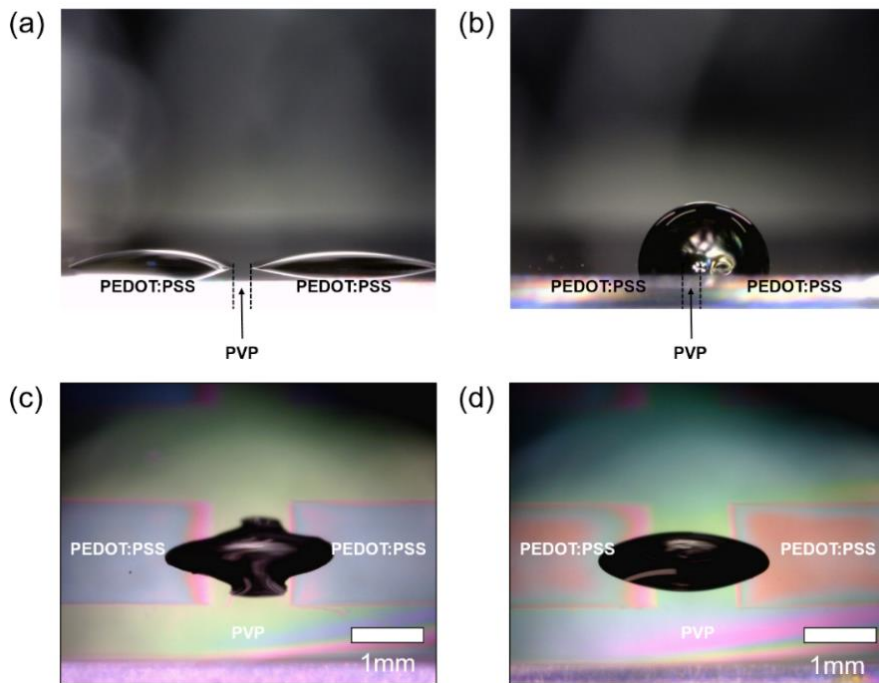


Figure 2.12 | Discernible wetting behaviors of water droplets located on (a) untreated and (b) treated PEDOT:PSS and PVP surfaces. Wetting characteristics of the TIPS pentacene solutions located on the (c) untreated and (d) polymer-treated PEDOT:PSS and PVP surfaces [16].

On the untreated surfaces, a certain amount of TIPS pentacene solution was quickly dewetted from the hydrophilic PEDOT:PSS side (Figure 2.12c). During printing, the relatively large volume of the TIPS pentacene solution located on the PVP dielectric side required a longer evaporation time, in comparison to the electrode side. As a result, the TIPS pentacene that was quickly crystallized on the PEDOT:PSS electrodes showed a highly shattered morphology, while on the PVP side, the TIPS pentacene formed layer like crystallites along the printing direction (arrow in Figure 2.10a). This kind of wetting behavior on patterned surfaces has also been utilized to develop unique patterns allocated only to predefined regions on a substrate [28].

In contrast, it was observed that the printed solution on the PS interlayer-assisted electrode and dielectric surfaces was steadily dried, thereby avoiding the coffee-ring effect (Figure 2.12d). The resulting interlayer-introduced system could modify the electrode and dielectric surfaces to maintain a similar solvent wettability, yielding an enhanced crystal layer of TIPS pentacene along the predefined surfaces (Figure 2.10b). The PS interlayer effects on the structural development of TIPS pentacene films onto the surfaces are clearly displayed in Figures 2.13 and 2.14. Particularly, it was found that a better morphological continuity near the contact region was indicated with the PS-Si(CH₃)₂Cl treated system (Figure 2.13).

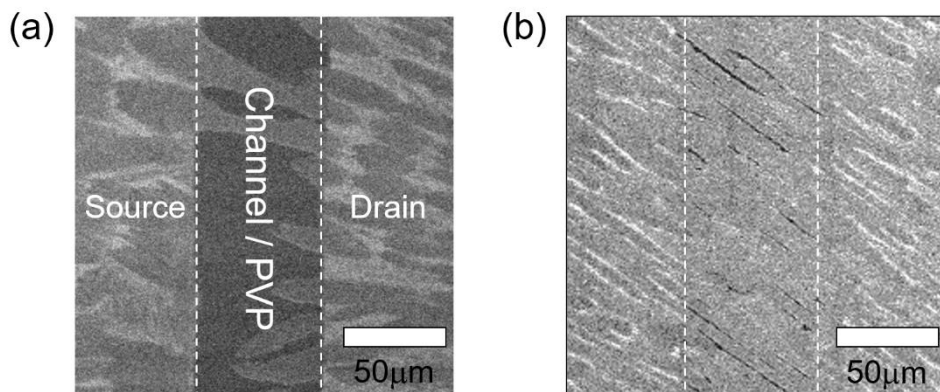


Figure 2.13 | SEM images of the TIPS pentacene channel layers near the contact region inkjet-printed on (a) without and (b) with PS-treated surfaces [16].

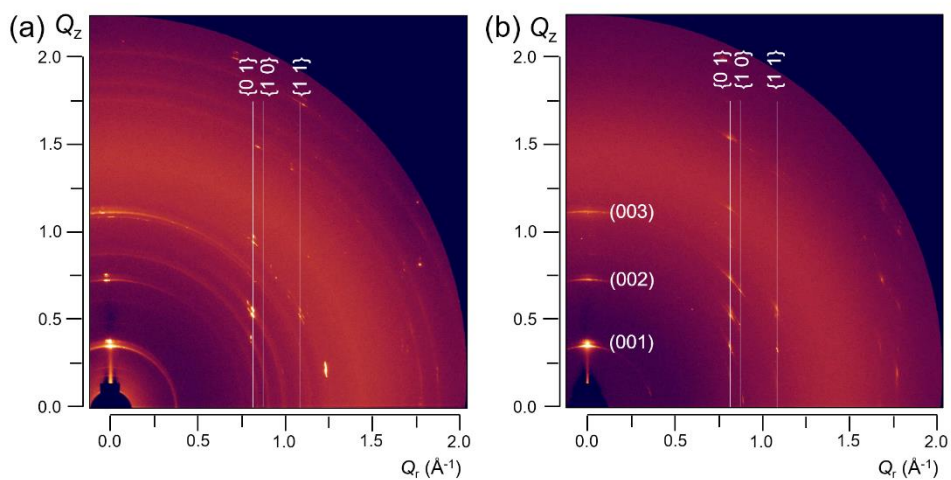


Figure 2.14 | 2D GIXD patterns of TIPS pentacene films inkjet-printed on (a) untreated and (b) PS-Si(CH₃)₂Cl-treated surfaces [16].

In addition, synchrotron-based 2D grazing incidence X-ray and diffraction (GIXD) (Pohang Accelerator Laboratory, 9A, Korea) was conducted on TIPS pentacene films inkjet-printed onto the untreated and PS-Si(CH₃)₂Cl-treated surfaces. Typical area of a TIPS pentacene layer inkjet-printed on a single TFT was approximately 1,500 × 1,500 μm², which was hard to be aligned using the GIXD mode with an incident angle of X-ray. Due to this reason, we inkjet-printed 3,000 × 5,000 μm² patterned layers of TIPS pentacene on both the untreated and PS-Si(CH₃)₂Cl-treated surfaces, which had the same geometry with TFTs used in this study. As shown in Figure 2.14, TIPS pentacene films on the PS-Si(CH₃)₂Cl-treated surface showed highly ordered crystal structure (Figure 2.14b), in comparison to the untreated system containing less-ordered crystals, as determined by the broad X-ray reflection along the Debye rings (Figure 2.14a).

The solvent wettability-driven crystal morphologies of TIPS pentacene were expected to yield different electrical performances of the resulting OTFTs (will be discussed in Chapter 2.2.3.3).

2.2.3.2. PEDOT:PSS Layers as Transparent Conducting Electrodes

PEDOT:PSS polymers have been widely utilized as conducting materials for transparent organic electronics applications [17, 28, 93]. Note that the thicker layer of PEDOT:PSS required to achieve high conductance yields a lower T_L . Figure 2.15a shows digital images of “SNU” letter-shaped PEDOT:PSS patterns inkjet-printed on the Arylite films with a pass number from 1 to 5, which clearly offer different readability.

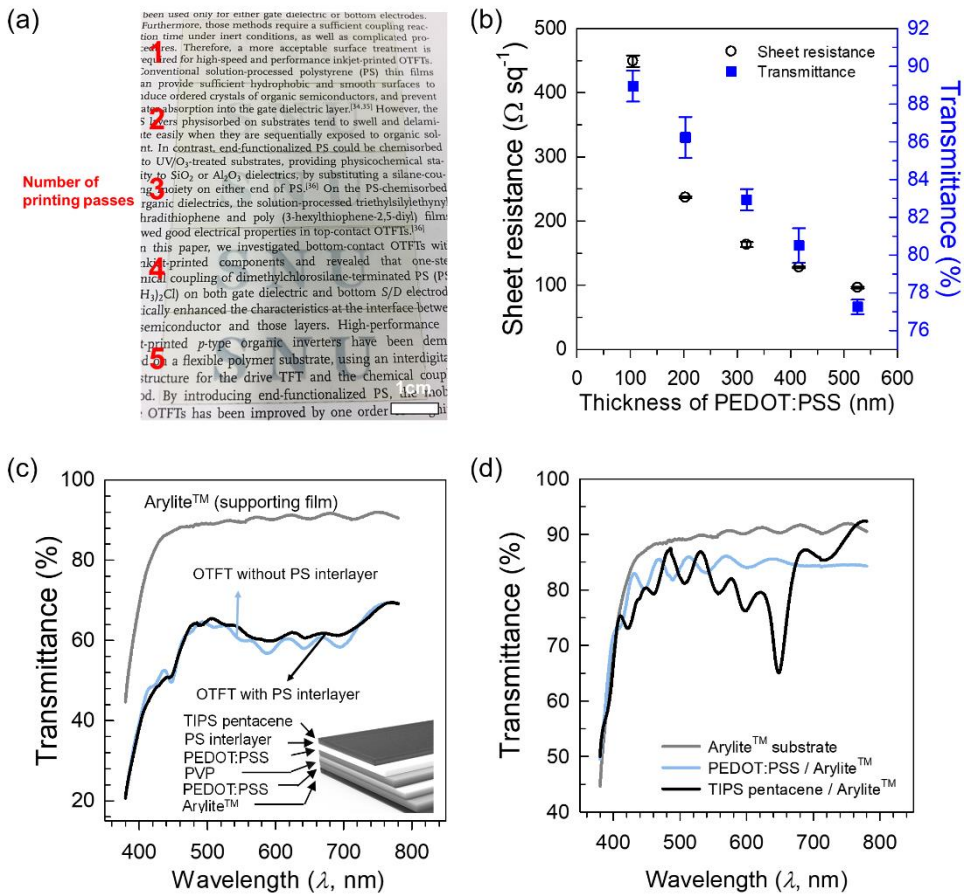


Figure 2.15 | (a) “SNU”-letter shaped PEDOT:PSS patterns having different thicknesses inkjet-printed on Arylite films with different number of printing passes from 1 to 5. (b) Optical and electrical characteristics of the PEDOT:PSS electrodes with different thicknesses. The jetting parameters for the PEDOT:PSS layers are summarized in Table 2.2, specifically, a drop spacing of 25 μm. (c) T_L variations of an Arylite substrate and fully printed OTFTs. (d) Transmittances of bare Arylite film, inkjet-printed PEDOT:PSS, and TIPS pentacene films on the Arylite substrate [16].

To investigate the thickness-dependent R_s and T_L of the conducting polymer films, different thick PEDOT:PSS layers were inkjet-printed on a $1 \times 1 \text{ cm}^2$ area of

Arylite films. As expected, the average R_s and T_L (at 550 nm) values of the PEDOT:PSS layers decreased monotonically from 449 to 93 Ω/sq and from 88.9 to 77.2%, respectively, with an increase in average layer thickness (h) ranging from approximately 105 to 525 nm (Figure 2.15b). Although a single-pass printed layer (with $h = 105$ nm) showed the highest T_L value of 88.9%, its R_s value, 449 Ω/sq , was too high to be used as a conducting electrode. In the all-inkjet-printed OTFTs and inverters, approximately 300 and 200 nm thick PEDOT:PSS layers, as gate and S/D electrodes, were designed to avoid a resistive–capacitive delay and a voltage drop on the electrodes. The average values of R_s for the resulting gate and S/D electrodes were observed to be 163 and 247 Ω/sq , respectively. Additionally, all the printed PEDOT:PSS electrodes showed an average resistivity of $5.0 \times 10^{-3} \Omega\cdot\text{cm}$, which was higher than those ($1 \sim 4 \times 10^{-4} \Omega\cdot\text{cm}$) of highly compact spun-cast PEDOT:PSS layers [94] but comparable to those of inkjet-printed single-walled carbon nanotube (SWCNT) ($2.2 \times 10^{-3} \Omega\cdot\text{cm}$) [19] and solution-processed transparent conductive oxide (e.g., $3.3 \times 10^{-3} \Omega\cdot\text{cm}$ for a gallium-doped zinc oxide [95]) systems reported previously. Particularly, the inkjet-printed PEDOT:PSS layers used in this study showed much better transmittance, surface roughness, and uniformity in comparison to the inkjet-printed SWCNT layer [19].

Figure 2.15c shows T_L of a 200 μm thick Arylite film and the fully printed OTFTs on the flexible substrate measured within the visible wavelength ranging from 380 to 780 nm. Note that in order to consider the worst-case in T_L , the measured samples were prepared by sequentially printing all organic layers composing the OTFTs over the whole Arylite substrates with the following order: PEDOT:PSS, PVP, PEDOT:PSS, optionally printed PS interlayer, and TIPS pentacene. The samples including the printed OTFTs caused a relatively higher light absorption at λ of 500 –

720 nm due to the TIPS pentacene layer (Figure 2.15d), in comparison to the bare Arylite film. Interestingly, the presence of the ultrathin PS interlayer (less than 6 nm [60, 87]) in the OTFT slightly improved the overall T_L of the device compared to the untreated system including irregular crystal morphology of TIPS pentacene. After the absorption portion is subtracted from the Arylite substrate, the fully printed OTFTs based on the untreated and treated surfaces showed the T_L values of 67.1 and 70.0% (at $\lambda = 550$ nm), respectively. These values were comparable to those of previously reported transparent OTFTs with organic or inorganic electrodes [96, 97].

As a flexible electrode, a PEDOT:PSS layer can maintain a sustainable conductance under an external stress, in comparison to the inkjet-printed Ag layer containing percolated nanoparticles. The mechanical properties of PEDOT:PSS layers were evaluated using a nanoindentation method (Figure 2.16); a well-defined diamond probe (loading resolution < 1 nN) was connected to a vertical transducer and a force gauge.

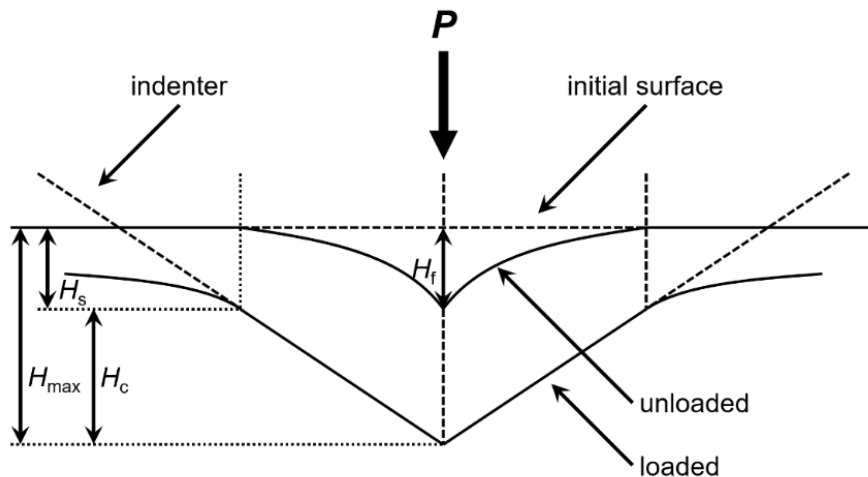


Figure 2.16 | Schematic illustration of the loading-unloading process during a nano-indentation [16].

Figure 2.17a shows the load force–displacement curve of an approximately 350 nm thick PEDOT:PSS layer on the Arylite film during nanoindentation. In general, the elastic and plastic deformations on a film surface simultaneously occur during the loading cycle. In contrast, the recovery of the elastic deformation occurs during the unloading cycle. When the loading–unloading response of the film was investigated, reduced Young’s moduli (E_r) of the thin films were extracted; a detailed calculation process of E_r from the curve is presented below. The E_r value of the printed PEDOT:PSS layer was calculated to be 0.61 GPa, much lower than that (47.5 GPa) of an Ag layer inkjet-printed with a similar thickness (Figure 2.17b). Under a stress, the printed PEDOT:PSS electrode is easily deformable, thereby enhancing the bending stability of the resulting OTFTs and inverters (will be also discussed in Chapter 2.3.3).

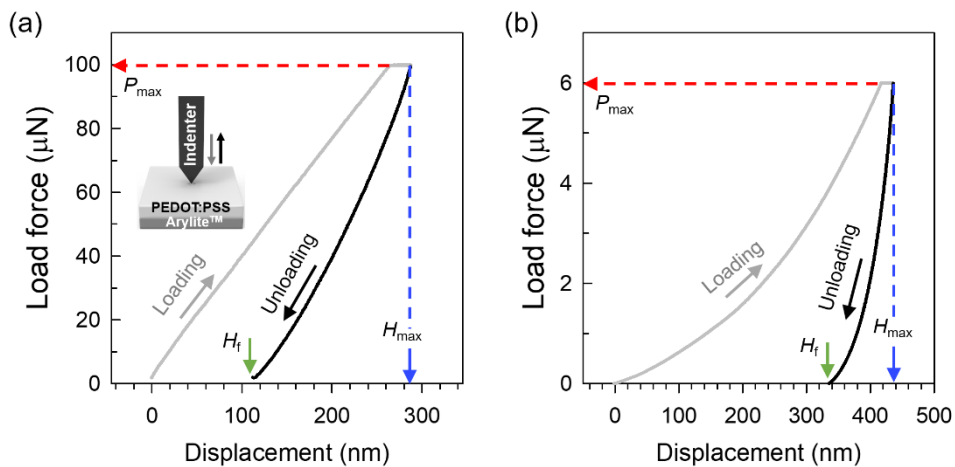


Figure 2.17 | Force–displacement curve of an approximately (a) 350-nm-thick PEDOT:PSS layer and (b) 400-nm-thick Ag layer on the Arylite film during a nano-indenting cycle of loading–unloading (see the inset of (a)) [16].

From the unloading curve in Figure 2.17a, b, the elastic stiffness (S) can be defined as the slope of the tangential line at the uppermost portion of the unloading curve [98]:

$$S = \frac{dP}{dH} \quad (2.6)$$

where P and H are the load force and displacement, respectively.

The loading-unloading process is illustrated schematically in Figure 2.16. Note that the depth at a final unloaded state (H_f) usually shows a non-zero value due to a plastic deformation observed during the previous loading cycle. The unloading curve can be modeled using a power law relation:

$$P = \alpha(H - H_f)^m \quad (2.7)$$

where α and m are power law fitting parameters.

Sink-in depth (H_s) is expressed as follows:

$$H_s = \varepsilon \frac{P_{max}}{S} \quad (2.8)$$

where ε is a parameter related to the indenter geometry.

The vertical displacement of the contact depth (H_c) can be calculated from H_s and the maximum depth (H_{max}):

$$H_c = H_{max} - H_s = H_{max} - \varepsilon \frac{P_{max}}{S} \quad (2.9)$$

Finally, E_r can be calculated by the following equation:

$$E_r = \frac{S}{2\beta} \sqrt{\frac{\pi}{A_p(H_c)}} \quad (2.10)$$

where β and $A_p(H_c)$ represent a geometrical constant and the projected area at the H_c during loading, respectively.

The measured and extracted parameters of the inkjet-printed PEDOT:PSS and Ag electrodes are summarized in Table 2.3.

Table 2.3 | E_r values of the inkjet-printed PEDOT:PSS and Ag electrodes based on the measured parameters.

Parameters	Inkjet-printed PEDOT:PSS	Inkjet-printed Ag
E_r (GPa)	0.61	47.5
H_c (nm)	193.3	298.24
S ($\mu\text{N}/\text{nm}$)	0.8	156.15
P_{\max} (mN)	0.1	6.0
H_{\max} (nm)	287.6	405.83
$A_p(H_c)$ (μm^2)	1.25	5.03

2.2.3.3. Electrical Properties of All-Inkjet-Printed OTFTs and Inverters

Electrical performance of all-inkjet-printed OTFTs and inverters were characterized in dark conditions. Figure 2.18 shows the drain current–gate voltage (I_{DS} – V_{GS}) transfer and drain current–drain voltage (I_{DS} – V_{DS}) output curves of OTFTs including TIPS pentacene layers on the untreated and PS interlayer-assisted S/D and dielectric surfaces. Because of the benefit of the introduced polymer, the maximum interface trap density (N_{SS}^{max}) at the semiconductor–dielectric interface in OTFTs estimated from an amorphous silicon transistor model [99] as shown in Equation 2.11 decreased up to $5.12 \times 10^{11} \text{ cm}^{-2} \cdot \text{eV}^{-1}$, approximately 25.2% of that ($2.03 \times 10^{12} \text{ cm}^{-2} \cdot \text{eV}^{-1}$) for the untreated device.

$$N_{SS}^{max} = \left(\frac{SS \log e}{kT/q} \right) \frac{C_{ins}}{q^2} \quad (2.11)$$

where k , T , q , and C_{ins} represent the Boltzmann constant, the absolute temperature, the electron charge, and the capacitance of the gate dielectric, respectively.

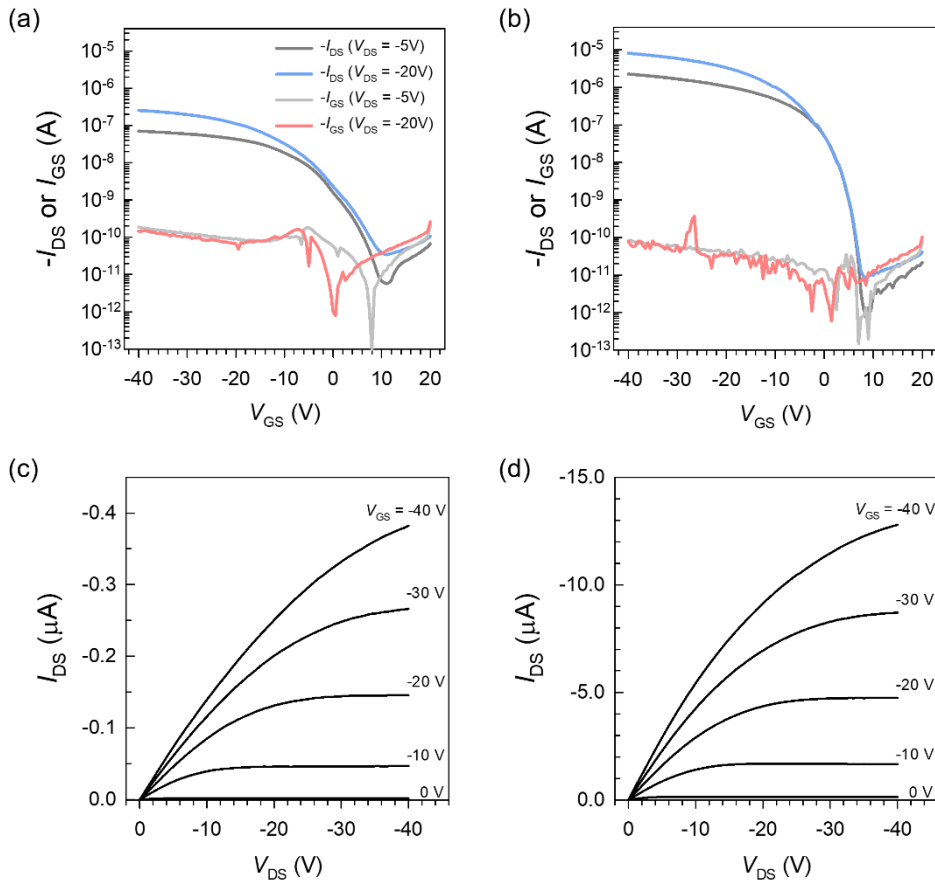


Figure 2.18 | (a, b) I_{DS} - V_{GS} transfer and (c, d) I_{DS} - V_{DS} output curves of TIPS pentacene OTFTs based on the (a, c) untreated and (b, d) PS interlayer-introduced PEDOT:PSS and PVP surfaces [16].

Particularly, the presence of the PS interlayer between the PEDOT:PSS and TIPS pentacene surfaces induced a significant decrease in the R_c from 208 to 16.2 $k\Omega \cdot cm$, as measured by the TLM (details provided in Chapter 2.1.3). Figure 2.19a, b show the R_{tot} - L graphs of the OTFTs on untreated and treated surfaces at $V_{DS} = -5$ V, respectively. The observed R_c values were comparable to those of bottom-contact and top-contact OTFTs with evaporated Au electrodes, respectively [53]. The

outstanding enhancement of a carrier injection property for the polymer-treated system was indicated by the improved linearity in the output curves at low V_{DS} regime (Figure 2.19c). Assuming $I_{DS} \propto V_{DS}^\delta$, a δ value close to 1 indicates that the output characteristic shows good linearity in the low V_{DS} regime. From the graph, δ values of the OTFTs changed from 1.07 to 0.99 by introducing the PS interlayer. The result strongly supported that the wettability-matching interface engineering could improve the minimization of the charge trap sites and the better contact and crystal structure of the organic semiconductor. It should be noted that the enhanced charge carrier injection properties after the PS-treatment are attributed to the morphological improvements of the TIPS pentacene semiconductor layer near the contact region, not a change of the work-function values of the PEDOT:PSS electrodes (~ 5.02 eV).

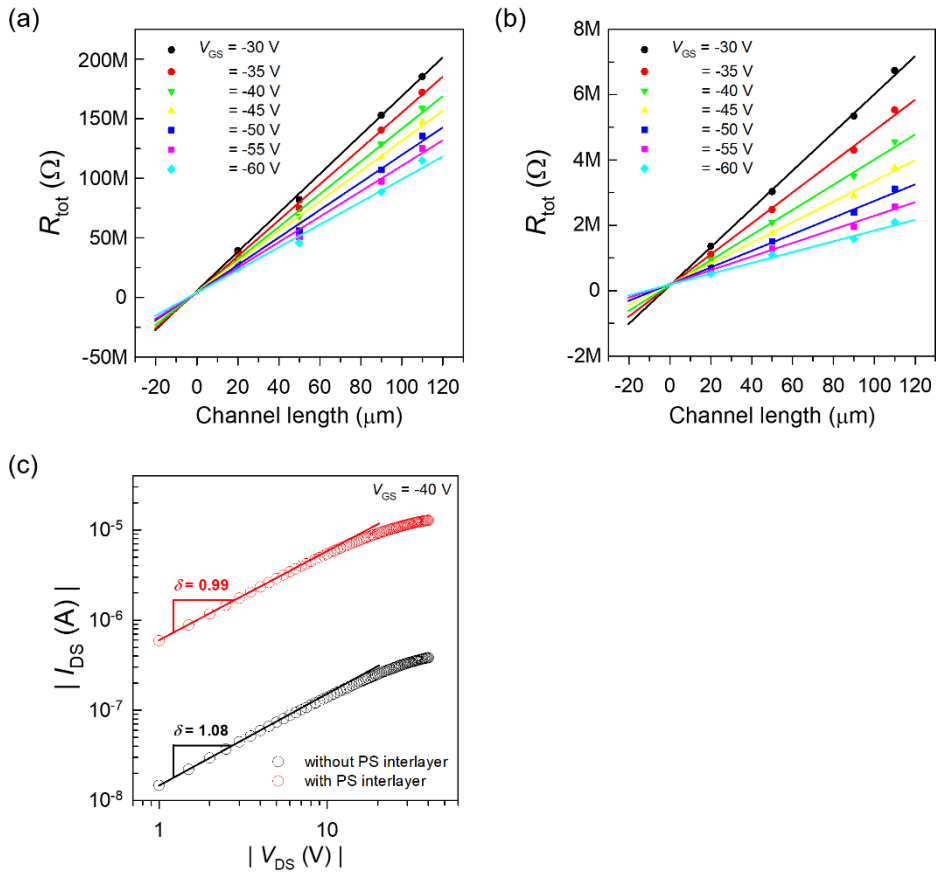


Figure 2.19 | (a, b) TLM results for OTFTs on (a) untreated and (b) treated surfaces.

(c) $I_{\text{DS}}-V_{\text{DS}}$ relationship in log scale of OTFTs [16].

As expected from the morphology of TIPS pentacene on the untreated electrode and dielectric surfaces (Figure 2.10a), the resulting OTFT showed a severe degradation in the electrical performance: μ_{FET} of less than $0.02 \text{ cm}^2/\text{V}\cdot\text{s}$, V_{th} of 4.41 V, SS of 4.60 V/dec, and $I_{\text{on}}/I_{\text{off}}$ of $\sim 10^4$. In contrast, the PS interlayer-introduced OTFTs showed drastic improvement in the electrical performance: $\mu_{\text{FET}} = 0.27 \text{ cm}^2/\text{V}\cdot\text{s}$, $V_{\text{th}} = 2.42 \text{ V}$, $SS = 1.16 \text{ V/dec}$, and $I_{\text{on}}/I_{\text{off}} > 10^6$. The extracted electrical characteristics are summarized in Table 2.4. The improved device performance

surpassed the previous works related to TIPS pentacene OTFTs with inkjet-printed PEDOT:PSS [73, 74] or Ag electrodes [60]. Detailed electrical characteristics of previously reported transparent OTFTs are also summarized in Table 2.5.

Table 2.4 | Typical electrical characteristics of TIPS pentacene OTFTs on the untreated and PS-Si(CH₃)₂Cl-treated surfaces.

OTFTs	μ_{FET} [cm ² /V·s]	V_{th} [V]	SS [V/dec]	$I_{\text{on}}/I_{\text{off}}$
Untreated	0.017 ± 0.010	4.41 ± 1.64	4.60 ± 1.01	$\sim 10^4$
Treated	0.27 ± 0.058	2.42 ± 0.48	1.16 ± 0.14	$> 10^6$

Table 2.5 | Comparative electrical characteristics of previously reported transparent OTFTs.

Substrate	Electrode	Semiconductor	μ_{ET}	$I_{\text{on}}/I_{\text{off}}$	R_c	Reference
			[$\text{cm}^2/\text{V}\cdot\text{s}$]		[$\text{k}\Omega\cdot\text{cm}$]	
Arylite	PEDOT:PSS	TIPS pentacene	0.27	$> 10^6$	16.2	This work
Arylite	PEDOT:PSS	Pentacene	0.035	$\sim 10^6$	~ 1000	[100]
PES	PEDOT:PSS	TIPS pentacene	0.05	$\sim 10^4$	N/A	[101]
PET	PEDOT:PSS	TIPS pentacene	0.0078	$\sim 10^4$	N/A	[73]
Arylite	Graphene	Pentacene	0.12	$\sim 10^4$	8 ~ 20	[102]
Glass	ITO	P3HT	0.01	$\sim 10^4$	N/A	[103]
Glass	ITO	Pentacene	0.226	N/A	260	[104]
Glass	$\text{Sb}_2\text{O}_3/\text{Ag}/\text{Sb}_2\text{O}_3$	Pentacene	0.3	$\sim 10^3$	N/A	[105]
Glass	$\text{WO}_3/\text{Ag}/\text{WO}_3$	PSeTPTI	0.038	~ 2 $\times 10^6$	N/A	[106]
Glass	$\text{WO}_3/\text{Ag}/\text{WO}_3$	Pentacene	0.0844	1.2 $\times 10^6$	252000	[107]
Glass	Ag network	DNTT	0.12	$> 10^7$	N/A	[108]

Based on the all-inkjet-printed OTFTs, an inverter including load ($W/L = 440 \mu\text{m}/320 \mu\text{m}$) and driver ($W/L = 2,050 \mu\text{m}/80 \mu\text{m}$) OTFTs was designed to be operated with a full-swing mode (Figure 2.20a) [60]. Figure 2.20b, c show typical output voltage (V_{out})–input voltage (V_{in}) transfer curves of TIPS pentacene-based inverters on the untreated and treated surfaces; the A_v is also plotted as a function of V_{in} (see

the insets). For the untreated inverter, a smooth $V_{out}-V_{in}$ inversion tended to shift to the negative direction with increasing V_{DD} (Figure 2.20b). However, the treated systems showed much higher A_v value of 7.17 V/V and maintained a V_{out} value close to 0 V in the negative V_{in} region without a shift of the switching voltage (V_S) (Figure 2.20c). These results were attributed to the PS interlayer-driven improvement in V_{th} , SS , and I_{on}/I_{off} (Table 2.4), as well as a distinguishable ratio of I_{on} between the load and driver OTFTs.

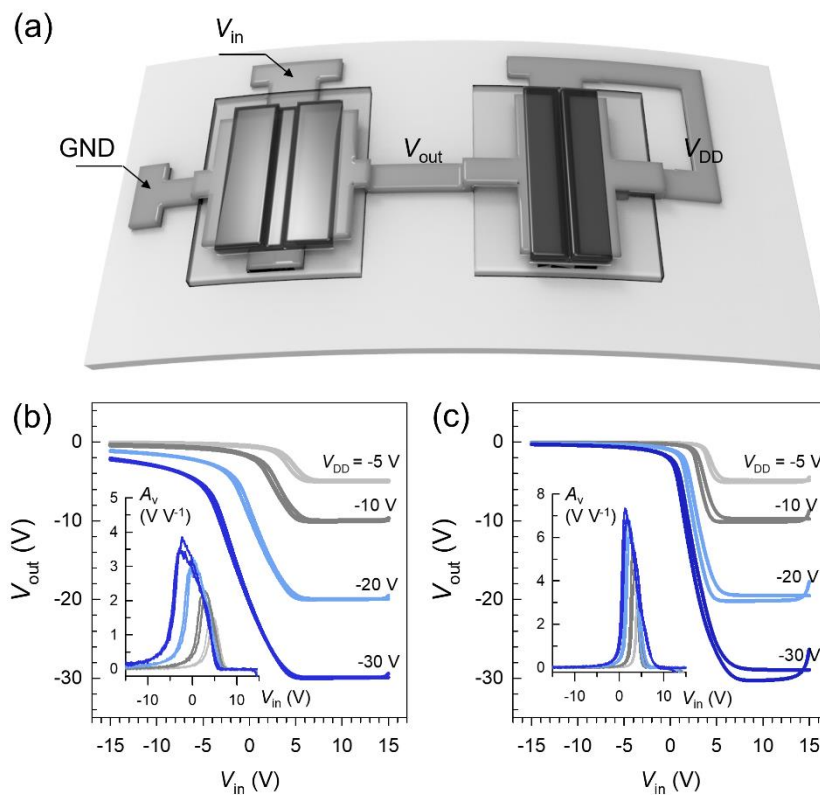


Figure 2.20 | (a) Scheme of an inkjet-printed all-organic inverter on a flexible substrate. Voltage-transfer curves of organic inverters on (b) untreated and (c) treated surfaces. The insets represent the corresponding A_v-V_{in} curves [16].

To characterize the bending stability of these flexible devices on the PS interlayer-introduced surfaces, bending tests were conducted on both the OTFTs and inverters (the inset in Figure 2.21a). During the measurements in a bent state with various R values of 15, 11, 7.5, and 5 mm (Figure 2.21a) and after 1000 bending–relaxation cycles at $R = 5$ mm (Figure 2.21b), no significant changes of electrical characteristics including μ_{FET} , V_{th} , SS , and $I_{\text{on}}/I_{\text{off}}$ were indicated as determined by the $I_{\text{DS}}-V_{\text{GS}}$ transfer curves of the OTFTs. Similarly, the PS interlayer-introduced inverters could maintain the full-swing transition of V_{in} with a slight voltage shift and steady A_{v} values in a bent state with various R values (Figure 2.21c) and after 1000 bending–relaxation cycles at $R = 5$ mm (Figure 2.21d). The $A_{\text{v}}-V_{\text{in}}$ curves are also plotted in the insets.

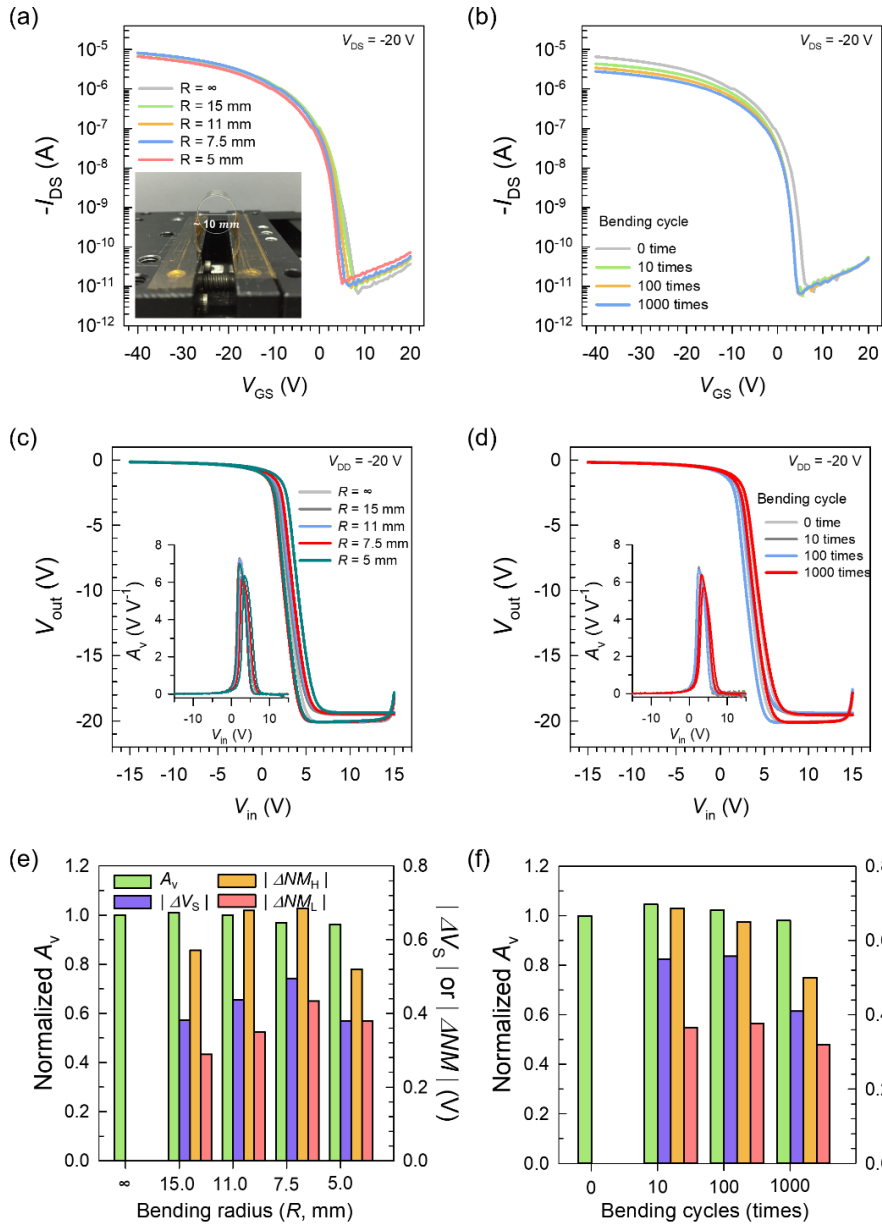


Figure 2.21 | (a, b) I_{DS} - V_{GS} transfer curves of OTFTs and (c, d) V_{out} - V_{in} voltage-transfer curves of organic inverters on the treated surfaces (a, c) in a bent state with various R values and (b, d) after different bending cycles at $R = 5$ mm. The inset in panel a represents an image of the custom-made bending machine used in this study, and the insets in panels c and d represent the corresponding A_v - V_{in} curves. (e, f) Subsequent relative changes in the electrical characteristics of the inverters [16].

Noise margins, the amount of noise that a logic circuit can tolerate, were also investigated to evaluate a sharp inversion in inverter systems (detailed explanation is presented below). The high- and low-level noise margins (referred to as NM_H and NM_L , respectively) were almost maintained after applying tensile stress during the bending tests. Figures 2.21e, f show variations in A_v , V_s , NM_H , and NM_L of the PS interlayer-introduced inverters, before and after bending. Table 2.6 summarizes all the electrical characteristics of the untreated and treated inverters. The electrical properties of the untreated OTFTs and inverters and their variations were severely degraded after bending (Figure 2.22).

Table 2.6 | Variations in the electrical performance of the TIPS pentacene-based inverters on untreated and polymer-treated surfaces, before and after 1000-cycle bending.

Inverters	Bending test	A_v [V/V]	$ \Delta V_S $ [V]	$ \Delta NM_H $ [V]	$ \Delta NM_L $ [V]	V_{out} [V] (at $V_{in} = -15V$)		
Untreated	Before	$R = \infty^a$	3.03 ± 0.09	0	0	0	-0.96 ± 0.18	
		$R = 5 \text{ mm}^b$	2.79 ± 0.06	2.50 ± 0.80	1.88 ± 0.76	2.60 ± 0.79	-1.16 ± 0.07	
	After	$R = \infty$	2.62 ± 0.07	1.45 ± 0.31	1.13 ± 0.28	1.56 ± 0.29	-1.04 ± 0.11	
		$R = \infty$	7.17 ± 0.28	0	0	0	-0.15 ± 0.005	
	Treated	Before	$R = 5 \text{ mm}$	6.90 ± 0.16	0.38 ± 0.05	0.52 ± 0.07	0.38 ± 0.06	-0.15 ± 0.005
			$R = \infty$	7.03 ± 0.23	0.41 ± 0.07	0.50 ± 0.08	0.32 ± 0.03	-0.17 ± 0.005

^ano bent state; ^bin a bent state

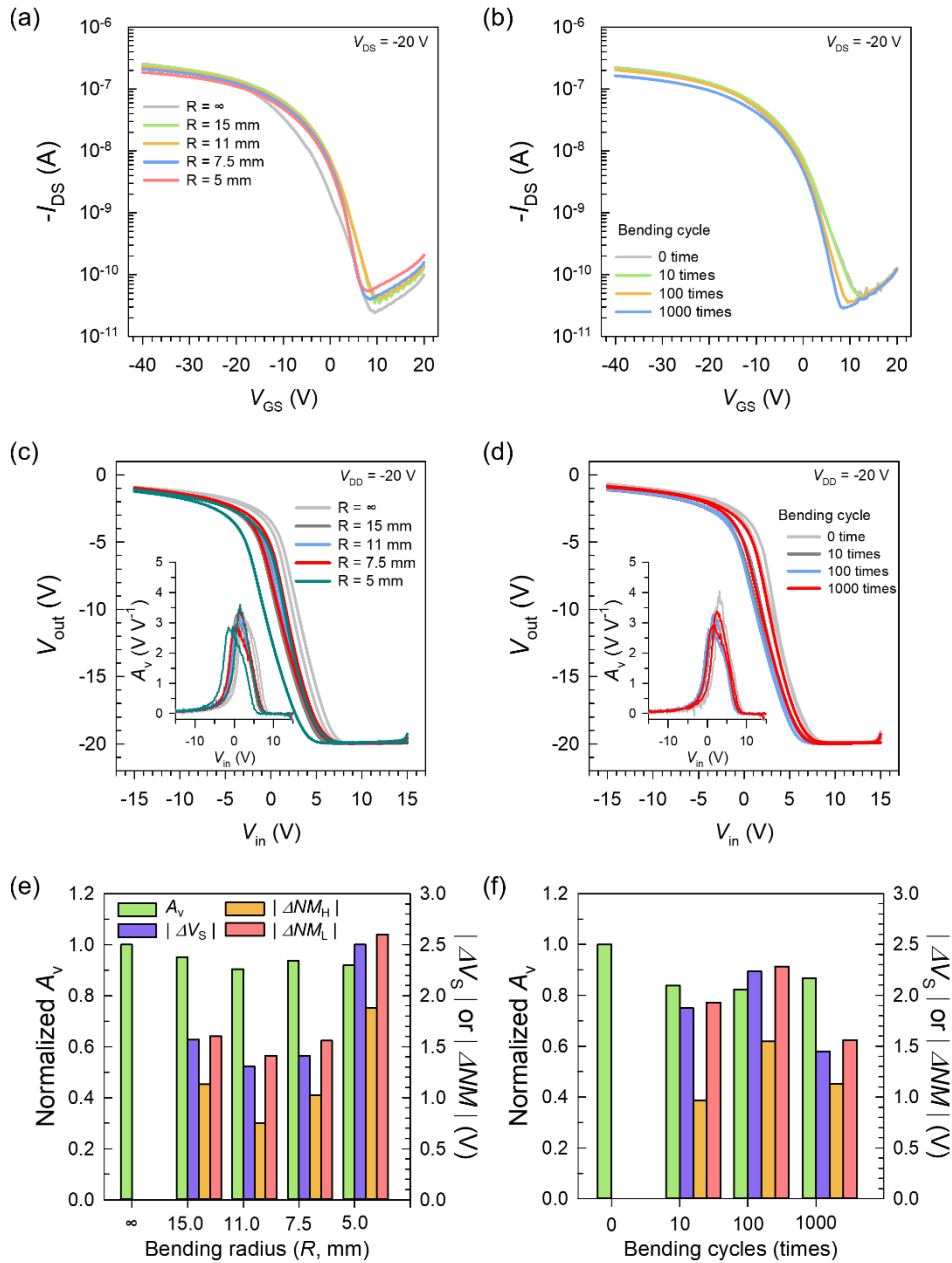


Figure 2.22 | (a, b) I_{DS} - V_{GS} transfer curves of OTFTs and (c, d) V_{out} - V_{in} voltage-transfer curves of organic inverters on the untreated surfaces (a, c) in a bent state with various R values, and (b, d) after different bending cycles at $R = 5$ mm (the insets in (c) and (d) represent the corresponding A_v - V_{in} curves). (e, f) Subsequent relative changes in the electrical characteristics of the inverters [16].

The terminology 'noise' in logic circuits means unwanted variations in voltage or current at logic nodes. If the magnitude of noise is larger than a critical value, known as the noise margin (NM) of the logic circuit, it will cause logic errors. When the noise value is smaller than NM , the noise will be attenuated as it passes from input to output. As a result, NM is used as a factor to specify the range over which the logic circuits will function properly.

For a noiseless system, we can write the equation for an inverter as:

$$V_{out} = f(V_{in}) \quad (2.12)$$

With noise v_n added, a noisy output is produced as:

$$V'_{out} = f(V_{in} + v_n) \quad (2.13)$$

A Taylor series expansion of the output function allows us to examine the important factors determining V_{out} in the presence of noise:

$$V'_{out} = f(V_{in}) + v_n \frac{\partial V_{out}}{\partial V_{in}} + v_n \frac{\partial^2 y}{\partial V_{in}^2} + \dots \quad (2.14)$$

Because the noise is small, higher-order terms could be ignored. Then, the noisy output could be simplified by the noiseless output plus the noise multiplied by A_v of the inverter. Therefore, if the inverter is operated in the region where $|A_v| < 1$, the circuit will attenuate the noise and hold the output in the desired range.

There are two unity gain points, where $A_v = -1$ (Figure 2.23). The two points

are defined as voltage input low (V_{IL}) and voltage input high (V_{IH}). These two unity gain points, the voltage output high (V_{OH}), and the voltage output low (V_{OL}) can be used to define the high- and low-level noise margins (referred to as NM_H and NM_L , respectively) as follows:

$$NM_H = V_{OH} - V_{IH} \quad (2.15)$$

$$NM_L = V_{IL} - V_{OL} \quad (2.16)$$

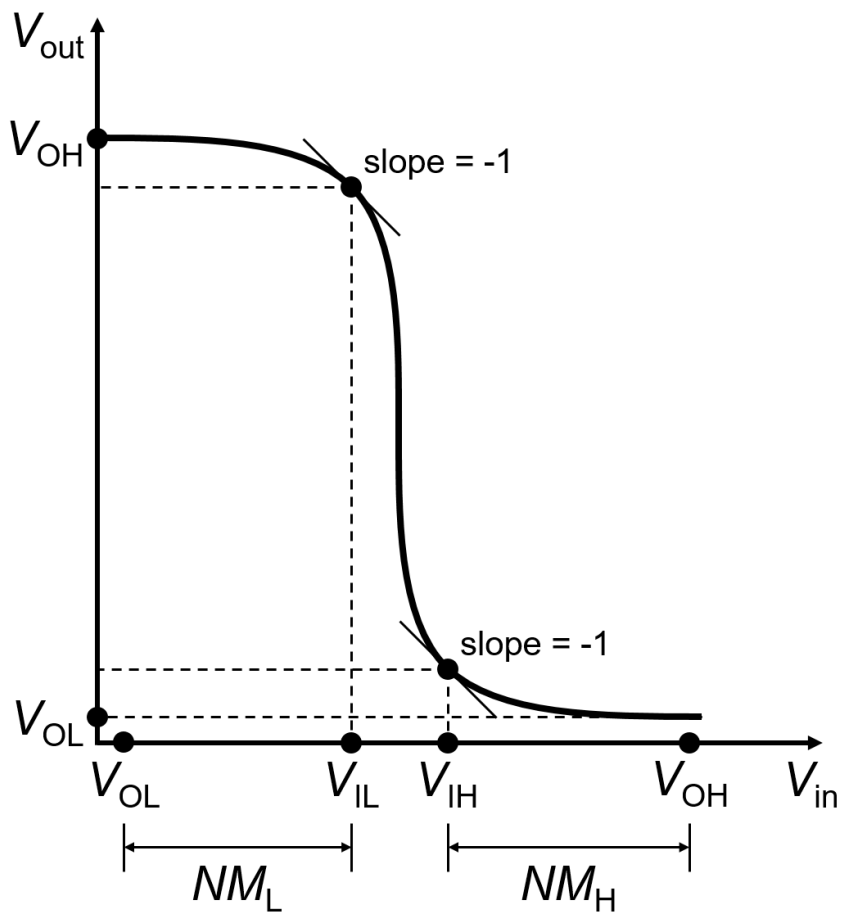


Figure 2.23 | Definition of NM in a voltage – transfer curve [16].

The PS interlayer-assisted inverters yielded not only intrinsically improved electrical characteristics but also maintained highly consistent values in A_v , V_S , NM_H , NM_L , and V_{out} (at $V_{in} = -15$ V) even after bending. It should be noted that consistent V_S , NM_H , and NM_L values of the polymer-treated inverters could be attributed to better semiconductor–dielectric interface with lower N_{SS}^{max} . These results also clearly indicate that the transparent OTFTs and inverters had excellent flexibility and reliability without significant degradation in the electrical characteristics under tensile stress.

2.2.4. Conclusion

We report a simple interface engineering technique for organic-based transparent polymer electrode and dielectric materials, which can be simultaneously modified for binding an end-silane-terminated PS without any preliminary treatment. By using the interface engineering methodology, fully inkjet-printed high performance transparent OTFTs and inverters were fabricated on flexible Arylite substrates. Considering the trade-off between T_L and R_S of printed PEDOT:PSS electrodes, the number of printing passes for gate and S/D electrodes was optimized. The introduction of a polymer interlayer to the electrode and dielectric surfaces could minimize the difference in γ between the PEDOT:PSS electrode and PVP dielectric surfaces. The PS interlayer yielded a significant decrease in interface trap density between the gate dielectric and the semiconductor layer and improved the ordering of the TIPS pentacene semiconductor layer. Moreover, the PS interlayer improved carrier injection from the S/D electrodes to the semiconductor layer without degrading T_L . The improved OTFTs on the treated surfaces showed a high μ_{FET} of $0.27 \text{ cm}^2/\text{V}\cdot\text{s}$ (about 15 times higher than that of the untreated OTFTs), V_{th} of 2.42 V,

SS of 1.16 V/dec, I_{on}/I_{off} of greater than 10^6 , and T_L of 70.0% (at 550 nm). The organic inverters with the PS interlayer also showed an excellent transition near 0 V, while maintaining A_v of 7.17 V/V (at $V_{DD} = -20$ V) during a 1000-cycle bending test at $R = 5$ mm. Because all of the layers consisted of soft polymers, much more stable operation under a tensile stress was possible. We believe all-inkjet-printed, all-organic TFTs and inverters on the facilely introduced surface-matching interlayer provide an attractive path toward the realization of high-performance transparent electronics, e.g., transparent display and sensor applications, on a flexible platform with a low-temperature and low-cost process.

Chapter 3

Photoresponse of Transparent Flexible Single-Walled Carbon Nanotube TFTs

We report all-inkjet-printed, transparent, and flexible single-walled carbon nanotube (SWCNT) thin-film transistors (TFTs) that are highly stable under day-to-day illumination conditions. The SWCNTs showed two different types of photoresponse depending on the power of the light source (high-power laser illumination, low-power fluorescent light, RGB LEDs, halogen lamp, and sunlight). Under high-power laser illumination, the current of the SWCNT TFTs decreased because of the photodesorption of the oxygen molecules near the nanotube networks. On the other hand, unlike common semiconducting materials, the transparent, flexible SWCNT TFTs showed no significant change under halogen light illumination nor under sunlight owing to high binding energy of the excitons inside the one-dimensional SWCNTs. Therefore, we believe that SWCNT-based transparent TFTs/circuits can be employed in the transparent devices as a practical application.

3.1. Introduction

For the practical application of transparent thin-film transistors (TFTs), the changes in their operational conditions under illumination should be negligible. Particularly for display applications, the variation in the driving current of TFTs due to a bright environment can lead to a variation in pixel brightness. In fact, common semiconducting materials, such as organic semiconductors [109], metal-oxides [110, 111], and two-dimensional materials [112], are known to be unstable under illumination. For a stable operation, researchers have tried synthesizing high-bandgap materials [113] or have incorporated additional structures such as plasmonic filters [114]. However, high-bandgap materials exhibit low mobility, and using additional structures increases the fabrication costs.

In this chapter, we report materials that do not undergo changes in their properties even under day-to-day light illumination conditions because they do not contribute to the photocurrent owing to the inherent properties of the material, despite electron-hole pair generation. Unlike common semiconducting materials, single-walled carbon nanotubes (SWCNTs) are very stable under illumination. Such an unusual photoresponse of SWCNTs has been attributed to the high binding energy of the excitons owing to enhanced Coulomb interaction in one-dimensional (1D) materials [115, 116]. Because of the strong quantum confinement of the electron-hole pairs in the quasi-1D nanotube, high exciton binding energies are expected, and the predicted values range from a few tens of milli-electron volts to 1 eV depending on the tube diameter, chirality, and dielectric screening [117-119]. Because the thermal energies at room temperature do not exceed typical exciton binding energies

of SWCNTs, it is difficult to separate the excitons generated inside the SWCNTs into free carriers without applying additional energy. Therefore, the operation of SWCNT TFTs can be changed only using high-power light sources such as a laser. On the other hand, because the operation of SWCNT TFTs does not change under relatively low-power light, such as halogen light and sunlight, SWCNT TFT-based circuits can be used for practical purposes. Furthermore, a SWCNT network is highly stable under bending stress and can be fabricated using a low-temperature, low-cost, and air-ambient solution process, which is an important technology for large-area transparent flexible electronics. We believe that these characteristics of SWCNT TFTs will help to realize of highly stable, transparent, and flexible electronic devices.

We classified SWCNT-based photodetectors based on fundamental photoresponse mechanisms into four types. Subsequently, we studied the different photoreactivities of the SWCNT TFTs under high-power laser and low-power halogen light illumination. When illuminated by a high-power laser, the drain current of the SWCNT TFTs varies because of the photodesorption of oxygen molecules in the vicinity of SWCNT network. The extent of the variation was found to depend on the wavelength and power intensity of the laser. On the other hand, when illuminated by a low-power halogen light or sunlight, the SWCNT TFTs showed no significant change in their operation and thus can be employed for practical applications. Finally, we show that the SWCNT TFTs can be used in transparent display/circuit applications by utilizing the aforementioned properties. We report all-inkjet-printed transparent SWCNT TFTs and an inverter based on the SWCNT TFTs with soluble conductive organic electrodes, the maximum process temperature of which is lower than 180 °C, thus making them compatible with typical flexible substrates. Their electrical characteristics do not undergo significant degradation under halogen light,

sunlight, or mechanical stress, thus providing an attractive path toward realizing highly stable, transparent, and flexible electronic devices, which can be implemented via a low-temperature and low-cost process.

3.2. Experiments

3.2.1. Non-Transparent Device Fabrication

A silicon dioxide (SiO_2) (200 nm)/heavily doped Si substrate was cleaned sequentially using acetone and isopropyl alcohol (IPA) in an ultrasonic bath. Before the active layer was deposited, a poly-L-Lysine (PLL) solution (0.1% (w/v) in H_2O , Sigma-Aldrich Corp.) was drop-cast onto the SiO_2 dielectric layer, followed by rinsing it with deionized (DI) water after 5 min, to promote the adhesion between the gate dielectric and the active layer (Figure 3.1a). For the active layer, a semiconductor-enriched SWCNT solution containing 1 mg of SWCNT powder (99.9%, NanoIntegrus Inc.) and 100 mL of *N*-Methyl-2-pyrrolidone (NMP), was drop-cast onto the PLL-treated substrate, followed by rinsing with toluene after 10 min (Figure 3.1b). The results show a well-formed SWCNT film with a desirable random network in the channel region (see Figure 3.2). Finally, for source/drain (S/D) electrodes, silver ink was inkjet-printed in a single pass with a drop spacing of 45 μm and a drop velocity of 10 m/s (Figure 3.1c). After printing, the S/D electrodes were sintered at 130 $^\circ\text{C}$ for 20 min. The defined channel width and length were 130 and 110 μm , respectively.

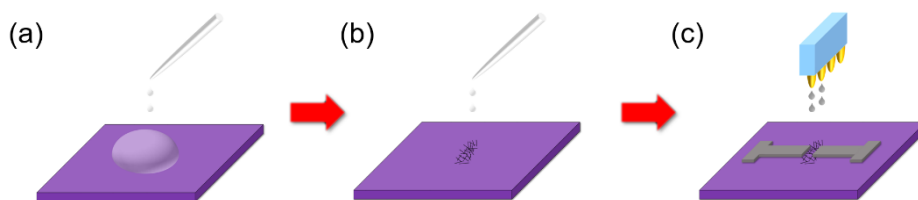


Figure 3.1 | Fabrication procedure of the SWCNT TFTs on a SiO_2/Si substrate.

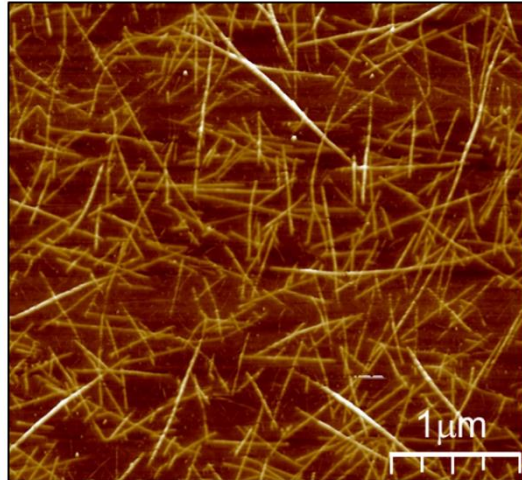


Figure 3.2 | AFM topologies of the SWCNT layers drop-cast on SiO₂ dielectrics from NMP-based solution.

3.2.2. Transparent Device Fabrication

Fully-printed, transparent, and flexible SWCNT TFTs were fabricated onto a 125 μm-thick polyethylene-naphthalate (PEN) substrate with a bottom-gate and top-contact S/D configuration. The substrate was sequentially ultrasonic-cleaned using IPA and DI water. For the transparent gate electrodes, a poly(3,4-ethylenedioxythiophene):polystyrenesulfonate (PEDOT:PSS) ink (1 wt.% in H₂O, Sigma-Aldrich) was inkjet-printed in two passes onto a cleaned substrate with a drop spacing of 40 μm and a drop velocity of 8 m/s and subsequently annealed at 130 °C for 20 min (Figure 3.3a). Onto the PEDOT:PSS gate electrodes, a poly(4-vinylphenol) (PVP) ink, which contains 10 wt.% of PVP powder (the molecular weight ≈ 25,000 g/mol) and 2 wt.% of poly(melamine-co-formaldehyde) (the number-average

molecular weight ≈ 432 g/mol, Sigma-Aldrich) as a cross-linking agent dissolved in propylene glycol methyl ether acetate ($\geq 99.5\%$), was inkjet-printed in a single pass with a drop spacing of $25\ \mu\text{m}$ and a drop velocity of $8\ \text{m/s}$ for the formation of a well-defined gate dielectric layer (Figure 3.3b). It should be noted that to minimize the formation of pin holes on the surface of the cross-linked PVP gate dielectric, ramped curing (ramping at $5\ ^\circ\text{C}/3\ \text{min}$ and sequential soaking at $100\ ^\circ\text{C}$ for $20\ \text{min}$ and at $180\ ^\circ\text{C}$ for $30\ \text{min}$) was conducted [13]. After the same type of PLL treatment (Figure 3.3c) was performed on the PVP dielectric (see Chapter 3.2.1), the semiconductor-enriched SWCNT ink (Isonanotubes-S, 95% purity, Nanointegris Corp.) was three-pass-printed onto the PLL-treated PVP dielectric with a drop spacing of $30\ \mu\text{m}$ and a drop velocity of $16\ \text{m/s}$, followed by rinsing with DI water after each printing pass (Figure 3.3d). A well-formed SWCNT film with a network denser than the film deposited from the NMP-based solution is confirmed (see Figure 3.4). Finally, for depositing the transparent S/D electrodes, a PEDOT:PSS ink was inkjet-printed in a single pass with a drop spacing of $30\ \mu\text{m}$ and a drop velocity of $8\ \text{m/s}$ and subsequently annealed under the same conditions as the gate electrodes (Figure 3.3e). The defined channel width and length were 130 and $80\ \mu\text{m}$, respectively.

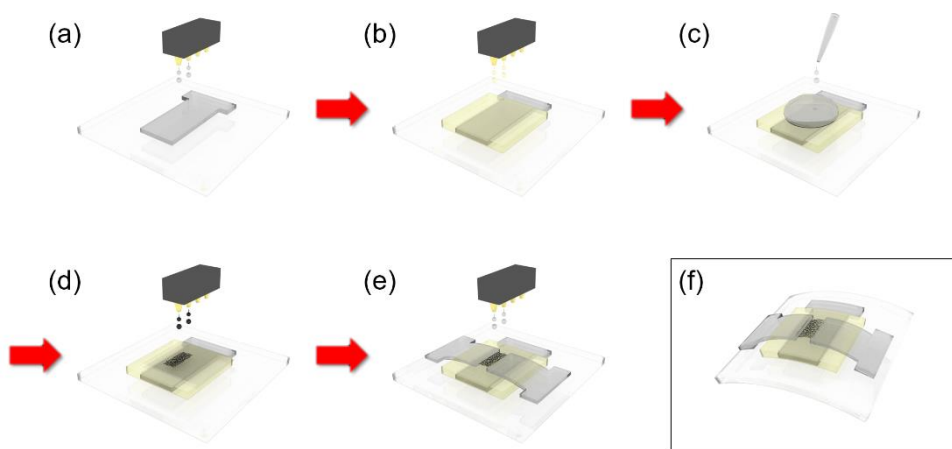


Figure 3.3 | Fabrication procedure of the transparent SWCNT TFTs on flexible PEN substrate.

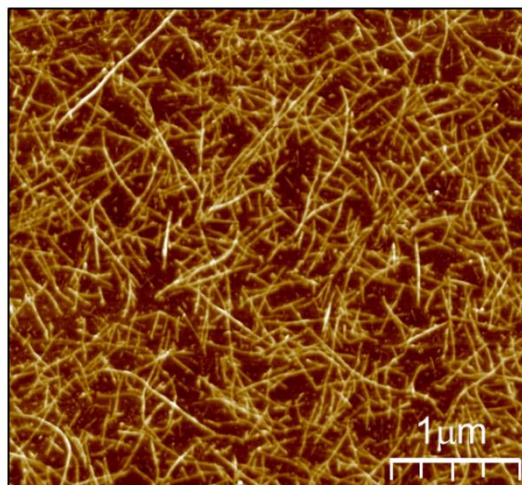


Figure 3.4 | AFM topologies of the SWCNT layers printed on PVP dielectrics from DI water-based ink.

3.2.3. High-Power Laser/Low-Power Light illumination

Laser diodes (MD4560V, MD5240V, and MD7860V for 450, 520, and 780 nm, respectively; DELOS LASER Corp.) were mounted onto the probe station and focused onto the samples. The laser power was measured using an optical power meter (PM160, Thorlabs Inc.). To examine their practical usability, the electrical properties of the all-inkjet-printed transparent SWCNT TFTs were investigated under different illumination conditions via fluorescent lamps, RGB LEDs, a halogen light source (FOK-100W, Fiber Optic Korea Co., Ltd.), and sunlight.

3.2.4. Characterization

The electrical properties of both the non-transparent and transparent SWCNT TFTs were measured using a semiconductor parameter analyzer (4156A, Agilent Technologies). The morphologies of the SWCNT layers were measured using an atomic force microscopy instrument (AFM, XE-100, Park Systems Corp.). The transmittances of the PEN substrate and the overall devices were measured using a spectrophotometer (LAMBDA 35, PerkinElmer Corp.). All the measurements were executed at room temperature in ambient air.

3.3. Results and Discussion

3.3.1. SWCNT TFTs as Photodesorption-Based Photodetectors

In Chapter 3, we report that the electrical properties of SWCNTs do not change under practical lighting conditions. However, in fact, SWCNTs have gained tremendous attention in photodetector applications because they have low bandgap and can absorb even infrared light.

Figure 3.5 shows the previously reported SWCNT-based photodetectors with respect to the power intensity and wavelength of the light used. We classified the SWCNT-based photodetectors based on the fundamental photoresponse mechanism into four types: photoconductors, heterojunction structures, bolometers, and photodesorption-based photodetectors. It should be noted that each category was classified with similar intensity and wavelength. In photoconductors, similar to common semiconductors, the optically generated electron-hole (e-h) pairs are separated in the channel because of the electric fields [120, 121]. However, because of the high binding energy of the e-h pairs in SWCNTs [115, 116], a significantly high-power laser is required to separate them. Furthermore, as it is difficult to obtain sufficient sensitivity with an individual SWCNT, a SWCNT film should be employed instead of an individual SWCNT [122, 123]. In addition, heterojunction structures have been used to effectively separate e-h pairs even under low-power light [122, 124, 125]. When SWCNTs are used as a film, the photothermal effect should be considered, as heat dissipation is suppressed at the intertube junctions [126]. When a SWCNT film is illuminated by high-power sources, the temperature of the film significantly increases because of the low heat capacity, which in turn

changes the conductance of the film [127, 128]. Finally, the photo-excited plasmons in SWCNTs induce hot electrons, which makes the oxygen molecules in the vicinity of SWCNTs to desorb. As oxygen molecules act as p-type dopants in an ambient environment, the reduced transistor current of the SWCNT TFT could be attributed to the photodesorption of the oxygen molecules [129]. It takes several hundreds of seconds for the oxygen molecules to re-adsorb and restore their properties, whereas the response time of the bolometric response is approximately several tens of milliseconds [129]. Considering that our devices showed a response time over hundreds of seconds (see Figure 3.6) and that the power of the light is similar to that of photodesorption-based photodetectors rather than photoconductors, it could be inferred that our devices can exhibit a photodesorption mechanism. Finally, it should be noted the power of sunlight is too low to induce a photoresponse.

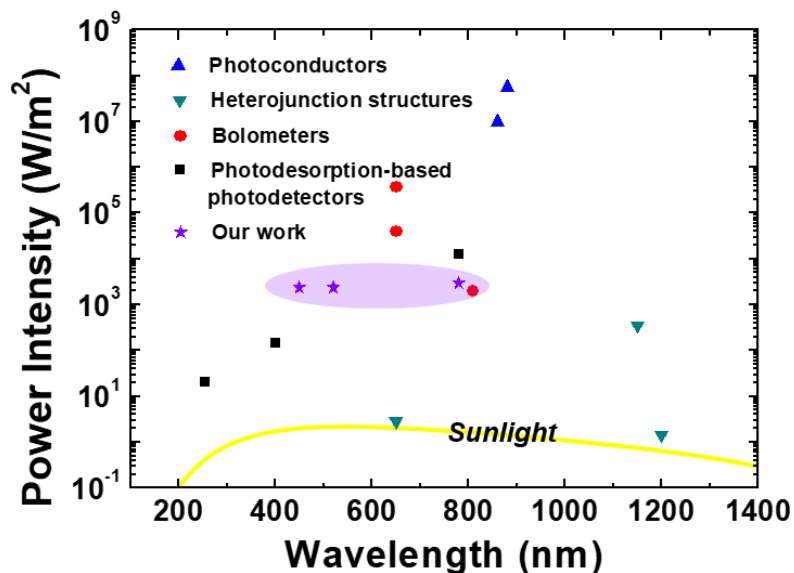


Figure 3.5 | Power intensity and wavelength of SWCNT-based photodetectors.

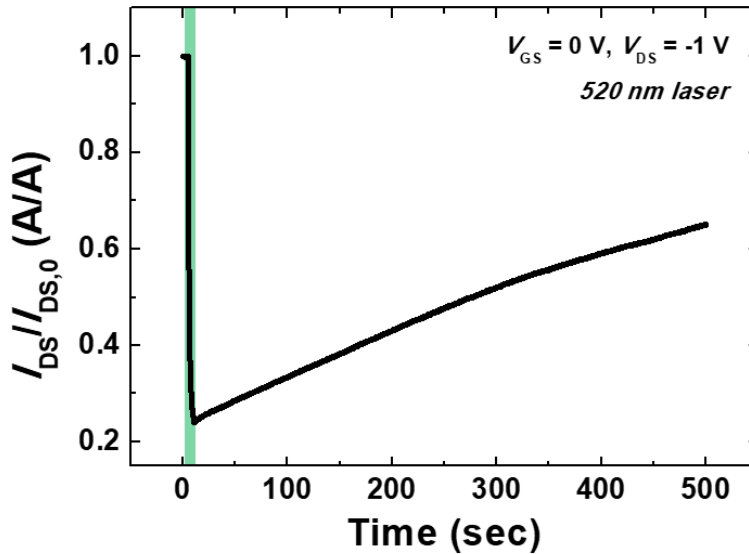


Figure 3.6 | Normalized I_{DS} of the SWCNT TFTs with respect to time during 520 nm laser illumination in air. Note that the shaded and unshaded regions represent the on and off periods of the laser, respectively. Laser power intensity is $\sim 2.4 \text{ kW/m}^2$.

Figure 3.7 shows the photoresponse of the SWCNT TFTs under laser illumination. Figure 3.7 shows that the photoresponse of the SWCNT TFTs depend on the wavelength of the laser. The lower the wavelength of the laser, the greater is the change in the drain current. In addition, the photoresponse of the SWCNT TFTs depends on the intensity of the laser (Figure 3.8). The higher the intensity of the laser, the greater is the change in the drain current. From the low intensity region of Figure 3.8, it also can be seen that the intensity at which drain current decreases depends on the wavelength of the laser. It should also be noted that the PLL layer (Figure 3.9) and S/D electrodes (Table 3.1) were barely affected by laser illumination.

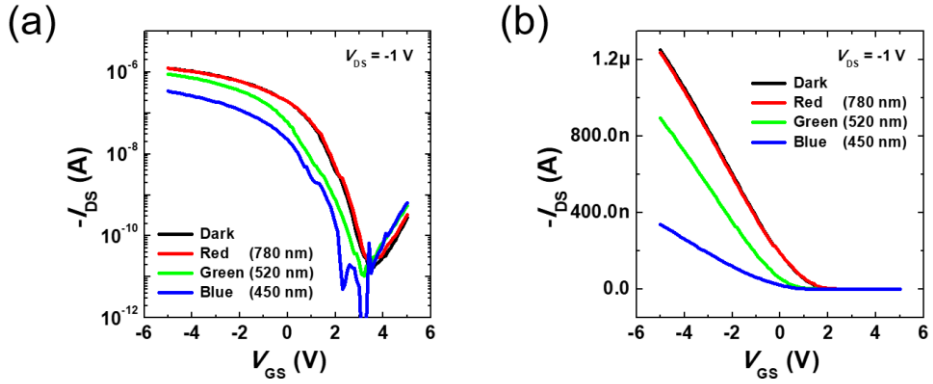


Figure 3.7 | I_{DS} - V_{GS} transfer characteristics of the SWCNT TFTs under laser illumination with various wavelengths (a) in a log scale and (b) in a linear scale. Laser power intensity is fixed at ~ 2.4 kW/m².

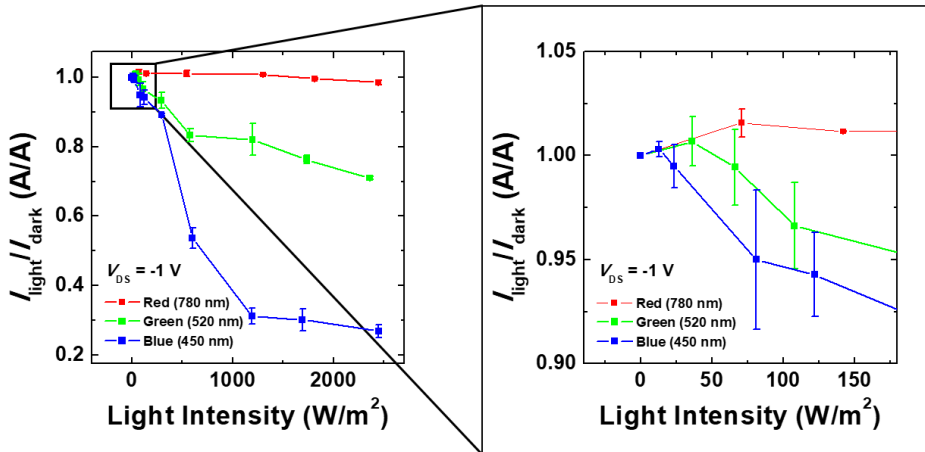


Figure 3.8 | Normalized on-current with respect to wavelength and power intensity.

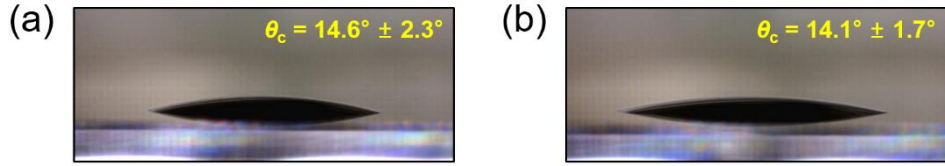


Figure 3.9 | Contact angle measurements of a water droplet on the PLL layers (a) before and (b) after laser illumination (520 nm, $\sim 2.4 \text{ kW/m}^2$).

Table 3.1 | Sheet resistance of silver and PEDOT:PSS electrodes before and after laser illumination (520 nm, $\sim 2.4 \text{ kW/m}^2$).

Electrodes	Normalized sheet resistance	
	Before laser illumination	After laser illumination
Silver	1.00	1.01 ± 0.06
PEDOT:PSS	1.00	1.00 ± 0.02

Unlike under laser illumination, there was no significant change in the electrical characteristics of the SWCNT TFTs under fluorescent light (Figure 3.10a), RGB LEDs (Figure 3.10b), halogen lamp (Figure 3.10c), or sunlight (Figure 3.10d), the emitted powers of which were similar to that of light under day-to-day conditions. On the other hand, the electrical characteristics of both indium gallium zinc oxide (IGZO)-based and poly(3-hexylthiophene) (P3HT)-based TFTs changed drastically even under halogen lamp illumination (Figure 3.11). Therefore, it is expected that transparent SWCNT TFTs could be employed in transparent displays or in circuits as practical applications.

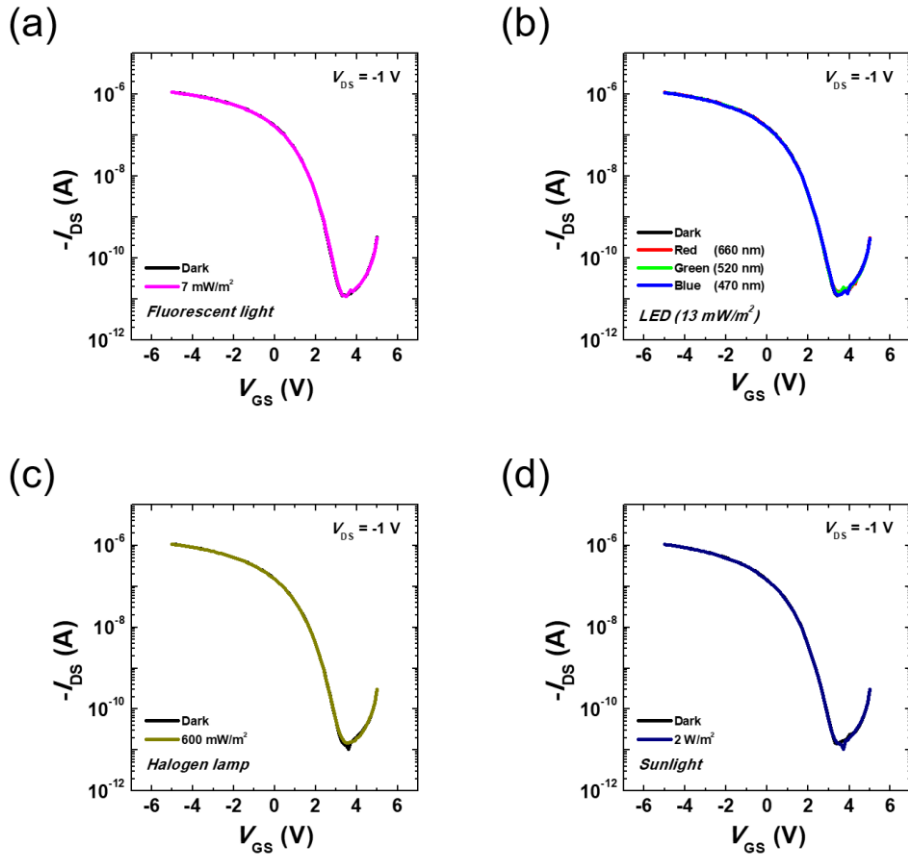


Figure 3.10 | I_{DS} – V_{GS} transfer characteristics of the SWCNT TFTs exposed under (a) fluorescent light, (b) RGB LEDs, (c) halogen lamp, and (d) sunlight.

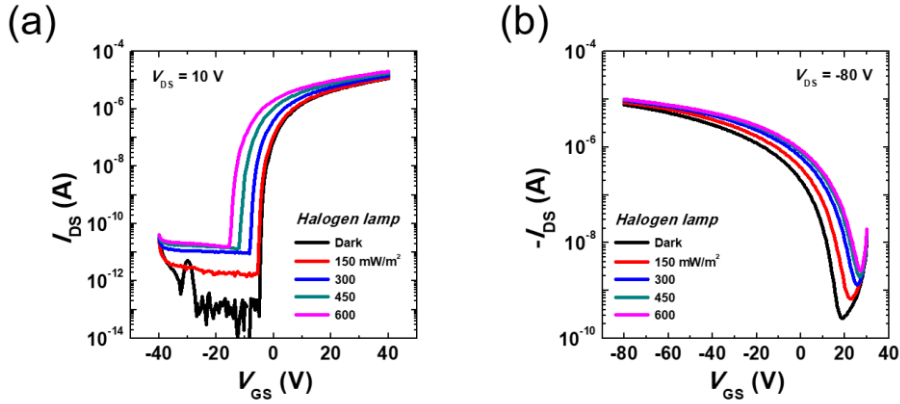


Figure 3.11 | I_{DS} - V_{GS} transfer characteristics of the (a) IGZO and (b) P3HT TFTs under halogen lamp illumination.

3.3.2. Illumination-Stable Transparent Flexible SWCNT TFTs

To investigate the practical usability of transparent and flexible SWCNT TFTs, we fabricated transparent SWCNT-based TFTs onto flexible platforms using all-inkjet-printing process (see Chapter 3.2.2). From Figure 3.12, it can be confirmed that the proposed devices are highly transparent and flexible. The proposed SWCNT TFT showed a transmittance of 79.29% including the substrate with a transmittance of 87.73% (at 550 nm). Furthermore, the device exhibited a transmittance of over 70% within the visible wavelength (400-800 nm) (Figure 3.12b).

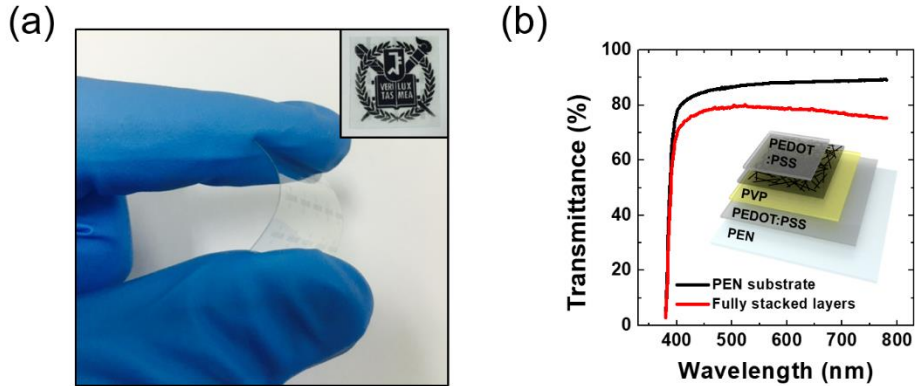


Figure 3.12 | (a) Digital image of the transparent SWCNT TFT arrays. In the inset, the device arrays were placed on a piece of paper with university symbols. (b) Transmittance spectra of 125 μm -thick PEN substrate (black line) and fully stacked films (red line). Inset shows the schematic of the stacked layers (PEDOT:PSS/SWCNT/PVP/PEDOT:PSS/PEN) of our devices.

Figure 3.13 shows the drain current–gate voltage ($I_{\text{DS}}-V_{\text{GS}}$) transfer and drain current–drain voltage ($I_{\text{DS}}-V_{\text{DS}}$) output curves of fully-printed transparent and flexible SWCNT TFTs, respectively. The SWCNT TFTs exhibited a field-effect mobility (μ_{FET}) of $7.01 \text{ cm}^2/\text{V}\cdot\text{s}$ in the linear regime, an on/off ratio ($I_{\text{on}}/I_{\text{off}}$) of $\sim 10^5$, and a subthreshold swing (SS) of $1.50 \text{ V}/\text{dec}$ at a V_{DS} of -1 V . From the output characteristics, it can be inferred that the contact properties between the PEDOT:PSS electrodes and the semiconducting-SWCNT are good, without exhibiting an S -shape. This is because the valence band edge of the SWCNT film [130] is similar to the work function value of the PEDOT:PSS electrode [112]. Understandably, the fully transparent devices exhibited highly stable operation under fluorescent light (Figure 3.14a), RGB LEDs (Figure 3.14b), halogen lamp (Figure 3.14c), and sunlight (Figure

3.14d).

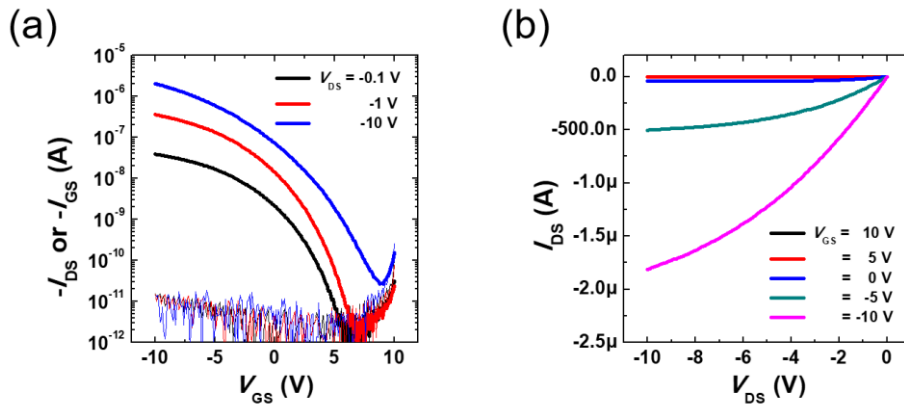


Figure 3.13 | (a) I_{DS} – V_{GS} transfer and (b) I_{DS} – V_{DS} output curves of transparent and flexible SWCNT TFTs.

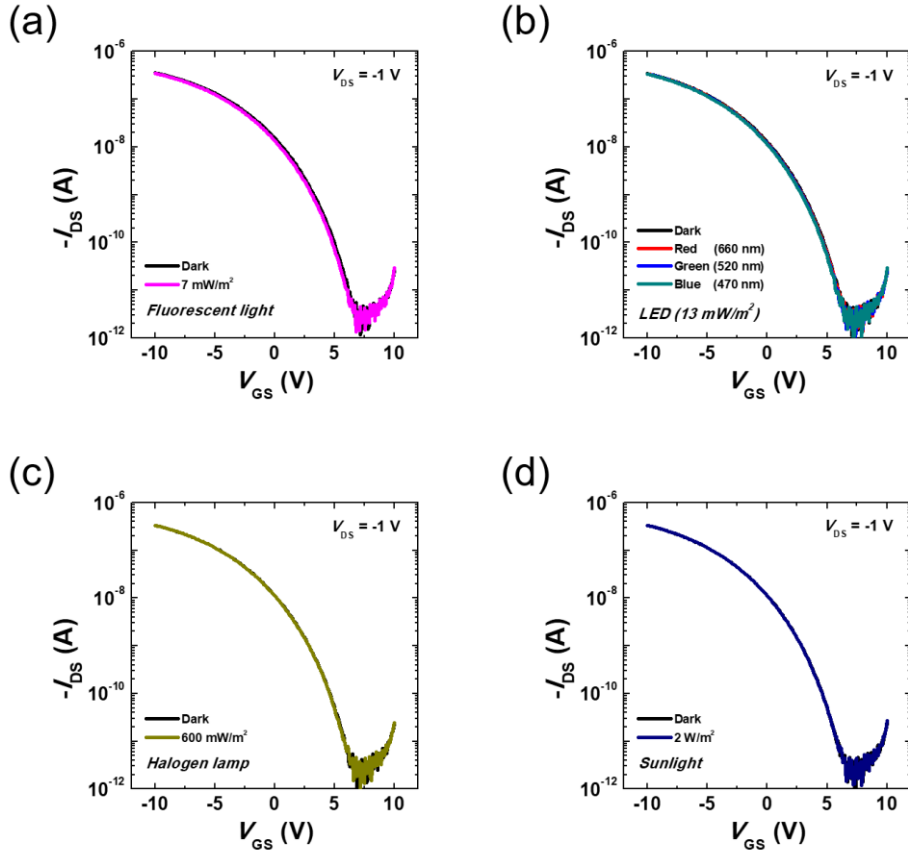


Figure 3.14 | Transfer characteristics of the transparent and flexible SWCNT TFTs exposed under (a) fluorescent light, (b) RGB LEDs, (c) halogen lamp, and (d) sunlight.

A mechanical stress was applied to the all-inkjet-printed transparent SWCNT TFTs using a custom-made bending machine (see Figure 3.15a). The flexibility of the devices was verified by carrying out two types of bending tests. First, the transfer characteristics of the SWCNT TFTs were measured in a bent state with several bending radius (R) values (see Figure 3.15b). Subsequently, they were measured after 1000 cycles of bending with R of 5 mm (see Figure 3.15c). In addition, the

SWCNT TFTs exhibited a highly stable operation during the bending tests. This results confirms that the fully-printed transparent SWCNT TFTs are highly stable and reliable under mechanical stress conditions.

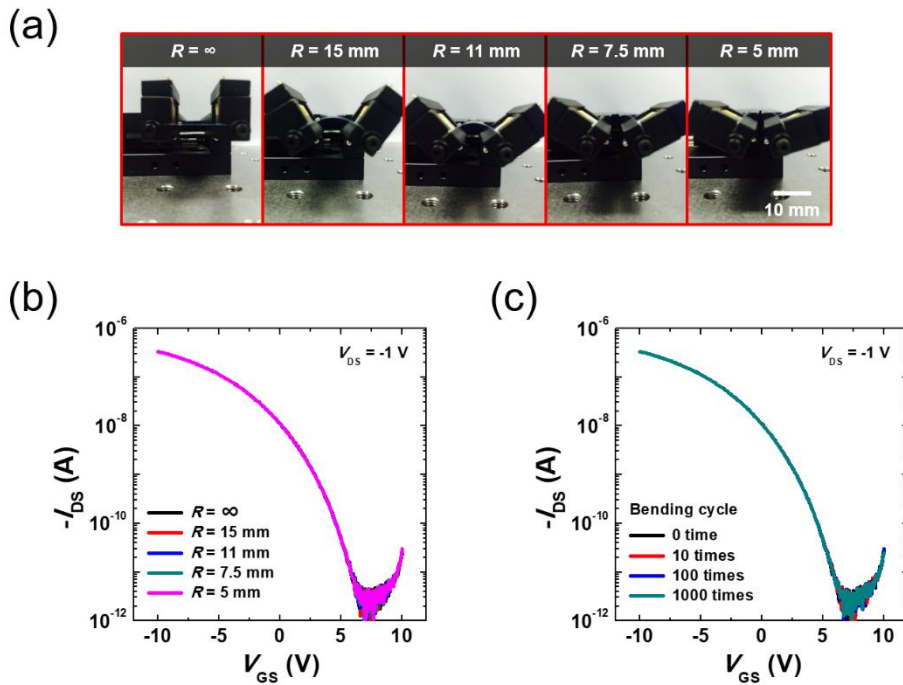


Figure 3.15 | (a) Image of the custom-made bending machine used with different R values. I_{DS} – V_{GS} transfer curves of the transparent and flexible SWCNT TFTs (b) in a bent state with various R values and (c) after different bending cycles at $R = 5$ mm.

Based on the all-inkjet-printed SWCNT TFTs, an inverter, including a load ($W/L = 130 \mu\text{m}/120 \mu\text{m}$) and a driver ($W/L = 530 \mu\text{m}/80 \mu\text{m}$), based on the SWCNT TFTs was designed to be operated in a full-swing mode. Figure 3.16a shows the typical output voltage (V_{out})–input voltage (V_{in}) transfer curves of the SWCNT-based

inverters. Figure 3.16b shows the corresponding voltage gain ($A_v = \partial V_{out}/\partial V_{in}$) as a function of V_{in} . The inverter exhibited an A_v value of 10.21 V/V (at supply voltage (V_{DD}) of 10 V) and maintained V_{out} close to 0 V in the positive V_{in} region and close to V_{DD} in the negative V_{in} region.

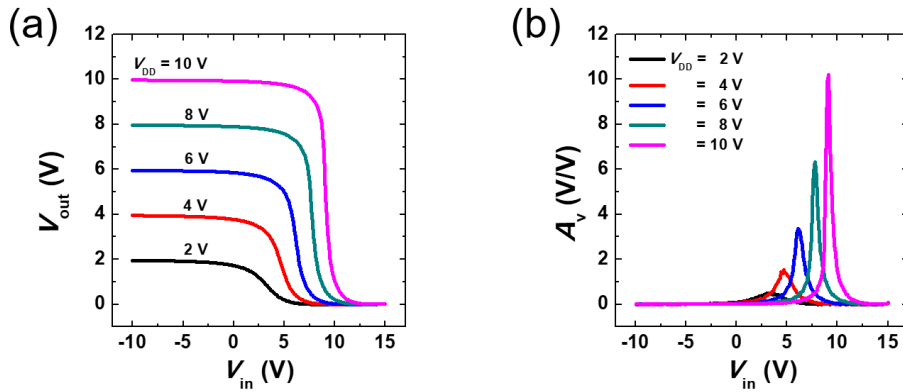


Figure 3.16 | (a) V_{out} - V_{in} voltage-transfer curves of a SWCNT-based inverter. (b) Corresponding A_v - V_{in} curves.

Finally, the operation of the transparent flexible inverter was measured in real time under halogen lamp illumination with V_{DD} of 10 V (Figure 3.17a, b). No significant change in the operation of the two inputs is observed before or after the light illumination. When the input is logic “1”, the output is “0” regardless of whether the halogen lamp is turned off and on. On the other hand, when the input is “0”, the output value is always “1” (Figure 3.17c).

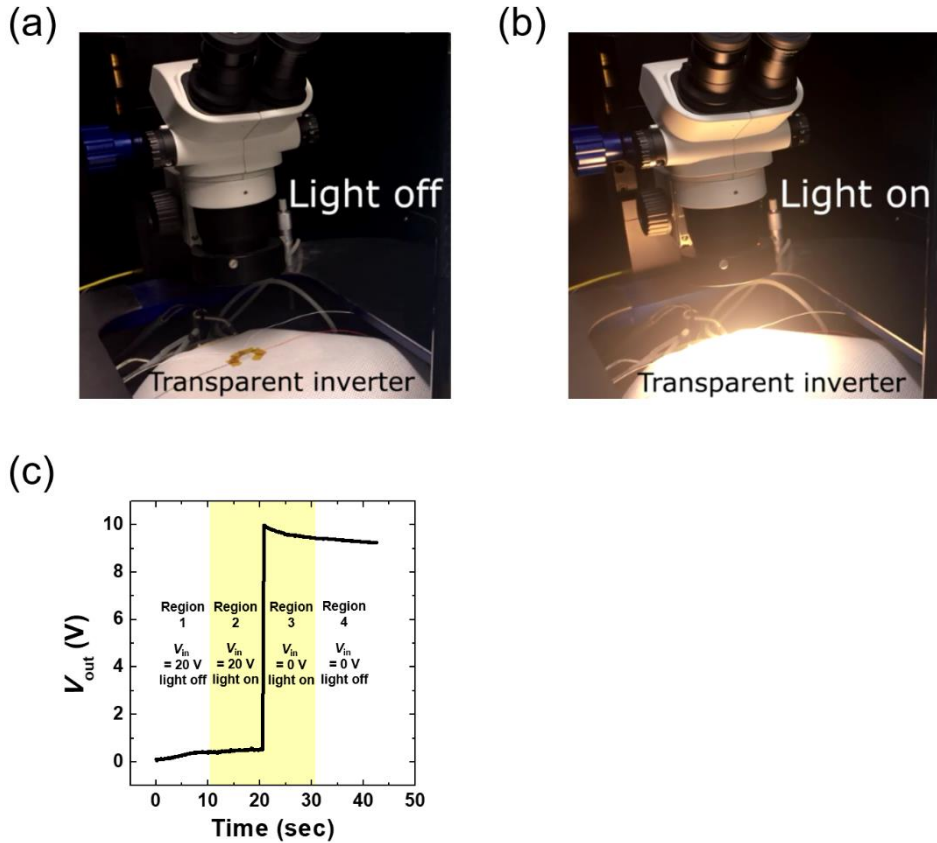


Figure 3.17 | (a, b) Halogen lamp illumination on the transparent SWCNT inverter: (a) off and (b) on state. (c) V_{out} of the inverters with respect to time during halogen lamp illumination in air. Note that Regions 1 and 2 and Regions 3 and 4 represent V_{in} values of 20 V and 0 V, respectively. It is also noted that the shaded (Regions 2 and 3) and unshaded (Regions 1 and 4) regions represent the on and off periods of the halogen lamp, respectively.

3.4. Conclusion

In this chapter, fully-inkjet-printed, transparent SWCNT TFTs were fabricated on a flexible PEN substrate. The transparent SWCNT TFTs exhibited a transmittance of 79.29% (at 550 nm), μ_{FET} of $7.01 \text{ cm}^2/\text{V}\cdot\text{s}$ in the linear regime, $I_{\text{on}}/I_{\text{off}}$ of $\sim 10^5$, and SS of $1.50 \text{ V}/\text{dec}$. The inverters based on the SWCNT TFTs exhibited an excellent A_v of $10.21 \text{ V}/\text{V}$ (at $V_{\text{DD}} = 10 \text{ V}$), showing an excellent transition near V_{DD} . Under high-power laser illumination, the current of the SWCNT TFTs decreased because of photodesorption of the oxygen molecules near the nanotube networks. On the other hand, under low-power light illumination (fluorescent light, RGB LEDs, halogen lamp, and sunlight), the power of which is similar to that of light in daily life, the changes in the electrical characteristics of the SWCNT TFTs were negligible, opening the possibility to use them in practical applications such as transparent displays or circuits. In addition, the electrical characteristics were maintained during a 1000-cycle bending test with R of 5 mm , ensuring high stability and reliability under mechanical stress. We believe that the all-inkjet-printed, transparent, and flexible SWCNT TFTs have excellent potential for realizing highly stable, transparent, and flexible electronic devices, which can be implemented via a low-temperature and low-cost process.

Chapter 4

Transparent Flexible MoS₂

Phototransistors

In this chapter, we report fully printed transparent chemical vapor deposition-synthesized monolayer molybdenum disulfide (MoS₂) phototransistor arrays on flexible polymer substrates. All the electronic components, including dielectric and electrodes, were directly deposited with mechanically tolerable organic materials by inkjet-printing technology onto transferred monolayer MoS₂, and their annealing temperature of <180 °C allows the direct fabrication on commercial flexible substrates without additional assisted-structures. By integrating the soft organic components with ultrathin MoS₂, the fully printed MoS₂ phototransistors exhibit excellent transparency and mechanically stable operation. We believe these strategies can be utilized to realize transparent and flexible two-dimensional electronics using low-temperature, large-area, and low-cost processes.

4.1. Introduction

In recent years, two-dimensional (2D) transition metal dichalcogenides (TMDCs) have attracted considerable attention as an emerging semiconductor for realizing field-effect transistor (FET), sensor, and optoelectronic applications due to their atomic thickness, high surface-to-volume ratio, tunable band gap, etc [41, 46, 131-135]. Specifically, ultrathin monolayer molybdenum disulfide (MoS_2) is one of the promising channel materials in optoelectronics devices, such as photosensors, photodetectors, and photodiodes [136-143]. However, it is still difficult to produce large-area monolayer TMDC films, by widely used top-down methods, such as mechanical exfoliation [47], thinning [144], and liquid intercalation [145]. In this regard, many bottom-up synthesis methods, including metal-organic chemical vapor deposition [146], physical vapor deposition [147], and atomic layer deposition (ALD) [148] have been reported to realize large-area optoelectronic devices. Among these candidates, the one-step chemical vapor deposition (CVD) method has been widely used to yield high-quality and large-area MoS_2 films [149-151]. CVD-synthesized MoS_2 films allow atomically thin, uniform, and large-area semiconducting properties with a direct band gap energy of 1.9 eV [149-151] and thus offer promising opportunities in high performance wearable optoelectronics.

However, other electronic components, including electrodes and dielectric layers, have been typically deposited with inorganic materials using ALD, thermal evaporation, and electron beam evaporation, which are not compatible with large-area flexible platforms. Specifically, unnecessary procedures, such as a photoresist deposition or ultraviolet exposure, can degrade the electrical characteristics of MoS_2

channel layers. Recently, the use of graphene electrodes or hexagonal boron nitride dielectric layers to introduce dangling bond free interfaces on MoS₂ has been suggested [152, 153]. However, these layers require complicated and time-consuming etching and transferring processes with additional supporting layers. Therefore, an approach to implement functional layers on flexible platforms is highly desirable for large-area MoS₂ applications. Furthermore, to fully utilize the excellent transparency and flexibility of monolayer MoS₂, the use of transparent organic materials is an attractive strategy to implement electronic components on flexible platforms.

Herein we fabricated flexible and transparent MoS₂ phototransistor arrays with all-organic components using drop-on-demand inkjet-printing technology. The CVD-synthesized monolayer MoS₂ channel layers were transferred onto flexible and transparent substrates using a polymer-assisted transfer method. Highly transparent organic electrodes and dielectric layers were directly deposited on the defined MoS₂ channel layer using cost-effective inkjet-printing technology without masks or assisted layers [48, 154-156]. By integrating ultrathin MoS₂ and mechanically tolerable organic layers, the printed transparent phototransistors exhibited good stability under repetitive bending cycle tests. By conducting the carefully optimized printing processes, the fabricated fully printed phototransistors exhibited comparable photocharacteristics, including photoresponsivity and external quantum efficiency (EQE), to those of previously reported phototransistors with inorganic components fabricated by conventional photolithographic processes on rigid silicon dioxide (SiO₂)/silicon (Si) substrates.

4.2. Experiments

4.2.1. Device Fabrication Process

Figure 4.1 shows the device fabrication process. The monolayer MoS₂ film was CVD-grown on SiO₂ (270 nm)/Si substrates (Figure 4.1b). The synthesized MoS₂ was patterned using reactive ion etching (RIE) while covered with a shadow mask to form the channel layers (Figure 4.1c, d). After a poly(methyl methacrylate) (PMMA) supporting layer was deposited by spin-coating on MoS₂/SiO₂ (Figure 4.1e), a REVALPHA thermal tape (Nitto Denko, Japan) was attached as a supporting layer. Then, the whole structure (tape/PMMA/MoS₂/SiO₂) was immersed into a potassium hydroxide (KOH) solution (~25%) at 70 °C to detach the tape/PMMA/MoS₂ structure from the SiO₂/Si substrates (Figure 4.1f) [157]. The tape/PMMA/MoS₂ structure was placed onto the polyethylene–naphthalate (PEN) substrate using isopropyl alcohol (IPA) as an adhesion promoter, and then the PMMA supporting layer was carefully removed (Figure 4.1g). Finally, the poly(3,4-ethylenedioxythiophene) polystyrenesulfonate (PEDOT:PSS) electrodes and cross-linked poly(4-vinylphenol) (PVP) dielectric layers were directly inkjet-printed without surface treatment (Figure 4.1h-k). Note that the device yield is not high at this stage because of relatively low yield in the PMMA-assisted transfer processes for large-area monolayer MoS₂ films, even though the inkjet-printing processes were carefully optimized.

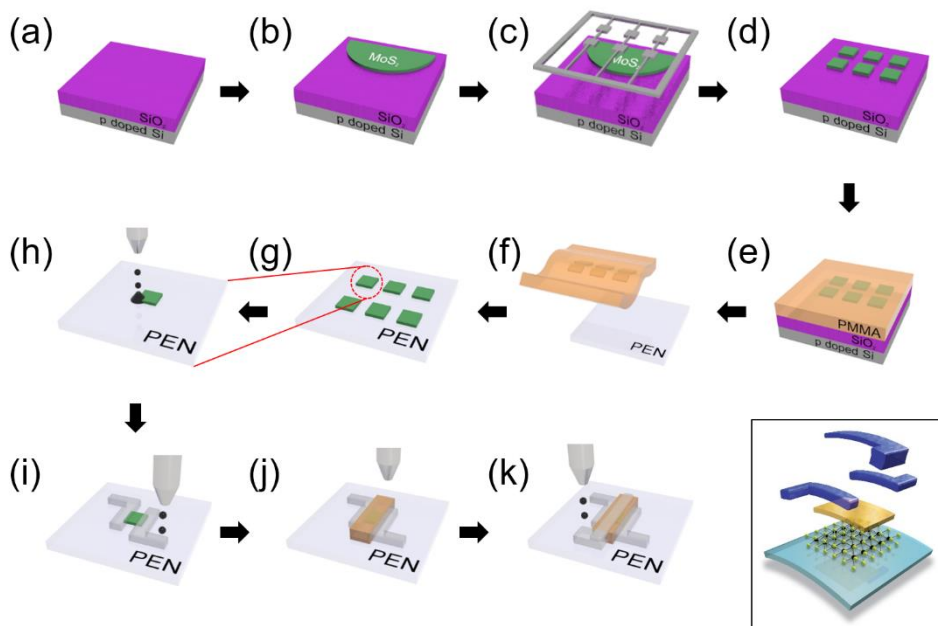


Figure 4.1 | (a) Cleaned the SiO₂/Si substrate. (b) CVD-grown MoS₂ on the SiO₂/Si substrate. (c) MoS₂ patterning process using RIE while covered with a shadow mask. (d) Clearly patterned monolayer MoS₂ film. (e) Spin-coated the PMMA supporting layer onto MoS₂/SiO₂. (f) After detaching the monolayer MoS₂ film from SiO₂ using a KOH solution, the MoS₂/PMMA structure was placed on the PEN substrate. (g) Transferred the MoS₂ onto the PEN substrate. Direct inkjet-printing of (h-i) PEDOT:PSS S/D electrodes, (j) PVP dielectric layer and (k) PEDOT:PSS gate electrodes [112].

4.2.2. MoS₂ Thin Film Synthesis

A dual-heating zone CVD system was used for synthesizing monolayer MoS₂ films. Two crucibles were placed in a quartz tube. One crucible that contained the sulfur (S) powder (99.5%, Sigma-Aldrich) was heated to ~ 200 °C, and the other crucible

that contained the molybdenum trioxide (MoO_3) powder (99.98%, Sigma-Aldrich) and SiO_2 substrate was heated to ~ 700 °C. Ar gas was used as a carrier gas.

4.2.3. Optimization of PMMA Supporting Layer Removal Process

Unfortunately, the wet transfer process produces the PMMA residues on atomically thin MoS_2 samples, which can be a factor to degrade the electrical characteristics. We measured the surface topography using an atomic force microscopy (AFM) (see Figure 4.2a). From the AFM result, it makes no significant differences in the surface roughness (~ 0.6 nm) before and after the PMMA assisted transfer process. As depicted in Figure 4.2b, the PMMA residues were not removed completely by the conventional PMMA removing method by rinsing with acetone. Therefore, additional procedures as described below were required to suppress the leakage current (I_{GS}) by eliminating the PMMA residues completely.

The PMMA/ MoS_2 /PEN structure was immersed into 70 °C acetone and IPA for 2 h. Then, the structure was annealed in a tube furnace for 4 h with 100 sccm Ar gas flow rate, which corresponds to a few mTorr in pressure. Finally, the structure was immersed again into acetone at 70 °C for 1 h. It should be noted that the well-known PMMA eliminating methods that use ultraviolet oxygen exposure or reactive ion etching cannot be employed in this work because these treatments can easily physically damage the MoS_2 monolayer.

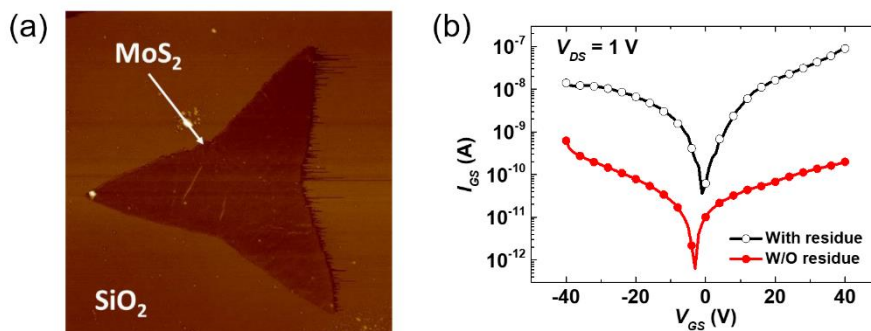


Figure 4.2 | (a) AFM image (scan size = $13 \mu\text{m} \times 13 \mu\text{m}$) of a CVD -grown MoS₂ triangular island after the PMMA-assisted transfer process. (b) Suppressed I_{GS} of the MoS₂ phototransistors after removing the PMMA supporting layer using the optimized process with (black line) and without (red line) the PMMA residue [112].

4.2.4. Inkjet-Printing for Organic Electrodes and Dielectric Layers Formation

The patterned CVD-synthesized monolayer MoS₂ film was transferred onto a transparent and flexible PEN substrate. It should be noted that the expression, “fully printed” can be widely accepted from direct printing via nozzles to the polymer-assisted transfer methods. Then, all the other components, including transparent conductive polymer electrodes and dielectric layers, were deposited by an inkjet-printing technique without any surface treatment under ambient conditions. For the source/drain (S/D) electrode formation, PEDOT:PSS ink (1 wt.% in H₂O, Sigma-Aldrich) was inkjet-printed in one pass on the MoS₂-transferred PEN substrate with a drop spacing of $40 \mu\text{m}$ and a drop velocity of 10 m/s at room temperature using an inkjet printer (DMP-2831, Dimatix Corp., Fujifilm, USA). After printing, they were

annealed at 130 °C for 30 min in an atmospheric environment. It should be noted that 2 wt.% of fluorosurfactant Zonyl FS-300 (Sigma-Aldrich Corp.) was added to the PEDOT:PSS ink to improve both the conductivity and ability to withstand tensile strain [17]. The defined channel width and length were 400 and 100 μm , respectively. On the inkjet-printed PEDOT:PSS S/D electrodes and transfer-printed MoS_2 channel layer, a PVP solution, which contained 10 wt.% of PVP powder (the molecular weight $\approx 25,000$) and 2 wt.% of poly(melamine-co-formaldehyde) as a cross-linking agent dissolved in propylene glycol methyl ether acetate ($\geq 99.5\%$), was inkjet-printed in two passes with a drop spacing of 25 μm and a drop velocity of 8 m/s for the formation of a well-defined gate dielectric layer. To minimize the formation of pin holes on the surface of the cross-linked PVP gate dielectric, ramped curing (ramping at 5 °C/3 min and sequential soaking at 100 °C for 20 min and 180 °C for 30 min) was conducted [13]. Finally, for the gate electrode formation, the same PEDOT:PSS ink added to 2 wt.% of Zonyl FS-300 was inkjet-printed onto the gate dielectric layer in two passes with the same printing and annealing conditions used for the formation of the S/D electrodes. The thicknesses of the device components were 125 μm , 1 μm , and 100 ~ 180 nm for the PEN substrate, PVP dielectric layer, and PEDOT:PSS contact electrodes, respectively.

4.2.5. Resolution of the Inkjet-Printed PEDOT:PSS Electrodes

In our inkjet-printing system, two kinds of ink cartridges which can eject 1 picoliter (pL) and 10 pL volume of ink droplets are available. As you can see in Figure 4.3, if a 1 pL cartridge is used, 30 μm -wide PEDOT:PSS source/drain electrodes having a minimum channel length of $\sim 15 \mu\text{m}$ could be printed onto the CVD-grown MoS_2 film. However, to achieve the reasonable electrical conductivity of a printed PEDOT:PSS electrode comparing to that of other reported transparent electrodes, PEDOT:PSS ink should be printed in multiple passes if a 1 pL cartridge is used because of its relatively high electrical resistivity ($\sim 4.72 \times 10^{-3} \Omega\cdot\text{cm}$). It should be noted that the thicknesses of PEDOT:PSS electrodes printed in 1 pass using 10 pL and 1 pL are 110 nm (Figure 4.4a) and 60 nm (Figure 4.4b), respectively. In other words, at least 2 passes printing is required to achieve the comparable electrical conductivity if a 1 pL cartridge is used. However, due to the limited resolution of our inkjet-printer (repeatability: $\pm 25 \mu\text{m}$ in the spec sheet from Fujifilm Corp.), it is still difficult to stack printed electrodes perfectly in the multi-pass printing process. Furthermore, the PEDOT:PSS source/drain electrodes printed using 10 pL and 1 pL cartridges had a root-mean-square (rms) surface roughness of 3.53 nm (Figure 4.4c) and 6.97 nm (Figure 4.4d), respectively, in a scan area of $10 \mu\text{m} \times 10 \mu\text{m}$ which is a critical parameter in the top-gate device structure to minimize the leakage current between the gate and S/D electrodes.

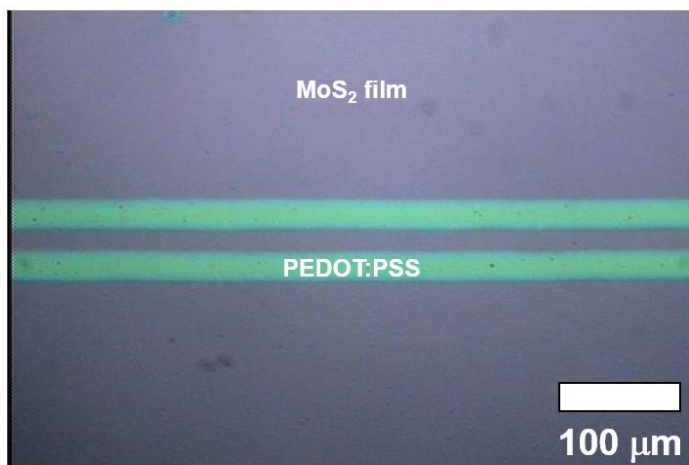


Figure 4.3 | Optical microscopic image of printed PEDOT:PSS S/D electrodes with minimum width and channel length using 1 pL cartridge onto a CVD-grown MoS₂ film [112].

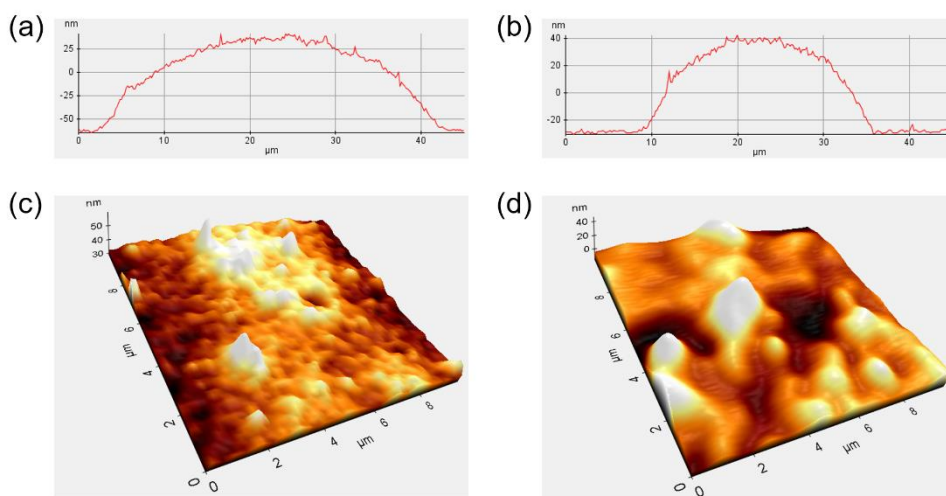


Figure 4.4 | Cross-sectional profiles of printed PEDOT:PSS electrodes using (a) 10 pL and (b) 1 pL cartridge onto a CVD-grown MoS₂ film. AFM topography images of printed PEDOT:PSS electrodes using (c) 10 pL and (d) 1 pL cartridge onto a CVD-grown MoS₂ film [112].

As aforementioned, we can also reduce a channel length up to 15 μm with our best if a 1 pL cartridge is used. However, due to the resolution-limitation of the inkjet-printer (repeatability: $\pm 25 \mu\text{m}$ in the spec sheet from Fujifilm Corp.), the deviation of the channel length was quite large ($\sim 20 \mu\text{m}$). Therefore, the optimized channel length was designed to 100 μm that can be routinely printed using our inkjet-printing system.

4.2.6. Experimental Conditions for Evaluating the Photocharacteristics

Monochromatic lasers with wavelengths of 405, 520, 658, and 780 nm were used (MDE4060V, MDE5240V, MDE6595V, and MDE7860V, respectively, Su Semiconductor) to investigate the photocharacteristics. All electrical characteristics of our MoS_2 phototransistors were measured using a semiconductor parameter analyser (Keithley 4200) and an individual monochromatic light with intensities ranging from 0.1-1000 W/m^2 .

4.3. Results and Discussion

Figure 4.5a schematically illustrates the device fabrication processes. First, a large-area monolayer MoS₂ film was synthesized with MoO₃ and S powders in the presence of Ar carrier gas [48]. The heating temperatures were 700 and 200 °C for MoO₃ and S powders, respectively. Then, the MoS₂ film synthesized on the SiO₂/Si substrate was patterned using a RIE system in an O₂ plasma. To define the channel region, the MoS₂ film was covered with a shadow mask. The patterned CVD-synthesized MoS₂ film was transferred onto a PEN substrate using the PMMA-assisted transfer method [157]. After attaching thermal tape as a supporting layer, the entire structure (supporting tape/PMMA/MoS₂/SiO₂/Si) was immersed in a potassium hydroxide solution (~25%) to detach the MoS₂ film from the SiO₂/Si substrate. Then, all the other components, including dielectric and electrodes, were inkjet-printed onto the patterned MoS₂ array without any surface treatments under ambient conditions. Specifically, PEDOT:PSS S/D electrodes, a cross-linked PVP gate dielectric layer, and a PEDOT:PSS top-gate electrode were sequentially inkjet-printed on the desired positions of the device substrate. The maximum processing temperature of 180 °C facilitated the direct integration of a wide range of printable organic materials onto the flexible substrate. It should be noted that the ultrathin MoS₂ channel layer was extremely sensitive to the surface roughness of underlying layers; therefore, a top-gate configuration was employed in this work because of the relatively poor surface roughness of the inkjet-printed PVP gate dielectric (rms roughness of ~4 nm) compared with that of the PEN substrate (rms roughness of ~1 nm). The contact properties of the PEDOT:PSS and PVP inks on the MoS₂ film

and PEN substrate were optimized with a consideration of the ink chemistry that allowed well-defined printed layers while preventing undesirable dewetting issues on the underlying layers (Figure 4.5b). Owing to the use of ultrathin MoS₂ and transparent organic layers, the fully integrated phototransistors exhibited high transparency (Figure 4.5c). Photographic images of our devices are shown on a piece of paper (left, Figure 4.5c) and in front of a building (right, Figure 4.5c). In particular, the laser-light transmitted the entire device structure without reflection or scattering (Figure 4.5d).

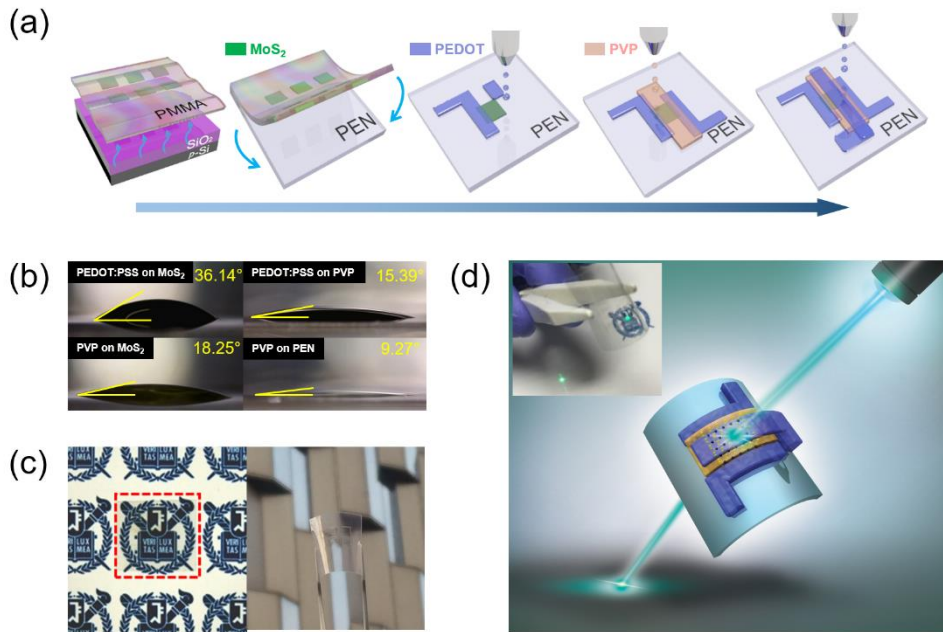


Figure 4.5 | (a) Schematic illustration of the fabrication processes for fully printed, flexible, and transparent CVD-synthesized MoS₂ phototransistors. (b) Contact angle measurements of PEDOT:PSS (top) and PVP (bottom) ink on the MoS₂ film (left) and PEN substrate (right). (c) Digital images of the transparent MoS₂ phototransistor arrays. In the left image, the device arrays (marked with a red square) were placed on a piece of paper with university symbols. The right image was taken in front of a building. (d) Photographic image (inset) and schematic of the devices under laser illumination [112].

The uniformity of the synthesized monolayer MoS₂ film on a SiO₂/Si substrate was evaluated by Raman and photoluminescence (PL) spectroscopy techniques. The Raman peak difference ($\sim 20.7 \text{ cm}^{-1}$) between in-plane E_{2g}¹ and out-of-plane A_{1g} (Figure 4.6a) and a distinct PL peak A ($\sim 670 \text{ nm}$; $\sim 1.85 \text{ eV}$) at the K point of the

Brillouin zone (Figure 4.6b) provided evidence that the CVD-synthesized MoS₂ film is an uniformly grown monolayer [139, 140, 158]. Interestingly, the blue-shifted PL signal of the transferred MoS₂ film on the PEN substrate was observed due to a slight tensile strain that was induced in the MoS₂ layer during the CVD synthesis process because of the difference in thermal expansion coefficients of the SiO₂/Si and MoS₂ layers [159, 160]. For the further investigation, PL mapping over an area of 20 μm × 20 μm was performed, as shown in the inset of Figure 4.6b. The color distribution indicated that the CVD-synthesized MoS₂ channel layer has uniform band gap energy at 1.85 eV. Cross-sectional scanning transmission electron microscopy (STEM) with energy dispersive X-ray spectroscopy (EDS) also supported that the MoS₂ layer was uniformly synthesized showing confined Mo and S signals (Figure 4.6c). To implement phototransistor arrays, the MoS₂ film was selectively patterned using RIE in an O₂ plasma (Figure 4.6d). Note that the CVD-synthesized monolayer MoS₂ film typically has a dark violet color on 270 nm-thick SiO₂ [48, 151, 158]. The white-dashed rectangles indicate the patterned MoS₂ channels after the RIE process.

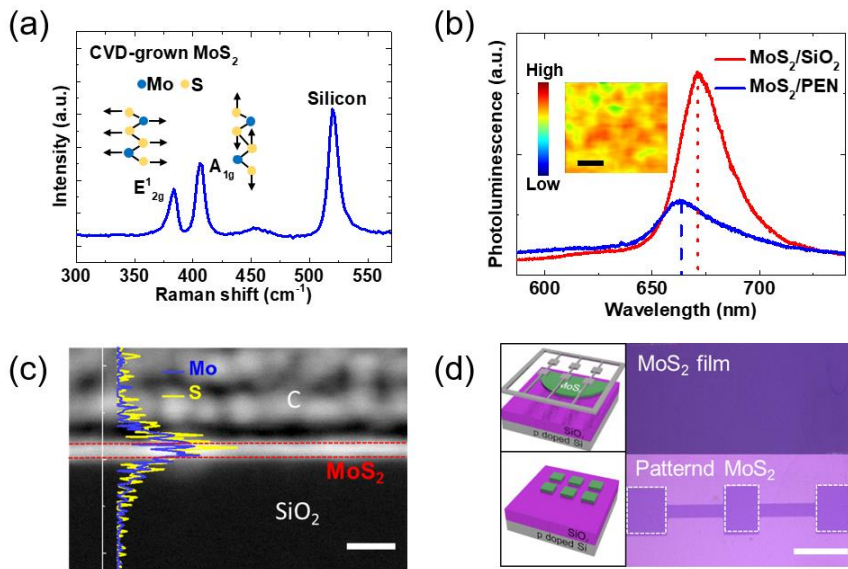


Figure 4.6 | (a) Raman spectrum of a CVD-synthesized monolayer MoS₂ film on a SiO₂/Si substrate. (b) PL spectra of CVD-synthesized monolayer MoS₂ films on SiO₂/Si and PEN substrates. The inset shows a PL intensity mapping at 670 nm (=1.85 eV). Scale bar is 5 μ m. (c) EDS data of Mo (blue line) and S (yellow line) and a cross-sectional STEM image of a CVD-synthesized MoS₂ film on a SiO₂/Si substrate. Scale bar is 5 nm. (d) Optical images of a CVD-synthesized MoS₂ channel before (top) and after (bottom) selective patterning processes. Scale bar is 400 μ m [112].

By exploiting the optimized PMMA-assisted transfer method, the patterned CVD-synthesized MoS₂ array was successfully transferred onto a PEN substrate without physical damage. The transferred patterned MoS₂ array films on the PEN substrate maintained its structural quality (Figure 4.6b and 4.7a); however, relatively weak PL and X-ray photoelectron spectroscopy (XPS) signals were observed

because of light scattering from the PEN substrates. The XPS spectra depicted in Figure 4.7a indicate the binding energies of the Mo 3d and S 2p orbitals (229.9, 233, 162.6, and 163.9 eV for Mo 3d_{5/2}, Mo 3d_{3/2}, S 2p_{3/2}, and S 2p_{1/2}, respectively). The difference between the binding energies of each orbital (3.1 and 1.3 eV for Mo 3d and S 2p, respectively) were consistent with the previously reported values [151] of CVD-synthesized monolayer MoS₂. In addition, the S/Mo atomic ratio of 1.95 estimated from the XPS, suggests that our synthesized MoS₂ film is stoichiometric. The lower binding energy of transferred MoS₂ film originated from the transferring process. The fully printed MoS₂ phototransistors with organic materials showed a high transmittance over 76% in the visible wavelength range, whereas the bare PEN substrate exhibited a transmittance of ~87% in the same wavelength range (Figure 4.7b). Noticeable absorption peaks at 1.87 and 2.02 eV (marked as arrows in Figure 4.7b) were observed. These peaks were attributed to the direct transition from the spin-orbit split valence band to the conduction band of MoS₂ monolayer, which is consistent with the previously reported results for both mechanically exfoliated [139, 140] and CVD-synthesized MoS₂ monolayers [161].

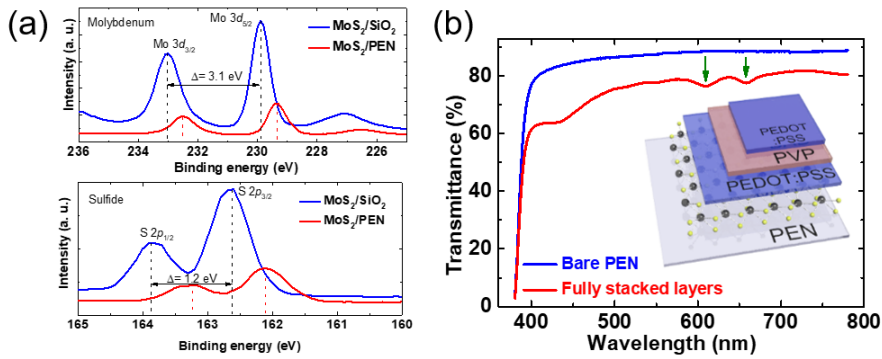


Figure 4.7 | (a) XPS spectra of a CVD-synthesized monolayer MoS₂ film on a SiO₂/Si (top) substrate and transferred MoS₂ film on the PEN (bottom) substrate. (b) Transmittance spectra of a bare PEN substrate (blue line) and fully stacked films (red line). Inset shows the schematic of the stacked layers (PEDOT:PSS/PVP/PEDOT:PSS/MoS₂/PEN) of our devices [112].

In particular, the wavelength of the onset of the absorption should correspond to the band gap energy. The PEDOT:PSS and PVP layers evenly reduced the optical transmittance by $\sim 5\%$ over the whole visible range. Because the fully transparent printed organic layers do not exhibit specific absorption peaks in the visible wavelength range, the photocharacteristics were entirely determined by the atomically thin MoS₂ channel layer without interference (Figure 4.8a). To consider the worst-case in transmittance, the measured films were prepared by sequentially printing all phototransistor layers over the entire PEN substrate in the following order: MoS₂, PEDOT:PSS, PVP, and PEDOT:PSS on the PEN substrate (see the inset illustration of Figure 4.7b). The fully printed phototransistors exhibited good

transparency (over ~76%) in the visible wavelength range (400 ~ 800 nm), whereas a PEN substrate exhibited a transmittance of 87% in the same wavelength range (Figure 4.8a). It is noted that the onset of strong absorption near 450 nm is not originated from the printed polymer, but from the CVD-grown monolayer MoS₂ film. As you can see in the Figure 4.8a, transmittance spectra of MoS₂/PEN (red line) as well as those of PEDOT/MoS₂/PEN (blue line), PVP/PEDOT/MoS₂/PEN (magenta line), and PEDOT/PVP/PEDOT/MoS₂/PEN (olive line) present strong absorption around a wavelength of 450 nm. For the further clear understanding, we added transmittance spectra of a bare PEN substrate (black line), printed PEDOT:PSS film on PEN substrate (red line), and printed PVP film on PEN substrate (blue line) (Figure 4.8b), which supports that the absorption spectra were not originated from the printed polymer but from the MoS₂ layer. Furthermore, the amount of photocurrent generated at PVP dielectric layer or PEDOT:PSS contact electrodes can be absolutely neglected comparing to that generated at semiconducting MoS₂ channel. In conclusion, the photocurrent is generated only in the MoS₂ channel layer.

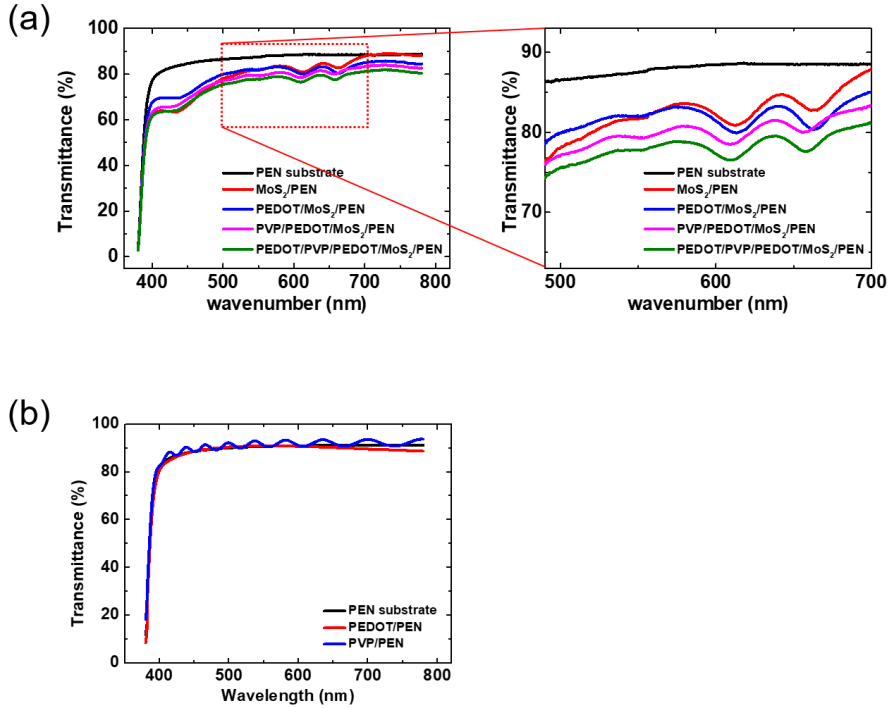


Figure 4.8 | (a) Transmittance spectra of the layer-by-layer stacked device structures from the bare PEN substrate to fully stacked structures (PEDOT:PSS/PVP/PEDOT:PSS/MoS₂/PEN films). (b) Transmittance spectra of a bare PEN substrate (black line), printed PEDOT:PSS film on PEN (red line), and printed PVP film on PEN (blue line) [112].

Figure 4.9a, b exhibit the transfer (drain-to-source current versus gate-to-source voltage, $I_{DS}-V_{GS}$) and output (drain-to-source current versus drain-to-source voltage, $I_{DS}-V_{DS}$) characteristics of a fully printed MoS₂ phototransistor measured in air. In particular, the I_{GS} , which can cause significant interference in the photocurrent [162], was greatly suppressed by removing the PMMA supporting layer very carefully and optimizing the inkjet-printing conditions for the PVP dielectric layer formation.

These efforts were necessary because the hydrophobic PMMA residue causes a critical dewetting issue during the PVP printing process, resulting in a high gate to source leakage current. As a result, the gate leakage current was drastically suppressed to < 1 nA after removing the PMMA layer with the optimized steps (Figure 4.2b). The extracted field-effect mobility in the linear regime (μ_{FET}) was found to be ~ 0.27 cm²/V·s using the following equation:

$$\mu_{FET} = \left(\frac{\partial I_{DS}}{\partial V_{GS}} \right) \frac{L}{W} \frac{1}{C_{ins} V_{DS}} \quad (4.1)$$

where $\left(\frac{\partial I_{DS}}{\partial V_{GS}} \right)$, L , W , C_{ins} , and V_{DS} denote the transconductance, channel length, channel width, capacitance between the channel and gate per unit area, and drain-to-source voltage, respectively.

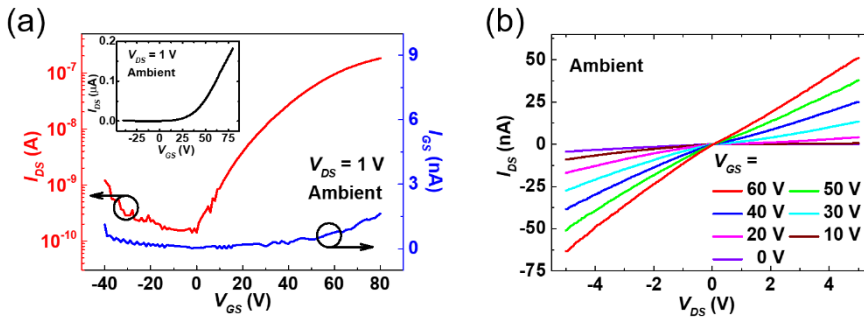


Figure 4.9 | (a) I_{DS} - V_{GS} curves using a log scale at $V_{DS} = 1$ V. Inset represents the I_{DS} - V_{GS} curves using a linear scale. (b) Linear plot of I_{DS} - V_{DS} curves [112].

The grain boundaries of the CVD-synthesized MoS₂ film [150], the low-

conductivity of the PEDOT:PSS electrode, and the low-k PVP dielectric deteriorated the electrical performance of the fully printed CVD-grown MoS₂ phototransistors. Although the difference in the electron affinity of monolayer MoS₂ (~4.0 eV) [163, 164] and the work function of the printed PEDOT:PSS layer ($\Phi_{\text{PEDOT:PSS}} \sim 5.07$ eV) (extracted by Equation 4.2 using ultraviolet photoelectron spectroscopy (AXIS Ultra DLD, He I source measurements, Figure 4.10), resulted in a high Schottky barrier, an ohmic-like contact property was exhibited with a good linearity of I_{DS} near low V_{DS} (Figure 4.9b and 4.11a) due to the chemical reactions at the PEDOT:PSS/MoS₂ interfaces [165].

$$\Phi_{\text{PEDOT:PSS}} = h\nu - E_{\text{SE}} \quad (4.2)$$

where h , ν , and E_{SE} denote the Planck constant, frequency and secondary edge of the He I source, respectively.

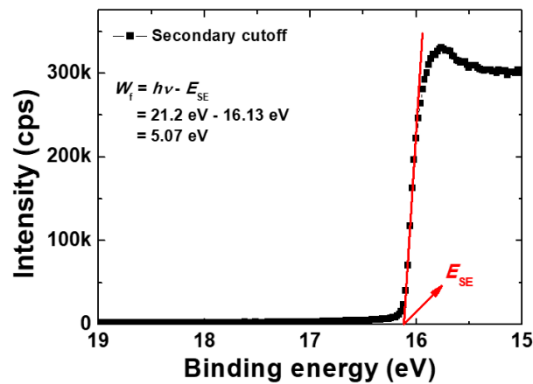


Figure 4.10 | Ultraviolet photoelectron spectroscopy of the PEDOT:PSS electrodes [112].

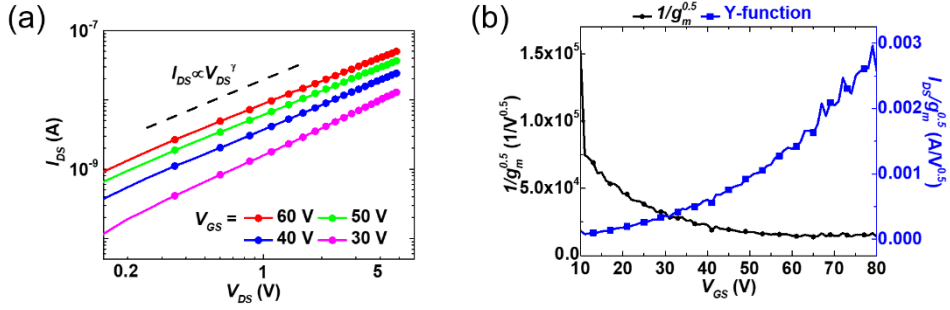


Figure 4.11 | (a) Log–log plot of I_{DS} – V_{DS} curves. The black dashed lines indicate the fitting line to the I_{DS} – V_{DS}^γ relation. The curves followed the relation $I_{DS} \propto V_{DS}^\gamma$ with an average γ value of ~ 1.2 well. (b) $1/g_m^{0.5}$ and Y -function ($I_{DS}/g_m^{0.5}$) of the MoS₂ phototransistors at V_{DS} of 1 V [112].

Furthermore, it should be noted that because the large-area MoS₂ channel also had a relatively high resistance due to the long-channel length of ~ 100 μm and large number of MoS₂ grain boundaries on the film [48], which resulted in an on-state current of $\sim 10^{-7}$ A, the contact resistance of PEDOT:PSS with the MoS₂ channel (~ 1.9 M Ω determined from the Y -function method [69], Figure 4.11b) was acceptable [24, 28]. The mobility and contact resistance, extracted using the Y -function (or Ghibaudo) method, were 0.37 cm²/V·s and ~ 1.9 M Ω , respectively (Figure 4.11b) [69]. Comparing to the width-normalized contact resistance values of the MoS₂ devices with conventional metal S/D electrodes, that of (≈ 760 k Ω ·mm) the printed PEDOT:PSS electrode and CVD-grown MoS₂ channel is relatively higher [48]. The grain boundaries of MoS₂ films and Schottky barriers at PEDOT:PSS/MoS₂ contacts would prohibit the charge injection. However, the contact resistance values are comparable with those of previously reported results

that describe contact properties between inkjet-printed PEDOT:PSS electrodes and organic semiconductors [24, 28].

Owing to the use of soft organic materials, the electrical performance was not degraded during a mechanical stability test over 1000 repetitive bending-relaxation cycles at a bending radius (R) of 5 mm, which corresponds to a uniaxial tensile strain of 1.26% (detailed calculation is shown below) along the channel length (Figure 4.12a).

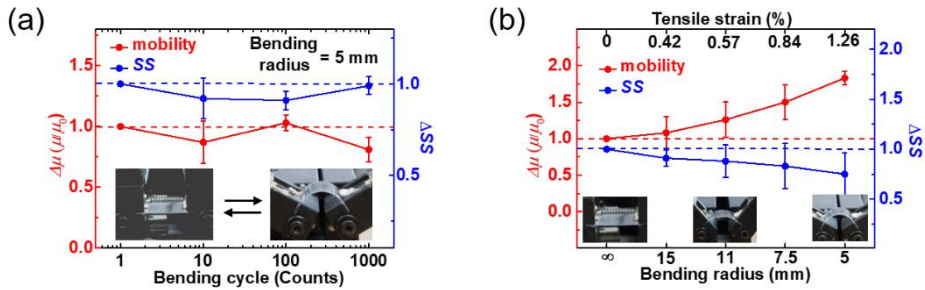


Figure 4.12 | The change in mobility (μ) and subthreshold swing (SS) versus (b) number of bending cycles with $R = 5$ mm and (c) R values of 5, 7.5, 11, 15, and ∞ [112].

As depicted in Figure 4.13, the applied tensile strain to the flexible phototransistors under bent conditions was calculated using the following equation.

$$\tan \theta \cong \theta = \frac{1}{R} = \frac{\varepsilon}{r'} \quad (4.3)$$

where θ , r , and ε denote the bent angle, one-half of the substrate thickness, and

increased length, respectively. The thicknesses of the monolayer MoS₂ film (~1 nm), PVP dielectric (~1 μm) and PEDOT:PSS electrodes (100 ~ 180 nm) are negligible compared with the thickness of the PEN substrate (~125 μm). The calculated tensile strains under bent conditions were 0.42, 0.57, 0.84 and 1.26 %, correspond to R of 15, 11, 7.5 and 5 mm, respectively.

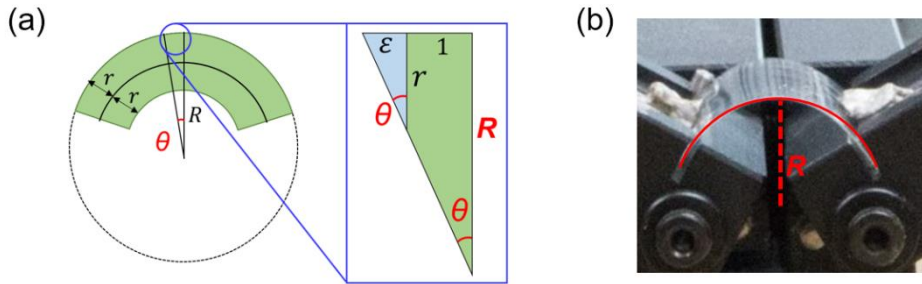


Figure 4.13 | (a) Schematic of a bent condition. The applied tensile strain can be calculated by the measured parameters. (b) Photograph of a MoS₂ phototransistor in a bent state with R [112].

The strain to the bent channel can be calculated as Equation 4.4.

$$\text{Strain} = \frac{t_{\text{MoS}_2} + t_{\text{total}}}{2R} \times 100 \cong \frac{t_{\text{total}}}{2R} \times 100 \quad (4.4)$$

where t_{MoS_2} and t_{total} denote the thickness of MoS₂ channel and thickness of the total device structure, respectively. In our device structure, the thickness-effect of monolayer MoS₂ (~1 nm) could be neglected by that of the PEN substrate (~125 μm). Therefore, the tensile strain applied to the atomically thin MoS₂ channel is much

lower compared as that applied to typical semiconductors with thicker layer.

The atomically thin MoS₂ layer allowed superior durability under a mechanical strain of 11% compared with widely used engineering materials, such as carbon nanotubes and oxide-based semiconductors [166, 167]. In contrast to the good mechanical stability under repetitive bending cycles, the mobility (μ) and subthreshold swing (SS) measured in a bent state (R of 15 mm, 11 mm, 7.5 mm, and 5 mm) increased as R decreased (Figure 4.12b). These enhancements can be attributed to a reduction in the band gap energy of CVD-synthesized MoS₂ when mechanically deformed (Figure 4.14) [134, 160, 166, 168].

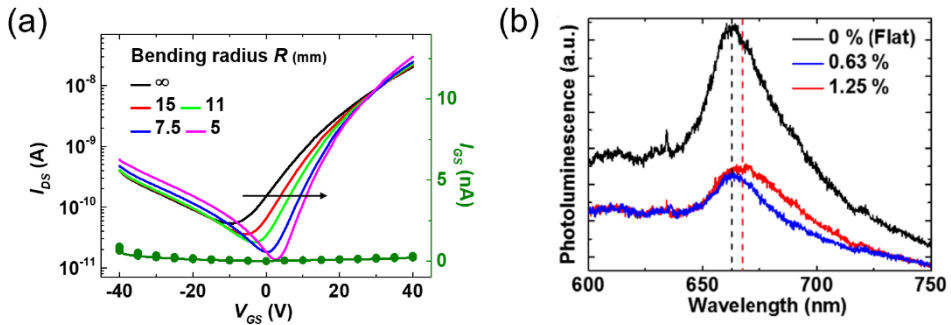


Figure 4.14 | (a) I_{DS} - V_{GS} of the MoS₂ phototransistor under bent conditions. (b) PL spectra of CVD-grown monolayer MoS₂ film under tensile strain [112].

The improved electrical performance of the phototransistors during applied tensile strain was attributed to the reduction in the band gap and a broadening of the band tails of the CVD-grown MoS₂. Because the applied tensile strain reduced the band gap energy, the conductivity of the MoS₂ channel layer increased [134, 160, 168]. From the following equation, the conductivity of the MoS₂ channel layer

increased as band gap energy decreased with applied tensile strain.

$$\sigma_{def} = \sigma_{rel} \left[-\frac{\varepsilon}{2k_B T} \frac{\partial E_g}{\partial \varepsilon} \right] \quad (4.5)$$

where σ_{def} , σ_{rel} , ε , E_g , k_B and T denote the conductance in the deformed state, conductance in the relaxed state, tensile strain, band gap energy, Boltzmann constant and temperature, respectively. The reduction of optical band gap energy of the CVD-grown monolayer MoS₂ under tensile strain was verified by the PL spectra measurements (Figure 4.14b). From the PL spectra, the optical band gap reduced at a rate of ~20 meV/% which is consistent to the reported theoretical and experimental results. Furthermore, the reduced charge scattering across the grain boundaries under tensile strain can improve the conductance as well [169]. Moreover, decreased electron effective mass can enhance the carrier mobility [170, 171]. Therefore, we believe that the modified band structure with applied tensile strain can be reduced to the change in mobility.

Figure 4.15 shows the photocharacteristics of the MoS₂ phototransistors under laser illumination. The measurements were executed after the devices were maintained on a 400 K hot-chuck in vacuum for 20 h to provide successfully suppressed I_{GS} by eliminating adsorbed water and oxygen molecules on the MoS₂ and gate dielectric layers. To investigate the contribution of the photocurrent ($I_{light} = I_{ph} + I_{dark}$) to I_{DS} , the ratio of I_{light} to I_{dark} in ON and OFF states was measured for different wavelengths with a fixed laser power density of 717 W/m² at $V_{DS} = 10$ V (Figure 4.15a). Note that the relation between the incident light power and photocurrent can be expressed like Equation 4.6.

$$h\nu = \frac{hc}{\lambda} = \frac{\text{incident power}}{\text{number of photons}} = E_0 + \frac{\hbar^2 k^2}{2m} \quad (4.6)$$

where h , ν , c , λ , E_0 , k , and m denote Plank constant, frequency, speed of light, wavelength, work function, wavenumber of electron, and mass of electron, respectively. As wavelength decreases at the same power, the number of photons and generated electron hole pairs are decreased altogether. However, the generated electrons get more kinetic energy and the number of electrons detected at electrical characterization setup is increased. As a result, as the wavelength decreases the photocurrent increases.

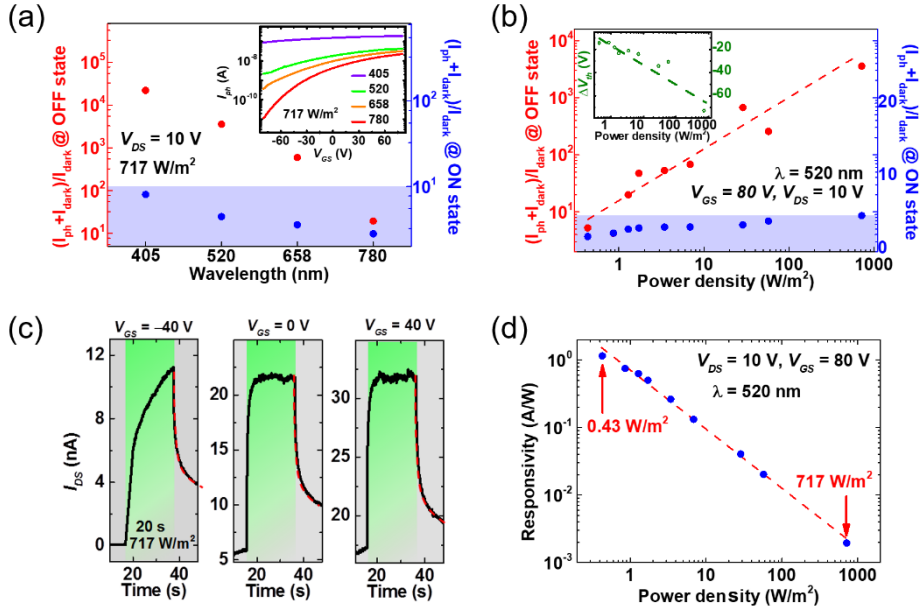


Figure 4.15 | (a) The ratio of I_{light} ($= I_{ph} + I_{dark}$) to I_{dark} in the ON and OFF states as a function of (a) wavelength and (b) laser power at a fixed $V_{DS} = 10$ V. Insets of (a) and (b) exhibit I_{ph} versus V_{GS} and the change in V_{th} with respect to the laser power, respectively. As the laser power increased, V_{th} shifted in the negative voltage direction, which indicates an increase in I_{ph} in the subthreshold regime. (c) Time-resolved photocurrent measurement under laser illumination ($\lambda = 520$ nm). The green-shaded regions indicate laser illumination for 20 s. (d) Responsivity of phototransistors as a function of power density under laser illumination ($\lambda = 520$ nm) [112].

The ON and OFF states are measured at $V_{GS} = 80$ and -80 V, respectively. Under laser illumination, the ratio in the OFF state drastically increased from $\sim 10^1$ to $\sim 10^4$, whereas in the ON state, the ratio was below 10 (see the blue-shaded region in Figure 4.15a) [172]. In particular, the I_{light}/I_{dark} ratio was increased from 10 to 1000

as a function of wavelength. An increase in the large I_{ph} in the OFF state was observed in our study compared with that of the previously reported phototransistors with mechanically exfoliated MoS₂ due to the relatively large channel area ($W/L = 400 \text{ }\mu\text{m}/100 \text{ }\mu\text{m}$) [142]. This advantage of CVD-synthesized MoS₂ offers opportunities for large-area optoelectronics applications with a good photosensitivity. Moreover, the ratio of currents in the ON and OFF states also showed good linearity in the laser power density (ranging from 0.43 to 717 W/m² at $\lambda = 520 \text{ nm}$), which is an important characteristic for photosensor applications (Figure 4.15b).

The photodecay time (τ_{decay}), which depends on V_{GS} , was also investigated by measuring the time-resolved photocurrent before and after laser illumination for 20 s with V_{GS} values of -40 , 0 , and 40 V at $\lambda = 520 \text{ nm}$ (Figure 4.15c). The decay curves were fitted by a stretched exponential equation,

$$I_{DS} = I_{ph,initial} \exp \left[-\left(\frac{t}{\tau}\right)^\beta \right] \quad (4.7)$$

where $I_{ph,initial}$, t , β , and τ denote I_{dark} , time, the fitting parameter, and relaxation time, respectively. After laser illumination with a power density of 717 W/m², τ_{decay} decreased from 6.7 to 1.7 s as V_{GS} increased from -40 to 40 V because the photocurrent contribution was weak at high V_{GS} , as previously mentioned. The shorter decay time compared with that of conventional CVD-synthesized MoS₂ phototransistors fabricated on a SiO₂/Si substrate is attributed to fewer interfacial traps between printed PVP dielectric and transferred MoS₂ layers [142, 173]. It should be noted that the effect of interfacial traps produced at MoS₂/SiO₂ during the high-temperature CVD-synthesis for large-area MoS₂ films [174, 175] could be

suppressed by the release and transfer processes onto other substrates. The monotonic decrease in responsivity with increasing incident photopower indicates that the trap states of CVD-synthesized MoS₂ are saturated (Figure 4.15d) [136, 173].

The responsivity and detectivity were also characterized for various laser wavelengths (Figure 4.16a). The fully transparent MoS₂ phototransistors exhibited comparable photoresponsivity and photodetectivity over the entire visible range from 400 to 800 nm compared with that of mechanically exfoliated MoS₂ phototransistors on opaque platforms [176, 177]. Moreover, the wavelength-dependent EQE (up to ~6.6%) also supports the fully printed transparent phototransistors, which exhibit good photocharacteristics, even though a top-gate configuration was employed (Figure 4.16b) [177]. Note that the wavelength-dependent EQE is dominantly attributed to the absorbance peaks in the MoS₂ layer (Figure 4.8a). Also, despite the use of the inkjet-printed electrodes and dielectric and transfer-printed MoS₂, our flexible and transparent MoS₂ phototransistors showed reasonable photoresponsivity compared to some of the previously reported values [137, 172, 176, 177]. Better photoresponsivity could be expected using a more optimized photocharacterization setup, for example laser density and the beam spot size of the laser.

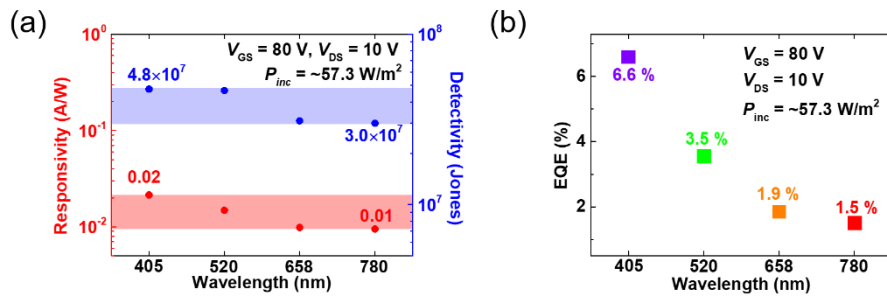


Figure 4.16 | (a) Photoresponsivity, photodetectivity, and (b) external quantum efficiency as a function of wavelength at a fixed $V_{GS} = 80$ V, $V_{DS} = 10$ V, and laser power density = 57.3 W/m² [112].

4.4. Conclusions

We have successfully demonstrated fully printed, transparent MoS₂ phototransistor arrays on flexible platforms. The CVD-synthesized monolayer MoS₂ and organic dielectric and electrode components were deposited directly onto flexible substrates using the optimized polymer-assisted transfer and inkjet-printing technologies, respectively. By employing ultrathin MoS₂ and transparent organic layers, the fully printed phototransistors exhibited excellent transparency and tolerance while maintaining electrical characteristics under tensile strain. Our work presents an opportunity to realize 2D TMDC-based low-cost wearable device applications beyond conventional electronics that employ brittle components.

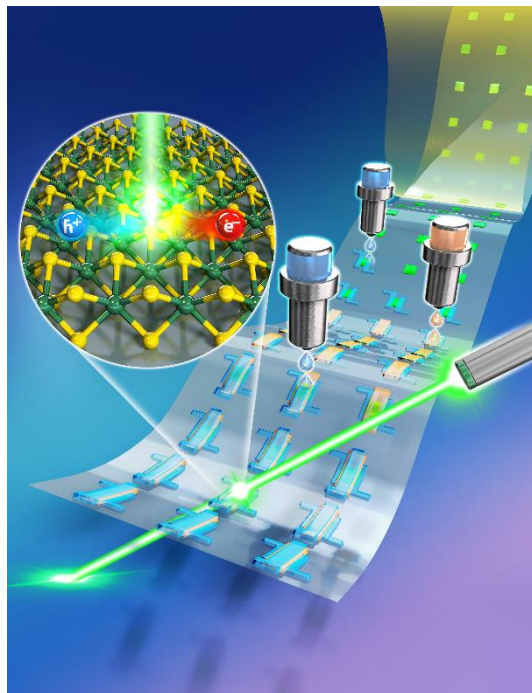


Figure 4.17 | Concept diagram of the fabrication process and photoresponse of transparent and flexible large-area MoS₂ phototransistor arrays.

Chapter 5

Conclusion

In this study, we propose transparent, flexible, and inkjet-printed TFTs based on organic semiconductors, SWCNTs, and MoS₂ with PEDOT:PSS electrodes and cross-linked PVP dielectrics. In addition, we proposed a facile interface engineering method to improve the electrical performance of transparent OTFTs and systematically analyzed the optical characteristics of transparent TFTs based on nano-materials.

First, to emphasize on the surface treatment in printed OTFTs, enhanced contact properties by conducting organo-compatible interface engineering between silver S/D electrodes and TIPS pentacene organic semiconductor layers for all-inkjet-printed OTFTs with a bottom-contact configuration were reported. The contact properties between the S/D electrodes and organic semiconductors were fully investigated using both TLM at various carrier concentrations and YFM at various channel lengths, and the contact resistances extracted using the two methods were in agreement with each other. Furthermore, by introducing an organo-compatible PS interlayer, the contact resistance was reduced by an order of magnitude showing better carrier injection characteristics. Based on these results, we believe that our

proposed interface engineering approach can be useful in solving contact-related issues that occur while realizing low-cost and highly integrated inkjet-printed short-channel OTFTs and their applications. In addition, we present a simple interface engineering technique for organic-based transparent polymer electrode and dielectric materials, which can be simultaneously modified for binding an end-silane-terminated PS without any preliminary treatment. By using this interface engineering methodology, fully inkjet-printed high-performance transparent OTFTs and inverters were fabricated on flexible Arylite substrates. Considering the trade-off between T_L and R_s of the printed PEDOT:PSS electrodes, the number of printing passes for gate and S/D electrodes was optimized. The introduction of a polymer interlayer to the electrode and dielectric surfaces could minimize the difference in γ between the PEDOT:PSS electrodes and PVP dielectric surfaces. The introduction of the PS interlayer led to a significant decrease in interface trap density between the gate dielectric and the semiconductor layer; in addition, it improved the ordering of the TIPS pentacene semiconductor layer. Moreover, the PS interlayer improved carrier injection from the S/D electrodes to semiconductor layer without a degradation in T_L . The improved OTFTs on the treated surfaces showed a high μ_{FET} of $0.27 \text{ cm}^2/\text{V}\cdot\text{s}$ (about 15 times higher than that of the untreated OTFTs), V_{th} of 2.42 V, SS of 1.16 V/dec, $I_{\text{on}}/I_{\text{off}}$ greater than 10^6 , and T_L of 70.0% (at 550 nm). The organic inverters with the PS interlayer also showed an excellent transition near 0 V, while maintaining an A_v of 7.17 V/V (at $V_{\text{DD}} = -20 \text{ V}$) during a 1000-cycle bending test at $R = 5 \text{ mm}$. Because all the layers consisted of soft polymers, significantly more stable operation under a tensile stress was realized. We believe all-inkjet-printed, all-organic TFTs and inverters on the facily introduced surface-matching interlayer have great potential in the realization of high-performance transparent electronics, e.g.,

transparent display and sensor applications, on a flexible platform using a low-temperature, low-cost process.

Next, we report on fully-inkjet-printed transparent SWCNT TFTs on a flexible PEN substrate. The transparent SWCNT TFTs showed a transmittance of 79.29% (at 550 nm), μ_{FET} in the linear regime of $7.01 \text{ cm}^2/\text{V}\cdot\text{s}$, $I_{\text{on}}/I_{\text{off}}$ of $\sim 10^5$, and SS of 1.50 V/dec. The inverters based on the SWCNT TFTs exhibited an excellent A_v of 10.21 V/V (at $V_{\text{DD}} = 10 \text{ V}$), showing an excellent transition near V_{DD} . Under high-power laser illumination, the SWCNT TFTs showed a decrease in current due to photodesorption near the nanotube networks. In contrast, under low-power light illumination (fluorescent light, RGB LEDs, halogen lamp, and sunlight), wherein light was emitted with the power similar to light in practical life, the SWCNT TFTs and inverter circuits showed negligible change in their electrical characteristics, indicating the possibility for their use in practical applications such as transparent displays. In addition, they maintained their electrical characteristics during a 1000-cycle bending test with R of 5mm, showing high stability and reliability under mechanical stress. We believe these all-inkjet-printed transparent flexible SWCNT TFTs have excellent potential for realizing high-performance and highly stable transparent and flexible electronics using a low-temperature, low-cost process.

Finally, we successfully demonstrated fully-printed, transparent MoS_2 phototransistor arrays on flexible platforms. The CVD-synthesized monolayer MoS_2 and organic dielectric and electrode components were deposited directly onto flexible substrates using the optimized polymer-assisted transfer and inkjet-printing technologies, respectively. By employing ultrathin MoS_2 and transparent organic layers, the fully-printed phototransistors exhibited excellent transparency and tolerance while maintaining electrical characteristics under tensile strain. Our work

highlights the possibility of realizing 2D TMDC-based low-cost wearable devices beyond conventional electronics that employ brittle components.

Based on these experiments, we believe that transparent and flexible electronic devices realized using inkjet-printing technology have great potential to serve as substitutes for the conventional photolithography patterning process as low-cost, environment-friendly processes. In addition, through the study on the implementation and characterization of transparent and flexible TFTs based on printing techniques using various materials, we present guidelines for applications in the field based on advantages and disadvantages of each material. We believe that our study and the obtained results make significant contributions to both academic and industrial research.

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Appendix

Portions of the work discussed in this dissertation are also presented in the following publications:

1. J. Ha[†], J. Seo, S. Lee, E. Oh, T. Lee, S. Chung^{*}, and Y. Hong^{*}, “Efficient Surface Treatment to Improve Contact Properties of Inkjet-Printed Short-Channel Organic Thin-Film Transistors”, *Journal of Nanoscience and Nanotechnology* **17**, 5718 (2017)
2. J. Ha[†], S. Chung[†], M. Pei, K. Cho, H. Yang^{*}, and Y. Hong^{*}, “One-Step Interface Engineering for All-Inkjet-Printed All-Organic Components in Transparent, Flexible Transistors and Inverters: Polymer Binding”, *ACS Applied Materials & Interfaces* **9**, 8819 (2017)
3. T.-Y. Kim[†], J. Ha[†], K. Cho, J. Pak, J. Seo, J. Park, J.-K. Kim, S. Chung^{*}, Y. Hong^{*}, and T. Lee^{*}, “Transparent Large-Area MoS₂ Phototransistors with Inkjet-Printed Components on Flexible Platforms”, *ACS Nano* **11**, 10273 (2017)

Publication List

Journal Papers

1. T.-Y. Kim[†], **J. Ha**[†], K. Cho, J. Pak, J. Seo, J. Park, J.-K. Kim, S. Chung^{*}, Y. Hong^{*}, and T. Lee^{*}, “Transparent Large-Area MoS₂ Phototransistors with Inkjet-Printed Components on Flexible Platforms”, *ACS Nano* **11**, 10273 (2017) (contributed equally as a *first-author*)
2. **J. Ha**, J. Seo, S. Lee, E. Oh, T. Lee, S. Chung^{*}, and Y. Hong^{*}, “Efficient Surface Treatment to Improve Contact Properties of Inkjet-Printed Short-Channel Organic Thin-Film Transistors”, *Journal of Nanoscience and Nanotechnology* **17**, 5718 (2017)
3. Y. Joo, J. Yoon, **J. Ha**, T. Kim, S. Lee, B. Lee, C. Pang, and Y. Hong^{*}, “Highly sensitive and bendable capacitive pressure sensor and its application to 1V operation pressure sensitive transistor”, *Advanced Electronic Materials* **3**, 1600455 (2017)
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6. S. Chung, **J. Ha**, and Y. Hong*, “Fully Inkjet-printed Short-channel Organic Thin-Film Transistors and Inverter Arrays on Flexible Substrates”, *Flexible and Printed Electronics* **1**, 045003 (2016)
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1. G. Kim, J. Park, **J. Ha**, C. Lee, and Y. Hong, “Fabrication of solution-processed flexible polymer light-emitting diodes with ITO/PEDOT:PSS bilayer transparent electrodes”, *The 8th International Conference on Flexible and Printed Electronics (ICFPE)*, Jeju, Korea, September (2017) (poster)
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3. J. Seo, **J. Ha**, B. Lee, H. Kim, and Y. Hong, “Hysteresis-free All-solution-processed Single-Walled Carbon Nanotube Thin-film Transistors Encapsulated with Fluoropolymer”, *International Conference on Amorphous and Nanocrystalline Semiconductors (ICANS)*, Seoul, Korea, August (2017) (poster)
4. T.-Y. Kim, **J. Ha**, K. Cho, Y. Song, J. Pak, J.-K. Kim, S. Chung, Y. Hong, and T. Lee, “Fully Flexible and Transparent CVD-Grown Monolayer MoS₂ Field-Effect Transistors with all Inkjet-Printed Components”, *The Materials Research Society (MRS) Spring Meeting*, Phoenix, USA, April (2017) (oral)
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국문 초록

최근, 투명하고 유연한 박막 트랜지스터(thin-film transistor, TFT)는 bendable, rollable, foldable, 혹은 wearable 전자 기기 등 다양한 차세대 전자 기기로 응용이 가능하여 많은 각광을 받고 있다. 한편, 잉크젯 프린팅 기술은 간단하며 저비용, 저온 및 대면적 공정을 가능하게 한다. 이러한 이유로, 다양한 용액 공정 혹은 잉크젯 프린팅 공정 기반 금속 산화물 층은 높은 광학적 투명도, 높은 전하 이동도 및 전하 농도 덕분에 투명 전자 소자 응용에 널리 사용되어 왔다. 그러나, 높은 어닐링 온도, 유기 불순물의 존재, 필름의 단단함 등 잉크젯 프린팅 공정을 이용하여 금속 산화물 기반 박막 트랜지스터를 유연 전자 소자에 이용하기 위해서는 해결해야 할 문제들이 여전히 남아 있다. 이러 문제를 극복하기 위하여, 투명한 전도성 고분자 및 유연한 반도체 재료가 투명하고 유연한 전자 기기 응용에 사용되어야 한다.

본 학위 논문에서는 투명 전극으로 poly(3,4-ethylenedioxythiophene):polystyrenesulfonate (PEDOT:PSS) 를, 세 종류의 반도체 활성층으로 6,13-bis (triisopropylsilyl)ethynyl pentacene (TIPS pentacene) 유기 반도체, 단일벽 탄소나노튜브, 이황화 몰리브덴을 사용한 잉크젯 프린팅 기반 투명 박막 트랜지스터 제작에 관하여 논의한다. 모든 층은 물질 자체적으로 유연하며 프린팅 공정을 이용하여 제작되어 유연한 플랫폼 상에 제작할 수 있었다. 나아가, 투명한 유기 박막 트랜지스터의 전기적 특성을 개선할 수 있는 간편한 표면 엔지니어링 방법을 제안 하였으며, 나노 재료를 기반으로 하는 투명 박막 트랜지스터의 광학적 특성을 체계적으로 분석 하였다. 다양한 재료를 활용한 인쇄 공정 기반 투명하고 유연한 박막 트랜지스터의 구현 및 특성 분석에 관한 연구를 통하여, 각 재료의

장단점을 바탕으로 각 응용 분야에 대한 가이드라인을 제시 하였다. 이러한 결과는 학계와 산업계 모두에 기여도가 높을 것으로 기대한다.

첫째, 인쇄 공정 기반 유기 박막 트랜지스터 제작에서는 소스/드레인 전극과 게이트 절연층의 표면 에너지 매칭이 중요하다. 표면 에너지가 매칭되지 않은 플랫폼에 유기 반도체를 프린팅할 경우 높은 접촉 저항을 야기할 뿐만 아니라 용매가 건조되는 과정에서 소스/드레인 전극 근처에서 불연속적인 결정 구조를 가지는 π -공액 반도체가 생성되어 전기적 특성이 떨어지게 된다. 본 학위 논문에서는 향상된 유기 반도체 결정 구조를 얻기 위하여, 유연한 기판 상에 전 인쇄 공정, 전 유기물 기반 투명한 유기 박막 트랜지스터 및 인버터를 제작 할 때 사용할 수 있는 투명한 유기 전극 및 게이트 절연체 층에 동시에 수행되는 효과적인 표면 엔지니어링 방법에 대해 소개한다. 이러한 잉크젯 프린팅 기반 유기 호환 폴리스티렌 중간층은 소자의 투과율을 저하시키지 않으면서, 보다 우수한 전하 주입 특성 및 반도체층의 결정성을 제공하며 게이트 절연체 상의 결함 부위를 최소화한다.

둘째, 투명 박막 트랜지스터를 실생활에서 사용하려면 조명 하에서 동작이 변하지 않아야 한다. 유기 반도체를 비롯한 일반적인 반도체 재료는 빛에 민감한 것으로 잘 알려져 있기 때문에, 조명 하에서도 안정적인 성능을 보이는 투명 박막 트랜지스터용 활성층이 필요하다. 단일벽 탄소나노튜브는 1차원 재료의 특성으로 인하여 내부에서 강한 쿨롱 상호 작용이 일어난다. 그로 인하여 높은 엑시톤 결합 에너지를 갖기 때문에 단일벽 탄소나노튜브를 이용한 박막 트랜지스터는 특이한 광 반응성을 나타낸다. 다른 반도체 재료를 이용하여 제작된 박막 트랜지스터들과는 달리, 단일벽 탄소나노튜브 기반 박막 트랜지스터는 고전력 레이저 조명 하에서 전류가 감소하지만, 실생활에서 사용되는 저전력 조명 하에서는 전기적 특성에 큰 변화를 보이지 않는다. 본 학위 논문에서는 이러한 특성을 활용하여 단일벽 탄소나노튜브 기반 박막 트랜지스터의 실생활에서 사용 가능한 투명하고

유연한 전자 소자에의 응용 가능성에 대하여 논의한다.

마지막으로, 단일벽 탄소나노튜브와는 달리 이황화 몰리브덴은 높은 광 반응성을 보인다. 이황화 몰리브덴의 이러한 특성은 웨어러블 디바이스의 필수 요소 중 하나인 광 센서에 응용이 가능하게 한다. 그러나, 기존의 이황화 몰리브덴 기반 박막 트랜지스터의 제작에서는 일반적으로 대면적 및 유연한 전자 소자에는 사용할 수 없도록 포토리소그래피 혹은 전사 공정을 사용한 무기 전극 및 유전체가 사용되었다. 실제 응용 분야에서 2차원 이황화 몰리브덴의 이점을 잘 활용하기 위해서는 저온, 대면적 및 저비용 공정을 사용하여 투명하고 유연한 2차원 전자 기기를 제작하기 위한 새로운 전략 개발이 필요하다. 본 학위 논문에서는 화학 증착법(chemical vapor deposition, CVD)으로 성장된 투명한 단분자층 이황화 몰리브덴을 이용하여 유연한 폴리머 기판 상에 전 인쇄 공정으로 제작된 광 트랜지스터에 대하여 보고한다. 전사된 단분자층 이황화 몰리브덴 상에 절연층 및 전극을 포함한 모든 층들은 기계적 변형에 잘 견딜 수 있도록 유기 물질을 잉크젯 프린팅하여 패터닝 하였다. 유연한 유기 층들을 매우 얇은 이황화 몰리브덴과 함께 사용함으로써 전 인쇄 공정 기반 이황화 몰리브덴 광 트랜지스터는 우수한 투명도와 기계적 안정성을 보인다.

주요어: 투명 일렉트로닉스, 유연 일렉트로닉스, 유기 박막 트랜지스터, 단일벽 탄소나노튜브 박막 트랜지스터, 이황화 몰리브덴 박막 트랜지스터, 잉크젯 프린팅

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