M.S. THESIS DISSERTATION

Improvement of Photosensitivity in Carbon Nanotube-based Near-Infrared Phototransistor by Selective Wetting Pattern

선택적 습윤 패턴을 통한 탄소 나노튜브 적외선 광 트랜지스터의 광감도 향상 연구

BY

SARA KHALED BAZHAIR

AUGUST 2018

DEPARTMENT OF ELECTRICAL ENGINEERING AND COMPUTER SCIENCE

COLLEGE OF ENGINEERING

Improvement of Photosensitivity in Carbon Nanotube-based Near-Infrared Phototransistor by Selective Wetting Pattern

선택적 습윤 패턴을 통한 탄소 나노튜브 적외선 광 트랜지스터의 광감도 향상 연구

2018 년 08 월

지도교수 이 신 두

이 논문을 공학석사 학위논문으로 제출함

서울대학교 대학원

전기정보 공학부

사라 칼레드

사라 칼레드의 공학석사 학위논문을 인준함

2018 년 05 월

위 원 장 ___이 창 희___ (인)

부위원장 ___이 신 두___ (인)

위 원 ___홍 용 택___ (인

Abstract

Recently, carbon nanotubes (CNT) based phototransistors (PT) have been gaining much attention due to the pronounced mechanical and electronic properties of CNTs, in addition to the ability of photodetection combined with the internal gain as in transistors. Near-infrared (NIR) detectors for medical applications such as health monitoring systems and industrial applications such as night vision and food inspection. For this, it is important to obtain devices the exhibit high photosensitivity for efficient and effective photoresponse to light exposure. To obtain high photosensitivity, photogenerated carrier recombination losses must be minimized. This is possible through the reduction of gate leakage current by controlling the vertical gate charge carriers to prevent them from passing through the gate insulator layer of the transistor device.

In this thesis, presented is an all solution processed NIR phototransistor consisting of a patterned network of single-walled carbon nanotubes as the photoactive layer of the transistor. The P-type lateral bottom-gate-top contact device was fabricated on a silicon substrate covered with a silicon dioxide insulator film and on a Glass substrate with patterned indium tin oxide (ITO) gate and a poly (4-vinyl phenol) (PVP) as the gate insulator. Applying a selective wetting method through a micro-patterning technique using a fluoropolymer-coated poly(dimethylsiloxane) (PDMS) stamp on the device insulator followed by deposition of carbon nanotubes (CNT) solution can leave a patterned film of a network of Single-walled CNTs (SWCNT). This assisted in confining the vertical flow of charge carriers by creating a hydrophically patterned barrier (PHB) and hence decreased the gate leakage current from order 10^{-8}~10^{-7} to an order of 10^{-9}~10^{-10}. A photoresponse was only observable upon exposure to NIR (980 nm) laser following the improvement by reduction of gate leakage, while without the PHB layer there was no detectable response to light exposure. On current showed a steady value when both devices were compared, and a notable decrease in off current led to an increase in on/off ratio. Through these results, we prove that the patterning of PHB layer on the gate insulator assists in creating a barrier to improve device performance effectively by reducing the leakage current. With materials such as CNTs, that exhibit superior properties, this a step ahead towards fully solution processable carbon nanotube electronics, where cost-effective and minimum labor fabrication procedures are in high demand.

Table of Contents

List of Figures

List of Tables

Intro

Chapter 1 Introduction

1. Phototransistors

1.1. Features and Trends

Phototransistors, or in other words, light detecting field effect transistors, have become irreplaceable in applications of security and imaging systems. They are known to produce higher currents than photodiodes in addition to being inexpensive, and small enough to fit in integrated computer chips. Phototransistors are known to produce a voltage, unlike photoresistors, and they are extremely fast thus provide instantaneouse output. There has been extensive progress in the fabrication of phototransistors that can demonstrate high photosensitivity to light exposure, some which employed organic materials as the medium to convert the incident photon energy into electrical charges, while others use non-organic materials.unlike photodiodes, phototransistors will combine the internal gain amplification with the photosensing to produce high photocurrent (drain current). The gate terminal voltage will control the drain current, where additional control is viable through the exposure of the active region to a light source. Before going further deep into more background topics relevant to the work done in this research thesis, we briefly explain the operation modes of a phototransistor.

A phototransistor operates by accepting incident photons from an exposure of light source of a specific wavelength, it will then cause the generation of photo-excitons (electron-hole pairs), which dissociate into free electrons and holes under the effect of an external electric field. Theses free charges will contribute to the flow of the conductive channel and hence contribute to the overall photocurrent extracted from the device. In case of a p-channel device operating in accumulation, $V_{GS} < V_T$, illuminating the active region results in a positive threshold voltage shift. That is because upon photogeneration and under electric field, holes will flow to the drain and electrons will accumulate under the source electrode. This will lower the hole injection barrier between the source and the active region channel. Upon illumination, an increase in drain current I_D will be noted as the threshold voltage is positively shifted due to the lowered contact rejection caused by the lowered injection barrier at the source. Electron trapping moieties, such as hydroxyl groups on the dielectric surface (SiO_2 or polymer insulator)

can lead to trapping sites at the active-layer/dielectric interface, which can capture the photoengrated carriers. In off state, that is when $V_{GS} > V_T$ (depletion mode), drain current will increase linearly as the illumination power. That is due to the compensated electrons, for every electron exiting there will be another injected until a recombination event takes place. The electric field assists in enhancing photogeneration due to the applied gate voltage.

1.2. Reduction of gate leakage current in phototransistors

Leakage current can effect FET based devices in multiples ways, for instance in case of light illumination, device photogenerated carrier recombination losses are increasing if the leakage current is high enough. The availability of free carriers proves essential for the photosensitivity and photoresponsivity of a phototransistor, therefore it is crucial to eliminate any factors that may lower the carrier lifetime or increase the recombination rate, such as defects at the insulator/semiconductor interface that as well assist in leakage. It has been established that patterning the semiconductor film forming the channel can eliminate the parasitic paths of the leakage current, and therefore assisting in increasing device response to light. This proves that the quality of the insulator film is essential for device performance, Therefore, various patterning and printing methods have been introduced such as optical lithography [1]. Researchers have as well demonstrated simple solution processable methods of printing that are compatible with large-scale fabrication of thin film devices [2]. One such successfully applied method, which we will demonstrate in this research, is microcontact printing, also considered as part of soft lithographic methods.

Another method to fabricate highly performing phototransistors is t utilize the superior material properties. For example, high optical absorption coefficients and enhanced carrier mobilities were achieved through organic and inorganic materials by either single-material systems or heterojunction systems. These include nanowires and nanoparticles such as carbon nanotubes (CNT) nanowires and lead sulfide (PbS) or germaium (Ge) quantum dots (QD), heterojunction systems that use organic-inorganic junctions such as Poly(3-hexylthiophene) (P3HT):PbS-QD, and organic-organic bulk heterojunctions such as DPP-DTT:PCBM [3, 4, 5, 6].

Some other works focusing on NIR phototransistors, which is the wavelength employed in this research subject, incorporate device design modifications such as vertical PTs. In vertical PT, carrier travel time to the top electrodes is reduced by the introduction of a vertical

path conductive channel that offers shorter distance. Layering multiples materials as layered-heterojunctions is another approach that can combine several properties required for a highly performing PT, such as high mobility, effective absorption layer and an exciton dissociation layer [source]. Similarly, reduction of gate leakage current can be achieved through several techniques including patterning of the semiconducting thin film of the active layer region. Ink-jet printing and ozone assisted printing are two such techniques.

2. The road to Mechanically Flexible Electronics

New generation flexible applications, demand smart electronics that are compatible with large area flexibility demands. However, device rigidity poses a serious obstacle in the way of such progress. Yet it is undeniable that remarkable progress took place over the years and hence getting TFT devices closer and closer to achieving highly flexible electronics. For the purpose of durable bendability, high mobility, low temperature, low cost and large-area integration, several materials were investigated for both the dielectric/insulator and active channel semiconductors of field effect transistor.

Figure 1.1 reviews a roadmap of dielectric and active layer materials that were investigated over time leading to well-established discoveries of advantages and disadvantages and proved essential for the operation of a transistor. With polymer insulating semiconductors and nano-carbon materials, such as single-walled carbon nanotubes (SWCNT), being the trend of research nowadays, considerable efforts are directed for FET based devices that employ them. For the great properties that SWCNTs hold (will be explained in the next chapter), CNT based FETs and phototransistors are becoming the center of focus as potential candidates for microelectronics and highly sensitive and responsive light detection techniques. With such pronounced efforts, NIR detectors based on films SWCNT phototransistors have been investigated. As much effort is made towards single CNT detectors, random network SWCNT thin film based phototransistors are gaining further importance [2].
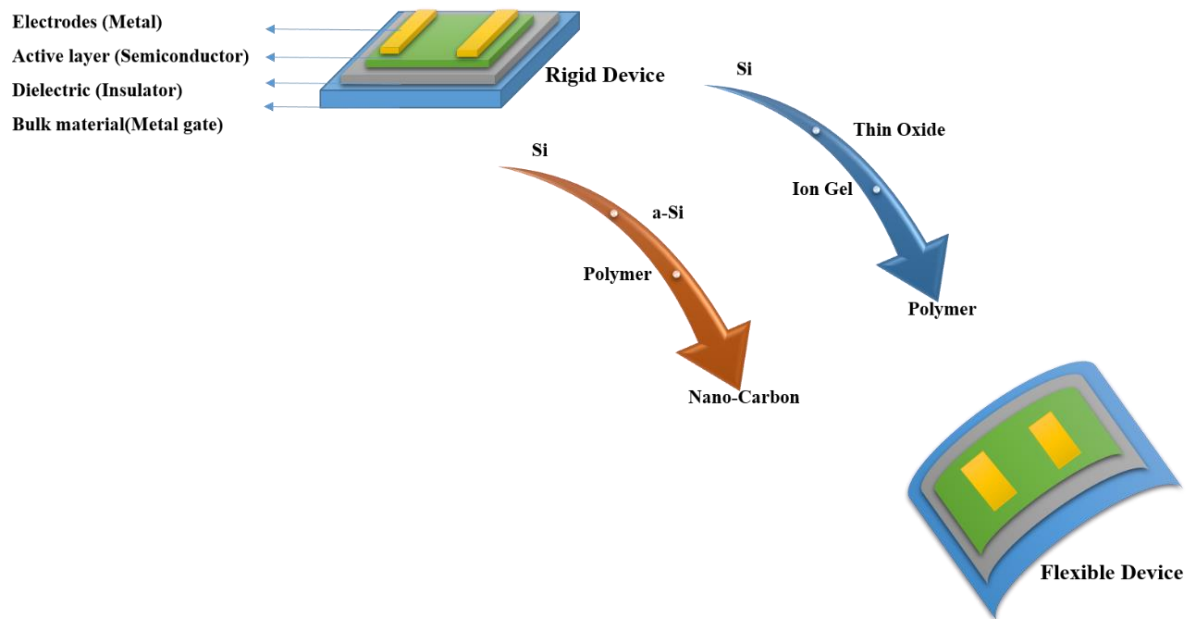
Figure 1.1 Demonstrating the roadmap from rigid to flexible devices, ther arrows indicate, past to present, the materials employed for dielectric (blue arrow) and semiconductor layer (orange arrow).

For the realization of large-area applications that employ flexible TFT arrays, organic polymers are the new class gate dielectric materials for ultrathin high-dielectric-constant (high-k) and low leakage current. Silicon dioxide has been used as a gate dielectric for decades. Device performance is improved as the drive current increases when the gate capacitance is increased, which requires decreasing the dielectric thickness as per the principles of parallal plate capacitors. Leakage currents, therefore, take further rise. Leakage limitation, however, sets a threshold to how low the k constant can be, therefore, replacing SiO_2 with a high-k insulator that endures high flexibility and can yield low thickness is the superior option. Silicon oxide was for a long term the major gate insulator choice, control of suitable doping options made Si the material for device channel formation. Nevertheless, it is not compatible for flexible device purposes, and could not keep its role with the increasing demand for applications such as wearable devices [7]. Following this, thin oxide, then Ion gel were investigated for their dielectric properties with the most recent choice being the polymer dielectric material.

Semiconducting polycrystalline, amorphous silicon (p-Si & a-Si) and polymer materials are investigated for their high mobility and applicability as transistor channel materials. Each of the above-mentioned materials revealed challenges such as low mobility and flexibility in case of a-Si, low uniformity and processability of p-Si and the high cost of metal oxides. Even though semiconducting polymers are widely investigated for their sustainable bendability, they still stand behind as semiconductors due to poor mobility and degradable chemical stability. This led researchers towards the investigation of nano-carbon materials. With this recent breakthrough, two-dimensional graphene and carbon nanotubes are studied, opening the road for high-quality flexible electronics era, where bendability and high mobility are a major attraction. CNT materials disclose a whole set of properties which if adequately processed into thin films, making it the leading material for future wearable devices and flexible applications. Some of those properties are high carrier mobility, stretchability and flexibility in addition to very high mechanical strength. All such properties highlight CNTs as perfectly suitable for channel materials of stretchable thin film transistors (TFT) [8, 9].

3. Single-Walled Carbon Nanotube Phototransistors and Solution Process

Single-walled carbon nanotube phototransistors (SWCNT-PT) has seen a great deal of progress, recently the potential in visible-ultraviolet and near-infrared (NIR) wavelength detection have been presented [10]. That combined with the excellent electronic and optoelectronic characteristics and the superior mechanical and chemical stabilities of SWCNTs; make it the subject of thermal and photo-responsive applications. CNT based optoelectronic devices are ideal for applications in areas of IR detection for such as military, optical communication, and scientific research. There have been notable and continuous progress in semiconductor device technologies. As much fcus has been given towards simple fabrication processes while keeping up with the soon to reach a limit moor's law, which empowered 50 years of advanced electronics and computing, lower fabrication costs have as well been achieved to keep the balance of technological advancement and industrial requirements. Among several semiconductor devices, field effect transistors (FET) are widely employed in light detection technologies such as photodiodes and phototransistors. That is, because of the ability to convert incident light of various wavelengths, depending on the active layer materials' bandgap, in the spectrum to a flow of charges that can contribute as the

5

photocurrent and hence make it applicable to a wide range of light sensing technologies. SWCNT-PT has proven to be superior to photodiodes due to its structure and fabrication simplicity, it's inexpensive cost and faster operation, their technologies have gone through extensive research, where several factors that contribute to the fabrication and development of a high performing device were discovered. More or less of these factors are dependent on the proper selection of gate insulator and active layer materials, in addition to the process used for the deposition of high-quality thin films.

One of the major shortcomings nowadays exist in the film processing of random network CNTs, where there is a lack of a simple yet effective CNT film deposition techniques that are fully solution processable. That being said, several methods of vacuum deposition and solution processes took place and were investigated for CNT thin film formation including methods to increase conduction and decrease leakage current. Some methods are spin coating, dip coating, spray coating and drop casting, which all aim for the formation of a thin film of the semiconducting CNTs that are dispersed in water or in a solvent. In addition to that, patterning methods are becoming more popular and employed mostly with organic thin film transistors (TFT) based devices [11].

4. Thesis Outline

In this thesis, presented are the outcomes and analysed the results of a single-walled carbon nanotube phototransistor fabricated using a selective micro-petterning step to control surface hydrophobicity of the dielectric in order to assist carbon nanotube (CNT) thin film self-patterning upon its deposition. In chapter 1, the latest advancmeents in SWCNT-PT fabrication and the importance of research in this field is elaborated. In chapter 2, introduced are the relevant background topics of CNT materials and material properties, where we describe the geometrical, electrical and optoelectronic properties of carbon nanotube materilas, and specifically single-walled CNT materials. Through this it is also emphasized on the relationship between the material optoelectronic properties and how they are controlled by the geometrical properties. Some of the material processing techniques employed on CNTs are discussed. These include thin film deposition processes that can be of direct growth nature, where the CNTs are growm from catalyst directly on the substrate, or solution process nature, where the maerials are processed from a solution form by dispersion in a solvent. The importance of

surface energy modification as a nessecary process to prepare substrate surface for the deposition on CNTs is also discussed.

Chapter 3, the experimental section introduces the basics of single-walled CNT phototransistors, followed by the experimental details of the device fabrication. It also introduces here the materials used followed by the device fabrication procedure and the basic concept of gate leakage current reduction throught the selective wetting pattern technique. Then, device characterization methods such as transfer curve measurement, optoelectronic properties measurement and parameter extraction results are shared. Chapter 4, discusses the reults that were obtained from the device measuremnts as a transitor and then as a phototransistor that was exposed to 980 nm of near-infrared (NIR) laser. This section demonstrates the sucsesful reduction in gate leakage current due to the barrier in the way of the vertical leakage current placed by a hydrophobicity pattern. The observed changes in on/off ratio and device hysteresis behavior are as well discussed. The observed photoresponse will as well be explained in this chapter through demonstrating the response of the drain current to the pulsed exposure of the NIR laser. Following that, an explanation of possible reasons for such behaviour and calculated parameters showing the device high photosensitivity in addition to high on/off ratio and low leakage current is discussed. The thesis is concluded by a summary of the procedures and findings of the research presented in this paper.

Chapter 2 Background

1. CNT Materials

Carbon nanotubes are nanometer-sized tubules of a network of carbon atoms in hexagonal assembly. They possess high mechanical flexibility and elasticity due to the high ratio of tube diameter to tube length (aspect ratio), of the CNT and the strong bonds. The electronic properties of CNTs are the major attraction with high conductance and very high current densities (10^9-10^{10}). More appealing is the ability to form a thin film of random CNT networks and its solution processability, making it suitable for thin film transistor (TFT) based applications [12].CNTs can be used as SWCNT or multiwall and double-walled tubes (MWCNT and DWCNT). In DWCNTs, one CNT is rolled to form diameter while another is rolled around it with a larger diameter leaving some spacing between the walls of the two tubes. Where MWCNT is formed through multiple SWCNT concentrically rolled so to form a tubule with multiple walls each separated by a spacing. The interest in this research is focused around SWCNT for their unique properties as thin film materials for future electronics. In the following sections, we emphasize those properties.

1.1. Structural Properties

The chirality system in Fig. 2.1 allows identification of the CNT type (armchair, zigzag or chiral). The chiral vector C_h, which acts as the circumferential vector of the SWCNT using the two unit vectors a_1 and a_2 and the chiral integer indices (n, m). To form a SWCNT, a graphene sheet, as in Fig. 2.1, is rolled along the chiral vector while the (0,0) point is overlapped with the (n, m) point, based on which the desired type of SWCNT is formed. The chiral angle θ is located between C_h and a_1. The diameter of the CNT is d_t and band gap energy are inversely proportional to the band gap of the target CNT, which effect the material electrical properties as well.
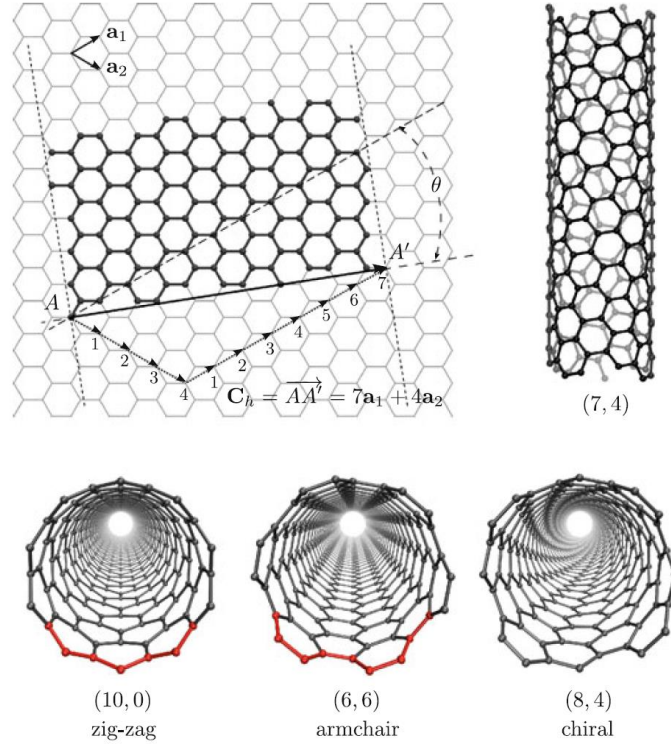
Figure 2.1 Sheet geometry of a honeycomb carbon sheet and the possible types of nanotubes producible through the control of chirality vector and indices **[13]**

1.2. Electronic and Optoelectronic Properties

Another approach to categorizing types of CNT is by the electronic type, in other words, semiconductors or metallic CNTs. This can be identified by the electronic band, as metallic systems the valance and conduction bad cross each other or touch at the fermi level, but in semiconducting systems, they do not meet and an energy gap exists E_g between them. The zone-folding model is used to identify the density of states at a certain energy level to reveal the electronic type of the CNT. In case of a metallic CNT, the valance and conduction bands meet or overlap at the fermi level, while the density of states (DOS) is not zero. In this case, the chiral indices are found $|n - m| = 3i$, and all other cases designate semiconducting CNTs where zero DOS on the Fermi energy level in addition to a band gap exist [14].

With the ability to control the geometrical structure of a tube through d_t and (n, m), the electronic structure and optical properties are influenced. It is expressed in the band structure of graphene and has a linear dispersion such as the two-dimensional (2D) energy. V_F is the fermi velocity ($10^6 \ m/s$), and k is the 2D wave vector This relation establishes the geometrical factor that influences the angular momentum of the electronic states. That is the perpendicular

two-dimensional wavevector component $k_\perp$. The value of angular momentum is largest with the highest $k_{\perp max}$ smallest with $k_{\perp min}$. A single particle model reveals interband transitions upon electronic excitation leading to electron-hole pairs that are bound with several hundred m V, where these binding energes are found to be inversely proportional to d_t .

The rolling of graphene sheets into a 1D SWCNT leads to a significantly high density of states energy levels, also known as the van Hove singularities. The optical transitions upon absorption of light, therefore, differ with semiconductor than metallic SWCNTs due to the difference in spacing between the van Hof singularities of the valance and conduction bands. Red-shifted peaks can be noticed when the energy gap between the van Hof singularities is small. The band gap is dependent on the diameter of the SWCNT, where large diameters result in smaller energy gaps. Optoelectronic properties of CNTs are most important when considering Thin films for TFTs, where they can be transparent and conductive films with performance relying on CNT purity, length, doping level and dispersion. CNT films were examined in light exposure over a wide range of wavelengths, including infrared as shown in Fig. 2.2, where the transmittance of carbon nanotubes is compared with several other materials. This certainly makes them attractive for the purpose of IR imaging that uses IR sensitive photodetectors and phototransistors [15].
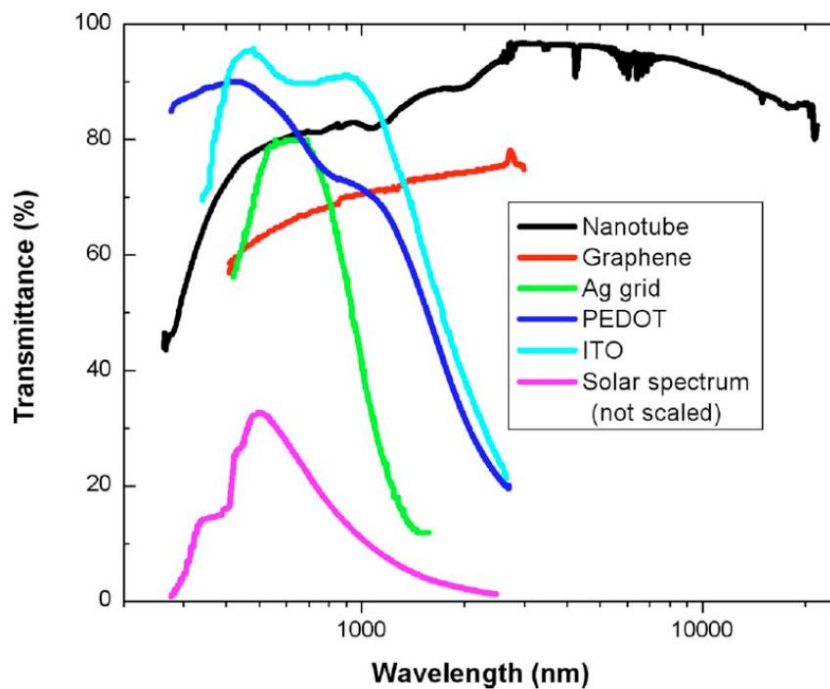
Figure 2.2 Optical transmittance of CNT and several other films in wide range **[16]**

10

2. CNT Thin Film Processing

1.1. From Direct Growth to Solution Process

There are two major CNT film fabrication methods (Fig. 2.3), one is known as the direct growth method, which refers to growing the tubes on the substrate instead of placing it from a solution phase as is done with the solution process methods. CNT growth is most commonly achieved through chemical vapor deposition (CVD), which uses catalyst particles to grow the SWCNTs at an extremely high temperature (> 800 ℃) with carbon and hydrogen gasses. The advantage of CVD methods is the ability to grow either random or aligned SWCNT networks. Alignment of the grown film can be controlled either by laser ablation, electric field force or gas flow, wherein SWCNT film growth and surface-oriented growth has proven more effective [17]. In general, CVD grown SWCNT films have shown superior electrical performance, however, even though aligned networks introduce high mobility devices but unfortunately, they show very low reproducibility.
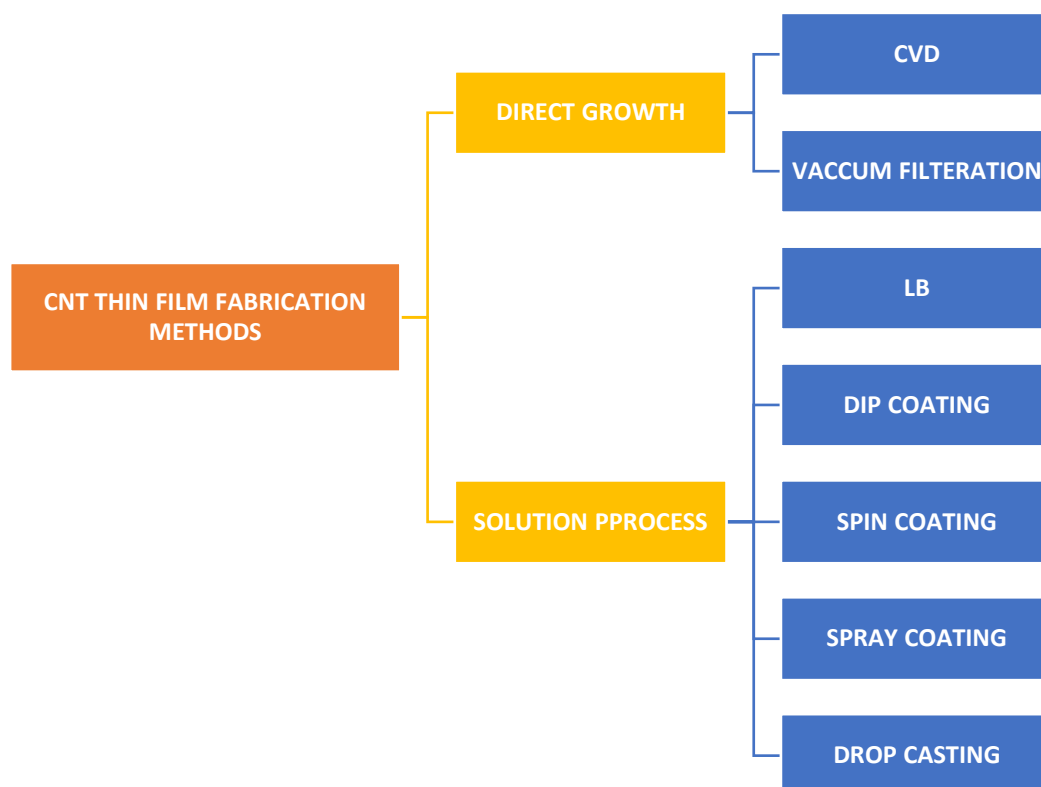
Figure 2.3 SWCNT film fabrication methods

With the vast advantages of direct growth methods, they present crucial disadvantages such as costly equipment and high-temperature processes that are not compatible with plastic substrates. Therefore, solution processes are promoted as the new potential candidate for being independent of high vacuum systems that elevate the costs of production, while as well offering fast production of thin films at low temperatures and making it compatible for large area applications. For solution based thin-film fabrication, solution viscosity and surface tension are two factors that, if properly controlled, can result in thin films of high quality and avoid thinning or rupture. Such factors are considered as rheological properties. Viscosity thus should always exceed a certain limit. Wetting agents are used to match the surface tension of inks with the substrate surface, viscosity can be increased by using additives. Surface tension mainly effects the interaction between CNT and substrate surface, which can result in adhesion of CNT only if the surface or the CNTs are treated to do so. Hence, prior to coating CNT dispersion on silicon, glass or plastic substrates, the surface energy is raised by treatments such as chemical or plasma. Similarly, additives are added to the CNT dispersion in order to lower the tension.

1.2. CNT Thin Film Deposition Processes

In general, the solution process of SWCNT films requires the consideration of the interaction between substrate and solution, where the goal is to produce an agglomeration free uniform film. Langmuir Blodgett (LB) method, for instance, uses horizontal lifting or vertical dipping, where it is reliant on the CNTs hydrophobic behavior, which yields good spreading on a hydrophilic surface. Although LB coating results in aligned films, it proved too slow in case more than a molecule in thickness is required [18]. LB can result in a randomly distributed CNT film while offering thickness control through a filtration method, however, even that can result in poor film integrity and hence is not suitable for FET thin film fabrication. Self-assembly (SA) processes were as well investigated with CNT films, where several techniques can promote their self-adhesion on the substrate. SA can assist in producing multilayer structures, yet so far it has been imperfect due to the slow production rate it offers. That is mainly because either the substrate is charged or molecular marks are used to guide the CNT-substrate interaction, which is a slow process its own. Simpler and more effective methods were thus studied for SWCNT film deposition that promises the potential for large-scale coating as well.

Thin film coating methods such as dip coating, spin coating, spray coating and drop casting, are all solution processes that basically require two stages, the coating, and the drying. In dip coating solution viscosity, CNT-substrate interaction, dipping speed and drying conditions (time and temperature) are all critical to producing high-quality films. Even though successful, dip coating result in coating both sides of the substrate which is not desired. In case of spin coating, spinning speed and time are two more factors that prove essential for uniform film formation. However, film non-uniformity proved to be a major drawback in this case. For CNT-FET devices, film uniformity is an essential property, for which drop casting followed by blow drying has shown great potential. In this process, instead of spinning at high speed, a small amount of solution is dropped on the target active area region and simply dried in the air [9].

1.3.   Surface Energy Modification

High-quality thin films are required for CNT device applications, therefore, surface energy modification techniques are given high priority. For example, to avoid undesired hysteresis in CNT-PT caused by trapped mobile ions or water residue at the insulator-semiconductor interface, methods like mechanical surface modification, plasma treatment of the surface, self-assembly monolayer, and Poly(dimethylsiloxane) (PDMS) stamp. CNT-dielectric interface requires methods such as surface hydrophobicity control to decrease hysteresis by coating a hydrophobic layer over the dielectric prior to CNT film deposition.

Surface energy or surface wettability (hydrophobicity) is determined by the contact angle(θ), which is the angle formed between the liquid-solid and the tangent to the liquid-solid-air contact point of the liquid droplet standing at equilibrium on the solid substrate. Surface wettability can vary according to surface energy (low to high surface energy), contact angle, and the forces of adhesion and cohesion. Surface is non-wettable as adhesion force is less than cohesive foce, that is at lower surface energy with contact angle $\theta > 90°$.Tthe surface is completely wettable at higher surface energy as the adhesion force is much larger than the cohesive force at a contact angle $\theta \sim 0°$. If the adhesion force is greater than or equal to cohesive force at a contact angle $0° < \theta \leq 90°$, the surface is partially wettable. While surface wettability is effected by roughness, inhomogeneity and chemical contaminations, there are several methods for the modification of the surface energy such as mechanical surface modification using AFM to scratch the surface to alter the morphology of the surface. Oxygen

or nitrogen plasma treatment will cross link the surface atom wih an ionized oxygen atom to increase the surface energy (surface hydrophobicity or wettability) and hence promote adhesion with similar concepts as for devices with conjugate polymers [19].

Chapter 3 Materials and Methods

1. Single-walled Carbon Nanotube Phototransistors (SWCNT-PT)

Figure 3.1 and 3.2 below illustrate the basic structure of a CNT based phototransistor and the semiconducting-CNT energy barrier due to contact with the metal electrodes. There are two type of CNT phototransistors, a single nanotube or thin film network based. In the first case, a single 1D CNT is placed in contact with metal electrodes each end using methods such as dielectrophoretic force and atomic force microscopy (AFM) manipulation system. On the other hand, in case of thin film CNT devices, it could be either a random or an aligned network of SWCNTs deposited as the active channel through either direct growth, solution processes or transfer printing methods.

1.1. Single CNT Phototransistor

Placing a single SWCNT result in a CNT-metal interface at each the drain and the source, forming two Schottky barriers connected in reverse. Upon the illumination, above bandgap photons will generate excitons in the nanotube and they decay to lower energy state as free electrons and hols. Electron-hole separation is caused by several processes, externally applied electric field, the internal field at the Schottky barrier, p-n junctions or due to defects. A photovoltage is generated in all these cases except in case of an externally applied bias, where a photoconductive effect takes place and leads to a change in current.

Fig. 3.1(a) is a basic single SWCNT-PT. the work function of the metal and the Fermi level of the CNT may either result in canceling the photocurrent or magnifying it depending on the contact nature. In other words, if identical Schottky barriers are formed at both ends of the CNT-metal contact, identical currents from the reversely connected Schottky diodes will flow from both barriers in opposing directions and hence cancel each other. This is presented in Fig. 3.1(b). In case the contact interface is varied by changing the metal on one side, it will create an asymmetric detector, where one is often a Schottky contact and one is an ohmic contact. This way the photocurrent generated at each contact will not cancel out. As shown in Fig. 3.1(c), the electron and hole injection at the ohmic contact is prevented and hence there is no photogeneration, while the maximum photocurrent is equal to the one generated at the Schottky barrier. The asymmetric device mechanism is considered best for improving device efficiency and sensitivity and hence yielding higher performance sensors [10].

(a)

Dielectric
Gate
Substrate

(b)

$E_{conduction}$

$hv > Eg$

E_f

metal

metal

$E_{valance}$

(c)

$E_{conduction}$

$hv > Eg$

E_f

metal

metal

$E_{valance}$
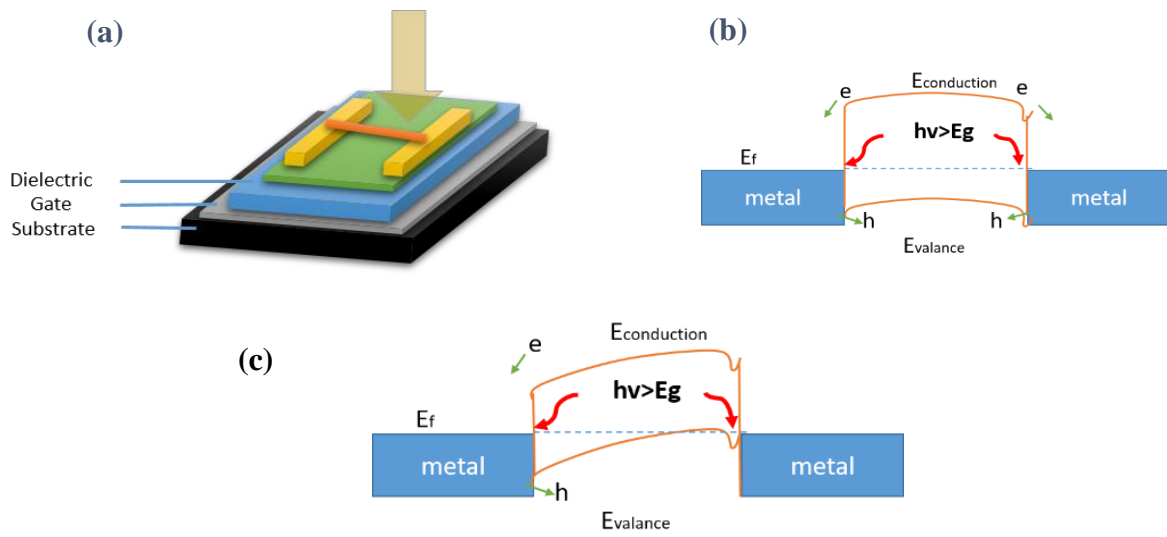
Figure 3.1 (a) basic structure of a single CNT based phototransistor. (b) schottky contact detector with schottky barrier at each metal-CNT contact. (c) schottky-ohmic contact detector.

1.2. Random network CNT phototransistor

Random network SWCNT films can be employed as the active channel in SWCNT-PT. Under a positive gate bias, carrier density and injection at source/drain (S/D) barrier are modulated. Electrons/holes will be induced and injected from the forward biased CNT-metal Schottky contact into the CNT, as normally is in a single CNT transistor. Through the CNT-CNT junction, electrons will be transferred through the random network of CNTs and hence yielding a conduction channel where electron extraction can be achieved at the CNT-drain contact. In the case of an ohmic contact, electrons and holes would be injected from the drain and collected at the source. Fig. 3.2(a) shows a basic bottom-gate top-contact random SWCNT film phototransistor. Following the same logic as the single CNT device, illuminating the contacts will result in photogeneration that will contribute to the injected holes and electrons through the nanotube. The transport of photocarriers will occur along the nanotube until it crosses a CNT-CNT junction. the charge carrier number can be modified along the CNT network through the application of a voltage between the gate and the S/D input. In Fig. 3.2(b), the metal-CNT junction for both n-type and a p-type SWCNT-PT.
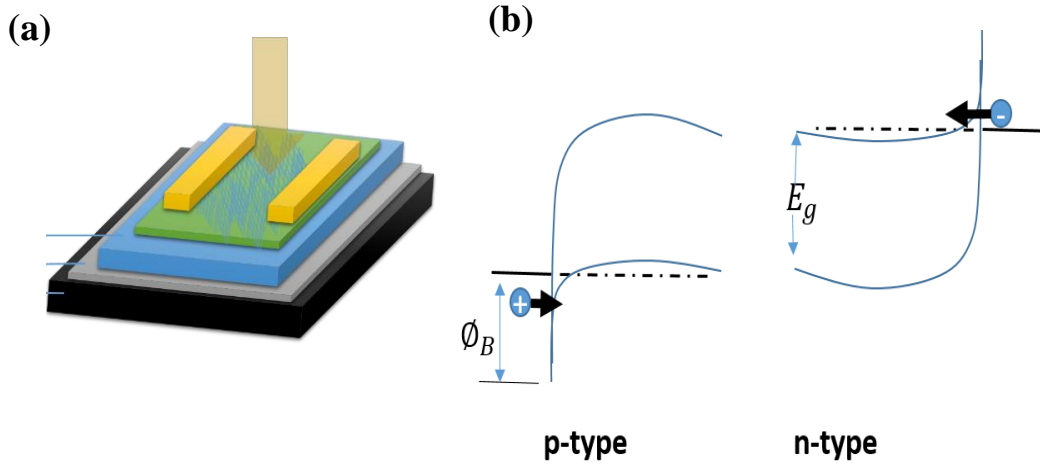
Figure 3.2 (a) Top-contact-bottom gate random network SWCNT-PT. (b) CNT (semiconductor) and metal barrier for a p-typr and an n-type transistor.

2. Materials

The dielectric material for the Glass substrate based device was prepared by 10% of poly(4-vinyl phenol -Mw 25000) (PVP) in Propylene glycol monomethyl ether acetate (PGMEA) with additive 10% of crosslinking agent Poly(melamine-co-formaldehyde) methylated solution. For the surface treatment of both glass and Si/SiO_2 an adhesion promoting solution named Ply L-Lysine (0.1% (w/V) H2O) was used. A Fluoropolymer (Novec™ EGC-1700, 3M) was used for the selective micro-patterning step using a poly(dimethylsiloxane) (PDMS) stamp. A solution of semiconducting single-walled carbon nanotubes >95% purity (in water) was used for the drop casting of the active layer.

3. Fabrication Process

Prior to any thin film deposition steps, the substrate was cleaned by sonication for 10 minutes in acetone, isopropyl alcohol, methanol, and deionized water (respectively). For this study the device fabrication took place on two kinds of substrates, Si substrate coated with 3000 $A°$ of SiO2 and a glass substarte coated with a patterned gate indium tin oxide (ITO). For the glass/ITO substarte, crosslinked PVP with 10% concentration in PGMEA was spin coated at a speed of 3000 rpm for 30 seconds and then anelaed for 10 minutes and 20 minutes at 100 and 200 cellcius respectively.

Surface modification for the deposition of a well adhered thin film of random SWCNTs was achieved by coating Poly L-Lysine solution by drop and dry. It was dropped on the entire substrate to cover all active regions of the intended devices and then rinsed with deionized water (DI) after 10 minutes. Following that, a pre-patterned PDMS stamp was dipped in the EGC solution with a controlled uniform speed to ensure proper coating of the stamp. The pattern on the stamp was matching that of the intended gate pattern in case of Si/SiO2 substrate and matching the ITO gate pattern in case of the glass substrate. Following that, a fluorinated polymer was printed on the surface of the dielectric with conformal contact while ensuring pattern alignment so to selectively modify surface hydrophobicity for the favor of CNT film patterning to cover only the active region of the device. The SWCNT (>95% in water) Solution was drop-casted for some time and then rinsed with DI water. As the last step, 50 nm-thick Gold (Au) contacts were thermally deposited through a shadow mask at the rate of 1.0 Å/s under 10^{-5} Torr. Fig. 3.3. and Fig 3.4 show the fabrication steps and the final device structures. PHB is the patterned hydrophobic layer which assists in blocking the vertical leakage current.
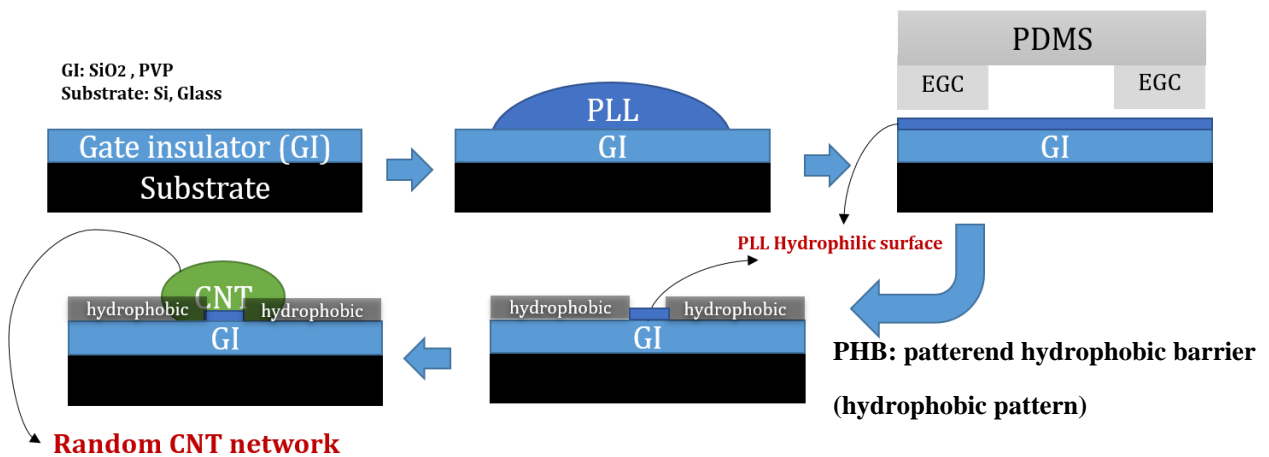

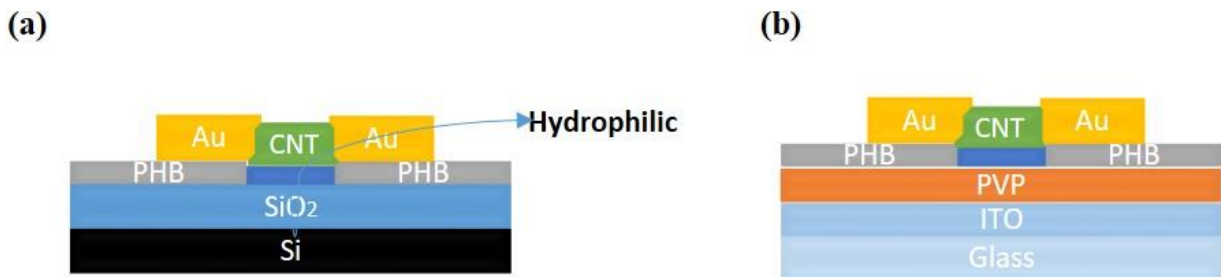Figure 3.4 SWCNT-PT fabrication steps starting with a bare substrate covered with SiO2 and another with PVP

Figure 3.3 The final structure of both SWCNT-PT devices after deposition of gold contacts. (a) Si/SiO2 based and (b) PVP based

3.1. SWCNT Adhesion Promotion and Film Patterning

When the deposited CNTs interact with the substrate surface, it may or may not adhere to the surface. To guide the self-adhesion or self-organization of SWCNTs on the surface of the dielectric on a substrate, the substrate is coated with a polymino acid, the electrostatic interaction between the oppositely charged CNT and surface ions is enhanced and thus facilitates the attachment of monodispersed CNTs on a solid surface. One such palymino acid is Poly L-Lysine (PLL), which is known as an adhesion enhancer that can be used for coating various surfaces.

By means of a PDMS stamp with the desired nano-topography patterns, immersing it in desired surface energy modification solutions, and then by simple conformal contact with the targeted surface area, it is possible to pattern the surface hydrophobically so to confine and pattern the SWCNT dispersion owing to their nature to disperse on hydrophilic surfaces. With this method, no patterning process is required post-deposition of the SWCNT. This leaves a patterned hydrophobic pattern (PHB) that will as well prevent the reaction between two surfaces in case of contact, where the fluorinated polymer used will modify the surface energy as directed by the patterns on the PDMS stamp and prevent the reaction between the underlying insulator layer and the CNT semiconductor layer. Fig. 3.3 demonstrates the process of micropatterning a substrate with a hydrophobicity patter via a fluorinated polymer solution and a PDMS stamp.

PDMS stamp dipped in EGC

PDMS stamp in direct contact with insulator covered substrate

1. PDMS stamp with pattern dipped in fluorinated polymer and lifted with a steady speed

2. Pattern on PDMS stamp. In case of glass/ITO substrate the pattern matches the ITO pattern

3. Fluorinated polymer patterned on dielectric in alignment with gate ITO pattern
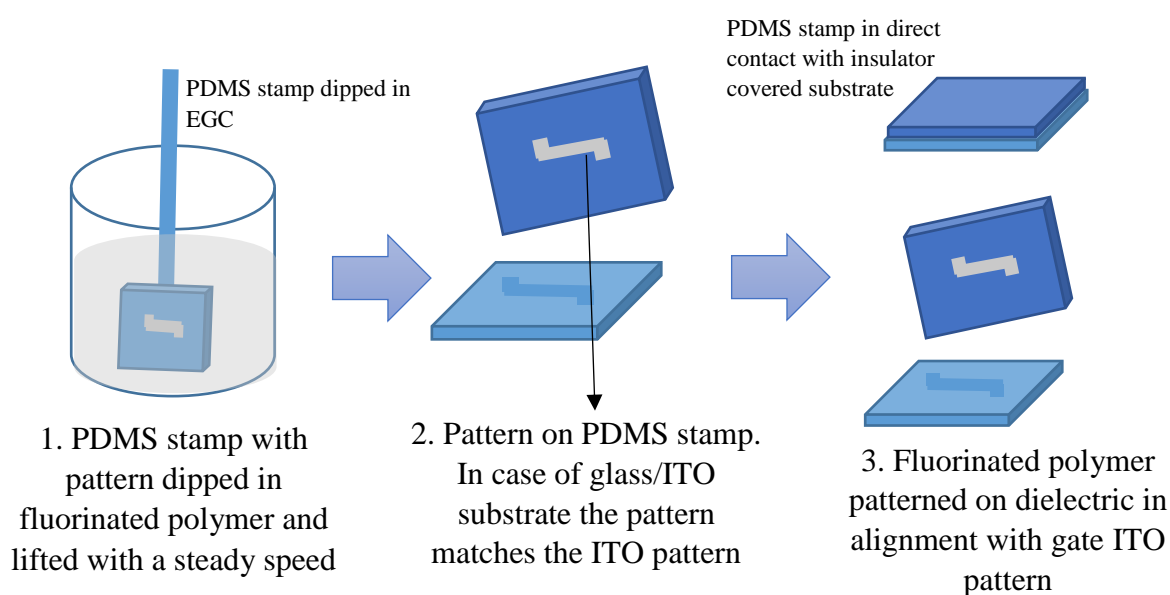
Figure 3.5 Processes for PDMS stamping to transfer the flourinated polymer for surface hydrophobicity (PHB) patterning

3.2. Basic Concept of Leakage Current Reduction by PHB pattern

Phototransistors are based on the mechanism and structure of field effect transistors (FET). Therefore, the concept of leakage current reduction is not far from FET devices. Fig. 3.6 illustrates the basic concept of blocking the vertical carriers using the PHB layer. When the EGC covered PDMS stamp contacts the gate insulator (GI) surface, a fluorinated polymer is transferred with the same pattern using a hydrophilic surface on the intended active area region and a hydrophobic (PHB) surface on all other regions. When the CNT solution is deposited it is adhered to the hydrophobic region due to its nature. The origin of leakage current can be from the vertical charges flowing through the gate insulator or due to the lateral charges flowing from source to drain.

To understand this, Fig. 3.6(a) is showing the flow of the vertical leakage and lateral
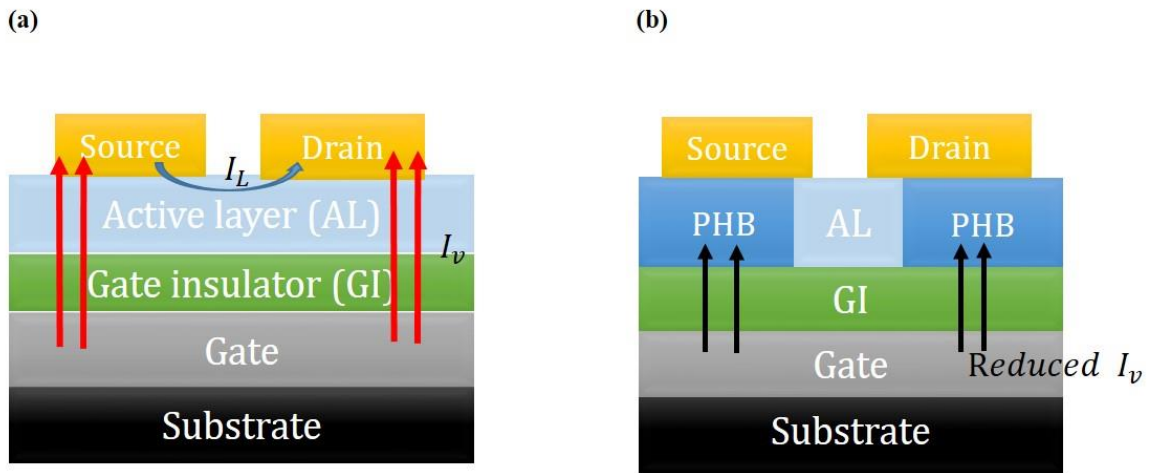
Figure 3.6 Illustration of the basic concept of introducing a PHB layer for leakage current reduction. (a) without PHB and (b) with PHB

charges I_V and I_L current without the application of a PHB. Here it is visible that a large vertical flow will exist as there is nothing standing in the way of these charge carriers, and hence causing a high leakage current that effects device performance and photosensitivity as well. on the other hand, applying a PHB layer creates a barrier that prevents vertical charge carriers from panatration through to the top contacts, and hence results in a reduced vertical leakage current contribution to the extracted carriers at the contact. This is illustarted in Fig. 3.6(b) [20].

4. Device Characterization and Methods

4.1. Transfer Characteristics

Prior to phototransistor measurements, device transistor performance was to be evaluated. Using the Agilent 4155C parameter analyzer, it was possible to measure the transfer output of the SWCNT transistor. By applying a sweeping voltage to the gate electrode ranging from -50 V to 50 V with a constant -5 V drain voltage V_D, Drain current I_D was obtained versus the gate voltage V_G. For the glass/ITO base device V_d was fixed at -50 V.

4.2. Measurement of Electro-Optical Properties

Fig. 3.4 below shows the SWCNT film absorbance measured using Fourier transform infrared spectroscopy (FT-IR) (Tensor 27, Bruker). In addition to the basic transistor performance parameters, the phototransistor performance as a light detector must be investigated. This is done through the evaluation of a few important figures of merit. Photosensitivity (P), as in Equation (1), is the photocurrent-to-dark current ratio and is a figure of merit indicating how sensitive the phototransistor is to the incident light. Where the photocurrent is merely the difference between the drain current level in illumination and in dark. Responsivity is another important figure of merit, which is given by equation (2) and is expressed as the ratio of photocurrent (I_{photo}) to the radiant energy power P .

$$P = \frac{I_{photo}}{I_{dark}} = \frac{I_{illumination} - I_{dark}}{I_{dark}} \qquad (1)$$

$$R = \frac{I_{photo}}{P} \quad (A/W) \qquad (2)$$

To obtain the photocurrent, devices are connected using the same procedure when performing the transfer curve characterization. A NIR laser source of wavelength 980 nm (100 mW/cm^2) was directed on the active region of the phototransistor while performing the measurement. For the purpose of evaluating this, the device is subjected to a pulse-like exposure, each exposure lasting few seconds. With the peak absorbance evident in the range ~950 to 1000 nm (Fig 3.7), the light source was chosen as the NIR wavelength of 980 nm (100mW).
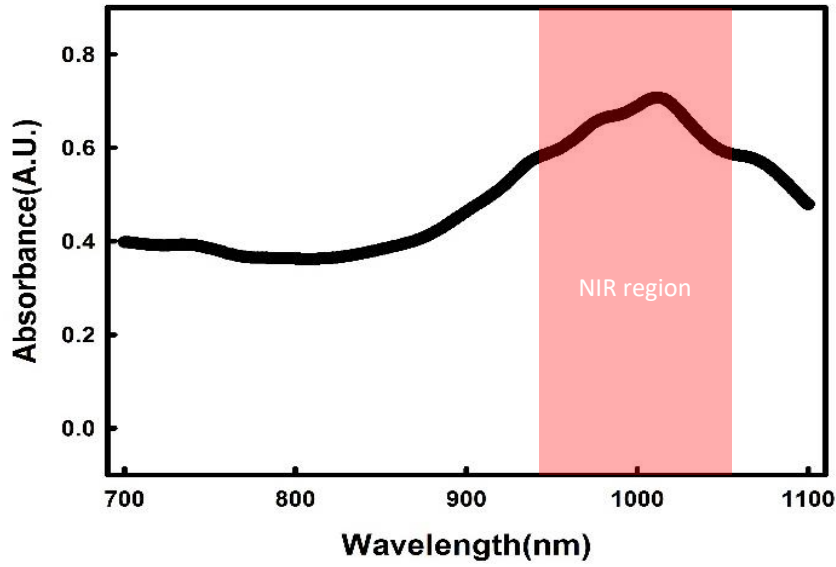
Figure 3.7 SWCNT film absorbance measurement over a wide range

4.3.   Device Parameters Extraction

Figure 3.8(a) is a basic lateral structure of a bottom-gate-top-contact SWCNT-PT. To obtain a plot of I_D versus V_{DS}, a direct current sweep was performed through an external bias applied to the gate electrode while the drain voltage V_D is swept from 0 to a certain value (source voltage $V_S = 0$). At $V_D = 0$ the drain current is 0 since there is no flow from drain to source in off state. As gate voltage is increase and reaches the linear region of operation at $V_{Gs} - V_T \geq V_{DS}$, drain current is linearly dependent on V_{DS}. Equation (3) below is the drain current in linear region, where W and L are he channel length and width, C_i and μ_{lin} are the insulator capacitance and the mobility of the device.

$$I_D = \frac{W}{L} . C_i . \mu_{lin} . (V_{GS} - V_T - \frac{V_{DS}}{2}) V_{DS} \qquad (3)$$

Also known as transfer characteristics through which device performance parameters can be evaluated. Some of the important parameters to verify device operation are in Equation (2), which is used to evaluate the drain current in the saturation region. When $V_{Gs} - V_T \leq V_{DS}$, the device is operating in a saturation region and drian current is evaluated by equation (4). Through this equation the extraction of threshold voltage (V_T) and the field effect mobility (μ_{FE}) are possible, where w/L is the width over the length of the device channel, C_i is the gate insulator capacitance. V_T and μ can be extracted by extrapolating the curve of the square root

of drain-source current (I_{DS}) versus the gate-source voltage (V_{GS}) at a fixed drain-source voltage (V_{DS}) as illustrated in Fig. 3.8(b). Equation (4) can be written as Eq. (5) and hence the threshold voltage and the CNT transistor field effect mobility μ_{FE} can be extracted from Eq. (6) and Eq. (7) respectively. On the other hand, on/off ratio can be evaluated by simply plotting drain current in logarithmic scale versus the gate voltage. This ratio is meant to be of a large value, which indicates the decrease in off current and hence a better performing device with minimum gate leakage.

$$I_D = \frac{W}{2L}\mu C_i(V_{GS} - V_{threshold})^2, \qquad V_{DS} \ll (V_{GS} - V_{threshold}) \qquad (4)$$

$$\sqrt{I_{DS}} = \sqrt{\frac{W}{2L}}\mu C_i V_{GS} - \sqrt{\frac{W}{2L}}\mu C_i V_{threshold} = AV_{GS} - B \qquad (5)$$

$$V_T = \frac{B}{A} \qquad (6)$$

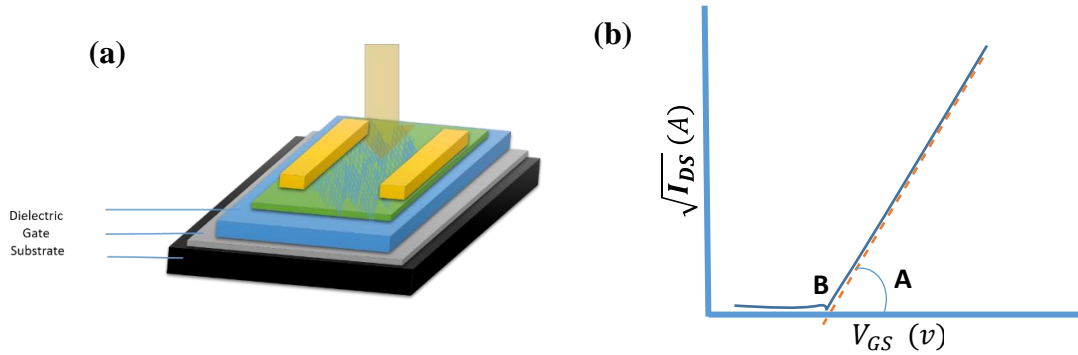$$\mu_{FE} = g_m L(V_d W C_i)^{-1} \qquad (7)$$

Figure 3.8 (a) Basic structure of a single-walled carbon nanotubes phototransistor. (b) Threshold voltage extraction method

Chapter 4 Results and Discussion

1. Improvement of Photosensitivity in SWCNT-PT by Selective Wetting Pattern

In this chapter, we discuss the results of the measurements and calculations performed according to the methods shared in chapter 3. We explain the behavior of the transfer curves and the response to the NIR laser illumination of the SWCNT-PT as a transistor and a NIR phototransistor under the pulsed exposure to a near-infrared laser source. The device substrate and insulator were Si/SiO2. Three notable results are worth mentioning and will be discussed in this section, one is the decreased gate leakage current, second is the increased on/off ratio, and the third is the consistenet hysteresis behavior in SWCNT-PT.

1.1. Leakage Current Reduction via Active Layer Patterning

The device based on patterned SWCNT film showed a remarkable decrease in leakage current of an order 10^{-2}, as is clearly depicted in Fig. 4.1. This decrease can be explained due to the elimination of parasitic pathways as the charge carriers in a patterned SWCNT thin film are constrained to the transistor channel and hence limiting the leakage current and reducing the potential for crosstalk. Due to the selective transfer of a fluoropolymer, a high water, and solvent resistant fluorocarbon-based polymer, on the surface of the dielectric so to only cover the intended active layer of the device, it was possible to pattern the film and confine the charge carriers. Previous research for gate leakage reduction has proved equally succesfull, howeer it required simutanouse annealing processes wich only increase labour.

1.2. Improvement of on/ off Ratio in Si/SiO2 Based SWCNT-PT

Figure 4.2 below demonstrates the transfer curve of the Si/SiO2 with and without the micropatterning of the SWCNT film (ID.P and ID respectively). Without the patterning step, on/off ratio of the Si-based transistor is 2.07×10^5, and shows a value of 2.27×10^5 when the SWCNT film is patterned. That is a difference of 0.2×10^5. As is visible from the figure, the off current reveals a great deal of decrease from an order of 10^{-9} to 10^{-10} due to the deposition of a patterned SWCNT film. It is expected to find a trade-off between high I_{on} and I_{on}/I_{off} ,

which can be due to the purity level of the semiconducting SWCNTs, in our case the device showed equal levels of on current while still increasing the on/off ratio notably.
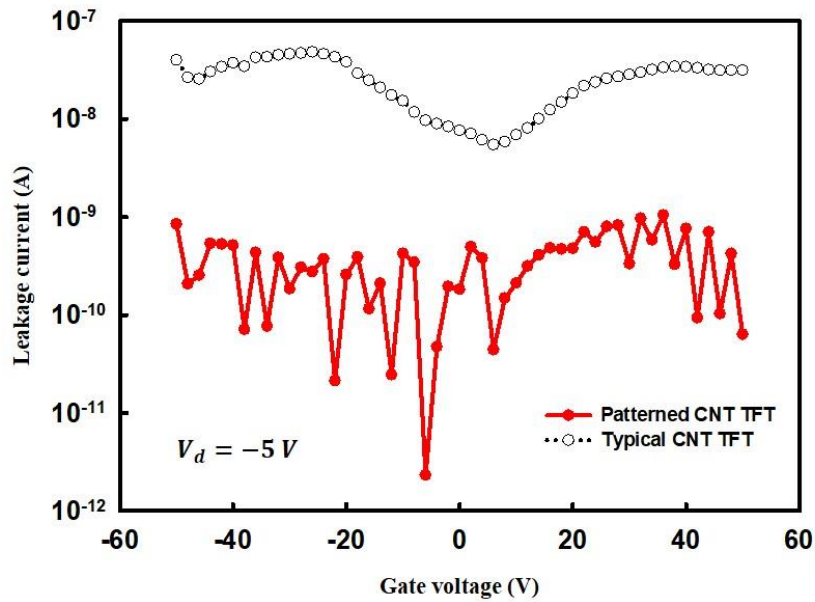

Figure 4.1 Gate leakage current improved as visible from the comparison of both devices (patterned and non-patterned).
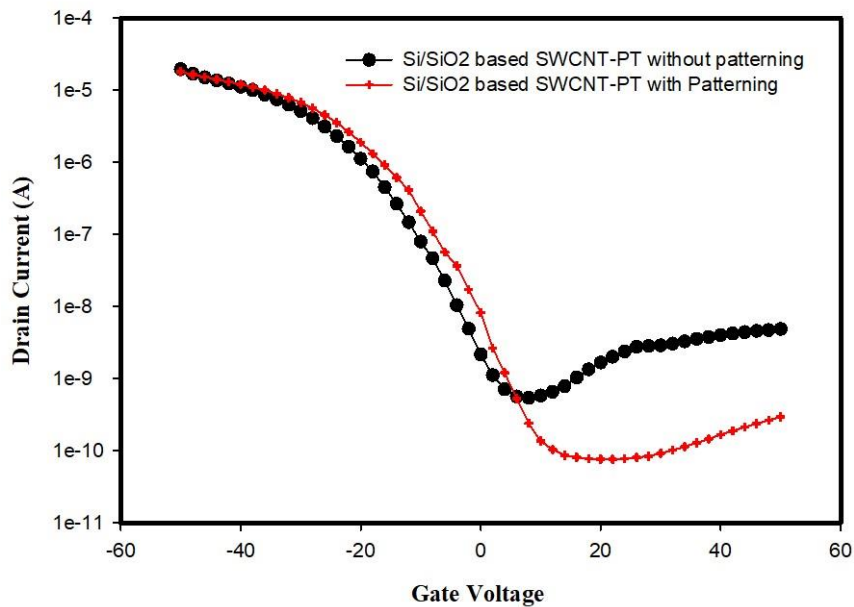

Figure 4.2 Drain current vs. Gate voltage of the Si/SiO2 based SWCNT transistors (patterned and non-patterned). On/off ratio increased visibly.

1.3. Hysteresis Effect in Si/SiO2 based SWCNT-PT

The first device (non-patterned) showed a threshold voltage shift of about $20.8\ V$. With the application of the patterned SWCNT film, V_T increased to about $29.9\ V$, which is a difference of $9.1\ volts$ in the hysteresis width between the two devices. Hysteresis is a common result of SCWNT devices, owing to several possible reasons, some of which we will explain here. Fig. 4.3 illustrates the SiO2 based device IV curve.

Hysteresis in CNT based FETs is a common and expected phenomenon, as observed in this device. It can be due to several common causes as is in metal oxide semiconductor (MOS) FETs, which can include Si/SiO2 interface trapped charges, fixed immobile oxide charges near the interface, mobile ionic charges, and oxide-trapped space charge associated with defects in SiO2. Woong Kim et al researches investigated the hysteresis in a single CNT FET, where they were able to conclude that charge trapping due to water molecules can be the main cause of hysteresis [21]. They discussed two types of charge trapping due to water molecules, one due to trappings at the Si/SiO2 interface and the other surrounding the CNT surface. In case of the interface traps, it depends on the silanol (Si-OH) groups on the SiO2 surface, where hydration can be caused by the bonding of water molecules through hydrogen bonds. In the latter case, water molecules are bound to the CNT surface and hence causing hydration, where vacuum pumping proved a suppressive solution for hysteresis.

We addressed this problem through the application of hydration preventative layers prior to the deposition of the SWCNT solution. However, it seems hysteresis never vanishes completely in CNT FETs, therefore more effective solutions are viable, such as the passivation of the SWCNT film using a hydrophobic layer that can prevent the penetration by water molecules through humidity in the ambient environment. Lefebvre et al demonstrated hysteresis-reduced CNT TFTs with hydrophobic dielectrics and passivation layers that proved effective [22].

(a)

(b)
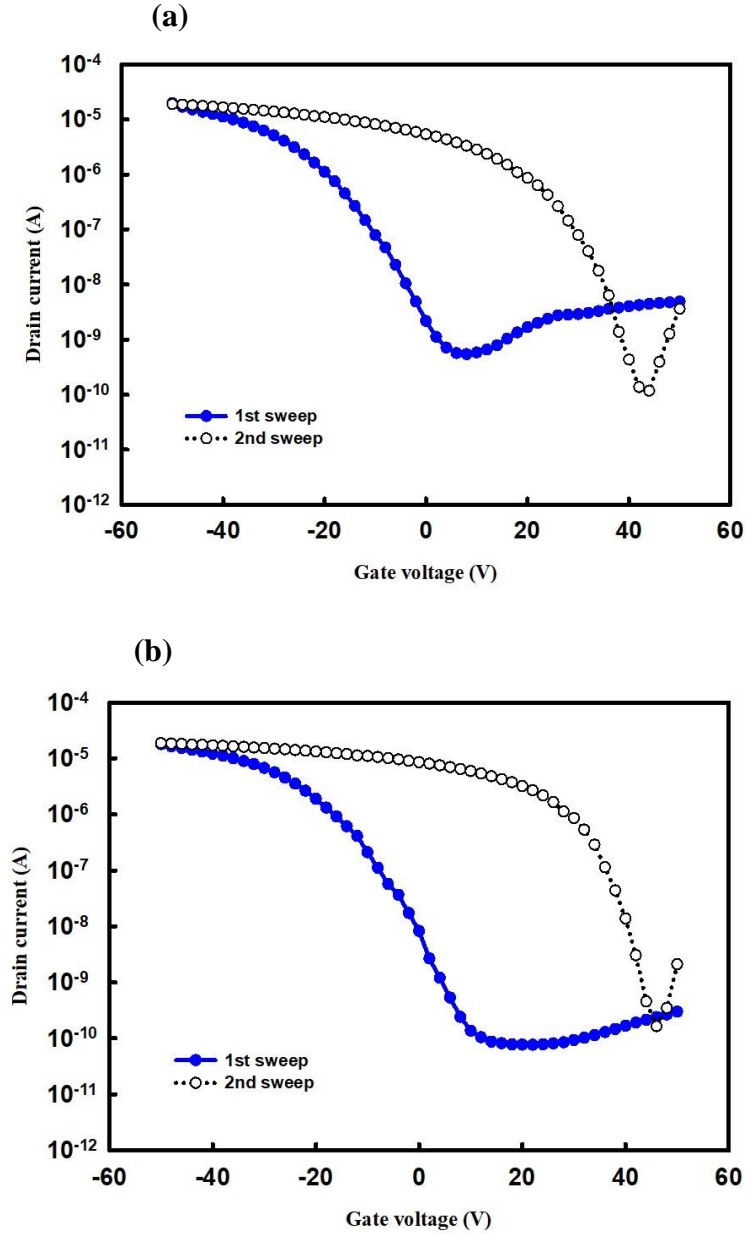
Figure 4.3 Drain current vs. gate voltage of SWCNT-PT (a) patterned and (b) non-patterned. Hysteresis is visible in both devices.

1.4.   Improvement of Photosensitivity via Active Layer Patterning

It is essential to point out here that the photo-response of the device was found dependent on the leakage current level. We established that for proper phototransistor operation a threshold of $I_G \leq 10^{-9}$ must be reached. In the inset of Fig. 4.4, the device shows no response to the NIR laser exposure, however, with the device that had a decreased level of leakage current it was possible to obtain a proper photoresponse as in Fig. 4.4. For SiO2 based

phototransistor through microcontact patterning, the dielectric surface of a transistor can be patterned by hydrophobic- hydrophilic regions. This causes a chemical change on the surface due to contact or due to the molecular transfer of the material to the targeted surface.

A transient (above the red line) and a steady-state response (below the red line) is present in the time-dependent measurement as can be seen from Fig 4.5. This can be explained due to the Extrinsic and Intrinsic behavior of the photocurrent. Due to the charge accumulation across the capacitor $SWCNT/SiO_2/Si$ and the illumination-induced band bending, a photocurrent displacement takes to rise, this is manifested as the transient. The steady-state response, on the other hand, is due to a rise in the positive photocurrent caused by the increased dissociation of photogenerated excitons. This increased dissociation takes place when a band bending is present at the electrode while there is a generation of photocarriers due to inter-band transitions in the SWCNTs. Sczygelski et al observed a similar behavior in SWCNT transistor with 99% purity of semiconducting CNTs [23].
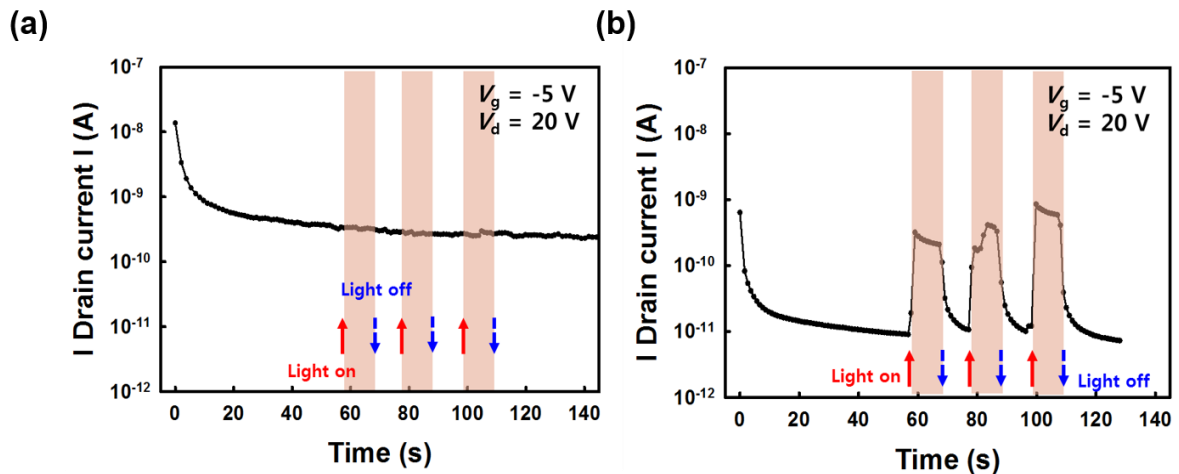
(a)   **(b)**

Figure 4.4 Dynamic photoresponse of (a) the non-patterned SWCNT-PT and (b) patterned one in a NIR laser pulse exposure (980nm, 100mW).
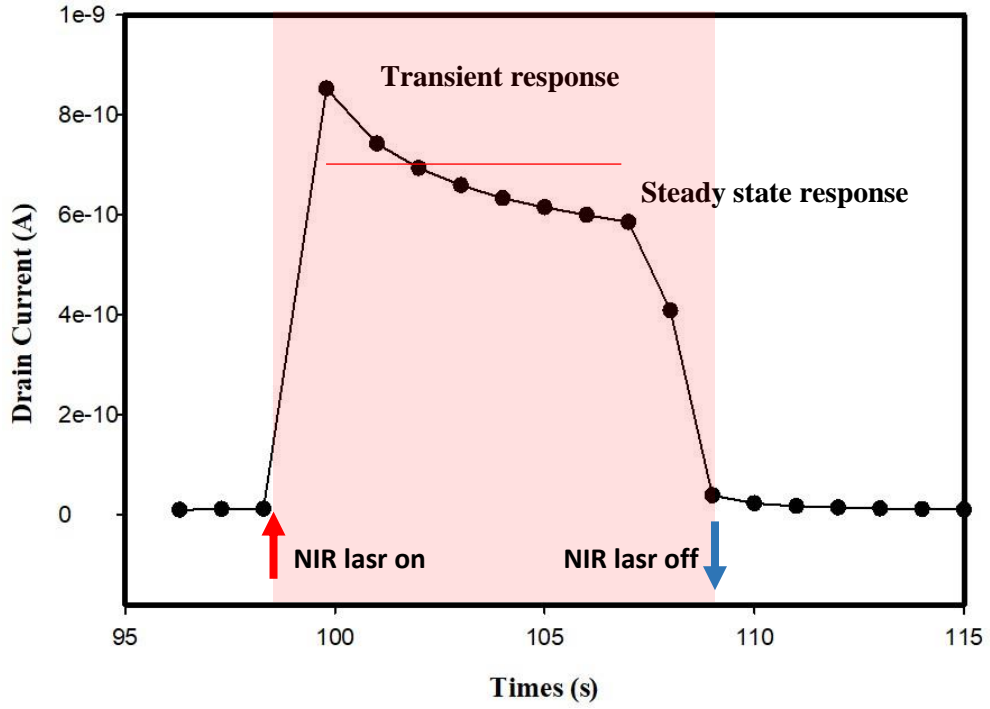
Figure 4.5 photo-response of the patterned SWCNT-PT in a pulsed NIR laser exposure

2. All-solution Processed SWCNT-PT

In this section, we investigate the photoresponse of the devices in question and compare the Si/SiO2 based phototransistor with the Glass/ITO/PVP phototransistor. We establish the applicability of the selective micropatterning technique on a glass substrate with a gate ITO. Since our interest lies in investigating the potential of this selective patterning method for phototransistor devices that require high mechanical flexibility, we apply the same method to an organic polymer gate dielectric instead of silicon dioxide. In light of that, we fabricated both devices following the procedure shared in the fabrication section and performed the IV characterization using the semiconductor parameter analyzer also following the exact same procedure.

1.1. Electrical Properties of PVP based SWCNT-PT

Figure 4.6 is the Drain current versus gate voltage of the organic-insulator based transistor. When we applied the selective patterning method on the SWCNT film of the Glass/ITO

substrate with PVP as the dielectric. Table 4.1 contains the values of on/off ratio and mobility of both devices.the on/off ratio in the PVP based device was found slightly lower, owing to the the quality of the organic insulator, the varying density of CNTsbetween both devices or the existence of metallic pathways in the SWCNT network.this is as well justifies lower mobility of PVP-based devices compared to SiO2 based. On/off ratio, in this case, was 9.19×10^5. Since cost-effective metallic free CNTs are not available, metallic pathways can increase at a higher density of the random network film. Sung-Jin Choi et al examined FETs with SWCNT purity of 99% and 90%, yet the same tradeoff is as well observed even with 1% metallic concentration in the SWCNT solution [24]. They demonstrated a spin alignment method for overcoming this by reducing tube-tube contact in the network, Nonetheless, our patterning method effectively reduces the off current while maintaining the on current at almost the same levels without using additional alignment techniques. And therefore proving to be less costly and require less labor at the same time.
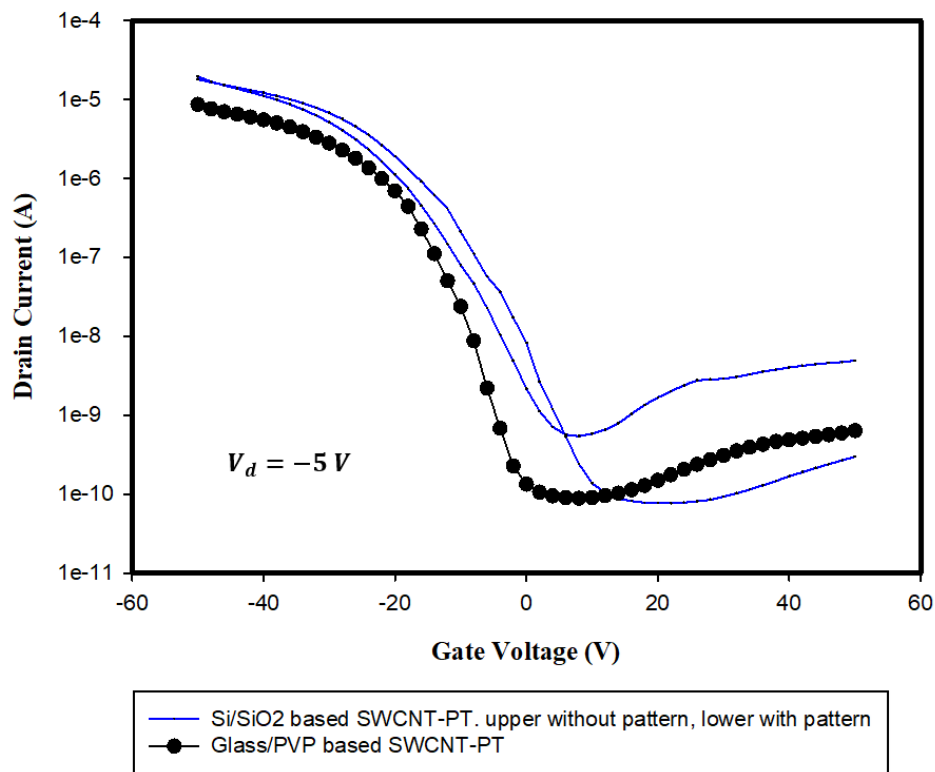

Figure 4.6 SiO2 based SWCNT-PT vs PVP based device

Table 4-1 Summarized values of electrical performance parameters (on/off ratio and mobility) of SiO2 and PVP based SWCNT-PT with a patterned CNT layer

	On/off ratio	Field Effect Mobility (cm^2Vs^{-1})
SiO2-based PT	$\mathbf{20.7 \times\times\times 10^4}$	$\mathbf{1.3}$
PVP-based PT	$\mathbf{7.86 \times 10^4}$	$\mathbf{9.49 \times 10^{-1}}$

1.2. Hysteresis in PVP based SWCNT-PT

The *IV* curve of several devices on the substrate, all fabricated with the same technique and under the same conditions. As we explained in the last section, hysteresis can be a cause of water molecules at the interface of the dielectric and the semiconductor, or it could be the result of the absence of the passivation. Since all of our devices were measured in ambient environments, there is a high possibility that water molecules may have gathered at the interface os Si/SiO2 or surrounding the CNT. However, one would expect that using the hydrophobicity control treatment via patterning may reduce the hysteresis. In this case, it seems even that did not suppress the hysteresis, which leads us to one possible reason, the absence of a barrier between the atmospheric humidity and the CNT film. Fig. 4.7 below shows the IV curve of the device.

We noticed a variation in the threshold voltage shift even among devices of the same sample, which can be attributed to the variation in SWCNT densities between the devices. Hiroo H. et al investigated the effect of carbon nanotube density on random network channel transistors on the device hysteresis behavior [25]. They proved that the device hysteresis is dependent on the CNT-density in the channel. Smaller hysteresis can result due to the higher density of CNTs, which we explain as follows. In case of a small dispersion density of CNTs in the channel, the inter-CNT distance, which determines the potential profile at the CNT-insulator interface, is larger. The large hysteresis is, in fact, a result of the large electric field compiling at the interface and leading to a large charge injection from the channel to the insulator. When there is an accumulation of a large number of charges at the insulator, it gives

rise to large hysteresis. In case of a dense network, SWCNT-PT will approach the parallel plate capacitor model due to the equipotential lines distribution dropping the potential barrier.
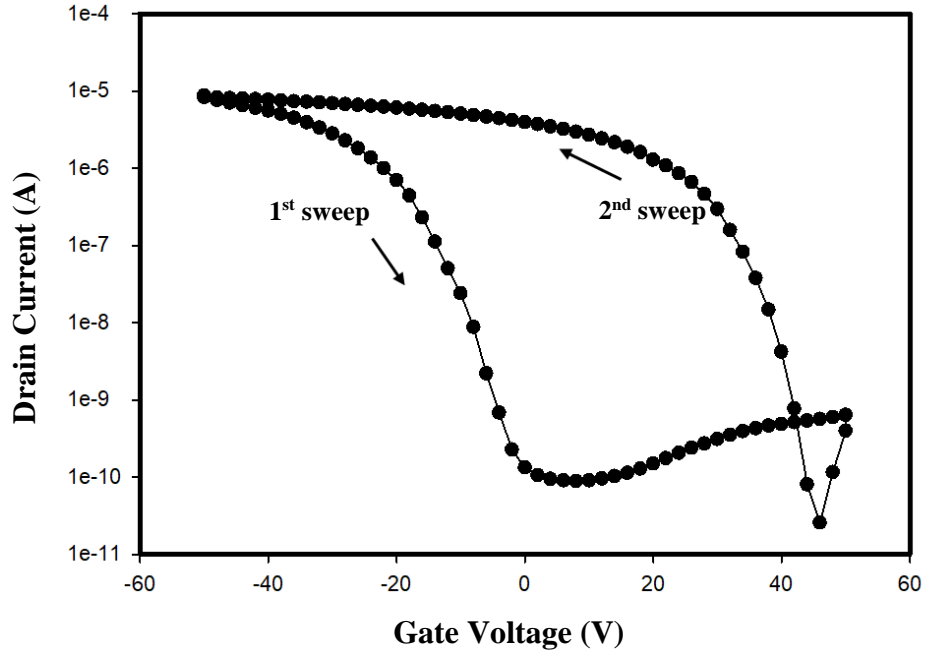

Figure 4.7 PVP based SWCNT-PT drain current vs. gate voltage

1.3. Photoresponse of PVP based SWCNT-PT

The photoresponse of the PVP base SWCNT-PT in comparison with the SiO_2 based PT is presented in Fig. 4.8, and its steady-state and transient photocurrent are clearly observable in Fig. 4.9. Table 4.1 compares the photosensitivity and photocurrent values of both phototransistors. The photoresponse of the PVP based device shows a steady state and a transient response as expected. With this result, we confirm the applicability of our solution process of selective micro-patterning to pattern the PHB layer for selective deposition of a thin film of SWCNT on a polymer dielectric, and as well the potential in mechanically flexible NIR phototransistors. With a significant decrease in leakage current owing to the selective wetting patterning of the film, then the values of photosensitivity (P) and photocurrent (I_{photo}) were measured to obtain the values in table 4.1. The photocurrent in this case was calculated as the difference between the current in dark and under illumination as obtained from the drain current vs time curves.

It can be noted that the photosensitivity in the PVP-based device is much smaller than that of the SiO2-based. This can be attributed to the fact that the mobility in PVP, in general, is much smaller than that of SiO2- based devices. Our device may exhibit low mobility and more low P compared to higher performing devices in recent research works, however, it clearly shows an improved sensitivity and performance using the cost and labor effective patterning concept we employed. The lower P is explained due to the low mobility as discussed previously.
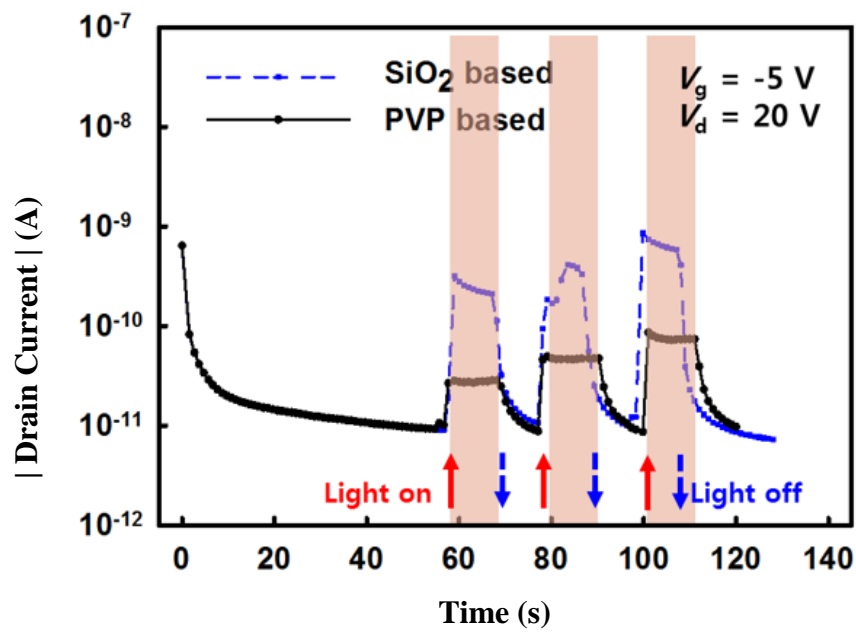
Figure 4.8 Dynamic photoresponse of the PVP based SWCNT-PT and the SiO2 based PT under a NIR laser pulse exposure (980nm, 100mw).
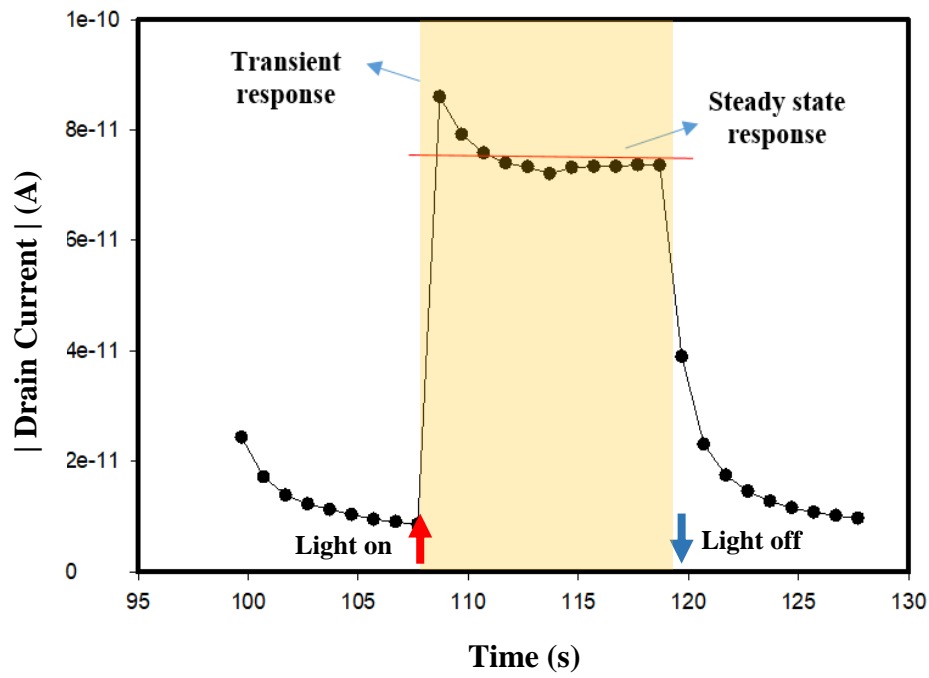
Figure 4.10 transient and steady-state response pf pvp based swcnt-pt

Table 4-2 Comparison of SWCNT-phototransistor performance parameters

	Si-Based Device	PVP-Based Device
P	84	10
R	$8.43 \times 10 - 9$	$6.3 \times 10 - 9$
I_{photo}	$8.43 \times 10 - 10$	$6.3 \times 10 - 10$

Chapter 5 Conclusion

In this thesis, we investigated the effect of selective micropatterning on SiO_2 and PVP dielectric-based SWCNT transistor. First, we investigate the effect on transistor performance of a Si/SiO_2 and Glass/ITO/PVP based FET, where the SWCNT random network was drop cast on the insulator surface and electrodes are evaporated on top of it. For the Si-based devices, one was fabricated without micro-patterning, both devices were characterized to analyze the on/off ratio and the leakage current level. Because we aim to study the applicability of this patterning method for flexible organic-insulator based SWCNT transistors, the organic-insulator based device with a patterned hydrophobic barrier for the selective deposition of SWCNT film was as well characterized for the same parameters.

We found that Si-based device showed an increased I_{on}/I_{off} ratio, which is attributed due to the off current reduction that could be caused by the metallic pathways in the SWCNT film. We also established that a tradeoff between high on current and high on/off ratio commonly exists in SWCNT transistors. We also successfully obtained a very similar IV curve with the organic-insulator device. We also analyzed the threshold voltage shift, which was shifted to the positive in all devices. We explain the non-vanishing hysteresis in all the devices to be because of the water molecules acting as charge traps at the insulator/semiconductor interface or surrounding the CNT. Since our devices were not passivated from the ambient environment, humidity could easily penetrate through to cause this effect. We also noted that hysteresis was not the same among various devices of the same sample even though they were fabricated using the same process. This is because of the varying SWCNTs density in the networks of each device. In other words, higher density CNT networks will reveal a parallel-plate model like phenomenon, and hence a small density of SWCNTs will drop the barrier and reduce the accumulation of charge at the insulator and therefore reducing the hysteresis. In addition to that, we noticed an effective decrease in leakage current in the device employing a patterned thin film. The selective-micro-pattern surface hydrophobicity control assisted in confining the leakage charge carriers and eliminated parasitic pathways.

Second, we studied the photoresponse of both devices that employed a patterned SWCNT film (Si-based and organic-insulator based). We observed an improved photosensitivity only for the devices revealing leakage current of a certain threshold level. after which we were able to obtain the dynamic time-dependent photoresponse of both devices to

observe, as is commonly observed in SWCNT transistors, a combined intrinsic and extrinsic photocurrent response. We attribute the transient photocurrent (extrinsic) to the illumination-induced band bending and charge accumulation across the capacitance, and the steady-state photocurrent (intrinsic) to the SWCNT inter-band absorption photo-generated excitons dissociation.

In summary, this thesis presents a technique for enhancing SWCNT-PT photosensitivity by reduction of gate leakage current through a PHB patterned using flouropolyer transferred from PDMS stamp, which assists in the selective deposition of SWCNT film. After studying the transfer characteristics and the photo-response of the devices employing the patterned films, we conclude that it is possible to fabricate a solution processable SWCNT phototransistor in the NIR band that will have the flexibility and cost-effectiveness required for the new generation electronics, while as well exhibiting improved photosensitivity to light exposure. If applied to an aligned network of CNT instrad of a random one, and with a passivation layer, this method could serve for highy performing carbon nanotube phototransistors.

Bibliography

[1] L. J. Gou, "Nanoimprint lithography : Methods and Material Requirments," *Advanced Materials,* vol. 19, p. 495, 2007.

[2] K. . C. Dickey, S. Subramania, J. E. Anthony, L.-H. Han, C. Shaochen and Y.-L. Loo, "Large-area patterning of a solution-processable organic semiconductor to reduce parasitic leakage and off currents in thin-film transistors," *Applied Physics Letters,* vol. 90, no. 24, 2007.

[3] H. Chen, C. K. C. Lai, K. w. C. Lai, C. K. M. Fung and R. Yang, "Development of infrared detectors using single carbon-nanotube-based field effect transistor," *IEEE transaction on nanotechnology,* vol. 9, no. 5, p. 582, 2010.

[4] M. H. Kuo, W. T. Lai, T. M. Hsu, Y. C. Chen, C. W. Chang, W. H. Chang and P. W. Li, "Designer germanium quantum dot phototransistor for near-infrared opticaldetection and amplification," *Nanotechnology,* vol. 26, no. 5, p. 0957, 2015.

[5] Z. Sun, J. Li and F. Yan, "Highly sensitive organic near-infrared phototransistors based on poly(3-hyxelthiphene) and PbS quantum dots," *Journal of Materials Chemistry,* vol. 22, p. 21673, 2012.

[6] H. Xu, J. Li, B. H. K. Leung, C. C. Y. Poon, B. S. Ong, Y. Zhang and . N. Zhao, "A high sensitivity near-infrared phototransistor based on an organic bulk heterojunction," *Nanoscale,* vol. 5, p. 11850, 2013.

[7] I. Manunza, A. Sulis and A. Bonfiglio, "Organic semiconductor field effect transistors for unconventional applications: flexible sensors and wearable devices," in *International Workshop on Wearable and Implantable Body Sensor Networks (BSN'06)*, Cambridge, MA, 2006.

[8] T. Durkp, S. A. Getty, E. Cobas and M. S. Fuhrer, "Extraordinary Mobility in Semicondcuting Nanotubes," *Nano Letters,* vol. 4, no. 1, p. 35 , 2004.

[9] Liangbing Hu, David S. Hecht and George Gru¨ner, "Carbon Nanotube Thin Films: Fabrication, Properties, and Applications," *Chem. Rev.,* vol. 110, p. 5790, 2010.

[10] Liangbing Hu, David S. Hecht and George Grüner, "Infrared transparent carbon nanotube thin films," *Applied Physics Letters,* no. 94, p. 081103, 2009.

[11] Z. Bao and M. M. Ling, "Thin Film Deposition, Patterning and Printing in Organic Thin Film Transistors," *Chemical Materials,* vol. 16, no. 23, p. 4824, 2004.

[12] S. H. Chae and Y. H. Lee, "Carbon Nanotubes and Graphene Towards Soft Electronics," *Nano Convergence,* vol. 1, no. 5, 2014.

[13] R. Bell, "The Structural and Electronic Properties of Carbon Nanotubes," in *Conduction in Carbon Nanotube Networks*, 2015, p. 9.

[14] P. Avouris, M. Freitag and V. Perebeinos, "Carbon Nanotube Photonics and Optoelectronics," *Nature Photonics,* vol. 2, p. 341, 2008.

[15] H. Chen, N. Xi, K. W. C. Lai, Fung, Carmen Kar Man and Yang, Ruiguo, "Development of Infrared Detectors Using Single Carbon-Nanotube-Based Field-Effect Transistors," *IEEE,* p. 582, 2010.

[16] R. Bell, "The Structural and Electronic Properties of Carbon Nanotubes," in *Conduction in Carbon Nanotube Networks*, 2015, p. 9.

[17] K. Liu, Y. Sun, L. Chen, C. Feng, X. Feng, K. Jiang, Y. Zhao and S. Fan, "Controlled growth of super-aligned carbon nanotube arrays for spinning continuous unidirectional sheets with tunable physical properties.," *Nano Letters,* vol. 8, no. 2, p. 700, 2008.

[18] Y. Kim, N. Minami, W. Zhu, S. Kazaoui, R. Azumi and M. Matsumoto, "Langmuir–Blodgett Films of Single-Wall Carbon Nanotubes: Layer-by-layer Deposition and In-plane Orientation of Tubes," *Jpns. J. Appl. Phys,* vol. 42, no. 12, pp. 7629 - 7634, 2003.

[19] X. Wang, "Surface Energy Patterning and Optoelectronic Devices Based on Conjugated Polymers," 2006.

[20] C.-M. Keum, J.-H. Bae, M.-H. Kim, W. Choi and S.-D. Lee, "Solution-processed low leakage organic field-effect transistors with self-pattern registration based on patterned dielectric barrier," vol. 13, no. 5, p. 778, 2012.

[21] W. Kim, A. Javey and O. Vermesh, "Hysteresis Caused by Water Molecules in Carbon Nanotube Field-Effect Transistors," *Nano Letters ,* vol. 3, no. 2, p. 193, 2003.

[22] J. Lefebvre, J. Ding, Z. Li, F. Cheng, N. Du and P. R. L. Malenfant, "Hysteresis free carbon nanotube thin film transistors comprising hydrophobic dielectrics," *Applied Physics Letters,* vol. 107, no. 24, p. 243301, 2015.

[23] E. Sczygelski, V. S. Sangwan, C.-C. Wu, . H. N. Arnold, K. Everaerts, T. J. Marks, H. C. Mark, . L. J. Lauhon, Avouris P, Chen Z and Perebeinos V, "Extrinsic and intrinsic photoresponse in monodisperse carbon nanotube thin film transistors," *Applied Physics Letters,* vol. 102, no. 8, p. 083104, 2013.

[24] S.-J. Choi, C. Wang, C. C. L, P. Bennett, A. Javey and J. Bojor, "comparatie study of solution-processed carbon nanotube network transistor," *Applied Physics Letters,* vol. 101, p. 112104, 2012.

[25] H. Hongoa, F. Nihey and S. Yorozu, "Relationship between carbon nanotube density and hysteresis charecteristic of carbon nanotube random network-channel field effect transistor," *Journal of applied physics,* vol. 107, no. 9, 2010.