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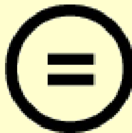

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Abstract

Fabrication of nano textured silicon through metal-assisted chemical etching (MACE) technique has attracted attention as a simple, low-cost and versatile technique for producing antireflective silicon layer. In this study, a novel single-step nickel assisted etching technique was applied to fabricate an antireflective, nonporous mono c-Si (black Si) in an aqueous solution containing hydrofluoric acid (HF), hydrogen peroxide (H_2O_2) and $NiSO_4$ at 40^oC. Field emission scanning electron microscope was used to characterize different morphologies of the textured Si. Optical reflection measurements of samples were carried out to compare the reflectivity of different morphologies. Results indicated that vertical as well as horizontal pores with nanosized diameters were bored in the Si wafer after 1hour treatment in the wet electroless etching solution containing different molar ratios of H_2O_2 to HF. Increasing H_2O_2 concentration in electrochemical etching solution had a considerable influence on the morphology of textured Si due to higher injection of positive charges from nickel atoms onto the silicon surface. Optimized concentration of H_2O_2 led to formation of an nanoporous antireflective Si layer with 2.1% reflectance of incident light.

Result indicated that further increase in molar ratio of H_2O_2 to HF led to formation of a cobblestone structure of silicon which dramatically enhance the reflection of incident light. nickel assisted etching technique

also was applied for producing an antireflective nano-scale porous structures on multi-crystalline silicon wafer. It was observed that nanotextured multi c-Si fabricated through optimized ration of oxidation agent to HF exhibited lower reflection than standard isotropic texturing using a standard acid solution. As a final step, the optimized texturing process was applied to fabricate multi c-si solar cell devices showing promising results regarding cell performance parameters.

In the second part of my study, Light Induced Electroless Plating technique was applied to deposit Ni seed layer on the n-side of a silicon diode structure. Morphology of the nickel seed layer and phase characterization of nickel silicide at different bath conditions and annealing temperatures was examined through scanning electron microscopy, X-ray diffractometer and Raman spectroscopy respectively. Moreover, transmission line measurement (TLM) technique was employed to determine the contact resistance of Ni/Si stack after thermal treatment and to understand its correlation with the chemical-structural properties. Results indicated that low electrical resistive mono-silicide (NiSi) phase as low as 5 mΩ.cm2 was obtained in temperature range of 450°C to 500°C.

Keyword : silicon, nickel, nanoporos, reflectin, metal assisted etching, metallization

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CHAPTER1.

Application of nickel for fabrication of nanoporous silicon

1.1. Introduction

1.1.1 Human Energy Consumption.

The human body is at a constant temperature of about 37°C. It hence contains thermal energy. As the body is continuously cooled by the surroundings, thermal energy is lost to the outside. Further, blood is pumped through the blood vessels. As it travels through the vessels, its kinetic energy is reduced because of internal friction and friction at the walls of the blood vessels, i.e. the kinetic energy is converted into heat. To keep the blood moving, the heart consumes energy. Also, if we want our body to move this consumes energy. Further, the human brain consumes a lot of energy. All this energy has to be supplied to the body from the outside, in the form of food. A grown up average body requires about 10 000 Kilojoule every day.1 We can easily show that this consumption corresponds to an average power of the human body of 115.7 W. In modern society, humans do not only require energy to keep their body running, but in fact we consume energy for many different purposes. We use energy for heating the water in our houses and for heating our houses. If water is heated, its thermal energy increases, and this energy must be supplied. Further, we use a lot of energy for transportation of people and products by cars, trains, trucks and planes. We use energy to produce our goods and also to produce food. Many people believe that tackling the energy problem is amongst

the biggest challenges for human kind in the 21st century. It is a challenge because of several problems: The first challenge the human kind is facing is a supply-demand problem. The demand is continuously growing. The world population is still rapidly growing, and some studies predict a world population of 9 billion around 2040 in contrast to the 7 billion people living on the planet today. All these people will need energy, which increases the global energy demand. Further, in many countries the living standard is rapidly increasing like China and India, where approximately 2.5 billion people are living, which represents more than a third of the World's population. Also the increasing living standards lead to an increased energy demand. According to the IEA World Energy Outlook 2013, the global energy demand growed about one third from 2011 to 2013. The increasing demand in energy has economic impact, as well. If there is more demand for a product, while supply does not change much, the product will get more expensive. This basic market mechanism is also true for Energy [1].

1.1.2 Renewable Energy Vs Nonrenewable Energies.

Fig 1.1 shows different energy sources and the ways we utilize them. We see that usually the chemical energy stored in fossil fuels is converted to usable forms of energy via heat by burning, with an efficiency of about 90%. Using heat engines, thermal energy can be converted in to mechanical energy. Heat engines have a conversion efficiency of up to 60%. The far majority of the current cars and trucks works on this principle. Mechanical energy can be converted in to electricity using electric generators with an efficiency of up to 99%. Most of the World's electricity is generated with an turbo generator that is connected to a steam turbine, where the coal is the major energy source. Along all the process steps of making electricity out of fossil fuels, at least 50% of the initial available chemical energy is lost in the various conversion steps. Chemical energy can be directly converted into electricity using a fuel cell. The most common fuel used in fuel cell technology is hydrogen. Typical conversion efficiencies of fuel cells are 60%. A regenerative fuel cell can operate in both directions and also convert electrical energy into chemical energy. Such an operation is called electrolysis; typical conversion efficiencies of hydrogen electrolysers of 50-80% have been reported. In nuclear power plants, energy is released as heat during nuclear fission reactions. With the heat steam is generated that drives a

steam turbine and subsequently an electric generator just as in most fossil fuel power plants. However, in the case of Photovoltaic the energy is directly converted to electricity [2].

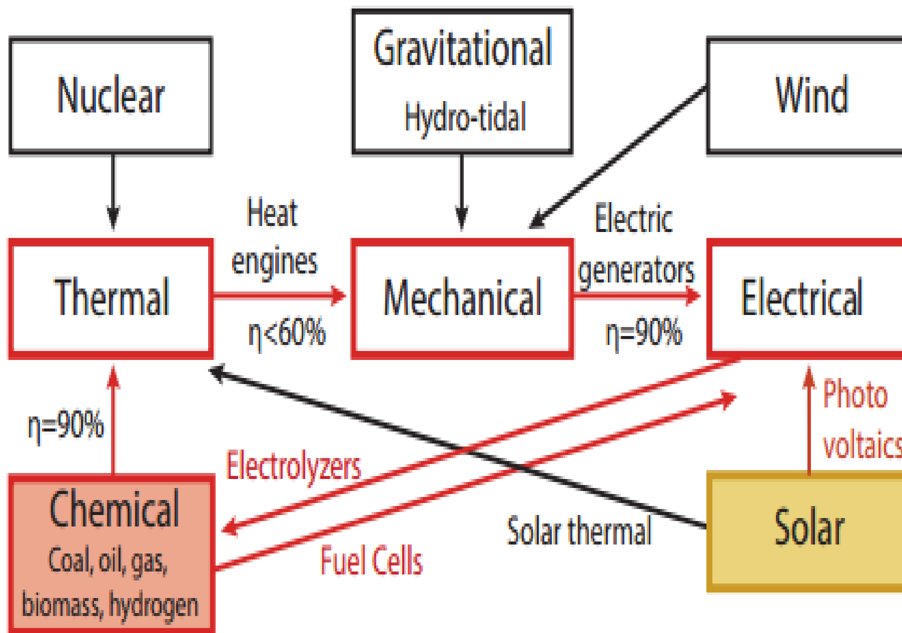


Fig 1.1 The different energy carriers and how we utilize them

1.1.3 Photovoltaic

In 1839, Edmund Becquerel (a French Physicist), on his article referred to his experiment " Action of Radiation on the Metal Blades" which led to following conclusion. "In summary this dissertation reveals the following facts. When rays containing the most refrangible rays of sunlight are facing with metal blades immersed in a liquid, such action results in electrical effects which cannot be attributed to a heat source"[3]. This being the first known observation of PV electricity generation, comes more than 2500 years after the use of solar energy as a tool for lighting fires by human being via concentration lenses. After years in 1873, Willoughby Smith, an English technician, realized that the electrical conductivity of selenium bars would change under the influence of solar radiation, being the first one observing photoconductivity[4]. After that, two additional studies on Se verified the PV effect consecutively[5]. However, The first Silicon PV cell having a P-N junction with 6 % efficiency was fabricated at Bel laboratory[6]. Later on scientists and engineers succeeded to fabricate solar cell that can convert up to 46% power efficiency through employing different technique [7]. Time line for solar cell efficiency according to highest efficiency is given in Fig1.2[8].

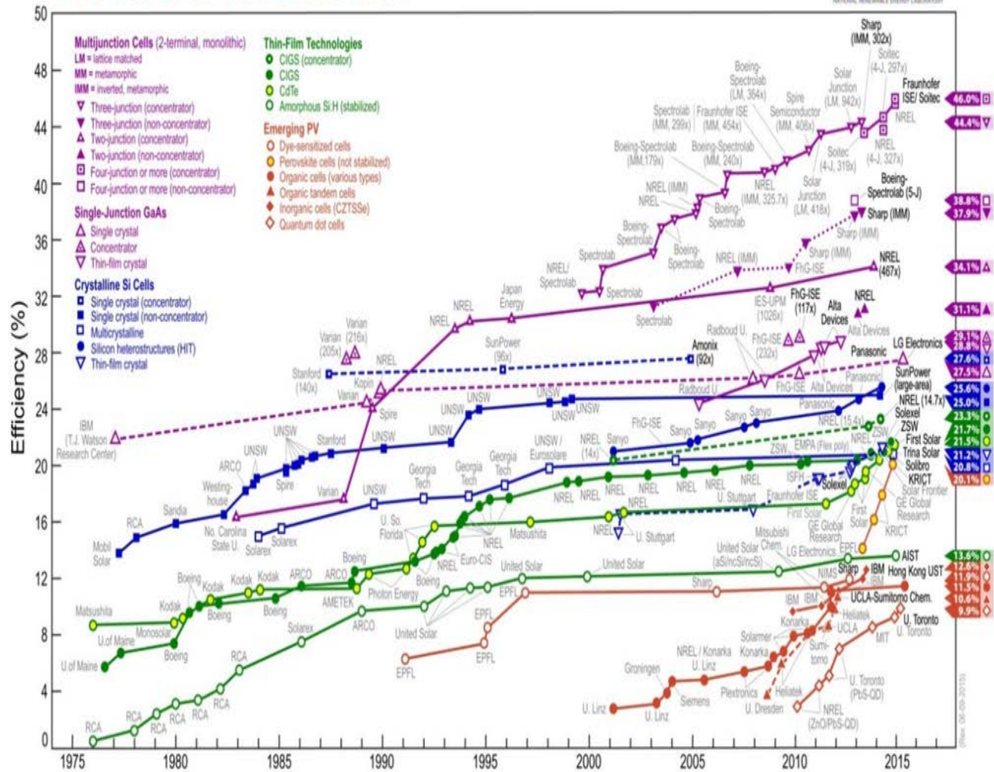


Fig 1.2 Timeline for non-concentrated PV efficiency development adapted from NREL best research cell efficiency graph.

1.1.3.1 Structure of silicon solar cell

1.1.3.1.1 Full Area Back Surface Field Cell.

Full area back surface field p type solar cell, called as. Al, BSF cell, constitutes the major part of the c-Si PV market today. As obvious from the cross sectional structure, it has a homogeneously doped emitter and back surface filed; a passivation layer on top of the emitter which also act as an antireflective coating and front/back metallization (Fig 1.3).

The homogeneous doping of emitter and BSF is its main technological advantage arising from process simplicity. On the other hand, the requirements of the low resistance Si-metal contacts entail a high doping concentration in the emitter which results in high front surface recombination loss. In addition, full area back contact cause high back surface recombination velocities. As a result, the device has an easy to fabricate structure that suffer from high surface recombination losses. Same Structure with n type base is also produced where emitter is p doped and BSF is formed by n doped. However, the simplicity somewhat sacrificed since n type base requires single side diffusion on the back side which is not necessary for its P based counterpart where BSF is spontaneously formed by liquid phase epitaxy of Al on Si which leads to P plus doing

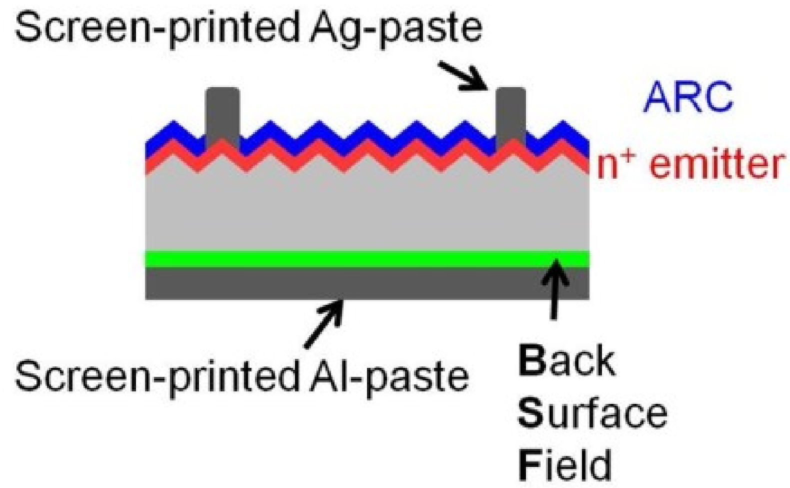


Fig 1.3 Full area back surface field solar cell structure

1.1.3.1.2 passivated Emitter Rear Cell (PERC)

In order to further decrease the recombination losses, in this technology, a back surface of the cell is passivated (Fig 1.4) by SiOx/AlOx-HfOx/SiNx stacks. However, since the passivation maintained by this insulator stack prevents current flow, local opening are formed on the dielectric film to enable contacts to the silicon surface. The competition between FF and Voc due to resistive losses respectively is optimized by providing a certain metal fraction on the back surface. Today's PERC cells have efficiencies as much as 22.1% for p type material [9] with an increasing market share due to the developments in production technology such as single side etching and laser structuring.

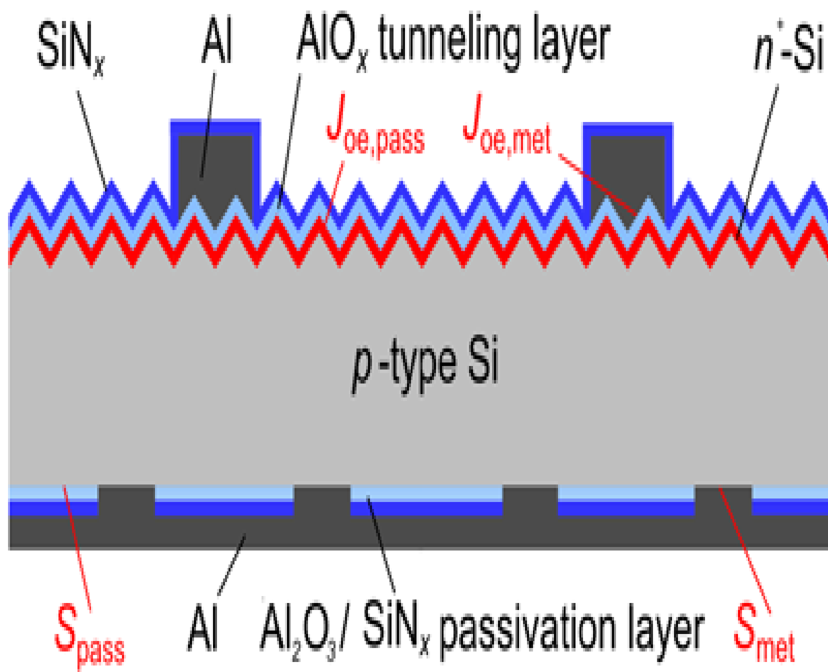


Fig 1.4 PERC structure

1.1.3.1.3 Passivation Emitter Rear Locally Diffused Cell

Although the PERC cell has a good back surface passivation, the contacting between the metal and the base material causes high resistive losses since the doping level of the base is usually kept low. To solve this problem, the back surface of the cell is locally doped with high concentration through the dielectric openings. Thus the metal-Si contact attains a lower resistance and the local doping acts as an electric mirror keep minority carriers away from the surface (Fig 1.7). Efficiencies as high as 25% have been reported for this kind of structure [10].

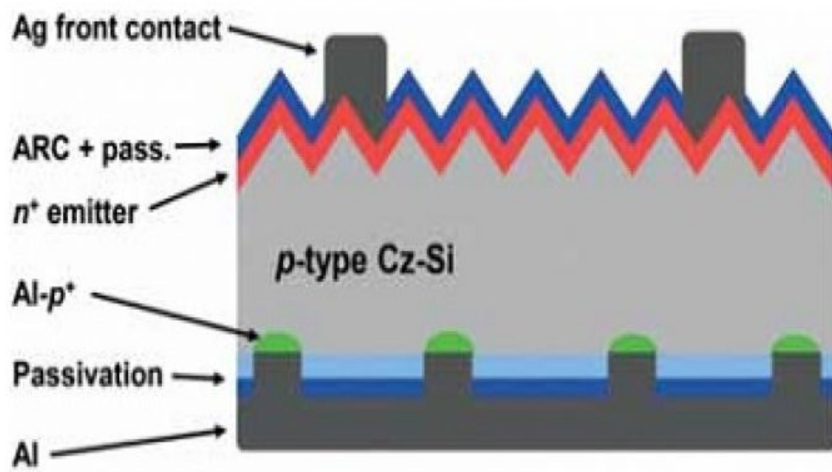


Fig 1.5 PERL Structure

1.1.3.1.4 Interdigitated back contact solar cell (IBC)

In order to get rid of the shadowing losses due to front side metallization, all contacts and therefore the p-n junction are placed to the rear side of the cell. This process not only helps to get higher current from the cell but also allows very large cross sectional area metallization which reduce series resistance losses (Fig 1.6). Despite these advantages, requirement for very high quality surface passivation, high bulk lifetimes and complicated back surface structuring are the technological handicape of this structure. Efficiencies as high as 25.2% have been reported for n type of c-Si IBC solar cells[10].

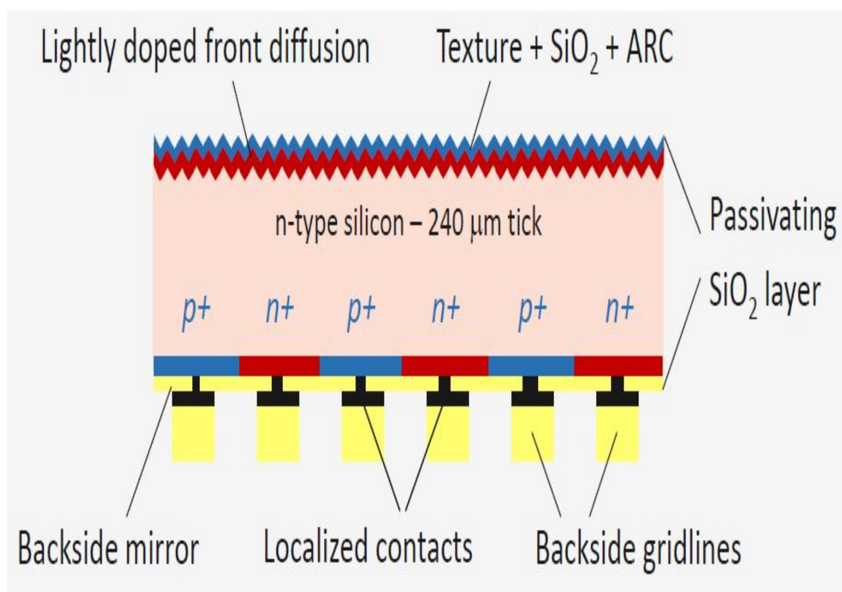


Fig 1.6 IBC structure

1.1.4 light trapping

Crystalline silicon solar cells are the dominant technology for solar panels, accounting for nearly 90% of the present market share. Crystalline silicon solar cells have achieved ~25% power conversion efficiency (PCE) in small area laboratory cells and up to 22% in larger area panels [11]. The silicon wafers utilized in solar panels are typically 180 μm thick and it is clear that a c-Si wafer with a thickness of the order of hundred micrometers will suffer from transmission losses (Fig 1.7). In the end, for c-Si, a competition between absorption of minority carriers occurs.

In order to solve the problems arising from insufficient absorption and limited diffusion length, increasing the optical path of the photon inside the semiconductor, " light trapping" , is preferred. With light trapping, the incoming photon the material thicker that it is in reality while created e-h pairs can travel along the semiconductor without recombination till separated by the junction. In 1982, Eli Yablonovitch and George D. Cody calculated the intensity enhancement factor limit for semiconductor sheets using statistical mechanical approaches as'4n2', called 'Yablonovitch Limit' where n is the refractive index of the semiconductor[12]. Hence, the material costs associated with thick silicon wafers are a considerable component of the system costs. It is of great interest to thin the c-Si wafers considerably, and employ recently developed light-trapping techniques[13]. As is well known, the reflectance of a silicon wafer after being sliced is so high that the maximal

photoelectric conversion efficiency of silicon-based solar cells is limited. Therefore, an alkaline texturization process has been used for silicon solar cells in industrial production. But the reflectance of this alkaline textured wafer is still greater than 10 %, and this process can only be used for monocrystalline silicon solar cells.

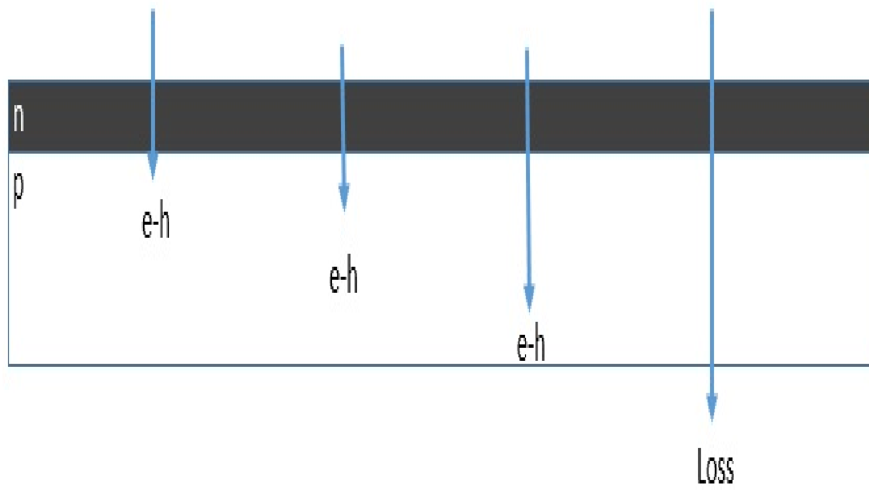
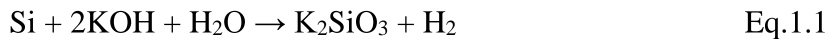


Fig 1.7 A wafer thinner than minority carrier diffusion length. All generated carriers may be collected while some portion of the spectrum is lost.

For mono c-Si, commonly alkaline etching is used as the texturing method [14]. This process takes the advantages of anisotropic etching property of KOH along (100) and (111) crystallographic planes. Etch rate of KOH for (100) plane can be as much as 600 times higher than that of (111) direction with the following reaction.



$$Si + 2KOH + H_2O \rightarrow K_2SiO_3 + H_2 \qquad \text{Eq.1.1}$$

The reaction results in a textured surface of micro pyramids with (111) oriented faces which can be considered as each stop for KOH etching. However, for multi-c Silicon, since there are several grains with different crystal orientations on the surface, anisotropic alkaline texturing is not applicable. Instead, HF, HNO_3, H_2O_2 bearing isotropic stain etching solution are used to form random texturing on the surface. During this process, HNO_3 is used for oxidation for Si and HF is used for etching of SiO_2.

$$Si + HNO_3 + 6HF \rightarrow H_2SiF_6 + HNO_3\, H_2O + H_2 \qquad \text{Eq. 1.2}$$

In addition to the previous standard methods, many other methods have been developed to reduce the reflectance by further modifying the surface morphology of the silicon wafer [15].

In 1998, the first “black silicon” was fabricated using the femtosecond laser pulses method by the Mazur lab of Harvard University, and the reflectance of this black silicon was 2.6 % in the wavelength range of 400–1100 nm[16]. In 2006, Zhou et al. used an electrochemical etching technology to make black silicon with a reflectance of lower than 5 % from 360 nm to 3300 nm[17]. In 2010, an average reflectance of 8.9 % in 300–850 nm was obtained from the silicon surface after being processed using the reactive ion etching (RIE) technique by Yoo et al [18]. However, the cost of femtosecond laser pulses and RIE methods are so high that they are not suitable for large-scale production, and the technological operation of electrochemical etching technologies is also not easy for industrialization. Therefore, the metal assisted chemical etching technology attracts much interest worldwide. In 2008, Peng et al. used thermal evaporated silver (Ag) nanoparticles as a catalyst to etch the silicon wafer in a hydrofluoric acid (HF) and hydrogen peroxide (H_2O_2) mixed solution, and the reflectance of the obtained silicon surface was lower than 5 % in the range of 200–1000 nm [19].

In 2008, Nishioka et al. coated single nano sized gold (Au) particle dispersion solution on the silicon wafer surface and then immersed the wafer in the HF and H_2O_2 mixed solution. Finaly average reflectance of lower than 5 % from 300 nm to 800 nm was achieved [20]. In 2009, Kensuke Nishioka et al. used Ag nanoparticles instead of Au and obtained a reflectance of lower than 5 % in the 200 – 1000 nm range [21]. In 2011, Liu et al. fabricated black silicon with a reflectance of 0.9 % from 250 nm to 1000 nm. Liu used reticular Ag film, which was made by the magnetron sputtering method, as a catalyst to assist the etching process in the mixed solution of HF and H_2O_2 [22]. There are also many other references about black silicon produced by metal-assisted chemical etching technologies [23].

In the present work we fabricated nanostructured c-Si wafers through single step MACE method with nickel as the catalyst metal. The proposed method is the first in the literature to prove a single step electroless Ni etching route of Si and Mono and multi-crystalline silicon solar cell was fabricated after optimization of electroless etching (EE) parameters to obtain black silicon wafer with the lowest reflectivity.

1.2 Materials and Methods

1.2.1 Process sequence of fabrication of silicon solar cell

For cell processing 156x156 mm^2, CZ growing mono-c Si and multi-crystalline, 180 μm thick boron doped Si wafer with a resistivity of 1-3 Ωcm were used to fabricate nanostructured black silicon solar cells. Process flow for solar cell fabrication is given in Fig 1.8.

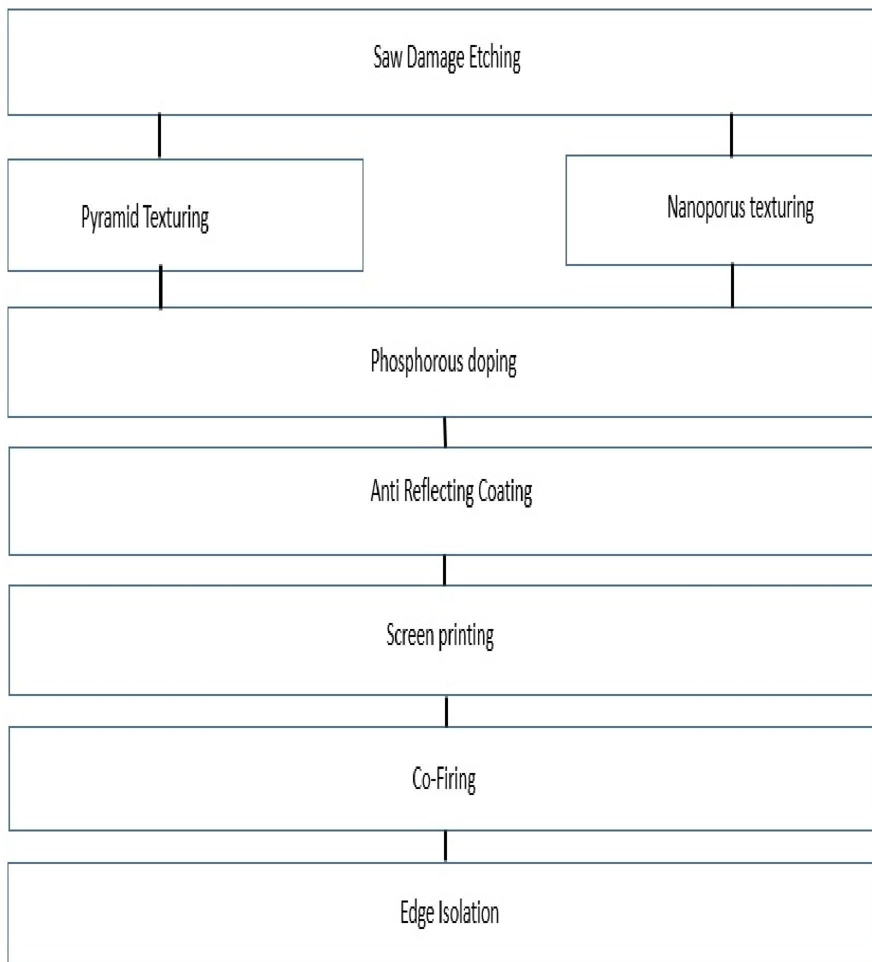


Fig 1.8 process sequence for pyramid and NP textured cell production.

Generally Saw Damage Etching is performed prior to texturing process in order to remove any residual wafer damaged caused by wire-sawing. The saw damage etching or removal (SDR) process was performed in a etching solution containing Potassium Hydroxide (KOH) and DI water with ratio of 1:5 respectively at 80°C for 4 minutes. This removed around 10 μm of saw damaged silicon from each side of the wafer resulting in a smooth surface, ready for texturing. SDR was followed by deionized water (DI) rinsing and HF:HCL dip for SiO_2 and metallic concentration removal. After (SDR) process. Wafer were subjected to RCA1 and RCA2 process for 30 minutes at 70°C based on below compositions (Table 1.1) to remove any residual metallic and organic contaminations from the surface of samples.

Table 1.1 Chemical composition of RCA1 and RCA2

RCA1	RCA2
H_2O_2:NH_4OH: H_2O (1:1:10)	HCL:H_2O_2:DI (1:1:20)

For texturing, wafers were divided into two sets. One set for reference alkaline texturing and the other was MAE nanowire texturing.

1.2.2 Alkaline Texturing

In case of Alkaline texturing (KOH texturing) of silicon, We used a 5 liters tank having temperature controller unit consisting of a heater and a thermocouple as well as a N_2 bubbler and a agitation system. The N_2 bubbler and the agitation unit were used to provide a homogeneous solution during the process. The etching solution containing of KOH, DI water and IPA. The solution was prepared inside the tank and the heater was set to the desired value. During the heating of the solution to reach to 75°C, the agitation system was set to dissolve KOH in the solution. During the etching process, the wafers were checked every 5 minutes to see the level of surface roughening. Since the RCA2 process produces a robust and thick oxide layer on the surface due to existence of H_2O_2. Therefore prior to alkaline process, the wafers were immersed into a 1:20 HF:DI solution for 30 seconds with the aim of removing the natural oxide on the surface of silicon. Right after natural oxide removal, the wafers were dipped into the tank and the etching process began. After the KOH etching, all wafers were rinsed with DI water and dried with N_2.

1.2.3 Theoretical view of (Alkaline Etching) Anisotropic etching

following chemical equation shows the mechanism of Anisotropic etching of silicon in aqueous KOH solution.[10].

$$Si + 4OH^{-}\ Si(OH)_4 + 4e \qquad \text{Eq. 1.3}$$

The (100) and (110) crystal planes are etched relatively higher than (111) planes (Table 1.2).

Table 1.2 Different etching rate of (100), (110), (111) crystal plane through anisotropic KOH texturing process.

Etchant	Etch Rate		
KOH 44%-85°C	100	110	111
	1.4μm/min	2.8μm/min	4.6x10-3 μm/min
	300	600	1

As a result, both (100) and (110) crystal planes are etched very faster than (111) planes. Therefore, small pyramids are remained after etching process as shown in Fig 1.9.

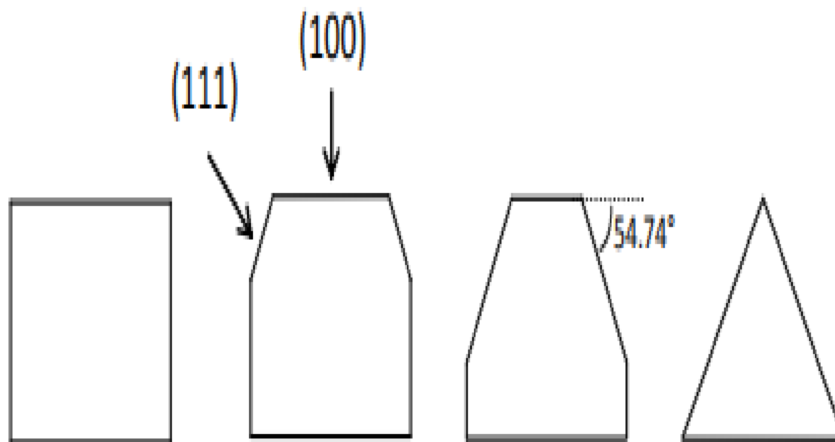


Fig 1.9 Anisotropic etching process of (100) oriented Silicon wafer. (100) and (110) plane are etched while (111) plane remains un-etched until pyramid structures start to occur with no (100) planes remaining.

1.2.4 Metal assisted Etching

Two set of Si wafers (Mono c-silicon and Multi c-silicon) were subjected to nickel assisted Etching. Prior to nickel assisted etching process all wafers were subjected to HF (38–40%) cleaning treatment for 2 minutes to allow the substrate surface to become hydrophobic which guaranties the removal of the thick SiO_2 layer formed after RCA2 process. The wet Electroless Etching (EE) solution was then prepared in a Teflon beaker containing constant concentrations of $NiSO_4$ (0.2 M) and H_2O mixed with different molar ratios of H_2O_2 to HF $\rho = \frac{[H2O2]}{[H2O2]+[HF]} \times 100$ varying from 4.2 % to 41.5% in order to examine the effect of the oxidant agent (H_2O_2) on the morphology of the textured Si after an hour etching treatment. At the end of the wet etching process, the textured wafers were dipped into HF/DI H_2O for 1 min to remove the thin oxide layer and some fractions of ionic contaminants. Morphologies and the composition of textured Si wafers were characterized through field emission scanning electron microscopy (FESEM, Hitachi, S-4800) attached to an energy-dispersive X-ray spectrometer (EDX). reflection measurements were made through a Si photodetector calibrated integrated sphere (Newport70679NS) in the wavelength range of 350 to 1100 nm.

1.2.5 Solid State Diffusion

Solid state diffusion was carried out in order to form of the p-n junction across the wafer enable photo-generated carriers to be separated through electric field in junction. Doping process was carried out in diffusion furnaces. The furnaces were tube type with three heating zones and were designed to process 4 inch wafers (Fig 1.10).

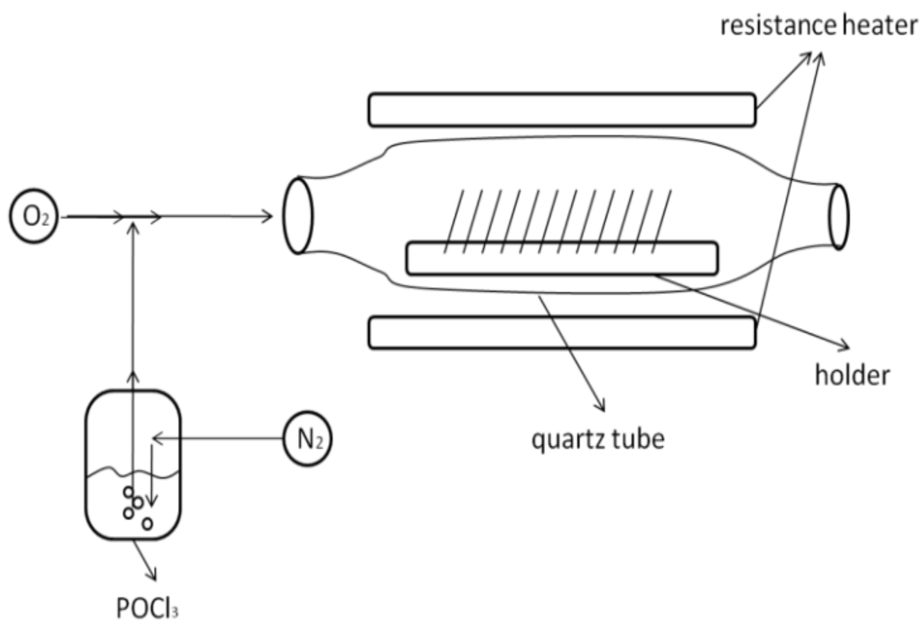


Fig 1.10 Tube furnace system for solid state diffusion

After the pre-diffusion cleaning (RCA1 and RCA2), samples were put in a quartz boat and then inserted in to the heated furnace for 5 minutes. This prevented the formation of thermal stress which may occur on the wafers due to quick change of temperature. For n-type doping of Si liquid $POCl_3$ is commonly used. It is carried with N_2 to the furnace by a bubbler and O_2 is used to help $POCl_3$ deposition according to the chemical equations;

$$4POCl_3+3O_2 \rightarrow 2P_2O_5+6Cl_2 \quad \text{Eg. 1.4}$$

$$P_2O_5+S \rightarrow SiO_2(P) \quad \text{Eg. 1.5}$$

Phosphorus is emerged into the oxide layer and then diffuses into the wafer by concentration gradient. The $SiO_2(P)$ layer formed on the Si surface is called the Phosphosilicate glass and is etched away from the surface after the end of the doping process. wafers were hold for 10 minutes inside the furnace in order to establish a temperature equilibrium with furnace in O_2+N_2 atmosphere. After the temperature stabilization, the predeposition step was started with the flow of $POCl_3^+$ O_2+N_2. After the drive-in step, all wafers were unloaded from the furnace and left for 15 minutes outside the furnace.

1.2.6 PSG removal

As it mentioned earlier the phosphorous glass on Si-wafers is removed in a HF solution or, as mentioned above, by applying an acid solution. The solar cell is transported on the surface of an etching bath in such a way that only the back side of the wafer is wetted. The wafers were then rinsed with water and dried with a drier.

1.2.7 Anti-Reflection Coating.

The number of absorbed photon is a key point that determines the output current of solar cell. Increasing the number of absorbed photon will increase the generated current and vice versa. Therefore, it is important to reduce the reflection of incident light from the surface of silicon. anti-reflective (AR) coating thin films are usually applied to the surfaces of the solar cells to enhance the number of photons absorbed by the solar cell. In some specific wavelength these coatings decrease the reflected intensity nearly to zero which have a considerable effect on the performance of solar cell.

In this study, we deposited a thin film (70 nm) Si_3N_4 layer with refractive index 2.00 on Si wafers by Plasma Enhanced Chemical Vapor Deposition (PECVD) system (Fig 1.11). In a PECVD system, Si_3N_4 deposition is carried out by decomposition of the gases SiH_4 and NH_3 at relatively low temperatures (200-300°C) in a plasma system with RF signal and a frequency of 380 kHz

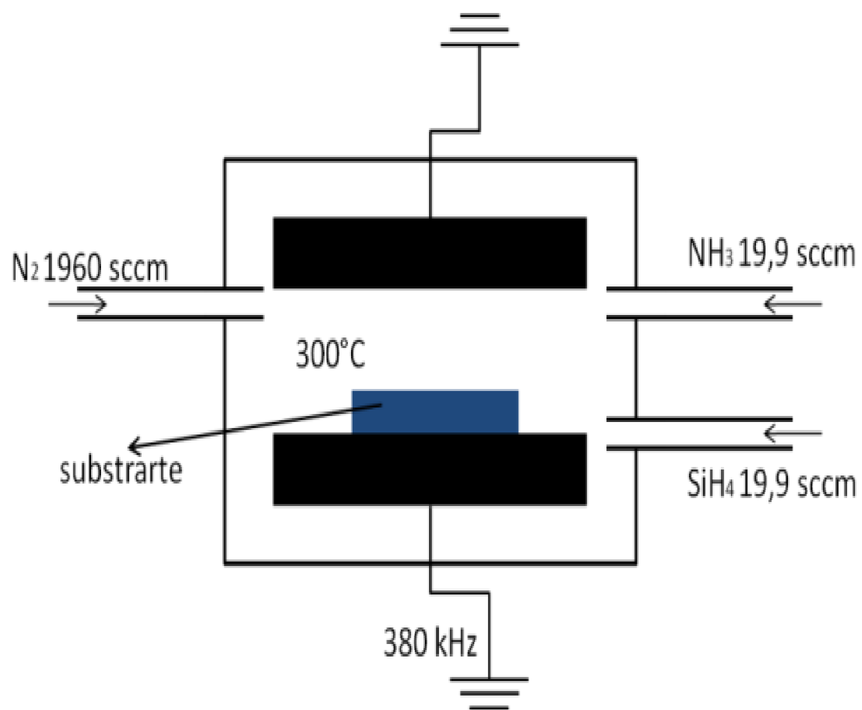
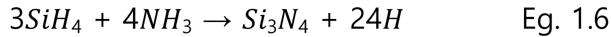


Fig 1.11 Schematic representation of PECVD

The chemical reactions which takes place during deposition of Si_3N_4 is as follow:



$$3SiH_4 + 4NH_3 \rightarrow Si_3N_4 + 24H \qquad \text{Eg. 1.6}$$

In order to optimize the thickness of our anti-reflective coating, several samples were coated with different thicknesses for reflectance measurements.

1.2.8 Metallization

Metallization is done at front and rear surfaces of the cells in order to carry the charge carrier separated by the p-n junction to an external load. Generally, the metallization on the front surface of the cell has a grid shape in order to let light into the solar cell while back side is fully covered. There are several ways of metallization used for solar cells such as, thermal evaporation, e-beam evaporation, screen printing. In this work, Metallization was conducted via screen printing of Ag finger to the front and full Al layer to the rear surface. After screen printing, Co-firing of the front and back metal was done in a conveyor belt furnace to form front fire through Ag contact and Al back surface field (Al: BSF).

In the case of the front contacts (Ag), the paste has to make contact with the emitter. To do this, the paste contains lead borosilicate glass ($PbO-B_2O_3$- SiO_2) and organic compounds. The lead borosilicate glass etches the SiNx antireflection coating and stimulates the adhesion of Ag contacts. This process takes place only at high temperatures, i.e., during the firing process at temperatures of around 90^oC. One disadvantage of this method is the formation of shadowing loss by the front silver contacts. In fact, the problem can be solved by using a photolithographic process; however, this method is more complicated.

1.2.9 Contact firing

After the screen printing of the front and back contacts, a firing process is needed in order to form an electrical contact between the pastes and the silicon material. In the case of the front side, silver paste has to penetrate through the silicon nitride layer and each to the emitter. Here the firing temperature is very critical for good and optimal solar cell performance. Low firing temperatures (below 800^oC) lead to very high series resistance, because at low temperature the pastes do not establish good electrical contacts with Si and at high temperature (higher than 900^oC), there is risk of shunting since pastes penetrate too deeply into the cell, (unwanted short circuits between the front and back contacts).

1.2.10 Edge Isolation

During solid state diffusion, both side of cell solar cell as well as edges are n doped. Although the Al back surface contact convert n type top type, still n-type regions are remained on the edges and some part of back side of the cell. It can lead to the recombination of electron and holes which can drop the performance of solar cell. Edge isolation can remove the shortcutting problem of the cell by electrically separating the front and back side of cell from each other's (Fig 1.12). This is accomplished by a 20W watt ND-YAG pulse lazer at Nurol technology factory. The wafer were hold with a distance of 25 mm from lazer cutter and the adges of the wafers were scribed at a speed of 300 mm/S with a frequency of 10kHz (1064 nm) laser.

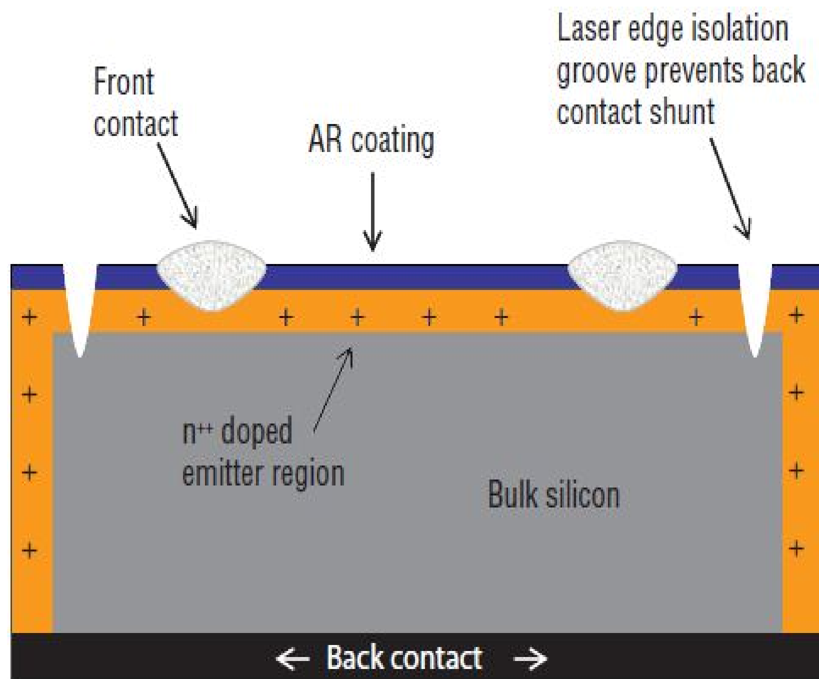


Fig 1.12 Cell with edge isolation completed by laser grooving from the front surface. Separated electron-hole pairs cannot recombine through back metal and n region contact.

1.2.11 I-V characteristic

I-V data, efficiency, fill factor, max power point, short circuit current and open circuit voltage of the cells were analyzed and measured using an AM1.5G calibrated class 3A flash solar simulator software (Fig 1.13). Sample and the source meter were connected through two probes from the front fingers and a cupper plate from the back side of the cell.

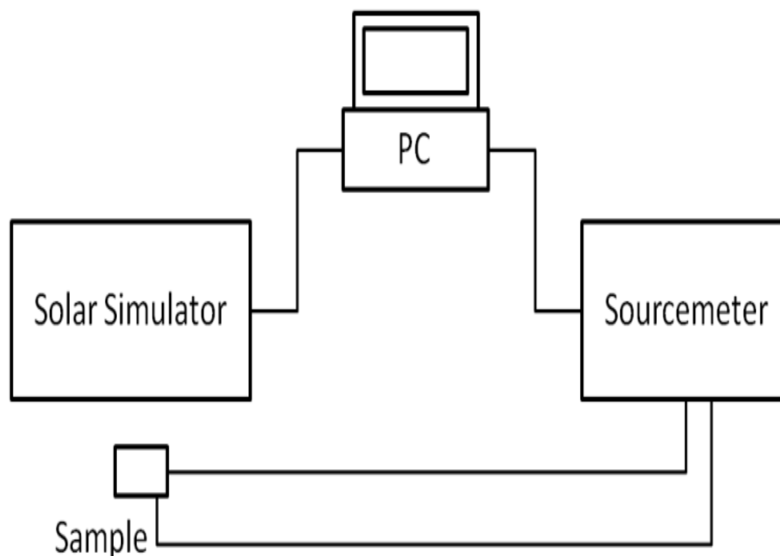


Fig 1.13: Experimental setup for I-V characterization

1.2.12 Reflectance

The setup consisted of an Oriel integrating sphere, a Stanford lock-in amplifier, an Oriel chopper and controller, a calibrated Oriel silicon detector, an Oriel UV light source, focusing lens and a PC (Fig 1.14)

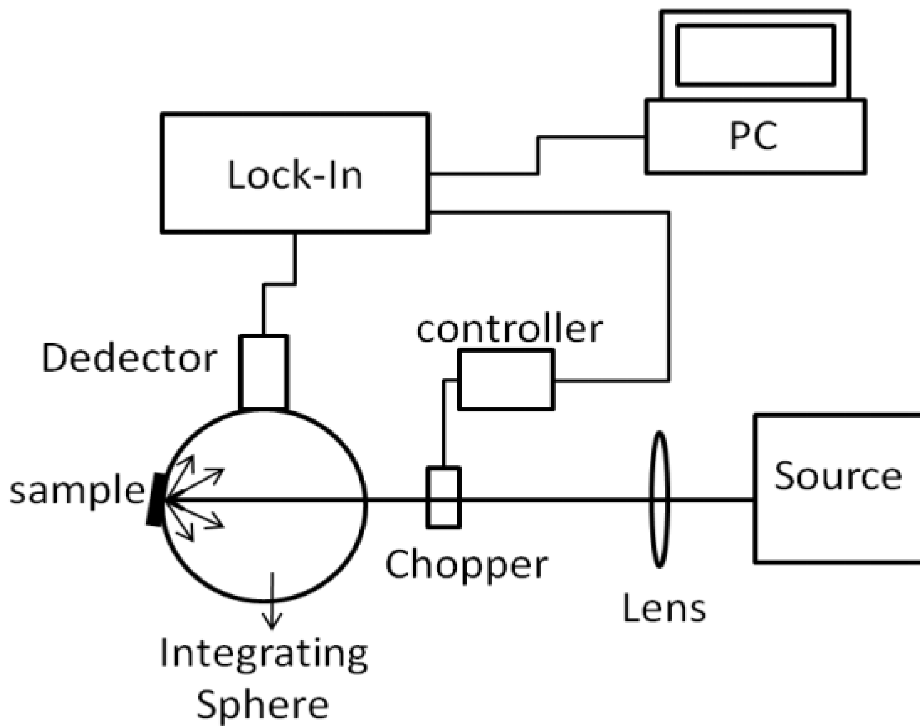


Fig 1.14 Reflectance measurement setup

Since the textured samples did not only have specular reflectance but also diffuse reflectance, We used integrating sphere for our reflection measurement (Fig 1.15). the sample is located in the integrating sphere with a 4-degree rotation with respect to the incoming beam and the reflected beam makes a uniform illumination inside the sphere. For measurements, first we used a calibration disk as a reference with 100% reflectance before real sample measurement. The total net reflectance of the samples was gained through the ratio of the reflectance from the sample to the calibration disk.

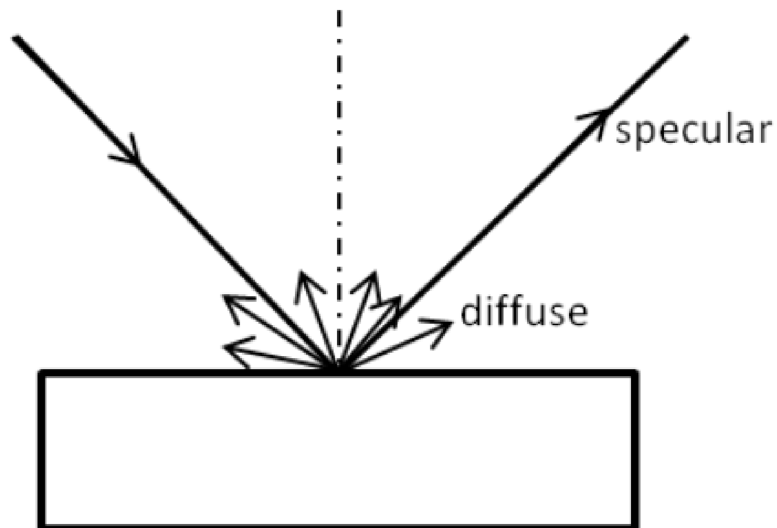


Fig 1.15 The incident beam undergoes both specular and diffuse reflectance.

1.3 Results and discussion

1.3.1 Nickel Assisted Etching of Mono-c Silicon

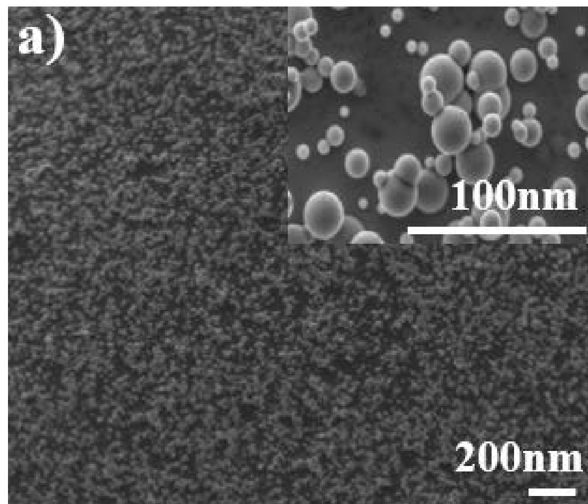
1.3.1.1 Nickel deposition on silicon substrate

Based on the displacement deposition mechanism, nickel atoms are deposited on the Si surface in the absence of a reducing agent. The nickel ions in the EE solution simply displace the Si atoms on the surface and make it possible for Si atoms to play the role of a reducing agent [24]. After 40 minutes of immersion of the Si wafer in the EE solution containing 0.2 M of $NiSO_4$ at 40°C, the Si surface is loaded with nearly spherical, isolated nickel particles (characterized by EDX; Fig 1.16 (b)), with average diameters of less than 100 nm. In some regions, nickel nanoparticles agglomerate and form nickel nanoclusters. It is assumed that higher bath temperatures or higher $NiSO_4$ concentrations enhance the surface coverage, essentially by increasing the surface density of nickel on Si substrate. As it can be clearly seen (Fig 1.16 (a)), some parts of Si substrate are left blank, providing space for reactive species for further redox reactions between deposited nickel and Si atoms. Inert of figure 1a illustrates the evolution of hydrogen (H_2) bubbles which were generated as nickel atoms were deposited on the surface of Si. This phenomenon has been extensively explained in the following paragraphs.

1.3.1.2 Mechanism of nickel-assisted etching of silicon

Fig 1.17, which includes six steps from left to right, shows a schematic mechanism of the formation of pores Si through reduced nickel atoms in an aqueous solution containing H_2O_2, HF and $NiSO_4$. In the initial step of the mechanism, two simultaneous cathodic reactions (Eq. 1.7 and 1.8) occur on the interface of nickel atoms [25].

Firstly, H_2 gas is evoluted due to the reduction of protons based on the equation (1.7) and then, hydrogen peroxide is reduced based on the equation (1.8)[26]. As illustrated before evolution of H_2 bubbles confirms the initiation of the reduction of H_2O_2 on the surface of nickel atoms causing nickel atoms to act as a microscopic cathode that precipitates on the surface of Si atoms (Equation. (1.9)).



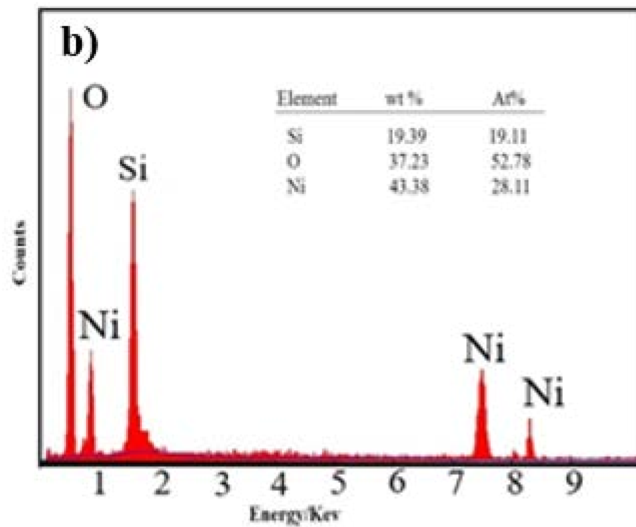


Fig 1.16 (a). SEM image of nickel nanoparticles deposited on a p-type (1 0 0) Si surface by immersion in a solution of $NiSO_4$ and HF at 25°C for 15 min without any incorporated reducing agent in ECE solution. The inset of Fig 1.16 (a) shows the spherical nickel formed during deposition of nickel on the silicon substrate. Fig 1.15 (b). EDX analysis of silicon substrate after deposition of nickel.

After the deposition of nickel on Si substrate (2nd step of Fig 1.17), the generated positive charges from the reduction of H_2O_2 are diffused into the nickel that acts as a catalyst. As the standard reduction potential of nickel is higher than Si, the generated positive charges are accelerated spontaneously and injected into the Si beneath nickel, causing oxidation of Si (Equation. (1.9)). Subsequently, the resulting SiO_2 is etched away and is dissolved by HF (Equation (1.10)) [27].

$$Si + 2H_2O \rightarrow SiO_2 + 4H^+ + 4e^- \qquad \text{Eq. 1.9}$$

$$SiO_2 + 6HF \rightarrow H_2SiF_6 + 2H_2O \qquad \text{Eq. 1.10}$$

fact that the rate of consumption of positive charges at the interfaces of nickel and Si is not as fast as the rate of injection of holes from 1st and 2nd reactions to nickel. This phenomenon is attributed to this fact that the electronegativity of nickel is very close to the silicon's electronegativity. Therefore, the injected positive charges from nickel into Si are accumulated at the interface of Ni/Si. This occurrence is attributed to the rate of injection of the charges on the top of the nickel particles. Consequently, a positive charge concentration gradient is formed that causes the diffusion of the charges from the interface of nickel (Ni)/Si to the side wall of the generated pores that results in the enlargement of the pores'width (the 3rd and the 4th steps of Fig 1.17). The 5th step in Fig 1.17 demonstrates the phenomenon in which the agglomerated nickel particles are separated into several small particles such that every particle probes the Si solely in different directions. Moreover, due to the unequal rate of the consumption and the injection of the positive

charges at the top and the bottom surfaces of nickel, the nicekl itself shrinks during etching, and eventually, it is completely dissolved in aueous solution at the end of the etching process. Absence of residual nickel is demonstrated by EDX analyse in following paragraphs. (6th step of Fig 1.17).

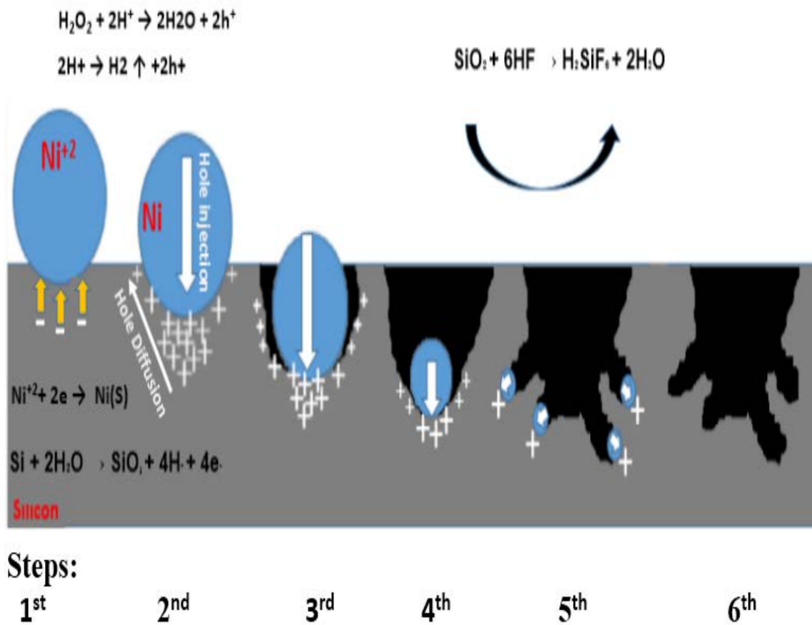


Fig 1.17 Schematic of the mechanism of generating porous silicon layer using reduced nickel atoms.

1.3.1.3 Morphology of Etched Silicon

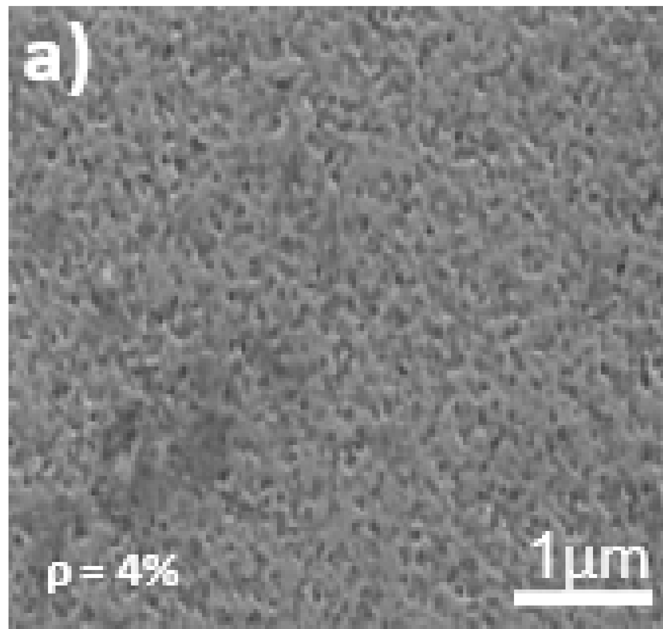
The concentration of oxidant agent affects not only the etching rate of Si but also the morphology of the textured Si in the electrochemical etching mechanism. The influence of concentration of oxidant agents on the structure of textured Si is associated with the volume of local current injected from positive charges into Si [28]. H_2O_2 is the most common oxidizer in wet chemical etching of Si and it is assumed that the relative concentration of H_2O_2 in the EE solution plays a similar role to critical current density (Jps) in electrochemistry [29]. Fig 1.18 shows the SEM micrographs of textured single crystalline Si after 1hr etching treatment with different molar concentrations of H_2O_2 to HF (ρ). As it can be seen in Fig 1.18 (a) , some shallow disrupted low dense porous structures were formed on the surface of Si as a result of the low concentration of H_2O_2 (ρ= 4.2 %). Formation of these sketchy low dense pores on the Si surface can be attributed to the low volume of the injected positive charges onto the Si surface. As ρ is increased to 8.1 %, more volume of positive charges are injected from nickel atoms to the Si surface leading to higher Si oxidation rate. Consequently, an array of deeper void spaces (pores) ranging from 30 to 40 nm in diameters (Fig 1.18 (b)) were formed in the direction normal to the Si surface ([1 0 0] direction). The nickel particles sank into the pores which were bored perpendicular to the Si surface. Since [1 0 0] direction showed the higher contact area than other directions, dissolvent of Si by HF from {1 0 0} plane form is more suitable when compared with other lattice planes [30]. Fig 1.18 (j)

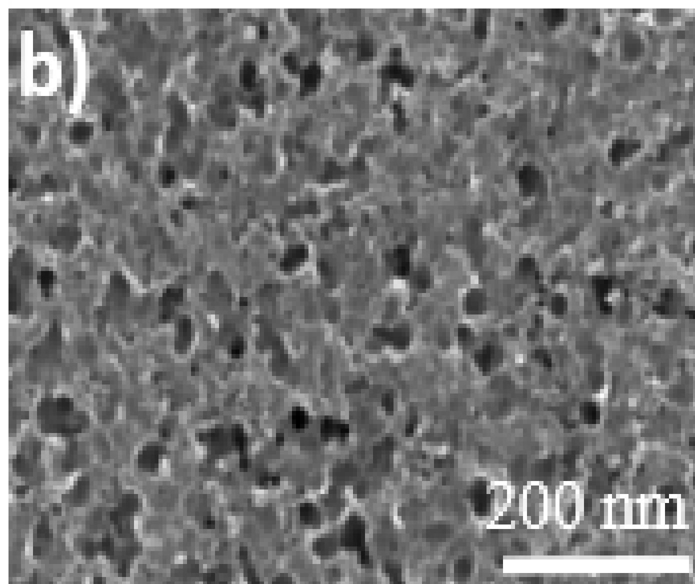
represents an EDX analysis of the Si surfaces after being subjected to nickel assisted etching treatment without any subsequent HCL cleaning process. It is evident that, unlike noble metals, residual nickel particles are absent from the bottom of trench and this demonstrates the dissolution of nickel particles at the end of the etching process as manifested from the last step in Fig (17)

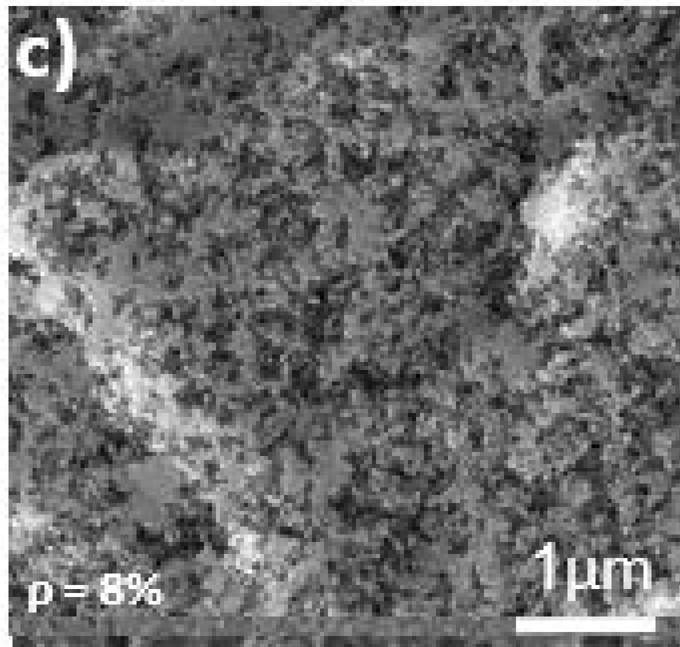
As observed from Fig 1.18(c), crater structures with a rounded morphology in the range of 200 – 700 nm in diameter were formed on the Si surface. Smaller and straight cylindrical macropores in the diameter range of 30–50 nm were bored inside these crates perpendicular to the Si surface. The enlarged view of the marked area in Fig 1.18 (c) is illustrated in Fig 1.18 (d). As it is seen, a mixture of pinholes with diameters of less than 20 nm along with the wider macropores indicate the wide-range size of deposited nickel particles on the Si surface. It is tough to explain the etching mechanisms that result in the formation of these craters, but it can be assumed that a mixed regime of polished and porous Si formation lead to the growth of such craters. As shown in Fig 1.18 (d), not only vertical pores, but also horizontal pores and trenches were exposed to the Si surface as trenches which were crocked and oriented in the directions normal to (100) (Shown in round marked area). An underlying suggestion for this phenomenon can be the random movement of nickel particles on the Si surface. Rectangle marked area in Fig 1.18 (d) depicts one of the trenches (Rectangle Marked in Fig 1.18 (d) bored with a length and

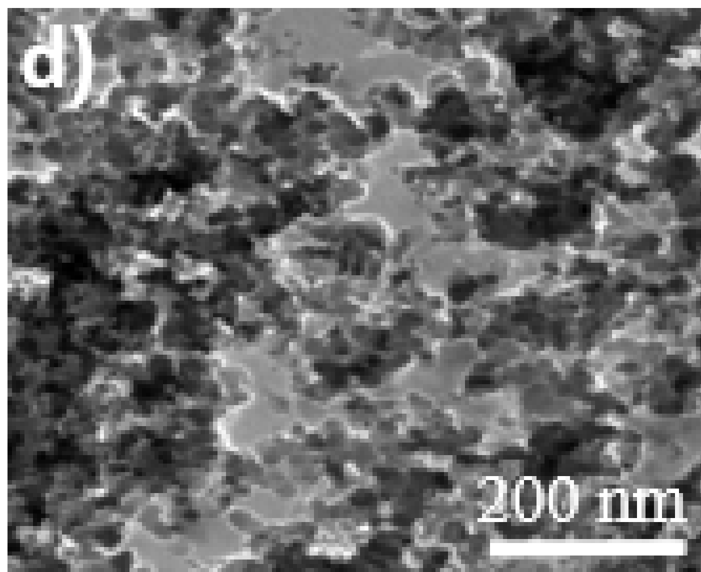
width of 375 nm and 65 nm, respectively. Note that the movement of the trench began from left to right. Initially, the width of the trench is larger, and as nickel particle propagates, it decreases and then saturates upon its movement towards the right side. It is obvious that no residual nickel was left behind at the end of the trench. Further increase in the concentration of H_2O_2 (ρ=26.1%) led to a special morphology of the etched Si as superfine homogeneous velvet structure of the textured Si was achieved on the surface of Si (Fig 1.18 (e). Fig 1.18 (f) illustrates the enlarged view of Fig 1.18 (e) and represents a nano-spongy morphology of the etched Si. Formation of this nanospongy structure of Si is attributed to the injection of adequate positive charges, which are homogeneously distributed over the whole Si surface through the Ni/Si interface. These injected positive charges were attracted near the nickel particles due to an induction by the image force. However, many positive charges escaped from the image force upon their injection. This can be the reason for the generation of the nanoporous Si layer on the Si surface when samples were treated in EE solutions containing optimized concentrations of H_2O_2 (ρ=26.1). Fig 1.18 (g) illustrates the cross-sectional view of a 2 μm thick nano-spongy structure of porous Si layer formed on the surface of Si after 1hour treatment in EE solution with ρ=26.1. The low rate of Si etching by nickel as compared to other noble metals can be attributed to the weak catalytic activity of nickel for reducing H_2O_2. Fig 1.18 (h) shows a random cross-section of Fig 1.18 (e) just under these porous layers. The cylindrical mesopores were formed perpendicular to the surface of Si and some of them were bent in right

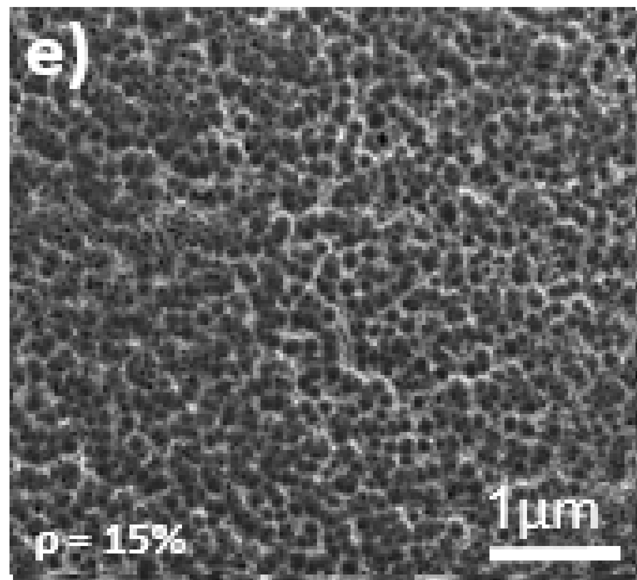
angles in the directions equivalent to [1 0 0]. The nickel particles also, like silver [31], changed their etching courses in directions which have the highest possibility of contact area, compared to the other directions. The length of these vertical pores is varied from 200 nm to 1μm, indicating various boring timing which can be associated with the different surviving time of nickel particles before decomposition in Wet Electroless Etching (EE) solution. Further increase in molar ratio (ρ = 41.5) led to the formation of a special cobblestone-like structure shown in fig 1.18 (i). Formation of this morphology of Si is unclear to us and it needs further research to find out the reason behind this special structure.

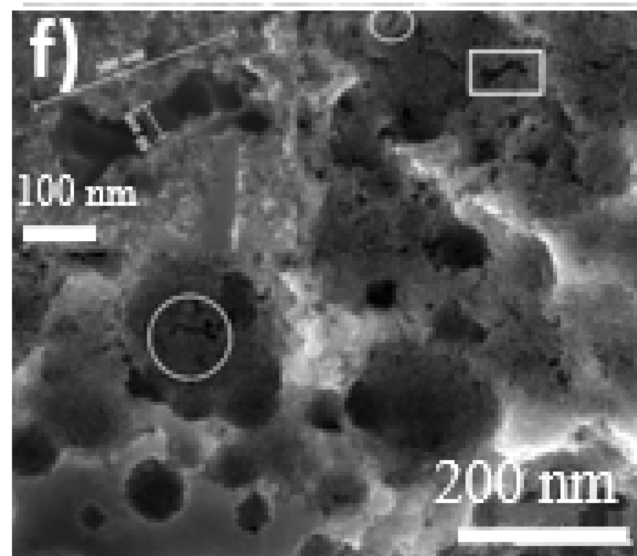

a)
ρ = 4%
1μm

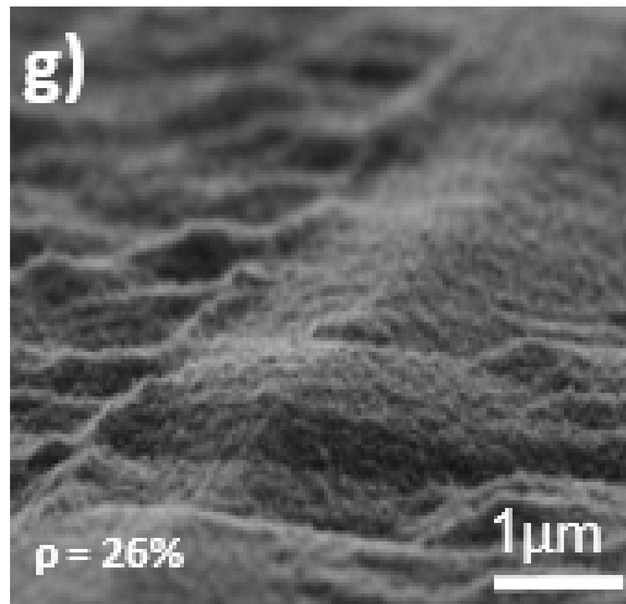

b)
200 nm

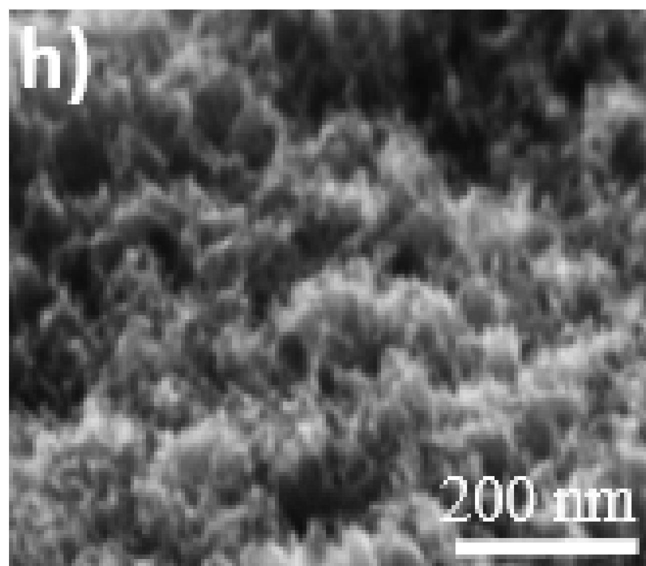

c)
ρ = 8%
1μm

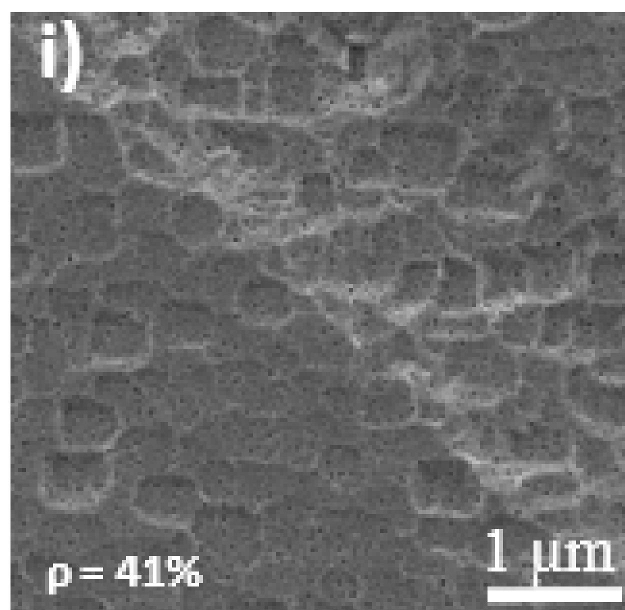

d)
200 nm

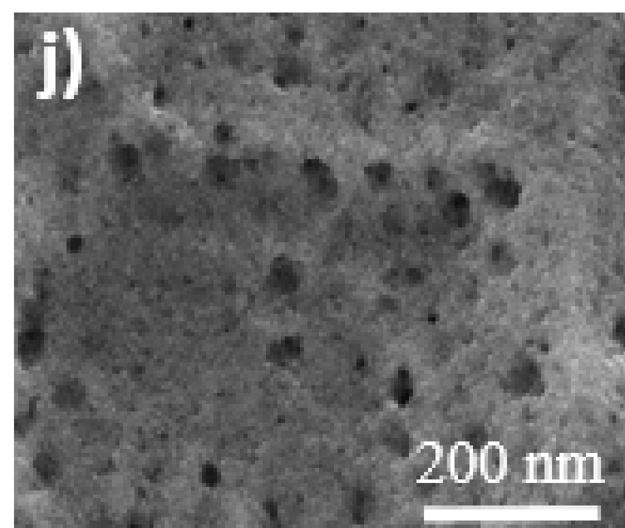

e)
1μm
ρ = 15%


f)
100 nm
200 nm


g)
1μm
ρ = 26%


h)
200 nm


i)
1 μm
ρ = 41%


j)
200 nm

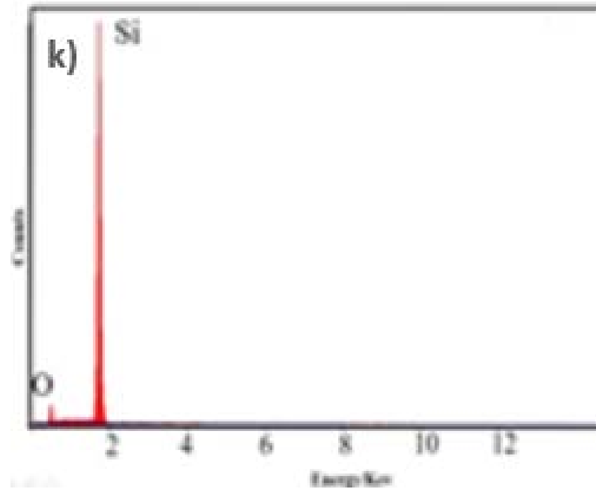


Fig. 1.18. SEM images of textured Si after treatment in an aqueous solution containing $NiSO_4$, HF and H_2O_2. Fig (a),(b) and (c),(d) and (e),(f) and (g),(h) and (i),(j) show plan-view SEM images of Si etched in ($\rho = 4.2$%), ($\rho = 8.1$ %), ($\rho = 15.1$%), ($\rho = 26.1$%) and ($\rho = 41.5$%), respectively. Fig (b) is an enlarged image of the area marked in Fig (a), Figure (d) is an enlargement of Fig (c). Figure (f) is an enlargement of Fig (e). Figure (h) is an enlargement of Fig (g). Figure (j) is an enlargement of Fig (i). Fig (k) is an EDS of top view of silicon after etching.

1.3.1.4 Reflection measurement

As discussed earlier, altering the concentration of H_2O_2 has significant influence on the morphology and size of the porous Si, which is expected to have influence on the reflections of incident light on a specific range of wavelength. Fig 1.19 displays the optical reflectance spectra in wavelength range of 350 to 1100 nm after 1 hour etching treatment of Si in an aqueous solution containing different concentrations of H_2O_2. It has been observed that reflectance of textured Si surface in all molar ratios of H_2O_2 is lower than that of planar Si. Reflectivity of sample etched in a solution with ρ= 4.2 % showed a slight decrease from 43.1% to 42.1% as compared to a planar Si. The small drop in reflectance is due to an existence of the separate low-dense etched sites on the Si surface that had a negligible effect on the absorption of incident light. However, increasing of ρ to 8.1% dramatically decreased the reflectance to 17.3% which can be verified by the morphology of the etched Si, as shown in Fig 1.18. Further increasing the ρ to 15.1 % exhibited a reduction in reflectance to 4.5%, which is due to the existence of mixture crates along with nano-sized pores on the Si surface.

The sample etched in ρ = 26.1% represented a reflectivity as low as 2.1% in the wavelength range of 350 to 1100 nm which was found to be the best antireflective performance in comparison with 5 other samples in this study. The considerable light-trapping characteristics of this sample is associated with the existence of the nanospongy textured Si layer which were formed on the Si surface with an optimum molar concentration of H_2O_2 in EE solution. Correspondingly, the higher optical absorption of this sample is supported by its black and dull appearance as represented by the inset in Fig 1.19 Further, increase in

the molar concentration of H_2O_2 from 26.1 % to 15.1 % dramatically enhanced the reflectance of the Si to 34.7 %, which can be attributed to the formation of a cobblestone-like Si structure, as shown in Fig 1.18 (i).

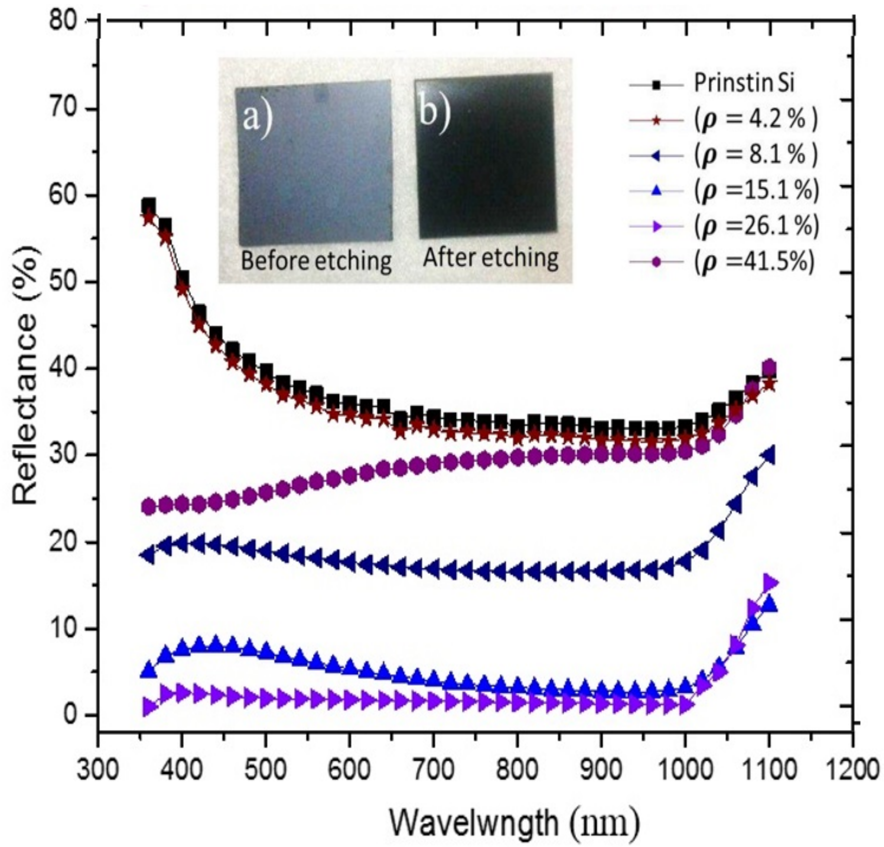


Fig 1.19. Reflectance as a function of wavelength of polished monocrystalline Si wafers etched in various concentrations of H_2O_2.

1.3.2 Ni Assisted Etching of Multi-C Silicon

Fig 1.20 represents two plan-view images comparing the color of Si samples before and after nickel etching treatment. It is seen that after the etching process is completed, the color of silicon is turned completely to black with a dull appearance which is a clear evidence of the absence of reflected light from the surface.

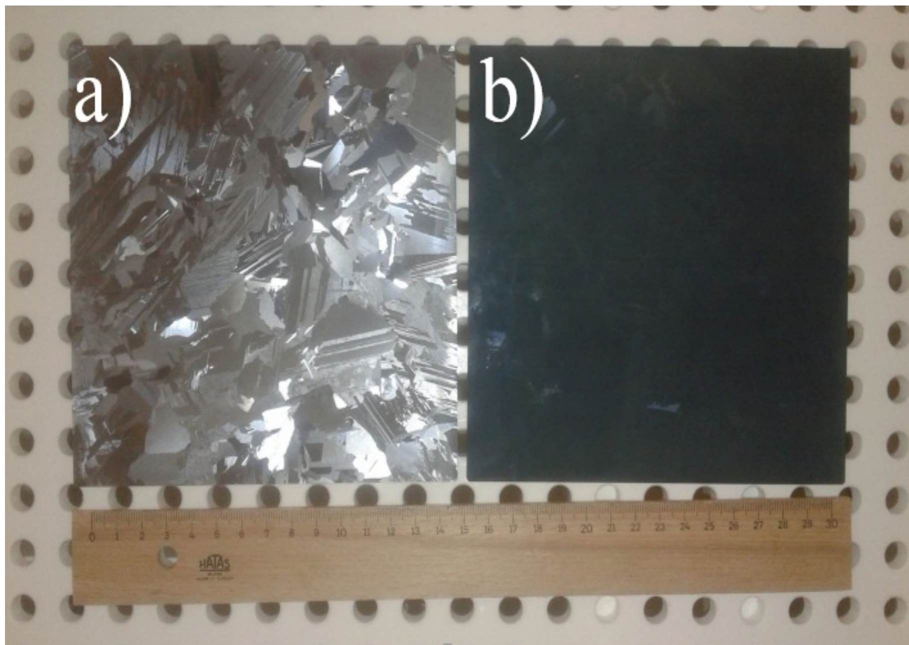
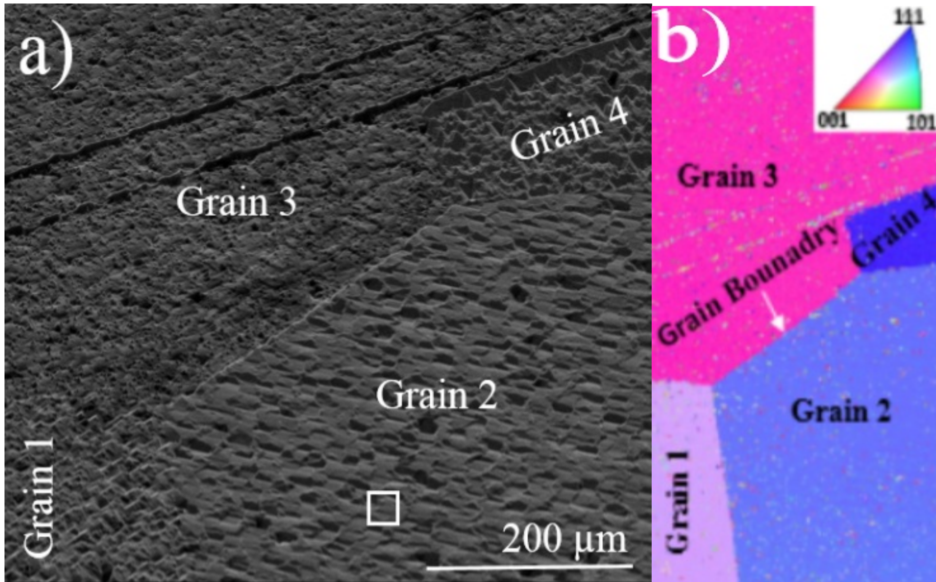
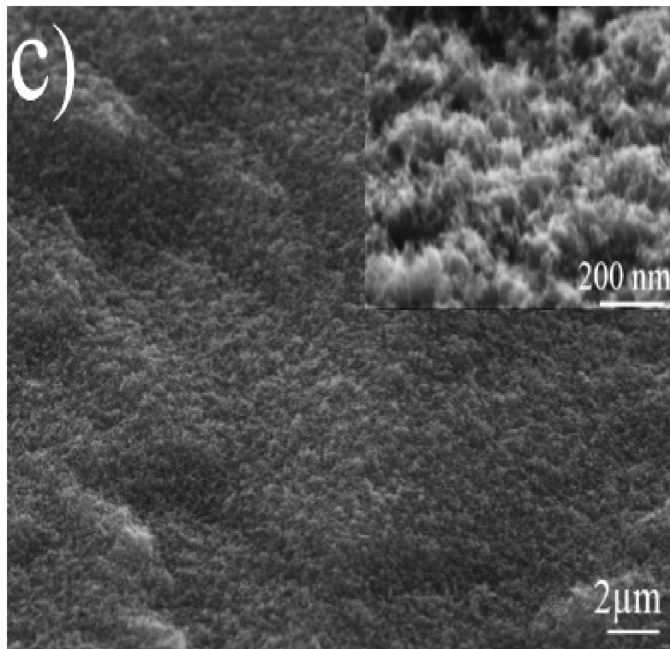


Fig 1.20 Plan view optical image of the surface of full wafer multi c-si (a) before and (b) after nickel Electroless Etching in an aqueous solution containing HF, H_2O_2, and $NiSO_4$.

Fig 1.21 (a) shows the top view image of textured Multi c-Si fabricated after 1 hour of electroless etching treatment in an aqueous $NiSO_4$ solution. It is evident that this part of the textured silicon consists of 4 separate grains with clear grain boundaries. We see that each grain shows a different shape of texturing indicating a dependence of the crystallographic orientations. Fig 1.21 (b) shows EBSD analyses of Fig 1.21 (a). Each color of the EBSD map represents a specific crystallographic orientation of the grains shown in Fig 1.21 (a). The diversity in the alignment of the textured silicon is associated with the different chemical reactivity of EE solution with specific plane lattice belonging to each separate grain.

Fig 1.21 (c) shows a magnification of marked area in Fig 1.21 (a). We see a very fine homogeneous and uniform structure of the textured silicon achieved with the nickel-assisted etching technique. The inset of Fig. 1.21 (c) shows magnified images of random areas of Fig 1.21 (c) which reveals a fluffy nanostructure of textured silicon. It is also seen that these nano-textured shapes are formed over each other like clouds, and they create an efficient anti-reflection coating on the surface. Fig 1.21 (d) shows a cross-section of the characteristics of the 1μm-thick nano-textured silicon layer formed on the surface of silicon after the 1-hour treatment. It is seen that some cylindrical pores with length ranging from 100nm – 300 nm bored into the silicon substrate under the 300 nm-thick nano-porous layer.


a)
Grain 4
Grain 3
Grain 2
Grain 1
200 µm
b)
111
001
101
Grain 3
Grain Bounadry
Grain 4
Grain 2
Grain 1


c)
200 nm
2µm

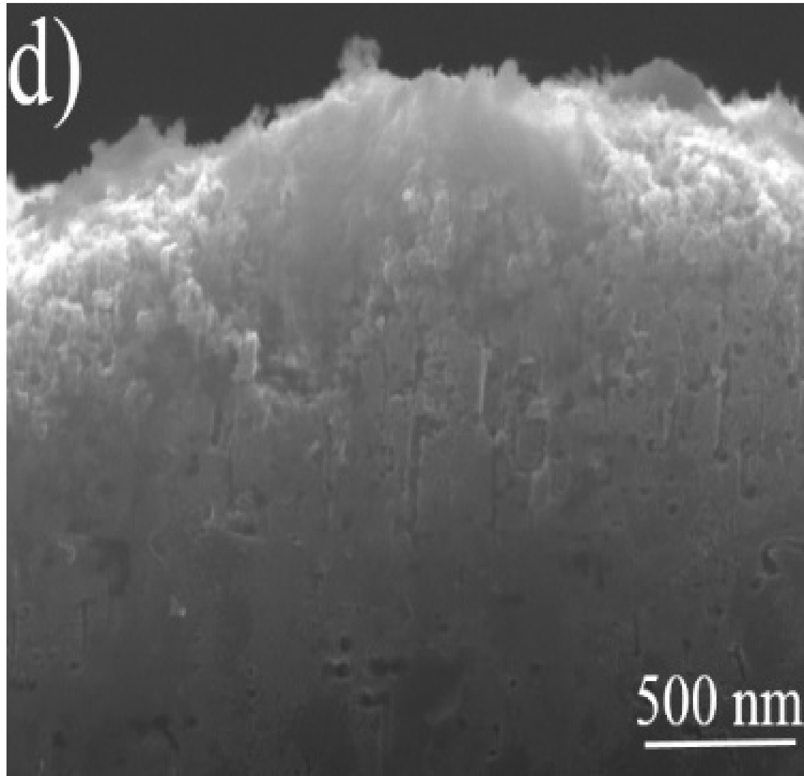


Fig 1.21 Plan view SEM image of textured multi c-Si through nickel-assisted etching. (b) EBSD map of grains orientation distribution (a) showing the different crystallographic orientation of grains, (c) Plan-view enlarged SEM image of marked area in Fig. (a), cross-section SEM image of the nano-textured surface of silicon obtained after 5 minutes with nickel assisted etching technique area.

Fig 1.22 shows the reflection spectrum of an iso-textured and MAE textured wafer after SiNx anti-reflective coating. It is obvious that the MAE textured and iso-textured samples have close reflection values in the wavelength range of 550 nm – 1100 nm. On the other hand, as it is seen in Table 1.3, AM1.5G weighted reflection values are lower for the MAE textured wafer due to its better performance in the blue – UV regions.

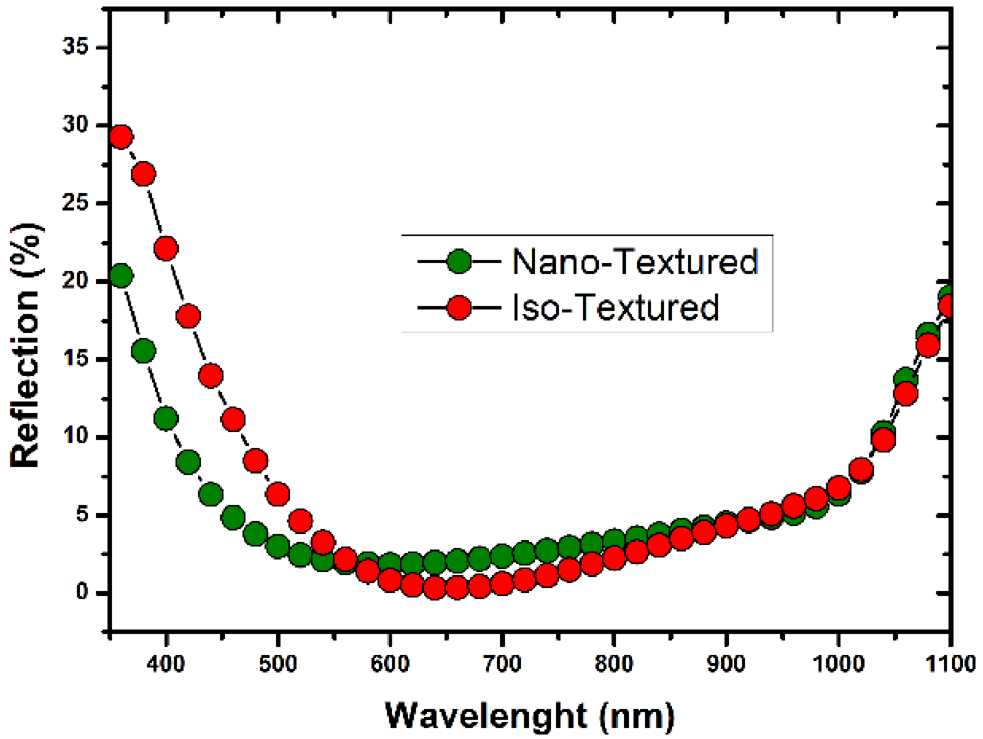


Fig. 1.22. Reflection results of iso and nano-textured surfaces as a function of wavelength.

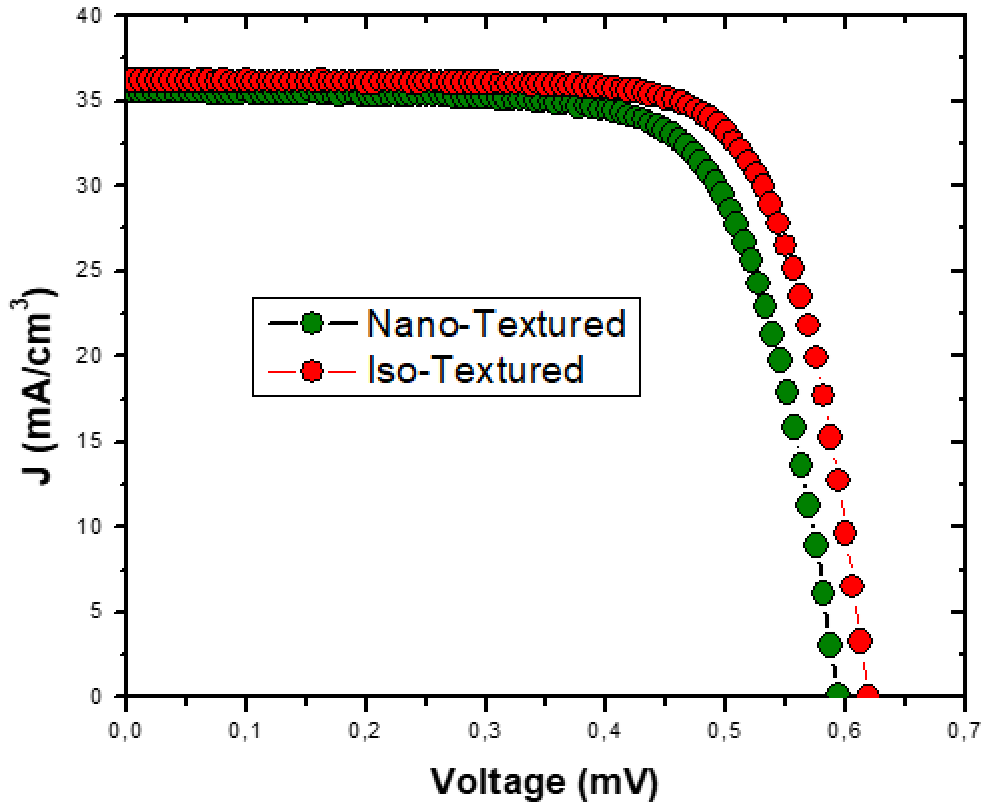


Fig 1.23 Current density of iso and nano-textured wafer solar cells as a function of voltage.

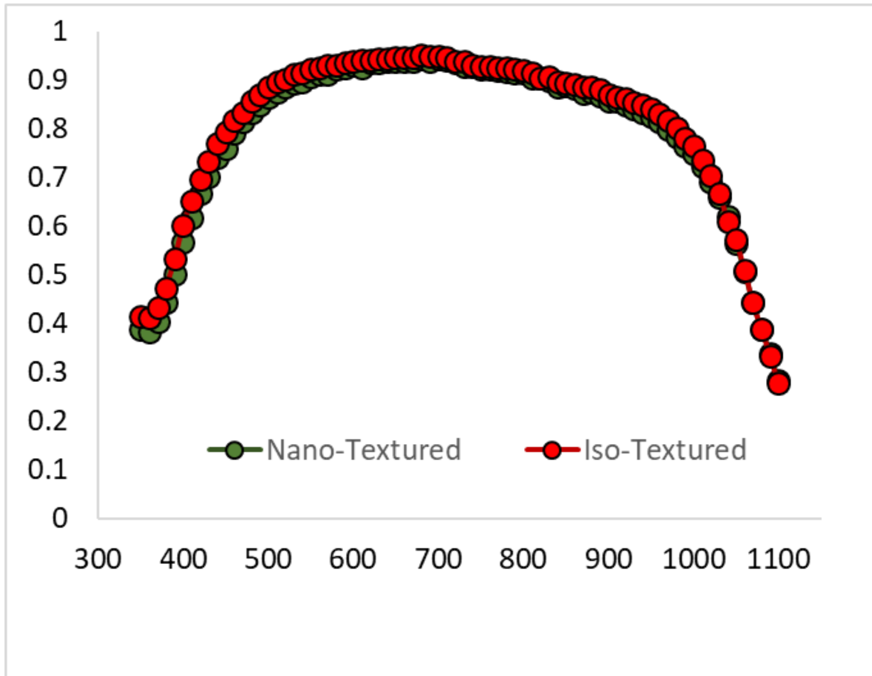


Fig 1.24 EQE curve of iso and nano-textured surfaces as a function of wavelength.

Fig 1.23 shows the I-V results of solar cells made on MAE textured Si wafer and compares it to the identically processed reference sample. We see that the solar cell fabricated on the sample textured by MAE with nickel as the catalyst performs quite well in terms of Voc and Isc values. As a first trial without any further optimization, this result represents a successful demonstration of the use of nickel in the MAE process. Due to the lower FF values, the efficiency of the cell is slightly lower than what we expected from the measured Voc and Isc values. It is clear that higher efficiency values are feasible by improving the FF through optimization of parameters determining the series and shunt resistance values. One particular problem is associated with the metallization of nano-textured surfaces with the standard Ag paste. The grain size of the Ag paste is usually greater than the features size of the textured surface which makes sticking of the metal fingers on the surface difficult[32]. Voc value of the samples textured with MAE is most likely related to the higher recombination on the surface of the cell due to the increased surface area. This is a typical problem of solar cells made on black Si and can be solved by employing a suitable passivation process such as highly conformal Atomic Layer Deposition (ALD) [33].

Table 1.3 Performance value of the iso and nano-textured silicon

Type	V_{oc}	J_{sc}	FF%	Eff	Reflection (%)
Iso-Textured	0.621	36.20	74.1	16.55	5.37
Nano-Textured	0.619	35.56	70.4	15.50	4.38

Table 1.3 displays the cell parameters extracted from the optical and electrical measurements. Although the nano-textured cells have lower reflection, the overall cell results show that iso-textured cells have a higher performance. First of all, the lower Voc values of a nano-textured cell are attributed to higher surface recombination due to insufficient passivation via PECVD SiNx. It is a well-known fact that black Si surface, which is a very complex structure, requires high-level passivation techniques such as highly conformal Atomic Layer Deposition (ALD). In addition, lower reflection and Jsc are indicators of low collection efficiency due to high Auger recombination on the tips of nano-texture since high doping level and effective junction depth is needed to collect generated carriers [31]. Lower FF is also a common problem faced in nano-textured cells since the grain size of front Ag paste is a lot larger than the black Si nano-texture.

1.4 Summary and Conclusion

The first world ever one-step nickel assisted chemical etching was developed and used as an economical technique for fabrication of antireflective nanotextured silicon wafer. The mechanism of one-step nickel assisted etching was illustrated schematically and discussed comprehensively. It was found that nickel cations were reduced from $NiSO_4$ on the silicon surface at 40^oC and caused in formation of nanosize vertical and horizontal pores on the surface of silicon in different crystallographic direction as a result of 1 hour etching treatment. Effect of the molar ratio of H_2O_2 to HF on the surface morphology and corresponding optical reflection was investigated. Results indicated that as concentration of H_2O_2 to HF increased from 4.2% to 8.1% optical reflectivity of textured silicon was decreased from 42.1% to 17.3%. Optimized concentration of H_2O to HF in wet etching solution resulted to the formation of nonporous structure of textured silicon which represented the lowest level of light reflection which was about 2.1%. However higher concentration of concentration led to formation of a side walk structure of etched silicon which enhanced the reflectivity of incident light to 34.7%. Moreover, nickel assisted etching of multi c-si wafer as an alternative texturing method to the traditional acid texturing process and the existing metal assisted etching method with more expensive noble metals was examined. We demonstrated the ability of texturing with nickel to enable the formation of black silicon with desirable reflection performance. This novel etching approach was applied to the fabrication of solar cell with industrial dimensions. Although some improvements through fabrication process and materials optimization was required, the performance of the cell made on isotropic nickel assisted etching shewed a promising potential for future applications.

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CHAPTER 2.

light induced electro less nickel metallization for silicon diode

2.1 Introduction.

Metallization of silicon solar cells is essential for obtaining higher efficiency and this can be achieved by establishing an improved metallization method. So far, screen printing is known as the most common metallization technology in the silicon based photovoltaic industry, as it is simple and fast. However, screen printing technique limits the efficiency of solar cell due to having a lower aspect ratio and higher contact resistance. The high price of silver pastes and shrinking silicon wafer thicknesses inspires the silicon solar cell manufacturers to find out a fresh metallization technique that consumes a lower quantity of silver without the pressing process of screen printing. The photovoltaic industry also prefers to fabricate high performance solar cell with a lower usage of silver pastes, as has been set out by the international technology roadmap for photovoltaics (ITRPV)[1]. Therefore, a considerable research has already been done on different metallization techniques to find a new way for metallization technology. The growth of metallization techniques with minor production costs and higher efficiencies is critical for the progression of solar cell manufacturing technology. These need has be understood and a workshop stablished for the metallization of crystalline silicon solar cells for the first time in Utrecht, The German, in 2010[2]. The next workshops were also conducted on the scope of metallization[3]. All of these workshops have dedicated to realize the need of improvement of the current state and recent advances of metallization technology. Among the all encouraging metallization techniques, the formation of metal contacts using Ni/Cu plating techniques has appeared to be one of the most promising candidates for future metallization of solar cells. Ni/Cu plating techniques has a high potential to boost the capability of metallization processes with accurate and low contact resistance. The technique

decreases the final production cost, and is suitable for use in mass production.

The standard processing steps of Ni/Cu contact formation involves two sequences: in the first step, (i) nickel metal film is plated on to the solar cell surface, followed by (ii) the final step of plating a copper metal film on top of the nickel. This Copper film over the nickel film serves as a conduction layer/contact for the solar cell [4,5,6,7]. The formation of nickel seed layer prior to Cupper through electroplating processes is a well-expanded technique that can only be used for conductors. The need of nickel seed layer is associated with this fact that since electroplating process cannot be done on semiconductors, an auto-catalytic method of nickel electroless plating (used to deposit nickel phosphorus or nickel boron) is needed in order to make contacts for the semiconducting surface of the cell. This nickel electroless plating method has already been evaluated and widely used in the formation of contacts for silicon solar cells [8,9]. The use of nickel as a seed layer is essential for metals to be plated on semiconducting or non-conducting materials. The process of nickel electroless plating needs a complexing agent, a buffer agent and a reducing agent that make it feasible for metal inos to deposit on the silicon surface. In spite of the conventional electroless plating of nickel seed layer, illumination is used while plating process, referred to as light induced electroless plating (LIEP)[10,11]. The approach of light induced plating (LIP)[12] invented by Fraunhofer ISE, broadly used for plating the silicon solar cell by many research groups. In the process of the LIP technique, a sample containing a n/p junction and an aluminum back contact formed by screen printing is immersed in a plating bath. The sample immersed in the plating solution is applied with a protective potential, so that rear of the cell can be made more cathodic, which results in the lowering of the aluminum corrosion[13]. The protective potential not only prevents the erosion of aluminum but also helps to

operate the cell closer to short circuit conditions and hence increases the plating uniformity[14]. The operating current density of the cell is enhanced by applied, resulting in faster plating rates. It is possible to control the height of the plated metal finger through The LIP arrangement. Moreover, LIP can be applied for metallization of the fully aluminum doped rea side at the same time. The schematic of such coper based LIP plating process is shown in Fig 2.1 In this work a detailed overview of the metallization technology based on the Ni/Cu plating process will be given. The experimental procedures involved for nickel seed layer formation by LIP will be discussed.

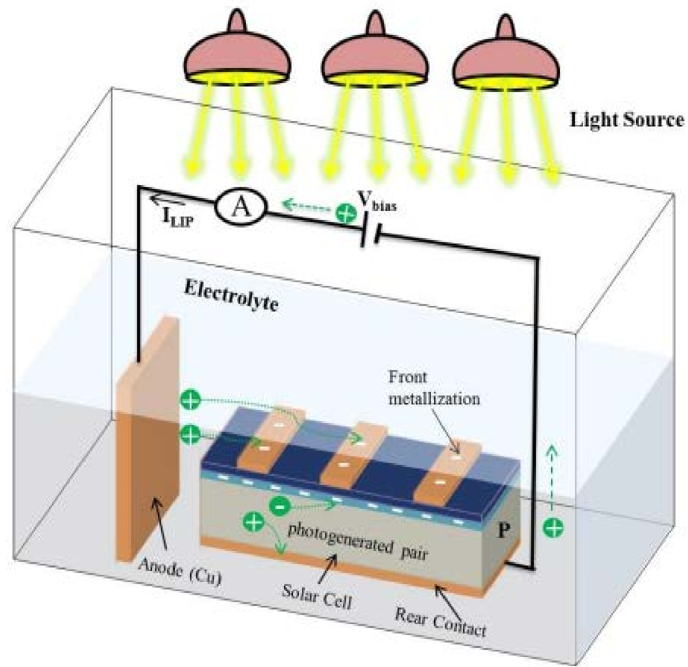


Fig 2.1 The schematic of Light Induced Electroless Metallization of silicon solar cell

2.1.1 Nickel Seed Layer Formation

In the first step, a couple of techniques such as electroless plating technique, light induced plating or laser assisted deposition can be used for Ni as a metal seed. In spite of nickel, other transition metals such as titanium (Ti) or tungsten (W) can also be used as a seed layer. Nickel is the most proper candidate since it plays a role as a diffusion barrier to Cupper as well as providing the low contact resistance to doped silicon. The nickel electroless deposition followed by an anneal treatment arranges an chance to form low resistivity ohmic contact layers[15]. There are a number of ways to perform the electroless plating process by adopting the concept of the oxidation reduction reaction. The plating rates can be changed significantly by using a light assisted plating (LIP) technique[16]. Laser assisted nickel deposition technique also provide another way for deposition of the nickel seed layer. The method is very much advantageous as the anti-reflection coating (ARC), ablation step can be performed along with the formation of the nickel seed layer. The adequate thickness and evenness over the entire front side patterned grid are the basic requirements for depositing an effective nickel barrier layer. The prevention of copper from being diffused for a desired lifetime defines the effectiveness of the barrier layer. However, a thinner nickel layer is favored as the nickel conductivity is low in comparison to Copper [17].

2.1.2 Electroless Plating

Electroless plating technique provide a well-established and suitable way for the nickel deposition process. It is an autocatalytic process that does not rely on the external supply of electricity. The reaction occurs during the deposition process providing the reduction of metals cations by means of electrons supplied by the reducing agent. The plating bath for nickel electroless plating is composed of the following bath compositions, including reducing agent of sodium hypophosphite [18].

a. Nickel chloride, ($NiCl_2 \cdot 6H_2O$) or nickel sulfate, ($NiSO_4[H_2O]_6$) as a main source of nickel
b. Sodium hypophosphite, ($NaH_2PO_2 \cdot H_2O$) as a reducing agent
c. Triammonium citrate [$(NH_4)_3C_6H_5O_7$] as a buffer and mild complex agent for nickel.

pH value of bath solution can be held in between 8 and 10 by adding of ammonium hydroxide (NH_4OH) to plating bath [19]. Catalytic oxidation-reduction reaction between hypophosphite ions and nickel is the base of this this plating process. The chemical reaction can be described as the sum of two simultaneous steps. The steps are outlined as follows [19]:

Step(1): $H_2PO_2^- + H_2O \rightarrow HPO_3^{2-} + H^-$ Eq. 2.1

Step(2) : $2H^- + Ni^{2+} \rightarrow Ni + H_2$ Eq. 2.2

Sum: $2H_2PO^{2-} + 2H_2O + Ni^{2+} \rightarrow Ni + H_2 + 4H^+ + 2HPO_3^{2-}$ Eq. 2.3

2.1.3 Light Induced Plating (LIP).

Light induced plating (LIP) baths were used for the deposition of nickel as a seed layer on silicon substrate. The chemical reactions (catalytic oxidation-reduction) occurring during the LIP nickel deposition process are the same as for the electroless plating bath explained in the previous section. However, the incorporation of a light source assists to adjust the electrochemical potential of the front and rear of the cell [20]. The photo voltage by the PN junction and the electronegativity of the substrates accommodate to govern the electron migration at the surface. moreover, the formation of these photo-generated electrons at the surface provides in the reduction of Ni^{2+} [21]. The plating process can be conducted at relatively lower temperatures with the addition of a light source in comparison to conventional electroless plating (non-LIP). Yu-Han et al., demonstrate light induced nickel plating (LINP) for p-type substrates having uniform metal surfaces and high intrinsic quality [22]. Apart, from higher plating rates with uniform metal surfaces, the process involves the difficulty regarding to the process characterization, as well as the dependence of plating on cell performance [23].

2.1.4 Laser Assisted Ni Deposition.

The use of lasers for depositing nickel as a seed layer has two advantage. The first one is it open the antireflection coating layer on the top of emitter layer and the second is it provide the condition for the seed layer deposition. The process involves the immersion of the solar cell in to an electrolyte solution and the application of a laser to write the grid from above. In fact, the temperature rise produced by the laser in the solution and the wafer provides the working basic of laser induced nickel deposition from an aqueous electrolyte solution[24]. Due to the producing of the heat in the area that is shine by laser, the antireflection coating layer is ablated. Subsequently the temperature rises in the electrolyte commence the decomposition of nickel particles. Moreover, at the same time, due to illumination of light, electron hole pairs are generated in the solar cell's junction. The generated electron moves to the top surface and induced the nickel deposition. A conformal deposited nickel throughout the process is required as the advantage of laser application. The water containing nickel salts could be helpful for the homogeneous coating of the wafers. The experience in laser induced deposition from liquids still needs more research to be stabilized [25]. The antireflective ablation accompanied with nickel deposition process by means of the laser chemical metal deposition (LCMD) process can play a key role in commercialization of nickel/cupper metallization for silicon solar cells. At Fraunhofer ISE, the LCMD process was applied for depositing nickel along with a nitride ablation step and followed by a Cu plating step [26].

Another laser based metal deposition process called laser transfer contact (LTC) was also used to deposit an nickel seed layer through an optically transparent glass and finger widths of less than 30 nm was obtained [27].

2. 1. 5 Nickel Silicide Formation.

After nickel deposition silicon/nickel stack is subjected to annealing process in a N_2 atmosfer to form an alloy of nickel and silicon. The alloy formed acts as seed layers for Copper, which is usually prepared at higher temperatures (300–400°C). This results in reduction of metal semiconductor contact resistance. The resistivity of nickel silicide is 14 $\mu\Omega$.cm, which is comparable to titanum silicide (13–16 $\mu\Omega$.cm) [28]. The nickel forms various phases with different compositions when heated at various temperature ranges, such as Ni_2Si (200–300 °C), NiSi (300–700°C) and $NiSi_2$ (700–900°C) [28]. The NiSi phase is identified as forming a lower resistivity state, and for that reason is beneficial for the metallization of silicon solar cells.

2. 1. 6 Uniform Nickel Seed Layer

Electroless nickel plating with a higher pH solution can solve the issue issue of depositing a uniform nickel layer on the surface of silicon [29]. The use LIP for nickel plating bath may also be useful for faster plating rates with higher level of uniformity. Apart from the uniformity of deposited nickel, this method can also help to improve contact adhesion. For a complete covering of the silicon surface an approach of depositing nickel seed layer with two steps nickel plating process, having a contact resistivity of 0.6 $m\Omega.cm^2$ has been demonstrated [30].

2. 2 Materials and Methods

P-type, single crystalline, (100) oriented Si wafers with a resistivity of 1Ωcm was used for preparing p-n junctions.

2.2.1 Texturization

The initial step in fabricating of a silicon solar cell is texturization process. Since some residual damages are left on the both side of As-cut silicon wafers. This saw damages appear as recombination center of photo generated electron hole pair. KOH texturing can remove those saw damage sites and also it can fabricate some pyramids on the surface of silicon which can dramatically enhanced the absorption of incident light. In order to texture the silicon wafer, a bath containing an alkaline etch solution consisting of de-ionized (DI)-water, potassium hydroxide (KOH) and isopropyl alcohol (IPA) was prepared. The KOH-IPA solution was heated to 80°C, and Si-wafers were immersed in bath. Alkaline solution is widely used as the standard KOH-IPA solution in the photovoltaic industry. The experimental setup used in this work is shown in Fig 2.2

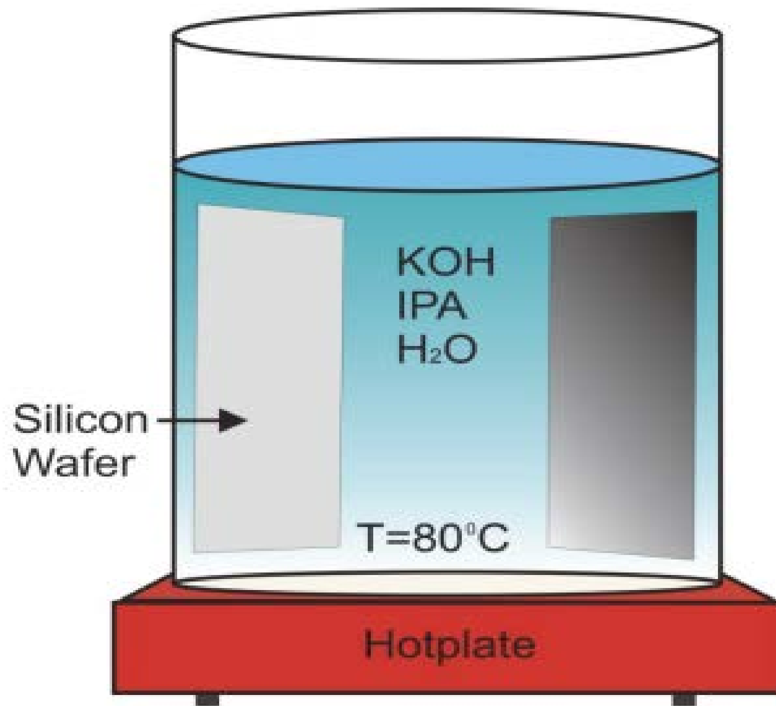


Fig 2.2 Experimental setup used in this study to texture mono-Si-wafers. Using a hotplate, the alkaline solution is heated in a glass beaker.

After that silicon wafers were subjected to solid state phosphorus-diffused in tube furnace to produce a n type layer on the surface of p type silicon wafer with resistivity of 50 Ω/square . Edge isolation was carried out with an industrial rear-etching process. A SiNx antireflection coating with a thickness of 80 nm and a refractive index of 2.07 was deposited on the front surface. Prior to the electroless plating, samples were subjected to a pre-treatment process, consisting of the following steps; (1) degreasing the surface using acetone by ultrasonic; (2) standard clean 1, using NH_4OH, H_2O_2, and H_2O in a volume ratio of 1:1:5 at 80°C for 10 min, (3) standard clean 2, using HCl, H_2O_2, and H_2O in in a volume ratio of 1:1:5 at 80°C for 10 min. A rinse with DI water and dilute HF dipping with 5% concentration was carried out at the end of each step for subsequent oxide removal and residual cleaning. Samples with conditioned surface were dipped into a plating bath composed of a mixture of $NiSO_4.6H_2O$ as the main nickel source, $NaH_2PO_2.H_2O$ as the reducing agent, $Na_3C_6H_5O_7$and NH_4Cl as complexing and buffer agent for nickel.

The cells were irradiated with a halogen lamp with density of 45 mW/Cm^2. Ammonia was used for pH control and temperature was controlled in the range of 60°C to 80°C. Fig 2.3 show a schematic of Light Induced Electroless Plating of nickel on n side of a silicon diode.

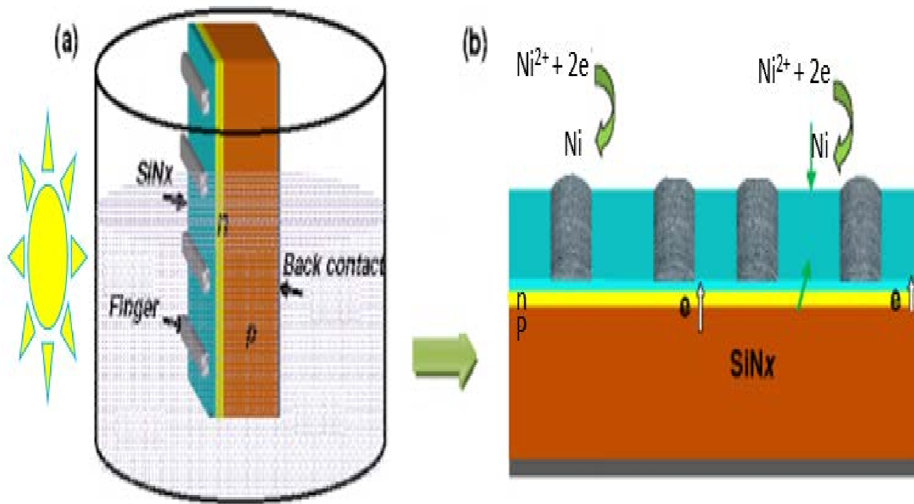


Fig 2.3 The schematic figure of Light Induced Electroless Plating of Ni seed layer on n side of a silicon diode.

Thickness of the deposited Ni-P films was measured using a surface profiler while surface topography of deposited nickel was examined using a Scanning Electron Microscopy.

Four-point probe measurement was used to examine the sheet resistance and electrical resistivity of deposited Ni-P film. Figure below shows the Four Point probe was applied for measurement of sheet resistance.

Fig 2.4 Four Point probe used for measuring the shear resistance of Ni-P film

Phosphorous content of Ni-P film was determined by X-Ray Photoelectron spectroscopy (XPS). In order to investigate the effect of annealing on the silicide formation, all deposited samples were annealed in a temperature range of 300°C – 900°C in a tube-furnace under N_2 atmosphere for 1 and 2 minutes.

TLM technique was applied to measure the contact resistance of Ni/NiSi/Si stack and phase transition for different types of nickel silicide was characterized using X-ray diffractometer and Raman Spectroscopy.

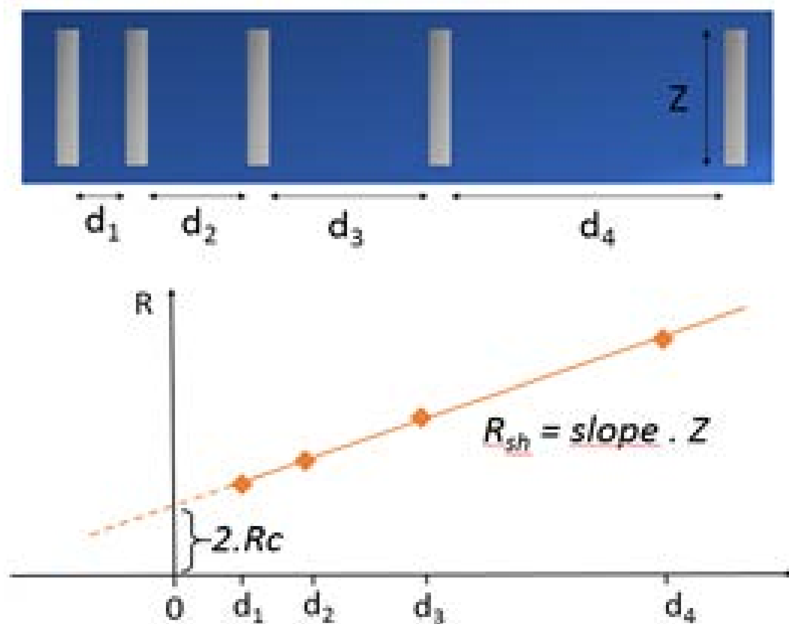


Fig 2.5 TLM technique was used to measure the contact resistivity.

2.3 Results and discussion

The first process in fabricating of silicon solar cell corresponds to the texturization of the as-cut silicon wafers with the aim of decreasing the reflectance of light from the surface wafer and removing the residual saw damages of as-cut silicon. Since KOH texturing is an anisotropic etching process then some crystal planes show higher rate of etching compare to others so it forms small pyramids is the rage of let than 10 μm. The saw damage should be removed in order to avoid high charge carrier recombination at the surface. An example of pyramidal texture generated via this etching process is shown in Fig 2.6. It is seen that small pyramids cover the silicon surface (etching time = 25 min).

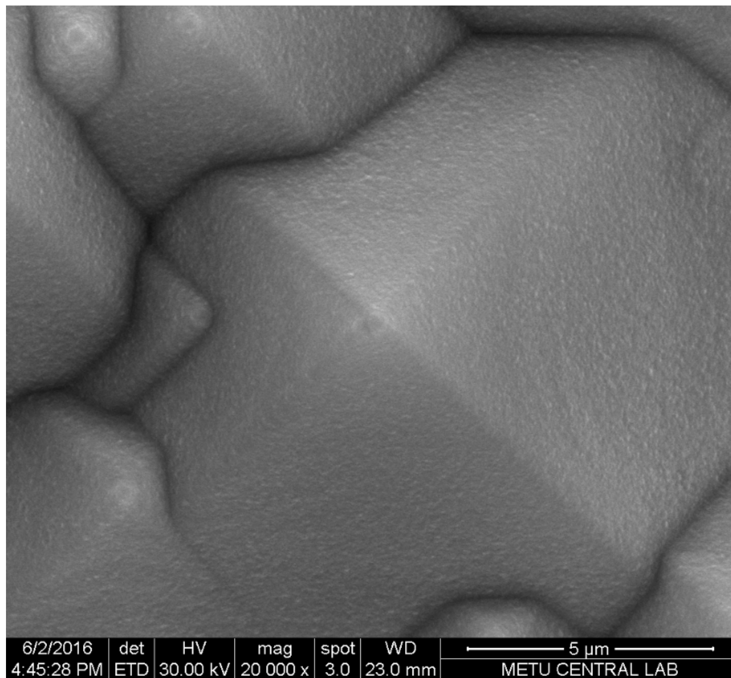


Fig 2.6 The pyramid texture on mono c-si wafer. The as-cut Si-wafer was etched for 25 min in standard KOH-IPA solution at 80°C.

2.3.1 Characterization of deposited Ni-P film

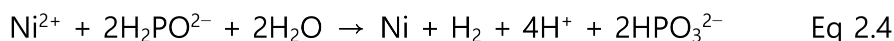
As it was mentioned in introduction, since the diffusion of Copper into emitter layer of silicon is undesirable for reliability of solar cell then surface coverage of nickel prior to copper plating is one of the most critical factor of light induced electroless plated nickel seed layer [28].

Fig 2.7 (a) and 2.7 (b) depicts the SEM images of the LIEP Ni-P film obtained at 60°C in an alkaline bath at a pH of above 10 for 5 minutes plating. As it is obviously seen in Fig 2.7 (a), surface of pyramids is homogeneously covered by nickel and this uniform and smooth coverage of nickel is due to the existence of super fine nickel particles which dispersed on the silicon surface. Such small grain sizes ensure a large contact area between the metal and the silicon semiconductor which is prerequisite for obtaining good level of adhesion between seed layer and Si substrate due to the negligible amount of voids in the Ni-P seed layer .

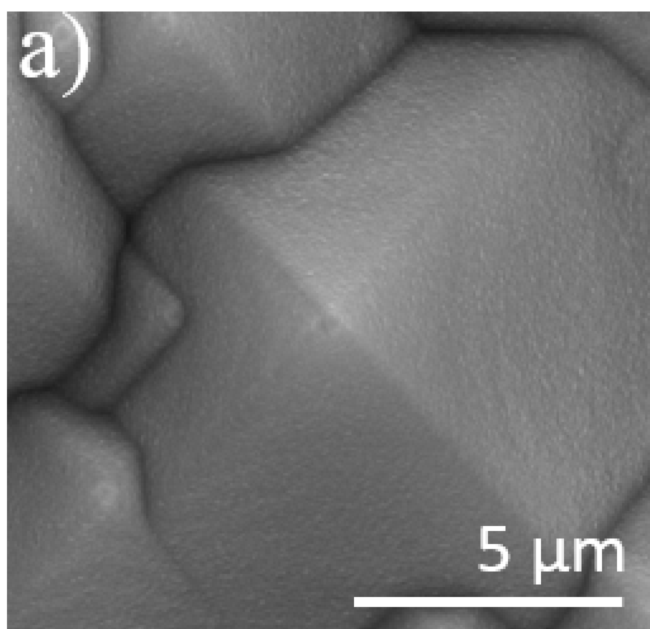
Fig. 2.7 (b) shows the cross-sectional SEM image of Ni-P seed layer on Si. It is apparent that fine nickel particles covers the valleys as well as the tip of pyramid uniformly with the thickness of about 200 nm which can reduce the risk of potential shunting of shallow junction (2). Fig 1 (c) and 1d show the surface of pyramid after 10 minutes immersion in nickel bath without any light illumination during plating process. As it is seen in Fig 2.7(c) even though the plating time was longer, deposited nickel did fully cover the surface of silicon pyramid and some arears were left blanket. Fig 2.7 (b) clearly shows that nickel deposition initiates from the tip of pyramids forming a rough and discontinuous film. It is expected that as plating time goes on, valise of pyramids also are filled by nickel. It is assumed that the fabrication of this conformal Ni-P film under light illumination was attributed not only to the bath conditions

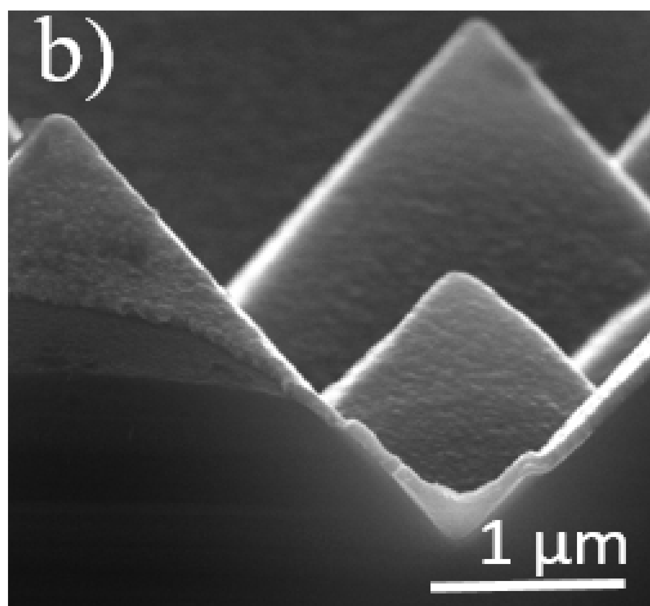
but to the role of light in providing electron for reducing the Ni^{2+} on the surface of silicon. Fig 2.8 represents SEM images that indicates the effect of pH tuning on the quality and size of Ni-P particles. As it is presented in Fig. 2.8 (a), the fine and nodular free Ni-P film were obtained for alkaline bah at pH of 10 at 60°C with plating intervals up to 5 min. Decreasing of pH from 10 to 8 (Fig 2.8 (a) to 2.8 (b)) results in rougher and bigger size of the Ni-P particles. As pH dropped from 8 to 6 (Fig 2 (c) and 2 (d)), nickel particles became bigger in size and moreover they appear as numerous individual spherical.

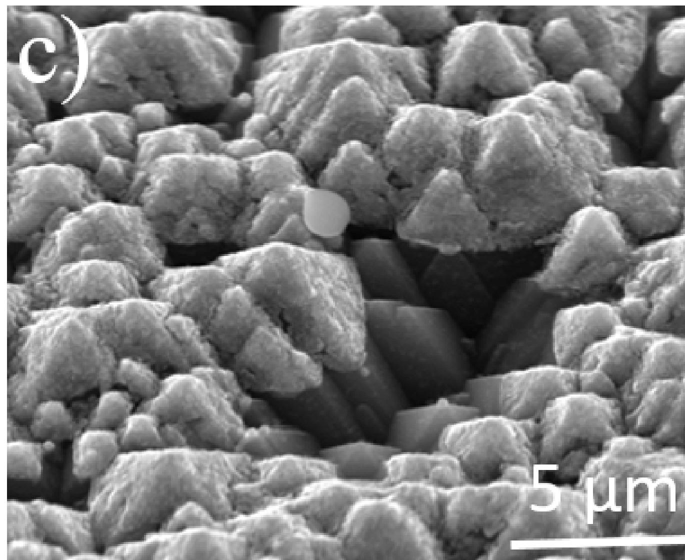
particles on the pyramid surface rather than a continuous thin metal layer which also demonstrates the low rate of nucleation of nickel particles for low pH values. Electroless nickel plating is an autocatalytic process by immersion of a substrate in a plating bath and it is based on the capture of electrons by the nickel cations Ni^{2+} present in the solution according to the following reaction.



$$Ni^{2+} + 2H_2PO^{2-} + 2H_2O \rightarrow Ni + H_2 + 4H^{+} + 2HPO_3^{2-} \qquad \text{Eq 2.4}$$


a)
5 µm


b)
1 µm



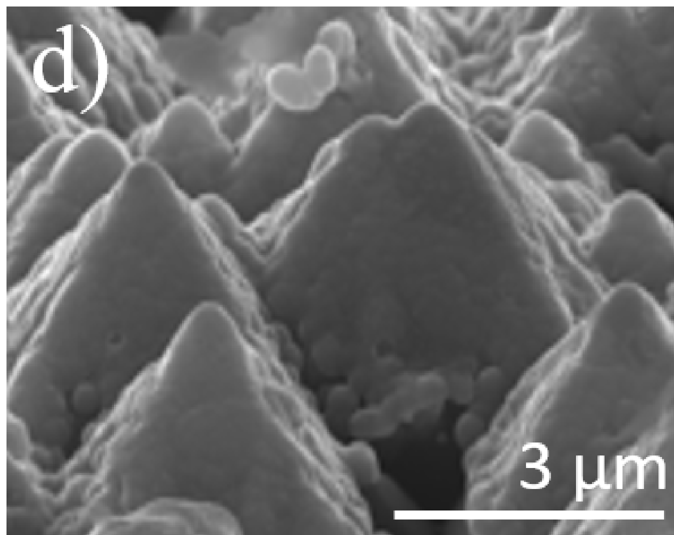
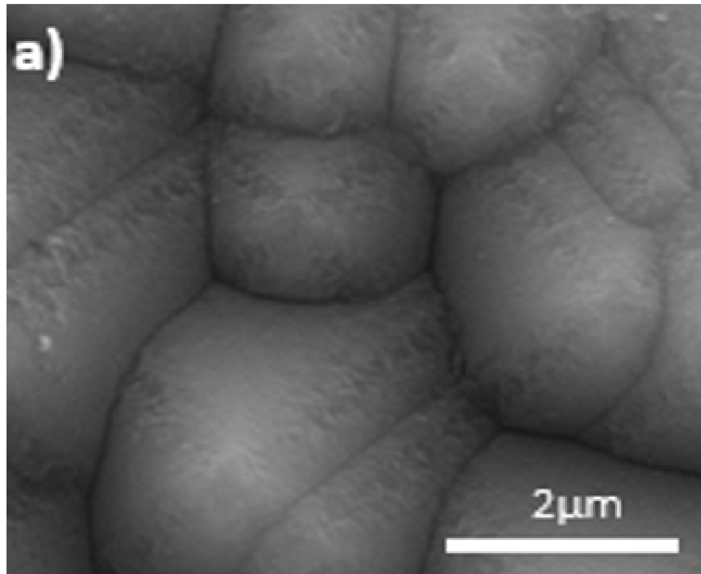
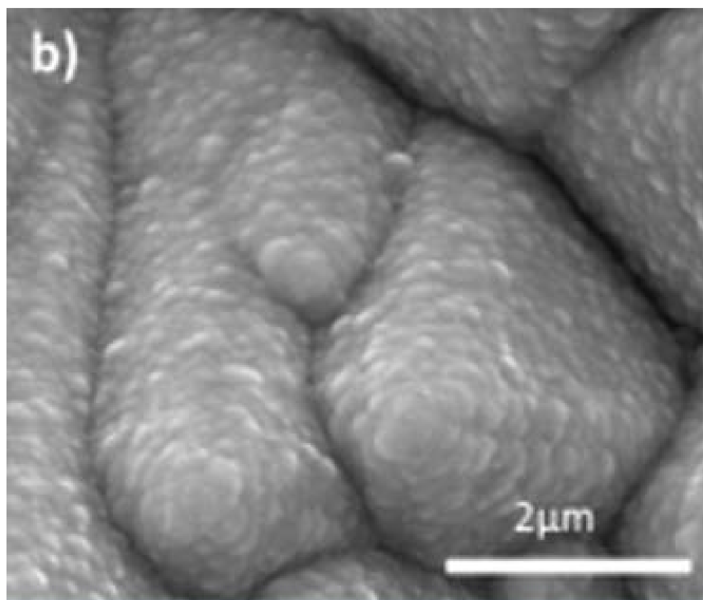


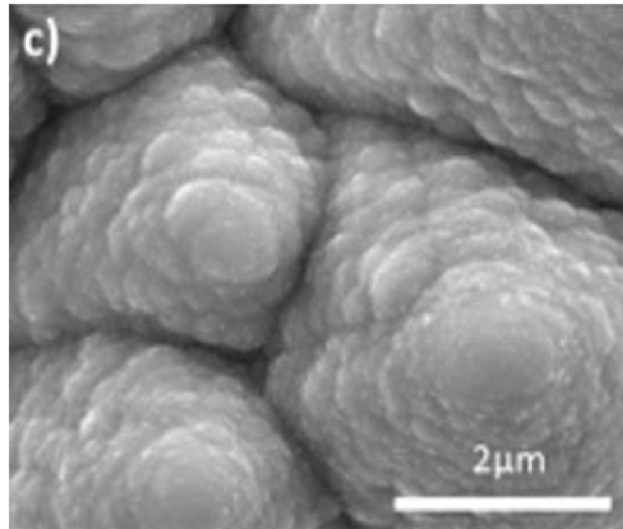
Fig 2.7 Light induced electroless Plated Ni-P seed layer fully covering silicon pyramids (a) Top view (b) Cross section. (c) Ni Plating on the surface of silicon without light illumination.

The enlargement and aggressive shape of particles with decreasing the pH is associated with the anodic reaction of NaH_2PO_2 as reducing agent which leads to the releasing of lower amount of free electrons in the bath facilating less oxidation of NaH_2PO_2. Therefore, the nucleation density of Ni-P particles on Si substrate becomes smaller since Ni^{2+} Ions confront less amount of free electrons and deposited Ni-P particles will grow more to reach to the neighbouring Ni-P particles therefore the size of particles become bigger.

Fig 2.8 (e) and 2.8 (f) represent the formation of a crack into the Ni-P film which tears and peels off the nickel seed layer from silicon substrate. As it is depicted in figure 2.8 (e) the Ni-P film could not tolerate the thickness of over 20 μm since it leads to releasing of mechanical stress in Ni-P film and eventually peeling off the film from the Si pyramid surface. Fig 2.8 (f) shows that crack propagates along to the nickel particle grain boundaries and it continuous through the whole surface of Ni-P film.


a)
2µm


b)
2µm



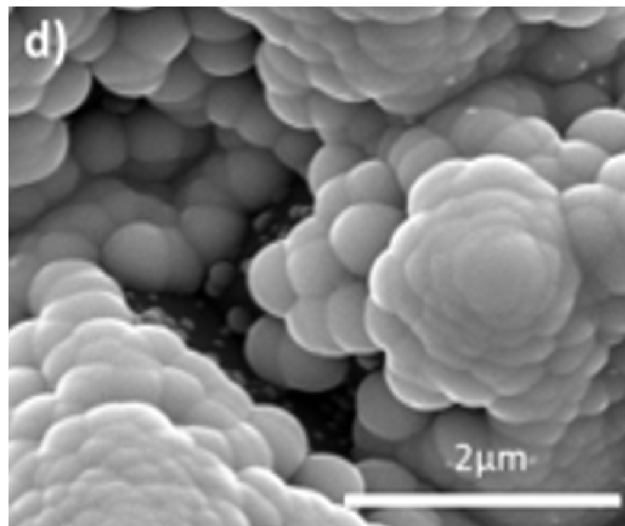
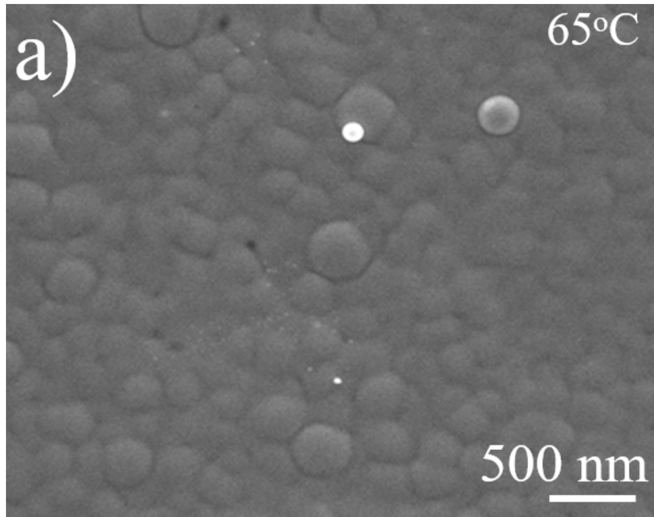
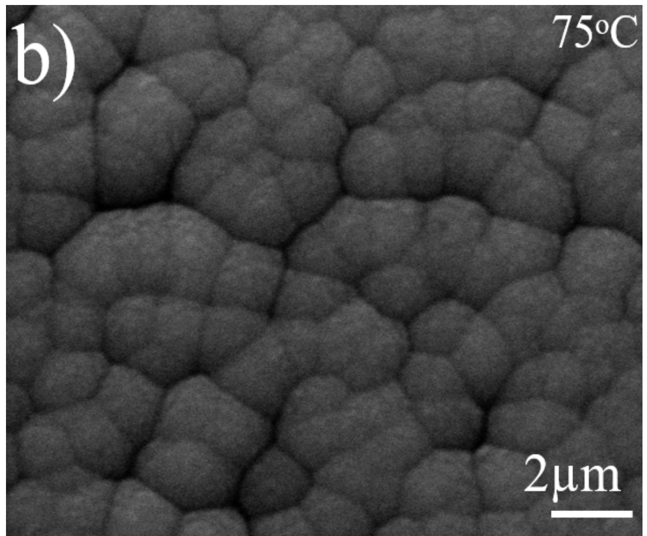


Fig 2.8 Top down of SEM micrographs showing the surface morphology of electroless plated nickel seed layer at 60°C and various pH. (a)10, (b)8, (c)7, and (d)6. (e), (f) SEM image showing the crack propagation into the Ni-P seed layer.

Fig 2.9 Represent the top view SEM image of deposited Ni-P film in three different temperatures. As it can be seen the size of nickel particles grow from 300 nm to 500 nm and finally to 15000 nm as the temperature of bath drops from 80°C to 70°C and to 60°C respectively. This phenomenon can be explained in this way that apart from the influence of pH on the morphology of deposited Ni-P film, the rate of the reduction reaction of nickel atoms is influenced by the temperature of bath in an exponential manner. This relation can be attributed to this fact that the temperature of bath provides the energy needed for the chemical bonding occurring from the metal oxidation. In the other word, temperature of bath supplies the activation energy for reduction of Ni^{2+} so at low temperature lower amount of Ni^{2+} is reduced and deposited on the Si surface [28].


a)
65°C
500 nm


b)
75°C
2μm

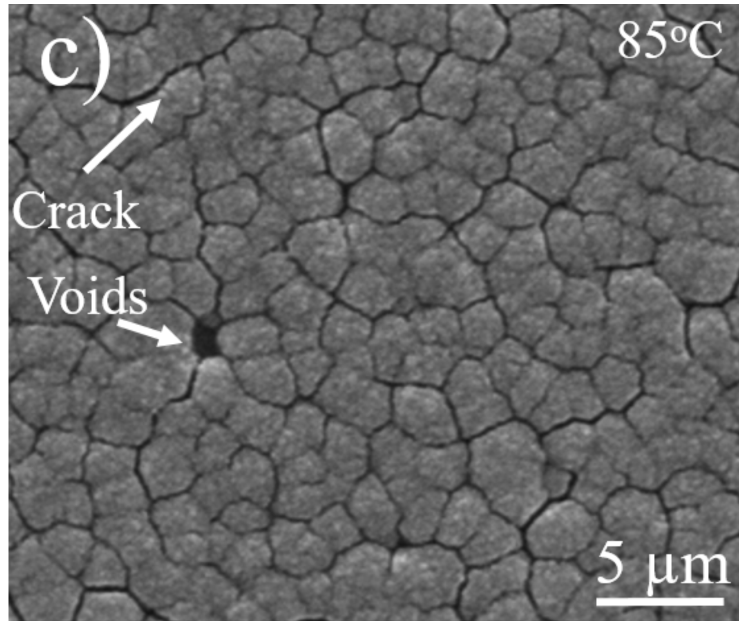
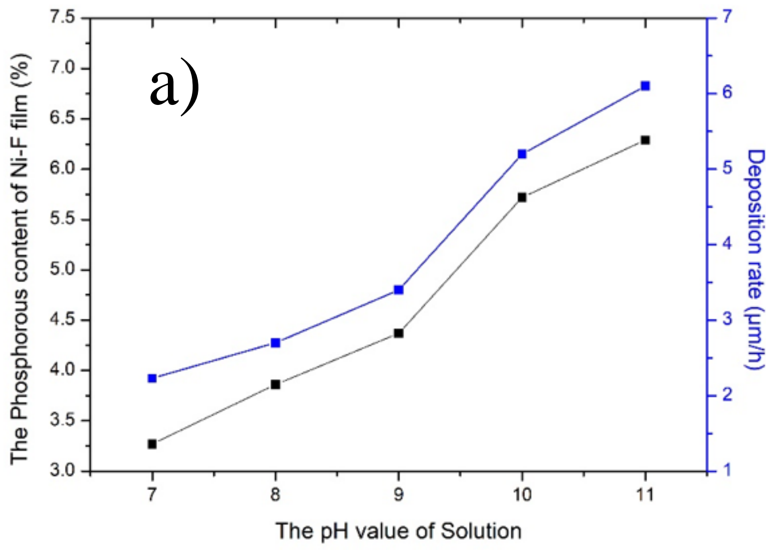
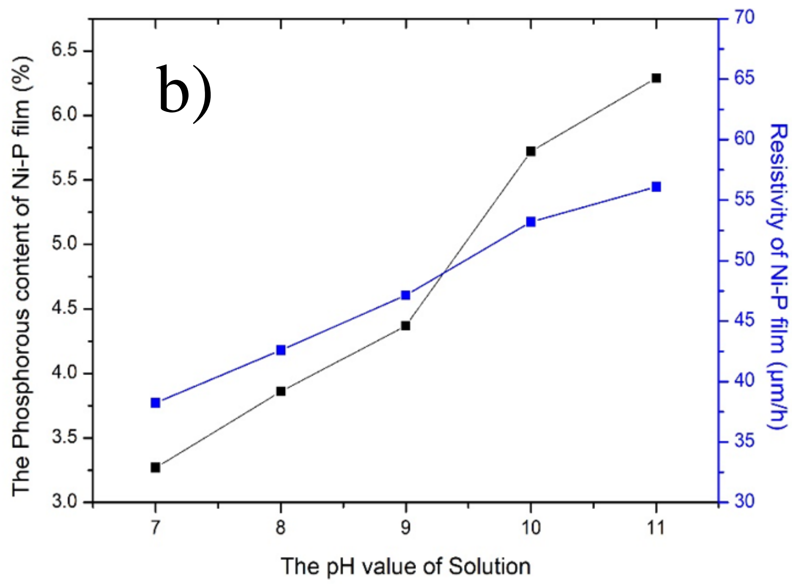
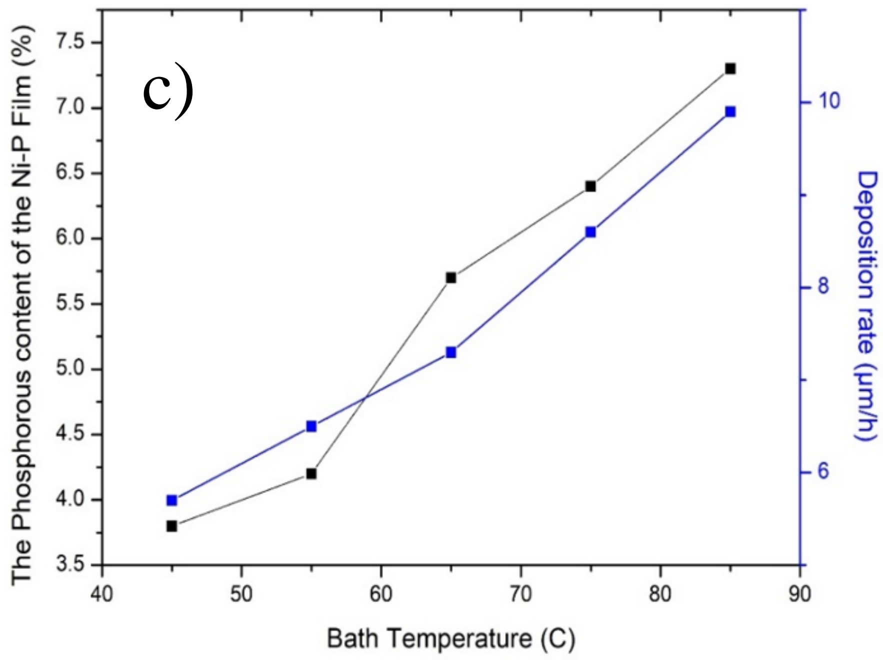


Fig 2.9 Top view SEM image of deposited nickel particles at different temperatures. (a) 65° C, (b)75°C and (c)85°C.


a)
The Phosphorous content of Ni-F film (%)
Deposition rate (μm/h)
The pH value of Solution
7.5
7.0
6.5
6.0
5.5
5.0
4.5
4.0
3.5
3.0
7
6
5
4
3
2
1
7
8
9
10
11


b)
The Phosphorous content of Ni-P film (%)
Resistivity of Ni-P film (μm/h)
The pH value of Solution
6.5
6.0
5.5
5.0
4.5
4.0
3.5
3.0
70
65
60
55
50
45
40
35
30
7
8
9
10
11


c)
The Phosphorous content of the Ni-P Film (%)
Deposition rate (µm/h)
Bath Temperature (C)
7.5
7.0
6.5
6.0
5.5
5.0
4.5
4.0
3.5
10
8
6
40
50
60
70
80
90

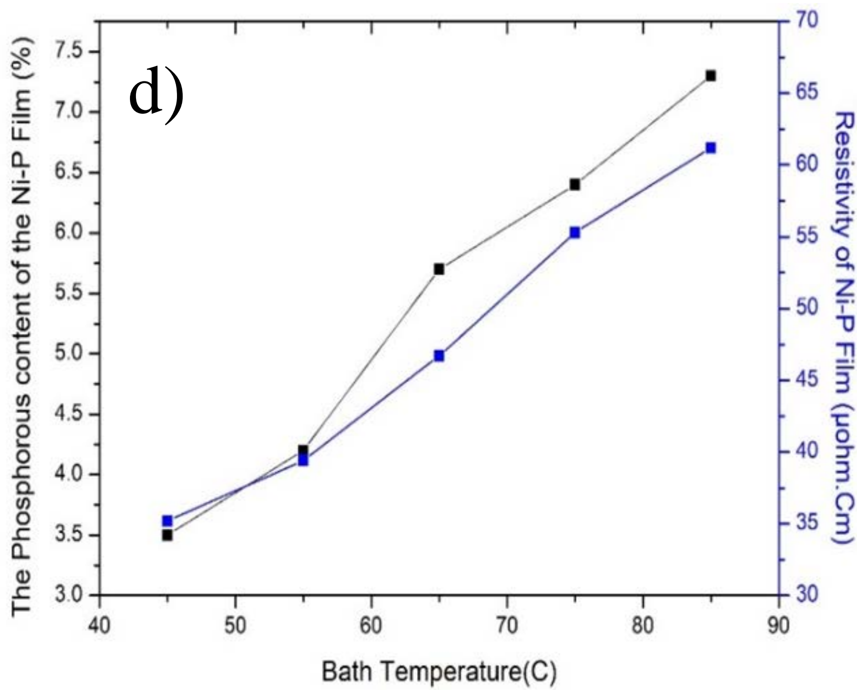


Fig 2.10 Electrical behavior and phosphorous content of electroless Ni-P seed layer as a function of (a) Effect of pH on the rate of deposition and content of phosphorous (b) Effect of pH of the resistivity of Ni-P Film. (c). Effect of temperature on the rate of deposition and content of phosphorous (d). Effect of pH om the resistivity of Ni-P film.

Fig 2.10 represent the effect of pH and temperature of bath on the amount of incorporated phosphorous and electrical resistivity of Ni-P film. As it is indicated in Fig 2.10 (a), as the temperature of bath increases, more amount of phosphorous are precipitated in the nickel film due to the increasing of the activity of sodium hypophosphite in our bath and they appear as collision centers in nickel structure and on the other hand, as it can be seen from Fig 2.9, the size of nickel particles deposited at 80°C is around 300 nm while it increases to 5000 nm at 70°C and 15000 nm at 60°C. This means that nickel particles grow faster at lower temperature of bath or in other word, at lower temperature less nucleation sites are formed which results in lower density of nucleation sites on a unit surface. Therefore, it results in lower density of grain boundaries which causes lower scattering of drifting electrons. Therefore, based on Fig 2.10 (a) the conductivity of deposited Ni-P layer is decreased as temperature is increased and this is attributed with this fact that the grain boundaries and incorporated phosphorous toms are considered as scattering matters in nickel phase and based on equation 2.5 they decrease the relaxation time of electron movement.

As it can be shown in Fig 2.10 (b) Increasing the pH has inverse effect on the activity of sodium hypophosphite which results in lower precipitation of incorporated phosphorous in Ni-P film. Meanwhile based on Fig. 2.8 as pH is increased the size of deposited Ni-P particles becomes finer which means that more density of grain boundaries is achieved. Therefore, the density of grain boundaries and the amount of incorporated phosphorous in Ni-P film as a function of varying pH have two opposite effect on the conductivity of Ni-P film. However, as Fig 2.10 (b) demonstrates the resistivity of film is decreased as the pH of bath is increased it means that the influence of incorporated phosphorous on the scattering of electrons during its movement in Ni-P film is higher that the role of density of Ni-P grain boundaries.

Eq 2.5 is known as quantum mechanical expression of the conductivity [31].

$$\boldsymbol{\sigma} = \frac{1}{3} v_f{}^2 \tau N(Ef) e^2 \qquad \text{Eq. 2.5}$$

Where;

σ : electrical conductivity;

τ : relaxation time;

vf : fermi velocity

N(Ef) : population density of electrons at Fermi level.

The relaxation time is defined as the time between two constructive collision of drifting electrons and impurities in solid.

2.3.2 Phase identification

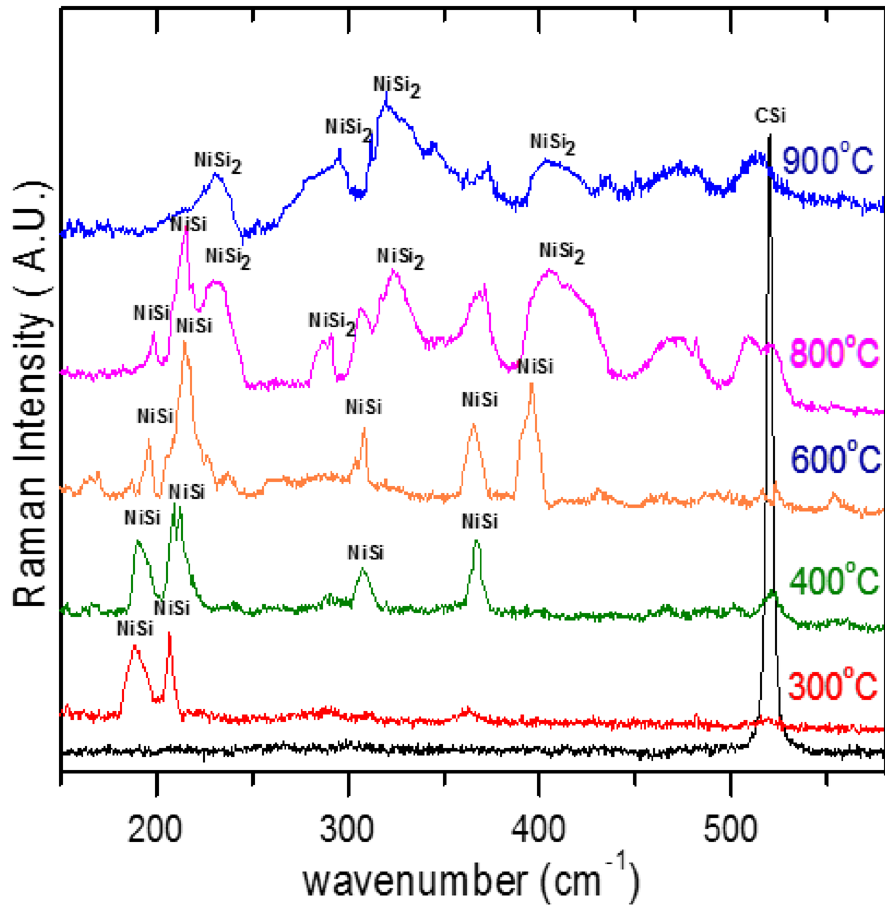


Fig 2.11 (a). Raman Spectra of NiSi film annealed at different temperatures on (100) Si substrates.

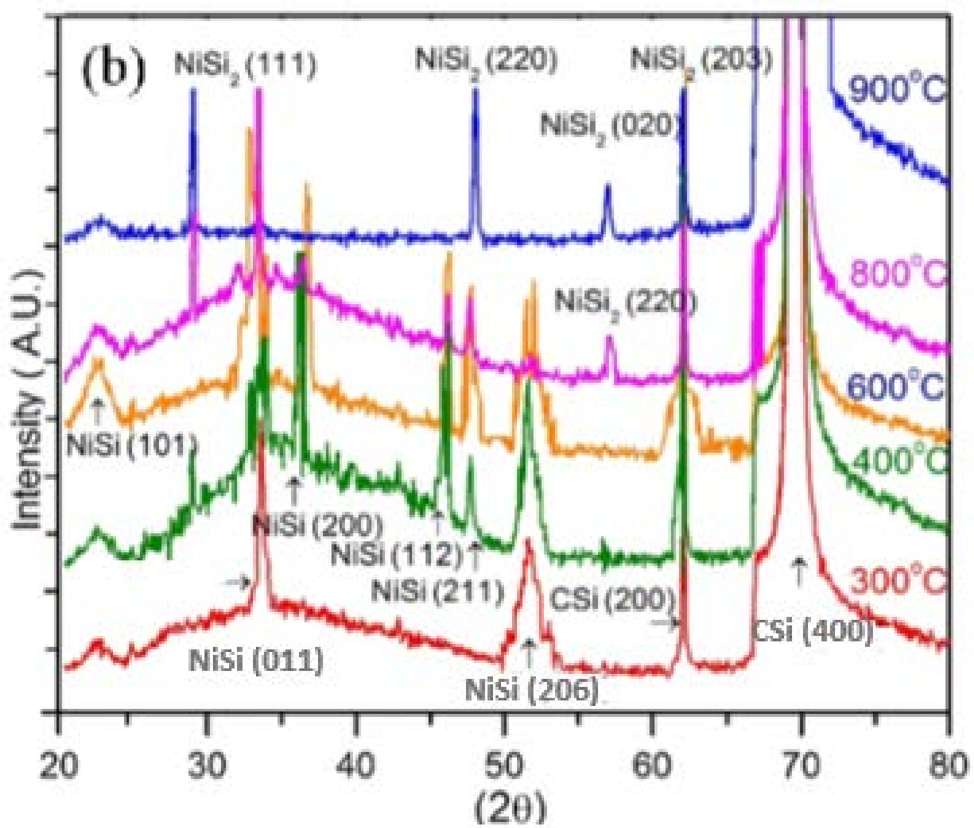


Fig 2.11 (b) XRD spectrum of the Si/NiP (200 nm) structure annealed at various temperatures without unreacted metal.

phase identification through X-ray diffractometer and Raman spectroscopy are two well-known techniques for phase characterization of different type of silicide[32]. Since the nickel silicide has orthorhombic crystal structure it is Raman active and based on group theory it is expected to be characterized by 12 Raman active optical phonons[33]. Figure 2.11 (a) represent a series of random position of Raman spectra of Si/Ni-P samples annealed at different temperatures. The Raman spectrum of the original silicon sample, before annealing, contains only the silicon sharp line at 520 cm^{-1}. it shows that there is no sign of silicide formation in the un-annealed Si/NiP film. However not all of its Raman active modes are detected due to various degree of texturing. Raman spectrum of Si/NiP film annealed at 300°C shows two distinguishable peaks at 189 cm^{-1} and 207 cm^{-1} belonging to nickel mono-silicide (NiSi). It is evident that these peaks are shifted by 8 cm^{-1} and 7cm^{-1} to lower frequency from the reference of powder nickel silicide and this movement of phonon peaks from higher frequency to lower frequency is associated with the existence of residual tensile stress which has remained in the NiSi film after annealing. As annealing temperature is increased to 400°C, two more new lines appeared at 308 cm^{-1} and 367 cm^{-1} which are unambiguously interpreted as lines for the nickel silicide. It is evident that increasing the annealing temperature from 300°C to 400°C results in releasing of tensile stress since first two pair of peaks appeared at 191 cm^{-1} and 209 cm^{-1} were moved 2cm^{-1} higher in frequency compared to same peaks formed at 300°C. Further annealing at 600°C result in formation of another peak of nickel silicide

at $397cm^{-1}$ and in this temperature existence of first two peaks at $197cm^{-1}$ and 214 cm^{-1} confirm that NiSi contains the lowest residual stress after at this temperature. For samples annealed in the critical phase transition temperature gap, above 600°C up to 800°C, Raman clearly demonstrate a mixture of NiSi and $NiSi_2$ phases while the 199 cm^{-1}, 227 cm^{-1}, 308 cm^{-1}, 369 cm^{-1}, 395 cm^{-1} belong to NiSi whereas 232 cm^{-1}, 317 cm^{-1}, 366 cm^{-1}, 405 cm^{-1} demonstrate the existence of $NiSi_2$. Existence of this peaks demonstrate the existence of high resistance $NiSi_2$ phase at 800°C which also was verified by XRD patterns. Moreover, as it can be seen at this temperature first two peaks of NiSi are positioned at 199 cm^{-1} and 220 cm^{-1} are shifted to the higher frequency side. This shifting of peaks from lower frequency to higher frequency is attributed to the remained compressive stress in nickel Silicide film. The most top graph represents the Raman Spectrum of sample annealed at 900°C. As it is shown there are couple of peaks at 232 cm–1, 297 cm^{-1}, 320 cm^{-1} and 402 cm^{-1} which are contributed to the existence of NiSi2 phase and there is also no distinguishable line belonging to low resistance NiSi which means that at 900°C transition of NiSi to $NiSi_2$ is fully completed and NiSi disappeared entirely. Fig2.11 (b), shows the X-ray diffraction patterns of Si/Ni-P samples after annealing at different temperatures. The first lowest pattern belongs to the sample which was annealed at 300°C, as it can be seen there are two sharp peaks at (200) and (400) planes contributed to the silicon substrate. Moreover, another two peaks were observed corresponding to NiSi (200) and NiSi (103) confirms that low resistance nickel mono-silicide already was formed in

this temperature which supported by Raman data as well. As the annealing temperature increases new peaks are diffracted from NiSi (111), NiSi (112) and NiSi (211) planes indicating that Orthorhombic crystal structure of NiSi is growing at 400C and the existence of this phase can be demonstrated by the diffraction of X-ray on the same planes even at 600°C. Further Annealing at 800°C results in the emerging of new peaks coexisting with former peaks belonging to NiSi. As it can be seen at 800°C NiSi peaks were getting weaker while the new crystalline orientations corresponding to $NiSi_2$(111), $NiSi_2$(020) and $NiSi_2$(203) were forming indicating that at 800°C demonstrating the existence of high resistance $NiSi_2$ which was also verified by Raman results. A further point that can be extracted from XRD peaks is that, due to the excellent epitaxy of a-$NiSi_2$ with Si at 2θ=62.5 we have an overlap of both $NiSi_2$ and crystalline Si substrate peaks however, since the lattice parametrs of $NiSi_2$ (5.416A) and Crystalline silicon (5.430) are different then their corresponding orientation which results is diffraction of X-ray are varied ((200) for Crystalline Si and (203) for $NiSi_2$) [33].

2.3.3 TLM Measurement

The Transfer Length Method [TLM] is commonly used to model the metal-semiconductor contact resistivity. The TLM consists of sets of resistors representing the metal, diffusion, and interfacial layers of a contact [34]. The variation of contact resistivity as a function of 1 and 2 minutes of annealing in different temperature is shown in Fig 2.12 The contact resistivity of as deposited 150 nm Ni-P film was 22.6 $m\Omega.cm^2$ while after annealing at 350°C, it drops to 35 percent of its original value. Further increasing in annealing temperature to 400°C and 500°C contribute to further drop of contact resistivity to 29.2 and 28.7 percent of its original value respectively. From 500°C to 800°C there is a moderate increasing of contact resistivity whereas this increasing trend accelerated as temperature raises from 800°C to 850°C which leads to a shift of contact resistivity to 45 percent of its original value. It can be obviously seen that the contact resistivity of sample annealed at 350°C and 700°C is more or less in the same range. The reason of this similarity can be explained in this way that although there are some peaks at 800 °C belonging to high resistance $SiNi_2$ however the initiation of formation of this phase is in the temperature range of 600 °C to 800 °C therefor at 700 °C we have a mixture of majority portion of low resistance NiSi phase and a minority portion of high resistance $NiSi_2$ phase which keeps its contact resistance almost similar to sample annealed at 350 °C. However as annealing temperature is increased the NiSi2 phase is growing more and consequently the contact resistivity is

increased. Above 850°C surprisingly contact resistivity suddenly increase to the highest point in this graph and this is due to existence of high resistance $NiSi_2$ phase which also was supported by XRD and Raman data.

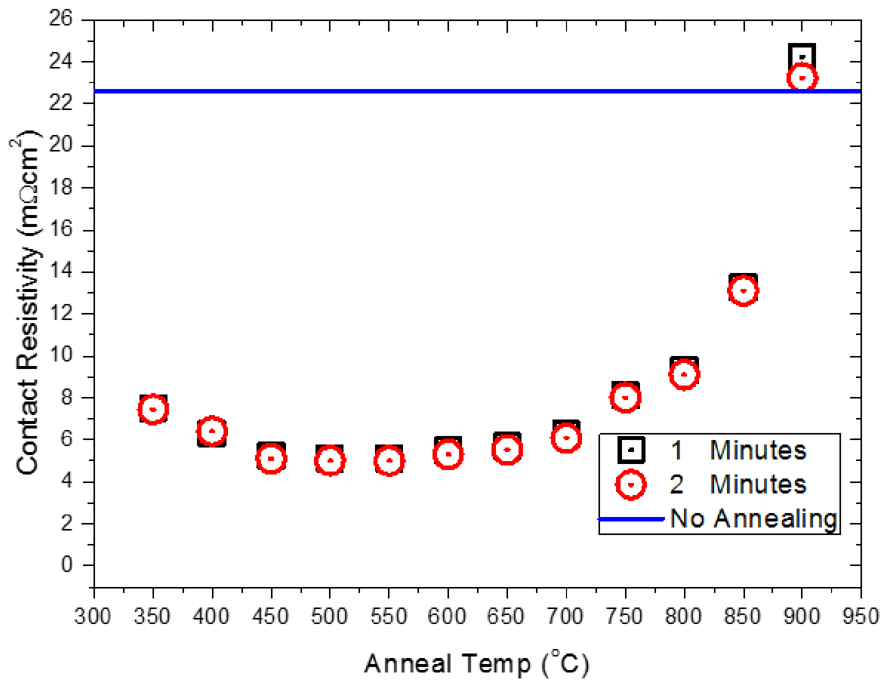


Fig 2.12 Transmission Line measurement of Ni-Si contact after 1 and 2 minutes annealing in N_2 atmosphere.

2.4 Conclusion

Material characterization of LIEP-based Ni-P seed layer and subsequent Ni silicide on the n-side of c-Si diode was investigated. It was shown that Ni-P film covered the valleys as well as the tip of the pyramids uniformly at 60 °C and at a pH above 10. The increase in pH leads to the decrease in phosphorus incorporation and the increase in the particle boundaries density of Ni-P film. Results indicated that the role of incorporated phosphorous had a larger influence on the conductivity of film than the role of boundaries density. Elevation of bath temperature resulted in an increase in the phosphorous precipitation as well as particle boundary density that correspondingly decreased the conductivity of Ni-P film. It was observed that Ni-P film thicker than 20 μm was peeled off from the top of the pyramids. We have identified the evolution of the residual stress in the film as a function of the annealing temperature. Raman and XRD measurements consistently revealed the phase transformation between NiSi and $NiSi_2$ phases upon varying annealing temperatures. It was found that as annealing temperature was increased from 300 ◦C to 600 ◦C, residual tensile stress of NiSi phase dropped to its minimum level. However, as annealing temperature exceeded 600 ◦C, a compressive stress was developed in NiSi phase and NiSi was fully transformed to NiSi2 at 900 °C. Based on the TLM measurements, the contact resistivity of Si/Ni stack followed the phase transformation sequence as a function of annealing temperature. The lowest contact resistivity was obtained in the temperature range of 450

$^{\circ}$C - 500 $\circ$C, where the NiSi/Si junction dominates the interface.

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1.6. Purpose of Research.

This work consists of two parts. In the first part the main purpose of this research was to use nickel as a catalyst to fabricate low reflective nanoporose single and multy crystalline silicon through wet electroless etching mechanism. An aqueous bath containing H2O2 and HF having particular amount of NiSO4 was prepared to provide redox reaction on the surface of silicon. Due to this redox reactions H2O2 is reduced and transfer positive charges to the nickel catalyst. Nickel inject the positive charges to the Si and etches it. We fabricate the Al-BSF solar cell on our nanotured Si wafer. In the second the pain purpose was to use cupper for metallization of silicon diode. However since the diffusability of cupper into silicon is high then light induced electroless plating technique was used to plate nickel on the silicon surface in order to play a role as a seed layer to prevent the diffusion of cupper into silicon.