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Ph.D.Dissertation

A Study on Subharmonically Injection-Locked PLL With Dual-Edge Complementary Switched Injection

상보적인 스위치 동작을 이용한 주입 고정 위상 동기화 루프의 설계에 관한 연구

by

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February, 2019

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A Study on Subharmonically Injection-Locked PLL With Dual-Edge Complementary Switched Injection

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A Study on Subharmonically Injection-Locked PLL With Dual-Edge Complementary Switched Injection

by

Sung-Yong Cho

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Abstract

As increasing demands for high speeds link systems and requiring design challenges in clock generation, the injection locking technique is widely used in clock multiplication. However, it is still difficult to design high performance of injection-locked clock multiplier (ILCM) because of its narrow lock-in range. In this thesis, a low-phase-noise subharmonically injection-locked sub-sampling all-digital phase-locked loop (ILPLL) is proposed using a dual-edge complementary switched injection (CSI) technique and sub-sampling bang-bang phase detector (SSBBPD) without an injection pulse generation and injection timing calibration circuitry. With the proposed IL-DCO and SSBBPD, the phase alignment mismatch between the PLL loop and injection path does not occurs and makes it possible to exhibit a simplified architecture.

Because the CSI technique exploits dual-edge injection, the performance impact of dual-edge injection when inaccurate injection time occurs is analyzed. Also, the CSI technique is analyzed with base on the charge transfer and derives the realignment factor of the injection. With the CSI technique and the direct connection of the digitally controlled oscillator (DCO) clock to the SSBBPD, the timing mismatch between the PLL loop and injection path becomes less sensitive to voltage and temperature drift. The proposed ILPLL prototype is fabricated in a 65-nm CMOS process and achieves a 168-fs integrated RMS jitter over 1 kHz to 40 MHz at a 5-GHz output frequency with 156.25-MHz reference clock while consuming 15.4 mW with an active area of 0.06 mm^2.

Keywords : All-digital PLL (ADPLL), dual-edge injection, frequency detector, injection-locked oscillator (ILO), reference spur, sense-amplifier, sub-sampling PLL

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Chapter 1

Introduction

1.1 Motivation

A low noise clock synthesizer has many applications such as high-performance serial link communication systems. Recently developed, injection locking technique is one of the most promising solution for low jitter at low power consumption [1]–[33]. One of the advantages of the injection locking is achieving high performance of clock generation with simple architecture. However, challenges remain in developing a robust clock generation using injection-locked oscillator (ILO). First of all, the subhamonically ILO has a small lock-in range with large multiplication factor. When the oscillator frequency is deviated from the lock-in range, the frequency could be unstable as known as quasi-lock [1]. Even though the oscillator is under injection locked, when the free-running frequency is not perfectly harmonic

of the injection frequency, the phase noise and spur performance is degraded. Nonetheless, the main reason of using injection locking is that it can expand the noise filtering bandwidth compared to conventional PLL bandwidth, which limited to one tenth of the reference frequency. It means that the injection locking can maximize the performance even with the jittery oscillator such as ring oscillator. For example, multiplying delay-locked loop (MDLL) structure [34]–[37], whose injection strength is a hundred percent, has a bandwidth of approximately 0.4 times reference frequency as studied in [2].

To overcome the narrow lock-in range of injection locking with large multiplication factor, it is necessary to adopt frequency tracking loop (FLL) in the background. Basically, the injection can be achieved with the conventional PLL structure. However, when the injection timing is not set, the phase of the oscillator clock try to align at the two points and the injection and PLL loop compete with each other. Consequently, the frequency error occurs and results in degrading phase noise and reference spurs. Recently, there are several methods to track real time frequency in the injection locked clock multiplier (ILCM). Nullifying the frequency error, they could achieve low jitter and low spur clock generation.

In this thesis, the proposed injection-locked PLL (ILPLL) achieve low jitter and wide range without additional injection timing calibration circuitry. The proposed ILPLL achieve –243.6 dBc of figure-of-merit (FOM), which is the state-of-the-art among recently presented PLLs.

1.2 Thesis Organization

This thesis is organized as follows. In Chapter 2, the basics of the ILO and ILCM are explained. With the prior arts of the ILCM, the designs are organized and introduced with the design issues. Then, the concept of the proposed ILPLL is briefly introduced.

In Chapter 3, an ILPLL with a dual-edge complementary switched injection (CSI) technique and a sub-sampling bang-bang phase detector (SSBBPD) is proposed. The operation of the CSI technique is demonstrated and the realignment factor of the injection is derived by charge transfer principle. With the linear model of the ILPLL, the phase noise transfer function of the injection-locked PLL is analyzed when dual-edge injection is achieved. From the analysis, the phase noises of the conventional PLL, single-edge ILPLL, and dual-edge ILPLL are compared each other. Additionally, the performance of the reference clock spurs is analyzed according to the injection timing and duty-cycle error. Finally, the implementation of the proposed ILPLL is explained with the detailed circuit diagram.

In Chapter 4, the measurement results are presented. The phase noise of the reference clock, free-running oscillator, ILPLL, and ADPLL are measured. Also, the reference clock spurs and integrated RMS jitter are measured over the duty-cycle of the reference clock and voltage variation.

Chapter 5 summaries the proposed works with the discussion of thesis contribution and concludes the thesis.

Chapter 2

Basic Injection-Locked Clock Multiplier

2.1 Injection-Locked Oscillator (ILO)

2.1.1 Introduction

Injection-locked oscillator has been studied since half a century ago [3]–[6]. When two clock systems are under operation on a shared medium, the oscillators in each system affect each other and could be pulled due to coupling through the substrate as shown in Fig. 2.1. An oscillator in the system or high swing data stream at the output of the transmitter can influence other side of the oscillator to be pulled since it contains considerable energy near their operation frequencies. By applying

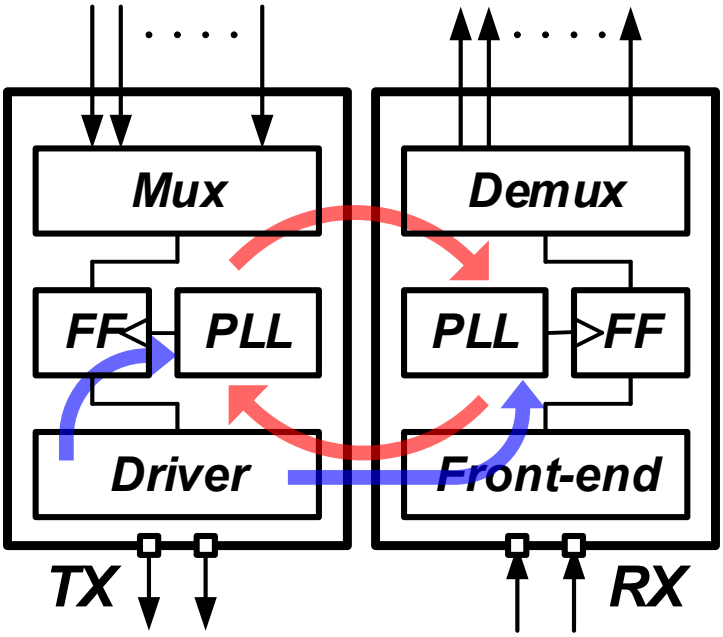


Fig. 2.1 Oscillator pulling in broadband clocking systems.

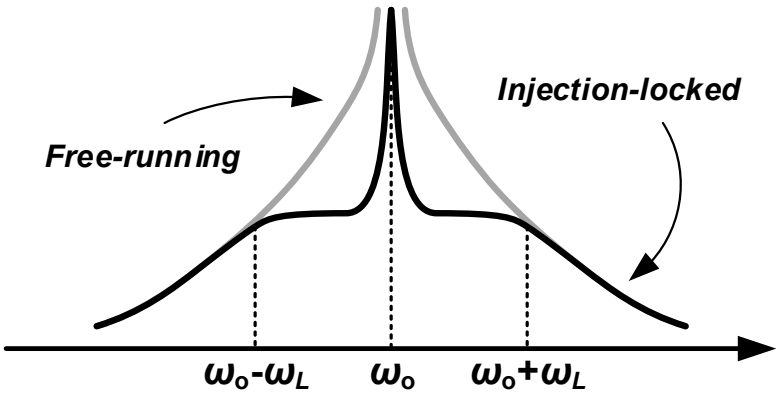


Fig. 2.2 Frequency domain of injection-locked oscillator.

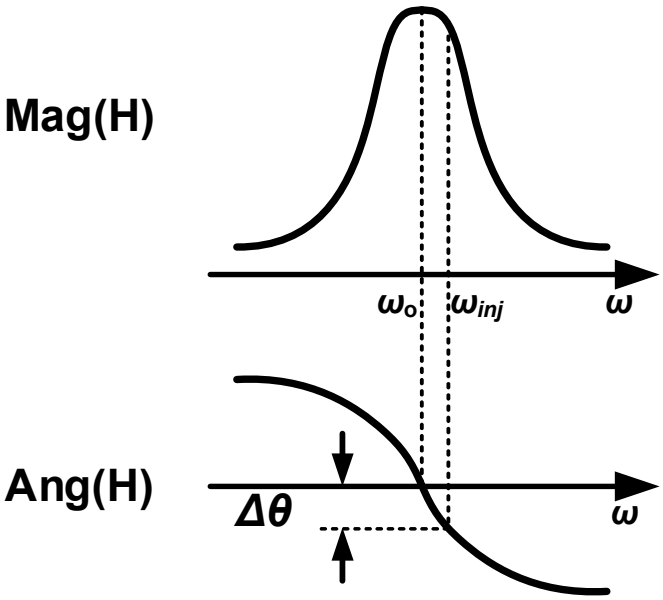
this phenomenon to the clock generation, a clean clock can be obtained by injecting a clock into a jittery oscillator as shown in Fig. 2.2. The phase noise of the clock is degraded toward the injection clock. To understand the injection phenomenon, consider a simple oscillator with resonance frequency of $\omega_o = 1/\sqrt{LC}$ having second-order bandpass filter as shown in Fig. 2.3(a). Considering the oscillator is under injection with additive input, the ILO can be modeled as shown in Fig. 2.3(b) [1]. When the ILO has a frequency near the resonance frequency, the phase shift occurs and it can be expressed as

$$\begin{aligned}\Delta\theta &= \frac{\pi}{2} - \tan^{-1}\left(\frac{1}{Q}\cdot\frac{{\omega_o}^2}{{\omega_o}^2 - \omega^2}\right)\\ &\approx \tan^{-1}\left(\frac{2Q}{\omega_o}(\omega_o - \omega)\right)\end{aligned} \tag{2.1}$$

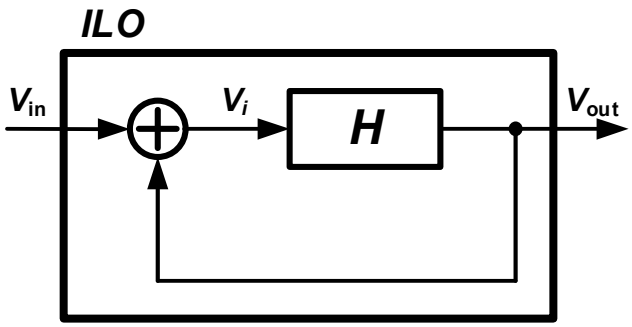
where Q is the Q-factor of the resonance unit. When the current flowing contains phase modulation in the resonant unit, the (2.1) can be expanded as

$$\Delta\theta \approx \tan^{-1}\left(\frac{2Q}{\omega_o}\left(\omega_o - \omega - \frac{d\varphi(t)}{dt}\right)\right) \tag{2.2}$$

where $\varphi(t)$ is term of instantaneous phase modulation. Regardless of the input and the output waveforms and considering only the injection frequency component in the fourier transform, the input and the output can be expressed with sinusoidal waveform as



(a)



(b)

Fig. 2.3 (a) Characteristic of oscillator and (b) modeling of the ILO.

$$V_{in} = V_{inj}\cos(\omega_{inj}t) \tag{2.3}$$

$$V_{out} = V_{osc}\cos(\omega_{inj}t + \Delta\theta) \tag{2.4}$$

where V_{inj} and V_{osc} are injection clock and resonant clock amplitude, respectively ($V_{inj} \ll V_{osc}$). Then, adder output is expressed as

$$\begin{aligned} V_i &= V_{inj}\cos(\omega_{inj}t) + V_{osc}\cos(\omega_{inj}t + \Delta\theta) \\ &\approx V_{osc}\cos(\omega_{inj}t + \varphi) \end{aligned} \tag{2.5}$$

where $\varphi = \tan^{-1}\left(\frac{V_{osc}\sin\Delta\theta}{V_{inj}+V_{osc}\cos\Delta\theta}\right)$. With the (2.2) and (2.4), the output voltage can be expressed as

$$\begin{aligned} V_{out} = V_{osc}\cos\Bigg(&\omega_{inj}t + \varphi \\ &+ \tan^{-1}\left(\frac{2Q}{\omega_o}\left(\omega_o - \omega_{inj} - \frac{d\varphi(t)}{dt}\right)\right)\Bigg) \end{aligned} \tag{2.6}$$

From the (2.4) and (2.6), the phase shift can be obtained as

$$\Delta\theta = \varphi + \tan^{-1}\left(\frac{2Q}{\omega_o}\left(\omega_o - \omega_{inj} - \frac{d\varphi(t)}{dt}\right)\right) \tag{2.7}$$

where

$$\frac{d\varphi(t)}{dt} = \frac{{V_{osc}}^2 + V_{inj}V_{osc}\cos\Delta\theta}{{V_{inj}}^2 + {V_{osc}}^2 + 2V_{inj}V_{osc}\cos\Delta\theta}\frac{d\Delta\theta}{dt} \approx \frac{d\Delta\theta}{dt} \tag{2.8}$$

From the tangent sum formula,

$$\begin{aligned}\tan(\Delta\theta - \varphi) &= \frac{\tan\Delta\theta - \tan\varphi}{1 + \tan\Delta\theta\tan\varphi} \\ &= \frac{V_{inj}\sin\Delta\theta}{V_{osc} + V_{inj}\cos\Delta\theta} \approx \frac{V_{inj}}{V_{osc}}\sin\Delta\theta\end{aligned} \tag{2.9}$$

According to (2.8) and (2.9),

$$\frac{d\Delta\theta}{dt} = \omega_o - \omega_{inj} - \frac{\omega_o}{2Q}\cdot\frac{V_{inj}}{V_{osc}}\sin\Delta\theta \tag{2.10}$$

When the ILO is locked, $d\Delta\theta/dt = 0$. On the other hand, if $d\Delta\theta/dt \neq 0$, the ILO is pulling continuously. Solving differential equation of (2.10), the expression of the phase shift for time is expressed as

$$\tan\left(\frac{\theta}{2}\right) = \frac{\omega_L}{\omega_o - \omega_{inj}} + \frac{\omega_q}{\omega_o - \omega_{inj}}\tan\left(\frac{\omega_q t}{2}\right) \tag{2.11}$$

where $\omega_q = \sqrt{\left(\omega_o - \omega_{inj}\right)^2 - {\omega_L}^2}$ and $\omega_L = \frac{\omega_o}{2Q}\cdot\frac{V_{inj}}{V_{osc}}$. As shown in Fig. 2.4, the phase of the oscillator clock is periodic with $2\pi/\omega_q$. It means that the frequency changes instantaneously periodically. In the next section, the time domain analysis

with the phase domain response (PDR) is examined in detail.

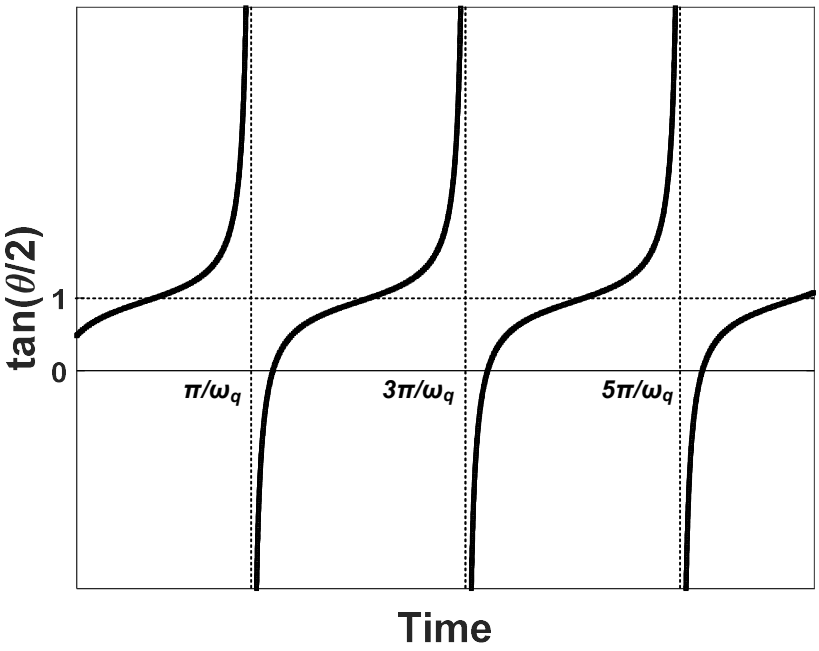


Fig. 2.4 Phase drift when the ILO is unlocked.

2.1.2 Phase Domain Response (PDR) Analysis

To investigate the injection effect in the time domain, a PDR analysis can be considered. Assuming that the injection pulse is dirac-delta function, the oscillator clock is pushing or pulling according to the injection timing as shown in Fig. 2.5. The PDR is obtained by the ratio of output phase shift to the input phase deviation as shown in Fig. 2.6. From the PDR, lock-in range of the injection with the division ratio *N* can be derived. Assume that the oscillator is under injection locked as shown in Fig. 2.7, the phase of the oscillator is reset every injection cycle T_{inj} and it is expressed as

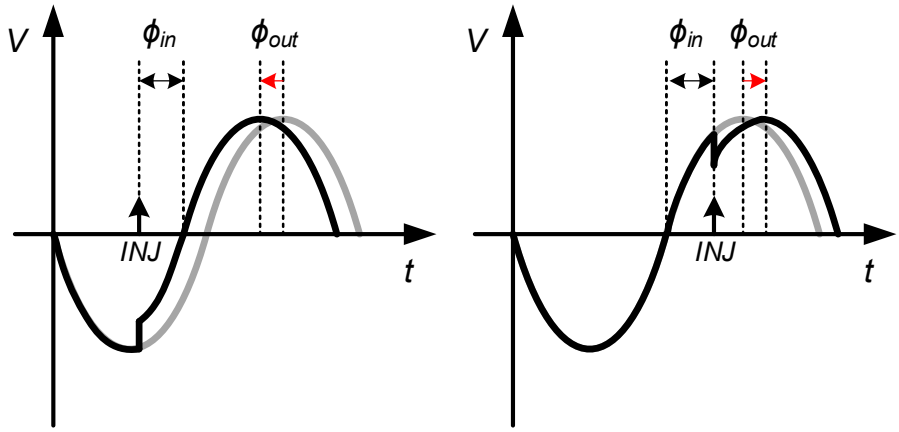
$$T_{inj} = N \cdot T_{osc} + \Delta T_{out}. \tag{2.12}$$

where T_{osc} is a oscillator period and ΔT_{out} $\left(= \frac{\phi_{out}}{2\pi} \cdot T_{osc}\right)$ is the amount of phase shifted. Then, the average frequency of the injection-locked oscillator is

$$f_o = \frac{N}{T_{inj}} = \frac{N}{N \cdot T_{osc} + \Delta T_{out}}. \tag{2.13}$$

From the (2.13), minimum and maximum locked frequency can be derived at $\Delta T_{out,min} = \frac{\phi_{out,min}}{2\pi} \cdot T_{osc}$ and $\Delta T_{out,max} = \frac{\phi_{out,max}}{2\pi} \cdot T_{osc}$, respectively and the lock-in range can be expressed as

$$f_L = \frac{f_{inj} \cdot \left(\phi_{out,max} - \phi_{out,min}\right)}{2\pi} \tag{2.14}$$



(a) (b)

Fig. 2.5 Time domain waveform when injection clock is (a) leading and (b) lagging.

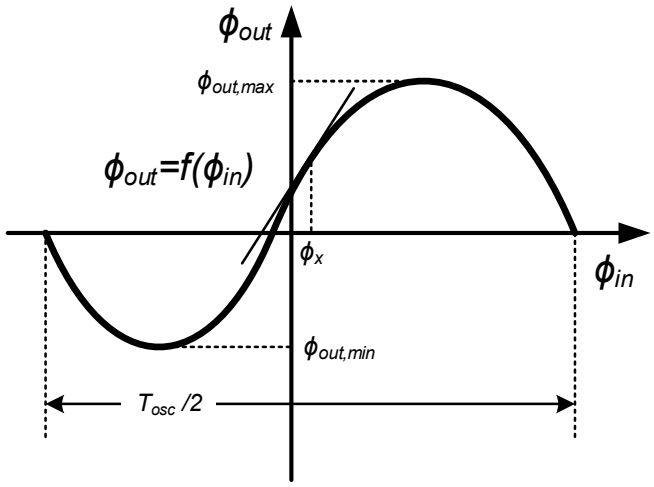
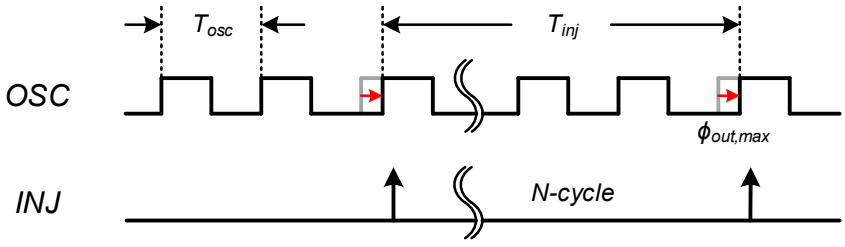
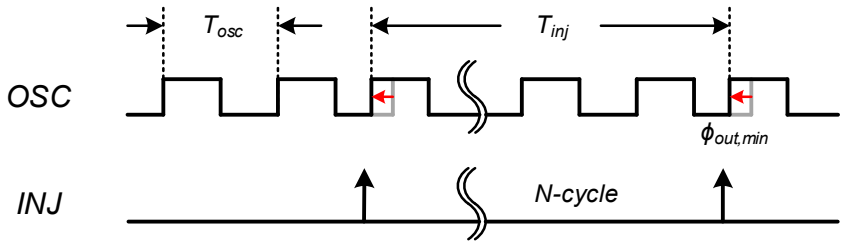


Fig. 2.6 Phase domain response (PDR).



(a)



(b)

Fig. 2.7 Time domain waveform when oscillator is under injection locked when injection is (a) lagging and (b) leading.

where f_{inj} is injection frequency. From the (2.14), lock-in range becomes narrow as the multiplication factor increase.

In practice, the injection pulse has a finite width rather than a dirac-delta function. Conventionally, an NMOS is located between differential nodes of the oscillator outputs as shown in Fig. 2.8 [7]. When a pulse is injected through the MOSFET, current flows between the differential nodes and the phase shift occur. [8] has presented the injection strength according to the pulse width. In terms of mixing the oscillator clock with the injection clock, injection pulse width D is one of the

important factors determining the realignment factor. When injection frequency f_{inj} is injected to the oscillator with $N \cdot f_{inj}$ frequency, where N is the division ratio, the harmonic of the 2Nth injection frequency produced the output of $N \cdot f_{inj}$ due to the mixing property. Therefore, the pulse width could be derived when 2Nth harmonic power is maximized. With the Fourier series, the injection clock with the pulse width D is expressed as

$$V(\mathrm{t}) = a_0 + \sum_{k=-\infty}^{\infty} \left(a_k \cos\left(2\pi k f_{inj} t\right) + b_k \sin\left(2\pi k f_{inj} t\right)\right). \tag{2.15}$$

The coefficients of harmonics are expressed as

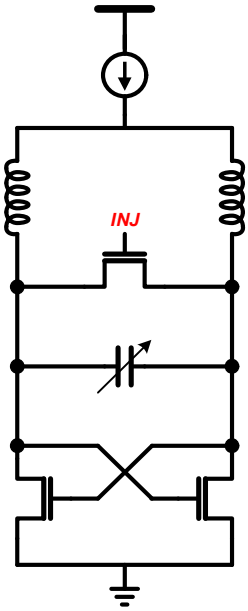
$$a_0 = A \cdot f_{inj} \cdot D \tag{2.16}$$

$$a_n = \frac{A \sin\left(2\pi n f_{inj} D\right)}{2\pi n} \tag{2.17}$$

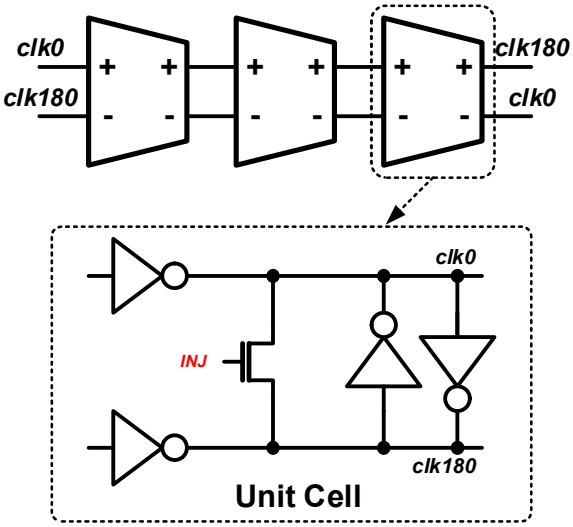
$$b_n = \frac{-A \cos\left(2\pi n f_{inj} D\right) + A}{2\pi n}. \tag{2.18}$$

where A is the amplitude of the injection clock. Therefore, the power of the 2Nth harmonic is derived as

$$P_{2N}{}^2 = a_{2N}{}^2 + b_{2N}{}^2 = \left(\frac{A \sin\left(2\pi N f_{inj} D\right)}{2N\pi}\right)^2. \tag{2.19}$$



(a)



(b)

Fig. 2.8 Conventional injection scheme in (a) LC oscillator and (b) inverter-based ring oscillator.

To maximize the 2*N*th harmonic power, the pulse width *D* is determined as

$$D = \frac{T_{osc}}{4} \quad or \quad \frac{3T_{osc}}{4} \tag{2.20}$$

where T_{osc} is the intrinsic frequency of the oscillator. From the results, to maximize the injection strength with pulse injection, the operation bandwidth of the ILO is limited not by the oscillator clock frequency, but by the pulse generator data rate.

As studied in [9], the injection pulse width is relationship with the asymmetric nature of the PDR, which appears as a delayed injection effect phenomenon. During the injection pulse enabled, the switch between differential nodes turns on and voltage across the capacitor is changed as shown in Fig. 2.9. Assuming the switch resistance R_{sw} is sufficiently smaller than resonance unit loss, the voltage change across the capacitor depends on the time constant of $R_{sw}\mathrm{C}$. Dividing pulse width into *K* small pulses having pulse width of *D*/*K*, the total change in capacitor voltage can be derived. The voltage change by the kth pulse can be expressed as

$$\Delta v_k = V_{c,k}\left(1 - e^{-\frac{D/K}{R_{sw}\mathrm{C}}}\right) \approx V_{c,k}\frac{D/K}{R_{sw}\mathrm{C}} \tag{2.21}$$

where $V_{c,k}$ is the capacitor voltage at the *k*th pulse. Assuming that the capacitor voltage is expressed as $V_c(t) = \sin(\omega_o t + \phi_{in})$ and the center of the injection is located at ϕ_{in}, $V_{c,k}$ can be expressed as

$$V_{c,k} = e^{-\frac{kD/K}{R_{sw}\mathrm{C}}} \sin(\phi_{in} + 0.5\omega_o D - \omega_o kD/K) \tag{2.22}$$

Then, total change of the capacitor voltage from the injection is expressed as

$$\begin{aligned} &\sum_k \Delta v_k \cos\left(\frac{\omega_o kD}{K}\right) \\ &= e^{-\frac{kD/K}{R_{sw}\mathrm{C}}} \sin(\phi_{in} + 0.5\omega_o D - \omega_o kD/K) \cos(\omega_o kD/K) \frac{D/K}{R_{sw}\mathrm{C}} \end{aligned} \tag{2.23}$$

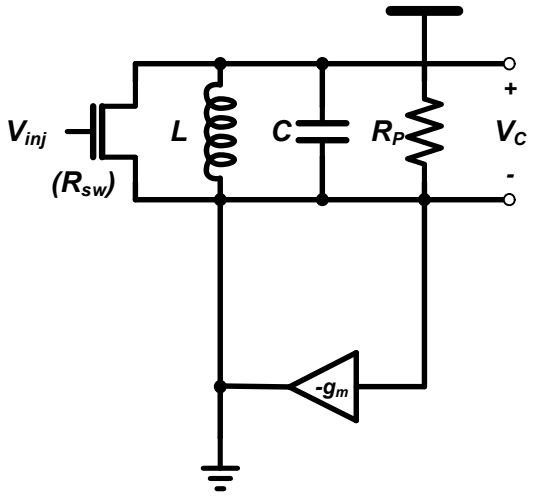
With infinite number of pulse divides, the (2.23) can be transformed into integration as

$$\begin{aligned} V_{c,total} &= \int_0^D e^{-\frac{x}{R_{sw}\mathrm{C}}} \sin(\phi_{in} + 0.5\omega_o D - \omega_o x) \cos(\omega_o x)\, dx \\ &= \frac{1}{2}\sin(\phi_{in} + 0.5\omega_o D)\left(1 - e^{-\frac{D}{R_{sw}\mathrm{C}}}\right) - \frac{1}{2 + 8(\omega_o R_{sw}\mathrm{C})^2} \\ &\times \begin{bmatrix} 2\omega_o R_{sw}\mathrm{C}\cos(\phi_{in} + 0.5\omega_o D) - \sin(\phi_{in} + 0.5\omega_o D) \\ -e^{-\frac{D}{R_{sw}\mathrm{C}}}(\phi_{in} - 1.5\omega_o D) - \sin(\phi_{in} - 1.5\omega_o D) \end{bmatrix} \end{aligned} \tag{2.24}$$

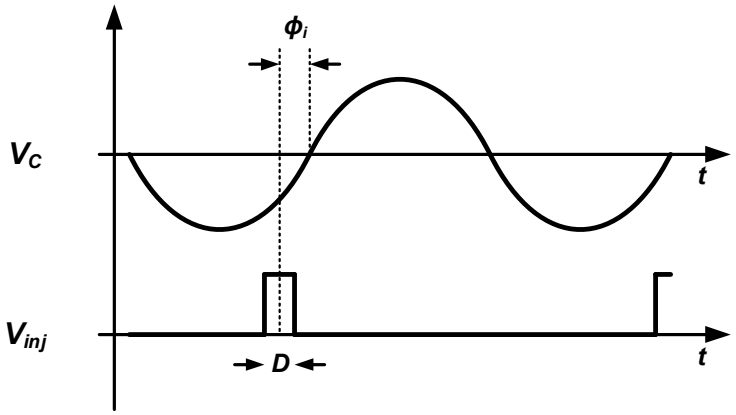
Finally, the output phase shift can be derived with the (2.24) as

$$\phi_{out} = \phi_{in} - \tan^{-1}\big(\tan(\phi_{in}) - V_{c,total}\sec(\phi_{in})\big) \tag{2.25}$$

As shown in Fig. 2.10, the output phase shift is asymmetric as increasing the pulse width.



(a)



(b)

Fig. 2.9 (a) Simplified LC oscillator circuit and (b) time waveform of the capacitor and injection voltage.

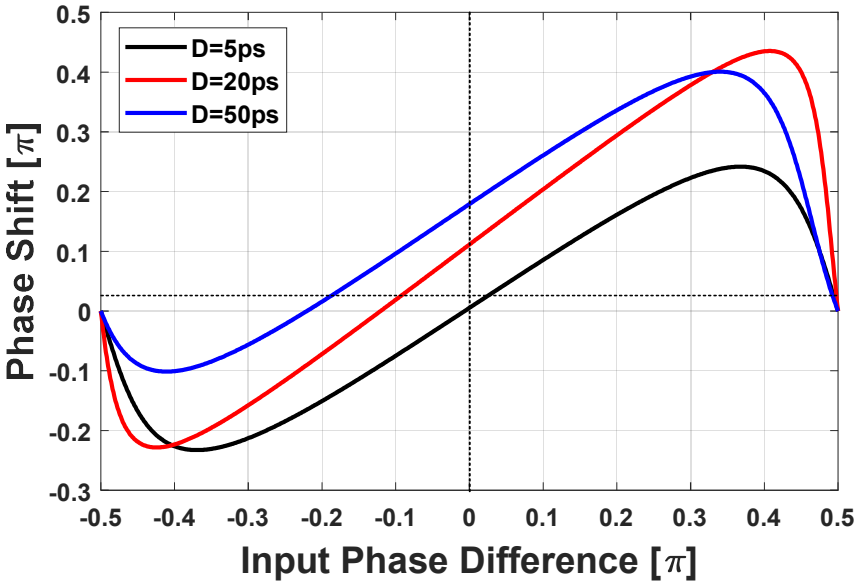


Fig. 2.10 Simulation results of the PDR according to the pulse width.

2.1.3 Noise Filtering Bandwidth

Noise filtering bandwidth by the injection is determined by the slope of the PDR. When the oscillator is injection locked at $\phi_{in} = \phi_x$ with small phase change, the realignment factor can be expressed as

$$\beta = \left.\frac{d\phi_{out}}{d\phi_{in}}\right|_{\phi_{in}=\phi_x}. \tag{2.26}$$

According to the realignment factor, the transfer function of the oscillator noise is simulated by behavior model in [6] as shown in Fig. 2.11 and Fig. 2.12. The oscillator noise filtering bandwidth of the injection is proportional to the realignment factor. In the Table 1, the normalized bandwidth in relationship with the injection clock frequency is organized according to the realignment factor. It is noticed that the realignment factor higher than 0.5 has a wider bandwidth compared to the conventional PLL.

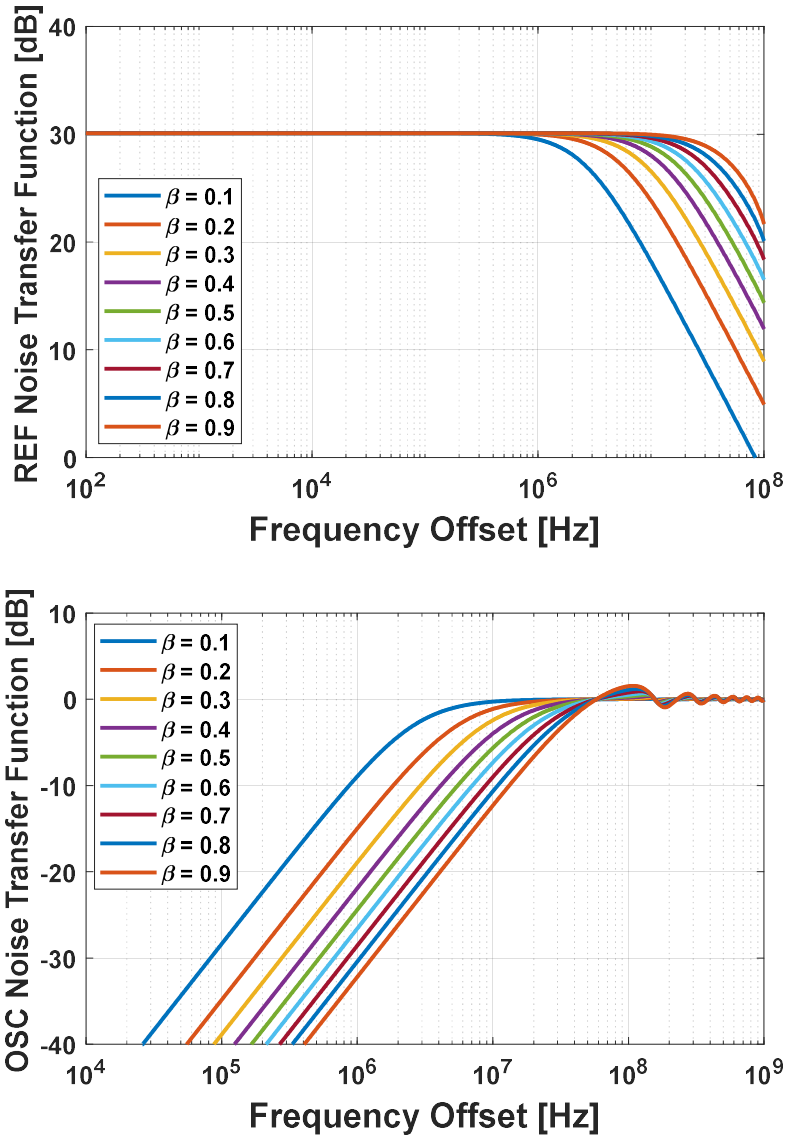


Fig. 2.11 Transfer function of the input noise and oscillator noise with injection locking according to the realignment factor.

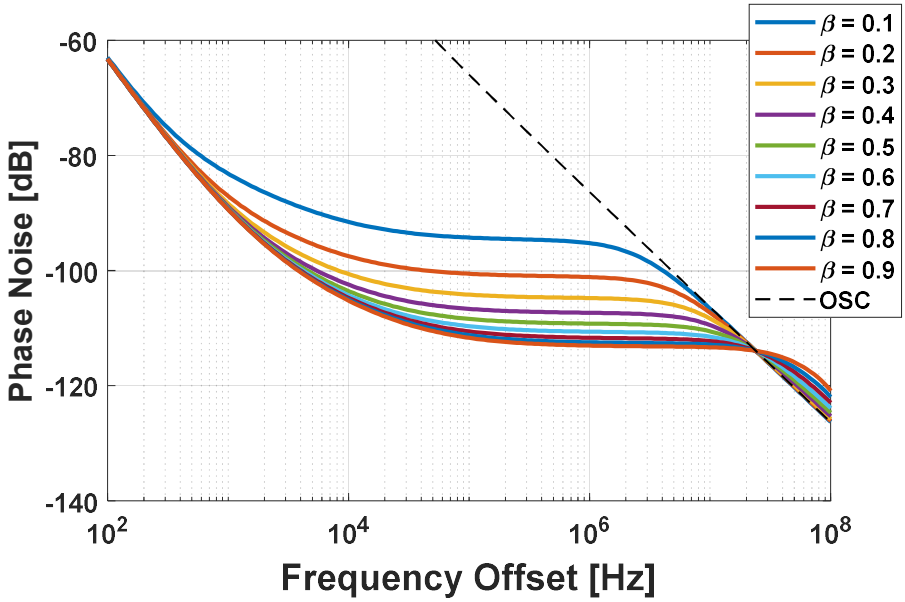


Fig. 2.12 Phase noise of the ILO according to the realignment factor.

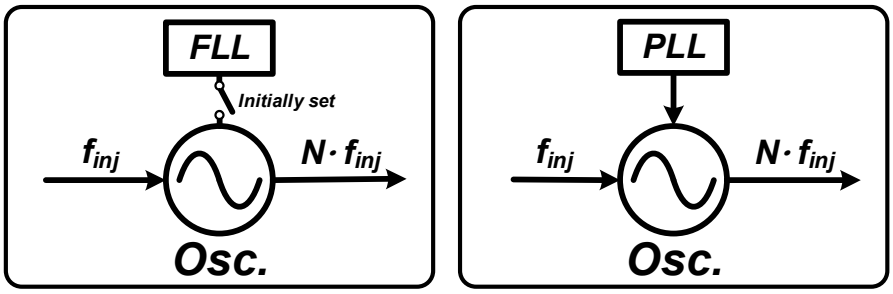
Table 1. Normalized noise filtering bandwidth of the oscillator.

β	Bandwidth / f_{inj}
0.1	0.017
0.2	0.035
0.3	0.056
0.4	0.078
0.5	0.102
0.6	0.129
0.7	0.157
0.8	0.186
0.9	0.214

2.2 Injection-Locked Clock Multiplier

2.2.1 Overview

Recently, subharmonic injection locking is widely used to implement a clock multiplier and there have been several approaches as discussed in [19]. The main challenge of the ILCM is to keep the free-running frequency of the oscillator near the target frequency across the PVT variations. Fig. 2.13(a) shows a clock multiplier whose frequency is initially set to integer times of the injection clock frequency by a frequency-locked loop (FLL) [10], [11]. The phase noise of the clock multiplier inside the lock-in range f_L is significantly decreased and determined mainly by the phase noise of the injection clock. However, such implementations are difficult to apply in practice because the free-running frequency drifts with voltage and temperature variations. Further, although the oscillator is perfectly tuned with the *N*th harmonic injection frequency, injection alone cannot suppress the phase noise sufficiently in the low-frequency region, where flicker noise dominates the noise level. This is because an injection-locked oscillator is basically a first-order low-pass filter in terms of phase noise [6], whereas the attenuation slope of the phase noise in the region below the flicker noise corner frequency f_C is higher than -20 dB/decade. As shown in Fig. 2.13(b), injection locking with a frequency-tracking loop (e.g., PLL with injection) can be a solution for this purpose [6], [8], [12], [14]. Fig. 2.14 illustrates a comparison of the phase noise between the injection alone and a PLL with injection. When the oscillator has a higher f_C, the phase noise below f_C



(a) (b)

Fig. 2.13 Clock multiplier using (a) injection only and (b) PLL with injection.

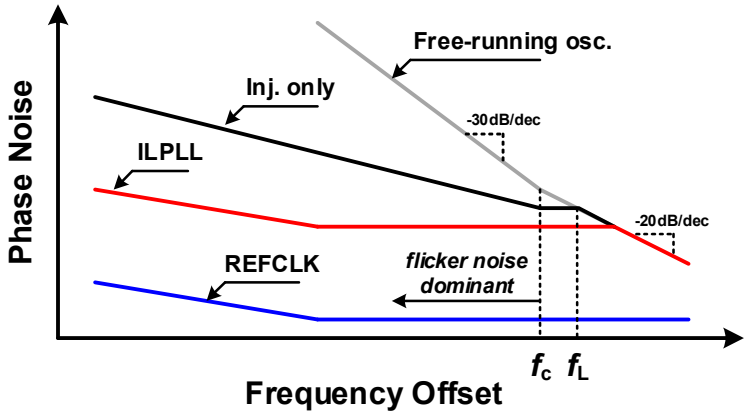
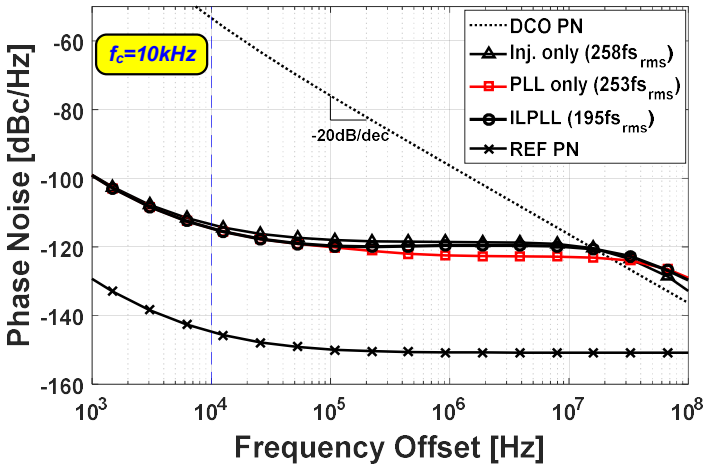


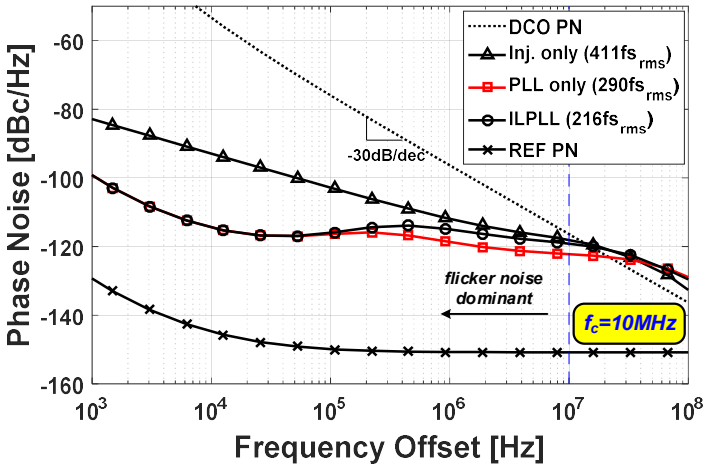
Fig. 2.14 Illustrated phase noise comparison between injection only and PLL with injection.

decreases significantly by combining the injection and PLL. Therefore, designer can choose whether or not to adopt additional loop depending on the performance of the oscillator and limitation of power dissipation.

To quantitatively investigate the effect of injection, the phase noise characteristic of the ILCM in relation with the flicker noise corner frequency f_C of the oscillator is analyzed. The phase noise transfer function of an injection-locked ADPLL is approximated as a linear model in [6] and the phase noise of the oscillator is based on Leeson's model in [38]. Fig. 2.15(a) shows the phase noise comparisons between injection only, PLL only, and ILPLL when the oscillator has a f_C of 10 kHz. The phase noise with the injection alone scheme is comparable to that of the PLL alone and the ILPLL. The PLL loop marginally improves the phase noise performance as the improvement of the integrate RMS jitter from 1 kHz to 40 MHz is 63 fs. Therefore, considering extra power dissipation and area, the additional PLL loop may not be desired or it would be sufficient to employ a low bandwidth frequency-tracking loop in order to desensitize against PVT variations. On the other hand, when the oscillator has a higher f_C of 10 MHz as shown in Fig. 2.15(b), the injection alone cannot cut down the phase noise sufficiently due to the first-order attenuation. Therefore, the additional PLL loop must be employed to suppress the phase noise below f_C as the integrated RMS jitter of the ILPLL decreases by about half in comparison with that of the injection alone. It is noteworthy that f_C of the ring oscillator becomes higher as CMOS technology scales down. Recently, there have been several efforts to employ continuously frequency-tracking loop (FTL) in the PLL-based ILCM, the replica-based ILCM and the real-time FTL-based ILCM. The details of each structure are introduced as follows.



(a)



(b)

Fig. 2.15 Simulated phase noise of free-running DCO, reference clock, injection only, PLL only, and PLL with injection when (a) f_C = 10 kHz and (b) f_C = 10 MHz. (f_{out} = 5 GHz, f_{ref} = 156.25 MHz and β = 0.6).

2.2.2 Prior Arts

2.2.2.1 PLL-based ILCM

In the PLL-based ILCM as shown in Fig. 2.16, the main challenge is to eliminate a timing conflict between the PLL loop and the injection path. This is because the injection path contains pulse generator and the PLL feedback path has a divider, which are delay elements. With the timing mismatch between PLL and injection paths, the frequency error of the oscillator cannot be detected, since the injection periodically reset the phase of the oscillator before the phase detection by the PLL path. Even though manually adjusting the delay line in the injection path, the voltage and temperature variations result in path mismatch from the delay line again and the frequency error occurs as shown in Fig. 2.17. To solve the timing issue, prior architectures [12]–[14] used an injection timing calibration circuit using delay line. However, the additional loop operates in the background, which complicates the structure and entails additional power consumption.

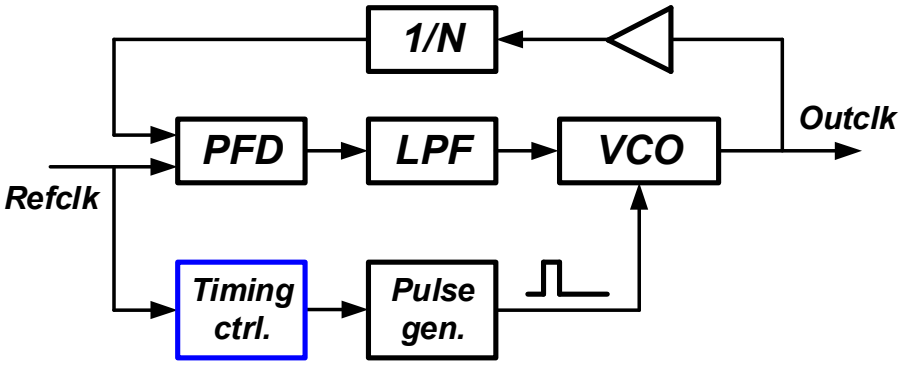


Fig. 2.16 Conventional PLL-based ILCM.

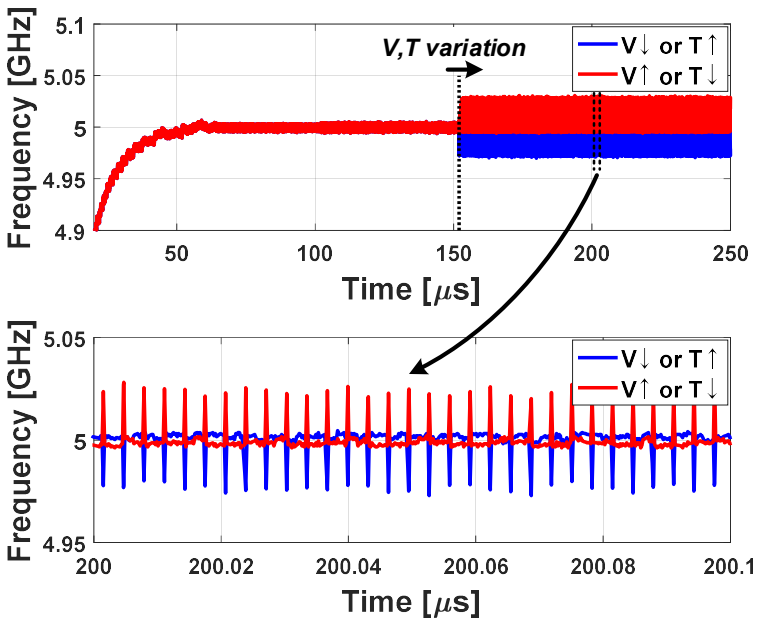


Fig. 2.17 Simulation results of PLL-based ILCM when voltage and temperature variations occur.

2.2.2.2 Replica-based ILCM

To solve the race condition, several ILCMs use a replica oscillator [25]–[27] that separates the PLL loop from the injection clock, thereby eliminating interference between two loops. Fig. 2.18 shows an ILCM using replica oscillator whose frequency is adjusted by the same control source. The main oscillator is only injection-locked within the lock-in range and the replica oscillator is for keeping target control voltage of the VCO by the PLL loop. Therefore, the race condition is solved by separating the PLL loop and the injection path. However, the frequency mismatch between the main and replica oscillator can occur, thereby requiring mismatch calibration loop. In this architecture, the ILCM starts with the initial calibration of the oscillators. Because the architecture uses replica oscillator and calibration loop, this leads to considerable amount of power dissipation and area.

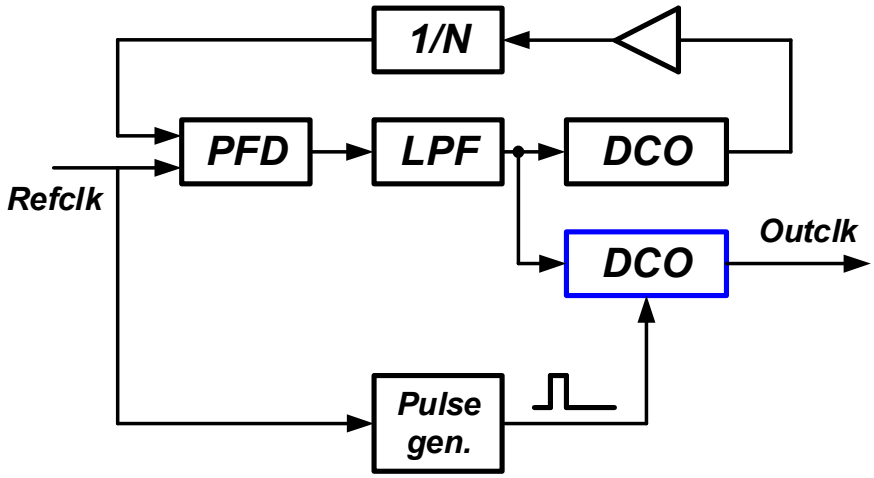


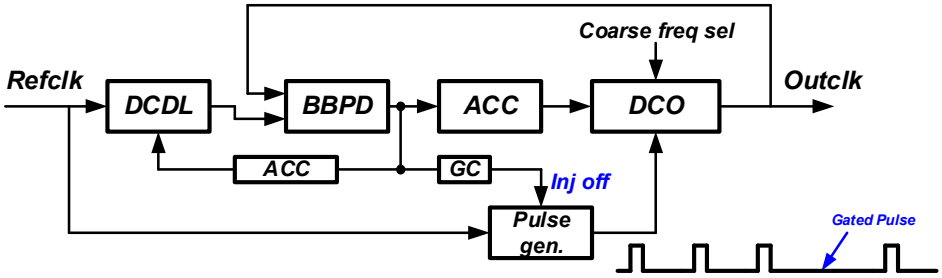
Fig. 2.18 Replica-based ILCM.

2.2.2.3 Real-Time FTL-based ILCM

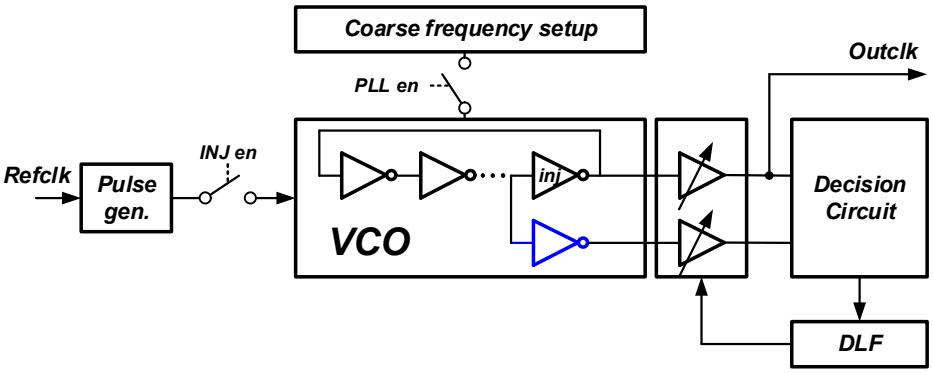
Recently, real-time FTL-based ILCM using phase detector has been developed to overcome the issues which the PLL-based ILCM and the replica-based ILCM have.

Fig. 2.19(a) shows an example of the FTL-based ILCM [28], [29]. In this design, frequency error can be detected by sacrificing the injection pulse every 2~8 cycle of injection frequency. It has an advantage of the adjusting the frequency by detecting the frequency drifts of the oscillator. However, part of the injection effect is sacrificed for detecting the frequency drift.

Another example is shown in Fig. 2.19(b) [30]–[32]. With a replica cell in the ring oscillator, the path delay difference between the injection cell and replica cell is relationship with the frequency error. Therefore, calibration of the injection path delay can nullify the frequency error with achieving low spur performance. However, when large voltage and temperature variations are encountered, limitation of the frequency capture range can lead to deviating from the target frequency.



(a)



(b)

Fig. 2.19 Real-time FTL-based ILCM using (a) pulse gating scheme and (b) replica delay cell.

2.3 Concept of the Proposed ILCM

The common features of the prior arts is utilizing a pulse generator and additional injection timing calibration circuitry. Hence, the pulse generator limits the ILCM clock frequency and the architecture becomes complex due to the calibration loop. Fig. 2.20 shows the concept of the proposed ILCM which is based on PLL-based ILCM. Without the pulse generator, injection is achieved with zero delay and it does not affected by pulse width. Therefore, the bandwidth limit of the ILCM is no longer limited by the pulse generator. Also, eliminating the divider in the PLL feedback path makes the PLL feedback path latency zero owing to the sub-sampling technique. With combining the proposed injection and sub-sampling techniques, the proposed ILCM does not require the injection timing calibration loop, thereby simplifying the overall structure. In later sections, the building blocks will be explained in detail and the analysis methods and noise effects will be investigated.

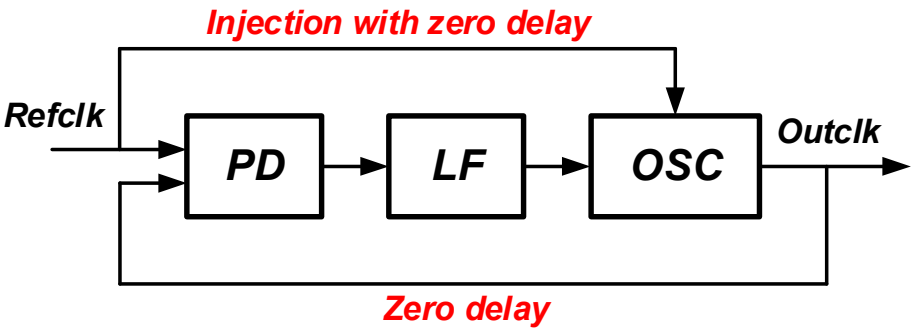


Fig. 2.20 Concept of the proposed ILCM.

Chapter 3

Design of Subharmonically ILPLL

3.1 Overview

In this chapter, an ILPLL with the dual-edge CSI and sub-sampling techniques without injection timing calibration circuits is proposed. The ILPLL achieves ultra-low jitter performance even with a large multiplication factor of 32. This chapter describes the design of the proposed ILPLL with analysis, which was presented in [19].

3.2 Proposed Architecture

3.2.1 Overall Architecture

The overall architecture of the proposed ILPLL is shown in Fig. 3.1. It employs the CSI and sub-sampling techniques to overcome the injection timing issues. In this architecture, the main PLL loop, which is the sub-sampling PLL, contributes to the suppression of the phase noise of the region under the flicker noise corner frequency as discussed before, and the reference clock injection widens the PLL bandwidth.

The front-end of the reference clock consists of a DCC and single-to-differential converter. The DCC is employed to minimize the F_{REF} and $2F_{REF}$ spur because the injection occurs at the dual-edge clock. From the output of the DCC, the differential injection clock is generated by the single-to-differential converter, which is not only injected into the DCO but also triggers the SSBBPD without a buffer circuit. The SSBBPD samples the DCO clocks before the level shifter, thus the PLL loop and injection path can have the same phase alignment time. In case of the input offset voltage of the SSBBPD, the offset timing of the PLL feedback path can be adjusted by the offset control code. Further, the direct proportional path from the SSBBPD to the DCO is adopted to minimize the loop latency [40]. During the operation of the ILPLL, the FLL works continuously in the background to prevent it from harmonic lock due to voltage and temperature drifts. Also, it supports a wide range of output frequency by controlling the frequency code word (FCW).

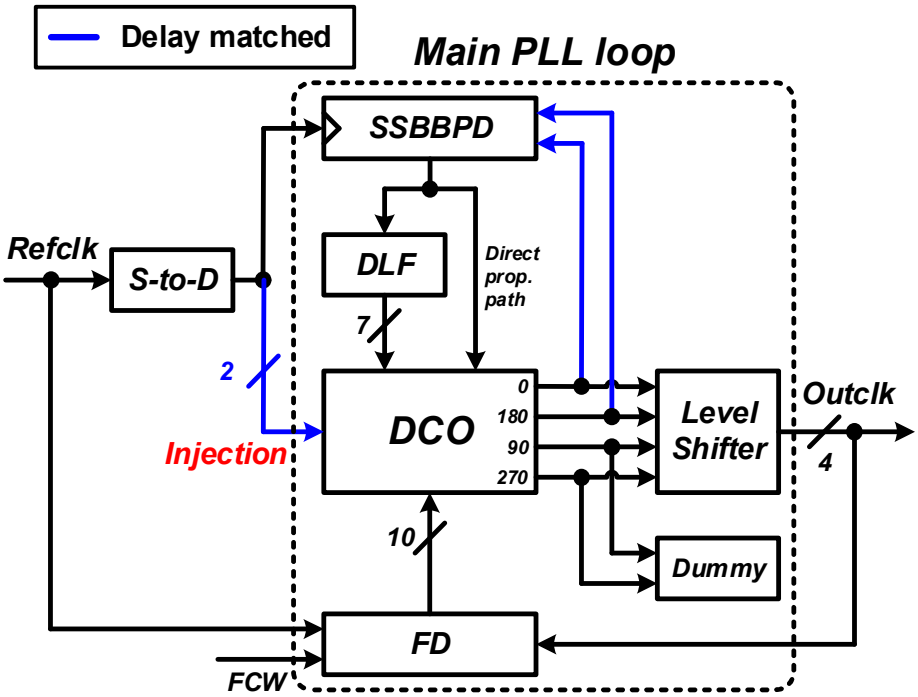


Fig. 3.1 Overall architecture of proposed ILPLL.

3.2.2 Dual-Edge Complementary Switched Injection

In order to inject a reference clock into the oscillator, a pulse generator is widely used to create a narrow pulse [6]–[9]. However, as the frequency of the oscillator increases, it becomes more difficult to generate a short injection pulse. In this work, a CSI technique is incorporated to accomplish the effect of short injection pulse and zero delay injection [17]–[19]. The DCO cell contains two pairs of series-transmission-gate switches between the differential clock nodes. The differential injection clocks operate the switches complementarily and the two pairs of the complementary switches maintain a constant capacitance on the DCO clock nodes. When one switch is off and the other is on, no direct current flows between the differential clock nodes and thus no effect is incurred on the DCO clock phase. On the other hand, when the switch states are swapped, a charge is injected into or drawn from the differential clock nodes. Further, during the transition of the switching operation, i.e., close to the crossing points of the differential injection clocks, direct short-circuit current flows on between the DCO differential clock nodes. As a result, phase shift occurs on the DCO clock. The simulation results of the free-running clock with the injection are shown in Fig. 3.3. When the injection clock is perfectly harmonic of the frequency of the free-running oscillator, the oscillator clock edge is locked with the injection clock edge. On the other hand, when the injection clock is deviated from the harmonic of the frequency of the free-running oscillator, the injection clock edge grows distant with the oscillator clock edge.

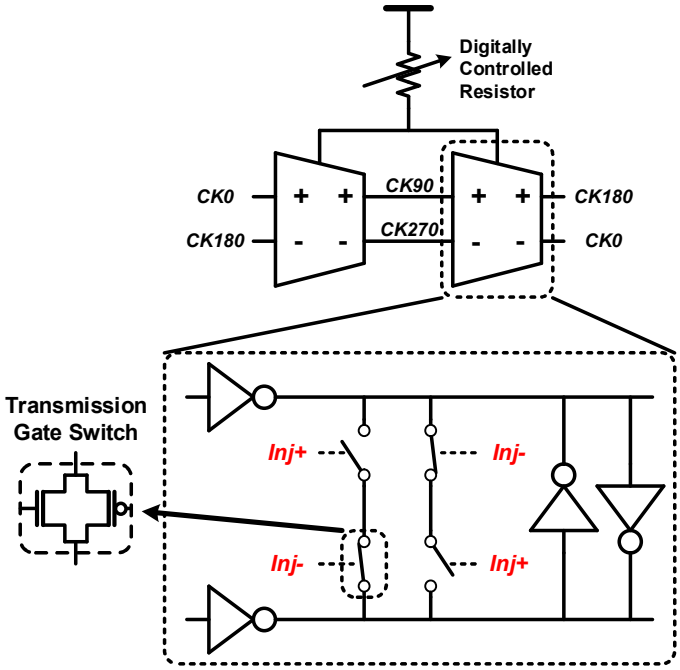


Fig. 3.2 Proposed injection-locked oscillator with CSI technique.

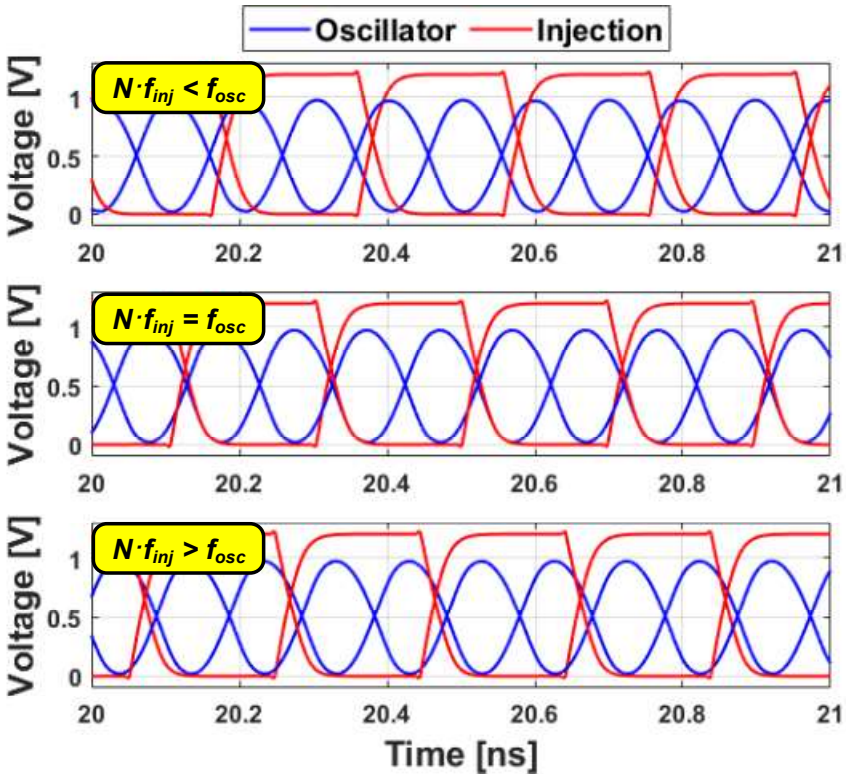


Fig. 3.3 Simulation results of the CSI technique with multiplication factor of two

In the circuit model of the complementary switched injection shown in Fig. 3.4, the load capacitance C_L of the DCO clock node and parasitic capacitance C_{par} representing the drain junction and gate-drain capacitance of the switches are included. During injection, there are two mechanisms of current flow between the differential nodes as mentioned above. One is the charge transfer caused by the switched capacitor operation due to the parasitic capacitance and the other is short-

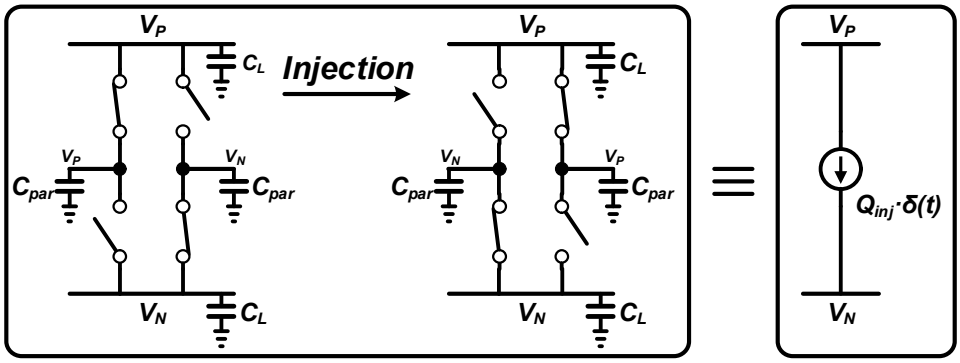


Fig. 3.4 Simplified model of switched capacitor injection.

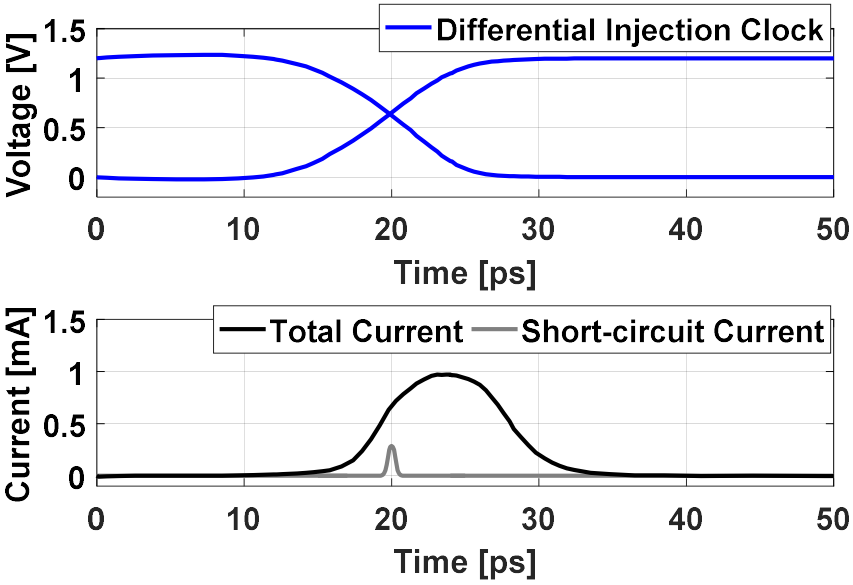


Fig. 3.5 Simulation result of current between differential nodes during injection.

circuit current across the switches partially on during the rise/fall overlap time of the injection clock. The simulation results in Fig. 3.5 indicate that the short-circuit current is negligible in comparison with the current from the switched capacitor operation. This is because the series-connected switches are simultaneously turned on weakly and only briefly during the transition time, whereas they are fully turned on and off for the switched capacitor operation. Assuming that the transition time of the injection clock is short, the amount of charge transfer on the *dcoclk0* and *dcoclk180* nodes after injection can be expressed as

$$Q_{inj} = C_{par} \cdot |V_P - V_N| \tag{3.1}$$

where V_P and V_N are node voltages of the *dcoclk0* and *dcoclk180* at the injection time. Then, the voltage variation of the *dcoclk0* and *dcoclk180* nodes due to the injection can be expressed as

$$\Delta V = |V_P - V_N| \cdot C_{par}/(C_{par} + C_L). \tag{3.2}$$

Consequently, under the approximation of linearity near the crossing points of the differential DCO clock as shown in Fig. 3.6, the realignment factor can be represented as

$$\beta = 2C_{par}/(C_{par} + C_L). \tag{3.3}$$

Fig. 3.7(a) and (b) illustrate the PDR and realignment factor, respectively, when switch size and injection transition time are varied. It indicates that the realignment

factor increases with an increased injection switch size. This is because the parasitic capacitance C_{par} has a linear relationship with the switch size. On the other hand, a longer transition time weakens the realignment factor because the clock edges move faster while the injection switches are in the transition region. Consequently, a longer transition time leads to more severe asymmetry in the PDR, which implies that pulling the phase of the oscillator is easier than pushing. The output frequency has only little effect on the realignment factor of the injection and the shape of the PDRs as shown in Fig. 3.8.

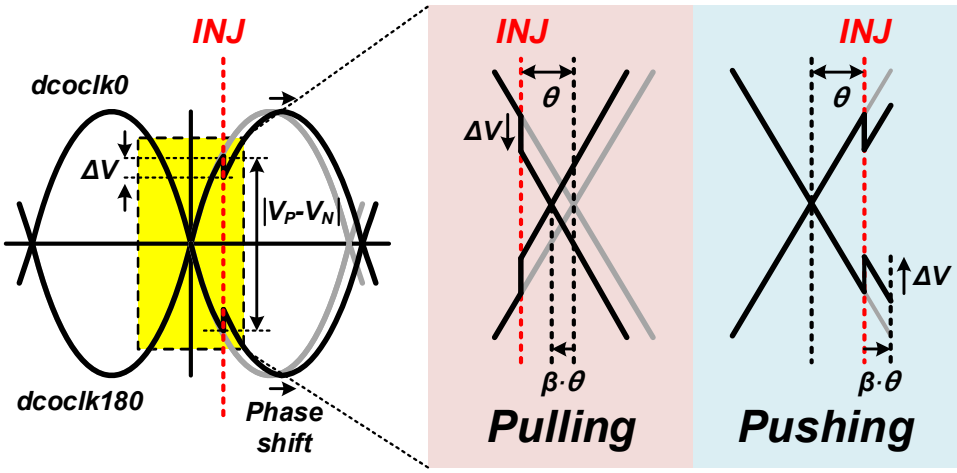
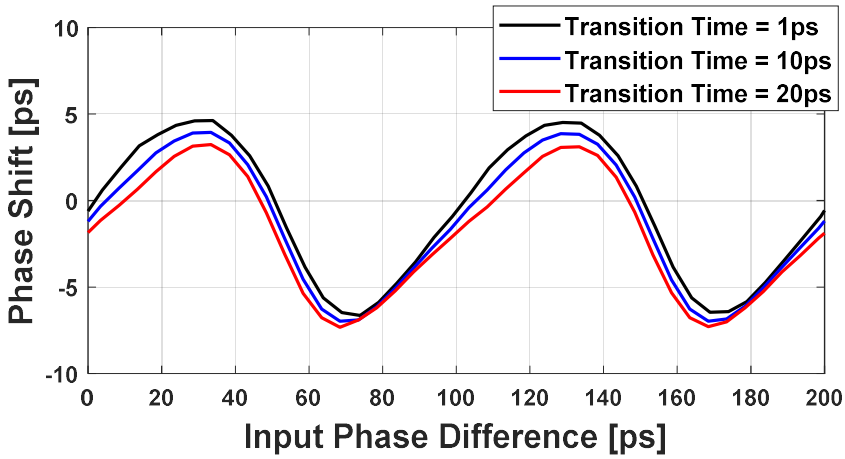
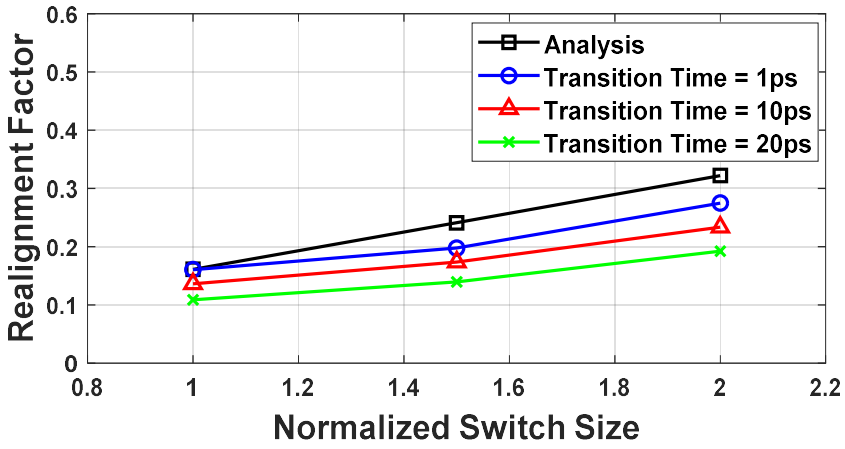


Fig. 3.6 Simplified injection effect on time-domain waveform.



(a)



(b)

Fig. 3.7 Simulation results of (a) phase domain response (PDR) and (b) realignment factor according to injection transition time and switch size.

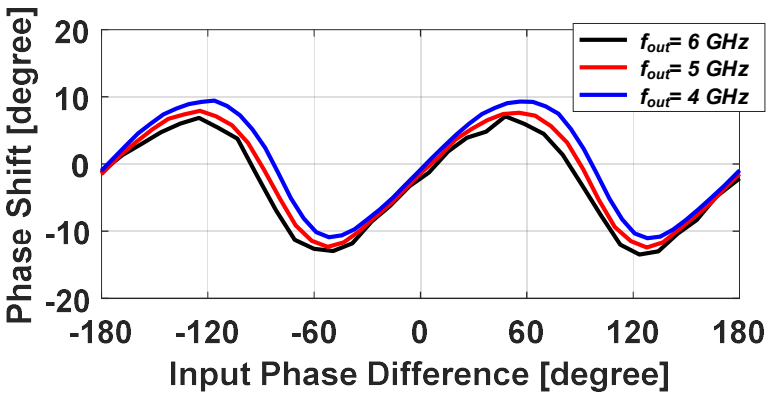


Fig. 3.8 Simulation results of PDRs according to the output frequency.

3.3 Analysis of the Injection-Locked PLL

3.3.1 Noise Analysis

The linear model of an all-digital sub-sampling ILPLL is shown in Fig. 3.9, where ϕ_{ref} and ϕ_{dco} are the reference clock phase noise and oscillator phase noise, respectively. K_{pd} and K_{dco} are phase detector and DCO gains, respectively. In addition to the conventional PLL noise model, $H_{rl}(j\omega)$ and $H_{up}(j\omega)$ are added as studied in [6] and they represent effect of the phase realignment and up-conversion of the reference noise to the DCO output, respectively. They can be expressed as

$$H_{rl}(j\omega) = 1 - \frac{\beta}{1 + (\beta - 1)e^{-j\omega T_{inj}}} e^{-j\omega \frac{T_{inj}}{2}} Sinc\left(\frac{\omega T_{inj}}{2}\right) \tag{3.4}$$

$$H_{up}(j\omega) = \frac{N_{inj} \cdot \beta}{1 + (\beta - 1)e^{-j\omega T_{inj}}} e^{-j\omega \frac{T_{inj}}{2}} Sinc\left(\frac{\omega T_{inj}}{2}\right) \tag{3.5}$$

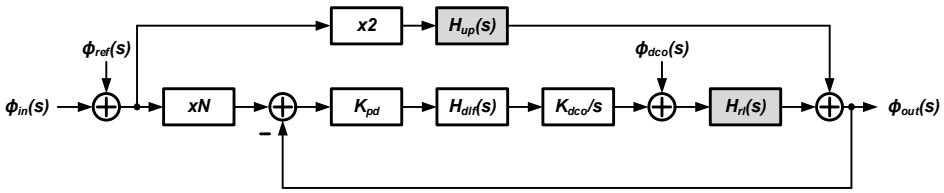


Fig. 3.9 Linear model of the ILPLL.

where T_{inj} is the injection clock period and N_{inj} is the division ratio of the injection clock and oscillator clock. Because of the dual-edge injection, $T_{inj} = T_{ref}/2$, $N_{inj} = N/2$, and frequency double factor is multiplied before up-conversion transfer function. The frequency multiplier *N* is added to the reference clock path virtually because there is no divide-by-*N* in the feedback path. The transfer function of the digital loop filter is expressed as

$$H_{dlf}(j\omega) = K_p + K_i \frac{1}{j\omega T_{ref}} \tag{3.6}$$

where K_p and K_i are proportional gain and integral gain, respectively, and T_{ref} is reference clock period. Then, open loop gain of the PLL loop is expressed as

$$H_{ol}(j\omega) = K_{pd} \cdot H_{dlf}(j\omega) \cdot \frac{K_{dco}}{j\omega} \cdot H_{rl}(j\omega). \tag{3.7}$$

Reference noise and oscillator noise transfer functions are expressed as

$$H_{\phi_{out},\phi_{ref}}(j\omega) = \frac{\phi_{out}}{\phi_{ref}}(j\omega) = \frac{N \cdot H_{ol}(j\omega) + 2H_{up}(j\omega)}{1 + H_{ol}(j\omega)} \tag{3.8}$$

$$H_{\phi_{out},\phi_{dco}}(j\omega) = \frac{\phi_{out}}{\phi_{dco}}(j\omega) = \frac{H_{rl}(j\omega)}{1 + H_{ol}(j\omega)}, \tag{3.9}$$

respectively. Then, each noise source to the output clock is expressed as

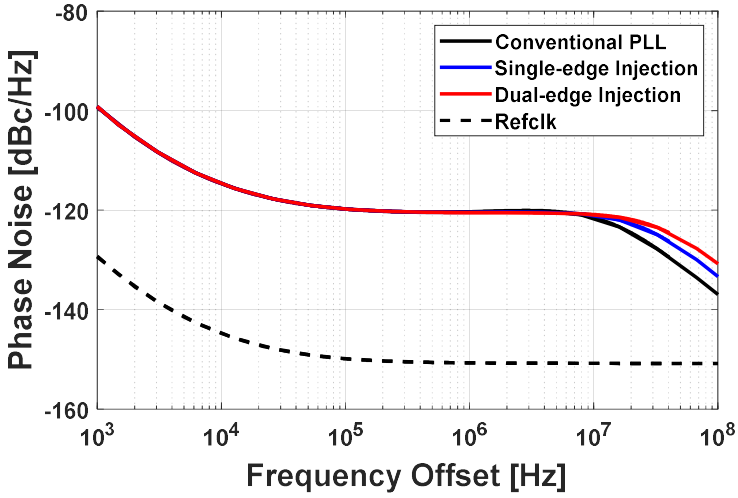
$$S_{\phi_{out},\phi_{ref}}(f) = \left|H_{\phi_{out},\phi_{ref}}(j\omega)\right|^2 \cdot S_{\phi_{n,ref}}(f) \tag{3.10}$$

$$S_{\phi_{out},\phi_{dco}}(f) = \left|H_{\phi_{out},\phi_{dco}}(j\omega)\right|^2 \cdot S_{\phi_{n,dco}}(f) \tag{3.11}$$

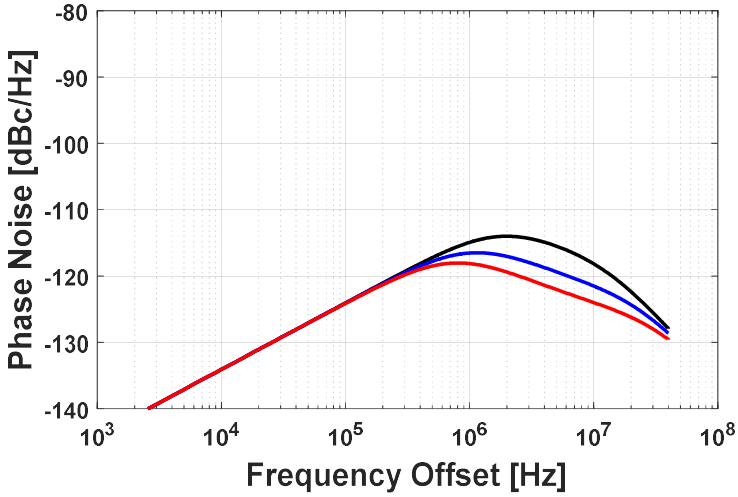
Assuming that the other noise sources such as DCO quantized noise and delta-sigma modulator noise is negligible compared to the total output noise, the total output noise expressed as

$$\mathcal{L}(f) = 10\log\left(S_{\phi_{out},\phi_{ref}}(f) + S_{\phi_{out},\phi_{dco}}(f)\right). \tag{3.12}$$

From (3.8)–(3.12), the each noise source contribution to the output according to no injection ($\beta = 0$), single-edge injection, and dual-edge injection is shown in Fig. 3.10. Because the dual-edge injection has more injection effects, the contribution of the reference noise source increases, but the oscillator noise is filtered out the most. Therefore, when the oscillator noise dominates over the total phase noise, the dual-edge injection shows the best performance in terms of the phase noise as shown in Fig. 3.11.


Conventional PLL
Single-edge Injection
Dual-edge Injection
Refclk
Phase Noise [dBc/Hz]
-80
-100
-120
-140
-160
10^3
10^4
10^5
10^6
10^7
10^8
Frequency Offset [Hz]

(a)


Phase Noise [dBc/Hz]
-80
-90
-100
-110
-120
-130
-140
10^3
10^4
10^5
10^6
10^7
10^8
Frequency Offset [Hz]

3.3.3 Spur Analysis

The phase noise of the dual-edge injection is more suppressed since the multiplying factor is halved in the transfer function representing the phase realignment, thereby the dual-edge injection improves the jitter performance. However, the duty-cycle error of the reference clock as well as the timing mismatch between the PLL loop and injection path can cause a reference spur in the ILPLL. The detailed analyses and effects are presented as follows.

In order to derive optimal injection timing in a conventional ILPLL, the total delay by the injection D_1 and PLL feedback D_2 should be integer times the period of the PLL output clock T_{DCO} as shown in Fig. 3.14(a). This requirement can be expressed as

$$D_1 + D_2 = k \cdot T_{DCO} \quad (k = 1,2,3, \dots) \tag{3.19}$$

where k is the delay in cycles. When $D_1 + D_2$ is not equal to integer times the DCO clock period, the offset frequency appears in the DCO and increases the reference spur as studied in [12]. To further investigate the effect of the dual-edge injection adopted in [17]–[20], [28], the duty-cycle error of the injection clock is additionally considered. Fig. 3.14(b) shows the timing diagram of a stable PLL without an injection. When dual-edge injection is performed with the initial phase mismatch θ_{init} and duty-cycle phase error $\Delta\theta_{duty}$, the DCO frequency drift occurs in response to the phase error detected by the PLL loop. Fig. 3.14(c) presents a timing diagram of a stable PLL with dual-edge injection.

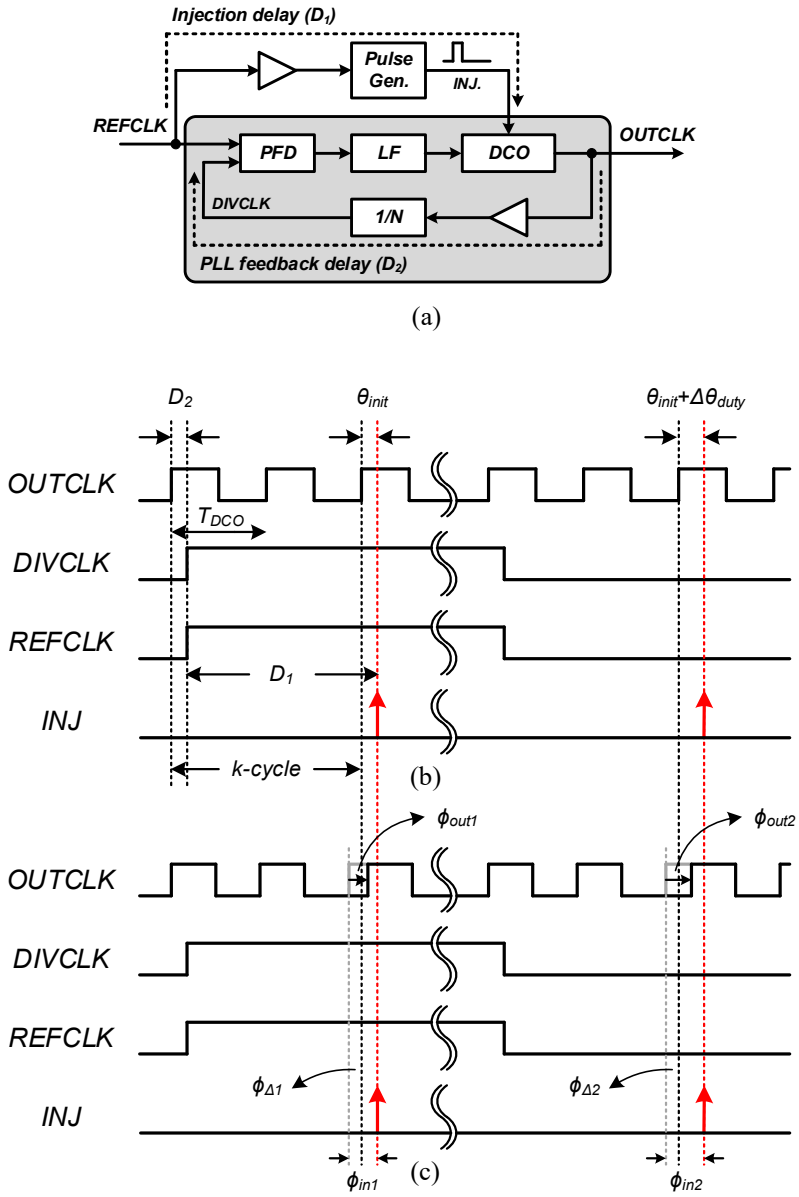


Fig. 3.14 (a) Block diagram of conventional ILPLL. Timing diagrams of stable PLL (b) without injection and (c) with dual-edge injection.

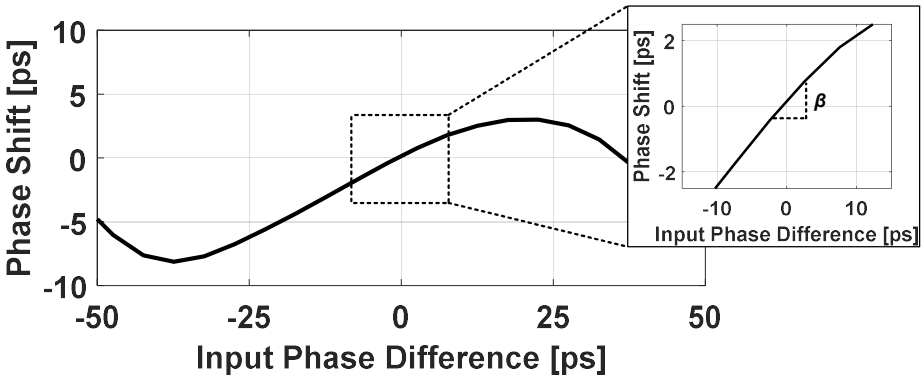


Fig. 3.15 Simulated phase shift by an injection according to input phase difference with the oscillator of 5-GHz output frequency.

To simplify the analysis, assume an ideal linear relationship between output phase shift and input phase deviation. PDR simulation result of the CSI technique is shown in Fig. 3.15, where the validity of the assumption is demonstrated under small phase shift. The ratio of the output phase shift ϕ_{out1} (ϕ_{out2}) to the input phase deviation ϕ_{in1} (ϕ_{in}) is denoted by realignment factor β and their relationship can be expressed as $\phi_{out1} = \beta \cdot \phi_{in}$ ($\phi_{out2} = \beta \cdot \phi_{in2}$). The input phase deviations of dual-edge are expressed as

$$\phi_{in1} = \theta_{init} + \phi_{\Delta 1} \tag{3.20}$$

$$\phi_{in2} = \theta_{init} + \Delta\theta_{duty} + \phi_{\Delta 2} \tag{3.21}$$

where $\phi_{\Delta 1}$ and $\phi_{\Delta 2}$ are the phase offset on the verge of the injection. These are expressed as

$$\phi_{\Delta 1} = k \cdot \Delta\omega \cdot T_{DCO} \tag{3.22}$$

$$\phi_{\Delta 2} = N/2 \cdot \Delta\omega \cdot T_{DCO} - (\phi_{out1} - \phi_{\Delta 1}) \tag{3.23}$$

where $\Delta\omega$ is the offset frequency of the DCO and N is the PLL division factor. The total output phase shift by the dual-edge injection is expressed as

$$\phi_{out1} + \phi_{out2} = N \cdot \Delta\omega \cdot T_{DCO}. \tag{3.24}$$

According to the (3.20)–(3.24), the frequency deviation of the DCO is expressed as

$$\Delta\omega = \frac{\beta \cdot \theta_{init} + \beta/(2-\beta) \cdot \Delta\theta_{duty}}{(N/2 - k \cdot \beta) \cdot T_{DCO}}. \tag{3.25}$$

The results of the analysis and Verilog simulation are shown in Fig. 3.16. The simulation is performed on the entire ILPLL model including the injection-locked DCO, the phase detector, and the digital loop filter. In the Verilog model of the injection-locked DCO, the output phase shift by the injection is defined as the product of the input phase deviation and the injection strength. The simulation results verify the analysis and indicates that the offset frequency increases with the duty-cycle error and initial phase mismatch. Fig. 3.17 shows the simulation result of the frequency domain when injection timing mismatch and reference clock duty-cycle error occurs.

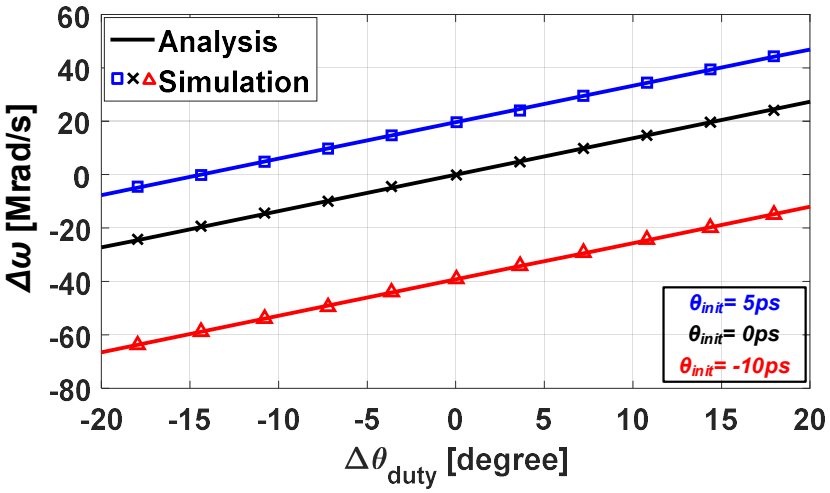
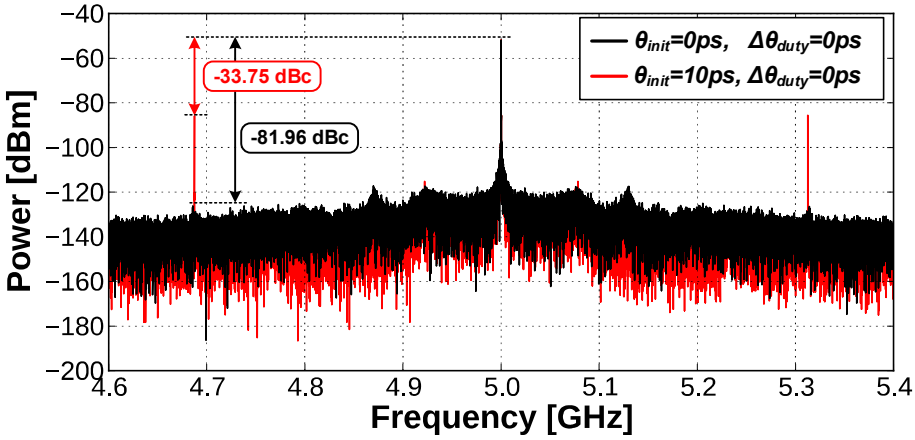
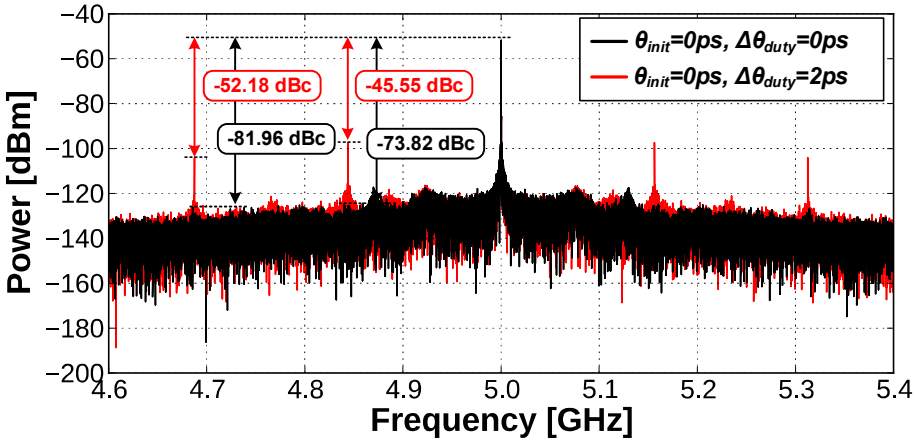


Fig. 3.16 Calculated and simulated offset frequency according to duty-cycle error and delay mismatch (F_{OUT} = 5 GHz, F_{REF} = 156.25 MHz, k=0 and β = 0.4).



(a)



(b)

Fig. 3.17 Simulation results in frequency domain of the ILPLL output clock when (a) injection timing mismatch exists and (b) duty-cycle error of the injection clock exists.

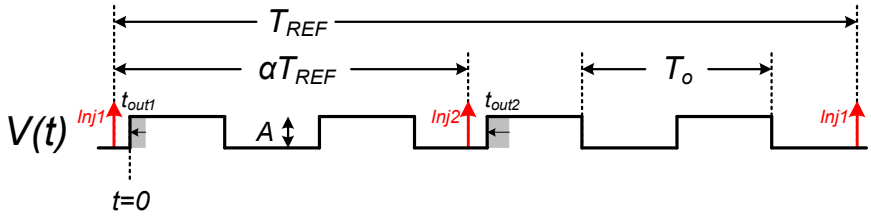


Fig. 3.18 Time-domain waveform of stable injection-locked clock (e.g., $N = 4$) with dual edge injection.

With the dual-edge injection, frequency deviation alone is not enough to analyze the reference spur as presented in [7]. Instead, Fourier series transform can be utilized. From (3.22)–(3.25), the reference spur of the ILPLL can be derived. The calculation is based on the fact that the injection leads to only PM distortion as studied in [45]. Fig. 3.18 shows the timing waveform of a stable injection-locked clock with dual-edge injection. Assuming that the oscillator works at the frequency of ω_o and the injection clock frequency is ω_{REF} $(\omega_o = N \cdot \omega_{REF} + \Delta\omega)$ with duty-cycle of α, the injection-locked clock is periodic with T_{REF}. Its Fourier series is expressed as

$$V(t) = a_0 + \sum_{m=-\infty}^{\infty} (a_m \, cos(m\omega_{REF}t) + b_m \, sin(m\omega_{REF}t)) \tag{3.26}$$

The coefficients of harmonics are expressed as

$$a_0 = \frac{1}{T_{REF}} \int_0^{T_{REF}} V(t)dt \tag{3.27}$$

$$a_m = \frac{1}{T_{REF}} \int_0^{T_{REF}} V(t) \cdot cos(m\omega_{REF} t)\, dt$$
$$= \frac{2}{m} 2\cos\left(\frac{1}{4} m(2t_{out2} - NT_o)\omega_{REF}\right)$$
$$\times \sec\left(\frac{mT_o\omega_{REF}}{4}\right) \sin\left(\frac{mNT_o\omega_{REF}}{4}\right) \tag{3.28}$$
$$\times \cos\left(\frac{1}{4} m(2t_{out} + T_o - 2NT_o)\omega_{REF}\right)$$

$$b_m = \frac{1}{T_{REF}} \int_0^{T_{REF}} V(t) \cdot sin(m\omega_{REF} t)\, dt$$
$$= \frac{2}{m} \cos\left(\frac{1}{4} m(2t_{out2} - NT_o)\omega_{REF}\right)$$
$$\times \sec\left(\frac{mT_o\omega_{REF}}{4}\right) \sin\left(\frac{mNT_o\omega_{REF}}{4}\right) \tag{3.29}$$
$$\times \sin\left(\frac{1}{4} m(2t_{out2} - 2NT_o)\omega_{REF}\right).$$

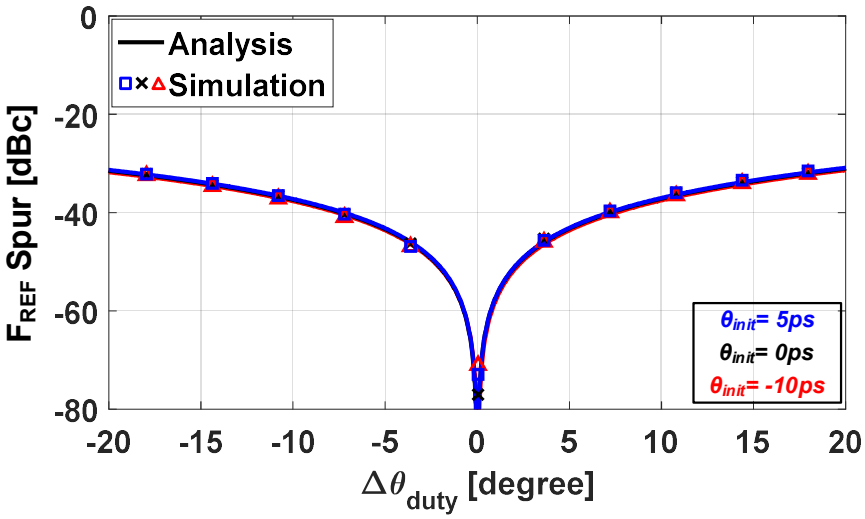
where A is the amplitude of the clock, T_o is the output frequency of the oscillator, and t_{out2} is the output time shift on the falling edge of the reference clock. The power of the *m*th harmonic of the reference can thus be expressed as

$$P_m = {a_m}^2 + {b_m}^2$$
$$= \left(\frac{2A}{m\omega_{REF} T_{REF}} \cdot \cos(m\omega_{REF}(2t_{out2} - NT_o)/4)\right. \tag{3.30}$$
$$\left. \times \sec(m\omega_{REF} T_o/4) \cdot \sin(mN\omega_{REF} T_o/4)\right)^2$$

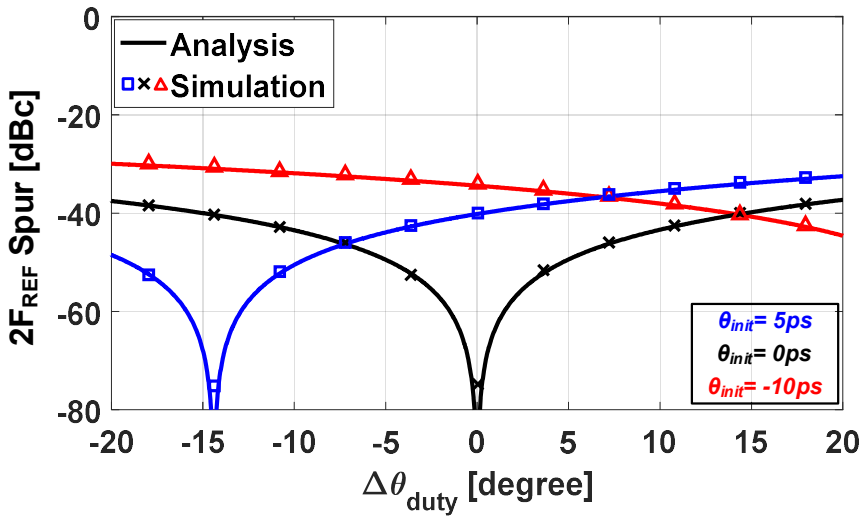
Therefore, the spur on *n* times reference frequency ($n \cdot F_{REF}$) can be obtained as

$$spur = 10 \cdot log_{10}(P_{N\pm n}/P_N). \tag{3.31}$$

For a fixed k, the calculated and simulated reference spur according to the duty-cycle error is indicated in Fig. 3.19. The duty-cycle error impacts on the both the reference frequency F_{REF} and two times reference frequency $2F_{REF}$ spurs. On the other hand, the initial phase mismatch has minimal influence on the F_{REF} spur and only affects $2F_{REF}$ spur. Therefore, both the duty-cycle error and initial phase mismatch should be minimized for improved performance of both spurs simultaneously. The simulation results of the reference spurs with different k-cycle is shown as below. When the delay mismatch or the duty-cycle error occurs ($\theta_{init} \neq 0$, $\Delta\theta_{duty} \neq 0$), the larger k leads to increasing the offset frequency and higher $2F_{REF}$ spur as shown in Fig. 3.20. In this work, the presented ILPLL enables $k = 0$ owing to the SSBBPD, which makes injection timing error less susceptible to voltage and temperature variations. Also, it comprises a duty-cycle corrector (DCC) to reduce the reference spurs.

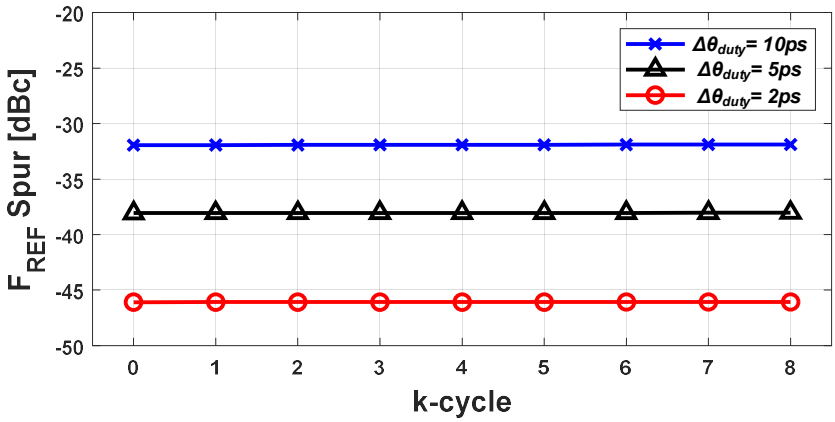


(a)

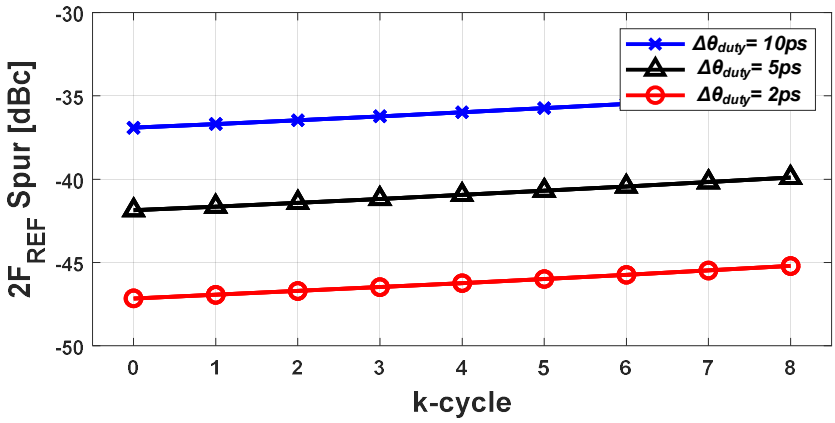


(b)

Fig. 3.19 Calculated and simulated spurs of the (a) F_{REF} and (b) $2F_{REF}$ according to delay mismatch and duty-cycle (F_{OUT} = 5 GHz, F_{REF} = 156.25 MHz, k=0 and β = 0.4).



(a)



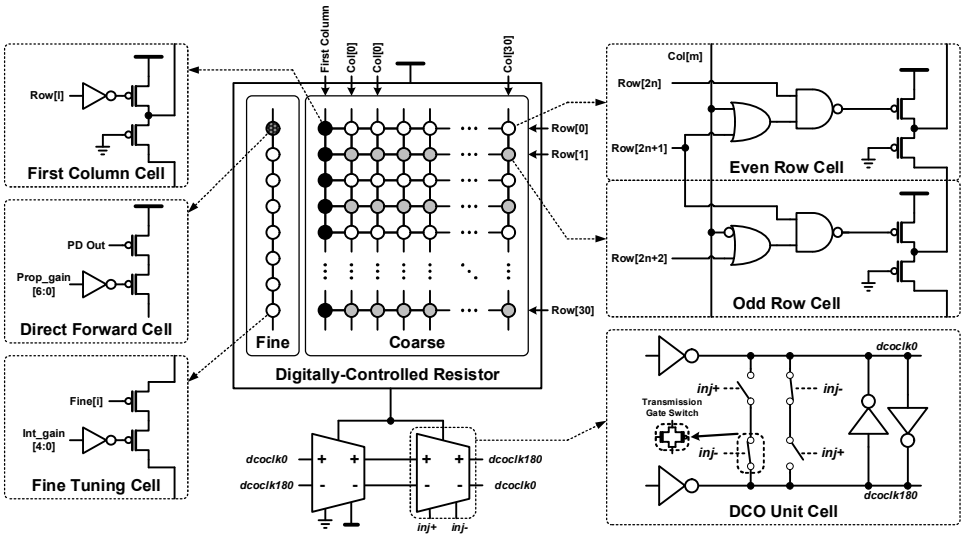
(b)

Fig. 3.20 Simulated phase shift by an injection according to input phase difference with the oscillator of 5-GHz output frequency.

3.4 Circuit Implementation

3.4.1 Digitally Controlled ILO

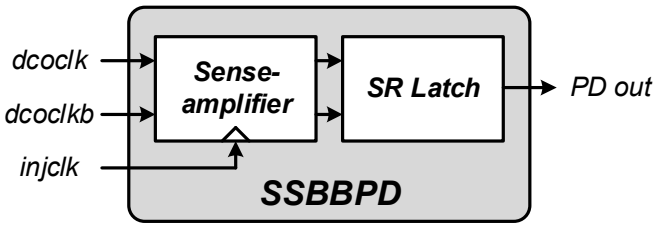
The circuit implementations of the DCO is described in Fig. 3.21. The DCO is composed of two digitally-controlled resistors (DCRs): one is for coarse frequency tuning [41] controlled by the FLL and the other is for fine frequency tuning controlled by the PLL. The switch resistor in the coarse DCR is made up of 1024 PMOS transistors and thermometer code is adopted. Also, the fine DCR consists of the seven parallel switch resistors. The step size of the coarse DCR is about 4 MHz and that of the fine DCR can vary from 0.6 MHz to 2 MHz.



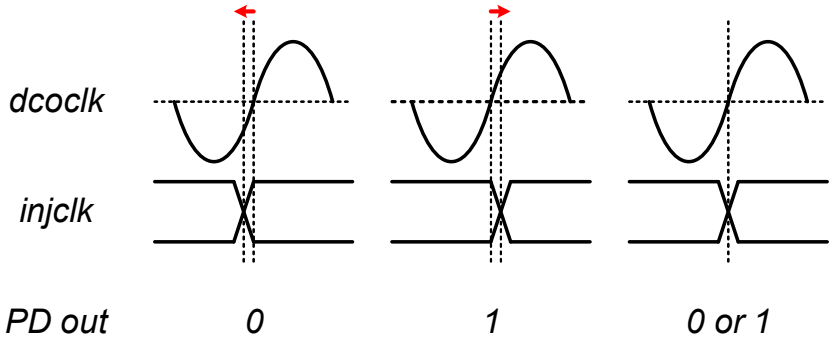
3.4.2 SSBBPD and Front-End

In the ILPLL, one of the most important keys to high performance is minimizing the phase alignment mismatch between the PLL loop and injection path. Although the two control paths are initially matched, voltage and temperature drifts cause a timing mismatch depending on the delay sensitivity to the drift. For example, the delay variation of an inverter-based delay line in terms of voltage and temperature variations ranges from -30% to 100% [39]. To solve this problem, an injection timing calibration circuit is proposed in [8], [12], [14]. However, this entails a substantial increase of power dissipation. In this work, an SSBBPD is adopted instead of the injection timing calibration circuit. As a result, the SSBBPD allows removing the latency of the buffer down to zero and makes the injection timing error less sensitive against the voltage and temperature drift.

The SSBBPD detects the voltage difference between the differential DCO clocks when it is triggered by the reference clock. Therefore, the DCO clock edge and the reference clock edge are aligned by the PLL as shown in Fig. 3.22. With the direct connection of the DCO clock to the SSBBPD, the proposed sense-amplifier [18] based on the tail-less structure eliminates the input capacitance variation due to the clock toggling as shown in Fig. 3.23(a). In comparison with the conventional sense-amplifier [42], the loading capacitance of the DCO output remains unchanged even if the reference clock toggles. As a result, it enables the DCO frequency to remain constant as indicated in Fig. 3.23(b).



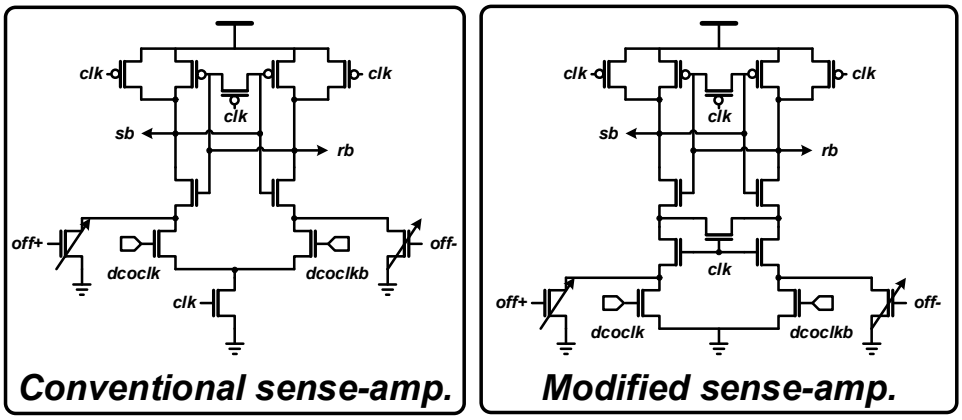
(a)



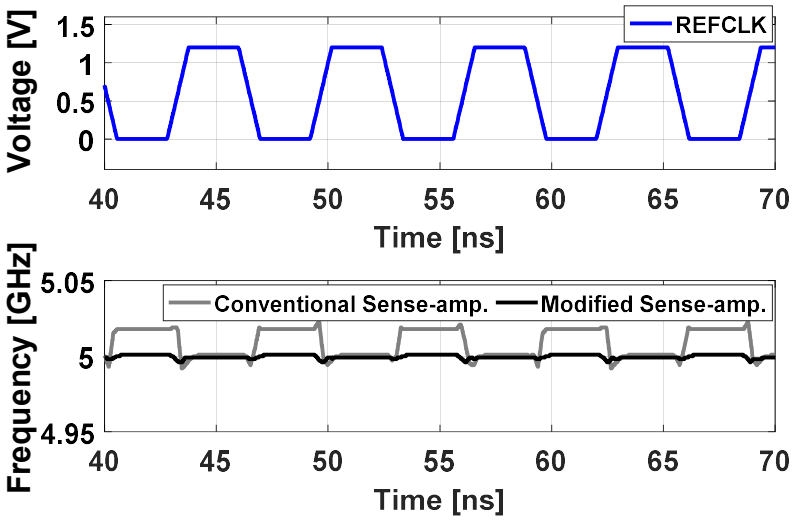
(b)

Fig. 3.22 (a) Block diagram and (b) time-domain waveforms of the SSBBPD.

In the designed sense-amplifier, the standard deviation of the input-referred offset is simulated as 28 mV_{diff}, as shown in Fig. 3.24. This offset voltage can lead to a timing mismatch of the two control paths as shown in Fig. 3.25(a). Therefore, the sense-amplifier is equipped with a mismatch calibration capability of covering up to 145-mV_{diff} offset by adjusting the offset control code. When the offset control code is initially set, the delay of the PLL feedback path varies less than 2.7 ps over the voltage and temperature variations as shown in Fig. 3.25(b). As a result, timing mismatch of the phase alignment between the two control paths is reduced to less



(a)



(b)

Fig. 3.23 (a) Conventional sense-amplifier and modified tail-less sense-amplifier. (b) Time-domain DCO frequency between conventional sense-amplifier and modified structure.

than 2.7 ps in the presence of the voltage and temperature drift.

The front-end of the reference clock consists of a DCC and single-to-differential converter as shown in Fig. 3.26. The DCC is composed of two-stage inverter-based unit cell. By inserting controllable pull-up/down MOSFETs in every stage, the rising and falling time of the buffered reference clock can be controlled and the difference between rising and falling time makes the duty-cycle adjustable. The duty-cycle error can be calibrated from -57 ps to 57 ps.

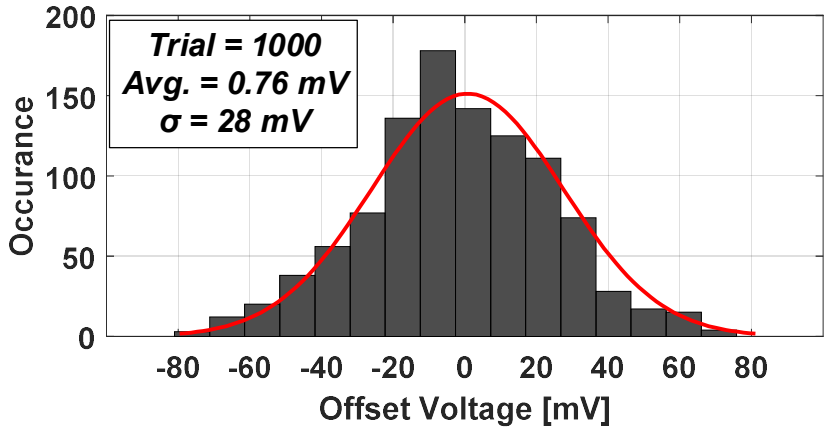
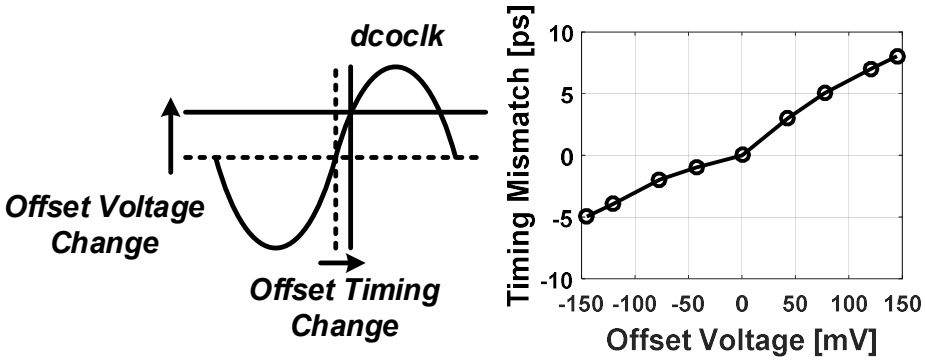
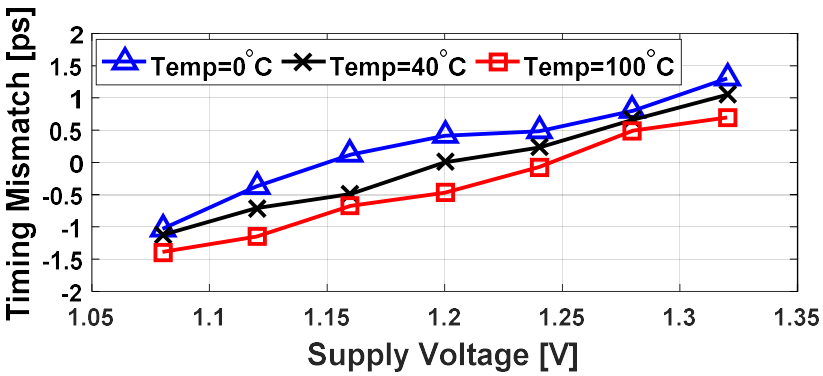


Fig. 3.24 Monte-Carlo simulation results of the sense-amplifier offset.



(a)



(b)

Fig. 3.25 (a) Simulation results of the timing mismatch according to the offset voltage with illustrated timing diagram. (b) Simulation results of the timing mismatch across supply voltage and temperature variation.

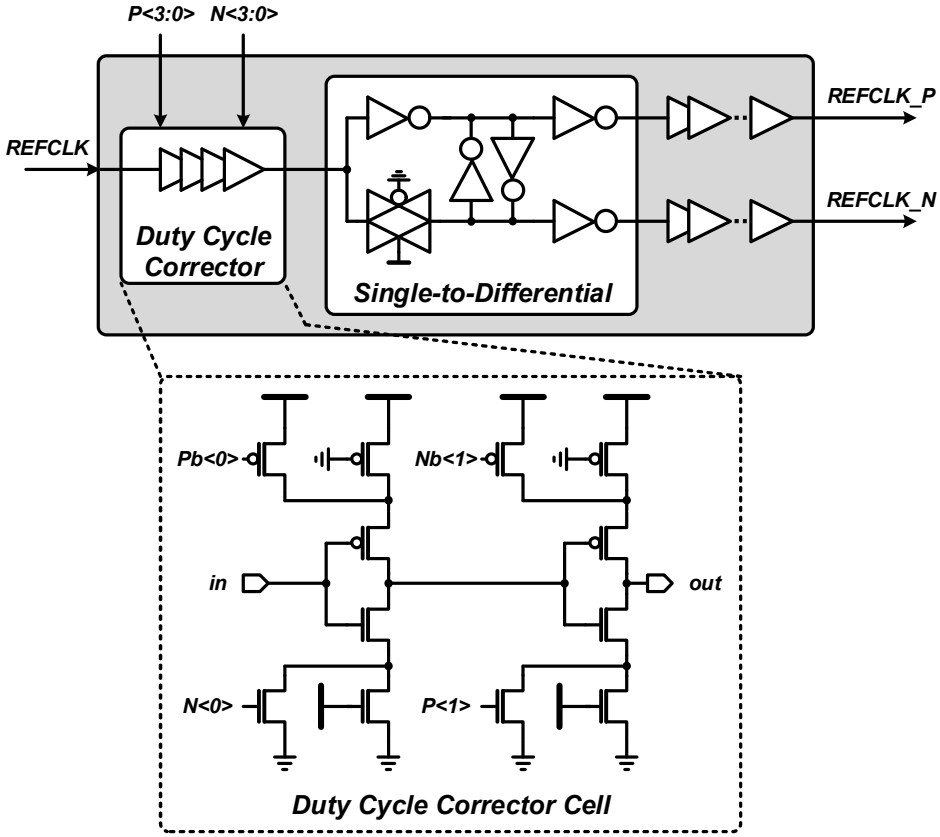


Fig. 3.26 Block diagram of front-end of reference clock.

3.4.3 Frequency Detector

In the PLL loop, the frequency detector works at the startup of the PLL and operates in the background. It does not detect the small frequency deviation of the injection-locked oscillator. However, because the frequency of the oscillator can vary significantly with the voltage and temperature variations, it can prevent harmonic lock from the frequency drift. Fig. 3.27(a) shows the frequency detector, the structure of which is based on [43], with the following timing requirements. First, the *REF_SYNC*, which is a reference clock synchronized by *DCOCLK*, should lag the last output of the divider. Further, the delay from *DCOCLK* to *REF_SYNC* should be less than a period of the *DCOCLK* as shown in Fig. 3.28(a). Hence, the timing constraint is expressed as

$$N_C \cdot t_{divider} < t_{DCOCLK-to-REF_SYNC} < T_{DCO} \tag{3.32}$$

where N_C is the number of dividers in the asynchronous counter and $t_{divider}$ is the latency of the divider. In [43], *REF_SYNC* is synchronized with the negative edge of *DCOCLK* assuming the last output of the divider leads the negative edge of *DCOCLK*. However, as the frequency of the oscillator and the division factor of the PLL increase, it is difficult to satisfy the timing requirements. In order to meet the timing requirements in the proposed ILPLL, the *DCOCLK* is divided before the counter and the requirement is modified as

$$N_C \cdot t_{divider} < (T_{DCO}/2) \cdot 2^{N_{DCO}} \tag{3.33}$$

where N_{DCO} is the number of divide-by-2 circuits from the *DCOCLK* to the counter input. The number of dividers in the counter and the frequency resolution of the counter can be expressed as

$$N_C = \|\log_2(T_{REF}/T_{DCO})\| + N_{REF} - N_{DCO} + M \tag{3.34}$$

$$\Delta f_{LSB} = \frac{1}{T_{REF}} \cdot \frac{2^{N_{DCO}}}{2^{N_{REF}}} \tag{3.35}$$

where T_{REF} is the period of the reference clock, N_{REF} is the number of divide-by-2 circuits from the reference clock to the counter input, and M is the number of additional dividers determined by the DCO maximum frequency. In this work, the designed frequency detector has a parameter of N_C = 6 and Δf_{LSB} = 156.25 MHz, which result from N_{DCO} = 4, N_{REF} = 4, and M = 1, thereby satisfying the timing requirements with detecting up to 10-GHz of DCO frequency. As a result, the frequency error is updated by 16 times the reference period as shown in Fig. 3.28(b) and derives the target DCO code through a digital accumulator.

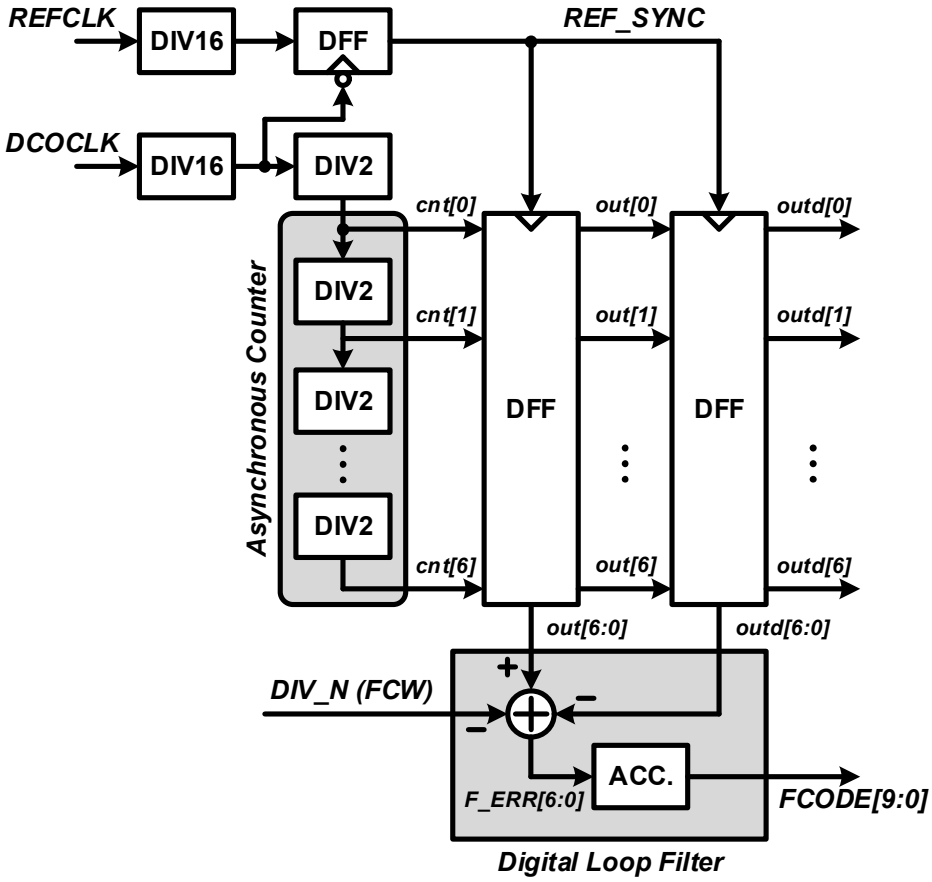
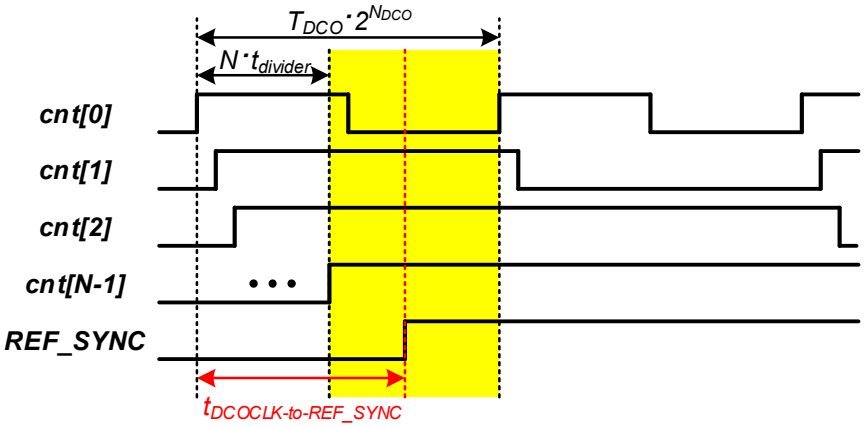
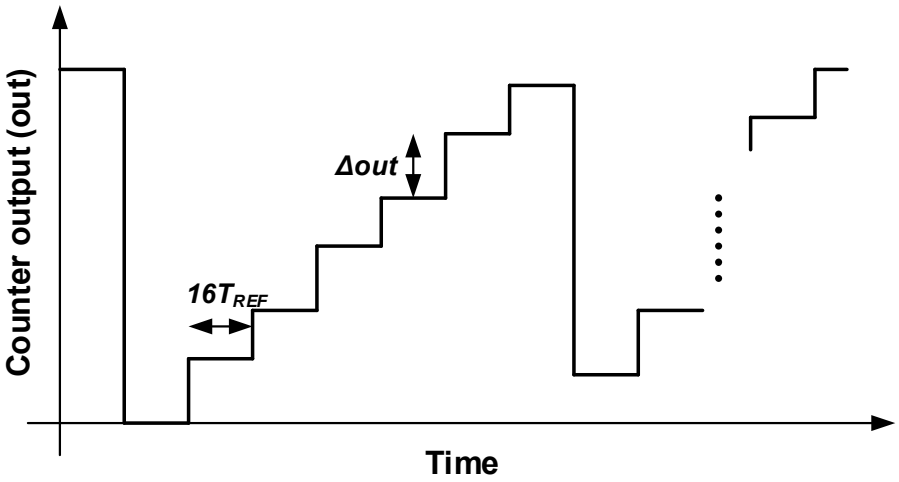


Fig. 3.27 Block diagram of frequency detector.



(a)



(b)

Fig. 3.28 (a) Timing diagram for timing constraint of frequency detector. (b) Counter output.

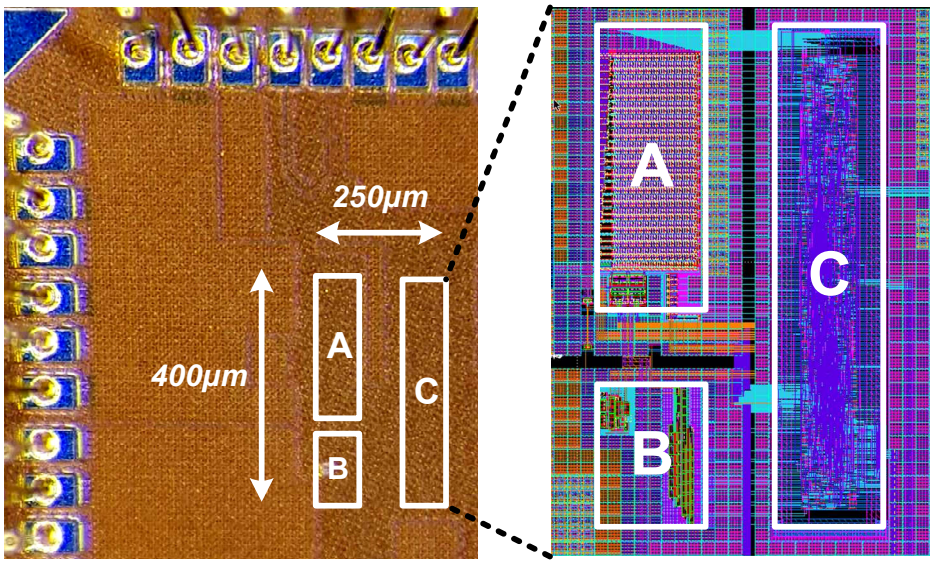
Chapter 4

Measurement

The prototype of the proposed ILPLL was fabricated in 65-nm CMOS technology and occupied a total active area of 0.06 mm^2. Fig. 4.1 shows the die microphotograph, which indicates that the digital logic occupies the majority of the area. With a 156.25-MHz reference clock, the power consumption of the ILPLL is 15.4 mW with a 1.2-V supply at 5-GHz output frequency.

Fig. 4.2 shows the phase noise spectrum of the 5-GHz clock. With the 156.25-MHz injection clock, the phase noise does not show sufficient reduction below the 10-MHz offset frequency because the slope of the DCO phase noise in the region is steeper than -20 dB/decade due to the flicker noise. However, with the combination of a PLL and injection, the phase noise decreases to -123.2 dBc/Hz at the 1-MHz offset frequency and the integrated RMS jitter from 1 kHz to 40 MHz becomes 168 fs. These are superior results to those of the PLL alone indicating -121.1 dBc/Hz at 1-MHz offset and 390-fs integrated jitter. This result demonstrates that in-band

phase noise is considerably suppressed by the PLL loop and the phase noise around the PLL bandwidth is reduced by the injection, which results in the reduced peaking as the phase margin is improved. The measured phase noise of the free-running is flat below 200 kHz because the equipment employs a direct phase noise measurement technique rather than the phase detection technique. Therefore, when



	Block Description	Power [mW]
A	DCO, SSBBPD	8
B	FD, S-to-D	1
C	Digital Loop Filter	6.4

Fig. 4.1 Die microphotograph and its block description with power consumption.

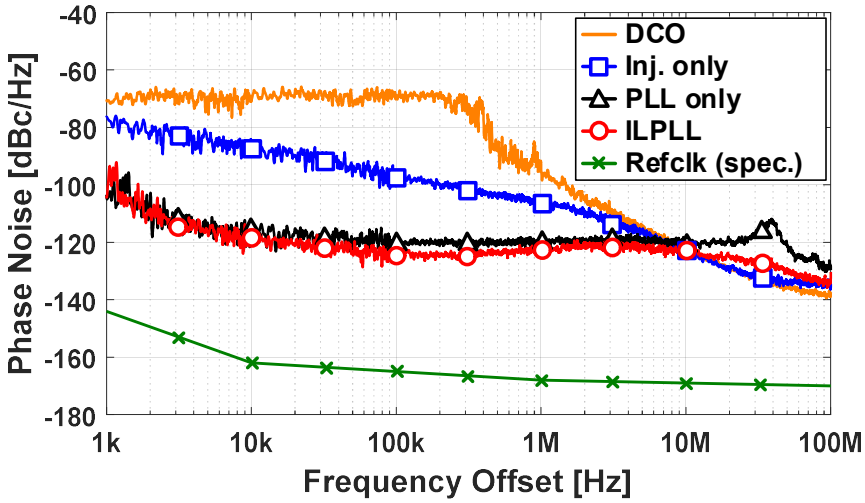


Fig. 4.2 Measured phase noises of a 5-GHz with injection only, PLL only, and ILPLL.

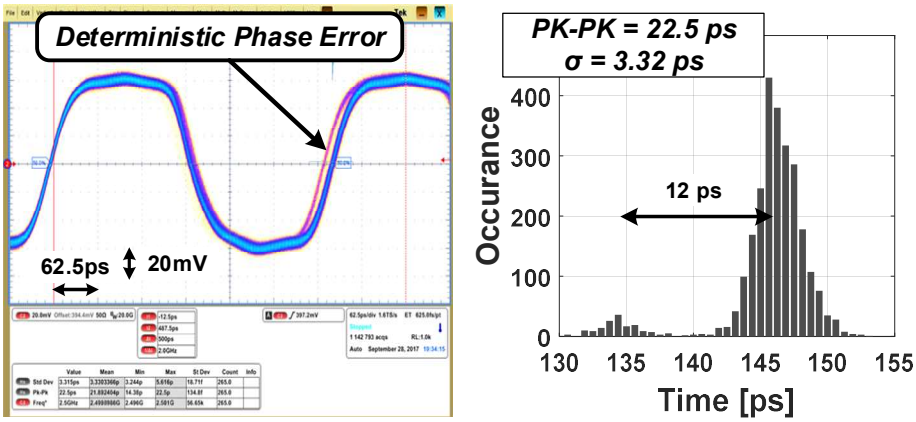
the DCO free-running frequency drifts while measurement is down, the amount of drifts appears as additional frequency offset, thereby showing the corner frequency of the flat region. Although the test measurement technique has the limitation on evaluating the phase noise of the free-running, jittery oscillators precisely at the low offset frequency region, it is inferred that the phase noise of the free-running DCO from the measured phase noise of the oscillator with injection alone, which indicates the slope of the phase noise below f_c is -10dBc/decade.

Fig. 4.3 shows the measured waveforms of the output clock and jitter histogram with the number of acquisitions more than a million times. When a delay mismatch exists between the injection and PLL paths, the deterministic phase error occurs as indicated in Fig. 4.3(a). The peak-to-peak jitter and RMS jitter are 22.5 ps and 3.32 ps, respectively. By adjusting the offset code of the SSBBPD, deterministic phase

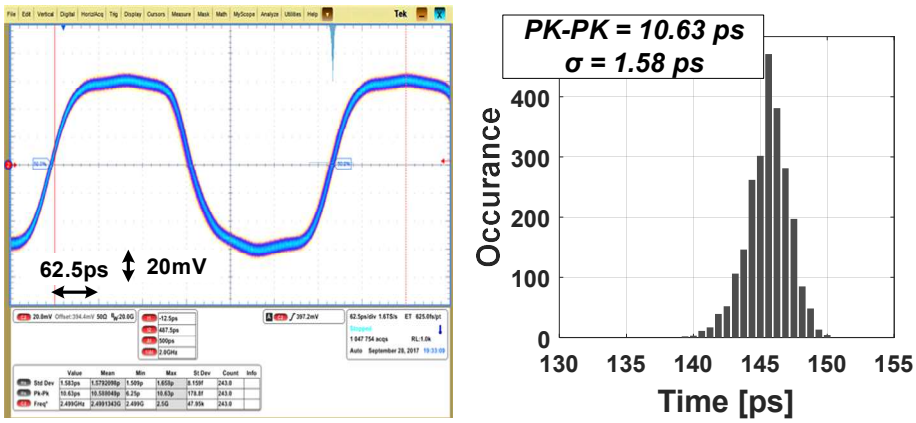
error disappears and peak-to-peak jitter and RMS jitter decrease to 10.63 ps and 1.58 ps, respectively as shown in Fig. 4.3(b).

Fig. 4.4(a) presents the measurement results of the F_{REF} and $2F_{REF}$ spur according to the variation of the duty-cycle of the reference clock. With increased duty-cycle error, spur at the F_{REF} and $2F_{REF}$ is degraded as shown in Fig. 4.4(b). Fig. 4.5(a) indicates the measurement results of the reference spur and integrated RMS jitter due to the delay mismatch under the 50% duty-cycle reference clock. As previously analyzed, the delay mismatch does not affect the F_{REF} spur. However, it has significant influence on the $2F_{REF}$ spur as shown in Fig. 4.5(b). In the optimized offset condition, the $2F_{REF}$ spur and the integrated RMS jitter have the best performance. This verifies that there is nearly zero conflict between the two aligning mechanisms in the proposed ILPLL. The F_{REF} spur at the optimized offset condition is -42 dBc, which is mainly due to the supply voltage fluctuation from the reference clocking circuitry leaking the substrate to the DCO, thereby impeding additional improvement of the reference spur.

To verify that the delay mismatch of the ILPLL is insensitive to the supply voltage drift, the $2F_{REF}$ spur and the integrated RMS jitter were measured across the supply voltage variation. Under the condition that the offset cancellation was initially set by the SSBBPD, the $2F_{REF}$ spur and integrated RMS jitter are nearly constant across the supply voltage from 1.17 to 1.3 V as indicated in Fig. 4.6. Fig. 4.7 shows the measurement results of the different clock output frequencies by changing the FCW. The integrated RMS jitter of the ILPLL is the lowest including injection alone and PLL alone regardless of the output frequency.

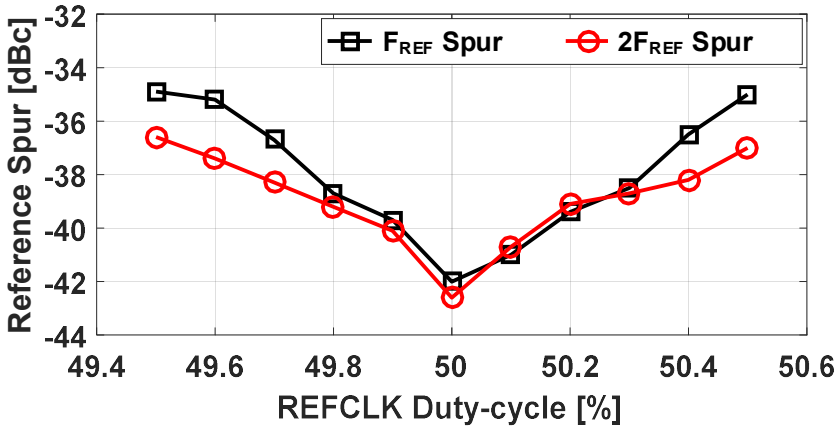


(a)

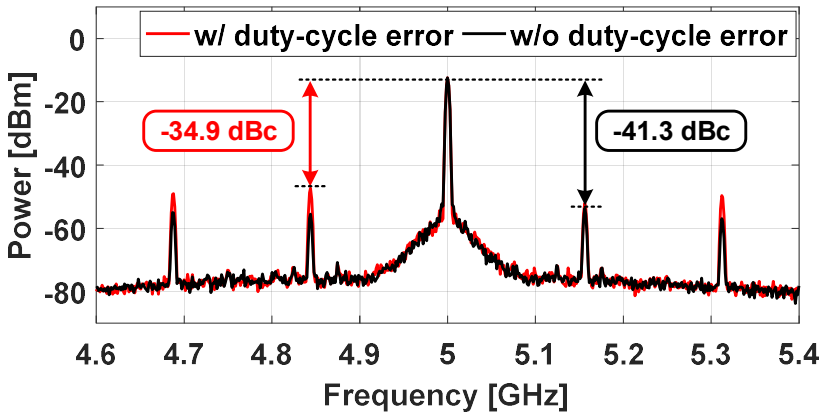


(b)

Fig. 4.3 Measured 2.5-GHz output clock and jitter histogram (a) when delay mismatch occurs and (b) when offset code of the SSBBPD is optimized.

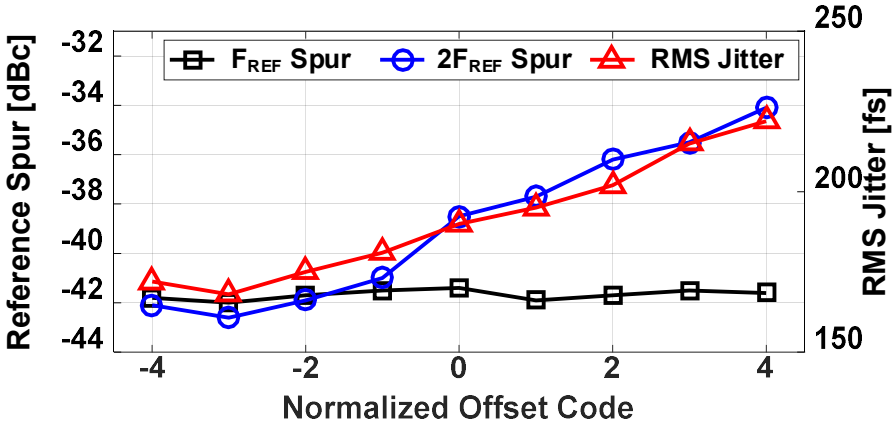


(a)

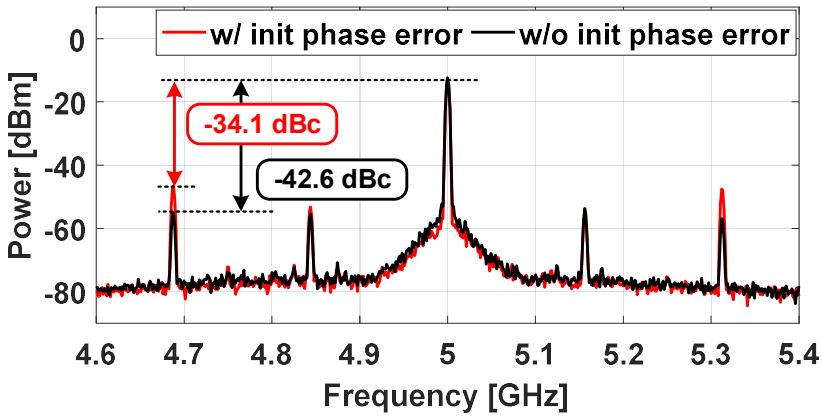


(b)

Fig. 4.4 Measured spurs of the F_{REF} and $2F_{REF}$ versus duty-cycle of the reference clock. (b) Measured output spectrums with and without duty-cycle error of the at 5-GHz frequency.



(a)



(b)

Fig. 4.5 Measured RMS jitter and spurs of the F_{REF} and $2F_{REF}$ versus offset code. (b) Measured output spectrums with and without delay mismatch at 5-GHz frequency.

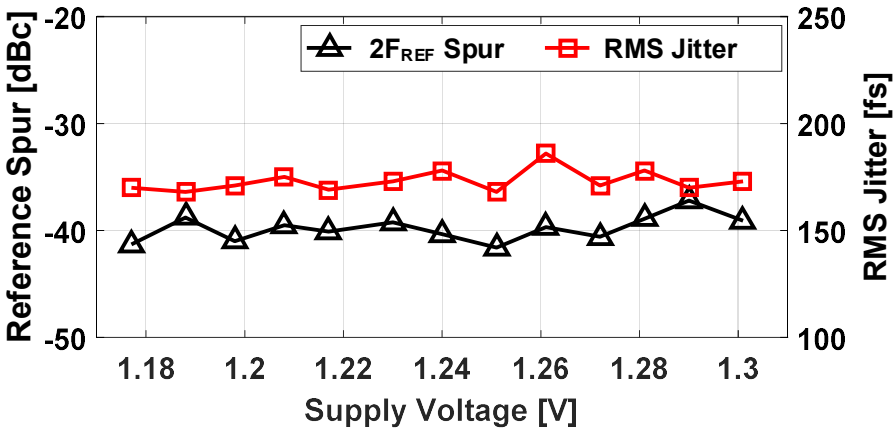


Fig. 4.6 Measured $2F_{REF}$ spur and RMS jitter over supply voltage variation.

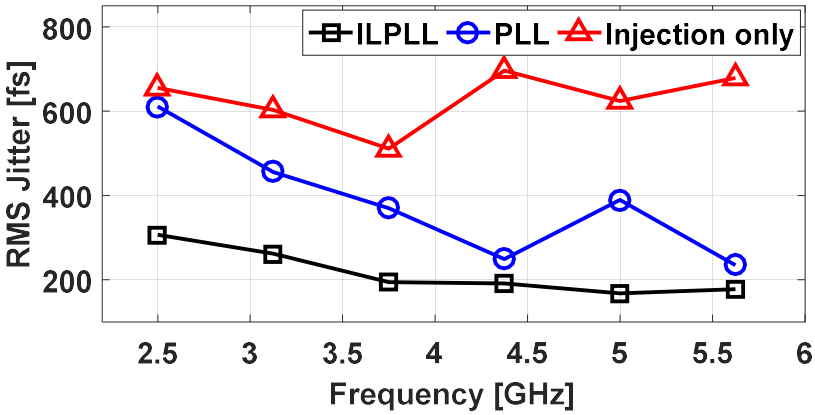


Fig. 4.7 Measured RMS jitter of different clock frequency.

In the Table 2, the performance of the proposed work is compared with other recently published ILCMs. The proposed work achieves the lowest FoM of -243.6 dB, where the FoM is defined in [40] as

$$\mathrm{FoM} = 10\log\left[\left(\frac{\sigma_t}{1s}\right)^2 \cdot \left(\frac{P_{DC}}{1mW}\right)\right]. \tag{4.1}$$

and the FoM of state-of-the-art ring oscillator based ILCM is plotted according to the output frequency as shown in Fig. 4.8. Since ILCMs with small multiplying factor have more injection effects, better performance is proposed as

$$\mathrm{FoM2} = 10\log\left[\left(\frac{\sigma_t}{1s}\right)^2 \cdot \left(\frac{P_{DC}}{1mW}\right) \cdot \left(\frac{1}{N}\right)\right]. \tag{4.2}$$

To consider such injection effect with the multiplying factor, FoM2 includes the multiplying factor for fair comparison. With a FoM2, the proposed work achieves the best performance among the ring oscillator-based ILPLLs in the literature.

Table 2. Performance comparison of ring oscillator based ILCMs.

	[20]	[25]	[28]	[30]	[34]	**This Work**
Technology [nm]	65	65	65	65	28	**65**
Topology	PLL	Dual-loop	PLL	Real-time FTL	MDLL	**PLL**
Reference frequency [MHz]	150	150	125	156.25	75	**156.25**
Dual-edge injection	Yes	No	Yes	No	Yes	**Yes**[††]
Output frequency [GHz] (Range [GHz])	0.9 (0.52-1.15)	0.9 (0.39-1.41)	5 (2.5-5.75)	2.5	2.4	**5 (2.5-5.63)**
Division factor	6	6	40	16	32	**32**
Integrated RMS jitter [ps] (Range [Hz])	0.42 (10k-10M)	1.7 (10k-40M)	0.34 (1k-40M)	0.198 (10k-40M)	0.7 (1k-40M)	**0.168 (1k-40M)**
Area [mm^2]	0.028	0.007	0.09	NA	0.024	**0.06**
Power [mW]	3.8	0.78	5.3	13.5	5.3	**15.4**
F_{REF} / $2F_{REF}$ spur [dBc]	NA / NA	-41 / -51	-53.5 / -46	-65 / NA	-58 / -51	**-42 / -42.6**
FoM [dB]	-241.3	-236.5	-242.1	-242.8	-241.3	**-243.6**
FoM2 [dB]	-249.52	-244.3	-258.1	-254.8	-256.36	**-258.67**

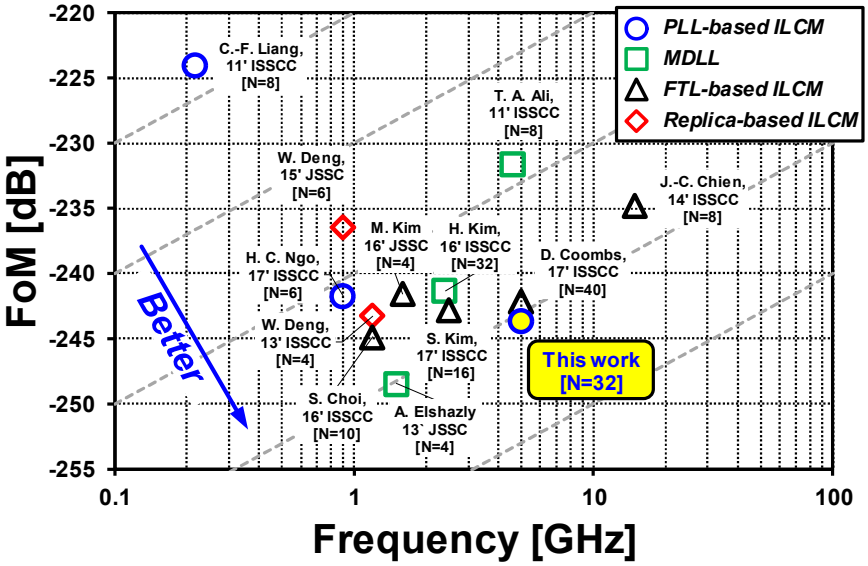


Fig. 4.8 FOM comparison among ring oscillator based ILCMs.

Chapter 5

Conclusion

In this thesis, the low jitter all-digital ILPLL is proposed using the dual-edge CSI and sub-sampling techniques. The proposed ILPLL is focused on simplifying the overall structure of the PLL to exclude additional calibration circuit. Adopting the dual-edge CSI and sub-sampling techniques makes it possible for injection delay and the PLL feedback latency to be zero, thereby eliminating conflict between the two loops. The phase noise analysis of the ILPLL with dual-edge injection was presented. Also, the effect of an inaccurate injection timing in the ILPLL was analyzed and degradation of the ILPLL performance was calculated in terms of the frequency offset and reference spur. With an optimum offset control code in the SSBBPD, the proposed ILPLL generated a wide range of clock frequencies from 2.5 GHz to 5.6 GHz without an additional calibration loop. The proposed ILPLL exhibited a 168-fs integrated jitter and -42 dBc reference spur at 5 GHz ensured robust operation over the voltage and temperature drifts.

Appendix A

Verilog Modeling of ILO

In this chapter, the modeling of the ILO by the Verilog is explained. Assuming that the injection is achieved by the injection clock rising edge, the output phase shift of the oscillator model is determined by the timing difference between the injection clock edge and the oscillator clock edge. Therefore, in the behavior model of the ILO, the phase difference of the oscillator and injection clocks should be sensed. In the real operation, the oscillator clock edge is adjusted in real time near the injection clock edge timing. However, in the behavior model, when the injection edge is lagging the oscillator clock, the oscillator clock edge is predetermined before applying the phase shift. To resolve the issue, the injection timing is determined by falling edge of the oscillator clock as shown in Fig. A.1. When the injection clock rising edge is within the interval of oscillator clock high, it is defined as injection lagging. On the other hand, the injection clock rising edge is within the interval of oscillator clock low, it is defined as injection leading. In the case of the injection

clock lagging, the input phase difference is calculated by subtracting the previous oscillator clock rising edge timing from the injection clock rising edge timing and the next falling edge of the oscillator is adjusted by multiplying realignment factor with the input phase difference. Similarly, in the case of the injection clock leading, the input phase difference is calculated by subtracting the difference between the previous oscillator clock falling edge and the injection clock rising edge from the half period of the oscillator clock. The example of the Verilog modeling of the ILO is shown in Fig. A.2.

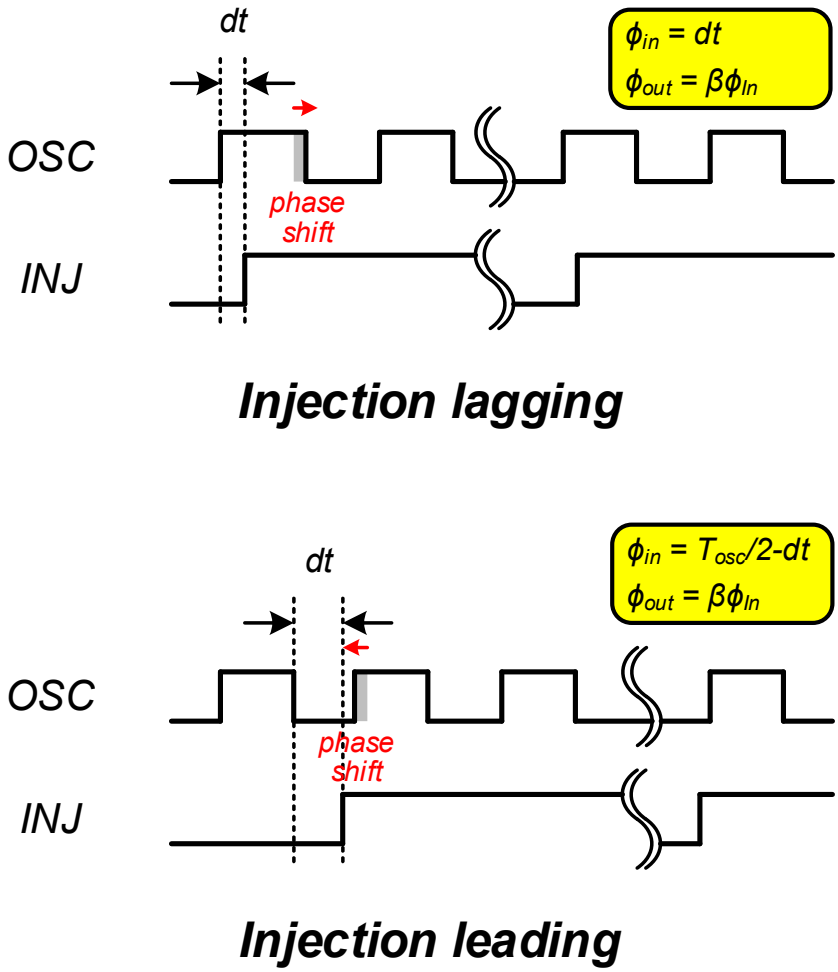


Fig. A.1 Illustration of the timing waveform detecting the input phase difference in Verilog.

```
module a_ilo(
input           wire            pd,
input           wire [30:0]     row,
input           wire [30:0]     col,
input           wire [ 6:0]     col_pd,
input           wire            dir_en,
input           wire            pd_out,
input           wire            inj,
input           wire            inj_en,
output          reg [1:0]       clk_dco
);

// DCO jitter generation
integer         fm_jtt_seed = 286; // Seed
parameter real  fm_jtt_mag = 2e-5; // Magnitude of fm jitter
real            fm_jtt = 0;     // DCO fm jitter
reg [1:0]       int_clk;
initial begin
                int_clk=2'b10;
end
always @(clk_dco[1])
fm_jtt = ($dist_normal(fm_jtt_seed,0,1))*fm_jtt_mag;
// 2stage differential ring oscillator
integer         num_row, num_col, num_total, num_col_pd;
integer         cnt_row,i;
integer         cnt_col,j;
integer         cnt_prop,k,num_prop;
integer         cnt_col_pd,l;
integer         inj_cnt;
always@(*)
                if (inj_en == 1'b1) begin
                        inj_cnt = 1;
                end else begin
                        inj_cnt = 0;
                end

parameter real inj_str = 0.4;
real freq;
real time_dco;
real time_half;
real dT_dif;
reg pos;
assign pdb = ~pd;
```

```
always@(*) begin
        cnt_row=0;
        for (i=0;i<31;i=i+1) begin
                if (row[i] == 1'b1) begin
                        cnt_row = cnt_row +1;
                end
        end
        if(pdb==1'b1) begin
                num_row = cnt_row;
        end
        else begin
                num_row = 0;
        end
end
always@(*) begin
        cnt_col=0;
        for (j=0;j<31;j=j+1) begin
                if (col[j] == 1'b1) begin
                        cnt_col = cnt_col+1;
                end
        end
        if (num_row%2) begin
                cnt_col = 31 - cnt_col;
        end
        if(pdb==1'b1) begin
                num_col = cnt_col;
        end else begin
                num_col = 0;
        end
end
always@(*) begin
        cnt_col_pd=0;
        for (l=0;l<7;l=l+1) begin
                if (col_pd[l] == 1'b0) begin
                        cnt_col_pd = cnt_col_pd+1;
                end
        end
        if(pdb==1'b1) begin
                num_col_pd = cnt_col_pd;
        end else begin
                num_col_pd = 0;
        end
end
```

```
parameter	real		f_min = 2;
parameter	real		f_max = 8;
parameter	real		f_step = (f_max-f_min)/961;
parameter	real		f_pstep = 0.002;
parameter	real		f_dirstep = 0.001;
parameter	real		assym = 0;

always@(*) begin
		num_total = ((num_row)*31 + num_col);
end

always@(num_total or num_col_pd or pd_out) begin
		freq = (f_min + (f_step * num_total))+num_col_pd*f_pstep-
f_dirstep*pd_out*dir_en;
end

always @(posedge clk_dco[1] or pd) begin
		if(pd) begin
				clk_dco[1] <= 1'b1;
				clk_dco[0] <= 1'b0;
		end else begin
				time_dco = $realtime;
				pos = 1;
				#(time_half)
				time_half = 1/freq/2 + fm_jtt +
dT_dif*inj_str*inj_cnt;

				clk_dco[1] <= ~clk_dco[1];

				clk_dco[0] <= ~clk_dco[0];
		end
end

always @(negedge clk_dco[1] or pd) begin
		if(pd) begin
				clk_dco[1] <= 1'b1;
				clk_dco[0] <= 1'b0;
		end else begin
				time_dco = $realtime;
				dT_dif = 0;
				pos = 0;
```

```
                                        #(time_half)

                                        time_half = 1/freq/2 + fm_jtt;

                                        clk_dco[1] <= ~clk_dco[1];

                                        clk_dco[0] <= ~clk_dco[0];
                        end
end

always @(posedge inj) begin
                        if(pos > 0) begin // injection leading
                                        dT_dif = $realtime - time_dco;
                        end else begin  // injection lagging
                                        dT_dif = ($realtime - time_dco) - time_half;
                        end
end

endmodule
```

Fig. A.2 An example of Verilog modeling of ILO.

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초 록

높은 속도의 어플리케이션의 수요 증가로 인하여 좋은 성능의 높은 주파수 생성기의 요구가 증가하고 있다. 이에 따라 주입 고정 발진기를 이용한 연구가 활발히 진행되고 있다. 본 논문에서는 상보적인 스위치 동작을 이용한 주입 고정 위상 동기화 루프 (subharmonically injection-locked phase-locked loop) 의 설계에 관한 연구에 대해 논의한다. 설계의 간소화를 위하여 상보적인 스위치 동작을 이용한 주입방법 (complementary switched injection) 을 제안하고 서브샘플링 위상 검출기 (sub-sampling phase detector) 를 사용하였다. 스위치 동작을 이용한 주입방법은 펄스발생기를 대체함으로써 지연시간이 발생하지 않도록 하였고 주입 클락의 듀얼 엣지에서 주입이 가능하여 싱글 엣지 주입보다 성능이 좋아진다는 장점이 있다. 서브샘플링 위상 검출기 또한 위상 동기화 루프의 피드백 경로에서 지연시간이 발생하지 않기 때문에 추가적인 주입 타이밍 루프가 없어도 주입 경로와 위상 동기화 루프에서 위상이 조정될 때 서로간의 불일치가 발생하지 않는다. 또한, 제안된 구조의 주입 고정 위상 동기화 루프는 전압이나 온도에 덜 민감하게 설계되었다. 제안한 스위치 동작을 이용한 주입방법을 전하 이동을 기반으로 분석하였고 잘못된 타이밍에 주입이 되었을 때 레퍼런스 스퍼에 대한 성능을 비교하였다. 65-nm CMOS 공정을 이용하여 만들어진 칩은 5 GHz 에서 15.4 mW 의 파워 소모와 0.06 mm^2 의 면적을 가진다. 또한, 동작영역은 2.5 GHz 에서 5.6 GHz 를 가지며 5 GHz 에서 168 fs rms 지터를 갖는다.

주요어 : 디지털 위상동기루프, 듀얼엣지 주입, 위상 검출기, 주입고정 발진기, 레퍼런스 스퍼, 감지 증폭기, 서브샘플링 위상동기루프.

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