Ph.D. Dissertation

Design of Injection-Locked PLL and CDR with Circuit Techniques for Optimum Operation

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by

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Department of Electrical Engineering and Computer Science

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Design of Injection-Locked PLL and CDR with Circuit Techniques for Optimum Operation

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Design of Injection-Locked PLL and CDR with Circuit Techniques for Optimum Operation

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Min-Seong Choo

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Abstract

Innovative injection-locking techniques for a high-speed serial link are proposed in both transmitter and receiver. Superior jitter performance is achieved using directly injecting the edge of the input signal to the oscillator. However, a frequency mismatch between the reference input and the local oscillator should be precisely adjusted to deliver the desired operation behavior. Besides, the injection strength should be chosen as a maximal value to achieve a wide bandwidth of the overall structure.

Firstly, a path-mismatch issue in the injection-locked phase-locked loop (ILPLL) is resolved by using a half-edge injection and deserialization of error information in the bang-bang phase and frequency detector (BBPFD). The injection timing is continuously tracked, and the frequency error between the reference clock and the local oscillator vanishes. The timing calibrator enables a robust ILPLL operation over the process, voltage, and temperature (PVT) variations. The proposed ILPLL consumes 5.65 mW at 5 GHz with 0.9-V supply voltage. The measured jitter integrated from 1 kHz to 40 MHz is 152 fs, and the spur levels at the reference and second subharmonic are –62 dBc and –53 dBc, respectively.

Secondly, to achieve a maximum bandwidth of the ILPLL, a technique that increases the injection strength as large as possible is proposed. Also, a phase domain response (PDR) of the injection-locked oscillator (ILO) is analyzed and re-derived for the physically implemented circuits. By doing so, more accurate PDR is obtained, and the optimal locking point is found. Thanks to the modification of the PDR and

the exclusion of the pulse generator, this work achieves a minimum reference spur and integrated jitter in both at the 15-GHz clock. The proposed ILPLL shows integrated jitter from 1 kHz to 40 MHz of 213 fs while achieving a power consumption of 17.81 mW at a clock rate of 15 GHz.

Third, the injection-locking technique is applied to a clock and data recovery (CDR) circuit. To widen the bandwidth of the jitter tolerance (JTOL), directly modulating the phase of the local oscillator is adopted using a rising-edge injection method. Also, similar to an ILPLL structure, a path mismatch between the injection path and the feedback system is compensated using the proposed tracking loop. Just modifying the conventional phase detection logic, 2X oversampling, the path mismatch is detected and eliminated to operate in the desired operating condition. The timing margin of the sampler is maximized thanks to the proposed tracking loop, and it satisfies the bit error rate less than 10^{-12} as 1-UIpp amplitude at the sinusoidal jitter frequency of 31 MHz. Also, the proposed ILCDR achieves the highest energy efficiency of 1.28 pJ/bit among the fully functional ILCDR chips published in the literature.

Keywords: All-digital phase-locked loop (ADPLL), injection-locked oscillator (ILO), injection-locked PLL (ILPLL), injection-locked CDR (ILCDR), injection-timing tracking, phase domain response (PDR)

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Chapter 1

Introduction

1.1 Motivation

With the continuous advance of the CMOS fabrication process, the complexity of very-large-scale integration (VLSI) has been increased. To embed much more functions and achieve higher controllability, a portion of the digital blocks in the entire system has been significant and increasing complexity of digital blocks makes timing budgets harsher. Therefore, for following a rapidly changing system and securing large timing margin, system clocks which have a higher bandwidth and lower jitter is required in numerous applications. Among some previously reported schemes, a methodology that utilizes an injection-locked oscillator (ILO) is a promising candidate to achieve them. Thus, this dissertation presents novel studies on an ILO-based phase-locked loop (PLL) and a clock data recovery (CDR) circuits.

ILOs have widely been adopted in many wireline transceivers since they make it possible to improve jitter performance, power consumption, and hardware size [23]–[34], [37]–[43], and [47]–[63]. Fundamentally, phase information in ILO is directly modified by the input injecting signal. Thus, available bandwidth employing ILO is relatively very high compared with the feedback-type applications such as PLL. Since the bandwidth of the overall system determines the amount of the noise suppression of the oscillator, as the system bandwidth increases, the jitter performance improves. More specifically, injection-locked phase locked loop circuits (ILPLLs), and data recovery circuits (ILCDRs) shows excellent jitter performance and low power consumption with minimal additive hardware in comparison to the conventional structures. Typically, to achieve a superior jitter tolerance (JTOL) performance in the conventional PLL or phase interpolator (PI) based CDRs, large power consumption should be required for better phase noise of the oscillator and the higher sensitivity of the sampler. However, an ILO has a large bandwidth because it directly forwards the transition of data to the local oscillator. In other words, an ILO tracks the phase of the input data stream rapidly, which results in higher JTOL performance.

Despite these advantages of the ILO-based systems, there are some issues have to be solved. In the case of ILPLLs, a robust operation is not ensured unless the injection timing is precisely controlled. Since the reference clock is directed to a phase detector, and at the same time injected into the oscillator, the two paths must be designed carefully since the phase of the oscillator might have already been adjusted by the injection before the phase detector catches the phase error, nullifying

the operation of the PLL or vice versa. To resolve the timing issue in conventional ILPLLs, several calibration methods have been reported in [23]–[30], [33], and [34]. In the case of ILCDR, the main issue to be resolved is a frequency offset between the input data stream and the local oscillator. When the offset is not eliminated, the timing margin of the receiver is reduced significantly. Thus, the reduced timing margin causes a bit error when consecutive identical digits show up. Besides, if the offset exceeds the locking range of an ILO, it could fail to lock. For these reasons, to employ an ILO in CDR applications, a timing calibrator that cancels out the offset is necessary for robust operation over the process, supply voltage, temperature (PVT) variations.

In this dissertation, researches on novel ILPLL and ILCDR are presented, proposing the circuit techniques solving the design challenges as mentioned above. In addition, all ILOs are designed based on the ring oscillator (RO) to get a better tuning range and small silicon area. Conventionally, since the ring oscillators exhibit poor phase noise performance compared with LC oscillators, RO-based PLL shows worse jitter performance though it has some merits. However, since the injection-locking technique can improve inherently poor jitter performance of the ring oscillators, RO-based ILOs have widely been researched in many clocking systems thanks to their remarkable jitter performance and simple implementation.

1.2 Thesis Organization

The remaining chapters in this thesis are organized as follows. In chapter 2, we provide sufficient background of injection-locking techniques and then design examples are introduced for many applications.

In Chapter 3, an injection-timing effect in a conventional injection-locked phase-locked loop (ILPLL) is analyzed, and the timing tracking loop is proposed using a simple technique omitting injection signal every other cycle to achieve a superior jitter performance in the ILPLL structure.

In Chapter 4, a phase domain response (PDR) of the injection-locked oscillator (ILO) is presented in physically implemented circuits that are different from the previous analysis. Using the simple observation, the overall characteristic of the PDR is modified to exhibit an excellent jitter performance.

In Chapter 5, a half-rate all-digital injection-locked clock and data recovery (ILCDR) with maximum timing-margin tracking loop are proposed. Simply adjusting the phase detection scheme embedded in the digital loop filter, the path mismatch in the conventional ILCDR is continuously detected and compensated.

Chapter 6 summarizes the proposed works and concludes this dissertation.

Chapter 2

Background on Injection-Locked Oscillator (ILO)

2.1 Injection-Locking Phenomenon

Injection locking is a physical phenomenon that can occur when an oscillator interferes with another clocking source at the very close frequency. If the coupling strength is strong enough and the two frequencies are almost the same, the input signal can capture the original clocking source. There are several natural examples illustrating injection locking: pendulum clocks on the same walls and synchronization of the metronomes on the flexible material as illustrated in Fig. 2.1 [1]–[2]. In this example, the four metronomes have almost the same oscillation frequency; they could have slightly different frequency due to the manufactory mismatch. At first, individual metronomes are initiated by hand; they have different

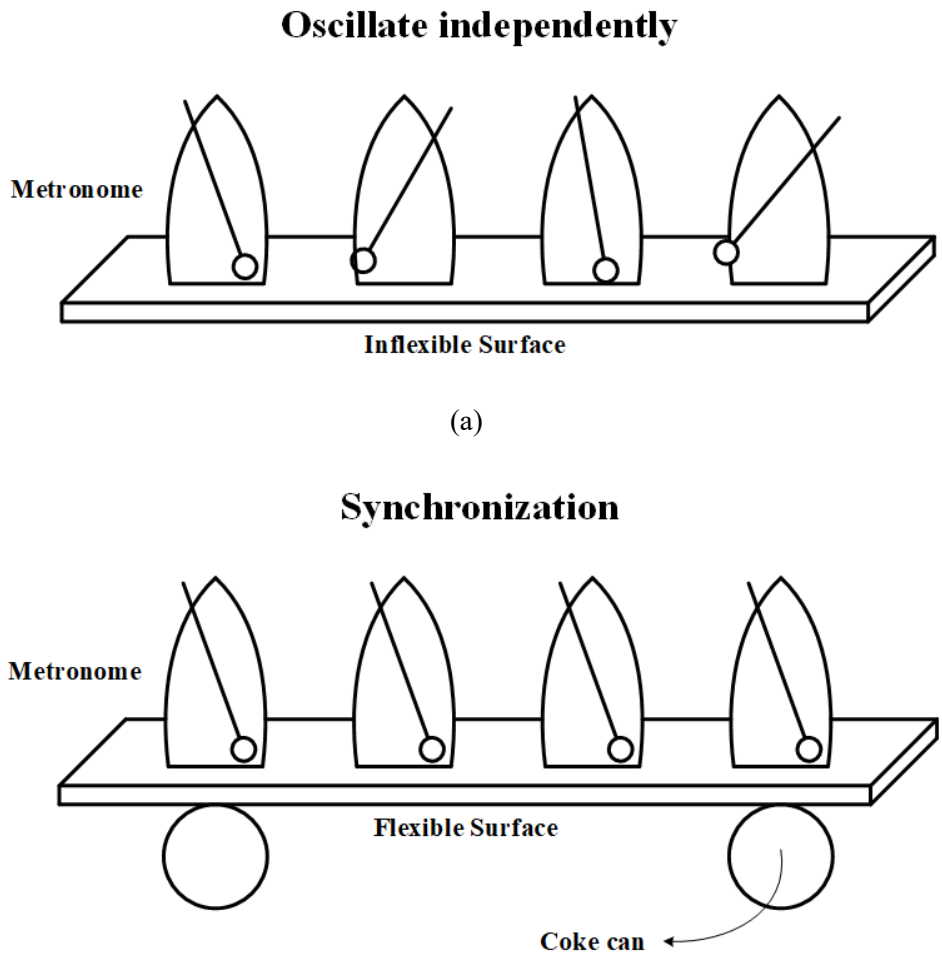


Fig. 2.1 Several metronomes placed on the (a) rigid and (b) soft surface.

phase and frequency as shown in Fig. 2.1(a). After the initialization, the rigid material is replaced to the flexible one using the coke can under the plate as illustrated in Fig. 2.1(b). Since the surface in Fig. 2.1(b) is versatile, the metronomes start to communicate with each other. After some time, they finally achieve the synchronized state, showing same phase and frequency.

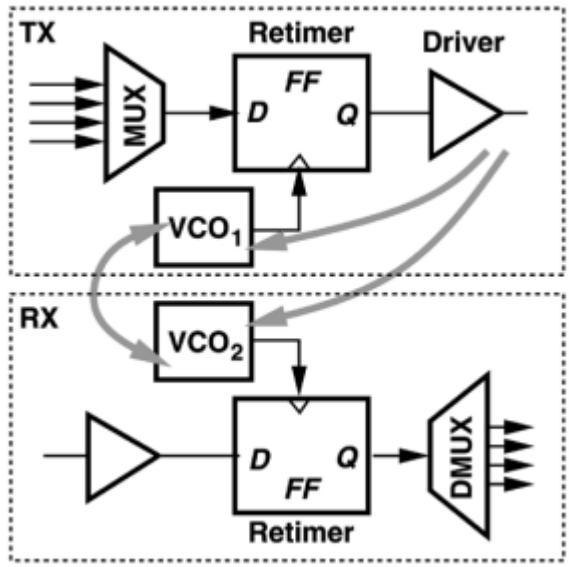


Fig. 2.2 An example of injection pulling in broadband transceiver reported in [16].

These situations could be performed on purpose like Fig. 2.1(b), or it could happen in an unwanted manner as shown in Fig. 2.2. If it occurred in an unintended way, it is regarded as a noise source. Thus, we have to eliminate the coupling effect between the signals consuming considerable cost. However, if the injection effect is performed in helpful or smart ways, that is, deliberately designed, we could achieve the desired performance (e.g., synchronization) at a relatively low cost.

2.2 Applications

Injection-locking technique has widely been exploited in many applications in the frequency synthesis related works. For instance, it is designed for high-performance clock multiplication [23]–[34], clock recovery for burst-mode operation [37]–[43], high-speed clock division [46]–[51], clock distribution for long-distance buffering [52]–[57], and even the delay elements [58]–[63].

2.2.1 Clock Multiplication

In the clock multiplication, injection-locked oscillators (ILOs) have been good alternatives of the conventional PLLs in the aspect of significant noise suppression. Because of its refreshment of the accumulated noise inherent in the noisy clock as shown in Fig. 2.3, it offers excellent noise performance in comparison to the conventional phase-locked loops especially in case of employing the ring oscillator. Another example of the multiplication of the clock is used in RF application which should synthesize the ultra-high-speed clock over tens of gigahertz. In this type of application, the primary goal of the design is to achieve the frequency, not for the stable operation, thus, minimizing the control circuits which might reduce the operating frequency, it can operate at an ultra-high speed such as over ten gigahertz.

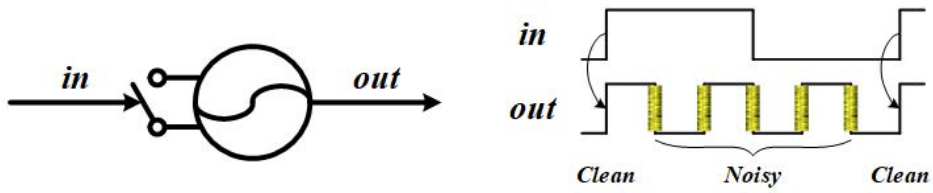
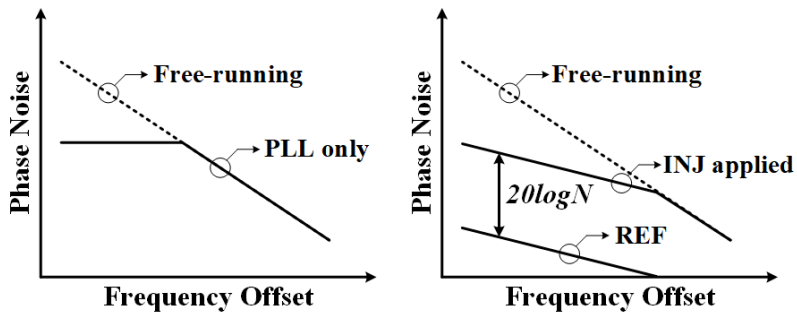


Fig. 2.3 An example of the injection-locked oscillator in clock multiplication and its conceptual timing diagram.



(a) (b)

Fig. 2.4 Phase noise curves of (a) PLL only and (b) injection-applied clock multiplications.

As shown in the Fig. 2.4(a), when the conventional PLL is utilized to synthesize clock, the jitter performance is determined by the loop bandwidth; usually, maximum feasible bandwidth is restricted to one-tenth of the frequency of the reference clock. Thus, the phase noise of the local oscillator should be designed having excellent phase noise, consuming large power dissipation. On the other hand, when the injection operation is applied to the local oscillator, as shown in Fig. 2.4(b), it follows the noise floor of the reference clock below the bandwidth, and the available bandwidth is much wider than the clock multiplication employing the PLL structure only. For this reason, carefully crafted an ILO-based clock synthesizer is a fascinating option concerning both the jitter performance and power consumption.

2.2.2 Clock Recovery

In the embedded clock recovery system, PLL-based CDR is widely adopted for its stable and straightforward implementation. However, PLL-based CDR exhibits very low JTOL in an aspect of the bandwidth due to their loop filter inside the loop. In other words, generally, it cannot tolerate at the very high frequency of the input jitter over tens of the megahertz. For this reason, the method of enhancing the loop bandwidth is developed using a gated voltage-controlled oscillator (GVCO) or ILO applied structure. Thanks to its inherent feature that replace the original edges with the input signal, it naturally achieves a wider bandwidth compared with the PLL-based structures. An ILO-based CDR is adequate for the burst-mode applications or passive optical network (PON) to satisfy the instantaneous phase-locking criteria.

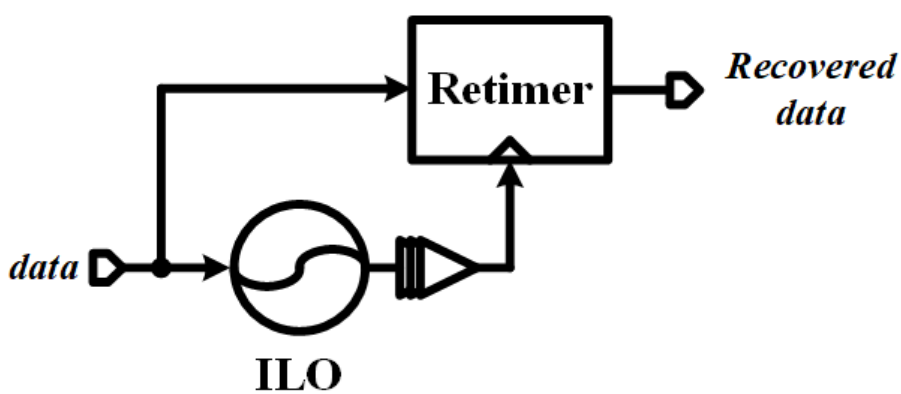


Fig. 2.5 An example of the clock and data recovery from the input data stream using an injection-locked oscillator.

2.2.3 Clock Divider

In the applications that should synthesize very high frequency such as tens of gigahertz, typical methods to divide the oscillation clock is not adequate for a specific technology. Mostly, flip-flop based divider is commonly employed at the front of the division in the PLL application. Because of its internal delay of the flip-flop, it is challenging to achieve higher bandwidth without any help of the circuit techniques. Moreover, even if the internal delay is reduced with specific skills, their power consumption matters in low-power mobile design. For this reason, ILOs are established and implemented in the high-frequency clock synthesizers. The primary design goal in the clock divider using ILO is to secure wide locking range nullifying the compensation circuits for simple design and speed limitation while consuming less power consumption.

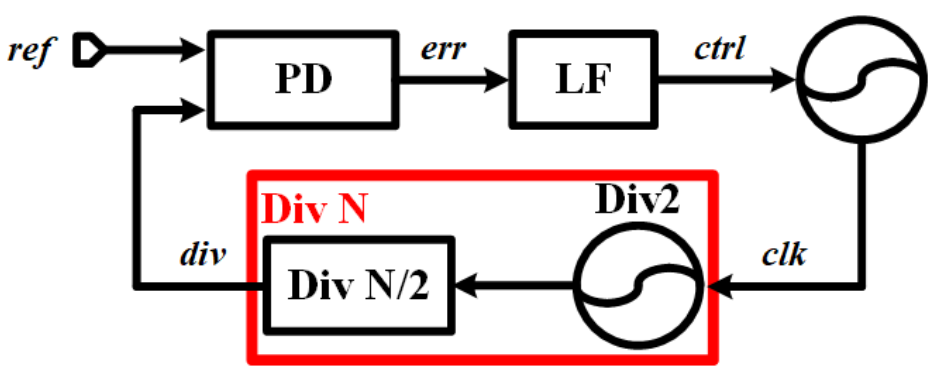


Fig. 2.6 An example of the injection-locked frequency divider in the application of the PLL.

2.2.4 Clock Distribution

In a typical design of the microprocessors and other high-speed applications, clock distribution is one of the challenging missions because of their considerable power consumption and clocking noise. Distributing a clock source from one point to the multiple points is very bothering, and if their arrival time should be almost identical for the timing issue, it is very tough to make it; in a conventional buffered structure such as H-tree, careful design in the layout should be followed. To mitigate the drawbacks in the traditional buffering strategy, ILOs are introduced and applied as shown in Fig. 2.7. If the ILOs are successfully transmitting the clock source just using the metal wires, there is little overhead for the circuit design, and power dissipation is minimized. When the oscillator is deliberately designed in the LC-tuned tank considering the parasitic capacitance of the global network, it could be a great solution that can secure less power dissipation, and high-quality clock, while the skew of the each received local clock is well matched.

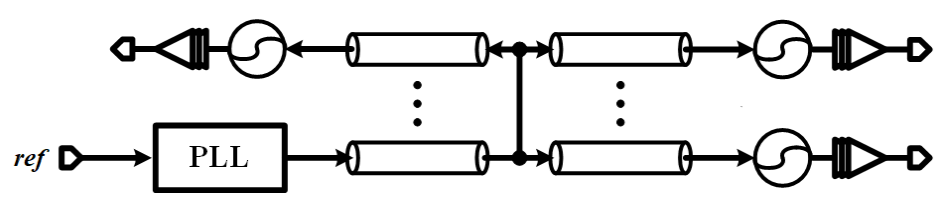


Fig. 2.7 An example of the clock distribution using an injection-locked oscillator.

2.2.5 Clock Deskewing

Since the ILOs have a phase relationship between the input and output signal while frequency deviation exists, the ILOs also can be used for delay element in the system. Since it can make the output phase from –180° to +180° by tuning the free-running oscillator's frequency, theoretically, which will be covered later in Section 2.3, it can be used in the application of delay element as shown in Fig. 2.8. However, it has to be designed carefully because while the locking is failed, it cannot provide stable clocking as we desire. Besides, the jitter transfer function is not consistent with the amount of the frequency deviation that is another research topic.

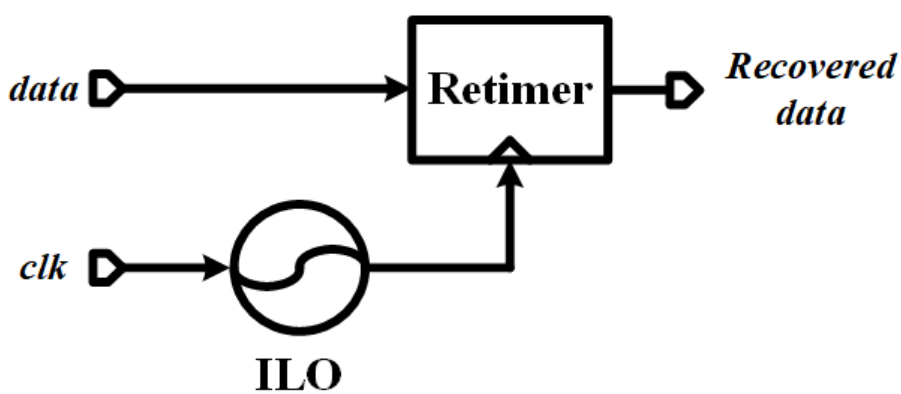


Fig. 2.8 An example of the injection-locked oscillator as a delay element in a source synchronous clock recovery structure.

2.3 Basic Analysis for ILO

2.3.1 Adler's Equation

In 1946, R. Adler first developed the equations for an ILO using a phasor diagram, indicating quick and straightforward insights into the phenomenon discovered in the oscillator as shown in Fig. 2.9 [7]. Since then, numerous researches expanding the theory have been published including K. Kurokawa [9], B. Razavi [16]. Since this equation is straightforward to understand the phenomenon, it is considered the first step to study the injection-locking technique. Originally, phasor diagram is usually developed when analyzing the linear system for sinusoidal waveforms of the same frequency which have an angular phase difference between the two signals. In the analysis of R. Adler, "rotating" phasor is employed for expressing signals with a slightly different frequency between the two signals. There are three assumptions to start the analysis.

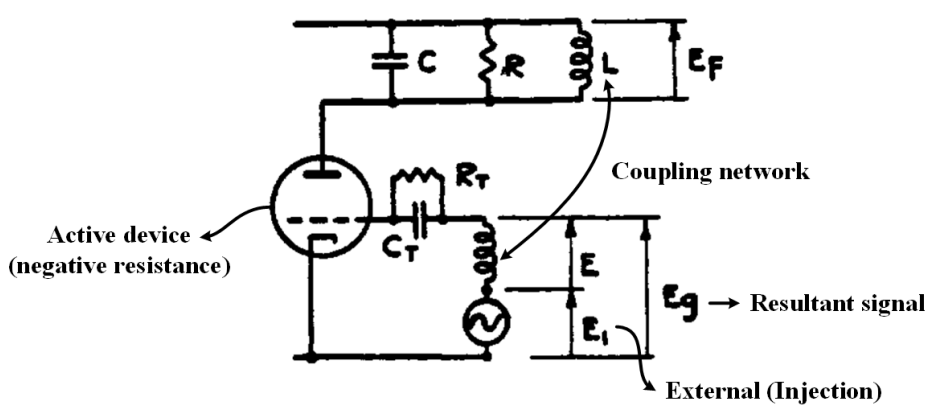


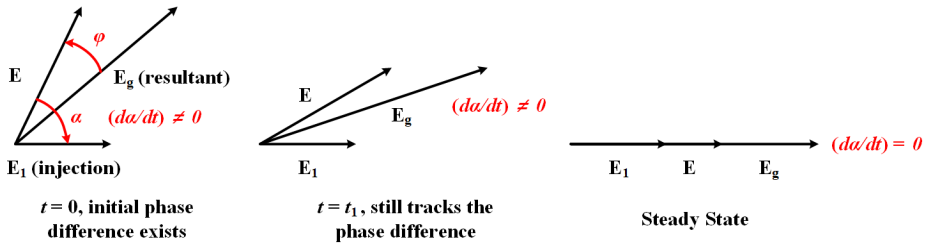
Fig. 2.9 Oscillator circuit developed in [7] with signal descriptions.

$$\omega_0 / 2Q >> \Delta\omega_0 . \tag{2.1}$$

$$T << 1/\Delta\omega_0, \text{ where } T = R_T C_T . \tag{2.2}$$

$$E_1 << E . \tag{2.3}$$

Equation (2.1) denotes that the injection frequency is very similar to the free-running frequency of the oscillator. In other words, this analysis assumed the case while the injection successfully captures the oscillator clock. Also, an amplitude fluctuation due to the injection operation is ignored assuming the amplitude control mechanism is very fast as in (2.2). Lastly, the analysis in this paper focuses on the weak injection as in (2.3). With the three assumptions and introducing the concept of the rotating phasor diagram, the injection phenomenon can be explained. In Fig. 2.10, an example of the injection when the free-running frequency equals the injection frequency, which is the most straightforward case. In Fig. 2.10(a), since the initial phase is not the same between the two signals, the output phase shift exists as $\varphi(t=0)$. At the time t_1 after that, the injection adjust the original signal, but not in the steady state, the output phase shift still exist, not zero as illustrated in Fig. 2.10(b). Finally, at the steady state, there is no phase difference between the two signals because of the zero frequency deviation as in Fig. 2.10(c). Expanding this observation to the case of non-zero frequency offset with the three assumptions (2.1), (2.2), and (2.3), the general equation can be derived using the rotating phasor diagram as in Fig. 2.9(a).



(a) (b) (c)

Fig. 2.10 A description of the injection-locking using rotating phasor diagram when the injection (a) starts, (b) is tracking, and (c) captures the original signal entirely while the frequency deviation is zero.

$$\sin\varphi = \frac{E_1}{Eg}\sin(-\alpha) = -\frac{E_1\sin\alpha}{\sqrt{E_1^2 + E^2 + 2E_1E\cos\alpha}} \approx -\frac{E_1}{E}\sin\alpha\,. \qquad (2.4)$$

Under the weak injection, $E_1 << E$, $\varphi << 1$, $\sin\varphi \approx \varphi$. Therefore, the following equation is derived.

$$\varphi = -\frac{E_1}{E}\sin\alpha\,. \qquad (2.5)$$

Also, using the phase relationship of the resonant RLC circuits as shown in Fig. 2.11 with the assumption of the equation (2.1), the following equations are derived.

$$\varphi = \frac{d\varphi}{d\omega}(\omega - \omega_0) = \frac{d\varphi}{d\omega}(\omega - \omega_1 - \omega_0 + \omega_1) = \frac{d\varphi}{d\omega}(\Delta\omega - \Delta\omega_0)\,. \qquad (2.6)$$

Moreover, by the definition of the angular frequency in the rotating phasor diagram in Fig. 2.10(a), $\Delta\omega$ is expressed as

$$\Delta\omega = \frac{d\alpha}{dt}\,. \qquad (2.7)$$

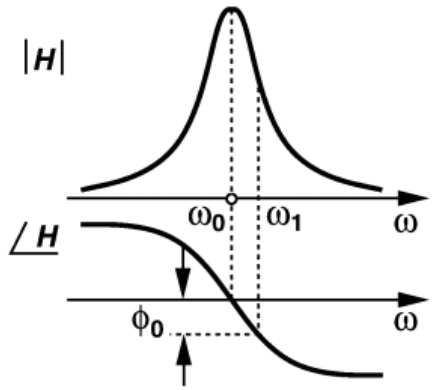


Fig. 2.11 Magnitude and phase versus angular frequency illustrating off-resonant frequency [16].

Combining (2.6) and (2.7),

$$\varphi = \frac{d\varphi}{d\omega}(\Delta\omega - \Delta\omega_0) = \frac{d\varphi}{d\omega}(\frac{d\alpha}{dt} - \Delta\omega_0). \tag{2.8}$$

For an RLC tank, the impedance is calculated as

$$Z = R \,||\, sL \,||\, \frac{1}{sC} = \frac{j\omega RL}{j\omega L + R - \omega^2 RLC}. \tag{2.9}$$

Its phase is calculated as

$$\begin{aligned} \angle Z &= \frac{\pi}{2} - \tan^{-1}\left(\frac{\omega L}{R - \omega^2 RLC}\right) = \frac{\pi}{2} - \tan^{-1}\left(\frac{\omega L}{R}\frac{{\omega_0}^2}{{\omega_0}^2 - \omega^2}\right) \\ &= \frac{\pi}{2} - \tan^{-1}\left(\frac{1}{Q}\frac{\omega_0}{2(\omega_0 - \omega)}\right) = \tan^{-1}\left(\frac{2Q}{\omega_0}(\omega_0 - \omega)\right) \end{aligned}. \tag{2.10}$$

Thus,

$$\tan(\angle Z) = \frac{2Q}{\omega_0}(\omega_0 - \omega)\,. \tag{2.11}$$

In the notation of the phasor diagram in Fig. 2.10(a), the phase of the RLC tank can be expressed as $\angle Z = -\varphi$. Also, using the assumption of $\varphi << 1$, $\tan\varphi$ is approximated to φ ($\tan\varphi \approx \varphi$). Thus, the equation of (2.11) can be re-derived as

$$\varphi = \frac{2Q}{\omega_0}(\omega - \omega_0)\,. \tag{2.12}$$

So its first derivative with respect to the angular frequency ω is

$$\frac{d\varphi}{d\omega} = \frac{2Q}{\omega_0}\,. \tag{2.13}$$

Combining (2.5) and (2.8),

$$-\frac{E_1}{E}\sin\alpha = \frac{d\varphi}{d\omega}\left(\frac{d\alpha}{dt} - \Delta\omega_0\right). \tag{2.14}$$

Substituting (2.13) to the (2.14),

$$\frac{d\alpha}{dt} = -\frac{E_1}{E}\frac{\omega_0}{2Q}\sin\alpha + \Delta\omega_0\,. \tag{2.15}$$

From the equation (2.15), lock range of the harmonic oscillator can be calculated in the steady state while instantaneous phase drift with respect to the time settles. Since the left term in (2.15) is zero in the steady state, the following relationship is obtained as

$$\sin\alpha = 2Q\frac{E}{E_1}\frac{\Delta\omega_0}{\omega},\ |\sin\alpha| = |2Q\frac{E}{E_1}\frac{\Delta\omega_0}{\omega}| \le 1,. \tag{2.16}$$

$$|\frac{\Delta\omega_0}{\omega}| \le \frac{1}{2Q}\frac{E_1}{E}. \tag{2.17}$$

From the locking range in (2.17), it can be induced that as the injection strength is higher and the quality-factor Q gets smaller, the locking range increases. Equation (2.15) is expressed in the simplified form as

$$\frac{d\alpha}{dt} = -B(\sin\alpha - K),\ B = \frac{E_1}{E}\frac{\omega_0}{2Q},\ K = 2Q\frac{E}{E_1}\frac{\Delta\omega_0}{\omega_0}. \tag{2.18}$$

With the aid of the CAD tool of MATHEMATICA, the results are easily obtained as illustrated in Fig. 2.12 when the frequency-deviation ω_0 is zero. As shown in Fig. 2.12, regardless of the initial phase $\alpha(0)$, its final value at the steady state is zero. In the case of non-zero frequency deviation ($\omega_0 \neq 0$), there are two cases of injection-locked and pulled situations. Its criteria are determined whether the K exceed one or not as derived in equation (2.17). While injection-locked, its output phase is illustrated in Fig. 2.13(a), showing the static phase shift between the two signals, in other words, at the steady state, its resultant output phase shift is not zero compared with the situation of zero frequency deviation as shown in Fig. 2.12. Fig. 2.13(b) shows the results while failed to injection locking, that is, injection pulling, thus it looks unstable or drifting.

```
sol = DSolve[{a'[t] == -B * (Sin[a[t]]), a[0] == C}, a[t], t]
```

$$\left\{\left\{a[t] \to 2\,\text{ArcCot}\left[e^{Bt}\,\text{Cot}\left[\frac{C}{2}\right]\right]\right\}\right\}$$

```
tab = Table[a[t] /. sol[[1]] /. {B → 10^6, C → c}, {c, -3 * Pi / 4, 3 * Pi / 4, Pi / 4}];

Plot[Evaluate[tab], {t, 0, 0.00001}, PlotRange → {-Pi, Pi}]
```

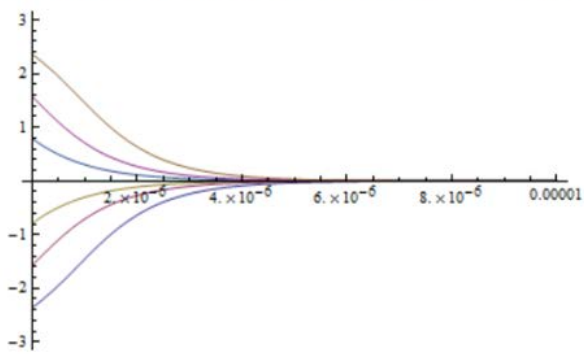


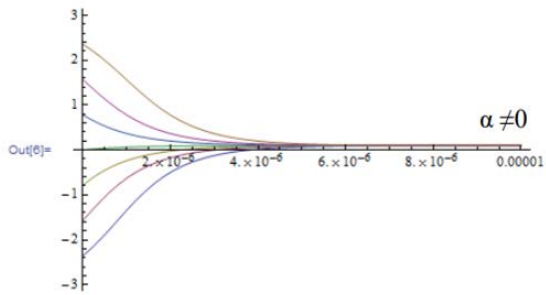
Fig. 2.12 Various output results of equation (2.18) with different initial phase shifts while the frequency offset is zero.

```
In[4]:= sol = DSolve[{a'[t] == -B * (Sin[a[t]] - K), a[0] == C}, a[t], t]

Out[4]= {{a[t] → 2 ArcTan[(1 - Sqrt[-1 + K^2] Tan[1/2 (-B Sqrt[-1 + K^2] t - 2 ArcTan[(-Sqrt[-1+K^2] + K Sqrt[-1+K^2] Tan[C/2]) / (-1+K^2)])]) / K]}}

In[5]:= tab = Table[a[t] /. sol[[1]] /. {B → 10^6, K → 0.1, C → c}, {c, -3*Pi/4, 3*Pi/4, Pi/4}];

In[6]:= Plot[Evaluate[tab], {t, 0, 0.00001}, PlotRange → {-Pi, Pi}]
```

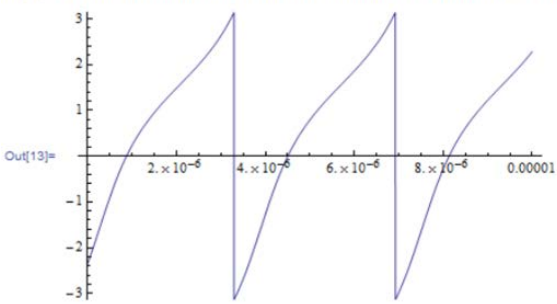


Out[6]=

(a)

```
In[12]:= tab2 = Table[a[t] /. sol[[1]] /. {B → 10^6, K → 2.0, C → c}, {c, -3*Pi/4, -3*Pi/4, 0}];

In[13]:= Plot[Evaluate[tab2], {t, 0, 0.00001}, PlotRange → {-Pi, Pi}]
```



Out[13]=

(b)

Fig. 2.13 General output-phase-shift results with various initial phase shifts when (a) injection locked and (b) injection pulling.

2.3.2 Phase Noise Analysis

In [14], the noise transfer function of an ILO is presented regarding the noise sources in the specific application of the clock multiplication of *N*. There exist two noise sources in the ILOs; the oscillator itself and the injected signal. The accumulated noise of the oscillator is replaced with the injected signal. Thus, the relationship between the two noise sources can be derived using some assumptions and the understanding of the injection operation. This analysis is carried out while the frequency deviation between the two signals is ideally zero, and only the phase noise is considered. Even [14] does not include the effect of the frequency offset between the two signals, its derivation of the noise relationship is very meaningful to investigate the transfer function of the ILO-based clock multiplication in the frequency domain. As illustrated in Fig. 2.14, the instantaneous phase difference between the local oscillator and the injected signal is represented as

$$\theta_e[n] = \theta_{inst\_vco}(nT_r^-) - N\theta_{ref}(nT_r). \tag{2.19}$$

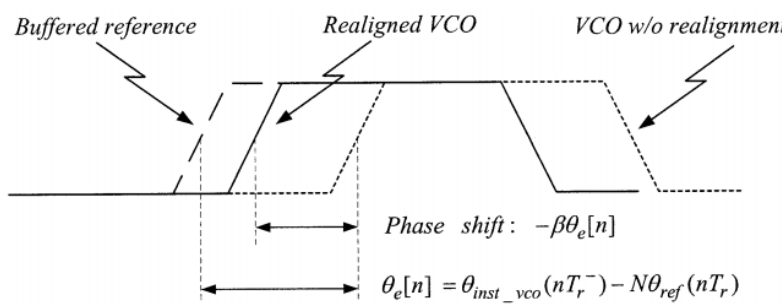


Fig. 2.14 Timing diagram before and after the injection affect the original clock edge reported in [14].

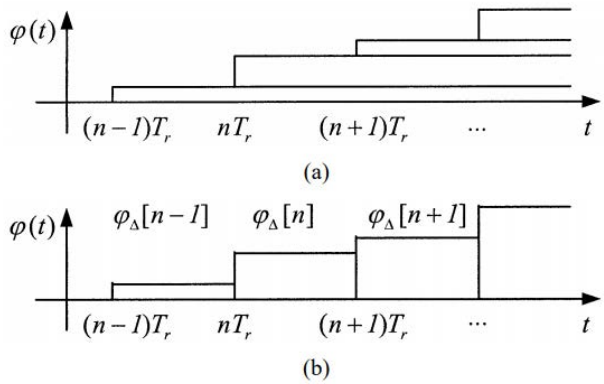


Fig. 2.15 The extra phase shift due to the injection operation (a) shown using the series phase steps and (b) impulse train employing hold operation reported in [14].

Here, T_r is the period of the reference clock and nT_r^- represents the time instant just before the injection is applied. After the injection happens, the amount of phase shift is defined as $-\beta\theta_e[n]$ assuming a linear relationship between the input and the output phase. From this observation, the phase noise of the instantaneous oscillator can be given combining the noise from the oscillator itself and the extra noise portion from the injection operation:

$$\theta_{inst\_vco}(t) = \theta_{vco}(t) + \varphi(t). \tag{2.20}$$

Also, since the oscillator is originally phase integrator, each phase realignment can be expressed as the sum of a step increment to the oscillator phase noise as shown in Fig. 2.15:

$$\varphi(t) = -\beta \sum_{n=-\infty}^{\infty} \theta_e[n] \cdot u(t - nT_r). \tag{2.21}$$

By introducing the impulse train and "hold" operation, the following relationship is derived as

$$\varphi_{\Delta}[n]-\varphi_{\Delta}[n-1]\equiv-\beta\theta_{e}[n]\,. \tag{2.22}$$

Combining (2.21) and (2.22) gives

$$\varphi(t)=\sum_{n=-\infty}^{\infty}\varphi_{\Delta}[n]\cdot h_{hold}(t-nT_{r})\,. \tag{2.23}$$

Taking the Fourier transform of (2.23),

$$\varphi(j\omega)=T_{r}e^{-j\omega T_{r}/2}\cdot\frac{\sin(\omega T_{r}/2)}{\omega T_{r}/2}\cdot\varphi_{\Delta}(z),\ \text{where } z=e^{j\omega T_{r}}\,. \tag{2.24}$$

Here, $\varphi_{\Delta}(z)$ is the z transform of $\varphi_{\Delta}(n)$.

Combining (2.19) and (2.22),

$$\varphi_{\Delta}[n]-\varphi_{\Delta}[n-1]=-\beta(\theta_{vco}[n]+\varphi_{\Delta}[n-1]-N\theta_{ref}[n])\,. \tag{2.25}$$

Taking the z transform of (2.24) and solving for the $\varphi_{\Delta}(z)$,

$$\varphi_{\Delta}(z)=\frac{-\beta}{1+(\beta-1)z^{-1}}\theta_{vco}(z)+\frac{N\beta}{1+(\beta-1)z^{-1}}\theta_{ref}(z)\,. \tag{2.26}$$

Combining (2.20), (2.24), and (2.26) gives

$$\theta_{inst\_vco}(j\omega)=\theta_{vco}(j\omega)H_{rl}(j\omega)+\theta_{ref}(j\omega)H_{up}(j\omega) \tag{2.27}$$

where

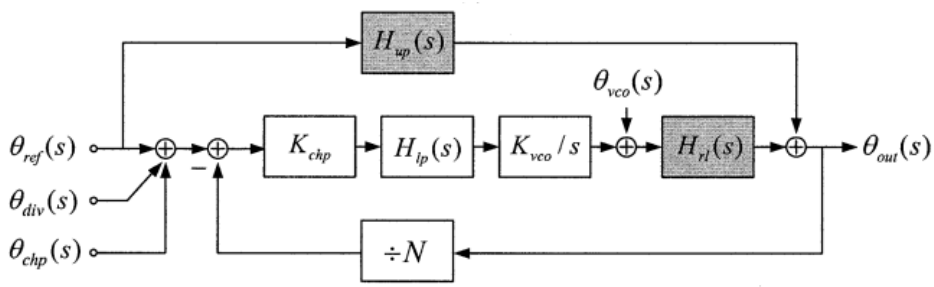


Fig. 2.16 Phase noise model of the injection-locked PLL including the effect of the realignment and the up-conversion of the reference noise reported in [14].

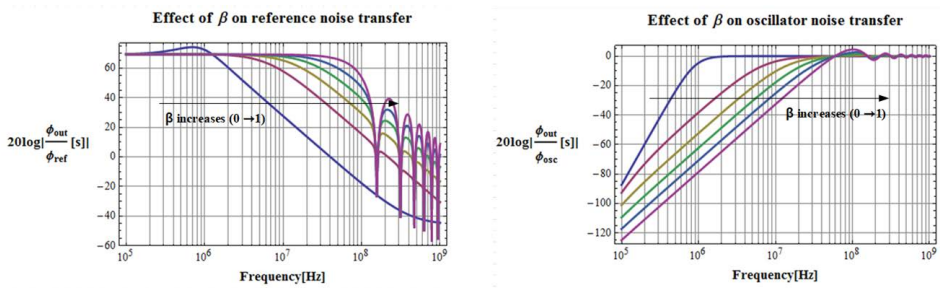
$$H_{rl}(j\omega) = 1 - \frac{\beta}{1+(\beta-1)e^{-j\omega T_r}} \cdot e^{-j\omega T_r/2} \cdot \frac{\sin(\omega T_r/2)}{\omega T_r/2} \tag{2.28}$$

and

$$H_{up}(j\omega) = \frac{N\beta}{1+(\beta-1)e^{-j\omega T_r}} \cdot e^{-j\omega T_r/2} \cdot \frac{\sin(\omega T_r/2)}{\omega T_r/2} \cdot \tag{2.29}$$

The transfer function $H_{rl}(j\omega)$ represents the effect of the phase realignment and $H_{up}(j\omega)$ represents the up-conversion of the reference noise.

Fig. 2.16 shows the phase noise model of the injection-locked PLL containing the transfer function of $H_{rl}(j\omega)$ and $H_{up}(j\omega)$. From the block diagram with the equations of (2.28) and (2.29), the output noise functions of the reference and oscillator are visualized in Fig. 2.17 with different realignment factor. Fig. 2.18 shows the noise suppression regarding the realignment factor when the oscillator noise is modeled as 1/s. As the injection strength increases, the amount of noise suppression also increases since the reference noise is extremely clean ($\theta_{ref} = 0$).



(a) (b)

Fig. 2.17 Noise transfer function of (a) the reference and (b) the oscillator with various realignment factor.

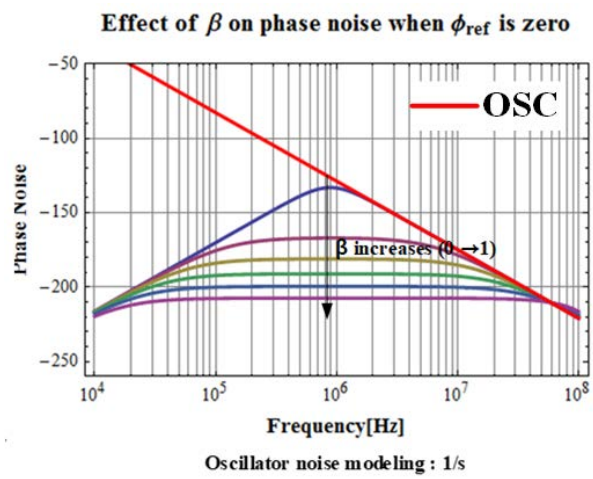


Fig. 2.18 Effect of realignment factor on phase noise when the reference noise is zero with different realignment factor.

2.4 Design Challenges

According to the usage of the ILOs, the design challenges are slightly different. For instance, if the ILOs are utilized as a clock de-skewing element, the frequency offset is deliberately generated to make the desired output phase shift. Except for the application of the clock deskewing, all other circuits employing the ILOs should be designed to have a minimum frequency deviation for better performance. In this thesis, we focus on the calibration method of the frequency difference between the injected signal and the local free-running oscillator in the PLL-based ILO structure. If the difference between the two signals is not well matched, performance degradation is inevitable. In PLL design, considerable deterministic noise is caused, deteriorating the spur performance as shown in Fig. 2.19. Similarly, in CDR application, the generated deterministic noise reduces the timing margin of the data sampler, degenerating the tolerance for the consecutive identical digits (CIDs).

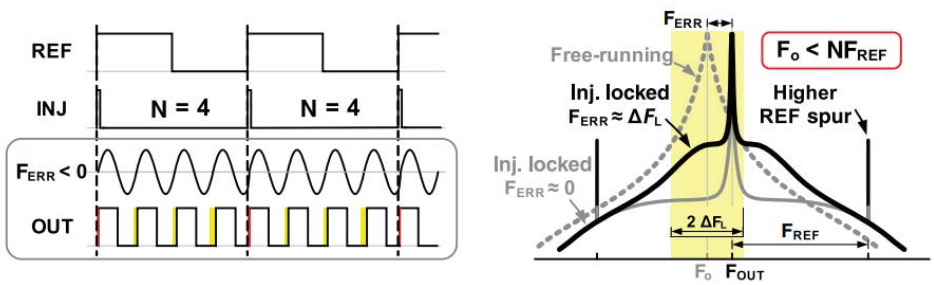


Fig. 2.19 An example of the clock multiplication when the frequency deviation exists reported in [28].

2.5 Recent Works

2.5.1 Clock Multiplication

There are several ways reported in recent papers to solve the design challenges mentioned in Section 2.4. Sacrificing the phase information of the injection edge as depicted in Fig. 2.20(a), so-called gated pulse in [28], the phase detector inside the closed loop can detect the path mismatch between the two-phase align mechanism. The timing diagram in Fig. 2.20(b) offers detailed operation of this scheme. Since the injection pulse is gated once every four cycles, the accumulated frequency error is accumulated over N cycles; thus, its error between the two signals or the two paths can be detected, and the injection timing is compensated with the zero crossing of the signal which is the optimum injection point.

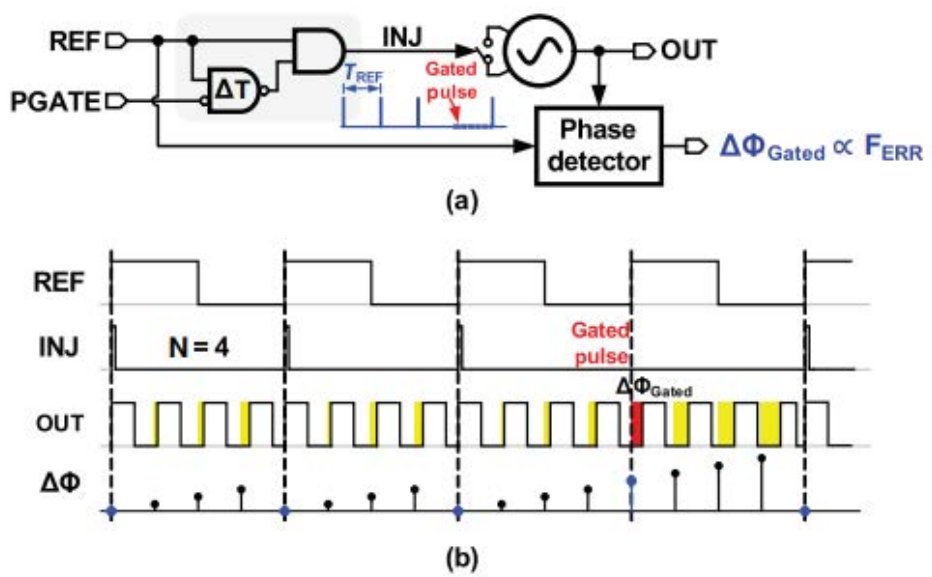


Fig. 2.20 (a) The concept of the pulse gating and (b) the timing diagram when the multiplication factor is four, and the gating rate is one fourth in [28].

The strategy suggested in [28] is very intuitive and straightforward, but, it has to sacrifice the high-quality of the reference to recognize it. In other words, it cannot achieve the maximum bandwidth compared with the scheme of full utilization of the reference clock. Next, nullifying the conventional phase detection in the PLL structure, the injection refreshes the local oscillator every cycle by employing the replica delay element as shown in Fig. 2.21 [30]. Assuming the same delay between the two elements, it can successfully discriminate the frequency deviation, the reference, and the local oscillator. However, it cannot confirm the perfect match because of the layout issues. In [30] as shown in Fig. 2.21, it compensates the path mismatch every negative edge of the reference rate, showing good reference spur level of –65 dBc/Hz.

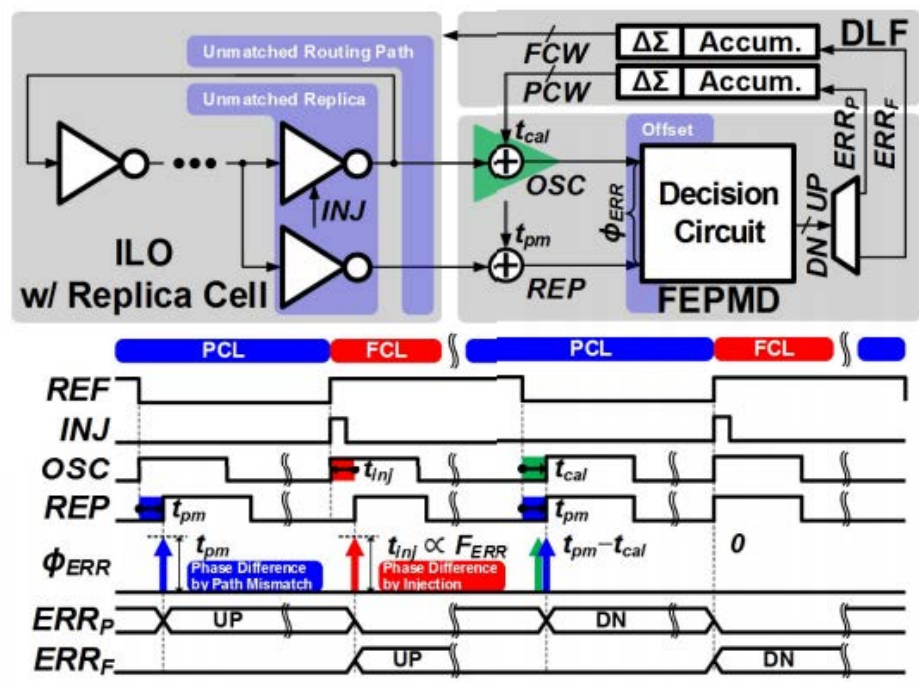


Fig. 2.21 Block diagram of the replica-delay scheme and its timing diagram adjusting the frequency of the oscillator and path mismatch between the replica cells reported in [30].

2.5.2 Clock Recovery

In Fig. 2.22, the PLL loop is present to make the similar frequency with the target frequency, in this example for 20 Gb/s data rate, 20 GHz [39]. The control voltage from the replica PLL is forwarded to the main ILO, VCO_1, then the input data stream is injected through the pulse generator and the phase align is achieved. This scheme works, but, the hardware overhead is enormous, resulting in large silicon area and power dissipation. Also, the mismatch between the reference clock and data rate is not zero, and the layout issue of the replica scheme should be solved to be more stable or robust. Moreover, although phase align is achieved from the input data stream, the timing margin of the data sampler in Fig. 2.22 is not ensured to have a maximum value of 0.5 UI (unit interval).

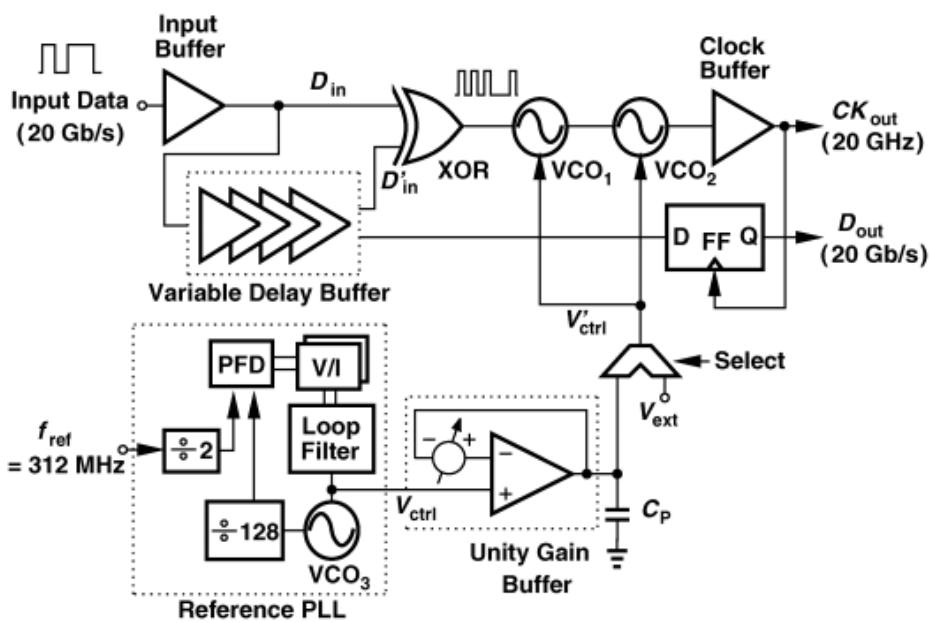


Fig. 2.22 Block diagram of the replica-based ILCDR with reference PLL published in [39].

Since the proposed structure in [39] has a dual loop to generate the frequency of the local clock, and the inherent mismatch issues cannot be avoided, there have been studied for ILCDRs applying single loop excluding the reference clock [42]–[43]. As an example of such approaches, combining traditional PLL-based architecture with the data injection is present as shown in Fig. 2.23. Unlike the simple combination of the two-phase adjustment operation without further consideration, [43] suggests a new methodology distinguishing the error information whether it is from the phase inequality or the frequency mismatch. In this way, it can control the variable delay line in front of the data sampler and the frequency of the local oscillator simultaneously with minimum hardware additives assisted by the digital control.

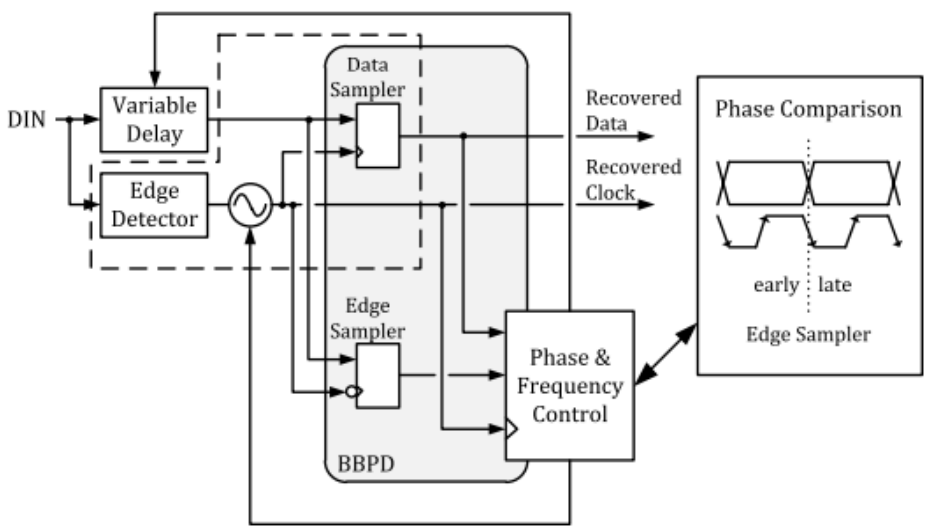


Fig. 2.23 An implementation example of the injection-locked clock and data recovery using the serial output of the phase detector to distinguish the error source [43].

Chapter 3

ILPLL with Injection-Timing Tracking

3.1 Overview

Conventional ring oscillators exhibit poor phase noise performance compared with LC oscillators. For this reason, a ring oscillator-based (RO-based) phase-locked loop (PLL) is designed to have a wide bandwidth to filter the considerable phase noise of the oscillator. However, the maximum feasible bandwidth is restricted to approximately one-tenth of the frequency of the reference clock. Even if they have poor jitter performance, RO-based PLLs have generally been explored because of their wide tuning range and small silicon area. To combine the advantages of RO-based PLLs with good jitter performance, injection-locked oscillators (ILOs) have widely been researched in many clock multipliers thanks to their remarkable jitter performance and simple implementation [23]–[34]. Fig. 3.1 shows the trend of a

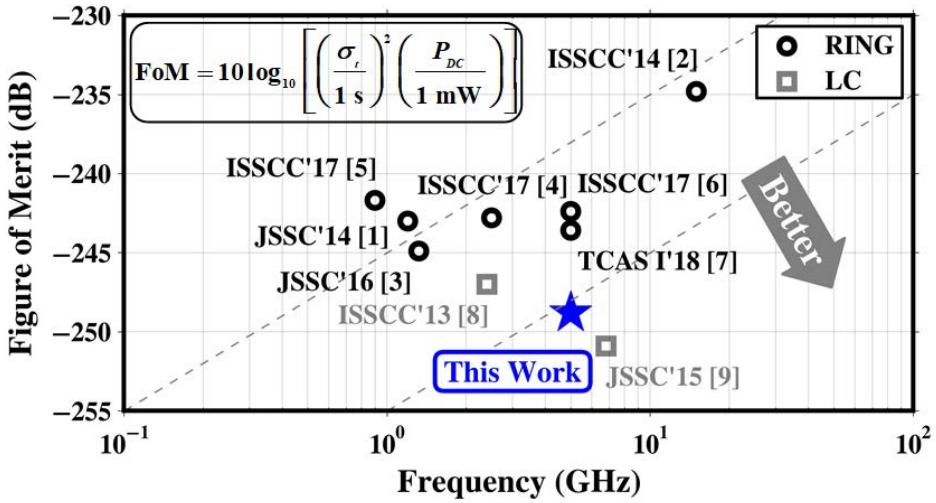


Fig. 3.1 The trend of the figure of merit (FoM) versus frequency by choice of oscillator type in recent published ILPLLs.

figure of merit (FoM) versus frequency by choice of oscillator types in recent injection-locked PLLs (ILPLLs) [24], [26]–[33]. As expected, LC-based ILPLLs [24], [28] exhibit better jitter performance than RO-based ones. The RO-based ILPLL proposed in this work, however, shows a FoM comparable to LC-based ILPLLs and outstanding power efficiency. Thus, carefully crafted RO-based ILPLLs could be an attractive choice in clock multiplication thanks to the ease of design and smaller active area than LC-based ILPLLs.

Although ILPLLs are appealing regarding noise suppression, a robust operation is not ensured unless the injection timing is precisely controlled. Since the reference clock is directed to a phase detector, and at the same time injected into the oscillator, the two paths must be designed carefully since the phase of the oscillator might have already been adjusted by injection before the phase detector catches the phase error,

nullifying the operation of the PLL or vice versa. To resolve the timing issue in conventional ILPLLs, several calibration methods have been reported in [23]–[30], [33], and [34].

In this work, to resolve the timing issue in ILPLL, an injection-timing calibrator that is focused on low power consumption is proposed, and a robust operation thereof is obtained over the process, supply voltage, and temperature (PVT) variations.

3.2 Analysis of Injection-Timing Effect

3.2.1 Frequency Error by Injection-Timing Mismatch in ILPLL

Fig. 3.2 shows a conventional ILPLL that includes delay elements in front of the phase detector. In this scheme, the timing mismatch is defined as $\Delta t = (\tau_{inj} + \tau_{clk}) - \tau_{ref}$. Once the feedback loop including the injection path locks, the phase detector cannot detect whether it locked to the desired timing or not. In [10], injection strength (β) is introduced as the ratio of the output phase shift to the input phase deviation and the phase noise model of the oscillator at a fixed frequency (f_{osc}) is presented without considering the loop. However, when the loop is closed, f_{osc} is varied depending on Δt.

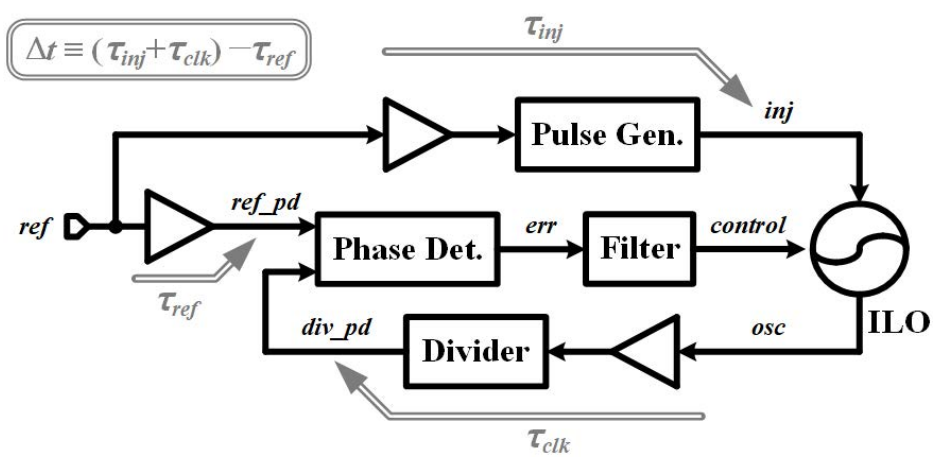
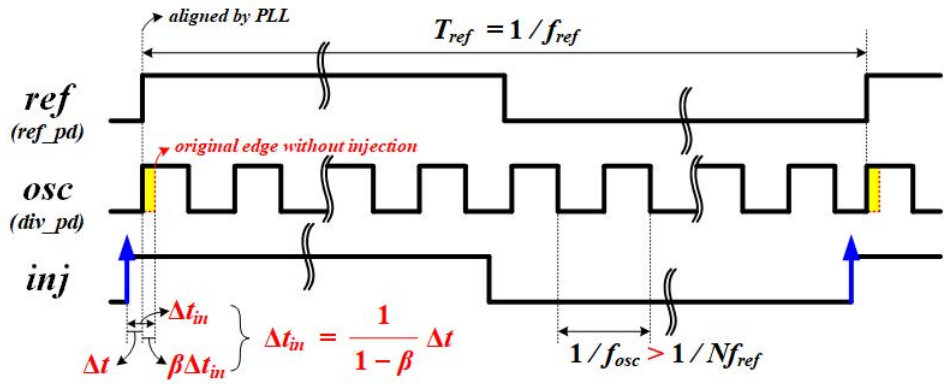
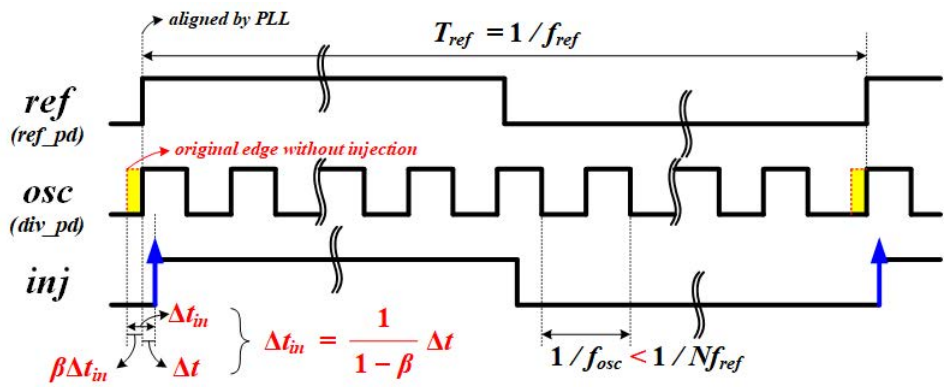


Fig. 3.2 Block diagram of conventional ILPLL with delay elements.



(a)



(b)

Fig. 3.3 Timing diagram of conventional ILPLL with Δt being (a) positive and (b) negative assuming τ_{ref} and τ_{clk} are zero.

Fig. 3.3 illustrates the timing diagram with fixed Δt being positive and negative assuming τ_{ref} and τ_{clk} are zero when the ILPLL achieves the phase lock in the steady state. Since the closed loop incorporating the PLL settles, the input phase error of the bang-bang phase and frequency detector (BBPFD) is zero on average regardless of the injection timing. The aligned phase of the oscillator (*osc*) is already changed by the reference injection, and the amount of phase shift due to the injection effect can be obtained from inverse operation of the equation in [14]. It is noted that the phase shift is not directly expressed as a function of Δt since the phase of *osc* in Fig. 3.3(a) is already disturbed by the injection as mentioned. Thus, we introduce a new variable to express the output phase shift. The new variable is denoted as Δt_{in}, and it means the input phase deviation in the definition of the injection strength [14]. Subsequently, its output phase shift is $\beta\Delta t_{\text{in}}$, and according to the timing relation demonstrated in Fig. 3, the following equation is derived as

$$\Delta t + \beta\Delta t_{in} = \Delta t_{in} . \tag{3.1}$$

Consequently, Δt_{in} can be written as

$$\Delta t_{in} = \frac{1}{1-\beta}\Delta t \tag{3.2}$$

, where $0 \le \beta < 1$.

Using the relationship between Δt and Δt_{in}, and the additional phase shift, f_{osc} is derived as a function of Δt as

$$\left(\beta\Delta t_{in} + \frac{1}{f_{osc}}\right) + \frac{N-1}{f_{osc}} = \frac{1}{f_{ref}} \quad . \tag{3.3}$$

The first term represents the period disturbed by the injection at the N-th cycle. Subsequently, without the injection operation over ($N-1$) cycles, the oscillator runs freely having a period of ($1/f_{osc}$); the second term in (3.3). Since we assumed that the ILPLL operates at the steady state, the sum of these two terms is identical to the period of the reference clock, $1/f_{ref}$. Then, f_{osc} is solved as a function of Δt_{in} as

$$f_{osc} = \frac{Nf_{ref}}{1-\beta f_{ref}\Delta t_{in}}. \tag{3.4}$$

We already have a relationship between Δt and Δt_{in} in (3.2), substituting (3.2) to (3.4),

$$f_{osc} = \frac{(1-\beta)Nf_{ref}}{(1-\beta)-\beta f_{ref}\Delta t}. \tag{3.5}$$

Equation (3.5) represents the frequency of the free-running oscillator is a function of the injection strength and the path mismatch in the ILPLL structure. When the injection strength is zero, in other words, injection is not applied to the oscillator, f_{osc} equals the Nf_{ref}, which is the target frequency of the ILPLL. Moreover, if the timing mismatch is ideally zero, f_{osc} is also equaled to the Nf_{ref}, which means there is no deterministic noise even the injection operation continuously modulates the phase of the local oscillator.

3.2.2 Deterministic Noise for Injection Timing

In the condition that the free-running frequency of the oscillator, f_{osc}, is within the locking range of the ILO, the injection signal captures the free-running oscillator. Considering the phase error is accumulated during ($N-1$) cycles and, the injection induces an additional phase shift periodically to achieve the phase lock, the average frequency of the output signal, f_{out}, equals to Nf_{ref}. Assuming the offset in the instantaneous output period is approximately αT_{out}, deterministic jitter (DJ) and reference spur ($Spur$) are derived as a function of the frequency error (Δf), where α is $\Delta f / Nf_{ref}$ [23].

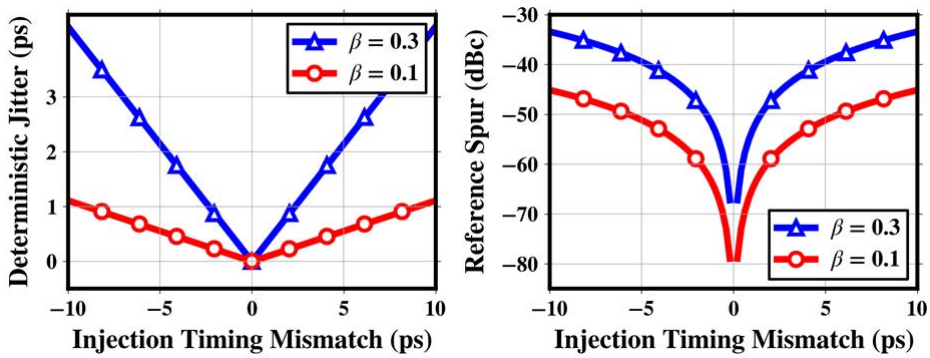
$$DJ \approx (N-1)\alpha T_{out} \approx \alpha T_{ref} . \tag{3.6}$$

$$Spur \approx 20\log_{10}(DJ / T_{out}) \approx 20\log_{10}(\alpha N) . \tag{3.7}$$

Because we made a relationship between f_{osc} and Δt in (3.1), the equations of DJ and $Spur$ can be re-derived concerning Δt. Substituting (3.1) into the equations, the following formulas are derived and visualized in Fig. 3.4(a) and Fig. 3.4(b), respectively.

$$DJ \approx \alpha T_{ref} = \frac{\Delta f}{Nf_{ref}^2} = \frac{f_{osc} - Nf_{ref}}{Nf_{ref}^2} = \frac{\beta\Delta t}{(1-\beta) - f_{ref}\beta\Delta t} . \tag{3.8}$$

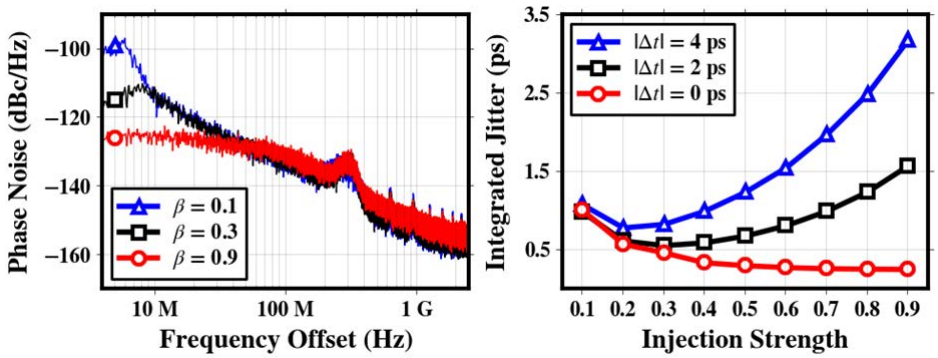
$$Spur \approx 20\log_{10}(\alpha N) = 20\log_{10}\left(\frac{Nf_{ref}\beta\Delta t}{(1-\beta) - f_{ref}\beta\Delta t}\right). \tag{3.9}$$



(a) (b)

Fig. 3.4 (a) Deterministic jitter and (b) reference spur calculated from the equations of (2) and (3) as a function of injection-timing mismatch (Δt) for two different injection strengths (β = 0.1 and β = 0.3) in conventional ILPLL. In this example, N = 16 and f_{ref} = 312.5 MHz.

In Fig. 3.4, when β is increased, the deterministic jitter is also increased more steeply with respect to the injection-timing mismatch because f_{osc} is much different from the target output frequency, Nf_{ref}, as shown in (3.1). In addition, phase noise performance is degraded by the injection-timing mismatch because of the decreased injection strength which will be covered in next Chapter 4. Therefore, overall jitter performance of the ILPLL hugely depends on the timing mismatch in the ILPLL, which forces continuous tracking mechanism of the mismatch to achieve a significant improvement of the jitter performance.



(a) (b)

Fig. 3.5 (a) Behavioral phase-noise simulations of ILPLL when injection timing is perfectly tuned and (b) calculated jitter as a function of injection strength. In this example, N = 16, f_{ref} = 312.5 MHz, the phase noise of an oscillator is –95 dBc/Hz at 1-MHz offset excluding flicker noise, and phase noise of reference clock is modeled as having a Gaussian random noise of –160 dBc.

Fig. 3.5 shows the behavioral simulations with several different conditions. In this example, N = 16, f_{ref} = 312.5 MHz, the phase noise of an oscillator is –95 dBc/Hz at 1-MHz offset excluding flicker noise, and phase noise of reference clock is modeled as having a Gaussian random noise of –160 dBc. In Fig. 3.5(a), the phase-noise curves are presented when injection timing is perfectly tuned, and three different injection strengths are applied. In this ideal case, β should be selected as large as possible to cut off the phase noise from the oscillator.

However, with the presence of non-zero Δt, blindly increasing injection strength might yield worse jitter performance due to the deterministic jitter and spur as indicated in (3.4) and (3.5). Simulation results are illustrated in Fig. 3.5(b). In this simulation, the integration range includes the reference frequency; thus, the deterministic noise analyzed in (3.4) and (3.5) is considered. As seen in Fig. 3.5(b), although

the optimum injection strength can be determined for the minimum integrated jitter given the timing mismatch, it is impossible to estimate the exact injection timing. In addition, variations of supply voltage and temperature make its estimation difficult as well. Therefore, to achieve the best performance in ILPLL, the injection strength should be chosen as large as possible and a continuous tracking mechanism of the injection timing under PVT variation must be incorporated.

3.3 Proposed ILPLL with Optimum Injection Timing

As analyzed in Section 3.2, injection-timing mismatch impacts jitter performance critically. In this work, by inserting a divider in front of the pulse generator, being similar to a pulse-gating scheme in [28] and [32], one of two edges of the reference clock is skipped to detect the timing discrepancy between two different modulation paths and the delay through the injection path is adjusted to an optimum value with a minimal hardware overhead. Since the proposed scheme extracts the timing error at the rate of the slow reference clock rather than an oscillation clock, it achieves significant power efficiency compared with [26]–[27], [29], and [30].

3.3.1 Half-Edge Injection and Detecting Injection Timing

Fig. 3.6 illustrates the timing diagram where the injection is intentionally omitted every other cycle. The errors from the bang-bang phase and frequency detector (BBPFD) are de-serialized and forwarded as err_{dco} when the injection is enabled and err_{dcdl} when the injection is skipped. Owing to the all-digital PLL (ADPLL) loop adjusting the phase of the oscillator, err_{dco} might settle to zero average even if it has frequency error (Δf). In this figure, err_{dco} is instantaneously zero assuming the loop has an exceptionally high gain for a simple explanation. For $(N-1)$ cycles right after injection is applied, Δf due to Δt is accumulated, and this phase error is detected as err_{dcdl} as highlighted in the gray text box in Fig. 3.7. Because the frequency of injection is $0.5 f_{ref}$, deterministic noises come at this rate and its harmonics, and these results are presented in next Section 3.5.

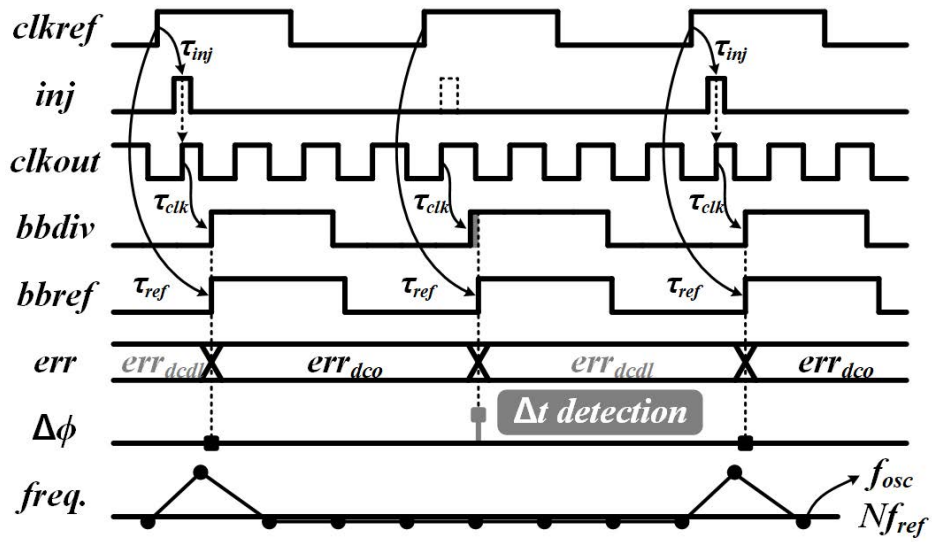


Fig. 3.6 The conceptual timing diagram of the half-edge injection with proposed tracking loop disabled when multiplication factor (*N*) is 4.

Fig. 3.7 shows the block diagram of the digital loop filter that detects the timing error in ILPLL. The de-serialization is easily implemented by using a counter. The separated errors are individually accumulated and modulated by delta-sigma modulator to mitigate quantization noise.

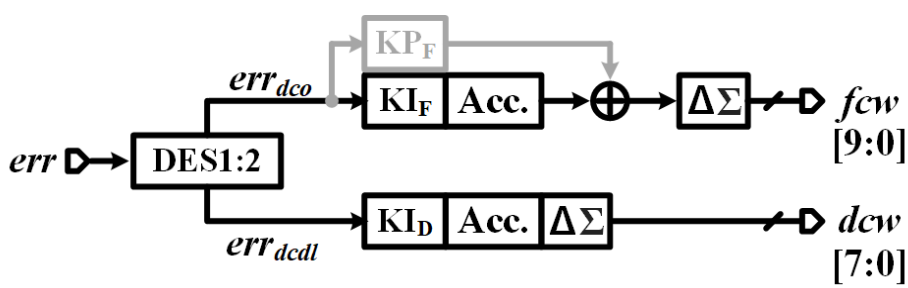


Fig. 3.7 Block diagram of the digital loop filter.

3.3.2 Overall Architecture and Operation Principle

Fig. 3.8 shows the block diagram and flowchart of the proposed ILPLL. The injection-timing mismatch defined in Section 3.2 is adjusted by 8-bit digitally controlled delay line (DCDL) until it comes to zero. The pulse-gating scheme in [28] and [32], though simplified for this work, is utilized to find the timing mismatch. By inserting a divider in front of the pulse generator as shown in Fig. 7(a), Δf is detected at the BBPFD because the phase error induced by Δt is accumulated over $(N - 1)$ cycles. The propagation delay through injection path (τ_{inj}) and clock divider (τ_{clk}) is fixed and unavoidable. In this reason, adjusting the delay ahead of BBPFD (τ_{ref}) is selected to eliminate it to zero, not integer multiples of the target period as described in [33].

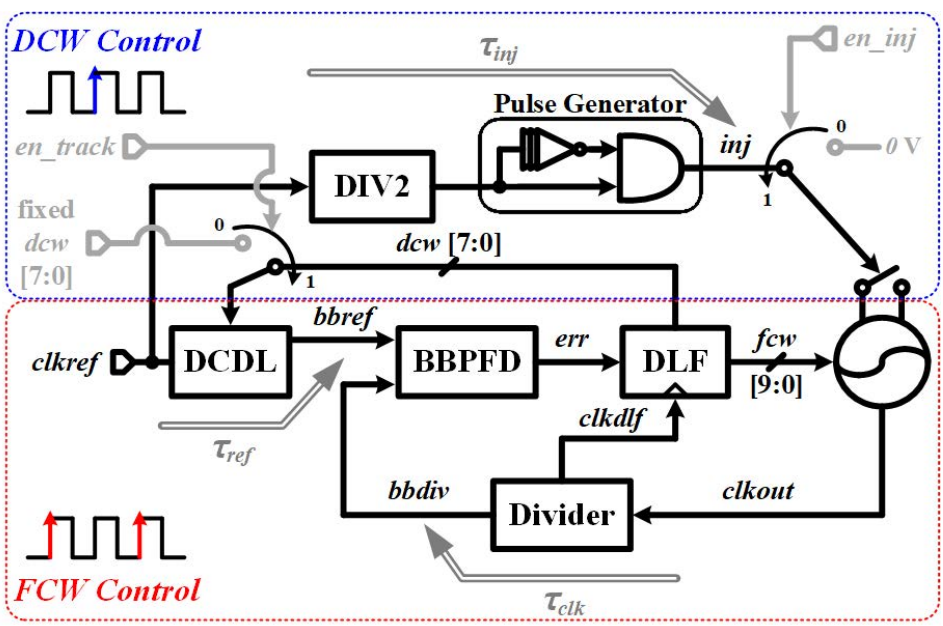


Fig. 3.8 Block diagram of the proposed ILPLL.

As depicted in Fig. 3.9, ADPLL operates at first for coarse tuning of the oscil-

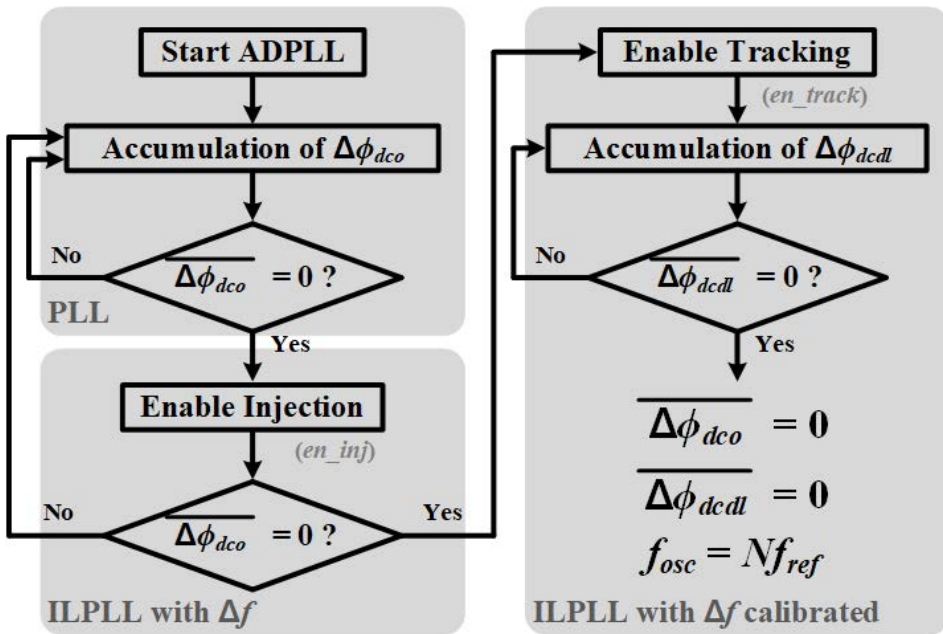
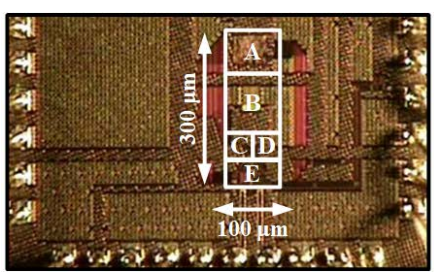


Fig. 3.9 Flowchart of the proposed ILPLL.

lator. After ADPLL is locked, the pulsed injection is applied (*en_inj*) to operate as a conventional ILPLL. When initial Δf induced by Δt is within the locking range of ILPLL, it achieves a locked state; however, it may not be the optimum condition. Subsequently, the proposed tracking loop turns on (*en_track*), and DCDL is adjusted to reduce the timing mismatch; thus, f_{osc} goes to the target frequency, Nf_{ref}. In other words, averaged errors of DCO ($\Delta\phi_{dco}$) and DCDL ($\Delta\phi_{dcdl}$) come to zero for both, which shows desired locking behavior.

3.4 Measurements

The prototype chip has been fabricated in 28-nm CMOS technology. The chip contains the proposed ILPLL, an open-drain clock driver for monitoring, and an I^2C interface that controls operation mode and several configurable parameters such as injection strength or the loop-filter gain. The ILPLL occupies an active area of 0.03 mm^2 and consumes 5.65 mW with the 312.5-MHz reference clock and 0.9-V supply voltage at 5 GHz as described in Fig. 3.10. The reference clock is sourced from a vector signal generator, Agilent E8267D, through bias tee and output clock is measured by a spectrum analyzer, Agilent E4445A. A digital power source, Agilent B2926A, is also used to measure the total current of each power domain and supply-variation test as shown in Fig. 3.13.



	Block Description	Power (mW)
A	Digital Loop Filter	2.6
B	ILDCO	3.38
C	Pulse Gen. & DCDL	6.83
D	PD & Deserializer	
E	Limiting Amplifier	

Fig. 3.10 Chip photomicrograph, block description, and separated power consumption at 10 Gb/s with a 0.9-V supply voltage.

3.4.1 Noise Suppression using Injection and Timing Calibrator

Fig. 3.11 shows the measured phase-noise curves with several different clock synthesizers. When an injection is applied without any loop, the noise under 100 kHz (1/*f* region) is not sufficiently filtered out since it operates as the first-order system offered by an injection locking. With PLL activated and injection with uncalibrated, fixed DCW, because there is a mismatch in injection timing, deterministic noise is shown at 156.25 MHz and its harmonics. The proposed ILPLL shows the lowest rms jitter integrated from 1 kHz to 40 MHz as 152 fs.

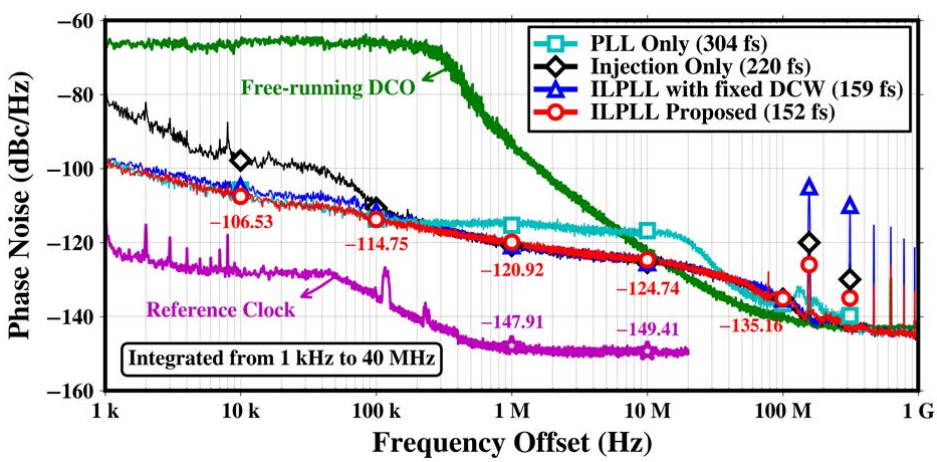


Fig. 3.11 Measured phase-noise curves of the output clock.

Although in-band noise suppression is almost the same as the ILPLL with fixed delay control word (DCW), the spurious tones at 156.25 MHz and its super-harmonics are reduced as much as 30 dB since Δt comes to zero in average by adapting the delay utilizing DCDL. In this result, it is demonstrated that the deterministic jitter induced by the timing mismatch is reduced, and it is more clearly found in the following spectrum analysis. Fig. 3.12 shows spectrum results with and without the timing calibrator when the injection is applied with PLL. The ILPLL with fixed DCW shows inferior reference spur compared with the proposed one. In this test of Fig. 3.11 and Fig. 3.12, normalized DCW is fixed to –15, which is equivalent to about 20-ps timing mismatch in SPICE simulation. As seen in Fig. 3.11, spurious tones at 156.25 MHz and 312.5 MHz show up, and the proposed tracking loop reduces these tones to –53 dBc and –62 dBc, respectively.

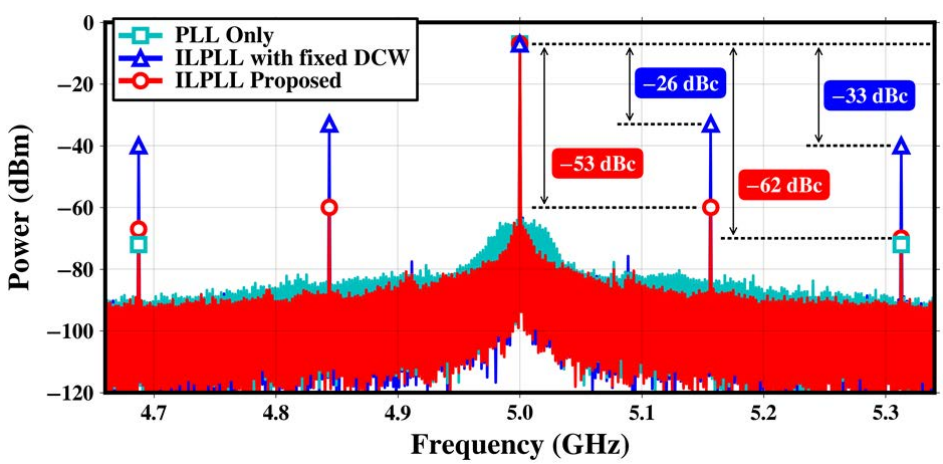
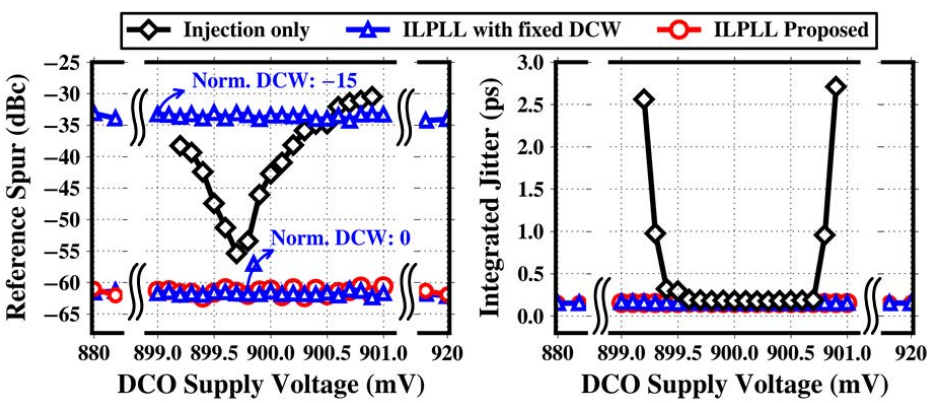


Fig. 3.12 Measured spectrums of the output clock.

3.4.2 Verification of Timing Calibrator with Variations

Fig. 3.13 shows the measured reference spur and integrated jitter of several different clock multipliers using injection with various supply voltage. This test is carried out using a digital power source, Agilent B2926A, which has a fine resolution of voltage less than 0.1 mV. With fixed f_{osc} and injection without any feedback loop, measured spur levels are susceptible to the supply-voltage variation, and the integrated jitter is abruptly increased at the edge of locking range. The ILPLL with fixed DCW shows constant spur values depending on DCW. Since Δt is fixed and not adjusted by the tracking loop, the deterministic noises are added when Δt is not zero. The proposed ILPLL shows consistent and minimum jitter performance for the supply-voltage variation irrespective of initial DCW.

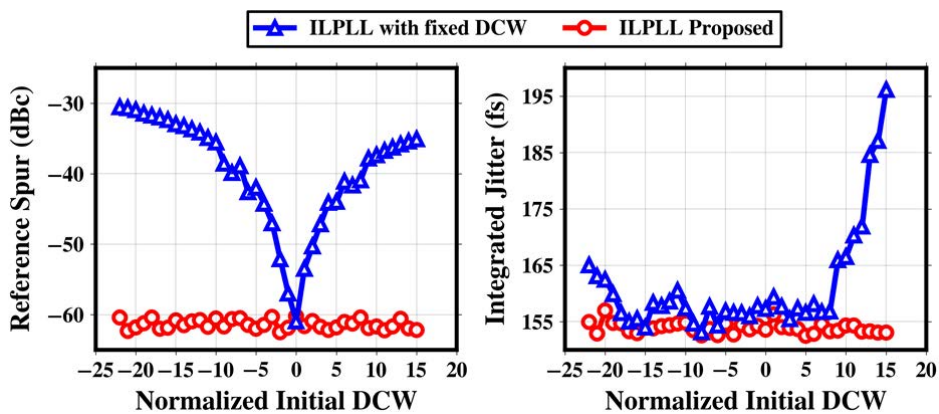
Fig. 3.14 shows the measured jitter performances as a function of normalized



(a) (b)

Fig. 3.13 Measured (a) reference spur and (b) integrated jitter with different injection-locked clock multiplier architecture over supply-voltage variation.

initial DCW controlled by I^2C interface with fixed 0.9-V supply voltage. With ILPLL alone, reference spur is very sensitive to DCW as shown in Fig. 3.14(a). The center code for expressing normalized DCW is defined to the point where ILPLL without the calibrator shows minimum spur level. When the proposed tracking loop operates, initial DCW converges to the optimum point where the timing mismatch is minimized, resulting in constant and minimum values for both the spur level and the integrated jitter over various initial DCWs as shown in Fig. 14(a) and (b).



(a) (b)

Fig. 3.14 Measured (a) reference spur and (b) integrated jitter with and without timing calibrator as a function of the normalized initial delay control word.

3.4.3 Performance Summary and Comparison

Table 3.1 shows performance summary and comparison with recently published RO-based ILPLLs [27], [29]–[33]. This work shows the best-integrated jitter compared with them. From the measured integrated jitter and power consumption, the figure of merit (FoM) is defined as

$$\mathrm{FoM} = 10\log_{10}\left[\left(\frac{\sigma_t}{1\ \mathrm{s}}\right)^2\left(\frac{P_{DC}}{1\ \mathrm{mW}}\right)\right], \tag{3.1.2}$$

where σ_t is integrated jitter, and P_{DC} is power consumption [17]. The calculated FoM in this work is –248.8 dB that is state-of-the-art among the RO-based ILPLLs [26]–[27], [29]–[33]. Regarding energy cost, this work exhibit the power efficiency as 1.13 mW/GHz that is considerably efficient between RO-based ILPLLs. For the RO-based ILPLLs which contain the timing-calibrator [26]–[27], [29]–[30], the proposed ILPLL shows much higher power efficiency since replica cells or decision circuits in [26]–[27], [29]–[30] operate at the frequency of oscillation which is the fastest rate in the whole chip. On the other hand, the proposed ILPLL adopts the architecture of conventional PLL except for the injection circuits and DCDL that are switched by the rate of the reference clock, thus, remarkable energy cost is obtained.

	ISSCC'14 [2]	JSSC'16 [3]	ISSCC'17 [4]	ISSCC'17 [5]	ISSCC'17 [6]	TCAS I'18 [7]	This Work
Technology (nm)	20	65	65	65	65	65	28
Active Area (mm^2)	0.044	0.06	0.064	0.028	0.09	0.06	0.03
Supply Voltage (V)	1.25 / 1.1	1.1	1.2	1.2	1.0	1.2	0.9
Reference Freq. (MHz)	1875	120	156.25	150	120	156.25	312.5
Output Freq. (GHz)	2–16	0.96–1.44	2.5	0.52–1.15	2.5–5.75	2.5–5.63	5
Mult. Factor (N)	8	10	16	6	20–46	32	16
Power (mW)	46.2	9.5	13.5	3.8	5.3 @ 5 GHz	15.4	5.65
Power Eff. (mW/GHz)	3.08	7.92	4.62	4.22	1.06	3.08	1.13
Reference Phase Noise or Integrated Jitter	−136.6 dBc/Hz @ 10 MHz	118 fs (10 kHz–40 MHz)	-	-	-	−165 dBc/Hz @ 1 MHz	−149 dBc/Hz @ 10 MHz
Output Int. Jitter (fs) (Range)	268 (100 kHz–1 GHz)	185 (10 kHz–40 MHz)	198 (10 kHz–40 MHz)	420 (10 kHz–10 MHz)	340 (10 kHz–40 MHz)	168 (1 kHz–40 MHz)	152 (1 kHz–40 MHz)
Reference Spur (dBc)	−48	−53	−65	-	−45	−42 @ f_{ref} −42.6 @ $2f_{ref}$	−62 @ f_{ref} −53 @ $0.5f_{ref}$
FoM (dB)	−234.8	−244.9	−242.8	−241.7	−242.4	−243.6	−248.8
Injection-Timing (Δf) Tracking	Pulse-Position Modulation	Replica-Delay Cell	TDDC	-	Pulse Gating	-	Half-Edge Injection

Table 3.1 Performance Summary and Comparison.

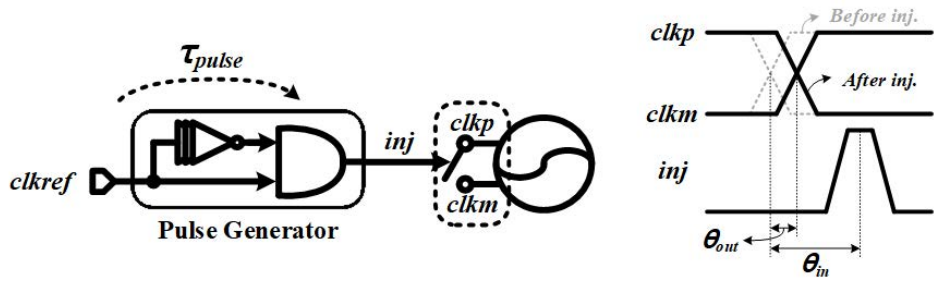
Chapter 4

ILPLL with Maximum Injection Strength

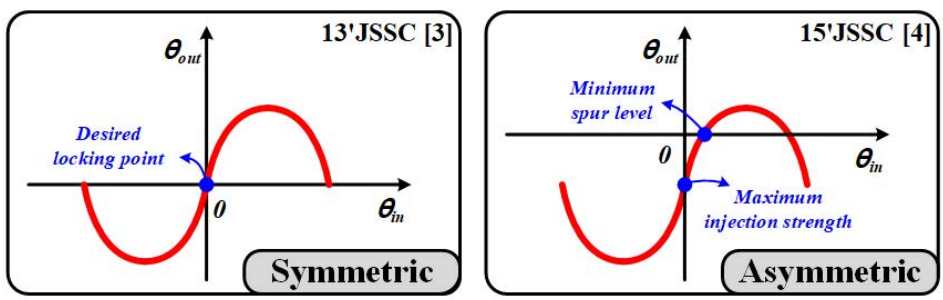
4.1 Overview

Injection-locked oscillators (ILOs) have been widely adopted in clock synthesis because of their superior jitter performance and simple implementation. Most analyses for the ILOs [14], [16], [25], and [28] have focused only on the relationship between the currents of the injection and the local oscillator. In addition, the analyses have been conducted in an over-simplified way ignoring the factors that may affect overall characteristics such as the injection duration or the voltage drop across the control circuit. In [28], the injection duration is considered as a variable for the overall phase domain response (PDR) showing asymmetry in certain cases.

Although the injection duration is considered in the analysis, it does not



(a)



(b) (c)

Fig. 4.1 (a) Conventional injection-locked oscillator (ILO) with a pulse generator and its timing diagram. (b) Symmetric [25] and (c) asymmetric [28] phase domain response (PDR) analyses.

include the effects from the parasitics of the actual circuit elements such as resistors or current sources. In this work, including implemented circuits controlling the frequency of the oscillator, the PDR is re-derived and adjusted to have a symmetric characteristic to find the best locking point.

The conventional injection scheme shorting the two differential nodes is shown in Fig. 4.1(a). It consists of a pulse generator to make an injection signal, followed by the oscillator. The timing diagram in Fig. 4.1(a) indicates the definition of the PDR of the ILO. The phase difference of the clock edge before the injection and the

center of the injection signal is defined as θ_{in}, and its resultant output phase shift is defined as θ_{out}. In [25], the PDR from a phasor diagram shows perfectly symmetric characteristic as shown in Fig. 4.1(b) regardless of any other variables. In the PDR analysis, θ_{in}-intercept means the minimum spur level and the slope corresponds to the realignment factor, indicating injection strength. Thus, in Fig. 4.1(b), the desired locking point is placed simply at the zero point ($\theta_{in} = 0$). However, referring to [28], the PDR can be asymmetric considering the integration effect of the injection pulse width. In case of the asymmetric PDR in Fig. 4.1(c), the excellent locking points for achieving the maximum injection strength and the zero phase offset do not coincide. Therefore, the minimum integrated noise and spur cannot be achieved simultaneously in the asymmetric PDR.

In this paper, the proposed injection-locked PLL (ILPLL) achieves an improved jitter performance based on the accurate analysis of the PDR on the ILO. In addition, the pulse generator in front of the ILO is eliminated to achieve a high-speed clock operation. As a result, 15-GHz ILPLL that shows the excellent jitter performance of 213 fs from 1 kHz to 40 MHz is obtained.

4.2 Previous Analyses of PDR

The modeling of the phase domain response (PDR) of the injection-locked oscillator (ILO) has widely been studied in different assumptions [25] and [28]. From the preceding PDR analysis, the characteristics of the ILO could be obtained such as injection strength and the overall locking range. Based on such parameters, the performance of the ILO-based architecture can be evaluated. Thus, an accurate estimation of PDR for the ILO should be performed preceding the design of the ILO in the physical implementation. The procedure to get a relationship between the input and output phase of the ILO is very similar with the impulse sensitivity function (ISF) proposed in [11]–[13] for phase noise investigation of the oscillator. The analysis based on ISF function is attempted and described, trying to explain the characteristic of the ILO under large-signal injection reported in [19], [20], and [22].

Section 4.2.1 reviews the PDR model of [25] for impulse injection assuming injection duration is extremely brief to be ignored. Since the analysis in [25] is so straightforward ignoring the injection duration, it fails to capture the asymmetric characteristic of the PDR. Section 4.2.2 reviews the PDR model in [28] that is more authentic than [25] incorporating the injection duration as an important variable to figure out the PDR of the ILO.

4.2.1 Impulse Injection

As illustrated in Fig. 4.1(a), the input and output phase relationships of an ILO is described according to the occurrence of the injection operation or not. In this analysis, it performs it for an LC-tuned oscillator, and the injection switch is composed of an N-type MOSFET. To simplify the analysis, while injection current flows through the duration of D, the injection MOSFET is modeled as an equivalent resistance, R_{on}. From [23], the voltage variation on the differential nodes while injection operates during D is approximates to

$$\Delta V \equiv V\gamma \sin(\phi_{in}) = V(1-e^{-(D/(R_{on}C))})\sin(\phi_{in}) \tag{4.1}$$

, where λ is constant, later, this assumption makes the analysis imperfect.

Also, it brings a voltage phasor diagram to calculate the relationship between the input and output phase shift of the ILO. There are two assumptions to proceed with the analysis: the one is the equivalent tank loss of the harmonic oscillator, and the injection duration of D are negligible. With the two assumptions and using the trigonometry of the phasor diagram in Fig. 4.3, the following relationship can be derived as

$$\tan(\phi_{in}-\phi_{out}) = \frac{V\sin(\phi_{in})-\Delta V}{V\cos(\phi_{in})}. \tag{4.2}$$

Solving the output phase shift as a function of ϕ_{in},

$$\phi_{out} = \phi_{in} - \tan^{-1}[(1-\gamma)\tan(\phi_{in})]. \tag{4.3}$$

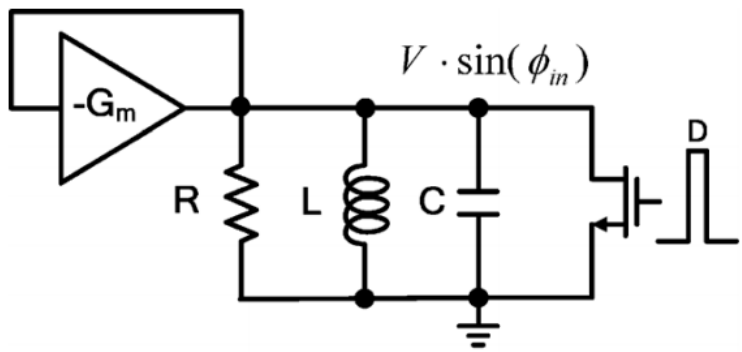


Fig. 4.2 Simplified half circuit of an LC oscillator with an injection N-type MOSFET [25].

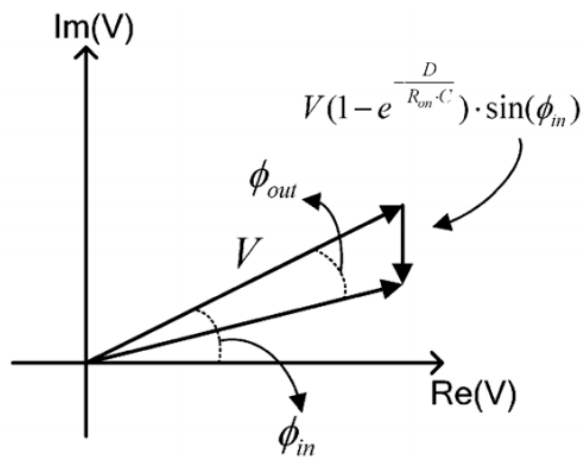


Fig. 4.3 Voltage phasor diagram when an LC oscillator is injected during the period of *D* [25].

Here, realignment factor in [14] is obtained by the first derivative of (4.3) with respect to the input phase ϕ_{in} as

$$\frac{d\phi_{out}}{d\phi_{in}} = 1 - \frac{(1-\gamma)\sec^2(\phi_{in})}{[(1-\gamma)\tan(\phi_{in})]^2 + 1}. \tag{4.4}$$

When $\phi_{in} = 0$, realignment factor in [14] is derived as

$$\frac{d\phi_{out}}{d\phi_{in}}|_{\phi_{in}=0} = \gamma. \tag{4.5}$$

From this formula, the analysis in [14] coincides while small-signal analysis is performed here. The transfer curve of the equation (4.3) is shown in Fig. 4.4. As illustrated in this figure, as the injection strength or realignment factor increases, the overall locking range of the ILO also increases, and the slope at the origin becomes more steeply. In addition, the overall configuration of the curve is perfectly balanced. In other words, whether the injection pulse pushes or pulls the local oscillator's clock edge, the amount of the output phase shift (ϕ_{out}) is the same regardless of its polarity. It is not able to describe the asymmetric feature that the physical implementation of the ILO exhibit; it is verified using HSPICE simulation in Appendix A.

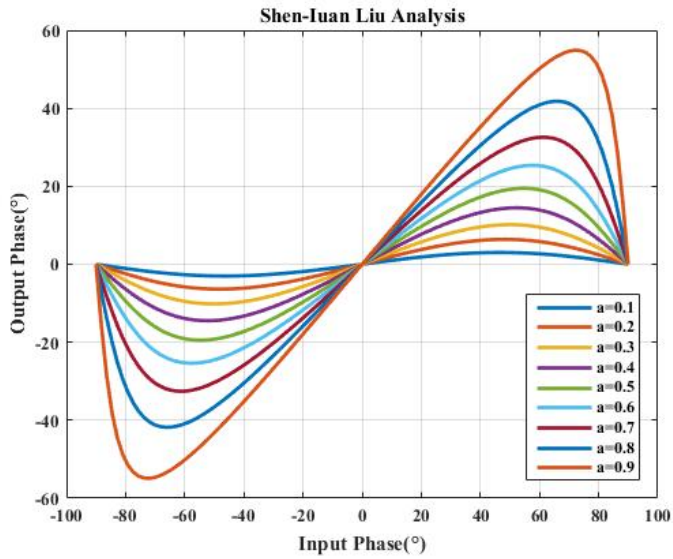


Fig. 4.4 Transfer curve of equation (4.3) with different injection strength from 0.1 to 0.9.

4.2.2 Pulse Injection

In this Chapter 4.2.2, we will discuss the investigation described in [28]. Since the study in [28] considers the pulse width of the injection signal as the significant variable indicating the output phase shift, it attains more precise consequence in comparison to the previous PDR analysis in Chapter 4.2.1. Unlike the simple voltage fluctuation in (4.1), it integrates the effective voltage change through the injection duration (D). In [28], it divides the pulse width into M infinitesimally small pulses, and its voltage change for the impulse signal is calculated as same as in [25]. The voltage change at the each of the divided pulse is added all together and substituted from the result of (4.1). After that, an almost the same procedure using trigonometry of the voltage phasor diagram is performed to get the output phase shift.

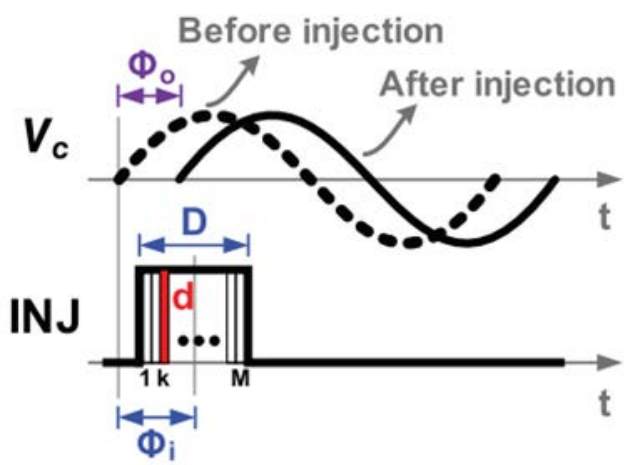


Fig. 4.5 Timing diagram of the ILO in LC oscillator considering the pulse width of D divided into infinitesimally small impulse pulses [28].

Each of the k-th pulse causes a change in V_c by δv_k and assuming the impulse pulse width is very narrow compared with the period of the oscillator as

$$d << \frac{2\pi}{\omega_0}. \tag{4.6}$$

Using the above assumption, the voltage change at k-th pulse is expressed as

$$\delta v_k = V_{c,k}(1 - e^{-d/\tau}) \approx V_{c,k}\frac{d}{\tau} \tag{4.7}$$

where $V_{c,k}$ indicates the capacitor voltage at k-th pulse.

The phase of $V_{c,k}$ changes from $\phi_{in} + 0.5\omega_0 D$ to $\phi_{in} - 0.5\omega_0 D$ since the position x changes from 0 to D. The general capacitor voltage $V_{c,k}$ can be expressed as

$$x = kd \rightarrow V_{c,k} = Ae^{-kd/\tau}\sin(\phi_{in} + 0.5\omega_0 D - \omega_0 kd). \tag{4.8}$$

Subsequently, the total normalized change in the capacitor voltage by the injection during D is derived as

$$\begin{aligned}\Delta_{inj} &= \frac{1}{A}\sum_k \delta v_k \cos(\omega_0 kd) = \frac{1}{A}\sum_k V_{c,k}\frac{d}{\tau}\cos(\omega_0 kd) \\ &= \sum_k e^{-kd/\tau}\sin(\phi_{in} + 0.5\omega_0 D - \omega_0 kd)\cos(\omega_0 kd)\frac{d}{\tau}\end{aligned}. \tag{4.9}$$

The $\cos(\omega_0 kd)$ term is added to explain the phase difference between pulses. To transform the summation in (4.2.9) to the integral formation, thin pulse d goes to

zero; then, the following equation is derived as

$$\Delta_{inj}(\phi_{in}) = \frac{1}{\tau}\int_0^D e^{-x/\tau}\sin(\phi_{in} + 0.5\omega_0 D - \omega_0 x)\cdot\cos(\omega_0 x)dx\,. \qquad (4.10)$$

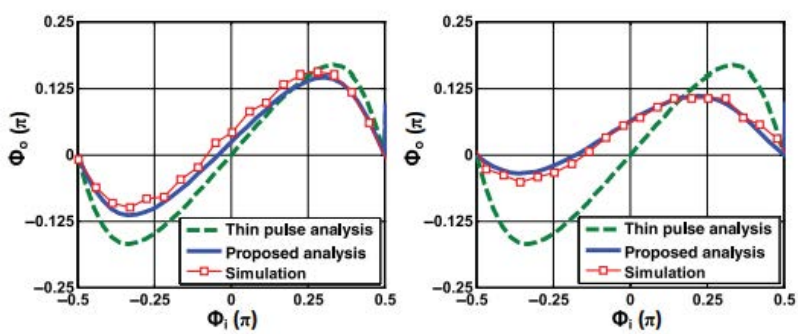
Solving this equation,

$$\Delta_{inj}(\phi_{in}) = \frac{1}{2}\sin\left(\phi_{in} + \frac{\omega_0 D}{2}\right)(1-e^{-D/\tau}) - \frac{1}{2+8\omega_0^2\tau^2}$$
$$\cdot\left[\begin{array}{l} 2\omega_0\tau\cos\left(\phi_{in} + \frac{\omega_0 D}{2}\right) - \sin\left(\phi_{in} + \frac{\omega_0 D}{2}\right) \\ -e^{-D/\tau}\left(2\omega_0\tau\cos\left(\phi_{in} - \frac{3\omega_0 D}{2}\right) - \sin\left(\phi_{in} - \frac{3\omega_0 D}{2}\right)\right)\end{array}\right]. \qquad (4.11)$$

Same trigonometric calculation in Section 4.2.1 is performed to deduce the output phase shift as a function of the input phase:

$$\phi_{out} = \phi_{in} - \tan^{-1}\left(\tan(\phi_{in}) - \Delta_{inj}\cdot\sec(\phi_{in})\right). \qquad (4.12)$$

In Fig. 4.6, an asymmetric feature appears when the pulse width increased from 20 ps to 40 ps while the integration effect is further considered.



(a) (b)

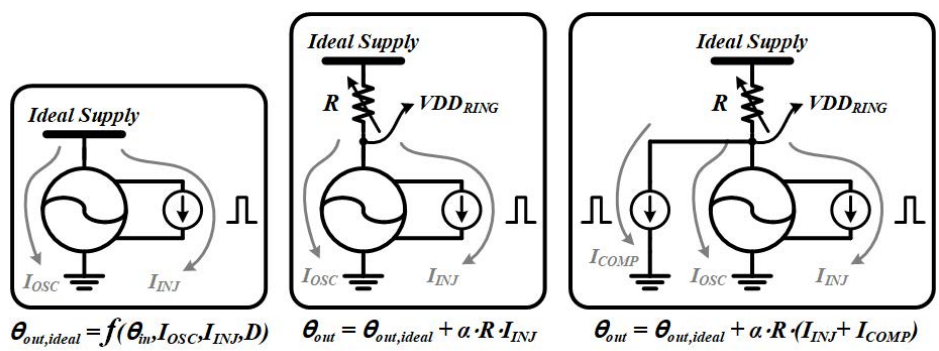
Fig. 4.6 PDR analysis and simulation results in case (a) R_{sw} = 20 Ω, D = 20 ps; (b) R_{sw} = 40 Ω, D = 40 ps in [28].

4.3 Parallel Translation of PDR

Previous analyses on the PDR in Section 4.2.1 [25] and Section 4.2.2 [28] focus only on the oscillator itself as shown in Fig. 4.7(a) for the ideal supply voltage. In these analyses, θ_{out} is determined by the current of the oscillator, I_{OSC}, the injection current, I_{INJ}, and the injection duration, D. The output phase in Fig. 4.7(a), $\theta_{out,ideal}$, can be defined as

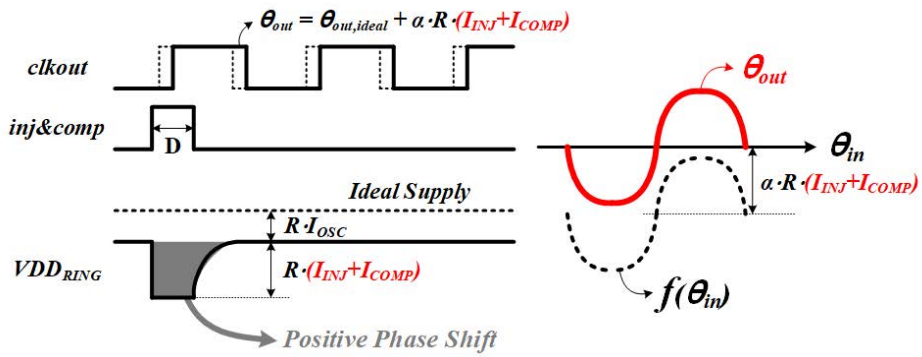
$$\theta_{out,ideal} = f(\theta_{in}, I_{OSC}, I_{INJ}, D). \tag{4.13}$$

It is noted that the PDR could have an asymmetric characteristic with a negative offset. It can easily pull the phase before the transition while it is challenging to push the phase after the transition. For this reason, the PDR tends to be asymmetric even with the ideal supply voltage.



(a) (b) (c)

Fig. 4.7 Block diagram of the ILO with (a) ideal supply voltage, (b) physical circuit implemented, and (c) proposed scheme.



(a) (b)

Fig. 4.8 (a) Timing diagram and (b) phase domain response (PDR) when voltage drop through the control circuit is considered.

On the other hand, the more realistic implementation of the oscillator is shown in Fig. 4.7(b) with a digitally-controlled resistor (DCR) included as a frequency-tuning unit [44]. In this example, when the injection current flows through the differential clock nodes, it passes through the resistor. Thus, the voltage drop during the injection time (D) makes a positive phase shift since the supply voltage of the core oscillator, VDD_{RING}, goes down and the delay time increases instantaneously as illustrated in Fig. 4.8(a). Its resultant output phase can be modified from (4.13) as

$$\theta_{out} = \theta_{out,ideal} + \alpha \cdot R \cdot I_{INJ}. \tag{4.14}$$

, where α is a fitting coefficient and R is the equivalent resistance of the DCR.

Since the target frequency of this work is very high as 15 GHz, the resistance in Fig. 4.7(b) should be designed as very small. Thus, the additional positive phase shift through the resistor due to the injection current, $\alpha \cdot R \cdot I_{INJ}$, is not sufficient to make the overall PDR symmetric in our work. Thus, we propose to use a

compensation current, I_{COMP}, from the supply voltage of the core oscillator to the ground directly. By doing so, an extra voltage drop through the resistor is obtained and, accordingly, a more significant positive phase shift can be achieved. The total phase shift owing to the control circuit makes the overall PDR characteristic move to the positive direction. The total output-phase shift in the proposed scheme is expressed as

$$\theta_{out} = \theta_{out,ideal} + \alpha \cdot R \cdot (I_{INJ} + I_{COMP}). \tag{4.15}$$

4.4 Circuit Implementation

4.4.1 Proposed ILO

The proposed injection-locked digitally-controlled oscillator (ILDCO) is presented in Fig. 4.9. It consists of a two-stage inverter-based ring oscillator with a 10-bit digitally-controlled resistor as described in [44]. Since the injection duration is much narrower than the target period, the maximally available frequency of the ILPLL is determined by not the oscillator but the pulse generator. For this reason, the injection cells are implemented by two n-type MOSFETs in series between each differential clock nodes, thereby obviating the use of the pulse generator as in [33].

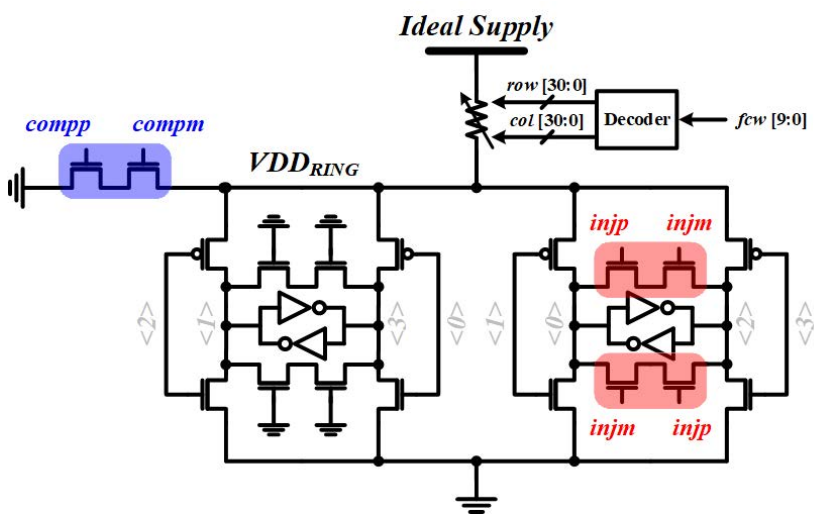
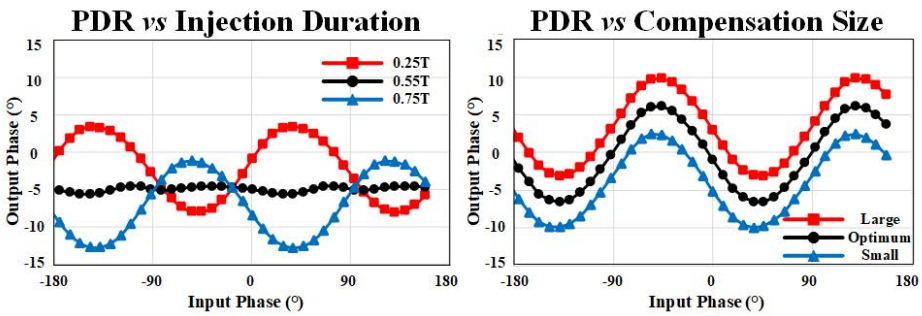


Fig. 4.9 Block diagram of the proposed ILDCO.



(a) (b)

Fig. 4.10 (a) Block diagram of the proposed ILDCO and the simulated phase domain response (PDR) with different (a) injection duration and (b) compensation switch size.

The injection current flows when both *injp* and *injm* in Fig. 4.9 are higher than the threshold voltage of the MOSFET. Compared with [33], the delay time between *injp* and *injm* is intentionally inserted so that it can flow sufficient charge through differential nodes. Based on the simulation results in Fig. 4.10(a), the injection strength is maximized when the injection duration is about 0.25 times the target period. In addition, since the injection cells are composed of only the n-type MOSFETs, the injection occurs only when the rising edge of the reference clock arrives. As described in Fig. 4.10(b), as the size of the compensation switches gets bigger, the overall PDR of the ILO shifts to the positive y-direction.

4.4.2 Overall Architecture of ILPLL

Fig. 4.11 illustrates the overall ILPLL architecture which combines the traditional PLL and the proposed injection scheme. After the PLL is locked in a steady state without an injection, the injection and compensation paths are enabled with a fixed delay through *clkref* to *bbref*. The delay is made tunable to verify the symmetry of the PDR, which is detailed in Section 4.5. When the injection and compensation currents flow, the proportional path in the digital loop filter is disabled because the injection path takes a similar action to direct proportional path. That is, only the integral path is enabled when the PLL and the injection run simultaneously.

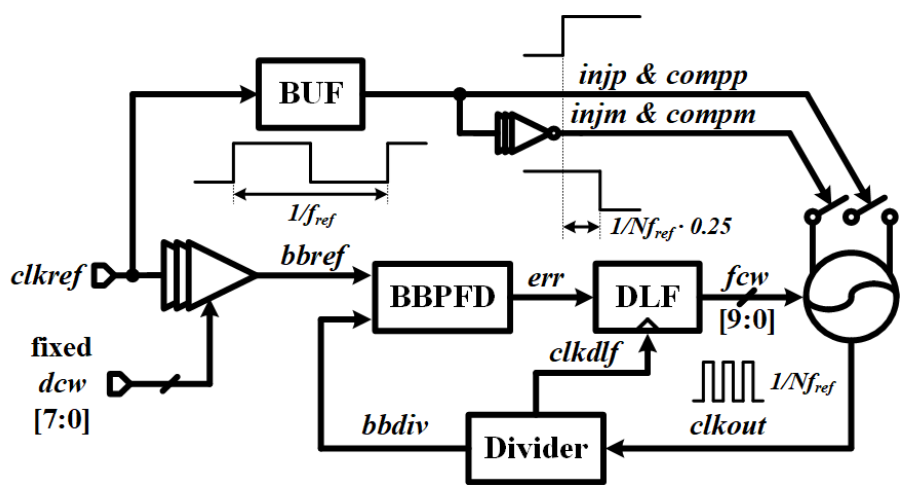
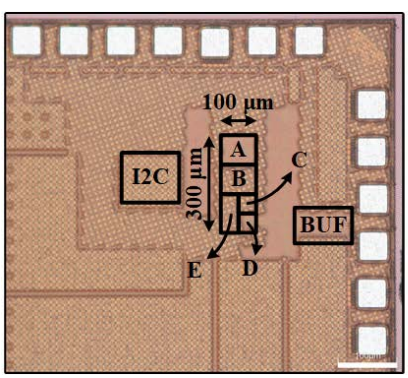


Fig. 4.11 The overall architecture of the injection-locked PLL (ILPLL).

4.5 Measurements

The proposed ILPLL fabricated in 28-nm CMOS technology occupies an active area of 0.03 mm^2, excluding an I2C interface, and consumes 17.81 mW with a 468.75-MHz reference clock and a 1.3-V supply voltage at the output clock frequency of 15 GHz. Fig. 4.12 shows a chip photomicrograph and the corresponding description of the building blocks with power breakdown, which indicates that the ILO dissipates most of the power. The reference clock is sourced from a vector signal generator, Agilent E8267D, through a bias tee, and the output clock is measured by a spectrum analyzer, Agilent E4440A. A digital power source, Agilent B2926A, is also used to measure the total current consumption of each power domain as described in Fig. 4.12(b).



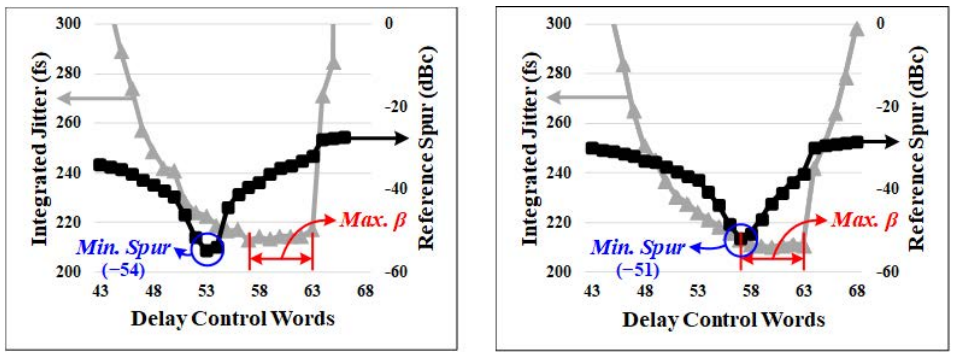
(a)

	Block Description	Power (mW)
A	Digital Loop Filter	1.4
B	ILDCO	9.88
C	Divider	2.42
D	BBPFD	
E	DCDL & etc.	

measured by Agilent B2926A

(b)

Fig. 4.12 (a) Chip photomicrograph, (b) block description, and separated power consumption at 15-GHz with a 1.3-V supply voltage.



(a) (b)

Fig. 4.13 Measured integrated jitter and reference spur of ILPLL (a) without and (b) with compensation switches in the ILDCO.

Fig. 4.13 shows the measured RMS jitter integrated from 1 kHz to 40 MHz and the reference spur level concerning the external delay control word (DCW) that adjusts the phase of the reference clock, *bbref*. The ILPLL in this work has two-phase modulation path, through the injection and the conventional PLL. If the delay mismatch between the two paths is not perfectly tuned, it cannot avoid additional deterministic jitter as mentioned in [23] and [28]. By adjusting the delay of the reference-clock path, the locking point in the PDR curve can be controlled. As shown in Fig. 4.13(a), turning off the compensation switches, the two paths are well matched at the DCW of 53 where the resultant reference spur level is minimized as –54 dBc. However, the corresponding integrated jitter is 220 fs which is not the minimum value. Since the injection strength determines the overall bandwidth of the ILPLL, as the injection strength increases, the measured integrated jitter decreases. In other words, even if the path mismatch between the two modulation points is perfectly matched, its injection strength at this point is not the maximum in the asymmetric PDR as described in the previous section. When the compensation switches are turned on,

the minimum spur level point, –51 dBc, appears within the maximum injection-strength range, as shown in Fig. 4.13(b). The additional voltage drop through the resistor in ILDCO due to the compensation current makes the overall characteristic of PDR less asymmetry.

In Fig. 4.14, the measured phase noise curves of the ILPLL at the minimum spur level measured with and without the compensation switches. Since the injection strength at the DCW of 53 without compensation is smaller than that at the DCW of 55 with compensation, its phase noise curve is slightly worse than the proposed one. For this reason, the measured integrated jitter with the proposed scheme is better as 213 fs compared with the conventional injection scheme as 220 fs.

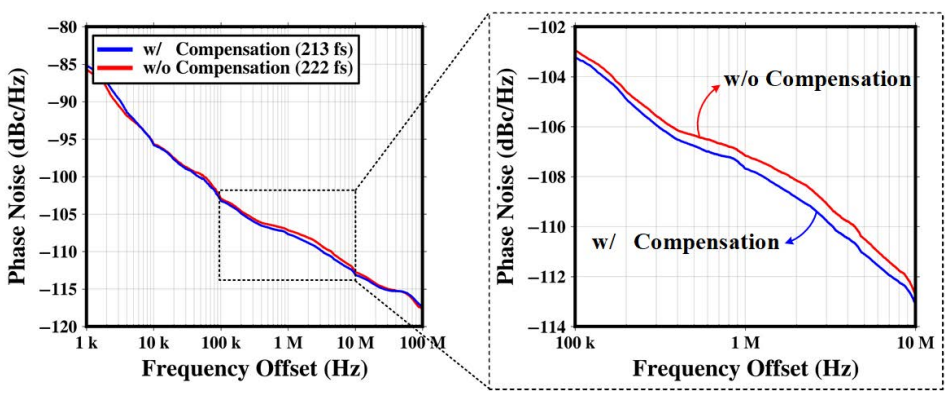


Fig. 4.14 Measured phase noise curves with and without compensation switches when the reference spur level shows the lowest value.

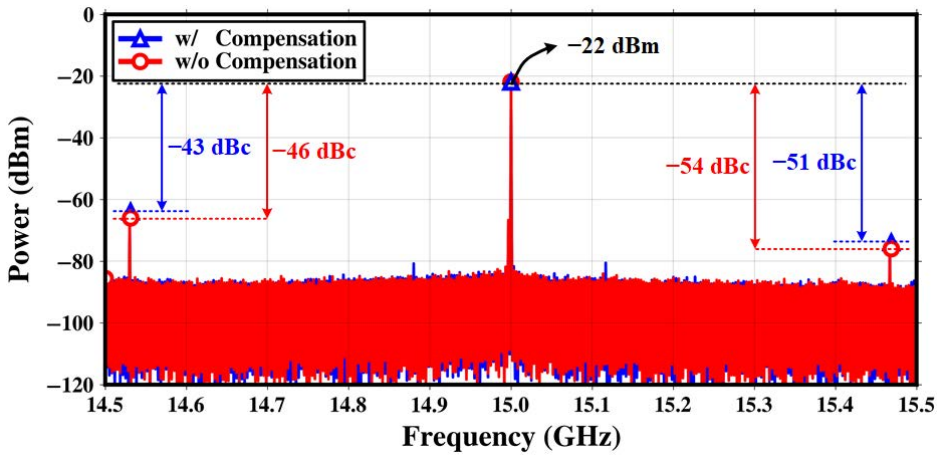


Fig. 4.15 Measured spectrums with and without compensation switches when the reference spur level shows the lowest value.

Fig. 4.15 shows the measured spectrums with and without the compensation switches. However, the minimum spur level of the proposed scheme is slightly deteriorated compared with the results without compensation current due to the additional action at the reference clock rate.

Table 4.1 summarizes the performance and compares with other recently published ILPLLs [27], [29]–[33]. From the measured integrated jitter and the power dissipation, the figure of merit (FoM) is calculated as –240.9 dB that is comparable to other works. This work shows the fastest clock speed of 15 GHz among the works employing the ring-type injection technique thanks to the exclusion of the pulse generator.

	ISSCC'14 [6]	JSSC'16 [7]	ISSCC'17 [8]	ISSCC'17 [9]	ISSCC'17 [10]	TCAS I'18 [11]	This Work
Technology (nm)	20	65	65	65	65	65	28
Active Area (mm^2)	0.044	0.06	0.064	0.028	0.09	0.06	0.03
Supply Voltage (V)	1.25 / 1.1	1.1	1.2	1.2	1.0	1.2	1.3
Reference Freq. (MHz)	1875	120	156.25	150	120	156.25	468.75
Output Freq. (GHz)	15	1.2	2.5	0.9	2.5–5.75	5	15
Mult. Factor (N)	8	10	16	6	20–46	32	32
Power (mW)	46.2	9.5	13.5	3.8	5.3	15.4	17.81
Power Eff. (mW/GHz)	3.08	7.92	4.62	4.22	1.06	3.08	1.18
Output Int. Jitter (fs) (Range)	268 (100 kHz–1 GHz)	185 (10 kHz–40 MHz)	198 (10 kHz–40 MHz)	420 (10 kHz–10 MHz)	340 (10 kHz–40 MHz)	168 (1 kHz–40 MHz)	213 (1 kHz–40 MHz)
Reference Spur (dBc)	–48	–53	–65	-	–45	–42	–51
FoM* (dB)	–234.8	–244.9	–242.8	–241.7	–242.4	–243.6	–240.9

*FoM $= 10\log_{10}\left[\left(\frac{\sigma_t}{1\text{ s}}\right)^2\left(\frac{P_{DC}}{1\text{ mW}}\right)\right]$ integrated jitter σ_t and DC power P_{DC}.

Table 4.1 Performance Summary and Comparison.

Chapter 5

ILCDR with Maximum Timing-Margin Tracking

5.1 Overview

Recently, an injection-locked clock and data recovery circuit (ILCDR) has widely been adopted in wireline receivers since it shows excellent jitter tolerance (JTOL) performance and low power consumption with minimal hardware [37]–[43]. Typically, to achieve a superior JTOL performance in the conventional phase-locked loop (PLL) or phase interpolator (PI) based CDRs, large power consumption should be required for better phase noise of the oscillator and the higher sensitivity of the sampler. However, an injection-locked oscillator (ILO) have a large bandwidth because it directly forwards the transition of data to the local oscillator. In other words, an ILO tracks the phase of the input data stream rapidly, which results in higher JTOL

performance. Despite its superior JTOL performance, the design of ILCDR has a critical issue to be resolved, which is a frequency offset between the input data stream and the local oscillator. When the offset is not entirely eliminated, the timing margin of the receiver is reduced significantly. Thus, the reduced timing margin causes a bit error when consecutive identical digits show up. Besides, if the offset exceeds the locking range of an ILO, it could fail to lock. For these reasons, to employ an ILO in CDR applications, a timing calibrator that cancels out the offset is necessary for robust operation over the process, supply voltage, temperature (PVT) variations.

In recently published papers, some efforts to calibrate the frequency offset have been made [38]–[43]. In [39]–[41], a replica oscillator embedded in a PLL forwards the control voltage to an ILO. Thus, the free-running frequency of an ILO, f_{osc}, is set within the locking range of an ILO and the phase is aligned instantly on the input data stream. However, this architecture is vulnerable to the PVT variations due to their structural limitation of replica scheme. In addition, the frequency difference between the input data stream and the external reference clock also causes the frequency mismatches between the two oscillators. Even if these mismatches are small, their impact on performance is critical, resulting in the degradation of the timing margin. To mitigate such performance degradation, an ILCDR using a single oscillator is presented [38]. However, the mismatches are still present as f_{osc} is set from the reference clock, not from the input data stream. The phase locking in [42] and [43] is performed without a reference clock and adopts the conventional PLL-based architecture, which has two-phase tracking paths. One is the direct injection to the

oscillator, and the other is through the phase detector. However, when the two path delays are not correctly calibrated, the frequency offset is inevitably occurred, degrading JTOL performance.

5.2 Proposed ILCDR with Maximum Timing-Margin Tracking

5.2.1 Overall Architecture and Operation Principle

Fig. 5.1 shows the proposed ILCDR architecture. The output clock is modulated by the two paths as mentioned above. When the sum of the two path delays, $\tau_{inj} + \tau_{clk}$, equals to the integer multiples of a bit time, the free-running frequency of an ILO (f_{osc}) is equal to the target frequency, f_{target}. In this work, f_{target} is 5 GHz since the input data rate is 10 Gb/s, and a half-rate clock recovery scheme is adopted. The injection-path delay, τ_{inj}, is continuously adjusted by the 8-bit digitally controlled delay line (DCDL), satisfying the condition using the proposed tracking loop. Since this work

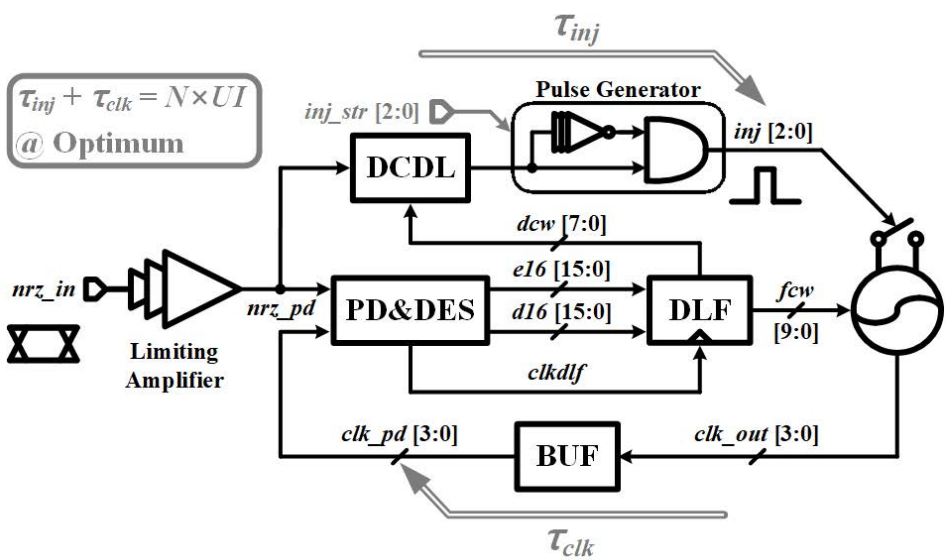
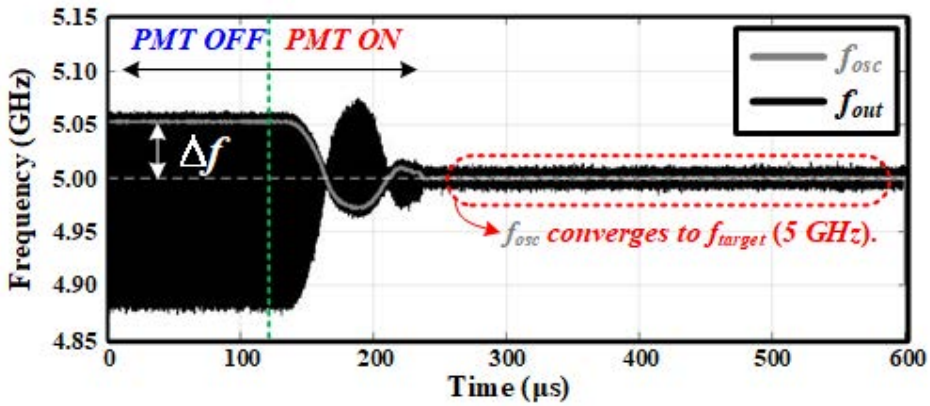
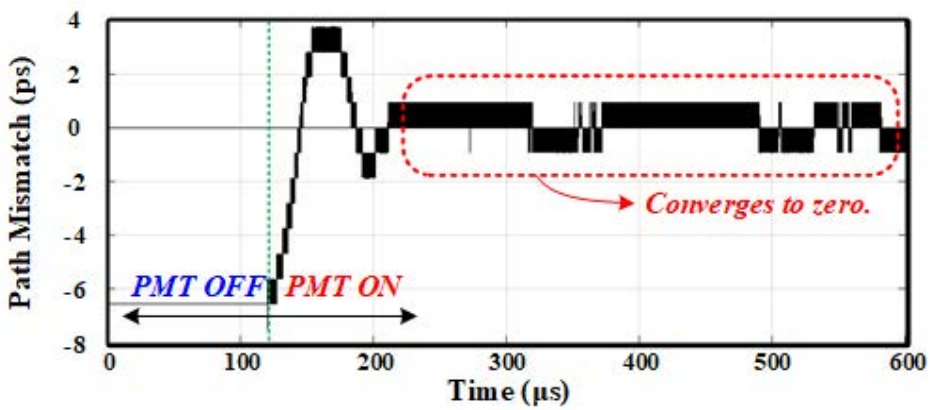


Fig. 5.1 Block diagram of the proposed ILCDR.



(a)



(b)

Fig. 5.2 Behavioral transient simulations of the proposed ILCDR. (a) Frequency versus time. (b) Path mismatch versus time. In this example, injection strength (β) is 0.8, and initial path mismatch is set to –6.56 ps with 10-Gb/s, 2^7–1 PRBS input data pattern.

utilizes only the information of the traditional 2X-oversampling phase detection in CDR, it is implemented with a minimal hardware overhead. The detailed operation of the proposed phase detector for extracting the path mismatch would be covered in following Section II.B.

Fig. 5.2 shows behavioral transient simulations demonstrating the operation of

the proposed path mismatch tracking (PMT) loop. In this simulation, initial path delay mismatch is set to –6.56 ps, and injection strength, β, defined in [14] is 0.8. The input data rate is 10 Gb/s with a $2^7 - 1$ PRBS pattern, which is identical to the test condition in Section 5.4. In Fig. 5.2(a), when the tracking loop is off (<100 μs), the timing mismatch forces the free-running frequency of the oscillator (f_{osc}) to deviate from the target frequency (f_{target}), showing the two-point modulation problem in a conventional structure. The amount of deviation in frequency is a function of the timing mismatch and the injection strength. In other words, the output frequency (f_{out}) is determined by not only the free-running oscillator but also the injection effect. After the PMT loop is enabled (>100 μs), the initial path mismatch is tracked, and finally converges to zero on average as shown in Fig. 5.2(b). Since the path mismatch is diminished owing to the loop, the corresponding free-running frequency of the oscillator (f_{osc}) also goes to the target value (f_{target}), and the amount of variation in the output frequency (f_{out}) is minimized. The timing margin of the sampler is maximized to the half of the unit data interval (0.5 UI) which is the optimal point for error-free operation. In addition, since the free-running frequency of the oscillator converges to the target frequency, it is much more tolerant to the consecutive identical digits than the typical PLL-based ILCDR with path mismatch.

5.2.2 Rising-Edge Injection and Detecting Injection Timing

Fig. 5.3 depicts the conceptual timing diagram under path delay mismatch when the proposed tracking loop is disabled. In this example, the path delay deviation causes the frequency error ($\Delta f = f_{osc} - f_{target} < 0$), and the inj pulse forces the oscillator to move forward in phase. For simplicity, it is assumed that the injection strength is strong enough to replace the original edges, and the CDR loop is also strong enough to correct the edges in every cycle. At the time t_0, the first edge of *clk_pd* [0] is aligned to the rising edge of *nrz_pd* by the CDR loop, and $\Delta\phi$ is zero. However, the next edge is replaced by the pulse injection, and therefore it is not aligned with the falling edge of *nrz_pd* due to the delay deviation. With the two assumptions and the fact that the injection is applied only at the rising edges of the input data stream, the

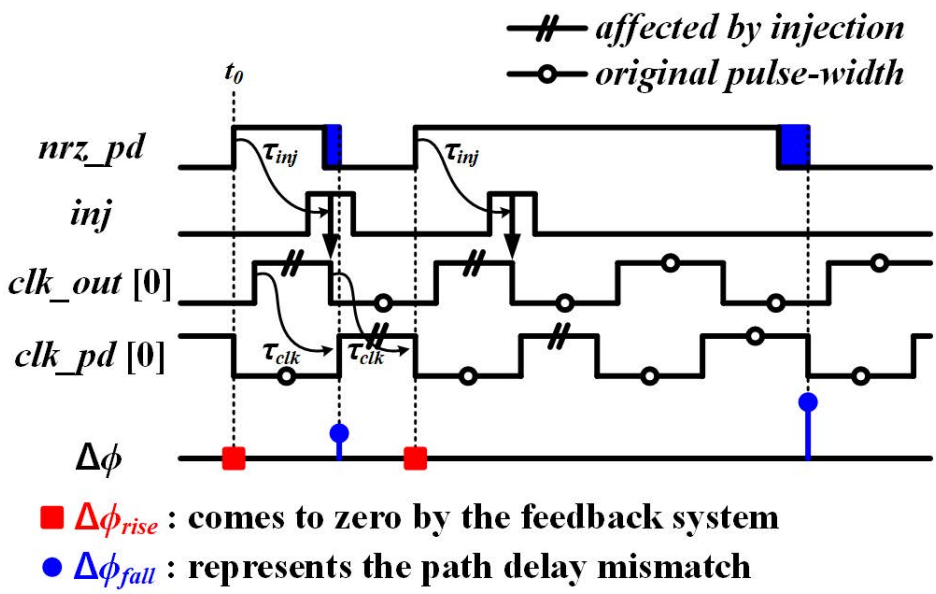


Fig. 5.3 Conceptual timing diagram under path delay mismatch when the PMT loop is disabled.

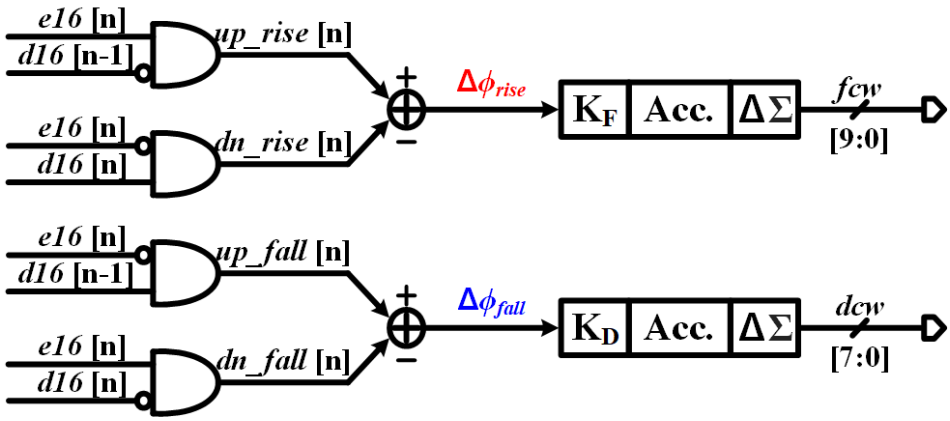


Fig. 5.4 Block diagram of the proposed phase detector in the digital loop filter that detects the path mismatch.

proposed phase detector embedded in the digital loop filter extracts the delay deviation on the two paths as $\Delta\phi_{fall}$.

Fig. 5.4 shows the block diagram of the proposed phase detector in the digital loop filter. To separate the error information, the XOR gates alone in the conventional phase detector are replaced by the AND gates with minimal hardware additives. The errors are divided into $\Delta\phi_{rise}$ and $\Delta\phi_{fall}$ according to the direction of the input data stream, in other words, whether the injection is applied or not. These separated errors are integrated and applied to the ILDCO and DCDL, respectively.

5.3 Proposed ILO

Fig. 5.5 shows the block diagram of the injection-locked digitally controlled oscillator (ILDCO). It consists of four-stage pseudo-differential ring oscillator for quadrature-phase clocks to operate in half-rate clock recovery. Injection cells are designed to short differential nodes in a binary-weighted array for various injection strengths. When an injection cell is disabled, *inj* is tied to low from the pulse generator. The dummy injection switches are equally implemented and tied to low for the rest of the differential nodes to generate accurate quadrature-phase clocks. Frequency tuning is performed using a 10-bit digitally controlled resistor array as described in [44].

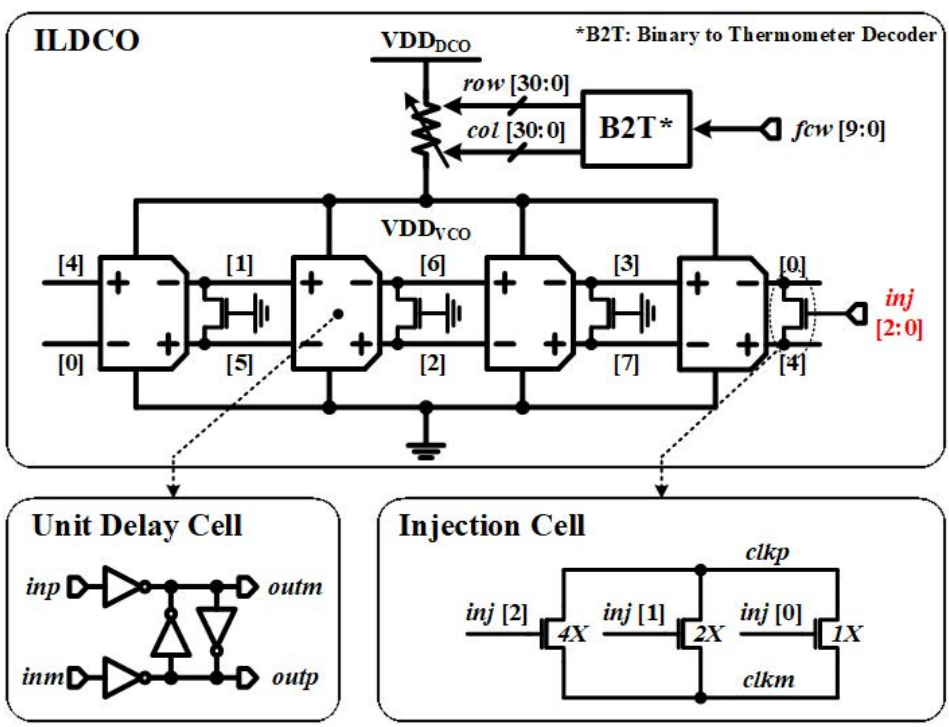
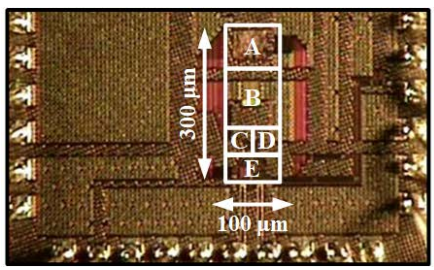


Fig. 5.5 Block diagram of the proposed phase detector in the digital loop filter that detects the path mismatch.

5.4 Measurements

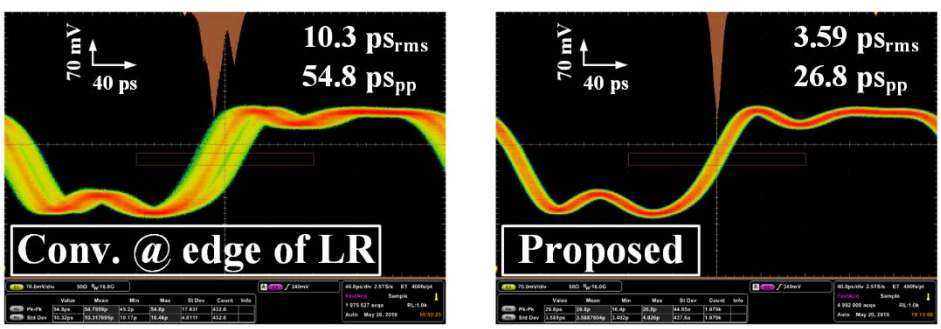
The proposed ILCDR fabricated in 28-nm CMOS technology occupies an active area of 0.03 mm^2 and consumes 12.8 mW at 10 Gb/s with a 0.9-V supply voltage. Fig. 5.6 shows a chip photomicrograph and description of the building blocks with power breakdown. Each power consumption is measured by the digital power source, Agilent B2926A.

Fig. 5.7 shows the measured jitter histograms of the 2.5-GHz recovered clock (divided by two) when the PMT loop is on and off. When the PMT loop is off, the delay control word is fixed to the edge of the locking range, satisfying the bit error rate less than 10^{-12}. As shown in Fig. 5.7(a), the histogram shows the irregular distribution with two peak tones. One is from the free-running frequency of the oscillator (f_{osc}), and the other is from the injection operation. The frequency offset caused by the path mismatch makes deterministic noise, and root-mean-square (rms) and peak-to-peak jitter are 10.3 ps and 54.8 ps, respectively. On the other hand, with the PMT loop on, normal Gaussian distribution is obtained as shown in Fig. 5.7(b), and rms and peak-to-peak jitters are 3.59 ps and 26.8 ps, respectively. From this result, it is found that the frequency offset made by the path mismatch is successfully attenuated using the proposed tracking loop.



	Block Description	Power (mW)
A	Digital Loop Filter	2.6
B	ILDCO	3.38
C	Pulse Gen. & DCDL	6.83
D	PD & Deserializer	
E	Limiting Amplifier	

Fig. 5.6 Chip photomicrograph, block description, and separated power consumption at 10 Gb/s with a 0.9-V supply voltage.

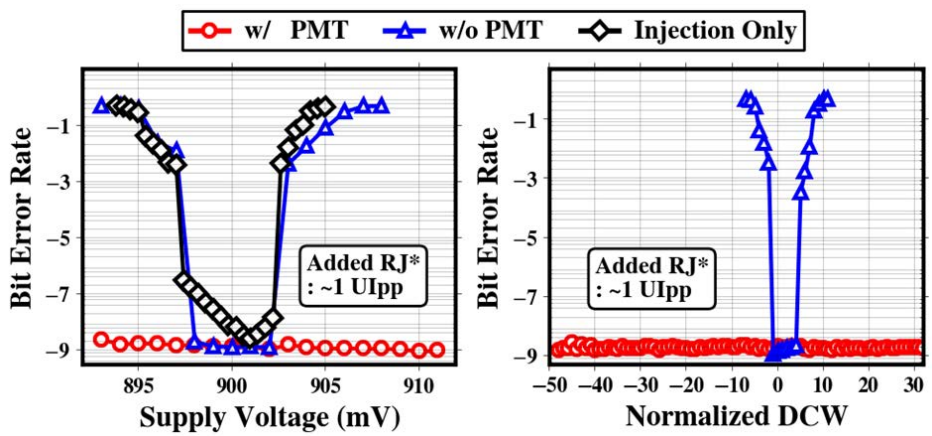


(a) (b)

Fig. 5.7 Measured jitter histograms of the 2.5-GHz recovered clock for (a) the conventional PLL-based ILCDR at the edge of the locking range and (b) the proposed ILCDR, satisfying the bit error rate less than 10^{-12}.

To investigate the effect of the path mismatch and verify the PMT loop, an extra test is performed as shown in Fig. 5.8. In this test, a significant amount of the random jitter (about 1 UIpp) equipped in JBERT, Agilent N4903A, is intentionally added to the input data stream to figure out the operation of the PMT loop, not to estimate the absolute tolerance of the proposed ILCDR. In Fig. 5.8(a), the separated power domains of ILDCO and all other blocks are tied together, and it is swept using the digital power source. Since the supply voltage determines the amount of path mismatch, the typical PLL-based ILCDR without the PMT loop (blue line with triangular markers) shows much narrower locking range than the proposed one (red line with circular markers). In addition, to find out the locking range of the ILDCO itself, an injection is applied to the oscillator with all other feedback loops disabled (black line with diamond markers). Since the frequency of the oscillator is controlled solely by the supply voltage in this test, there is a single point that shows the minimum bit error rate.

In order to further validate the operation of the PMT loop, the delay control words are varied in the same test condition, and the corresponding bit error rates are measured. With the PMT loop on, the initial delay control word is gradually adapted to the optimum value with the flat bit error rate, which is almost equal to the lowest bit error rate of the disabled PMT. In addition, the locking range concerning the delay control words is much wider than the disabled one about ten times.



(a) (b)

***Note that a significant amount of *Random Jitter* (~ 1 UIpp) is intentionally added.**

Fig. 5.8 Measured bit error rate at 10 Gb/s with several different ILCDR with various (a) supply voltage and (b) delay control words. In this test, the random jitter of about 1 UIpp is intentionally added for degradation of bit error rate.

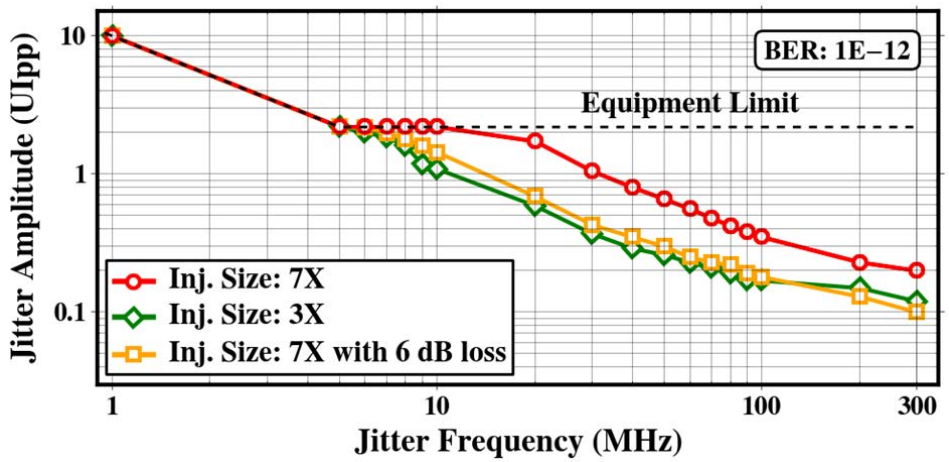


Fig. 5.9 Measured jitter tolerance of the proposed ILCDR for $2^7 - 1$ PRBS pattern at 10 Gb/s with the bit error rate of 10^{-12} in several different test conditions.

Fig. 5.9 shows the measured JTOL for $2^7 - 1$ PRBS pattern at 10 Gb/s with several different test conditions when the target bit error rate is 10^{-12}. The injection strengths and channels of the input data are varied in this test. When the size of the injection cells is 7X as explained in Fig. 2, the proposed ILCDR tolerates 1-UIpp sinusoidal jitter amplitude at the frequency of 31 MHz (red line with circular markers). In the other condition, the injection size is changed to 3X, and it shows the degraded JTOL performance compared with the strong injection since the injection strength determines the bandwidth of the overall architecture. In addition, to investigate the effect of inter-symbol interference, lossy channel (6-dB loss at the Nyquist frequency) is used with 7X injection size (yellow line with square markers). With 6-dB lossy channel, it achieves over 10-MHz jitter frequency when 1-UIpp sinusoidal jitter amplitude is applied.

Table 5.1 Performance Summary and Comparison.

	ISSCC'08 [6]	JSSC'15 [7]	JSSC'16 [8]	This Work
Technology (nm)	250	90	28	28
Architecture	Full rate	Full rate	Half rate	Half rate
Oscillator Type	GVCO (RING)	ILO (RING)	ILO (RING)	ILO (RING)
Supply Voltage (V)	3.3 / 1.8	1.2	0.9	0.9
Data Rate (Gb/s)	10.3125	2.2	1 – 12	10
Power (mW)	856	6.1	22.9[3] / 11.0[4]	12.8
Bit Error Rate	$< 10^{-12}$	$< 10^{-12}$	$< 10^{-9}$	$< 10^{-12}$
Jitter Tolerance	1.0 UIpp @ 20 MHz[1] 0.27 UIpp @ 80 MHz	1.0 UIpp @ 4 MHz[1] 0.3 – 0.6 UIpp @ 10 MHz	1.09 UIpp @ 100 MHz 0.56UIpp @ 300 MHz[5]	1.0 UIpp @ 31 MHz 0.2 UIpp @ 300 MHz
Active Area (mm^2)	9.0	0.44	-	0.03
Energy Efficiency (pJ/bit)	83.01	2.77[2]	1.9[3] / 0.9[4]	1.28
Path Mismatch Tracking	No	No	Yes	Yes

[1] Estimated from JTOL results.

[2] Excluding limiting amplifier.

[3] Including analog front end, de-multiplexer, and excluding digital logics.

[4] Excluding analog front end, de-multiplexer, and digital logics.

[5] Measured by the internal calculation circuits, not external equipment.

Table 5.1 summarizes the performance and compares with other recently published ILCDRs. This work shows the best JTOL performance between the works [37]–[43] satisfying the bit error rate less than 10^{-12} as 1-UIpp amplitude at the sinusoidal jitter frequency of 31 MHz. In addition, the proposed ILCDR achieves the highest energy efficiency of 1.28 pJ/bit among the fully functional ILCDR chips published in the literature.

Chapter 6

Conclusion

In this dissertation, various circuit techniques employing injection-locked oscillator (ILO) are proposed. At first, an injection-locked phase-locked loop (ILPLL) utilizing a timing calibrator is presented. Since the ILPLL alone cannot achieve a robust jitter performance over PVT variations, in this work, by continuously tracking an injection timing using half-edge injection and separated error information from the phase detector, consistent operation on ILPLL is guaranteed and verified in experiments by varying supply voltage and timing of injection.

Secondly, we presented a phase domain response (PDR) analysis for the physically implementable injection-locked oscillator (ILO). Based on the analysis, a new ILO with compensation switches that mitigate the highly asymmetric characteristic of the PDR is proposed. Besides, for a high-speed operation employing

injection technique, this work excludes the pulse generator before injection happens. Thanks to the compensation current and the exclusion of the pulse generator, this work achieves a minimum reference spur and integrated jitter in both at the 15-GHz clock. The proposed ILPLL shows integrated jitter from 1 kHz to 40 MHz of 213 fs while achieving a power consumption of 17.81 mW at a clock rate of 15 GHz.

And last, it describes a new injection-locked clock and data recovery circuit (ILCDR) that continuously tracks the frequency offset between the input data stream and the local oscillator. The proposed ILCDR adjusts the conventional phase detector with respect to the polarity of the data transition. By employing the strong injection at the rising edges of the input data stream and the path-tracking loop, the proposed ILCDR achieves the exceptional jitter tolerance performance and remarkable energy efficiency compared with the existing ILCDR architectures.

Appendix A

PDR Simulation Deck using HSPICE

From the phase domain response (PDR), the characteristics of the injection-locked oscillator (ILO) are obtained such as the injection strength or the locking range. Therefore, an accurate PDR estimation should be carried out in advance of designing the overall structure employing ILO such as ILPLL or ILCDR. Elementary PDR-simulation results are illustrated in Fig. A.1. According to the definition of the PDR, the input phase should be swept to get meaningful results. Preparatory to performing main PDR simulation, the timing range is limited from –180° to +180° without the injection as shown in Fig. A.1 to obtain the consistent results irrespective of the operating frequency. In addition, the period is measured to convert the time-domain data into the phase domain. Subsequently, with the timing information extracted from the previous simulation in the absence of the injection, the input phase is swept from –180° to +180° and its output phase shift is measured after 10 or 20 cycles to avoid the amplitude-fluctuation effect as mentioned in [11]–[13]. Moreover, the parameters such as the injection-cell size or the injection duration can be varied using a simple TCSH script as shown in Fig. A.2. Numerous results of the PDR simulation are shown in Fig. A.3.

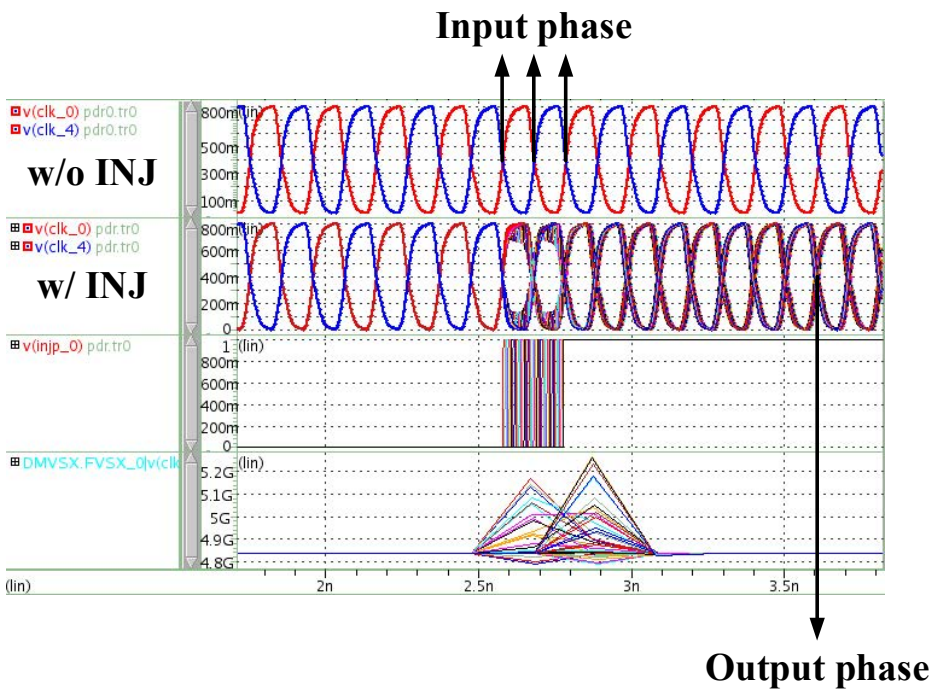


Fig. A.1 PDR example in transient simulation.

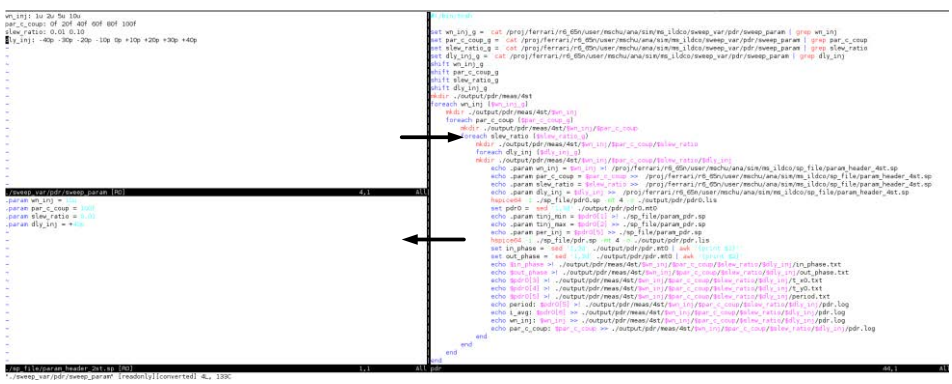


Fig. A.2 PDR-simulation procedure using TCSH language.

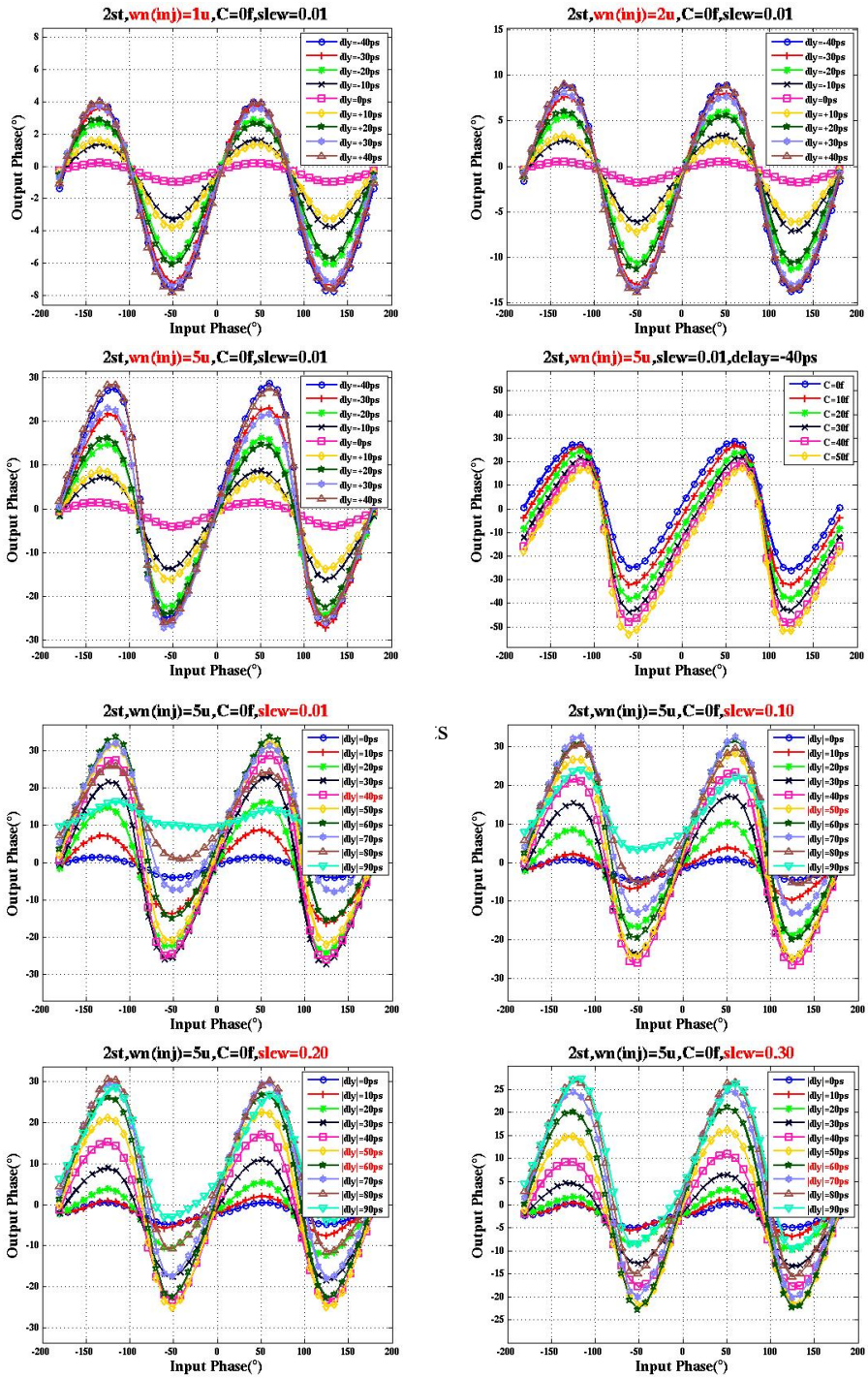


Fig. A.3 Various PDR simulation results.

Appendix B

Measurement Automation using Python Language

B. 1 Motivation

Most of the test setups for the chip designers are quite simple and repeated work. For example in the design of clock synthesis, we have to measure the phase noise and the spectrum of the output clock. Moreover, to get the best result in “already” fabricated chip, usually, a numerous time should be spent for sweeping supply voltage or several digital parameters we can control. All of these actions can be replaced using the Python language. Since all of the test sequences is automated with the help of the Python, every result from the test is more reliable than hand-involved test setups. Also, we could implement the test at any time, for instance, everybody in the laboratory leave work; the best test condition to get a better noise performance. In short, minimizing the involvement of the man, we can save the meaningless time-consuming in front of the equipment by adjusting the test condition by hand. Moreover, we can find the best test condition from the already fabricated product, spending minimum time.

B. 2 Implementation

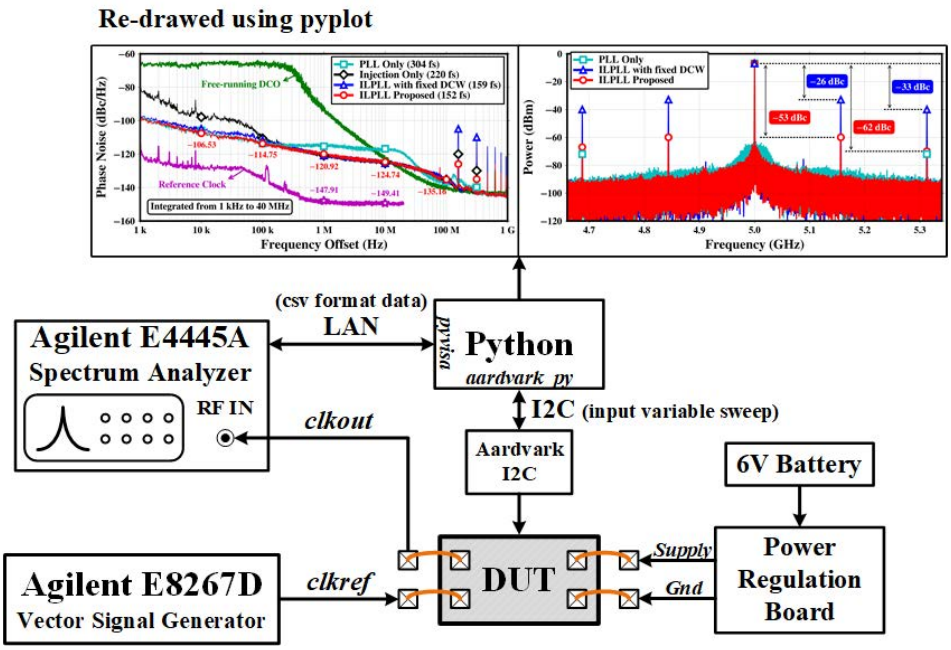


Fig. B.1 An example of measurement automation using python.

At first, we had to find a way to communicate the I2C interface using the Python language. If the I2C data bus can be controlled, we can make the simple loop to perform the various test conditions. Fortunately, “aardvark_py” package from TOTALPHASE provides the Total Phase Aardvark Python API package for easy distribution and installation via PyPI [4]. From this library, we can easily read/write the data bus implemented in I2C.

Secondly, we have to communicate between the instrument and personal computer. It can be performed using “pyvisa” library [3]. From the package, we can control the equipment without manually pressing the button. For example in the meas-

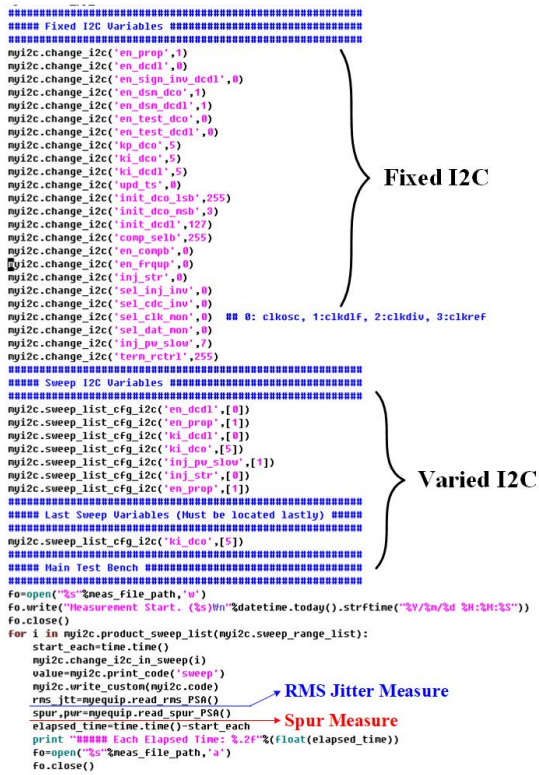


Fig. B.2 An example of main test bench using python.

urement in Chapter 3 of ILPLL, after the I2C data is controlled employing the "aardvark_py" library, then, we start to measure the phase noise of the output clock. After the measurement is finished, a spectrum analysis begins, and the spur level is measured using the command embedded in the spectrum analyzer, Agilent E4440A. Fig. B.2 shows the top test bench having similar syntax with HSPICE. Fig. B.3(a) shows the output command after one measurement is done and Fig. B.3(b) shows the saved data from the automation procedure. Detailed code description or more information about our work can be delivered via email address (mschoo@isdl.snu.ac.kr).

선택 C:₩WINDOWS₩system32₩cmd.exe - python main.py test.csv

```
var_name:en_sign_inv_dcdl,value:0
var_name:upd_ts,value:0
var_name:upd_inj,value:0
var_name:inj_pw_slowp,value:255
var_name:inj_pw_slowm,value:0
var_name:inj_str,value:7
var_name:comp_str,value:4
var_name:en_prop,value:0
var_name:en_dcdl,value:0
var_name:init_dcdl,value:32
```

Var name	Value(dec)	Value(hex)
en_prop	0	00
inj_pw_slowp	255	FF
upd_inj	0	00
inj_str	7	07
comp_str	4	04
inj_pw_slowm	0	00
ki_dco	7	07
init_dcdl	32	20
en_dcdl	0	00
upd_ts	0	00
en_sign_inv_dcdl	0	00

```
##### Measured RMS Jitter_Trac2: 322.50 (fs)
##### Measured RMS Jitter_Trac1: 325.10 (fs)
##### Measured Spur Level_Right: -34.14 (-dBC)
##### Measured Spur Level_Left: -32.09 (-dBC)
##### Measured Carrier Power: -20.97 (-dBC)
##### Each Elapsed Time: 96.42
```

(a)

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파일(F) 편집(E) 서식(O) 보기(V) 도움말(H)

```
Measurement Start. (2018/10/25 09:53:08)
72, 10630.70, 11109.08, -25.00, -28.45, -28.23
73, 11502.75, 13662.60, -29.80, -30.02, -25.49
74, 9277.15, 9993.03, -22.63, -25.02, -27.56
75, 513.54, 556.03, -24.02, -24.54, -21.90
76, 431.78, 432.46, -10.65, -11.86, -60.28
77, 408.17, 406.85, -24.52, -25.15, -21.88
78, 385.07, 382.93, -24.86, -25.63, -21.86
79, 314.52, 311.79, -48.48, -48.89, -21.83
80, 357.68, 355.26, -25.98, -27.03, -21.83
81, 347.92, 344.29, -26.54, -27.53, -21.83
82, 346.41, 343.78, -27.00, -28.20, -21.82
83, 339.80, 336.53, -28.12, -29.25, -21.83
84, 333.41, 330.06, -28.89, -30.20, -21.82
85, 333.28, 330.67, -30.07, -31.62, -21.80
86, 327.20, 323.62, -31.17, -32.80, -21.80
87, 321.45, 318.22, -32.95, -34.78, -21.82
88, 317.35, 313.60, -35.90, -37.80, -21.83
89, 317.16, 314.49, -38.37, -40.89, -21.82
90, 315.98, 313.36, -41.27, -45.24, -21.83
91, 314.52, 311.79, -48.48, -48.89, -21.83
```

(b)

Fig. B.3 An example with (a) output command while one measurement is done and (b) saved data after several measurements are performed.

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국문 초록

본 논문에서는 고속 시리얼 링크에서 사용할 수 있는 주입-고정화 기술 (Injection-locking technique) 을 제안한다. 클럭 생성기에서는, 깨끗한 레퍼런스 클럭의 에지를 직접 발진기 (oscillator) 에 주입하기 때문에, 좋은 지터 특성을 얻을 수가 있다. 그러나, 레퍼런스 클럭과 발진기의 주파수가 정확하게 맞지 않으면, 최적의 동작 상태를 보장할 수 없다. 또한, 넓은 밴드위스를 얻기 위하여 주입 세기 (Injection strength) 는 가장 강한 값을 가질 수 있도록 설계하여야 한다.

첫번째로, 기존의 주입-고정 위상-동기화 루프 (Injection-locked phase-locked loop) 에 존재하는 경로 불일치 (path mismatch) 문제를 절반-에지 주입 (half-edge injection) 기술과 뱅뱅 위상-주파수 검출기 (bang-bang phase-frequency detector) 의 결과를 나누는 방법으로 해결하였다. 경로 불일치 문제를 해결함으로써, 레퍼런스 클럭과 발진기 사이의 주파수 차이가 평균적으로 없어졌으며, 이로 인하여 주입 고정의 효과를 극대화 할 수 있었다. 제안하는 주입-고정 위상-동기화 루프는 0.9 V 의 정격 전압과 5 GHz 의 클럭 속도에서 5.65 mW 의 전력을 소모한다. 1 kHz 에서 40 MHz 까지 적분된 지터의 양은 152 fs 이며, 레퍼런스 클럭 주파수 대역과와 2분주 대역에서의 측정된 스퍼의 양은 각각 –62 dBc 와 –53 dBc 이다.

두번째로, 주입-고정 위상-동기화 루프의 밴드위스를 넓게 가져가기 위하여, 주입 세기를 최대한 높은 값으로 만들 수 있는 기술을 제안한다. 주입-고정 발진기 (injection-locked oscillator) 의 위상 영역 응답 (phase domain response) 을 실제 구현된 회로에 대하여 분석하고, 이를 변형함으로써, 정확한 위상 영역 응답을 구할 수 있었으며, 최적의 동작 영역 또한 확보할 수가 있었다. 제안하는 주입-고정 위상-동기화 루프는 1.3 V 의 정격 전압과 15 GHz 의 클럭 속도에서 17.8 mW 의 전력을 소모하였고, 적분된 지터의 양은 213 fs 이고, 레퍼런스 스퍼의 양은 –51 dBc 이다.

세번째로, 클럭 및 데이터 복구 회로 설계에 있어서, 높은 지터 내성 (jitter tolerance) 특성을 얻기 위하여 주입-고정 발진기가 사용되었다. 주입-고정 위상-고정화 루프에서와 마찬가지로, 경로 불일치 문제를 제안하는 추적 루프를 이용하여 해결하였다. 제안하는 추적 루프는 기존의 위상 검출기를 변형하는 방식으로 설계가 되었고, 이를 통해 최적의 동작 영역을 보장할 수가 있다. 수신기 앞단의 샘플러에서의 타이밍 마진을 최대한으로 보장할 수 있는 제안하는 회로는 31 MHz 의 사인 지터 주파수에서 1 UIpp 의 지터 크기에서 10^{-12} 보다 적은 비트 에러율을 보인다. 또한, 제안하는 주입-고정 클럭 및 데이터 복구 회로는 10 Gb/s 의 데이터 속도에서 1.28 pJ/bit 의 에너지 효율을 가진다.

주요어: 올 디지털 위상-고정화 루프, 주입-고정 발진기, 주입-고정 위상-고정화 루프, 주입-고정 클럭 및 데이터 복구, 주입 타이밍 추적, 위상 도메인 반응

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