이학박사 학위논문

Highly integrated time-based data acquisition system using FPGA for PET scanners

FPGA를 이용한 시간 기반 고집적 PET 데이터 수집 장치

2019 년 7 월

서울대학교 대학원
의과학과

원 준 연

Thesis for the Degree of
Doctor of Philosophy in Science

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July 2019

Seoul National University Graduate School
Major in Biomedical Sciences

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Abstract

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Positron emission tomography (PET) is a widely used functional imaging device for diagnosing cancer and neurodegenerative diseases. PET instrumentation studies focus on improving both spatial resolution and sensitivity to improve the lesion detectability while reducing radiation exposure to patients.

The silicon photomultiplier (SiPM) is a photosensor suitable for high-performance PET scanners owing to its compact size and fast response. However, the SiPM-based PET scanners require a large number of readout channels owing to a high level of granularity. For example, the typical whole-body PET scanners require more than 40,000 SiPM channels. Therefore, the highly integrated data acquisition (DAQ) system that can digitize a large number of SiPM signal with preserving its fast temporal response is required to develop the high-performance SiPM-based PET scanners.

Time-based signal digitization is a promising method to develop highly

integrated DAQ systems owing to its simple circuitry and fast temporal response. In this thesis, studies on developing highly integrated DAQ systems using a field-programmable gate array (FPGA) were presented.

Firstly, a 10-ps time-to-digital converter (TDC) implemented within the FPGA was developed. The FPGA-TDCs suffer from the non-linearity, because FPGAs are not originally designed to implement TDC. We proposed the dual-phase sampling architecture considering the FPGA clock distribution network to mitigate the TDC non-linearity. In addition, we developed the on-the-fly calibrator that compensated the innate bin width variations without introducing the dead time.

Secondly, the time-based SiPM multiplexing and readout method was developed using the principle of the global positioning system (GPS). The signal traces connecting every SiPM to four timing channels were used to encode the position information. The position information was obtained using the innate transit time differences measured by four FPGA-TDCs. In addition, the minimal signal distortion by multiplexing circuit allowed to use a time-over-threshold (ToT) method for energy measurement after multiplexing.

Thirdly, we proposed a new FPGA-only digitizer. The programmable FPGA input/output (I/O) port was configured with stub-series terminated logic (SSTL) input receiver, and each FPGA I/O port functioned as a high-performance voltage comparator with a fast temporal response. We demonstrated that the FPGA can be used as a high-performance DAQ system by directly digitizing the time-of-flight (TOF) PET detector signals using the FPGA without any front-end electronics.

Lastly, we developed comparator-less charge-to-time converter (QTC) DAQ systems to collect data from a prototype high-resolution brain PET scanner. The energy channel consisted of a QTC combined with the SSTL input receiver of the

FPGA. The timing channel was a TDC implemented within the same FPGA. The detailed structure of brain phantom was well-resolved using the developed high-resolution brain PET scanner and the highly-integrated time-based DAQ systems.

Keyword : Data acquisition (DAQ) system, Field-programmable gate array (FPGA), Positron Emission Tomography (PET), Silicon photomultiplier (SiPM), Time-of-flight (TOF), Time-to-digital converter (TDC)

Student Number : 2013-21782

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Chapter 1. Introduction

1.1. Background

1.1.1. Positron Emission Tomography

Positron emission tomography (PET) is a functional imaging tool to visualize the distribution of the injected positron-emitting radiopharmaceutical, and thus widely used to diagnose cancer and neurodegenerative diseases. The studies on PET instrumentations have focused on improving spatial resolution, signal-to-noise ratio (SNR), and sensitivity to detect small lesion and to reduce radiation dose to patients. High spatial resolution can be achieved by using small-pitch scintillation crystal and photosensor [1-4]. High SNR can be achieved by measuring time-of-flight (TOF) information of annihilation photon pairs [5-7]. High sensitivity can be achieved by extending the axial length of the PET scanner [8, 9].

1.1.2. Silicon Photomultiplier

The silicon photomultiplier (SiPM) is a photosensor suitable for high-performance PET scanners. Firstly, compact size enables not only the high-resolution scintillation crystal identification [3, 4] but also one-to-one coupling to improve timing resolution [10, 11]. Secondly, fast temporal response and high gain allow TOF measurement [10, 11]. Lastly, the SiPM is a cost-effective photosensor that can be used long-axial field-of-view (FOV) PET scanners owing to mass production using CMOS technology [9].

However, the high level of granularity in SiPM is a major challenge in developing SiPM-based PET scanners. Individual signal digitization requires the complex and large volume of data acquisition electronics.

1.1.3. Data Acquisition System

Typical data acquisition (DAQ) systems consist of energy, timing channels, field-programmable gate arrays (FPGAs), and auxiliary digital electronics [12, 13] as shown in Figure 1-1. The energy channel processes the energy and position information from the detectors with light sharing and/or charge division circuit. It consists of analog-to-digital converters (ADCs). The digitized values by ADCs are input into the FPGA that accumulates values for a predetermined period to obtain energy and position information. The timing channel processes the arrival time and thus TOF information of gamma-rays. It consists of high-speed amplifiers, comparators, and digital-to-analog converters (DACs). The comparator generates a digital timing pulse when the leading edge of the signal crosses the threshold voltage applied by a DAC. The digital timing pulse is input into a time-to-digital converter (TDC) that can measure the arrival time with precise time resolution. Currently, TDCs are usually implemented within the FPGA.

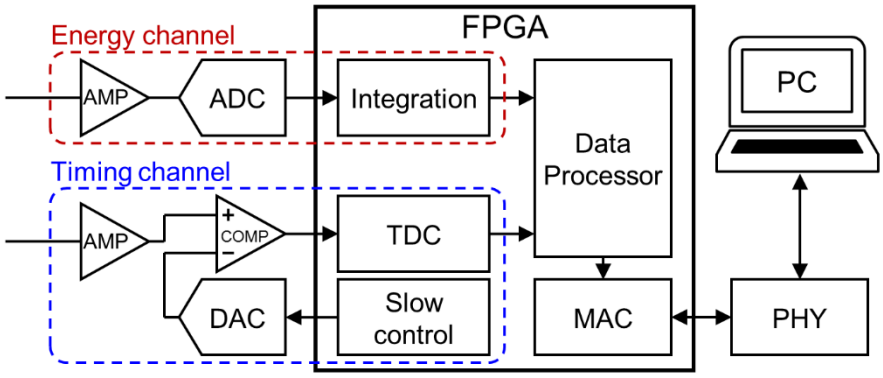

Figure 1-1. Conventional DAQ system.

1.1.4. Time-based Signal Digitization Method

Time-based signal digitization methods that use timing channels to obtain both energy and timing information are widely used to simplify DAQ systems and further to increase the number of readout channels for SiPM-based PET scanners, because the timing channel is much smaller, simpler, and more power-efficient than the energy channel.

Time-over-threshold (ToT) method is a straightforward time-based signal digitization method by applying a single threshold to the signal and extract the energy and timing information from the pulse width and the transition time, respectively [14] as shown in Figure 1-2 (a). This method has the advantage that it requires only a single voltage comparator for both energy and timing measurements. However, the ToT method has the disadvantages of non-linear energy measurement and poor energy and/or timing resolutions. The low threshold to detect the early photons degrades the energy resolution and the high threshold for energy discrimination deteriorates the timing resolution. Thus, the dual-threshold method to apply low and high thresholds for the timing and energy channels, respectively, was developed to obtain good energy and timing resolutions for the TOF PET detectors [15, 16] as shown in Figure 1-2 (b).

A dynamic ToT method uses a single voltage comparator with an adaptive threshold to improve energy linearity and resolution as shown in Figure 1-2 (c). The threshold starts at a low level and increases gradually after the signal crosses the low threshold. This method can achieve both good energy and timing resolution because low and high thresholds are used for timing and energy measurements, respectively. However, the dynamic requires complex threshold circuits such as a monostable vibrator [17] or a DAC [18].

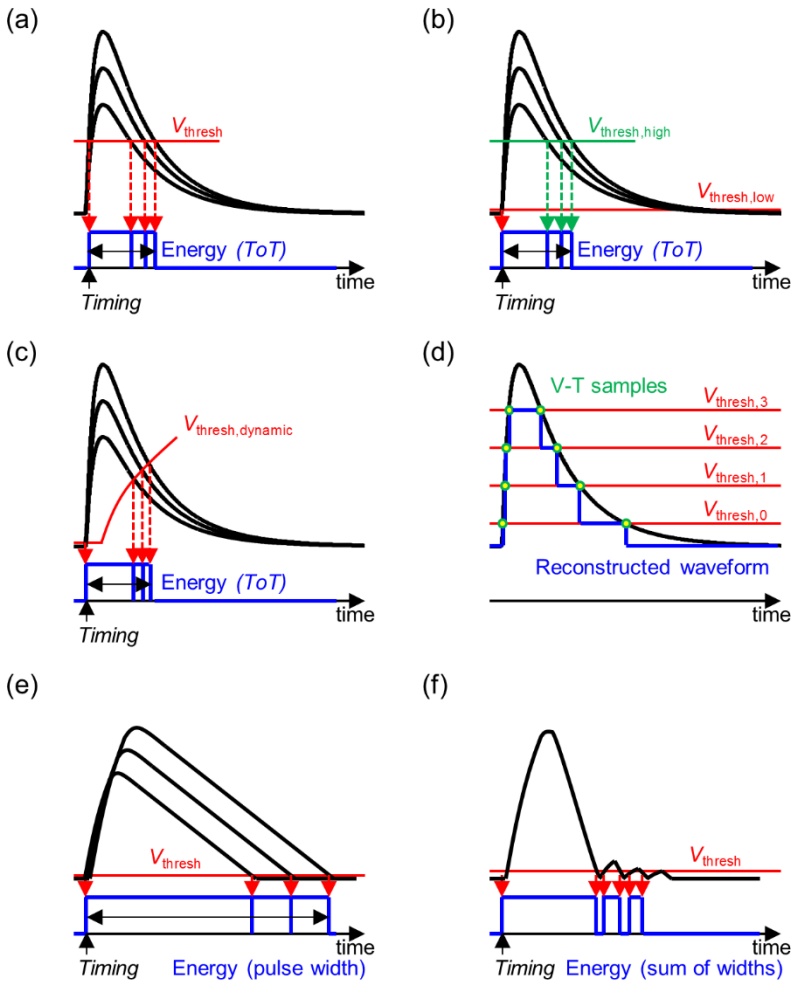

Figure 1-2. Time-based signal digitization methods. (a) Simple ToT with a single threshold. (b) Dual-threshold ToT. (c) Dynamic threshold ToT. (d) Multi-voltage-threshold. (e) Charge-to-time converter. (f) 1-bit sigma delta modulation.

The multi-voltage threshold (MVT) method uses multiple comparators and obtains multiple samples to reconstruct the analog signals [19, 20] as shown in Figure 1-2 (d). The energy and timing information is extracted from the reconstructed signals. However, the MVT method requires multiple comparators for each signal, thus degrading the level of integration.

The charge-to-time converter (QTC) involves the integrator [21, 22] as shown

in Figure 1-2 (e). This method collects the charge and provides a dual-slope pulse of which width is proportional to the input charge. The advantage of the non-gated QTC is a simple circuitry, because it automatically controls its idle, charge, and discharge phases using a diode. The gated QTC is complex to implement because it requires digitally controlled switches and associated digital controllers; however, has the advantage that it can modify the integration window [23]. In addition, a 1-bit sigma-delta modulator adaptively discharges the charges stored in the feedback capacitor in the integrator. It measures energy as the sum of the modulated pulse is greater than the threshold voltage [24, 25] as shown in Figure 1-2 (f).

A new approach to using the FPGA as a digitizer significantly improves the level of integration of the time-based signal digitization method [20, 24-26]. The digital low-voltage differential signaling (LVDS) input receiver of FPGA can be used as a voltage comparator for signal digitization and the logic state of the receiver is directly processed by a TDC implemented within the same FPGA. However, each LVDS input receiver requires a pair of configurable input/output (I/O) ports of FPGA, and thus this method has the drawback that the number of readout channels is less than half the total number of available I/O ports.

Therefore, the FPGA-based time-based digitization is a promising method to implement the highly integrated DAQ systems for the SiPM-based PET scanners.

1.2. Purpose of Research

The aim of this thesis is to develop highly-integrated time-based DAQ systems. The time-based DAQ system is a device that collects energy, position and timing data using only time information.

In Chapter 2, the TDC implemented in the FPGA was presented. Two new architectures for FPGA-TDC were developed. The first architecture is a dual-phase sampling of delay-line considering the FPGA clock distribution network. The second architecture is an on-the-fly calibration method that measures bin-width fluctuations due to PVT variations and reflects updated bin widths in time measurements automatically.

In Chapter 3, a new time-based SiPM multiplexing method was presented. The crystal position was encoded using the innate transit times from each SiPM to readout channels. The crystal position can be identified using the time difference of arrival (TDOA) positioning method widely used in the global positioning system (GPS). Compared with the conventional multiplexing method that requires four ADCs, four TDCs were used.

In Chapter 4, the FPGA-only digitization method was presented. The SiPM signal was directly digitized by FPGA without any amplifiers. In addition, compared with the conventional DAQ system, no discrete comparator and ADC are required. The FPGA I/O port was configured with stub-series terminated logic (SSTL) that is widely used in the memory interface. The energy information was obtained using a ToT method and the timing information was obtained using the FPGA-TDC.

In Chapter 5, the highly integrated 165-channel comparator-less QTC DAQ system for high-resolution brain PET scanners was presented. The energy chain was

implemented by combining a QTC with the SSTL input receiver to improve energy linearity. The dual-slope output of QTC was directly digitized by an FPGA. The timing chain was a TDC implemented within the same FPGA. The detailed structure of the Hoffman brain phantom was clearly resolved using the developed time-based DAQ systems and the brain PET scanners.

Chapter 2. FPGA-based Time-to-Digital Converter

2.1. Background

TOF measurement of annihilation gamma pair can improve the image quality of the PET scanner [5-7, 27]. Because the gamma-ray propagates with the speed of light, the precise time measurement device is required to measure the TOF difference of gamma pairs.

The time-to-digital converter (TDC) is a precise time measurement device. The FPGA-TDC is widely used for TOF PET scanners, because the number of channels and the resolution can be configurable and TDC can be embedded into the data processing FPGA.

Most FPGA-TDCs use coarse-fine architecture [28-41]. The coarse counter operating the main clock frequency provides a coarse time with a resolution of the time period and covers a wide dynamic range. The fine time interpolator provides a sub-clock-period time with a fine resolution covers one clock period. The primitive carry chain for fast arithmetic operation is usually used to implement the delay line of the fine time interpolator. However, the carry chain is not originally designed for precise time measurement, most FPGA-TDCs suffer from the non-linearity. Non-linearity is all deviations from the ideal TDC with uniform resolution.

We developed the dual-phase tapped-delay-line architecture considering the clock distribution network [38] and the bin-width tuning method [39] to mitigate the bin width variations. In addition, we developed a fast on-the-fly bin width calibration method to measure the bin width variations and reflect them in the time measurement to reduce the uncertainty [38].

2.2. Materials and Methods

2.2.1. Tapped-Delay-Line TDC

The tapped-delay-line (TDL) is a fundamental block to implement the fine time interpolator of the TDC [29-41] as shown in Figure 2-1. The asynchronous hit signal propagates along the TDL with changing the logic states of the delay elements until the hit signal synchronizes with the rising edge of the main clock signal. The flip-flops operating at the main clock signal sample the propagation states of the TDL and provide a thermometer code. The fine-code encoder converts the thermometer code into a fine code in two steps. The thermometer code is converted into a one-hot code using multiple bubble suppressor [40]. The fat-tree encoder converts the one-hot code to the binary code [39]. The coarse counter is a binary counter operating at the main clock period of T_0. The hit detect flag is generated during one clock period when the first logic state of the TDL is inverted. The hit detect flag is delayed by 9 clock periods using a shift register (SRG) and then latches the coarse count N and the fine code. The fine-time interpolator converts the fine code into the fine time f with a dynamic range of T_0. The code density test is used to measure the individual bin widths and reflect them into fine time measurements [38, 40]. The hit arrival time t_{arr} is calculated as in (2.1).

$$t_{\mathrm{arr}} = N \times T_0 - f \tag{2.1}$$

The carry chain is widely used to implement the TDL and the total propagation time of the TDL should be greater than T_0.

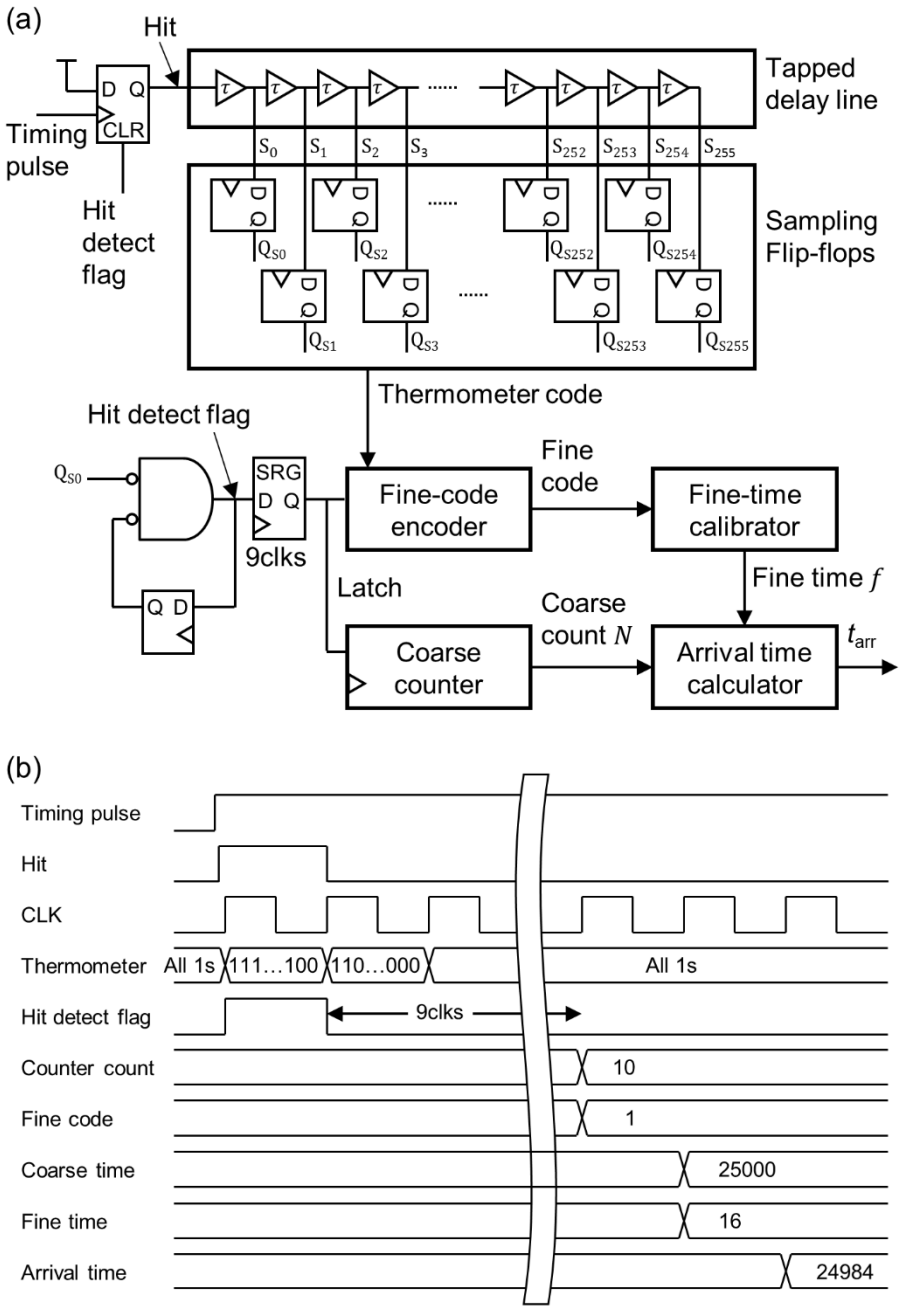

Figure 2-1. Tapped-delay-line TDC. (a) Architecture. (b) Timing diagram.

2.2.2. FPGA

The Virtex-6 evaluation kit (ML605, Xilinx) was used to implement TDC. The FPGA consists of the array of configurable logic blocks (CLBs) that can be driven by the clock buffers.

The CLB consists of look-up tables (LUTs), multiplexers, a carry logic, and distributed memories. Each carry logic is a carry look ahead logic and has four sums and four carry out. The carry logic can be cascaded to increase the total propagation time.

The global buffer located at the center of the FPGA can feed clock signals all the CLBs. In addition, the FPGA has multiple clock regions where the CLBs in the same clock region have the minimum clock skew.

2.2.3. Dual-Phase TDL TDC with On-the-Fly Calibrator

2.2.3.1. FPGA Clock Distribution Network

TDL implementation on the single clock region can mitigate the non-linearity, because the CLBs in the same clock region have the minimum clock skew. Figure 2-2 shows the clock delays and the clock skews for the TDL with 960 bins on the Virtex-6 evaluation kit. The Virtex-6 FPGA has 2×6 clock regions and each clock region is 40 CLBs high. The inter-clock-region clock skew was less than 2 ps; however, the intra-clock-region clock skew was greater than 100 ps.

The clock region crossing of TDL can cause ultra-wide bin or several missing bins [38]. In the case where the TDL crosses from the long- to the short-clock-delay region as shown in Figure 2-3 (a), the last bin of the long-clock-delay region becomes the ultra-wide bin. There is a clock skew T_{skew} when the flip-flops in the short-clock-

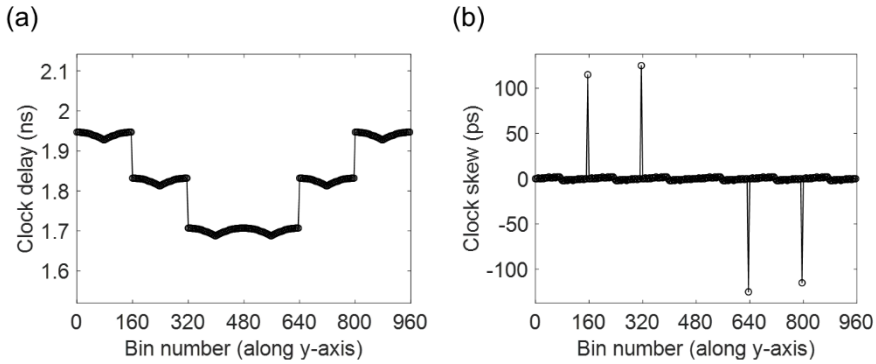

Figure 2-2. The clock distribution network of the Virtex-6 FPGA. (a) Clock delay. (b) Clock skew.

delay region sample the propagation states, but those in the long-clock-delay region do not sample the propagation states. If a transition propagates through the short-clock-region during this period, then the propagation states stored in the flip-flops in the short-clock-delay region are "*unpropagated*" sequences, although the transition has already propagated. After T_{skew}, those in the long-clock-delay region sample the propagation states, in which the last bin of the long-clock-delay region is "*propagated*". Thus, T_{skew} is added to the bin width of the last bin of the long-clock-delay region and the last bin becomes the ultra-wide bin. In contrast, in the case where the TDL crosses from the long- to the short-clock-delay region as shown in Figure 2-3 (b), the invalid thermometer code causes several missing bins. The flip-flops of the short-clock-delay region near the boundary can sample the valid propagation pattern of "*propagated, unpropagated*". However, After T_{skew}, those in the long-clock-delay region also sample the propagation pattern of "*propagated, unpropagated*", because the transition continues to propagate along the TDL. Thus, the invalid thermometer pattern of "*propagated, unpropagated, propagated, unpropagated*" appears in the vicinity of the boundary between the short- and the

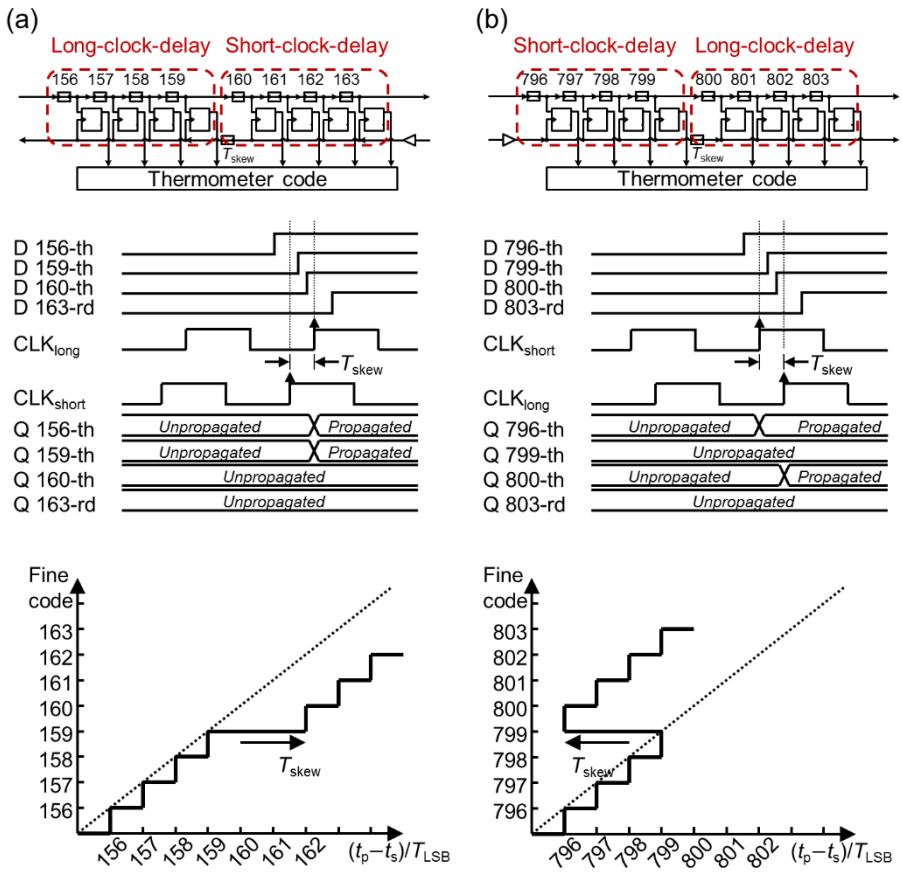

Figure 2-3. Timing diagrams and transfer functions of TDC in case of clock region crossing. (a) Clock region crossing from a long- to a short-clock-delay region. (b) Clock region crossing from a short- to a long-clock-delay region.

long-clock-delay region.

In the TDC transfer function, as shown in Figure 2-3, where t_p and t_s correspond to the propagation time along the delay line and the relative sampling time, respectively, early sampling shifts the transfer function of the short-clock-delay region to the right by T_{skew}, and thus introduces the ultra-wide bin. On the other hand, late sampling shifts the transfer function of the long-clock-delay region to the left by T_{skew}, causing the ambiguity in encoding of the corresponding fine code. Therefore, it is essential to implement the TDL in the single clock region to mitigate nonlinearity.

It is difficult to implement the TDL within a single clock region for the Virtex-6 FPGA. The minimum clock period for Virtex-6 FPGA fabric was 1.67 ns. At least 167 taps were required to implement the TDL considering the T_{LSB} was 10 ps, but the maximum number of taps in the single clock region was limited to 160. There was an interpolation loss of 70 ps when implementing the TDL TDC within a single clock region.

2.2.3.2. The Principle of Dual-Phase TDL TDC

A new architecture using two TDLs of TDL_0 and TDL_{180} sampled at the rising edges of the in-phase clock CLK_0 and the 180° out-of-phase clock CLK_{180} was developed to implement TDC in the single clock region. The hit signal was split within the FPGA and fed into two TDLs. Each TDL covers a slightly longer period than half of T_0. In the case where the hit arrives at a TDC when CLK_0 is at a logic low, as shown in Figure 2-4 (a), the flip-flops of TDL_0 and TDL_{180} are in the states sampled at L_1 and L_2, respectively. Only the flip-flops of TDL_0 have the valid propagation states required to interpolate the fine time t_{f0}. The coarse count is obtained at the rising clock of CLK_0 immediately after the hit arrives, and the corresponding coarse count N yields the coarse time $N \times T_0$. The arrival time t_{arr} is therefore derived as in (2.2)

$$t_{\mathrm{arr}} = N \times T_0 - t_{\mathrm{f0}} \tag{2.2}$$

In the case where the hit arrives at a TDC when CLK_0 is at a logic high, as shown in Figure 2-4 (b), the flip-flops of TDL_0 and TDL_{180} are in the states sampled

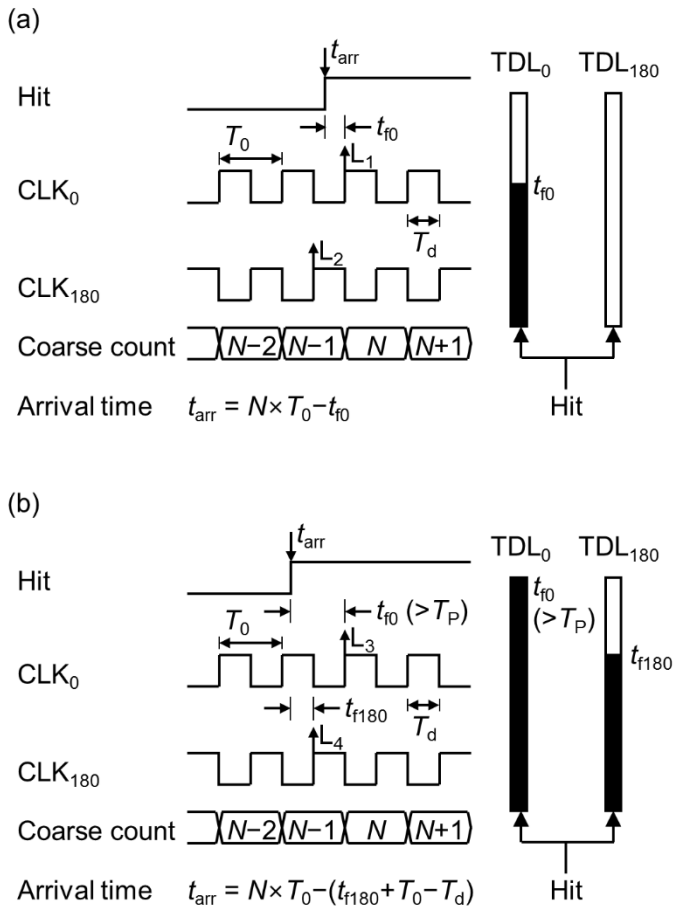

Figure 2-4. The principle of dual-phase TDL TDC. (a) In the case where the TDL_0 is selected to measure the fine time. (b) In the case where the TDL_{180} is selected to measure the fine time.

at L_3 and L_4, respectively. In this case, the sampled propagation states of TDL_0 are either valid or invalid because t_{f0} can be longer than the total delay time of a single TDL (T_P), as shown in Figure 2-4 (b). However, the sampled propagation states of TDL_{180} can be valid and provide a fine time t_{f180}. Therefore, t_{f180} is used when CLK_0 is at a logic high. The fine time is then derived as the sum of the period during which the CLK_0 is at a logic low ($T_0 - T_d$) with t_{f180} where T_d is the duration when the CLK_0 is at a logic high. As per the previous case, the coarse count is obtained from the rising clock of CLK_0 immediately after the hit arrives, and the corresponding coarse

count N yields the coarse time $N \times T_0$. The t_{arr} is therefore derived as in (2.3)

$$t_{\mathrm{arr}} = N \times T_0 - (t_{\mathrm{f180}} + T_0 - T_{\mathrm{d}}) \tag{2.3}$$

2.2.3.3. The Principle of Pipelined On-the-Fly Calibrator

The proposed on-the-fly calibration method is based on the code density test [40]. The code density test is a statistical method estimating every bin width. When the random hit signals are fed into the fine time interpolator, the portion of the number of collected hit signals into each fine code to the total number of hit signals is the same as the portion of the respective bin width to the clock period T_0. The i-th bin width w_i is estimated as in (2.4). The H_i and H_{total} are the measured number of hit signals collected into the i-th bin and a total number of hit signals, respectively. The i-th fine time f_i is calculated as in (2.5).

$$w_{\mathrm{i}} = \frac{H_{\mathrm{i}}}{H_{\mathrm{total}}} \times T_0 \tag{2.4}$$

$$f_{\mathrm{i}} = \frac{w_{\mathrm{i}}}{2} + \sum_{\mathrm{k}=0}^{\mathrm{i}-1} w_{\mathrm{k}} \tag{2.5}$$

The proposed calibration method is conducted in two parallel steps as shown in Figure 2-5. The first step is the bin width identification based on the code density test; it is implemented using a fixed-depth FIFO (first in first out) memory and a set of binary counters serving as a bin width estimator. Each bin corresponds to one counter, the collected value of which is proportional to its own bin width. When the hit arrives at the TDC, the TDC yields the fine code. The new fine code is then

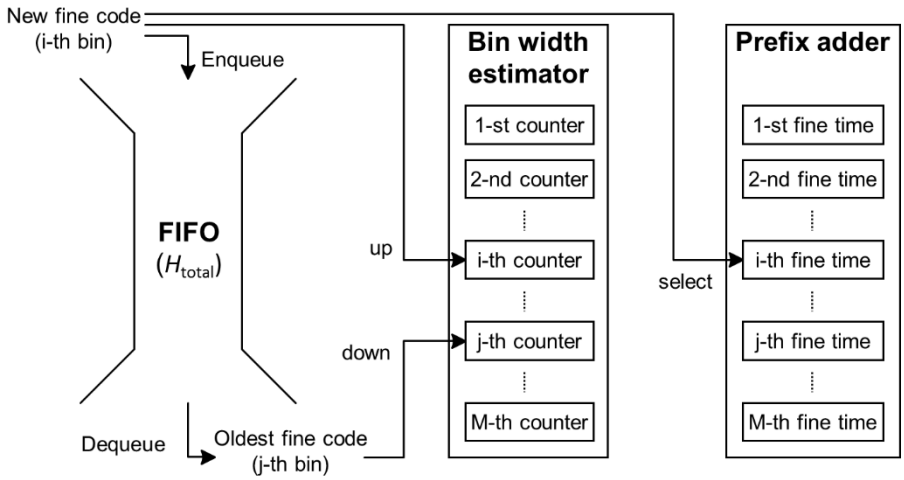

Figure 2-5. The principle of on-the-fly calibrator.

enqueued into a FIFO while increasing the value of the corresponding counter by one. Then, the oldest stored fine code is dequeued while decreasing the value of the corresponding counter by one. Using this process, the FIFO stores the most recent fine codes and the counters have up-to-date bin width information. Therefore, a H_{total}-depth FIFO and a H_i-count bin yield the w_i as in (2.4). For example, if the depth of the FIFO is 20,000 and the clock period is 2,500 ps, then the bin width of a 256-count bin is 256/20,000×2,500 ps = 32 ps. However, note that the bin width identification guarantees the calibration accuracy when a sufficient number of fine codes are booked in the FIFO.

The second step is the calibration information update, along with the continuous bin width identification. As shown in Figure 2-6, the pipelined and parallel prefix adder integrates bin widths, stored in a bin width estimator, to generate the calibration information. This process takes $2\times\log_2$(number of bins)−1 clock cycles. The fine time f_i is then calibrated to the center of the TDC bins as in (2.5).

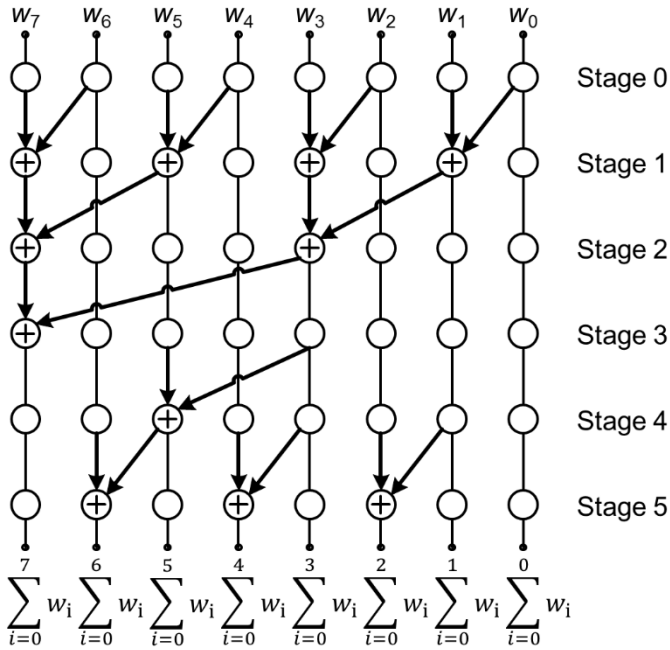

Figure 2-6. Prefix adder.

2.2.3.4. Implementation of Dual-Phase TDL TDC with On-the-Fly Calibrator

The dual-phase TDL TDC was implemented in the Virtex-6 evaluation kit. It consisted of the coarse counter and the fine time interpolator as shown in Figure 2-7. In the fine time interpolator, the TDL_0 was driven by a 400 MHz reference clock (CLK_0) and TDL_{180} is driven by a 180° out-of-phase clock (CLK_{180}). A built-in 200 MHz differential oscillator (SiT9102, SiTime) provided the input clock to the mixed-mode clock manager (MMCM) that generated the high-performance clocks of CLK_0 and CLK_{180}.

Each TDL consisted of 128 bins using 32 CLBs and two TDLs were located in parallel within the same clock region. When a hit was asserted into a TDC, the hit

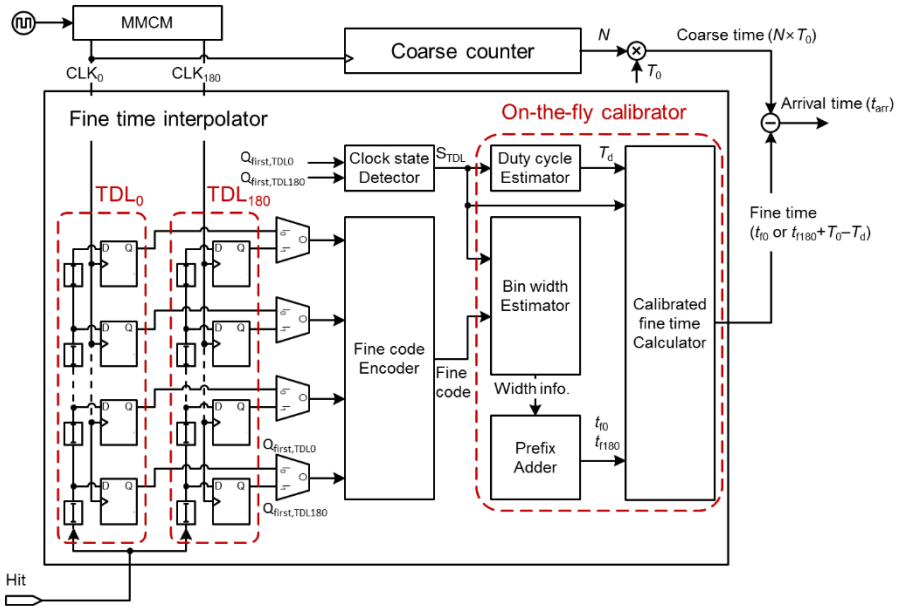

Figure 2-7. Implementation of dual-phase TDL TDC with on-the-fly calibrator.

was split and fed into the two TDLs almost simultaneously. The flip-flops of TDL_0 and TDL_{180} sampled the propagation states at the rising edges of CLK_0 and CLK_{180}, respectively, and thus two different 128-bit thermometer codes were obtained for a single event. The S_{TDL} was used to select the TDL to interpolate the fine time and to measure the duty cycle T_d.

In the case where only the first bin of TDL_0 was inverted as shown in Figure 2-4 (a), the S_{TDL} was at a logic low. In the case where both the first bins of TDL_0 and TDL_{180} were inverted as shown in Figure 2-4 (b), the S_{TDL} was at a logic high. A set of multiplexers selected one of the propagation states from TDL_0 or TDL_{180} depending on the S_{TDL}. The fine code encoder converted a selected 128-bit thermometer code into a 7-bit binary fine code.

The coarse counter driven by CLK_0 generated the coarse time with 2.5 ns resolution. Therefore, in this architecture, the two 128-bin delay lines driven by

CLK_0 and CLK_{180} provided the same effective dynamic range for the fine time as that of a 256-bin delay line without clock region crossing. The 10-ps delay bins and the effective 256-bin delay line allowed a dynamic range of 2,560 ps that covered the single clock period of 2.5 ns.

The on-the-fly calibrator consisted of a duty cycle estimator, a bin width estimator, a prefix adder, and a calibrated fine time calculator. It contained a fixed-depth FIFO, two sets of 128 binary counters used to store the bin width information of TDL_0 and TDL_{180}, and one binary counter used for the duty cycle estimator. When a hit arrived at the TDC, the fine code encoder yielded the 7-bit fine code and the clock state detector yielded the S_{TDL}. These new codes were concatenated as an 8-bit code and enqueued into the FIFO while the oldest code was dequeued. As stated above, these 8-bit codes corresponded to two sets of 128 binary counters and provided the up-to-date bin width information. In addition, S_{TDL} was used to estimate the T_d. If S_{TDL} was at a logic high, it was involved in increasing or reducing the value of the duty cycle estimator. Using this process, the duty cycle estimator then provided up-to-date duty cycle information. Using the bin width information, two prefix adders can then generate the fine time either t_{f0} or t_{f180}. The calibrated fine time calculator yielded the calibrated fine time of either t_{f0} when S_{TDL} was at a logic low or $t_{f180}+T_0-T_d$ when S_{TDL} was at a logic high. The t_{arr} was calculated as in (2.2) and (2.3)

2.2.4. Experimental Setups and Data Processing

Two dual-phase TDL TDCs with on-the-fly calibrators were implemented in the Virtex-6 FPGA evaluation kit for arrival time difference measurements. The random hits were generated using a ^{22}Na point source, a scintillation detector, and the

auxiliary electronics. The ^{22}Na point source emitted radiation with a uniform time distribution. The scintillation detector, which consisted of a photomultiplier tube (R9800, Hamamatsu Photonics K. K.) coupled with an LYSO scintillation crystal, converted a gamma-ray into an electrical signal. The auxiliary electronics, which contained a timing discriminator (N840, CAEN), a fan-in/fan-out unit (N401, CAEN), and translator units (N89, CAEN) in order, converted an electrical signal to two copies of FPGA-compatible digital hits. Before two hits were asserted to two TDC channels, respectively, a dual delay unit (N108A, CAEN) was added to provide the known arrival time differences between two hits. The Virtex-6 FPGA evaluation kit was located in a temperature-controlled box when conducting the code density test and temperature drift test.

2.2.4.1. TDC Characteristics

The TDC channel was characterized using the code density test with changing the ambient temperature from 10 to 50 °C in steps of 5 °C. The 102,400 samples were collected for the respective temperature.

The least significant bit (LSB) T_{LSB}, the differential non-linearity (DNL), and the integral non-linearity (INL) were characterized. The T_{LSB} was calculated by dividing T_0 by the sum of the last bin numbers of TDL_0 and TDL_{180}. The differential non-linearity (DNL) is a term describing the deviation of each bin width from its ideal value. The DNL of the i-th bin width w_i is calculated as in (2.6). The INL is a term describing the deviation of each fine time from the ideal TDC characteristics. The INL of the i-th bin is calculated as in (2.7)

$$\mathrm{DNL_i} = \frac{w_\mathrm{i} - T_\mathrm{LSB}}{T_\mathrm{LSB}} \tag{2.6}$$

$$\mathrm{INL_i} = \sum_{\mathrm{k=0}}^{\mathrm{i}} \mathrm{DNL_k} \tag{2.7}$$

The root-mean-square (RMS) quantization error σ_{cal} of the ideal TDC with an LSB of T_{LSB} is $T_{\mathrm{LSB}}/\sqrt{12}$ [40]. However, the σ_{cal} of FPGA-TDC is deteriorated because the bin width of the FPGA-TDC is non-uniform. The σ_{cal} considering bin-width variations is calculated as in (2.8) [33, 40]. The equivalent bin width w_{eq} is calculated as the bin width of the ideal TDC that has the RMS quantization error of σ_{cal}.

$$\sigma_{\mathrm{cal}} = \sqrt{\sum_{\mathrm{i=0}}^{M} \frac{w_\mathrm{i}^2}{12} \times \frac{w_\mathrm{i}}{T_0}} = \frac{w_{\mathrm{eq}}}{\sqrt{12}} \tag{2.8}$$

2.2.4.2. Arrival Time Difference Measurements

The arrival time differences from 0 to 20 ns in steps of 0.5 ns were measured by two TDC channels in three conditions ‘online calibration’, ‘offline calibration’, and ‘none’. The on-the-fly calibrator continuously updated the calibration information in the ‘online calibration’ measurements. The fine codes were used to generate the calibration information using the computer in the ‘offline calibration’. All bin widths were considered equal to T_{LSB} in the ‘none’ measurements. The 51,200 samples were collected for each measurement. The measurement uncertainty was evaluated using the maximum value of the standard deviation of the Gaussian fit.

In addition, the arrival time difference, fixed at zero, was measured in three different conditions. The first condition was with the active on-the-fly calibrator (‘real-time calibration’). In this condition, the on-the-fly calibrator continuously compensated for the nonlinearity. The second and third conditions were with the on-the-fly calibrator disabled (‘non-real-time calibration’). Under these conditions, the on-the-fly calibrator generated the calibration information at specific temperatures (10 and 50°C in the second and third sets of measurements, respectively) and did not update the calibration information, although the temperature changed. This calibrator operating mode conversion was performed by disabling the binary counters that serve as the duty estimator and the bin width estimator.

2.3. Results

2.3.1. TDC Characteristics

The FPGA temperature was higher than the ambient temperature by 8–9°C. The core voltage was stabilized but decreased with the temperature increase, with values of 1.013 V at 10 °C, 1.011 V at 20 °C, 1.009 V at 30 °C, 1.006 V at 40 °C, and 1.004 V at 50 °C.

The TDC characteristics were summarized as shown in Table 2-1. The T_{LSB}, the σ_{cal}, and the w_{eq} slightly increased with the ambient temperature. The positive DNL and the negative DNL appear alternately as shown in Figure 2-8. However, the high positive DNL and the continuous negative DNL were not observed by implementing TDC in a single clock region. The patterns of the DNL and the INL were almost identical regardless of the ambient temperature; however, the INL values were significantly affected by the temperature drift.

Table 2-1. TDC characteristics.

	T_{LSB} (ps)	T_d (ps)	σ_{cal} (ps)	w_{eq} (ps)	DNL (LSB)	INL (LSB)
10 °C	9.92	1,237	5.33	18.46	[–1.00, +2.11]	[–1.81, +4.23]
15 °C	9.92	1,226	5.33	18.48	[–1.00, +2.06]	[–1.55, +4.57]
20 °C	10.08	1,230	5.34	18.49	[–1.00, +1.93]	[–1.86, +3.29]
25 °C	10.08	1,232	5.41	18.73	[–1.00, +1.94]	[–1.63, +4.54]
30 °C	10.08	1,227	5.38	18.65	[–1.00, +2.01]	[–1.27, +4.86]
35 °C	10.25	1,228	5.42	18.76	[–1.00, +1.99]	[–1.69, +3.81]
40 °C	10.25	1,227	5.47	18.93	[–1.00, +2.02]	[–1.62, +4.51]
45 °C	10.25	1,230	5.51	19.08	[–1.00, +1.91]	[–1.70, +4.72]
50 °C	10.33	1,228	5.51	19.10	[–1.00, +1.87]	[–1.74, +4.28]

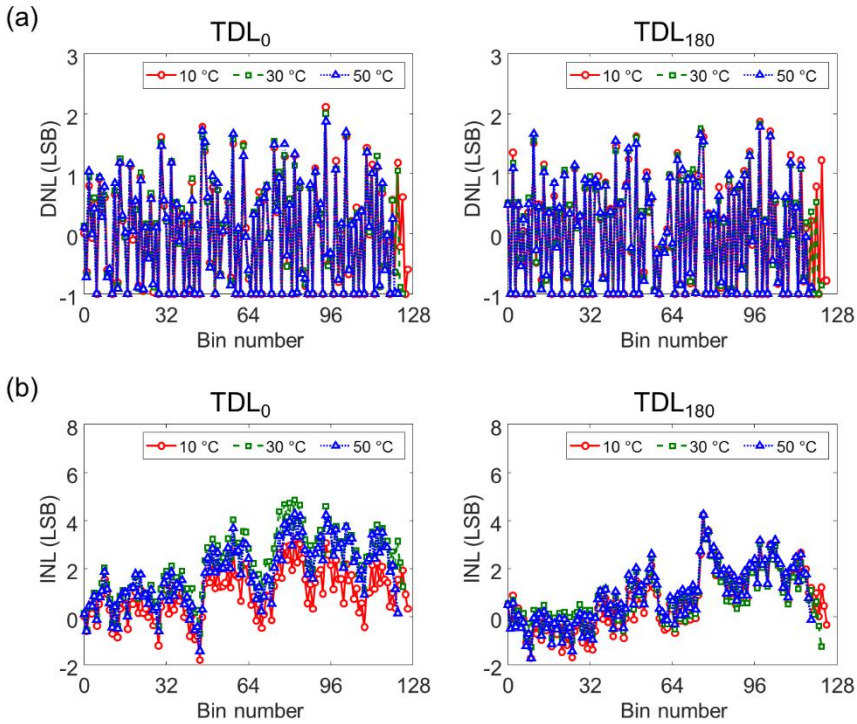

Figure 2-8. The nonlinearity of dual-phase TDL TDC. (a) DNL. (b) INL.

2.3.2. Arrival Time Difference Measurements

Figure 2-9 shows the time difference histograms for both hits arriving within a single clock period (Figure 2-9 (a)) and the second hit arriving a single clock period later (Figure 2-9 (b)). The propagation delay differences between the two TDC channels introduced by the external devices and cables were compensated. Figure 2-10 shows the measured uncertainty for time intervals. The measurement uncertainty values were 13.39, 12.87, and 23.65 ps with online and offline calibration methods and without calibration, respectively. The on-the-fly calibrator reduced the measurement uncertainty as well as had the comparable calibration performance with the offline calibration.

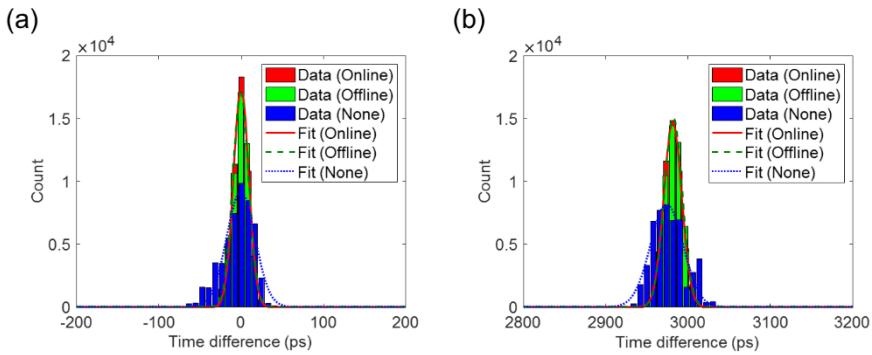

Figure 2-9. Time difference histograms obtained with online and offline calibration methods and without calibration. (a) Time difference of 0 ns. (b) Time difference of 3 ns.

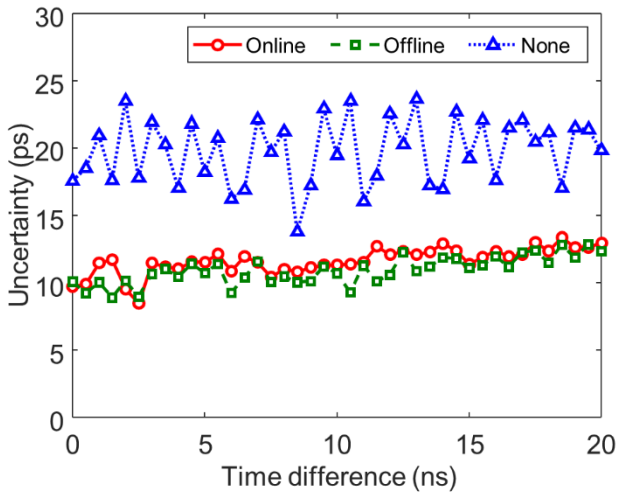

Figure 2-10. Measurement uncertainty for the time differences with online and offline calibration methods and without calibration.

As shown in Figures 2-11 and 2-12, the measurement uncertainty for the time differences conducted with 'real-time calibration' was less than 11.07 ps. In contrast, the measurement uncertainty of the other measurements that were conducted with 'non-real-time calibration' increased up to 44.62 ps.

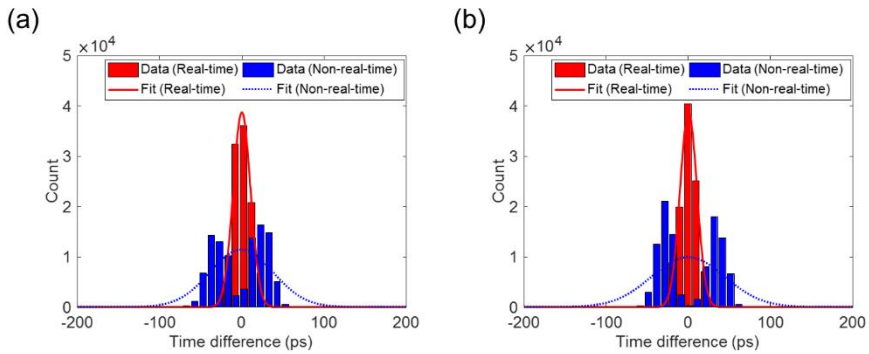

Figure 2-11. Time difference histograms with real-time calibration and non-real-time calibration. (a) In the second set of measurements with non-real-time calibration, the time differences were measured at 50 °C and the calibration information was obtained at 10 °C. (b) In the third set of measurements with non-real-time calibration, the time differences were measured at 10 °C and the calibration information was obtained at 50 °C.

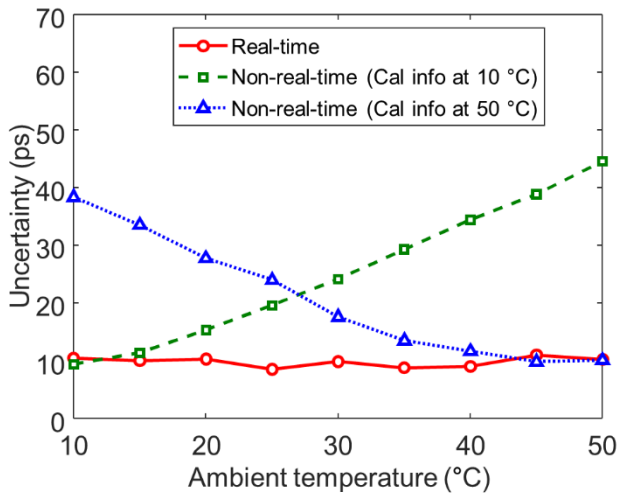

Figure 2-12. Measurement uncertainty of the time difference measurements with real-time calibration and non-real-time calibration. The ambient temperature changed from 10 °C to 50 °C in steps of 5 °C.

2.4. Discussion

The dual-phase TDL TDC enabled to implement the TDC in a single clock region with a moderate clock frequency of 400 MHz. Two 128-bin delay lines driven by CLK_0 and CLK_{180} provided the same effective dynamic range for the fine time as that of a 256-bin delay line without clock region crossing. The 10-ps delay bins and the effective 256-bin delay line covered the single clock period of 2.5 ns.

Although the positive DNL and the negative DNL appeared alternately because of the unbalanced propagation delay of the carry chain, the ultra-wide bin and the continuous missing bins were not observed as shown in Figure 2-8 (a). The DNL values ranged from −1 to +2 LSB and the DNL can be improved using the bin width tuning method [39].

The INL ranged from −1.70 to +4.72 LSB and was affected by the temperature drift significantly as shown in Figure 2-8 (b); however, the on-the-fly calibrator can compensate for the INL without introducing the dead time.

The on-the-fly calibrator can improve the measurement uncertainty and showed comparable performance with the offline calibrator as shown in Figures 2-9 and 2-10. The on-the-fly calibrator with the pipelined structure can compensate for the INL variations under the temperature drifts, and thus the maintained the TDC performance as shown in Figures 2-11 and 2-12. In addition, the on-the-fly calibrator has the self-calibration capability because the gamma rays from the object obey Poisson statistics.

The FPGA-TDC is a fundamental block to implement the FPGA-based DAQ systems. The developed FPGA-TDC with the on-the-fly calibrator would improve the resolution and the performance of the highly integrated FPGA DAQ systems.

Chapter 3. Time-based Multiplexing Method

3.1. Background

The SiPM signal multiplexing is a practical method to reduce the number of signals to handle a large number of output channels from the SiPM-based PET detectors. The most widely used multiplexing methods for the PET detectors are the charge division methods. In the charge division methods, the number of readout channels is reduced to four or five (usually, four channels for encoding the position information and one channel for timing measurement) using resistor [42, 43] or capacitor [44, 45] networks.

However, the charge division circuits have two main disadvantages. The first disadvantage is signal distortion. The shape of the signal is considerably depending on the SiPM position of the charge division network. In addition, the charge division methods demand energy measurement devices. Time pickoff devices are also required for timing measurement.

The waveform sampling method that uses a fast waveform digitizer provides both energy and timing information [46]. In addition, the time-based multiplexing method that uses a waveform digitizer can simplify the multiplexing circuits because the passive components required for charge division can be removed [47]. However, the waveform sampler should contain the ADC and a subsequent FPGA, thus the DAQ system cannot be fully simplified. Thus, a fully time-based multiplexing and readout method is required to simplify both multiplexing and DAQ systems

3.2. Materials and Methods

3.2.1. Delay Grid Multiplexing

Fully time-based multiplexing and readout method consist of a delay grid that connects every SiPM output into the four timing pickoff channels [48]. The position of each SiPM within a multiplexing circuit (delay grid) is decoded using the principle of TDOA positioning. In the GPS that uses the TDOA positioning, the signal from the transmitter propagates through the medium and is received by multiple synchronized receivers. The position of the transmitter is localized using the known locations of the receivers and the TDOA information.

Similar to GPS, the position information on the fired SiPM can be decoded using the innate transit time differences from the SiPM channel to the readout channels. The transmitters, the medium, and the receivers in GPS correspond to the SiPM channels, the delay grid, and the time pickoff devices in the proposed multiplexing method. The delay grid consists of the traces in the row and column directions on a printed circuit board (PCB) where the SiPM channels of each row are connected and two column traces tie the ends of the row traces, as shown in Figure 3-1. Unit delay (u) is the transit time between the adjacent cathodes. The four corner nodes of the delay grid, referred to as the A, B, C, and D nodes in a counterclockwise direction, are connected into the amplifiers and the output of each amplifier is fed into the time pickoff device. When the SiPMs fire, the current signals from the SiPM flow into the delay grid and the identical signals are fed into the four corner nodes with the difference in transit times. As indicated in Table 3-1, the transit times from the SiPM channel to the readout channels are encoded uniquely.

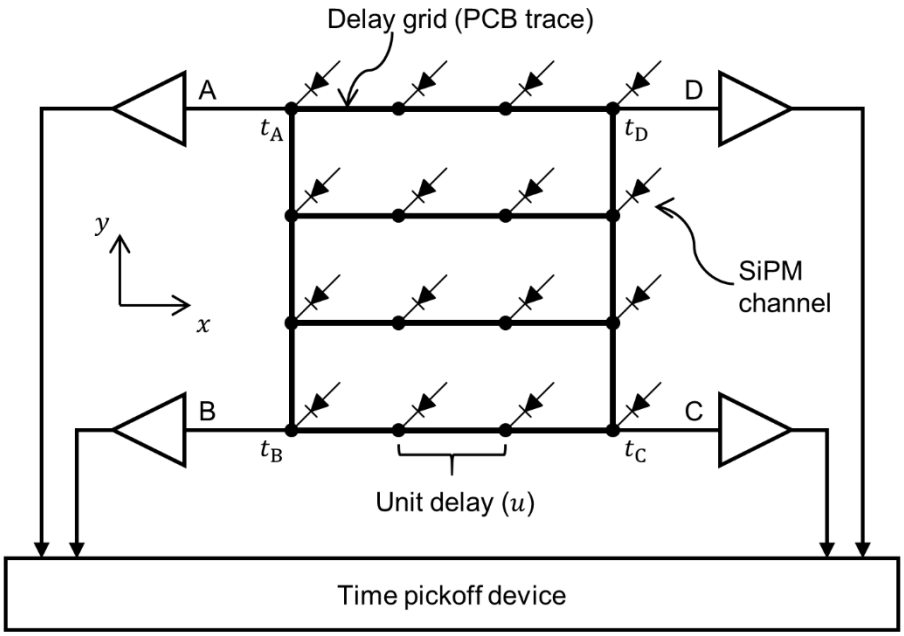

Figure 3-1. Conceptual diagram for the delay grid multiplexing. Position for each SiPM channel is uniquely encoded using the innate transit times from a SiPM channel to the four corner nodes.

Table 3-1. Look-up table for decoding the position and the time information.

Firing position		Corner node arrival time				Decoded position		Timing
x	y	t_A	t_B	t_C	t_D	$\hat{x}$	$\hat{y}$	t_γ
0	0	$3u + t_{det}$	$0u + t_{det}$	$3u + t_{det}$	$6u + t_{det}$	$-1.5u$	$-1.5u$	
0	1	$2u + t_{det}$	$1u + t_{det}$	$4u + t_{det}$	$5u + t_{det}$	$-1.5u$	$-0.5u$	
0	2	$1u + t_{det}$	$2u + t_{det}$	$5u + t_{det}$	$4u + t_{det}$	$-1.5u$	$0.5u$	
0	3	$0u + t_{det}$	$3u + t_{det}$	$6u + t_{det}$	$3u + t_{det}$	$-1.5u$	$1.5u$	$3u$
1	0	$4u + t_{det}$	$1u + t_{det}$	$2u + t_{det}$	$5u + t_{det}$	$-0.5u$	$-1.5u$	$+ t_{det}$
1	1	$3u + t_{det}$	$2u + t_{det}$	$3u + t_{det}$	$4u + t_{det}$	$-0.5u$	$-0.5u$	
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	
3	3	$3u + t_{det}$	$6u + t_{det}$	$3u + t_{det}$	$0u + t_{det}$	$1.5u$	$1.5u$	

Using the TDOA measurements obtained at the A, B, C, and D nodes, the positions can be decoded as in (3.1) and (3.2). The values t_A, t_B, t_C and t_D are the corner node arrival times at the A, B, C, and D nodes, which are the sums of the transit times from the SiPM channel to the A, B, C, and D nodes and the gamma arrival time t_γ, respectively. The t_γ is the time when the gamma-ray interacts with the SiPM-based scintillation detector and calculated as in (3.3).

$$\hat{x} = \frac{+t_A + t_B - t_C - t_D}{4} \tag{3.1}$$

$$\hat{y} = \frac{-t_A + t_B + t_C - t_D}{4} \tag{3.2}$$

$$t_\gamma = \frac{+t_A + t_B + t_C + t_D}{4} \tag{3.3}$$

3.2.2. Detector for Concept Verification

Figure 3-2 shows a SiPM-based detector assembled to show the feasibility of the proposed multiplexing method. The SiPM detector consisted of an array of 4×4 LGSO crystals (Hitachi Chemical Ltd) and one-to-one coupled SiPM (S11064-050P; Hamamatsu Photonics. K.K.) as shown in Figures 3-2 (a) and (b). Each SiPM channel had an active area of 3×3 mm^2 and both pitches of the cathode pins along the x and y directions were 4 mm as shown in Figure 3-2 (c). Each crystal had a dimension of 3×3×20 mm^3. All crystal surfaces were chemically polished and wrapped with enhanced specular reflectors (ESR, 3M) with the exception of the exit face. Optical adhesive (Optically Clear Adhesive 8146-4, 3M) with a refractive index of 1.474 and a uniform thickness of 100 μm was used to improve the optical coupling between the crystal and the SiPM.

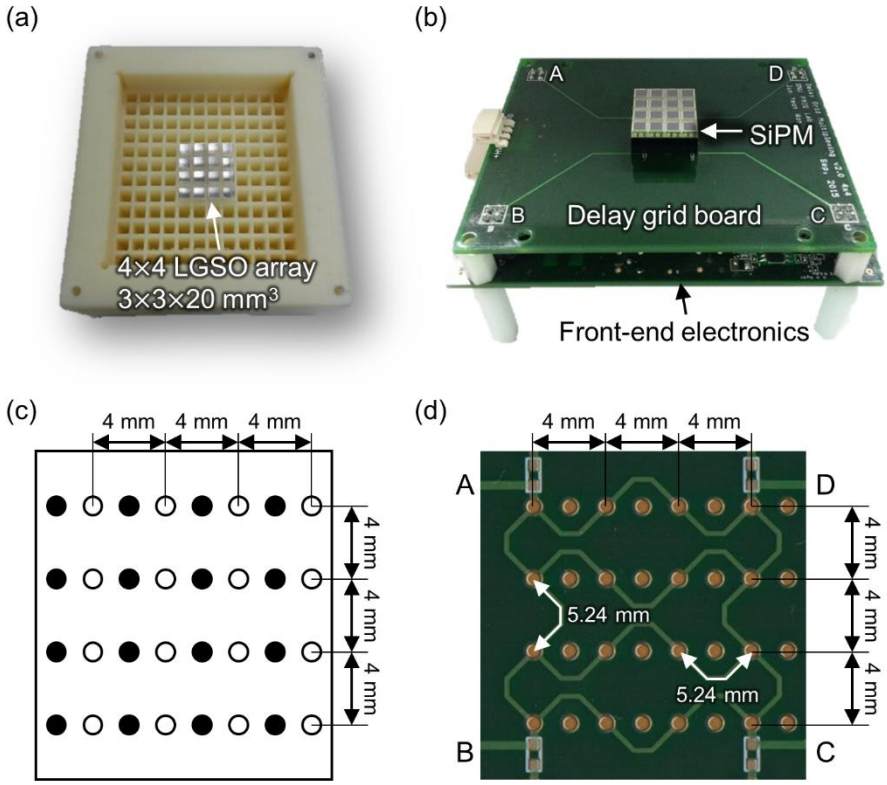

Figure 3-2. LGSO/SiPM detector using the proposed multiplexing method. (a) LGSO crystal array assembled into the frame. (b) Mounted SiPM on a delay grid board and the front-end electronics. (c) Backside of the employed SiPM. The blank and the filled circles indicate the pinout of the cathodes and the anodes, respectively. (d) Detailed view of a delay grid board.

All the crystals were assembled into an in-house frame produced in our previous work [49] using a 3D printer (Mojo, Stratasys), as shown in Figure 3-2 (a). The crystal pitches along the *x* and *y* directions were 4.05 and 4.50 mm, respectively, which were equal to the SiPM pitches. As shown in figure 3-2 (b), the LGSO/SiPM detector was mounted on a delay grid board.

The delay grid is a planar array of the microstrips on an FR-4 substrate with the relative permittivity of 4.3 as shown in Figure 3-2 (d). The trace lengths between the cathode pins along the *x* and *y* directions were 5.24 mm. The width of the trace and the height with respect to the reference plane were 0.3 and 1.3 mm, respectively.

3.2.3. Front-end Electronics

Front-end electronics provided either analog or digital signals containing the corner node arrival times with the time pickoff device. The signal chain was as follows. The four corner nodes of the delay grid board were connected to an in-house front-end electronics that contained the amplifiers and the comparators, as shown in Figure 3-2 (b).

Figure 3-3 shows the detailed schematic of the front-end electronics for the LGSO/SiPM detector. The current signals that arrived at the A, B, C, and D nodes were converted into the voltage signals with an input impedance of 10 Ω and then amplified by −24 using inverting amplifiers. These signals were denoted as the A, B,

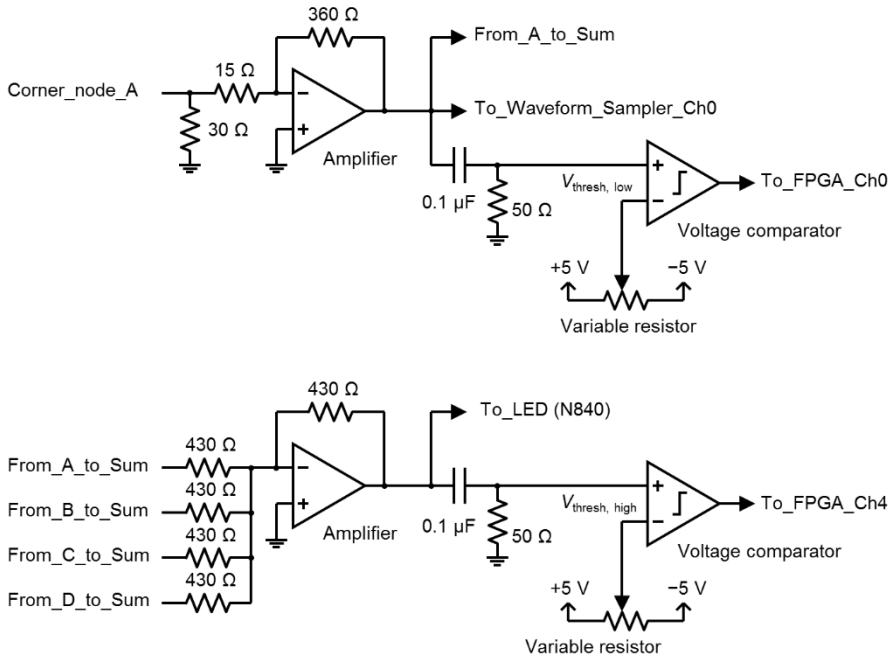

Figure 3-3. Schematic of the front-end electronics for the LGSO/SiPM detector. In the measurements using the waveform sampler, the bypass capacitors between the amplifiers and the comparators were detached. In the measurements using the FPGA-TDC, the cables connecting the front-end electronics to the waveform sampler and the leading edge discriminator (LED) module were detached.

C, and D signals, respectively. The summing amplifier added the A, B, C, and D signals and then provided the Sum signal. The traces from the A, B, C, and D amplifiers to the summing amplifier were designed to be the same lengths. Either analog A, B, C, and D signals or digital A, B, C, D, and Sum signals after discriminating the analog signals with the comparators were transmitted to the time pickoff device. The voltage threshold of the comparator was adjusted using a variable resistor and fixed during the measurement.

3.2.4. Experimental Setups

The LGSO/SiPM detector was evaluated in the coincidence detection mode with a reference detector, as shown in Figure 3-4. We used the PMT-based scintillation detector with a single timing resolution (STR) of 197 ps full width at half maximum (FWHM) as the reference detector [50]. A ^{22}Na point source (approximately 9 μCi) was attached to the reference detector. The distance between the LGSO/SiPM and reference detectors was 20 cm. The ambient temperature was fixed at 20 °C using a temperature-controlled box.

We obtained 400,000 coincidence events for every measurement, with the exception of ToT nonlinearity calibration. In order to calibrate the nonlinearity of ToT, we acquired 1,024,000 coincidence events for a ^{22}Na and 1,024,000 singles events for ^{131}I and ^{137}Cs.

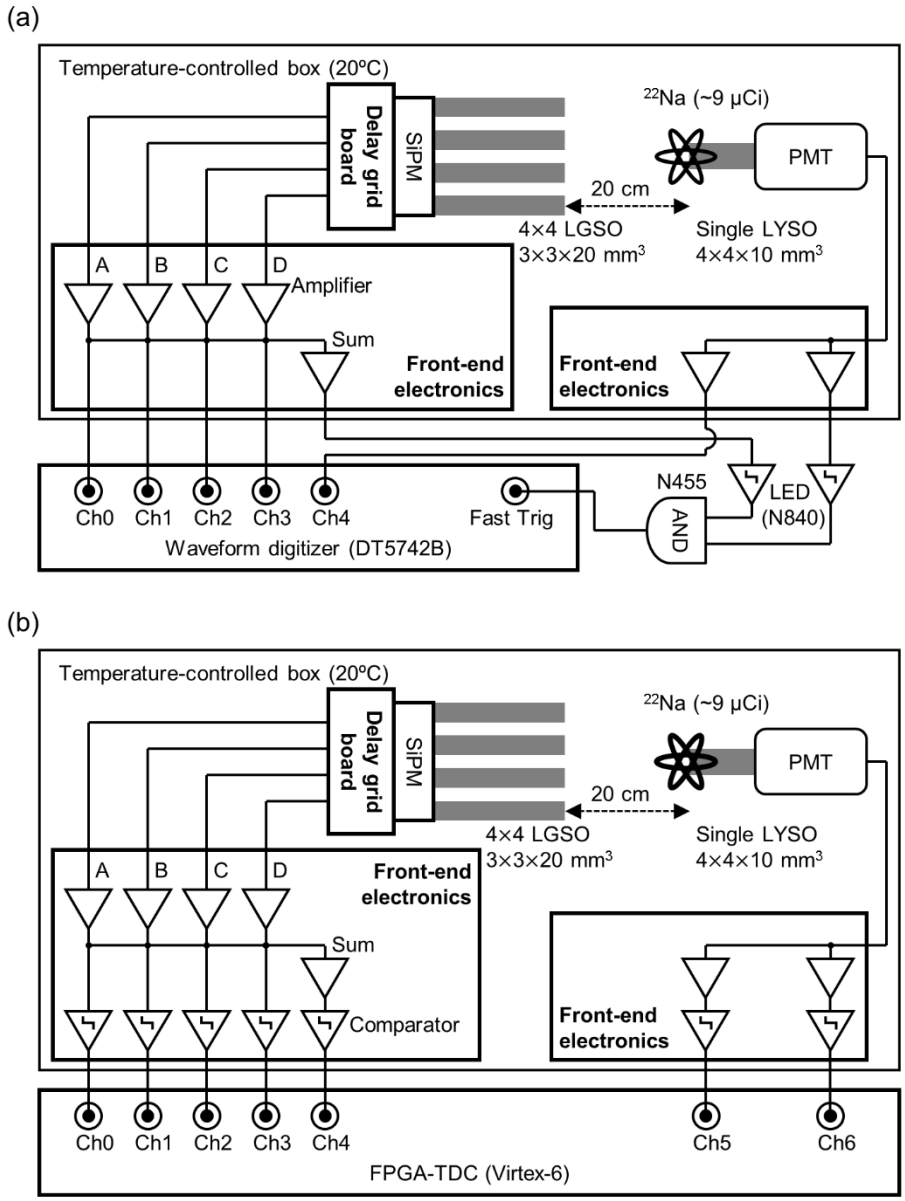

Figure 3-4. Experimental setups using (a) the waveform digitizer and (b) the FPGA-TDC.

3.2.4.1. Data Acquisition Using the Waveform Digitizer

For the purpose of initial verification, we used a fast waveform digitizer (DT5742B, CAEN) based on switched capacitor arrays (SCAs). The SCA is the fourth version of the domino ring sampler (DRS4, PSI) and provides a resolution of 12 bits and a sampling rate of up to 5 Giga-samples/sec [46].

The leading edge discriminator (LED) modules (N840; CAEN) and a coincidence unit (N455; CAEN) were used to obtain only coincidence events, as shown in Figure 3-4 (a). The A, B, C, and D signals were acquired using a waveform digitizer at the respective readout channels. The output of the summing amplifier was used to generate a trigger, and instead, the Sum signal was obtained by adding the sampled A, B, C, and D waveforms. The time differences from the four corner nodes to the respective readout channels due to cable length differences were corrected before adding the sampled A, B, C, and D waveforms. The signal from the reference detector was also sampled.

The common bias voltage was applied to all SiPM channels where the breakdown voltages were –69.7 V. The overvoltage was swept from 2.1 to 3.6 V (bias voltages from –71.8 to –73.3 V) in steps of 0.3 V to find the optimal bias voltage where the SiPM provided the lowest coincidence timing resolution (CTR).

3.2.4.2. Data Acquisition Using the FPGA-TDC

After verifying the concept of delay grid multiplexing using the waveform digitizer, we replaced the waveform digitizer with an FPGA-TDC to verify that the readout circuits can be further simplified. A multi-channel TDC with a 10-ps resolution and the sub-10-ps single-shot precision implemented in a Virtex-6 FPGA was used [38, 39].

In the front-end electronics for the LGSO/SiPM detector, the A, B, C, D, and Sum signals of the LGSO/SiPM detector were discriminated using the voltage comparators, and then the digital signals that contained the arrival times and ToT were transmitted to the FPGA-TDC. In the front-end electronics for the reference detector, the signal from the reference detector was discriminated by two comparators with different threshold levels. In the FPGA, either singles or coincidence events within the predetermined time window were obtained [51]. The overvoltage of 2.7 V at which the SiPM provided the lowest CTR in the measurements using the waveform digitizer was applied to the LGSO/SiPM detector when the FPGA-TDC was employed as a data acquisition system.

3.2.5. Data Processing and Analysis

3.2.5.1. Waveform Digitizer

Rise Time and Decay Time

To show that the signal was not distorted by the multiplexing circuit, the rise and decay times of the A, B, C, D, and Sum signals were obtained. The rise time was evaluated using the time taken by a signal to change from 10% to 90% of its peak amplitude v_{peak}. The decay time τ was obtained by fitting the trailing edge of the waveform to an exponential decay function $v_{\mathrm{peak}} \times \exp(-t/\tau)$.

Time Pickoff

To obtain the position and the gamma arrival time t_{γ}, we sampled the signals at 5 Giga-samples/sec and interpolated the leading edge of the waveform using a cubic spline interpolation by a factor of 20 to obtain the resolution of 10 ps, and thus minimize the quantization error. We picked off the corner node arrival times by

applying either constant voltage discriminator (also known as LED) or constant fraction discriminator (CFD) to the leading edge of the interpolated waveforms where the baseline for time pickoff was determined at the onset of the signal with time window of 2 ns in order to minimize the effect of dark noise on time pickoff [52]. The threshold for time pickoff was determined as the percentage of peak amplitude of events within an energy window and denoted as the percentage (%) threshold hereinafter. For LED, the constant voltage threshold calculated by averaging the percentage thresholds of all the events within the energy window was applied to every signal. For CFD, the threshold was determined as a constant percentage of peak amplitude for each signal.

Position

The position information was obtained from the corner node arrival times t_A, t_B, t_C, and t_D using equations (3.1) and (3.2). Both LED and CFD were employed and the percentage threshold used for obtaining the position information was swept from 2% to 40% in order to analyze the effect of threshold on the position.

The flood map was used to display the position information, while the events within a 400–600 keV energy window were employed. Flood-map quality was evaluated using a distance-to-width ratio (DWR) in the flood map. The DWR is defined as the distance between the two adjacent spots in the flood map to the average FWHM of the two spots, and it is calculated as in (3.4).

$$\mathrm{DWR} = \frac{2}{N_{\mathrm{adj}}}\left(\sum_{\mathrm{i,j}\ \in\ \mathrm{adj\ pair}}^{N_{\mathrm{adj}}} \frac{x_{\mathrm{i}} - x_{\mathrm{j}}}{w_{\mathrm{x,i}} + w_{\mathrm{x,j}}} + \frac{y_{\mathrm{i}} - y_{\mathrm{j}}}{w_{y,\mathrm{i}} + w_{\mathrm{y,j}}}\right) \tag{3.4}$$

In equation (3.4), x_i, y_i and x_j, y_j are the x and y positions of the i-th and j-th crystals in the flood map, respectively. The $w_{x,i}$, $w_{y,i}$ and $w_{x,j}$, $w_{y,j}$ are the FWHM of 1D profiles along the x and y directions of the i-th and j-th crystals, respectively. N_{adj} is the number of adjacent crystal pairs. A larger DWR indicates that the crystals are more clearly resolved.

To perform a per-crystal analysis, the crystals in the flood map were identified using the k-means clustering, while the initial values of the iterations were determined as the peak positions of the flood map. All the results were represented as the mean ± standard deviation of the measurements of resolved crystals.

Energy

Energy information was calculated using the integration of sampled waveforms (sum of areas of the baseline-corrected A, B, C, and D waveforms). The baseline for energy integration was calculated using the mean value of the first 50 data points (10 ns) before the onset of the signal on an event-by-event basis. The energy integration window was 700 data points (140 ns).

The photopeak positions and the energy resolution were evaluated. The energy resolution was obtained by fitting the energy with a Gaussian function on a per-crystal basis.

CTR

The t_γ can be acquired using either digital LED or CFD. The percentage threshold used to pickoff t_γ was swept from 1% to 5% in steps of 0.5% and the 2% threshold yielded the lowest CTR values for both LED and CFD, and thus the 2% threshold was employed.

The events within the 400–600 keV energy windows of the LGSO/SiPM and reference detectors were employed to evaluate the CTR. The CTR between two identical LGSO/SiPM detectors $\mathrm{CTR}_{\mathrm{Test/Test}}$ was calculated and notated hereinafter. From the FWHM of Gaussian fits applied to the time-difference histograms between the LGSO/SiPM and reference detectors $\mathrm{CTR}_{\mathrm{Test/Ref}}$, the STR of the reference detector of 197 ps FWHM was subtracted in the quadrature, and then that of the LGSO/SiPM detector was multiplied by $\sqrt{2}$, as in (3.5).

$$\mathrm{CTR}_{\mathrm{Test/Test}} = \sqrt{2} \times \sqrt{\mathrm{CTR}_{\mathrm{Test/Ref}}^2 - \mathrm{STR}_{\mathrm{Ref}}^2} \tag{3.5}$$

3.2.5.2. FPGA-TDC

Dual-threshold ToT

Dual-threshold ToT was employed for both the LGSO/SiPM and reference detectors to extract the precise timing and energy information. As shown in Figure 3-5, the arrival time t_{arr} was obtained using the time when the signal crossed the low threshold $V_{\mathrm{thresh,low}}$ in its leading edge, while the ToT was calculated by subtracting this arrival time from the time when the signal crossed the high threshold $V_{\mathrm{thresh,high}}$ in its trailing edge. For the LGSO/SiPM detector, the $V_{\mathrm{thresh,low}}$ of 2% threshold and the $V_{\mathrm{thresh,high}}$ of 40% threshold were applied to the four corner readout channels and Sum readout channel, respectively; the ToT was calculated within an FPGA by subtracting t_{γ} from the time when the Sum signal crossed the $V_{\mathrm{thresh,high}}$ in its trailing edge. For the reference detector, the $V_{\mathrm{thresh,low}}$ of 5% threshold and the $V_{\mathrm{thresh,high}}$ of 30% threshold were applied to the respective channels. For both detectors, false

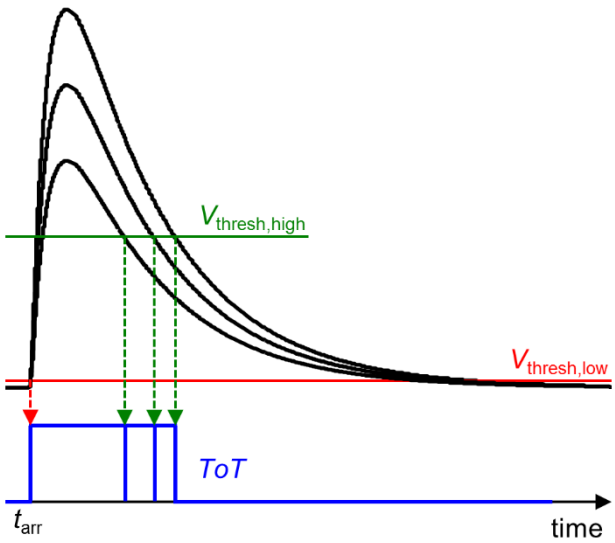

Figure 3-5. Dual-threshold ToT.

events with peak amplitudes lower than the $V_{thresh,high}$ were rejected.

The ToT measurement was calibrated into the energy value using the calibration curve that compensated both nonlinearities of SiPM and ToT [15].

$$ToT(E) = c + a \times \ln[1 - \exp(-b \times E)] \tag{3.6}$$

In equation (3.6), E indicates the energy of the incident gamma ray and a, b, and c are the constants to be determined for each crystal. Nonlinearity calibration was conducted in three steps. First, we obtained the photopeak positions of the ToT spectra for three radioisotopes with known energies: ^{131}I (364 keV), ^{22}Na (511 keV), and ^{137}Cs (662 keV). Second, we solved equation (3.6) to acquire the calibration curve on a per-crystal basis. Third, we applied per-crystal calibration curves to the ToT measurements.

Performance Evaluation

The x and y positions and the t_γ were calculated from the corner node arrival times obtained by an FPGA-TDC using the equations (3.1), (3.2), and (3.3), respectively. Energy, DWR, and CTR were assessed using the same data analysis procedures conducted with the waveform digitizer.

3.3. Results

3.3.1. Waveform Digitizer

3.3.1.1. Waveform, Rise Time, and Decay Time

Figure 3-6 shows the A, B, C, and D signals that originated from the corner, edge, and center locations of the multiplexing circuit. For each event, the A, B, C, and D signals were almost identical, but with the TDOAs. The TDOAs described in Table 3-1 were measured as expected. The signal arrived at the four corner nodes in

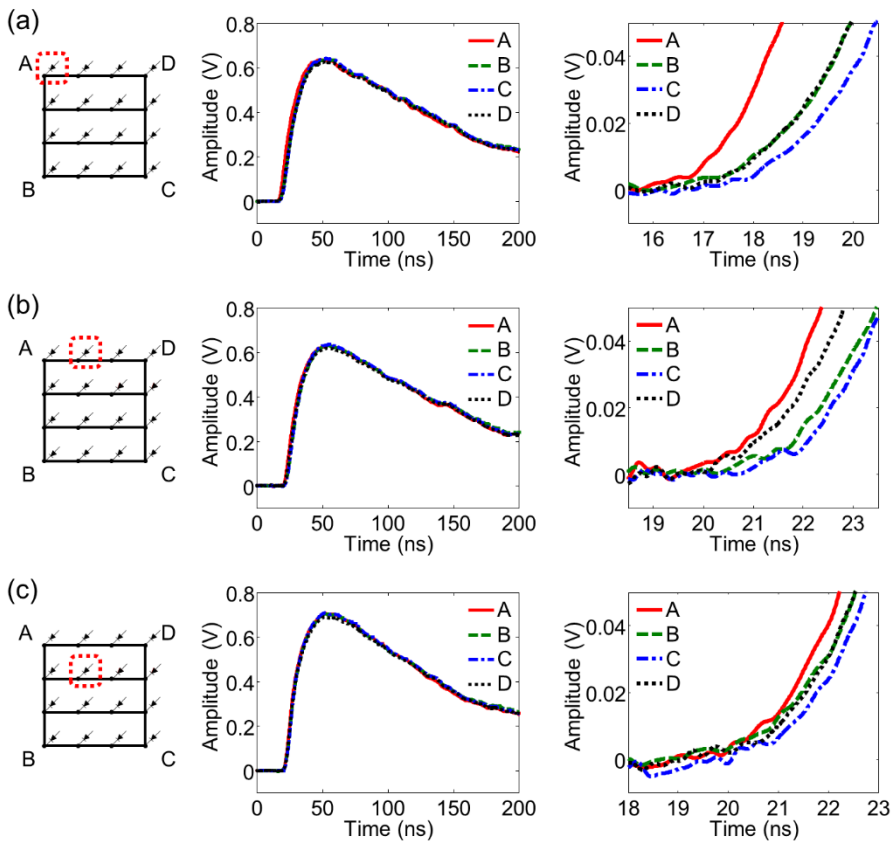

Figure 3-6. Waveforms obtained at the four corner readout channels. (a) Full and detailed views of waveforms for event that originated from corner location (at firing position (0, 3)). (b) Full and detailed views of waveforms for event that originated from edge location (at firing position (1, 3)). (c) Full and detailed views of waveforms for event that originated from center location (at firing position (1, 2)).

order of closeness from the firing SiPM channel to the corner nodes. As shown in Figure 3-6 (b), the signal that originated from the SiPM channel location (1, 3) arrived at the A, D, B, and C nodes in order.

We could observe that the signal shape and the amplitude did not change considerably as the signal propagated along the delay grid. Although there were slight differences at the onsets of the A, B, C, and D signals, the overall signal shapes, including the rise and decay times, were consistent throughout the multiplexed SiPM

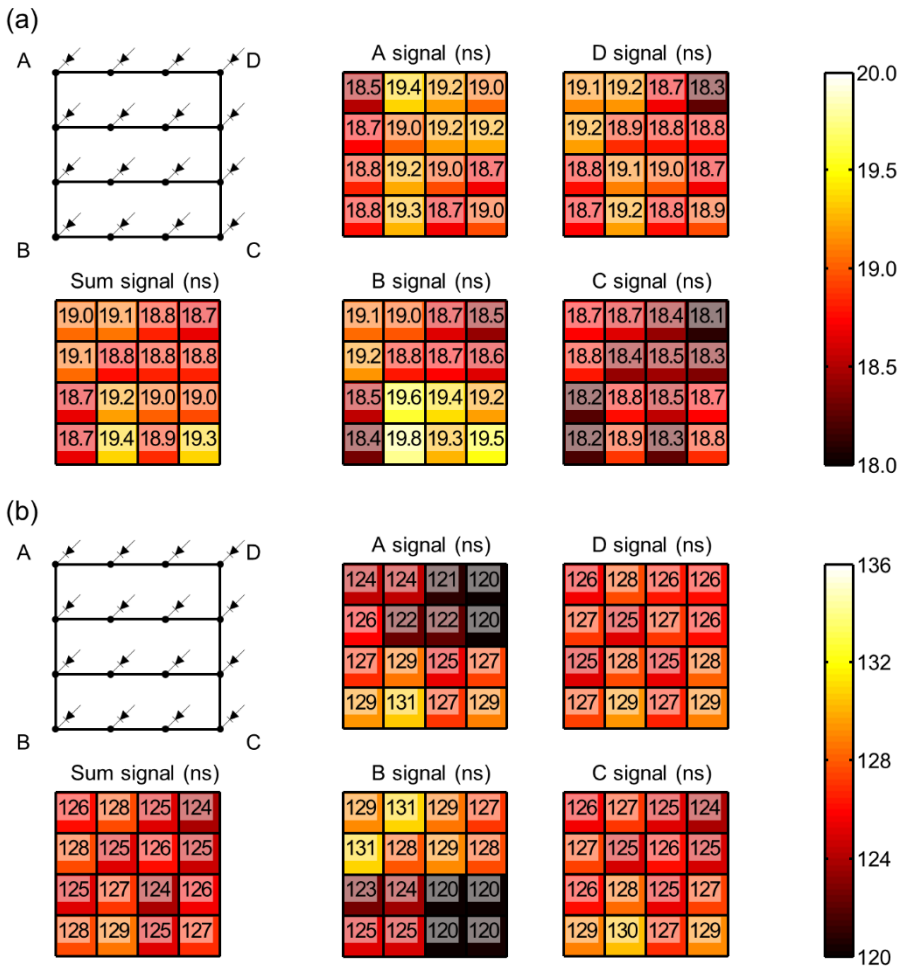

Figure 3-7. Rise and decay times. (a) 10%-90% rise times of the A, B, C, D, and Sum signals for events detected at 16 SiPM channels. (b) Decay times of the A, B, C, D, and Sum signals for events detected at 16 SiPM channels.

channels. Figure 3-7 show the average rise and decay times of the A, B, C, D, and Sum signals corresponding to photopeak events detected at 16 SiPM channels, respectively. The rise times of the A, B, C, D, and Sum signals were 19.0 ± 0.3, 19.0 ± 0.4, 18.5 ± 0.3, 18.9 ± 0.2, and 19.0 ± 0.2 ns, respectively. The decay times of the A, B, C, D, and Sum signals were 125 ± 4, 125 ± 4, 127 ± 2, 127 ± 1, and 126 ± 1 ns, respectively. The rise and decay times of the A, B, C, and D signals were almost the same and also uniform throughout 16 SiPM channels. In addition, the rise and decay times of the Sum signal were more consistent than those of the A, B, C, and D signals.

3.3.1.2. Flood Map

Figure 3-8 shows the flood maps acquired using LED and CFD methods for the overvoltages of 2.1 V to 3.6 V and the percentage thresholds of 2% to 40%. The 16 crystals were clearly resolved for all measurements. In addition, as the percentage threshold increased, the size of the flood map also increased and a pincushion distortion appeared.

Figure 3-9 shows the DWRs for the flood maps shown in Figure 3-8. LED and CFD provided similar DWRs, and such DWRs were the largest at the 25% threshold. In addition, the DWRs increased with the overvoltage of up to 3.3 V.

Figure 3-10 shows the representative flood map and 1D profiles obtained using CFD with the 25% threshold at the overvoltage of 2.7 V. DWR was 9.8. The distances between the adjacent spots along the x and y directions were 367 ± 54 and 386 ± 127 ps, respectively. The FWHMs of the spots along the x and y directions were 39 ± 5 and 41 ± 4 ps, respectively.

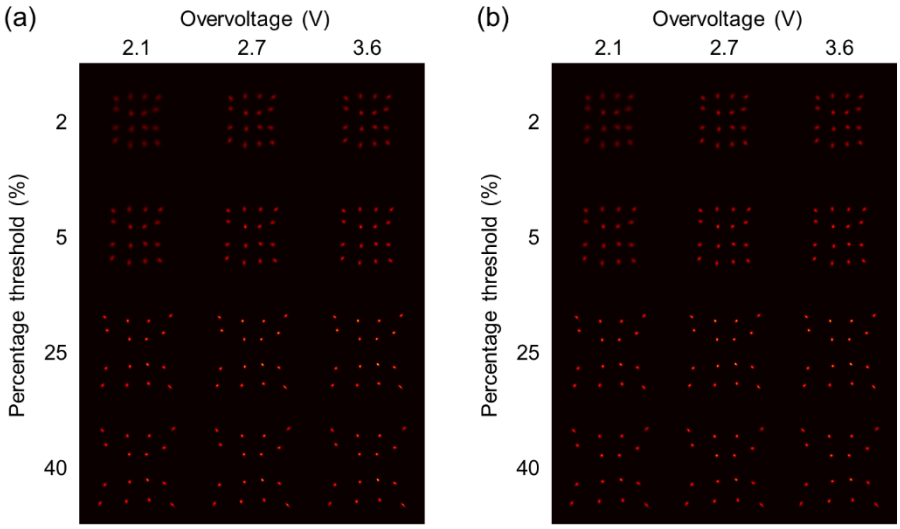

Figure 3-8. Flood maps obtained using the waveform digitizer. (a) LED. (b) CFD.

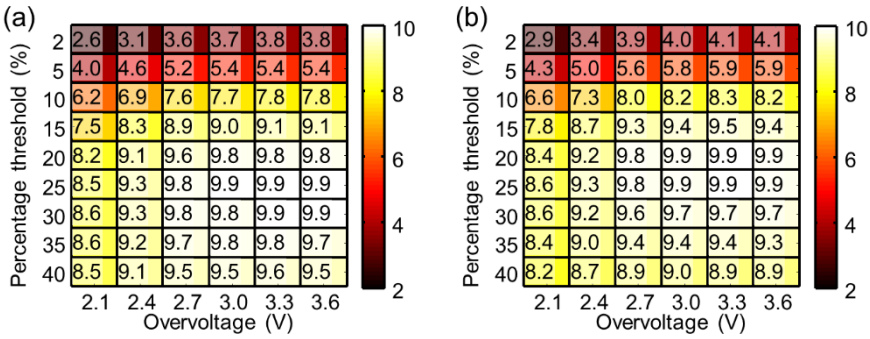

Figure 3-9. DWR values obtained using the waveform digitizer. (a) LED. (b) CFD.

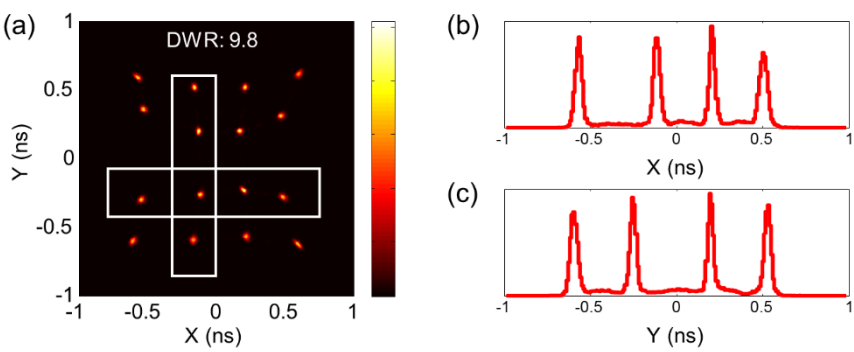

Figure 3-10. Representative flood map and 1D profiles obtained using the waveform digitizer. (a) Flood map obtained using CFD with the 25% threshold at the overvoltage of 2.7 V. (b) 1D profile along the *x* direction. (c) 1D profile along the *y* direction.

3.3.1.3. Energy

Figure 3-11 shows the energy measurements of the LGSO/SiPM detector using the waveform digitizer. Because the time pickoff method, either LED or CFD, and the threshold did not affect the energy measurements, those obtained using CFD with the 25% threshold were described. The photopeak positions were not affected by both the time pickoff method and the overvoltage.

As shown in Figures 3-11 (a) and (b), the photopeak region of the total energy histogram was widened due to gain variation. The per-crystal energy resolutions after crystal identification were evaluated as a function of the overvoltage, as shown in Figure 3-12 (c). The error bars in Figure 3-12 (c) indicate the standard deviation of the energy resolutions of the multiplexed SiPM channels. The per-crystal energy

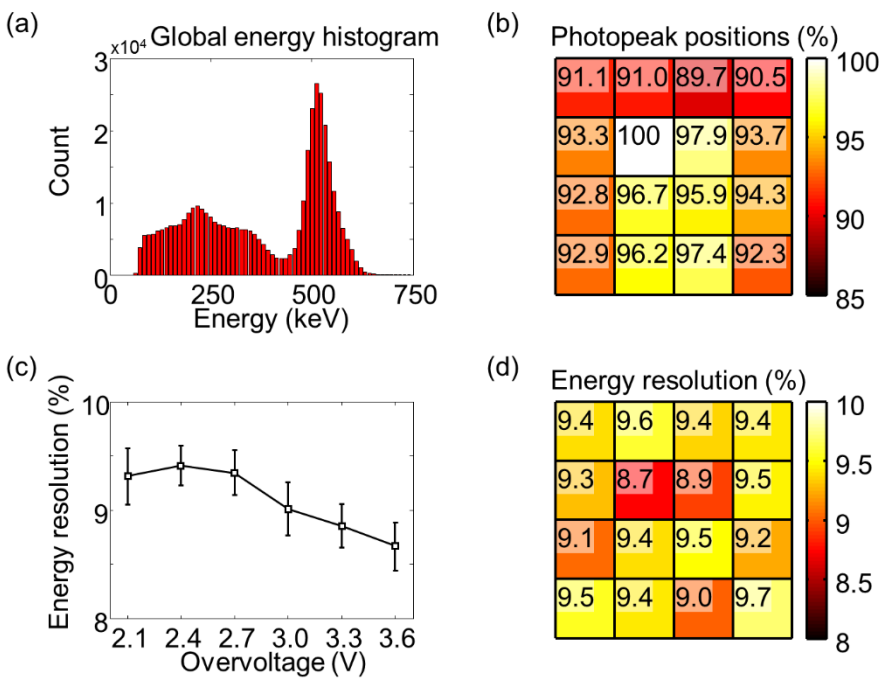

Figure 3-11. Energy measurements for the LGSO/SiPM detector using the waveform digitizer. (a) Global energy histogram. (b) Photopeak positions. (c) Per-crystal energy resolutions against the overvoltage. (d) Representative per-crystal energy resolutions obtained at an overvoltage of 2.7 V.

resolution values were 9.3 ± 0.3, 9.4 ± 0.2, 9.3 ± 0.2, 9.0 ± 0.2, 8.9 ± 0.2, and 8.7 ± 0.2% FWHM at 511 keV at the respective overvoltages from 2.1 V to 3.6 V. The energy resolution value of a reference detector was 10.1% FWHM at 511 keV.

3.3.1.4. CTR

Figure 3-12 (a) shows the time difference histogram using CFD. Figure 3-12 (b) shows the CTR values against the overvoltage and the error bars indicate the standard deviation of CTR values of the multiplexed SiPM channels. The lowest CTR values obtained using LED and CFD were 408 ± 13 and 382 ± 13, respectively, at an overvoltage of 2.7 V. Figures 3-12 (c) and (d) show the respective per-crystal CTR values measured at an overvoltage of 2.7 V using LED and CFD.

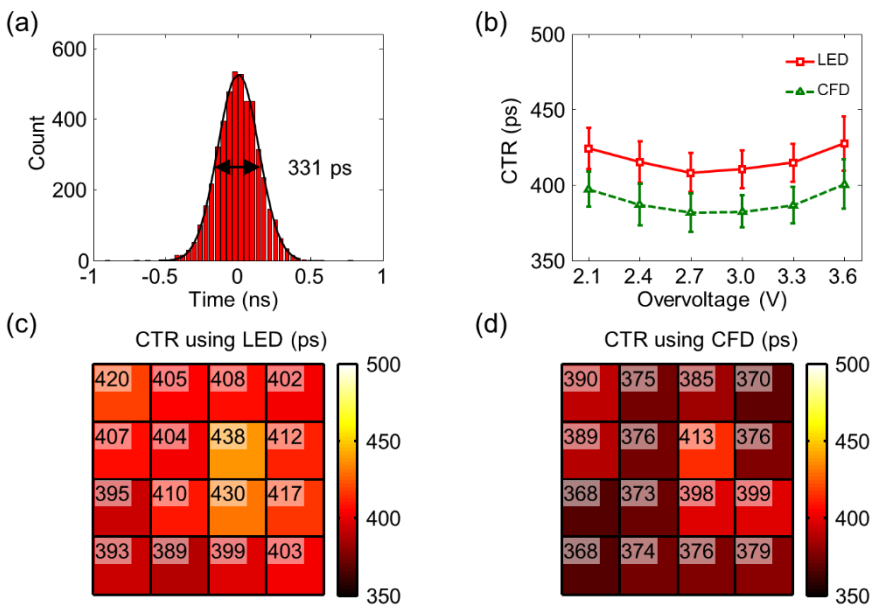

Figure 3-12. CTR values using the waveform digitizer. (a) Time difference spectrum between a SiPM channel with location (1, 2) and a reference detector. CFD was used. (b) CTR values against the overvoltage. (c) Per-crystal CTR values using LED. (d) Per-crystal CTR values using CFD.

3.3.2. FPGA-TDC

3.3.2.1. ToT and Energy

Figure 3-13 shows the ToT measurements for the LGSO/SiPM detector using the FPGA-TDC. As shown in Figure 3-13 (a), the photopeak region was resolved well using the ToT. Figure 3-13 (b) shows the calibration curve, and the error bars indicate the standard deviation of the ToT peak positions of the multiplexed SiPM channels. Figures 3-13 (c) and 3-13 (d) show the ToT peak positions and the per-crystal energy resolutions for 511 keV photopeak measured at 16 SiPM channels, respectively. The ToT peak positions of the 16 SiPM channels had the same tendency as the photopeak positions obtained using the waveform digitizer (Figure 3-11 (b)). The per-crystal energy resolution was 25.4 ± 0.8% FWHM at 511 keV.

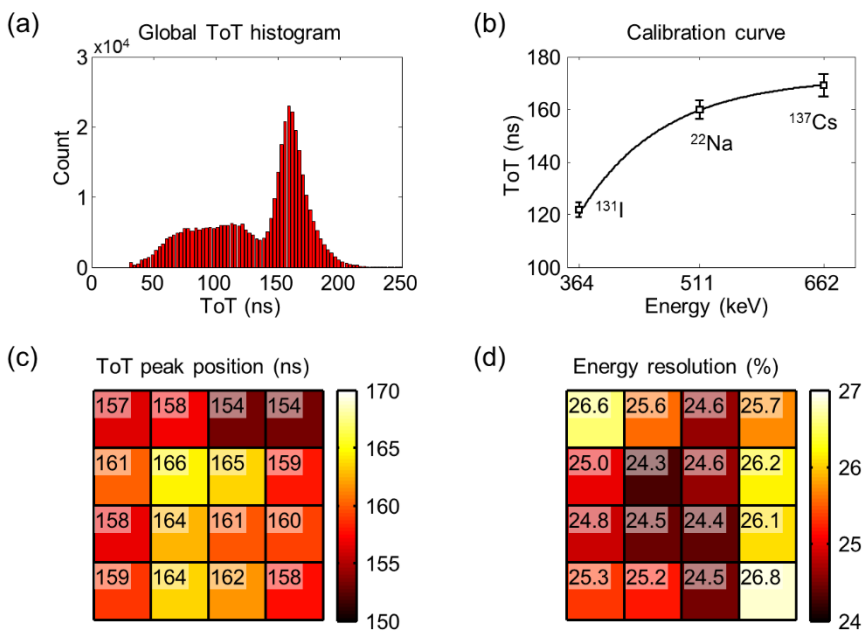

Figure 3-13. ToT measurements using the FPGA-TDC. (a) Global ToT histogram before gain variation correction. (b) ToT peak positions against energy. (c) ToT peak positions for 511 keV photopeak measured at 16 SiPM channels. (d) Per-crystal energy resolutions.

3.3.2.2. Flood Map

Figure 3-14 shows the flood map and 1D profiles while the DWR was 6.1. The distances between the adjacent spots along the *x* and *y* directions were 232 ± 25 and 295 ± 54 ps, respectively. The FWHM of the spots along the *x* and *y* directions were 42 ± 4 and 46 ± 2 ps, respectively.

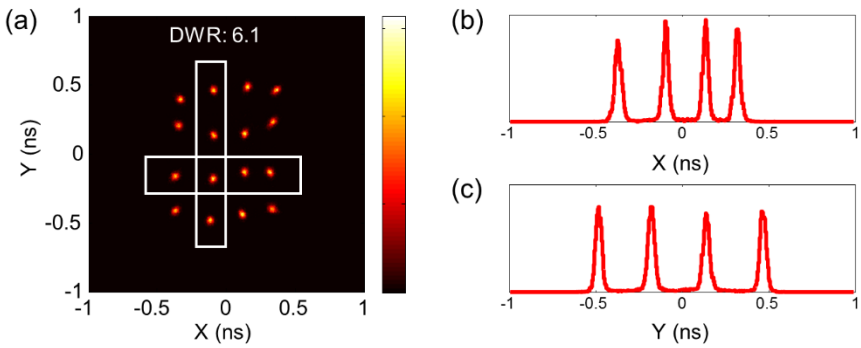

Figure 3-14. Flood map and 1D profiles obtained using the FPGA-TDC. (a) Flood map obtained using the FPGA-TDC with the 2% threshold at an overvoltage of 2.7 V. (b) 1D profile along the *x* direction. (c) 1D profile along the *y* direction.

3.3.2.3. CTR

Figures 3-15 (a) and (b) show the time difference histogram using the FPGA-TDC and the per-crystal CTR values, respectively. The per-crystal CTR was 406 ± 16 ps FWHM. The CTR values acquired using the FPGA-TDC were comparable with those measured using the waveform digitizer with the LED. As with the CTR values measured using the waveform sampler, these CTR values were uniform throughout the multiplexed SiPM channels.

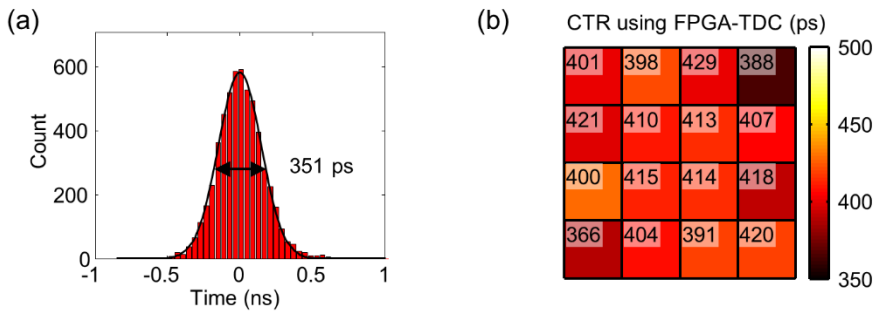

Figure 3-15. CTR measurements using the FPGA-TDC. (a) Time difference histogram between a SiPM channel with location (1, 2) and a reference detector. (b) Per-crystal CTR values obtained at an overvoltage of 2.7 V.

3.4. Discussion

The fully time-based multiplexing combined with FPGA-TDC-based readout method was proposed. The traces that connect every SiPM signals to the four timing pickoff channels were used to encode position information. The crystals were clearly resolved using the innate transit time differences measured at the four readout channels. The DAQ system of delay grid multiplexing can be simplified, because the timing channels were used to decode the position information.

In addition, the delay grid multiplexing can employ ToT after multiplexing because the signal shape and the amplitude did not change considerably by the multiplexing circuit, as shown in Figure 3-7. The minimal signal distortion allowed the consistent CTR values throughout the multiplexed SiPM channels as shown in Figures 3-12 and 3-15. Note that the conventional charge division circuits suffer from the signal distortion depending on the position of the charge division network.

In summary, the position, the energy, and the gamma arrival time were obtained using TDCs implemented in a single FPGA, while a dual-threshold ToT method could be applied after multiplexing. The fully simplified multiplexing and readout method would be useful for SiPM-based PET scanners that require simple electronics.

Chapter 4. FPGA-Only Signal Digitization Method

4.1. Background

Individual signal readout from the SiPM detectors can draw the best timing performance [10, 11] and improve sensitivity by identifying and recovering inter-crystal scattering events [53]. However, the biggest challenge with individual signal readout is the number of energy and timing channels that increases linearly with the number of SiPM channels.

The conventional DAQ systems usually use ADCs for energy measurements [12, 13]. However, ADC is not suitable for digitizing individual signals, because it is a large, power-intensive, and costly chip. The timing channel is space-, cost-, and power-efficient compared with the energy channel because the timing channel requires a discrete comparator and the TDC. In addition, TDC is usually implemented in the FPGA. Thus, time-based signal readout using the timing channels to obtain both energy and timing information is widely used to digitize individual signals as shown in Figure 4-1 (a) [19, 21-25, 54-56].

The FPGA-only digitization method is a promising individual signal digitization method because the discrete comparators in the time-based readout channels can be replaced with the general-purpose input/output (GPIO) ports of the FPGA. The GPIO ports of the FPGA can be configured to support various JEDEC standards, and the LVDS interface enables to digitize analog signals in the time domain as shown in Figure 4-1 (b) [24-26, 55]. However, the conventional FPGA-only digitization method using LVDS input receivers has the disadvantage that each LVDS input receiver requires two GPIOs: one for the signal and the other for the threshold. Thus, a new and more integrated FPGA-only signal digitization method

using only one GPIO for readout channel has been developed as shown in Figure 4-1 (c) [56].

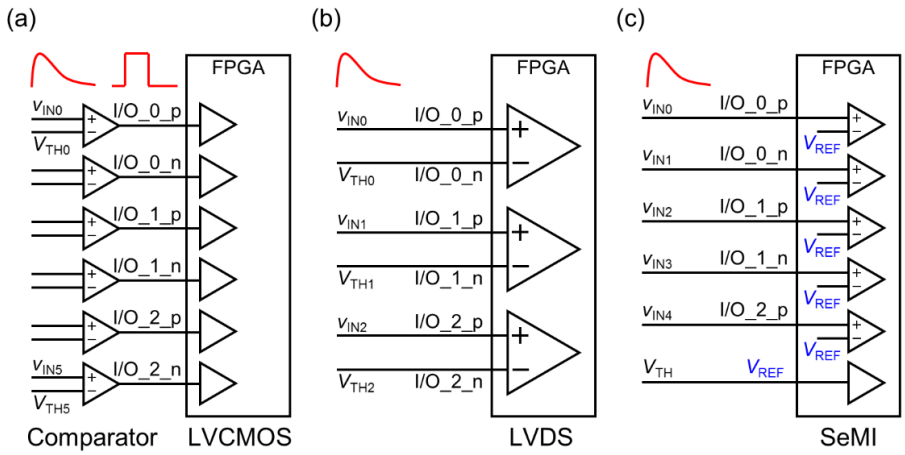

Figure 4-1. Time-based signal digitization methods. (a) Conventional time-based signal digitization method using the discrete voltage comparators. (b) Conventional FPGA-only signal digitization method using the LVDS input receivers. (c) Proposed FPGA-only signal digitization method using the single-ended memory interface input receivers.

4.2. Materials and Methods

4.2.1. Single-ended Memory Interface Input Receiver

Stub-series terminated logic (SSTL) and high-speed transceiver logic (HSTL) are single-ended JEDEC standards widely used in memory interfaces. Hereinafter, the SSTL and HSTL are denoted as single-ended memory interface (SeMI) in this thesis. The SeMI is a voltage-referenced interface where the I/O ports in an I/O bank share a common voltage reference V_{REF} that can be externally adjusted.

The principle of using each FPGA GPIO as the voltage comparator is as follows. The FPGA GPIO is configured with SSTL or HSTL input receiver and a common threshold is externally applied to a dedicated V_{REF} port. If the analog signal is greater than V_{REF}, the SeMI input receiver provides 1. Otherwise, the SeMI input receiver provides 0.

4.2.2. SeMI Digitizer

A new FPGA-only digitizer that digitizes the analog signal using the SeMI input receiver and the following timestamp modules is referred to as a SeMI digitizer in this thesis.

A Kintex-7 FPGA evaluation kit (KC705, Xilinx) was used to implement a new FPGA-only digitizer consisting of 82 energy and 82 timing channels as shown in Figure 4-2. The energy channel consisted of the SeMI input receiver and a multiphase counter (MPCNT). The ToT when the analog signal was greater than V_{REF} was measured with a resolution of 625 ps as shown in Figure 4-3. The timing channel consisted of the SeMI input receiver and TDC. The logic transition time when the analog signal crossed V_{REF} was measured with a resolution of 10 ps as shown in

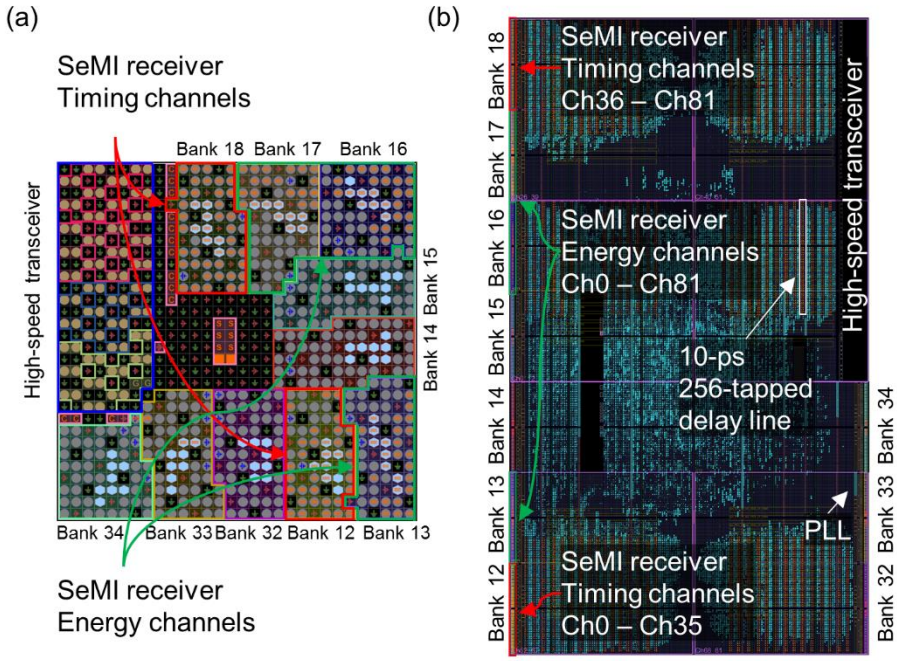

Figure 4-2. The layout of the SeMI digitizer using a Kintex-7 FPGA. (a) I/O ports. 164 GPIO ports were configured with SeMI input receivers. (b) Implementation.

Figure 4-3.

The input signal was fed into the SeMI input receiver directly and terminated to the ground using a 50 Ω resistor. A bypass capacitor of 0.1 μF was placed between V_{REF} and the ground for each dedicated V_{REF} port. The V_{REF} was adjusted using a 12-bit DAC (LTC2625, Linear Technology) from 0 to 2.048 V in steps of 0.5 mV.

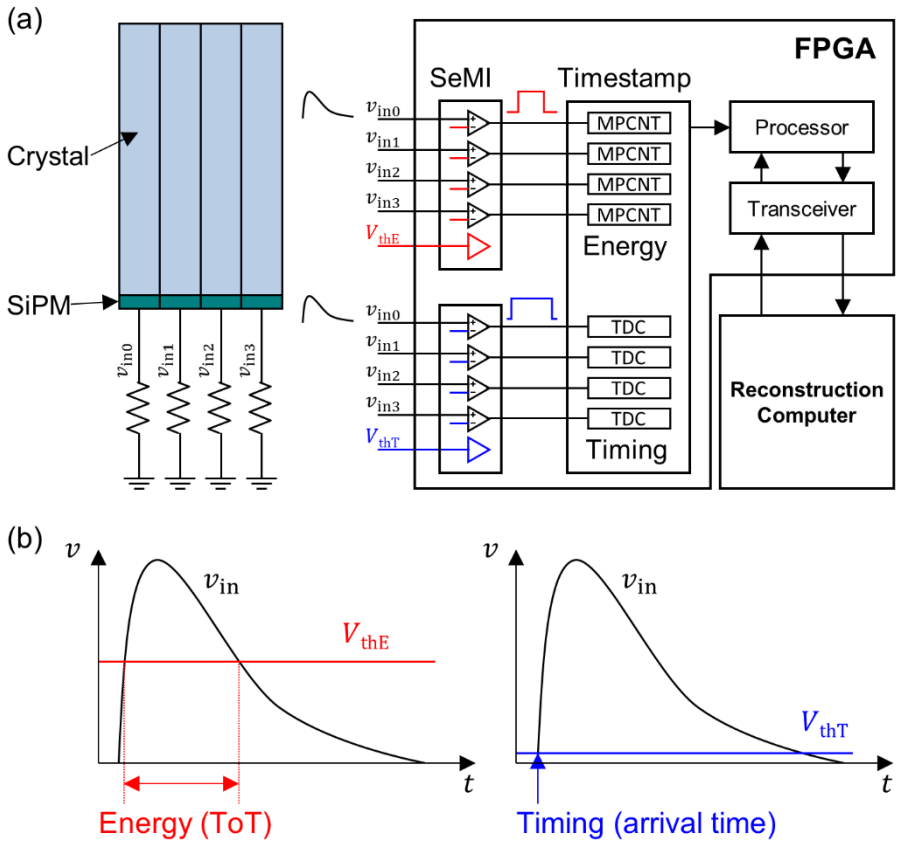

Figure 4-3. Conceptual diagram of the SeMI digitizer. (a) Individual signal digitization of SiPM-based TOF PET detector. (b) Energy and timing measurement methods using the SeMI digitizer.

4.2.3. Experimental Setup for Intrinsic Performance Characterization

The intrinsic performance of the SeMI digitizer was evaluated by applying the test pulses to SeMI digitizer. The test pulses were generated using a two-channel digital detector emulator (DT5800D, CAEN).

4.2.3.1. ToT

The triangular pulse v_{TRI} with the period, the offset voltage, and the peak-to-peak voltage of 1 μs, 1 V, and 2 V, respectively, was applied to the energy channel of the SeMI digitizer as shown in Figure 4-4 (a). Five energy channels located in different I/O Banks (Banks 12, 13, 16, 17, and 18) were evaluated. The SeMI input receivers were configured with HSTL and SSTL input receivers. The ToT value of the v_{TRI} was measured with changing the V_{REF} from 0.05 V to 1.95 V in steps of 0.05 V. The ToT values of 51,200 test pulses were collected and the mean and FWHM values were evaluated.

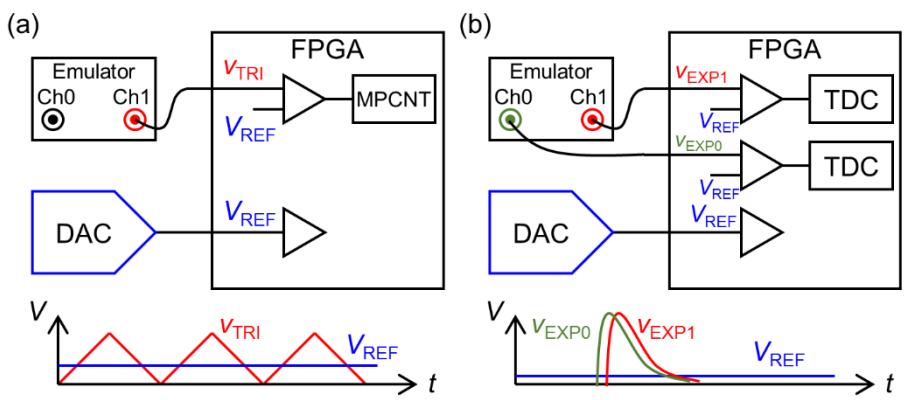

Figure 4-4. Experimental setup for the intrinsic performance characterization of the SeMI digitizer. (a) ToT. (b) Timing.

4.2.3.2. Timing

Two timing channels in the same I/O Bank (Bank 12) were evaluated and the SeMI input receivers were configured with HSTL and SSTL input receivers. Two copies of exponential pulses v_{EXP0} and v_{EXP1} with a fixed arrival time difference were fed into the two timing channels of the SeMI digitizer as shown in Figure 4-4 (b). The time differences were swept from −3008.4 to +3008.4 in steps of 501.4 ps. The 10-90% rise, decay times, and peak amplitude of exponential pulses were 7 ns, 40 ns, and 1 V, respectively. The V_{REF} of 50 mV was fixed. The time differences of 51,200 test pulses were collected and the mean and standard deviation (SD) values were evaluated.

4.2.4. Experimental Setup for Individual Signal Digitization

Data from two identical TOF PET detectors were obtained using the SeMI digitizer and the energy and coincidence timing resolutions were compared with those obtained using the 5-GSPS waveform digitizer (DT5742B, CAEN).

4.2.4.1. TOF PET Detector

Each detector consisted of a 3×3×20 mm^3 LYSO scintillation crystal coupled with a SensL J-series SiPM evaluation board (MicroFJ-SMA-30035, SensL) as shown in Figure 4-5. All the crystal surfaces were mechanically polished and the five surfaces except for the exit face were covered with the ESR films. The exit face was coupled with the SiPM using the optical grease (BC-630, Saint-Gobain). The detector was optically isolated using an in-house acrylonitrile butadiene styrene (ABS) frame made using a 3D printer (Mojo, Stratasys).

The SensL J-series SiPM has three terminals: bias input (cathode), standard

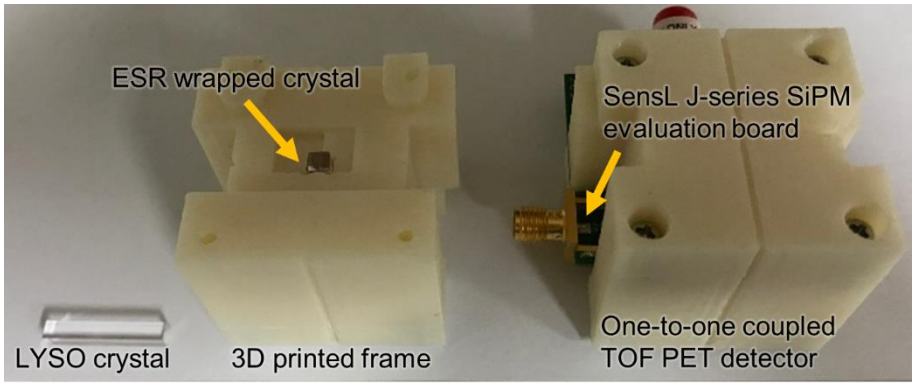

Figure 4-5. One-to-one coupled TOF PET detector.

output (anode), and fast output (high-pass filtered anode). The bias voltage of 32.0 V that corresponded to the overvoltage of 7.5 V was applied to the cathode. The standard and fast outputs were used to collect the energy and timing information.

The ^{22}Na point source was located between two detectors, with a face-to-face distance of 1 cm. The 51,200 coincidence events were collected. The ambient temperature was 25 °C and no thermal regulation was applied.

4.2.4.2. Data Acquisition Using the Waveform Digitizer

The in-house two-channel fan-out buffers and nuclear instrument modules (NIMs) were used to collect the coincidence events as shown in Figure 4-6 (a). The standard output signals of both detectors were fed into respective fan-out buffers. Each fan-out buffer consisted of two amplifiers with respective gains of +1 and −1. The inverted standard output signals were fed into the discriminator module (N843, CAEN), the coincidence module (N455, CAEN), and the NIM-TTL-NIM adapter (N89, CAEN) sequentially to generate coincidence trigger.

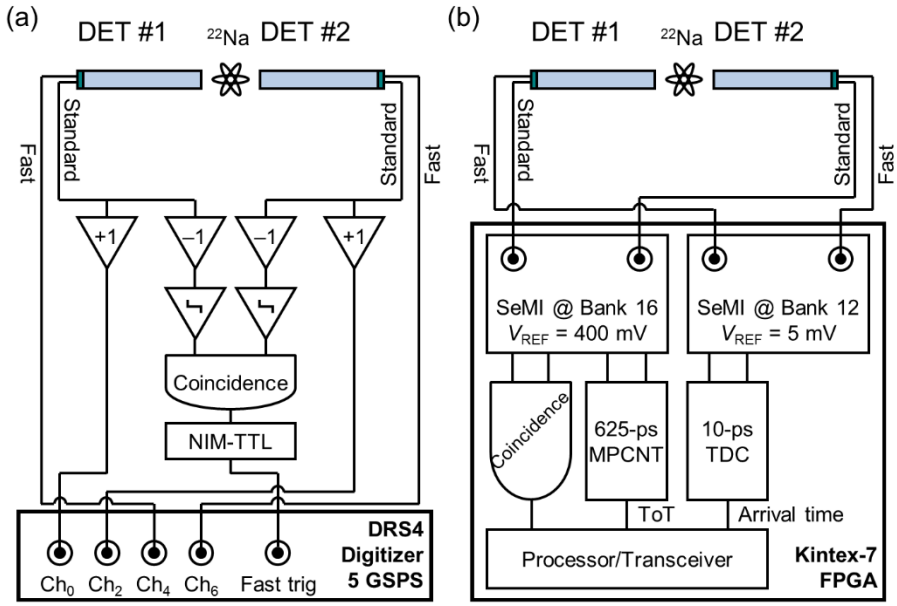

Figure 4-6. Experimental setups for performance evaluation of TOF PET detectors using (a) waveform digitizer and (b) SeMI digitizer.

The non-inverted standard output and the fast output signals were fed into the waveform digitizer with a sampling rate of 5 GSPS and a resolution of 12 bit.

The energy information was obtained from the standard output signal using two different methods. One was the integration method of summing the standard output signals for 160 ns after baseline correction. The other was the *in-silico* ToT method, the ToT was obtained by applying a digital threshold of 400 mV to the sampled standard output signal after baseline correction. The ToT calibration curve within the energy window of 250 to 750 keV by fitting *in-silico* ToT values and integrated values into the exponential function. The *in-silico* ToT values were converted into energy values using the ToT calibration curve.

The timing information was obtained using the digital leading edge discrimination method to fast output signals. The leading edge of the signal was interpolated 20 times, and a digital threshold of 5 mV was applied for time pickoff.

4.2.4.3. Data Acquisition Using the SeMI Digitizer

The standard output and the fast output signals were directly fed into the SeMI digitizer without any front-end electronics as shown in Figure 4-6 (b). Two energy and two timing channels of the 164-channel SeMI digitizer were used to collect data of TOF PET detectors. Energy channels were the SSTL input receivers with a V_{REF} of 400 mV and implemented in the Bank 16. Timing channels were the SSTL input receivers with a V_{REF} of 5 mV implemented in the Bank 12.

The energy was obtained by applying the ToT calibration curve to the ToT measurement of the standard output signal. The timing was obtained using the TDC. The coincidence windows were generated using the standard output signals, and the events within both windows were collected [51].

4.2.4.4. Data Analysis

The energy peak positions and the energy resolutions were evaluated by fitting the photopeak of the energy histogram to the Gaussian function. The CTR was evaluated by fitting the time difference histogram of coincidence events within both energy windows into the Gaussian function. The energy window was twice the FWHM of the photopeak. The energy resolution and the CTR values were expressed as the FWHM value of the Gaussian function.

4.3. Results

4.3.1. Results of Intrinsic Performance Characterization

4.3.1.1. ToT

The mean values of ToT for the v_{TRI} were changed linearly with the V_{REF} as shown in Figures 4-7 (a) and (b). Linear fitting was applied to measured data and the R^2 value, slope, *x*-intercept, and *y*-intercept of the linear fits were 1.0000, –0.5 ns/mV, 2 V, and 1 μs, respectively. The *x*-intercept and *y*-intercept corresponded the peak-to-peak voltage and period of the v_{TRI}. In addition, The FWHM values of ToT for the v_{TRI} were less than 3%, except for very short ToT as shown in Figures 4-7 (c) and (d).

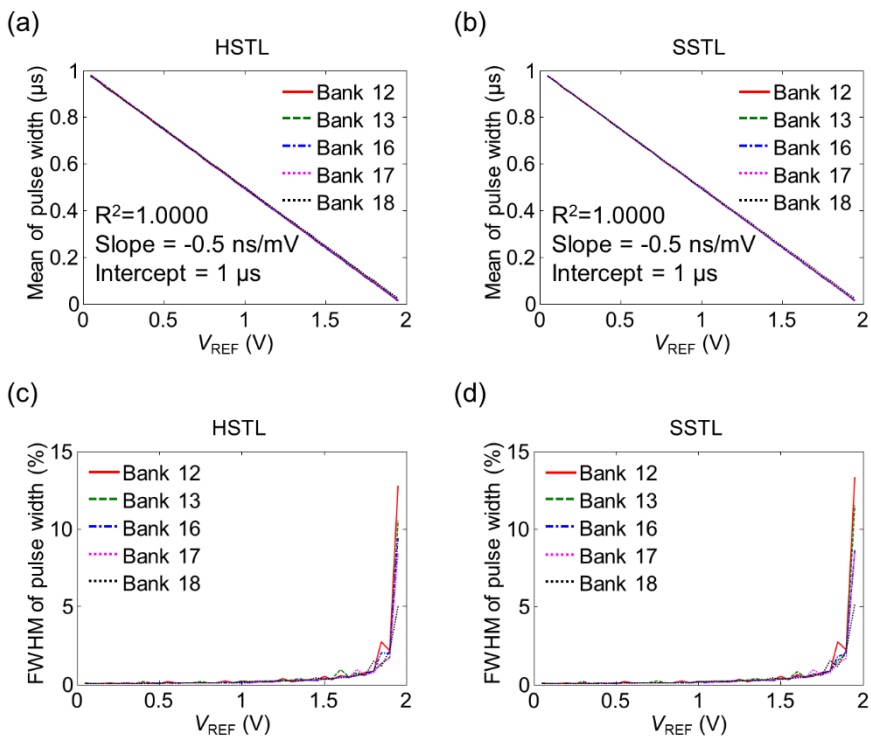

Figure 4-7. ToT measurement using the SeMI digitizer. Mean and FWHM values of the measured ToT of the triangular pulse v_{TRI} against the reference voltage V_{REF}. The SeMI input receiver was configured with an HSTL or SSTL input receiver.

The SeMI input receivers implemented in multiple I/O Banks showed almost identical performance. In addition, the I/O configuration either HSTL or SSTL did not affect the ToT measurements.

4.3.1.2. Timing

The time differences between v_{EXP0} and v_{EXP1} were accurately measured as shown in Figures 4-8 (a) and (b). In addition, the SD values were less than 14.6 ps (= 34.4 ps FWHM) as shown in Figure 4-8 (c). The I/O configuration either HSTL or SSTL did not affect the timing performance of the SeMI digitizer.

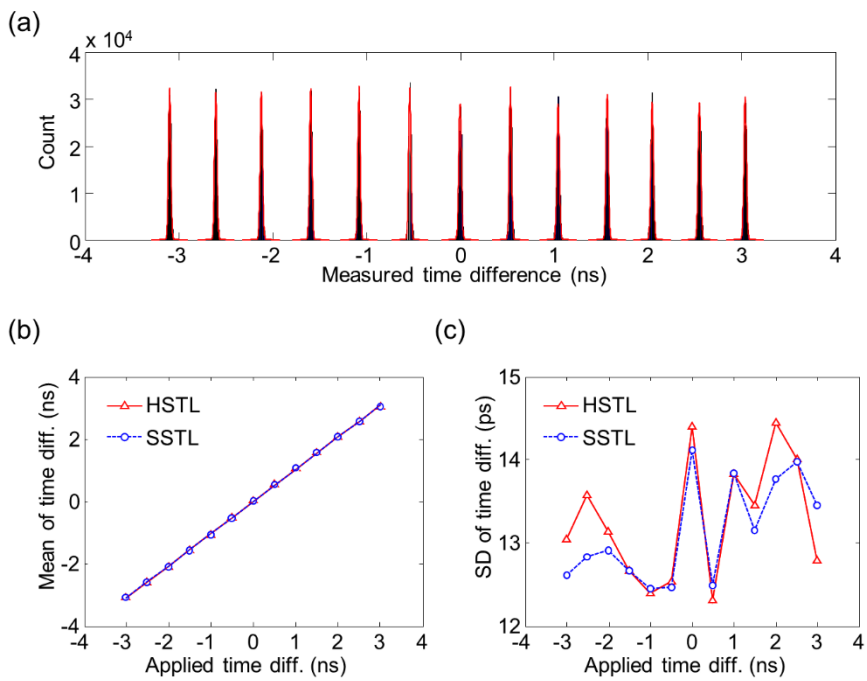

Figure 4-8. Arrival time difference measurement. (a) Merged arrival time difference histogram. (b) Mean values of the measured time differences. (c) Standard deviation values of the measured time differences.

4.3.2. Results of Individual Signal Digitization

4.3.2.1. Energy

The ToT calibration curves were calculated using the integration and *in-silico* ToT values as shown in Figure 4-9 (a). The *in-silico* ToT and SeMI ToT values were converted into energy values using the respective ToT calibration curves. Figure 4-10 shows the energy histograms obtained using the integration, *in-silico* ToT, and SeMI ToT methods. The SeMI digitizer resolved photopeak well. The energy resolutions of two detectors using the integration method were 6.1% and 6.8%. Those using the in-silico ToT method were 7.5% and 6.5%. Those using the SeMI ToT were 7.7% and 7.1%.

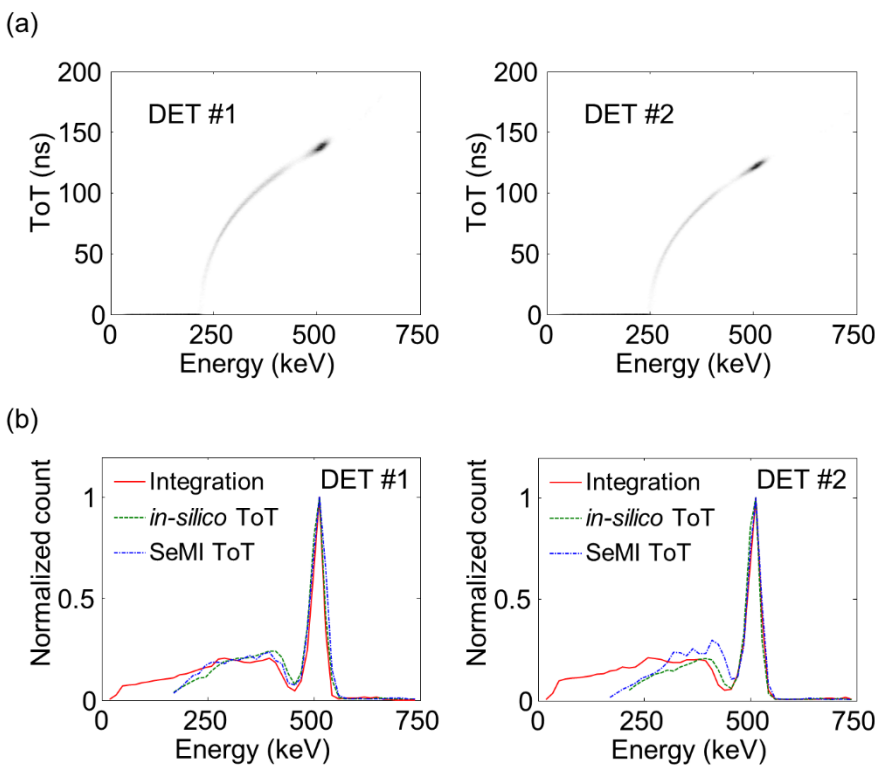

Figure 4-9. Energy histograms. (a) Relationship of energy and ToT. (b) Normalized energy histograms using integration, *in-silico* ToT, and SeMI ToT methods.

4.3.2.2. CTR

Figure 4-10 shows the time difference histograms obtained using the waveform digitizer and the SeMI digitizer. The energy windows generated by the integration, *in-silico* ToT, and SeMI ToT methods were applied. The CTR values were 203, 205, and 204 ps FWHM, respectively.

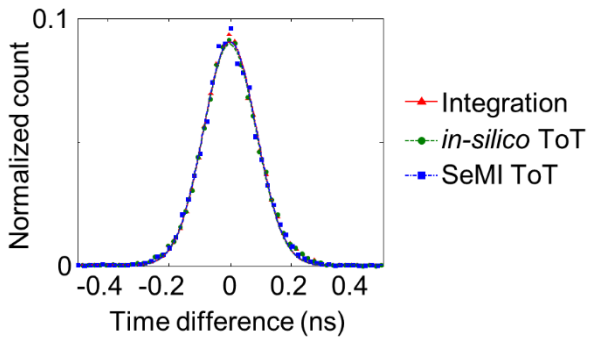

Figure 4-10. Normalized time difference histogram. The energy windows generated using integration, *in-silico* ToT, and SeMI ToT methods were applied.

4.4. Discussion

In the results of intrinsic performance evaluation of the SeMI digitizer, the SeMI input receiver functioned as the fast voltage comparator without undesirable offset voltage. The fast transition of SeMI input receiver is suitable for TOF measurement. The timing jitter of a single timing channel was less than 10.3 ps. In addition, the SeMI input receiver does not require any offset voltage calibration for both energy and timing channels. Furthermore, the multiple SeMI input receivers showed the equivalent performance and crosstalk between the adjacent SeMI input receivers was negligible, and thus all GPIOs can be used as high-performance voltage comparators for the time-based digitizer.

The SeMI digitizer also showed the comparable performance with the 5 GSPS waveform digitizer. The energy resolution and the CTR using the SeMI digitizer were almost identical with those obtained using the 5 GSPS waveform digitizer. In addition, the CTR of 204 ps was obtained by directly digitizing SiPM signals without any front-end electronics.

The SeMI digitizer greatly simplifies the high-performance DAQ electronics, because it does not require front-end electronics such as a discrete comparator, ADC or TDC. Therefore, the SeMI digitizer is useful for applications that require multichannel signal digitization such as individual signal readout to achieve the best performance [57, 58] and the total-body PET scanners to increase the sensitivity [8, 9, 59]. In addition, the SeMI digitizer is suitable for simultaneous PET/MRI scanners where the early signal digitization preferred but the volume of electronics is limited [58, 60-62]

The SeMI digitizer can be combined with other time-based readout and

multiplexing methods. The MVT can be used by applying the signal to SeMI digitizer located in multiple I/O Banks [54, 55]. The QTC [21, 22] which is also known as pulse width modulation [23] can be combined with the SeMI digitizer. The QTC requires a common threshold for energy measurement and thus is suitable with the SeMI digitizer. The time-based multiplexing methods such as strip-line multiplexing [47] and delay grid multiplexing [48] that identify crystal positions using transit time differences employ the common threshold for time pickoff.

Furthermore, the FPGA-only digitizer has the inherent advantages of FPGA: fast time to market and low non-recurring engineering. Compared with the conventional FPGA-only digitizer using the LVDS input receivers, the LVDS digitizer is more flexible than the SeMI digitizer. Each digitization channel using LVDS input receiver has an individual threshold, and thus thresholds for MVT method can be optimized [54, 55]. In addition, the dynamic threshold method and the sigma-delta modulation can be applicable [24, 25]. However, the SeMI input receiver can handle twice as signal channels as the LVDS digitizer and the layout becomes easier. Therefore, the SeMI digitizer is well-suitable for ToT and QTC.

Chapter 5. Comparator-less QTC DAQ Systems for High-Resolution Brain PET Scanners

5.1. Background

A brain PET scan is the most sensitive imaging modality to diagnose neurodegenerative diseases before the morphological changes occur [63-65]. However, the conventional PET scanners suffer from the relatively poor spatial resolution that leads to inaccurate quantitative analysis due to partial volume effect [66-68]. In addition, a parallax error further deteriorates the spatial resolution in the peripheral region of the brain. Thus, the high-resolution brain PET scanner that can mitigate partial volume effect and parallax error is required for accurate diagnosis of neurodegenerative diseases.

PET detectors with small crystal pitches and depth-of-interaction (DOI) capability can achieve a high spatial resolution of the entire brain region uniformly. The staggered DOI PET detector with dual-layer crystals with relative offsets of one half a crystal pitch in both *x*- and *y*-directions is widely used in brain and small-animal PET scanners owing to narrow gaps between block detectors [69-72]. In addition, the staggered DOI PET detector is compatible with the charge division circuits and the DAQ systems that obtain position and energy information using charge measurement channels, because the staggered DOI PET detector uses light sharing design.

The highly integrated FPGA-only digitizer simplifies DAQ system using all FPGA GPIOs as voltage comparators and it is suitable for individual signal digitization of the one-to-one coupled PET detectors [56]. However, it is challenging to acquire data of light sharing PET detectors using the SeMI digitizer, because the

ToT method intrinsically suffers from the energy non-linearity. In addition, most charge division circuits distort the waveform of the energy signal depending on the position and make it impossible to obtain crystal position using ToT method [73].

Contrary to other time-based readout methods, the QTC converts the input charge into the pulse width linearly [21-23]. The non-gated QTC can simplify the QTC design because it does not require complex control logic and switches [21, 22]. Thus, the QTC can be used to obtain data from the high-resolution staggered DOI PET detectors with light sharing and charge division circuits. In addition, the QTC is well-suited with the SeMI digitizer, because it requires the common threshold for charge measurements [56].

5.2. Materials and Methods

5.2.1. Brain PET Scanner

5.2.1.1. Block Detector

The high-resolution staggered DOI PET detector consisted of a dual-layer crystal array coupled with a SiPM array as shown in Figure 5-1. The upper-layer crystals were 13×13 array of 1.78×1.78×8 mm^3 LSO crystals and the lower-layer crystals were 14×14 array of 1.78×1.78×12 mm^3 LSO crystals. The crystals were optically isolated using ESR film except for the exit face, and crystal pitches for both layer crystals were 1.86 mm. The lower-layer crystals were coupled with the SiPM array that consisted of a 2×2 array of 4×4 SiPMs (S13361-3050NE-04, Hamamatsu Photonics K. K.). The optical grease (BC-630, Saint-Gobain) was used to enhance optical coupling between the crystal and the SiPM arrays. The cross-section of the block detector was 26×26 mm^2.

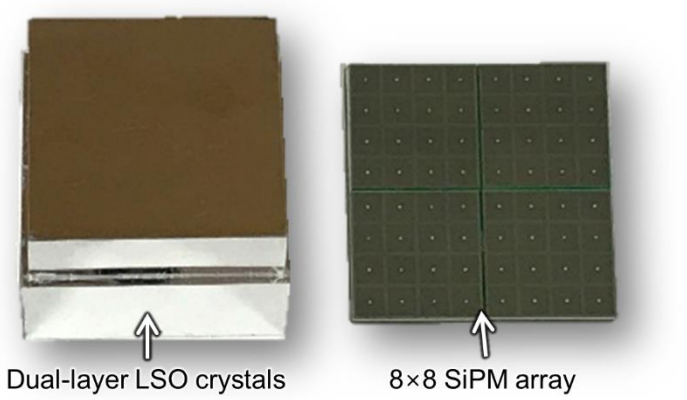

Figure 5-1. Block detector.

5.2.1.2. Sector

Each sector consisted of up to 2×2 block detectors and a front-end board (FEB) as shown in Figure 5-2. The FEB multiplexed energy and timing signals. The 64 SiPM anodes of the block detector were multiplexed into 8 row and 8 column signals using amplifiers (AD8003, Analog Devices), and then further multiplexed into the four position-encoded energy signals of X^+, X^-, Y^+, and Y^- using weighted summing circuits. In addition, 8 column signals were fed into respective comparators (ADCMP601, Analog Devices), and then the comparator outputs were logically OR-ed to generate a single digital timing pulse. The multiplexing ratios for energy and timing signals were 64:4 and 64:1, respectively. The 16 energy and 4 timing signals per sector were output.

The on-board micro-controller unit (ATmega128A, Atmel) controlled DAC (AD5629R, Analog Devices) outputs using the inter-integrated circuit (I^2C) interface to adjust SiPM bias voltages and comparator threshold voltages.

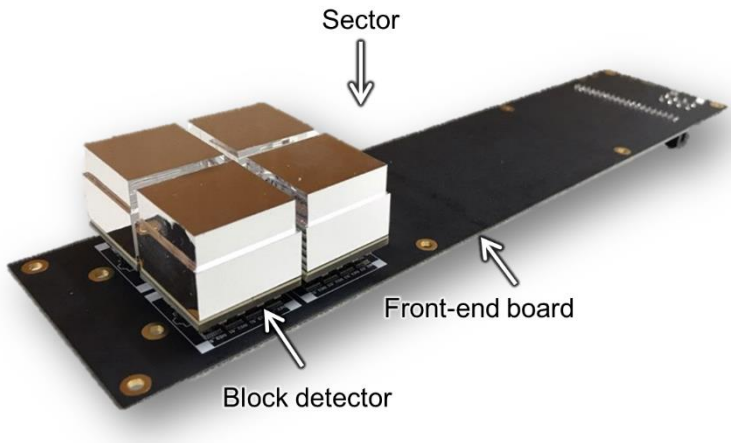

Figure 5-2. Sector. It consisted of 2×2 block detectors and a front-end board.

5.2.1.3. Scanner Geometry

The brain PET scanner consisted of 14 sectors with a ring diameter of 254 mm as shown in Figure 5-3. Two block rings with an axial length of 54 mm can be equipped, but the single block ring with the axial length of 26 mm was equipped. The DC-fans and aluminum heat sinks were mounted on the FEB for thermal regulation.

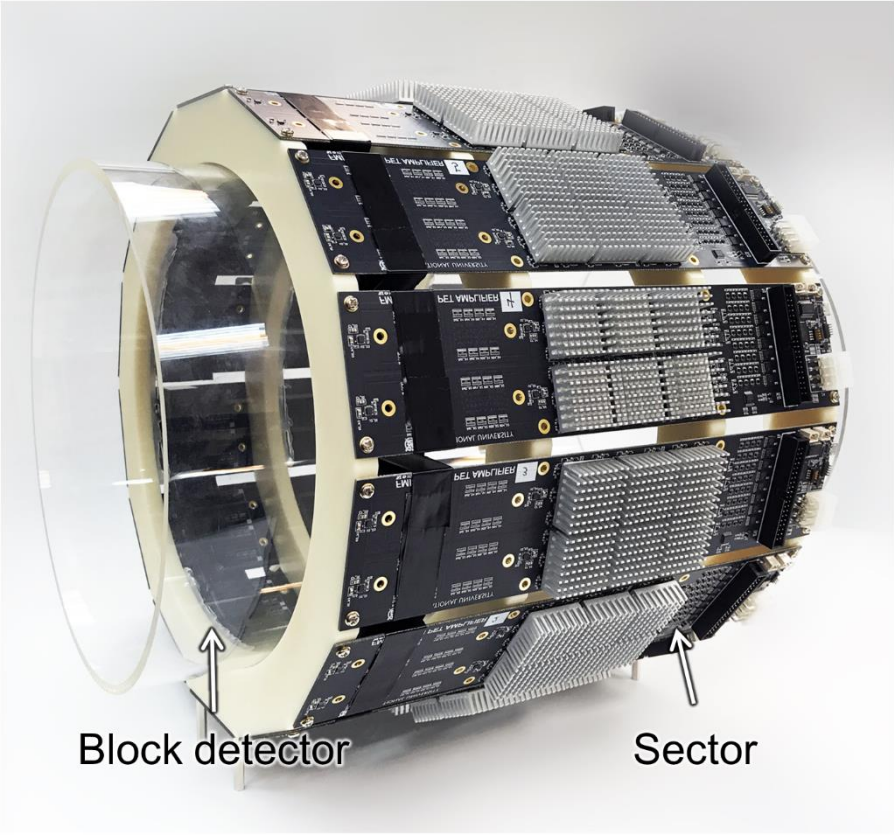

Figure 5-3. Prototype high-resolution brain PET scanner.

5.2.2. Comparator-less QTC DAQ Systems

The comparator-less QTC DAQ systems were developed to collect data from a high-resolution brain PET scanner as shown in Figure 5-4. The DAQ consisted of a QTC board, a Kintex-7 evaluation kit (KC705, Xilinx), and switched-mode power supplies. It was housed in a 19-inch 3U aluminum case.

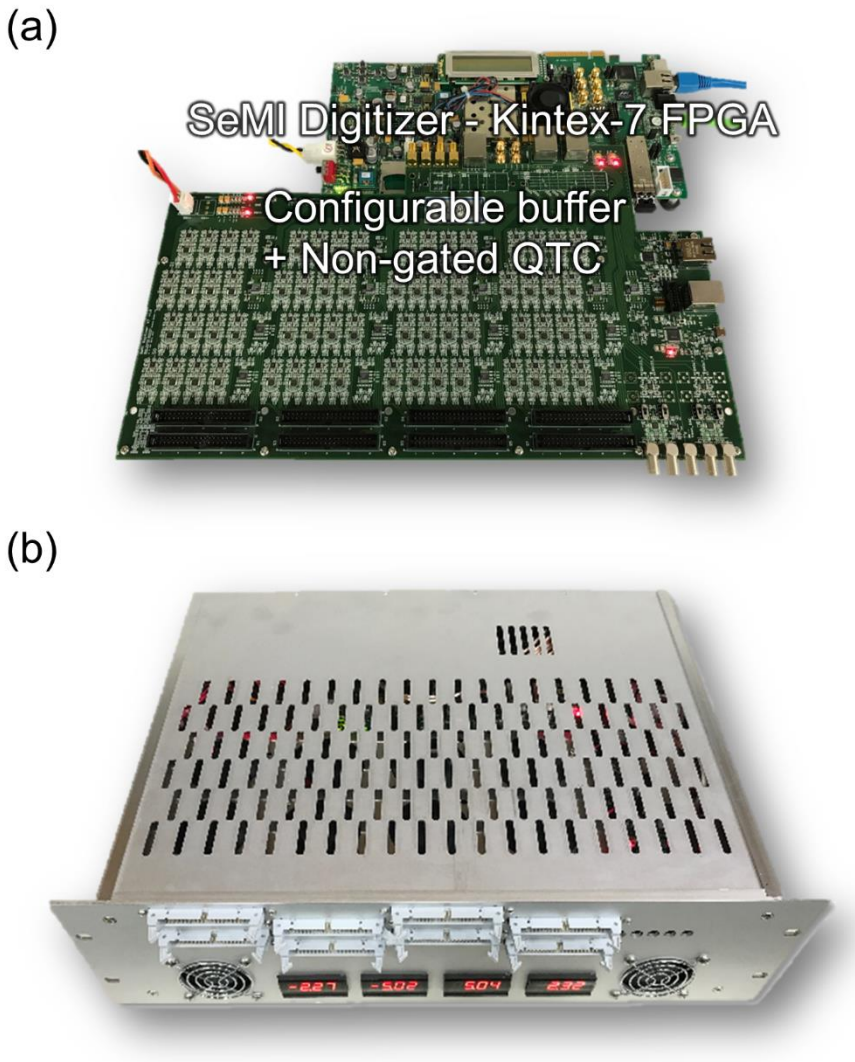

Figure 5-4. Comparator-less QTC DAQ system. (a) The DAQ system contained 132 energy and 33 timing channels. (b) The DAQ system housed in a 19-inch 3U case.

Each DAQ system had 132 energy and 33 timing channels to digitize signals from up to 33 block detectors.

The energy channel consisted of a configurable buffer, a non-gated QTC, a SeMI input receiver, and an MPCNT as shown in Figure 5-5. The configurable buffer can receive either differential or single-ended input with both polarities. It consisted of a differential amplifier (ADA4932-2, Analog Devices) and a double pole double throw switch (JS202011CQN, C&K). If the input signal v_{in} was positive, the inverting output was selected as the input of the non-gated QTC. If the single-ended input v_{in} was positive, the inverting output $-v_{in}\times R_f/(2\times R_g)$ was selected as the QTC input, and vice versa. The R_f and R_g were 1 kΩ. The selected voltage output of the differential amplifier was AC-coupled and then converted into the current input i_{in} using a resistor R_{in}.

The non-gated QTC converted i_{in} into the dual-slope pulse of which pulse width was proportional to i_{in}. It consisted of an amplifier (AD8066, Analog Devices), a Schottky diode (1PS10SB82, NXP), a DAC (LTC2625, Linear Technology), and a few passive components. The inverting input of the amplifier was at the virtual

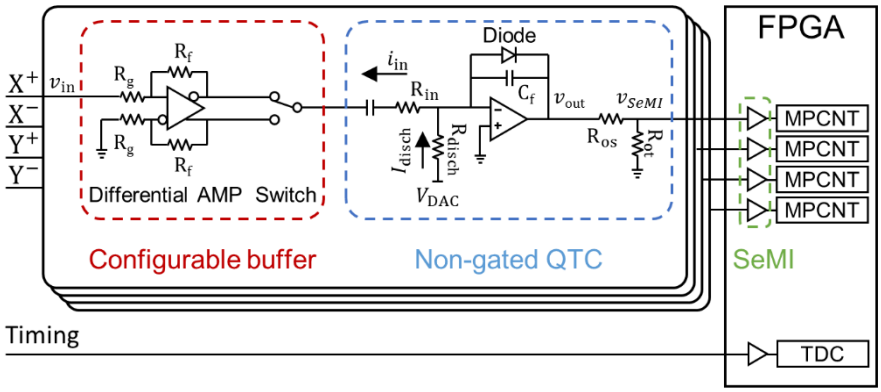

Figure 5-5. Schematic of energy and timing channels for data acquisition of each block detector.

ground, so that the voltage output of the differential amplifier and the DAC voltage output V_{DAC} were converted into the current input i_{in} and the discharge current I_{disch} using R_{in} and R_{disch} as in (5.1) and (5.2), respectively. The R_{in}, C_f, R_{disch}, and I_{disch} were 24 Ω, 200 pF, 1 kΩ, and 1 to 2 mA, respectively.

$$i_{\mathrm{in}} = \frac{v_{\mathrm{in}}}{\mathrm{R_{in}}} \times \frac{\mathrm{R_f}}{2\mathrm{R_g}} \tag{5.1}$$

$$I_{\mathrm{disch}} = \frac{V_{\mathrm{DAC}}}{\mathrm{R_{disch}}} \tag{5.2}$$

The non-gated QTC automatically controlled the idle, charge, and discharge phases [21, 22]. In the idle, the diode flowed the I_{disch}, and the voltage output v_{out} of the amplifier was at the baseline of −0.3 V. When the i_{in} became greater than I_{disch}, the QTC was in the charge phase. The diode blocked and $i_{in} - I_{disch}$ began to charge the feedback capacitor C_f, and then the v_{out} rose. When the i_{in} became smaller than I_{disch}, the QTC was in the discharge phase, the diode started to flow the current of $I_{disch} - i_{in}$, and if i_{in} was zero in the discharge phase, the v_{out} dropped linearly until v_{out} restored the baseline. The pulse width during the charge and discharge phases was proportional to the input charge by applying the threshold voltage slightly greater than the baseline. The input signal v_{SeMI} was the linearly attenuated signal of the v_{out} to limit the upper voltage level of v_{SeMI} less than the I/O Bank supply voltage of 2.5 V. The resistor dividers R_{os} and R_{ot} with the resistor values of 50 Ω were used. The threshold voltage for the v_{SeMI} was applied to the dedicated V_{REF} port of the I/O Bank. The V_{REF} value was −0.1 V. The pulse width was measured using an MPCNT with a resolution of 625 ps.

The timing channel was a heterogeneous sampling TDL TDC implemented in the same FPGA [38, 39]. The coarse counter was a 12-bit binary counter operating at the main clock frequency of 400 MHz and provided the coarse count N. The fine time interpolator consisted of a 300-tap carry chain, sampling flip-flops, a fine-code encoder, and a fine-time calibrator. The LSB of TDC was 10 ps. The asynchronous timing signal was delayed with changing the states of delay elements, and sampled by flip-flops at the rising time of the main clock signal. The sampled states were converted into a fine code using a fine-code encoder. The fine code was calibrated to a fine time f of which dynamic range was 0 to 2500 ps using a fine-time calibrator. The arrival time t_{arr} was calculated as in (5.3).

$$t_{\mathrm{arr}} = N \times 2500 \ \ \mathrm{ps} - f \tag{5.3}$$

The Kintex-7 evaluation kit has 192 accessible ports in five I/O Banks (Bank 12, 13, 16, 17, and 18) through FPGA Mezzanine Card (FMC) connectors. 132 energy channels were implemented by configuring 132 GPIOs of the I/O Bank 12, 13, 16, and 17 as the SSTL input receivers. The threshold of −0.1 V was applied to the semi-dedicated V_{REF} ports. 33 timing channels were implemented by configuring 33 GPIOs of the I/O Bank 18 as LVCMOS input receivers. Although the SeMI input receiver can digitize analog timing signals with a low jitter of 10 ps [56], the LVCMOS input receiver was used to receive the digital timing signal from the FEB.

5.2.3. Data Acquisition Chain of Brain PET Scanner

Two comparator-less QTC DAQ systems were used to collect data from the prototype high-resolution brain PET scanner. The signals from the 6 sectors were fed into the first time-based DAQ and the other signals from the 8 sectors were fed into the second time-based DAQ system through 40 pin ribbon cables. Two time-based DAQ systems and the master DAQ were connected using daisy chains through 2.5 Gbps gigabit transceivers and pairs of coaxial cables. The master DAQ was implemented using a Virtex-6 evaluation kit (ML605, Xilinx). It identified the prompt and delayed coincidence events based on timestamps and transmitted them to the computer through 1 Gbps Ethernet [74].

Two time-based DAQ systems were synchronized using an in-house clock distributor. The clock distributor consisted of a 2:8 clock fanout buffer (8SLVD1208, IDT) and a 200 MHz clock oscillator (SiT9120, SiTime). The clock distributor fed common clock and synchronization signals to two time-based DAQ systems.

5.2.4. Experimental Setups and Data Processing

5.2.4.1. Energy Linearity

The energy linearity of the energy channel was measured by applying the exponential pulses v_{EXP} with different amplitudes to the energy channel. The digital detector emulator (DT5800D, CAEN) was used. The 10-90% rise and decay times of the v_{EXP} were 7 ns and 40 ns, respectively. The peak amplitudes were swept from 0.6 to 3.3 V in steps of 0.3 V. The I_{disch} was 2 mA. The pulse width when the v_{SeMI} was higher than the V_{REF} was measured. The pulse widths of the v_{SeMI} for 10,240 test pulses were measured and the mean and FWHM were evaluated.

5.2.4.2. Performance Evaluation of Block Detector

The signals from the block detector were digitized using the time-based DAQ system and the waveform digitizer (DT5742B, CAEN) to verify that the time-based DAQ has the comparable DAQ performance with the waveform digitizer as shown in Figure 5-6. The reference detector (R9800, Hamamatsu Photonics K. K.) and the NIMs were used to obtain the coincidence events. The ^{22}Na point source was attached at the reference detector and the distance between the block detector and the reference detector was 20 cm. The timing pulse of the high-resolution DOI detector was converted to NIM trigger using NIM-TTL-NIM adapter (N89, CAEN) and then fed into the coincidence module (N455, CAEN). The timing pulse of the reference detector was generated using the discriminator module (N843, CAEN), and then fed into the coincidence module. The coincidence trigger was fed into the

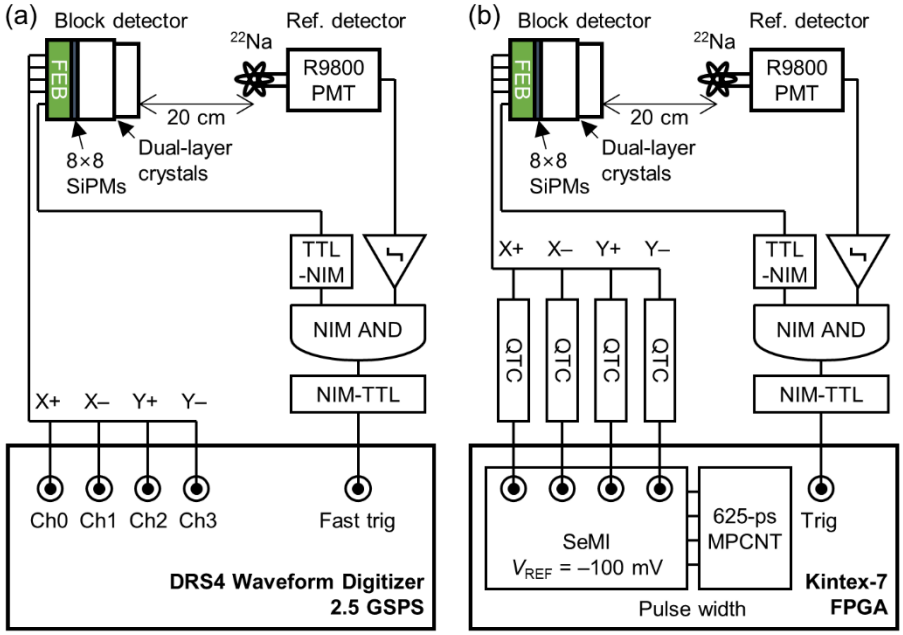

Figure 5-6. Experimental setups for performance evaluation of block detector using (a) waveform digitizer and (b) comparator-less QTC DAQ

NIM-TTL-NIM adapter, and then converted into TTL interface. Both the waveform digitizer and the time-based DAQ system collected 2,000,000 coincidence events.

In the experimental setup using the waveform digitizer as shown in Figure 5-6 (a), the coincidence trigger was fed into the fast trigger of the waveform digitizer. In addition, four energy signals were input into the waveform digitizer. The waveform digitizer samples the energy signals with a sampling rate of 2.5 GSPS and a resolution of 12 bits. The energy signals of X^{+}, X^{-}, Y^{+}, and Y^{-} were accumulated for 140 ns after the respective baseline correction, and the energy values of $E_{\mathrm{X}^{+}}$, $E_{\mathrm{X}^{-}}$, $E_{\mathrm{Y}^{+}}$, and $E_{\mathrm{Y}^{-}}$ were obtained.

In the experimental setup using the time-based DAQ system as shown in Figure 5-6 (b), the coincidence trigger was fed into the trigger channel. The energy signals were digitized by four energy channels and the measured pulse widths were considered as the energy values of $E_{\mathrm{X}^{+}}$, $E_{\mathrm{X}^{-}}$, $E_{\mathrm{Y}^{+}}$, and $E_{\mathrm{Y}^{-}}$.

The normalized crystal positions of x and y and the energy E were calculated as in (5.4), (5.5), and (5.6), respectively.

$$x = \frac{E_{\mathrm{X}^{+}} - E_{\mathrm{X}^{-}}}{E_{\mathrm{X}^{+}} + E_{\mathrm{X}^{-}}} \tag{5.4}$$

$$y = \frac{E_{\mathrm{Y}^{+}} - E_{\mathrm{Y}^{-}}}{E_{\mathrm{Y}^{+}} + E_{\mathrm{Y}^{-}}} \tag{5.5}$$

$$E = \frac{E_{\mathrm{X}^{+}} + E_{\mathrm{X}^{-}} + E_{\mathrm{Y}^{+}} + E_{\mathrm{Y}^{-}}}{4} \tag{5.6}$$

The per-crystal energy photopeak positions and energy resolutions were evaluated after crystal identification. The energy resolution values were expressed as the FWHM value of the Gaussian function.

5.2.4.3. Phantom Studies

A hot-rod, a uniform phantom, a 2D Hoffman brain phantom was imaged using the developed high-resolution PET scanner and the time-based DAQ systems. A hot-rod phantom has six types of hot rods with diameters of 1.2, 1.6, 2.4, 3.2, 4.0, and 4.8 mm. The uniform phantom has an inner diameter of 10.5 cm. All phantoms were filled with ^{18}F-FDG with the respective activities of 1.3, 1.7, and 1.7 mCi. The scan times were 2 hours.

The phantom images were reconstructed using the 3D ordered subset expectation maximization (OSEM). For the hot-rod phantom, the iteration number, the number of subsets, and voxel size were 64, 4, 0.465×0.465 ×0.93 mm^3. For the uniform phantom, those were 2, 4, and 0.93×0.93 ×0.93 mm^3. For the 2D Hoffman brain phantom, those were 32, 4, 0.93×0.93 ×0.93 mm^3. The post-filters with the respective Gaussian kernel sizes of 0.93 and 1.86 mm were applied to the hot-rod and the 2D Hoffman brain phantom images.

The direct normalization was conducted using data obtained with a ^{68}Ge quality assurance phantom source. The attenuation correction was based on the *x*-ray CT scan. The random correction from the delayed coincidence data generated by the coincidence processor was applied. The scatter correction was not applied.

The uniformity was calculated using the reconstructed uniform phantom image as in (5.7).

$$\text{Uniformity} = \frac{\text{SD}(\text{Intensity}_{\text{ROI}})}{\text{Mean}(\text{Intensity}_{\text{ROI}})} \tag{5.7}$$

5.3. Results

5.3.1. Energy Linearity

The pulse width of the modulated exponential pulse was linearly changed with the amplitude of the exponential pulse. The linear fit was applied and the R^2 value was 0.9981 as shown in Figure 5-7 (a). The FWHM value of the pulse width was less than 3% as shown in Figure 5-7 (b).

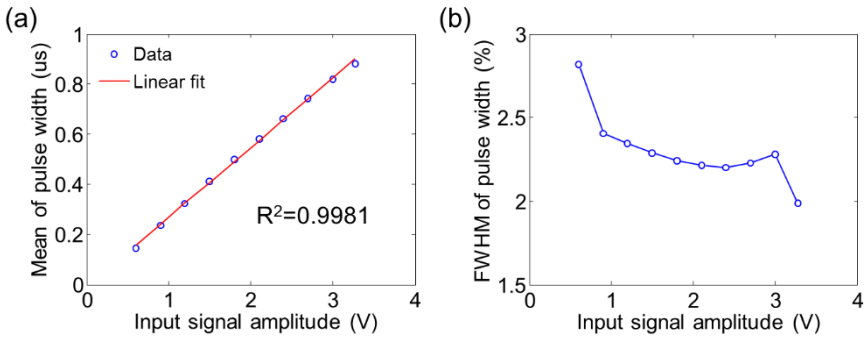

Figure 5-7. Energy linearity of the comparator-less QTC DAQ. (a) Mean values of the measured pulse width. (b) FWHM values of the measured pulse width.

5.3.2. Performance Evaluation of Block Detector

Figure 5-8 shows the flood maps obtained using the waveform digitizer and the time-based DAQ system. For both DAQ systems, all crystals of both crystal layers were clearly resolved in the flood maps. This represents that the position information of high-resolution crystals with small pitches of 1.86 mm and the two-layer DOI information can be obtained using four energy channels of the time-based DAQ system.

Normalized per-crystal photopeak positions were almost identical for the waveform digitizer and the time-based DAQ system as shown in Figure 5-9 (a). Per-

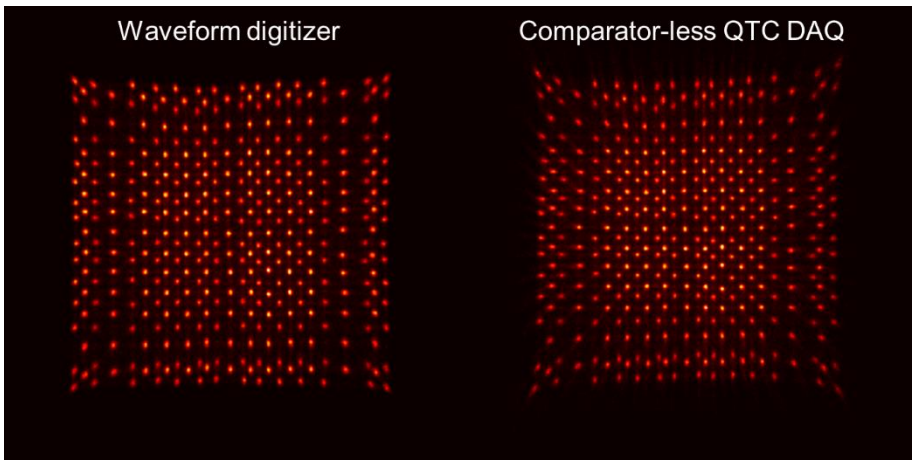

Figure 5-8. Flood maps obtained using the waveform digitizer and the time-based DAQ system.

crystal energy resolutions were slightly degraded especially for the lower-layer corner crystals as shown in Figure 5-9 (b). The energy resolutions for the upper and the lower layers obtained when using the waveform digitizer were 9.9 ± 0.4% and 10.2 ± 0.9%, respectively. Those obtained using the time-based digitizer were 11.0 ± 0.6% and 11.4 ± 1.4%, respectively.

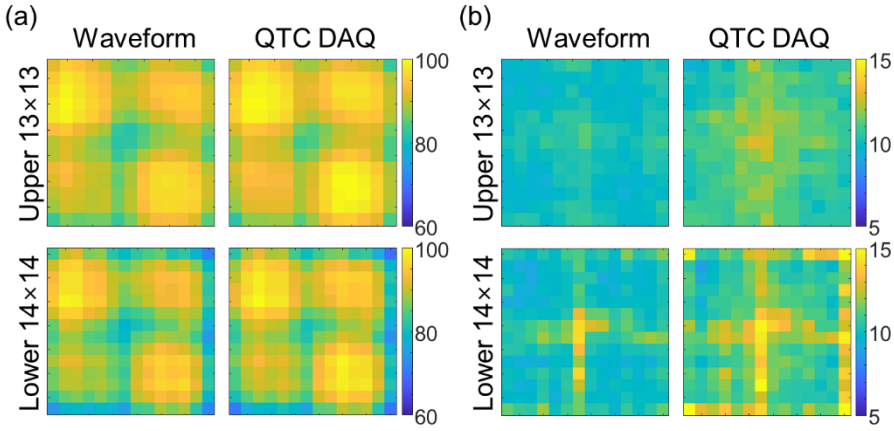

Figure 5-9. Normalized photopeak positions and energy resolutions obtained using the waveform digitizer and the time-based DAQ system. (a) Photopeak positions. (b) Energy resolutions.

5.3.3. Phantom Studies

The hot rods with a diameter of down to 1.6 mm were resolved in the reconstructed image as shown in Figure 5-10. The uniformity was 1.82% as shown in Figure 5-11. The detailed structure of the brain phantom was clearly resolved as shown in Figure 5-12.

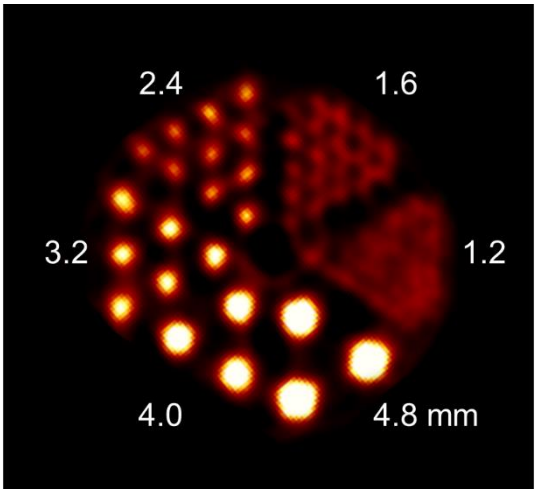

Figure 5-10. Reconstructed hot-rod phantom image.

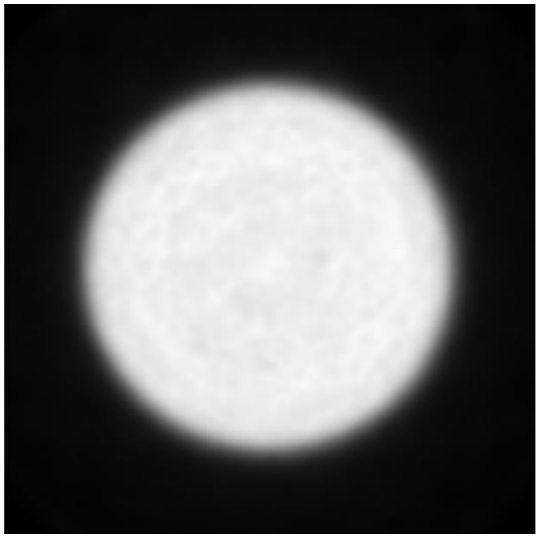

Figure 5-11. Reconstructed uniform phantom image.

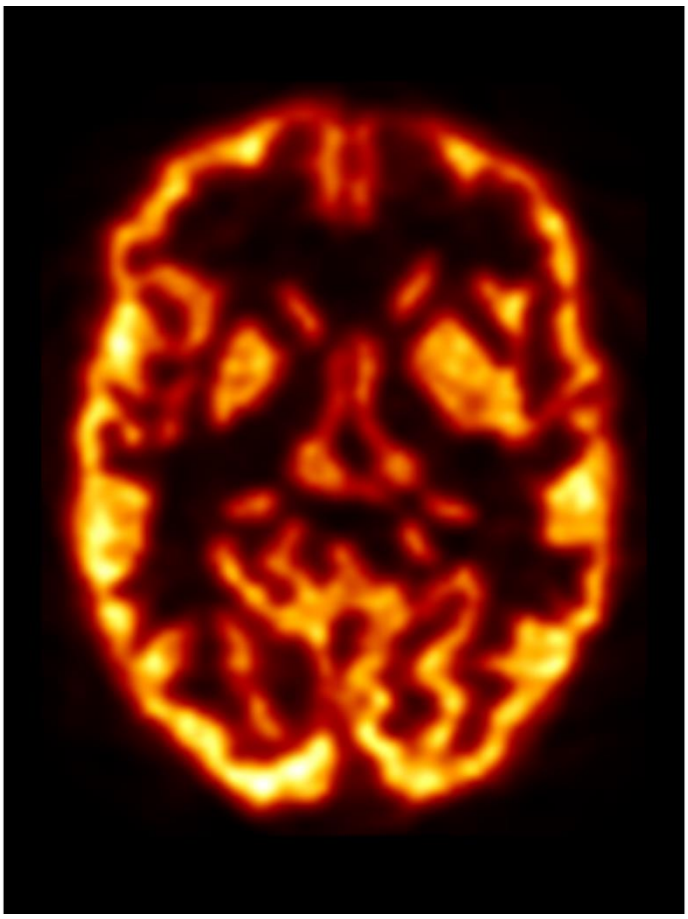

Figure 5-12. Reconstructed 2D Hoffman brain phantom image.

5.4. Discussion

The combination of QTC with SeMI input receiver has the advantages of multichannel signal digitization capability and energy linearity. The non-gated QTC is a simple electronics that consists of the amplifier, a few passive electronics, and a voltage source. In addition, the non-gated QTC requires a common single threshold that the SeMI input receivers provide with zero offset voltage. Thus, the 132 amplifiers and 132 of the 192 available GPIO ports were used to implement 132 energy channel channels. The second advantage is energy linearity. The non-gated QTC is an integrator that converts the input charge into the pulse width linearly regardless of the pulse shape. In addition, the structure of integrator is robust to the noise. The third advantage is a simple data processing. The pulse width of the dual-slope pulse can be easily measured using the MPCNT without complex pulse reconstruction procedure.

The linear charge measurement capability of the QTC enabled to resolve all crystals of the high-resolution staggered DOI PET detectors. Although the spots for edge crystals were blurred in the flood map and the energy resolutions were degraded due to a low charge injection to one of the four QTC channels, this can be mitigated by increasing the input current in the energy channel and/or decreasing the charge division ratios in the charge division circuit.

The comparator-less QTC DAQ systems demonstrated multichannel signal digitization capability by visualizing phantom images successfully. The high-resolution brain PET scanner and the time-based DAQ systems can resolve small rods with a diameter of 1.6 mm and detailed structures of the brain. This would mitigate the partial volume effect. In addition, two-layer DOI information was well-

distinguished in the flood map, and this would increase the uniformity of the spatial resolution. Furthermore, the pipelined data processing, the gigabit transceivers with line rates of 2.5 Gbps, and the online coincidence processing can handle data from the radioactive source with an activity of 2 mCi without a bottleneck.

Chapter 6. Conclusions

The SiPM-based PET scanner is a promising PET scanner with high resolution and high sensitivity. The highly integrated DAQ system is required to draw the best performance of the SiPM-based PET scanners. The step-by-step methods to implement highly integrated DAQ systems using FPGA were proposed in the thesis.

Firstly, we developed a fundamental block of FPGA-TDC with the on-the-fly calibrator. The TDC with a 10-ps resolution and a sub-10-ps precision enabled the TOF measurements that can increase the SNR of the PET scanner. In addition, high-resolution TDC allows obtaining position information using TDOA positioning in the delay grid multiplexing.

The SeMI digitizer that enables almost all FPGA GPIOs as the high-performance voltage comparator is one of the most highly integrated signal digitization methods. The SiPM signals can be directly digitized by FPGA without any front-end electronics. The SeMI digitizer would be used for one-to-one coupled TOF PET scanner because of its fast temporal response.

The comparator-less QTC DAQ where the non-gated QTC combined with the SeMI input receiver enables to collect data from the high-resolution brain PET scanner with light sharing and charge division circuit.

We simplified the DAQ system using FPGA as the high-performance digitizer. The ADC, the TDC, and the discrete voltage comparator that involve in signal digitization were integrated with the FPGA. In addition, the FPGA performed the original functions of data processing, control, and high-speed data transfer. Consequently, we developed the highly integrated DAQ system using the FPGA itself as the high-performance all-in-one DAQ system for SiPM-based PET scanners.

Bibliography

1. Chatziioannou, A.F., et al., *Performance evaluation of microPET: a high-resolution lutetium oxyorthosilicate PET scanner for animal imaging.* Journal of nuclear medicine : official publication, Society of Nuclear Medicine, 1999. 40(7): p. 1164-1175.
2. Cherry, S.R., et al., *MicroPET: a high resolution PET scanner for imaging small animals.* IEEE Transactions on Nuclear Science, 1997. 44(3): p. 1161-1166.
3. Seifert, S., et al., *First characterization of a digital SiPM based time-of-flight PET detector with 1 mm spatial resolution.* Physics in Medicine and Biology, 2013. 58(9): p. 3061-3074.
4. Yamamoto, S., et al., *Development of a Si-PM-based high-resolution PET system for small animals.* Physics in Medicine and Biology, 2010. 55(19): p. 5817-5831.
5. Karp, J.S., et al., *Benefit of time-of-flight in PET: experimental and clinical results.* J Nucl Med, 2008. 49(3): p. 462-70.
6. Surti, S., *Update on time-of-flight PET imaging.* J Nucl Med, 2015. 56(1): p. 98-105.
7. Vandenberghe, S., et al., *Recent developments in time-of-flight PET.* EJNMMI Phys, 2016. 3(1): p. 3.
8. Berg, E., et al., *Development and evaluation of mini-EXPLORER: a long axial field-of-view PET scanner for non-human primate imaging.* J Nucl Med, 2018.
9. Cherry, S.R., et al., *Total-Body PET: Maximizing Sensitivity to Create New Opportunities for Clinical Research and Patient Care.* J Nucl Med, 2018. 59(1): p. 3-12.
10. Cates, J.W. and C.S. Levin, *Advances in coincidence time resolution for PET.* Phys Med Biol, 2016. 61(6): p. 2255-64.
11. Gundacker, S., et al., *State of the art timing in TOF-PET detectors with LuAG, GAGG and L(Y)SO scintillators of various sizes coupled to FBK-SiPMs.* Journal of Instrumentation, 2016. 11(08): p. P08008-P08008.
12. Choong, W.S., et al., *A front-end readout Detector Board for the OpenPET electronics system.* J Instrum, 2015. 10.
13. Fontaine, R., et al., *The Hardware and Signal Processing Architecture of LabPETTM, a Small Animal APD-Based Digital PET Scanner.* IEEE Transactions on Nuclear Science, 2009. 56(1): p. 3-9.
14. Kipnis, I., et al., *A time-over-threshold machine: the readout integrated circuit for the BABAR Silicon Vertex Tracker.* IEEE Transactions on Nuclear Science, 1997. 44(3): p. 289-297.
15. Grant, A.M. and C.S. Levin, *A new dual threshold time-over-threshold circuit for fast timing in PET.* Physics in Medicine and Biology, 2014. 59(13): p. 3421-3430.
16. Njejimana, L., et al., *Design of a Real-Time FPGA-Based Data Acquisition Architecture for the LabPET II: An APD-Based Scanner Dedicated to Small Animal PET Imaging.* IEEE Transactions on Nuclear Science, 2013. 60(5): p. 3633-3638.
17. Shimazoe, K., et al., *Dynamic Time Over Threshold Method.* IEEE Transactions on Nuclear Science, 2012. 59(6): p. 3213-3217.
18. Yonggang, W., et al., *A Linear Time-Over-Threshold Digitizing Scheme and Its 64-channel DAQ Prototype Design on FPGA for a Continuous Crystal PET Detector.* IEEE Transactions on Nuclear Science, 2014. 61(1): p. 99-106.
19. Kim, H., et al., *A Multi-Threshold Sampling Method for TOF PET Signal Processing.* Nucl Instrum Methods Phys Res A, 2009. 602(2): p. 618-621.
20. Xie, Q., et al., *Potentials of Digitally Sampling Scintillation Pulses in Timing Determination in PET.* IEEE Trans Nucl Sci, 2009. 56(5): p. 2607-2613.
21. Parl, C., et al., *Fast Charge to Pulse Width Converter for Monolith PET Detector.* IEEE Transactions on Nuclear Science, 2012. 59(5): p. 1809-1814.

22. Liu, S.B., et al., *The non-gated charge-to-time converter for TOF detector in BES III.* Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, 2010. 621(1-3): p. 513-518.
23. Bieniosek, M.F., P.D. Olcott, and C.S. Levin, *Compact pulse width modulation circuitry for silicon photomultiplier readout.* Phys Med Biol, 2013. 58(15): p. 5049-59.
24. Zhao, Z., et al., *A Novel Read-Out Electronics Design Based on 1-Bit Sigma-Delta Modulation.* IEEE Transactions on Nuclear Science, 2017. 64(2): p. 820-828.
25. Zhao, Z., et al., *An Advanced 100-Channel Readout System for Nuclear Imaging.* IEEE Transactions on Instrumentation and Measurement, 2018: p. 1-11.
26. Wu, J., S. Hansen, and Z. Shi, *ADC and TDC Implemented Using FPGA.* Nuclear Science Symposium Conference Record, 2007. NSS '07. IEEE, 2007: p. 281-286.
27. Son, J.W., et al., *Proof-of-concept prototype time-of-flight PET system based on high-quantum-efficiency multianode PMTs.* Med Phys, 2017. 44(10): p. 5314-5324.
28. Daigneault, M.-A. and J.P. David, *A High-Resolution Time-to-Digital Converter on FPGA Using Dynamic Reconfiguration.* IEEE Transactions on Instrumentation and Measurement, 2011. 60(6): p. 2070-2079.
29. Fishburn, M., et al., *A 19.6 ps, FPGA-Based TDC With Multiple Channels for Open Source Applications.* IEEE Transactions on Nuclear Science, 2013. 60(3): p. 2203-2208.
30. Hong, K.J., et al., *FPGA-based Time-to-Digital Converter for Time-of-Flight PET Detector.* Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC), 2012 IEEE, 2012: p. 2463-2465.
31. Kalisz, J., *Review of methods for time interval measurements with picosecond resolution.* Metrologia, 2004. 41(1): p. 17-32.
32. Shen, Q., et al., *A 1.7 ps Equivalent Bin Size and 4.2 ps RMS FPGA TDC Based on Multichain Measurements Averaging Method.* IEEE Transactions on Nuclear Science, 2015. 62(3): p. 947-954.
33. Szplet, R., et al., *A 2.9 ps equivalent resolution interpolating time counter based on multiple independent coding lines.* Measurement Science and Technology, 2013. 24(3).
34. Szplet, R. and K. Klepacki, *An FPGA-Integrated Time-to-Digital Converter Based on Two-Stage Pulse Shrinking.* IEEE Transactions on Instrumentation and Measurement, 2010. 59(6): p. 1663-1670.
35. Szplet, R., R. Szymanowski, and D. Sondej, *Measurement Uncertainty of Precise Interpolating Time Counters.* IEEE Transactions on Instrumentation and Measurement, 2019: p. 1-9.
36. Torres, J., et al., *Time-to-Digital Converter Based on FPGA With Multiple Channel Capability.* IEEE Transactions on Nuclear Science, 2014. 61(1): p. 107-114.
37. Wang, J., et al., *The 10-ps Multitime Measurements Averaging TDC Implemented in an FPGA.* IEEE Transactions on Nuclear Science, 2011. 58(4): p. 2011-2018.
38. Won, J.Y., et al., *Dual-Phase Tapped-Delay-Line Time-to-Digital Converter With On-the-Fly Calibration Implemented in 40 nm FPGA.* IEEE Trans Biomed Circuits Syst, 2016. 10(1): p. 231-42.
39. Won, J.Y. and J.S. Lee, *Time-to-Digital Converter Using a Tuned-Delay Line Evaluated in 28-, 40-, and 45-nm FPGAs.* IEEE Transactions on Instrumentation and Measurement, 2016. 65(7): p. 1678-1689.
40. Wu, J., *Several Key Issues on Implementing Delay Line Based TDCs Using FPGAs.* IEEE Transactions on Nuclear Science, 2010. 57(3): p. 1543-1548.
41. Zhao, L., et al., *The Design of a 16-Channel 15 ps TDC Implemented in a 65 nm FPGA.* IEEE Transactions on Nuclear Science, 2013. 60(5): p. 3532-3536.
42. Siegel, S., et al., *Simple charge division readouts for imaging scintillator arrays using a multi-channel PMT.* IEEE Transactions on Nuclear Science, 1996. 43(3): p. 1634-1641.

43. Goertzen, A.L., et al., *Design and Performance of a Resistor Multiplexing Readout Circuit for a SiPM Detector.* IEEE Transactions on Nuclear Science, 2013. 60(3): p. 1541-1549.
44. Olcott, P.D., G. Glover, and C.S. Levin, *Cross-Strip Multiplexed Electro-Optical Coupled Scintillation Detector for Integrated PET/MRI.* IEEE Transactions on Nuclear Science, 2013. 60(5): p. 3198-3204.
45. Downie, E., X. Yang, and H. Peng, *Investigation of analog charge multiplexing schemes for SiPM based PET block detectors.* Physics in Medicine and Biology, 2013. 58(11): p. 3943-3964.
46. Ritt, S., R. Dinapoli, and U. Hartmann, *Application of the DRS chip for fast waveform digitizing.* Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, 2010. 623(1): p. 486-488.
47. Kim, H., et al., *A Silicon Photo-multiplier Signal Readout Using Strip-line and Waveform Sampling for Positron Emission Tomography.* Nucl Instrum Methods Phys Res A, 2016. 830: p. 119-129.
48. Won, J.Y., G.B. Ko, and J.S. Lee, *Delay grid multiplexing: simple time-based multiplexing and readout method for silicon photomultipliers.* Phys Med Biol, 2016. 61(19): p. 7113-7135.
49. Kwon, S.I. and J.S. Lee, *Signal encoding method for a time-of-flight PET detector using a silicon photomultiplier array.* Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, 2014. 761: p. 39-45.
50. Ito, M., J.P. Lee, and J.S. Lee, *Timing Performance Study of New Fast PMTs With LYSO for Time-of-Flight PET.* IEEE Transactions on Nuclear Science, 2013. 60(1): p. 30-37.
51. Ko, G.B., et al., *Development of FPGA-based coincidence units with veto function.* Biomedical Engineering Letters, 2011. 1(1): p. 27-31.
52. Yeom, J.Y., et al., *Readout Electronics and Data Acquisition of a Positron Emission Tomography Time-of-Flight Detector Module With Waveform Digitizer.* IEEE Transactions on Nuclear Science, 2013. 60(5): p. 3735-3741.
53. Lee, M.S., S.K. Kang, and J.S. Lee, *Novel inter-crystal scattering event identification method for PET detectors.* Phys Med Biol, 2018.
54. Xi, D., et al., *FPGA-Only MVT Digitizer for TOF PET.* IEEE Transactions on Nuclear Science, 2013. 60(5): p. 3253-3261.
55. Pałka, M., et al., *Multichannel FPGA based MVT system for high precision time (20 ps RMS) and charge measurement.* Journal of Instrumentation, 2017. 12(08): p. P08001-P08001.
56. Won, J.Y. and J.S. Lee, *Highly Integrated FPGA-Only Signal Digitization Method Using Single-Ended Memory Interface Input Receivers for Time-of-Flight PET Detectors.* IEEE Trans Biomed Circuits Syst, 2018. 12(6): p. 1401-1409.
57. Becker, R., et al., *The SAFIR project: an innovative high rate preclinical PET/MR detector towards dynamic multimodal imaging.* EJNMMI Phys, 2015. 2(Suppl 1): p. A15.
58. Omidvari, N., et al., *PET performance evaluation of MADPET4: a small animal PET insert for a 7 T MRI scanner.* Phys Med Biol, 2017. 62(22): p. 8671-8692.
59. Surti, S. and J.S. Karp, *Impact of event positioning algorithm on performance of a whole-body PET scanner using one-to-one coupled detectors.* Phys Med Biol, 2018. 63(5): p. 055008.
60. Ko, G.B., et al., *Simultaneous Multiparametric PET/MRI with Silicon Photomultiplier PET and Ultra-High-Field MRI for Small-Animal Imaging.* J Nucl Med, 2016. 57(8): p. 1309-15.
61. Vandenberghe, S. and P.K. Marsden, *PET-MRI: a review of challenges and solutions in the development of integrated multimodality imaging.* Phys Med Biol, 2015. 60(4):

p. R115-54.
62. Yoon, H.S., et al., *Initial results of simultaneous PET/MRI experiments with an MRI-compatible silicon photomultiplier PET scanner.* J Nucl Med, 2012. 53(4): p. 608-14.
63. Drzezga, A., et al., *Potential Clinical Applications of PET/MR Imaging in Neurodegenerative Diseases.* J Nucl Med, 2014. 55(Supplement 2): p. 47S-55S.
64. Gerhard, A., et al., *In vivo imaging of microglial activation with [11C](R)-PK11195 PET in idiopathic Parkinson's disease.* Neurobiol Dis, 2006. 21(2): p. 404-12.
65. Silverman, D.H.S., *Brain ^{18}F-FDG PET in the Diagnosis of Neurodegenerative Dementias: Comparison with Perfusion SPECT and with Clinical Evaluations Lacking Nuclear Imaging.* J Nucl Med, 2004. 45(4): p. 594-607.
66. Zaidi, H. and M.-L. Montandon, *The New Challenges of Brain PET Imaging Technology.* Current Medical Imaging Reviews, 2006. 2(1): p. 3-13.
67. Mehranian, A. and H. Zaidi, *Impact of time-of-flight PET on quantification errors in MR imaging-based attenuation correction.* J Nucl Med, 2015. 56(4): p. 635-41.
68. Shidahara, M., et al., *Functional and structural synergy for resolution recovery and partial volume correction in brain PET.* Neuroimage, 2009. 44(2): p. 340-8.
69. Ito, M., S.J. Hong, and J.S. Lee, *Positron emission tomography (PET) detectors with depth-of- interaction (DOI) capability.* Biomedical Engineering Letters, 2011. 1(2): p. 70-81.
70. Ito, M., et al., *A Four-Layer DOI Detector With a Relative Offset for Use in an Animal PET System.* IEEE Transactions on Nuclear Science, 2010. 57(3): p. 976-981.
71. Stortz, G., et al., *Performance of a PET Insert for High-Resolution Small-Animal PET/MRI at 7 Tesla.* J Nucl Med, 2018. 59(3): p. 536-542.
72. Thompson, C.J., et al., *Evaluation of High Density Pixellated Crystal Blocks With SiPM Readout as Candidates for PET/MR Detectors in a Small Animal PET Insert.* IEEE Transactions on Nuclear Science, 2012. 59(5): p. 1791-1797.
73. Park, H., G.B. Ko, and J.S. Lee, *Hybrid charge division multiplexing method for silicon photomultiplier based PET detectors.* Phys Med Biol, 2017. 62(11): p. 4390-4405.
74. Son, J.-W., J.Y. Won, and J.S. Lee. *Evaluation of a FPGA-based Real-Time Coincidence System for High Count Rate PET Scanners*. in *2017 IEEE Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC)*. 2017.

Abstract in Korean (국문 초록)

양전자방출단층촬영 (Positron Emission Tomography; PET) 장치는 암과 신경퇴행성 질환을 영상화하는 데 널리 쓰이는 기능 영상장치이다. 최근 PET 스캐너 연구는 공간 분해능과 장비 민감도를 높여 병변의 진단을 쉽게 하면서 환자의 방사선 피폭을 줄이는 방법에 초점을 맞추고 있다.

실리콘 관증배기 (silicon photomultiplier; SiPM)은 크기가 작고 반응속도가 빠르기 때문에 고성능 PET 스캐너에 적합한 광검출소자이다. 하지만 SiPM 기반 PET 스캐너는 개별 SiPM의 크기가 작기 때문에 수많은 데이터 수집 채널이 필요하다. 예를 들어, 전신 PET 스캐너를 SiPM으로 구성할 경우 40,000개 이상의 SiPM 소자가 필요하다. 따라서, SiPM의 성능을 유지하면서 다채널 신호 디지털화가 가능한 고집적 데이터 수집장치 (data acquisition; DAQ)가 고성능 SiPM PET 스캐너 개발에 필요하다.

시간 기반 신호 디지털 방법은 단순한 회로와 빠른 반응속도 덕분에 고집적 DAQ 시스템을 구현하는 유망한 방법이다. 본 학위논문에서는 프로그램 가능 게이트 배열 (field-programmable gate array; FPGA)을 이용하여 고집적 DAQ 시스템을 개발하는 연구내용을 다룬다.

첫째로, 10 ps 의 분해능을 갖는 FPGA 기반 시간-디지털 변환기 (time-to-digital converter; TDC)를 개발하였다. FPGA는 TDC 구현을 위한 집적소자가 아니므로 FPGA에 구현된 TDC는 일반적으로 비선형성 문제를 가진다. 이를 해결하기 위해 비선형성 문제를 야기하는 FPGA의

클락 신호 분배 구조를 고려하여 이중 위상 샘플링 방법을 제안하였다. 또한, FPGA TDC 고유의 불균일한 분해능을 측정하고 보상하기 위하여 실시간 보정기술을 개발하였다.

둘째로, GPS 원리를 사용한 시간 기반 신호 부호화 (multiplexing) 및 수집 방법을 개발하였다. 부호화 회로는 SiPM을 네 개의 시간 수집 채널로 연결한 도선으로 구성되고 위치정보는 각 SiPM으로부터 네 개의 시간 수집 채널까지의 고유한 도파시간 차이를 계산해서 수집할 수 있다. 또한, 기존 전하 분배 부호화 회로와 달리 신호가 왜곡되지 않기 때문에 문턱 전압 방법 (time-over-threshold; ToT) 방식으로 에너지를 수집하는 것이 가능하였다.

셋째로, FPGA만으로 아날로그 신호를 디지털화 하는 새로운 방법을 개발하였다. FPGA의 프로그램 가능 입출력포트를 stub-series terminated logic (SSTL) 수신기로 프로그램하면, 각각의 FPGA 입출력포트가 빠른 시간 반응성을 가진 고성능 전압비교기로 동작한다. 비정시간 (time-of-flight; TOF) 측정 가능 PET 검출기의 신호를 전단회로 없이 FPGA만으로 디지털화하여 FPGA를 고성능 DAQ 장치로 사용할 수 있음을 입증하였다.

마지막으로, 공간분해능이 뛰어난 뇌전용 스캐너로부터 데이터를 수집하기 위해 전압비교기를 사용하지 않는 시간 기반 DAQ 장치를 개발하였다. 에너지 측정 채널은 시간-전하 변환기 (charge-to-time converter; QTC)와 FPGA의 SSTL 수신기로 구성하였다. 시각 측정 채널은 FPGA 기반 TDC로 구성하였다. 개발한 뇌전용 스캐너와 고집적 시간

기반 DAQ 장치로 획득한 뇌모양 팬텀의 자세한 구조들은 잘 구분되었다.

주요어 : 데이터 수집장치(DAQ), 현장프로그램가능 게이트 배열 (FPGA), 양전자방출단층촬영(PET), 실리콘 광증배기(SiPM), 비정시간(TOF), 시간-디지털 변환기(TDC)

학번 : 2013-21782