Ph.D. DISSERTATION

Nano-structured Resistive Random Access Memory for Neuromorphic System

신경 모방 시스템 구현을 위한 나노 구조의 저항 변화 메모리

BY

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February 2020

DEPARTMENT OF ELECTRICAL AND
COMPUTER ENGINEERING
COLLEGE OF ENGINEERING
SEOUL NATIONAL UNIVERSITY

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지도교수 박 병 국

이 논문을 공학박사 학위논문으로 제출함

2020 년 2 월

서울대학교 대학원

전기컴퓨터공학부

김 민 휘

김민휘의 공학박사 학위논문을 인준함

2020 년 2 월

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Abstract

Recently, the field of mimicking and utilizing the operation of the human brain neural network is gradually expanding due to the rapid development of the machine learning algorithms based on big data. However, the von Neumann architecture, which is widely used today, has inherent incompatibility as hardware that realizes very parallel structure and low energy consumption of brain neural network. Therefore, in order to artificially realize various functions such as learning, memory, reasoning, and judgment, a fundamental change at the hardware level is ultimately required. Meanwhile, silicon-based semiconductor device and integrated circuit fabrication technology, which has remarkably developed in recent decades, is considered as the most suitable technology to meet the demands of this change, and discussion is being actively conducted in academic and industrial fields.

In this paper, silicon nitride-based resistive switching memory was

fabricated, and the electrical characteristics of the device were verified and its application was studied.

First, at the individual device level, the resistance change phenomenon of the two terminal memory devices through voltage application was confirmed and various electrical characteristics were confirmed. The effects of the additional formation of nanometer thin silicon oxide film on the operating characteristics of the resistive memory device was investigated. In addition, it was confirmed that the overshoot current flowing into the device can be suppressed, thereby improving the operation uniformity of the device. I also proposed and validated a circuit model of a resistive switching memory that can be used in circuit-level simulation regardless of material and structure.

At the array level, resistive switching memory having an area of tens of nanometers was fabricated and its electrical properties were verified. In this process, the anisotropic wet etching process was applied at room temperature to form the wedge-structured silicon bottom electrodes, and it was confirmed that the operating voltage and energy consumption decrease in the switching

operation as the device area decreases.

By using multi-level resistive switching memory as an artificial synapse and utilizing the vector-matrix multiplication function of the cross-point array structure, I confirmed that the structure and problem solving ability of the artificial neural network obtained by software machine learning can be implemented with energy efficient hardware neural network.

Keywords: Resistive switching random access memory, wedge-structured RRAM, cross-point array, synaptic device, neuromorphic system.

Student number: 2013-20758

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Chapter 1
Introduction

1.1 Resistive Switching Random Access Memory (RRAM)

Recently, resistive switching random access memory (RRAM) has been widely investigated as a leading candidate for next generation nonvolatile memory applications [1]-[5] and as a synaptic device in neuromorphic system [6]-[13] due to the scaling limit of the present NAND Flash memory technology and RRAM's advantageous features such as simple structure, low cost, high density [14], fast operation [15]-[17], and CMOS compatibility [18], [19].

In order to implement a high-density RRAM, several array structures have been proposed. Fig. 1.1 shows schematic of representative 3D RRAM arrays. However, compared to the recent successful commercialization of high-density 3D NAND Flash memory, 3D RRAM has yet to show a significant competitive advantage.

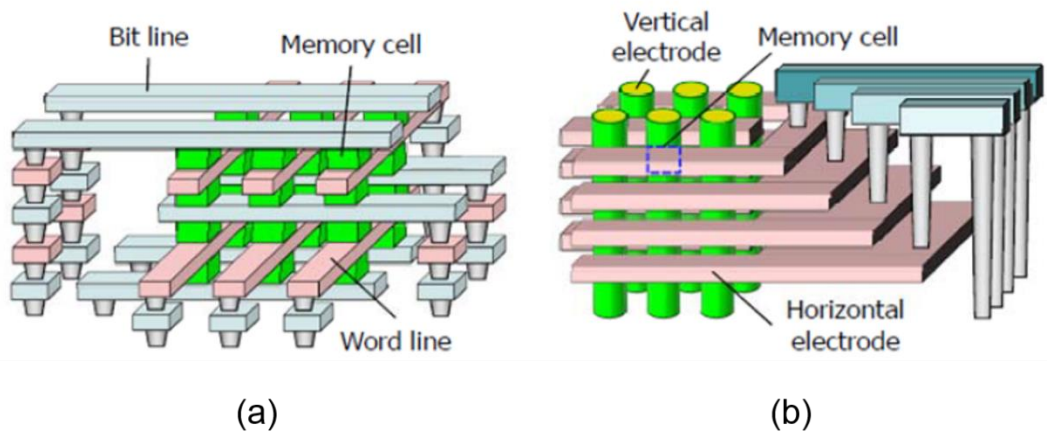


Fig. 1.1. Schematic diagrams of (a) 3D stacked cross-point and (b) vertical RRAM array structure [20].

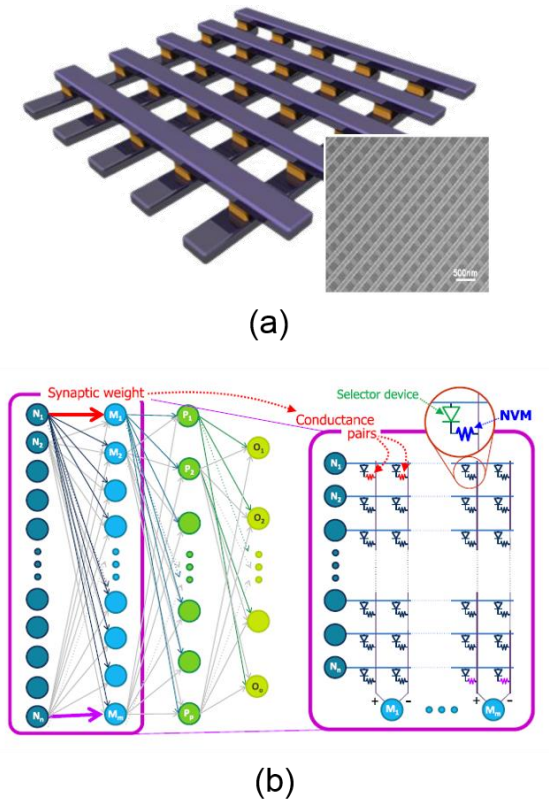


Fig. 1.2. (a) RRAM cross-point array [21] and (b) its application to hardware implementation of artificial neural network [22].

For the realization of the neuro-inspired non-von Neumann computing architecture, cross-point array structure with adjustable nonvolatile memory cells are expected to play a key role. This is because, ideally, the product of

the input vector and the conductivity matrix, which is one of the most important part of machine learning algorithms, can be carried out naturally (energy and time efficiently) if the synaptic elements that can control the electrical conductivity are located between two crossing lines (Fig. 1.2).

Many researches have been carried out on RRAM as one of candidates for such a synaptic element. Fig. 1.3 shows the types and ratios of research topics and applications for RRAM. It can be seen that the number of studies applying RRAM to neuromorphic systems increases, and the application to high-density memory field decreases every year. In addition, the type of synaptic devices used in the hardware implementation of the artificial neural network shows that RRAM occupies the highest ratio among Flash-based devices and phase change memory (PCM) as shown in Fig. 1.4. However, there still remain reliability issues such as endurance degradation and uncontrolled variations of resistance states and operation voltages [23], [24] (Fig. 1.5).

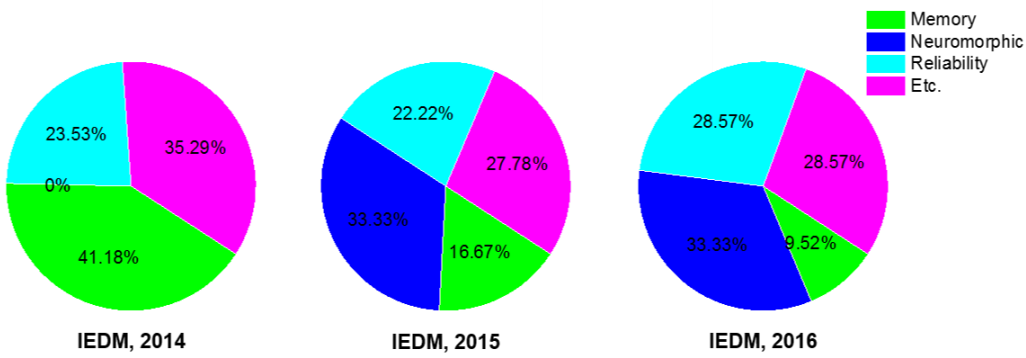


Fig. 1.3. Application or research topics of RRAM reported at International Electron Devices Meeting (IEDM) 2014, 2015 and 2016, respectively.

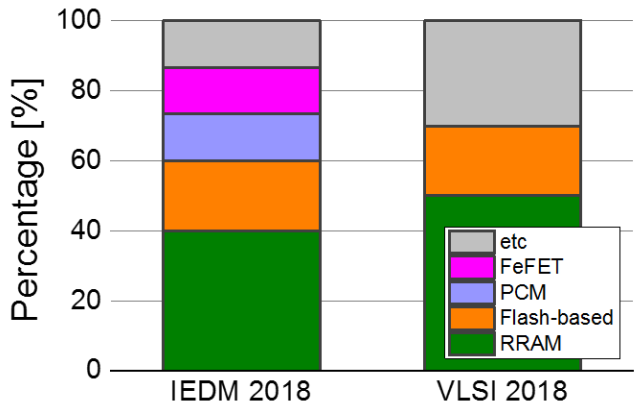
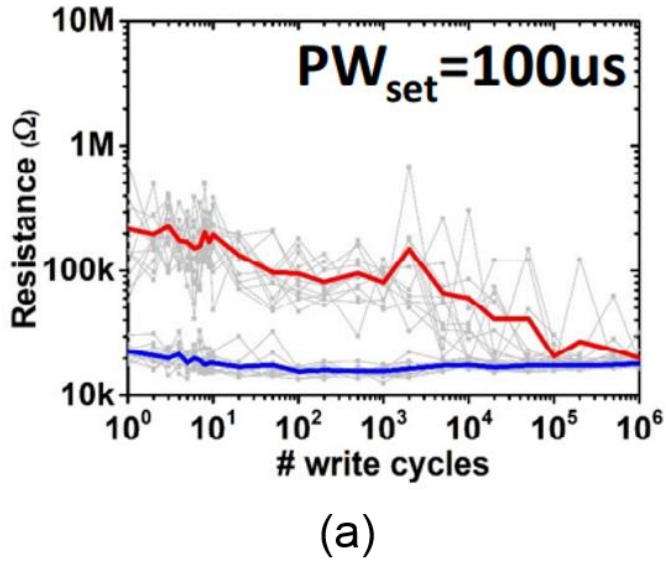
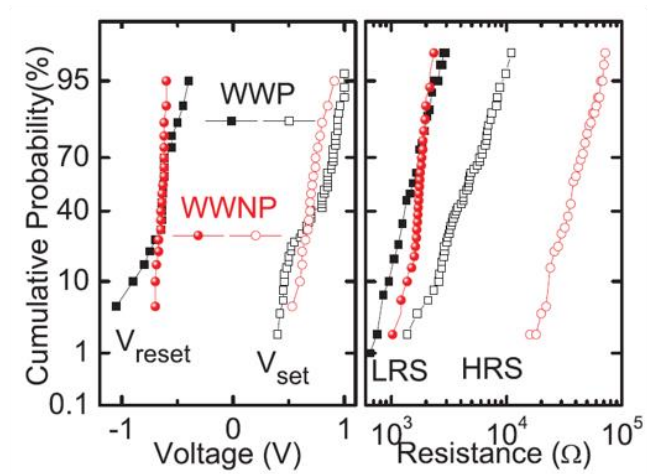


Fig. 1.4. Types of synaptic elements used to implement hardware neural networks presented at major semiconductor conference (IEDM, VLSI 2018).



(a)



(b)

Fig. 1.5. Representative reliability issue of RRAM. (a) Degradation of switching cycle characteristics (endurance). (b) Variability of operation voltage and resistance state [23], [24].

1.2 Silicon Nitride-based RRAM

Dielectric and trap characteristics of silicon nitride (Si_3N_4) material have been extensively studied since it has been one of the most widely used material in conventional semiconductor process particularly as masking layer and charge trapping layer of 3D NAND Flash memory structure [25]. Meanwhile, silicon nitride as a switching layer of the RRAM cell has been studied by several groups due to its advantageous characteristics such as CMOS compatibility [26]. These researches have been mainly performed focusing on conduction and switching mechanisms mostly being limited in material level or analysis of DC characteristics [26]-[35]. In one of our previous works, the gradual resistance switching phenomenon on DC characteristics and multi-level data retention characteristics of Si_3N_4-based CMOS compatible RRAM have been reported [27], there have not been controllability of resistance states by each pulse and appropriate guidelines for

the pulse operation of RRAM. Also, there have been several works demonstrating gradual resistance switching of MIM structured RRAM in pulse operation, those results have not shown the dependence of pulse conditions on resistance change thoroughly and the gradual resistive characteristics have obtained by using relatively long pulses (10 μs ~ 2 ms) [6, 36].

Chapter 2
Electrical Characteristics of Silicon Nitride-based RRAM

2.1. Basic Electrical Characteristics

We have thoroughly investigated resistive switching characteristics of CMOS compatible SiN_x-based resistive memory cell in both DC and pulse operation which is one of the most important feature for synaptic device modifying its connecting weight continuously in neuromorphic system. In our experiments, resistive memory cells with $Ni/Si_3N_4/SiO_2/p^+$-Si layers were fabricated. The schematic of device structure is shown in Fig. 2.1. p^+-Si bottom electrode (BE) was formed with an ion implantation of BF_2^+. Next,

SiO_2 as the tunnel barrier (for reducing operating current and improving non-linearity) and Si_3N_4 as the actual resistive switching layer were deposited by medium-temperature oxidation (MTO) and plasma-enhanced chemical vapor deposition (PECVD), in sequence. Thickness of the tunnel barrier (SiO_2) and the switching layer (Si_3N_4) was 2.5 nm and 5 nm, respectively. Finally, Ni top electrode (TE) was deposited by a thermal evaporator, and then TE was patterned by a shadow mask containing circles with 100-μm diameter.

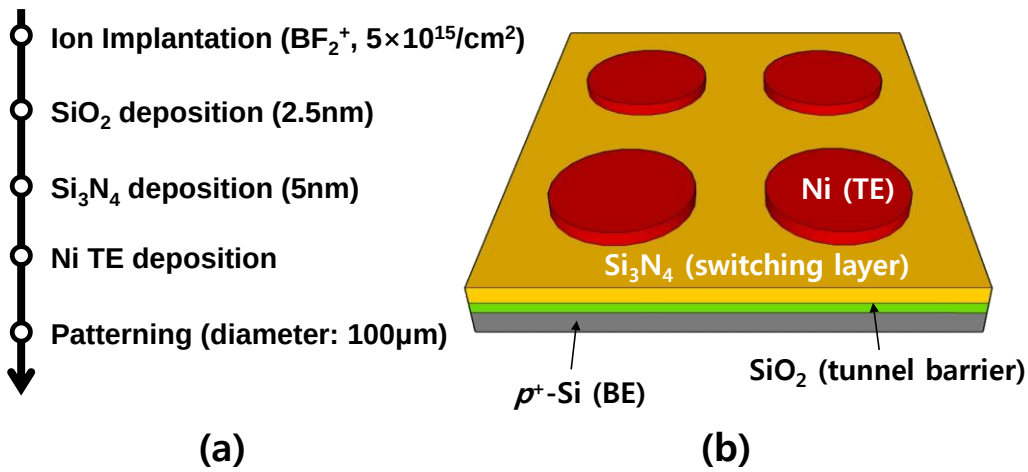


Fig. 2.1. (a) Process flow of the fabricated resistive memory cell. (b) Schematic of the fabricated Ni/Si_3N_4/SiO_2/p^+-Si structured cell.

DC and pulse switching characteristics of the fabricated resistive memory cells were measured by using Keithley 4200-SCS SPA and 4225-PMU ultra-fast *I-V* module. As shown in Fig. 2.2, voltage was swept from 0 V to 6 V under the compliance current (I_C) of 100 μA for set operations and from 0 V to −5 V without the current limit for reset operations. In pulse operation, all the positive set and negative reset pulses were applied after initial forming operation. To read the resistance states of the memory cells, voltage was swept from 0 V to 1 V. To check gradual switching phenomenon, identical positive (V_A = 9 V, t_W = 100 ns, t_R = t_F = 500 ns) and negative pulses (V_A = −5 V, t_W = 100 ns, t_R = t_F = 500 ns) were applied between TE and BE repeatedly. After each pulse, DC sweep from 0 V to 1 V was carried out to measure resistance states. To analyze the effect of the pulse condition such as pulse width (t_W), rise time (t_R), fall time (t_F) and amplitude (V_A), parameters have been changed (Fig. 2.3). For all applied pulses, transient response (voltage-time, current-time waveforms) was measured to analyze the resistive switching phenomenon.

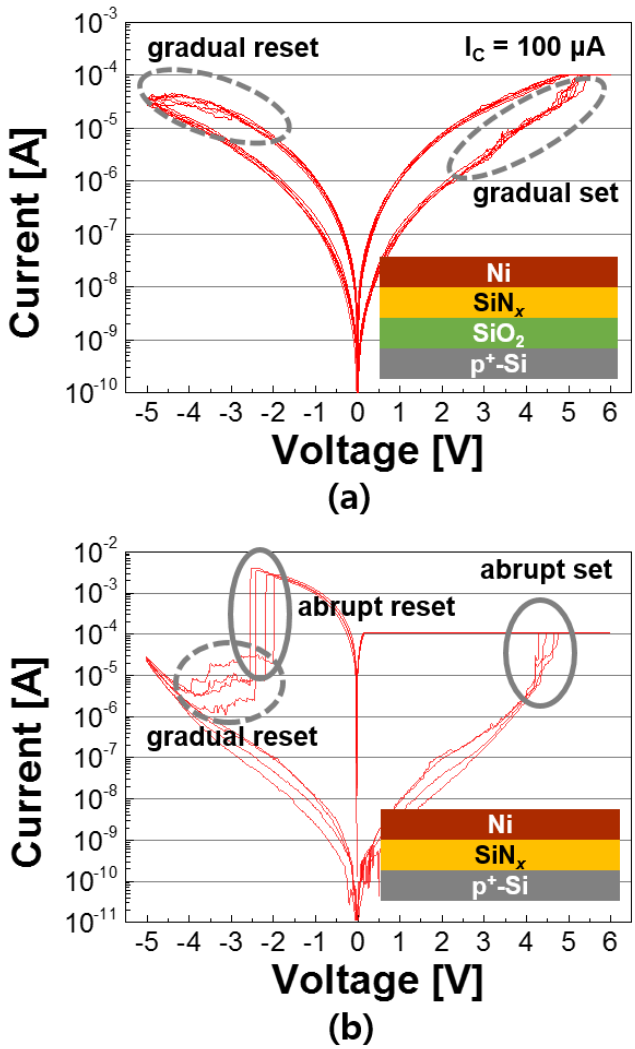


Fig. 2.2. Typical DC characteristics (a) of Ni/Si_3N_4 (5 nm)/SiO_2 (2.5 nm)/p^+-Si structured cell showing both gradual set (from LRS to HRS) and gradual reset (from HRS to LRS) operation and (b) of Ni/Si_3N_4 (5 nm)/p^+-Si structured cell showing abrupt set and reset operation.

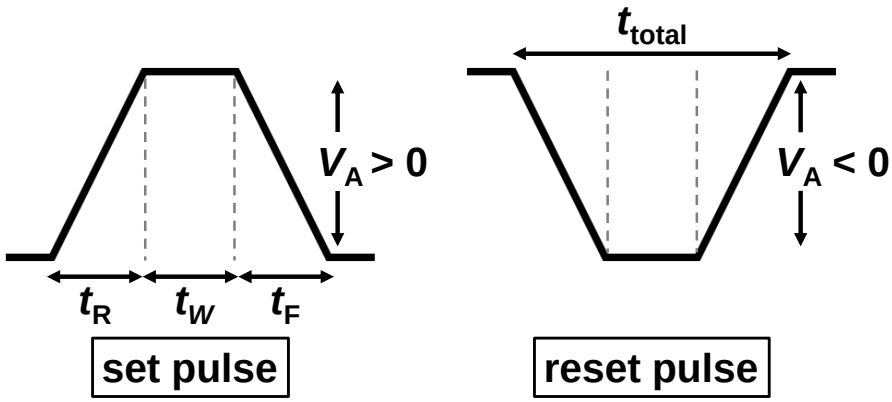


Fig. 2.3. Definition of pulse amplitude (V_A), width (t_W), rise (t_R), fall (t_F) time and total pulse duration (t_{total}).

For each device, 100 cycles of switching operation were performed by voltage sweep from 0 V to 6 V (set) and 0 V to −5 V (reset) for analyzing DC characteristics. Fig. 2.1(a), (b) shows the representative DC curves of $Ni/Si_3N_4/SiO_2/p^+$-Si and $Ni/Si_3N_4/p^+$-Si, respectively. Compared to the characteristics of $Ni/Si_3N_4/p^+$-Si structured cell which was fabricated without SiO_2 deposition step, those of $Ni/Si_3N_4/SiO_2/p^+$-Si structured cell show larger operation voltages, smaller on/off ratio (R_{HRS}/R_{LRS}) and especially gradual resistance switching phenomenon due to inserted SiO_2 layer.

Gradual reset phenomenon of $Ni/Si_3N_4/SiO_2/p^+$-Si structured cell appears to be related with significantly decreased reset current (from over 1 mA to below 0.1 mA). As a supporting evidence, we can point the additional gradual reset phenomenon found in cells without SiO_2 layer after abrupt decrease of current (Fig. 2.2(b)). In addition, even in cells with SiO_2 layer, abrupt reset operation has been occasionally found (usually in case of the leaky LRS state after strong set operation leading to large reset current).

Gradual set operation can also be considered as an effect of the SiO_2 layer. In set operation, the resistance of the Si_3N_4 layer would decrease. Then, a large portion of the cell bias voltage would be applied to the SiO_2 layer, since the resistance value of the SiO_2 layer would not change much while that of Si_3N_4 layer decreases significantly. This procedure leads to self-limiting effect, preventing uncontrolled dielectric breakdown and providing gradual resistance change phenomenon.

2.2. Gradual Switching Operation by Voltage Pulse

2.2.1. Resistance Change by Identical Pulse

To investigate the gradual resistance change by pulse, positive (V_A = 9 V, t_W = 100 ns, t_R = t_F = 500 ns) and negative (V_A = −5 V, t_W = 100 ns, t_R = t_F = 500 ns) pulses were applied consecutively between two electrodes (TE and BE) of Ni/Si_3N_4/SiO_2/p^+-Si structured cell. Fig. 2.4(a) shows that the resistance states can be reliably controlled by applying positive (set) and negative (reset) pulses. Because the resistance state changes linearly in case of set and saturates in case of reset, the on/off ratio (R_{HRS}/R_{LRS}) stays below 10 (R_{HRS}/R_{LRS} = 7.6 for set operation, 2.8 for reset operation). Therefore, other pulse scheme such as incremental pulse width or pulse amplitude needs to be adopted for improved on/off ratio over 10. As the pulse width (t_W) and pulse amplitude (V_A) increase in set and reset operation, respectively, the resistance state changes more rapidly than the previous case (Fig. 2.4(b)), resulting in higher on/off ratio (R_{HRS}/R_{LRS} = 33.6 for set operation, 15.7 for reset

operation). Pulse condition needs to be modified for rapid resistance change and improved on/off ratio. As mentioned in DC operation, the reason for gradual resistance change by repeated pulses is due to the voltage dividing effect which gives more and more portion of applied voltage to the inserted SiO_2 layer in the process of resistive switching. In the case of consecutive negative (reset) pulses, the amount of change decreases because of the increased resistance state of the Si_3N_4 layer leading to decrease of reset current by each reset operation.

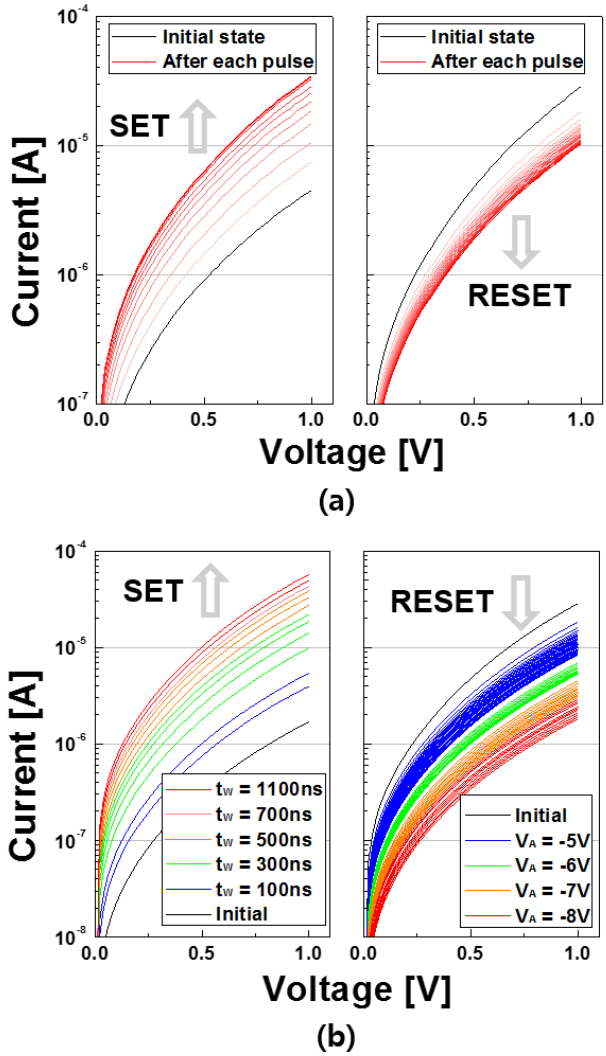


Fig. 2.4. (a) I-V curves of Ni/Si_3N_4/SiO_2/p^+-Si structured cell by consecutive set (V_A = 9 V, t_W = 100 ns, fixed condition) and reset (V_A = −5 V, t_W = 100 ns, fixed condition) pulses and (b) after incremental set (V_A = 9 V, t_W = 100 ~ 1100 ns) and reset (V_A = −5 V ~ −8 V, t_W = 100 ns) pulses.

2.2.2. Effect of Pulse Width

To confirm the effect of pulse width (t_W) on resistance change in set operation, positive pulses with width from 100 ns to 1300 ns (V_A = 9 V, t_R = t_F = 500 ns) were applied to Ni/Si_3N_4/SiO_2/p^+-Si structured cell. Fig. 2.5 shows the change of read current (@ 1 V) after each pulse with different width (t_W = 100 ns ~ 1300 ns). Read current shows clear dependency which tends to increase more rapidly by the pulse with a wider peak. As a result, the resistive memory cell needs fewer number of pulses to achieve a certain LRS from HRS.

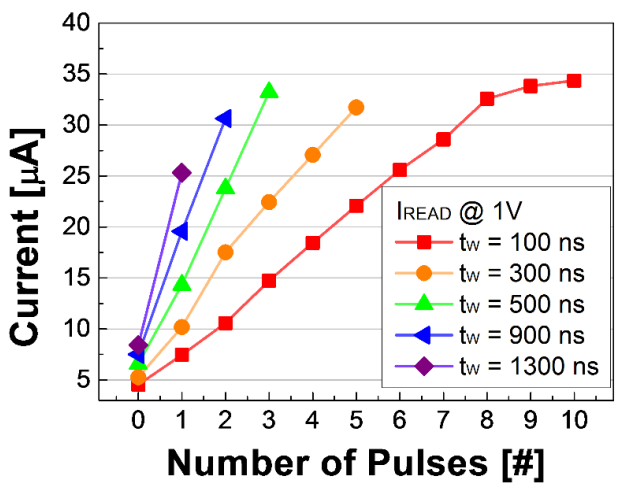


Fig. 2.5. Pulse width (t_W) dependent gradual resistance change of Ni/Si_3N_4/SiO_2/p^+-Si structured cell.

2.2.3. Effect of Pulse Rise and Fall Time

In addition to the pulse width, rise and fall time influence the change rate of resistance state (Fig. 2.6). To the HRS cell, the pulses with the same amplitude (V_A = 9 V or 10 V) and the same width (t_W = 100 ns) are applied with different rise (t_R) and fall time (t_F). In the cases of V_A = 9 V and 10 V, there was a clear tendency that read current (@ 1 V) increases more sharply by each pulse as rise/fall time increases. The total duration of a pulse can be defined as the sum of the pulse rise time, width and fall time ($t_{total} = t_R + t_W + t_F$). As shown in Fig. 2.7, when the total pulse duration (t_{total}) is the same as 1500 ns (Fig. 2.7(a)) or 1900 ns (Fig. 2.7(b)), square-like pulse (black line) changes resistance state more rapidly than triangle-like pulse (red line). From all these results (Fig. 2.5-2.7), it can be concluded that the applied pulse area affects the change of resistance state critically. To check another factor, pulse amplitude (V_A), we compared the case of V_A = 9 V and 10 V.

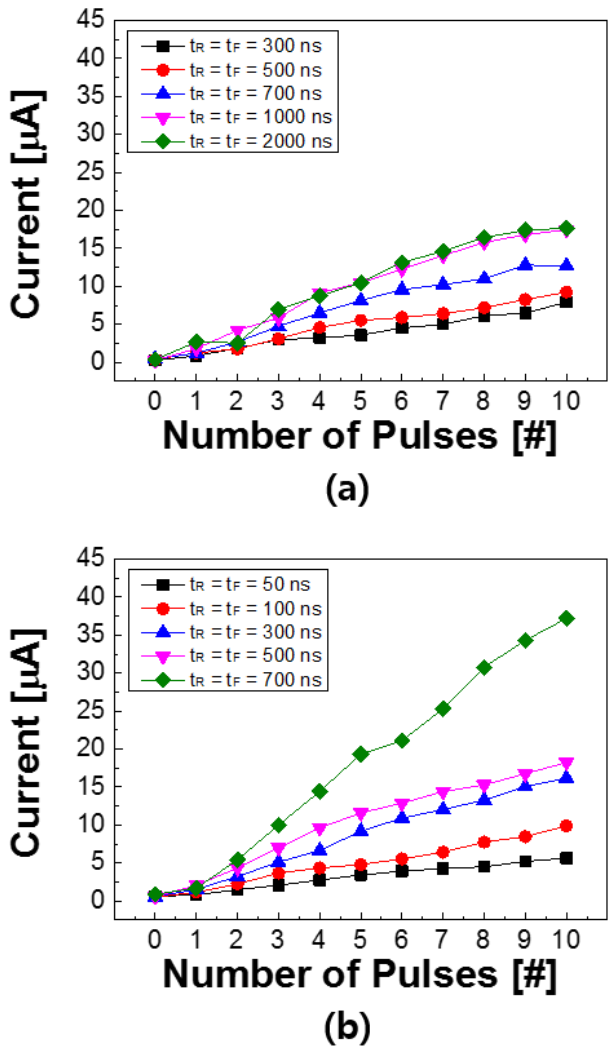


Fig. 2.6. Effect of pulse rise (t_R) and fall time (t_F) on resistance change of $Ni/Si_3N_4/SiO_2/p^+$-Si cell. Compared to (a), (b) shows a more sharp increase of current in the same rise and fall time. Pulse condition: (a) V_A = 9 V, t_W = 100 ns, t_R = t_F = 300~2000 ns, (b) V_A = 10 V, t_W = 100 ns, t_R = t_F = 50~700 ns.

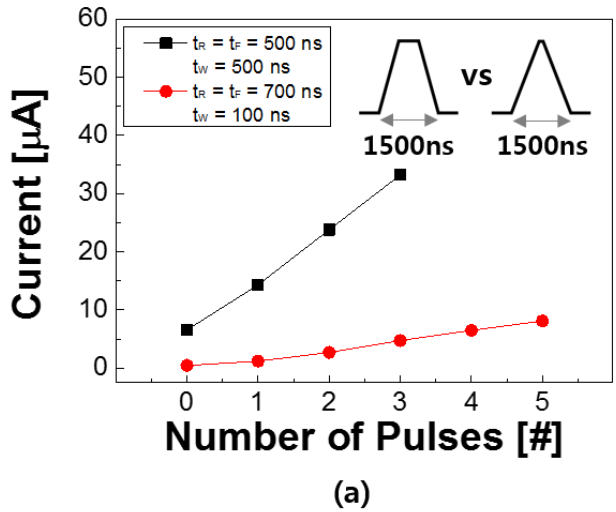


Fig. 2.7. Comparison the effect of pulse width (t_W) and rise (t_R)/fall time (t_F). When total time of the applied pulse is same, the square-like pulse (black) change more sharply than the triangle-like pulse (red). The results directly mean that the pulse area applied to DUT influence the resistance change.

2.2.4. Effect of Pulse Amplitude

The effect of pulse amplitude (V_A) on the resistance change can be clearly seen by comparing Fig. 2.8(b) and Fig. 2.8(c) with Fig. 2.9(c) and Fig. 2.9(d). For the same rise and fall time (t_R = t_F = 300 ns), Fig. 2.9(c) (V_A = 10 V) shows sharper increase of current compared with Fig. 2.8(b) (V_A = 9 V). Likewise, for the same rise and fall time (t_R = t_F = 700 ns), Fig. 2.9(d) (V_A = 10 V) shows sharper increase compared with Fig. 2.8(c) (V_A = 9 V). Furthermore, it can be found that when the larger pulses (V_A = 10 V) were applied, resistive switching cell responded to shorter pulses (t_R = t_F = 50 ns) while the smaller pulses (V_A = 9 V) could change resistance state with relatively long pulses (t_R = t_F = 300 ns). Fig. 2.8(a), (b) and 2.9(a), (b) elucidate this point clearly.

Meanwhile, it should be noted that the pulses which have amplitude below a certain threshold are not able to change the state of resistive switching cells as can be seen in DC characteristics (Fig. 2.2). In other words, a pulse

with a small amplitude (ex. V_A = 1 V) is hard to change resistance state even though pulse width is long enough (ex. t_W > 1 sec). To examine the threshold for resistive switching of the Ni/Si_3N_4/SiO_2/p^+-Si structured cell, pulses with V_A = 5 V, 5.5 V, 6 V (t_W = 3 μs, t_R = t_F = 500 ns) were applied several times. As can be seen in Fig. 9, the resistive switching cell does not respond to pulses with V_A = 5 V even though the pulse width is 3 μs while responding to the pulses with V_A = 5.5 V, 6 V. Moreover, the transient characteristics show stronger responses as the amplitude (V_A) increases from 5 V to 6 V. The result of DC sweep carried out between each pulse is shown in Fig. 2.11. Similar to the transient responses, there is larger difference of resistance state for the larger amplitude.

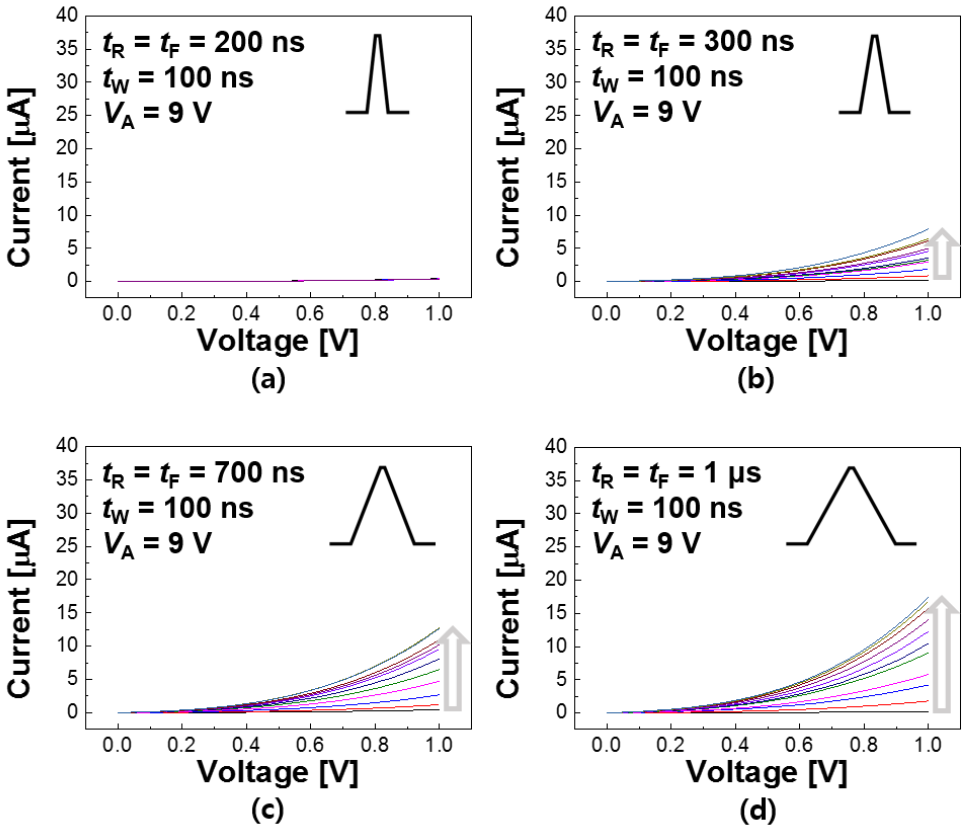


Fig. 2.8. Rise (t_R) and Fall time (t_F) dependent gradual resistance change of $Ni/Si_3N_4/SiO_2/p^+$-Si structured cell. Pulse condition: (a) V_A = 9 V, t_R = t_F = 200 ns (b) 9 V, 300 ns (c) 9 V, 700 ns (d) 9 V, 1000 ns

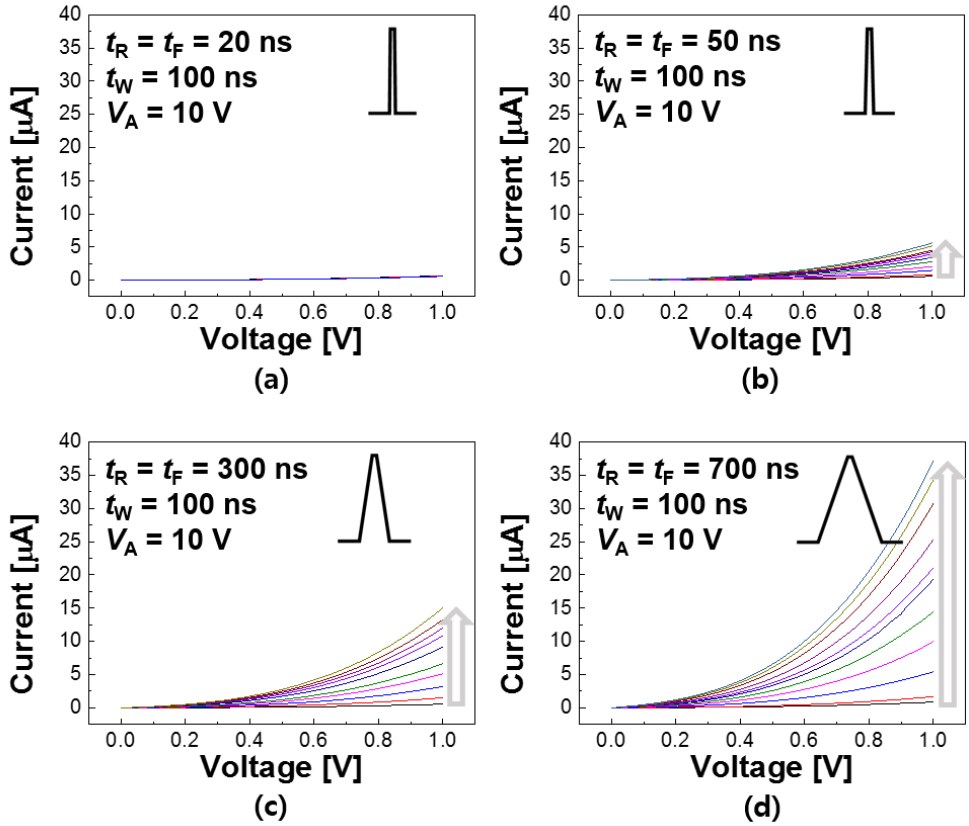


Fig. 2.9. Rise (t_R) and Fall time (t_F) dependent gradual resistance change of $Ni/Si_3N_4/SiO_2/p^+$-Si structured cell. Pulse condition: (a) 10 V, 20 ns (b) 10 V, 50 ns (c) 10 V, 300 ns (d) 10 V, 700 ns (t_W = 100 ns in all cases).

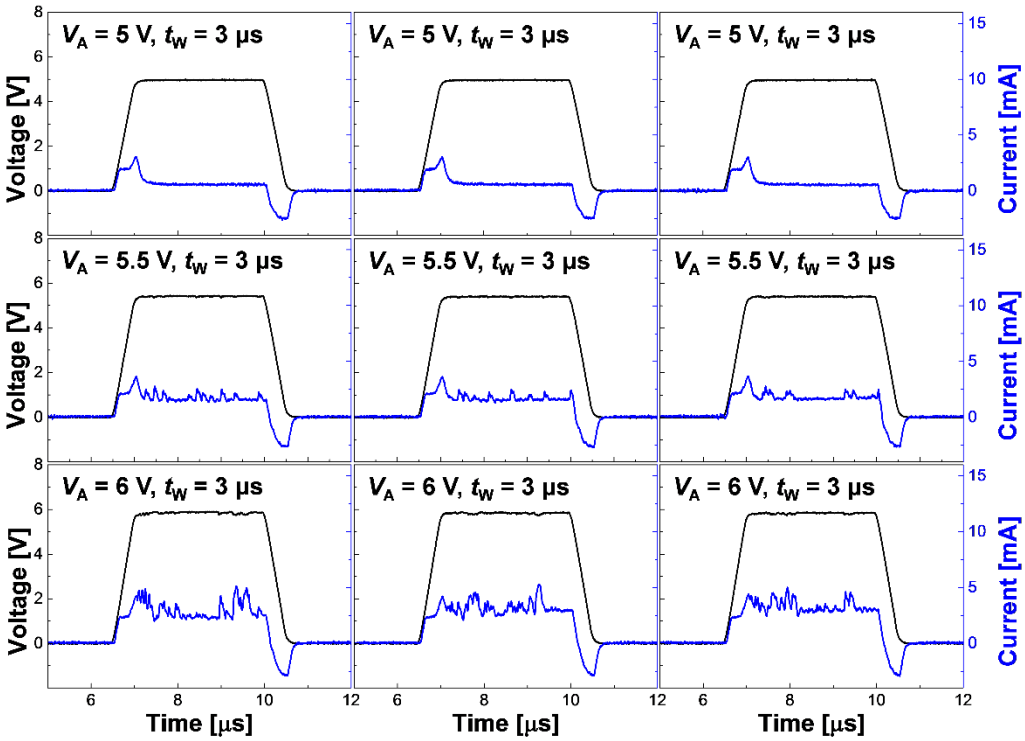


Fig. 2.10. Transient response for applied pulses with V_A = 5 V, 5.5 V, 6 V (t_W = 3 μs, t_R = t_F = 500 ns). These results (with Fig. 2.11) confirm that pulse below a certain threshold voltage is not able to change resistance state of the cell.

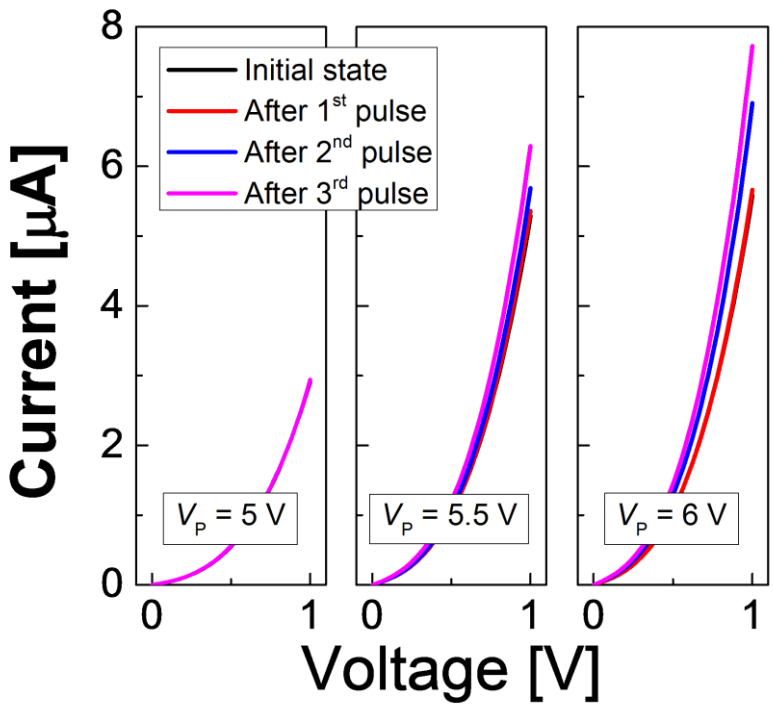


Fig. 2.11. Resistance change by consecutively applied three pulses with amplitude, V_A = 5 V, 5.5 V, 6 V. Between the applied pulses, DC sweep from 0 to 1 V was carried out to read the resistance state. DC curves show that pulse amplitude below 5 V can't change the resistance state.

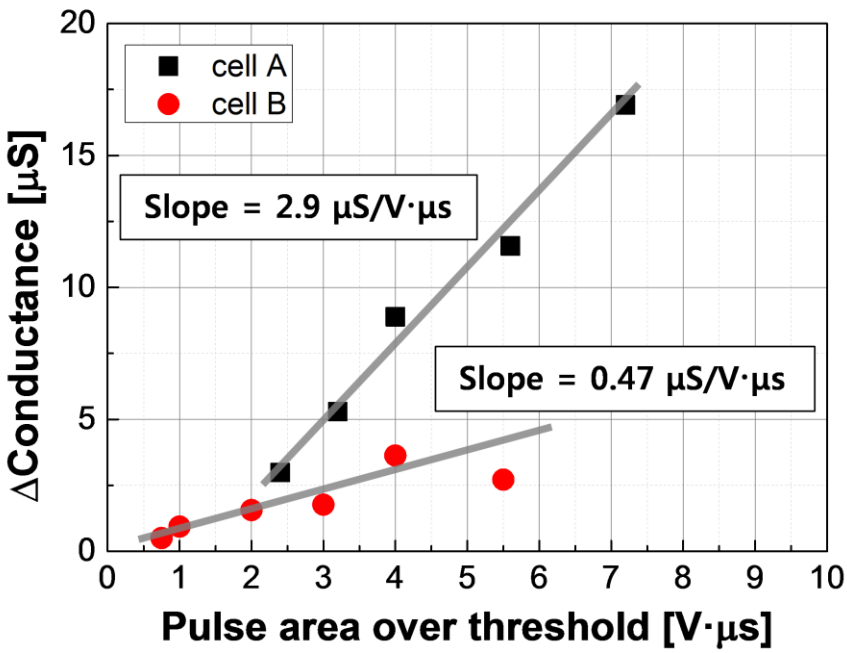


Fig. 2.12. Pulse area (over 5 V) versus conductance change of Si_3N_4/SiO_2 memory cell. Results show the linear dependence of the effective pulse area on the degree of conductance change. Cell A shows larger dependence on pulse area change (slope = 2.9 μS/V-sec) relatively than cell B (slope = 0.47 μS/V-sec). It is important to note that these characteristics are preferable as uniform as possible in the cell-to-cell.

From the above results, it can be expected that the degree of conductance change is proportional to the area over the threshold voltage of the applied pulse for the memory cell showing the gradual resistance change phenomenon. As shown in Fig. 2.12, the change in conductivity in each memory cell tends to increase linearly in proportion to the applied pulse area. It should be noted that there is a difference in the degree of change in conductivity due to each pulse in different cells, which may be improved by fabricating a memory device with uniform device-to-device characteristics.

2.3 Internal Overshoot Current Issue

2.3.1. Introduction

Reliability problem especially in terms of switching variability such as operation voltage, resistance states and switching speed have been a big issue of RRAM and prevented its application to industry. To be used as a synaptic device with two terminals, RRAM must essentially exhibit a continuous and reliable change in its conductivity [37-39]. In order to improve the uniformity of the switching operation, various studies have been carried out including attempts to reduce the overshoot current occurring in the set operation [40-41]. However, those researches could not include in-depth consideration on the measurement environment and precise analysis of overshoot current from the measured data. In addition, reducing the displacement current by changing the shape of the applied pulse may not be a suitable solution because the measured displacement current generated by the time-varying voltage signal in the planar capacitor structure is not the actual current flowing into the cell through

narrow conducting path.

We have investigated the effect of additional thin SiO_2 layer on switching variability of SiN_x-based resistive memory (RRAM). Also, the internal overshoot current actually flowing into the fabricated SiN_x-based RRAM cell during the switching process is confirmed by the accurate circuit implementation. It is confirmed that the addition of a thin SiO_2 layer can significantly reduce the internal overshoot current leading to the improvement of switching uniformity. Furthermore, we confirm the increase of low resistance state value (R_{LRS}) value and the decrease of cell capacitance (C_{DUT}) can be effective ways to suppress the internal overshoot current of RRAM.

2.3.2. Measurement Environment and Circuit Implementation

DC and pulse switching characteristics of the fabricated resistive memory cells were measured by using Keithley 4200-SCS SPA and 4225-

PMU ultra-fast *I-V* module. Measurement environment was implemented to SPICE equivalent circuit with reference to the equipment manual and experimental test. Capacitances of DUT and parasitic element were determined considering measured displacement current as well as its theoretical value ($C = \varepsilon \cdot A/t$) (Fig. 2.13(a)). In measuring the characteristics of two terminal resistive memory device, equipment can obtain read current from both of two channels. The first one is current read by channel 1 (I_{Ch1}) which includes capacitive current occurred by parasitic capacitance and memory cell capacitance and resistive current of memory cell (I_{Res}). Different from I_{Ch1}, current of channel 2 (I_{Ch2}) only includes cell capacitive current and resistive current because there is no charge and discharge effect of parasitic capacitance by applied voltage pulse.

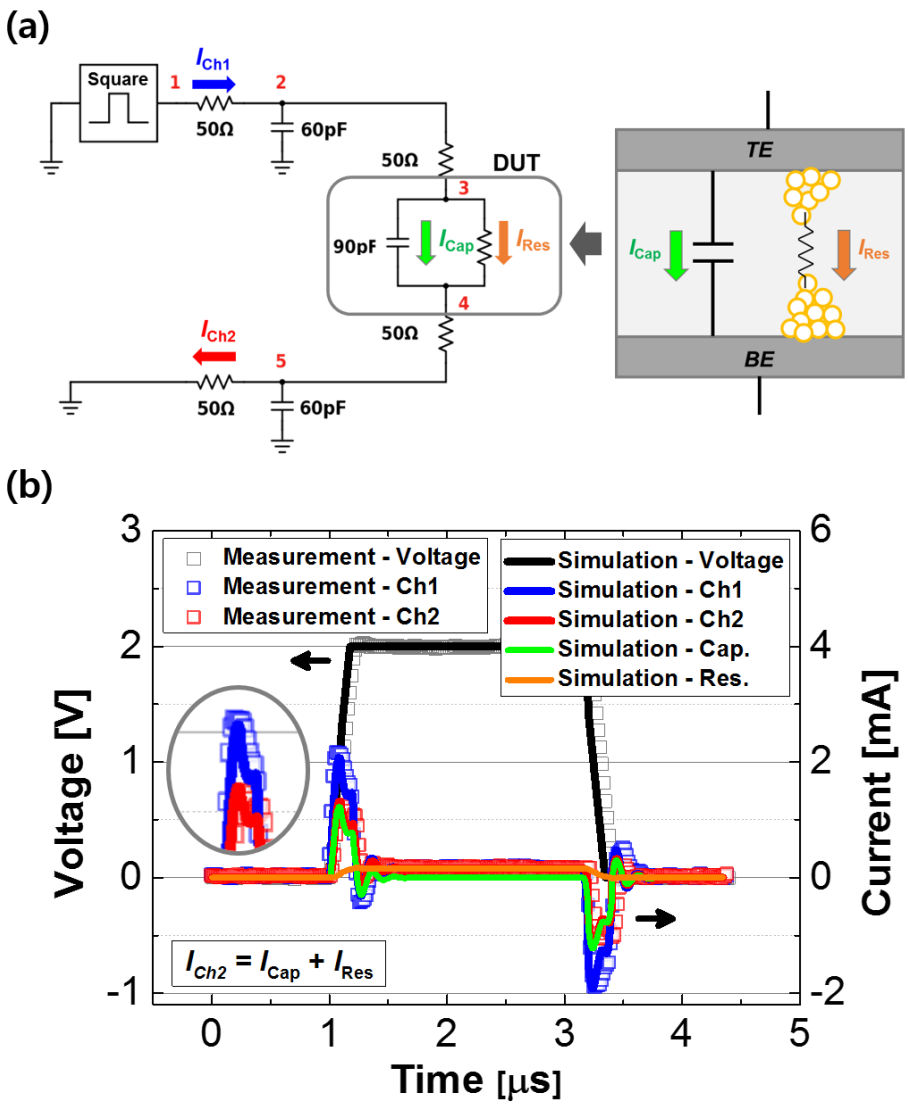


Fig. 2.13. (a) Circuit implementation of the measurement environment and Schematic diagram of the filamentary resistive memory cell. (b) Waveforms of applied voltage and output current in both measurement and circuit simulation.

Fig. 2.13(b) shows the waveforms of applied voltage and output current in both measurement and circuit simulation. It should be noted that this 2 V test pulse is applied for checking the capacitive current when the DUT is connected, and for obtaining the parasitic capacitance (C_p) and the inherent capacitance of the device (C_{DUT}). Thus, switching operation does not occur by this test pulse. Comparing both I_{Ch1} and I_{Ch2} in measurement (symbol) and simulation (solid line) results, it can be confirmed that the circuit is well implemented with the actual measurement environment. In addition, we can exactly separate and observe displacement (capacitive) current by only cell capacitance (green line) and resistive current through narrow conducting path of RRAM cell (orange line) from measured I_{Ch2} (red line) by circuit implementation. The classification of two current elements is quite important because displacement current does not actually flow through memory cell while resistive current is the only element directly flowing through resistive switching layer.

2.3.3. Internal Overshoot Current in Set Operation

Figs. 2.14(a) and (b) show the representative DC curves of Ni/SiN_x/p^+-Si and Ni/SiN_x/SiO_2/p^+-Si structured resistive memory cell, respectively. Compared to the characteristics of Ni/SiN_x/p^+-Si structured cell, those of Ni/SiN_x/SiO_2/p^+-Si structured cell show slightly larger operation voltages, smaller on/off ratio (R_{HRS}/R_{LRS}) and especially more gradual resistance switching phenomenon due to inserted SiO_2 layer with a large band gap. This gradual reset phenomenon appears to be related with significantly suppressed reset current from over 5 mA to below 0.1 mA. As a supporting evidence, it can be pointed out that the additional gradual reset phenomenon is observed after abrupt current drop in curves of Ni/SiN_x/p^+-Si structured cell (Fig. 2.14(a)). In addition, even in curves of Ni/SiN_x/SiO_2/p^+-Si structured cell, abrupt reset operation has been occasionally found in case of the leaky low resistance state (LRS) after strong set operation leading to large reset current. Hence, it is most important to reduce LRS current for gradual reset switching

without severe overshoot effect.

For each device, 100 cycles of switching operation were performed to investigate switching variability. Figs. 2.15(a) and (b) show HRS and LRS distribution and resistance change from LRS to HRS and from HRS to LRS of each device. Compared to the resistance distributions of Ni/SiN_x/p^+-Si structured cell, those of Ni/SiN_x/SiO_2/p^+-Si structured cell show more tight distribution and the reason is in stable resistance transition in set and reset operation. Also, it can be seen that the improved distribution is due to the suppression of excessive LRS and HRS by insertion of SiO_2 layer (Fig. 2.15(c)). To sum it up, when the excessive leaky state occurred in set operation, it leads to high reset current and abrupt reset operation. This abrupt reset operation results in excessive HRS and large resistance distribution. Therefore, it is important to understand the cause of the excessive leaky state occurring in the set operation in detail.

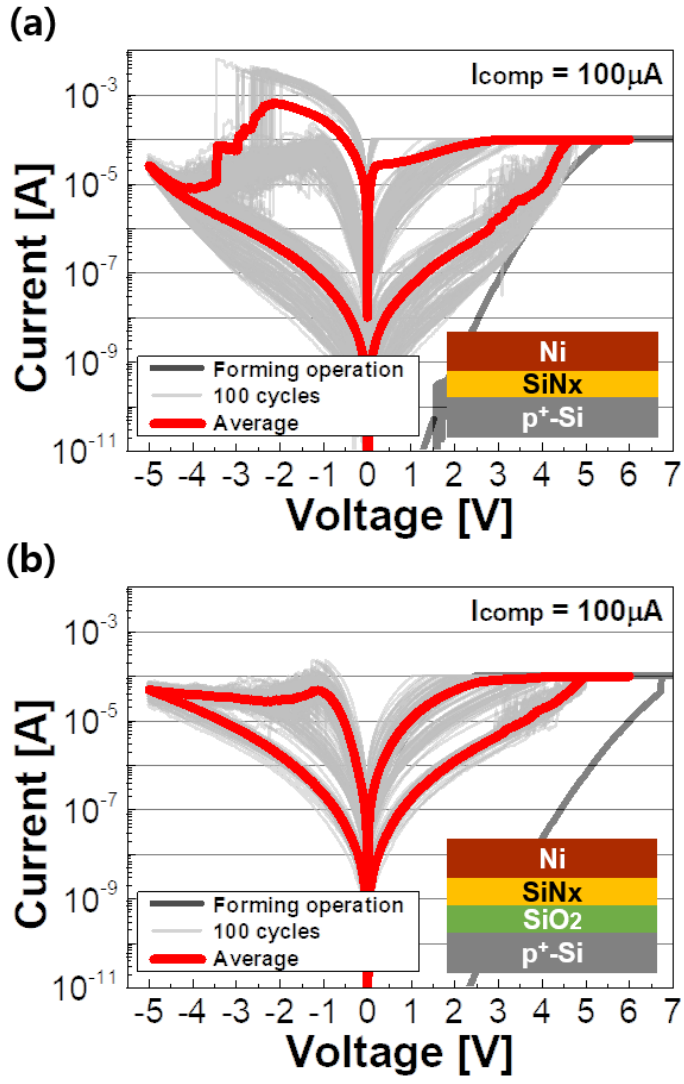


Fig. 2.14. DC characteristics of (a) Ni/SiN_x/p^+-Si structured resistive memory cell showing abrupt set operation leading to excessive LRS and abrupt reset operation and (b) Ni/SiN_x/SiO_2/p^+-Si structured cell showing both gradual set and gradual reset operation.

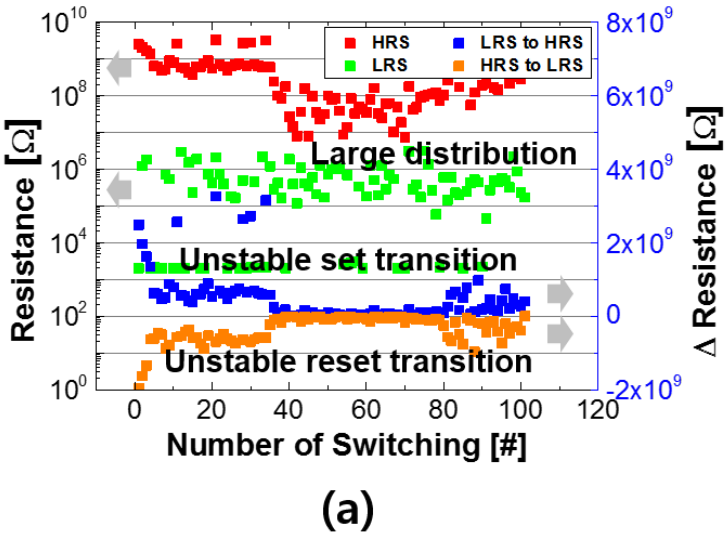
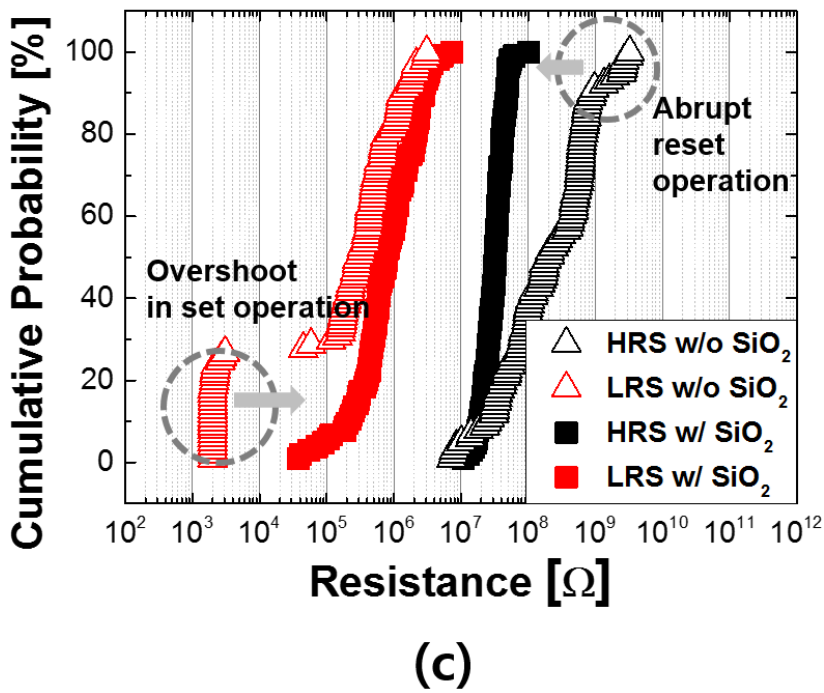


Fig. 2.15. Distributions of HRS (red) and LRS (green) and resistance change from LRS to HRS (blue) and from HRS to LRS (orange) of (a) Ni/SiN_x/p^+-Si structured cell and (b) Ni/SiN_x/SiO_2/p^+-Si structured cell over 100 cycles.



(c)

(c) Cumulative distributions of resistance states of each device. The distribution is improved through suppression of excessive LRS and HRS.

2.3.3.1. Effect of Thin Tunnel Barrier Layer

With a circuit implemented for measuring environment, the transient characteristics of various current elements in set operation have been investigated. In the SPICE model of the fabricated device, when the voltage applied to DUT, it is designed to induce an artificial set switching operation from HRS to LRS. For a more detailed description of the SPICE model, please refer to the previous study [42]. For both

Ni/SiN_x/p^+-Si and Ni/SiN_x/SiO_2/p^+-Si structured cells, the set voltage (V_{SET}) of SiN_x switching layer is approximately 6 V and simulated channel 2 current (red line) is fitted to have same current level with measured channel 2 current (red symbol). As shown in Fig. 2.16(a), it is found that the internal overshoot current is generated and flowing through actual resistive memory cell (orange line). In detail, this overshoot current originates from sudden voltage decrease between each electrode (grey line), leading to generate negative capacitive element (green line). The negative current element is added to resistive current

element, making a sharp peak. Compared to Ni/SiN_x/p^+-Si structured cell, Ni/SiN_x/SiO_2/p^+-Si structured cell shows decreased capacitive current and no peak of overshoot current due to the series resistance element by tunnel barrier layer (Fig. 2.16(b)). As a result, it is thought that the internal overshoot current occurred in each switching operation directly affects making excessive LRS (Fig. 2.15(c)).

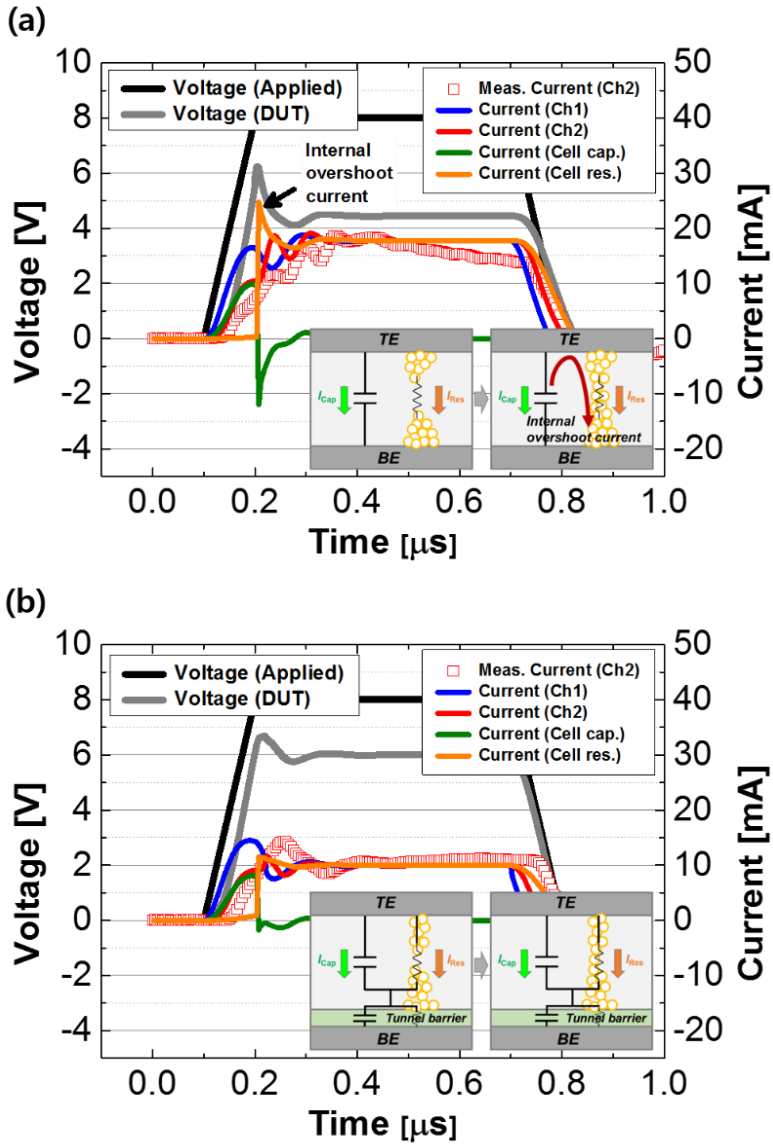


Fig. 2.16. Measured (symbol) and simulated (solid line) current element of (a) Ni/SiN_x/p^+-Si and (b) Ni/SiN_x/SiO_2/p^+-Si structured cell in set operation.

2.3.3.2. Effect of Resistance State and Cell Capacitance

The internal overshoot current flowing through the resistive path is mostly decided by the low resistance state value after set switching operation and the capacitance of the RRAM device. Thus, it can be expected that area scaling of RRAM device is an effective way to suppress the internal overshoot current because larger R_{LRS} and smaller C_{DUT} can be implemented. As shown in Figs. 2.17(a)-(c), internal overshoot current with higher peak is generated when the resistance state of the RRAM device is changed to smaller value because the actual voltage divided to the DUT decreases more sharply in set operation. This overshoot current generated instantaneously can cause more strong resistance change leading to smaller R_{LRS}. It is believed that this procedure is of great relevance with variability of the low resistance state because the overshoot current and the LRS resistance value are considered to have a positive feedback effect.

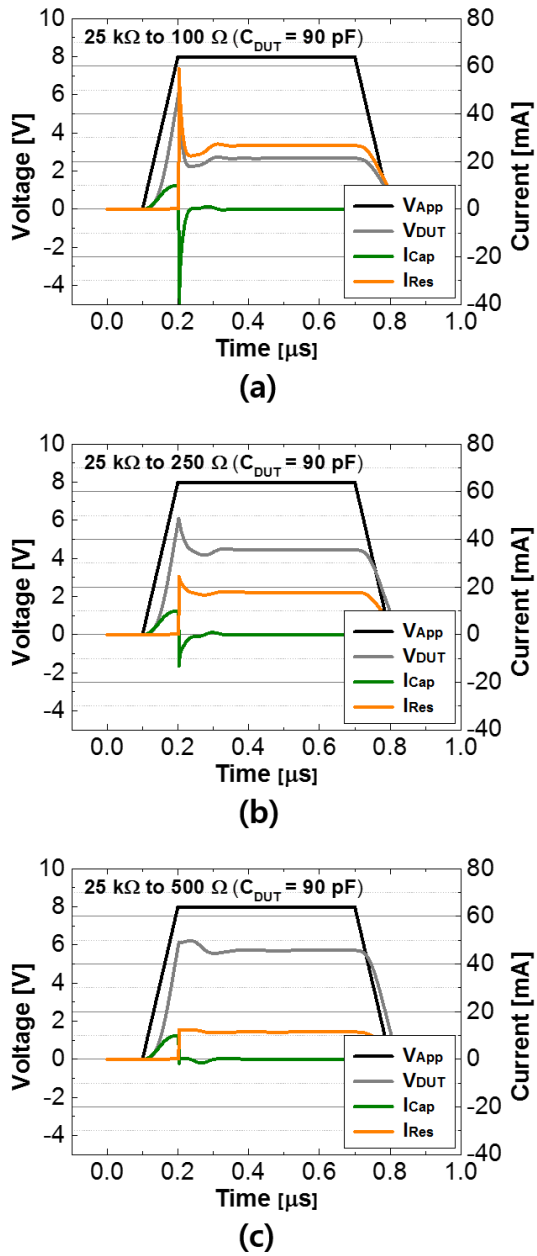


Fig. 2.17. Changes of internal overshoot current according to the low resistance state value (R_{LRS} = (a) 100, (b) 250, (c) 500 Ω, respectively).

The overshoot current is also affected by the capacitance of the device itself. As shown in Figs. 2.18(a)-(c), it can be seen that less overshoot current is generated during the set switching process as the capacitance of the device is reduced by a factor of 10 (for example, when the area of a device is reduced, the switching layer is thickened, or a material having a small dielectric constant is used) because less charge is accumulated across the device. The decrease of the capacitance also affects the operation speed. The time required for the device to be applied to the operating voltage of about 6 V was 103, 75 and 72 ns when the capacitance was 90, 9 and 0.9 pF, respectively. As a result, it can be concluded that the decrease of the capacitance due to the change of the device area, the thickness and the material, and the increase of the LRS resistance are effective in improving the uniformity of the resistance state by reducing the internal overshoot current as well as improving the operation speed.

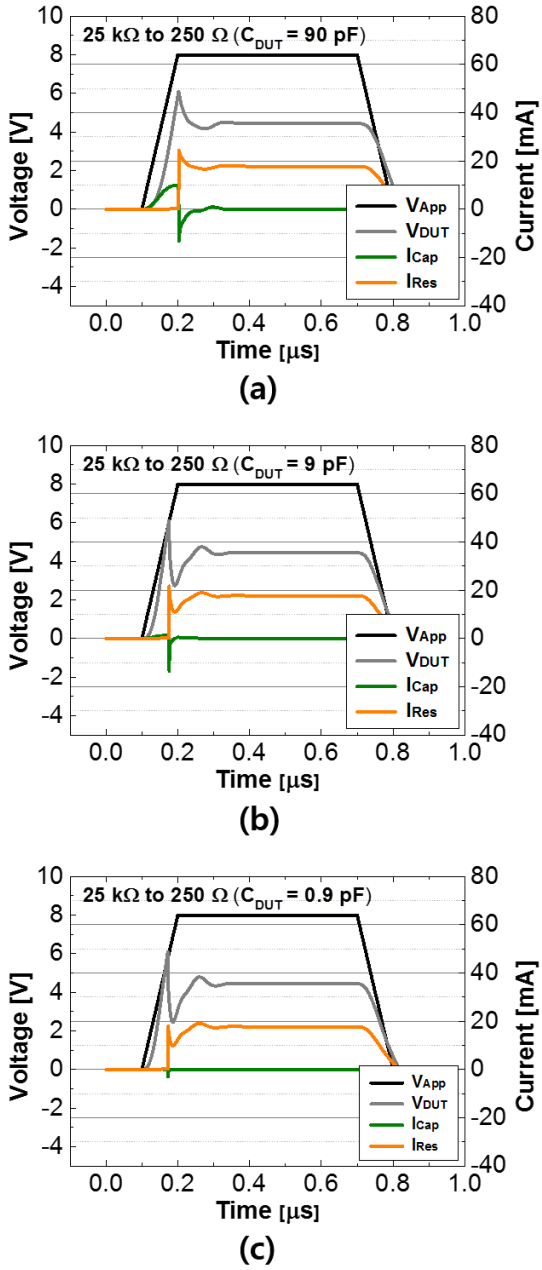


Fig. 2.18. Changes of internal overshoot current according to the cell capacitance (C_{DUT} = (a) 90, (b) 9, (c) 0.9 pF, respectively).

2.4 Circuit-Level Simulation of Resistive Switching Memories

In this part, a simple, reliable, and universal circuit model of bipolar-switching resistive-switching random-access memory (RRAM) is presented for the circuit-level simulation of high-density cross-point RRAM array. For higher accuracy and reliability, the compact model has been developed being corrected by the measurement results from the fabricated RRAM devices having SiN_x and HfO_x switching layers showing different reset switching behaviors. In the SPICE simulation, the RRAM cross-point array is virtually realized by embedding the empirically modeled memory cells, by which device performances such as read margin and power consumption in the high-density array are closely investigated.

For higher reliability to predict the device performances of RRAM memory cell in the high-density array and design such array architecture,

circuit-level modeling of both RRAM single cell and array is increasingly demanded.

Although several circuit models of RRAM device have been reported [43-47], they have limitation in accuracy and reliability for large-area circuit simulation due to model complexity resulting in excessively long simulation time and lack of ability to fully describe the bias-dependent various RRAM characteristics. Meanwhile, RRAM devices having transition metal oxides (TMOs) as the switching layer materials, including NiO_x, TiO_x, TaO_x, AlO_x, and HfO_x as well as Si-embedding dielectrics such as SiN_x and SiO_x have gained great deal of interests owing to their merits of fast switching speed, strong endurance, enhanced retention capability, and full Si CMOS processing compatibility.

2.4.1. A Circuit Model of Resistive Switching Memories

A RRAM cell can be used as a memory element in a cross-point array structure and also as a synaptic device in a neuromorphic system. Circuit simulation of such an array or a system requires an accurate and versatile circuit model of the resistive memory element.

As it is known, the switching layer of a filamentary-type RRAM consists of primitive insulating region and extremely narrow conducting path. The conducting path can be further divided into remaining path and gap regions [48-49]. The gap region is repeatedly connected and disconnected by set and reset operations as shown in the schematic diagram (Fig. 2.19(a)).

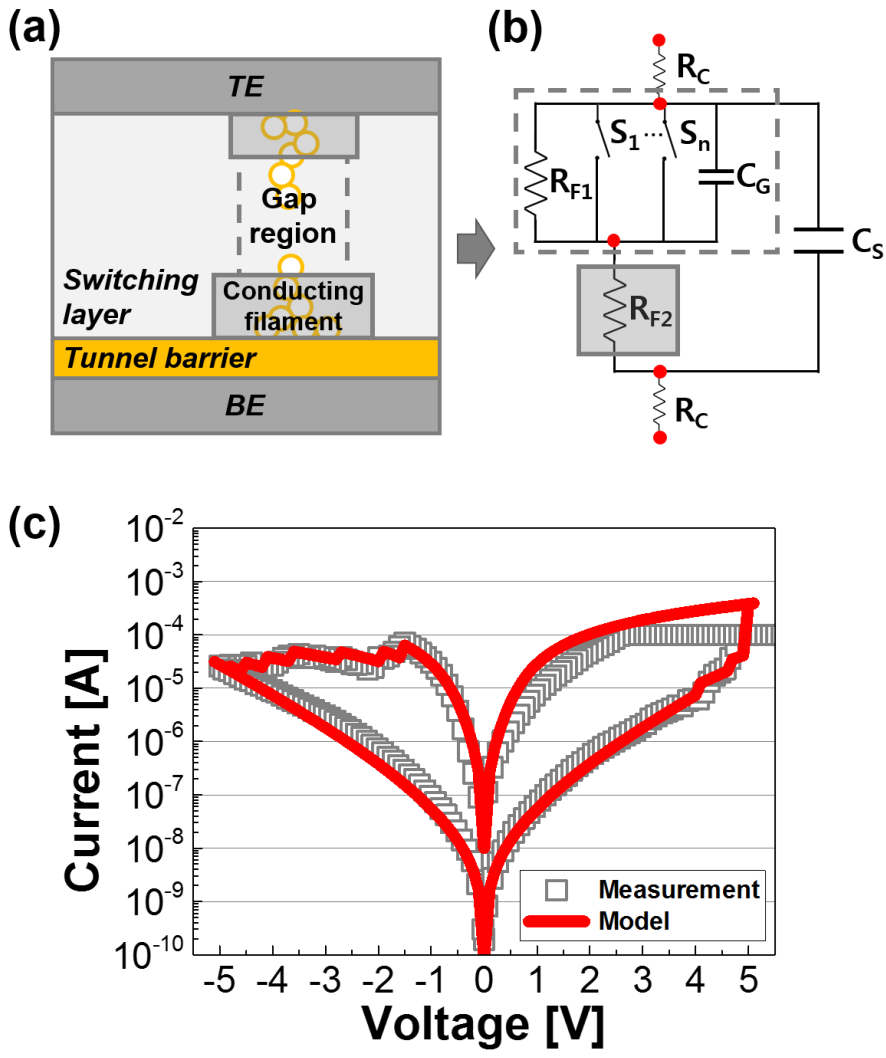


Fig. 2.19. (a) Schematic of a filamentary-type RRAM cell. (b) Circuit representation of a filamentary-type RRAM cell using simple components. (c) Results of measurement and modeling of $Ni/SiN_x/SiO_2/p^+$-Si structured memory cell.

Several circuit components are used to describe the voltage-dependent DC switching characteristics of a SiN_x-based RRAM on a circuit. Our circuit model consists of a non-linear resistor (R_F) for representing the remaining conducting path, several voltage-controlled switches (S_1-S_n) for describing the gradual resistance change behavior, and two capacitors (C_G, C_S) corresponding to the capacitive elements of the gap region and entire cell region, respectively (Fig. 2.19(b)). Parameters in non-linear resistance can be simply determined to represent the conduction behaviors of high and low resistance state. In addition, parameters of the multiple voltage-controlled switches such as threshold voltage (V_T), hysteresis voltage (V_H), and on/off resistance (R_{ON}, R_{OFF}) can be controlled to match various resistance switching behavior regardless of material, device structure, and size. Fig. 2.19(c) shows the measurement results and modeling behavior of Ni/SiN_x/SiO_2/p^+-Si structured memory cell. It can be seen that gradual set and reset switching characteristics

in addition to the conduction behaviors of the LRS and HRS states are simply matched.

We confirm that this modeling frame can be adopted to various RRAM devices having different device structures, switching layer materials and thicknesses leading to different switching and conduction behaviors as shown in Figs. 2.20, 2.21. Figs. 2.21(a) and (b) show the current-voltage (I-V) characteristics of HfO_x RRAM devices with different switching layer thicknesses. The increased set (V_{SET}) and reset (V_{RESET}) voltages by the change in HfO_x thickness from 3.5 nm to 6 nm and increased low-resistance state resistance (R_{LRS}) and high-resistance state one (R_{HLS}) are fitted in high precision by controlling the parameters of S1, R1, and R2. Figs. 2.20(a) and (b) depict the I-V characteristics of SiN_x RRAM devices with and without a tunneling oxide (SiO_2) layer [27]. The device with insertion of a tunneling layer shows relatively smaller on/off current ratio, the ratio between LRS and HRS currents at read voltage ($I_{LRS}@V_{READ}/I_{HRS}@V_{READ}$). It is noted that the

reset switching type (i.e., abrupt, step-like gradual reset, and continuous gradual reset) can be determined by the LRS resistance value. The large conducting path caused by current overshoot shows abrupt reset switching. As the strength of conducting path is weakened or the gap region is increased, the gradual reset switching is observed for SiN_x-based RRAM devices [50]. Comparing the characteristics of two devices in Fig. 2.21(a) and (b), the resistance of SiN_x device seems to be larger than that of SiN_x/SiO_2 device. It is because high reset current makes it difficult to control the reset operation and causes an excessive reset current for SiN_x RRAMs. This high reset current level results from the previous excessive set operation. However, characteristics including initial resistance state prior to forming operation and the switching voltage are higher in the SiN_x/SiO_2 RRAM device. This difference is also described by simply controlling R1, R2, and voltage controlled switches.

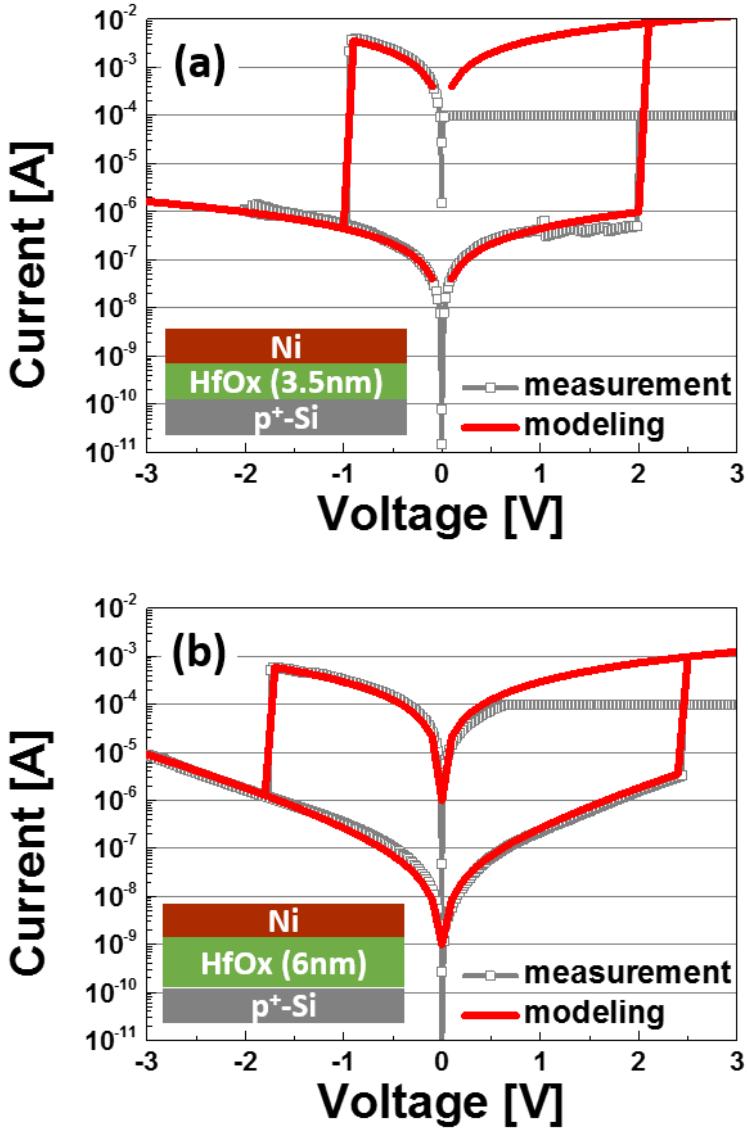


Fig. 2.20. DC characteristics of HfO_x RRAM devices in comparison between fabricated devices and proposed circuit models. The switching layer materials and thicknesses are (a) 3.5-nm HfO_x, (b) 6-nm HfO_x.

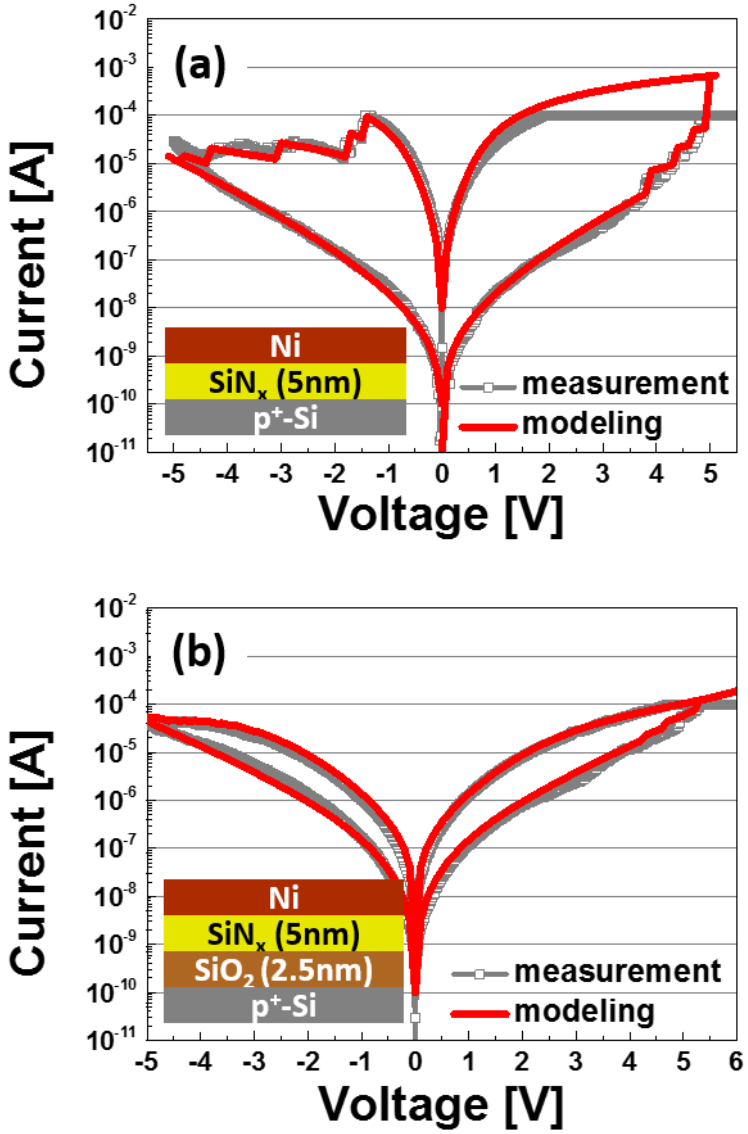


Fig. 2.21. DC characteristics of SiN_x-based RRAM devices in comparison between fabricated devices and proposed circuit models. The switching layer materials and thicknesses are (a) 5-nm SiN_x, and (b) 5-nm SiN_x/2.5-nm SiO_2.

2.4.2. Circuit Simulation of RRAM Cross-Point Array

Utilizing SPICE simulation, individual cell model has been adopted to RRAM cross-point array schematically shown in Fig. 2.22(a). By selecting a target cell and applying V_{SET} and V_{READ}, read margin and power consumption have been investigated in each array made up of RRAM cells with different configurations. Here, the read margin is defined to be the difference between read voltages at low-resistance and high-resistance states ($V_{READ,LRS} - V_{READ,HRS}$)/$V_{READ}$). In performing set and reset operations, 1/2 V scheme is used to select one cell and prevent electrical interference from adjacent cells as shown in Fig. 2.22(b). Also, in conducting read operation, V_{READ} is applied to the selected wordline (WL) and I_{READ} is sensed and amplified with use of load resistance (R_L = 10kΩ) at the same time as demonstrated in Fig. 2.22(c). As can be seen in Fig. 2.23(a), read margin increases with decreasing low resistance value and this is because the read current flowing in load resistance increases. As shown in Fig. 2.23(b), read margin tends to increase as a

function of on/off ratio (R_{HRS}/R_{LRS}). However, the read margin of SiN_x-based RRAM memory array is smaller than that of HfO_x (thickness = 6 nm) one despite the larger on/off ratio of the latter group since read margin is also closely related with low resistance state (LRS) of target cell. From these results, it can be concluded that both LRS state and on/off ratio of resistive memory cells are important characteristics to determine the read margin in cross-point array structure. In the cross-point array with high density and capacity, power consumption in read operation also become an important parameter along with read margin. Power consumption in read operation can be evaluated with the power consumed by voltage source for reading a target cell. Power consumption shows large dependence on resistance of target cell in the LRS as shown in Fig. 2.24(a). In addition, number of cells in the LRS affects power consumption in read operation. In cross-point array, the LRS cells are randomly selected and power consumptions are evaluated, respectively. As shown in Fig. 2.24(b), power consumption shows dependence

on number of LRS patterns. In detail, power consumption increases largely when LRS cells sharing the same selected wordline is added while other cells affect slightly. Consequently, using the circuit model for each device, we investigated the effect of on/off ratio and LRS state of resistive memory cell on read margin. Also, it is revealed that and power consumption is determined by LRS state and number of LRS patterns. Importantly, LRS value has a trade-off for read margin and power consumption.

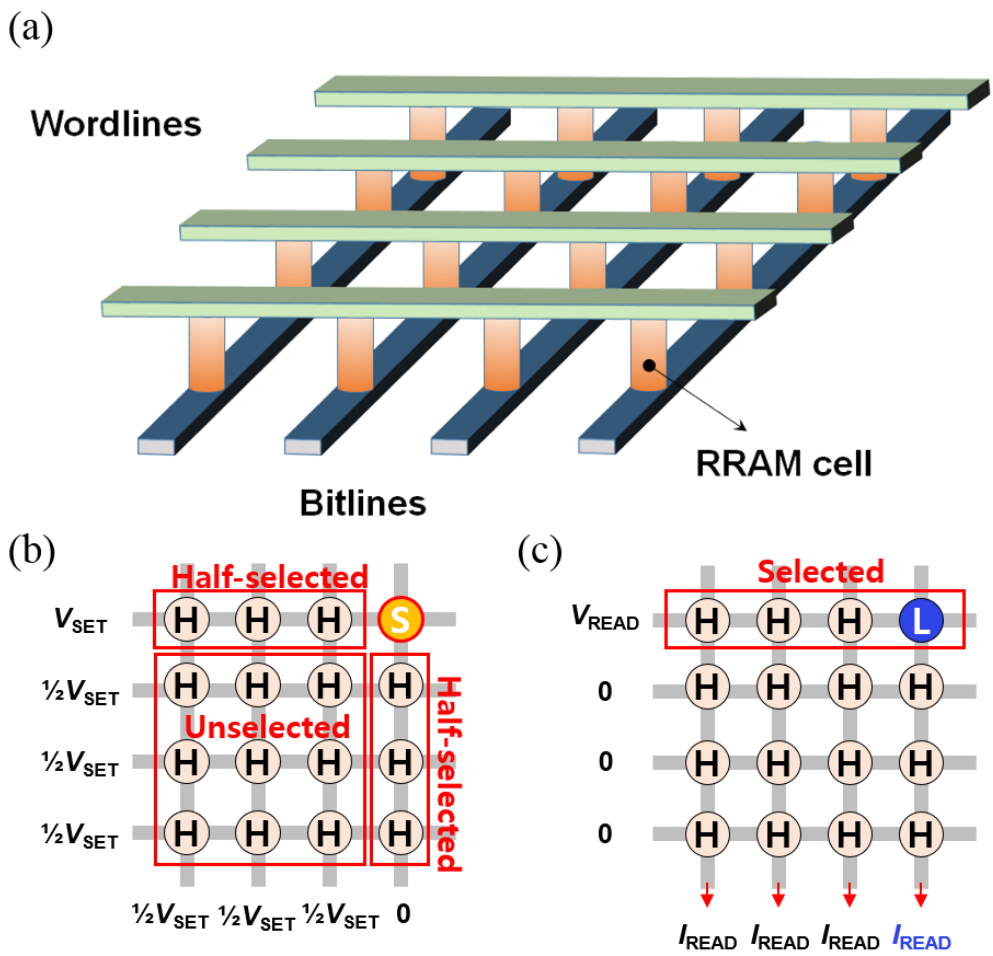


Fig. 2.22. (a) Schematic of the simulated 4×4 cross-point array. The characteristics of compact model are implanted to individual cells. (b) Set and reset operations. 1/2 V scheme is used to select on cell properly and prevent electrical interference (voltage disturbance) from other cells. (c) Read operation. V_{READ} is applied to the selected WL.

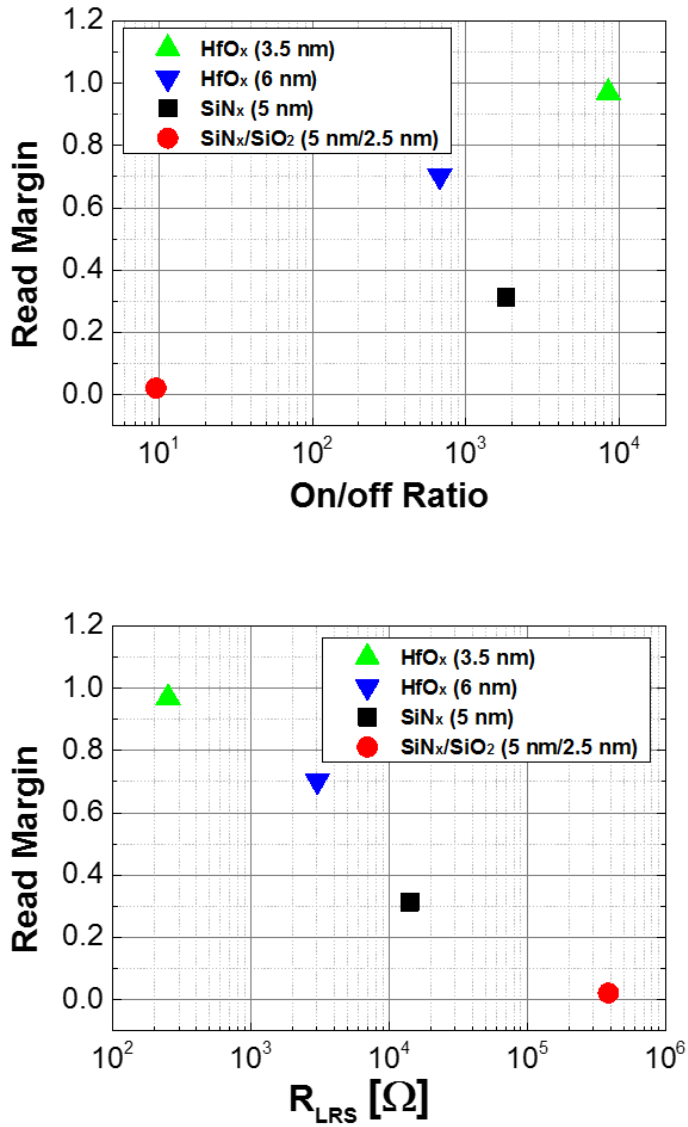


Fig. 2.23. Read margin (= ($V_{READ,LRS}$ − $V_{READ,HRS}$)/V_{READ}) as a function of (a) on/off resistance ratio and (b) low resistance state value (R_{LRS}) of each resistive memory cell.

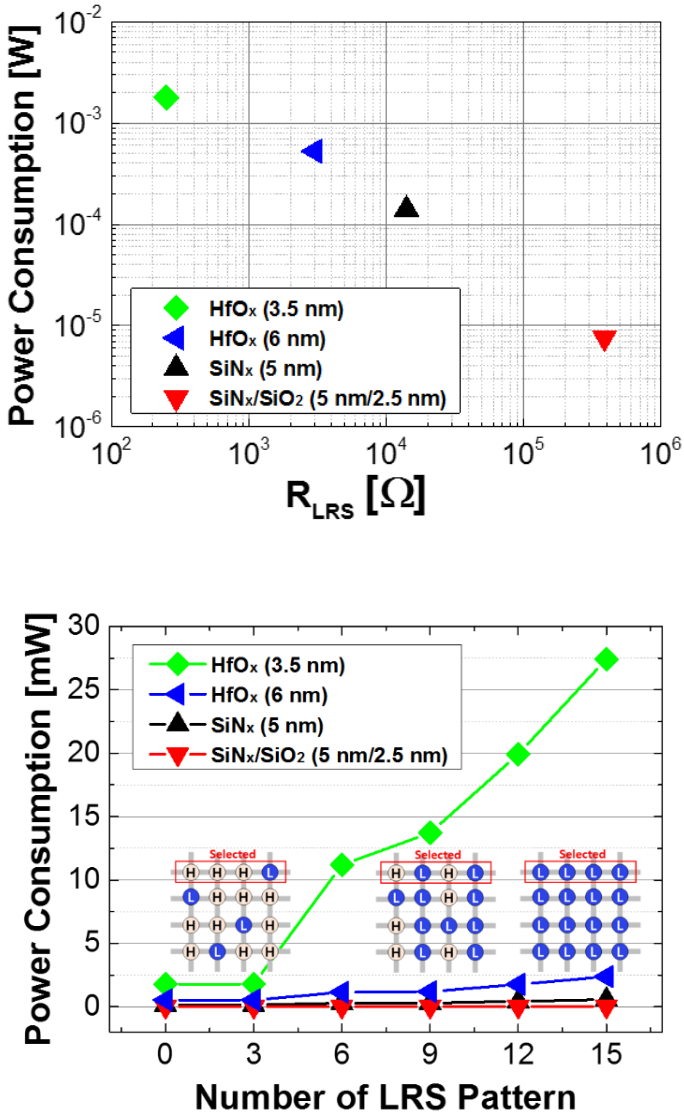


Fig. 2.24. Power consumption in read operation as a function of (a) low resistance state value (R_{LRS}) and (b) number of LRS patterns.

Chapter 3

A Nano-Structured RRAM Cross-Point Array

It is known that area scaling of RRAM cell affects energy consumption and resistance in the switching process. We herein introduce the fabrication of an RRAM cross-point array with a silicon wedge-structure and investigate its resistive switching characteristics. The effect of reducing the device area on energy consumption is discussed. Finally, we verify the input vector-conductance matrix multiplication function of a 2×2 RRAM array with different conductivities.

3.1 Fabrication of Wedge-Structured RRAM Array

To miniaturize the cell area, a resistive memory array is fabricated using an anisotropic wet etch process. First, we prepare the pre-cleaned p-type (100) wafer (Fig. 3.1(a)). Subsequently, line and space patterns are formed by photolithography followed by dry etching using HBr gas of etch rate 42 Å/s to form the silicon fin structure (Fig. 3.1(b)). Next, we use the TMAH anisotropic wet etch process to form the Si wedge structure with a pointed tip (Fig. 3.1(c)). We fill the Si bottom electrode (BE) using the SiO_2 deposition and CMP processes (Figs. 3.1(d)-(e)). We use DHF wet etching to reveal the fine areas of the pointed silicon tip (Fig. 3.1(f)). We deposited 5, 7, 9 nm SiN_x as a switching layer material (Fig. 3.1(g)). Finally, top electrodes are formed through Ti metal deposition and patterning to a width of 500 nm (Fig. 3.1(h)).

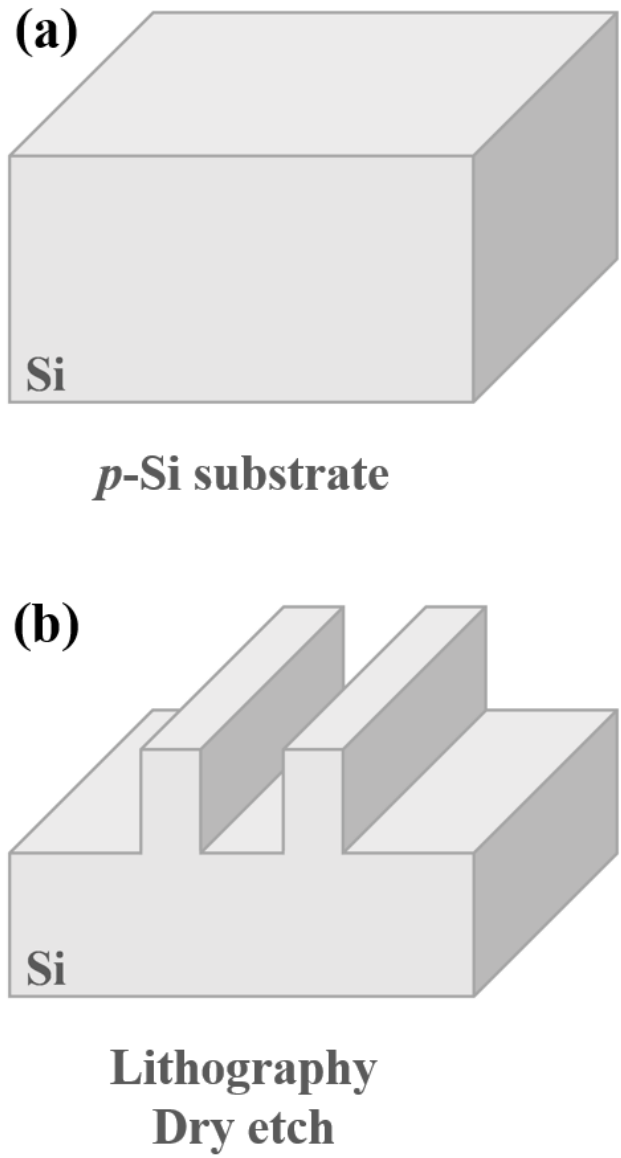
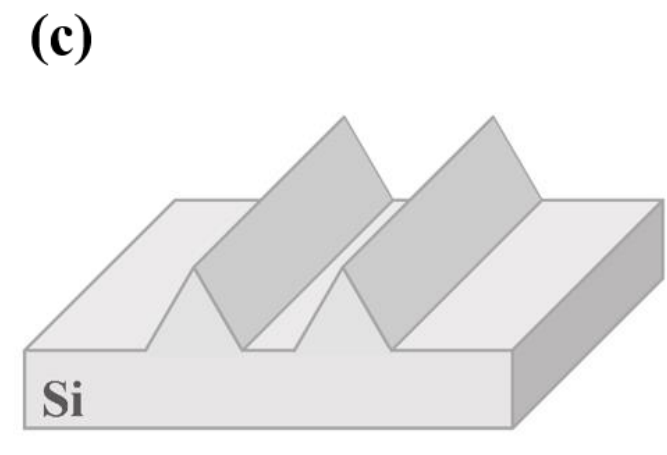
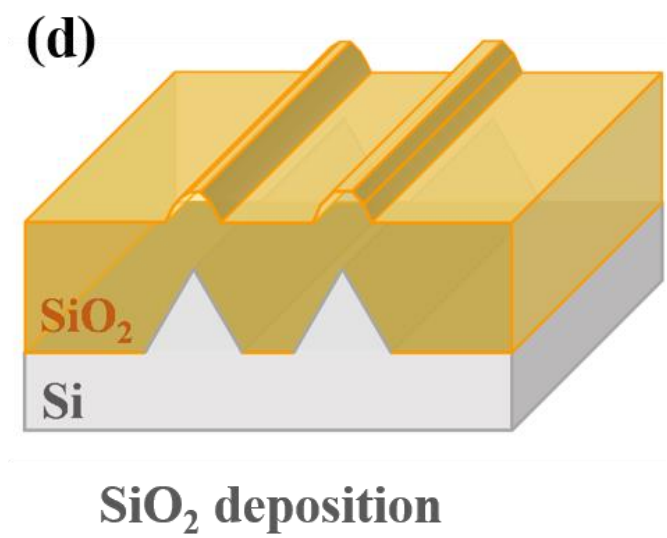
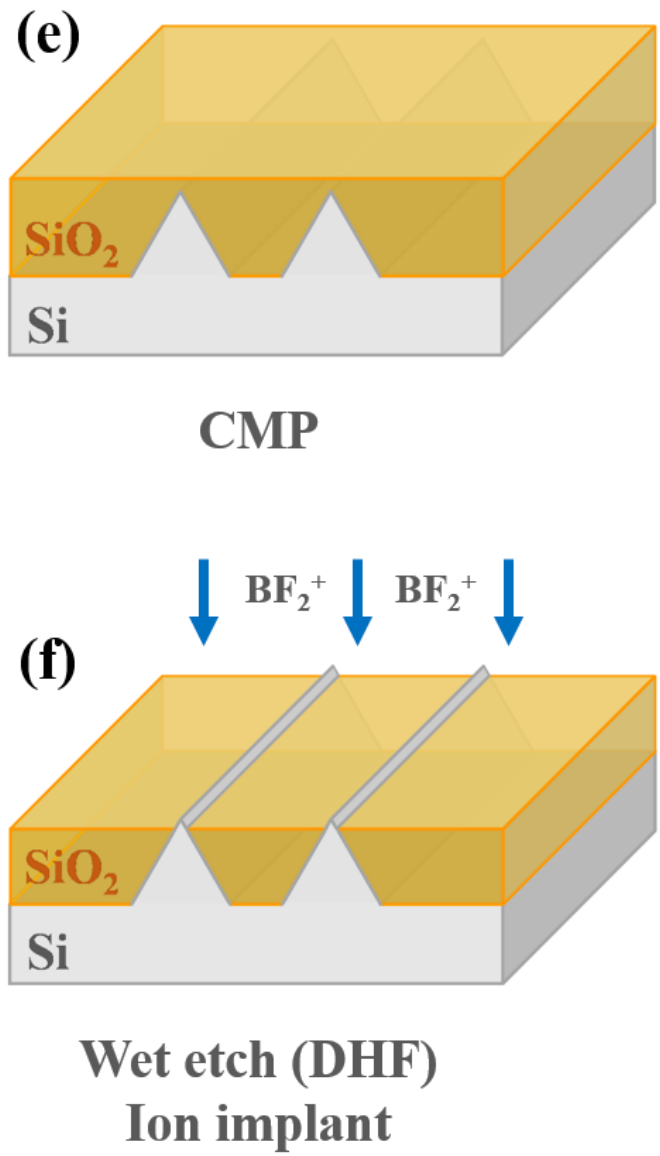


Fig. 3.1. Process flow for wedge-structure RRAM cross-point array. (a) (100)-orientation silicon wafer preparation. (b) Photolithography and dry etch.

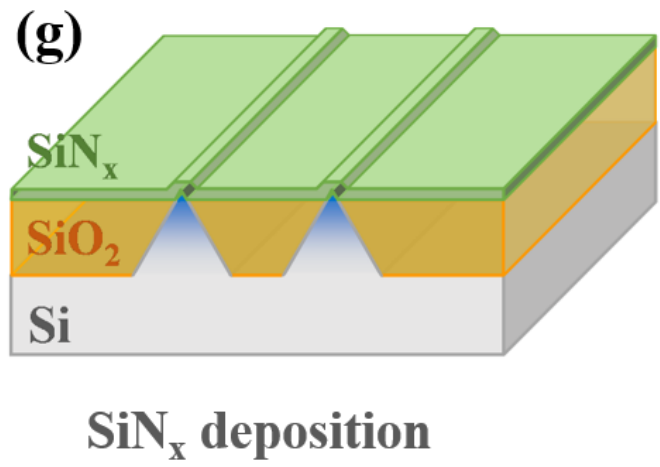


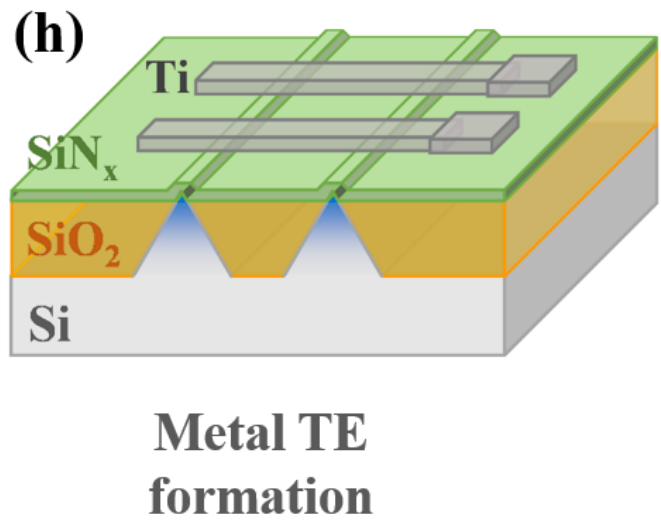


(c) Silicon wet etch (25% TMAH solution). (d) SiO_2 deposition.



(e) CMP process. (f) SiO_2 wet etch (DHF) and ion implantation.





(g) Silicon nitride (switching layer) deposition. (h) Titanium deposition and top electrode (TE) patterning.

Fig. 3.2(a) shows an SEM image of the silicon bottom electrode lines (two dummy lines and an actual electrode line) from bird's eye view after wet etching at room temperature. It is confirmed that a pointed tip is finely formed exposing (111) planes. A transmission electron microscopy (TEM) image cross-sectional view and an energy dispersive x-ray spectroscopy (EDS) line scan confirm a Ti/SiN_x/p^+-Si-structured RRAM device, as shown in Figs. 3.3(b) and (c).

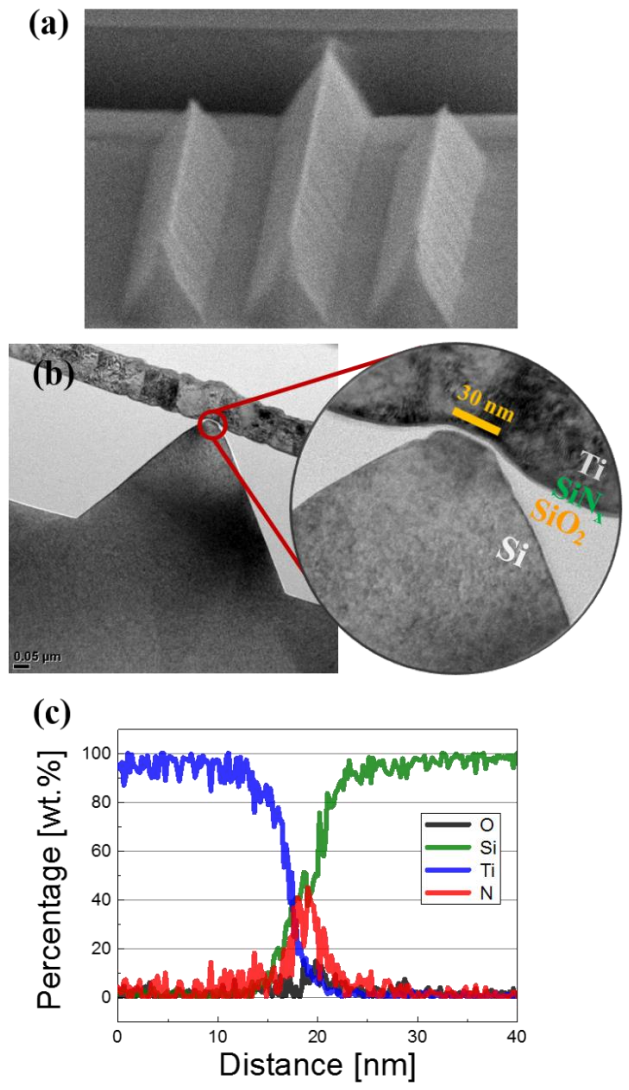


Fig. 3.2. (a) SEM image of Si bottom electrode lines from bird's eye view after TMAH wet etch process at room temperature. (b) TEM images of cross-sectional view of wedge-structured RRAM cell. (c) EDS line scan of the Ti/SiN_x/p^+-Si-structured cell.

3.2 Anisotropic Wet Etch Process of Crystalline Silicon

From a silicon fin structure, we dipped wafers into a TMAH solution for an anisotropic silicon wet etch. Next, 400 ml of the TMAH solution of 25% concentration was prepared at room temperature (temperature inside TMAH solution was 17.2 °C). To estimate the etch rate of silicon on (100) and (110) planes and to determine the conditions under which the nanoscale wedge structure was formed, the wet etch time was set to 8–13 min. After the wet etch and cleaning steps, the cross-sectional view of each sample was verified by a field emission scanning electron microscopy (FE-SEM).

Fig. 3.3 shows the silicon wet etch procedure using TMAH solution. Starting from the fin structure, the fin exhibits a narrower structure and the top of the fin is sharpened (Fig. 3.3(a)-(c)). As time goes by, the wedge structure with steep slope disappears, and a blunt wedge that reveals (111) planes is formed (Fig. 3.3(d)-(f)). Fig. 3.4 shows the etch rates of the (100) plane and near the (110) sidewall plane (slope = 87°) of the low-temperature TMAH

solution. The etch rate of the (110) plane compared to that of the (100) plane is nearly doubled, which is consistent with the previous experimental results at high temperatures. Depending on the aspect ratio of the fin, various wedge structure can be obtained (Fig. 3.5). When the aspect ratio is much larger than 1, a sharp wedge and a blunt wedge is shown. When the aspect ratio is smaller than 1, wedge structure is not formed.

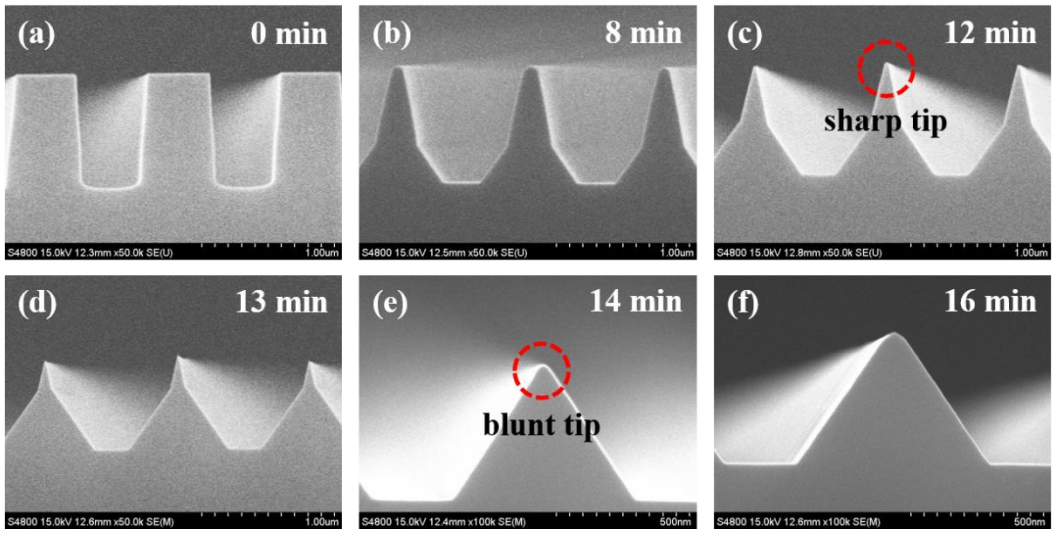


Fig. 3.3. Silicon anisotropic wet etching process using TMAH solution. (a) 0 min, (b) 8 min, (c) 12 min, (d) 13 min, (e) 14 min, (f) 16 min after being immersed in the solution.

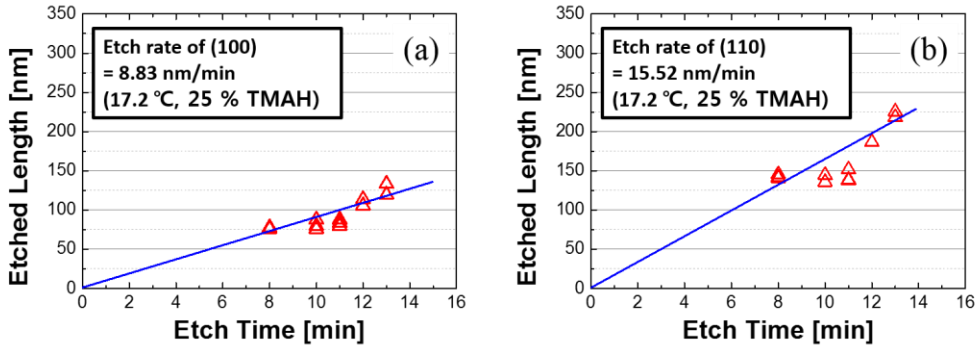


Fig. 3.4. Etch rates of (a) 100 plane and (b) near (110) sidewall plane (slope = 87°) of low-temperature TMAH solution.

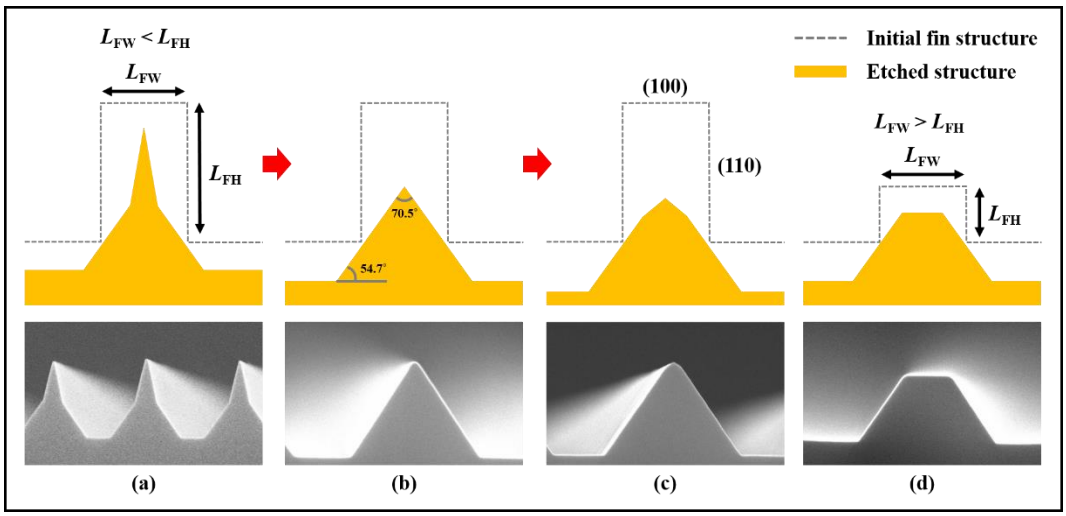


Fig. 3.5. Anisotropic wet etch procedure of silicon fin structures. (a)-(c) When the fin structure has a much larger aspect ratio 1, various wedge structures can be formed depending on the etch time. (d) When the aspect ratio is smaller than 1, the wedge structure is not formed.

3.3 Electrical Characteristics

3.3.1. Switching and Memory Characteristics

Figs. 3.6(a)-(c) show the basic memory characteristics of SiN_x-based RRAM unit cells. As shown by the DC switching characteristics, set voltage decreases from 6 V to 3.5 V and the reset voltage decreases from −3 V to –2.2 V as the thickness of the switching layer is reduced from 9 nm to 5 nm (Figs. 6(a)-(b)). The retention characteristics show that both the LRS and HRS do not change much within 10^3 s while maintaining over 10^2 of on/off resistance ratio (Fig. 3.6(c)).

3.3.2. Cell Area Dependency

Resistive memory cells having various cell areas from planar to pointed tip structures were fabricated. In the pulse operation, the effect of the

cell area on the resistance change characteristics was confirmed. When one switching operation was performed using set and reset pulses of the same voltage amplitude, it was confirmed that both the set and reset currents decreased according to the effective cell area (Fig. 3.7(a)). Fig. 3.7(b) shows that the set current decreases from 4.1 mA to 0.81 mA, and the reset current decreases from 3.4 mA to 0.82 mA when the effective area decreases from 0.25 μm^2 to 0.025 μm^2. It has been reported that the switching and conduction process are closely related to Si dangling bonds generation/re-passivation [51]. It is also known that the effective area of the cell where the electrodes cross is proportional to the amount of charges accumulated on both electrodes before the switching process, and these charges flow into the cell internally during the switching procedure affecting the degree of dielectric breakdown and the resistance state, as shown in Fig. 3.8 [52]. Consequently, this internal overshoot current affects the distribution of the resistance states, in addition to the energy consumption in the switching operation, as shown in Fig. 3.7(b).

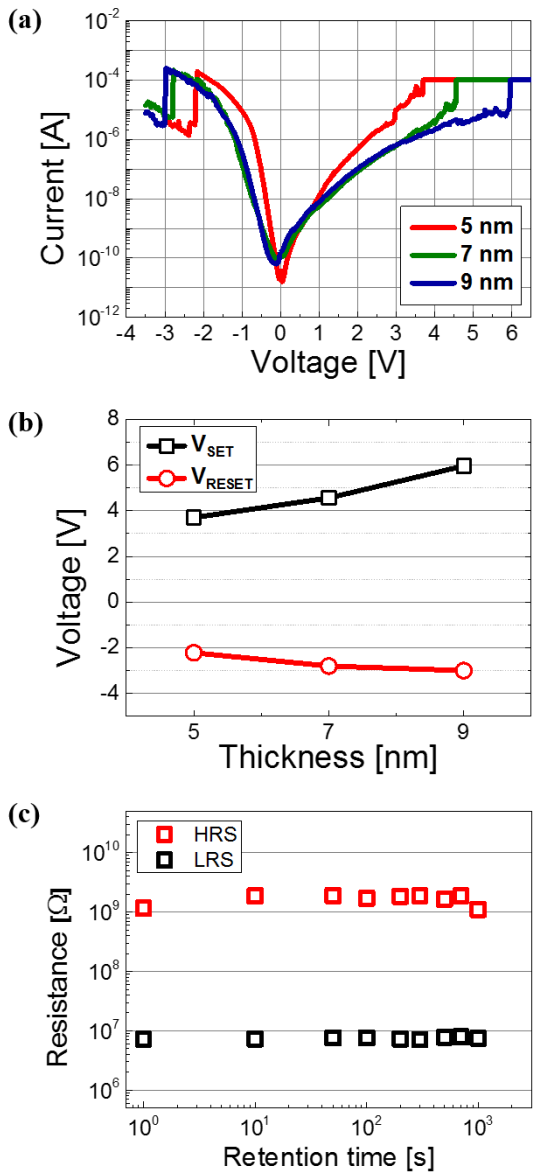
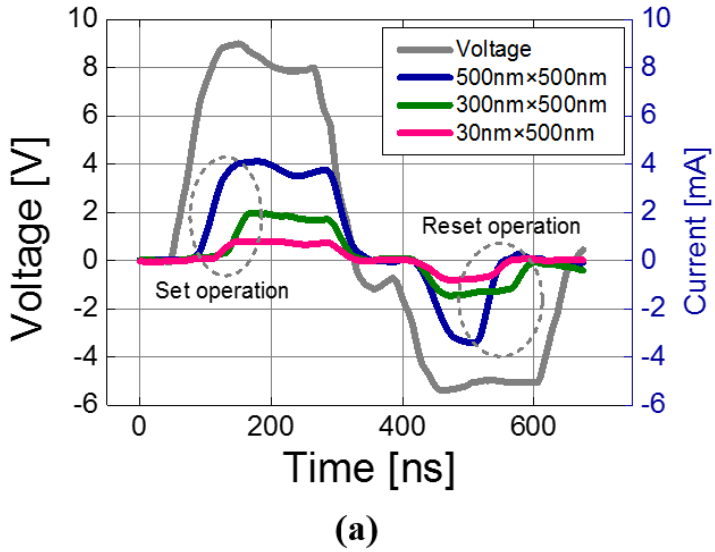
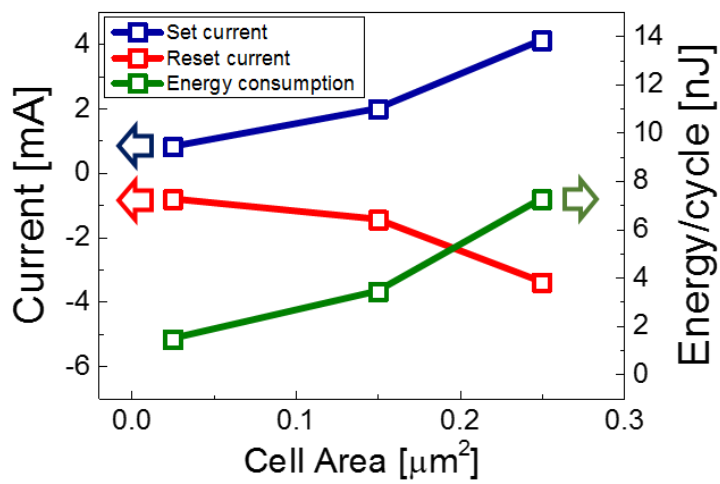


Fig. 3.6. Basic memory characteristics of SiN_x-based RRAM unit cell. (a) DC switching characteristics and (b) Set and reset voltages depending on the switching layer thickness (5, 7, and 9 nm). (c) Retention characteristics



(a)



(b)

Fig. 3.7. (a) Pulse switching operation of SiN_x-RRAM cells. (b) Changes in the set, reset current and energy consumption per cycle according to the different cell areas.

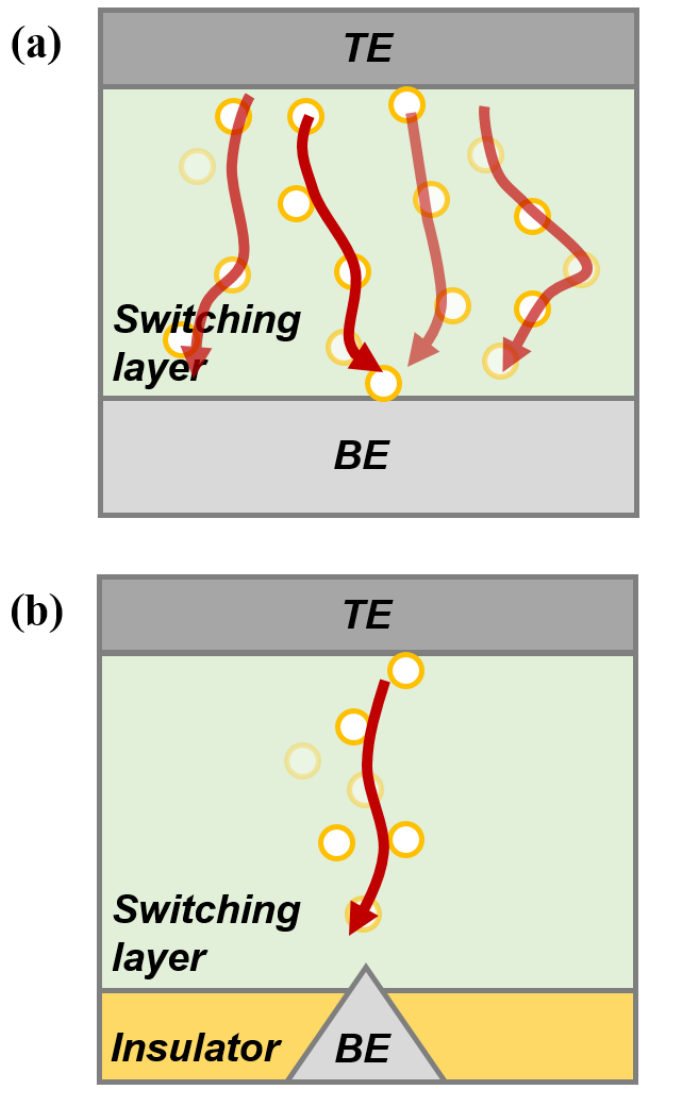


Fig. 3.8. Comparison of conduction characteristics of (a) typical planar structure and (b) nanoscale wedge-structured resistive memory cells.

3.4 Vector-Matrix Multiplication Function of RRAM Array

To obtain the resistance state of the resistive memory cell, the two methods shown in Fig. 3.9 can be considered. In the one-cell access method of Fig. 3.9(a), however, the exact conductivity of the accessed cell (G_{11}) cannot be obtained owing to the parasitic sneak current component ($I = V_1 \cdot (G_{12}//G_{22}//G_{21})$) flowing through the remaining cells. Therefore, we used the word-line (WL) access method applying the read voltage (1 V) to the selected WL, and 0 V to the remaining WL and all BLs (Fig. 3.9(b)).

As shown in Figs. 3.10(a), (c), a 1-V bias is applied to the first WL and the second WL to obtain the conductivity of each cell from each bit line current (I_1, I_2). Next, we confirm that the product of the input voltages and the conductivity matrix is converted appropriately to current by applying a bias to both WLs simultaneously. Figs. 3.10(b), (d) show the bit line currents I_1, I_2 owing to each cell, which are proportional to conductivity. Fig. 3.10(f) shows

the sum of two currents by the cells (1-μm width) on the same bit line when applying the voltages simultaneously (Fig. 3.10(e)). As shown, the measured current (opaque lines) is smaller compared to the sum of the ideal current by calculation (translucent lines). In the nanowedge-structured cells (30-nm width), the difference between the measured and calculated currents was reduced by 4.9% and 7.2%, respectively. However, further improvements and analyses should be performed.

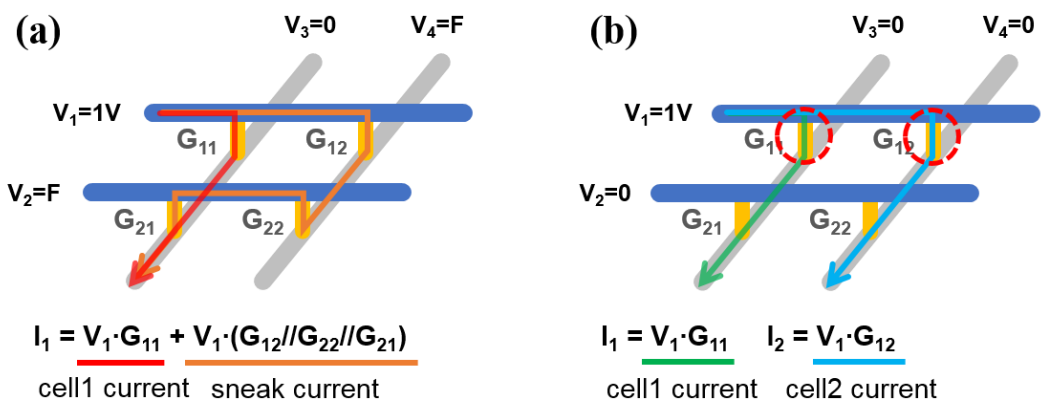


Fig. 3.9. Two read schemes of RRAM cross-point array. (a) One-cell access and (b) word-line access method.

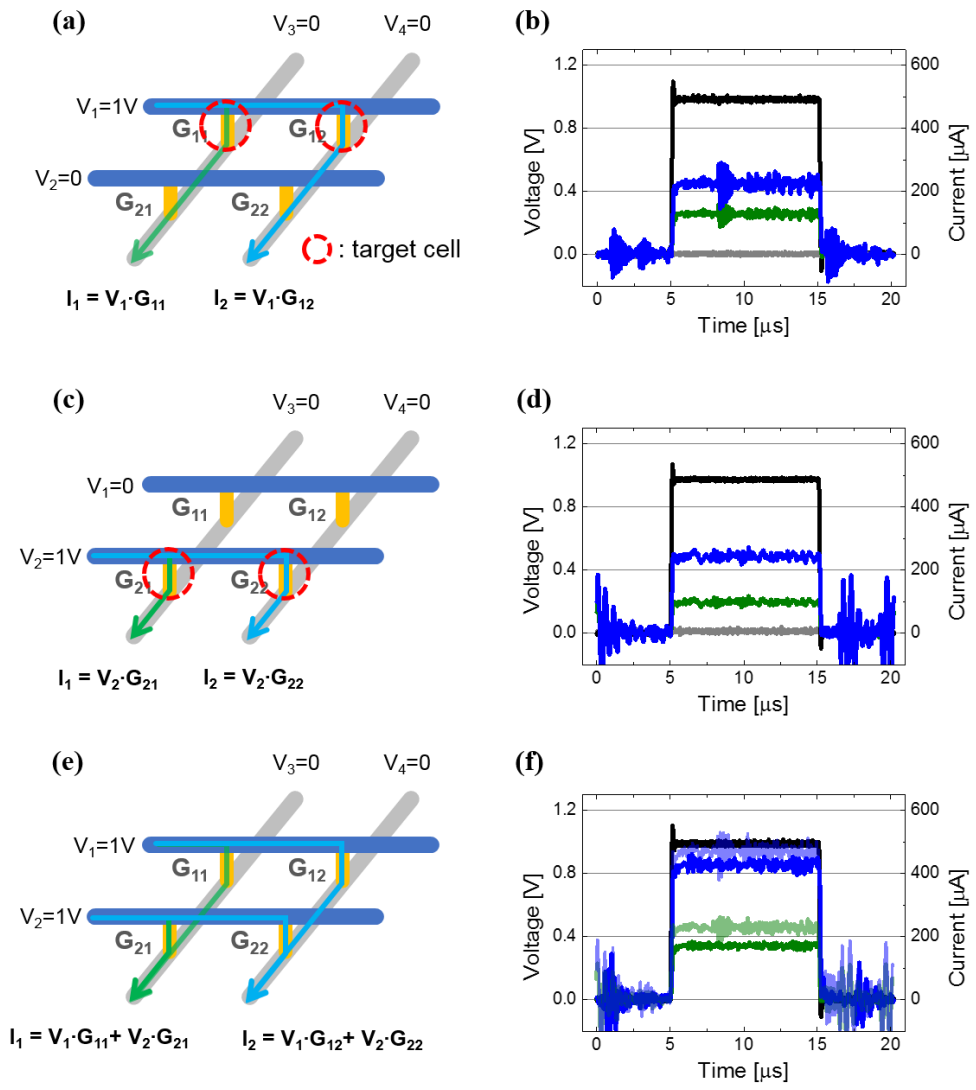


Fig. 3.10. Measurement for input voltage vector-conductivity matrix multiplication function of RRAM cross-point array. (a) Input voltage: (V_1, V_2) = (1 V, 0 V), (c) (V_1, V_2) = (0 V, 1 V), (e) (V_1, V_2) = (1 V, 1 V). (b), (d), (f) Output current by input pulses in (a), (c), (e), respectively.

Chapter 4

Application to Hardware Implementation of Artificial Neural Network

As the understanding of biological neural networks is deepened and various machine learning algorithms have been gradually developed from this, learning, memory, and inference abilities have been successfully imitated with the conventional computing system [53]-[54]. However, today's computing systems that have a serial memory architecture and are aimed at computing speed have a fundamental inconsistency in performing machine learning algorithms that require massive parallel processing. The inconsistency leads to a tremendous amount of power consumption in performing simple tasks such

as recognition of objects and voice [55]. Neuromorphic computing systems that model the structure and function of human brain neural networks at the hardware level have been studied in order to alleviate these problems [56]-[58]. Recently, researchers have successfully demonstrated that various artificial neural networks and their hardware implementations can perform tasks such as image pattern recognition [9], [59]. Among them, spiking neural network (SNN) is designed to emphasize the biological aspects of the human brain. It differs from the non-spiking networks in that spikes contain timing or frequency information. A representative artificial neuron model for SNN is the integrate-and-fire (I&F) model [60] and I&F type neuron circuit that implement the behavior of biological neurons have been proposed and developed in various forms. In the I&F type neuron circuit, charges are accumulated in the capacitor by time-dependent spikes and emit new pulses when the voltage across the capacitor exceeds a certain threshold. Meanwhile, two-terminal memory devices such as phase change memory (PCRAM) and

resistive random access memory (RRAM) [61]-[62], and three- or more terminal devices have been proposed and studied as synapse units [63].

4.1 Reinforcement Learning

Reinforcement learning (RL) algorithm is used in situations where the agent experiences the process of taking actions and observations under a certain policy and receiving a reward (e.g. a score in the game), and aims to find an optimal policy that maximizes the future reward by applying the Bellman equation which is the key algorithm. Recently, it has been reported that reinforcement learning algorithms allow machines to have the ability to outperform human expert in several computer games [64]. We trained a fully-connected 1-layer neural network with the RL algorithm to output the optimal selection in a given situation of “Rush Hour” game and convert the network representing the value function to the conductance levels of analog RRAMs.

In the reinforcement learning process, an action (A_t) having the maximum output value is selected through an inference, and an arbitrary action is selected according to a certain probability (ε). This action is reflected in the environment, and the next state (S_{t+1}) and appropriate reward (R_{t+1}) are given (Fig. 4.1). At first, there are many arbitrary attempts in the situation where the network does not understand the problem environment and goal, therefore, gives meaningless outputs. When the problem is solved by chance and a reward is given, the network gradually tries to make a choice to maximize the reward from the next trial.

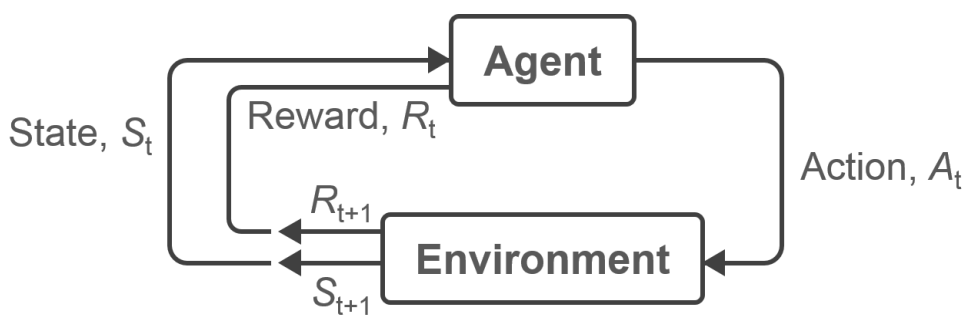


Fig. 4.1. Process of reinforcement learning. Agent and environment interact with each other through action and reward.

We consider a simple Rush Hour game as an example of a sequential problem that machines can have ability to solve like a human. In this game, several cars are arranged in a horizontal or vertical direction at 6×6 positions. The goal of this game is to move these cars effectively and escape the red car to the right exit with the least moves. The basic rules are that the car can only move in the 6×6 positions and to the empty space. Also, a horizontally placed car can only move horizontally, and a vertically placed car can only move vertically. Two example stages of this game are shown in Fig. 4.2. While an average adult will not take a minute to solve the problem of Fig. 4.2(a), the problem of Fig. 4.2(b) is quite complicated and not easy to figure out which car to move first.

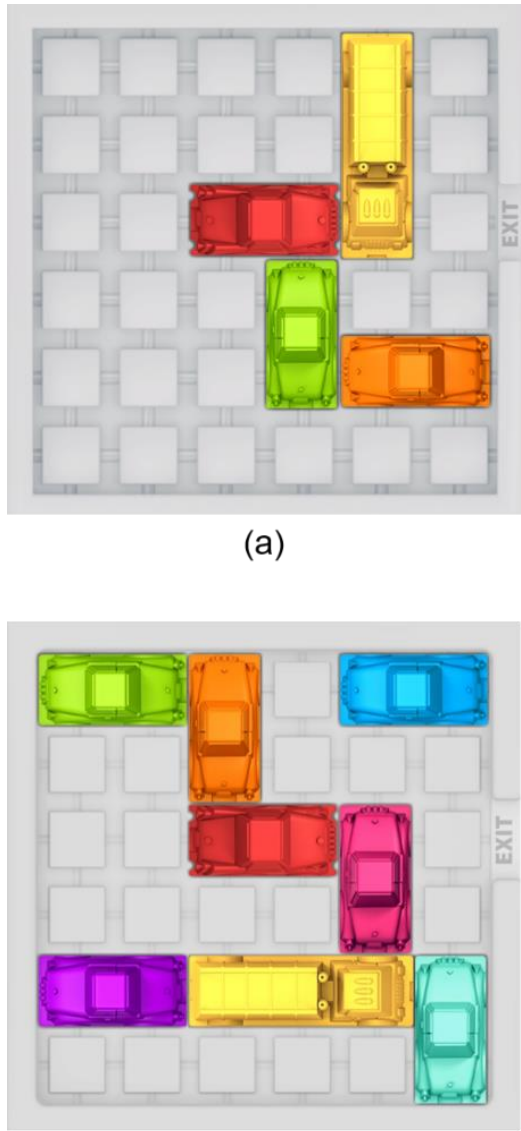


Fig. 4.2. Two examples of a sequential task: relatively (a) easy and (b) difficult Rush Hour game. The goal of the game is to get the red car out of the right exit with the least number of moves.

4.2 RRAM Based Spiking Neural Network

Fig. 4.3 shows the structure of the spiking neural network and two main parts that construct the hardware implementation of the network (An analog RRAM cross-point array and an integrate-and-fire neuron circuit). This artificial network has 288 inputs and 10 outputs, and 288×10 weight elements. 288 inputs represent each location of the game environment and the color of the cars (6×6×8). 10 outputs indicate the car number and the direction in which it can move (8+2). Input pulses have 2 μs width and 4 μs period. Fig. 4.3(b) shows analog RRAM cross-point array structure that performs the multiplication of the vector input and the conductance matrix efficiently in terms of time and energy, and that is known to be suitable for the hardware implementation of a fully-connected neural network [65]-[66]. An integrate-and-fire (I&F) neuron circuit consisting of inverters and current mirrors and showing characteristics similar to biological neuron has been proposed and demonstrated experimentally [67]. The overall structure of I&F neuron circuit

is shown in Fig. 4.3(c), which is divided into two parts: synaptic input integration part and spike (action potential) generation part. When a signal comes from the synapses having different conductance levels (G_1-G_4), the membrane capacitor (C_1) integrates the current signal like the soma part of biological neurons. When the membrane potential (V_{mem}) integrated at the capacitor exceeds a certain threshold, an output spike is generated discharging capacitor C_1. The experimental results and further explanations and can be found in Fig. 4.4 and [67].

So far, resistive memory devices having a variety of materials and structures have proven to show a steady and gradual resistance (conductance) level [68]-[69]. We have confirmed that RRAM devices with 7 nm thick SiN_x/SiO_2 structures show reliable and analog conductance changes over low current range. Several studies have been carried out on the reliable conductance change characteristics of these devices [70] and on the realization

of stable operation by suppression of internal overshoot current [52]. Further details on the structure and fabrication of the device can be found in [71].

Figs. 4.5(a)-(b) shows reliable conductance change characteristics of SiN_x-based RRAM obtained from two synaptic potentiation and depression operations. DC sweeps from 0 to 1 V show these RRAMs can have a number of conductance levels in a wide current range (Fig. 4.5(a)). In addition, unlike other metal-oxide-based RRAMs operating in the hundreds of μA [68]-[69], SiN_x-based RRAMs with a thin tunnel oxide layer can reliably operate in low current ranges from a few μA to tens of μA, which is advantageous characteristics in terms of energy consumption in large-scale array structures [52]. As shown in Fig. 4.6(b), pulses with 1.5 V amplitude, 2 μs width were applied and it was also confirmed that various conductance levels can be distinguished in the read operation. Figs. 4.6(a)-(b) show the reliability of this device for repeated read operations. The device does not show a read current (conductance) change at 2 V stress over 1 ms (Fig. 4.6(a)). Also, it is

confirmed that read current hardly changes even after 800 repetitive read operations (Fig. 4.6(b)).

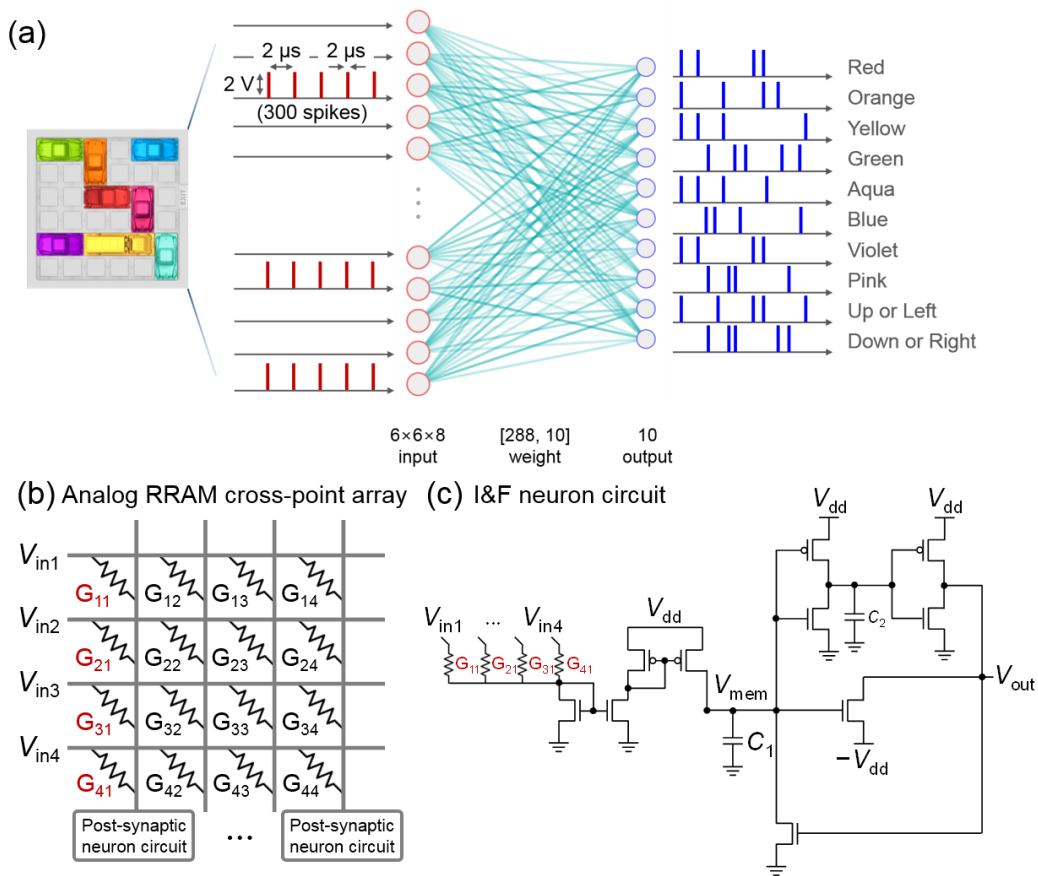


Fig. 4.3. (a) Structure of a spiking neural network and its hardware implementation with (b) cross-point array of analog RRAM synapses and (c) integrate-and-fire (I&F) neuron circuit.

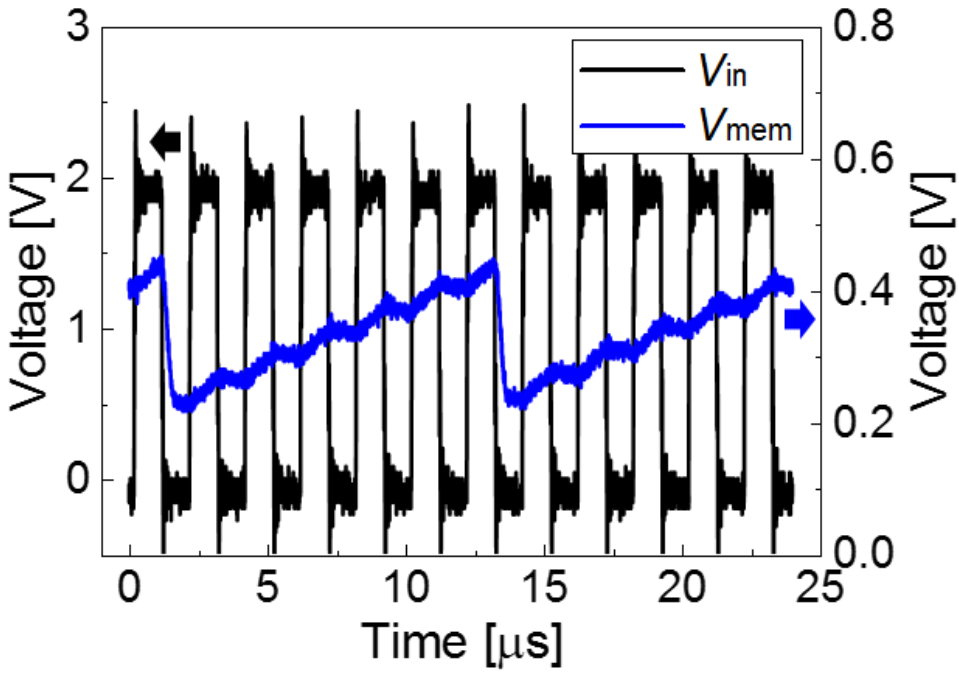


Fig. 4.4. Measured input voltage pulses (V_{in}) and membrane potential (V_{mem}) integrated at the capacitor (C_1). Reprinted from [68] with permission.

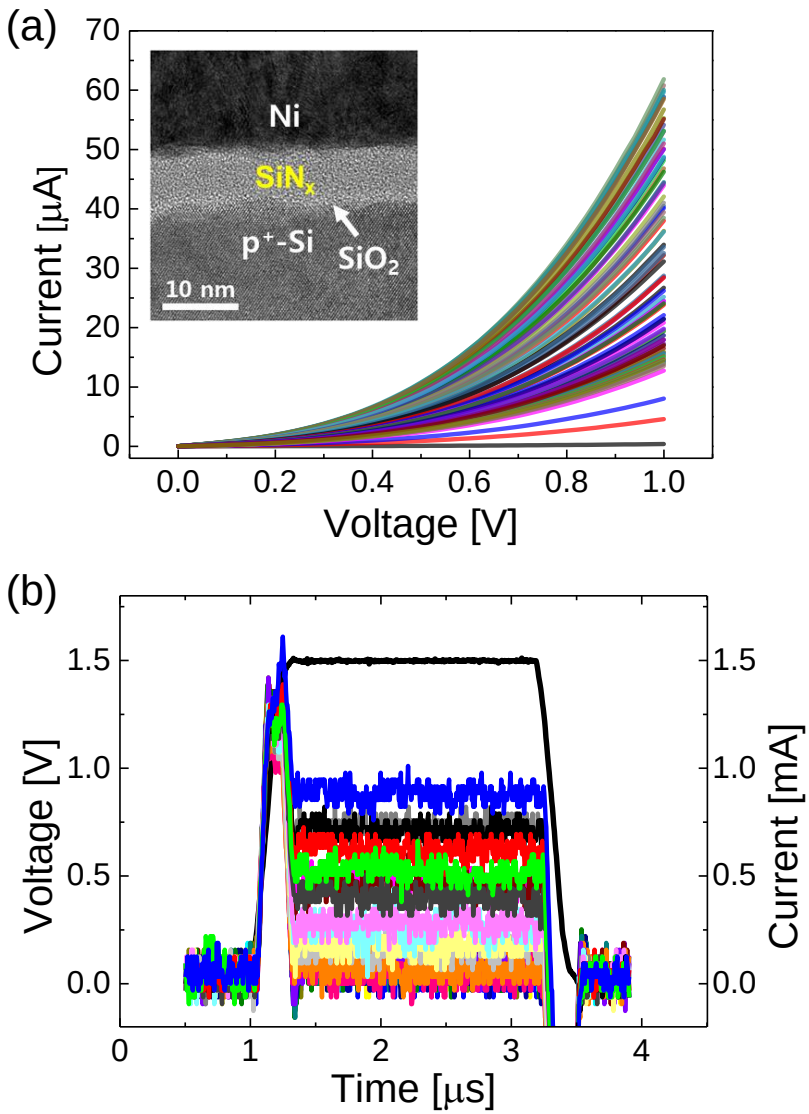


Fig. 4.5. Reliable and gradual conductance change characteristics of silicon nitride based RRAM. (a) DC I-V curves and (b) V-t and I-t waveforms of various conductance levels.

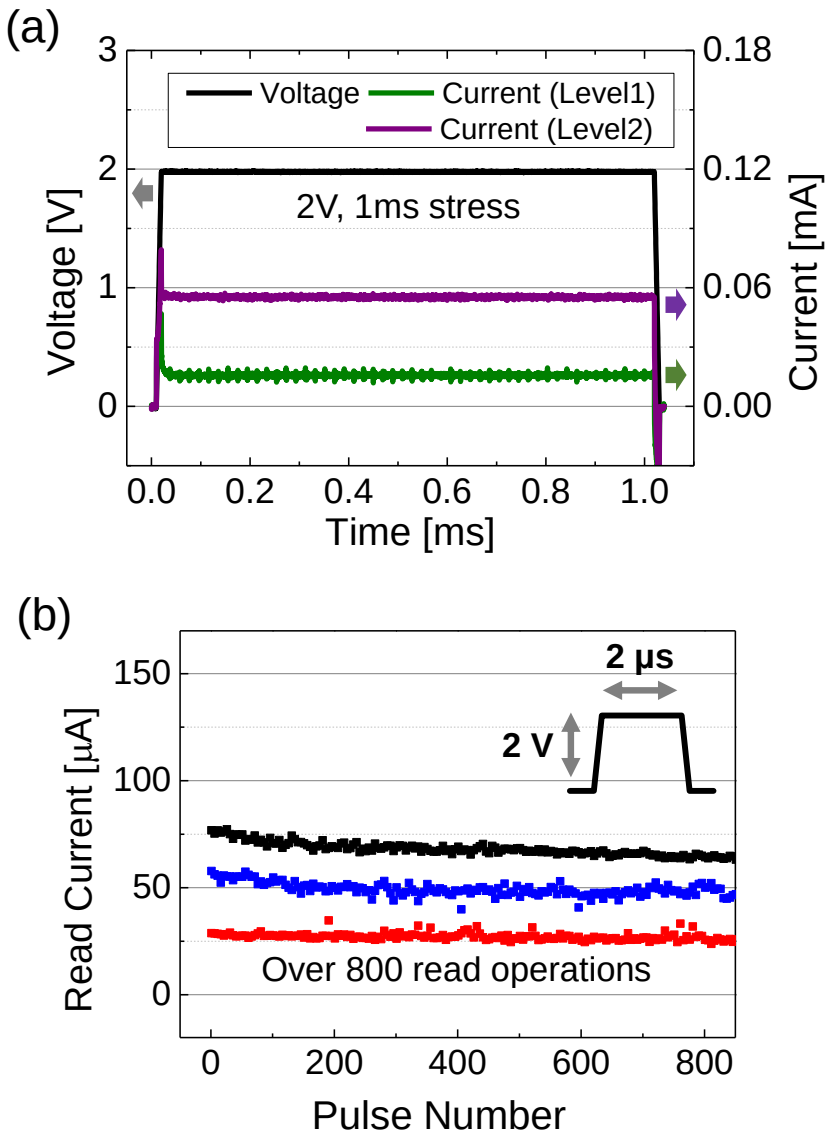


Fig. 4.6. (a) Stress test using 2 V amplitude, 1 ms width pulse and (b) read disturb test for over 800 read operations for different resistance states.

Fig. 4.7 shows how many moves of cars are required to escape the red car for each episode during the reinforcement learning process. At the beginning of the learning process, more than 2600 moves are usually required, and these attempts are quite arbitrary and change every time the network is learned. This result means that there have been a lot of attempts moving the car out of the given boundary, towards other cars in adjacent location, and moving meaninglessly. On the other hand, the red car can escape with minimum moves at the end of the learning process. This means that once learning is done, the network naturally acquires the rules of the game and the location of the cars, and consequently find the fastest way to get the red car out.

Fig. 4.7. Number of moves required to escape the red car during the reinforcement learning process.

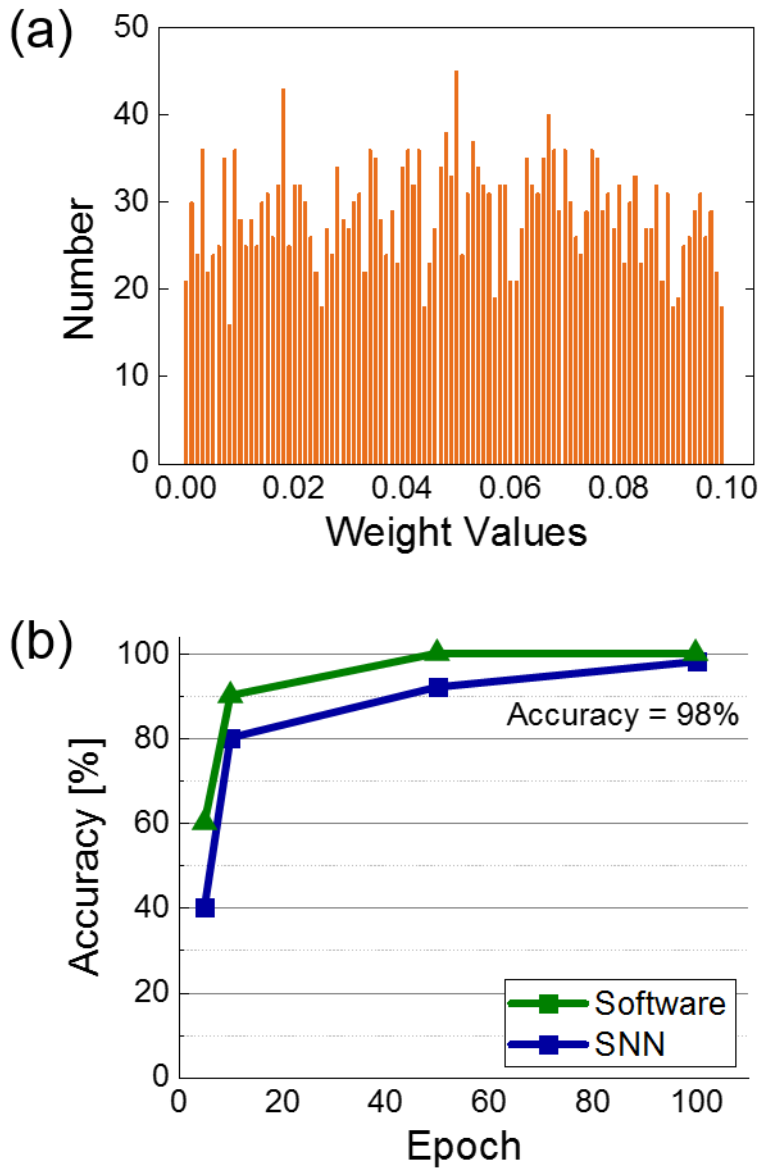


Fig. 4.8. (a) Distribution of 288×10 weight values in the trained neural network after 100 epochs. (b) Accuracy test for 300 training samples and 50 test samples over 100 epochs (Green: Software, Blue: SNN).

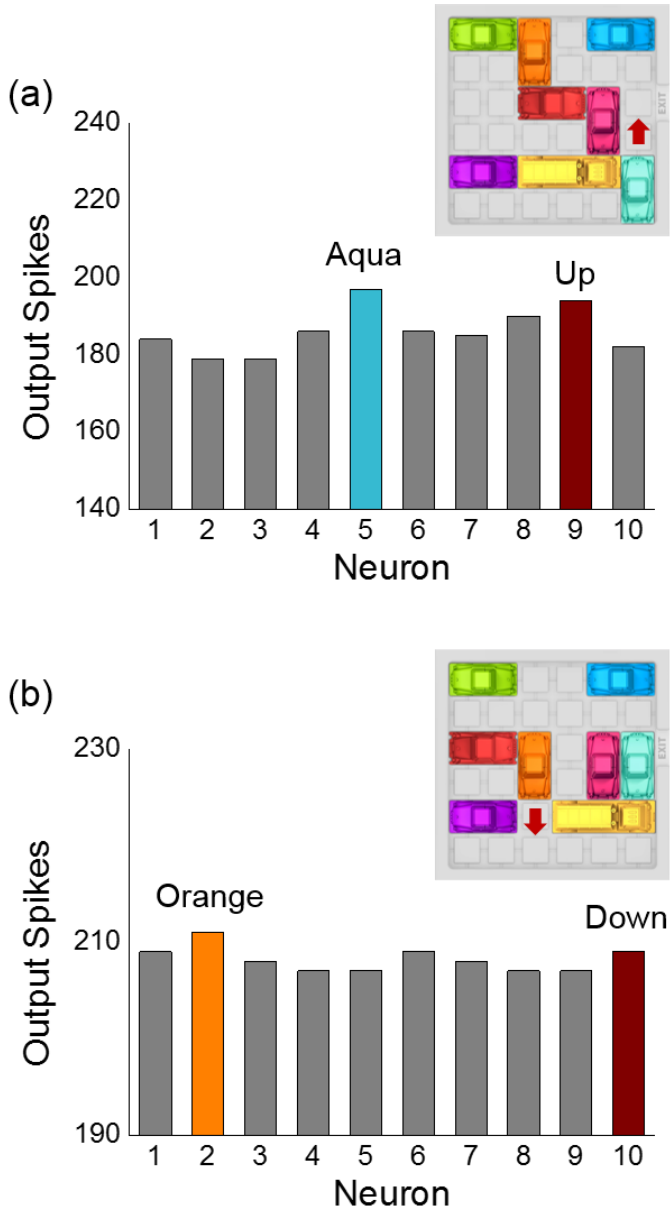


Fig. 4.9. Number of output spike from the trained spiking neural network for (a) the initial state and state after seven steps of Rush Hour game.

As shown in Fig. 4.8(a), weight values obtained from this whole learning process range from 0 to 0.1. These values can be mapped to analog conductance levels matching the characteristics of resistive memory-based synaptic devices as shown in Fig. 4.5. We made 300 training samples and 50 test samples in consideration of various situations caused by moving cars from the example problem of Fig. 4.2(b). Fig. 4.8(b) shows the results of accuracy test for 100 epochs. In system-level simulations, it was confirmed that the spiking neural network that is transferred the exact synaptic weights (conductance levels) from the result of software training have the ability to solve the sequential problem with least moves. When tested for 50 samples, 98 % accuracy was obtained after 100 epochs.

Figs. 4.9(a), (b) show the number of output spikes by the spiking neural network when each state of the Rush Hour game is received as an input. In the first state of a given problem (Fig. 4.9(a)), neuron 5 and 9 output the spikes with the highest frequency, and thus moving the aqua car upward is the

optimal choice. Likewise, moving the orange car downward is the best choice in the state after seven steps (Fig. 4.9(b)). Following these actions, the red car can escape after 14 steps in the end.

The size of the network can be increased or decreased depending on the input or output encoding method. Comparing the result of 20 accuracy tests for different input encoding methods, one-hot and binary encoding methods are almost the same, but the analog input leads to significant loss of accuracy (Fig. 4.10). These results suggest that the hardware implementation of artificial neural network requires optimization in terms of accuracy, area, and energy consumption.

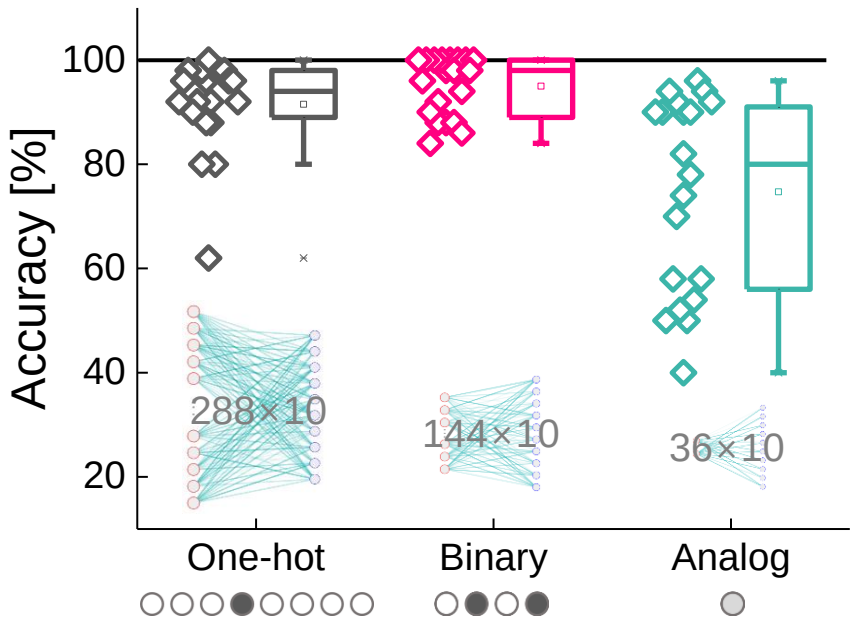


Fig. 4.10. Accuracy test from software training according to various input encoding method (One-hot vs binary vs analog encoding).

So far, we have confirmed the operation of a hardware spiking neural network that provides the optimal action for each of various states in Rush Hour game. This network with analog conductance values can also learn and solve problems that have different levels of difficulty and number of cars.

However, the size of the network may need to be adjusted depending on the conditions and the difficulty of the game.

In this chapter, we have shown that a spiking neural network consisting of a cross-point array with analog RRAM synapse devices and I&F neuron circuits can solve the sequential problem through reinforcement learning. We present the gradual and reliable characteristics of silicon nitride based analog RRAMs that operate in the current range of less than 60 μA, guaranteeing low power operation possibilities. In the reinforcement learning process, we have confirmed that the network has gradually gained the ability to solve the problem with the change of 288×10 synaptic weights, and these values are mapped to conductance levels of the resistive memory based hardware synaptic element. This work demonstrates that the problem-solving abilities of reinforcement learning algorithms can be implemented with energy-efficient hardware spiking neural network.

Chapter 6

Conclusions

In this dissertation, a silicon nitride-based RRAM is fabricated and the electrical characteristics of the devices are verified. Resistance change of the two terminal resistive memory devices through voltage application is confirmed and various electrical characteristics such as abrupt/gradual resistance switching and switching speed are analyzed. Effect of the additional insertion of thin silicon oxide tunnel barrier layer on the operating characteristics is confirmed and investigated. In this process, it is confirmed that the overshoot current flowing into the device can be suppressed, thereby

improving the uniformity of the device operation. I also propose and validate a circuit model of a resistive memory device that can be used for circuit-level simulation regardless of material and structure.

A resistive switching memory array with device area on the order of tens of nanometers is fabricated and verified its electrical characteristics. In this experiment, an anisotropic wet etching process is applied at room temperature to refine the silicon bottom electrode into a nanoscale wedge structure. In addition, it is confirmed that the operating voltage and energy consumption decrease in the resistance switching operation as the device area decreases.

By taking advantage of the vector-matrix multiplication function of the cross-point array structure using analog resistance switching memory as an artificial synapse, it is confirmed that the structure and problem solving ability of the artificial neural network obtained through software machine learning can be implemented with energy efficient hardware neural network.

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초 록

최근 빅데이터에 기반한 기계학습 알고리듬의 급격한 발전으로 인간 뇌 신경망의 동작을 모방하는 적용 분야가 점차 확대되고 있다. 하지만 현재 널리 사용되는 폰 노이만 구조의 연산 시스템은 뇌 신경망의 매우 병렬적인 구조와 낮은 에너지 소모를 구현하는 하드웨어로서 내재적인 부조화를 가지고 있다. 따라서 인간의 훌륭한 학습, 기억, 추론, 판단 등의 기능을 인공적으로 실현하기 위해서 궁극적으로 하드웨어 수준에서의 근본적인 변화가 요구되고 있다. 한편, 최근 수십 년간 눈부신 발전을 이루어 온 실리콘 기반의 반도체 소자와 집적회로 제작 기술은 이러한 변화의 요구에 부응하는 가장 적합한 기술로 여겨지며 학계와 산업계에서 활발한 논의가 이루어지고 있다.

본 논문에서는 실리콘 질화막 기반의 저항 변화 메모리를 제작, 소자의 전기적 특성을 확인하며 그 활용에 대해 연구하였다.

우선 개별 소자 단위에서 전압 인가에 의한 두 단자 메모리 소자의 저항 변화 현상을 확인하고 다양한 전기적 특성을 확인하였다. 나노 수준의 얇은 실리콘 산화막의 추가 형성이 저항 변화 메모리 소자의 동작 특성에 미치는 영향을 확인하고 분석하였다. 이 과정에서 소자 내부로

흐르는 오버슛 전류가 억제되어 소자 동작의 균일성 개선에 영향을 줄 수 있음을 확인하였다. 또한 물질과 구조에 관계없이 회로 수준의 시뮬레이션에 사용할 수 있는 저항 변화 메모리 소자의 회로 모델을 제안하고 검증하였다.

어레이 단위에서 수십 나노 미터 수준의 면적을 갖는 저항 변화 메모리를 제작하고 전기적 특성을 확인하였다. 이 과정에서 비등방성 습식 식각 공정을 상온에서 적용하여 단결정 실리콘 하부 전극을 쐐기 구조로 미세화하고, 소자 면적의 감소에 따라 저항 변화 동작에서 동작 전압과 소모 에너지가 감소함을 확인하였다.

다단계의 전도도를 갖는 저항 변화 메모리를 인공 시냅스로 사용하는 교차점 어레이 구조의 벡터-행렬 곱 연산 기능을 활용하여, 소프트웨어 기계 학습을 통해 얻은 인공 뇌신경망의 구조와 문제 해결 능력을 에너지 효율적인 하드웨어로 구현할 수 있음을 확인하였다.

주요어 : 저항 변화 메모리, 다단계 전도도를 갖는 시냅스 소자, 교차점 어레이, 뉴로모픽 시스템, 인공 뇌신경망.

학번 : 2013-20758

List of Publications

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