Ph.D. Dissertation

Quadrature Resonant Clock with Frequency Tuning Capacitor and Amplitude Control Feedback Loop

주파수 보정과 진폭 조절 피드백 루프를 포함한
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Quadrature Resonant Clock with Frequency Tuning Capacitor and Amplitude Control Feedback Loop

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Abstract

This thesis presents a quadrature resonant clock generator for driving four 4.3-mm load wires with tuning capacitors and an amplitude control feedback loop. By using frequency tuning capacitors, which reduce the mismatch in operation and LC resonant frequencies, the proposed clock generator offers power reduction by 20-25% compared with conventional CMOS clock driver and by 23-34% compared with conventional CML clock driver over a wide voltage swing. The amplitude control feedback loop, which determines the bias current of the negative gm cell, maintains the constant optimized clock swing over wide PVT variations. Measurement result from the prototype chip fabricated in 65 nm CMOS shows that total power consumption of the proposed quadrature resonant clock is 11.92 mW in 7-GHz operation with four 559-fF load wire capacitances. Measured period jitter is 573.6 fs_{rms} and phase noise at 1MHz offset is -138.37 dBc/Hz.

Keywords : Amplitude control feedback loop, clock distribution, frequency tuning, injection locking oscillator, quadrature resonant clocking.

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Chapter 1

Introduction

1.1 Motivation

As the technology develops and shrinks, two important challenges in designing high performance integrated circuit (IC) are to reduce power consumption and to extend the data bandwidth. In particular, considering the market expansion of the mobile devices including tablet devices, wearable devices such as augmented reality (AR) and virtual reality (VR) machines, and internet of things (IoT), low power IC design is very important since the limited battery size and hence the weight of the mobile devices can be proportionally decreased. Furthermore, as shown in the Figure 1.1, in power-hungry data centers for telecommunications, storage systems cloud services, cooling cost could reach 50% of the total energy consumption due to energy loss of the integrated circuits [1] -[4] .

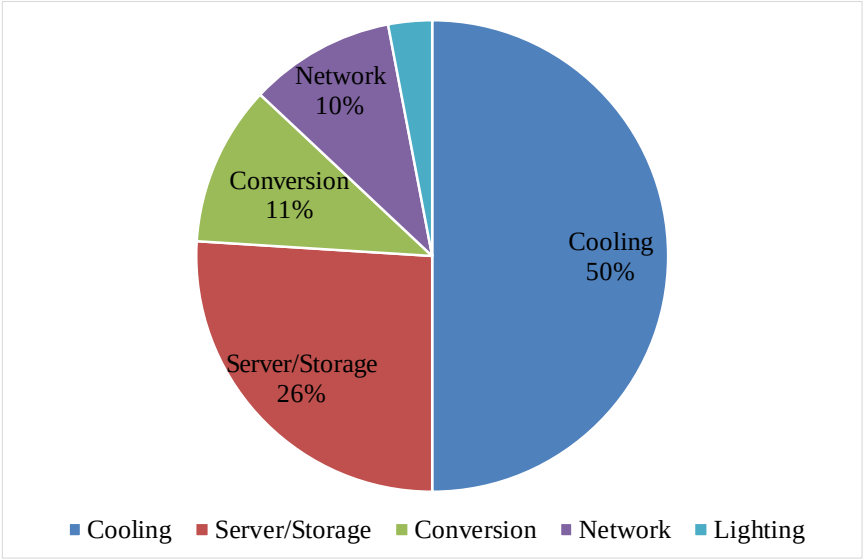

Figure 1.1. Typical data center energy consumption.

Meanwhile, in order to extend the data bandwidth, the frequency of the clock used in the system must also be increased or multi-rate clock system such as quadrature clocking should be used. However, the conventional clock distribution system typically takes up 15-40% of the power consumption of the entire chip [5] -[8] . In general, the conventional clock trees are composed of the complementary metal–oxide–semiconductor (CMOS) or current-mode logic (CML) type clock repeaters which are the easiest and simplest method of the clock distribution system. However, the CMOS type clock repeaters have the disadvantage that there is a bandwidth limitation, and the CML type clock repeaters have the disadvantage that it consumes a lot of power. Therefore, the resonant clocking, one of the methods to reduce clock tree power consumption, has been studied and applied in very-large-scale integration (VLSI) systems [7] -[35] .

Generally, most of the resonant clocking applications are constructed using wire parasitic capacitors with fixed value inductors [7] -[30] . LC resonance between the parasitic capacitors and the inductors is used to reduce the power consumed in the clock switching process. In those cases, which is using fixed value inductors for LC resonance, a mismatch between the resonant frequency and the operation frequency which is the intended target frequency of the output clock may occur due to PVT variations. If there is a significant difference between the two frequencies, the LC tank can be degenerated as a passive load rather than a resonator, which increases power consumption. Thus, a tuning mechanism must be incorporated to fully optimize the performance especially in a varied frequency range. One way to solve this problem is to use two or more inductors to change the resonant frequency using a switch for selection [31] -[35] . However, this method also suffers from the additional power consumption due to the series resistance of the switch which degrades Q of the resonator. In addition, there is also a mode control issue when the inductor is switched and the operating mode is changed.

To solve these problems, the proposed quadrature resonant clock uses a frequency tuning capacitor in the LC oscillator. The operation and resonant frequencies are matched by using a frequency tuning capacitor in a phase-locked loop (PLL) during power-up. In that way, the best power reduction can be achieved over a wide operation frequency. In addition, the quality of the clock, such as phase noise, is improved as well when there is less frequency mismatch. Also, the proposed resonant clock is implemented by quadrature to provide four-phase clock in quarter-rate systems.

1.2 Thesis Organization

This thesis is organized as follows. In Chapter 2, background information about the quadrature resonant clocking scheme is described. The features, design issues, advantages and the disadvantages of the prior works which are the basic conventional resonant clocking scheme, standing-wave oscillator, resonant clocking scheme using inductor tuning are organized and discussed. Also, the basic concept of the proposed quadrature resonant clocking scheme is briefly introduced followed by the basic theory of the injection-locked oscillator and LC quadrature oscillator. The phase domain response of the injection-locked oscillator and the bi-modal operation of the LC quadrature oscillator is analyzed briefly.

In Chapter 3, the proposed quadrature resonant clocking scheme is described. The overall architecture of the proposed quadrature resonant clocking scheme is depicted and functionality is explained. Then, the design method of the clock distribution wire is analyzed using RC ladder model of the wire and Q factor calculation. Design of the LC quadrature oscillator core including negative gm cell, quadrature coupling cell and delay cell preventing bi-modal operation is described followed by the explanation about two feedback loops – frequency control loop and amplitude control loop. In the last section of the Chapter 3, two types of the injection cell are described with some simulation results.

In Chapter 4, the measurement results of the prototype chip are presented. The power consumption of the proposed quadrature resonant clocking scheme is measured, and compared with the power consumption of the two types of the conventional clock

distributing methods. By using the amplitude monitoring circuit, the waveform of the internal output clock is measured. Also, the phase noise, jitter of the output clock is measured. And phase error of the quadrature clock is measured. At the end of the Chapter 4, the proposed quadrature resonant clocking scheme is compared with the prior works of conventional resonant clocking scheme, and summarize the advantages of the proposed scheme.

Finally, Chapter 5 summarizes the proposed works and concludes this thesis.

Chapter 2

Background on Quadrature Resonant Clock

2.1 Overview

In recent years, As the mobile device market expands, the need for low-power circuit design is increasing. Furthermore, the frequency of clocks used in VLSI systems is getting faster and faster. In this situation, distribution of high quality, high frequency clocks to the entire local systems has become a very important factor in determining the performance of the VLSI system. One of the methods of distributing clocks to the local system is using CMOS or CML type clock repeaters or using buffers in the middle of the loading wire as shown in the Figure 2.1 and Figure 2.2. However, using conventional repeaters as a method for distributing high frequency clocks

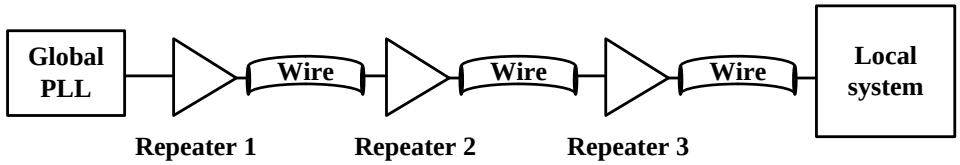

Figure 2.1. Clock distribution scheme using repeaters.

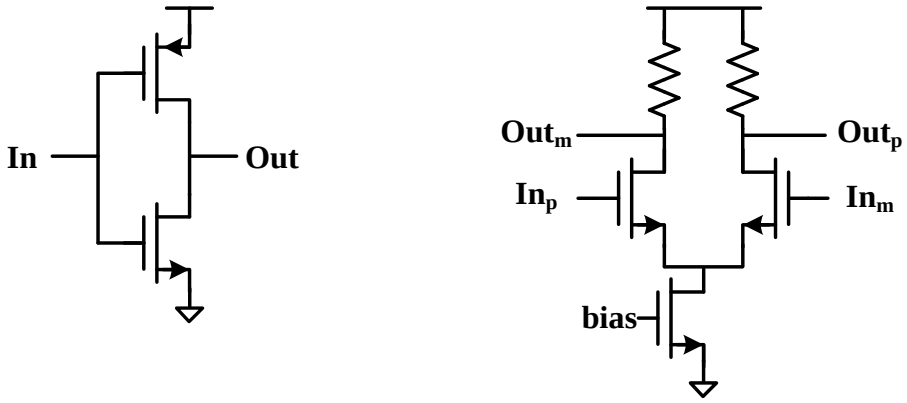

Figure 2.2. CMOS and CML type buffer.

has some problems. One is bandwidth limitation and the other is that buffers consume too much power. Furthermore, the circuit that consumes a lot of power is vulnerable to supply noise, so the quality of the clock such as jitter and phase noise deteriorates and the performance of the entire circuit is also deteriorated when using conventional CMOS or CML based repeaters.

To solve the problems of consuming too much power, the resonant clocking, one of the powerful methods to reduce clock distribution power consumption, has been studied for a long time. However, the conventional resonant clocking scheme has

frequency mismatch problem. Therefore, to solve this frequency mismatch problem, the quadrature resonant clocking scheme using resonant frequency tuning capacitor is proposed in this thesis.

In this chapter, before explaining the proposed quadrature resonant clocking scheme in the later chapter, conventional resonant clocking scheme is firstly described followed by an explanation about the scheme using multiple inductors. And proposed quadrature resonant clocking scheme and basic theory of injection-locked oscillator and LC quadrature oscillator is described in the later sections.

2.2 Prior Works

2.2.1 Basic Resonant Clocking Scheme

The most basic and simplest resonant clocking scheme which is conventionally used to reduce the clock tree power consumption is shown in the Figure 2.3. A simple resonant clocking scheme is a structure in which an inductor considering the operating frequency and wire parasitic capacitance values is added to the clock tree structure using the basic clock buffers. This simple structure can be found in [7] -[23] and [25] -[27] , and it can be confirmed that many processors are used this structure to reduce the power used for clock distribution.

The basic principle of resonant clocking to reduce power consumption is as follows. As the resonance occurs in the LC tank, the impedance at the buffer output stage decreases which is shown in the Figure 2.4, so the clock can be distributed using less power. In this structure, the ratio of the reduced power is determined by the value of the Q factor of the entire load wire and inductor. For example, when the Q factor of the load wire and the entire inductor is 3, the power consumption is reduced to a third when the resonant clocking scheme is used compared to when the resonant clocking scheme is not used. Therefore, proper wire and inductor design that determines the overall Q factor is an important factor in determining the performance of resonant clocking.

However, this simple structure has a fatal problem. In a situation where the resonant frequency determined by the load wire parasitic capacitance and the inductance

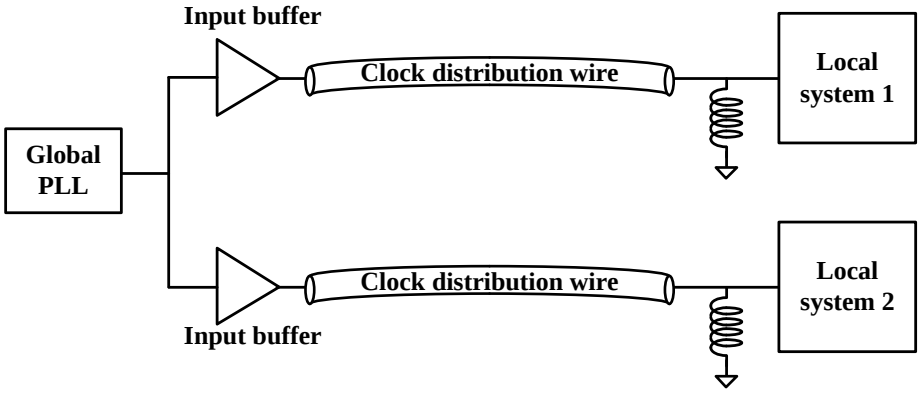

Figure 2.3. Block diagram of the basic resonant clocking scheme.

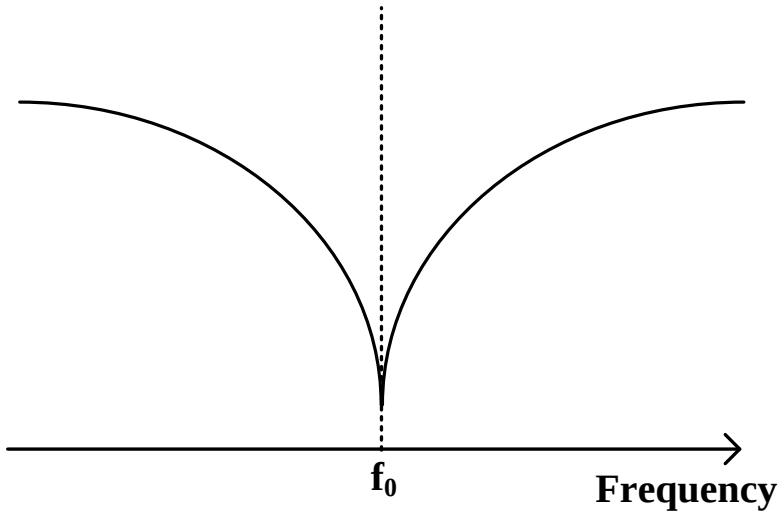

Figure 2.4. Impedance of LC tank

and the actual operating frequency of the system are different, the impedance at the buffer output stage is larger than the target value, so power consumption cannot be sufficiently reduced. Therefore, this basic structure is vulnerable to process mismatch and is not suitable for applications having a wide frequency range in which the operating frequency is not set to a single value.

Therefore, a resonant clocking structure using multiple inductors has been studied to solve these problems and apply a resonant clocking scheme to applications having a wide frequency range.

2.2.2 Standing-Wave Oscillator

The standing-wave oscillator, a type of resonant clocking scheme, is implemented as distributed oscillator, with gain elements such as cross-coupled inverters uniformly spaced throughout the clock network in order to overcome losses [28] -[30] . The basic resonant clocking scheme in Figure 2.3 is mainly used with H-tree to distribute clocks to the local sectors, whereas standing-wave oscillators are mainly used for global clock distribution. Therefore, as shown in Figure 2.5, the standing-wave oscillator is designed in such a way that the inductor is connected to the ring-shaped distribution wire or the mesh surrounding the entire chip. In general, the length of the clock distribution wire is very long, so it is important to arrange the inductors uniformly and well.

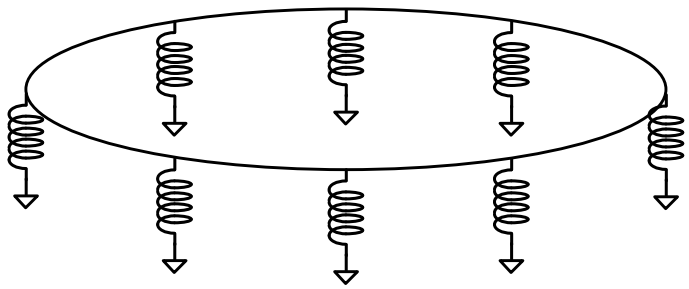

Figure 2.5. Basic structure of the standing-wave oscillator.

2.2.3 Resonant Clocking Scheme Using Multiple Inductors

The basic resonant clocking scheme using only one inductor has a problem that power consumption cannot be effectively reduced when the resonant frequency and operation frequency are different. If there is a significant difference between the two frequencies, the LC tank can be degenerated as a passive load rather than a resonator, which increases power consumption. One way to solve this problem is to use two or more inductors to change the resonant frequency using a switch for selection as shown in the Figure 2.6. This structure using multiple inductors is mainly used for to applications having a wide frequency range [31] -[35] because the clock distribution power consumption can be effectively reduced over a wider range than the basic resonant clocking method.

The principle of resonant clocking scheme using multiple inductors is to tuning the resonant frequency by changing the inductance in the LC tank. If one of the multiple inductors can be selected and used according to the situation, an inductor suitable for the operation frequency is selected. Since the resonance frequency is inversely proportional to the inductance, a larger inductor is used in the low frequency region and a smaller inductor is used in the high frequency region. At least one switch per inductor must be added to make this selection when compared to the basic resonant clocking structure.

However, the method of using these multiple inductors also has some problems. First, because a limited number of inductors cannot cover all the ranges, there is inevitably a frequency range that cannot optimize the reduction of clock tree power.

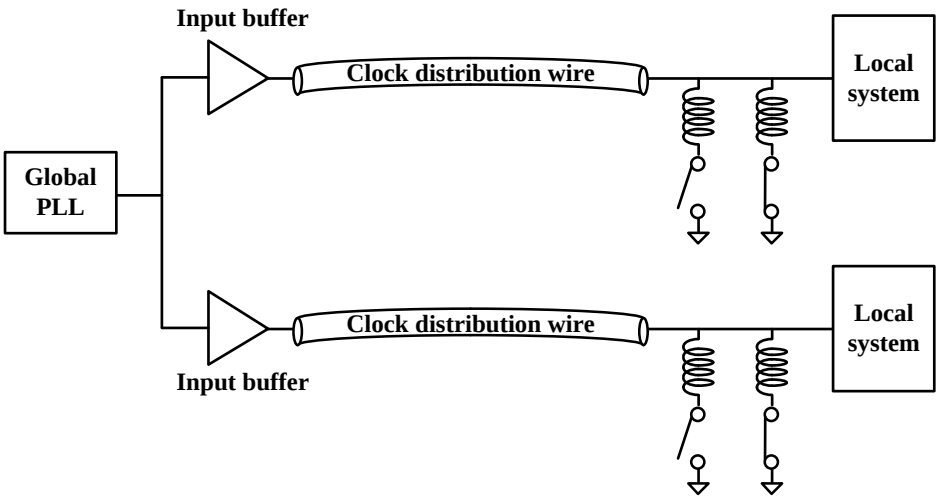

Figure 2.6. Block diagram of the basic resonant clocking scheme using multiple inductors.

Therefore, being vulnerable to process mismatch is the same as the basic resonant clocking scheme. Also, as the switch is used, the parasitic resistance component of the switch deteriorates the overall Q factor, which results in increased power consumption. In addition, the use of multiple inductors requires a large area, which is a problem of increasing the cost required to manufacture an IC.

Eventually, the method of tuning the resonant frequency by changing the inductance has problems due to the limitation of the characteristics of the inductor. Therefore, the method of tuning the resonant frequency by changing the capacitance of the LC tank is more suitable for the resonant clocking scheme.

2.3 Concept of the Proposed Quadrature Resonant Clock with Frequency Tuning Capacitor

As discussed in the previous sections, there are problems with existing resonant clocking designs. In the case of a design using one inductor, the impedance of the LC tank cannot be optimized when a difference occurs between the resonant frequency and the operation frequency. Therefore, it can be effectively operated only at one specified operation frequency and cannot be applied to applications with a wide frequency range. There is also the problem of being vulnerable to process mismatch affecting resonant frequency.

Even if you try to solve this problem by using multiple inductors, some problems that worsens the performance of resonant clocking still remain. The use of a finite number of inductors does not cover a continuous frequency range. There is also an optimization problem depending on the control method at the boundary of modes depending on which inductor is used. In addition, the series resistance of the switch used to selectively use the inductor exacerbates the Q factor, thereby increasing the power consumption used for clock distribution. In addition, there is a problem with too large an area caused by using multiple inductors.

In this thesis, as shown in the Figure 2.7, we propose a resonant clocking scheme that minimizes the difference between the operation frequency and the resonant

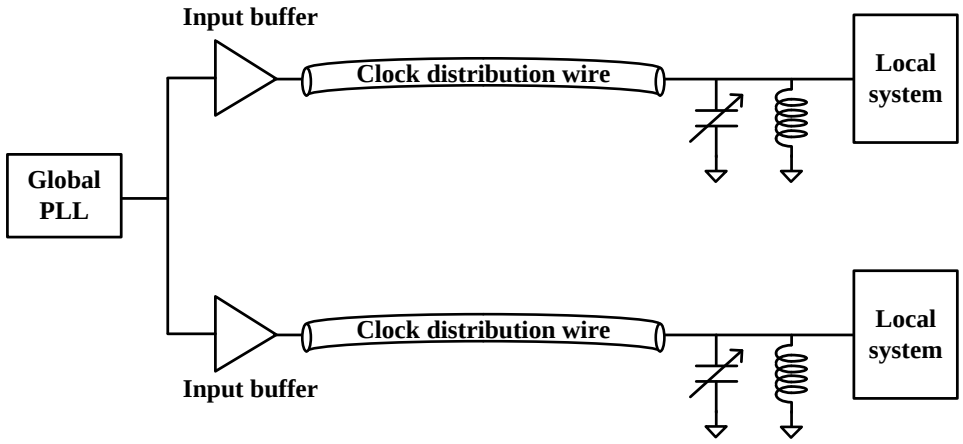

Figure 2.7. Basic concept block diagram of the resonant clocking scheme using frequency tuning capacitor

frequency by controlling the resonant frequency using a frequency tuning capacitor. Using this method, the resonant frequency can be adjusted to an appropriate value in a wide operating frequency range while using one inductor. Therefore, it is possible to obtain an optimized power reduction effect in all frequency ranges, cope with mismatches, and also have the advantage of not occupying a large area.

Additionally, the proposed quadrature resonant clocking scheme includes a feedback loop to control the amplitude of the output clock, thereby adjusting the amplitude change caused by the frequency tuning process and PVT variations to an optimized value. Detailed structural descriptions and details of circuit design and analysis related to Q factor are covered in later sections.

2.4 Injection-Locked Oscillator

2.4.1 Similarity Between the Resonant Clocking and the Injection-Locked Oscillator

The basic resonant clocking scheme which is shown in the Figure 2.3, consists of an input buffer, the load wire, and an inductor added for LC resonance. Considering that the load wire can be regarded as an RC lumped model, the structure of the load wire and the inductor can be said to be the same as that of the LC tank of the LC oscillator. Therefore, in the same way as the LC oscillator, the resistance component of the LC tank can be canceled by using a negative gm cell in the resonant clocking scheme. In addition, it can be considered that the input buffer of the basic resonant clocking scheme plays the same role as the injection cell used for the injection-locked oscillator (ILO). This similarity between the resonant clocking scheme and the ILO can be confirmed by the Figure 2.8 and the Table 2.1. Therefore, the design and the analysis method of ILO such as injection cell design, injection strength, injection locking range and phase domain response can be used to design and analyze the resonant clocking scheme.

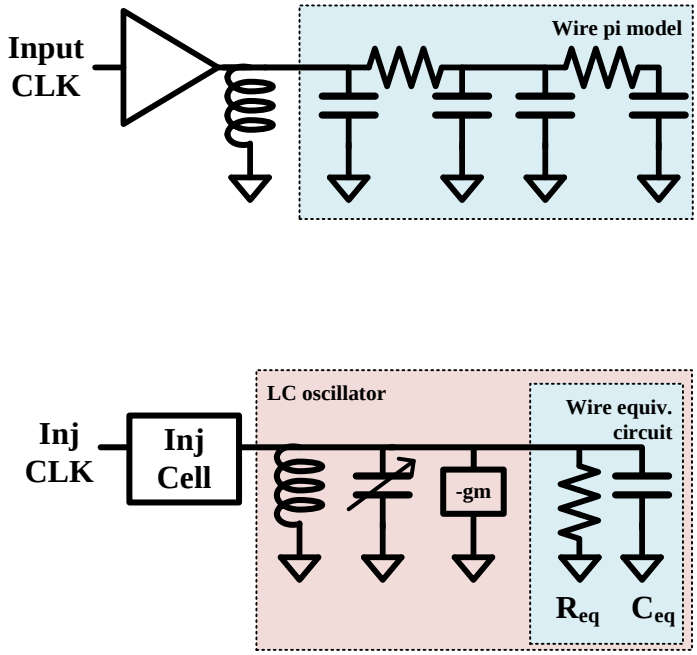

Figure 2.8. Similarity between resonant clocking scheme and ILO.

Table 2.1. Comparison between resonant clocking scheme and ILO.

Resonant clock	**ILO**
Input clock	Injection clock
Input buffer	Injection cell
Wire parasitic cap	Cap bank

2.4.2 Basic Principles of the Injection-Locked Oscillator

The first observed injection locking phenomenon is two pendulums moving synchronously when only the pendulums tied on the same bar close to each other. Adler defined the relationship between an injection signal and a free running oscillator, and behavior of an injection pulling. Razavi rewrote the relationship and presented about a locking range and a phase noise, etc.

The injection-locked oscillators are widely used in clock generators as shown in the Figure 2.9, Figure 2.10, Figure 2.11. The injection-locked frequency divider (ILFD) replaces the divider in PLL which operates at high frequency and consumes a lot of power. The injection-locked frequency multiplier (ILFM) is the one of the solutions to generate local oscillators in millimeter-wave band. The injection-locked clock multiplier (ILCM) can improve the performance of PLL.

The most basic parameters of the ILO are injection strength and locking range. In the case of the basic LC oscillator with injection shown in the Figure 2.12, for an example, the injection strength and single side locking range are defined as follows.

$$injection\ strength = \frac{I_{inj}}{I_{osc}} \tag{2.1}$$

$$\begin{aligned} locking\ range &= \frac{\omega_0}{2Q}\frac{\frac{I_{inj}}{I_{osc}}}{\sqrt{1-\left(\frac{I_{inj}}{I_{osc}}\right)^2}} \\ &\approx \frac{\omega_0}{2Q}\frac{I_{inj}}{I_{osc}} \end{aligned} \tag{2.2}$$

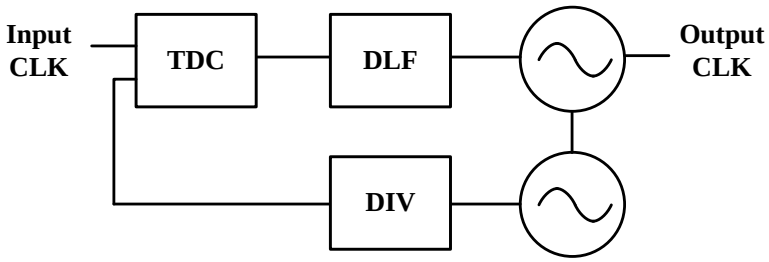

Figure 2.9. Injection-locked frequency divider.

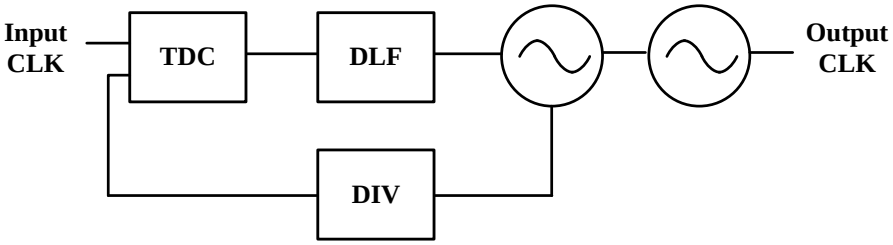

Figure 2.10. Injection-locked frequency multiplier.

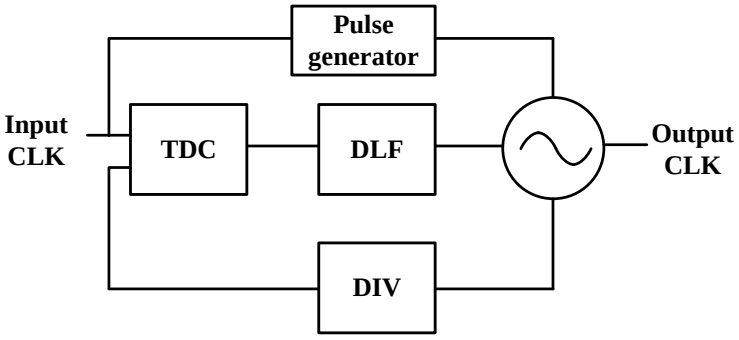

Figure 2.11. Injection-locked clock multiplier.

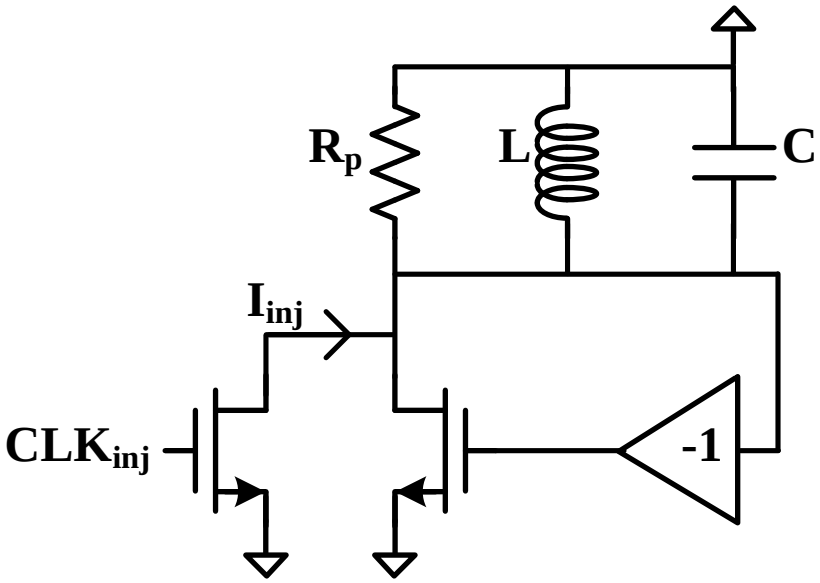

Figure 2.12. Basic LC oscillator with injection.

2.4.3 Phase Domain Response

The locking range of previous section is suitable only for the LC oscillator with sinusoidal wave injection, sinusoidal output not for the other types of oscillator such as ring oscillator and the ILO with pulse type injection. The analysis, based on the impulse sensitivity function (ISF) and phase domain response (PDR), make it possible to define the lock range more easily.

The phase of the output clock changes due to the effect of injection, and the amount of change depends on when injection is performed. PDR is a function of the relative phase of injection ϕ and shows the changed phase of the output clock as shown in the Figure 2.13. Considering the PDR curve in the Figure 2.14, the locking range can be defined as follows.

$$locking\ range = \frac{\omega_0(P_{max} - P_{min})}{2\pi N} \tag{2.3}$$

Where the N is frequency ratio between operation frequency and injection frequency.

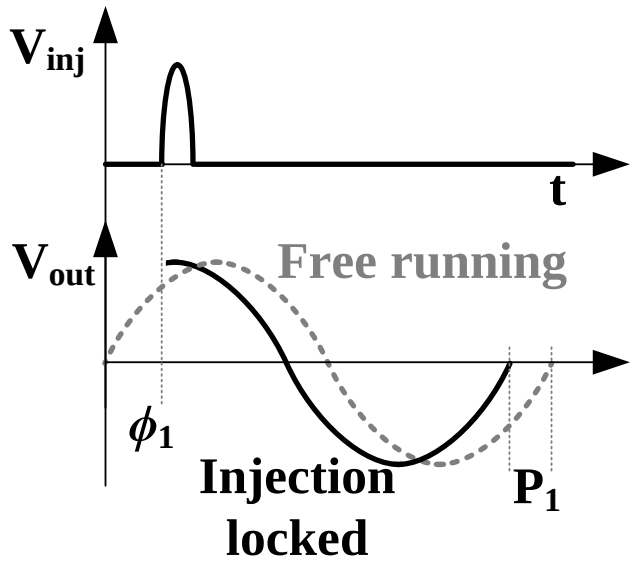

Figure 2.13. Single pulse injection at $\phi 1$.

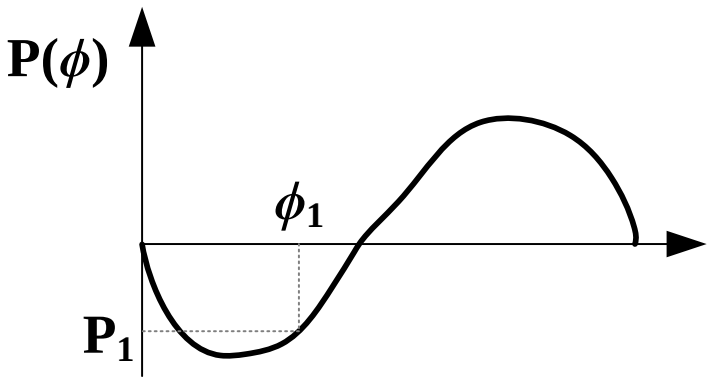

Figure 2.14. PDR curve example.

2.5 LC Quadrature Oscillator

2.5.1 Overview

Since the proposed quadrature resonant clocking scheme is very similar to the LC quadrature oscillator, understanding the LC quadrature oscillator is very helpful in following the proposed quadrature resonant clocking scheme. Therefore, this section describes the basic principles, operation modes and characteristics of the LC quadrature oscillator.

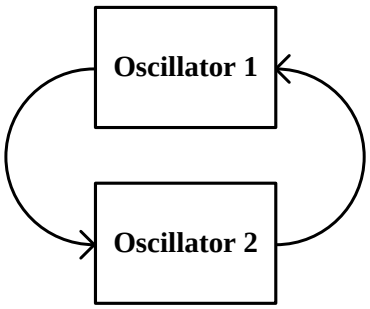

Figure 2.15 Two oscillators coupled each other.

When two identical oscillators are properly coupled as depicted in the Figure 2.15, the two oscillators operate with a phase shift of 90°. The LC quadrature oscillator is designed on this principle. How to implement this coupling structure is explained in the next section.

2.5.2 Basic Principles of the LC Quadrature Oscillator

The coupling state of Figure 2.15 is shown as a small-signal model, as shown in Figure 2.16. Circuit analysis based on this model is as follows.

$$G_{m1}V_1\frac{-RZ_T}{Z_T-R}=V_2 \tag{2.4}$$

$$G_{m2}V_2\frac{-RZ_T}{Z_T-R}=V_1 \tag{2.5}$$

Assuming $V_1, V_2 \neq 0$, and dividing (2.4) by (2.5), the equation of V_1, V_2 is derived as follows.

$$G_{m1}V_1^2-G_{m2}V_2^2=0 \tag{2.6}$$

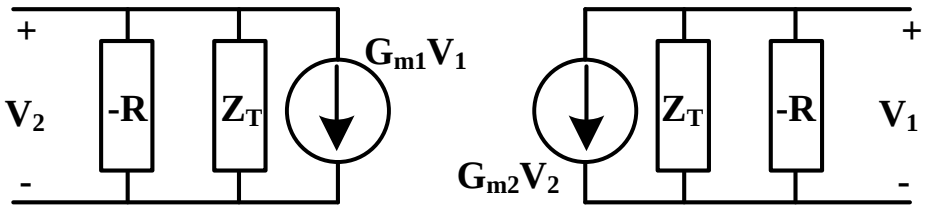

Figure 2.16. Small-signal model of quadrature oscillator.

This result predicts two important cases. If $G_{m1} = G_{m2}$, then

$$V_1^2 - V_2^2 = 0 \tag{2.7}$$

$$V_1 = \pm V_2. \tag{2.8}$$

In this case, the two oscillators operate with a phase difference of zero or 180°. However, if $G_{m1} = -G_{m2}$, then

$$V_1^2 + V_2^2 = 0 \tag{2.9}$$

$$V_1 = \pm jV_2. \tag{2.10}$$

In this case, the phase difference is 90° or -90°. These two cases are called "in-phase coupling" and "anti-phase coupling". The Figure 2.17 and Figure 2.18 are the illustration of the cases respectively. Since the output of the in-phase coupling oscillator is not a quadrature clock, this section presents an analysis of the anti-phase coupling oscillator.

A linear model of an anti-phase coupling LC quadrature oscillator shown in the Figure 2.18 consists of two coupled parallel RLC circuits as represented in Figure 2.19. In parallel with each tank there are negative resistances $-1/g_m$, which cancel the losses. Two differential transconductances g_{mc} provide the coupling, and are responsible for the quadrature outputs.

In the linear model of the LC quadrature oscillator which is shown in Figure 2.19 the loop gain is derived as follows.

$$G_{loop}(s) = -g_{mc}^2 \left(\frac{sL}{1 + sL\left(\frac{1}{R_p} - g_m\right) + s^2 LC} \right)^2 \tag{2.11}$$

Using the Barkhausen criterion for the loop gain with $1/g_m = R_p$, the equation

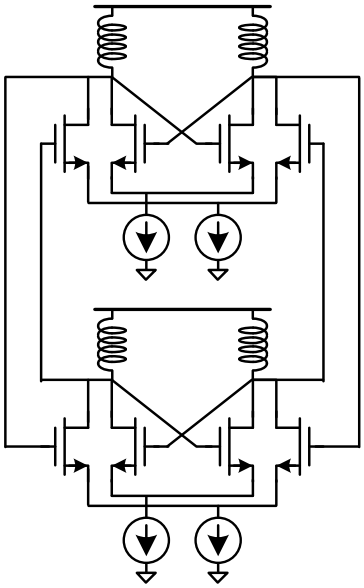

Figure 2.17. In-phase coupling

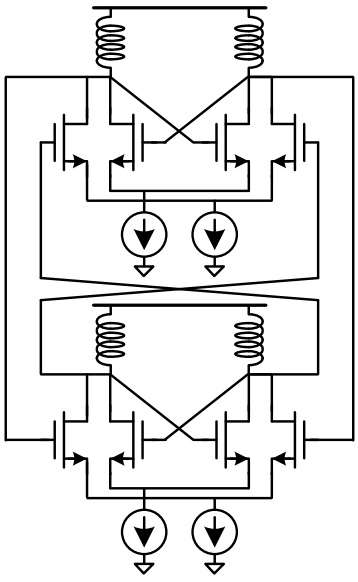

Figure 2.18. Anti-phase coupling.

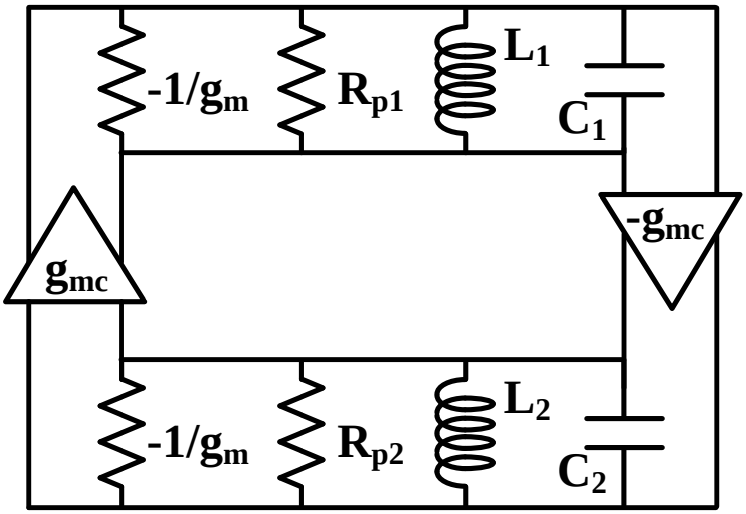

Figure 2.19. Linear model of the anti-phase coupling LC quadrature oscillator.

(2.11) is solved as follows.

$$1 = -g_{mc}^2 \left(\frac{sL}{1+s^2LC}\right)^2 \tag{2.12}$$

$$\pm j = \frac{g_{mc} sL}{1+s^2LC}. \tag{2.13}$$

By making $s = j\omega$, the equation (2.13) is solved in order to ω as follows and have two solutions.

$$\pm 1 = \frac{g_{mc}\omega L}{1-\omega^2 LC} \tag{2.14}$$

$$\omega^2 \pm \frac{g_{mc}}{2C} 2\omega L - \omega_0^2 = 0. \tag{2.15}$$

Where the $\omega_0 = 1/\sqrt{LC}$. The oscillation frequency ω_{osc1} and ω_{osc2} are derived as follows.

$$\omega_{osc1} = +\frac{g_{mc}}{2C} + \omega_0 \sqrt{1 + \frac{g_{mc}^2 L}{4C}} \tag{2.16}$$

$$\omega_{osc2} = -\frac{g_{mc}}{2C} + \omega_0 \sqrt{1 + \frac{g_{mc}^2 L}{4C}}. \tag{2.17}$$

Assuming that,

$$\frac{g_{mc}^2 L}{4C} \ll 1 \tag{2.18}$$

the equations (2.19) and (2.20) are derived.

$$\omega_{osc1} \approx \omega_0 + \frac{g_{mc}}{2C} \tag{2.19}$$

$$\omega_{osc2} \approx \omega_0 - \frac{g_{mc}}{2C}. \tag{2.20}$$

From equations (2.19) and (2.20) it is observed that coupling two oscillators will produce some shift in the oscillation frequency. And the phenomenon that the LC quadrature oscillator has two solutions is called the bi-modal operation of the LC quadrature oscillator [36] -[38] and is discussed in more detail in the later section.

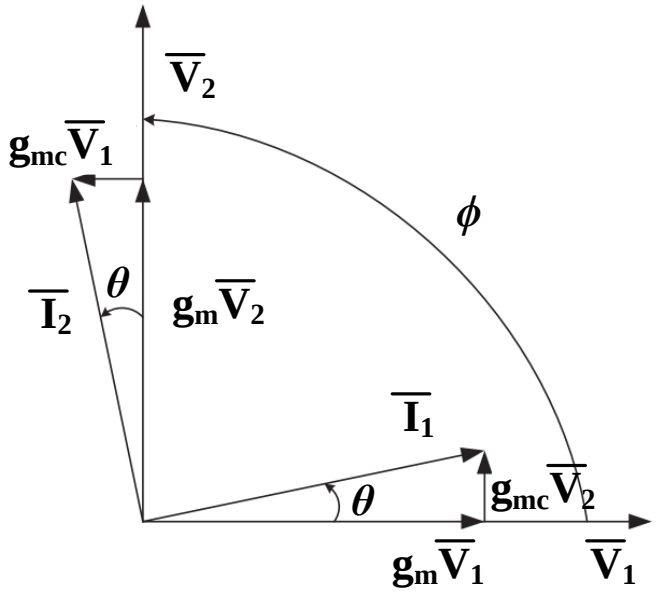

Figure 2.20. Phasor diagram of the LC quadrature oscillator.

In the Figure 2.20, the currents and the voltages in the LC oscillator are represented by a phasor diagram, where ϕ represents the phase difference between the $\overline{V1}$ and $\overline{V2}$, and θ is the phase difference between $\overline{I1}$ and $\overline{V1}$, which is

$$\theta = \arctan\left(\frac{g_{mc}}{g_m}\right) = \arctan(coupling\ factor). \qquad (2.21)$$

The LC quadrature oscillator circuit without mismatches is symmetric and this implies that there is perfect quadrature, $\phi = \pi/2$, otherwise the voltages and currents would be different in the two oscillators, which is incompatible with the circuit symmetry

The equations (2.19), (2.20), and (2.21) indicates that, as the bias current of the

differential pair for quadrature coupling increases (and so does the g_{mc} and coupling factor), the oscillation frequency must deviate from ω_0 by a greater amount so that each LC tank provides the required phase shift. Since the LC tanks operate at a frequency that is increasingly farther from the resonance frequency, the Q factor falls, raising the phase noise. From this point of view, it is desirable to minimize the coupling factor.

In the case when the mismatches exist between the two LC insufficient coupling fails to force them to equal frequencies. A coupling factor of approximately 0.25 typically provides a reasonable compromise between Q degradation and oscillation reliability.

2.5.3 Bi-Modal Operation of the LC Quadrature Oscillator

Bi-modal operation of the LC quadrature oscillator, as discussed in the previous section, is the phenomenon that the LC quadrature oscillator has two frequency solutions, which are (2.19) and (2.20). Both solutions have the quadrature output clocks, I, Ib, Q, Qb, with 90° phase difference. However, in one solution, I clock leads Q clock but in the other, I clock lags Q clock. Since the relationship between I clock and Q clock is critical to most multi-rate applications using quadrature clock, predictability and stability of two solutions is important.

Thanks to [36] , analysis of the LC quadrature oscillator based on the injection locking is complete and this section briefly introduces the analysis process and results about bi-modal operation.

Figure 2.21 shows the LC quadrature oscillator under injection. The anti-phase coupling of two LC oscillators is expressed as an injection based equivalent circuit. Applying the generalized Adler's equations to each oscillator leads to the following equations.

$$\frac{d\theta_1}{dt} = \omega_0 - \frac{\omega_0}{2Q}\frac{I_C \sin(\theta_2 - \theta_1 - \phi)}{I - I_C \cos(\theta_2 - \theta_1 - \phi)} \tag{2.22}$$

$$\frac{d\theta_2}{dt} = \omega_0 + \frac{\omega_0}{2Q}\frac{I_C \sin(\theta_1 - \theta_2 - \phi)}{I + I_C \cos(\theta_1 - \theta_2 - \phi)} \tag{2.23}$$

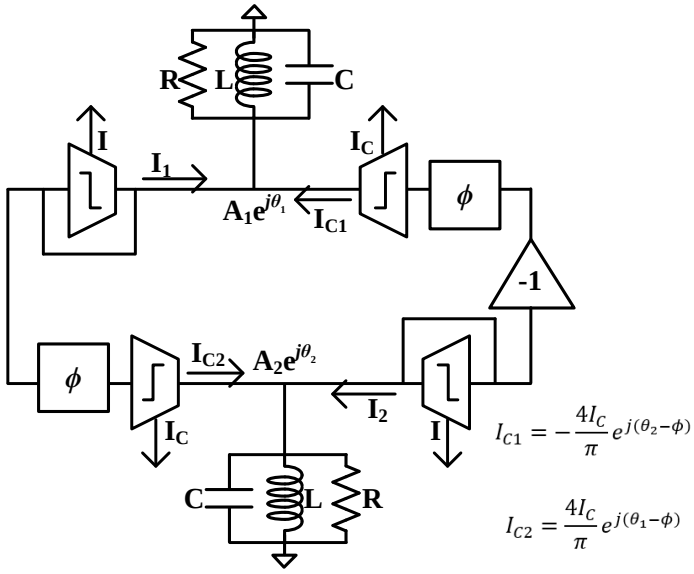

Figure 2.21. LC quadrature oscillator.

$$RC\frac{dA_1}{dt} + A_1 = \frac{4R}{\pi}(I - I_C\cos(\theta_2 - \theta_1 - \phi)) \tag{2.24}$$

$$RC\frac{dA_2}{dt} + A_2 = \frac{4R}{\pi}(I + I_C\cos(\theta_1 - \theta_2 - \phi)) \tag{2.25}$$

Considering the stable oscillator condition, $dA_1/dt = dA_2/dt = 0$,writing the two output phases as $\theta_1 = \omega_{osc}t$ and $\theta_2 = \omega_{osc}t + \psi = \omega_{osc}t \pm \pi/2$, defining the coupling ratio $m = I_c/I$, the amplitude and the frequency of the two modes are derived as follows.

$$\omega_{osc,m1} = \omega_0 - \frac{\omega_0}{2Q}\frac{m\cos\phi}{1 - m\sin\phi} \tag{2.26}$$

$$A_{m1} = \frac{4IR}{\pi}(1 - m\sin\phi) \tag{2.27}$$

$$\omega_{osc,m2} = \omega_0 + \frac{\omega_0}{2Q}\frac{m\cos\phi}{1 + m\sin\phi} \tag{2.28}$$

$$A_{m2} = \frac{4IR}{\pi}(1 + m\sin\phi) \tag{2.29}$$

The frequencies of equation (2.26) and (2.28) are identical to the equations (2.19) and (2.20). Using perturbation analysis, assuming that $\theta_1 = \omega_{osc}t + \hat{\theta}_1$ and $\theta_2 = \omega_{osc}t + \psi = \omega_{osc}t \pm \pi/2 + \hat{\theta}_2$, where $|\hat{\theta}_1|, |\hat{\theta}_2| \ll 1$, following equations are derived for the first mode.

$$\frac{d\hat{\theta}_1}{dt} = \frac{\omega_0}{2Q}\frac{m(m - \sin\phi)}{(1 - m\sin\phi)^2}(\hat{\theta}_2 - \hat{\theta}_1) \tag{2.30}$$

$$\frac{d\hat{\theta}_2}{dt} = \frac{\omega_0}{2Q}\frac{m(m - \sin\phi)}{(1 - m\sin\phi)^2}(\hat{\theta}_1 - \hat{\theta}_2) \tag{2.31}$$

$$\frac{d(\hat{\theta}_1 - \hat{\theta}_2)}{dt} = -\frac{\omega_0}{Q}\frac{m(m - \sin\phi)}{(1 - m\sin\phi)^2}(\hat{\theta}_1 - \hat{\theta}_2) \tag{2.32}$$

And for the second case, in the same way, following equations are derived.

$$\frac{d(\hat{\theta}_1 - \hat{\theta}_2)}{dt} = -\frac{\omega_0}{Q}\frac{m(m + \sin\phi)}{(1 + m\sin\phi)^2}(\hat{\theta}_1 - \hat{\theta}_2) \tag{2.33}$$

The equations (2.32) and (2.33) are the form of $dx/dt = kx$. When the coefficient

k is negative, x will decay. That means, in the equation (2.32), when $m - \sin\phi > 0$, the perturbation will decay and the mode will be restored. Therefore, the first mode is conditionally stable when $\sin\phi < I_C/I$. In the same way, the second mode is unconditionally, always stable.

Considering the coupling ratio is usually a small number in the range of 0.1 to 0.4, it is not that complicated that inserting the small phase shift in the quadrature coupling path. However, the recommended phase shift is 90° because the first mode is always unstable with the phase shift of 90°. In addition, according to the [36] , the quadrature accuracy and phase noise are also the best when the 90° phase shift is inserted in the quadrature coupling path.

2.5.4 Phase Noise of the LC Quadrature Oscillator

In an LC oscillator the noise is originated in three different blocks: the lossy LC tank, the transistors of the differential pair, and the tail current source. Considering the equivalent circuit of the LC oscillator in the Figure 2.22 as a very beginning, assuming that the only noise source is the thermal noise [39] , the phase-noise contribution of the tank can be calculated, which is represented either as a current source across the tank with a spectral density or as a voltage noise source in series with the tank with spectral density.

$$S(i_n) = \frac{4kT}{R_p} \tag{2.34}$$

$$S(v_n) = S(i_n)|Z_T|^2 \tag{2.35}$$

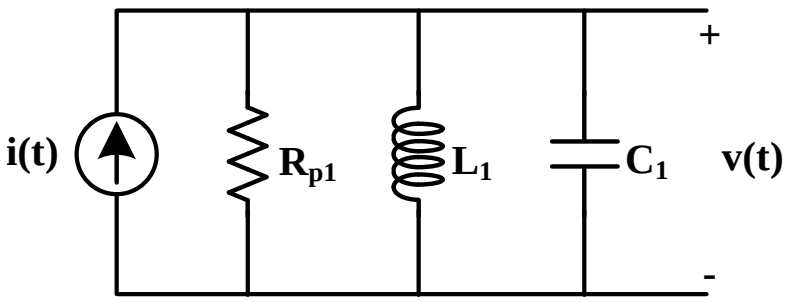

Figure 2.22. Equivalent circuit of the LC oscillator.

Using the model of Figure 2.22, for small offset frequencies with respect to the fundamental frequency ($\omega_m \ll \omega_0/2Q$) the impedance of the LC tank, Z_T, is approximated by [39] and [40] as follows.

$$|Z_T(\omega_0 + \omega_m)|^2 \approx R_p^2 \frac{1}{4Q^2}\left(\frac{\omega_0}{\omega_m}\right)^2 \tag{2.36}$$

The definition of the Q factor in [41] is as follows where $A = |Z(j\omega)|$, $\theta = \arg|Z(j\omega)|$ and the resonant frequency $\omega_0 = 1/\sqrt{LC}$.

$$Q = \frac{\omega_0}{2}\sqrt{\left(\frac{dA}{d\omega}\right)^2 + \left(\frac{d\theta}{d\omega}\right)^2} \tag{2.37}$$

In a stable LC oscillator $dA/d\omega = 0$ [41] , and for $Q_0 = Q(\omega_0)$

$$\begin{aligned} Q_0 &= \frac{\omega_0}{2}\left|\frac{d\theta}{d\omega}\right|_{\omega=\omega_0} \\ &= R_p\sqrt{\frac{C}{L}} = \frac{R_p}{\omega_0 L} \end{aligned} \tag{2.38}$$

Considering that the losses in the capacitors are much lower than those in the inductors, the resonator quality factor is determined mainly by the inductor, and the parallel resistance is obtained from the inductor quality factor [40] .

Using equations (2.34), (2.35), and (2.36),

$$\begin{aligned} S(v_n) &= \frac{4kT}{R_p}\left|R_p\frac{\omega_0}{2Q\omega_m}\right|^2 \\ &= 4kTR_p\left(\frac{\omega_0}{2Q\omega_m}\right)^2 \end{aligned} \tag{2.39}$$

From (2.39) it can be concluded that increasing Q factor leads to a reduction in the

noise spectral density, when all the other parameters remain unchanged. The output noise is frequency dependent, due to the filtering action of the tank: the spectral density is inversely proportional to the square of the offset frequency. This behavior is due to the fact that the voltage frequency response of an RLC tank rolls off as $1/f$ to each side of the center frequency, and power is proportional to the square of voltage [42] .

An important aspect is that thermal noise affects both amplitude and phase, and equation (2.39) includes their combined effect. In the absence of amplitude limiting, the amplitude-noise and phase-noise powers are equal. However, considering an amplitude limiting mechanism of the oscillator, the mechanism removes most of the amplitude-noise. Therefore, the total noise power in the oscillator will be approximately half the noise given by (2.39) [39] , [40] , and [43] .

The phase noise spectral density is derived as follows by dividing by the carrier power, $P_{carrier} = V_{tank}^2/R_p$.

$$\mathcal{L}(\Delta\omega) = 10\log\left[\frac{2kT}{P_{carrier}}\left(\frac{\omega_0}{2Q\omega_m}\right)^2\right] \tag{2.40}$$

It should be noted that (2.40) is only valid for the $1/f^2$ region of the noise spectrum. A complete equation of the phase noise spectral density for all the spectral oscillator regions was presented by [44] .

In the case of the LC quadrature oscillator, a maximum of 3 dB improvement of the oscillator phase-noise can exist in two coupled LC oscillators when compared with a single LC oscillator.

$$\mathcal{L}(\Delta\omega) = 10\log\left[\frac{1}{2}\frac{2kT}{P_{carrier}}\left(\frac{\omega_0}{2Q\omega_m}\right)^2\right] \tag{2.41}$$

This maximum 3 dB improvement, due to coupling, is obtained when the oscillators are isolated and oscillate at their common resonance frequency. When the oscillators are coupled, the oscillation frequency changes according to the equations (2.19) or (2.20). In this case, Q factor which is different from the equation (2.38) is derived as follows.

The impedance phase of an RLC circuit is

$$\theta(\omega) = \frac{\pi}{2} - \arctan\frac{\omega L/R_p}{1-\omega^2 LC} \tag{2.42}$$

and

$$\frac{d\theta(\omega)}{d\omega} = \frac{LR_p(CL\omega^2+1)}{C^2L^2R_p^2\omega^4 - 2CLR_p^2\omega^2 + L^2\omega^2 + R_p} \tag{2.43}$$

Substituting (2.43) in (2.37) and using the stable LC oscillator condition, $dA/d\omega = 0$ [41] ,

$$Q = \frac{\omega_0}{2}\left|\frac{LR_p(CL\omega^2+1)}{C^2L^2R_p^2\omega^4 - 2CLR_p^2\omega^2 + L^2\omega^2 + R_p}\right| \tag{2.44}$$

When the oscillators are coupled, the theoretical equation (2.44) for Q factor should be used.

At the resonant frequency, the equation (2.43) simplifies to

$$\frac{d\theta(\omega)}{d\omega} = -2CR_p \tag{2.45}$$

And Q factor is given by (2.38) as expected.

The most important conclusion from this study is that the performance of the single LC oscillators is different from the performance of the LC quadrature oscillators. Coupled LC oscillators can have a theoretical phase noise improvement of 3 dB, but, any deviation from the resonance frequency due to mismatches and to coupling will reduce Q and increase the phase noise.

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Chapter 3

Design of the Proposed Quadrature Resonant Clock

3.1 Overview

In this chapter, a quadrature resonant clock with frequency tuning capacitor and amplitude control feedback loop is proposed. The proposed quadrature resonant clocking scheme achieves high power reduction ratio under all operating conditions by tuning out the frequency mismatch using the frequency tuning capacitors.

3.2 Overall Architecture

Figure 3.1 shows the overall block diagram of the proposed quadrature resonant clocking scheme incorporating four 4.3-mm load wires, two inductors, two frequency tuning capacitors, two negative gm cells, quadrature coupling cells, an input injection cell, pulse generation cell, a peak detector and a PLL for frequency tuning.

The parasitic capacitor and the inductor of the load wire act as the LC resonator, and the LC quadrature oscillator is composed of the resonator, the negative gm cell, and the quadrature coupling cell. The bang-bang phase frequency detector (BBPFD) and the peak detector generate up and down information for the phase and amplitude of the output clock, respectively. The digital loop filter (DLF) uses the information received from the BBPFD and peak detector to generate the signal that controls the tuning capacitor and the bias current of the negative gm cell. The input clock is injected into the load wire and the quadrature oscillator core through the pulse generation cell and the injection cell. The design, simulation results, and analysis of each part of the proposed quadrature resonant clock are covered in later sections.

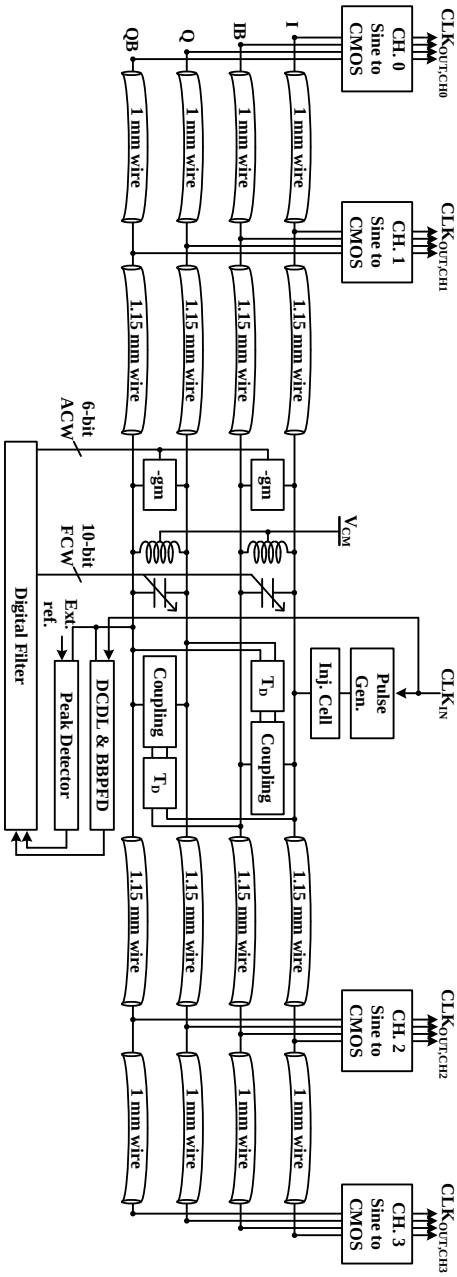

Figure 3.1. Overall architecture of the proposed quadrature resonant clock.

3.3 Load Wire Design and Q Factor Calculation

The shape of the load wire in the resonant clock is very important because it determines the capacitance affecting the resonant frequency of the LC tank. The shape also determines parasitic resistance, which is the most dominant parameter to determine the Q factor. Q factor is an indicator of how much power consumption can be reduced, so optimizing load wire parasitic resistance is one of the most important things in resonant clocking design.

Parameters that determine the shape of the load wire include width, length, thickness, spacing between adjacent wires, and distance from the top and bottom metal layers. These parameters affect the parasitic resistance and capacitance of the wire. In the case of wire width as an example, if the wire is too narrow, the parasitic resistance becomes too large, resulting in poor power reduction. On the contrary, the larger wire width offers smaller resistance and hence better power reduction with a higher Q factor. However, if the capacitor is too large for the operation frequency, the inductor becomes too small to implement with an on-chip spiral inductor. Furthermore, if the capacitor becomes too large, it is difficult to set the tuning capacitor large enough, making it difficult to implement a wide tuning range.

As a method of verifying the performance of the resonant clock in the circuit design process, there is a method of calculating the Q factor of the entire system including the inductor, the parasitic capacitance of the load wire, and the parasitic resistance

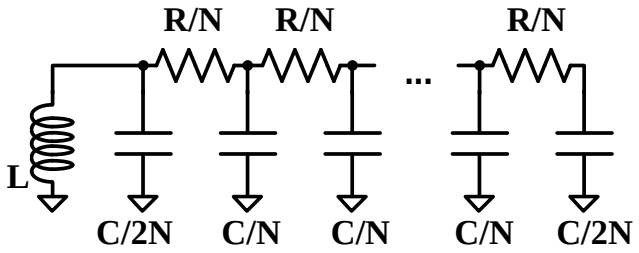

Figure 3.2. N-stage π model of clock distribution wire.

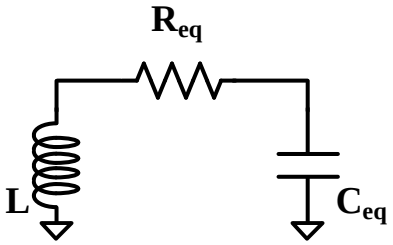

Figure 3.3. Equivalent circuit of the N-stage π model of the clock distribution wire.

of the load wire. In this thesis, the N-stage π model of the lumped wire is used to calculate the Q factor. The Figure 3.2 and Figure 3.3 show the N-stage π model and its equivalent circuit. To simplify the process of calculating the Q factor, an equivalent circuit of the N-stage π model of the lumped wire is used, and the equivalent resistance (R_{eq}) and the equivalent capacitance (C_{eq}) of the equivalent circuit are calculated as follows according to the [45] . In the Figure 3.4, which shows the simplest RC tree, value of R, C and the admittance at the driving point, Y(s), are expressed as follows.

$$Y(s) = \frac{sC}{1+sRC} = \sum_{n=1}^{\infty}(-1)^{n-1}R^{n-1}C^n s^n = \sum_{n=1}^{\infty} y_n s^n. \qquad (3.1)$$

$$C = y_1. \tag{3.2}$$

$$R = -\frac{y_2}{y_1^2}. \tag{3.3}$$

Meanwhile, in the Figure 3.5, the impedance and admittance of the open-ended RC network are defined as follows.

$$Z_{in} = Z_0 \frac{Z_L + Z_0 tanh(\gamma l)}{Z_0 + Z_L tanh(\gamma l)}. \tag{3.4}$$

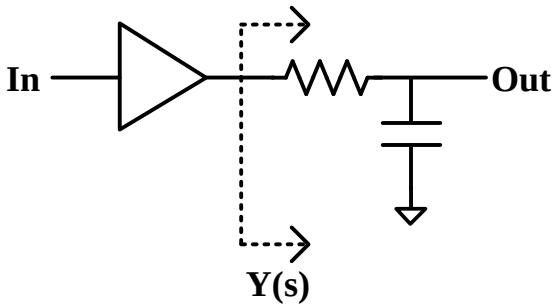

Figure 3.4. Simple RC tree modeling the driving point admittance.

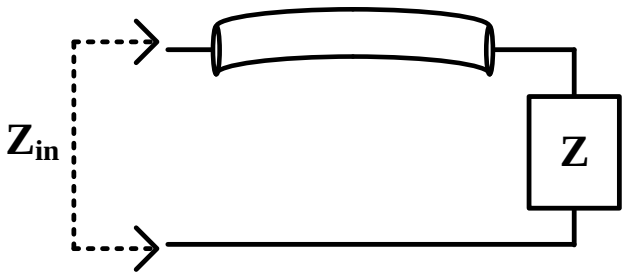

Figure 3.5. Open-ended RC network.

$$Y = \frac{tanh(\gamma l)}{Z_0}. \tag{3.5}$$

$$\gamma l = \sqrt{sRC}. \tag{3.6}$$

$$Z_0 = \sqrt{\frac{R}{sC}}. \tag{3.7}$$

Since the admittance Y(s) in equation (3.1) and (3.2) must match, it can be summarized as follows.

$$\begin{aligned} Y &= \sqrt{\frac{sC}{R}}\left(tanh\left(\sqrt{sRC}\right)\right. \\ &= \sqrt{\frac{sC}{R}}\left(\sqrt{sRC} - \frac{1}{3}sRC\sqrt{sRC} + \cdots\right) \\ &= sC - \frac{1}{3}s^2RC^2 + \frac{2}{15}s^3R^2C^3 + \cdots \\ &= \sum_{n=1}^{\infty} y_n s^n. \end{aligned} \tag{3.7}$$

Therefore, if the equivalent circuit of the open-ended RC network circuit in Figure 3.5 is constructed as the simple RC tree circuit shown in Figure 3.4, the equivalent resistance (R_{eq}) and the equivalent capacitance (C_{eq}) are determined as follows by using the equations (3.2), (3.3) and (3.7).

$$C_{eq} = C. \tag{3.8}$$

$$R_{eq} = \frac{R}{3}. \tag{3.9}$$

Meanwhile, the block diagram of the LC resonator composed only of the load wire

and the inductor of proposed resonant clocking scheme of Figure 3.1 is shown in the Figure 3.6. Using the R_{eq} and the C_{eq} obtained through the equation (3.8) and (3.9), the equivalent half circuit of the LC resonator in the Figure 3.6 is constructed as shown in the Figure 3.7. The R_W and C are equivalent resistance and capacitance of the 2.15 mm load wire which are derived by using the equation (3.8) and (3.9). Deriving the Q factor from the equivalent half circuit of the LC resonator in Figure 3.7 is as follows.

$$Q = \frac{1}{(R_L + 0.5R_w)}\sqrt{\frac{L}{2C}}. \tag{3.10}$$

As a result of simulation using the obtained equivalent circuits and equations, it can be confirmed that when using an inductor of 1 nH at an operating frequency of 7 GHz, the capacitance of one 4.3 mm wire is approximately 600 fF. In order to design a wire having parasitic capacitance obtained in this way, the structure of the wire must first be determined and the parameters including the width of the wire, spacing between adjacent wires, and distance from the top and bottom metal layers should be determined by referring to the post layout simulation results.

Two pairs of the ground shielded differential wires (GND-CLK-CLKb-GND) were used for the design of the quadrature load wire used in the proposed quadrature resonant clocking scheme. Also, the ground plane was set with metal 2 under the load wire. Based on this structure, parasitic capacitance and parasitic resistance components can be extracted according to the width and spacing of wires. The Table 3.1 is an example of parasitic extraction result according to the metal layer of the load wire when both width and spacing are 1um. Referring to Equation (3.10), the smaller the

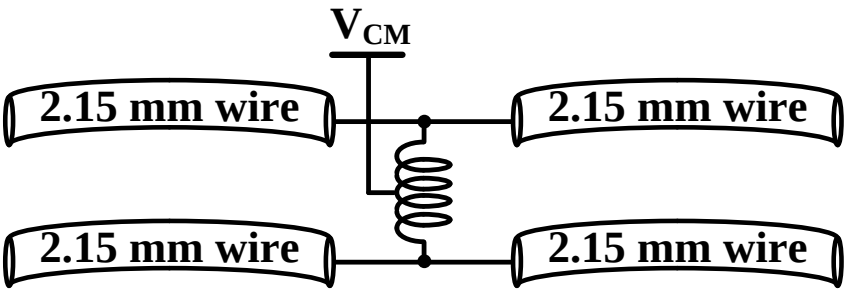

Figure 3.6. Block diagram of LC resonator.

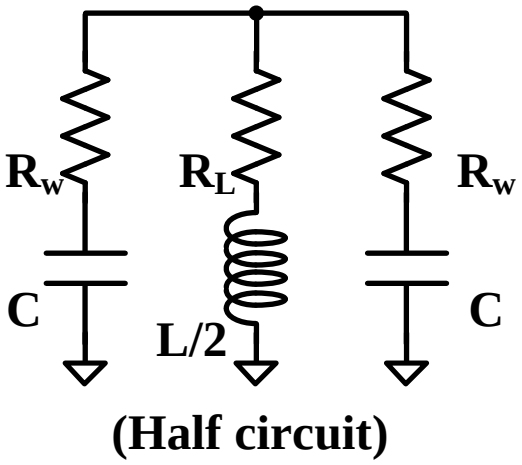

Figure 3.7. Equivalent half circuit of the LC resonator.

series parasitic resistance, the larger the Q factor and thus the more power consumption can be reduced. Therefore, it is suitable to design the load wire with metal 8. In addition, the width and spacing of wires were set to satisfy the aforementioned 600 fF capacitance condition. The final version of load wire is designed to have a capacitance

and resistance of about 130 fF/mm and 15 Ω/mm with the total length of 4.3 mm per each clock wire. The total Q factor of the resonator calculated using equation (3.10) is 4.56. The layout of the quadrature clock distribution wire is shown in the Figure 3.8.

Table 3.1. Example of parasitic extraction result according to the metal layer of the load wire.

Metal Layer	**Width (um)**	**Length (um)**	**Spacing (um)**	**R (ohm)**	**C (fF)**
M3	1	100	1	11.3	24.5
M4	1	100	1	11.3	11.5
M5	1	100	1	11.3	9.4
M6	1	100	1	11.3	8.9
M7	1	100	1	11.3	8.6
M8	1	100	1	2.2	17.6

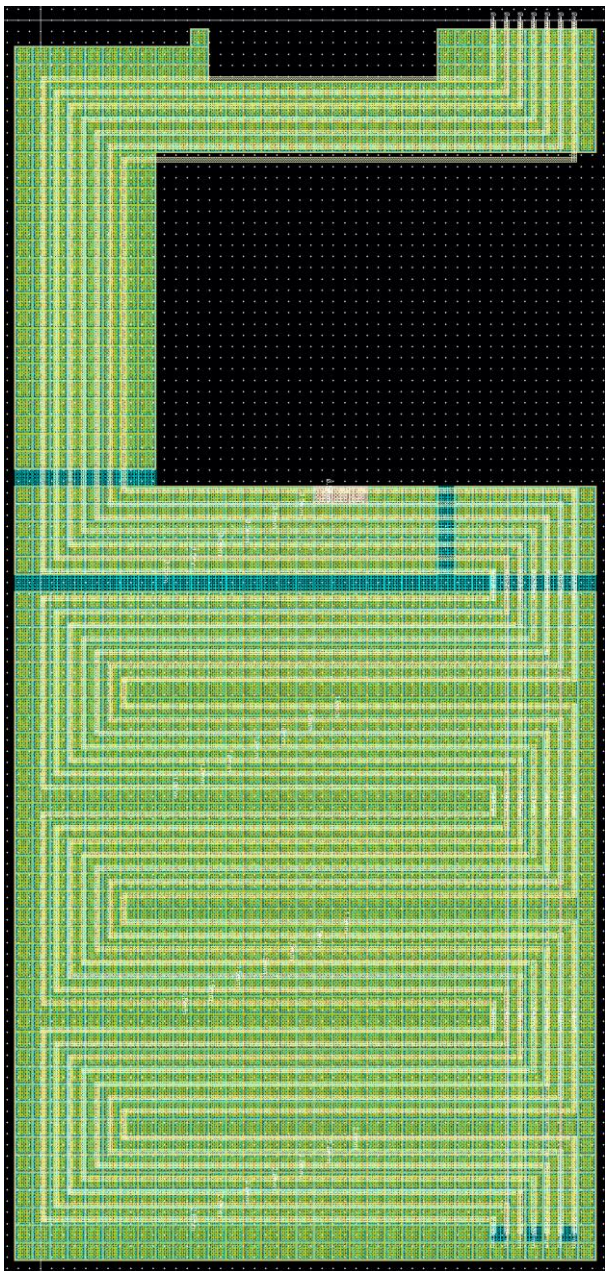

Figure 3.8. Layout of the quadrature clock distribution wire.

3.4 Design of the LC Quadrature Oscillator Core

As discussed earlier, considering the equivalent half circuit in Figure 3.7, the resonant clocking scheme has many structural similarities to LC oscillators. There are only differences in the way capacitors are implemented (cap bank for the LC oscillator and load wire parasitic capacitor for the resonant clocking scheme), and they share a common principle of operation using the resonance between the inductor and the capacitor. Therefore, the design method of LC oscillator can be applied to design the resonant clocking scheme. Therefore, the proposed quadrature resonant clocking scheme has the negative gm cell and the quadrature coupling cell in the same way as the LC quadrature oscillator. The circuit diagram of the LC quadrature oscillator core is shown in Figure 3.9.

The inductor constituting the LC resonator is 0.95 nH, and the Q factor of the inductor alone is about 15. A 3-turn spiral inductor is used to minimize the area, and the layout of the spiral inductor is shown in Figure 3.10. The spiral inductor occupies an area of 146*142 um^2

The negative gm cell is designed based on the cross-coupled NMOS transistors which is one of the most basic design of the LC quadrature oscillator. The quadrature coupling cell is designed based on the basic differential pair with antiphase coupling. The quadrature coupling ratio determined by the ratio of the bias current of the negative gm cell and the bias current of the coupling cell is designed to be adjustable in

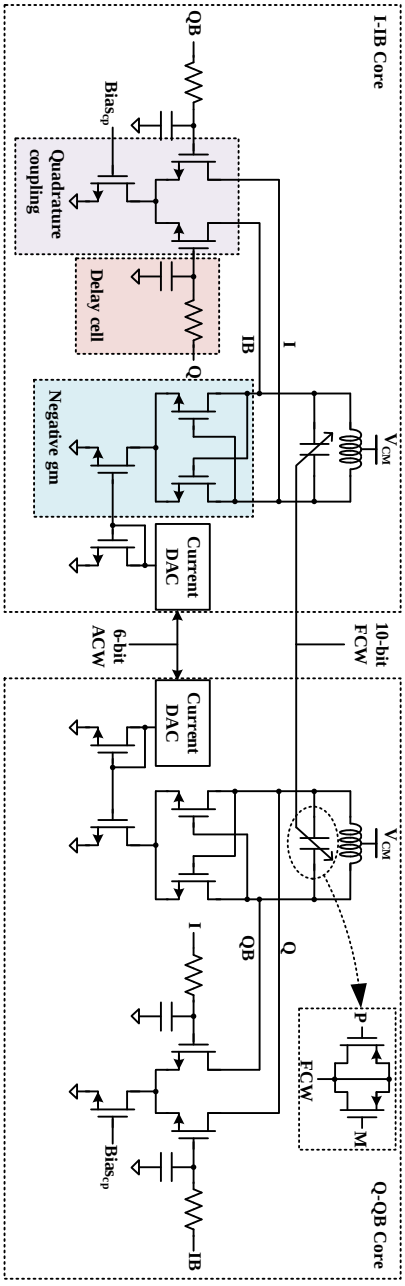

Figure 3.9. Circuit diagram of the LC quadrature oscillator core.

the range of 0.2 to 0.5.

In front of the quadrature coupling NMOS differential pair, the first-order RC delay unit (T_D) is inserted to avoid the bi-modal oscillation which is conditionally stable [36] -[38] . In addition, the delay unit improves the quality of the output clock according to [36] when the delay is close enough to 90°. When the inserted phase shift is 90°, the LC quadrature oscillator has only one oscillation mode unconditionally. Therefore, the most appropriate delay is 90°. However, producing exactly 90° is difficult considering mismatch and PVT variations. Also, 90° can only be created using an active delay line or a high-order filter, but these methods have some problems that the designing the active delay line or high-order filter is complicated and they consume a lot of power. Therefore, in the proposed quadrature resonant clocking scheme, the first-order filter is used for less design complexity and less power consumption.

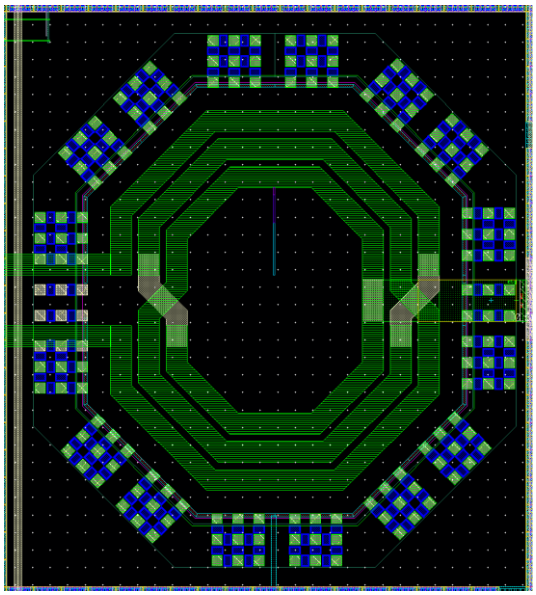

Figure 3.10. Layout of the spiral inductor.

The LC quadrature oscillator has only one mode when the quadrature coupling ratio is less than 2/3 when a 60° phase shift is inserted into the first-order RC filter.

The LC quadrature oscillator core includes a tuning capacitor to tune the resonant frequency to reduce the difference between the resonant frequency and the operation frequency, and the current digital-to-analog converter (DAC) to adjust the bias current of the negative gm cell that controls the amplitude. The tuning capacitor is controlled by the 10-bit binary digital code (frequency control word, FCW) and the bias current of the negative gm cell is controlled by the 6-bit binary digital code (amplitude control word, ACW). The detailed control method of the FCW and the ACW will be covered in later sections.

Figure 3.11 shows the result of the post layout simulation that the free running output of the oscillator appears well with only the LC quadrature oscillator circuit configured as described in this section. The waveform in Figure 3.11 confirms that there is no problem with free running oscillation with the initial condition.

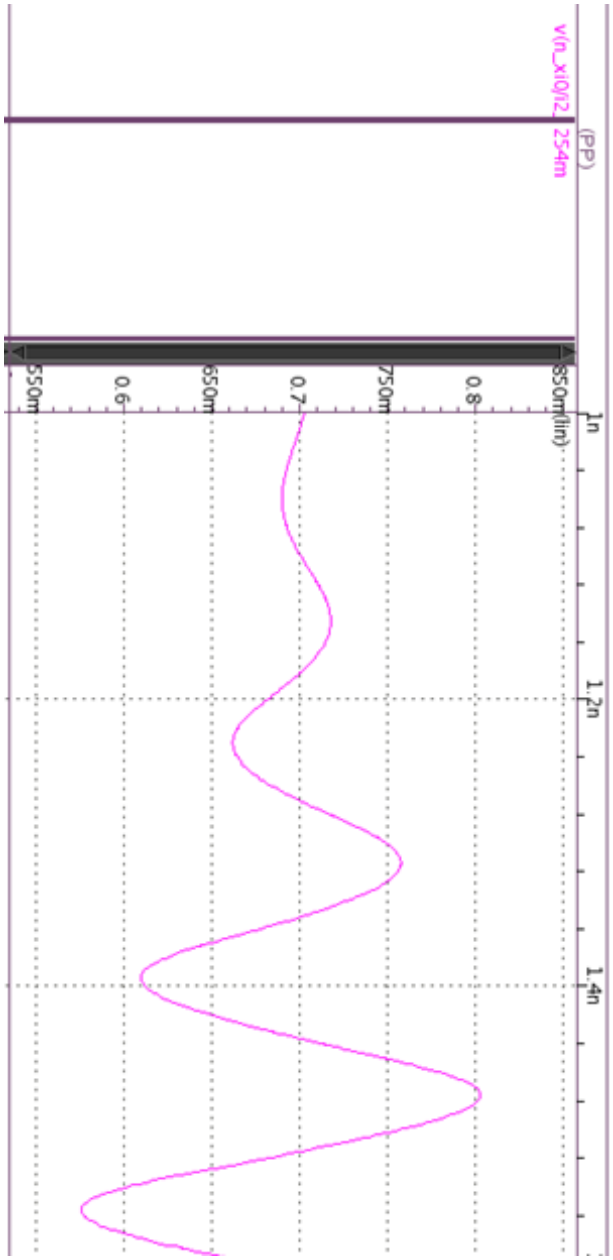

Figure 3.11. Post layout simulation result of the LC quadrature oscillator.

3.5 Feedback Loops

3.5.1 Frequency Control Loop

As shown in the previous chapters, the resonant frequency optimization using the tuning capacitor is essential to solve the problems of the existing resonant clocking scheme caused by the difference between the resonant frequency and the operation frequency. If the difference between the resonant frequency and the operation frequency is not eliminated, the power reduction is not optimized because the impedance of the LC tank cannot be optimized and the LC tank cannot function as a resonator. In addition, it is very important to optimize the resonant frequency using a tuning capacitor in order to apply a resonant clocking scheme to an application having a wide frequency range.

As shown in the Figure 3.12, in the proposed quadrature resonant clocking scheme, frequency tuning is performed using a BBPFD and a DLF_{FCW}, which are the same as in PLL. The BBPFD generates up and down information by comparing which of the reference clock and oscillator output clock comes first. The DLF_{FCW} uses the information received from the BBPFD to generate the signal that controls the tuning capacitor (FCW). DLF_{FCW} also includes a delta-sigma modulator.

The BBPFD is composed of a phase frequency detector (PFD), an arbiter and a latch as shown in the Figure 3.13. The PFD generates up (UP) and down (DN) pulse, then, the arbiter determines which one comes earlier. The latch holds the output states until next state come.

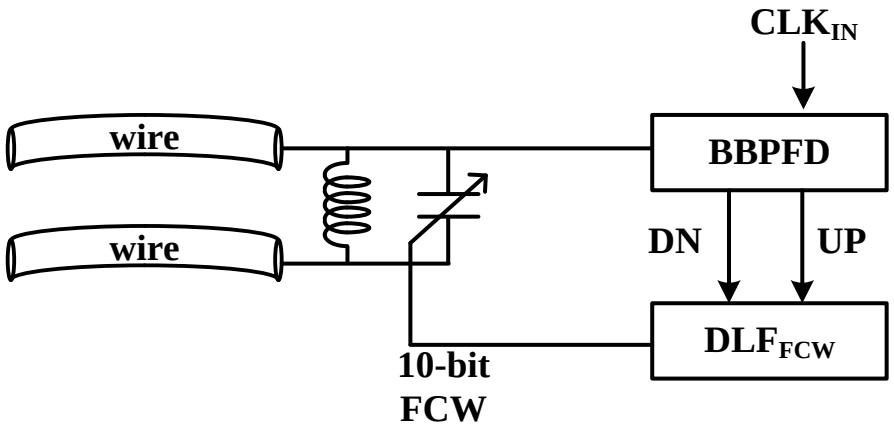

Figure 3.12. Frequency control feedback loop.

The DLF_{FCW}, which is shown in the Figure 3.14, filters the input from the BBPFD and generates the 10-bit frequency control word (FCW). The DLF_{FCW} is composed of the proportional path and the integral path. The proportional path just multiplies the gain of β to the input (UP, DN) and corrects the phase error. On the contrary, the integral path holds the frequency information by accumulating the input information with the gain of α.

When the frequency control loop completes the operation and the output frequency becomes the lock state, the DLF_{FCW} ignores the UP and DN so that the FCW does not change during the input injection process. If the FCW is not fixed, the phase of the output clock is changed by the injection clock. Then, DLF_{FCW} tries to compensate for this phase change. However, since the output frequency is fixed by the effect of input injection, FCW changes in the wrong direction until it goes out of the injection rock range. Therefore, FCW must be fixed when the operation of the feedback loop is

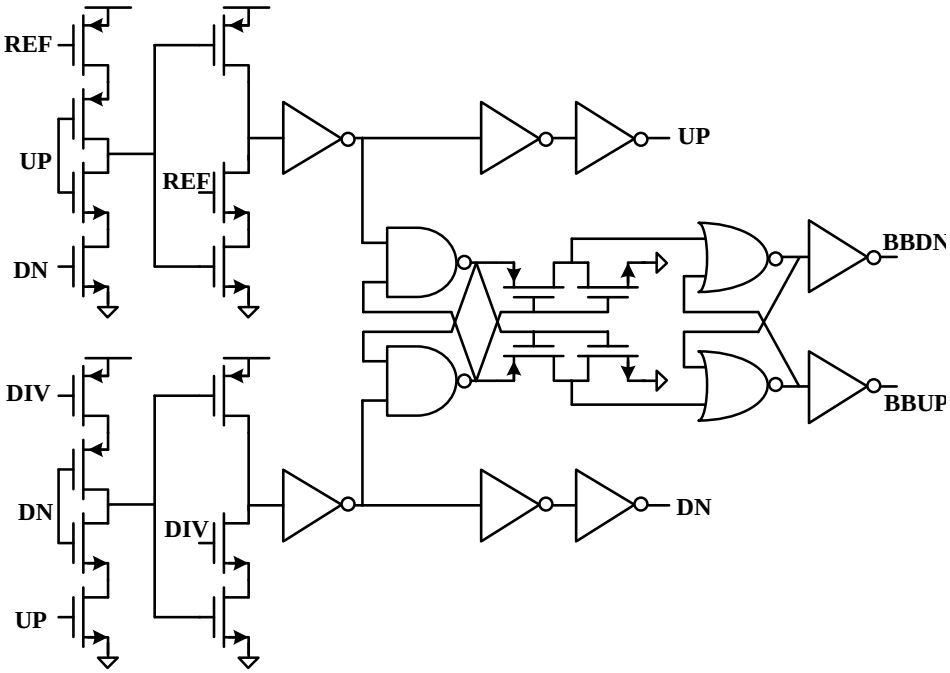

Figure 3.13. BBPFD.

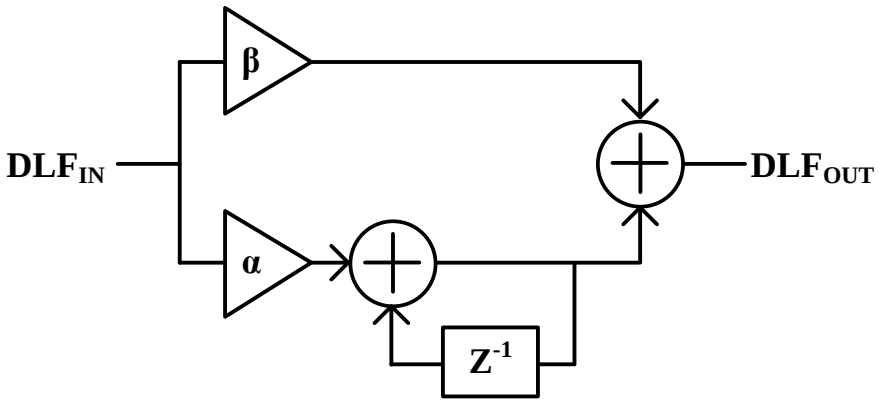

Figure 3.14. DLF_{FCW}.

completed and injection is started.

The transient simulation results showing the frequency control feedback loop locking behavior are shown in Figure 3.15. The waveform of output clock (I, Ib), the frequency of the output clock, 10-bit FCW and BBPFD output signals (UP, DN) are shown. The simulation is done using AMS simulator. Due to the limitation of the simulation speed, the DLF_{FCW} gain is largely set, so it is not fully locked, but it is sufficient to verify the functionality of the frequency control feedback loop.

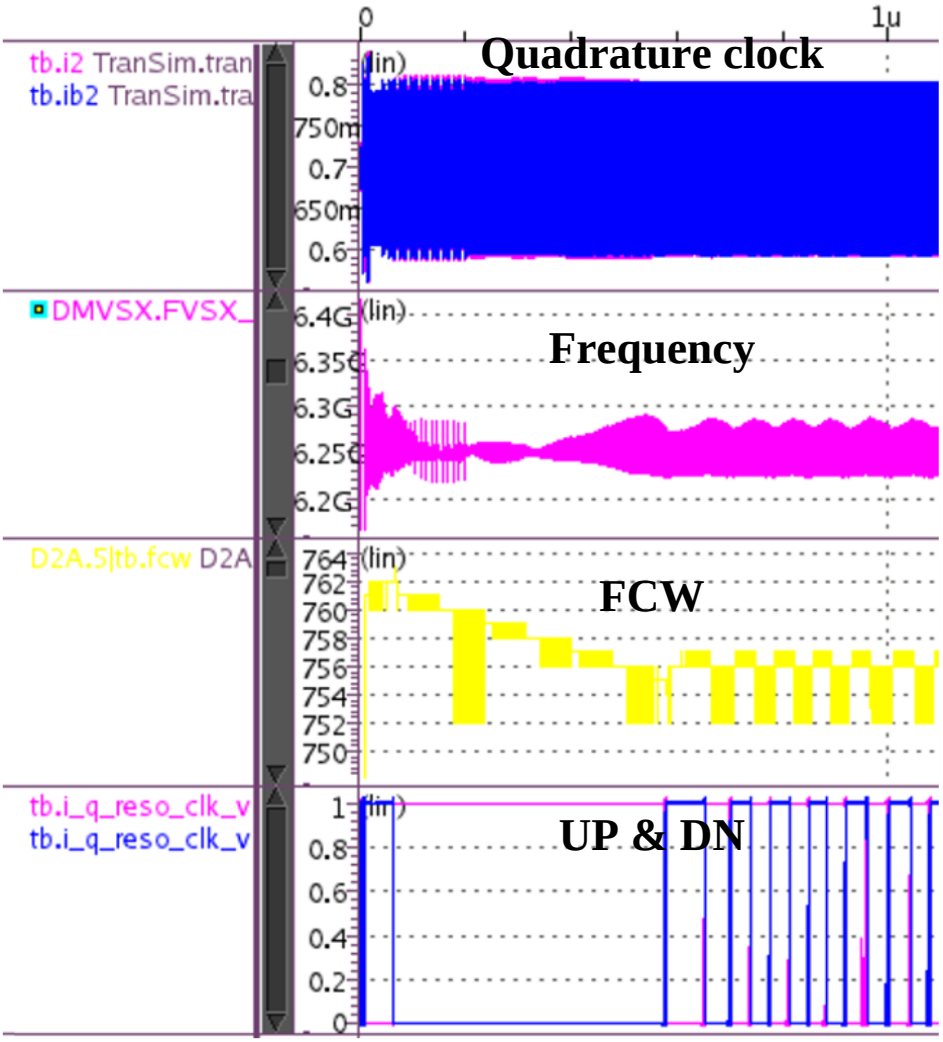

Figure 3.15. transient simulation results showing the frequency control feedback loop locking behavior

3.5.2 Amplitude Control Loop

The bias current of the negative gm cell is one of the most important design parameters in the proposed quadrature resonant clock system because it determines total power consumption and the amplitude of the output clock. Therefore, a feedback loop is required to maintain a constant amplitude even under PVT variations and transient conditions that may vary during frequency tuning, while minimizing power consumption. For example, since the capacitance of the LC resonator also affects the amplitude of the output clock, the amplitude of the output clock varies depending on the change of the FCW. Therefore, in the proposed quadrature resonant clocking scheme, there is a feedback loop that controls the amplitude.

As shown in the Figure 3.16, the amplitude control feedback loop consists of a

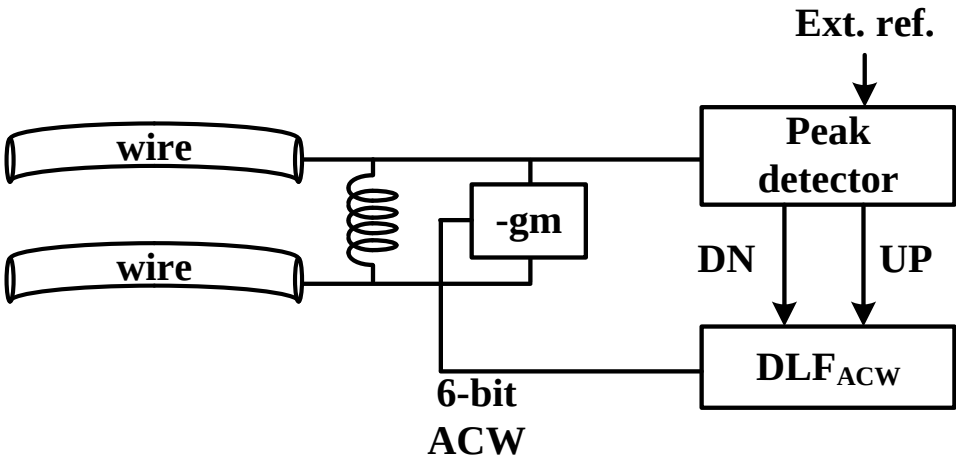

Figure 3.16. Amplitude control feedback loop.

peak detector and a DLF_{ACW}. The peak detector generates up and down information by comparing which of the DC reference value and the peak value of the output clock is larger. The DLF_{ACW} uses the information received from the peak detector to generate the signal that controls the bias current of the negative gm cell (ACW). DLF_{ACW} also includes a delta-sigma modulator.

The DLF_{ACW} uses the peak detector output to generate a 6-bit binary code (ACW) to control the bias current of the negative gm cell. The DLF_{ACW} is almost similar to the DLF_{FCW}, but one difference is that DLF_{ACW} is a first-order digital filter with no proportional path. The amplitude control feedback loop uses a first-order filter because the loop is free from stability issues. The block diagram of DLF_{ACW} is shown in the Figure 3.17.

The circuit shown in the Figure 3.18 is schematic of the peak detector to find the peak value of the sine wave clock and compare it with the DC reference value. The first stage of the peak detector is a source-follower based integrator which hold the

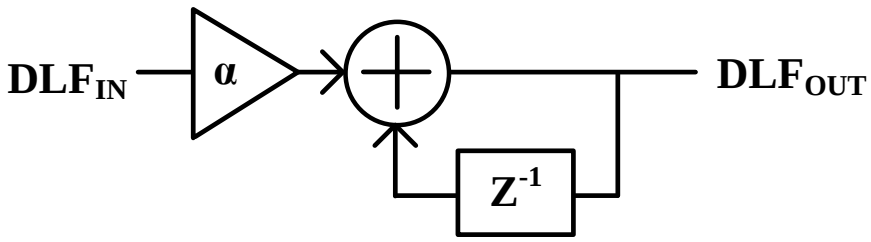

Figure 3.17. DLF_{ACW}.

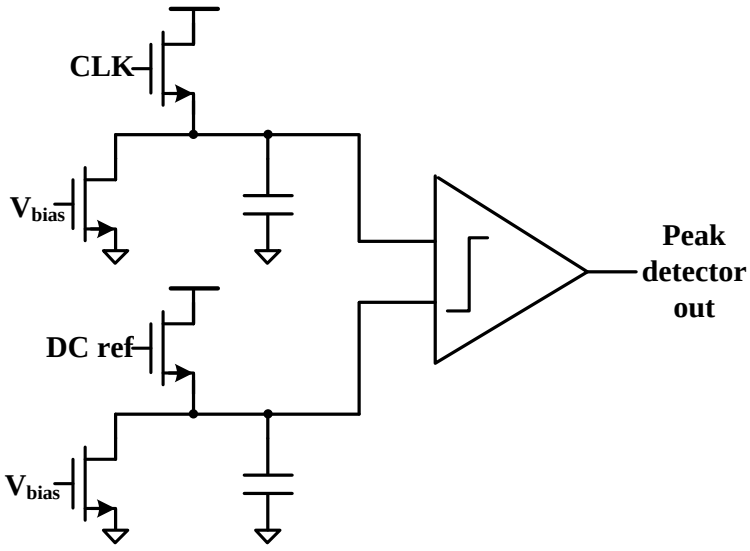

Figure 3.18. Peak detector.

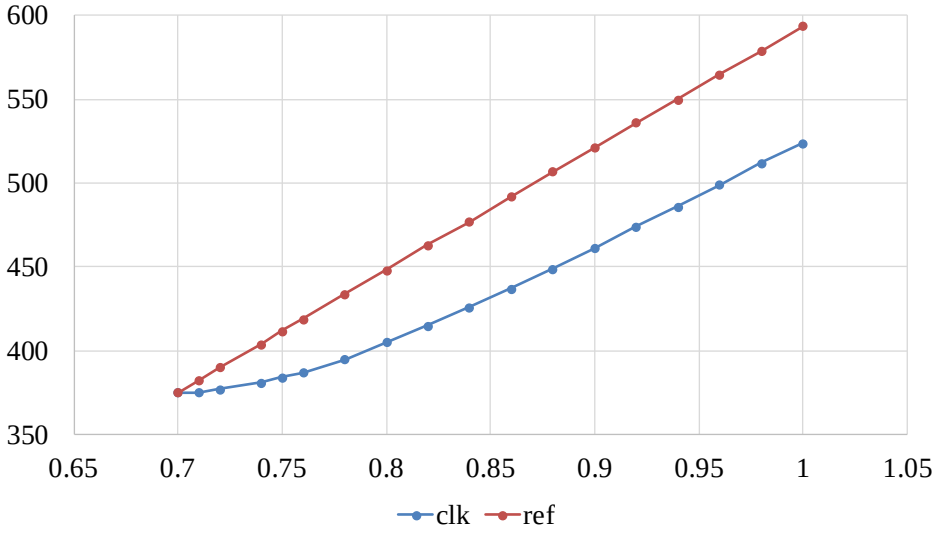

Figure 3.19. Simulation result of the peak detector.

output at the peak value of the input clock. The second stage of the peak detector is a clocked-comparator. Figure 3.19 is the input-to-output simulation result graph of the first stage of the peak detector.

The transient simulation results showing the amplitude control feedback loop locking behavior are shown in Figure 3.20. The waveform of output clock (I, Ib, Q, Qb) and peak detector output are shown.

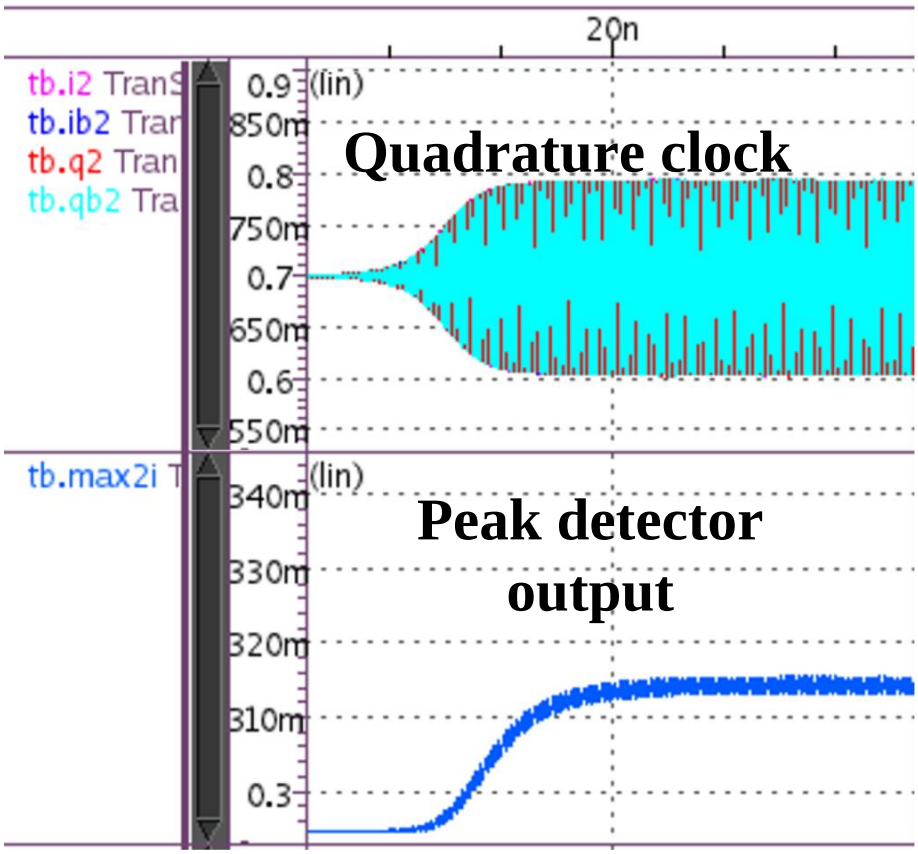

Figure 3.20. transient simulation results showing the amplitude control feedback loop locking behavior

3.7 Injection Cell

3.7.1 Overview

As described in the previous chapter, the resonant clocking scheme and ILO are structurally very similar. In ILO, the injection cell takes over the role of the input buffer of the resonant clocking scheme. Therefore, it is very important to decide how to inject the input clock and design the injection cell and peripheral circuits suitable for the method.

In this section, two methods for input injection are described. One is to inject single-phase pulse and the other is to inject quadrature clock. The structure of the injection cell is different depending on the injection method. Two types of chips designed each way of the input injection are fabricated, and there is no significant difference in injection performance itself.

However, since the method of injecting the single-phase pulse is advantageous for the configuration of the measurement environment and the circuit design complexity of the method of injecting the single-phase pulse is low, other sections of this thesis mainly describe the chip implemented by the method of injecting the single-phase pulse.

3.7.2 Single-Phase Pulse Injection

Single-phase pulse injection is a method of injecting a pulse generated using a single-ended input clock. Since the switch structure can be used as an injection cell, it has the advantage of simple circuit design. However, because the input is injected into only one of the four output nodes (I, Ib, Q, and Qb) in the quadrature oscillator, distortion may inevitably occur in only one of the output clocks, and an asymmetrical output may occur.

Figure 3.21 is a block diagram of a switch-type injection cell and a pulse generation block used in a single-phase pulse injection method. The proposed quadrature resonant clock uses a single NMOS as an injection switch. In general, when injecting pulses to the LC oscillator using a switch, the method of shortening complimentary nodes is often used as shown in Figure 3.22. However, in the proposed design, the output node is shorted to GND using an NMOS switch. The reason why the structure of shortening the GND and output clock nodes is used is that sufficient injection strength can be obtained even if a smaller NMOS is used than the shortening method

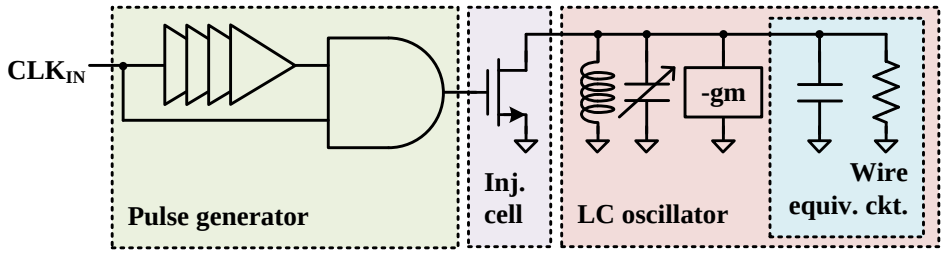

Figure 3.21. Injection cell and pulse generator.

of the complimentary node. The simulated PDR curve along the width of the NMOS (2 μm, 4 μm, 6 μm) is shown in the Figure 3.23. The results of the injection lock range simulation when using such an injection cell are shown in Figure 3.24. The 2-um width injection cell is used and it is the result of the input injection into the free running oscillator without frequency tuning.

The pulse used for injection is generated simply by using a delay line and an AND gate so that the power consumption is minimized. The pulse width that has a decisive effect on the injection strength is the same as the delay time of the delay line, and is generally used at about a quarter of the clock period. The delay line is digitally controlled by the 6-bit control signal and the delay of it is designed to be adjustable from 20- 90 ps.

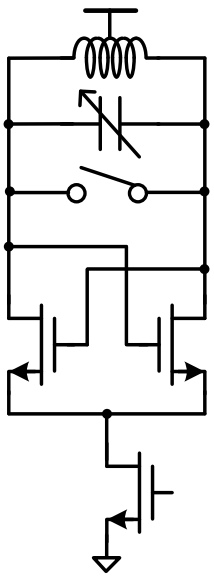

Figure 3.22. Conventional design of injection-locked LC oscillator.

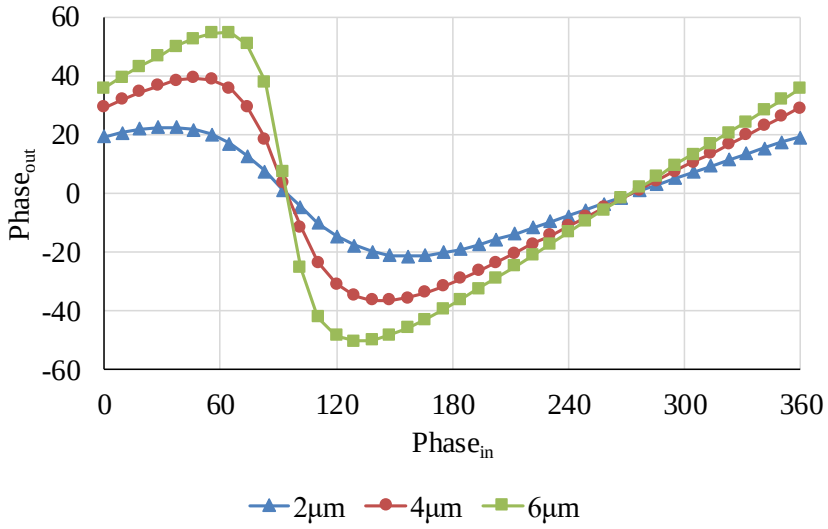

Figure 3.23. PDR curve of the injection cell.

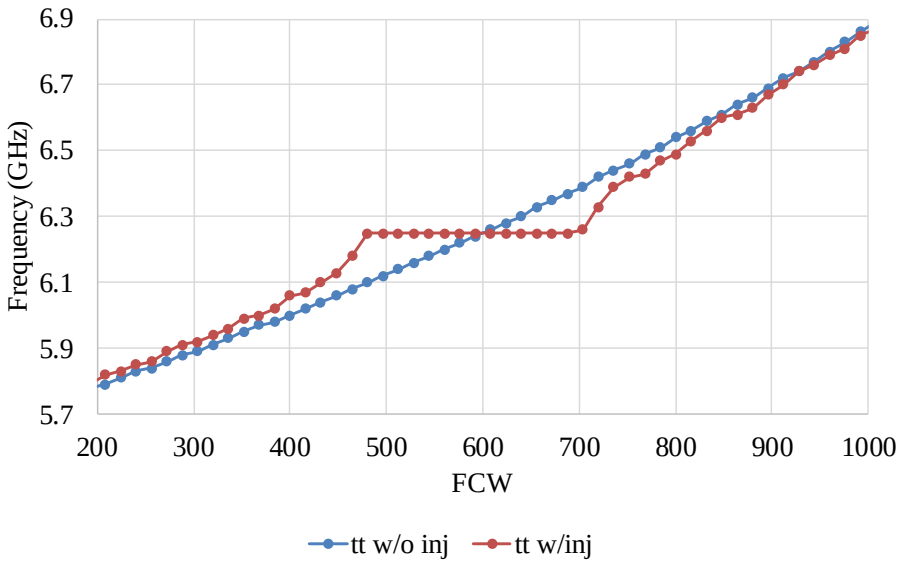

Figure 3.24. Injection lock range simulation.

However, the single-phase pulse injection structure has a problem as shown in the Figure 3.25. In most ILOs, it is common that the clock distortion occurs while the injection cell is switched on. However, in this single-phase injection structure, since the input is injected into one of the four phases, distortion occurs only in one of the quadrature clocks. This asymmetric distortion causes quadrature phase error and may cause problems in quarter-rate circuit operation. According to the simulation results shown in the Figure 3.25, phase error of about 2° may occur. To remove the phase error, it is recommended to remove asymmetric distortion using a poly-phase filter (PPF) or phase error correction circuits.

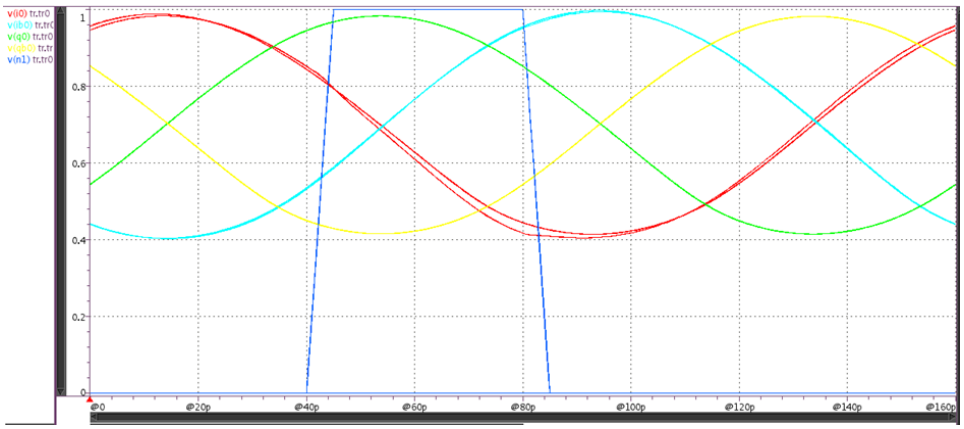

Figure 3.25. simulation result of the asymmetric distortion of output clock.

3.7.3 Quadrature Clock Injection

As discussed in the previous section, when only a single-phase pulse is injected into a quadrature oscillator, distortion occurs in the quadrature output clock, causing a problem of phase error. Since the phase error of the multi-phase clock can cause problems in a multi-rate system using the clock, a method other than single-phase injection may be an alternative.

Quadrature clock injection is one of the injection methods that can prevent clock skew. As shown in the Figure 3.26, asymmetric distortion can be prevented by injecting the input to the quadrature oscillator using a differential pair. It also has the advantage of not requiring a pulse generator because it is a differential pair structure.

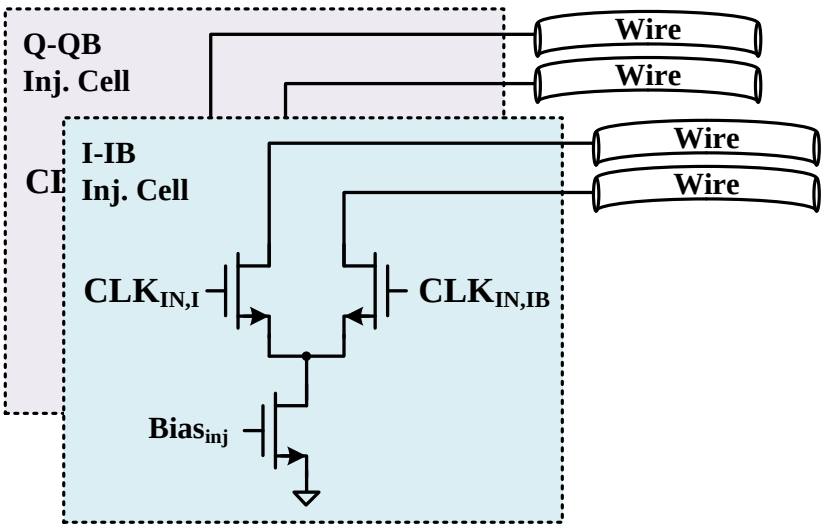

Figure 3.26. Quadrature clock injection scheme.

Therefore, this structure is suitable for applications where the input clock is not a single-ended multi-phase clock. If the input clock is a single-ended or differential clock rather than a quadrature, a multi-phase generation block such as PPF or delay locked loop is required. In this case, the quadrature clock injection method is not suitable because design complexity and power consumption may increase.

Chapter 4

Measurement

4.1 Overview

The prototype chip of the proposed quadrature resonant clocking scheme has been fabricated in 65-nm CMOS technology and photomicrograph of the chip is shown in the Figure 4.1. The active area of the prototype chip occupies an area of 0.004 mm^2. The prototype chip includes quadrature clock distribution wires, proposed quadrature resonant clock generator, two inductors, two tuning capacitors, sine wave-to-full-swing CMOS converters (S2C converter) for comparison with other types of clock distribution buffers, and a monitor circuit for measuring the internal clock amplitude. The measurement setup is depicted in Figure 4.2.

There are two ways to measure the quadrature phase of the high frequency output clock. One is to measure the waveform of the high frequency quadrature clock directly,

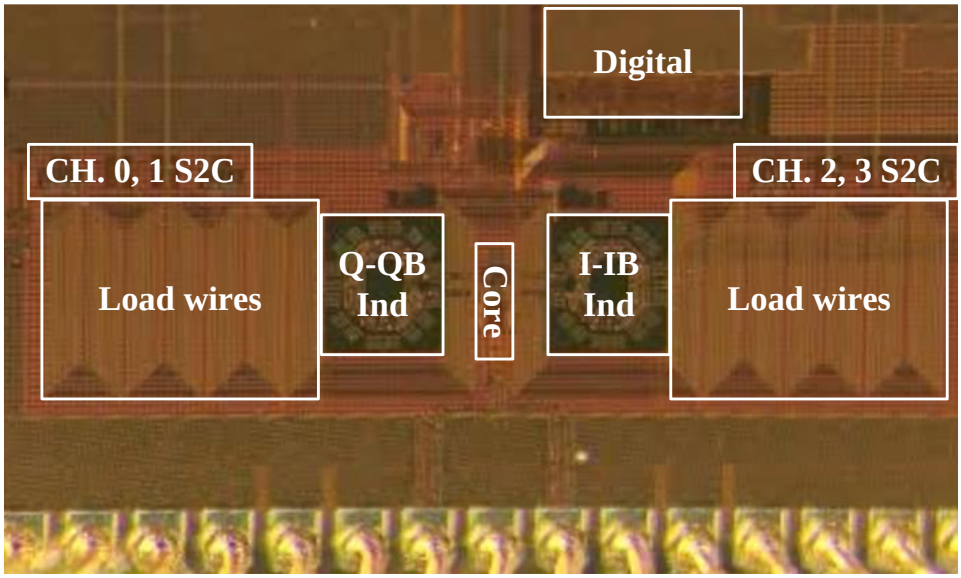

Figure 4.1. Photomicrograph of the prototype chip.

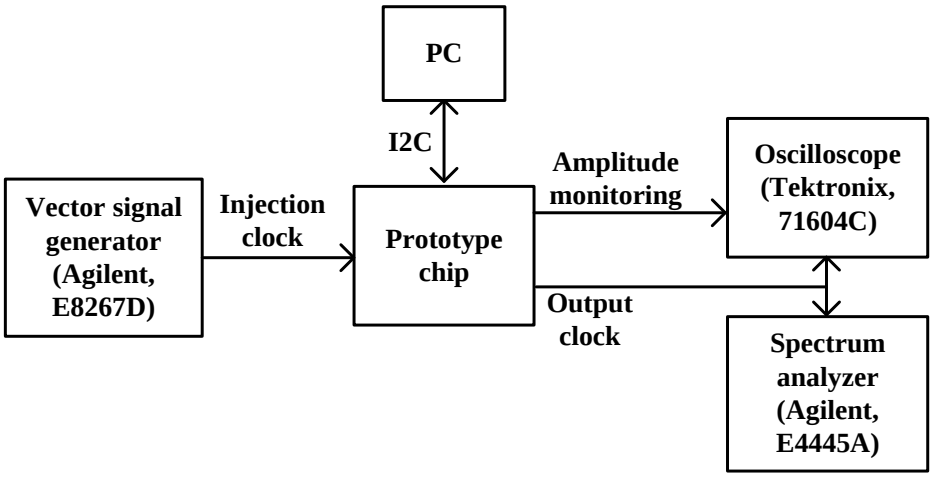

Figure 4.2. Measurement setup.

and the other is to measure the clock waveform that is down converted using a mixer as shown in the Figure 4.3 [46] . The down converting method using a mixer is a method of measuring the waveform of a clock with a low frequency while maintaining the phase of the quadrature output clock. Therefore, it has the advantage of being less affected by external noise. However, there is a difficulty in that a clock having a frequency similar to the frequency of the output clock is additionally required. Therefore, in the proposed quadrature resonant clocking scheme, a method of directly measuring the waveform of the output clock is used. Also, as shown in the Figure 4.4, a method of sharing output path of the quadrature clock using multiplexer (MUX) is used to minimize delay mismatch in the output path.

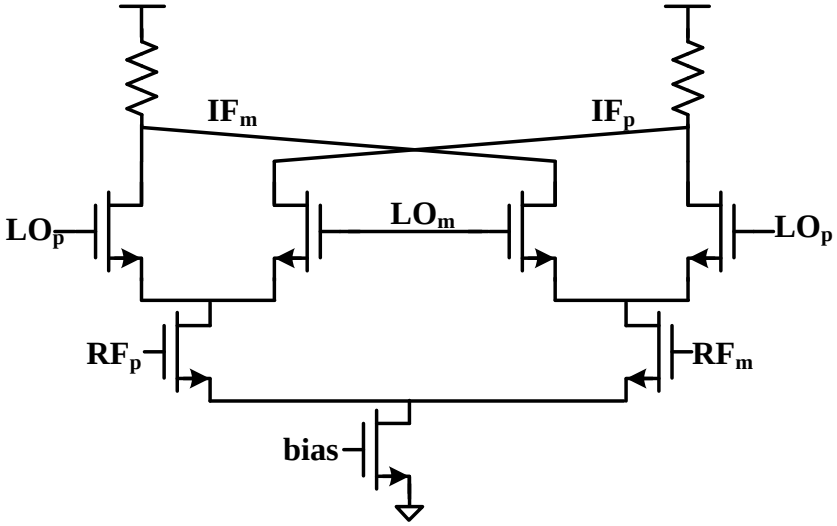

Figure 4.3. Gilbert mixer.

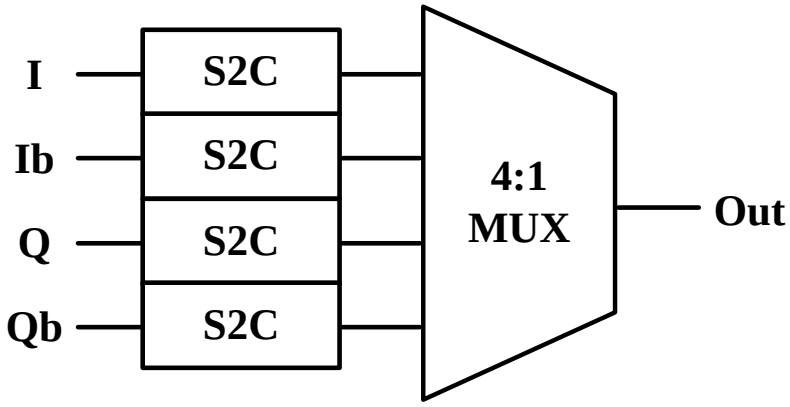

Figure 4.4. Output stage of the output quadrature clock using MUX.

4.2 Power Consumption

Measured total power consumption of the proposed quadrature resonant clocking scheme is 11.92 mW at the operation frequency of 7 GHz. The LC quadrature oscillator core including the negative gm cell and the quadrature coupling cell consumes 6.2 mW and the remainder is consumed by 4-channel S2C converters and a pulse generator. Detailed power breakdown of the proposed quadrature resonant clocking scheme is described in the Table 4.1.

To compare the power consumption of the proposed quadrature resonant clocking scheme and the other types of clock distribution buffers, a CMOS-based buffer and a CML-based buffer that distribute the clock on the same load wires as that used by the proposed resonant clocking scheme are designed and simulated.

The proposed quadrature resonant clock scheme consumes about 20-25% less power when compared with CMOS-based clock as depicted in the Figure 4.5. In addition, proposed quadrature resonant clocking scheme shows a large reduction in

Table 4.1. Power breakdown.

Block	Power (mW)
Quadrature core	6.2
Pulse generator	0.5
S2C	5.2

power consumption in all frequency ranges.

The Figure 4.6 shows the comparison with CML-based clock buffers when the clock peak-to-peak swings are varied. When driving the same wire, the proposed scheme consumes 23-34% less power than the CML-based clock buffers with the same peak-to-peak swing.

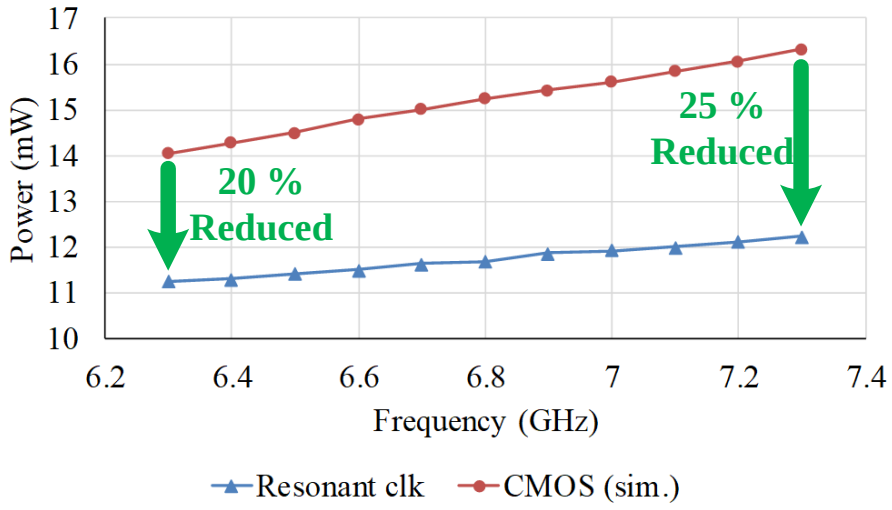

Figure 4.5. Total power consumption compared with CMOS-based clock buffer.

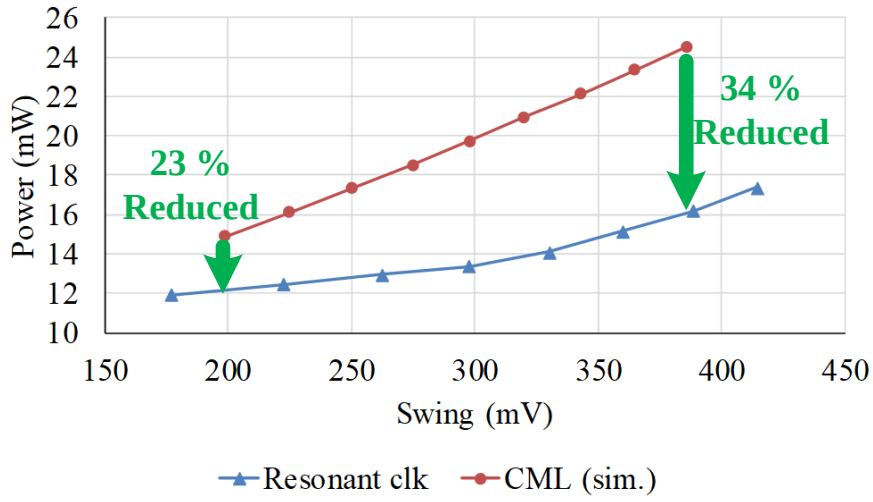

Figure 4.6. Total power consumption compared with CML-based clock buffer.

4.3 Internal Amplitude Monitoring

In order to verify the operation of the amplitude control loop, it is necessary to be able to measure the amplitude of the clock inside the chip. The circuit shown in the Figure 4.7 is the amplitude monitoring circuit which consists of a sampler and a delay line. By 2-dimensional sweep of V_{REF} and V_{CTRL} which controls the delay of the sampling clock, the internal clock waveform can be measured as presented in the Figure 4.8. It is difficult to measure the phase of the clock perfectly due to the problem of the sampler offset, hysteresis characteristic of the sampler, random noise, and linearity of the delay line, but the maximum, minimum value and peak-to-peak amplitude of the internal clock can be measured. The measured values are 0.965 V, 0.716 V, 0.249 V respectively.

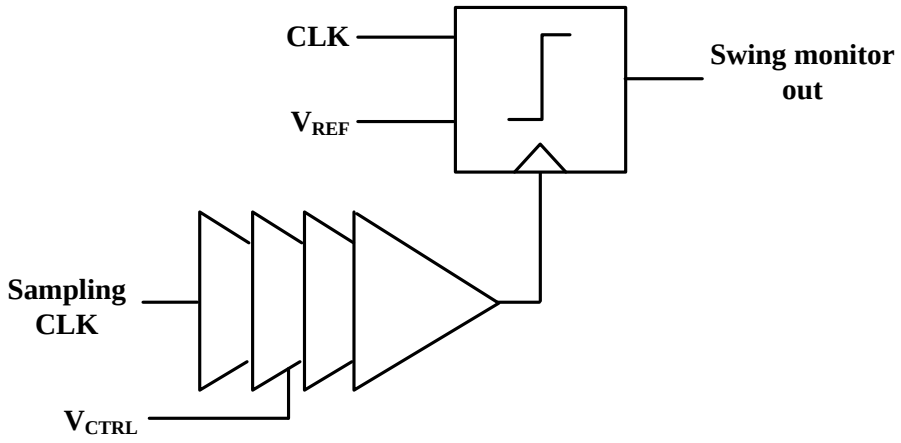

Figure 4.7. Internal amplitude monitoring circuit.

The Figure 4.9 shows the measured amplitude of the internal clock when the amplitude control feedback loop is enabled or disabled when the current bias of the negative gm cell is arbitrarily changed. When the amplitude control feedback loop is enabled, the amplitude of the clock remains constant even if the external conditions change.

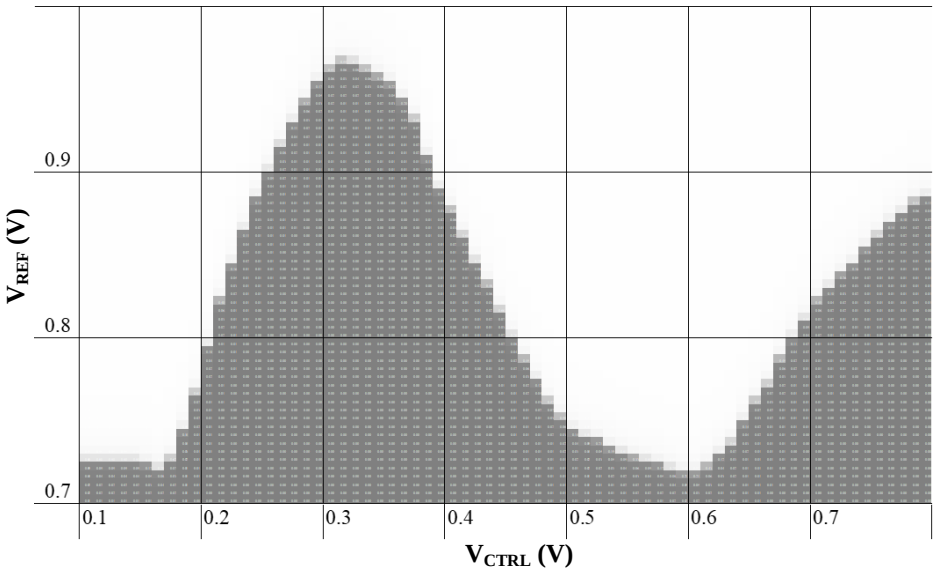

Figure 4.8. Measured internal clock waveform.

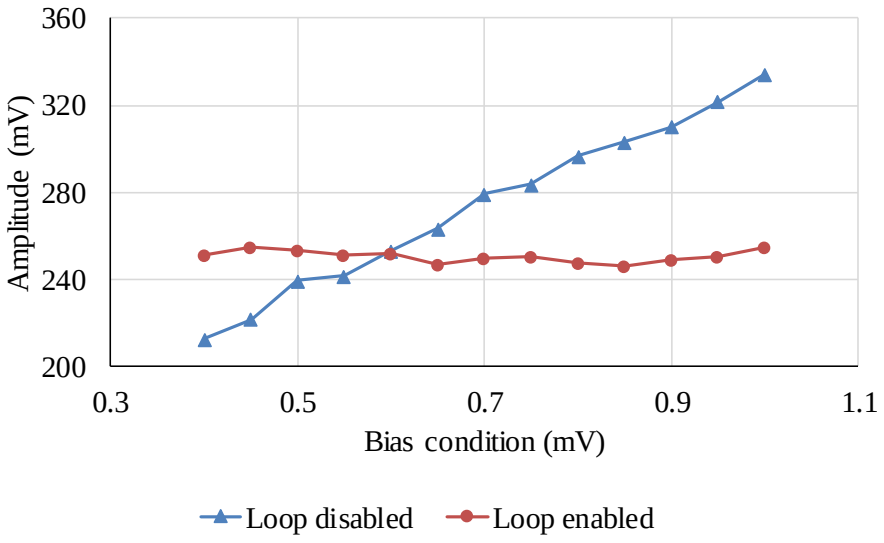

Figure 4.9. Amplitude control loop functionality test result.

4.4 Output Clock Characteristic

The waveform of the output clock of the proposed quadrature resonant clocking scheme is measured as shown in the Figure 4.10. The phase error of the four phases are measured as less than 3°. 1-UI period jitter is measured as 573.6 fs_{rms}.

Figure 4.11 shows the phase noise plot of the output clock in 7-GHz operation and measured result is -138.37 dBc/Hz at 1 MHz offset. Meanwhile, Figure 4.12 shows the phase noise plot of the 7-GHz input clock and measured result is -137.31 dBc/Hz

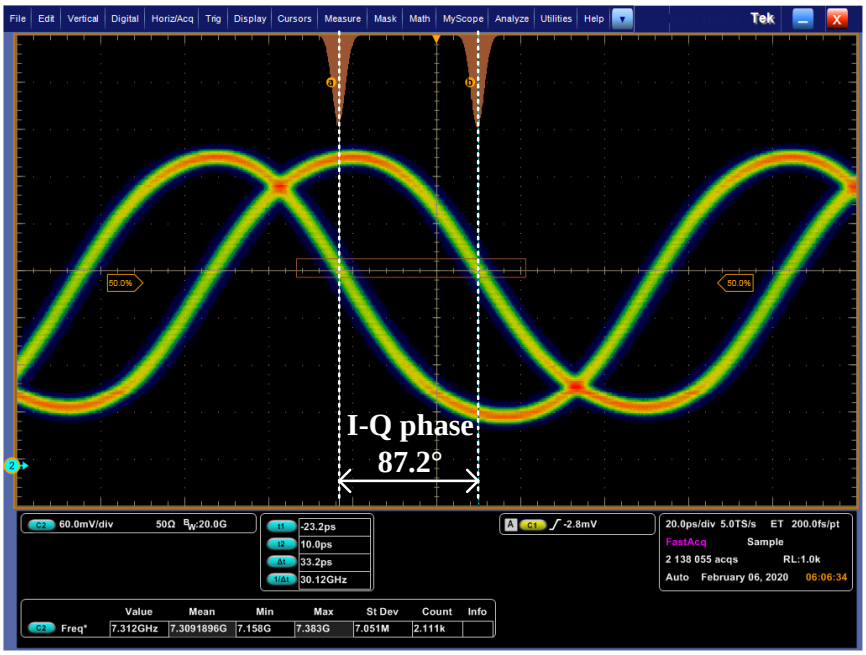

Figure 4.10. Waveform of the output clock.

at 1 MHz offset. Just as the well-designed, tuned ILO exhibits the lowpass jitter filter characteristics on the oscillator phase noise, the proposed clock generator offers very low jitter limited by the phase noise of the input clock source. The measurement results of phase noise when matched or unmatched resonant and operation frequencies are shown in the Figure 4.13. Phase noise performance is better when the resonant frequency is tuned to the operation frequency compared with the case when the operation frequency is changed while the resonant frequency is fixed at 7 GHz.

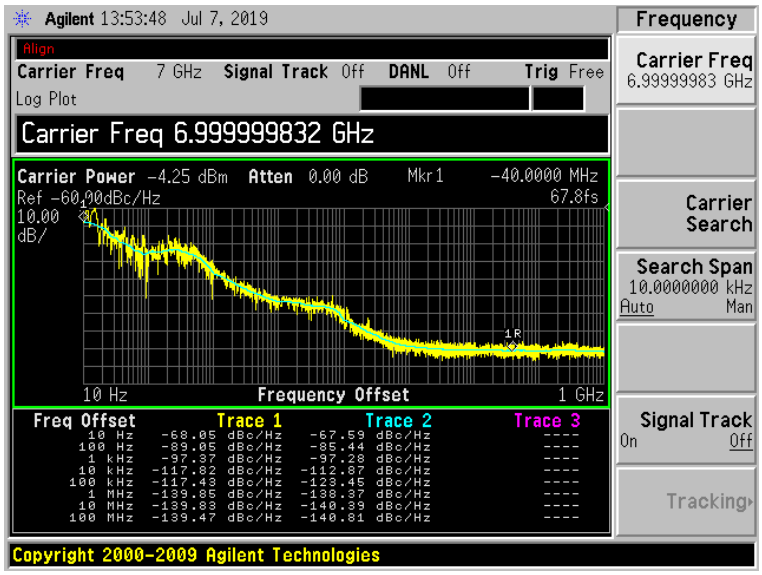

Figure 4.11. Phase noise of the output clock at 7 GHz operation.

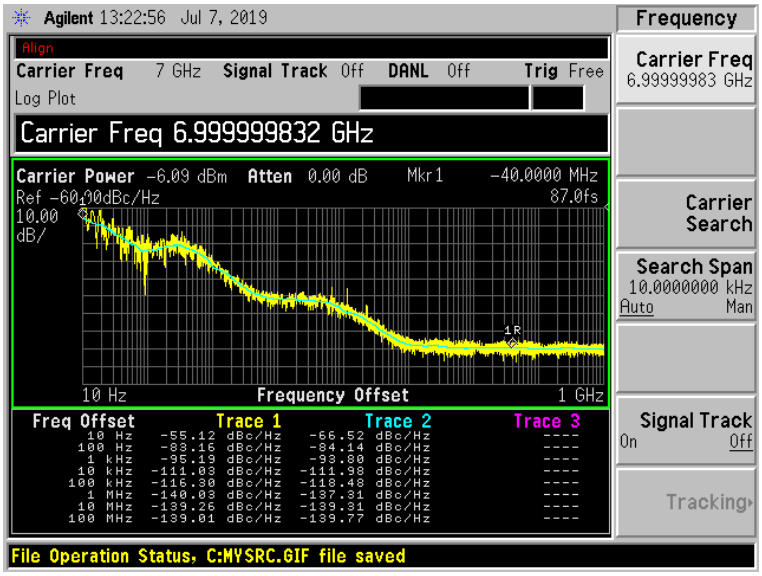

Figure 4.12. Phase noise of the input clock.

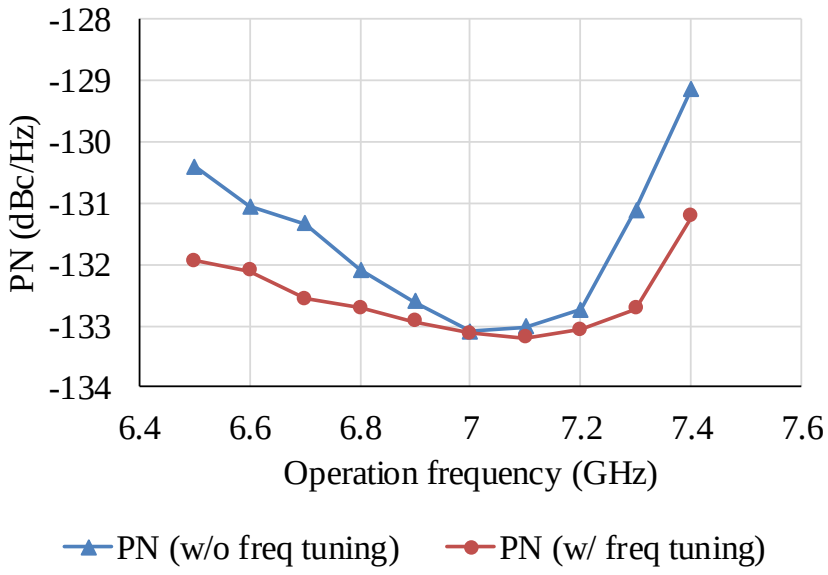

Figure 4.13. Phase noise comparison w/ and w/o frequency tuning

4.5 Summary

The performance of the proposed quadrature resonant clock is summarized and compared with the previous works in the Table 4.2. The proposed quadrature resonant clock, when compared with the conventional resonant clocks, exhibits the high power reduction ratio under all operating conditions by tuning out the frequency mismatch using the frequency tuning capacitors. Because of the [7] and [27] has 830 and 16 sectors respectively, it is unfair to simply compare total power. Therefore, the following figure of merit (FoM) is suggested.

$$FoM = \frac{(Total\ power)}{(Load\ wire\ capacitance) * (Frequency)}. \quad (4.1)$$

Table 4.2. Table comparing proposed quadrature resonant clock with the state-of-the art scheme.

	Chan, JSSC'09 [7]	**Sathe, JSSC'13 [8]**	**Xu, JSSC'09 [27]**	**Restle, ISSCC'14 [35]**	**This Work**
Technology	90 nm	32 nm SOI	0.18 um	22nm SOI	65 nm CMOS
Type	Single-ended	Single-ended	Single-ended	Single-ended	Quadrature
Load wire capacitance	2 nF	N/A	100 pF	N/A	2.236 pF
Inductance	1.2 nH	0.5-1.3 nH	3 nH	0.3-2.5 nH	0.95 nH
Number of inductors	830	5	16	N/A	2
Q factor	1.6	3.6-3.8	N/A	N/A	4.56
Frequency	4-5 GHz	0.5-4 GHz	2 GHz	2.5-5 GHz	6.3-7.3 GHz
Total power	24 W	N/A	500 mW	N/A	11.92 mW
Power reduction	5-25 %	0-35 %	N/A	0-37 %	20-34 %
FoM	2.4 mW/pF/GHz	N/A	2.5 mW/pF/GHz	N/A	0.76 mW/pF/GHz

Chapter 5

Conclusion

In this thesis, a 7 GHz quadrature resonant clocking scheme with the resonant frequency tuning capacitors and amplitude control feedback loop is described. The proposed resonant clocking scheme distribute the input clock through 4.3 mm load wire which capacitance is almost 600 fF.

By using the tuning capacitor, frequency difference between the operation frequency and the LC resonant frequency is barely exist. By reducing the frequency mismatch, optimized power reduction is achieved under the all operation condition while reducing the phase noise. Also, the amplitude control feedback loop is employed to maintain the constant clock amplitude under PVT variations.

A prototype chip fabricated in 65-nm CMOS technology occupies 0.004 mm^2, and consumes 11.92 mW at 7 GHz. The quadrature oscillator core consumes 6.2 mW Power reduction is between 20% to 25% when compared with the CMOS-base clock buffers and 23% to 34% when compared with conventional CML-based clock buffers.

Measured phase noise of the output clock is -138.37 dBc/Hz at 1 MHz offset while phase noise of the input clock is -137.31 dBc/Hz at 1 MHz offset. The proposed clock generator offers very low jitter limited by the phase noise of the input clock source. The phase error of the quadrature phases is measured as less than 3°. 1-UI period jitter is measured as 573.6 fs_{rms}.

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초 록

본 논문에서는 클럭 전달을 위한 4.3mm 전선을 통해 클럭을 전달하는 회로를 인덕터와 커패시터의 공진현상을 이용해서 저전력을 소모하여 설계할 수 있는 방법을 제시한다. 또한 두 개의 피드백 루프를 포함하고 있다. 주파수 조절을 위한 피드백 루프는 공진 주파수를 조절하여 동작 주파수와의 차이를 제거한다. 그렇게 함으로써 모든 주파수 조건에서 저전력, 고효율 동작이 가능해지며 위상 노이즈 및 지터 특성도 좋아진다. 진폭 조절을 위한 피드백 루프는 외부 조건이 변화하는 상황에서도 일정한 진폭을 가지는 클럭이 나오도록 한다. 이러한 내용들을 검증하기 위하여 65nm CMOS 공정을 이용하여 프로토타입 칩을 제작하였다. 전력 소모 측정 결과, 본 논문에서 제안하는 방식은 11.92mW 의 전력을 소모한다. 또한 기존에 사용해왔던 CMOS 방식의 클럭 전달용 버퍼에 비해서는 같은 주파수 조건에서 약 20-25% 가량 적은 전력을 소모한다. 그리고 CML 방식의 버퍼와 같은 진폭을 가지는 경우로 비교하는 경우에는 약 23-34% 가량 적은 전력을 소모한다. 지터는 측정 결과 $573.6fs_{rms}$ 로 확인되었고, 1MHz 오프셋에서의 위상 노이즈는 -138.37dBc/Hz 로 측정되었다.

주요어 : 주입 고정 발진기, 주파수 조정, 진폭 조절 피드백 루프, 클럭 전달, 쿼드러처 레조넌트 클럭

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Ph.D. Dissertation

Quadrature Resonant Clock with Frequency Tuning Capacitor and Amplitude Control Feedback Loop

주파수 보정과 진폭 조절 피드백 루프를 포함한
쿼드러처 레조넌트 클럭의 설계

by

Chang-Soo Yoon

August, 2020

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Quadrature Resonant Clock with Frequency Tuning Capacitor and Amplitude Control Feedback Loop

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Quadrature Resonant Clock with Frequency Tuning Capacitor and Amplitude Control Feedback Loop

by

Chang-Soo Yoon

A Dissertation Submitted to the Department of
Electrical and Computer Engineering
in Partial Fulfillment of the Requirements for the Degree of
Doctor of Philosophy
at
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August, 2020

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Abstract

This thesis presents a quadrature resonant clock generator for driving four 4.3-mm load wires with tuning capacitors and an amplitude control feedback loop. By using frequency tuning capacitors, which reduce the mismatch in operation and LC resonant frequencies, the proposed clock generator offers power reduction by 20-25% compared with conventional CMOS clock driver and by 23-34% compared with conventional CML clock driver over a wide voltage swing. The amplitude control feedback loop, which determines the bias current of the negative gm cell, maintains the constant optimized clock swing over wide PVT variations. Measurement result from the prototype chip fabricated in 65 nm CMOS shows that total power consumption of the proposed quadrature resonant clock is 11.92 mW in 7-GHz operation with four 559-fF load wire capacitances. Measured period jitter is 573.6 fs_{rms} and phase noise at 1MHz offset is -138.37 dBc/Hz.

Keywords : Amplitude control feedback loop, clock distribution, frequency tuning, injection locking oscillator, quadrature resonant clocking.

Student Number : 2012-20820

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Chapter 1

Introduction

1.1 Motivation

As the technology develops and shrinks, two important challenges in designing high performance integrated circuit (IC) are to reduce power consumption and to extend the data bandwidth. In particular, considering the market expansion of the mobile devices including tablet devices, wearable devices such as augmented reality (AR) and virtual reality (VR) machines, and internet of things (IoT), low power IC design is very important since the limited battery size and hence the weight of the mobile devices can be proportionally decreased. Furthermore, as shown in the Figure 1.1, in power-hungry data centers for telecommunications, storage systems cloud services, cooling cost could reach 50% of the total energy consumption due to energy loss of the integrated circuits [1] -[4] .

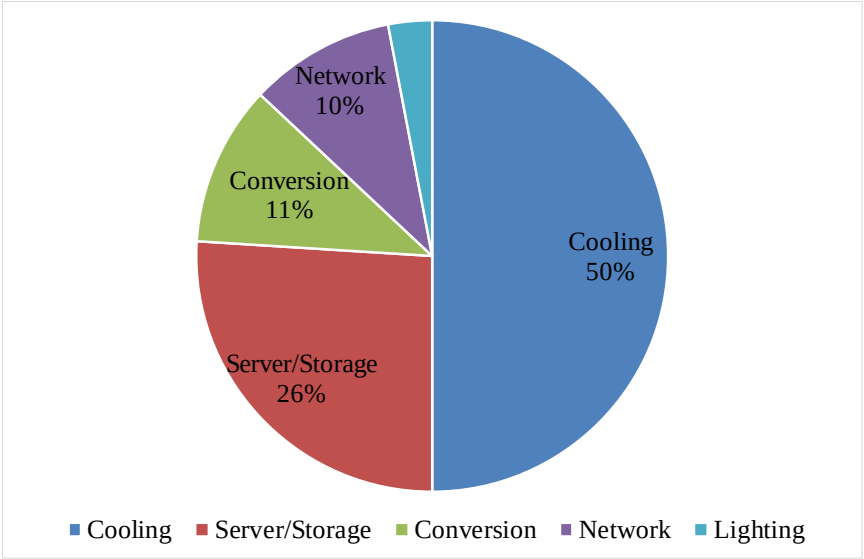

Figure 1.1. Typical data center energy consumption.

Meanwhile, in order to extend the data bandwidth, the frequency of the clock used in the system must also be increased or multi-rate clock system such as quadrature clocking should be used. However, the conventional clock distribution system typically takes up 15-40% of the power consumption of the entire chip [5] -[8] . In general, the conventional clock trees are composed of the complementary metal–oxide–semiconductor (CMOS) or current-mode logic (CML) type clock repeaters which are the easiest and simplest method of the clock distribution system. However, the CMOS type clock repeaters have the disadvantage that there is a bandwidth limitation, and the CML type clock repeaters have the disadvantage that it consumes a lot of power. Therefore, the resonant clocking, one of the methods to reduce clock tree power consumption, has been studied and applied in very-large-scale integration (VLSI) systems [7] -[35] .

Generally, most of the resonant clocking applications are constructed using wire parasitic capacitors with fixed value inductors [7] -[30] . LC resonance between the parasitic capacitors and the inductors is used to reduce the power consumed in the clock switching process. In those cases, which is using fixed value inductors for LC resonance, a mismatch between the resonant frequency and the operation frequency which is the intended target frequency of the output clock may occur due to PVT variations. If there is a significant difference between the two frequencies, the LC tank can be degenerated as a passive load rather than a resonator, which increases power consumption. Thus, a tuning mechanism must be incorporated to fully optimize the performance especially in a varied frequency range. One way to solve this problem is to use two or more inductors to change the resonant frequency using a switch for selection [31] -[35] . However, this method also suffers from the additional power consumption due to the series resistance of the switch which degrades Q of the resonator. In addition, there is also a mode control issue when the inductor is switched and the operating mode is changed.

To solve these problems, the proposed quadrature resonant clock uses a frequency tuning capacitor in the LC oscillator. The operation and resonant frequencies are matched by using a frequency tuning capacitor in a phase-locked loop (PLL) during power-up. In that way, the best power reduction can be achieved over a wide operation frequency. In addition, the quality of the clock, such as phase noise, is improved as well when there is less frequency mismatch. Also, the proposed resonant clock is implemented by quadrature to provide four-phase clock in quarter-rate systems.

1.2 Thesis Organization

This thesis is organized as follows. In Chapter 2, background information about the quadrature resonant clocking scheme is described. The features, design issues, advantages and the disadvantages of the prior works which are the basic conventional resonant clocking scheme, standing-wave oscillator, resonant clocking scheme using inductor tuning are organized and discussed. Also, the basic concept of the proposed quadrature resonant clocking scheme is briefly introduced followed by the basic theory of the injection-locked oscillator and LC quadrature oscillator. The phase domain response of the injection-locked oscillator and the bi-modal operation of the LC quadrature oscillator is analyzed briefly.

In Chapter 3, the proposed quadrature resonant clocking scheme is described. The overall architecture of the proposed quadrature resonant clocking scheme is depicted and functionality is explained. Then, the design method of the clock distribution wire is analyzed using RC ladder model of the wire and Q factor calculation. Design of the LC quadrature oscillator core including negative gm cell, quadrature coupling cell and delay cell preventing bi-modal operation is described followed by the explanation about two feedback loops – frequency control loop and amplitude control loop. In the last section of the Chapter 3, two types of the injection cell are described with some simulation results.

In Chapter 4, the measurement results of the prototype chip are presented. The power consumption of the proposed quadrature resonant clocking scheme is measured, and compared with the power consumption of the two types of the conventional clock

distributing methods. By using the amplitude monitoring circuit, the waveform of the internal output clock is measured. Also, the phase noise, jitter of the output clock is measured. And phase error of the quadrature clock is measured. At the end of the Chapter 4, the proposed quadrature resonant clocking scheme is compared with the prior works of conventional resonant clocking scheme, and summarize the advantages of the proposed scheme.

Finally, Chapter 5 summarizes the proposed works and concludes this thesis.

Chapter 2

Background on Quadrature Resonant Clock

2.1 Overview

In recent years, As the mobile device market expands, the need for low-power circuit design is increasing. Furthermore, the frequency of clocks used in VLSI systems is getting faster and faster. In this situation, distribution of high quality, high frequency clocks to the entire local systems has become a very important factor in determining the performance of the VLSI system. One of the methods of distributing clocks to the local system is using CMOS or CML type clock repeaters or using buffers in the middle of the loading wire as shown in the Figure 2.1 and Figure 2.2. However, using conventional repeaters as a method for distributing high frequency clocks

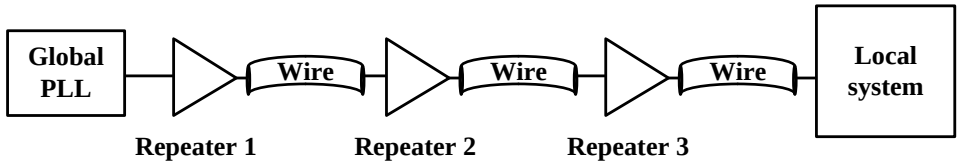

Figure 2.1. Clock distribution scheme using repeaters.

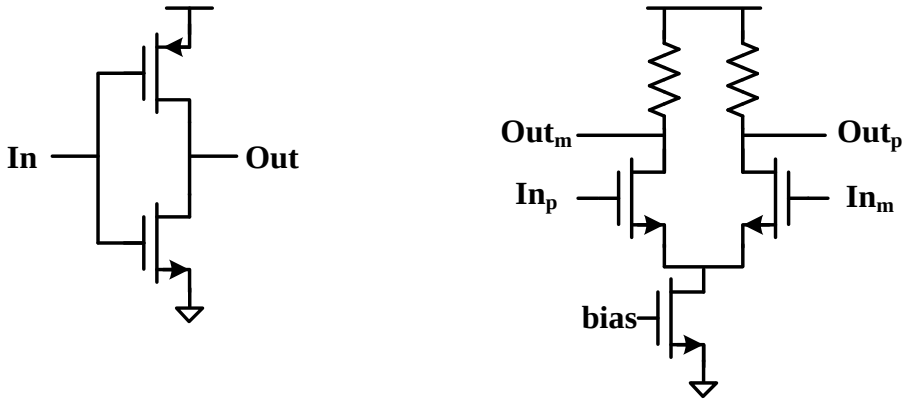

Figure 2.2. CMOS and CML type buffer.

has some problems. One is bandwidth limitation and the other is that buffers consume too much power. Furthermore, the circuit that consumes a lot of power is vulnerable to supply noise, so the quality of the clock such as jitter and phase noise deteriorates and the performance of the entire circuit is also deteriorated when using conventional CMOS or CML based repeaters.

To solve the problems of consuming too much power, the resonant clocking, one of the powerful methods to reduce clock distribution power consumption, has been studied for a long time. However, the conventional resonant clocking scheme has

frequency mismatch problem. Therefore, to solve this frequency mismatch problem, the quadrature resonant clocking scheme using resonant frequency tuning capacitor is proposed in this thesis.

In this chapter, before explaining the proposed quadrature resonant clocking scheme in the later chapter, conventional resonant clocking scheme is firstly described followed by an explanation about the scheme using multiple inductors. And proposed quadrature resonant clocking scheme and basic theory of injection-locked oscillator and LC quadrature oscillator is described in the later sections.

2.2 Prior Works

2.2.1 Basic Resonant Clocking Scheme

The most basic and simplest resonant clocking scheme which is conventionally used to reduce the clock tree power consumption is shown in the Figure 2.3. A simple resonant clocking scheme is a structure in which an inductor considering the operating frequency and wire parasitic capacitance values is added to the clock tree structure using the basic clock buffers. This simple structure can be found in [7] -[23] and [25] -[27] , and it can be confirmed that many processors are used this structure to reduce the power used for clock distribution.

The basic principle of resonant clocking to reduce power consumption is as follows. As the resonance occurs in the LC tank, the impedance at the buffer output stage decreases which is shown in the Figure 2.4, so the clock can be distributed using less power. In this structure, the ratio of the reduced power is determined by the value of the Q factor of the entire load wire and inductor. For example, when the Q factor of the load wire and the entire inductor is 3, the power consumption is reduced to a third when the resonant clocking scheme is used compared to when the resonant clocking scheme is not used. Therefore, proper wire and inductor design that determines the overall Q factor is an important factor in determining the performance of resonant clocking.

However, this simple structure has a fatal problem. In a situation where the resonant frequency determined by the load wire parasitic capacitance and the inductance

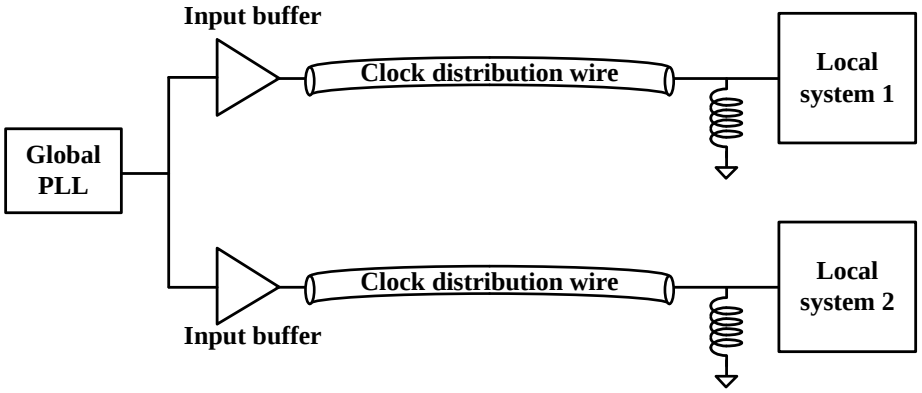

Figure 2.3. Block diagram of the basic resonant clocking scheme.

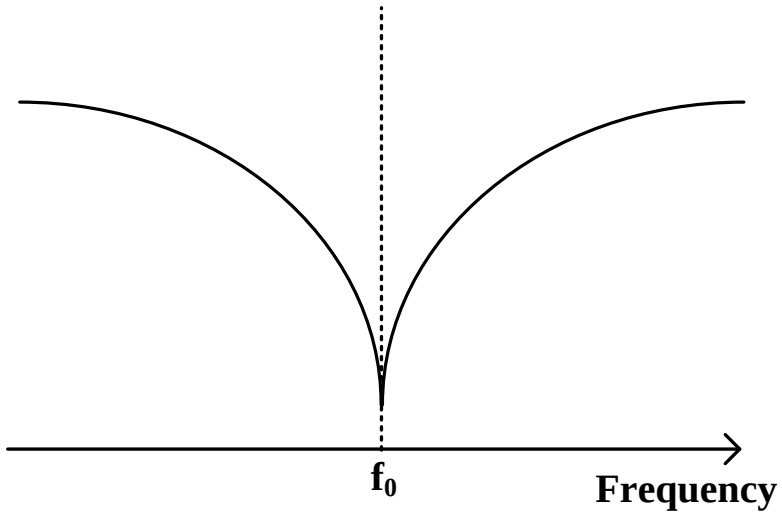

Figure 2.4. Impedance of LC tank

and the actual operating frequency of the system are different, the impedance at the buffer output stage is larger than the target value, so power consumption cannot be sufficiently reduced. Therefore, this basic structure is vulnerable to process mismatch and is not suitable for applications having a wide frequency range in which the operating frequency is not set to a single value.

Therefore, a resonant clocking structure using multiple inductors has been studied to solve these problems and apply a resonant clocking scheme to applications having a wide frequency range.

2.2.2 Standing-Wave Oscillator

The standing-wave oscillator, a type of resonant clocking scheme, is implemented as distributed oscillator, with gain elements such as cross-coupled inverters uniformly spaced throughout the clock network in order to overcome losses [28] -[30] . The basic resonant clocking scheme in Figure 2.3 is mainly used with H-tree to distribute clocks to the local sectors, whereas standing-wave oscillators are mainly used for global clock distribution. Therefore, as shown in Figure 2.5, the standing-wave oscillator is designed in such a way that the inductor is connected to the ring-shaped distribution wire or the mesh surrounding the entire chip. In general, the length of the clock distribution wire is very long, so it is important to arrange the inductors uniformly and well.

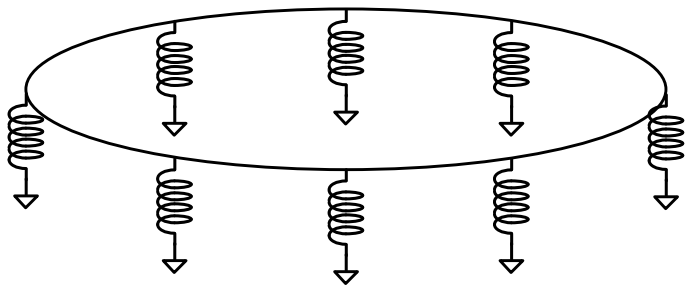

Figure 2.5. Basic structure of the standing-wave oscillator.

2.2.3 Resonant Clocking Scheme Using Multiple Inductors

The basic resonant clocking scheme using only one inductor has a problem that power consumption cannot be effectively reduced when the resonant frequency and operation frequency are different. If there is a significant difference between the two frequencies, the LC tank can be degenerated as a passive load rather than a resonator, which increases power consumption. One way to solve this problem is to use two or more inductors to change the resonant frequency using a switch for selection as shown in the Figure 2.6. This structure using multiple inductors is mainly used for to applications having a wide frequency range [31] -[35] because the clock distribution power consumption can be effectively reduced over a wider range than the basic resonant clocking method.

The principle of resonant clocking scheme using multiple inductors is to tuning the resonant frequency by changing the inductance in the LC tank. If one of the multiple inductors can be selected and used according to the situation, an inductor suitable for the operation frequency is selected. Since the resonance frequency is inversely proportional to the inductance, a larger inductor is used in the low frequency region and a smaller inductor is used in the high frequency region. At least one switch per inductor must be added to make this selection when compared to the basic resonant clocking structure.

However, the method of using these multiple inductors also has some problems. First, because a limited number of inductors cannot cover all the ranges, there is inevitably a frequency range that cannot optimize the reduction of clock tree power.

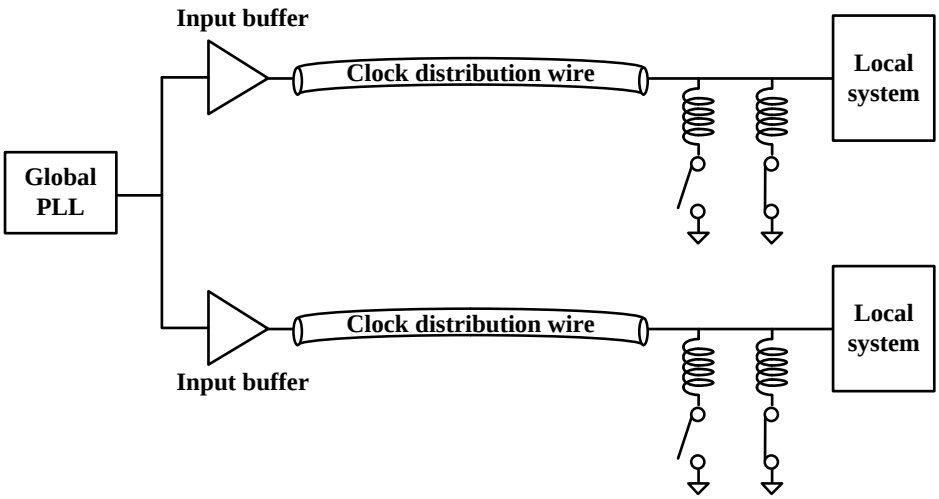

Figure 2.6. Block diagram of the basic resonant clocking scheme using multiple inductors.

Therefore, being vulnerable to process mismatch is the same as the basic resonant clocking scheme. Also, as the switch is used, the parasitic resistance component of the switch deteriorates the overall Q factor, which results in increased power consumption. In addition, the use of multiple inductors requires a large area, which is a problem of increasing the cost required to manufacture an IC.

Eventually, the method of tuning the resonant frequency by changing the inductance has problems due to the limitation of the characteristics of the inductor. Therefore, the method of tuning the resonant frequency by changing the capacitance of the LC tank is more suitable for the resonant clocking scheme.

2.3 Concept of the Proposed Quadrature Resonant Clock with Frequency Tuning Capacitor

As discussed in the previous sections, there are problems with existing resonant clocking designs. In the case of a design using one inductor, the impedance of the LC tank cannot be optimized when a difference occurs between the resonant frequency and the operation frequency. Therefore, it can be effectively operated only at one specified operation frequency and cannot be applied to applications with a wide frequency range. There is also the problem of being vulnerable to process mismatch affecting resonant frequency.

Even if you try to solve this problem by using multiple inductors, some problems that worsens the performance of resonant clocking still remain. The use of a finite number of inductors does not cover a continuous frequency range. There is also an optimization problem depending on the control method at the boundary of modes depending on which inductor is used. In addition, the series resistance of the switch used to selectively use the inductor exacerbates the Q factor, thereby increasing the power consumption used for clock distribution. In addition, there is a problem with too large an area caused by using multiple inductors.

In this thesis, as shown in the Figure 2.7, we propose a resonant clocking scheme that minimizes the difference between the operation frequency and the resonant

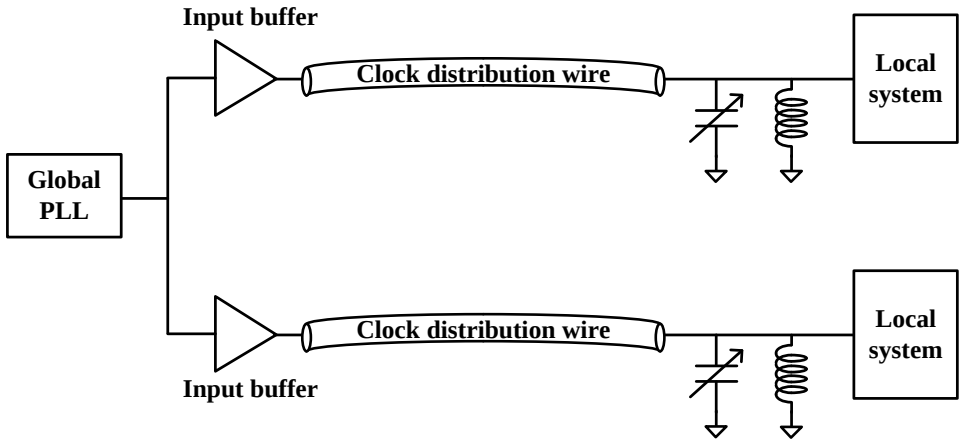

Figure 2.7. Basic concept block diagram of the resonant clocking scheme using frequency tuning capacitor

frequency by controlling the resonant frequency using a frequency tuning capacitor. Using this method, the resonant frequency can be adjusted to an appropriate value in a wide operating frequency range while using one inductor. Therefore, it is possible to obtain an optimized power reduction effect in all frequency ranges, cope with mismatches, and also have the advantage of not occupying a large area.

Additionally, the proposed quadrature resonant clocking scheme includes a feedback loop to control the amplitude of the output clock, thereby adjusting the amplitude change caused by the frequency tuning process and PVT variations to an optimized value. Detailed structural descriptions and details of circuit design and analysis related to Q factor are covered in later sections.

2.4 Injection-Locked Oscillator

2.4.1 Similarity Between the Resonant Clocking and the Injection-Locked Oscillator

The basic resonant clocking scheme which is shown in the Figure 2.3, consists of an input buffer, the load wire, and an inductor added for LC resonance. Considering that the load wire can be regarded as an RC lumped model, the structure of the load wire and the inductor can be said to be the same as that of the LC tank of the LC oscillator. Therefore, in the same way as the LC oscillator, the resistance component of the LC tank can be canceled by using a negative gm cell in the resonant clocking scheme. In addition, it can be considered that the input buffer of the basic resonant clocking scheme plays the same role as the injection cell used for the injection-locked oscillator (ILO). This similarity between the resonant clocking scheme and the ILO can be confirmed by the Figure 2.8 and the Table 2.1. Therefore, the design and the analysis method of ILO such as injection cell design, injection strength, injection locking range and phase domain response can be used to design and analyze the resonant clocking scheme.

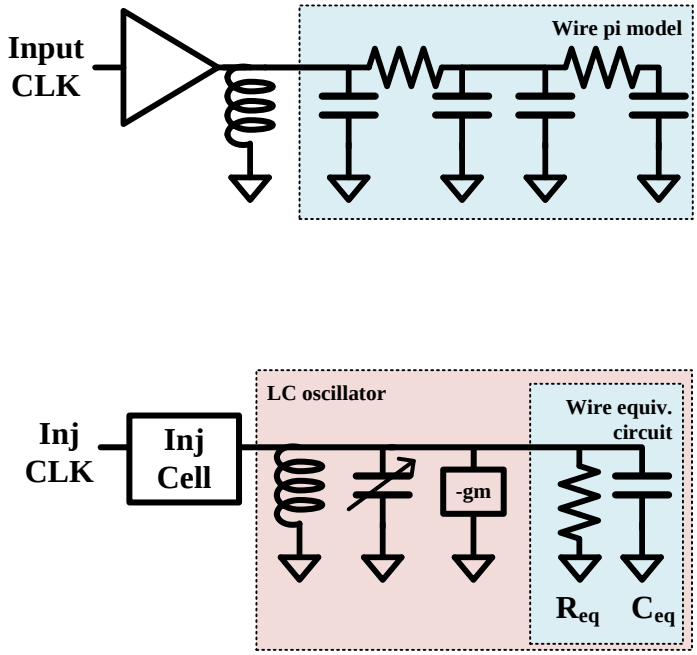

Figure 2.8. Similarity between resonant clocking scheme and ILO.

Table 2.1. Comparison between resonant clocking scheme and ILO.

Resonant clock	**ILO**
Input clock	Injection clock
Input buffer	Injection cell
Wire parasitic cap	Cap bank

2.4.2 Basic Principles of the Injection-Locked Oscillator

The first observed injection locking phenomenon is two pendulums moving synchronously when only the pendulums tied on the same bar close to each other. Adler defined the relationship between an injection signal and a free running oscillator, and behavior of an injection pulling. Razavi rewrote the relationship and presented about a locking range and a phase noise, etc.

The injection-locked oscillators are widely used in clock generators as shown in the Figure 2.9, Figure 2.10, Figure 2.11. The injection-locked frequency divider (ILFD) replaces the divider in PLL which operates at high frequency and consumes a lot of power. The injection-locked frequency multiplier (ILFM) is the one of the solutions to generate local oscillators in millimeter-wave band. The injection-locked clock multiplier (ILCM) can improve the performance of PLL.

The most basic parameters of the ILO are injection strength and locking range. In the case of the basic LC oscillator with injection shown in the Figure 2.12, for an example, the injection strength and single side locking range are defined as follows.

$$injection\ strength = \frac{I_{inj}}{I_{osc}} \tag{2.1}$$

$$\begin{aligned} locking\ range &= \frac{\omega_0}{2Q}\frac{\frac{I_{inj}}{I_{osc}}}{\sqrt{1-\left(\frac{I_{inj}}{I_{osc}}\right)^2}} \\ &\approx \frac{\omega_0}{2Q}\frac{I_{inj}}{I_{osc}} \end{aligned} \tag{2.2}$$

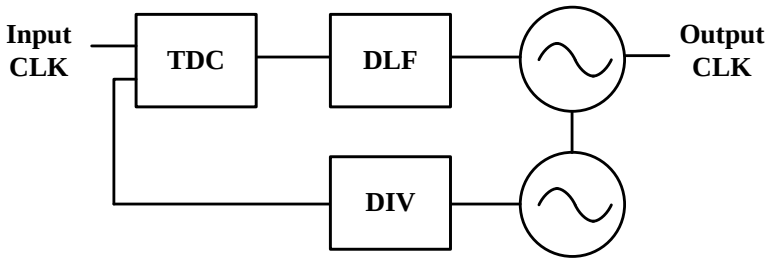

Figure 2.9. Injection-locked frequency divider.

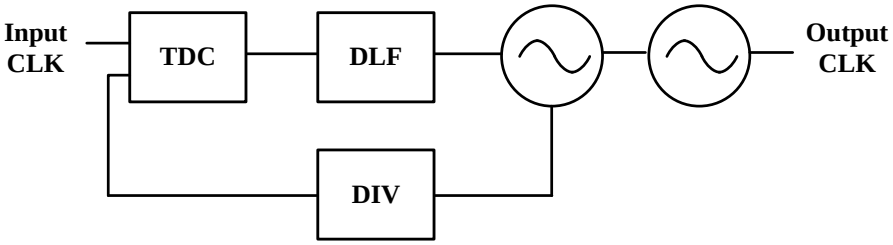

Figure 2.10. Injection-locked frequency multiplier.

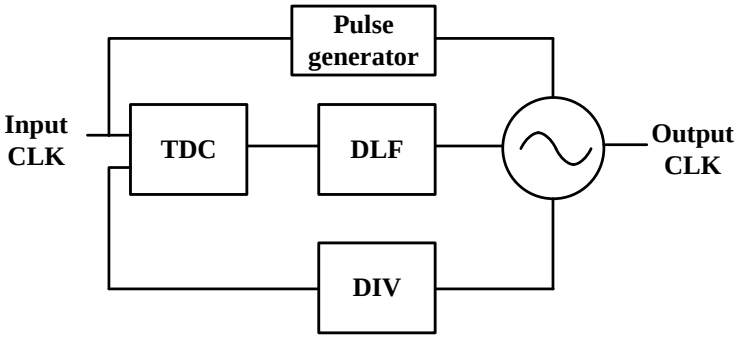

Figure 2.11. Injection-locked clock multiplier.

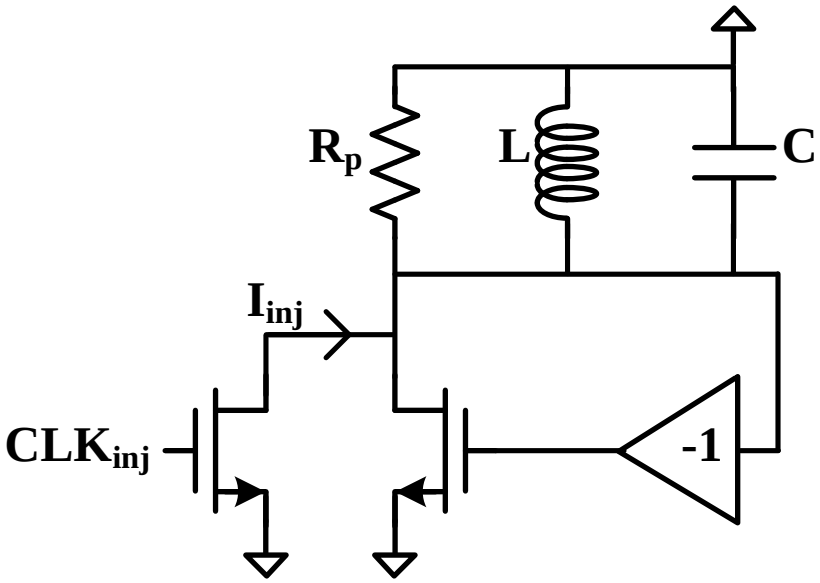

Figure 2.12. Basic LC oscillator with injection.

2.4.3 Phase Domain Response

The locking range of previous section is suitable only for the LC oscillator with sinusoidal wave injection, sinusoidal output not for the other types of oscillator such as ring oscillator and the ILO with pulse type injection. The analysis, based on the impulse sensitivity function (ISF) and phase domain response (PDR), make it possible to define the lock range more easily.

The phase of the output clock changes due to the effect of injection, and the amount of change depends on when injection is performed. PDR is a function of the relative phase of injection ϕ and shows the changed phase of the output clock as shown in the Figure 2.13. Considering the PDR curve in the Figure 2.14, the locking range can be defined as follows.

$$locking\ range = \frac{\omega_0(P_{max} - P_{min})}{2\pi N} \tag{2.3}$$

Where the N is frequency ratio between operation frequency and injection frequency.

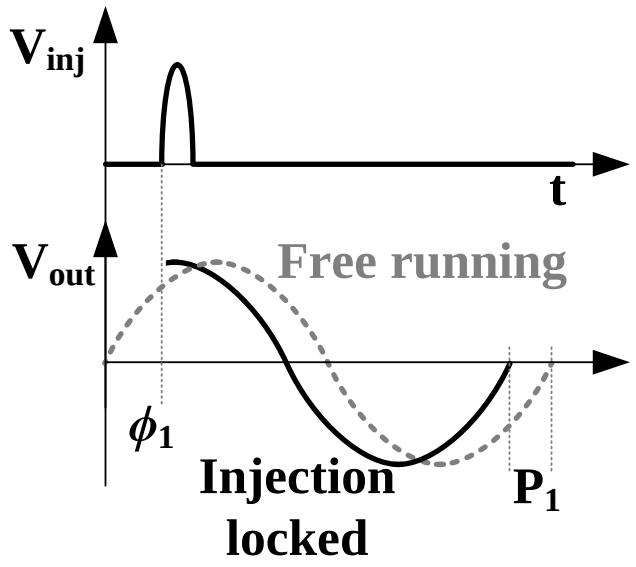

Figure 2.13. Single pulse injection at $\phi 1$.

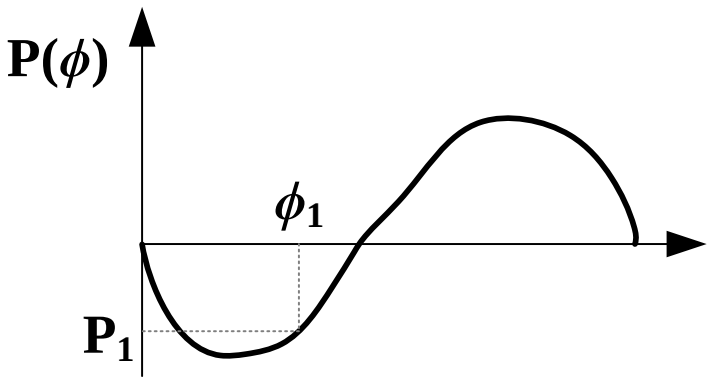

Figure 2.14. PDR curve example.

2.5 LC Quadrature Oscillator

2.5.1 Overview

Since the proposed quadrature resonant clocking scheme is very similar to the LC quadrature oscillator, understanding the LC quadrature oscillator is very helpful in following the proposed quadrature resonant clocking scheme. Therefore, this section describes the basic principles, operation modes and characteristics of the LC quadrature oscillator.

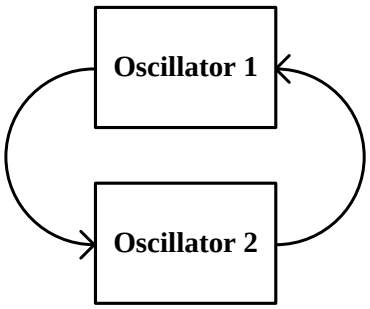

Figure 2.15 Two oscillators coupled each other.

When two identical oscillators are properly coupled as depicted in the Figure 2.15, the two oscillators operate with a phase shift of 90°. The LC quadrature oscillator is designed on this principle. How to implement this coupling structure is explained in the next section.

2.5.2 Basic Principles of the LC Quadrature Oscillator

The coupling state of Figure 2.15 is shown as a small-signal model, as shown in Figure 2.16. Circuit analysis based on this model is as follows.

$$G_{m1}V_1\frac{-RZ_T}{Z_T-R}=V_2 \tag{2.4}$$

$$G_{m2}V_2\frac{-RZ_T}{Z_T-R}=V_1 \tag{2.5}$$

Assuming $V_1, V_2 \neq 0$, and dividing (2.4) by (2.5), the equation of V_1, V_2 is derived as follows.

$$G_{m1}V_1^2-G_{m2}V_2^2=0 \tag{2.6}$$

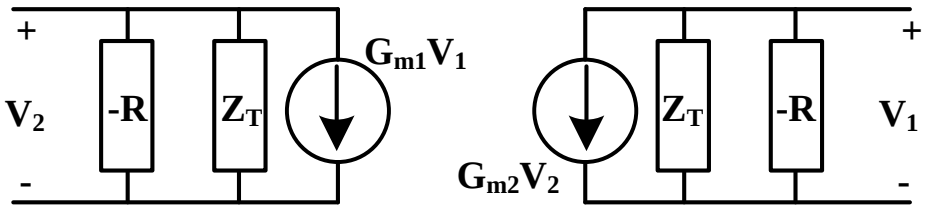

Figure 2.16. Small-signal model of quadrature oscillator.

This result predicts two important cases. If $G_{m1} = G_{m2}$, then

$$V_1^2 - V_2^2 = 0 \tag{2.7}$$

$$V_1 = \pm V_2. \tag{2.8}$$

In this case, the two oscillators operate with a phase difference of zero or 180°. However, if $G_{m1} = -G_{m2}$, then

$$V_1^2 + V_2^2 = 0 \tag{2.9}$$

$$V_1 = \pm jV_2. \tag{2.10}$$

In this case, the phase difference is 90° or -90°. These two cases are called "in-phase coupling" and "anti-phase coupling". The Figure 2.17 and Figure 2.18 are the illustration of the cases respectively. Since the output of the in-phase coupling oscillator is not a quadrature clock, this section presents an analysis of the anti-phase coupling oscillator.

A linear model of an anti-phase coupling LC quadrature oscillator shown in the Figure 2.18 consists of two coupled parallel RLC circuits as represented in Figure 2.19. In parallel with each tank there are negative resistances $-1/g_m$, which cancel the losses. Two differential transconductances g_{mc} provide the coupling, and are responsible for the quadrature outputs.

In the linear model of the LC quadrature oscillator which is shown in Figure 2.19 the loop gain is derived as follows.

$$G_{loop}(s) = -g_{mc}^2 \left(\frac{sL}{1 + sL\left(\frac{1}{R_p} - g_m\right) + s^2 LC} \right)^2 \tag{2.11}$$

Using the Barkhausen criterion for the loop gain with $1/g_m = R_p$, the equation

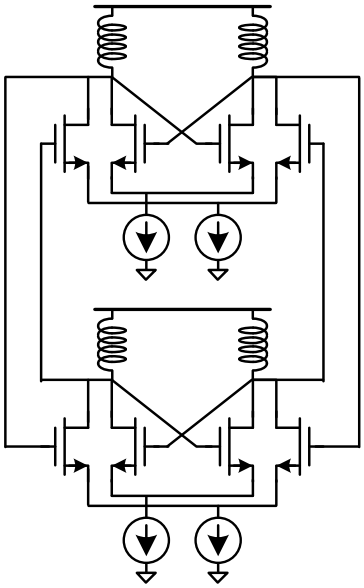

Figure 2.17. In-phase coupling

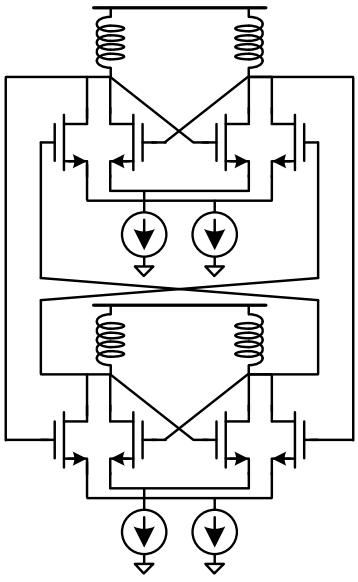

Figure 2.18. Anti-phase coupling.

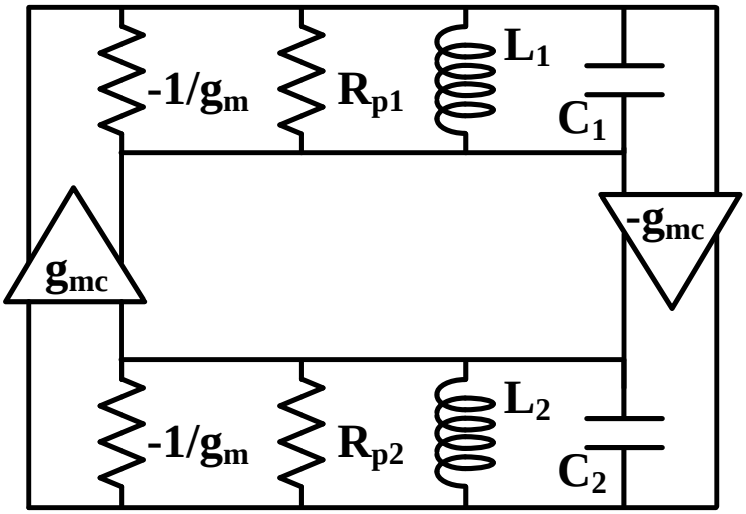

Figure 2.19. Linear model of the anti-phase coupling LC quadrature oscillator.

(2.11) is solved as follows.

$$1 = -g_{mc}^2 \left(\frac{sL}{1+s^2LC}\right)^2 \tag{2.12}$$

$$\pm j = \frac{g_{mc} sL}{1+s^2LC}. \tag{2.13}$$

By making $s = j\omega$, the equation (2.13) is solved in order to ω as follows and have two solutions.

$$\pm 1 = \frac{g_{mc}\omega L}{1-\omega^2 LC} \tag{2.14}$$

$$\omega^2 \pm \frac{g_{mc}}{2C} 2\omega L - \omega_0^2 = 0. \tag{2.15}$$

Where the $\omega_0 = 1/\sqrt{LC}$. The oscillation frequency ω_{osc1} and ω_{osc2} are derived as follows.

$$\omega_{osc1} = +\frac{g_{mc}}{2C} + \omega_0 \sqrt{1 + \frac{g_{mc}^2 L}{4C}} \tag{2.16}$$

$$\omega_{osc2} = -\frac{g_{mc}}{2C} + \omega_0 \sqrt{1 + \frac{g_{mc}^2 L}{4C}}. \tag{2.17}$$

Assuming that,

$$\frac{g_{mc}^2 L}{4C} \ll 1 \tag{2.18}$$

the equations (2.19) and (2.20) are derived.

$$\omega_{osc1} \approx \omega_0 + \frac{g_{mc}}{2C} \tag{2.19}$$

$$\omega_{osc2} \approx \omega_0 - \frac{g_{mc}}{2C}. \tag{2.20}$$

From equations (2.19) and (2.20) it is observed that coupling two oscillators will produce some shift in the oscillation frequency. And the phenomenon that the LC quadrature oscillator has two solutions is called the bi-modal operation of the LC quadrature oscillator [36] -[38] and is discussed in more detail in the later section.

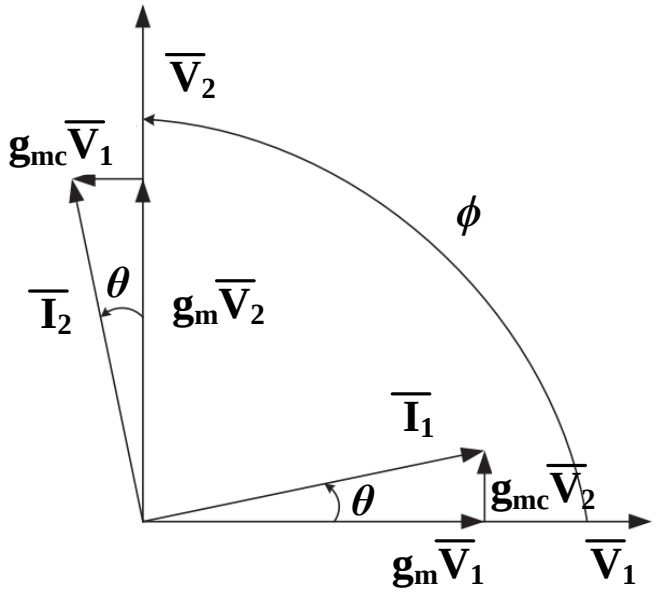

Figure 2.20. Phasor diagram of the LC quadrature oscillator.

In the Figure 2.20, the currents and the voltages in the LC oscillator are represented by a phasor diagram, where ϕ represents the phase difference between the $\overline{V1}$ and $\overline{V2}$, and θ is the phase difference between $\overline{I1}$ and $\overline{V1}$, which is

$$\theta = \arctan\left(\frac{g_{mc}}{g_m}\right) = \arctan(coupling\ factor). \qquad (2.21)$$

The LC quadrature oscillator circuit without mismatches is symmetric and this implies that there is perfect quadrature, $\phi = \pi/2$, otherwise the voltages and currents would be different in the two oscillators, which is incompatible with the circuit symmetry

The equations (2.19), (2.20), and (2.21) indicates that, as the bias current of the

differential pair for quadrature coupling increases (and so does the g_{mc} and coupling factor), the oscillation frequency must deviate from ω_0 by a greater amount so that each LC tank provides the required phase shift. Since the LC tanks operate at a frequency that is increasingly farther from the resonance frequency, the Q factor falls, raising the phase noise. From this point of view, it is desirable to minimize the coupling factor.

In the case when the mismatches exist between the two LC insufficient coupling fails to force them to equal frequencies. A coupling factor of approximately 0.25 typically provides a reasonable compromise between Q degradation and oscillation reliability.

2.5.3 Bi-Modal Operation of the LC Quadrature Oscillator

Bi-modal operation of the LC quadrature oscillator, as discussed in the previous section, is the phenomenon that the LC quadrature oscillator has two frequency solutions, which are (2.19) and (2.20). Both solutions have the quadrature output clocks, I, Ib, Q, Qb, with 90° phase difference. However, in one solution, I clock leads Q clock but in the other, I clock lags Q clock. Since the relationship between I clock and Q clock is critical to most multi-rate applications using quadrature clock, predictability and stability of two solutions is important.

Thanks to [36] , analysis of the LC quadrature oscillator based on the injection locking is complete and this section briefly introduces the analysis process and results about bi-modal operation.

Figure 2.21 shows the LC quadrature oscillator under injection. The anti-phase coupling of two LC oscillators is expressed as an injection based equivalent circuit. Applying the generalized Adler's equations to each oscillator leads to the following equations.

$$\frac{d\theta_1}{dt} = \omega_0 - \frac{\omega_0}{2Q}\frac{I_C \sin(\theta_2 - \theta_1 - \phi)}{I - I_C \cos(\theta_2 - \theta_1 - \phi)} \tag{2.22}$$

$$\frac{d\theta_2}{dt} = \omega_0 + \frac{\omega_0}{2Q}\frac{I_C \sin(\theta_1 - \theta_2 - \phi)}{I + I_C \cos(\theta_1 - \theta_2 - \phi)} \tag{2.23}$$

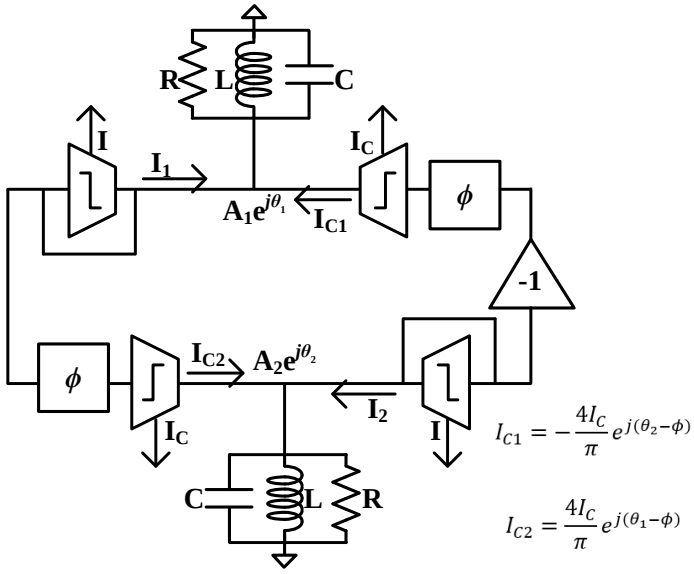

Figure 2.21. LC quadrature oscillator.

$$RC\frac{dA_1}{dt} + A_1 = \frac{4R}{\pi}(I - I_C\cos(\theta_2 - \theta_1 - \phi)) \tag{2.24}$$

$$RC\frac{dA_2}{dt} + A_2 = \frac{4R}{\pi}(I + I_C\cos(\theta_1 - \theta_2 - \phi)) \tag{2.25}$$

Considering the stable oscillator condition, $dA_1/dt = dA_2/dt = 0$,writing the two output phases as $\theta_1 = \omega_{osc}t$ and $\theta_2 = \omega_{osc}t + \psi = \omega_{osc}t \pm \pi/2$, defining the coupling ratio $m = I_c/I$, the amplitude and the frequency of the two modes are derived as follows.

$$\omega_{osc,m1} = \omega_0 - \frac{\omega_0}{2Q}\frac{m\cos\phi}{1 - m\sin\phi} \tag{2.26}$$

$$A_{m1} = \frac{4IR}{\pi}(1 - m\sin\phi) \tag{2.27}$$

$$\omega_{osc,m2} = \omega_0 + \frac{\omega_0}{2Q}\frac{m\cos\phi}{1 + m\sin\phi} \tag{2.28}$$

$$A_{m2} = \frac{4IR}{\pi}(1 + m\sin\phi) \tag{2.29}$$

The frequencies of equation (2.26) and (2.28) are identical to the equations (2.19) and (2.20). Using perturbation analysis, assuming that $\theta_1 = \omega_{osc}t + \hat{\theta}_1$ and $\theta_2 = \omega_{osc}t + \psi = \omega_{osc}t \pm \pi/2 + \hat{\theta}_2$, where $|\hat{\theta}_1|, |\hat{\theta}_2| \ll 1$, following equations are derived for the first mode.

$$\frac{d\hat{\theta}_1}{dt} = \frac{\omega_0}{2Q}\frac{m(m - \sin\phi)}{(1 - m\sin\phi)^2}(\hat{\theta}_2 - \hat{\theta}_1) \tag{2.30}$$

$$\frac{d\hat{\theta}_2}{dt} = \frac{\omega_0}{2Q}\frac{m(m - \sin\phi)}{(1 - m\sin\phi)^2}(\hat{\theta}_1 - \hat{\theta}_2) \tag{2.31}$$

$$\frac{d(\hat{\theta}_1 - \hat{\theta}_2)}{dt} = -\frac{\omega_0}{Q}\frac{m(m - \sin\phi)}{(1 - m\sin\phi)^2}(\hat{\theta}_1 - \hat{\theta}_2) \tag{2.32}$$

And for the second case, in the same way, following equations are derived.

$$\frac{d(\hat{\theta}_1 - \hat{\theta}_2)}{dt} = -\frac{\omega_0}{Q}\frac{m(m + \sin\phi)}{(1 + m\sin\phi)^2}(\hat{\theta}_1 - \hat{\theta}_2) \tag{2.33}$$

The equations (2.32) and (2.33) are the form of $dx/dt = kx$. When the coefficient

k is negative, x will decay. That means, in the equation (2.32), when $m - \sin\phi > 0$, the perturbation will decay and the mode will be restored. Therefore, the first mode is conditionally stable when $\sin\phi < I_C/I$. In the same way, the second mode is unconditionally, always stable.

Considering the coupling ratio is usually a small number in the range of 0.1 to 0.4, it is not that complicated that inserting the small phase shift in the quadrature coupling path. However, the recommended phase shift is 90° because the first mode is always unstable with the phase shift of 90°. In addition, according to the [36] , the quadrature accuracy and phase noise are also the best when the 90° phase shift is inserted in the quadrature coupling path.

2.5.4 Phase Noise of the LC Quadrature Oscillator

In an LC oscillator the noise is originated in three different blocks: the lossy LC tank, the transistors of the differential pair, and the tail current source. Considering the equivalent circuit of the LC oscillator in the Figure 2.22 as a very beginning, assuming that the only noise source is the thermal noise [39] , the phase-noise contribution of the tank can be calculated, which is represented either as a current source across the tank with a spectral density or as a voltage noise source in series with the tank with spectral density.

$$S(i_n) = \frac{4kT}{R_p} \tag{2.34}$$

$$S(v_n) = S(i_n)|Z_T|^2 \tag{2.35}$$

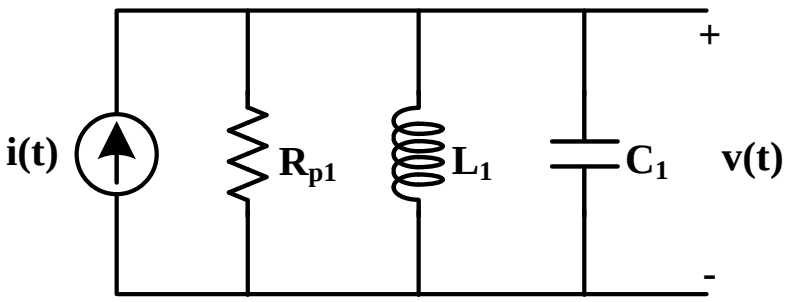

Figure 2.22. Equivalent circuit of the LC oscillator.

Using the model of Figure 2.22, for small offset frequencies with respect to the fundamental frequency ($\omega_m \ll \omega_0/2Q$) the impedance of the LC tank, Z_T, is approximated by [39] and [40] as follows.

$$|Z_T(\omega_0 + \omega_m)|^2 \approx R_p^2 \frac{1}{4Q^2}\left(\frac{\omega_0}{\omega_m}\right)^2 \tag{2.36}$$

The definition of the Q factor in [41] is as follows where $A = |Z(j\omega)|$, $\theta = \arg|Z(j\omega)|$ and the resonant frequency $\omega_0 = 1/\sqrt{LC}$.

$$Q = \frac{\omega_0}{2}\sqrt{\left(\frac{dA}{d\omega}\right)^2 + \left(\frac{d\theta}{d\omega}\right)^2} \tag{2.37}$$

In a stable LC oscillator $dA/d\omega = 0$ [41] , and for $Q_0 = Q(\omega_0)$

$$\begin{aligned} Q_0 &= \frac{\omega_0}{2}\left|\frac{d\theta}{d\omega}\right|_{\omega=\omega_0} \\ &= R_p\sqrt{\frac{C}{L}} = \frac{R_p}{\omega_0 L} \end{aligned} \tag{2.38}$$

Considering that the losses in the capacitors are much lower than those in the inductors, the resonator quality factor is determined mainly by the inductor, and the parallel resistance is obtained from the inductor quality factor [40] .

Using equations (2.34), (2.35), and (2.36),

$$\begin{aligned} S(v_n) &= \frac{4kT}{R_p}\left|R_p\frac{\omega_0}{2Q\omega_m}\right|^2 \\ &= 4kTR_p\left(\frac{\omega_0}{2Q\omega_m}\right)^2 \end{aligned} \tag{2.39}$$

From (2.39) it can be concluded that increasing Q factor leads to a reduction in the

noise spectral density, when all the other parameters remain unchanged. The output noise is frequency dependent, due to the filtering action of the tank: the spectral density is inversely proportional to the square of the offset frequency. This behavior is due to the fact that the voltage frequency response of an RLC tank rolls off as $1/f$ to each side of the center frequency, and power is proportional to the square of voltage [42] .

An important aspect is that thermal noise affects both amplitude and phase, and equation (2.39) includes their combined effect. In the absence of amplitude limiting, the amplitude-noise and phase-noise powers are equal. However, considering an amplitude limiting mechanism of the oscillator, the mechanism removes most of the amplitude-noise. Therefore, the total noise power in the oscillator will be approximately half the noise given by (2.39) [39] , [40] , and [43] .

The phase noise spectral density is derived as follows by dividing by the carrier power, $P_{carrier} = V_{tank}^2/R_p$.

$$\mathcal{L}(\Delta\omega) = 10\log\left[\frac{2kT}{P_{carrier}}\left(\frac{\omega_0}{2Q\omega_m}\right)^2\right] \tag{2.40}$$

It should be noted that (2.40) is only valid for the $1/f^2$ region of the noise spectrum. A complete equation of the phase noise spectral density for all the spectral oscillator regions was presented by [44] .

In the case of the LC quadrature oscillator, a maximum of 3 dB improvement of the oscillator phase-noise can exist in two coupled LC oscillators when compared with a single LC oscillator.

$$\mathcal{L}(\Delta\omega) = 10\log\left[\frac{1}{2}\frac{2kT}{P_{carrier}}\left(\frac{\omega_0}{2Q\omega_m}\right)^2\right] \tag{2.41}$$

This maximum 3 dB improvement, due to coupling, is obtained when the oscillators are isolated and oscillate at their common resonance frequency. When the oscillators are coupled, the oscillation frequency changes according to the equations (2.19) or (2.20). In this case, Q factor which is different from the equation (2.38) is derived as follows.

The impedance phase of an RLC circuit is

$$\theta(\omega) = \frac{\pi}{2} - \arctan\frac{\omega L/R_p}{1-\omega^2 LC} \tag{2.42}$$

and

$$\frac{d\theta(\omega)}{d\omega} = \frac{LR_p(CL\omega^2+1)}{C^2L^2R_p^2\omega^4 - 2CLR_p^2\omega^2 + L^2\omega^2 + R_p} \tag{2.43}$$

Substituting (2.43) in (2.37) and using the stable LC oscillator condition, $dA/d\omega = 0$ [41] ,

$$Q = \frac{\omega_0}{2}\left|\frac{LR_p(CL\omega^2+1)}{C^2L^2R_p^2\omega^4 - 2CLR_p^2\omega^2 + L^2\omega^2 + R_p}\right| \tag{2.44}$$

When the oscillators are coupled, the theoretical equation (2.44) for Q factor should be used.

At the resonant frequency, the equation (2.43) simplifies to

$$\frac{d\theta(\omega)}{d\omega} = -2CR_p \tag{2.45}$$

And Q factor is given by (2.38) as expected.

The most important conclusion from this study is that the performance of the single LC oscillators is different from the performance of the LC quadrature oscillators. Coupled LC oscillators can have a theoretical phase noise improvement of 3 dB, but, any deviation from the resonance frequency due to mismatches and to coupling will reduce Q and increase the phase noise.

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Chapter 3

Design of the Proposed Quadrature Resonant Clock

3.1 Overview

In this chapter, a quadrature resonant clock with frequency tuning capacitor and amplitude control feedback loop is proposed. The proposed quadrature resonant clocking scheme achieves high power reduction ratio under all operating conditions by tuning out the frequency mismatch using the frequency tuning capacitors.

3.2 Overall Architecture

Figure 3.1 shows the overall block diagram of the proposed quadrature resonant clocking scheme incorporating four 4.3-mm load wires, two inductors, two frequency tuning capacitors, two negative gm cells, quadrature coupling cells, an input injection cell, pulse generation cell, a peak detector and a PLL for frequency tuning.

The parasitic capacitor and the inductor of the load wire act as the LC resonator, and the LC quadrature oscillator is composed of the resonator, the negative gm cell, and the quadrature coupling cell. The bang-bang phase frequency detector (BBPFD) and the peak detector generate up and down information for the phase and amplitude of the output clock, respectively. The digital loop filter (DLF) uses the information received from the BBPFD and peak detector to generate the signal that controls the tuning capacitor and the bias current of the negative gm cell. The input clock is injected into the load wire and the quadrature oscillator core through the pulse generation cell and the injection cell. The design, simulation results, and analysis of each part of the proposed quadrature resonant clock are covered in later sections.

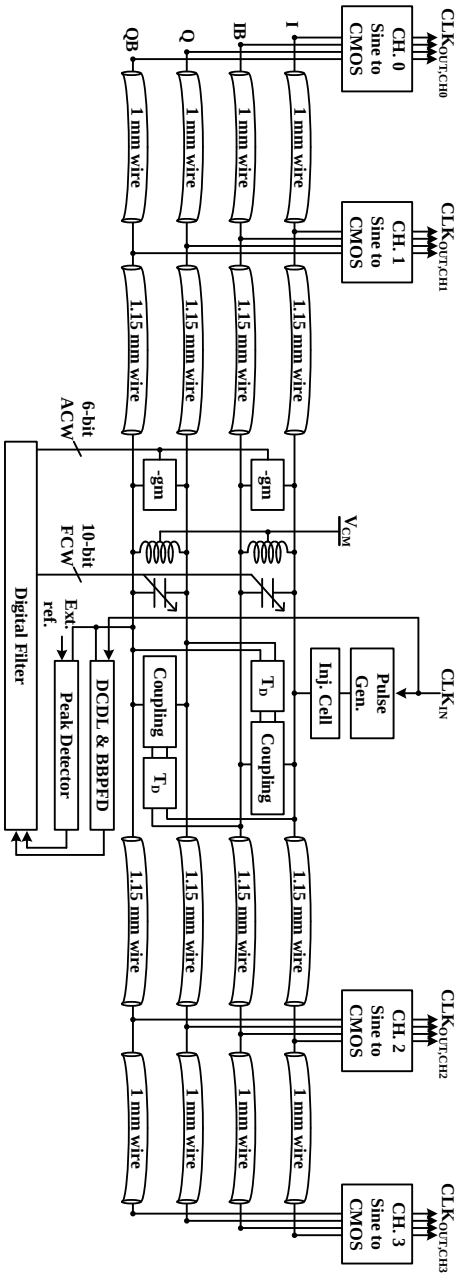

Figure 3.1. Overall architecture of the proposed quadrature resonant clock.

3.3 Load Wire Design and Q Factor Calculation

The shape of the load wire in the resonant clock is very important because it determines the capacitance affecting the resonant frequency of the LC tank. The shape also determines parasitic resistance, which is the most dominant parameter to determine the Q factor. Q factor is an indicator of how much power consumption can be reduced, so optimizing load wire parasitic resistance is one of the most important things in resonant clocking design.

Parameters that determine the shape of the load wire include width, length, thickness, spacing between adjacent wires, and distance from the top and bottom metal layers. These parameters affect the parasitic resistance and capacitance of the wire. In the case of wire width as an example, if the wire is too narrow, the parasitic resistance becomes too large, resulting in poor power reduction. On the contrary, the larger wire width offers smaller resistance and hence better power reduction with a higher Q factor. However, if the capacitor is too large for the operation frequency, the inductor becomes too small to implement with an on-chip spiral inductor. Furthermore, if the capacitor becomes too large, it is difficult to set the tuning capacitor large enough, making it difficult to implement a wide tuning range.

As a method of verifying the performance of the resonant clock in the circuit design process, there is a method of calculating the Q factor of the entire system including the inductor, the parasitic capacitance of the load wire, and the parasitic resistance

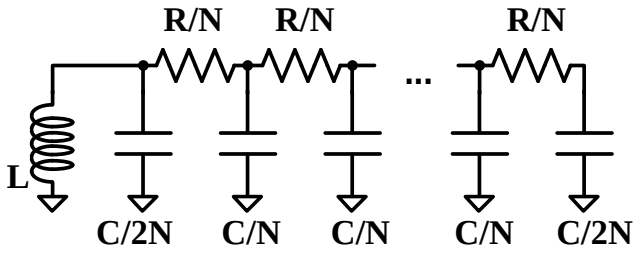

Figure 3.2. N-stage π model of clock distribution wire.

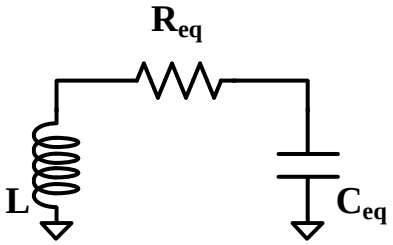

Figure 3.3. Equivalent circuit of the N-stage π model of the clock distribution wire.

of the load wire. In this thesis, the N-stage π model of the lumped wire is used to calculate the Q factor. The Figure 3.2 and Figure 3.3 show the N-stage π model and its equivalent circuit. To simplify the process of calculating the Q factor, an equivalent circuit of the N-stage π model of the lumped wire is used, and the equivalent resistance (R_{eq}) and the equivalent capacitance (C_{eq}) of the equivalent circuit are calculated as follows according to the [45] . In the Figure 3.4, which shows the simplest RC tree, value of R, C and the admittance at the driving point, Y(s), are expressed as follows.

$$Y(s) = \frac{sC}{1+sRC} = \sum_{n=1}^{\infty}(-1)^{n-1}R^{n-1}C^n s^n = \sum_{n=1}^{\infty} y_n s^n. \qquad (3.1)$$

$$C = y_1. \tag{3.2}$$

$$R = -\frac{y_2}{y_1^2}. \tag{3.3}$$

Meanwhile, in the Figure 3.5, the impedance and admittance of the open-ended RC network are defined as follows.

$$Z_{in} = Z_0 \frac{Z_L + Z_0 tanh(\gamma l)}{Z_0 + Z_L tanh(\gamma l)}. \tag{3.4}$$

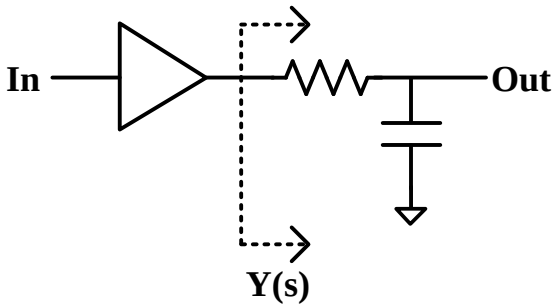

Figure 3.4. Simple RC tree modeling the driving point admittance.

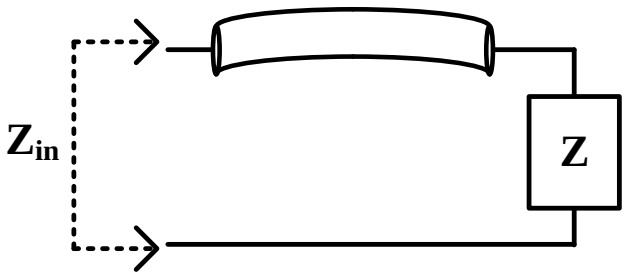

Figure 3.5. Open-ended RC network.

$$Y = \frac{tanh(\gamma l)}{Z_0}. \tag{3.5}$$

$$\gamma l = \sqrt{sRC}. \tag{3.6}$$

$$Z_0 = \sqrt{\frac{R}{sC}}. \tag{3.7}$$

Since the admittance Y(s) in equation (3.1) and (3.2) must match, it can be summarized as follows.

$$\begin{aligned} Y &= \sqrt{\frac{sC}{R}}\left(tanh\left(\sqrt{sRC}\right)\right. \\ &= \sqrt{\frac{sC}{R}}\left(\sqrt{sRC} - \frac{1}{3}sRC\sqrt{sRC} + \cdots\right) \\ &= sC - \frac{1}{3}s^2RC^2 + \frac{2}{15}s^3R^2C^3 + \cdots \\ &= \sum_{n=1}^{\infty} y_n s^n. \end{aligned} \tag{3.7}$$

Therefore, if the equivalent circuit of the open-ended RC network circuit in Figure 3.5 is constructed as the simple RC tree circuit shown in Figure 3.4, the equivalent resistance (R_{eq}) and the equivalent capacitance (C_{eq}) are determined as follows by using the equations (3.2), (3.3) and (3.7).

$$C_{eq} = C. \tag{3.8}$$

$$R_{eq} = \frac{R}{3}. \tag{3.9}$$

Meanwhile, the block diagram of the LC resonator composed only of the load wire

and the inductor of proposed resonant clocking scheme of Figure 3.1 is shown in the Figure 3.6. Using the R_{eq} and the C_{eq} obtained through the equation (3.8) and (3.9), the equivalent half circuit of the LC resonator in the Figure 3.6 is constructed as shown in the Figure 3.7. The R_W and C are equivalent resistance and capacitance of the 2.15 mm load wire which are derived by using the equation (3.8) and (3.9). Deriving the Q factor from the equivalent half circuit of the LC resonator in Figure 3.7 is as follows.

$$Q = \frac{1}{(R_L + 0.5R_w)}\sqrt{\frac{L}{2C}}. \tag{3.10}$$

As a result of simulation using the obtained equivalent circuits and equations, it can be confirmed that when using an inductor of 1 nH at an operating frequency of 7 GHz, the capacitance of one 4.3 mm wire is approximately 600 fF. In order to design a wire having parasitic capacitance obtained in this way, the structure of the wire must first be determined and the parameters including the width of the wire, spacing between adjacent wires, and distance from the top and bottom metal layers should be determined by referring to the post layout simulation results.

Two pairs of the ground shielded differential wires (GND-CLK-CLKb-GND) were used for the design of the quadrature load wire used in the proposed quadrature resonant clocking scheme. Also, the ground plane was set with metal 2 under the load wire. Based on this structure, parasitic capacitance and parasitic resistance components can be extracted according to the width and spacing of wires. The Table 3.1 is an example of parasitic extraction result according to the metal layer of the load wire when both width and spacing are 1um. Referring to Equation (3.10), the smaller the

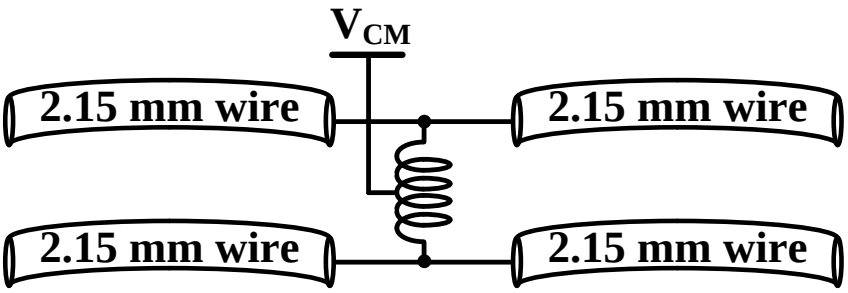

Figure 3.6. Block diagram of LC resonator.

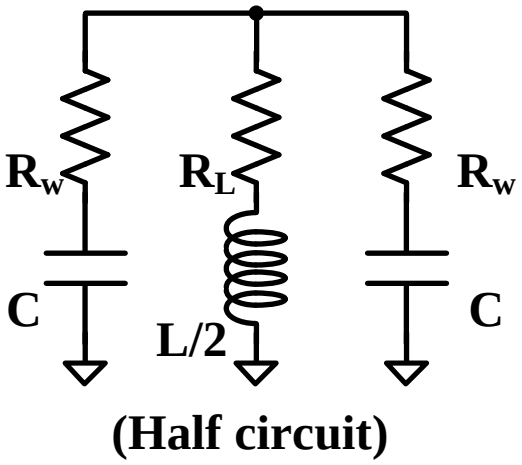

Figure 3.7. Equivalent half circuit of the LC resonator.

series parasitic resistance, the larger the Q factor and thus the more power consumption can be reduced. Therefore, it is suitable to design the load wire with metal 8. In addition, the width and spacing of wires were set to satisfy the aforementioned 600 fF capacitance condition. The final version of load wire is designed to have a capacitance

and resistance of about 130 fF/mm and 15 Ω/mm with the total length of 4.3 mm per each clock wire. The total Q factor of the resonator calculated using equation (3.10) is 4.56. The layout of the quadrature clock distribution wire is shown in the Figure 3.8.

Table 3.1. Example of parasitic extraction result according to the metal layer of the load wire.

Metal Layer	**Width (um)**	**Length (um)**	**Spacing (um)**	**R (ohm)**	**C (fF)**
M3	1	100	1	11.3	24.5
M4	1	100	1	11.3	11.5
M5	1	100	1	11.3	9.4
M6	1	100	1	11.3	8.9
M7	1	100	1	11.3	8.6
M8	1	100	1	2.2	17.6

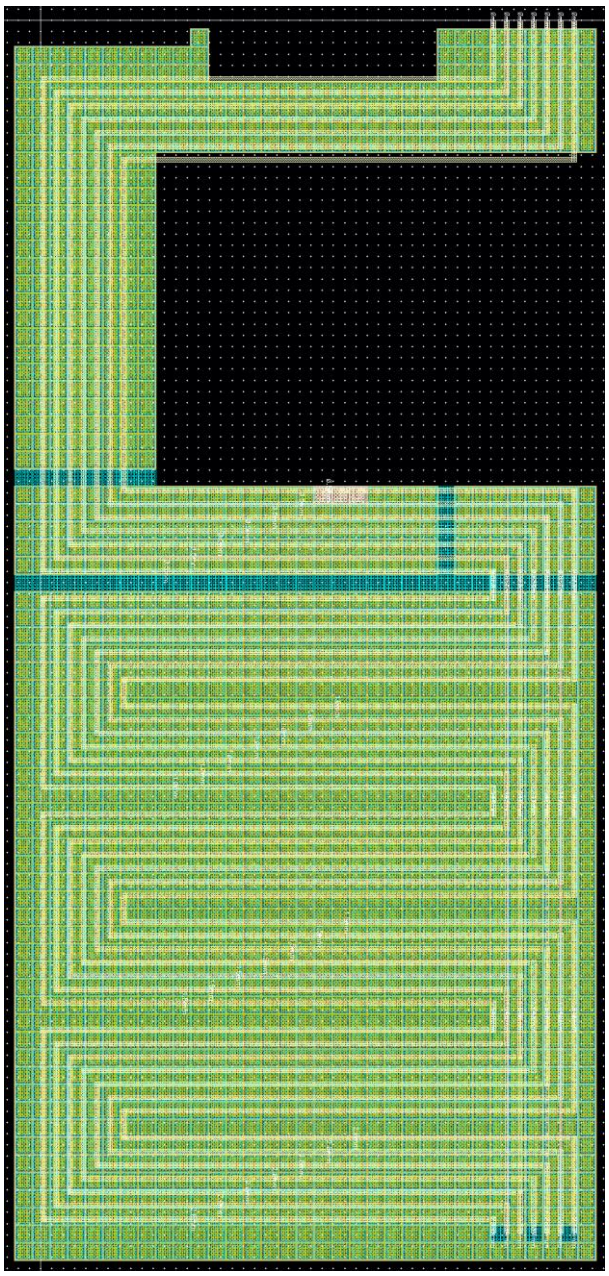

Figure 3.8. Layout of the quadrature clock distribution wire.

3.4 Design of the LC Quadrature Oscillator Core

As discussed earlier, considering the equivalent half circuit in Figure 3.7, the resonant clocking scheme has many structural similarities to LC oscillators. There are only differences in the way capacitors are implemented (cap bank for the LC oscillator and load wire parasitic capacitor for the resonant clocking scheme), and they share a common principle of operation using the resonance between the inductor and the capacitor. Therefore, the design method of LC oscillator can be applied to design the resonant clocking scheme. Therefore, the proposed quadrature resonant clocking scheme has the negative gm cell and the quadrature coupling cell in the same way as the LC quadrature oscillator. The circuit diagram of the LC quadrature oscillator core is shown in Figure 3.9.

The inductor constituting the LC resonator is 0.95 nH, and the Q factor of the inductor alone is about 15. A 3-turn spiral inductor is used to minimize the area, and the layout of the spiral inductor is shown in Figure 3.10. The spiral inductor occupies an area of 146*142 um^2

The negative gm cell is designed based on the cross-coupled NMOS transistors which is one of the most basic design of the LC quadrature oscillator. The quadrature coupling cell is designed based on the basic differential pair with antiphase coupling. The quadrature coupling ratio determined by the ratio of the bias current of the negative gm cell and the bias current of the coupling cell is designed to be adjustable in

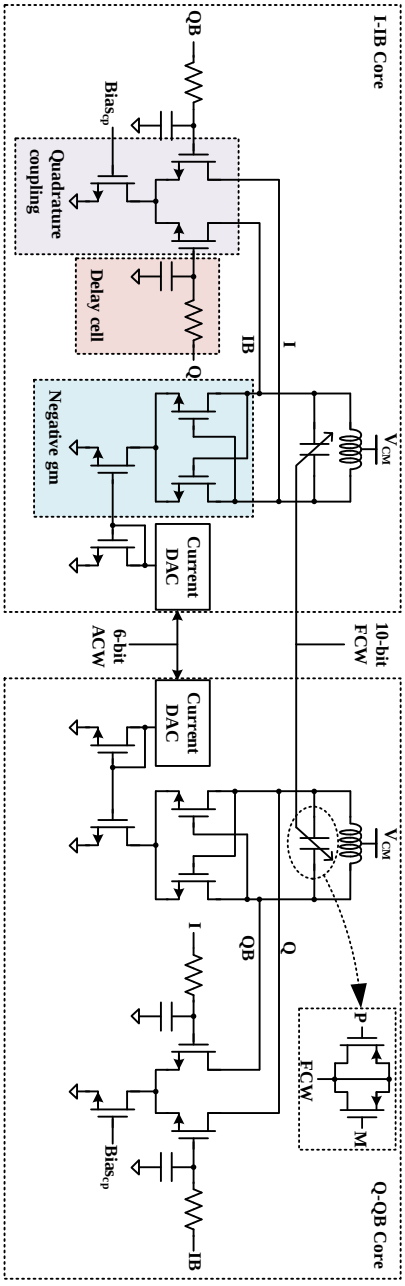

Figure 3.9. Circuit diagram of the LC quadrature oscillator core.

the range of 0.2 to 0.5.

In front of the quadrature coupling NMOS differential pair, the first-order RC delay unit (T_D) is inserted to avoid the bi-modal oscillation which is conditionally stable [36] -[38] . In addition, the delay unit improves the quality of the output clock according to [36] when the delay is close enough to 90°. When the inserted phase shift is 90°, the LC quadrature oscillator has only one oscillation mode unconditionally. Therefore, the most appropriate delay is 90°. However, producing exactly 90° is difficult considering mismatch and PVT variations. Also, 90° can only be created using an active delay line or a high-order filter, but these methods have some problems that the designing the active delay line or high-order filter is complicated and they consume a lot of power. Therefore, in the proposed quadrature resonant clocking scheme, the first-order filter is used for less design complexity and less power consumption.

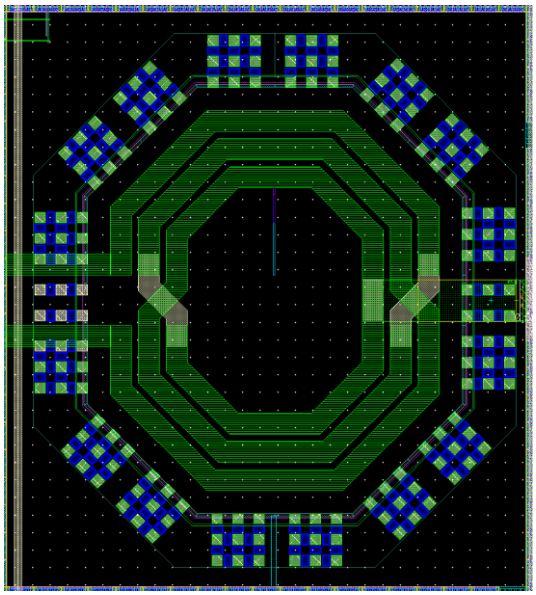

Figure 3.10. Layout of the spiral inductor.

The LC quadrature oscillator has only one mode when the quadrature coupling ratio is less than 2/3 when a 60° phase shift is inserted into the first-order RC filter.

The LC quadrature oscillator core includes a tuning capacitor to tune the resonant frequency to reduce the difference between the resonant frequency and the operation frequency, and the current digital-to-analog converter (DAC) to adjust the bias current of the negative gm cell that controls the amplitude. The tuning capacitor is controlled by the 10-bit binary digital code (frequency control word, FCW) and the bias current of the negative gm cell is controlled by the 6-bit binary digital code (amplitude control word, ACW). The detailed control method of the FCW and the ACW will be covered in later sections.

Figure 3.11 shows the result of the post layout simulation that the free running output of the oscillator appears well with only the LC quadrature oscillator circuit configured as described in this section. The waveform in Figure 3.11 confirms that there is no problem with free running oscillation with the initial condition.

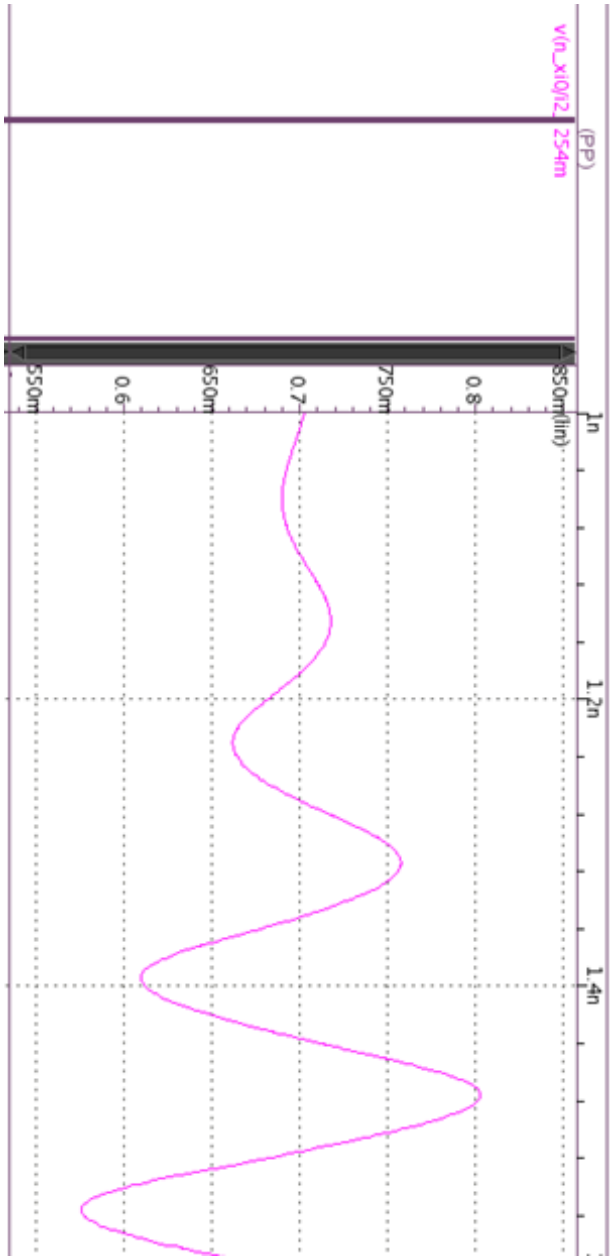

Figure 3.11. Post layout simulation result of the LC quadrature oscillator.

3.5 Feedback Loops

3.5.1 Frequency Control Loop

As shown in the previous chapters, the resonant frequency optimization using the tuning capacitor is essential to solve the problems of the existing resonant clocking scheme caused by the difference between the resonant frequency and the operation frequency. If the difference between the resonant frequency and the operation frequency is not eliminated, the power reduction is not optimized because the impedance of the LC tank cannot be optimized and the LC tank cannot function as a resonator. In addition, it is very important to optimize the resonant frequency using a tuning capacitor in order to apply a resonant clocking scheme to an application having a wide frequency range.

As shown in the Figure 3.12, in the proposed quadrature resonant clocking scheme, frequency tuning is performed using a BBPFD and a DLF_{FCW}, which are the same as in PLL. The BBPFD generates up and down information by comparing which of the reference clock and oscillator output clock comes first. The DLF_{FCW} uses the information received from the BBPFD to generate the signal that controls the tuning capacitor (FCW). DLF_{FCW} also includes a delta-sigma modulator.

The BBPFD is composed of a phase frequency detector (PFD), an arbiter and a latch as shown in the Figure 3.13. The PFD generates up (UP) and down (DN) pulse, then, the arbiter determines which one comes earlier. The latch holds the output states until next state come.

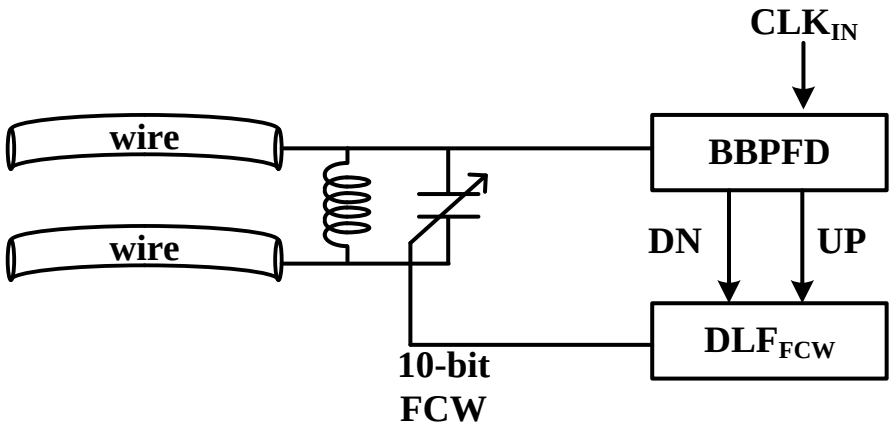

Figure 3.12. Frequency control feedback loop.

The DLF_{FCW}, which is shown in the Figure 3.14, filters the input from the BBPFD and generates the 10-bit frequency control word (FCW). The DLF_{FCW} is composed of the proportional path and the integral path. The proportional path just multiplies the gain of β to the input (UP, DN) and corrects the phase error. On the contrary, the integral path holds the frequency information by accumulating the input information with the gain of α.

When the frequency control loop completes the operation and the output frequency becomes the lock state, the DLF_{FCW} ignores the UP and DN so that the FCW does not change during the input injection process. If the FCW is not fixed, the phase of the output clock is changed by the injection clock. Then, DLF_{FCW} tries to compensate for this phase change. However, since the output frequency is fixed by the effect of input injection, FCW changes in the wrong direction until it goes out of the injection rock range. Therefore, FCW must be fixed when the operation of the feedback loop is

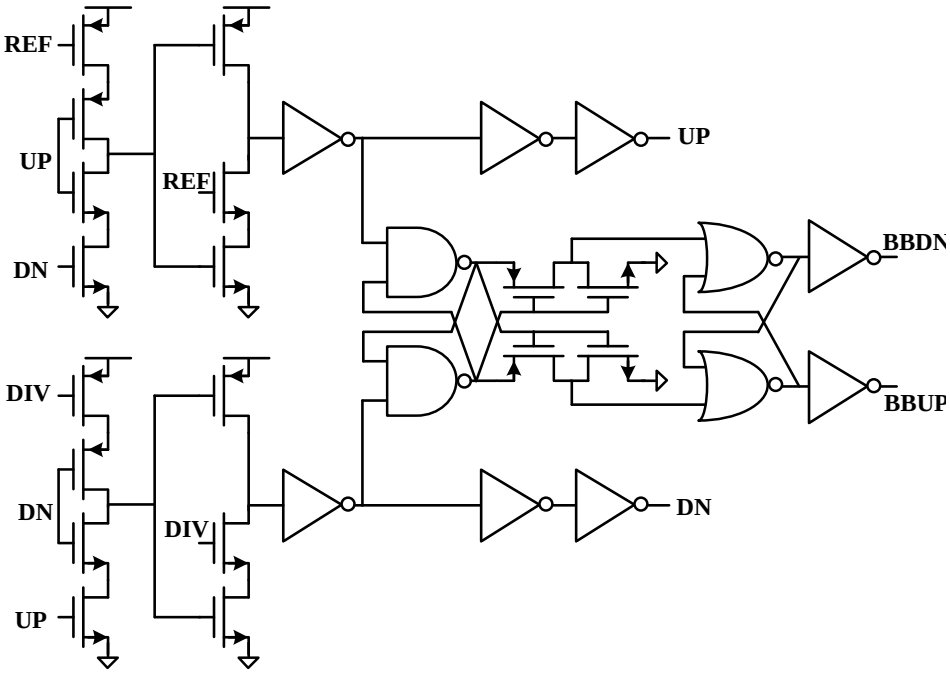

Figure 3.13. BBPFD.

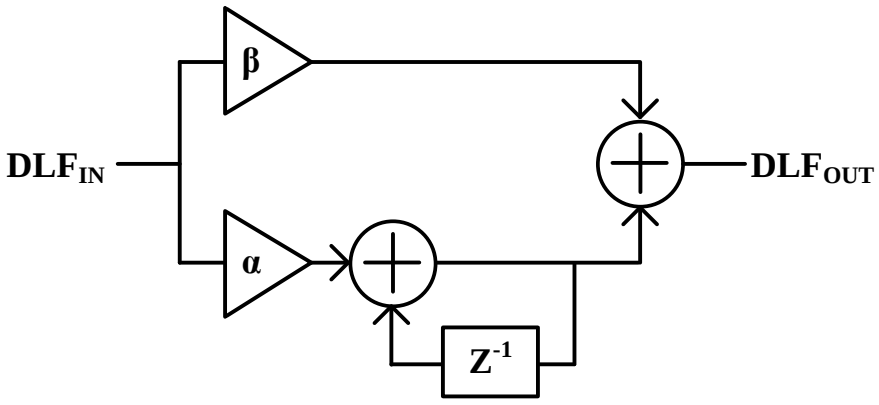

Figure 3.14. DLF_{FCW}.

completed and injection is started.

The transient simulation results showing the frequency control feedback loop locking behavior are shown in Figure 3.15. The waveform of output clock (I, Ib), the frequency of the output clock, 10-bit FCW and BBPFD output signals (UP, DN) are shown. The simulation is done using AMS simulator. Due to the limitation of the simulation speed, the DLF_{FCW} gain is largely set, so it is not fully locked, but it is sufficient to verify the functionality of the frequency control feedback loop.

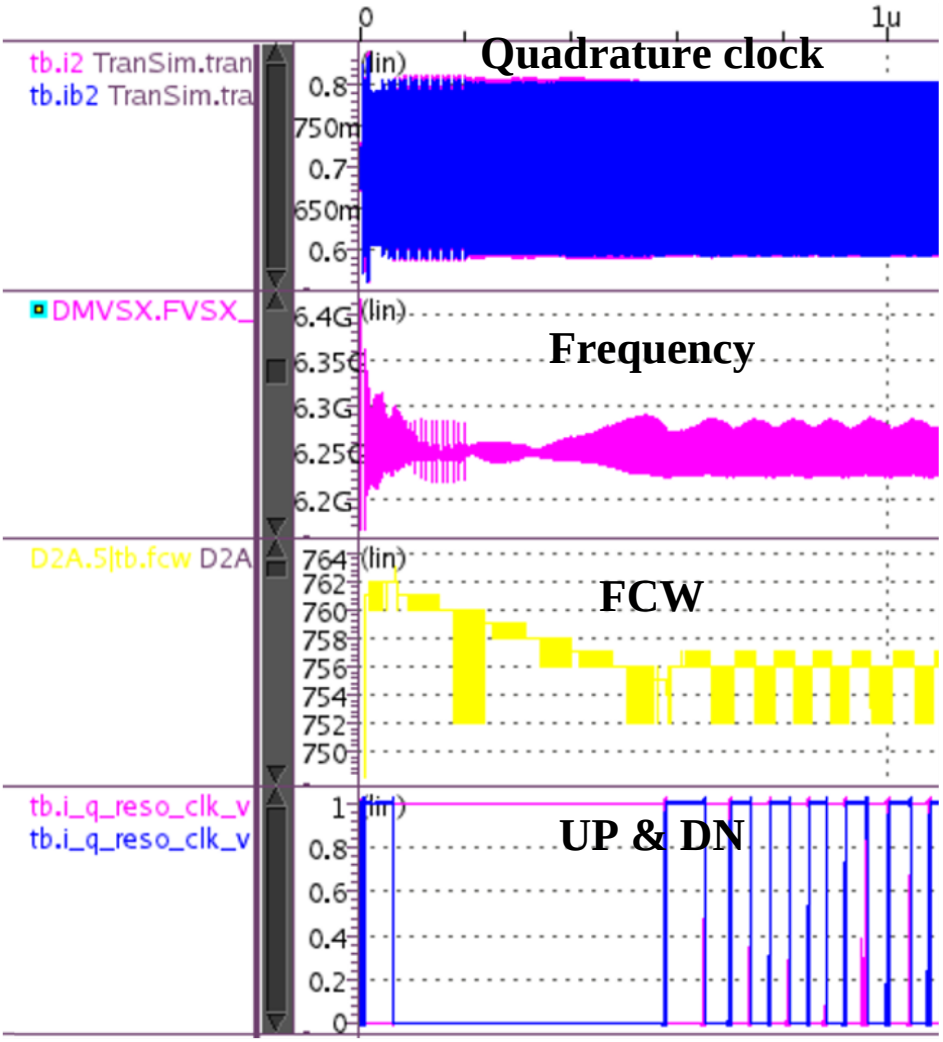

Figure 3.15. transient simulation results showing the frequency control feedback loop locking behavior

3.5.2 Amplitude Control Loop

The bias current of the negative gm cell is one of the most important design parameters in the proposed quadrature resonant clock system because it determines total power consumption and the amplitude of the output clock. Therefore, a feedback loop is required to maintain a constant amplitude even under PVT variations and transient conditions that may vary during frequency tuning, while minimizing power consumption. For example, since the capacitance of the LC resonator also affects the amplitude of the output clock, the amplitude of the output clock varies depending on the change of the FCW. Therefore, in the proposed quadrature resonant clocking scheme, there is a feedback loop that controls the amplitude.

As shown in the Figure 3.16, the amplitude control feedback loop consists of a

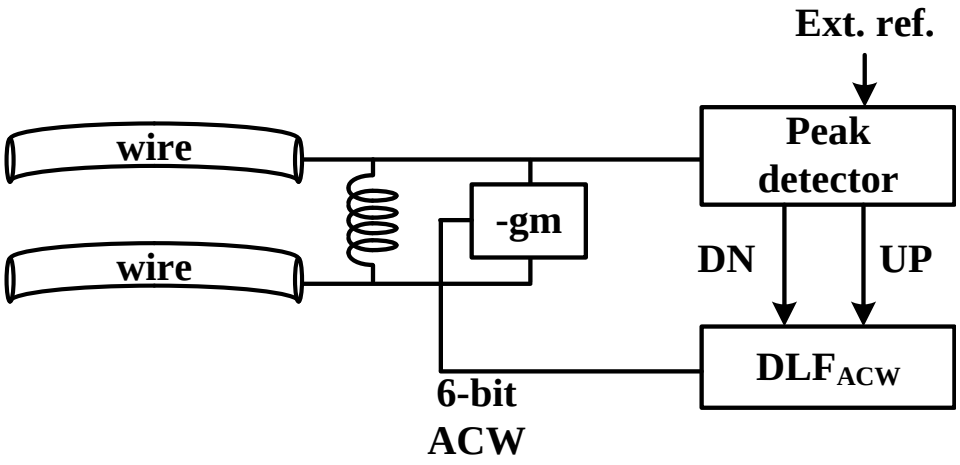

Figure 3.16. Amplitude control feedback loop.

peak detector and a DLF_{ACW}. The peak detector generates up and down information by comparing which of the DC reference value and the peak value of the output clock is larger. The DLF_{ACW} uses the information received from the peak detector to generate the signal that controls the bias current of the negative gm cell (ACW). DLF_{ACW} also includes a delta-sigma modulator.

The DLF_{ACW} uses the peak detector output to generate a 6-bit binary code (ACW) to control the bias current of the negative gm cell. The DLF_{ACW} is almost similar to the DLF_{FCW}, but one difference is that DLF_{ACW} is a first-order digital filter with no proportional path. The amplitude control feedback loop uses a first-order filter because the loop is free from stability issues. The block diagram of DLF_{ACW} is shown in the Figure 3.17.

The circuit shown in the Figure 3.18 is schematic of the peak detector to find the peak value of the sine wave clock and compare it with the DC reference value. The first stage of the peak detector is a source-follower based integrator which hold the

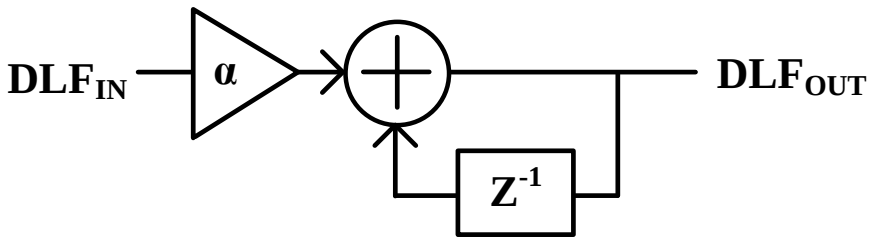

Figure 3.17. DLF_{ACW}.

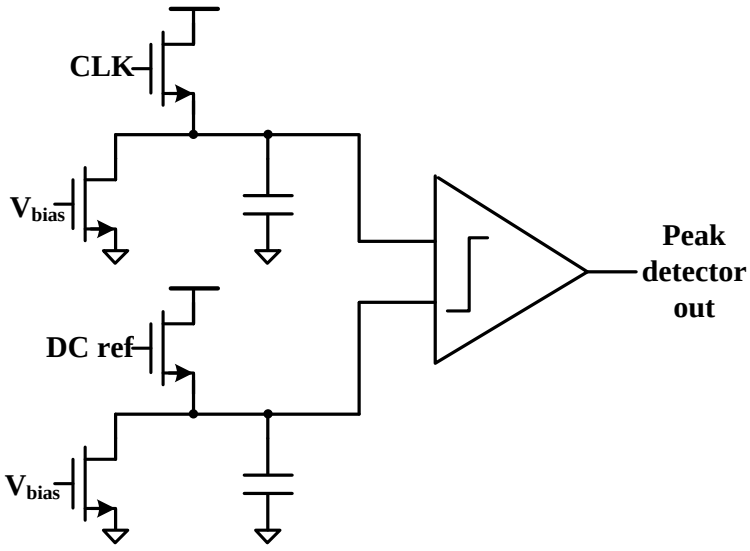

Figure 3.18. Peak detector.

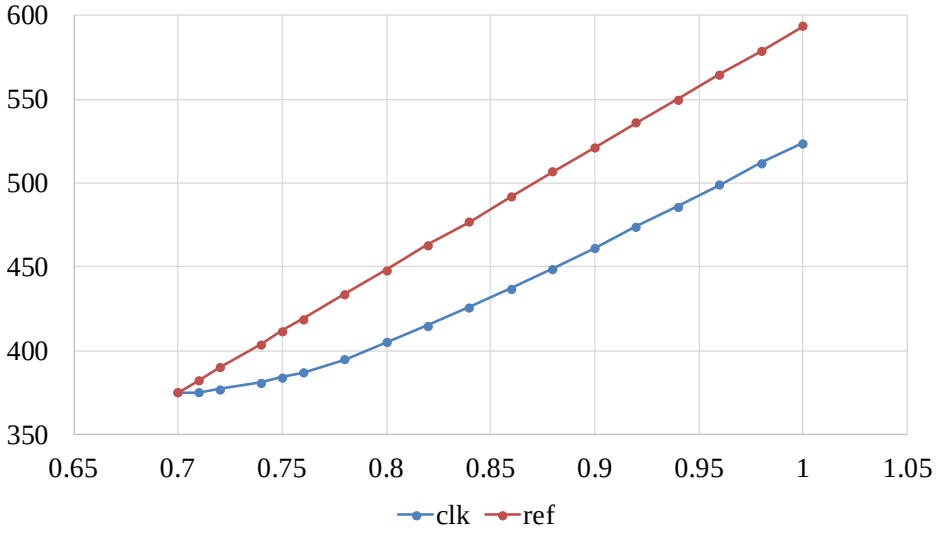

Figure 3.19. Simulation result of the peak detector.

output at the peak value of the input clock. The second stage of the peak detector is a clocked-comparator. Figure 3.19 is the input-to-output simulation result graph of the first stage of the peak detector.

The transient simulation results showing the amplitude control feedback loop locking behavior are shown in Figure 3.20. The waveform of output clock (I, Ib, Q, Qb) and peak detector output are shown.

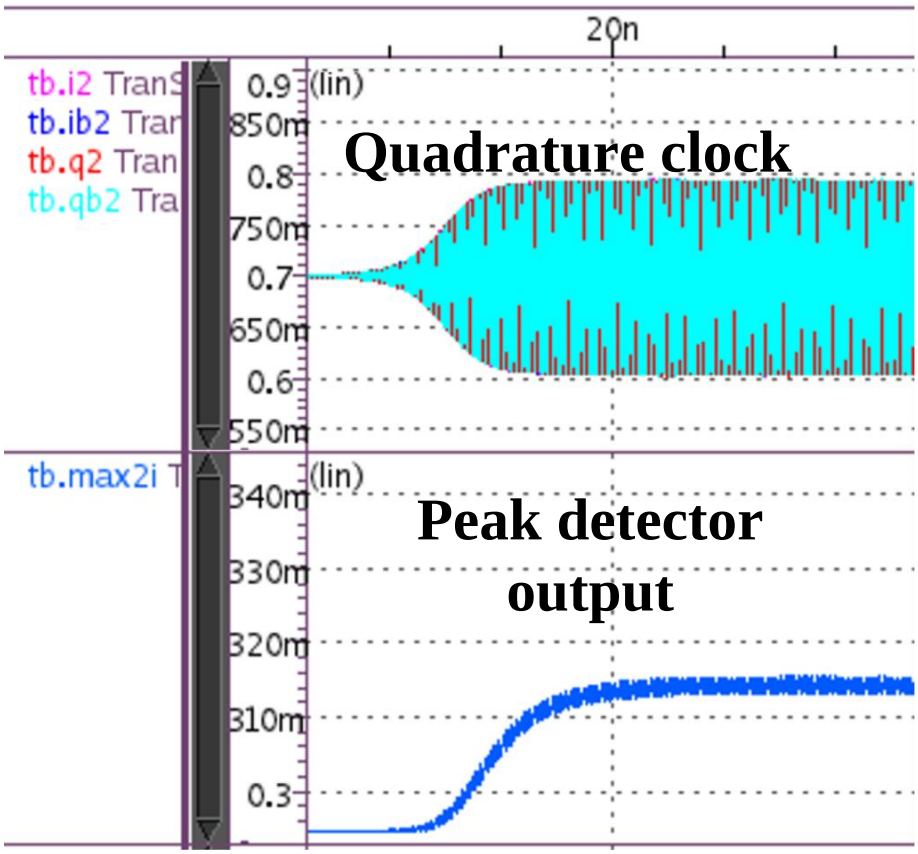

Figure 3.20. transient simulation results showing the amplitude control feedback loop locking behavior

3.7 Injection Cell

3.7.1 Overview

As described in the previous chapter, the resonant clocking scheme and ILO are structurally very similar. In ILO, the injection cell takes over the role of the input buffer of the resonant clocking scheme. Therefore, it is very important to decide how to inject the input clock and design the injection cell and peripheral circuits suitable for the method.

In this section, two methods for input injection are described. One is to inject single-phase pulse and the other is to inject quadrature clock. The structure of the injection cell is different depending on the injection method. Two types of chips designed each way of the input injection are fabricated, and there is no significant difference in injection performance itself.

However, since the method of injecting the single-phase pulse is advantageous for the configuration of the measurement environment and the circuit design complexity of the method of injecting the single-phase pulse is low, other sections of this thesis mainly describe the chip implemented by the method of injecting the single-phase pulse.

3.7.2 Single-Phase Pulse Injection

Single-phase pulse injection is a method of injecting a pulse generated using a single-ended input clock. Since the switch structure can be used as an injection cell, it has the advantage of simple circuit design. However, because the input is injected into only one of the four output nodes (I, Ib, Q, and Qb) in the quadrature oscillator, distortion may inevitably occur in only one of the output clocks, and an asymmetrical output may occur.

Figure 3.21 is a block diagram of a switch-type injection cell and a pulse generation block used in a single-phase pulse injection method. The proposed quadrature resonant clock uses a single NMOS as an injection switch. In general, when injecting pulses to the LC oscillator using a switch, the method of shortening complimentary nodes is often used as shown in Figure 3.22. However, in the proposed design, the output node is shorted to GND using an NMOS switch. The reason why the structure of shortening the GND and output clock nodes is used is that sufficient injection strength can be obtained even if a smaller NMOS is used than the shortening method

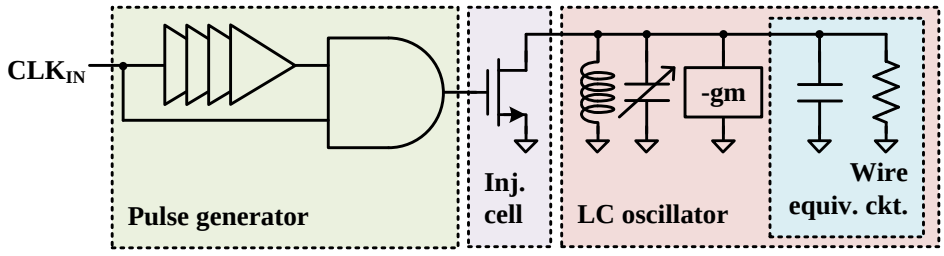

Figure 3.21. Injection cell and pulse generator.

of the complimentary node. The simulated PDR curve along the width of the NMOS (2 μm, 4 μm, 6 μm) is shown in the Figure 3.23. The results of the injection lock range simulation when using such an injection cell are shown in Figure 3.24. The 2-um width injection cell is used and it is the result of the input injection into the free running oscillator without frequency tuning.

The pulse used for injection is generated simply by using a delay line and an AND gate so that the power consumption is minimized. The pulse width that has a decisive effect on the injection strength is the same as the delay time of the delay line, and is generally used at about a quarter of the clock period. The delay line is digitally controlled by the 6-bit control signal and the delay of it is designed to be adjustable from 20- 90 ps.

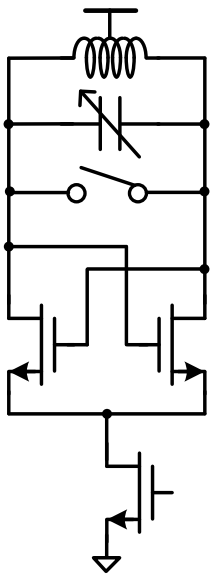

Figure 3.22. Conventional design of injection-locked LC oscillator.

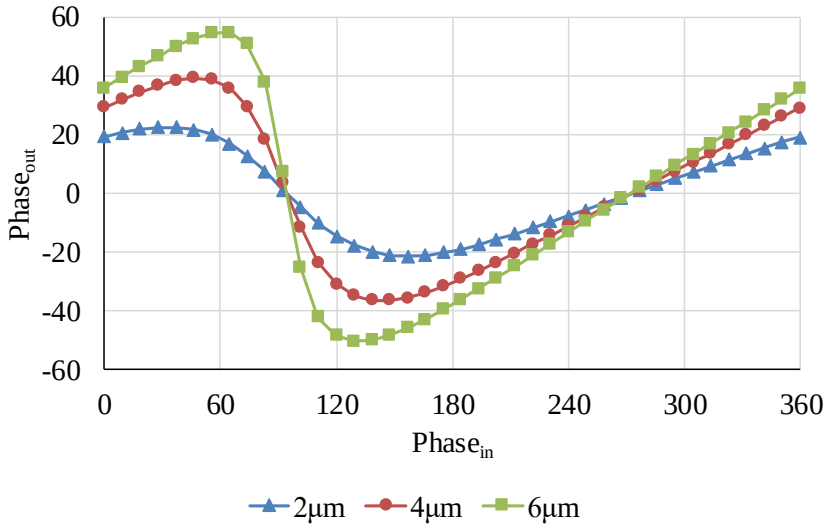

Figure 3.23. PDR curve of the injection cell.

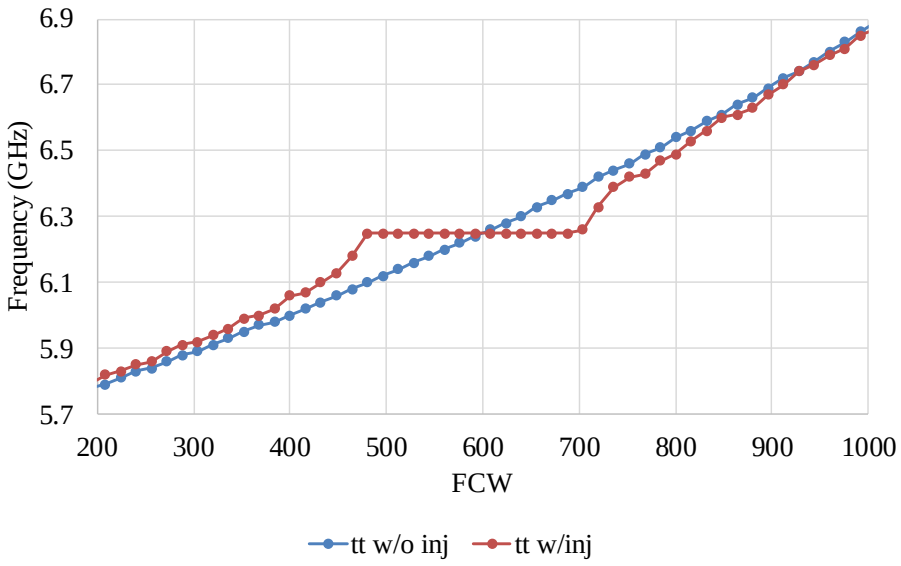

Figure 3.24. Injection lock range simulation.

However, the single-phase pulse injection structure has a problem as shown in the Figure 3.25. In most ILOs, it is common that the clock distortion occurs while the injection cell is switched on. However, in this single-phase injection structure, since the input is injected into one of the four phases, distortion occurs only in one of the quadrature clocks. This asymmetric distortion causes quadrature phase error and may cause problems in quarter-rate circuit operation. According to the simulation results shown in the Figure 3.25, phase error of about 2° may occur. To remove the phase error, it is recommended to remove asymmetric distortion using a poly-phase filter (PPF) or phase error correction circuits.

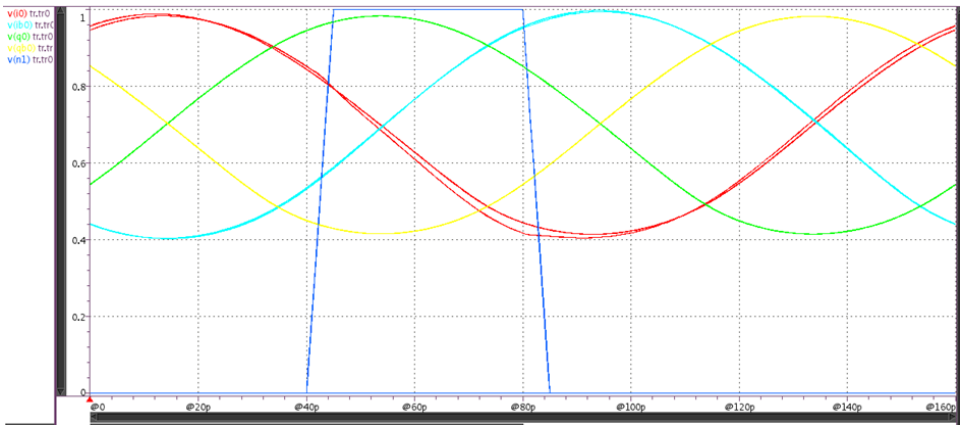

Figure 3.25. simulation result of the asymmetric distortion of output clock.

3.7.3 Quadrature Clock Injection

As discussed in the previous section, when only a single-phase pulse is injected into a quadrature oscillator, distortion occurs in the quadrature output clock, causing a problem of phase error. Since the phase error of the multi-phase clock can cause problems in a multi-rate system using the clock, a method other than single-phase injection may be an alternative.

Quadrature clock injection is one of the injection methods that can prevent clock skew. As shown in the Figure 3.26, asymmetric distortion can be prevented by injecting the input to the quadrature oscillator using a differential pair. It also has the advantage of not requiring a pulse generator because it is a differential pair structure.

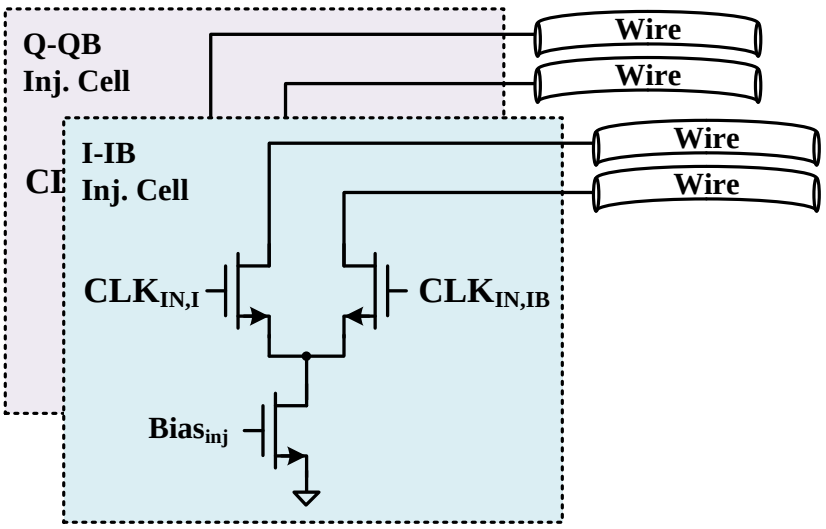

Figure 3.26. Quadrature clock injection scheme.

Therefore, this structure is suitable for applications where the input clock is not a single-ended multi-phase clock. If the input clock is a single-ended or differential clock rather than a quadrature, a multi-phase generation block such as PPF or delay locked loop is required. In this case, the quadrature clock injection method is not suitable because design complexity and power consumption may increase.

Chapter 4

Measurement

4.1 Overview

The prototype chip of the proposed quadrature resonant clocking scheme has been fabricated in 65-nm CMOS technology and photomicrograph of the chip is shown in the Figure 4.1. The active area of the prototype chip occupies an area of 0.004 mm^2. The prototype chip includes quadrature clock distribution wires, proposed quadrature resonant clock generator, two inductors, two tuning capacitors, sine wave-to-full-swing CMOS converters (S2C converter) for comparison with other types of clock distribution buffers, and a monitor circuit for measuring the internal clock amplitude. The measurement setup is depicted in Figure 4.2.

There are two ways to measure the quadrature phase of the high frequency output clock. One is to measure the waveform of the high frequency quadrature clock directly,

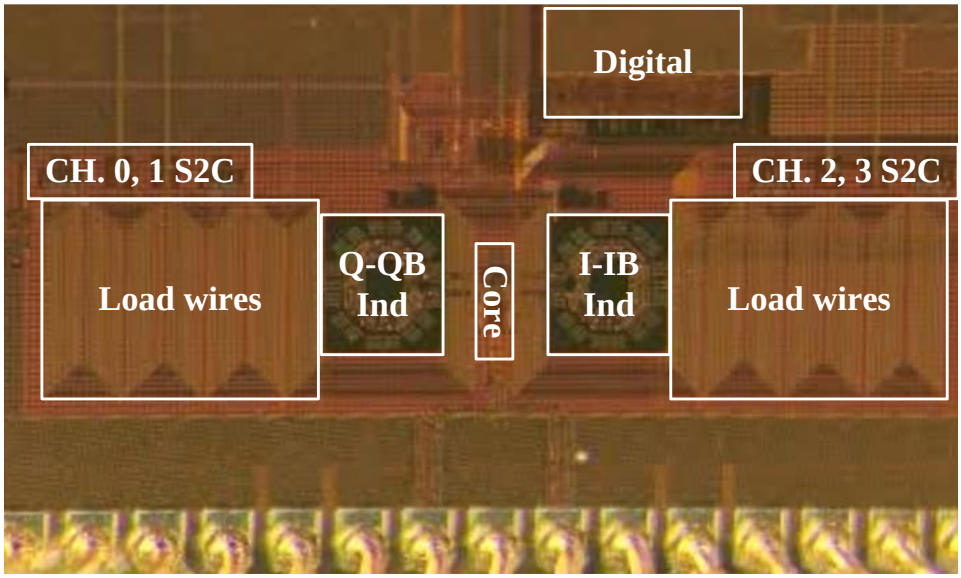

Figure 4.1. Photomicrograph of the prototype chip.

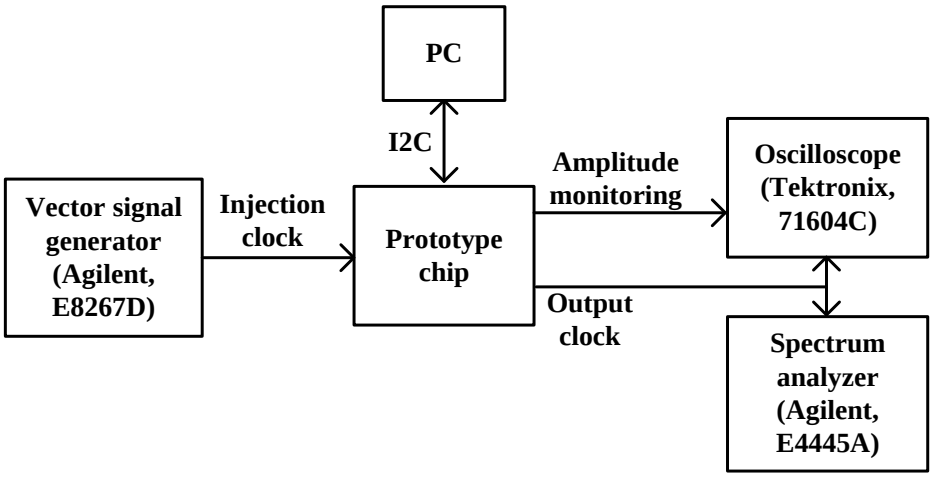

Figure 4.2. Measurement setup.

and the other is to measure the clock waveform that is down converted using a mixer as shown in the Figure 4.3 [46] . The down converting method using a mixer is a method of measuring the waveform of a clock with a low frequency while maintaining the phase of the quadrature output clock. Therefore, it has the advantage of being less affected by external noise. However, there is a difficulty in that a clock having a frequency similar to the frequency of the output clock is additionally required. Therefore, in the proposed quadrature resonant clocking scheme, a method of directly measuring the waveform of the output clock is used. Also, as shown in the Figure 4.4, a method of sharing output path of the quadrature clock using multiplexer (MUX) is used to minimize delay mismatch in the output path.

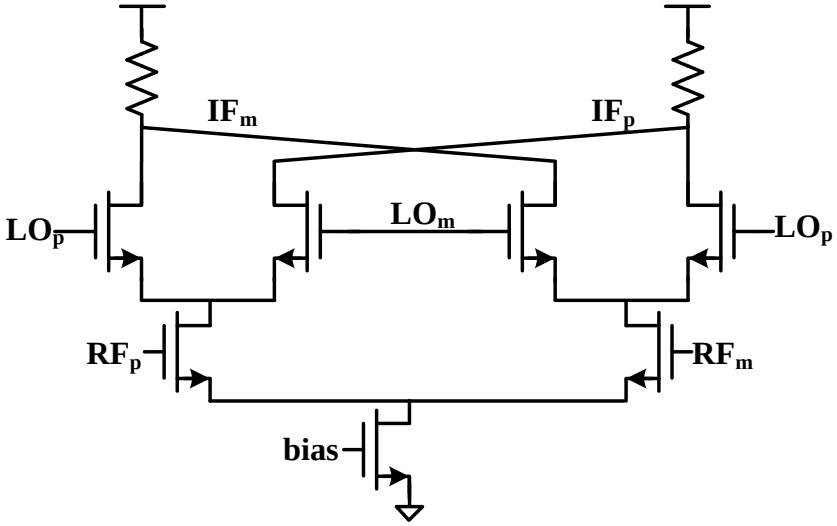

Figure 4.3. Gilbert mixer.

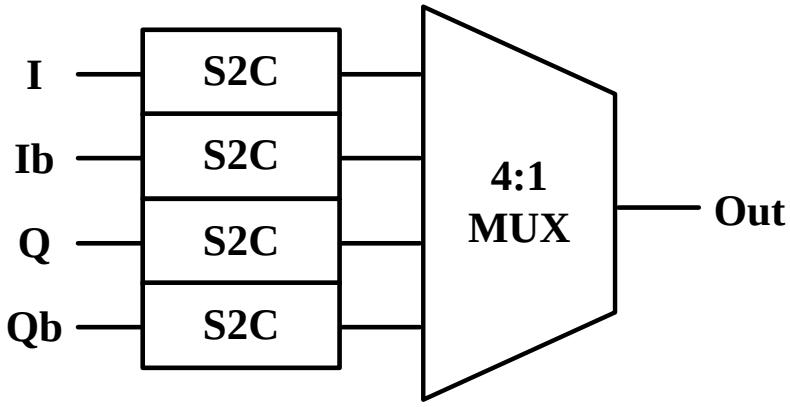

Figure 4.4. Output stage of the output quadrature clock using MUX.

4.2 Power Consumption

Measured total power consumption of the proposed quadrature resonant clocking scheme is 11.92 mW at the operation frequency of 7 GHz. The LC quadrature oscillator core including the negative gm cell and the quadrature coupling cell consumes 6.2 mW and the remainder is consumed by 4-channel S2C converters and a pulse generator. Detailed power breakdown of the proposed quadrature resonant clocking scheme is described in the Table 4.1.

To compare the power consumption of the proposed quadrature resonant clocking scheme and the other types of clock distribution buffers, a CMOS-based buffer and a CML-based buffer that distribute the clock on the same load wires as that used by the proposed resonant clocking scheme are designed and simulated.

The proposed quadrature resonant clock scheme consumes about 20-25% less power when compared with CMOS-based clock as depicted in the Figure 4.5. In addition, proposed quadrature resonant clocking scheme shows a large reduction in

Table 4.1. Power breakdown.

Block	Power (mW)
Quadrature core	6.2
Pulse generator	0.5
S2C	5.2

power consumption in all frequency ranges.

The Figure 4.6 shows the comparison with CML-based clock buffers when the clock peak-to-peak swings are varied. When driving the same wire, the proposed scheme consumes 23-34% less power than the CML-based clock buffers with the same peak-to-peak swing.

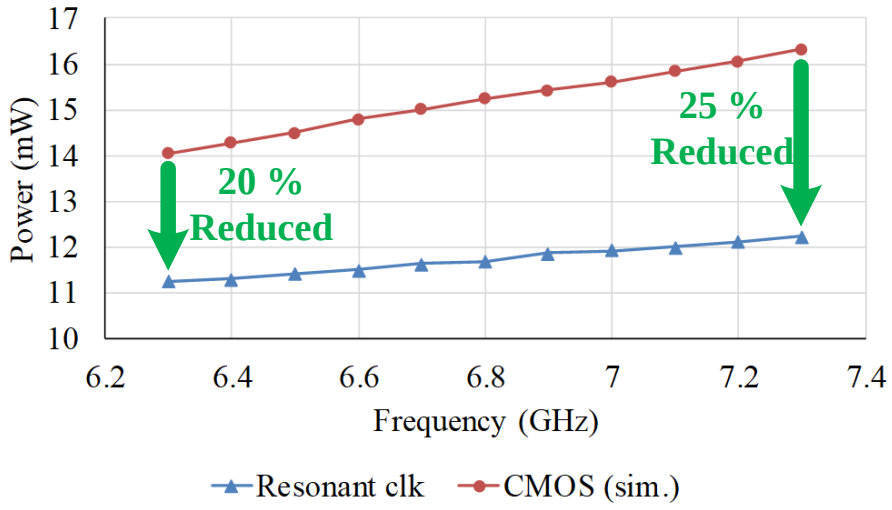

Figure 4.5. Total power consumption compared with CMOS-based clock buffer.

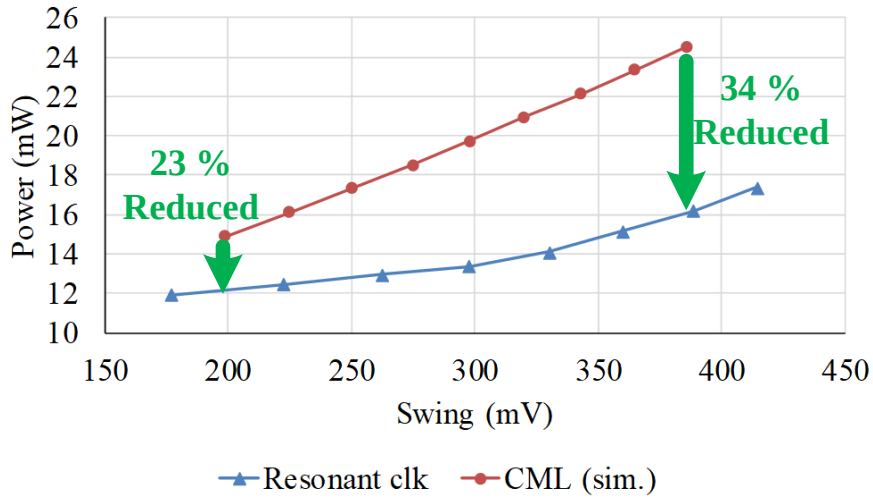

Figure 4.6. Total power consumption compared with CML-based clock buffer.

4.3 Internal Amplitude Monitoring

In order to verify the operation of the amplitude control loop, it is necessary to be able to measure the amplitude of the clock inside the chip. The circuit shown in the Figure 4.7 is the amplitude monitoring circuit which consists of a sampler and a delay line. By 2-dimensional sweep of V_{REF} and V_{CTRL} which controls the delay of the sampling clock, the internal clock waveform can be measured as presented in the Figure 4.8. It is difficult to measure the phase of the clock perfectly due to the problem of the sampler offset, hysteresis characteristic of the sampler, random noise, and linearity of the delay line, but the maximum, minimum value and peak-to-peak amplitude of the internal clock can be measured. The measured values are 0.965 V, 0.716 V, 0.249 V respectively.

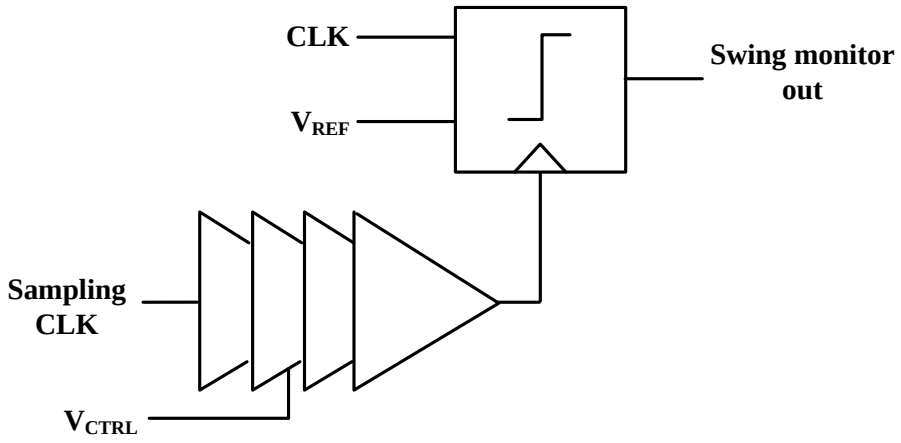

Figure 4.7. Internal amplitude monitoring circuit.

The Figure 4.9 shows the measured amplitude of the internal clock when the amplitude control feedback loop is enabled or disabled when the current bias of the negative gm cell is arbitrarily changed. When the amplitude control feedback loop is enabled, the amplitude of the clock remains constant even if the external conditions change.

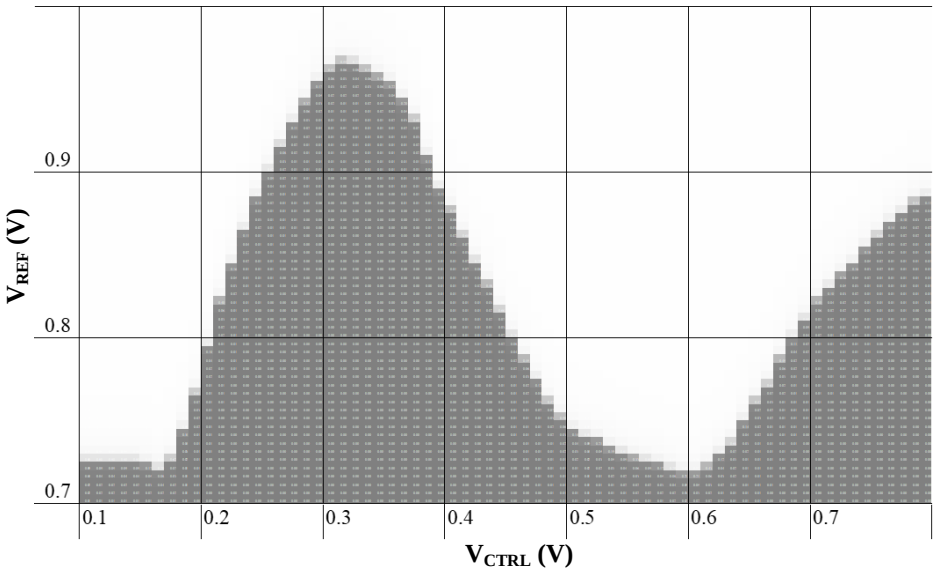

Figure 4.8. Measured internal clock waveform.

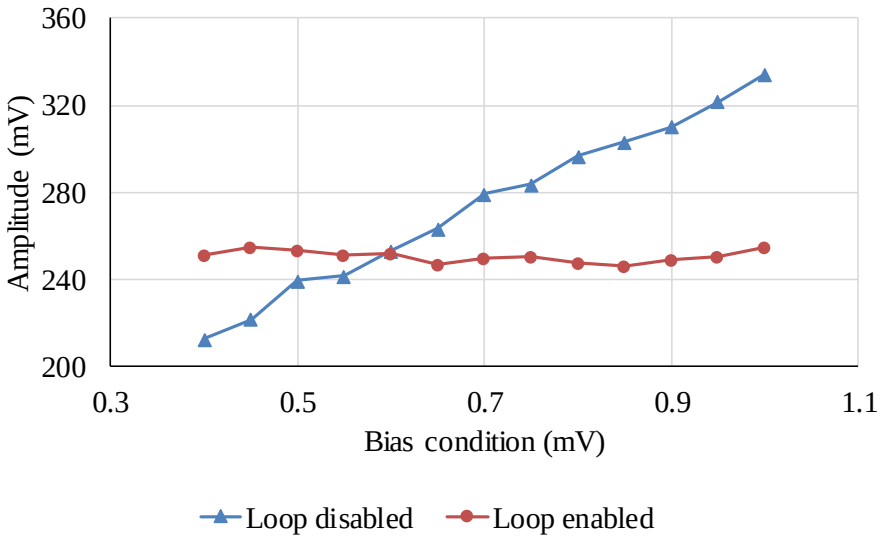

Figure 4.9. Amplitude control loop functionality test result.

4.4 Output Clock Characteristic

The waveform of the output clock of the proposed quadrature resonant clocking scheme is measured as shown in the Figure 4.10. The phase error of the four phases are measured as less than 3°. 1-UI period jitter is measured as 573.6 fs_{rms}.

Figure 4.11 shows the phase noise plot of the output clock in 7-GHz operation and measured result is -138.37 dBc/Hz at 1 MHz offset. Meanwhile, Figure 4.12 shows the phase noise plot of the 7-GHz input clock and measured result is -137.31 dBc/Hz

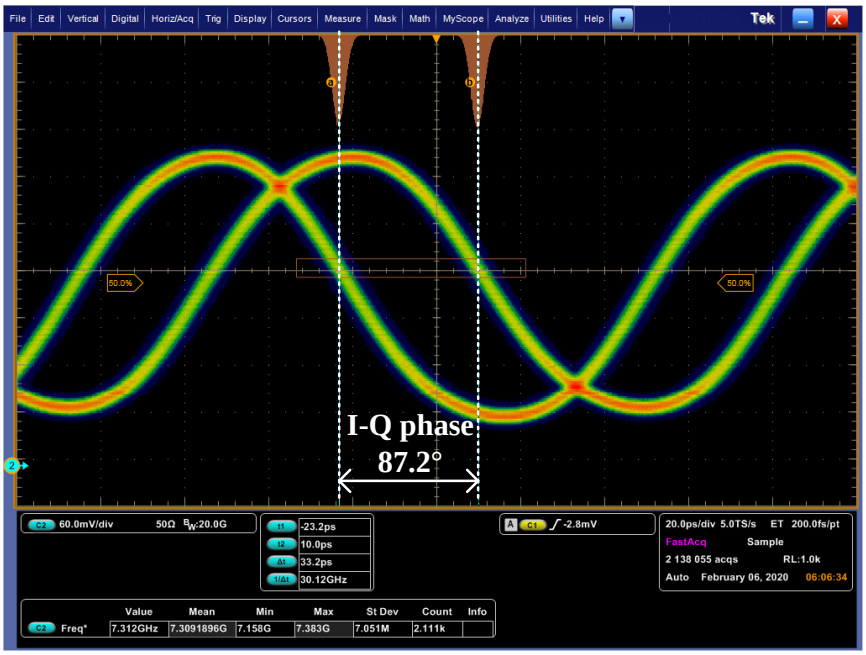

Figure 4.10. Waveform of the output clock.

at 1 MHz offset. Just as the well-designed, tuned ILO exhibits the lowpass jitter filter characteristics on the oscillator phase noise, the proposed clock generator offers very low jitter limited by the phase noise of the input clock source. The measurement results of phase noise when matched or unmatched resonant and operation frequencies are shown in the Figure 4.13. Phase noise performance is better when the resonant frequency is tuned to the operation frequency compared with the case when the operation frequency is changed while the resonant frequency is fixed at 7 GHz.

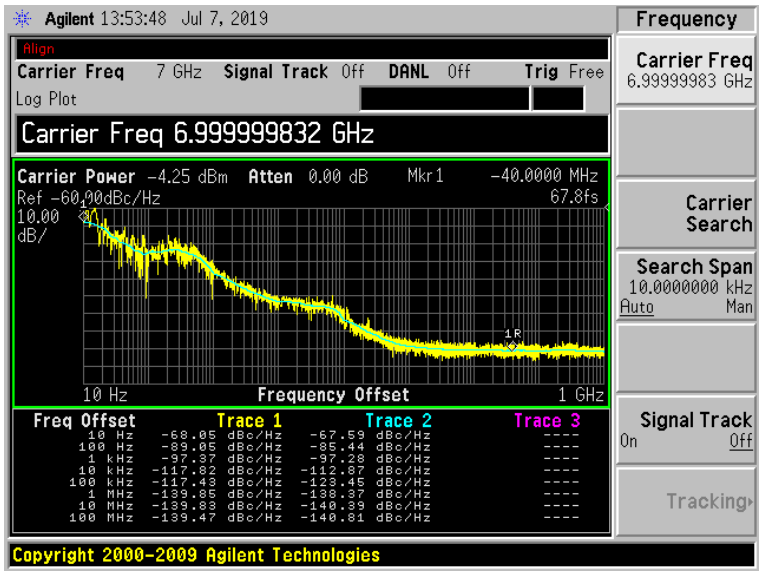

Figure 4.11. Phase noise of the output clock at 7 GHz operation.

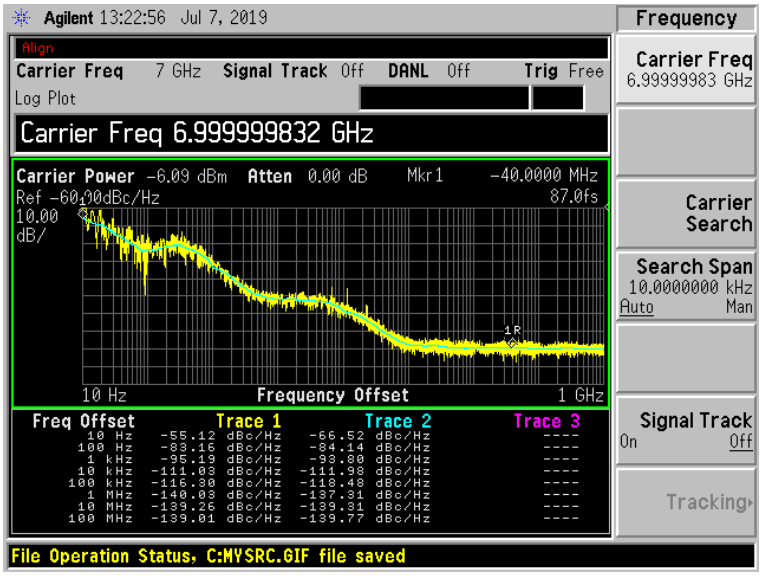

Figure 4.12. Phase noise of the input clock.

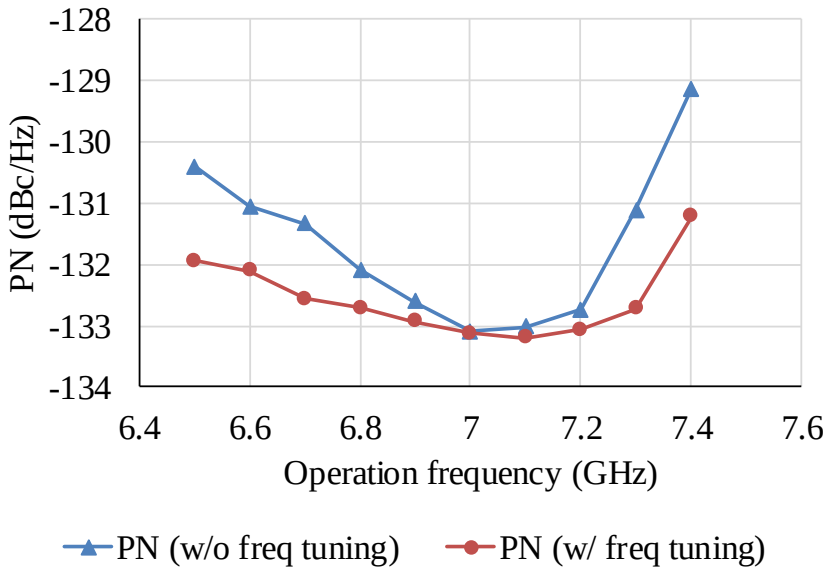

Figure 4.13. Phase noise comparison w/ and w/o frequency tuning

4.5 Summary

The performance of the proposed quadrature resonant clock is summarized and compared with the previous works in the Table 4.2. The proposed quadrature resonant clock, when compared with the conventional resonant clocks, exhibits the high power reduction ratio under all operating conditions by tuning out the frequency mismatch using the frequency tuning capacitors. Because of the [7] and [27] has 830 and 16 sectors respectively, it is unfair to simply compare total power. Therefore, the following figure of merit (FoM) is suggested.

$$FoM = \frac{(Total\ power)}{(Load\ wire\ capacitance) * (Frequency)}. \quad (4.1)$$

Table 4.2. Table comparing proposed quadrature resonant clock with the state-of-the art scheme.

	Chan, JSSC'09 [7]	**Sathe, JSSC'13 [8]**	**Xu, JSSC'09 [27]**	**Restle, ISSCC'14 [35]**	**This Work**
Technology	90 nm	32 nm SOI	0.18 um	22nm SOI	65 nm CMOS
Type	Single-ended	Single-ended	Single-ended	Single-ended	Quadrature
Load wire capacitance	2 nF	N/A	100 pF	N/A	2.236 pF
Inductance	1.2 nH	0.5-1.3 nH	3 nH	0.3-2.5 nH	0.95 nH
Number of inductors	830	5	16	N/A	2
Q factor	1.6	3.6-3.8	N/A	N/A	4.56
Frequency	4-5 GHz	0.5-4 GHz	2 GHz	2.5-5 GHz	6.3-7.3 GHz
Total power	24 W	N/A	500 mW	N/A	11.92 mW
Power reduction	5-25 %	0-35 %	N/A	0-37 %	20-34 %
FoM	2.4 mW/pF/GHz	N/A	2.5 mW/pF/GHz	N/A	0.76 mW/pF/GHz

Chapter 5

Conclusion

In this thesis, a 7 GHz quadrature resonant clocking scheme with the resonant frequency tuning capacitors and amplitude control feedback loop is described. The proposed resonant clocking scheme distribute the input clock through 4.3 mm load wire which capacitance is almost 600 fF.

By using the tuning capacitor, frequency difference between the operation frequency and the LC resonant frequency is barely exist. By reducing the frequency mismatch, optimized power reduction is achieved under the all operation condition while reducing the phase noise. Also, the amplitude control feedback loop is employed to maintain the constant clock amplitude under PVT variations.

A prototype chip fabricated in 65-nm CMOS technology occupies 0.004 mm^2, and consumes 11.92 mW at 7 GHz. The quadrature oscillator core consumes 6.2 mW Power reduction is between 20% to 25% when compared with the CMOS-base clock buffers and 23% to 34% when compared with conventional CML-based clock buffers.

Measured phase noise of the output clock is -138.37 dBc/Hz at 1 MHz offset while phase noise of the input clock is -137.31 dBc/Hz at 1 MHz offset. The proposed clock generator offers very low jitter limited by the phase noise of the input clock source. The phase error of the quadrature phases is measured as less than 3°. 1-UI period jitter is measured as 573.6 fs_{rms}.

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초 록

본 논문에서는 클럭 전달을 위한 4.3mm 전선을 통해 클럭을 전달하는 회로를 인덕터와 커패시터의 공진현상을 이용해서 저전력을 소모하여 설계할 수 있는 방법을 제시한다. 또한 두 개의 피드백 루프를 포함하고 있다. 주파수 조절을 위한 피드백 루프는 공진 주파수를 조절하여 동작 주파수와의 차이를 제거한다. 그렇게 함으로써 모든 주파수 조건에서 저전력, 고효율 동작이 가능해지며 위상 노이즈 및 지터 특성도 좋아진다. 진폭 조절을 위한 피드백 루프는 외부 조건이 변화하는 상황에서도 일정한 진폭을 가지는 클럭이 나오도록 한다. 이러한 내용들을 검증하기 위하여 65nm CMOS 공정을 이용하여 프로토타입 칩을 제작하였다. 전력 소모 측정 결과, 본 논문에서 제안하는 방식은 11.92mW 의 전력을 소모한다. 또한 기존에 사용해왔던 CMOS 방식의 클럭 전달용 버퍼에 비해서는 같은 주파수 조건에서 약 20-25% 가량 적은 전력을 소모한다. 그리고 CML 방식의 버퍼와 같은 진폭을 가지는 경우로 비교하는 경우에는 약 23-34% 가량 적은 전력을 소모한다. 지터는 측정 결과 $573.6fs_{rms}$ 로 확인되었고, 1MHz 오프셋에서의 위상 노이즈는 -138.37dBc/Hz 로 측정되었다.

주요어 : 주입 고정 발진기, 주파수 조정, 진폭 조절 피드백 루프, 클럭 전달, 쿼드러처 레조넌트 클럭

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