Ph.D. DISSERTATION

The Effect of Interfacial Layer on the Electrical Properties of Atomic-Layer-Deposited p-Type SnO Thin-Film Transistors

by

Younjin Jang

February 2021

DEPARTMENT OF MATERIALS SCIENCE AND ENGINEERING

COLLEGE OF ENGINEERING

SEOUL NATIONAL UNIVERSITY

The Effect of Interfacial Layer on the Electrical Properties of Atomic-Layer-Deposited p-Type SnO Thin-Film Transistors

Advisor : Prof. Cheol Seong Hwang

by

Younjin Jang

A thesis submitted to the Graduate Faculty of Seoul National University in partial fulfillment of the requirements for the Degree of Doctor of Philosophy

Department of Materials Science and Engineering

February 2021

Approved

by

Chairman of Advisory Committee : Jin Young Kim

Vice-chairman of Advisory Committee : Cheol Seong Hwang

Advisory Committee : SangBum Kim

Advisory Committee : Jeong Hwan Han

Advisory Committee : Woojin Jeon

Abstract

This dissertation investigates the improvement of the electrical properties of thin-film transistor (TFT) devices using atomic-layer deposition (ALD)-based high-quality p-type SnO thin film, with the aim of securing research technology for next-generation semiconductor channels and dielectric film materials.

First, the origin of hysteresis in the drain-source current (I_{DS}) – gate-source voltage (V_{GS}) characteristics of ALD p-type SnO TFTs was examined by adopting ALD Al_2O_3 interfacial layers (IL) between the SnO channel layer and the SiO_2 gate insulator (GI) layer. The SnO TFTs with SiO_2 GI exhibited a large hysteresis voltage (V_{hy}) owing to the trap state density near the interface between the SnO active layer and the SiO_2 GI (border trap). Both the experimental results and the theoretical calculations showed that the origin of the border traps was the Sn_{Si}^{+0} gap states in SiO_2, which was induced by the Sn diffusion into the SiO_2 layer. The adoption of Al_2O_3 films as ILs suppressed the Sn diffusion. The effectiveness of IL, however, is dependent on the thickness, crystallinity, and density of the Al_2O_3 films. The V_{hy} of the SnO TFTs can be decreased when the thickness and density of the ILs increase as long as the amorphous structure of the Al_2O_3 IL is maintained after the rapid thermal annealing (RTA) process. The p-type ALD SnO TFTs with optimum ILs exhibited a high on/off ratio of I_{DS} (1.2×10^5), high field effect mobility

($1.6\ cm^2V^{-1}s^{-1}$), and a small V_{hy} (0.2 V).

Second, abnormal electrical properties in SnO devices with Al_2O_3 interfacial layer were examined. An in-depth analysis was conducted on how mobile oxygen vacancies (V_O) in the IL thin film affects three types of characteristics; the V_{GS} dependence, gate current characteristics, and capacitance characteristics.

One of the abnormal characteristics is the V_{GS} dependence. The gate-induced electrical instability of SnO TFTs with SiO_2 and Al_2O_3/SiO_2 gate dielectric layers was evaluated. The V_{hy} and threshold voltage (V_{th}) in the transfer characteristics of SnO TFTs depended on the sweep range and rate of V_{GS}. The TFT with an Al_2O_3/SiO_2 gate dielectric layer exhibited reduced V_{hy} and stable V_{th} compared to the device without an Al_2O_3 layer. The introduction of an Al_2O_3 layer between the SnO channel and the SiO_2 layer suppressed the electron and hole trapping at the channel/dielectric interface and contained V_O's that counteracted the hole trapping effect.

Another abnormal characteristics due to V_O's inside the Al_2O_3 IL is reflected in the gate current characteristic. A large I_{GS} is related to the field-induced migration of the V_O's in the Al_2O_3 layer. The V_O could produce an internal electric field that could balance with the external electric field. The charge transfer through the gate dielectric could be affected, and gate leakage can be dominant compared to the channel current in the depletion bias region. As a results, the hysteresis directions of I-V and C-V do not coincide with each other.

The other abnormal characteristics due to V_O's inside the Al_2O_3 IL is reflected in the capacitance characteristic. The additional capacitance is observed in the specific voltage. At the sufficiently negative V_{GS}, most of the V_O must be dragged toward the Al_2O_3/SiO_2 interface, making them inactive to the AC stimulus (hole trapping/detrapping) in the accumulation bias region. It seems that the energy level of the V_O within the bandgap of the SnO is closer to the valence band, so it incurs the additional capacitance by hole trapping in the accumulation region. However, as the V_{GS} further decreased, the V_O's are migrated toward the Al_2O_3/SiO_2 interface again, which removed the additional capacitance at sufficiently negative V_{GS} region.

Third, in order to improve the performance of the SnO TFTs, an Al-doped HfO_2 (Al: HfO_2) thin film having a high dielectric constant replacing the Al_2O_3 thin film was adopted as an IL. Al doping can suppress the crystallization of HfO_2 thin film, but it acts as an obstacle to the thin film density, greatly deteriorating the performance of the SnO TFT device. On the other hand, when the crystallized Al: HfO_2 IL was adopted, a large V_{hy} (6.4 V) was shown, but excellent TFT device performance (μ_{FE}= 5.7 $cm^2/V{\cdot}s$, SS= 0.39 V/dec., I_{on}/I_{off}= 5.6×10^5) were achieved due to the high dielectric constant of HfO_2-based film (ε_r=26). Although it was necessary to apply bias stress for a long time for program and erase operation, the SnO/Al:HfO_2/SiO_2 stacked TFTs demonstrated electrical programmable and erasable characteristics as well as data retention capability. Therefore, SnO TFT devices can be used for memory devices as well as electronic circuits according to IL materials with different

hysteresis characteristics.

Keywords: p-type tin monoxide, atomic layer deposition, oxide thin-film transistors, interfacial layer, diffusion barrier, high-k gate dielectric, hysteresis voltage, threshold voltage, trap states, charge trapping, oxygen vacancy, ionic charge effect

Student Number: 2014-21554

Younjin Jang

Table of Contents

List of Figures

List of Tables

List of Abbreviations

AES	Auger electron spectroscopy
AFM	Atomic Force Microscopy
AIMD	ab initio molecular dynamics
ALD	Atomic Layer Deposition
BE	Bottom electrode
BW	Backward
CBM	Conduction band minimum
CCW	Counterclockwise
CET	Capacitance-equivalent thickness
CMOS	Complementary metal oxide semiconductor
CVD	Chemical vapor deposition
CW	Clockwise
DFT	Density functional theory
DOS	Density of states
EDS	Energy-dispersive spectroscopy
$E_{ext.}$	External electric field
$E_{int.}$	Internal electric field
E_{ox}	Effective oxide electric field
E_{VO}	The energy level of the oxygen vacancy (V_O) within the bandgap of the SnO
FE-SEM	Field-emission scanning electron microscopy
FFT	fast Fourier transform
FIB	Focused ion beam
FW	Forward

GAXRD	Grazing-angle incidence X-ray diffraction
GI	Gate insulator
GGA	Generalized gradient approximation
HRTEM	High-resolution transmission electron microscopy
HSE	Heyd, Scuseria, and Ernzerhof
I_{DS}	Drain-source current
$I_{GS,}$ I_G	Gate-source current or gate current
IL	Interfacial layer
I_{on}/I_{off}	On-off ratio of drain-source current
NBS	Negative Bias stress
N_{bt}	Border trap density
N_{it}	Interface trap density
PAW	Projector-augmented wave
PBE	Perdew, Burke, and Ernzerhof
PDA	Post-deposition annealing
RTA	Rapid thermal annealing
SE	Spectroscopic ellipsometry
$Sn(dmamp)_2$	Bis(1-dimethylamino-2-methyl-2propoxy)tin(II)
SR	Sweep rate
SS	Subthreshold swing
STEM	Scanning transmission electron microscopy
TFT	Thin-film transistor
TMA	Trimethyl aluminum
TOF-SIMS	Time-of-flight secondary ion mass spectrometer
VASP	Vienna Ab Initio Simulation Package
VBM	Valence band maximum
V_{BE}	Bottom electrode voltage

V_{DS}	Drain-source voltage
V_{GS}, V_G	Gate-source voltage or gate voltage
V_{hy}	Hysteresis voltage
$V_O^{\cdot\cdot}$	Doubly ionized oxygen vacancy
V_{th}	Threshold voltage
XRF	X-ray fluorescent spectroscopy
XRR	X-ray reflectivity
XPS	X-ray photoelectron spectroscopy
μ_{FE}	Field-effect mobility

1. Introduction

1.1. Overview

Semiconducting-oxide-based thin-film transistors (TFTs) have attracted for use in display, storage memory, and complementary logic circuits due to their properties, including transparency, low processing temperature, and high carrier mobility [1–3]. The fabrication of the complementary metal oxide semiconductor (CMOS) circuit, however, which is indispensable for a low-power-consuming electronic circuit, has been deterred by the (i) unavailability of high-performance p-type semiconducting oxides and (ii) the low electrical characteristics of the p-type oxide TFTs compared to those of n-type ones [4,5]. As the valence band maximum (VBM) of the oxide semiconductor is located very deep from the vacuum level, it is difficult to find a suitable shallow acceptor, which makes p-type doping difficult [6]. Also, the VBM of the oxide semiconductor is mainly composed of localized O *2p* orbitals, resulting in low hole mobility [6,7]. Therefore, increasing the energy level and the dispersion of VBM are the key factors to achieving high-performance p-type oxide semiconductors. Hybridization with a spherical metal orbital close to the O *2p* energy level has been suggested to overcome these problems [7], and the p-type characteristics of various p-type oxide materials, such as Ag_2O, Cu_2O, $CuAlO_2$, SnO, and NiO, were evaluated. According to Togo *et al.*[8] and Ogo *et al.*[9], Tin monoxide (SnO) could be the most promising p-type material because there

is a significant overlap of O *2p* and Sn *5s* orbitals in its valence band, which can induce high hole mobility. The simple layered structure of SnO is additional merit of such material.

SnO, however, is a meta-stable phase compared with the fully oxidized SnO_2, and thus, it could be easily oxidized to SnO_2 through oxidation under an oxygen-abundant condition ($SnO + O_2/2 \rightarrow SnO_2$) or through disproportionation reaction even without oxygen ($2SnO \rightarrow SnO_2 + Sn$) [10,11]. Therefore, the process window for achieving phase-pure SnO is narrow and sensitive to the various process conditions, such as the pressure, deposition and post-deposition annealing (PDA) temperatures, gas atmosphere, and passivation conditions [12–18]. Most of the past relevant researches in the field were conducted using the radio frequency (RF) sputtering method with an high-purity SnO target at a sufficiently low pressure to deposit the SnO thin films. Nonetheless, the sputtering technique is often inadequate for growing a high-quality oxide semiconductor channel material due to the probable involvement of the damaging effect induced by the energetic ion bombardment. The chemical vapor deposition (CVD) process is thus more preferred considering its far less damaging growth condition. The strong tendency to form the more stable SnO_2 phase during the CVD process, however, hinders the growth of the SnO film [19–23].

It was recently reported that p-type SnO thin films were successfully fabricated using the atomic layer deposition (ALD) method when the Sn ion in

the Sn precursor (bis(1-dimethylamino-2-methyl-2-propoxy)tin(II), $Sn(dmamp)_2$, which was also adopted in this work) has a +2 oxidation state, and H_2O was adopted as the oxygen source [24,25]. Compared to the sputtering method, the ALD method has the advantages of highly conformal growth on a high-aspect-ratio structure and a low damage effect, which are suitable features for three-dimensionally stacked devices. Also, the optimal thickness of the SnO channel layer for the high-performance TFT device, especially with a high I_{on}/I_{off} current ratio of I_{DS}, is only ~5–10 nm, which can hardly be precisely controlled by the conventional sputtering technique or CVD. In ALD, the film thickness is determined by the number of ALD cycles, with a given growth per cycle of a highly saturated ALD process. Therefore, an accurate control of the film thickness with high uniformity at the atomic layer over a large wafer area can be achieved. Nevertheless, the research on the ALD SnO film is still at its early stage, and its electrical properties have not been sufficiently analyzed in many previous works.

In this dissertation, the high-performance SnO-based p-type TFTs with improved bias stability with low hysteresis voltage (V_{hy}) was fabricated. For in-depth analysis, the effects of the Al_2O_3 barrier layer on the device performance of the p-type SnO TFT were further exploited, focusing on the threshold voltage (V_{th}) instability, displacive gate current, and additional capacitance effect. In additon, a comparative study on electrical characteristics of p-type SnO TFTs with Al_2O_3 and Al-doped HfO_2 interfacial layer (IL) was conducted. This study

will be helpful to provide the useful design concept for high performance p-channel SnO devices.

The organization of this dissertation is as follows. Chapter 2 gives brief descriptions based on the relevant literatures reviewed. Descriptions about the overview of p-type metal oxide semiconductor, the p-type SnO, the p-type SnO thin films grown by ALD and its application to TFTs will be concerned. Chapter 3 explains the growth behavior and characterizations of p-type SnO thin films grown by ALD. In addition, optimization of fabrication process for ALD SnO TFT will be demonstrated. Chapter 4 presents electrical performances of ALD SnO TFTs with and without an Al_2O_3 IL. It scrutinizes the influences about chemical reaction between the channel material and gate insulator (GI) depending on IL conditions. Chapter 5 provides in-depth analysis of IL-inserted SnO device with reduced V_{hy}, which show abnormal electrical properties. Chapter 6 explains the results of the investigations about the effect of different IL on the performance of SnO TFTs. Chapter 7 provides the conclusion of the dissertation.

1.2. Bibliography

[1] A. Nathan, S. Lee, S. Jeon, J. Robertson, *J. Disp. Technol.* **2014**, *10*, 917.

[2] E. S. Hwang, J. S. Kim, S. M. Jeon, S. J. Lee, Y. Jang, D.-Y. Cho, C. S. Hwang, *Nanotechnology* **2018**, *29*, 155203.

[3] E. Fortunato, P. Barquinha, R. Martins, *Adv. Mater.* **2012**, *24*, 2945.

[4] Z. Wang, H. A. Al-Jawhari, P. K. Nayak, J. A. Caraveo-Frescas, N. Wei, M. N. Hedhili, H. N. Alshareef, *Sci. Rep.* **2015**, *5*, 9617.

[5] Y. Li, J. Yang, Y. Wang, P. Ma, Y. Yuan, J. Zhang, Z. Lin, L. Zhou, Q. Xin, A. Song, *IEEE Electron Device Lett.* **2018**, *39*, 208.

[6] N. Sarmadian, R. Saniz, B. Partoens, D. Lamoen, *Sci. Rep.* **2016**, *6*, 20446.

[7] T. Kamiya, H. Hosono, *Int. J. Appl. Ceram. Technol.* **2005**, *2*, 285.

[8] A. Togo, F. Oba, I. Tanaka, K. Tatsumi, *Phys. Rev. B* **2006**, *74*, 195128.

[9] Y. Ogo, H. Hiramatsu, K. Nomura, H. Yanagi, T. Kamiya, M. Hirano, H. Hosono, *Appl. Phys. Lett.* **2008**, *93*, 032113.

[10] L. Y. Liang, Z. M. Liu, H. T. Cao, Z. Yu, Y. Y. Shi, A. H. Chen, H. Z. Zhang, Y. Q. Fang, X. L. Sun, *J. Electrochem. Soc.* **2010**, *157*, H598.

[11] M. Batzill, U. Diebold, *Prog. Surf. Sci.* **2005**, *79*, 47.

[12] J. A. Caraveo-Frescas, P. K. Nayak, H. A. Al-Jawhari, D. B. Granato, U. Schwingenschlogl, H. N. Alshareef, *ACS Nano* **2013**, *7*, 5160.

[13] H. Luo, L. Y. Liang, H. T. Cao, Z. M. Liu, F. Zhuge, *ACS Appl. Mater. Interfaces* **2012**, *4*, 5673.

[14] H. Luo, L. Y. Liang, Q. Liu, H. T. Cao, *ECS J. Solid State Sci. Technol.* **2014**, *3*, Q3091.

[15] P.-C. Hsu, C.-C. Wu, H. Hiramatsu, T. Kamiya, H. Hosono, *ECS J. Solid State Sci. Technol.* **2014**, *3*, Q3040.

[16] I.-T. Cho, M. U, S.-H. Song, J.-H. Lee, H.-I. Kwon, *Semicond. Sci. Technol.* **2014**, *29*, 045001.

[17] H. Yabuta, N. Kaji, R. Hayashi, H. Kumomi, K. Nomura, T. Kamiya, M. Hirano, H. Hosono, *Appl. Phys. Lett.* **2010**, *97*, 072111.

[18] H. Luo, L. Liang, H. Cao, M. Dai, Y. Lu, M. Wang, *ACS Appl. Mater. Interfaces* **2015**, *7*, 17023.

[19] G. Sanon, R. Rup, A. Mansingh, *Thin Solid Films* **1990**, *190*, 287.

[20] R. Y. Korotkov, P. Ricou, A. J. E. Farran, *Thin Solid Films* **2006**, *502*, 79.

[21] J. Lančok, A. Santoni, M. Penza, S. Loreti, I. Menicucci, C. Minarini,

M. Jelinek, *Surf. Coat. Technol.* **2005**, *200*, 1057.

[22] J. Szuber, G. Czempik, R. Larciprete, D. Koziej, B. Adamowicz, *Thin Solid Films* **2001**, *391*, 198.

[23] S. G. Ansari, S. W. Gosavi, S. A. Gangal, R. N. Karekar, R. C. J. Aiyer, *Mater. Sci.: Mater. Electron.* **1997**, *8*, 23.

[24] J. H. Han, Y. J. Chung, B. K. Park, S. K. Kim, H. S. Kim, C. G. Kim, T. M. Chung, *Chem. Mater.* **2014**, *26*, 6088.

[25] S. H. Kim, I.-H. Baek, D. H. Kim, J. J. Pyeon, T.-M. Chung, S.-H. Baek, J.-S. Kim, J. H. Han, S. K. Kim, *J. Mater. Chem. C* **2017**, *5*, 3139.

2. Literature

2.1. The overview of p-type oxide semiconductors

Figure 2.1 shows the schematic diagrams of a conventional architecture with bottom logic circuit only and a three-dimensional stacked architecture using CMOS logic circuits placed at each memory layer [1]. Since external circuit needed for connecting with stacked memory layer for conventional architecture, where the logic devices are on Si wafer, peripheral circuit area is increased. As a result, density efficiency decreases, and fabrication process becomes complex. In addition, circuit interference and RC delay are serious problems for device operations. Therefore, the logic device must be stacked together with memory device for integration efficiency, process simplicity, and circuit configuration to systematically operate the characteristics of the two connected devices.

This further emphasizes the need for process development of oxide semiconductors with high carrier mobility, low process temperature, and device uniformity characteristics. However, the technological development of logic devices consisting of oxide semiconductor-based transistors has reached its limit. This is because p-type oxide semiconductor, an essential component of CMOS logic devices, has lower electrical properties than n-type ones.

The reason for this is the inherent band characteristics of oxide semiconductors. As shown in **Figure 2.2**, the VBM is composed of localized oxygen *2p* orbitals, so the hole mobility is low. In addition, the VBM is located

at a deep energy level, and there are high concentrations of deep states right above it (**Figure 2.3**) [2]. It makes p-type doping and the inversion operations difficult. Therefore, increasing the energy level of VBM or dispersing it through hybridization with metal orbital is a key factor for obtaining a high-performance p-type oxide semiconductor. To solve this problem, it is necessary to develop a new p-type oxide channel material having high hole mobility.

Recently, a high-speed computational screening method based on the first principle calculation has been actively conducted to find a new p-type oxide semiconductor (**Figure 2.4**). According to K. Yim *et al.* [3] and Y. Youn *et al.* [4], it is reported that the use of a hydrogen selector based on the formation energy of hydrogen interstitial defects can provide high accuracy and fast calculation speed in predicting hole concentration. According to the results, the proposed p-type oxide candidates are largely classified into three groups. The Cu bearing oxide, Pt-group bearing oxide, and multi-anion compound were proposed as candidate groups. In the case of Cu or Pt-based oxides, the hybridization of the *d*-orbital of the metal and the *2p* orbital of oxygen constitutes the valence band and can exhibit p-type characteristics (**Figure 2.5**) [5]. However, the effective mass of hole is large, and it is difficult to expect excellent electrical characteristics. In the case of multi-anion compounds, the chalcogen anion raises the energy level of the valence band and has a low hole effective mass. Nevertheless, there is a limitation that it is difficult to produce a raw material possessing excellent chemical stability and reactivity. In

particular, in the case of such a multi-component material, it is difficult to obtain the stable composition ratio and uniformity of the thin film. In addition, the problem of selecting the reactant gas for production of the material and process difficulties such as particle contamination in the chamber limits the actual application of the material. Meanwhile, SnO, which does not belong to the three representative groups, is the only binary material among the candidate groups. It is reported that it has a low hole effective mass because *s* orbital of tin is hybridized with the *2p* orbital of oxygen. For this reason, SnO is attracting huge attention as the most promising material among p-type oxides because of its electrical properties and processability.

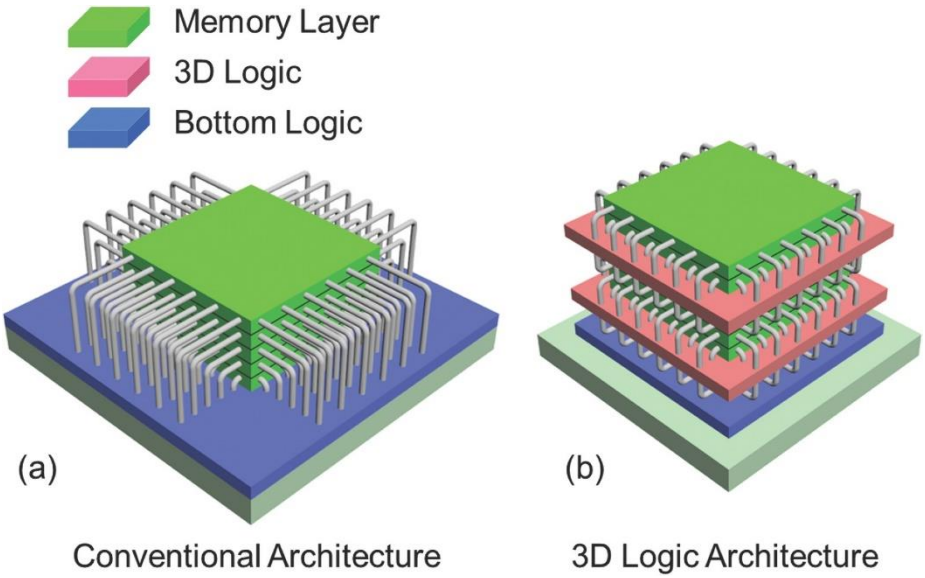
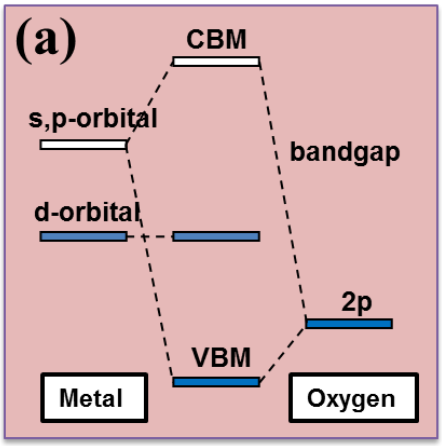


Figure 2.1. Schematic diagrams of (a) a conventional and (b) a three-dimensional stacked architecture between logic circuits and memory layers.



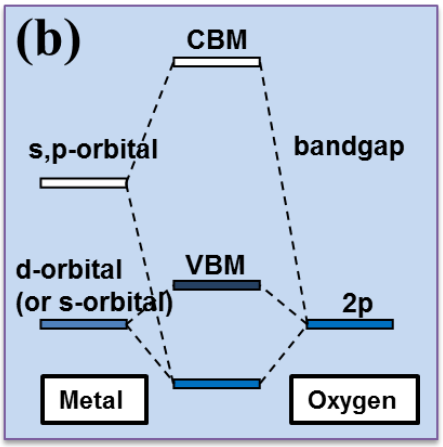


Figure 2.2. Schematic energy diagrams of (a) n-type and (b) p-type oxide semiconductors.

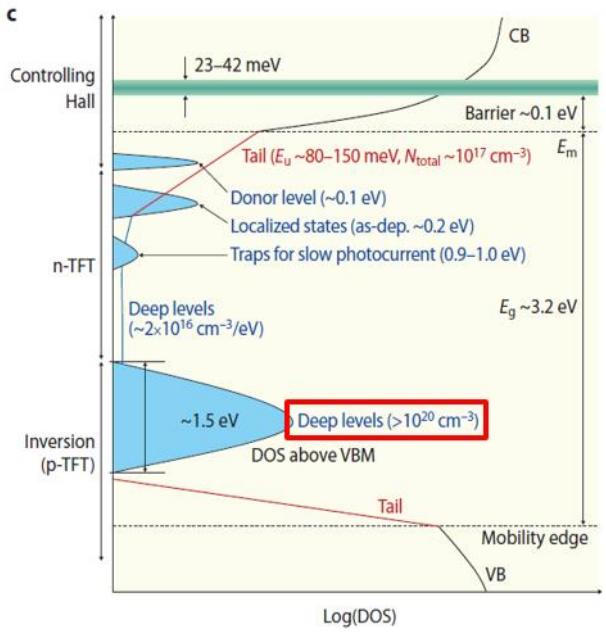


Figure 2.3. Schematic diagram of sub-gap density of states for oxide semiconductors.

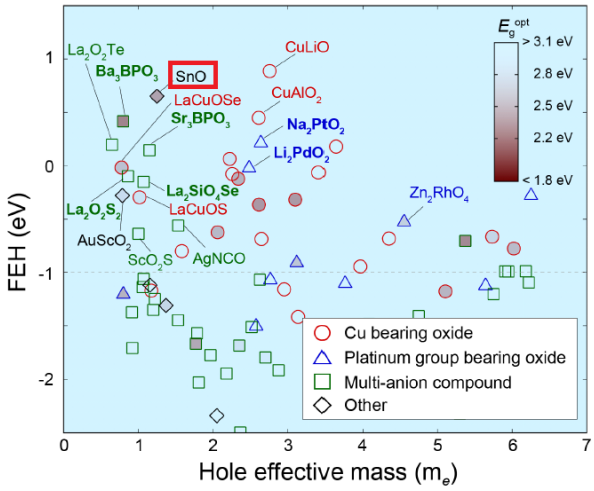


Figure 2.4. Results of high-speed computational screening method of two- and three-component substances using a hydrogen selector. FEH> –1 eV region corresponds to the p-type oxide candidate group that guarantees transparency.

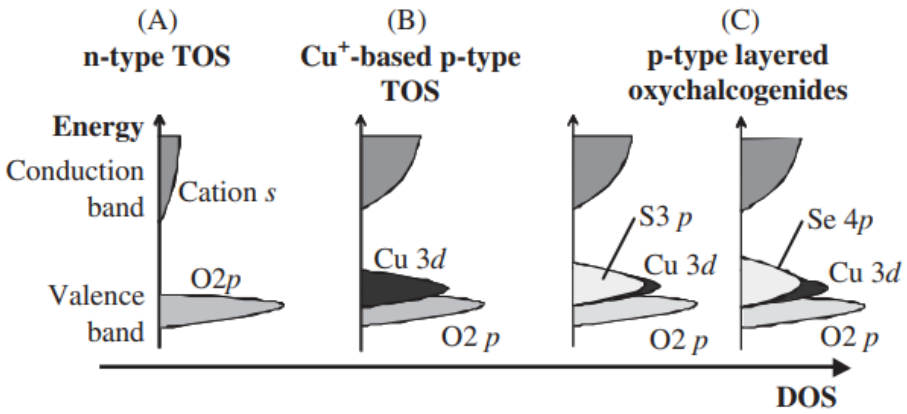


Figure 2.5. Simplified band structures of oxide semiconductors. (a) Typical n-type oxide semiconductor, (b) Cu^{+}-based p-type oxide semiconductor, (c) Oxychalcogenide-based p-type oxide semiconductor.

2.2. The p-type SnO

As shown in **Figure 2.6,** SnO is a material in which four oxygens and one Sn are arranged in a pyramid shape to form a layered structure [6]. It has a large optical band gap of about 2.7–3.0 eV and an electronic band gap of about 0.7 eV.

Based on the first principle calculation reported by Togo *et al*. [6], the origin for obtaining p-type conductivity of SnO are as follows. As mention above, the Sn *5s* orbital near VBM can reduce the localization by O *2p* orbital. This allows the SnO material to have high hole mobility (**Figure 2.7**). In addition to this, the film should be in an oxygen-rich condition where intrinsic defects such as V_{Sn} (Sn vacancy) and O_i (O interstitial) are easily formed. When these defects are completely ionized, they can act as acceptor-like defects and contribute to the p-type conductivity. However, since O_i is hardly ionized, V_{Sn} becomes a major defect that acts as a source of hole carriers (**Figure 2.8**). If the film is Sn-rich condition, intrinsic defects such as Sn_i (Sn interstitial) and V_O (O vacancy) are easily formed, contributing to n-type conductivity.

The most important point to consider obtaining p-type SnO is phase control. This is because the most common oxides of Sn at atmospheric pressure and room temperature have two forms: SnO and SnO_2 [7]. However, the problem comes from the fact that each material has p-type and n-type conductivity, respectively. Since p-type SnO is known to be thermodynamically unstable under ambient conditions, it can be easily converted into stable n-type SnO_2

depending on factors such as temperature, gas atmosphere, and pressure [8–10]. As shown in **Figure 2.9**, the thermal stability of SnO materials is only achieved in the temperature range up to 270 °C [7]. Moreover, it has been found that the deposited films often show multi-phases containing metallic Sn, SnO_2, or Sn_3O_4 rather than pure SnO [11]. As a result, the p-type conductivity of SnO can only be obtained by carefully controlling deposition or heat treatment conditions [12].

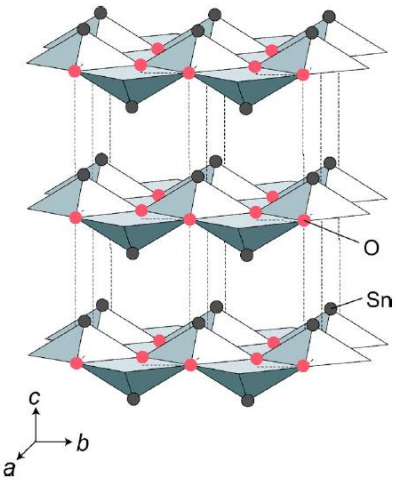


Figure 2.6. The crystal structure of SnO material.

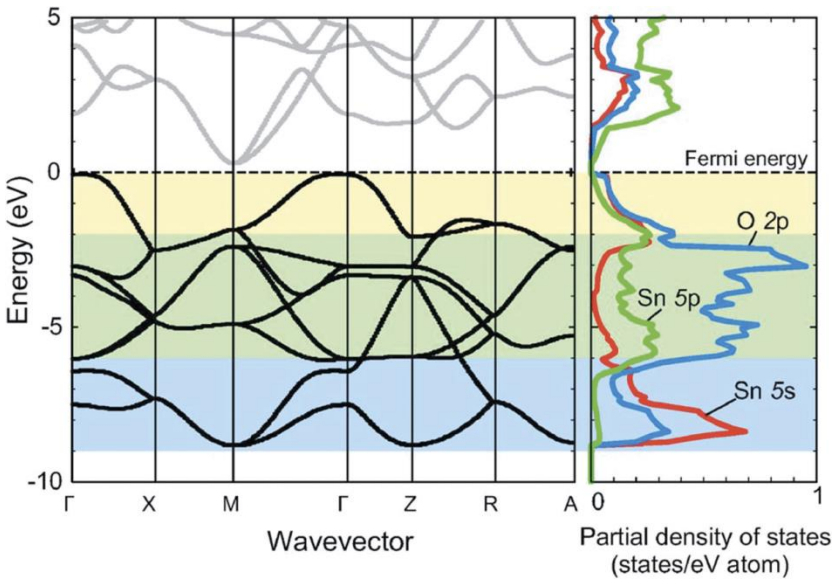


Figure 2.7. Band structure (left) and density of states (right) of the unit cell of the SnO perfect crystal.

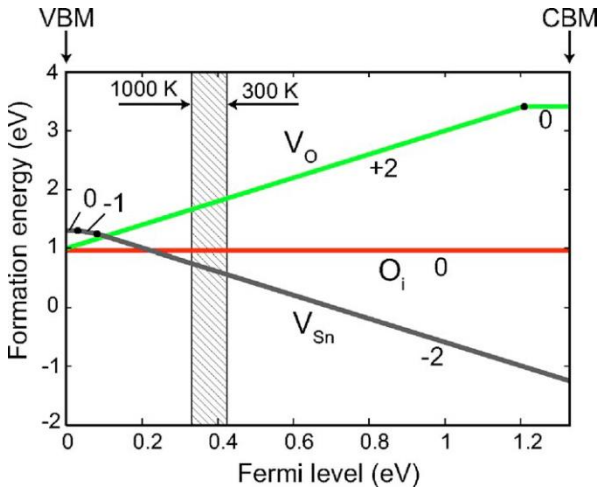


Figure 2.8. Formation energies as a function of the Fermi level when SnO is in O-rich condition.

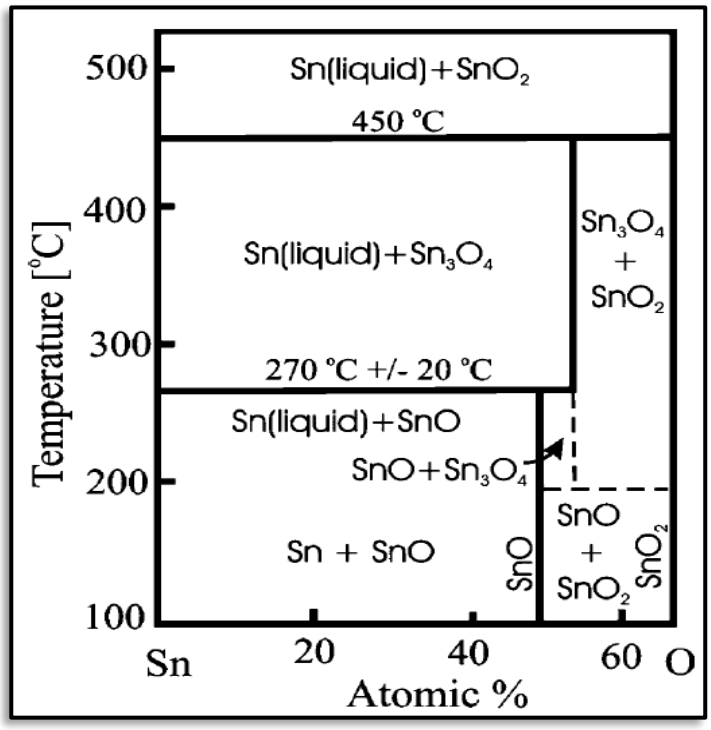


Figure 2.9. Phase diagram as function of temperature and atomic ratio between Sn and O.

2.3. The p-type SnO thin films grown by ALD and its application to TFTs

Despite such advantages, due to the thermodynamic metastable property of the SnO material, it is easily oxidized to SnO_2 with a lower energy level of n-type. Therefore, the process window for obtaining SnO is very narrow, and it is sensitive to the process conditions as shown in **Figure 2.10** [12]. In order to obtain a p-type thin film with excellent electrical properties, it is important to stably obtain a single SnO phase.

In this respect, ALD is the most appropriate method for obtaining meta-stable SnO. The ALD method does not have the problem of damage caused by high-energy ions, unlike the common process technology of sputtering method. Therefore, it is more suitable for growing high-quality oxide semiconductor channel materials. Moreover, unlike CVD, ALD is a method in which the reactants are separated and injected sequentially (**Figure 2.11**) [13]. However, research on ALD p-type oxide semiconductors is still at an early stage compared to its importance.

Table 2.1 shows a summary of previous studies that reported electrical properties among tin oxide materials deposited by ALD method [14–26]. Many Sn precursors and oxygen source were used, but almost all of them were SnO_2 film with n-type characteristics. Among the studies on ALD SnO_x thin films, only one research was reported as a p-type characteristic until 2017 (**Figure 2.12**) [20]. In addition, it was confirmed that even if the same Sn precursor

($Sn(dmamp)_2$) was used, the electrical type changed according to the degree of oxidation of the oxygen source [18–20]. Therefore, a selection of an oxidizing agent and process conditions is particularly important in conducting an experiment.

However, in most of the studies, SnO thin film deposition has been performed using the sputtering method. As a result, there was a limitation in that the on/off ratio was low as well as the hysteresis voltage was large due to carrier trapping at the interface (**Table 2.2**) [27–35]. It is known that the hysteresis is mainly caused by border traps. It is located slightly away from the channel interface and the energy level is deep within the dielectric band gap (**Figure 2.13**) [36]. It is caused by slowing the trapping and de-trapping of the carrier. In order to utilize SnO devices in real logic devices, this hysteresis problem must be solved, but no such analysis or improvement method has been suggested. Border traps are mainly caused by chemical interactions between the gate dielectric and the channel material. Therefore, when ALD SnO thin film is applied, it is expected that this hysteresis problem can be solved by securing not only high-quality channel film properties but also good interfacial properties.

The SnO TFT device fabricated by the ALD method is a technology with exceptional originality that has few reports on related contents. Developing the ALD process for p-type SnO and fabricating SnO TFT devices are essential for preoccupying research technology of the next-generation p-type material.

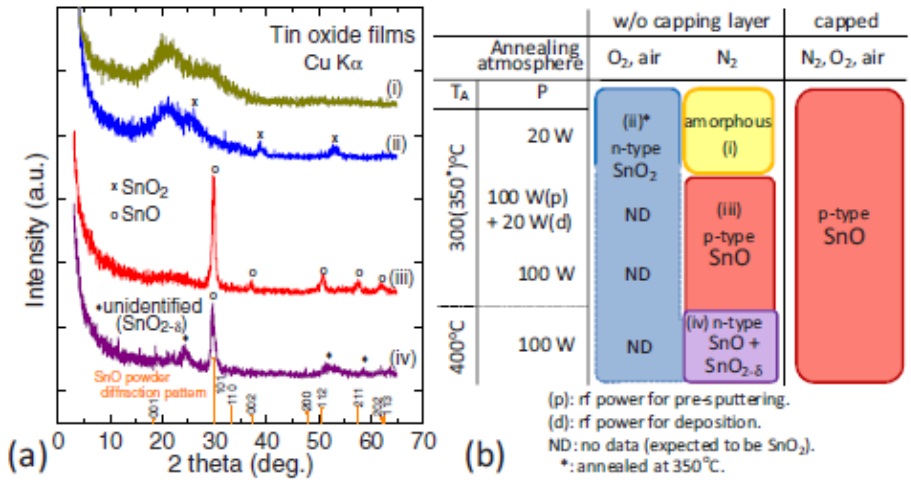


Figure 2.10. (a) XRD spectra and (b) schematic phase classification of SnO_X films with different rf sputtering power, annealing temperature, and atmosphere.

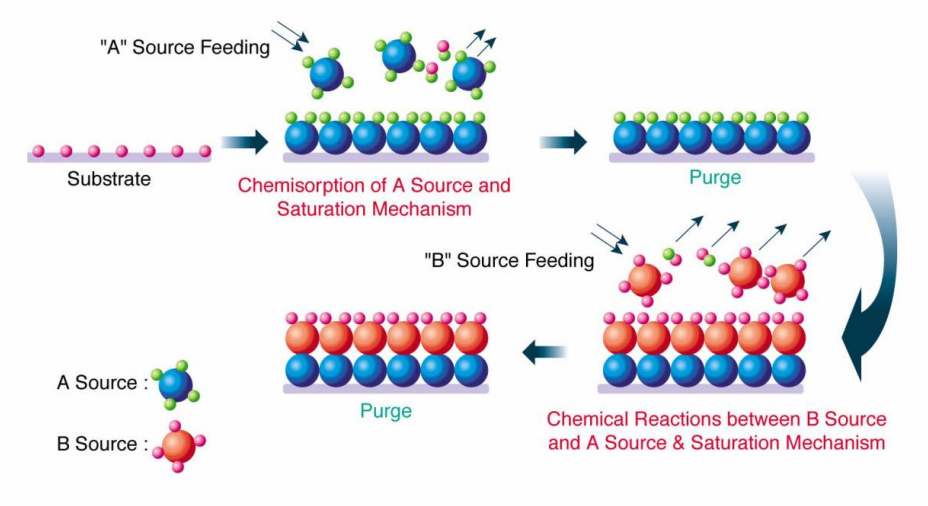


Figure 2.11. Schematic diagram of the mechanism of ALD process.

Table 2.1. Reported electrical properties of the ALD SnO_x films.

Reagent 1 (Sn-containing)	Reagent 2 (oxidizer)	Substrate	Temperature (°C)	Resistivity (Ω*cm)	Carrier type	Journal inform.
$SnCl_4$	H_2O	Soda lime glass Coming 7059 glass	500	0.06-0.20	**N-type**	H. Viirola et al., Thin Solid Films, 249, 144 (1994)
	H_2O H_2O+O_3	Soda lime glass	500	0.1-89	**N-type**	M. Utriainen et al., J. Electrochem. Soc., 146, 189 (1999)
	H_2O	Si (100)glass	300	0.01	**N-type**	H. –E. Cheng et al., Procedia Engineering, 36, 510 (2012)
			350	0.06		
			400	0.11		
			450	0.06		
TMT	NO_2	Si	400	0.21	**N-type**	V.E. Drozd et al., Appl. Surf. Sci. 82/83, 591 (1994)
			425	0.17		
			450	0.13		
TET	NO_2	Si	250	0.027		
			290	0.012		
Sn(dmamp)$_2$	PEALD	Si/SiO_2-200nm	130	0.37	**N-type**	B.K. Lee et al., Mat. Res. Bulletin, 47, 3052 (2012)
			200	0.02		
	O_3	Si/SiO_2-100nm, Si, TiN	100-230	$1.3X10^{-3}$~1	**N-type**	M.-J. Choi et al., Applied Surface Science, 320, 188 (2014)
Sn(tbba)	H_2O	Si/SiO_2-300nm	150-210	4.9-14.5	**P-type**	Jeong Hwan Han et al., Chem. Mat., 26, 6088 (2014)
	H_2O_2 (50%)	Si/SiO_2, glass, SiN membrane	100-220	0.015-0.025	**N-type**	J. Heo et al., Chem. Mater. 22, 4964 (2010)
	NO	silica glass	250	0.008		J. Heo et al., J. Chem. Mater. 22, 4599 (2012)
Sn(acac)$_2$	O_3	Si(100)/SiO_2-100nm	200	0.6	**N-type**	S.K. Selvaray et al., J. Vac. Sci. Technol. A, 32, 01A112 (2014)
TDMASn	H_2O H_2O_2	Si, glass	100	6	**N-type**	D.-w. Choi et al., Appl. Surf. Sci., 313, 585 (2014)
			200	0.00097		
	O_3	Si, SiO_2, glass	125	273	**N-type**	D. Choi et al., Surface & Coatings Technology, 259, 238 (2014)
			200	0.000563		
DBTA	O_2 PEALD	YSZ(100), YSZ(110), YSZ(111)	300	0.02	**N-type**	S. Kim et al., Journal of Crystal Growth, 348, 15 (2012)

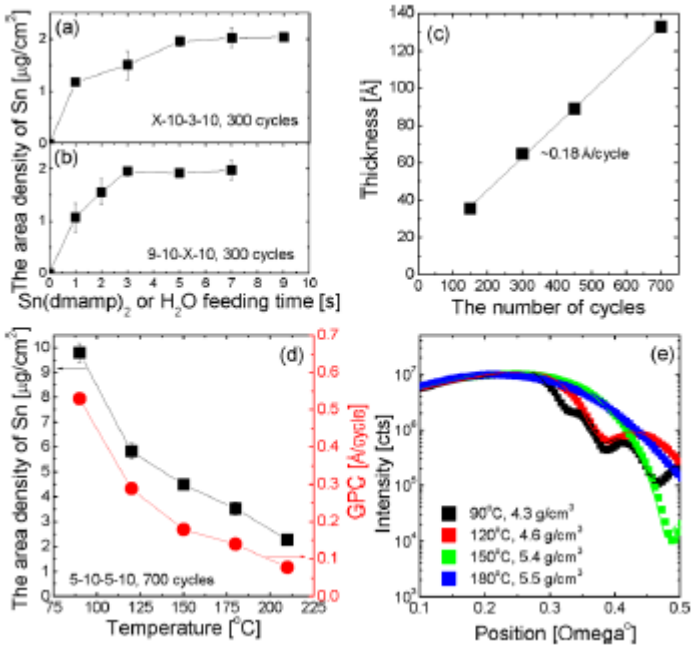


Figure 2.12. The first report on p-type SnO thin-film using ALD method.

Author	dep. method	$d_{ch.}$ [nm]	Gate dielectric	$PDA_{diel.}$	W/L [μm]	μ_{FE} [$cm^2V^{-1}s^{-1}$]	S.S [$Vdec^{-1}$]	I_{on}/I_{off}	V_{hy}, Driving Voltage (V)	year
Hosono	**PLD**	20	PLD Al_2O_3 (210 nm)	X	300/50	1.3	-	10^2		2008
J.A. Caraveo	**DC reactive Sputt.**	15	ALD HfO_2 (220 nm)	X	50/50	6.75	7.63~10	10^3	3.67 (-30V~+40V)	2013
Z. Wang	**DC reactive Sputt.**	20	ALD ATO (220 nm)	X	-	2.39	7.5	10^3	- (-30V~+30V)	2015
Azida Azmi	**DC reactive Sputt.**	-	Thermal SiO_2 (100 nm)	X	100/150	0.5	12.5	10^3	8.26 (-40V~+40V)	2017
			Spin-cast ZrO_2 (22 nm)	400℃/air/1h		2.5	0.88	10^3	1.0 (-5V~+5V)	
Z. Wang	**RF magnetron Sputt.**	25	ALD HfO_2 (140 nm)	X	250/100	2.01	2.51	10^3	3.3	2018
M. P. Hung	**Thermal evap.**	15	ALD Al_2O_3 (100 nm)	X	600/200	1.4	-	10^4	2.5 (-20V~+20V)	2018
Maarten Rockelé	**E-beam evap.**	20	ALD Al_2O_3 (100 nm)	X	1400/5	1.6	-	10^3	- (-15V~+10V)	2018
X. Guan	**DC reactive Sputt.**	15	ALD HfO_2 (140 nm)	X	200/200	3.55	-	10^3	- (-20V~+20V)	2019
M.-H. Wu	**DC reactive Sputt.**	20	ALD HfO_2 (20 nm)	X	1/0.2	1	0.32	10^5	0.3 (-2V~+3V)	2019

Table 2.2 Recent research on the p-type SnO TFTs with hysteresis voltage values specified.

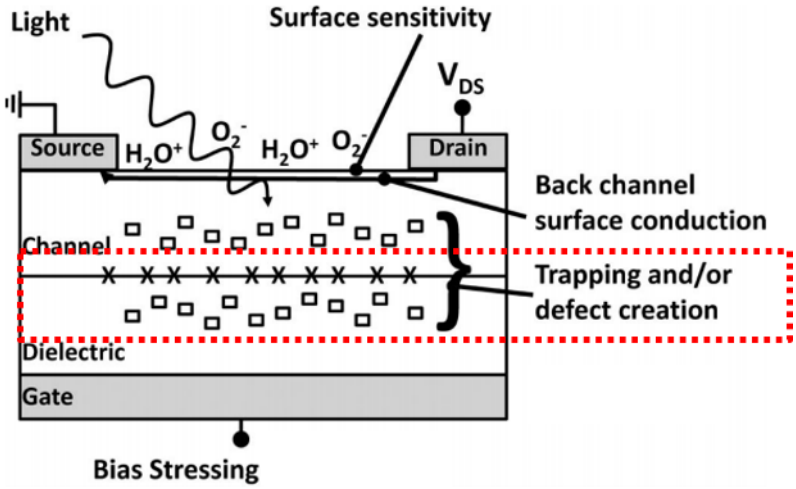


Figure 2.13. Schematic summary of the potential instabilities in the oxide TFTs.

2.4. Bibliography

[1] J. Y. Seok, S. J. Song, J. H. Yoon, K. J. Yoon, T. H. Park, D. E. Kwon, H. Lim, G. H. Kim, D. S. Jeong, C. S. Hwang, *Adv. Funct. Mater.* **2014**, *24*, 5316.

[2] T. Kamiya, K. Nomura, H. Hosono, *J. Display Technol.* **2009**, *5*, 468.

[3] K. Yim, Y. Youn, M. Lee, D. Yoo, J. Lee, S. H. Cho, S. Han, *npj Comput. Mater.* **2018**, 4, 17.

[4] Y. Youn, "Computational identification of p-type transparent Semiconductors", Doctoral dissertation, Seoul National University, **2018**.

[5] T. Kamiya, H. Hosono, *Int. J. Appl. Ceram. Technol.* **2005**, *2*, 285.

[6] A. Togo, F. Oba, I. Tanaka, K. Tatsumi, *Phys. Rev. B* **2006**, *74*, 195128.

[7] M. Batzill, U. Diebold, *Prog. Surf. Sci.* **2005**, *79*, 47.

[8] H. Hosono, Y. Ogo, H. Yanagi, and T. Kamiya, *Electrochem. Solid-State Lett.* **2011**, *14*, H13.

[9] H. Giefers, F. Porsch, G. Wortmann, *Solid State Ion.* **2005**, *176*, 199.

[10] W. H. Doh, W. Jeong, H. Lee, J. Park, J. Y. Park, *Nanotechnology* **2016**, *27*, 335603.

[11] J. Zhang, X. Kong, J. Yang, Y. Li, J. Wilson, J. Liu, Q. Xin, Q. Wang, A. Song, *Appl. Phys. Lett.* **2016**, *108*, 263503.

[12] H. Yabuta, N. Kaji, R. Hayashi, H. Kumomi, K. Nomura, T. Kamiya, M. Hirano, H. Hosono, *Appl. Phys. Lett.* **2010**, *97*, 072111.

[13] C. J. Hwang, *Physics and High Technology* **2012**, *21*, 37.

[14] H. Viirola, L. Niinistö, *Thin Solid Films* **1994**, *249*, 144.

[15] M. Utriainen, K. Kovács, J. M. Campbell, L. Niinistö, F. Réti, *J. Electrochem. Soc.* **1999**, *146*, 189.

[16] H. –E. Cheng, D. -C. Tian, K. -C. Huang, *Procedia Eng.* **2012**, *36*, 510.

[17] V. E. Drozd, V. B. Aleskovski, *Appl. Surf. Sci.* **1994**, *82/83*, 591.

[18] B. K. Lee, E. Jung, S. H. Kim, D. C. Moon, S. S. Lee, B. K. Park, J. H. Hwang, T. -M. Chung, C. G. Kim, K. -S. An, *Mat. Res. Bulletin* **2012**, *47*, 3052.

[19] M. -J. Choi, C. J. Cho, K. -C, Kim, J. J. Pyeon, H. -H. Park, H. -S. Kim, J. H. Han, C. G. Kim, T. -M. Chung, T. J. Park, B. K, D. S. Jeong, S. -H, Baek, C. -Y. Kang, J. -S. Kim, S. K. Kim, *Appl. Surf. Sci.* **2014**, *320*, 188.

[20] J. H. Han, Y. J. Chung, B. K. Park, S. K. Kim, H. S. Kim, C. G. Kim, T. M. Chung, *Chem. Mater.* **2014**, *26*, 6088.

[21] J. Heo, A. S. Hock, R. G. Gordon, *Chem. Mater.* **2010**, *22*, 4964.

[22] J. Heo, S. B. Kim, R. G. Gordon, *J. Chem. Mater.* **2012**, *22*, 4599.

[23] S.K. Selvaray, A. Feinerman, C. G. Takoudis, *J. Vac. Sci. Technol. A*, **2014**, *32*, 01A112.

[24] D. -W. Choi, W. J. Maeng, J. -S. Park, *Appl. Surf. Sci.*, **2014**, *313*, 585.

[25] D. Choi, J. -S. Park, *Surf. Coat. Technol.* **2014**, *259*, 238.

[26] S. Kim, D. -H. Kim, S. -H. Hong, *J. Cryst. Growth* **2012**, *348*, 15.

[27] Y. Ogo, H. Hiramatsu, K. Nomura, H. Yanagi, T. Kamiya, M. Hirano, H. Hosono, *Appl. Phys. Lett.*, **2008**, *93*, 032113.

[28] J. A. Caraveo-Frescas, P. K. Nayak, H. A. Al-Jawhari, D. B. Granato, U. Schwingenschlogl, H. N. Alshareef, *ACS Nano* **2013**, *7*, 5160.

[29] Z. Wang, H. A. Al-Jawhari, P. K. Nayak, J. A. Caraveo-Frescas, N. Wei, M. N. Hedhili, H. N. Alshareef, *Sci. Rep.* **2015**, *5*, 9617.

[30] A. Azmi, J. Lee, T. J. Gim, R. Choi, J. K. Jeong, *IEEE Electron Device Lett.* **2017**, *38*, 1543.

[31] Z. Wang, H. Kim, H. N. Alshareef, *Adv. Mater.* **2018**, *30*, 1706656.

[32] M. P. Hung, J. Genoe , P. Heremans, S. Steudel, *Appl. Phys. Lett.* **2018**, *112*, 263502.

[33] M. Rockelé, K. Vasseur, A. Mityashin, R. Müller, A. Chasin, M. Nag, A. Bhoolokam, J. Genoe, P. Heremans, K. Myny, *IEEE Trans. Electron devices*, **2018**, *65*, 514.

[34] X. Guan, Z. Wang, M. K. Hota, H. N. Alshareef, T. Wu, *Adv. Electron. Mater.* **2019**, *5*, 1800538.

[35] M. -H. Wu, H. -C. Lin, P. -W. Li, *IEEE Trans. Electron devices* **2019** *66*, 1766.

[36] J. F. Conley, *IEEE Trans. Device Mater. Reliab.* **2010**, *10*, 460.

3. Characterizations of p-type SnO thin films grown by atomic layer deposition (ALD) and its application to TFTs

3.1. Process development of the ALD SnO

3.1.1. Introduction

The deposition techniques of p-type SnO reported in previous studies can be divided into four types as follows. The first method is to use Sn source and O source respectively [1–3]. Deposition methods such as sol-gel, sputtering, and ALD have been reported to use this method in general and are the most commonly used methods. In order to carry out this method, the amount of O source must be precisely controlled to prevent oxidation to SnO_2, which is more thermodynamically stable. The second method is to use only SnO source [4,5]. The sputtering method is mainly used. However, due to the limitations of manufacturing high-purity SnO targets and difficulty in controlling impurities, the experimental results using this method are very few. The third method is to use SnO source and Sn source at the same time [6,7]. This is a method derived from the experimental results published by H. N. Alshareef group that metal Sn can increase the hole mobility of p-type SnO thin films [6]. In 2018, S. J. Lee *et al.* reported on the composition, microstructure, and electrical performance

of the SnO thin film deposited using this method [7]. The films with high Sn concentration showed irregular surface shape including large protrusions. Since these morphological features cause non-uniform device characteristics, precise control of metal Sn concentration is required for this method. The fourth method is to deposit a SnO_2 thin film and convert it into a SnO thin film [8]. To perform this method, it is necessary to apply a high temperature for decomposition or inject a reducing gas during the deposition or heat treatment process. However, it is difficult to obtain a pure SnO thin film through this method because not only the SnO phase, but also several phases such as metal Sn, Sn_3O_4, and remaining unreduced SnO_2 can coexist.

Among them, the notable results can be found that J. H. Han *et al*. reported that a stable and chemically reliable deposition method to achieve p-type SnO films is presented using ALD from the $Sn(dmamp)_2$ and H_2O [3]. The report shows successfully developed an ALD process for single-phase SnO films with a composition ratio close to 1:1. However, since there is only the result of Hall measurement, further characterizations are required to understand the electrical characteristics through the TFT device.

In this work, the device fabrication process was developed to fabricate the SnO-based TFTs by ALD which is superior to sputter process in terms of the fabrication of high-quality oxide semiconductor. The growth behavior of thin film was also studied according to the sequence change of ALD process. In addition, one of the critical issues for SnO TFTs, the low I_{on}/I_{off} current ratio,

was solved by adopting a very low SnO channel thickness (≤10 nm) [9–12].

3.1.2. Experimental procedure

SnO thin films were grown via ALD using $Sn(dmamp)_2$ as the Sn source, and H_2O as O source, whose oxidizing power is lower than ozone, to prevent the deposition to SnO_2. The original sequence of a single ALD cycle was as follows: 1) Sn precursor injection (7 s); 2) Sn precursor purge (10 s); 3) H_2O injection (5 s); and 4) H_2O purge (20 s). To investigate the effect of the ALD sequence on the properties of SnO thin films, the original sequence was modified as follows: 1) Sn precursor injection (1 s); 2) Sn precursor purge (5 s); 3) H_2O injection (0.5 s); and 4) H_2O purge (30 s). For efficient purging of water in both cases, a pulse method was introduced in which the vacuum was pulled out for 5 s and the purge sequence was repeated for 5 s.

The thicknesses of all the ALD films were measured using spectroscopic ellipsometry (SE, M-2000, J.A. Woollam). The crystal structures of the films were investigated using grazing-angle incident X-ray diffraction (GAXRD, X'pert Pro, PANalytical) with an incident angle of 0.5° using Cu K_α X-ray radiation. The surface morphology of the films was imaged by field-emission scanning electron microscopy (FE-SEM, S-4800, Hitachi). The film morphologies were examined by the atomic force microscopy (AFM, JSPM-5200, JEOL). The film density was evaluated by means of X-ray reflectivity (XRR, X'pert Pro, PANalytical) measurements. To investigate the chemical

binding state of the annealed films, X-ray photoelectron spectroscopy (XPS, AXIS SUPRA, Kratos) was employed. The depth profiling of the films was carried out using Auger electron spectroscopy (AES, PHI 660, Perkin-Elmer).

3.1.3. Results and discussion

Figure 3.1 shows the saturation behavior of SnO ALD after 50 cycles deposited on the Si substrate at the temperature of 150 ℃. The self-limiting growth behavior was confirmed that the thickness did not increase over a certain time. The ALD sequence (7 s – 10 s – 5 s – 20 s) for SnO deposition was obtained.

Within the temperature range considering the thermal stability of SnO (<270 ℃), the deposition temperature was set to 100, 150, and 200 ℃ in order to check the change in the growth behavior of the thin film according to the deposition temperature. The deposition rate was compared through changes in film thickness over the number of cycle repetitions (**Figure 3.2**). Stable ALD behavior with a constant deposition rate was confirmed under all the temperature conditions, and 1.1 Å/cycle of growth rate was verified at 100 and 150 ℃, while a slightly increased, 1.8 Å/cycle, growth rate was confirmed at 200 ℃. The deposition uniformity of the thin film was 96%, 93%, and 98% for each deposition temperature (in order of low deposition temperature). A high

uniformity of over 90% was confirmed under all conditions, and excellent deposition reproducibility was also obtained.

It has been studied that the crystallinity of the SnO thin film can affect the p-type transfer characteristics. With a view to determine the optimum deposition temperature for obtaining the SnO crystallinity, the phase change and grain growth behavior of the thin film according to the change of deposition temperature were monitored. **Figure 3.3** is the result of GAXRD to validate the presence of crystallization of the thin film. As the deposition temperature was increased from 100 ℃ and 150 ℃ to 200 ℃, it was confirmed that crystallization proceeded from the amorphous phase to the tetragonal phase. From the surface images using SEM and AFM shown in **Figure 3.4**, it can be seen that the grains grew significantly when the film was deposited at 200 ℃, which is the same as that of the GAXRD.

XPS spectra were analyzed to check the dominance of Sn^{2+}–O bonding which is the origin of p-type characteristics by using $Sn(dmamp)_2$ and H_2O with low oxidizing power in **Figure 3.5**. It was confirmed by the peak shifts of both Sn *3d* and O *1s* towards the lower binding energy that Sn^{2+}–O bonding was prevailed comparing to Sn^{4+}–O bonding at 200 ℃, though Sn^{4+} ion was presented at all of the conditions because of the autoxidation. On the other hand, insufficient thermal energy seemed to induce amorphous structure at 100 and 150 ℃, even with the presence of the Sn^{2+}–O bonding.

AES was utilized to check the uniformity and purity in the thickness direction of thin films by deposition temperature (**Figure 3.6**). The ratio of Sn to O increased when the deposition occurred at 200 ℃ compared to lower temperatures. This can be interpreted as an increase in the Sn/O ratio as the divalent oxidation state of Sn ions is structurally well maintained when crystallization occurs during the deposition process, unlike when the thin film is in an amorphous phase. Meanwhile, all the films show their impurities less than 3 at. %, indicating the adsorption and surface reaction of the Sn precursor based on the ALD reaction, and the desorption reaction of by-products proceeded smoothly.

Figure 3.7 is the result from XRR analysis to figure out the density of the SnO thin film. It was verified that the density of the thin film increased as the deposition temperature increased, and the tendency of the surface roughness according to the deposition temperature was also consistent with the AFM results in **Figure 3.4**. It can be deduced that the optimum deposition temperature of the ALD process for obtaining the excellent electrical properties of the SnO thin film is 200 °C through a series of analyses as mentioned earlier. In the case of SnO thin films deposited at 100 ℃ and 150 ℃, as shown in **Figure 3.4**, the grain is diminutive and has a porous structure, so it is expected that the systematic connection between nearby atoms is not formed properly, and thus it will exhibit insulating properties. On the other hand, the SnO thin film

deposited at 200 ℃ is expected to show excellent p-type characteristics when applied to the TFT channel considering the crystallinity, the distribution of grain, chemical states, and film density. Based on the growth behavior of the SnO thin film and the optimum ALD deposition temperature conditions identified through this study, the SnO ALD process was developed to optimize the properties of the thin film.

Figure 3.8 shows the control of ALD process conditions for the enhancement of the physical and electrical properties of ALD SnO thin film at 200 ℃. It demonstrates the saturation behavior of the thickness growth according to the injection time of the Sn precursor and the oxygen source under 200 ℃. 50 cycles applied for ALD deposition on the Si substrate. Unlike at 150 ℃, the saturation behavior of H_2O purge did not occur until 120 s when deposited in the original sequence at 200 ℃. This is induced by the excessive injection of H_2O, thus the decrease of water injection time from 5 s to tenfold (0.5 s) secured the new ALD sequence (1 s – 5 s – 0.5 s – 30 s) after the observation of the saturation point.

As in **Figure 3.9**, the growth rate was much higher than that from the previous report (0.08 Å/cycle) when H_2O was injected for 5 s, even though purged for 20, 30, and 60 s. When the injection time of H_2O was decreased to 0.5 s, the growth rate was 0.11 Å/cycle which is comparable to the literature [3],

and therefore the adoption of the modified ALD sequence produced the stable growth of SnO.

As can be seen in **Figure 3.10**, a significant difference in crystallinity could not be observed, but the surface roughness decreased by about 35% from 2.09 nm to 1.36 nm from the surface image in **Figure 3.11**. This is attributed to change of the adsorption efficiency of the precursors by the modified ALD sequence.

Figure 3.12 shows the XPS spectra to validate the change of chemical states of the thin film according to the sequence modification. The peak shift of Sn *3d* towards the lower binding energy was observed when applied the modified ALD sequence. The change of the ratio of Sn^{2+} to Sn^{4+} was confirmed after the deconvolution of XPS spectra that the ratio showed an increment from 0.67 to 0.77 after adopting the modified sequence. The SnO thin film with the modified ALD condition is predominantly composed of the Sn^{2+}–O bonding, which is consistent with the change in O *1s* peak. Namely, the decrease of Sn^{4+} ions inducing structural disorder in SnO contributed to the reduction of surface roughness, while lowering the deposition rate and increasing the areal density of Sn. The density value of the SnO thin film obtained through was 5.87 g/cm^3, which is about 91% of the theoretical density, confirming that it has excellent thin film density characteristics. Based on these results, it is expected that the hole concentration, which is the major carrier of the p-type semiconductor, can be increased only by the change in the injection and purge time of the oxygen

source. When the SnO thin film is applied as a channel film to a TFT device, it is expected that the on-off ratio of drain-source current (I_{on}/I_{off}) in the transfer characteristics will be improved as the on current increases.

3.1.4. Summary

Through the research, the optimum deposition temperature (200 ℃) of the SnO ALD process was secured in consideration of film qualities such as the crystallinity, density, surface roughness and chemical states of the thin film. In addition, it was confirmed that the optimization technique for the ALD process was effective in improving the properties of the SnO thin film.

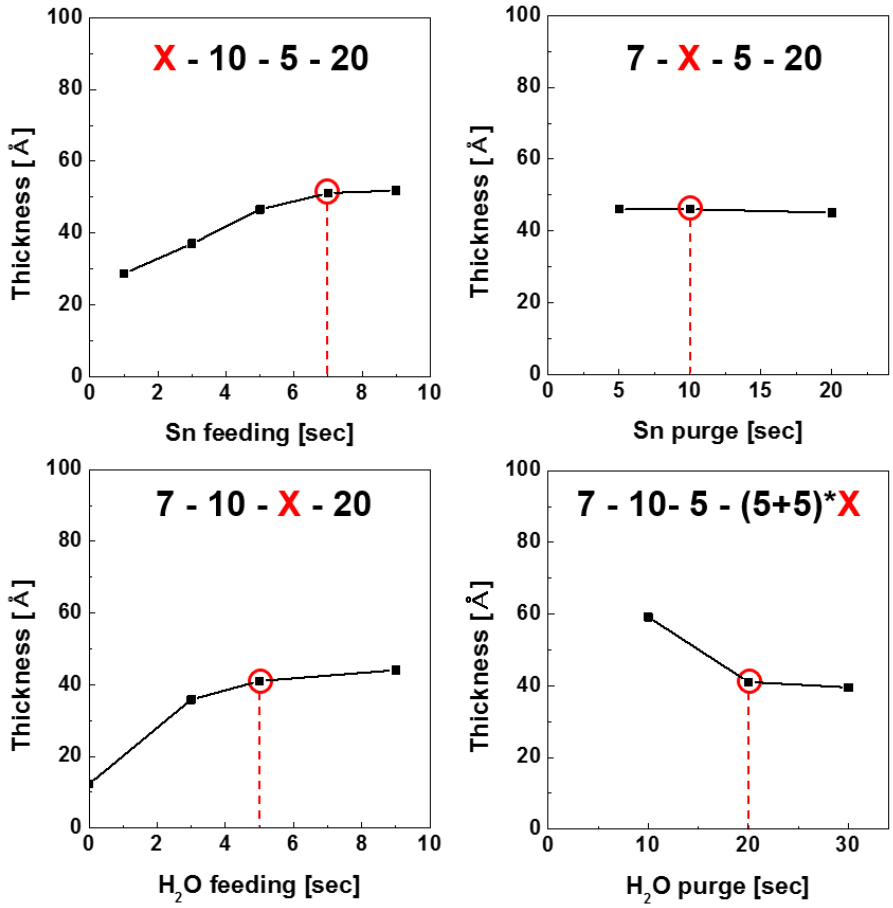


Figure 3.1. Saturation behaviors of SnO ALD.

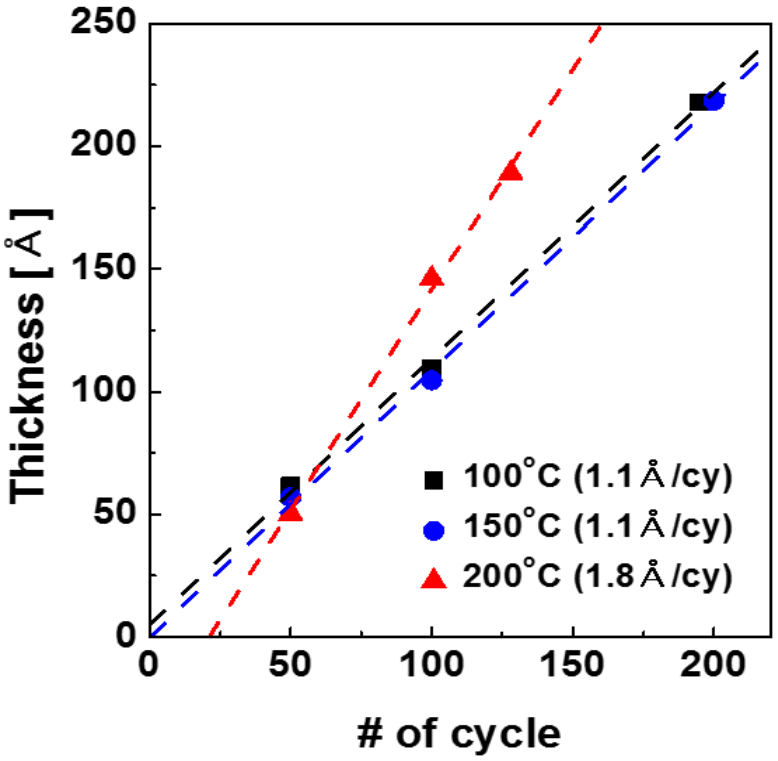


Figure 3.2. Growth rate of SnO thin film depending on the deposition temperature.

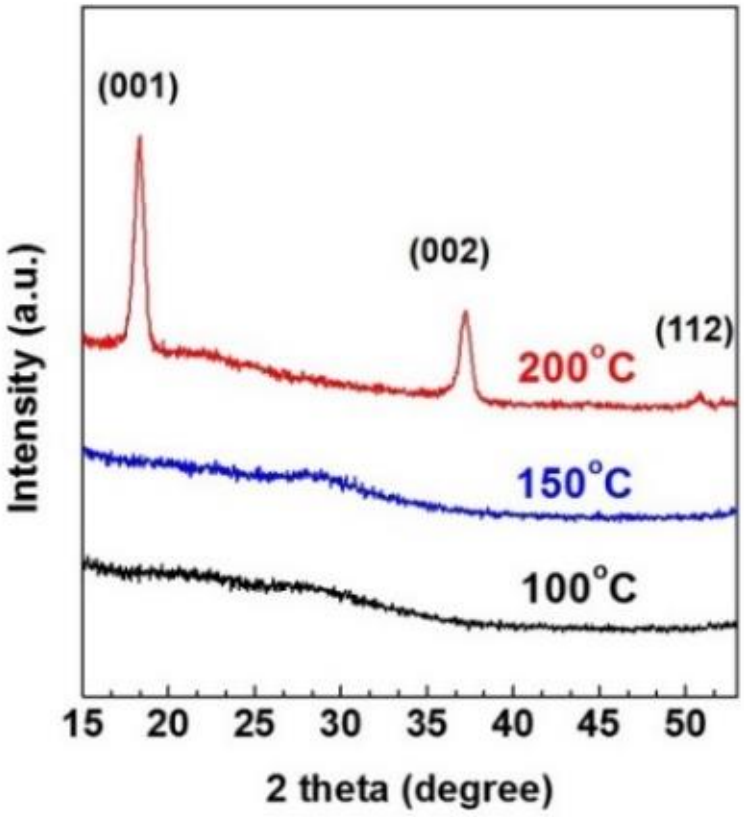


Figure 3.3. GAXRD spectra of ALD SnO thin film depending on the deposition temperature.

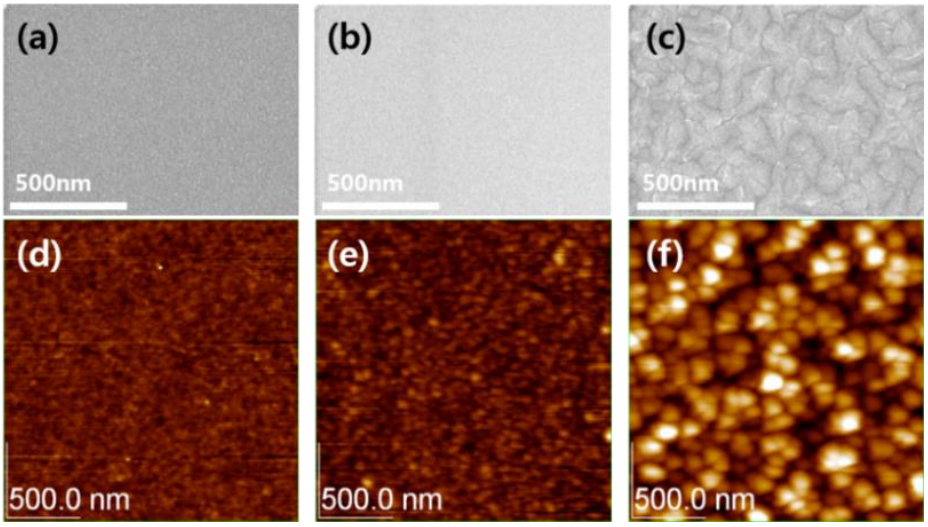


Figure 3.4. Topological images by (a–c) SEM and (d–f) AFM of ALD SnO thin film depending on the deposition temperature of (a, d) 100 ℃, (b, e) 150 ℃, and (c, f) 200 ℃.

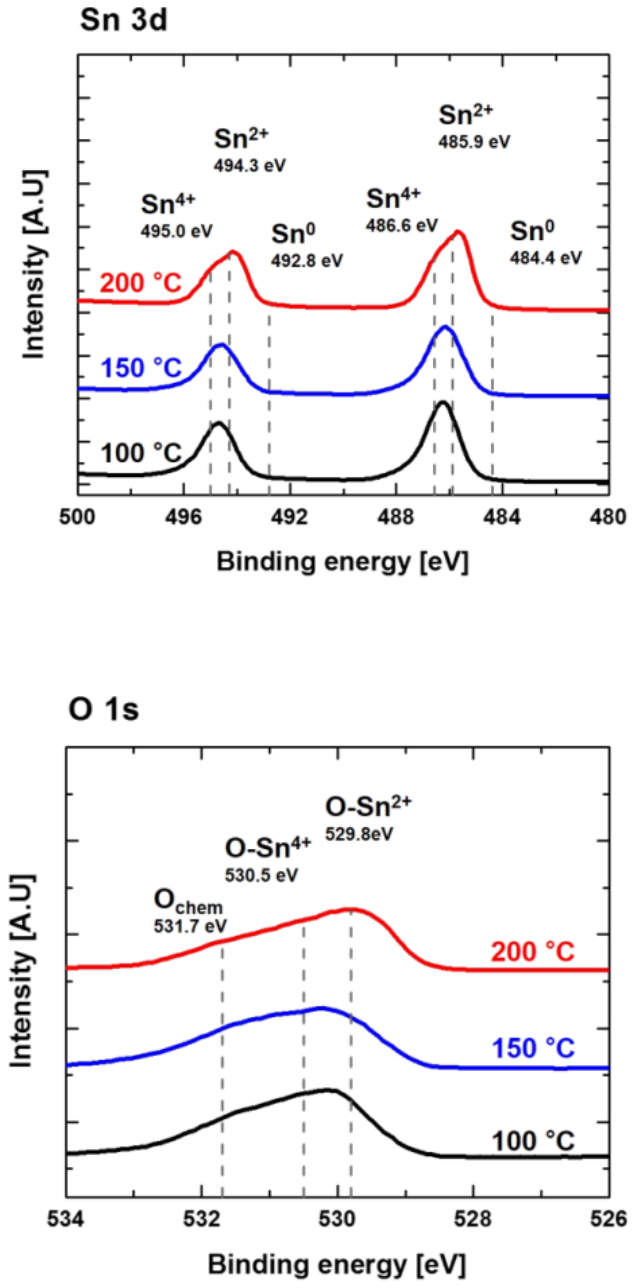


Figure 3.5. XPS spectra of (a) Sn *3d* and (b) O *1s* of ALD SnO thin film depending on the deposition temperature.

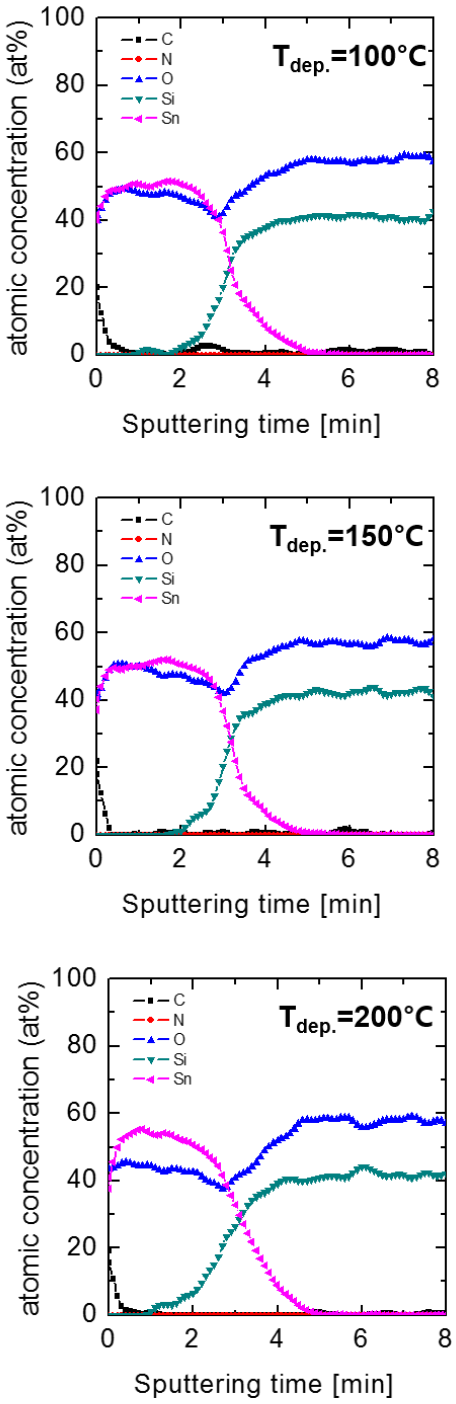


Figure 3.6. AES analysis of ALD SnO thin film depending on the deposition temperature.

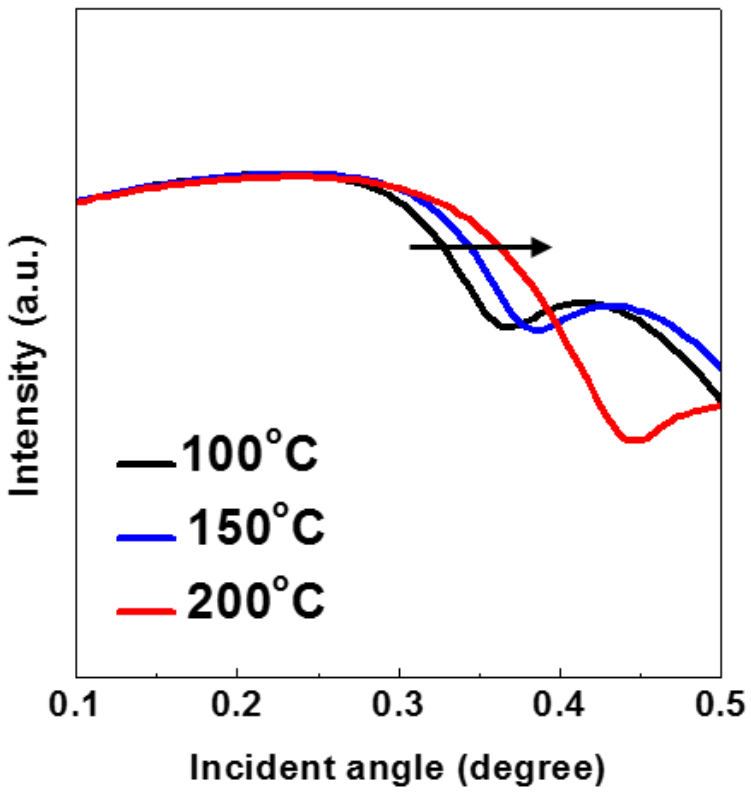


Figure 3.7. XRR measurement of ALD SnO thin film depending on the deposition temperature.

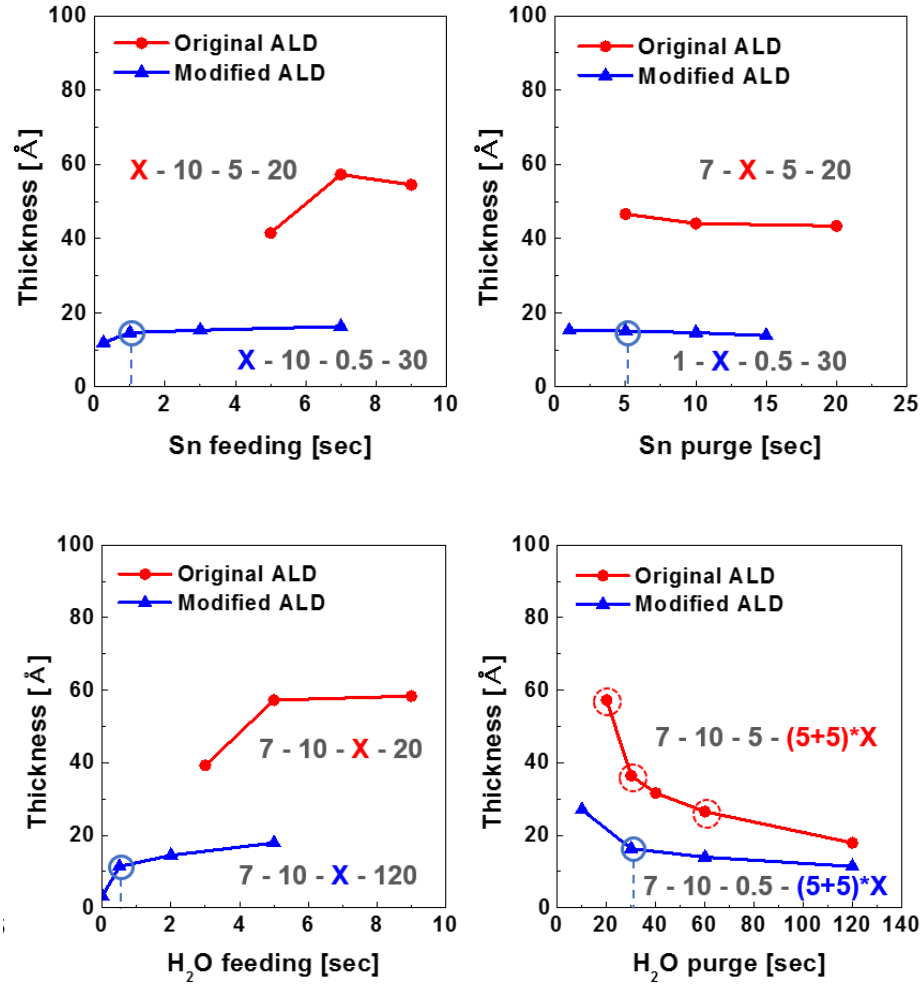


Figure 3.8. Saturation behaviors of SnO thin film deposited at 200 ℃ depending on the injection time of both Sn precursor and oxygen source.

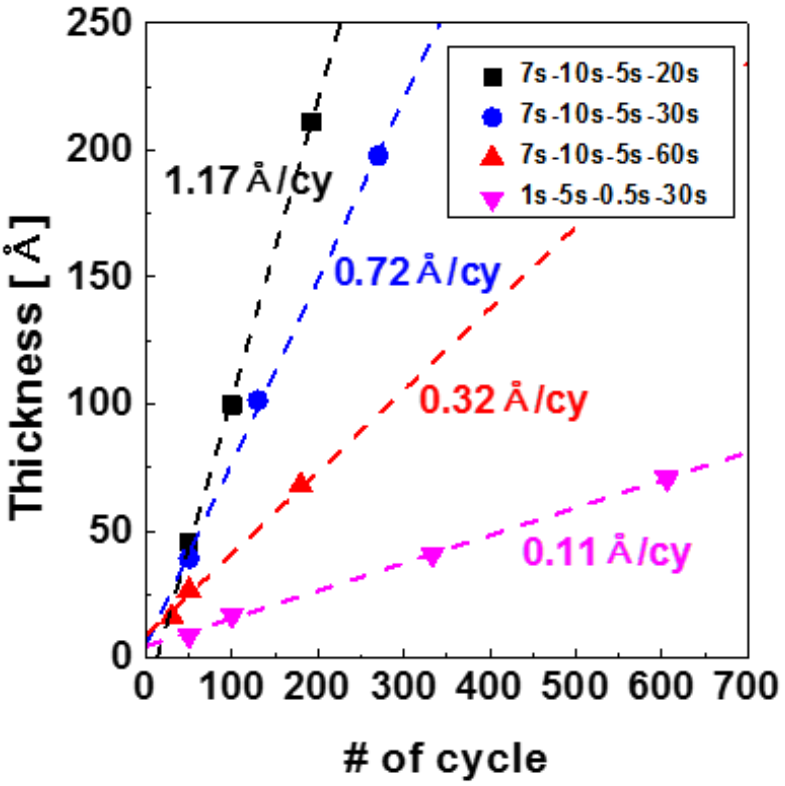


Figure 3.9. The change of growth rate SnO thin film with various ALD sequence.

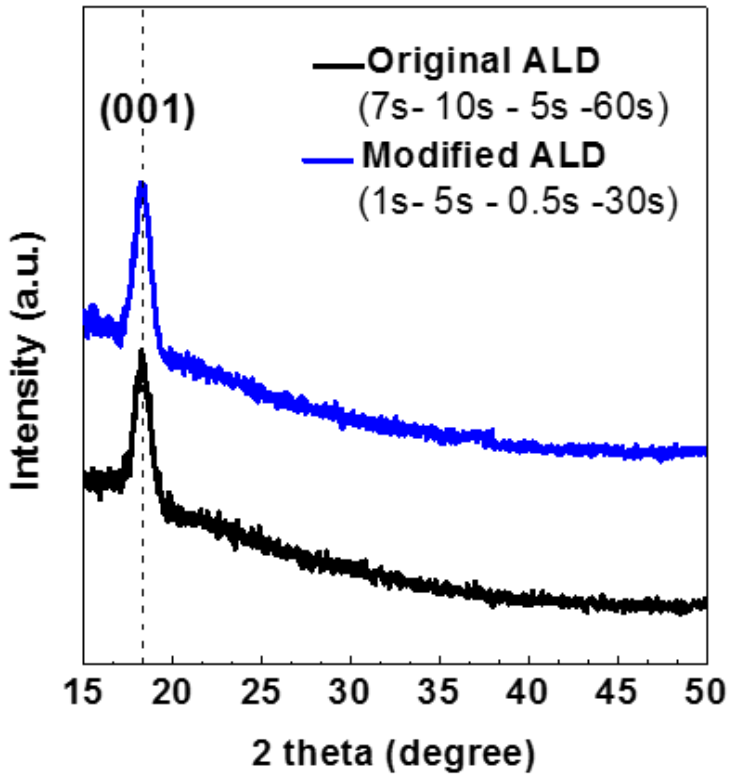


Figure 3.10. GAXRD spectra of SnO thin film with different ALD sequence.

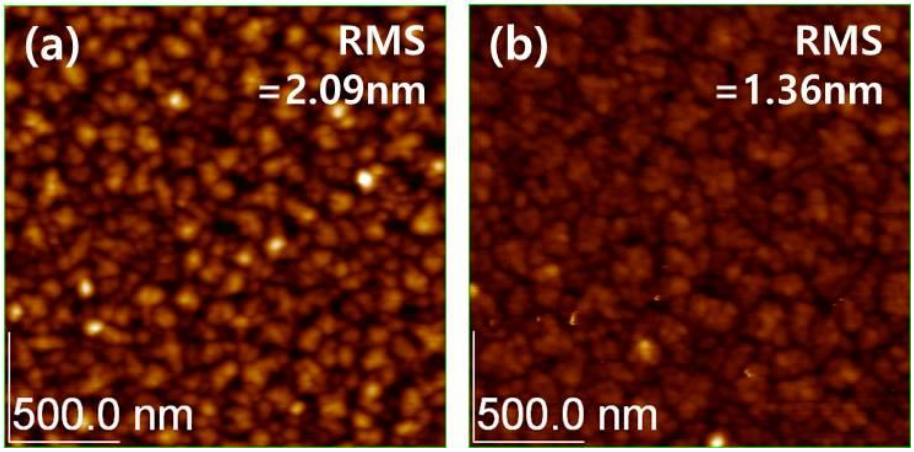


Figure 3.11. Surface images of SnO thin film with different ALD sequence. (a) the original sequence (7 s – 10 s – 5 s – 60 s) and (b) modified sequence (1 s – 5 s – 0.5 s – 30 s).

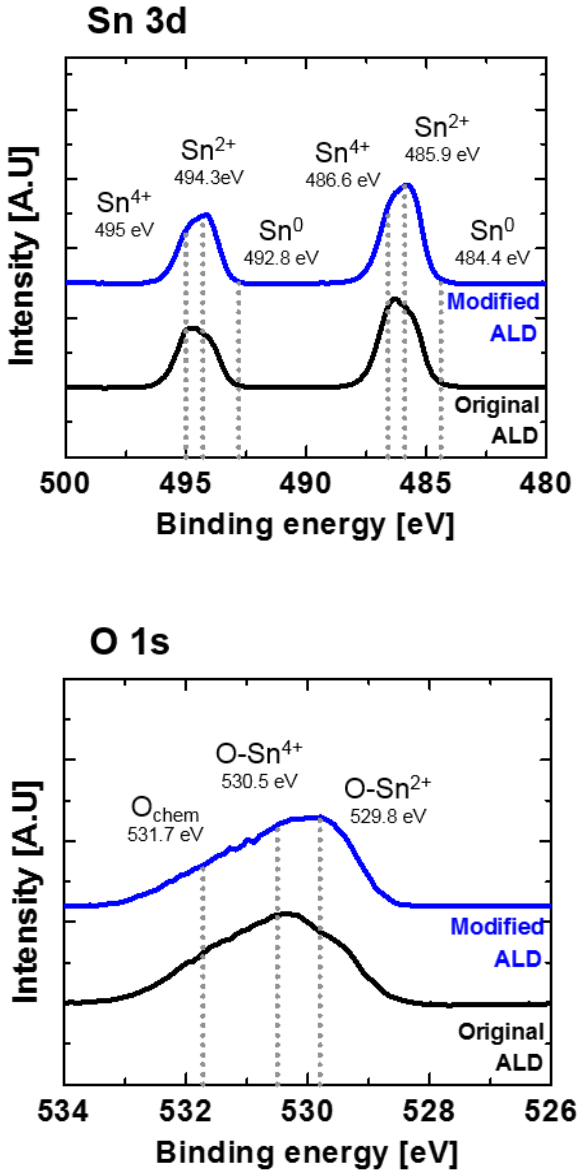


Figure 3.12. XPS spectra of SnO thin film with different ALD sequence.

3.2. ALD SnO thin film to channel layer of TFT device

3.2.1. Introduction

The relationship between the results of the characterization of the thin film obtained from the previous study and the electrical properties of the SnO thin film according to the deposition temperature was evaluated to assess the applicability of the ALD SnO thin film to the channel film of TFT device.

3.2.2. Experimental procedure

The crystal structure, depth profiling of the film, and chemical bonding state were investigated using GAXRD, AES, and XPS, which are the same measurements as described in chapter 3.1.2. To evaluate the electrical properties of the thin film, the Hall measurement equipment was used to measure the conductivity, hole concentration, and Hall mobility characteristics of the ALD SnO thin film, but it was not possible to secure the characteristics due to the measurement reliability limitation by the thin semiconductor film thickness ($\leq$20 nm). Instead, a four-point probe (FPP-5000) was utilized to confirm the resistivity of the SnO films.

Prior to the fabrication of the patterned TFT devices by photolithography, a simple evaluation for the p-type operation characteristics was proceeded using the non-patterned devices without PDA in order to eliminate the deterioration factor of ALD SnO channel during the fabrication process. A heavily doped p-

type Si substrate was used as bottom gate, and thermally oxidized SiO_2 (100 nm) and ALD SnO (20 nm) were as insulating layer and channel film, respectively. As the source and drain electrodes for the p-type semiconductor, gold (Au) film having a large work function in the range of 5.1 to 5.47 eV was deposited to a thickness of 80 nm using a sputter method.

A method of fabricating the SnO TFTs by photolithography process is as follows. The gate electrode, GI, and the channel film were made of a heavily doped p-type Si, 100 nm of thermally oxidized SiO_2, and 20 nm of ALD SnO, respectively, which is the same as the non-patterned devices. The ALD SnO channel layer was patterned through the photolithography process and the optimization of the wet etching process using the diluted hydrofluoric acid solution. The width and length of TFTs were set to 20 μm and 5 μm, respectively. For the source/drain metals, 80-nm-thick Au was deposited via sputtering and was patterned using the conventional liftoff method after patterning the channel film.

To confirm the PDA temperature range of the device to stably obtain the SnO due to its thermodynamic metastability, the relationship between the phase change in terms of temperature (oxidation state) and the change in the electrical properties of the SnO TFT device was analyzed. For this, the PDA was performed for 1 h in a vacuum (~1 mTorr) in a tube furnace after the patterning of the device was completed.

When adopting a passivation layer to a TFT device, trimethyl aluminum

(TMA) was used as a source for the metal element in the ALD process of the Al_2O_3 thin film. As the oxygen source, H_2O having a lower oxidizing power than ozone was used for a short injection time to prevent oxidation of the SnO surface (back channel region). The ALD sequence for passivation was as follows: 1) Al precursor injection (1 s); 2) Al precursor purge (10 s); 3) H_2O injection (0.5 s); and 4) H_2O purge (30 s). In the same method as the SnO deposition, a pulse method was utilized by repeating the sequence of the vacuum being pulled out for 5 s and the purge sequence for 5 s for efficient purging of water. The deposition of the ALD Al_2O_3 thin film was also carried out at 150 °C, which is lower than the deposition temperature of the ALD SnO thin film to minimize the influence on the SnO channel layer.

A Hewlett-Packard 4155 semiconductor parameter analyzer was used to measure the electrical properties of the fabricated TFTs. It was carried out at room temperature and in the dark.

3.2.3. Results and discussion

In the case of deposition temperature of 100 ℃ and 150 ℃, it was out of the measurable range due to the high resistivity. However, the conduction characteristic was observed when deposited at 200 ℃, showing the semiconductive property with a sheet resistance of 6.02 MΩ/sq. and a resistivity of 3.15 Ω·cm. As predicted in the previous study, the low temperature of

deposition (100 and 150 ℃) produced the insulating SnO thin film because of its amorphous structure, small grain size, and porous structure. On the other hand, the SnO thin film deposited at 200 ℃ exhibited semiconductive behavior due to its crystallinity (tetragonal phase), large grain distribution, high film density, and chemical state dominated by divalent SnO.

The results of the transfer characteristics of the non-patterned TFTs depending on the deposition temperature of the ALD SnO thin film were consistent with the results of the electrical characteristics evaluation of the thin film through the previous four-point probe. In the case of a device that applied SnO film deposited at 100 °C or 150 °C as a channel layer, a drain current of 10^{-11} A or less was measured and the insulator characteristics were detected. However, in case of a device that applied SnO film deposited at 200 ℃ as a channel layer, it shows an on current of 10^{-5} A in the negative gate voltage (V_{GS}) region and off current as low as 1 order in the positive V_{GS} region. It showed the possibility of switching operation for p-type TFT device.

However, this low on/off current ratio characteristic is a result of the use of the channel layer in which the patterning process has not been performed. It can be considered as the large leakage current across the entire SnO thin film due to the fringe field effect. Therefore, it is necessary to fabricate a patterned device based on a photolithography process in order to use an ALD SnO thin film as a channel layer of a TFT device.

Based on the evaluation of the SnO thin film for the channel layer according to the ALD deposition temperature, ALD SnO film deposited at 200 ℃ was used in the subsequent experiments and studies. Specifically, process technology for TFT manufacturing was developed, and electrical characteristics of the pattern TFTs were analyzed.

Figure 3.14 is a schematic diagram of the fabrication process of TFT device by patterning ALD SnO channel film and Au electrode based on photolithography. **Figure 3.15** indicates the drain current (filled symbol) and the gate leakage current (empty symbol), respectively. The drain-source voltage (V_{DS}) was fixed at -0.1 V. For SnO TFT devices fabricated based on the photolithography process, improved switching behavior of p-type characteristics and low gate leakage current characteristics ($\leq 10^{11}$ A) were observed. This showed a marked difference when compared with the results of the simple evaluation device (e.g., non-patterned device) mentioned above. The on/off current ratio increased with increasing PDA temperature until 300 °C, but when the temperature was increased to 350 °C or higher, a significant degradation in electrical characteristics was observed.

To understand the transfer characteristics of the TFT device that changes depending on the PDA temperature, the ALD SnO thin film was analyzed according to the PDA temperature. **Figure 3.16** shows the result of GAXRD, and the intensity of the (001) and (002) crystal peaks corresponding to the tetragonal phase of SnO decreased as the PDA temperature increased. This is

consistent with the previous report that some of the Sn^{2+}-O bonds inside the thin film seem to be oxidized due to the oxygen diffused into the thin film during the PDA process. This resulted in the growth of SnO_2 nanocrystals and a structural disorder of the SnO film. Similar results were observed in elemental analysis in the thickness direction of the thin film through AES measurement (**Figure 3.17**). Unlike the thin film before the PDA process, it was confirmed that in the case of the thin film subjected to the PDA at 300 °C, the ratio of O to Sn increases from the surface and decreases toward the inside. Through this, it is possible to understand the change in the oxidation state of the SnO thin film due to the PDA treatment. When the XPS analysis was performed on the SnO thin film (**Figure 3.18**), it was observed that the Sn *3d* peak and O *1s* peak shifted toward higher binding energy in the case of the SnO film after PDA at 300 ℃ compared to that of SnO film before PDA.

Based on the GAXRD, AES, and XPS results, it is estimated that the n-type SnO_2 nanocrystals, which were induced by the PDA process, generated electrons. They reduce the concentration of holes, the majority carrier of the p-type SnO film.

Therefore, it is interpreted that the controllability of the V_{GS} is improved, and the I_{on}/I_{off} increases due to the influence of the controlled carrier concentration. Nevertheless, the loss of on current occurred to a certain extent as the hole concentration decreases with the increase of the PDA temperature (**Figure 3.15**). When PDA was applied at higher than 300 ℃, it was confirmed that the SnO

thin film no longer functions as a p-type semiconductor. This result may be due to the significant reduction in hole concentration and structural disturbance of carrier conduction by excessively generated SnO_2.

Through this study, it was identified that control of the hole concentration of the SnO channel layer is an important factor for obtaining excellent performance of the p-type SnO devices. It was also clearly confirmed that this is possible when accompanied by appropriate techniques for TFT fabrication.

Based on this, further research on improving TFT performance was carried out on the following factors: (1) modification of the ALD sequence, (2) optimization of the device structure.

In order to confirm the change in TFT performances according to ALD SnO optimization, a method of reducing the injection time of H_2O, which was confirmed in the previous study, was introduced. The electrical characteristics of the devices were evaluated by applying the original sequence (7 s – 10 s – 5 s – 60 s) and the modified sequence (1 s – 5 s – 0.5 s – 30 s) to the deposition of SnO channel layers. The thickness of thermal SiO_2 was reduced from 100 nm to 35 nm thick to improve the controllability of the V_{GS}, and the thickness of the ALD SnO film was reduced from 20 nm to 7 nm. A PDA treatment was not performed to observe only the effect of change in the physical properties of the SnO thin film through the modification of the ALD conditions and the change in the structure of the TFT device.

Figure 3.19 shows the results of the transfer and output characteristics of the

TFT device according to the ALD sequence modification of the SnO thin film. The V_{DS} was fixed at -1 V.

Comparing with the result in **Figure 3.15** was confirmed that the I_{on}/I_{off} can be improved using the original ALD sequence only by reducing the thickness of the SnO channel layer. By introducing the modified ALD sequence, the increment of not only the on current but also the I_{on}/I_{off} by 2 order was detected (I_{on}/I_{off} ~10^5). In addition, it is verified that the modification of ALD sequence greatly improved the induced drain current and saturation behavior as well (**Figure 3.19**b, c). As previously studied on ALD sequence optimization, these are results reflecting the improvement in the transport properties of hole carriers due to the reduction of the surface roughness and the increase of the Sn^{2+} component ratio.

Following the understanding of the relationship between the optimization of ALD sequence and the TFT performance, Al_2O_3 passivation layer was introduced on the top of the SnO TFT. The change in electrical characteristics due to the additional structure optimization of the TFT device was analyzed.

An Al_2O_3 thin film showing ALD self-limiting behavior was used as the passivation layer (**Figure 3.20**a), and a schematic diagram of a TFT device adopting the corresponding layer of 15 nm thickness is shown (**Figure 3.20**b).

Figure 20c validates the transfer characteristics of the SnO TFT depending on the existence of the ALD Al_2O_3 passivation layer. The application of passivation layer reduced the off current and improved the I_{on}/I_{off} to 5×10^5,

especially the subthreshold swing (SS, 0.65 V/dec.) as well as the field-effect mobility (μ_{FE}, 2.17 $cm^2/V \cdot s$). This can be accompanied by 1) prevention of oxidation or air molecule adsorption to the channel film, 2) the decrease of the defect concentration on the back-surface by the reduction of dangling bonds during the deposition of Al_2O_3 layer, 3) interaction between Al_2O_3 and SnO thin film, enhancing the hole conduction characteristics on the back-surface of the SnO channel film. The introduction of the passivation film is expected to contribute to achieving a higher I_{on}/I_{off}, μ_{FE}, and low SS by preventing additional oxidation of the SnO channel layer during the PDA process.

3.2.4. Summary

Through this study, it was confirmed that the improvement of film quality of the channel layer by applying the temperature optimized for ALD SnO deposition is the most decisive factor in determining the performance of the ALD SnO TFT device. In addition, it was demonstrated that the development of the manufacturing process and device structure is also effective in obtaining a p-type TFT having an excellent I_{on}/I_{off} value.

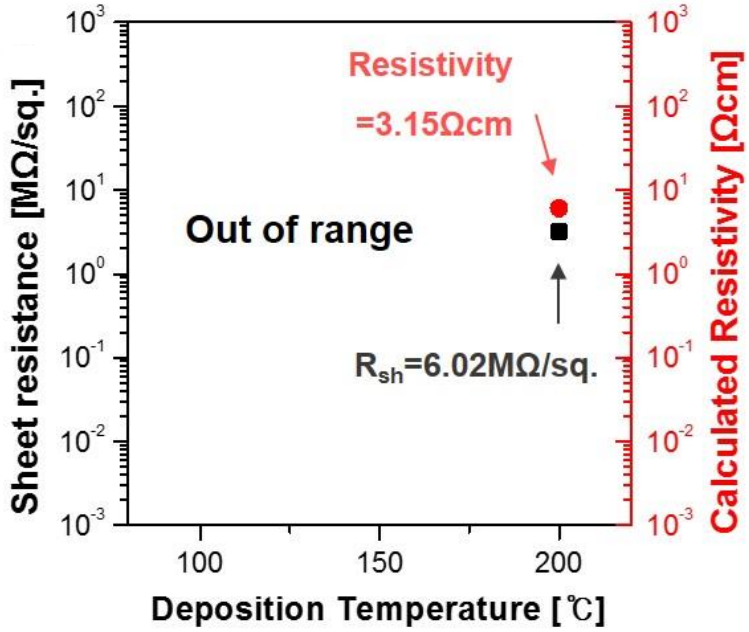


Figure 3.13. Sheet resistance and the resistivity of ALD SnO thin film measured by four-point probe.

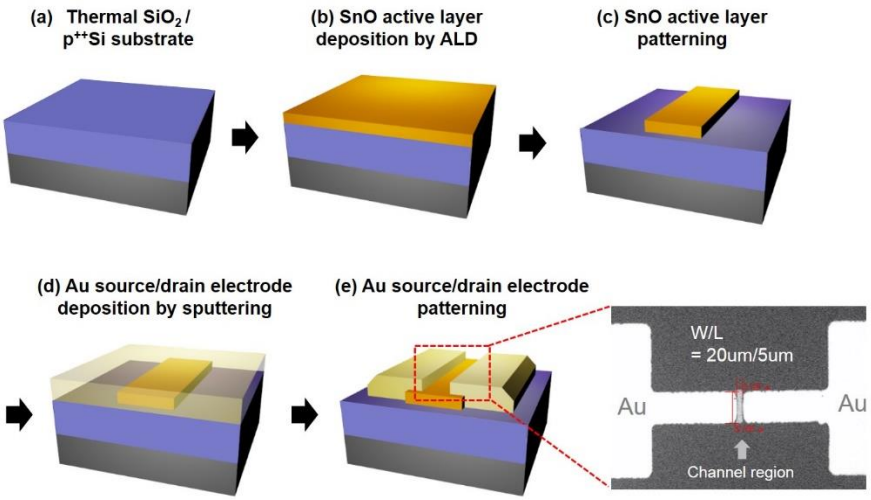


Figure 3.14. Schematic diagram of the fabrication of ALD SnO TFT and optical microscope image of the top view of the channel region of fabricated SnO TFT device.

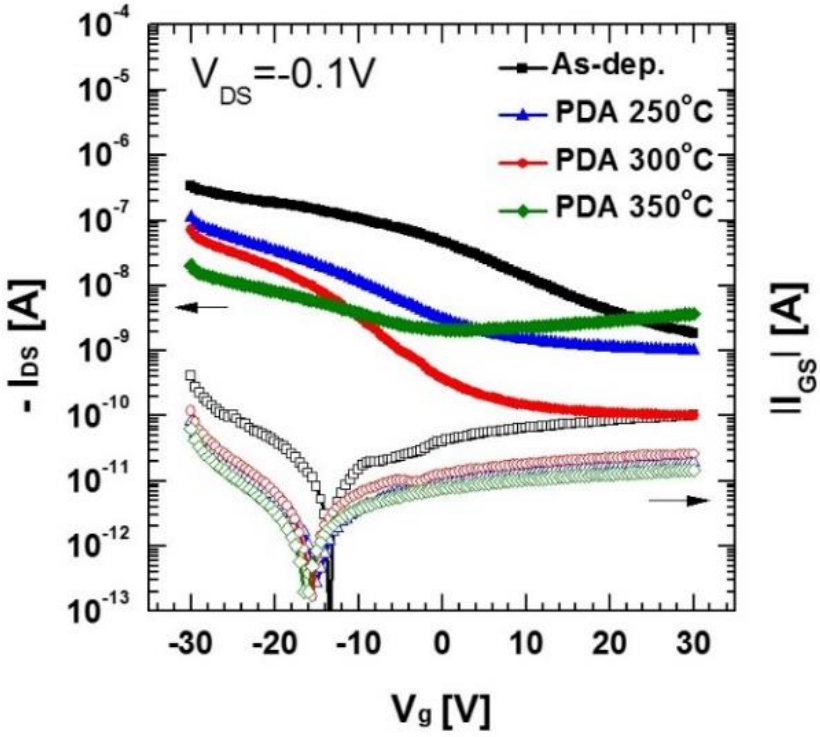


Figure 3.15. V_{GS}-I_{DS} characteristics of ALD SnO TFT depending on the PDA temperature.

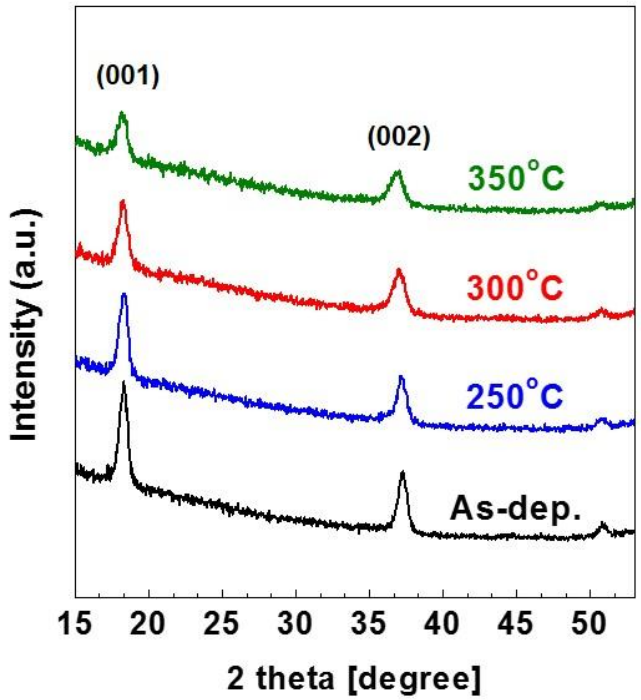


Figure 3.16. GAXRD spectra of ALD SnO thin film depending on the PDA temperature.

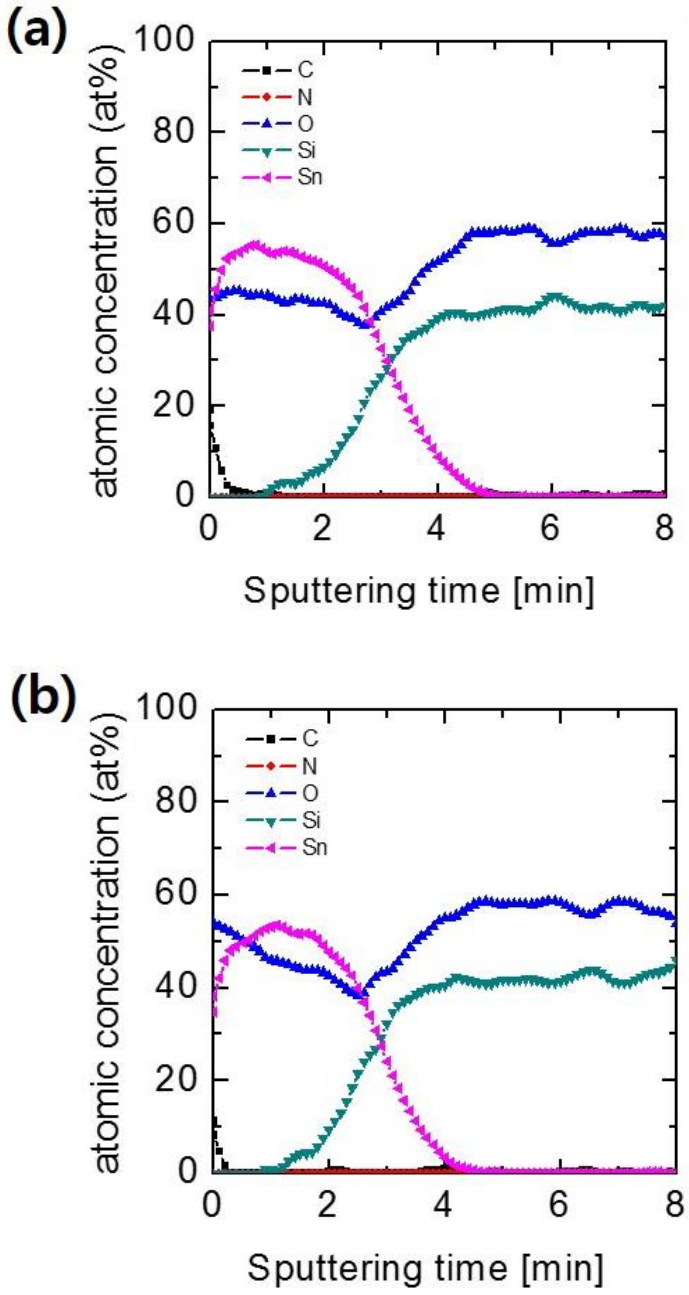


Figure 3.17. AES spectra ALD SnO TFT (a) before PDA and (b) after PDA at 300 ℃.

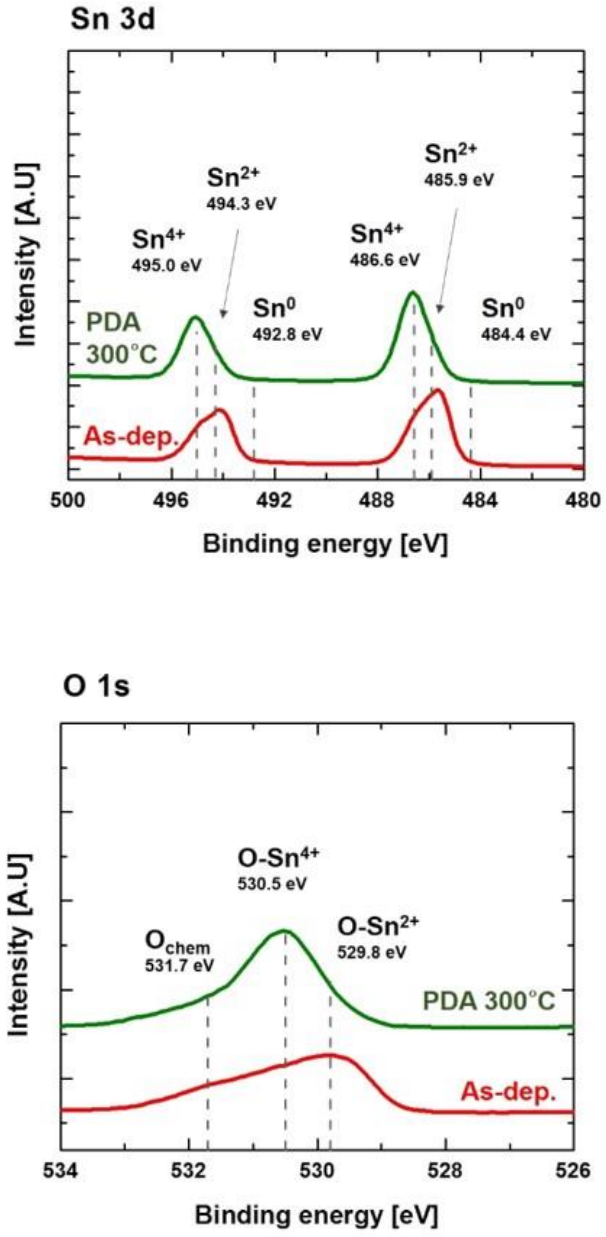


Figure 3.18. XPS spectra of Sn *3d* (upper) and O *1s* (lower) of ALD SnO TFT before and after PDA.

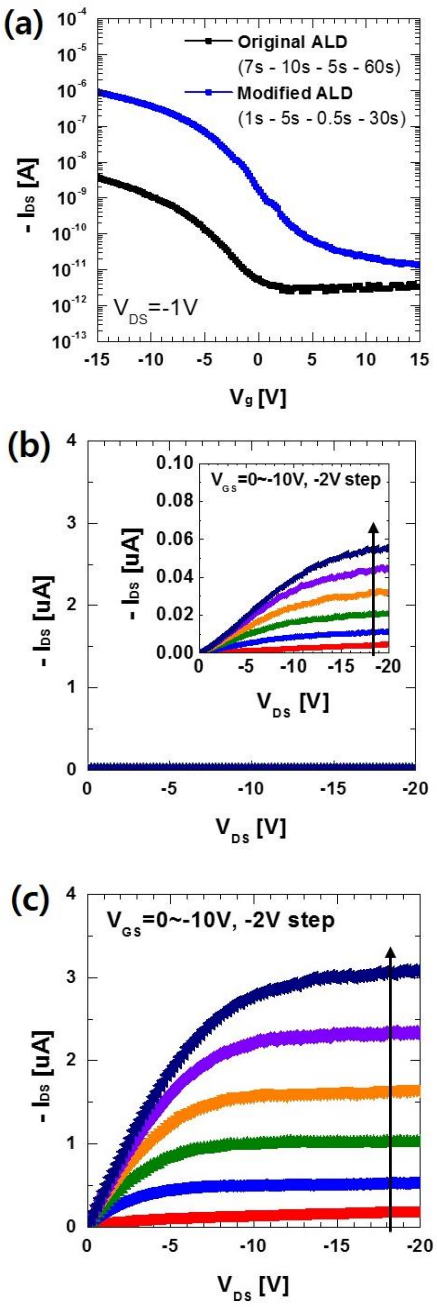


Figure 3.19. (a) Transfer characteristics of ALD SnO TFT device with different sequence, and its output characteristics fabricated by (b) original sequence (7 s – 10 s – 5 s – 60 s) and (c) modified sequence (1 s – 5 s – 0.5 s – 30 s).

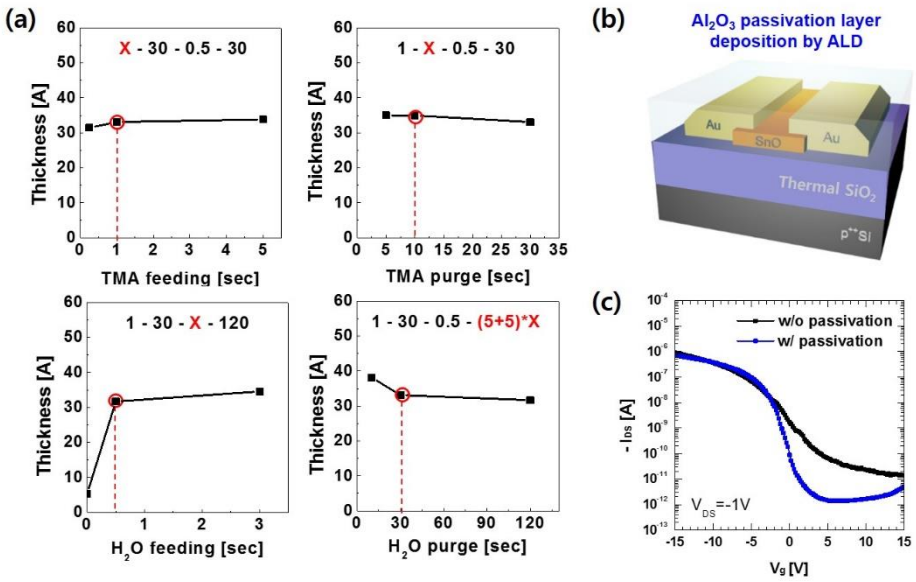


Figure 3.20. (a) Saturation behavior of ALD Al_2O_3, (b) a schematic device of of SnO TFT using ALD Al_2O_3 as a passivation layer, and (c) transfer characteristics of SnO TFT device with and without ALD Al_2O_3 passivation layer.

3.3. Bibliography

[1] H. A. Al-Jawhari, J. A. Caraveo-Frescas, M. N. Hedhili, *J. Electron. Mater.* **2015**, *44*, 117.

[2] H. Luo, L. Y. Liang,z Q. Liu, and H. T. Caoz, *ECS J. Solid State Sci. Technol.* **2014**, 3, Q3091.

[3] J. H. Han, Y. J. Chung, B. K. Park, S. K. Kim, H. S. Kim, C. G. Kim, T. M. Chung, *Chem. Mater.* **2014**, *26*, 6088.

[4] H. -N. Lee, B. -J. Song, J. C. Park, *J. Disp. Technol.* **2014**, *10*, 288

[5] T. Yang, J. Zhao, X. Li, X. Gao, C. Xue, Y. Wu, R. Tai, *Mater. Lett.* **2015**, *139*, 39.

[6] J. A. Caraveo-Frescas, P. K. Nayak, H. A. Al-Jawhari, D. B. Granato, U. Schwingenschlogl, H. N. Alshareef, *ACS Nano* **2013**, *7*, 5160.

[7] S. J. Lee, Y. Jang, H. J. Kim, E. S. Hwang, S. M. Jeon, J. S. Kim, T. Moon, K. -T. Jang, Y. -C. Joo, D. -Y. Cho, C. S. Hwang, *Appl. Mater. Interfaces* **2018**, *10*, 3810.

[8] P. -C. Hsu, C. -J. Hsu, C. -H Chang, S. -P. Tsai, W. -C. Chen, H. -H. Hsieh, C. -C. Wu, *ACS Appl. Mater. Interfaces* **2014**, *6*, 13724.

[9] Z. Wang, H. A. Al-Jawhari, P. K. Nayak, J. A. Caraveo-Frescas, N. Wei, M. N. Hedhili, H. N. Alshareef, *Sci. Rep.* **2015**, *5*, 9617.

[10] S. H. Kim, I.-H. Baek, D. H. Kim, J. J. Pyeon, T.-M. Chung, S.-H. Baek, J.-S. Kim, J. H. Han, S. K. Kim, *J. Mater. Chem. C* **2017**, *5*, 3139.

[11] C.-Y. Jeong, D. Lee, Y.-J. Han, Y.-J. Choi, H.-I. Kwon, *Semicond. Sci. Technol.* **2015**, *30*, 085004.

[12] U. Myeonghun, Y.-J. Han, S.-H. Song, I.-T. Cho, J.-H. Lee, H.-I. Kwon, *J. Semicond. Technol. Sci.* **2014**, *14*, 666.

4. Reduction of the Hysteresis Voltage in Atomic-layer-deposited p-Type SnO Thin-Film Transistors by Adopting Al_2O_3 Interfacial Layer TFTs

4.1. Bulk effect on hysteresis behavior of ALD SnO TFTs

4.1.1. Introduction

The optimization of ALD process and TFT fabrication to adopt SnO as the channel layer was found to be effective in obtaining p-type semiconductor devices with excellent I_{on}/I_{off} in previous studies.

Nonetheless, the change in V_{th} according to the sweep direction of the V_{GS}, that is, the hysteresis behavior, was not eliminated regardless of PDA process for the device, as in **Figure 4.1**a. In order to improve the problem for practical application of the p-type oxide semiconductor to CMOS logic devices, this study attempted to investigate the mechanism for this in terms of materials and to suggest improvement directions.

4.1.2. Experimental procedure

The process for TFT fabrication is the same as chapter 3.2.2. However, the thickness of SnO channel was changed in the range of 5 to 9 nm, which was

confirmed through SE (M-2000, J.A. Woollam) with X-ray fluorescent spectroscopy (XRF, Quant'X, Thermo SCIENTIFIC) measurement.

4.1.3. Results and discussion

Figure 4.1b shows the result of the V_{GS} sweep in one direction for 10 times in repetition, where no change in V_{th} of the transfer properties was observed. Therefore, it can be inferred that the hysteresis behavior found in SnO TFT devices is not caused by simple repeated measurements. It depends on the sweep direction of the V_{GS}. This phenomenon is known to be caused by carrier trapping, based on the directionality (counterclockwise, CCW) of hysteresis behavior.

The source of carrier trapping can be divided into two cases: bulk trapping by the polycrystalline characteristics of the SnO thin film and interfacial trapping between the channel layer and the GI layer.

First, to check the relationship between the hysteresis behavior and carrier trapping by the SnO bulk region, the experiment was conducted with the thickness of the SnO channel film as a variable (**Figure 4.1**c).

It was expected that the grain size would change with increasing thickness and followed by varying the carrier trapping. However, it was confirmed that the hysteresis voltage ($V_{hy}=V_{th,\,BW} - V_{th,\,FW}$) was all the same regardless of the SnO thickness and PDA (where the V_{GS} sweep from negative to positive as forward (FW) and the V_{GS} sweep from positive to negative as backward (BW)).

The rapid increase of the on current at 6 nm identifies that the critical thickness for crystallization of the SnO thin film is 6 nm. Furthermore, when a channel film having a specific thickness or more is applied (>7 nm), the rapid increase in the off current can be interpreted as the leakage current increases due to the back-channel current.

4.1.4. Summary

Thus, it was confirmed that the optimization of the channel film thickness was effective in improving the I_{on}/I_{off} characteristics, but not in reducing the V_{hy}. Based on this, further studies were conducted to confirm the interfacial effect between the channel layer and the GI layer after excluding the carrier trapping factor in the SnO bulk region for hysteresis behavior.

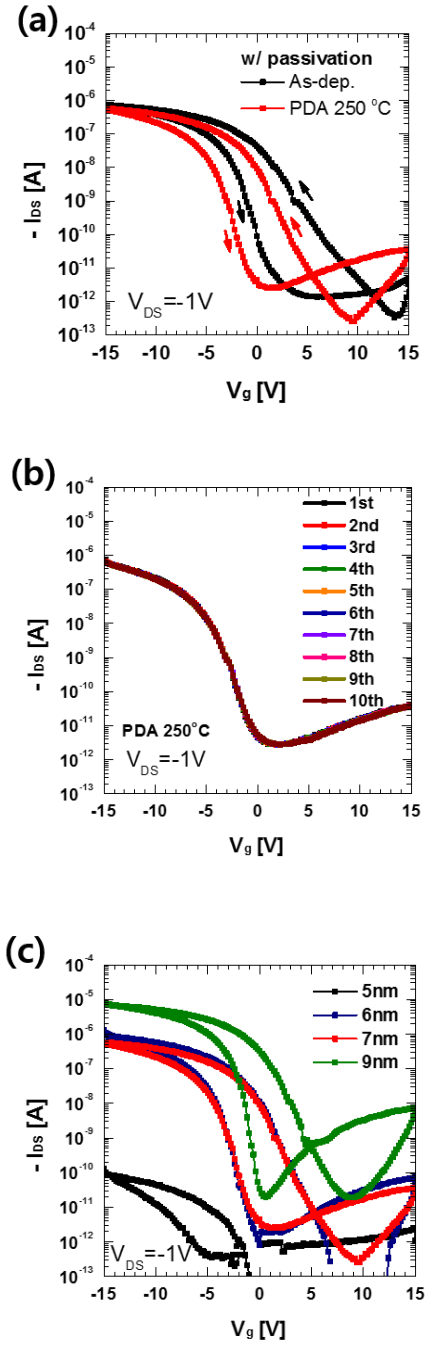


Figure 4.1. (a) Transfer curve of ALD SnO TFT before and after PDA at 250 ℃ showing hysteresis behaviors, (b) multiple sweep of transfer curve, and (c) the change of hysteresis behavior depending on the thickness of SnO channel.

4.2. Interfacial effect on hysteresis behavior of ALD SnO TFTs

4.2.1. Introduction

The high interfacial trap density (N_{it}) induced a high SS in the drain-source current (I_{DS}) –V_{GS} characteristics, and the large V_{hy} in the I_{DS}-V_{GS} curve. High V_{hy} means that the V_{th} of the TFT varies largely upon the FW and BW sweep of the V_{GS}, which is mainly ascribed to the involvement of the border traps (N_{bt}). N_{bt} is different from N_{it} in that they respond to the gate stress rather slowly because their location is slightly off from the GI/channel interface, and their energy level is deep in the band gap of the GI, making the trapping/detrapping of the carriers at N_{bt} slower than the usual time constant of N_{it}. These two critical parameters, N_{it} and N_{bt}, are mainly determined by the chemical interaction between the GI and SnO channel materials. The most common GI, however, thermally grown SiO_2, has shown significant degradation in the transport characteristics, most notably the high V_{hy} in the I_{DS}-V_{GS} curves, suggesting that there can be a significant adverse reaction between the two layers.

Therefore, in this work, the ALD Al_2O_3 film was interposed between the two layers as the IL, and its effects on the hysteresis behavior in p-type ALD SnO TFTs were examined. While the as-grown Al_2O_3 film generally has an amorphous structure, its physical and chemical properties are largely dependent

on its density, which can be varied by PDA using the rapid thermal annealing (RTA) process. In some cases, the film was crystallized by PDA involving the formation of grain boundaries, which could act as fast diffusion paths. All these process variables and accompanying property modification must thus be carefully examined, as shown in this work.

This work attempted to correlate the observed device performance with the atomic scale phenomenon by adopting the density functional theory (DFT), which calculated the defect (impurity) formation energy and stable impurity concentration, band alignment, and density of states (DOS). The calculation results corroborated the TFT performance data, confirming that the Sn diffusion into the SiO_2 GI was the main reason for the very high V_{hy} value, and amorphous Al_2O_3 with a high density provided the device with an effective barrier suppressing the adverse chemical reaction.

4.2.2. Experimental procedure

Heavily doped p-type silicon and thermally grown SiO_2 were used as the gate and the GI, respectively. The ALD Al_2O_3 films (from 2.5 to 15 nm) were adopted as ILs between the active layer and the GI. To meet the capacitance with increasing thickness of the ILs, a 35-nm-thick SiO_2 thin film was used for 5-nm-thick or less thick ILs, and a 30-nm SiO_2 thin film was used for the 15-nm-thick ILs. RTA treatment of the ILs was carried out for 2 minutes at temperatures ranging from 650 to 1000 ℃, and oxygen was used as the

annealing gas. For the channel material, 7-nm-thick SnO thin films were grown via ALD, using $Sn(dmamp)_2$ and H_2O as the Sn and O sources, respectively, at a temperature of 200 ℃. The heating temperatures of the Sn precursor and the delivery line were fixed at 70 and 120 ℃, respectively. The H_2O was maintained at 5 ℃ to suppress the excessive vapor pressure. Ar gas was used as a carrier gas of the Sn precursor and as a purge gas for both the Sn and O sources. The sequence of a single ALD cycle was as follows: (1) Sn precursor injection (1 s); (2) Sn precursor purge (5 s); (3) H_2O injection (0.5 s); and (4) H_2O purge (30 s). The SnO active layer was patterned via photolithography and wet etching using a diluted hydrofluoric acid solution. TFT devices with a gate length and width of 5 and 20 μm, respectively, were fabricated. For the source/drain metals, 80-nm-thick Au was deposited via sputtering and was patterned using the conventional liftoff method. After the 15-nm-thick Al_2O_3 film was deposited as a passivation layer, the fabricated device was annealed at 250 ℃ for 3 min in a N_2 atmosphere.

The thicknesses of all the films were measured using SE (M-2000, J.A. Woollam). The films were characterized using GAXRD (X'Pert Pro, PANalytical) for the crystal structure and XRR (X'Pert Pro, PANalytical) for the film density. XPS (AXIS SUPRA, Kratos) was used for oxidation state analysis, AES (PHI 660, Perkin-Elmer) for atomic concentration depth profiling, capacitance-voltage (C-V) measurements (HP4194A impedance

analyzer) for the capacitance characteristics, time-of-flight secondary ion mass spectrometer (TOF-SIMS, TOF.SIMS-5, ION-TOF) for element diffusion profiling, and high-resolution transmission electron microscopy (HRTEM, JEM-2100F, JEOL) for determining the internal structure of the films. A cross-sectional TEM specimen was prepared using the focused ion beam (FIB, Helios 650, FEI) etching technique. The electrical characteristics of the fabricated TFTs were measured at room temperature and in a dark box using a Hewlett-Packard 4155 semiconductor parameter analyzer. All I-V curves were measured at fixed steps voltage (V_{step}, 0.2 V) and integration time (t_{step}, 16.7 msec) of V_{GS} sweep. The sweep rate of V_{GS} (SR), SR= V_{step}/t_{step}, was calculated to be 12 V/s.

For the DFT calculations, Vienna *Ab-Initio* Simulation Package (VASP) [1,2] and the projector-augmented wave (PAW) [3,4] method were used. The generalized gradient approximation (GGA) parameterized by Perdew, Burke, and Ernzerhof (PBE) [5] and the hybrid functional proposed by Heyd, Scuseria, and Ernzerhof (HSE) [6] were used for the exchange-correlation functional, with the plane wave basis function within 500 eV cutoff energy. The *3s* and *3p* orbitals of Al; the *3s* and *3p* orbitals of Si; the *4d*, *5s*, and *5p* orbitals of Sn; and the *2s* and *2p* orbitals of O were treated as valence electrons. At first, unit cell calculations were conducted for the experimentally found phases: tetra-SnO, am-SiO_2, am-Al_2O_3, and γ-Al_2O_3. The amorphous structures were generated through the melt-quenching technique, using ab-initio molecular dynamics (AIMD) at a fixed density: 2.2 g/cm^3 for am-SiO_2 and 3.2 g/cm^3 for am-Al_2O_3.

After the melt-quenching molecular dynamics using the PBE functional, relaxation of the atomic position was conducted using HSE at the fixed cell. The details of the generation of amorphous and atomic structures are presented in **Table 4.1**.

4.2.3. Results and discussion

The device fabrication process is explained in detail in the experiment section, but it is briefly described here. **Figure 4.2** shows a schematic diagram of the fabrication process of ALD SnO TFT devices with Al_2O_3 ILs. A 30- or 35-nm-thick SiO_2 layer was thermally grown on a heavily doped p-type Si wafer, which serves as the gate, and Al_2O_3 thin films were grown on SiO_2 via thermal ALD. Then a 7-nm-thick SnO film was grown through the same thermal ALD. The SnO layer was patterned to the 5-μm-long and 20-μm-wide rectangular channel. For the source/drain metals, 80-nm-thick Au was deposited via sputtering, and was patterned using the conventional liftoff method. The fabricated devices were passivated by depositing a 15-nm-thick ALD Al_2O_3 film. The passivation effectively suppressed the oxidation of SnO, and the passivated SnO TFTs maintained stable electrical characteristics over ~1 year without degradation (**Figure 4.3**).

Figure 4.4a shows the schematic diagram of the fabricated SnO TFT, and **Figure 4.4**b shows the HRTEM of the cross-section of the SnO channel/Al_2O_3 IL/SiO_2 GI, where the IL underwent RTA at 1000 ^oC for 2 minutes. As shown

in **Figure 4.4**b, the SnO, Al_2O_3, and SiO_2 layers were structurally uniform and clearly discerned from the others. To examine the crystallographic structure of the thin films, the fast Fourier transform (FFT) patterns were obtained for a selected area corresponding to the SnO (region 1) and Al_2O_3 (region 2). It was observed that the SnO film had a tetragonal structure on the RTA-treated Al_2O_3 film and showed a clear layered structure with interlayer spacing (4.85 Å) of the (001) plane (JCPDS 006-0395). This result was consistent with the GAXRD spectra of the SnO films grown on a SiO_2/Si substrate in **Figure 4.5**a. The 5-nm-thick Al_2O_3 IL film exhibited a mixed phase consisting of a small portion of γ-phase crystallites (JCPDS 010-0425) embedded in a largely amorphous matrix. The IL films after the PDA at lower temperatures remained amorphous, which had a critical influence on the interdiffusion and device performance, as will be shown later.

Figure 4.4c, d shows the chemical status of the as-grown ALD SnO films grown on a SiO_2/Si substrate measured via XPS. From the deconvoluted Sn *3d* and O *1s* spectra, it can be determined that the SnO thin films contained two oxidation states: divalent SnO (Sn^{2+}) and tetravalent SnO_2 (Sn^{4+}) without a metallic Sn (Sn^0) state, where the Sn^{2+} component was dominantly presented. As the meta-stable SnO is easily oxidized to SnO_2, the tetravalent state is generally observed in the SnO film surface even though the films are grown under a low oxygen partial pressure or PDA is not performed [7–9]. In the case of the O *1s* orbital, the chemical peak associated with adsorbed oxygen caused

by the exposure of the sample to air was also observed, which confirmed that the involvement of Sn^{4+} was due to the exposure of the film to the atmosphere.

Additionally, AES showed that the atomic concentration ratio of Sn to O in the film was approximately 1:1, and that the film had no carbon or nitrogen contamination that had been included in the $Sn(dmamp)_2$ precursor (**Figure 4.5**b). As these impurities can act as scattering or trapping centers, the preparation of an impurity-free film is essential for enhancing the TFT performance. Therefore, it can be predicted that this SnO film will exhibit the p-type characteristics of TFTs.

Figure 4.6a-d shows the transfer characteristics of the p-type ALD SnO TFTs with no IL and with 2.5-, 4.0-, and 5.0-nm-thick Al_2O_3 ILs, respectively, measured in both forward (FW, negative to positive) and backward (BW, positive to negative) V_{GS} sweep. In these cases, all the ILs were annealed at 1000 ℃ for 2 minutes via RTA in an O_2 atmosphere. All the transfer curves in **Figure 4.6** were measured by starting the sweep from the V_{GS} of –15 V with a sweep rate of 12 V/s. Here, I_{on}/I_{off} is the ratio of maximum and minimum currents, and the field effect mobility (μ_{FE}) and subthreshold swing (SS) are the maximum and minimum values calculated from the FW curves, respectively. The difference in V_{GS} at an I_{DS} value of 1 nA between FW and BW sweep was designated as the V_{hy}. The extracted parameters in the transfer characteristics at a V_{DS} of –1.0 V are summarized in **Table 4.2**. As expected based on the SnO film characteristics shown in **Figure 4.4**, all the devices showed typical p-type

behaviors; that is, the drain current increased at the negative V_{GS} region. **Figure 4.6**a and **Table 4.2** show that the ALD SnO TFT without an IL had a high field effect mobility (μ_{FE}) of 1.8 $cm^2/V{\cdot}s$, a relatively small subthreshold swing (SS) of 0.88 V/decade, and a high I_{on}/I_{off} ratio of 2.8×10^5. A very large counterclockwise V_{hy} of 4.0 V was observed, however, which was attributed to the charge carrier trapping mostly at N_{bt} and N_{it} [10]. In contrast, the V_{hy} of the ALD SnO TFTs with Al_2O_3 ILs substantially decreased with increasing IL thickness from 2.5 to 5.0 nm (**Figure 4.6**b-d). Although V_{hy} decreased from **Figure 4.6**a to d, the I_{on} decreased and the SS slightly increased with the increasing Al_2O_3 thickness (**Table 4.2**), which could have been due to the decrease in the capacitance density of the GI stack. Especially, there were rather significant μ_{FE} and I_{on} losses for the case of the SnO TFTs with a 5-nm-thick IL. The performance degradation of this TFT might be associated with the IL structure, which showed a mixed phase consisting of a small portion of crystalline embedded in amorphous Al_2O_3, as can be seen in **Figure 4.4**b. The transport characteristics of the mixed-phase (amorphous + crystalline) GI is expected to be worse than those of the single-phase GI because there are many scattering centers at the boundary between the two phases [11,12].

As shown in **Figure 4.7**, V_{hy} did not depend on starting point of V_{GS} sweep, that is, transfer curve for the negative V_{GS} start (–15 V → +15 V → –15 V) exhibited same V_{hy} with that of the positive V_{GS} start (+15 V → –15 V → +15 V). The symmetrical hysteresis behavior indicated that there were a few donor-

like or acceptor-like interface traps present in both the SnO/SiO_2 and SnO/Al_2O_3 interfaces. The transfer characteristics of SnO TFTs were repeatedly measured up to 10 times, but V_{hy} did not change either (**Figure 4.8**). Furthermore, transfer curve for zero V_{GS} start (0 V → +15 V → –15 V → 0 V or 0 V → –15 V → +15 V → 0 V) was measured for the devices without IL and with 5-nm-thick Al_2O_3 IL as shown in **Figure 4.9**. The hysteresis behaviors were identified to be same regardless of the starting point of V_{GS} (–15, 0, +15 V) except for the first backward V_{GS} sweep from 0 V (0 V → –15 V) in the devices without IL (**Figure 4.9b**). This small difference is understandable because the carrier trapping has not occurred at 0V yet. This must be also the case for the first forward V_{GS} sweep from 0 V (0 V → +15 V), but the I_{DS} remained low since this corresponds to the depletion condition. Therefore, the difference cannot be seen if any under this circumstance. In all case, however, the major part of the hysteresis was attributed to the electron trapping under the positive V_{GS}, which was gradually disappeared by increasing the thickness of Al_2O_3 IL. The irrelevance of the major V_{hy} to the starting point of V_{GS} and gradual disappearance of the V_{hy} with increasing IL thickness indicated that the reduction of the electron trapping was mainly determined by N_{bt} rather than N_{it}.

To investigate the determining factors affecting N_{bt}, the interdiffusion between the SnO and GI layers was examined, which is expected to generate a trap state slightly away from the GI/channel interface. The TOF-SIMS analysis

was carried out to confirm the elemental depth profiling. **Figure 4.10**a-c shows the TOF-SIMS depth profiles related to Sn element (Sn^+, SnO_2^-, SnO^-, and Sn^-) of the SnO/SiO_2, SnO/Al_2O_3(2.5nm)/SiO_2, and SnO/Al_2O_3(5.0nm)/SiO_2 specimens, respectively, after the RTA of the Al_2O_3 ILs at a temperature of 1000 ^oC, which is equivalent to the condition in **Figure 4.6**. Depth profiles of the other major elements (O^-, Al^-, Si^-) of the specimens are shown in **Figure 4.11**. The $SiOH^+$ and $AlSiO^+$ functional groups were used as a reference for identifying the interface with a SiO_2 thin film. It was observed that the abundant Sn^+ ions contributed by SnO thin film diffused into the SiO_2 GI in the absence of the IL. However, their diffusion depth was significantly decreased when adopting ILs, and a 5-nm-thick IL showed especially efficient suppression of the diffusion into the GI. In the case of the other ions (SnO_2^-, SnO^-, Sn^-), the intensity was greatly reduced in the Al_2O_3 region and then increased again in the SiO_2 region, which is reflecting the low and high solubility of Sn element for Al_2O_3 and SiO_2, respectively. In other words, it implies that Sn element can more easily diffuse into the SiO_2 layer than Al_2O_3 layer. In particular, as the ILs are inserted, the SIMS intensity at the interface of SiO_2 decreased by three orders of magnitude for SnO_2^- ions and decreased by one order of magnitude for SnO^- and Sn^- ions compared with the SnO/SiO_2. Due to the diffusion barrier function of IL, the amount of diffused Sn in the SiO_2 film falls below the solubility limit, and the overall intensity of the Sn-related ions decreased by ~ two orders of magnitude. To complement the measurement limitation on the

accurate diffusion depth of Sn atoms in TOF-SIMS analysis, the elemental line profiles of $SnO/Al_2O_3/SiO_2$ sample were also obtained by energy dispersive spectroscopy (EDS) in scanning transmission electron microscopy (STEM) (**Figure 4.12**). The EDS analysis indicated that the Gaussian-like diffusion depth profile of Sn atoms in Al_2O_3 IL, which may be correlated with the dependence of V_{hy} on the IL thickness shown in **Figure 4.6**.

In **Figure 4.11**, it was also confirmed that significant Si-diffusion into the SnO layer occurred for the case of direct contact between the SiO_2 and SnO layers, and the Al_2O_3 ILs effectively suppressed it. The effects of the Al_2O_3 IL on such interdiffusion and the following variations in the electrical properties were further investigated by theoretical studies using the DFT calculation. It will be shown that while the defects generated by the cation (Si or Al) diffusion from the GI oxides to the SnO active layer formed no gap states, the defects generated by Sn diffusion from the SnO to GI oxides formed the gap states in GI oxides.

Figure 4.13a, b shows the activation energy of Sn diffusion from one substitutional site to the nearest substitutional site in am (amorphous)-SiO_2 and am-Al_2O_3, respectively. The initial position and charged state of the Sn substitutional defect were determined by the formation energy calculation (see **Figure 4.14**) and set to the most stable state (Sn_{Si}^{+0} in am-SiO_2 and Sn_{Al}^{-1} in am-Al_2O_3). The activation energy of Sn diffusion in am-SiO_2 was predicted to be much lower than that in am-Al_2O_3, and this calculation result was consistent

with the experimental results that the diffusion depth of Sn into am-SiO_2 was longer than that into am-Al_2O_3 (**Figure 4.10**). Both experiments and calculations indicated that the am-Al_2O_3 acted as an effective diffusion barrier for Sn atoms.

Figure 4.14a-c shows the formation energy of the Sn substitutional defects in am-SiO_2, am-Al_2O_3, and γ-Al_2O_3, respectively, where the various charge states of the Sn ions are noted in the figure. The positions of the aligned VBM and conduction band minimum (CBM) of SnO were obtained from the band alignment calculation (**Figure 4.15**) and are indicated by the dashed red and blue lines in **Figure 4.14**, respectively. The DOSs are shown on the right side for the most stable charged state in the range of the band gap of SnO. It was shown that Sn_{Si}^{+0} is the most stable and has the gap states at approximately 0.8 eV above the CBM of SnO in am-SiO_2 (~1.3 eV below the CBM of SiO_2), which formed the N_{bt}; that Sn_{Al}^{-1} is the most stable and has the gap states at approximately 2.4 eV below the VBM of SnO in am-Al_2O_3 (~2.1 eV above the VBM of am-Al_2O_3); and that the Sn_{Al}^{-1} state is the most stable state and has no gap states in γ-Al_2O_3. Note that the defects generated by the cation (Si or Al) diffusion from the GI oxides to the SnO active layer were identified to have had a negligible concentration and showed no gap states (**Figure 4.16** and **4.17**).

Using the calculated positions of VBM, CBM, and the gap states of the defects, the schematic band diagrams in the positive and negative V_{GS} are shown in **Figure 4.18**a, b for the samples without and with ILs, respectively.

When SnO contacts with am-SiO_2, the Sn in SnO diffuses to the am-SiO_2 and substitutes Si to form Sn_{Si}^{+0}. This defect state has gap states located at ~0.8 eV above the CBM of SnO, and the gap states become empty for negative V_{GS} (left figure in **Figure 4.18**a) and partially filled for positive V_{GS} reversibly (right figure in **Figure 4.18**a). This explains why the SnO/am-SiO_2/p^{++}Si stacks showed $V_{th,\,FW}$~0 V for the forward sweep and $V_{th,\,BW}$>0 V for the backward sweep, and consequently, large hysteresis (**Figure 4.6**a). On the other hand, when an am-Al_2O_3 IL is inserted between SnO and am-SiO_2, the Sn in SnO diffuses to the am-Al_2O_3 and substitutes Al to form a fixed charge, Sn_{Al}^{-1}. Note that although the equilibrium Sn concentration in am-Al_2O_3 is higher than that in am-SiO_2 by several orders of magnitude (**Figure 4.19**; lower formation energy of Sn_{Al}^{-1} than Sn_{Si}^{+0} in **Figure 4.14**), the actual Sn concentration in am-Al_2O_3 may be lower than the equilibrium value due to the high activation energy for diffusion (**Figure 4.13**), which was also verified in the previous diffusion profile (**Figure 4.10**). This defect state, however, has gap states located at ~2.4 eV below the VBM of SnO, and the gap states were always filled by electrons regardless of the gate bias (**Figure 4.18**b) because the maximum voltage applied to the Al_2O_3 film, Al_2O_3(15 nm)/SiO_2(30 nm) stacks in $\pm$15 V, is lower than 2.5 V (**Figure 4.20**). These findings with effective barrier function of Al_2O_3 for Sn diffusion explain why $V_{th,\,FW}$ was shifted to >0 V and why the hysteresis was reduced by employing am-Al_2O_3 ILs (**Figure 4.6**b-d).

In order to further investigate the quantitative relation between the degree of

reduction of Sn diffusion at the SiO_2 interface (**Figure 4.10**) and the corresponding V_{hy} of SnO TFTs (**Figure 4.6**), the effective trap density ($N_{bt} = V_{hy}.C_{ox}/q$), where C_{ox} is the capacitance density of GI stack and q is the elementary charge, was estimated. The N_{bt} was calculated to be 2.6×10^{12}, 1.3×10^{12}, and 3.7×10^{11} cm^{-2} for SnO TFTs with no IL and with 2.5-, and 5.0-nm-thick ILs, respectively. Considering the TOF-SIMS analysis in **Figure 4.10**, the N_{bt} decreased as the intensity of Sn-related ions decreased at the SiO_2 interface. For the given C_{ox} values, N_{bt} must be below ~ 10^{11} cm^{-2} to make V_{hy} negligible (< ~10 mV).

From these calculations, it can be expected that the SnO TFTs may show better performance if the am-Al_2O_3 IL is completely crystallized to γ-Al_2O_3, because the Sn_{Al}^{-1} in γ-Al_2O_3 has no gap states (**Figure 4.14**c) and the equilibrium concentration of the Sn substitutional defects in γ-Al_2O_3 is much lower than that in am-Al_2O_3 (**Figure 4.19**). This may seem to be compatible with the results shown in **Figure 4.6**d, where the partially crystallized IL showed the lowest V_{hy} value (0.6 V). More complicated behaviors of Sn diffusion and Al_2O_3 IL crystallization, however, are involved, as shown below.

Figure 21a, b shows the transfer characteristic results of the 15-nm-thick am-Al_2O_3 and the γ-Al_2O_3 IL, respectively, whose structure could be altered by varying the annealing temperature to 800 and 1000 ℃. The GAXRD spectra in **Figure 4.21**c indicate that the former remained amorphous, but the latter was crystallized into the γ-phase. Interestingly, the TFT with the IL annealed at 800 ℃

showed a minimum V_{hy} of 0.2 V and N_{bt} of 1.2×10^{11} cm^{-2} with a promising μ_{FE} of 1.6 $cm^2/V\cdot s$, an SS of 1.06 V/decade, and an I_{on}/I_{off} ratio of 1.2×10^5 (**Figure 4.21**a). The device with the IL annealed at 1000 ℃, however, showed a significantly increased V_{hy} of 3.8 V and N_{bt} of 2.4×10^{12} cm^{-2} (**Figure 4.21**b, see **Table 4.2** for more detailed information). This phenomenon is consistent with a previous report that the impurity diffusion is accelerated along the grain boundaries when the Al_2O_3 film is crystallized [13]. This implies that the Sn diffusion from SnO to am-SiO_2 is reactivated through the grain boundaries of the crystallized γ-Al_2O_3, although it was 15 nm thick. During the sufficiently high positive V_{GS} stressing (V_{GS} sweep into +15 V), the minority carrier in the SnO active layer (electron) could be transported to the SiO_2 GI probably through the grain boundaries of the crystallized Al_2O_3 and could be trapped at the Sn_{Si}^{+0} states. It should be noted that the band gap of SnO is only ~0.7 eV, which is much smaller than that of the n-type oxide semiconductor, such as ZnO or the In-Ga-Zn-O system, so the minority carrier can be accumulated at a sufficiently high positive V_{GS}.

As shown in **Figure 4.21**d, XPS analysis was performed to examine the change in the chemical states according to the Sn diffusion into the Al_2O_3 film. **Figure 4.21**d shows the Al *2p* XPS spectra of the Al_2O_3(15 nm)/SiO_2 (black line) and SnO(7 nm)/Al_2O_3(15 nm)/SiO_2 (red line) samples, where the Al_2O_3 films underwent RTA at 800 and 1000 ℃, respectively. This represents the chemical-state change of the Al_2O_3 according to the presence and absence of

the ALD SnO layer on top. As shown in **Figure 4.21**d (bottom data), there was no apparent difference in the Al *2p* peaks of the am-Al_2O_3 films with and without a SnO overlayer. On the other hand, the Al *2p* peak of the γ-Al_2O_3 film shifted towards the lower binding energy by ~0.3 V when the SnO layer was present (**Figure 4.21**d, top data) compared with the data of only Al_2O_3 IL. This shift can be interpreted as follows: the Al-O interaction was weakened because the lower-valence-state Sn^{2+} was substituted for the higher-valence-state Al^{3+} ions. The result shown in **Figure 4.21**d elucidates that the Sn diffusion presumably along the grain boundaries was more dominant in the crystallized Al_2O_3 film, which was not taken into account in the DFT calculation. Therefore, the amorphous phase of the Al_2O_3 films should be maintained to obtain hysteresis-free characteristics in SnO TFT operation.

As long as the amorphous structure of the Al_2O_3 IL phase was maintained, V_{hy} decreased as the thickness of am-Al_2O_3 increased due to its effective function as an Sn diffusion barrier (**Table 4.2**). In addition to the thickness, the density of am-Al_2O_3 can have effects on the TFT characteristics. **Figure 4.22**a, b presents the transfer characteristics of the SnO TFTs with 5-nm-thick ILs annealed at 650 and 800 ℃, respectively. The corresponding data for the same-structure device with the RTA temperature of 1000 ℃ was included in **Figure 4.6**d, where the Al_2O_3 IL was composed of (mainly) amorphous phase and (minorly) γ-Al_2O_3 (**Figure 4.4**b). It appeared that the crystallization of the am-Al_2O_3 film was enhanced when the film thickness increased from 5 to 15 nm,

which is consistent with the previous reports [14,15]. The film densities of the am-Al_2O_3 films annealed at different temperatures were measured through XRR supported by the refractive index using SE, as shown in **Figure 4.23**. **Figure 4.12**c shows the graph that plots the V_{hy} values and the film densities of the am-Al_2O_3 ILs as a function of the RTA temperature (again, the 1000 ℃-annealed 5-nm-thick IL is a mixture of amorphous and crystalline phases). As the annealing temperature increased from 650 to 1000 ℃, the film density increased from 3.39 to 3.90 g/cm^3, and V_{hy} decreased from 3.6 to 0.6 V. This indicates that the density of the am-Al_2O_3 ILs had a crucial effect on hysteresis reduction by preventing the diffusion of Sn into the SiO_2 GI. There have been several reports on the influence of the film density on the diffusion barrier ability [16,17]. These reports suggest that films with a higher density can more effectively block the atomic diffusion. Therefore, it is reasonable that the Sn diffusion is suppressed more effectively as the Al_2O_3 film density increases in the SnO/am-Al_2O_3/SiO_2 structure.

4.2.4. Summary

In conclusion, the effects of the IL on the hysteresis behaviors of p-type ALD SnO TFTs were examined in this study. The SnO/am-SiO_2/p^{++}Si stacks showed a V_{hy} of 4.0 V resulting from the substitutional defects of Sn_{Si}^{+0}, which has gap states near the CBM of SnO. In contrast, the Sn substitutional defects in am-

Al_2O_3 has gap states far below the VBM of SnO, which can hardly induce the hysteresis effect because they always remain trapped during the entire V_{GS} sweep. Therefore, adopting the am-Al_2O_3 ILs between the SnO active layer and the am-SiO_2 GI results in the significant reduction of the hysteresis effect. The maintenance of the amorphous phase, thickness, and density of the Al_2O_3 ILs was identified to have crucial effects on hysteresis reduction because the Sn diffusion barrier property is dependent on these parameters. By retaining the amorphous phase, an appropriately high thickness (15 nm), and a high film density of the Al_2O_3 ILs, it was possible to reduce the V_{hy} to 0.2 V, with high TFT performances: a μ_{FE} of 1.6 $cm^2/V{\cdot}s$, an SS of 1.06 V/decade, and an I_{on}/I_{off} of 1.2×10^5, which were achieved when the 15-nm-thick Al_2O_3 IL was annealed at 800 ℃. An excessively thick IL, however, can lead to gate capacitance degradation, so optimization of the Al_2O_3/SiO_2 gate stack for both hysteresis and capacitance is required to improve the device performance, which is planned for the future work.

		Lattice parameters						# of atoms/ cell	Density [g/cm^3]
		a [Å]	b [Å]	c [Å]	α	β	γ		
tetra-SnO	**Unit cell**	3.80	3.80	4.97	90.0°	90.0°	90.0°	4	6.23
	Supercell	11.40	11.40	9.94	90.0°	90.0°	90.0°	72	
tetra-SnO_2	**Unit cell**	4.76	4.76	3.19	90.0°	90.0°	90.0°	6	6.93
am-SiO_2	**Supercell**	10.29	10.29	10.29	90.0°	90.0°	90.0°	72	2.20
am-Al_2O_3	**Supercell**	11.40	11.40	9.76	90.0°	90.0°	90.0°	120	3.20
γ-Al_2O_3	**Unit cell**	5.51	5.59	14.24	89.6°	93.0°	120.3°	40	3.58
	Supercell	11.03	11.19	14.24	89.6°	93.0°	120.3°	160	

Table 4.1. Structure parameters calculated by HSE with the unified α=0.25. The amorphous supercell was generated by the melt-quenching technique using ab-initio molecular dynamics with PBE functional, and the atomic position was finally relaxed using HSE functional: melting 7000 K → quenching 2500 K to 300 K (100 K/ps) → 0 K MD → PBE relaxation → HSE relaxation at the fixed cell. The denoted supercell was used to calculate defect formation energy using HSE functional with α=0.25.

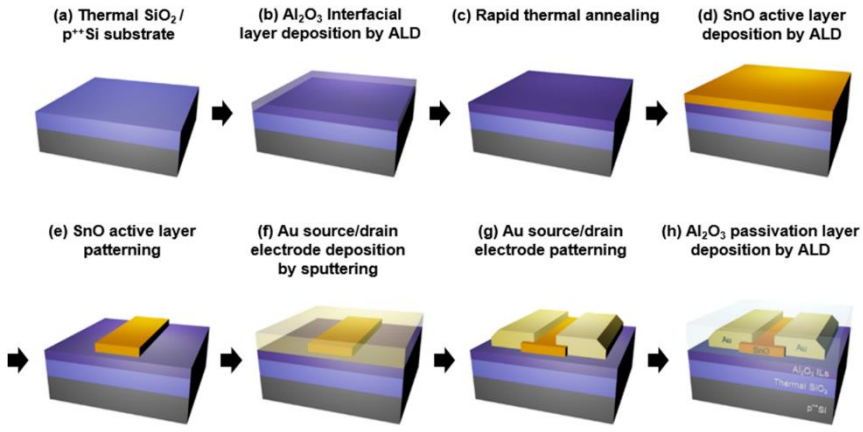


Figure 4.2. Schematics of the fabrication process of ALD SnO thin film transistors, in which annealed Al_2O_3 ILs were inserted between the SnO active layer and the SiO_2 gate insulator.

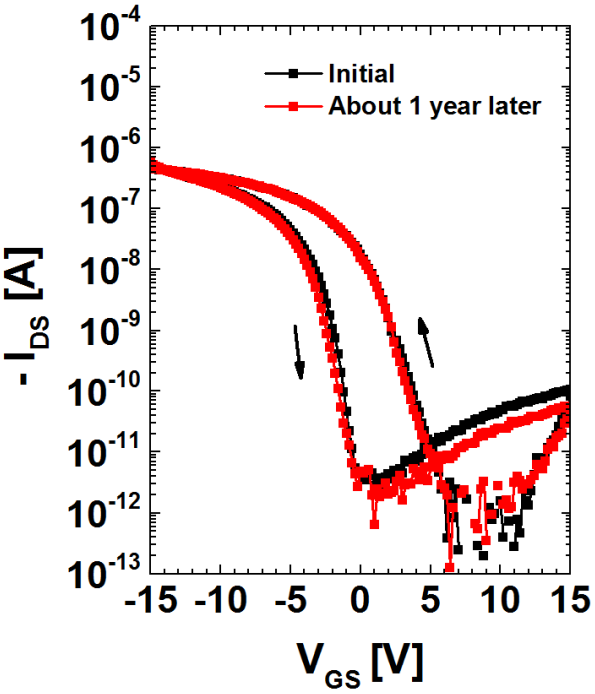


Figure 4.3. Long term stability of ALD SnO TFTs with a passivation layer. Here, the transfer characteristics of the SnO TFTs without ILs are shown. During each measurement, the devices were stored at room temperature. The passivated SnO TFTs exhibit remarkable stability over one year without degradation of on current and V_{th}. This result shows that the passivation layer effectively suppresses the oxidation reaction from SnO to SnO_2, and TFT devices can maintain stable electrical characteristics for such a long period.

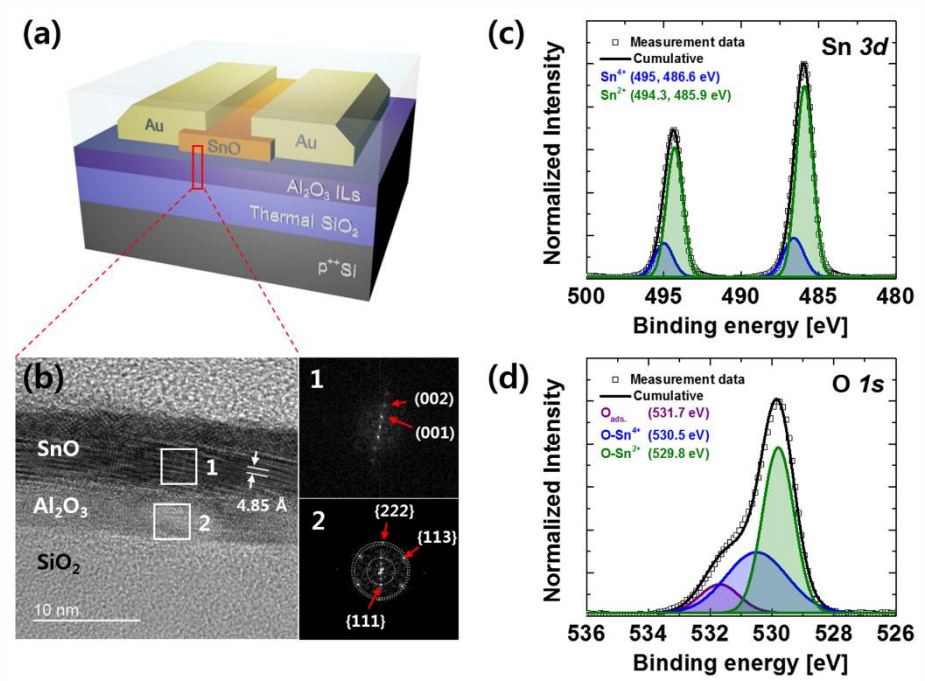
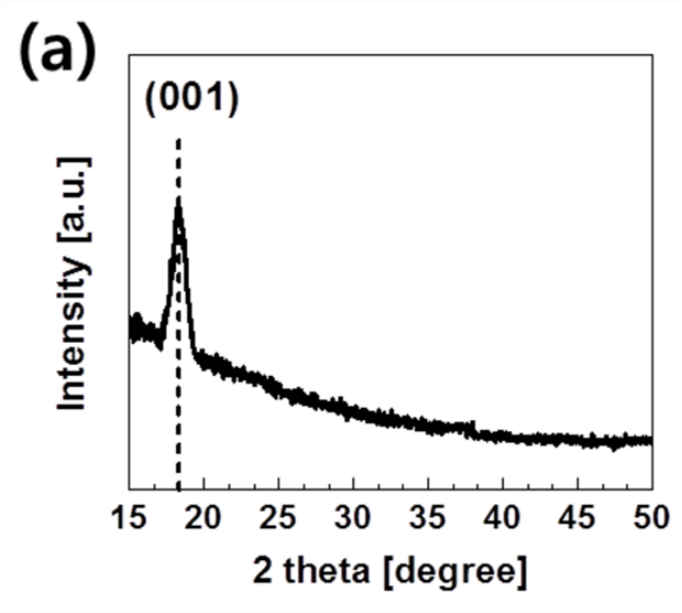


Figure 4.4. (a) Schematics of the ALD SnO TFTs with Al_2O_3 ILs. (b) HRTEM images of the cross-section in the SnO(7 nm)/Al_2O_3(5 nm, RTA 1000 ℃)/SiO_2 sample. 1 and 2 show the FFT patterns for a selected area corresponding to the tetragonal SnO, and partially crystallized Al_2O_3, respectively. XPS spectra of the (c) Sn *3d* and (d) O *1s* core levels for the 7-nm-thick SnO films grown on a SiO_2/Si substrate.



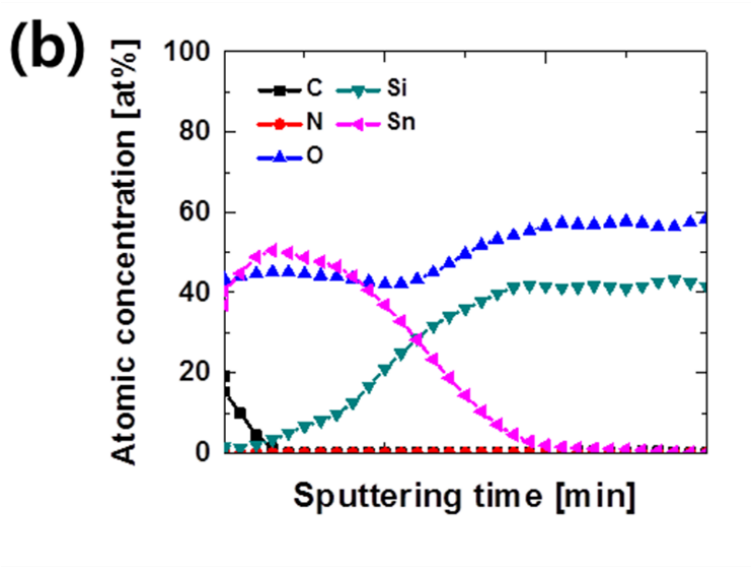


Figure 4.5. Thin film characteristics of the 7-nm-thick SnO films grown on SiO_2/Si substrate measured by (a) GAXRD, (b) AES depth profiling.

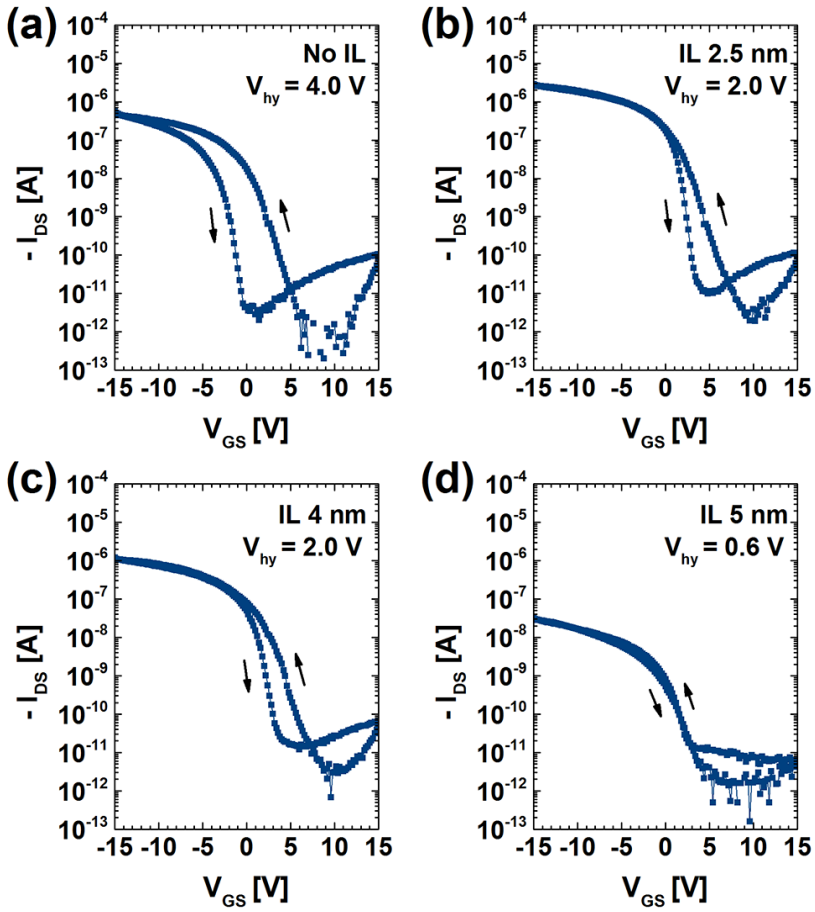


Figure 4.6. Transfer characteristics of the SnO TFTs (a) without ILs and with (b) 2.5-nm-thick, (c) 4-nm-thick, and (d) 5-nm-thick Al_2O_3 ILs, respectively. In the cases where Al_2O_3 ILs were inserted, the ILs were annealed at 1000 ℃ via RTA. The V_{DS} was fixed at −1 V in all the cases.

Interfacial layer (IL) condition			Electrical properties of SnO TFTs using different IL conditions				
Thickness [nm]	Phase	RTA temperature [ºC]	I_{on}/I_{off} [a)]	μ_{FE} [b)] [$cm^2/V{\cdot}s$]	SS [c)] [V/decade]	V_{hy} [d)] [V]	N_{bt} [e)] [$/cm^2$]
0		-	2.8×10^5	1.8	0.88	4	2.6×10^{12}
2.5	am-	1000	2.9×10^5	5.4	0.51	2	1.3×10^{12}
4	am-	1000	9.9×10^4	3.2	0.74	2	1.3×10^{12}
5	am- + γ	1000	7.5×10^3	0.1	1.03	0.6	3.7×10^{11}
15	γ	1000	4.4×10^5	1.8	0.74	3.8	2.4×10^{12}
15	am-	800	1.2×10^5	1.6	1.06	0.2	1.2×10^{11}

Table 4.2. Main TFT parameters extracted from the transfer characteristics of each condition (all the parameters were calculated from the forward-direction curves in the transfer characteristics)

a)I_{on}/I_{off} is the ratio of maximum and minimum currents.

b)Field effect mobility (μ_{FE}) is the maximum value at $V_{DS} = -1$ V.

c)Subthreshold swing (SS) is the minimum value at $V_{DS} = -1$ V.

d)Threshold voltage is the gate voltage for a value of I_{DS} at 1 nA, and hysteresis voltage (V_{hy}) is the threshold voltage difference between the forward and backward directions.

e)Effective trap density (N_{bt}) is the value of V_{hy} multiplied by capacitance density of the gate insulator stack divided by the elementary charge.

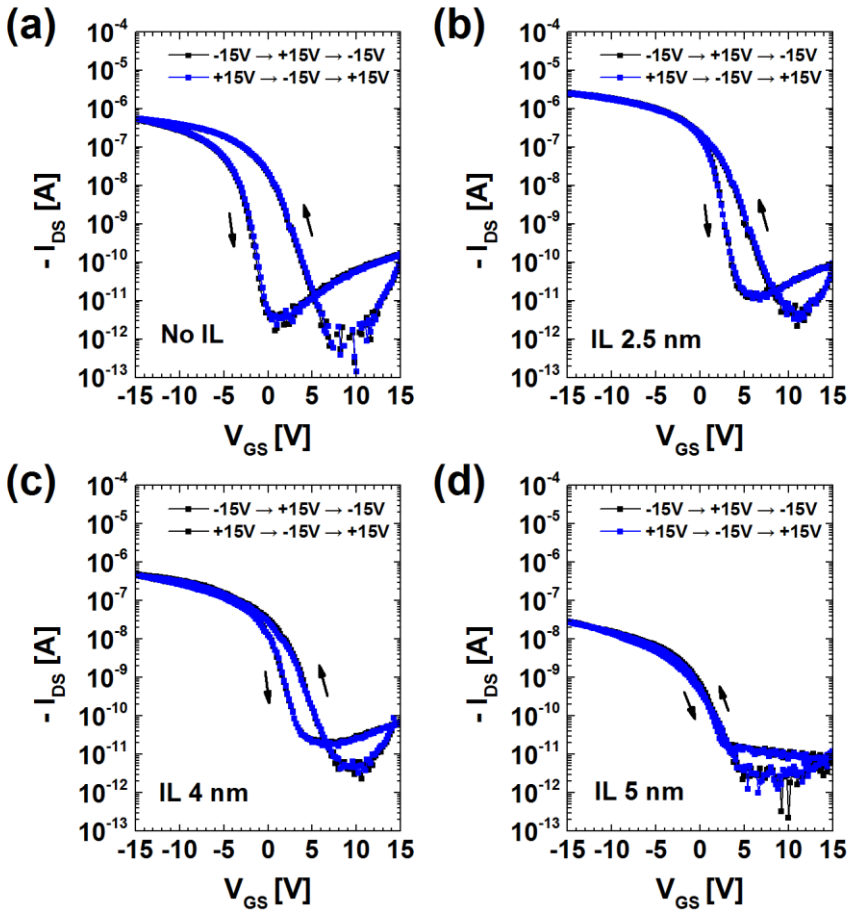


Figure 4.7. Transfer characteristics of the SnO TFTs measured with the different starting V_{GS} and a given V_{DS} of –1 V. The devices (a) without ILs and with (b) 2.5-nm-thick, (c) 4-nm-thick, and (d) 5-nm-thick Al_2O_3 ILs.

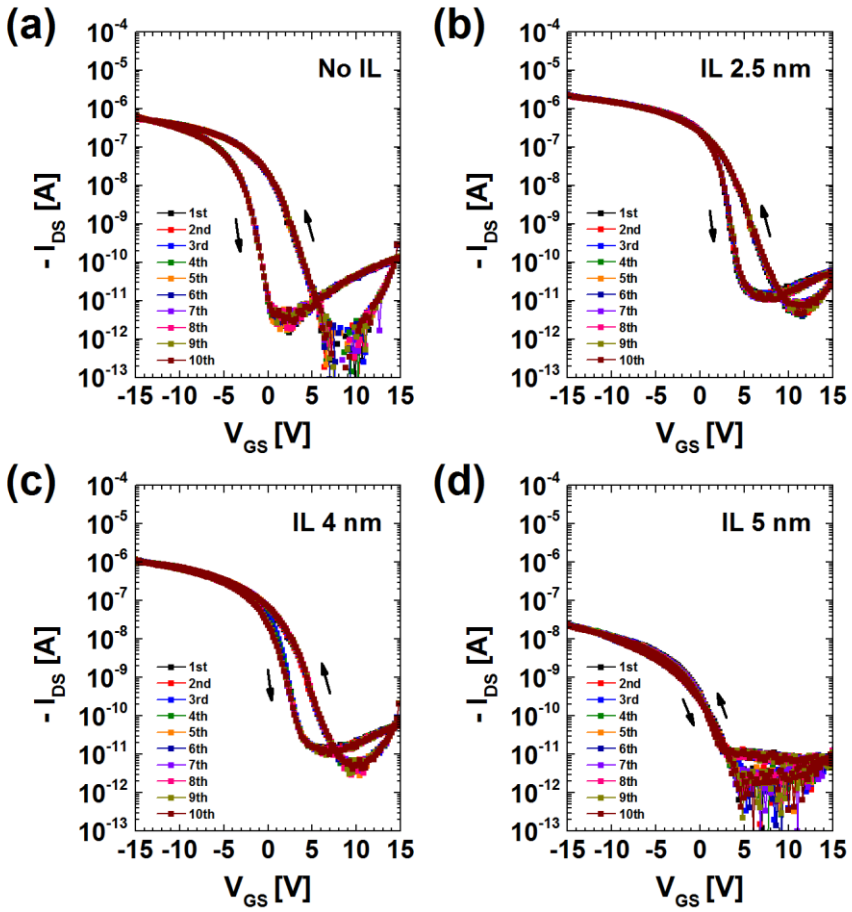


Figure 4.8. Transfer characteristics of the SnO TFTs measured by 10 times repetition of the V_{GS} sweep at V_{DS} of –1 V. The devices (a) without ILs and with (b) 2.5-nm-thick, (c) 4-nm-thick, and (d) 5-nm-thick Al_2O_3 ILs.

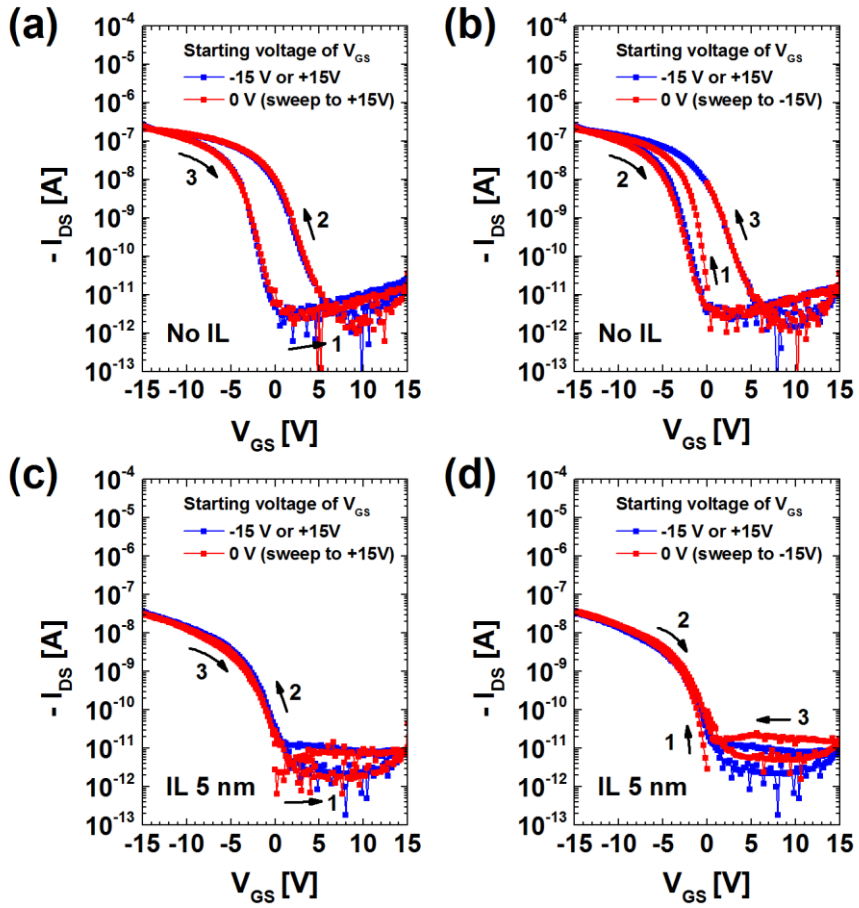


Figure 4.9. Transfer characteristics of the SnO TFTs measured with the 0 V starting V_{GS} and a given V_{DS} of –1 V. The devices without ILs starting with (a) forward gate voltage sweep (0 V → +15 V → –15 V → 0 V) and (b) backward gate voltage sweep (0 V → –15 V → +15 V → 0 V). The devices with 5-nm-thick Al_2O_3 ILs starting with (c) forward gate voltage sweep (0 V → +15 V → –15 V → 0 V) and (d) backward gate voltage sweep (0 V → –15 V → +15 V → 0 V).

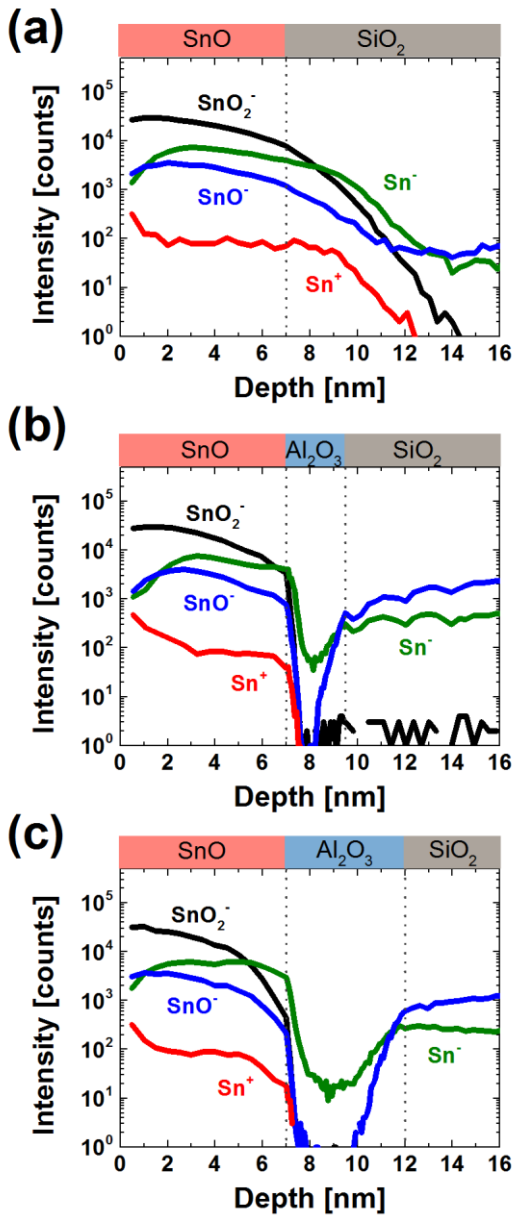


Figure 4.10. TOF-SIMS depth profiles related to Sn of the SnO thin films (a) without an IL and with (b) a 2.5-nm-thick IL and (c) a 5-nm-thick IL annealed at 1000 ℃ via RTA.

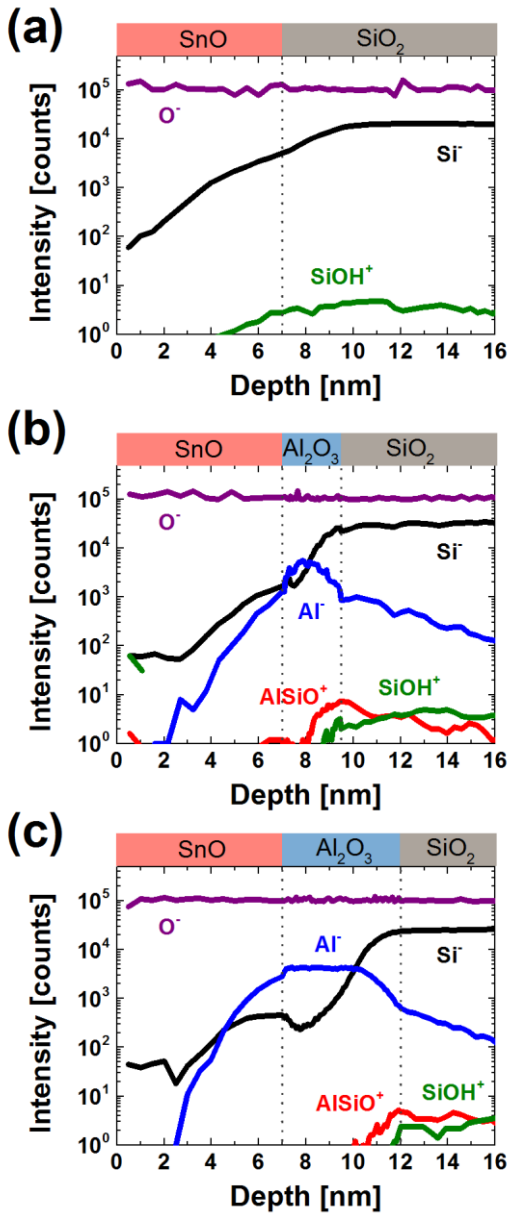


Figure 4.11. TOF-SIMS depth profiles of the SnO thin films (a) without an IL and with (b) a 2.5-nm-thick IL and (c) a 5-nm-thick IL annealed at 1000 ℃ via RTA, respectively.

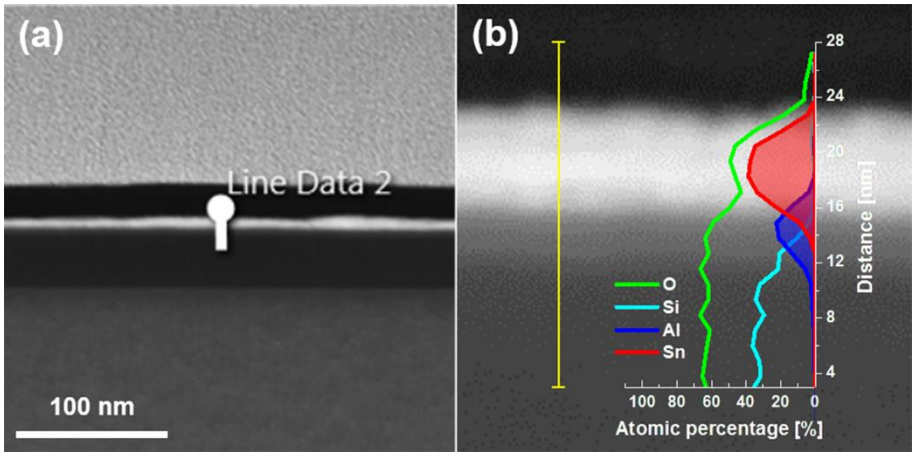


Figure 4.12. Nanochemical analysis for the cross section in the SnO(7 nm)/Al_2O_3(5 nm, RTA 1000 ℃)/SiO_2 sample. (a) STEM image showing a region where EDS line scan is performed. (b) The elemental line profiles for O (green), Si (cyan), Al (blue), Sn (red) revealed by STEM-EDS measurement. The vertical axis is the distance from the SiO_2 gate insulator to carbon-coated SnO layer, whereas the horizontal axis is the atomic fraction of each species.

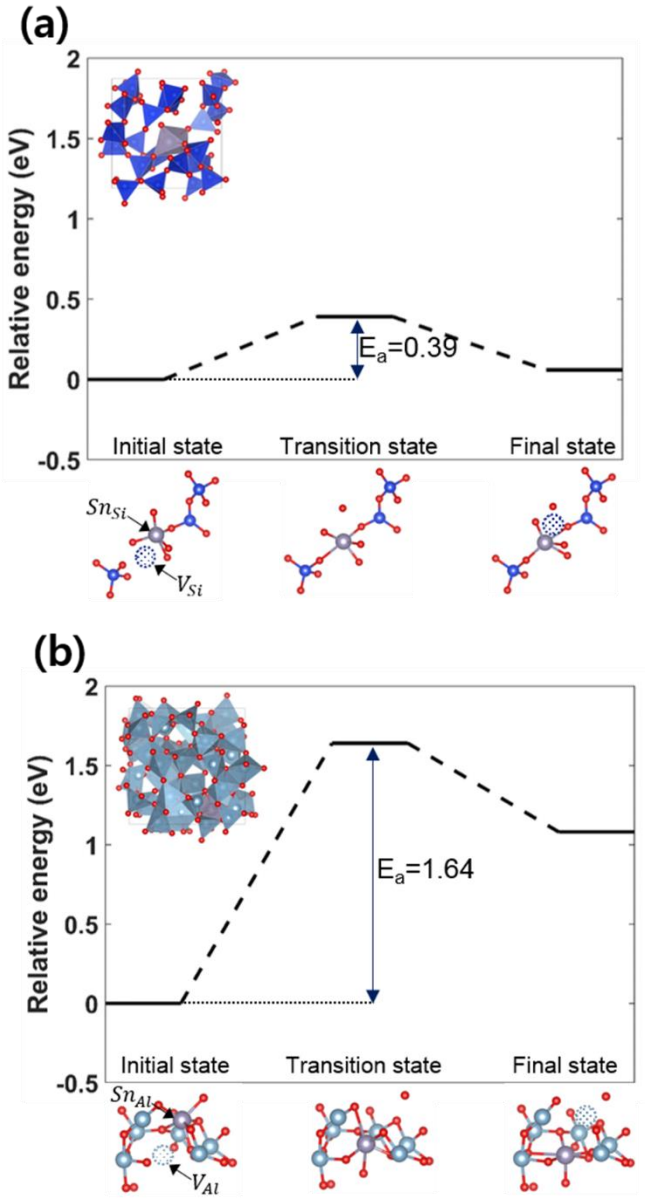


Figure 4.13. (a) Calculated activation energy of Sn diffusion from one substitutional site to the nearest substitutional site: (a) Sn_{Si}^{+0} in am-SiO_2 and (b) Sn_{Al}^{-1} in am-Al_2O_3.

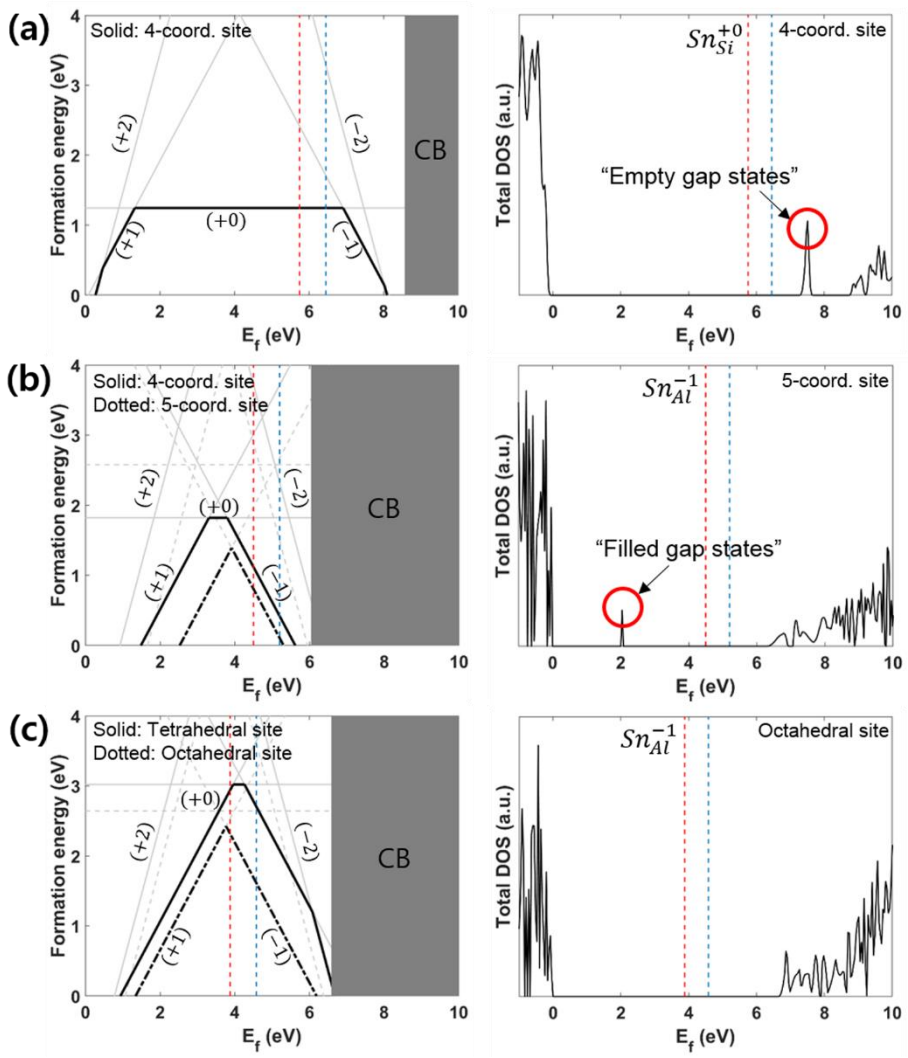


Figure 4.14. Calculated formation energy of the Sn substitutional defects in the several charged states and density of states (DOSs) of the most energetically stable charged state in the SnO bandgap range: (a) Sn_{Si} in am-SiO_2; (b) Sn_{Al} in am-Al_2O_3; and (c) Sn_{Al} in γ-Al_2O_3. The dashed red and blue lines indicate the aligned VBM and CBM of SnO, respectively.

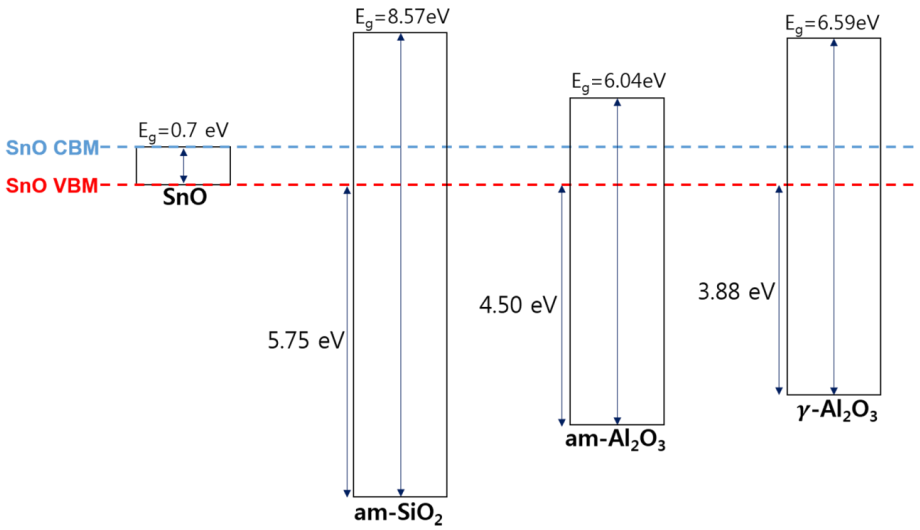


Figure 4.15. Calculated band gap and band alignment of each oxide. Averaged electrostatic potential (AEP) was calculated with respect to the vacuum level in the slab structure using PBE functional, and the position of VBM was calculated in the bulk structure using HSE functional with the optimized fraction α of Fock exchange: α=0.32 for SnO, α=0.45 for SiO_2, and α=0.32 for Al_2O_3. The validity and effectiveness of this calculation approach were reported in the previous literature.

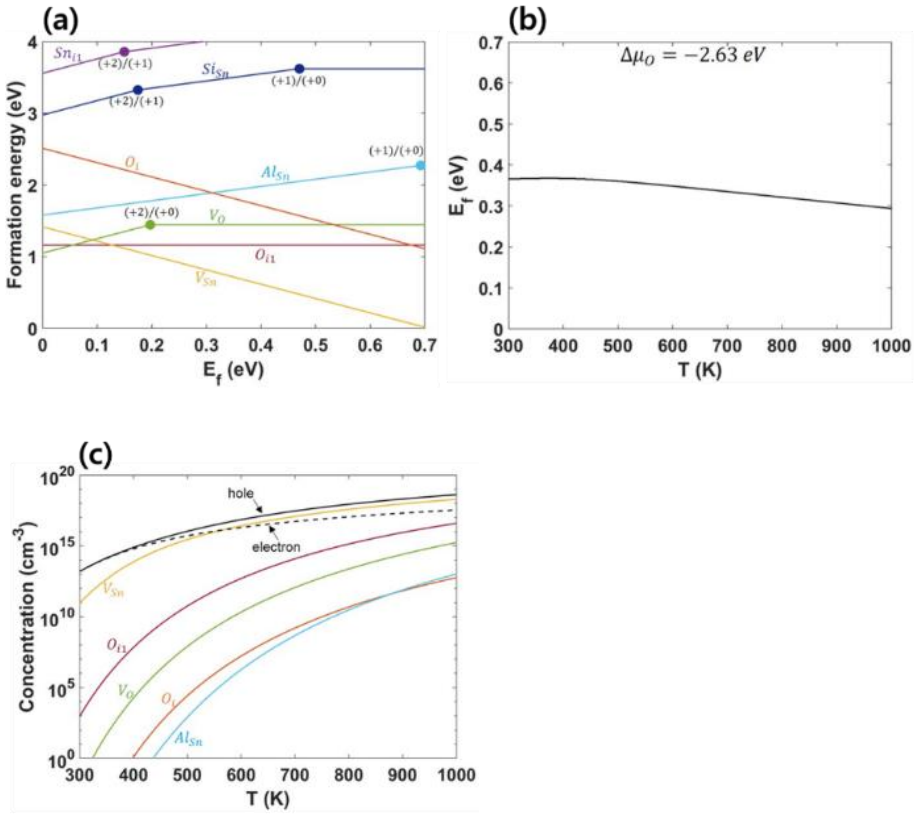


Figure 4.16. (a) Calculated formation energy of defects in SnO, (b) electronic potential satisfying charge neutrality in SnO at the fixed μ_O, and (c) concentration of defects and charge carriers in SnO. Two types of the interstitial site were considered following the previous research: 4-coordinate site denoted as O_i and 5-coordinate site denoted as O_{i1} for oxygen interstitials. Note that interstitial defects generated by cation (Si or Al) diffusion from GI oxides to SnO channel, ex. Al_i and Al_{i1}, were also calculated but the interstitial defects were identified to have higher energy than substitutional defects and not denoted in this figure.

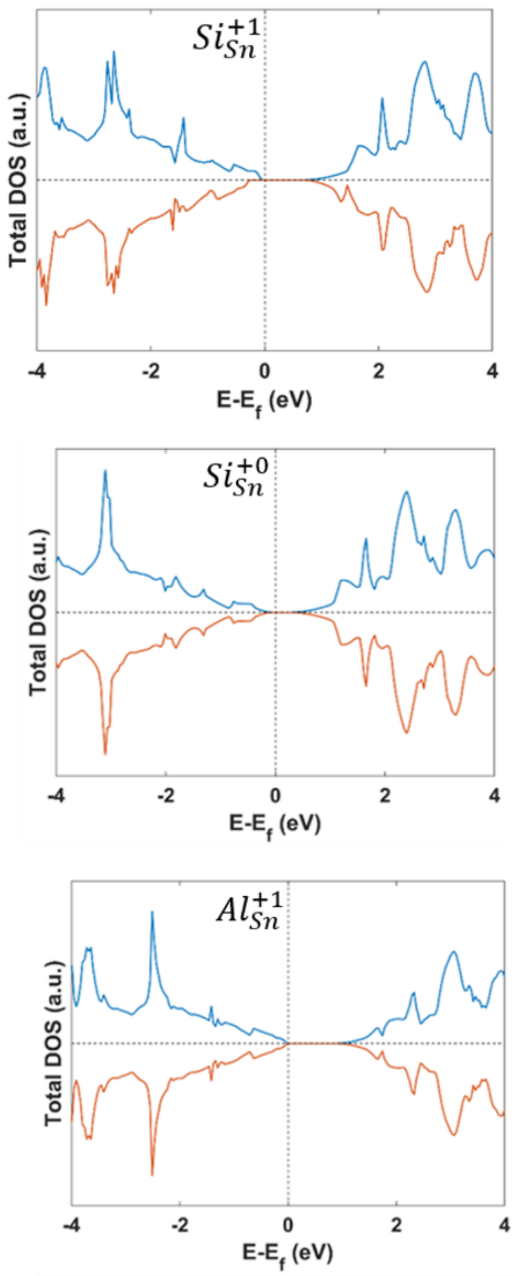


Figure 4.17. Calculated DOSs of substitutional defects generated by cation (Si or Al) diffusion from GI oxides to SnO active layer in the energetically stable charged states.

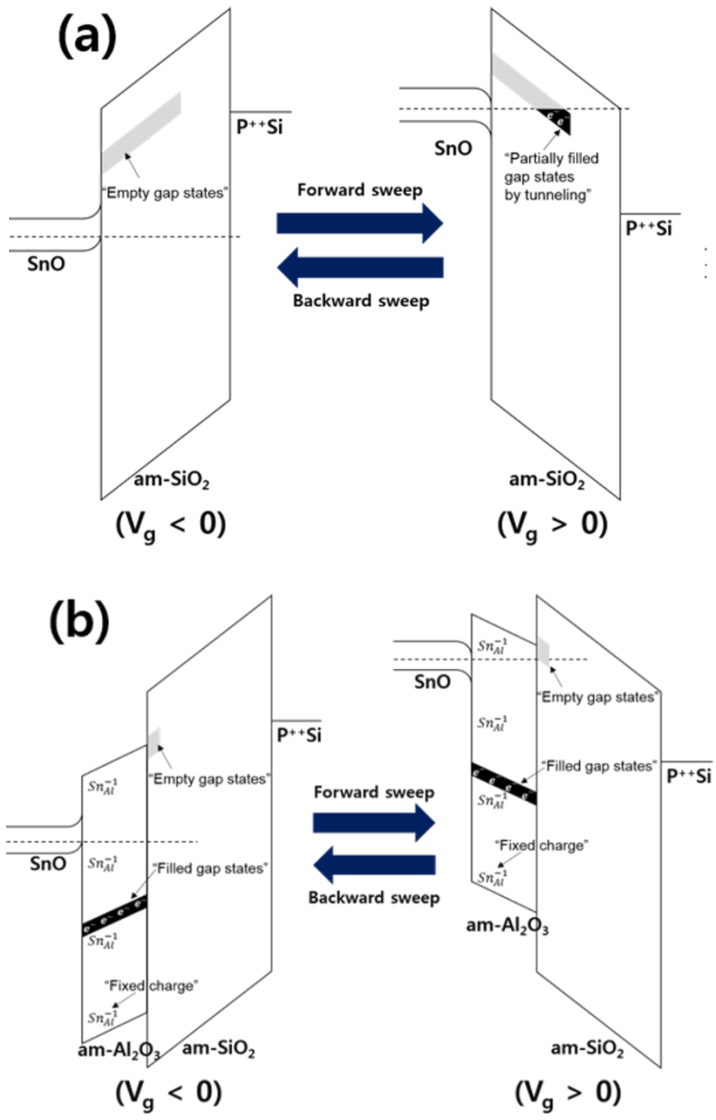


Figure 4.18. Schematic band diagrams of (a) SnO/am-SiO_2/p^{++}Si and (b) SnO/am-Al_2O_3/am-SiO_2/p^{++}Si. Note that the positions of VBM, CBM, and the gap states of defects are aligned according to the band alignment and DOS calculations.

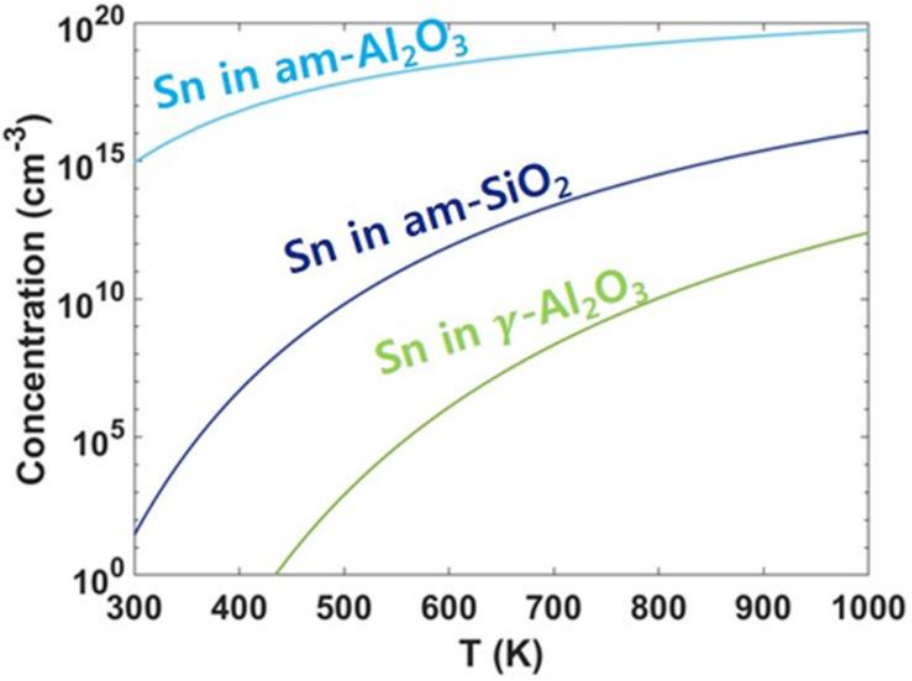


Figure 4.19. Calculated defect concentration of Sn_{Si} in am-SiO_2, Sn_{Al} in am-Al_2O_3, and Sn_{Al} in γ-Al_2O_3 in the electrochemical equilibrium condition without gate bias: E_f=[VBO of each oxide]+[electronic potential satisfying charge neutrality in SnO], and $\mu_{O(SnO)} = \mu_{O(SiO_2)} = \mu_{O(Al_2O_3)} = \frac{1}{2}\mu_{O_2(gas)} - 2.63\ eV$.

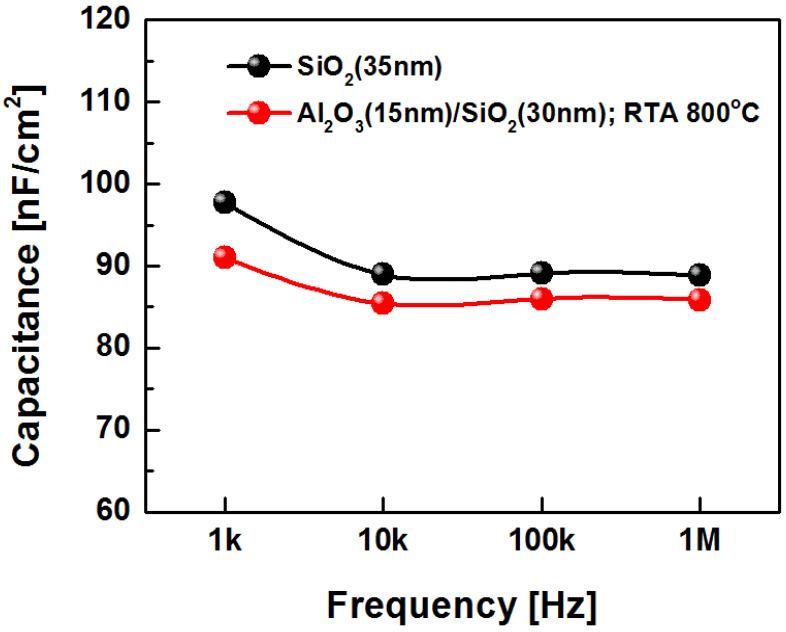


Figure 4.20. Capacitance vs. frequency measured in the metal/dielectric/metal configuration using two different gate dielectrics: One is the SiO_2 (35 nm), and the other is Al_2O_3 (15 nm)/SiO_2 (30 nm). In the cases of the Al_2O_3/SiO_2 gate dielectrics, the films were annealed at 800 ℃ via RTA.

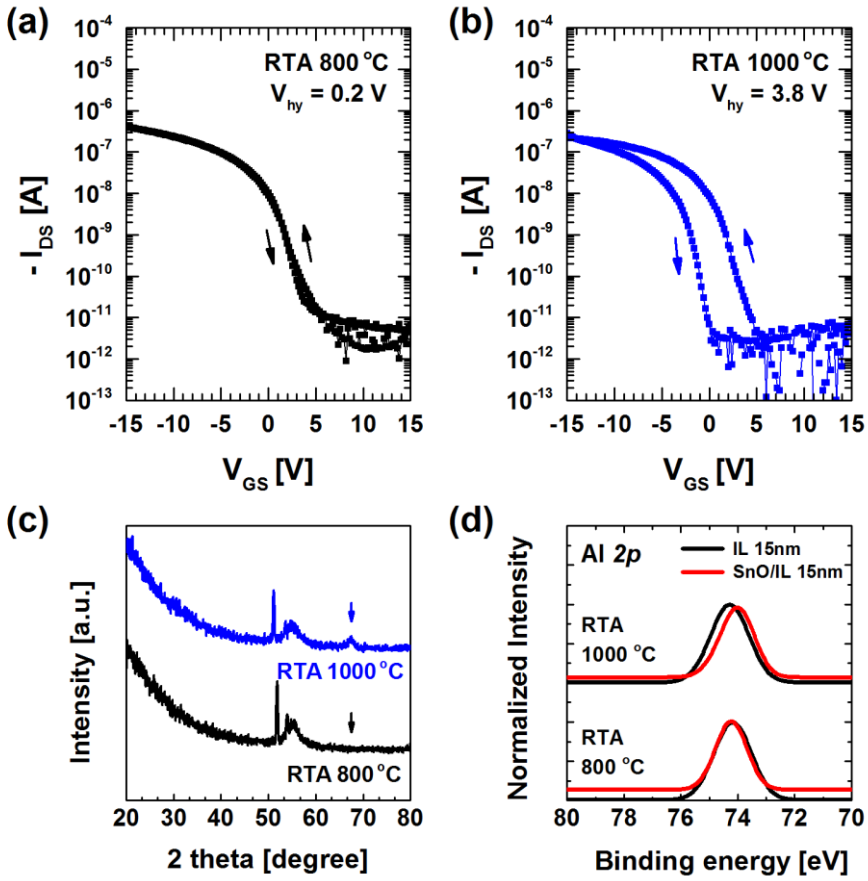


Figure 4.21. Transfer characteristics of the SnO TFT with 15-nm-thick ILs annealed at (a) 800 ℃ and (b) 1000 ℃ via RTA. (c) GAXRD spectra of the 15-nm-thick Al_2O_3 films by RTA temperature. (d) Al *2p* XPS spectra of the Al_2O_3(15 nm)/SiO_2 and SnO(7 nm)/Al_2O_3(15 nm)/SiO_2 samples, in which the Al_2O_3 films were annealed at 800 ℃ (bottom) and 1000 ℃ (top), respectively.

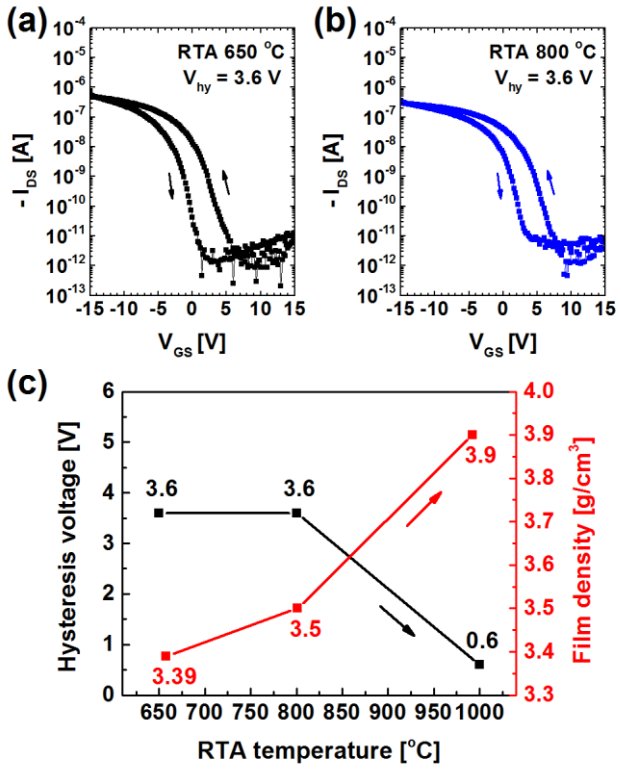


Figure 4.22. Transfer characteristics of the SnO TFT with a 5-nm-thick IL annealed at (a) 650 ℃ and (b) 800 ℃ via RTA. The result of the SnO TFT with an IL annealed at 1000 ℃ was not included in this figure. (c) Hysteresis voltage in the transfer characteristics and Al_2O_3 film density of the 5-nm-thick ILs extracted from XRR fitting as a function of the RTA temperatures from 650 to 1000 ℃.

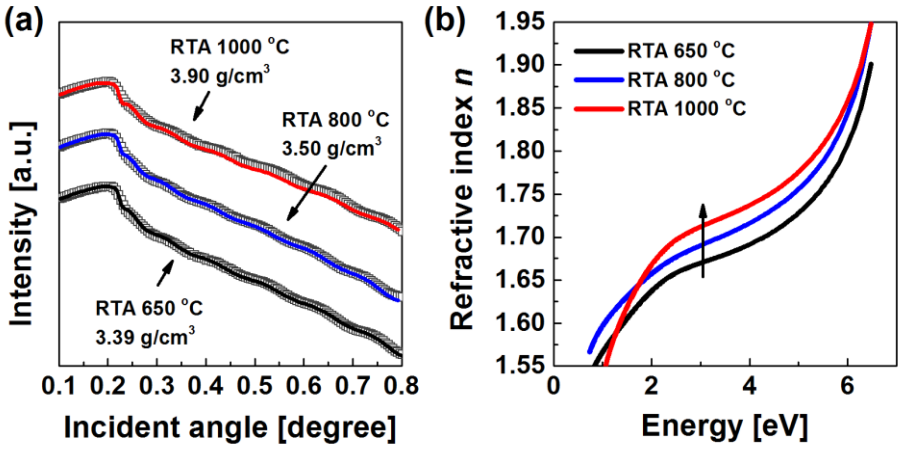


Figure 4.23. (a) Measured XRR (blank dot) for 5nm-thick Al_2O_3 films in comparison to the fitted data (line curves). Annealing temperature and film density resulting from the fit are indicated. (b) Dispersion of the refractive index as extracted from the fit to the SE results of the 5nm-thick Al_2O_3 films to ensure the accuracy of the calculated film density. This reflects the increase of the film density with RTA temperature, which is consistent with the XRR results.

4.3. Bibliography

[1] G. Kresse, J. Furthmuller, *Comput. Mater. Sci.* **1996**, *6*, 15.

[2] G. Kresse, J. Furthmuller, *Phys. Rev. B* **1996**, *54*, 11169.

[3] P. E. Blochl, *Phys. Rev. B* **1994**, *50*, 17953.

[4] G. Kresse, D. Joubert, *Phys. Rev. B* **1999**, *59*, 1758.

[5] J. P. Perdew, K. Burke, M. Ernzerhof, *Phys. Rev. Lett.* **1996**, *77*, 3865.

[6] J. Heyd, G. E. Scuseria, M. Ernzerhof, *J. Chem. Phys.* **2003**, *118*, 8207; **2006**, *124*, 219906.

[7] S. Hwang, Y. Y. Kim, J. H. Lee, D. K. Seo, J. Y. Lee, H. K. Cho, *J. Am. Ceram. Soc.* **2012**, *95*, 324.

[8] J. Um, S. E. Kim, *ECS Solid State Lett.* **2014**, *3*, P94.

[9] W. Xia, H. Wang, X. Zeng, J. Han, J. Zhu, M. Zhou, S. Wu, *CrystEngComm* **2014**, *16*, 6841.

[10] M. Egginger, S. Bauer, R. Schwodiauer, H. Neugebauer, N. S. Sariciftci, *Monatsh. Chem.* **2009**, *140*, 735.

[11] Y. Fujisaki, Y. Inoue, T. Kurika, S. Tokito, H. Fujikake, H. Kikuchi, *Jpn. J. Appl. Phys.* **2004**, *43*, 372.

[12] C. D. Dimitrakopoulos, A. R. Brown, A. Pomp, *J. Appl. Phys.* **1996**,

80, 2501.

[13] S. Jakschik, U. Schroeder, T. Hecht, D. Krueger, G. Dollinger, A. Bergmaier, C. Luhmann, J. W. Bartha, *Appl. Surf. Sci.* **2003**, *211*, 352.

[14] S. Migita, J. W. Park, T. Yasuda, M. Nishizawa, R. Kuse, T. Nabatame, A. Toriumi, in *Extended Abstracts of the 2003 Int. Conf. Solid State Devices Materials (SSDM)*, IEEE, Piscataway, NJ **2003**, p. 470.

[15] S. Jakschik, U. Schroeder, T. Hecht, M. Gutsche, H. Seidl, J. W. Bartha, *Thin Solid Films* **2003**, *425*, 216.

[16] W.-H. Lee, Y.-L. Kuo, H.-J. Huang, C. Lee, *Mater. Chem. Phys.* **2004**, *85*, 444.

[17] K.-C. Park, K.-B. Kim, I. J. M. M. Raaijmakers, K. Ngan, *J. Appl. Phys.* **1996**, *80*, 5674.

5. Examination of Abnormal Electrical Properties in SnO devices with Al_2O_3 interfacial layer

5.1. Effects of mobile oxygen vacancies within Al_2O_3 film on gate voltage dependence

5.1.1. Introduction

SnO-based p-type TFTs have received considerable attention recently for use in electronic circuits, sensors, and optoelectronic and memory devices due to its high hole mobility [1–7]. The development of a p-type TFT is essential for fabricating the complementary TFT circuits by combining it with the n-type TFT, which generally outperforms the p-type TFT with a far higher carrier mobility and on/off current ratio. In part 4, one of the most severe problems of the SnO-based p-type TFT, the involvement of a large V_{hy}, could be significantly mitigated by interposing an optimally annealed thin Al_2O_3 layer between the SiO_2 GI and the SnO channel layer [8]. The origin of the involvement of a large V_{hy} for the SiO_2/SnO structure was the substantial diffusion of Sn into the SiO_2, which forms a large density of slow traps. The Al_2O_3 layer efficiently blocks such an adverse diffusion. This work further exploited the effects of the Al_2O_3 barrier layer on the device performance of the

p-type SnO TFT, focusing on the V_{th} instability. V_{th} instability is one of the crucial issues of the TFT-based electronic circuits, which must be entirely suppressed to operate the circuits stably.

The origin of the hysteresis and instability of the transfer characteristics under the gate bias stress has been studied by several groups [8–12]. It has been suggested that the interface between the SnO channel and the GI introduces charge traps and causes electrical instabilities [8–12]. Nevertheless, the changes in the V_{hy} and V_{th} shifts depending on the sweep range or the rate of V_{GS} have not been evaluated carefully for the p-type SnO TFTs. In this work, the SnO TFTs with two different gate dielectric layers, SiO_2 and Al_2O_3/SiO_2, were fabricated, and the changes in the V_{hy} and V_{th} shifts for different V_{GS} stress conditions were examined to understand the instability of these devices.

5.1.2. Experimental procedure

To fabricate SnO TFTs with a bottom-gated structure, heavily doped p-type silicon was used as the gate electrode, and 35-nm-thick thermal SiO_2 was used as the GI (device S). For the other case, a 15-nm-thick Al_2O_3 layer was grown on the 30-nm-thick thermal SiO_2 layer through ALD at a substrate temperature of 200 ^oC, using $Al(CH_3)_3$ and H_2O as the Al precursor and oxygen source, respectively. RTA at 800 ^oC was carried out under an O_2 atmosphere to make the Al_2O_3 layer denser (device AS). Here, the thicknesses of the two dielectric layers were chosen to make the capacitance equivalent thickness of the GI in

the two types of devices similar. Then a 7-nm-thick SnO thin film was deposited as a channel layer using the same ALD tool at a substrate temperature of 200 ^{o}C. $Sn(dmamp)_2$ and H_2O were used as the Sn precursor and oxygen source, respectively.

A channel region with a width of 20 μm and a length of 5 μm was defined via the conventional photolithography and wet etching. An 80-nm-thick Au layer was deposited as the source/drain electrode via sputtering, and was patterned through the lift-off method. For the passivation layer, a 15-nm-thick Al_2O_3 film was deposited on the fabricated TFT via ALD at 150 ^{o}C, and was then annealed in N_2 at 250 ^{o}C for 3 minutes. The electrical characteristics of the SnO TFTs were evaluated at room temperature using a HP4155 semiconductor parameter analyzer in a dark box.

The C-V characteristic was measured in Au/SnO/dielectric/heavily doped p-type Si configuration with the two different dielectric stacks using a HP4194A impedance analyzer. The dielectric constants of SiO_2 and Al_2O_3 were estimated ~3.9 and ~8.6, respectively, and the capacitance equivalent thickness was calculated to be 38.8 nm and 36.8 nm for SnO/SiO_2 and $SnO/Al_2O_3/SiO_2$ devices.

5.1.3. Results and discussion

Figure 5.1a and b show the schematic diagrams of devices S and AS, respectively. **Figure 5.1**c presents the transfer curves (I_{DS}, vs. V_{GS}) of both

devices at a V_{DS}=–1 V measured in both the FW (from negative to positive) and BW (from positive to negative) sweeps in V_{GS}. The V_{th} was determined from the linear fitting of an $I_{DS}/g_m^{0.5}$-V_{GS} plot at a V_{DS} of –1 V, where g_m means the transconductance, which minimizes the influence of parasitic series resistances and mobility degradation [13,14]. A V_{th} shift between FW sweep ($V_{th,\,FW}$) and BW sweep ($V_{th,\,BW}$) was designated as the V_{hy} ($V_{th,\,BW}$-$V_{th,\,FW}$). As shown in **Figure 5.1**c, device S showed a large CC) hysteresis (V_{hy}=4.0 V) with a ~10^5 current ratio between the on and off states ($I_{on/off}$). In contrast, device AS exhibited 20 times smaller hysteresis (V_{hy}=0.2 V) without a significant loss of device properties (μ_{FE}=1.8 $cm^2/V{\cdot}s$, SS=1.0 V/dec., and I_{on}/I_{off}=6.3×10^4) compared to device S. To understand this improvement, the gate-induced electrical instability in the transfer characteristics of both devices was examined.

Figure 5.2 shows the variations in V_{th} and V_{hy}, depending on the sweep range of V_{GS}. Here, the V_{GS} SR was 1.43 V/sec, whose effects are discussed later. For such tests, the maximum negative voltage of V_{GS} sweep ($-V_{GS,\,max}$=–15 V, **Figure 5.2**a) and the maximum positive voltage of V_{GS} sweep ($+V_{GS,\,max}$=+15 V, **Figure 5.2**b) were fixed. The transfer curves under each sweep condition can be found in **Figure 5.3** and **5.4**. The changes in the V_{hy} calculated from **Figure 5.2**a and b are shown in **Figure 5.2**c, where the V_{hy} values higher and lower than 0 V represent CCW and clockwise (CW) hysteresis, respectively. As shown in **Figure 5.5**, the SS of the two devices also depended on the V_{GS} range, indicating that the N_{it}, as well as the N_{bt}, was affected by V_{GS} range. In the

previous work, however, it was demonstrated that the hysteresis behavior of SnO TFTs was mainly determined by the N_{bt} rather than N_{it} [8]. Therefore, to calculate V_{hy}, only the V_{th} shift induced by N_{bt} was considered, excluding the effect of SS.

As shown in **Figure 5.2**a, only the $V_{th,\,BW}$ was dependent on the $+V_{GS,\,max}$ in both devices, suggesting that the device state during the BW sweep is determined by the $+V_{GS,\,max}$. As the $+V_{GS,\,max}$ increased, a significant shift of the $V_{th,\,BW}$ was observed only for device S, while only a slight shift was shown for device AS. In contrast, the $V_{th,\,FW}$ of the two devices were almost independent of the $+V_{GS,\,max}$, suggesting that the device states during the FW sweep were solely determined by the $-V_{GS,\,max}$, which was –15 V in this case.

Similar but also distinctive variations could be found under the varying $-V_{GS,\,max}$ conditions, as shown in **Figure 5.2**b. As the absolute value of $-V_{GS,\,max}$ increased, $V_{th,\,FW}$ substantially shifted into a negative value for device S. Interestingly, the $V_{th,\,BW}$ also slightly shifted in the negative direction even with the given $+V_{GS,\,max}$ value (+15 V). This performance might have been due to the incomplete elimination of trapped carriers (hole), which induced the significant negative shift of the $V_{th,\,FW}$ during the repeated transfer measurements. Device AS showed entirely different behaviors under identical test conditions. The $V_{th,\,FW}$ initially slightly shifted in the positive voltage direction (up to –25 V), and then followed the trend of device S at –30 V. As the $V_{th,\,FW}$ shift was well suppressed, the $V_{th,\,BW}$ did not vary substantially for the given $+V_{GS,\,max}$ value

(+15 V).

These V_{th} shifts and hysteresis-related phenomena originated from charge trapping/de-trapping at or near the channel/dielectric interfaces and within the GIs [15]. The traps responsible for such hysteretic behavior have relatively deep levels, making the time constant for the detrapping longer compared with that of the I_{DS}-V_{GS} sweep. As such, the transfer curves became hysteretic.

The general positive shift of the $V_{th,\ BW}$ in **Figure 5.2**a suggests electron trapping at the SnO/SiO_2 (SnO/Al_2O_3/SiO_2) interface, which occurred mostly under the sufficiently high +V_{GS} condition. Also, the general negative shift of the $V_{th,\ FW}$ in **Figure 5.2**b suggests hole trapping at the SnO/SiO_2 (SnO/Al_2O_3/SiO_2) interface, which occurred mostly under the sufficiently (absolutely) high –V_{GS} condition. The much larger $V_{th,\ BW}$ ($V_{th,\ FW}$) shift of device S compared with device AS in **Figure 5.2**a (**Figure 5.2**b) suggests that the former has a much higher N_{bt} than the latter, which is consistent with the previous report [8]. The generally smaller magnitude of the positive shift of the $V_{th,\ BW}$ (max ~ +4 V) compared with the negative shift of the $V_{th,\ FW}$ (max ~ –13 V) of device S indicated that the electron trapping at the interface was ~1/3 of the hole trapping. Such a discrepancy could have been induced either by the lower density of electron trap sites compared with that of the hole traps or the lower available electron density compared with the hole density under the maximum positive and negative V_{GS} conditions, respectively. As the SnO channel is of a p-type nature and the source/drain contacts (Au) must have a

higher barrier for the electron injection than that for the hole, the latter might have a higher relevance. **Figure 5.2**c summarizes the variations in the V_{hy} under different $V_{GS,\ max}$ conditions.

These mechanisms, however, cannot explain the peculiar behavior of device AS, in which the $V_{th,\ FW}$ positively shifted up to –25 V of the $V_{GS,\ max}$. If the same hole trapping mechanism were applied, the $V_{th,\ FW}$ must have shifted in the negative voltage direction.

To clarify the mechanism of the V_{th} shift and V_{hy} change for the negative V_{GS} observed in **Figure 5.2**, the dependence of the $V_{th,\ FW}$ on the V_{GS} SR was analyzed, as shown in **Figure 5.6**a. The SR of V_{GS} was defined as the V_{GS} step over the integration time. These data revealed that the charge trapping and detrapping are dynamic processes depending on the SR. For the case of device S with the $V_{GS,\ max}$ of –15 V (black square symbol), the $V_{th,\ FW}$ was ~–4.5 V when the SR was 0.36 V/s, which decreased to ~-3.4 V when the SR increased to 14.3 V/s. As discussed above, the negative value of $V_{th,\ FW}$ could be ascribed to the hole trapping under the highly negative V_{GS} condition. During the V_{GS} sweep into the positive region, a part of the trapped holes was detrapped, and the $V_{th,\ FW}$ became less negative. Such a trend became more evident as the SR increased. When the SR was small, the time during which the trapped holes were retained in the negative bias region, especially before the $V_{th,\ FW}$ was reached, was longer, and the $V_{th,\ FW}$ remained a highly negative value.

Device AS, however, showed a trend opposite that shown by device S under

the identical condition of $V_{GS,\,max}$ of –15 V (red circle symbol). This device had a pristine V_{th} of ~0 V, so the $V_{th,\,FW}$ of ~1.0 V for the case of SR of 0.36 V/s (the V_{th} had shifted into the positive value direction) suggests that an opposite charge effect had occurred. As a negative V_{GS} cannot induce electron trapping at the channel/Al_2O_3 interface, the only probable mechanism is the rearrangement of the ionic charges in the Al_2O_3 film. The most probable charge defect in the Al_2O_3 film must be the doubly ionized oxygen vacancy ($V_O^{\cdot\cdot}$, which follows the Kröger-Vink notation, where the "$^{\cdot\cdot}$" denotes the effective positive charge) [16]. Under the application of V_{GS} of –15 V, part of the $V_O^{\cdot\cdot}$'s was dragged towards the Al_2O_3/SiO_2 interface, which decreased the positive charge density near the channel/Al_2O_3 interface, making the $V_{th,\,FW}$ shift towards a positive value. During the forward sweep of the V_{GS}, a certain portion of the dragged $V_O^{\cdot\cdot}$'s could be released from the Al_2O_3/SiO_2 interface, which decreased the $V_{th,\,FW}$ shift. As the SR increased, the time during which the dragged $V_O^{\cdot\cdot}$'s were retained at the Al_2O_3/SiO_2 interface decreased, and greater recovery of the original $V_{th,\,FW}$ could be achieved.

Such a $V_O^{\cdot\cdot}$-related mechanism, however, could not explain the test results when the $V_{GS,\,max}$ further increased to –25 V, where the $V_{th,\,FW}$ of device AS was as high as ~2.4 V at the SR of 0.71 V/s, which slightly increased to ~2.7 V as the SR increased to 14.3 V/s (blue triangle symbol). As mentioned above, such a large shift of the $V_{th,\,FW}$ could not have been induced by the electron trapping because the V_{GS} remained in the negative-bias range. Thus, the only feasible

mechanism is again the redistribution of the $V_O^{\cdot\cdot}$'s within the Al_2O_3 layer, with a higher degree of their migration towards the Al_2O_3/SiO_2 interface. If the migrated $V_O^{\cdot\cdot}$'s moved back towards the channel/Al_2O_3 interface during the forward sweep of the V_{GS}, it should have shown a decrease in the $V_{th,\,FW}$, as in the case of $V_{GS,\,max}$ of –15 V. Therefore, it should be assumed that hole trapping also occurred under such a highly negative $V_{GS,\,max}$ condition, which could be released during the forward V_{GS} sweep. The fact that there was no decrease in the $V_{th,\,FW}$ with the increasing SR implied that the migrated $V_O^{\cdot\cdot}$'s did not relax back to their original configuration during the forward sweep of the V_{GS} at least up to $V_{th,\,FW}$. Perhaps they were trapped at the Al_2O_3/SiO_2 interface.

Such $V_O^{\cdot\cdot}$-related $V_{th,\,FW}$ behavior could explain the abnormal $V_{th,\,FW}$ behavior of device AS shown in **Figure 5.2**b at the $V_{GS,\,max}$ values ranging from –10 to –30 V. At the $V_{GS,\,max}$ of –10 V, both the $V_O^{\cdot\cdot}$ migration and the hole trapping were not severe, and as such, the $V_{th,\,FW}$ remained at ~0 V. As the $V_{GS,\,max}$ increased up to –25 V, the $V_O^{\cdot\cdot}$ migration dominated the $V_{th,\,FW}$ variation, which increased it to ~2.5 V. When the $V_{GS,\,max}$ further increased up to –30 V, additional hole trapping occurred, which decreased the $V_{th,\,FW}$, while a further increase in $V_O^{\cdot\cdot}$ migration did not occur perhaps because all the available $V_O^{\cdot\cdot}$'s had already migrated.

The involvement of two types of charge effects in device AS could also be identified by the stress time-dependent V_{th} variation (ΔV_{th}=$V_{th,\,FW}$ after stress - $V_{th,\,FW}$ fresh), as shown in **Figure 5.6**b, where the $V_{GS,\,stress}$ of –15 V (black

square and red circle symbol) and –25 V (blue triangle symbol) was applied to the two types of devices with the indicated stress time. The transfer curves under negative bias stress (NBS) can be found in **Figure 5.7**. Device S showed a monotonous decrease (absolute increase) in ΔV_{th} down to ~–1.4 V after 100 s, suggesting hole trapping (black square symbol) [9–12]. In contrast, device AS showed an initial increase in ΔV_{th} up to ~0.8 V at the stress time of 10 s with the $V_{GS,\ stress}$ of –15 V, and a decrease in it afterward (red circle symbol). This behavior suggested that the initial change of the ΔV_{th} was dominated by the $V_O^{\cdot\cdot}$ migration up to 10 s, which was then followed by hole trapping. Therefore, in this case, the degree of hole trapping could be estimated by the variation in the ΔV_{th} from the maximum to the minimum values, which was ~–1.0 V. From the trend of the red line, the ΔV_{th} of device AS after the stress time of 110 s would not be largely different from the value of 100s. This value is smaller than the corresponding value of device S (–1.4 V), suggesting that the hole trapping was less severe in device AS. Nonetheless, this behavior elucidated that the much smaller ΔV_{th} of 0.25 V of device AS compared with the –1.4 V value of device S after the 100 s stress time did not necessarily mean that the hole trapping of the former was 5.6 times smaller than that of the latter. Taking into consideration of the flat band voltage from the C-V measurements, the overall effective oxide electric field (E_{ox}) at V_{GS} = –15 V was evaluated to be –3.09 MV/cm and –4.26 MV/cm for device S and AS, respectively. The local E_{ox} for Al_2O_3 and SiO_2 layers in the AS device were calculated to be –1.93

MV/cm and –4.27 MV/cm, respectively. Although the overall E_{ox} was higher for the case of the AS device, the decreased E_{ox} across the Al_2O_3 layer, due to its higher *k* value, helped to improve the reliability. This effect is combined with the strong counteracting effect between hole trapping and $V_O^{\cdot\cdot}$ migration, making the overall reliability of $SnO/Al_2O_3/SiO_2$ device superior to the other.

When $V_{GS,\ stress}$ was –25 V, the stress time-dependent V_{th} variation due to the mobile charge and hole trapping effects became more prominent (blue triangle symbol). The device AS showed an abrupt increase in ΔV_{th} up to 1.95 V at a shorter stress time of 1 s (see the right panel of **Figure 5.6**b, which is an enlarged image of the dashed portion of the main graph), and then an abrupt decrease in it to –6.15 V after 100 s. As the $V_{GS,\ stress}$ became as high as –25 V, the $V_O^{\cdot\cdot}$ migration in the Al_2O_3 layer at the shorter stress time increased, whereas, at the later times, the even more significant hole trapping at the interface dominated the V_{th} variation. The involvement of mobile charge defects, however, could induce different types of adverse effects in device AS, and a thorough investigation of this will be the topic of the subsequent research.

One of the aforementioned adverse effects can be identified in **Figure 5.8**. The presence of ion migration in the Al_2O_3 layer was supported by the measurement of the displacement current (I_{GS}) through the GI under V_{GS} stress. It was known that the effect of ion migration in the electric field is similar to that of ferroelectric polarization, which was reflected in the displacement current [15,17–20]. As shown in **Figure 5.8**a, for device S, I_{GS} exhibited only

the current change due to capacitive charging when V_{GS} was applied. When the SR increased, the displacive I_{GS} showed a marginal increase, but it was still one order of magnitude smaller compared with that of device AS, as shown in **Figure 5.8**b. For the case of device AS, the displacive I_{GS} was one order of magnitude higher than that of device S for all the SRs. The I_{GS}-V_{GS} curves with the different V_{DS} values (**Figure 5.9**) did not show notable change, which suggested that the interface properties between channel and Au contact did not affect the displacement characteristics. As a result, the displacement characteristics were mainly determined by the dielectric properties, and such a large I_{GS} must be related to the field-induced migration of the $V_O^{\cdot\cdot}$'s in the Al_2O_3 layer. The possible influence of such high I_{GS} should be further investigated, especially under the pulse-type device operation and combined circuitry, such as the inverter and the ring oscillator.

5.1.4. Summary

In summary, the gate-induced electrical instability of the p-type SnO TFTs with SiO_2 and Al_2O_3/SiO_2 gate dielectric layers was evaluated in this study. The insertion of an Al_2O_3 layer between the SnO and SiO_2 layers reduced the V_{hy} and V_{th} shifts for both the positive and negative V_{GS}. The former was due to the suppression of electron trapping at the channel/dielectric interface, which is attributed to the barrier properties of the Al_2O_3 layer. The latter was due to the counteracting effect between the hole trapping at the channel/dielectric

interface and the oxygen vacancy migration in the Al_2O_3 film, which was highly dependent on the sweep range and the rate of negative V_{GS}. The possible influence of the higher ionic-charge effect within the Al_2O_3 layer on the device performance must be further scrutinized. Although the insertion of an Al_2O_3 layer with a mobile ion is beneficial for reducing the V_{hy} and V_{th} shifts of SnO TFTs, the major contribution to the electrical instability for negative VGS still resulted from the hole trapping. Therefore, it is necessary to improve the channel/dielectric interface and to investigate the transient effects of hole trapping/de-trapping to completely eliminate the instability problems of SnO TFTs.

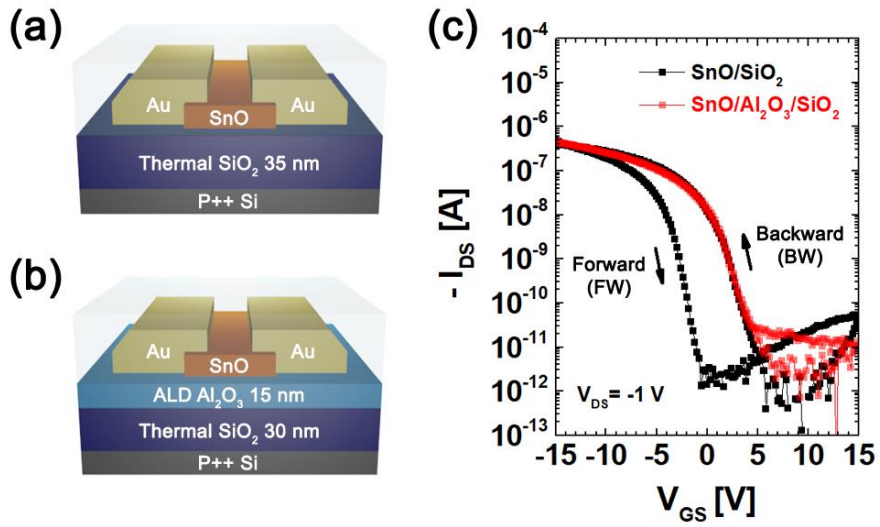


Figure 5.1. Schematic diagrams of the p-type SnO TFTs with (a) SiO_2 and (b) Al_2O_3/SiO_2 gate dielectric layers. (c) The I_{DS}-V_{GS} characteristics measured in the FW and BW sweeps for both the (a) and (b) devices.

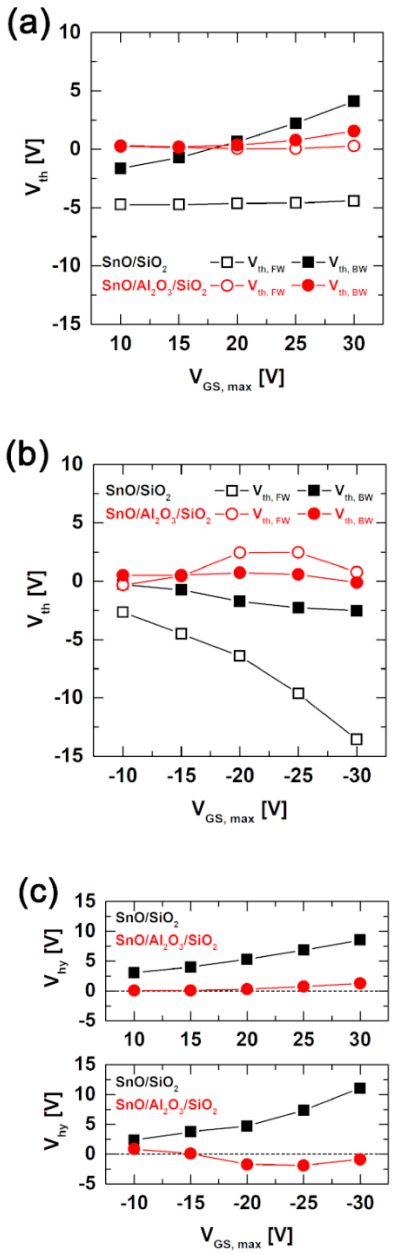


Figure 5.2. Variations in V_{th} as a function of the sweep range of the (a) positive V_{GS} with a fixed $-V_{GS, max}$ (–15 V), and of the (b) negative V_{GS} with a fixed $+V_{GS, max}$ (+15 V). (c) Calculated V_{hy} from the data shown in (a) and (b) for each device.

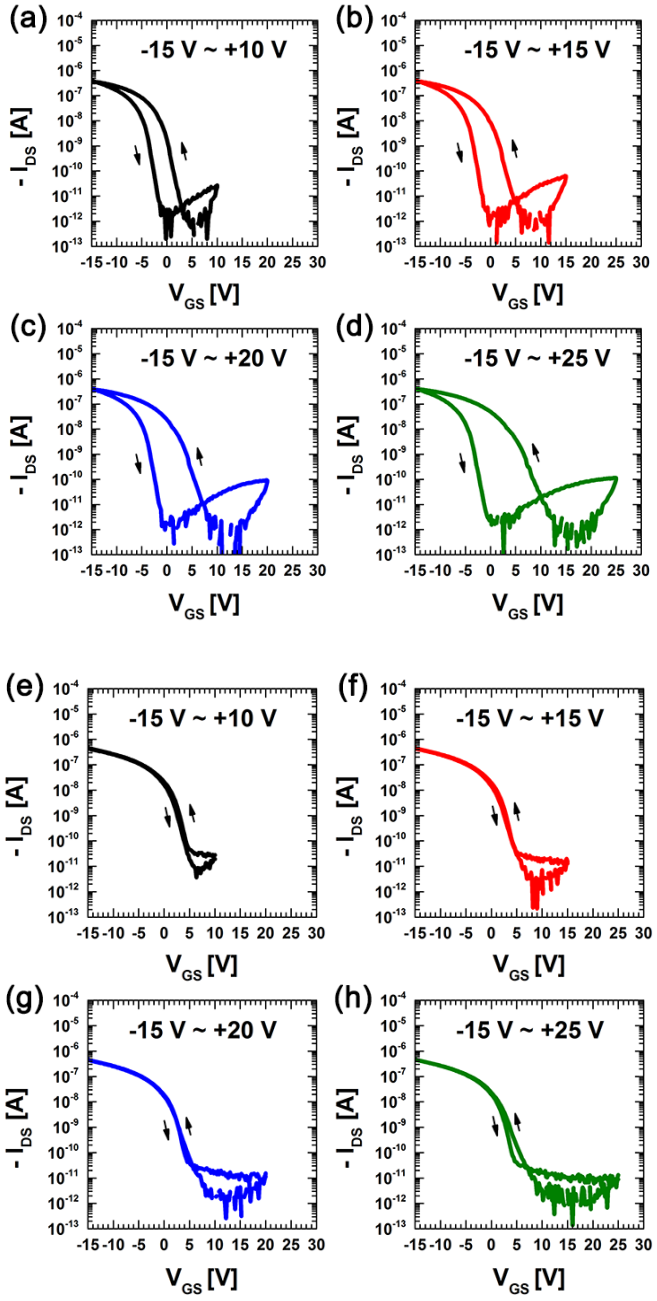


Figure 5.3. Transfer characteristics of SnO TFTs with (a–d) SiO_2 and (e–h) Al_2O_3/SiO_2 gate dielectric layers, at drain voltage (V_{DS})= –1 V, with the changes of the sweep range of the positive gate voltage (V_{GS}). The sweep range of the negative V_{GS} was fixed at –15 V.

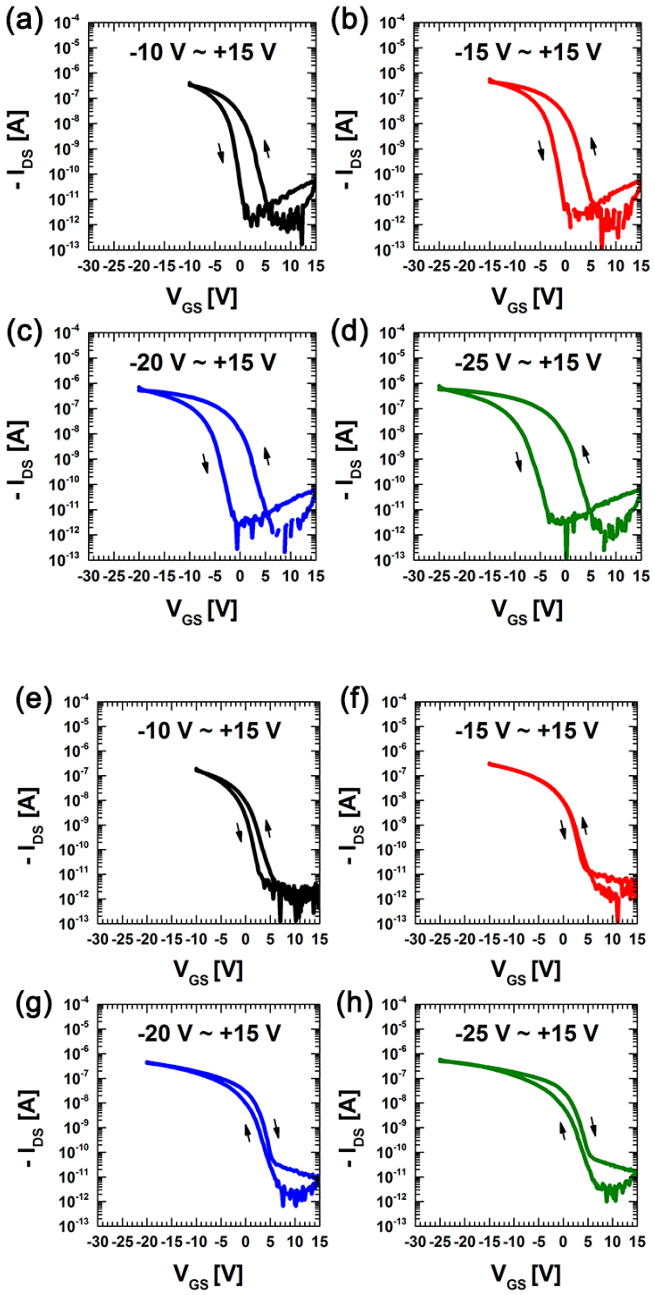


Figure 5.4. Transfer characteristics of SnO TFTs with (a–d) SiO_2 and (e–h) Al_2O_3/SiO_2 gate dielectric layers, at V_{DS}= –1 V, with the changes of the sweep range of the negative V_{GS}. The sweep range of the positive V_{GS} was fixed at +15 V.

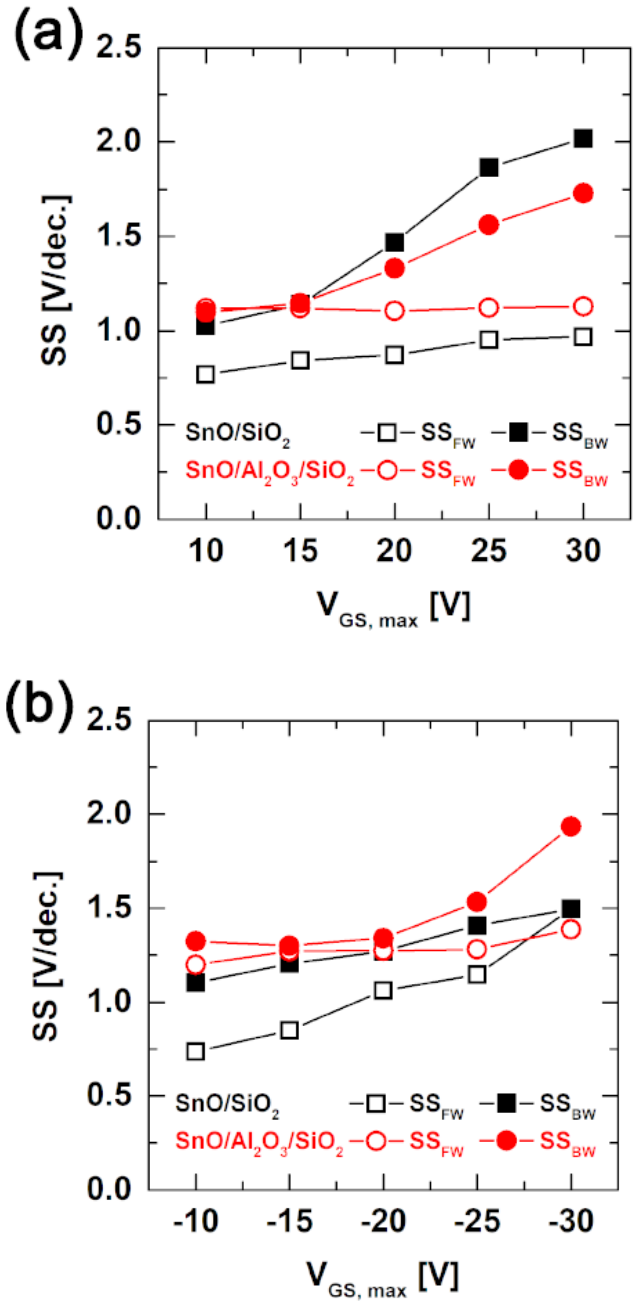


Figure 5.5. Variations in the subthreshold swing (SS) as a function of the sweep range of the (a) positive V_{GS} with a fixed $-V_{GS,\,max}$ (–15 V), and of the (b) negative V_{GS} with a fixed $+V_{GS,\,max}$ (+15 V).

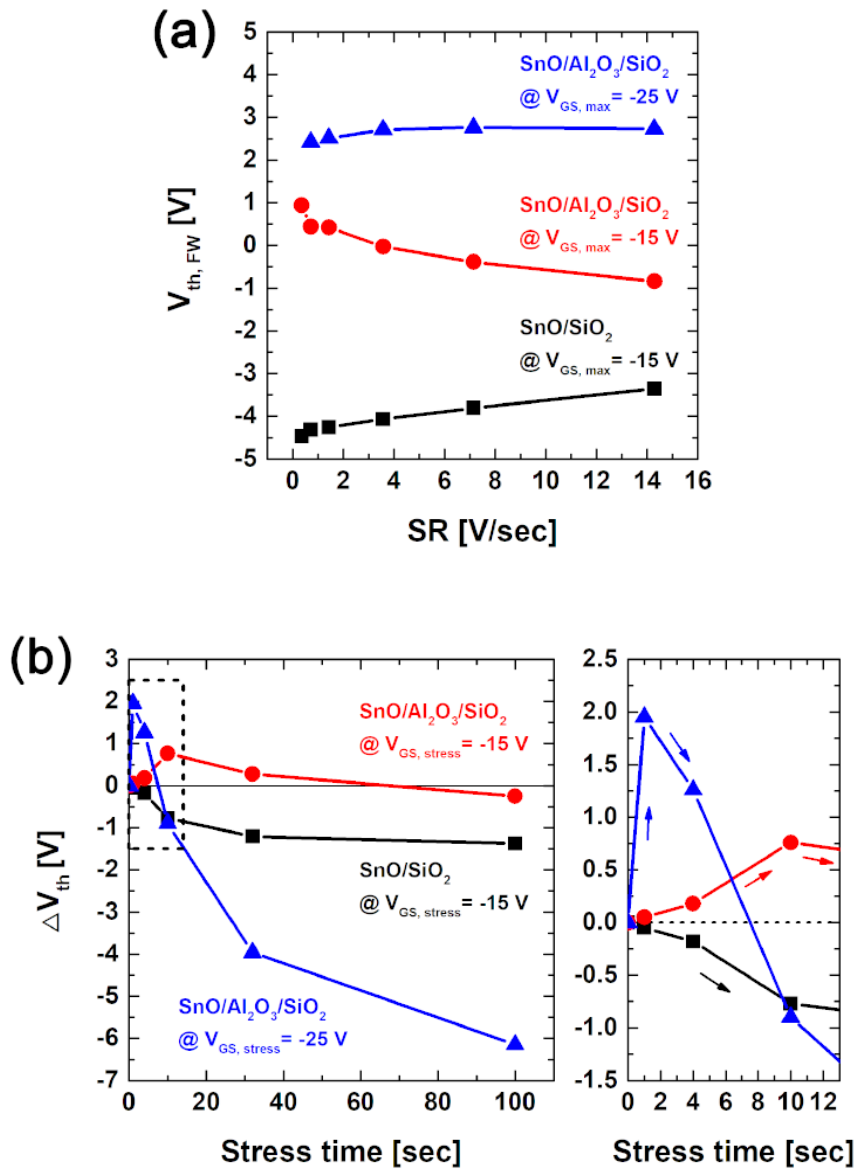


Figure 5.6. (a) Plot of $V_{th,\,FW}$ as a function of V_{GS} SR with a fixed $+V_{GS,\,max}$ (+15 V). (b) V_{th} shift of two stacks as a function of stress time. Here, the V_{GS} was maintained at –15 V (black square, red dot) and –25 V (blue triangle), respectively, while the source and drain were grounded.

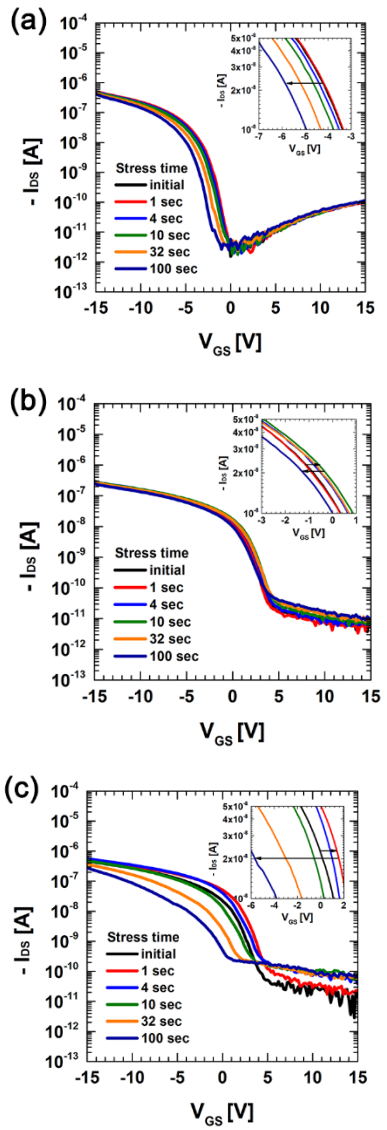


Figure 5.7. Evolution of the transfer characteristics for SnO TFTs with (a) SiO_2 and (b, c) Al_2O_3/SiO_2 gate dielectric layers as a function of the negative bias stress (NBS) time. Here, the V_{GS} was maintained at –15 V for (a) and (b), and –25 V for (c), while the source and drain were grounded. The insets in (a–c) show an enlarged view of the transfer curve, and arrows indicate the direction of movement of the curve.

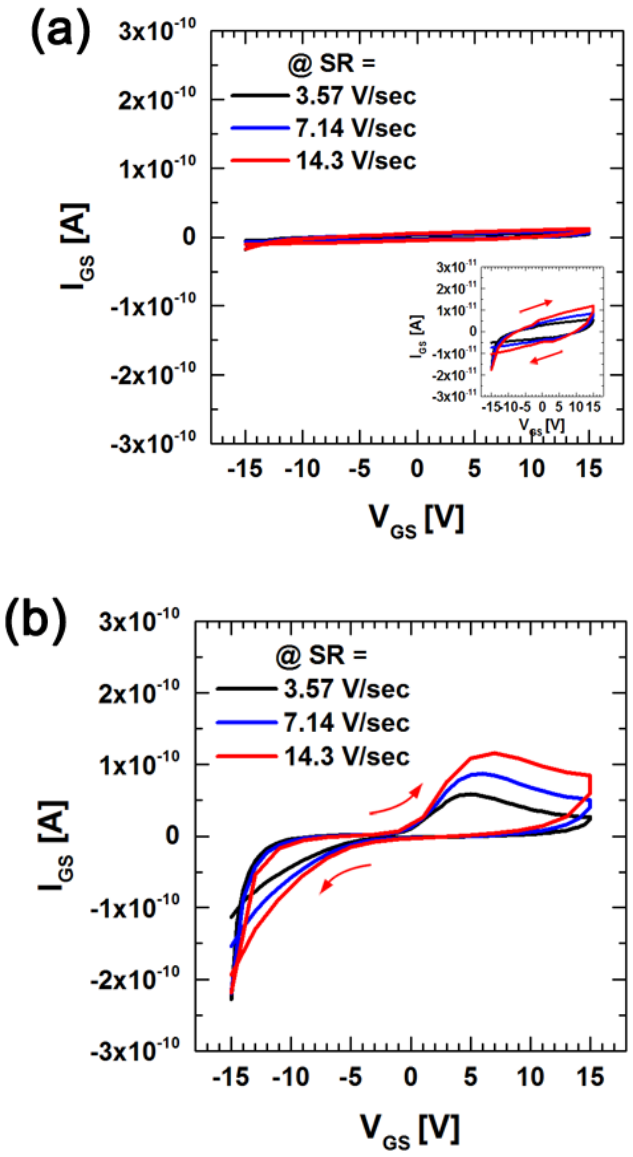


Figure 5.8. Displacement current (I_{GS}) between the gate and a grounded source electrode vs. the applied V_{GS} through the (a) SnO/SiO_2 and (b) $SnO/Al_2O_3/SiO_2$ stacks with different V_{GS} SRs. The inset in (a) shows an enlarged view of the curve, and the arrows show the direction of the curves according to the V_{GS} sweep.

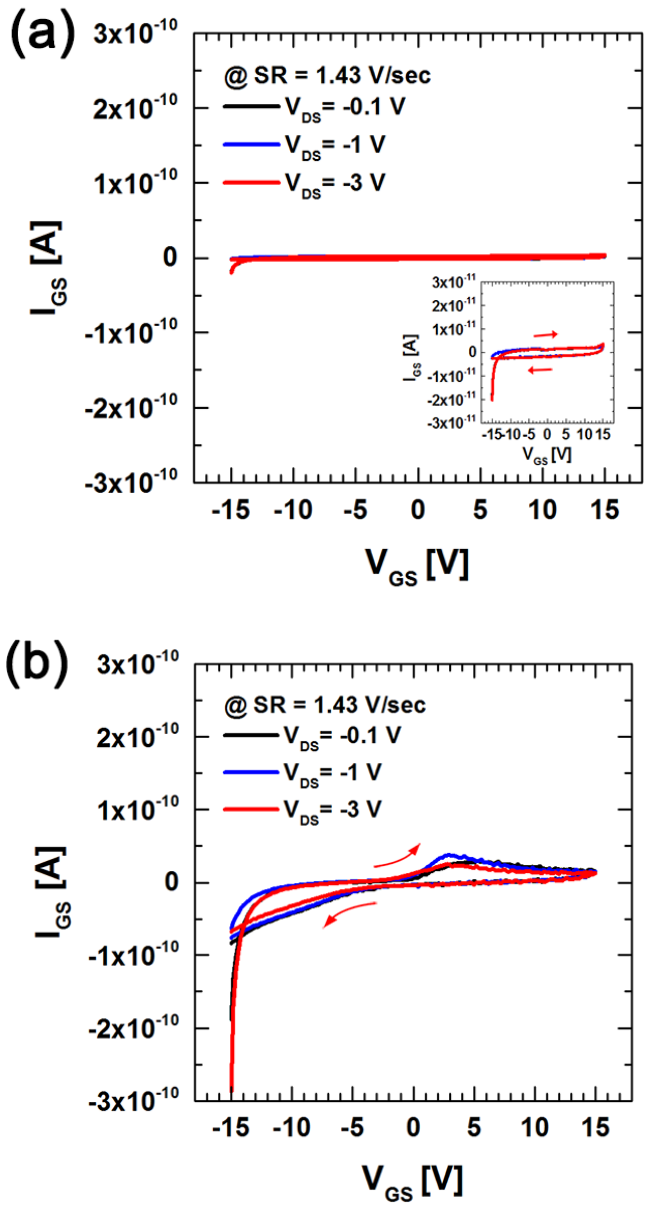


Figure 5.9. Displacement current (I_{GS}) between the gate and a grounded source electrode vs. the applied V_{GS} through the (a) SnO/SiO_2 and (b) $SnO/Al_2O_3/SiO_2$ stacks with different V_{DS}. The arrows show the direction of the curves according to the V_{GS} sweep.

5.2. Effects of mobile oxygen vacancies within Al_2O_3 film on gate current and capacitance characteristics

5.2.1. Introduction

Reports of mobile ion (O^{2-}) or $V_O^{\cdot\cdot}$ migration inside gate dielectrics have been mainly reported for resistive switching devices and electric double-layer-based capacitive storage devices. The phenomena that can be taken into account for changes in gate current (I_G) by insertion of Al_2O_3 layer are as follows.

The first is the resistive switching current, which occurs when the Al_2O_3 layer performs a resistive switching function due to the internal mobile charge species [21]. In this case, the hysteresis directions of the I_G-V_G curve (linear-scale) in the $-V_G$ and $+V_G$ regions are generally opposite. If the change in I_G with the clockwise direction is maintained across the entire V_G region, this phenomenon can be excluded.

The second is the tunneling current, which is the current generated by trap-assisted tunneling of electrons. Resonant tunneling, which is the current through positively charged trap states generated by impact ionization or local heating effects, has also been reported to cause the I_G change [22]. However, the Al_2O_3 layer must be in direct contact with the gate metal to facilitate the inflow of electrons into the thin film. In addition, the peak shape of the resonant tunneling current has a unique current shape according to V_G.

The third case is the faradaic current due to the redox reaction of the Al_2O_3

layer [23]. It is possible to explain the asymmetry of the current peaks in $-V_G$ and $+V_G$ regions due to the difference in activation energy of each reaction. However, this phenomenon is a result of the generation and disappearance of electrons accompanying the recombination/dissociation reaction between O^{2-} and $V_O^{\cdot\cdot}$.

And in the last case, the internal electric field ($E_{int.}$) changes due to the mobile charge inside Al_2O_3, and the I_G changes as a gate leakage. In previous papers, the I_G characteristics when high-k oxide was applied as a gate dielectric layer or IL were not analyzed closely. The I_G characteristics were simply analyzed for a range of current values. In general, the drain current is often regarded as the channel current because the channel current dominates the gate leakage. However, when the gate leakage rapidly increases in a specific V_G region, the measured drain current mainly reflects the gate leakage characteristics, not the channel current. In such cases, the performance of TFT device can be misunderstood.

Since $V_O^{\cdot\cdot}$ has the most probable charge defect in high-k oxide, careful consideration of the effect of $V_O^{\cdot\cdot}$ on gate leakage is required. In addition, in order to improve the device performance, it is necessary to fully understand and analyze the instability characteristics induced by mobile charges in gate dielectric layer or IL.

In this part, the change in the behavior of charge carriers cuased by $V_O^{\cdot\cdot}$ migration of $SnO/Al_2O_3/SiO_2$ gate-stacked devices was analyzed through

evaluation of I-V (or C-V) characteristics according to the V_G range (or frequency) change.

5.2.2. Experimental procedure

The $SnO/Al_2O_3/SiO_2$ gate-stacked devices for TFT and MOSCAP used in this study is the same as the device analyzed in chapter 5.1. The details of fabrication and measurement for the ALD SnO devices can be found in chapter 5.1.2.

The I_G is defined as the current between the gate and a grounded source electrode through the $SnO/Al_2O_3/SiO_2$ stacks. The I_G characteristics were measured depending on the sweep range of V_{GS}. The $-V_{G,\,max}$ was varied from -25 V to -15 V, while the $+V_{G,\,max}$ was fixed at +15 V.

The C-V characteristics were measured at different frequencies. The voltage was applied to the bottom electrode (BE) like the gate electrode of the TFT device, and the top electrode was grounded like the source electrode of the TFT device. The gate voltage was specified as V_G, and the bottom electrode voltage was specified as V_{BE}. It was difficult to analyze the C-V results below 1 kHz and above 100 kHz, because severe noise and curve degradation problems, respectively, were observed. Therefore, only the results in the range from 1 kHz to 100 kHz could be discussed in this work. The C-V measurement show the FW and BW sweep results between –20 V and +15 V, where the DC SR was 5

V/sec.

5.2.3. Results and discussion

Figure 5.10 shows the (a) I-V curve and (b) C-V measurement of the TFT and capacitor of $SnO/Al_2O_3/SiO_2$ stacked device, respectively. The device exhibits three different hysteresis behaviors according to the FW and BW sweeps.

The first is horizontal transition of the curve. This is a commonly interpreted hysteresis behavior, caused by the flat band voltage (V_{FB}) shift between FW and BW seep. The second is the value difference in the region of depletion bias, which is stated as region A. The device shows an abnormal behavior where the hysteresis directions of the I-V and C-V curves do not coincide. In general, the drain current increases as the gate capacitance gets larger, since the induced charge carrier concentration increases. However, the current value of FW is higher than that of BW, though the capacitance value of FW is lower than that of BW. The third is the value difference in the range of accumulation bias, which is stated as region B. It shows the abnormal behavior that the capacitance value of BW is increased and recovered in a certain voltage range. This is a result that cannot be observed with the current value of the TFT device. These three types of behaviors correspond to the $V_{O}^{\cdot\cdot}$ migration, the most probable defect in high-k oxide, which will be discussed below. Previous studies have revealed the mechanism of determining the V_{th} (or V_{FB}) of the FW sweep by

$V_O^{\cdot\cdot}$. Referring to previous results, the sweep range was set to -20 V to +15 V in **Figure 5.10**, mainly to observe the $V_O^{\cdot\cdot}$ effect for region A and B.

Figure 5.11 summarizes the three charge effects that can be generated by $V_O^{\cdot\cdot}$ migration in $SnO/Al_2O_3/SiO_2$ gate-stacked devices (TFTs and capacitors) by a band diagram. The red and blue arrows indicate the behavior induced by DC and AC stimulus, respectively. Scheme specified as charge effect (1) is the field-induced $V_O^{\cdot\cdot}$ migration to the adjacent layer, e.g., SiO_2 or SnO. Scheme specified as charge effect (2) is the change of electron amount inflow/outflow to the gate (or BE) due to the formation of $E_{int.}$ induced by $V_O^{\cdot\cdot}$. Scheme specified as charge effect (3) is the change of AC reactivity of hole carrier according to the $V_O^{\cdot\cdot}$ position that determines the activation of $V_O^{\cdot\cdot}$ energy level (E_{Vo})

The first charge effect is the case of the field-induced migration of $V_O^{\cdot\cdot}$ in the Al_2O_3 thin film to the adjacent layer, that is, the SiO_2 or SnO film by DC stimulus. In the case of $V_O^{\cdot\cdot}$ migration in the multilayered oxide structure, factors such as $V_O^{\cdot\cdot}$ formation energy, Gibbs free energy difference in different oxidized states (phase transition), ionic mobility, migration barrier at the interface, and gate bias stress are considered. In the case of $V_O^{\cdot\cdot}$ defects in SiO_2 material, the formation energy is known to be remarkably high. Therefore, field-induced migration of $V_O^{\cdot\cdot}$ to the SiO_2 layer at V_G (or V_{BE}) < 0 is not easy to occur. On the other hand, it has been reported that the formation energy of $V_O^{\cdot\cdot}$ defects in SnO material is sufficiently low. Therefore, it is necessary to

consider the field-induced migration of $V_O^{\cdot\cdot}$ into the SnO layer at V_G (or V_{BE}) > 0.

Assuming that the phenomenon occurs by satisfying all of the above factors, the structural and electrical characteristics can be changed as follows. The formed Sn- $V_O^{\cdot\cdot}$ bond can function as a generator of electron donor state, hole scattering center or a leakage path for gate-injected charge (based on SnO-based ReRAM research). Accordingly, changes in electrical properties such as decrease in hole concentration/mobility, increase in off-current or increase in gate current may occur. All expected results act as the degradation factors in the electrical properties of SnO channel layer.

However, the measurement results do not correspond to these expected properties, and the reason can be attributed to the fact that a gate bias stress large enough to cross the migration barrier at the interlayer interface is not applied. In this device, the oxide bilayer (Al_2O_3/SiO_2) structure was used as the gate dielectric. Since the low-k SiO_2 (ε_r~3.9, 30 nm) layer was used quite thickly, the local electric field of both the depleted SnO (ε_r~7.8, 7 nm) and the Al_2O_3 (ε_r~8.6, 15 nm) are relatively small across the layer. In this case, the local electric field calculated through **Figure 5.10**b is 2.03, 1.83, 4.04 MV/cm, respectively, in the order of SnO, Al_2O_3, and SiO_2 layers.

In addition, since it is estimated that the SnO/Al_2O_3 interface is defective (discussed later in **Figure 5.17**), the degree of $V_O^{\cdot\cdot}$ migration into the SnO layer compared to the degree of $V_O^{\cdot\cdot}$ trapping at the SnO/Al_2O_3 interface is

considered to be insignificant.

Therefore, in a later discussion, based on the assumption that the range of field-induced $V_O^{\cdot\cdot}$ migration behavior is limited to the inside of the Al_2O_3 thin film, the relationship between the charge effects (2) & (3) shown in **Figure 5.11** and the abnormal electrical characteristics shown in **Figure 5.10** was investigated in detail.

Figure 5.12 is log scale and linear scale of I_G-V_G curve of the TFT device, respectively. The formation of the E_{int} is reflected to the gate leakage characteristics as depicted in charge effect (2) in **Figure 5.11**. Alignment of mobile charge species such as O^{2-} or $V_O^{\cdot\cdot}$ inside high-k oxide forms an $E_{int.}$, and balancing it with the external electric field ($E_{ext.}$) at a specific voltage have been reported in many studies. This behavior is represented by a linear relationship between $V_{G,\,max}$ (maximum value of $-V_G$ applied to the TFT device) – $V_{G,\,min}$ (V_G value when I_G has a minimum value) in the I_G characteristic. As shown in the inset of **Figure 5.12**a, it was observed that a linear relationship between $V_{G,\,min}$ and $V_{G,\,max}$. The minimum value of I_G at $V_{G,\,min}$ is almost similar, so it was not regarded as a measurement error point.

The phenomenon that I_G has a minimum value at a specific V_G other than 0 V can be interpreted as suppressing most of the charge transfer because the electric field applied to the gate dielectric is minimized at a specific V_G. Therefore, as studied in the part 5.1, the absolute value of $-V_{G,\,max}$ increases, the more $V_O^{\cdot\cdot}$'s are aligned at the interface. Therefore the balance with the $E_{ext.}$

occurs at the larger negative voltage of FW sweep of V_G (**Figure 5.13**). Accordingly, when the absolute value of $-V_{G,\,max}$ increases, $V_{G,\,min}$ become more negative.

In other words, the $E_{int.}$ formed by $V_O^{\cdot\cdot}$ is becomes a competing factor that offsets an $E_{ext.}$ formed throughout the gate stack by the applied V_G (or V_{BE}), followed by the influence to the degree of band bending of the Al_2O_3 thin film (**Figure 5.14**). As a result, the amount of electron inflow/outflow to the gate (or BE) changes, included to the displacive current of I_G of the TFT device, as shown in **Figure 5.12**b. At this point, $+I_G$ and $-I_G$ indicate the in/out of the electron to the gate terminal, respectively. In addition, considering the band alignment, since the electron barrier (3.5 eV) is lower than the hole barrier (4.4 eV), it is assumed that the electron is the charge carrier that mainly contributes to I_G.

The section (1) in **Figure 5.12**b is the V_G range in which $V_O^{\cdot\cdot}$'s distributed in the Al_2O_3 thin film gradually align to the Al_2O_3/SiO_2 interface as the FW sweep of V_G progresses. As $E_{int.}$ increases, $E_{ext.}$ cancels out and the amount of electrons flowing from the gate decreases. Thus, the absolute value of $-I_G$ gradually decreases after reaching the maximum value ($-I_{G,\,max}$) in $-V_{G,\,max}$. In this case, a rapid decrease in current means that when a large negative voltage is applied as the starting voltage, the reaction proceeds quickly. This suggests that the condition of $V_{G,\,max} \leq -15$ V is quite energetic for the movement and alignment of $V_O^{\cdot\cdot}$'s.

The section (2) in **Figure 5.12**b is the V_G range where the alignment of $V_O^{\cdot\cdot}$'s at the Al_2O_3/SiO_2 interface is completed. $E_{int.}$ is maximized and balanced with $E_{ext.}$ having a flat band structure of $SnO/Al_2O_3/SiO_2$ stack. This hinders the charge transfer, minimizing I_G, as already discussed in **Figure 5.12**a. In this case, near the SnO/Al_2O_3 interface, hole accumulation is maintained in the SnO channel due to the negative charge effect due to the formation of the $V_O^{\cdot\cdot}$ poor region.

The section (3) in **Figure 5.12**b is the V_G range where the alignment of $V_O^{\cdot\cdot}$'s at Al_2O_3/SiO_2 is no longer maintained and $V_O^{\cdot\cdot}$'s being pushed towards SnO/Al_2O_3 as $+V_G$ is applied. As the opposite direction of $E_{ext.}$ becomes dominant, the amount of electron emitted to the gate increases. Furthermore, at the point where $V_O^{\cdot\cdot}$'s are pushed to the maximum degree, I_G has a maximum value ($+I_{G,\,max}$). Besides, hole depletion occurs as the negative charge effect reduces at the SnO/Al_2O_3 interface. Following is the explanation why the value of $+I_{G,\,max}$ is altered with a fixed position according to the increment of the absolute value of $-V_{G,\,max}$.

For mobile ions to move in the oxide layer, they must exceed the potential wells in the bulk or interface. It has been reported that potential wells or ion traps in the interface energetically exist more deeply than in the bulk.

Based on this, the position of $+I_{G,\,max}$ is determined by the action potential (activation energy) required for $V_O^{\cdot\cdot}$'s to leave the Al_2O_3/SiO_2 interface, which is highly dependent on the quality (interface trap charge) of the Al_2O_3/SiO_2

interface.

Since $V_O^{\cdot\cdot}$'s are aligned on the same interface, the corresponding action potential for each $V_O^{\cdot\cdot}$ ion is the same under all conditions. The difference in the amount of $V_O^{\cdot\cdot}$'s does not affect this. In other words, near at $V_G \sim +5$ V, each $V_O^{\cdot\cdot}$ has enough energy to escape from the interface, and pushed out at the same time, so the $+I_{G,\,max}$ positions are the same under all conditions.

On the other hand, the amount of the aligned $V_O^{\cdot\cdot}$'s affects the current intensity. This is due to the relationship between the amount of migrated $V_O^{\cdot\cdot}$'s and the resulting $E_{int.}$. The greater the amount of $V_O^{\cdot\cdot}$'s simultaneously pushed out of the interface, the more rapidly the $E_{int.}$ decreases, affecting the slope of I_G-V_G curve. As the amount of aligned $V_O^{\cdot\cdot}$'s increases, it occurs in a shorter time that $E_{ext.}$ becomes dominant over $E_{int.}$. This results in significant band bending of Al_2O_3 layer and the amount of electrons emitted to the gate increases rapidly. This is different from the behavior of section (2), which first induces the alignment of $V_O^{\cdot\cdot}$'s by varying the $-V_{G,\,max}$ value. In the case of section (3), this is the effect of applying the same starting voltage to force the $V_O^{\cdot\cdot}$'s, which has already been aligned, to be pushed out of the interface. Therefore, when the $-V_{G,\,max}$ changes, there is no change in the position of the displacive peaks (i.e. $+I_{G,\,max}$), but there is significant change in the intensity of the peaks.

The section (4) in **Figure 5.12**b is the V_G range where $V_O^{\cdot\cdot}$'s begins to align at the SnO/Al_2O_3 interface as the FW sweep of V_G progresses further. The reverse $E_{int.}$ is recreated and cancels $E_{ext.}$, the amount of electrons emitted to the

gate decreases. This leads to $+I_G$ intensity is gradually decreased after having $+I_{G,\,max}$.The section (5) in **Figure 5.12**b is the V_G range where the alignment of the pushed $V_O^{\cdot\cdot}$'s at the SnO/Al_2O_3 interface is completed as the BW sweep of V_G proceeds further. Therefore, it has an $I_{G,\,min}$ point at the maximum degree of $V_O^{\cdot\cdot}$'s alignment, and shows a low current value in the linear scale.

Since the magnitudes of $+V_{G,\,max}$ are the same as +15 V, no major difference is observed at the $I_{G,\,min}$ points unlike the section (2). However, a slight change of the current intensity at $+V_{G,\,max}$ and position of $I_{G,\,min}$ are observed (**Figure 5.15**), as some $V_O^{\cdot\cdot}$'s are fixed at the interface of Al_2O_3/SiO_2 by $-V_{G,\,max}$.

The section (6) in **Figure 5.12**b is the V_G range where the reverse process proceeds of the section (1) since $-V_G$ is applied again. This results indicated that even if $V_G \leq -5$ V, $V_O^{\cdot\cdot}$'s have enough energy to move and align. In contrast to the sudden change of $-I_G$ due to a large starting voltage of $-V_{G,\,max}$,$-I_G$ increases gradually as $-V_G$ increases gradually in this section.

As the arrangement of the $V_O^{\cdot\cdot}$'s inside Al_2O_3 changes according to the V_G sweep, there is a specific region in which the I_G increases. The capacitance characteristics can be affected if the gate leakage is dominant compared to the channel current. Since the change of I_G in the $-V_G$ range occurs in the SnO accumulation region, the channel current has a relatively high current level ($\sim 10^{6}$ A) even if the I_G increases as a leakage current ($\sim 10^{-10}$ A). Therefore, this does not significantly affect device operation. On the other hand, the I_G change in the $+V_G$ range occurs in the SnO depletion region with a sufficiently low off

current. Therefore, when the I_G becomes dominant compared to the channel current, the capacitance value decreases. As a result, the difference in capacitance value according to the sweep direction in Region A of the C-V curve is shown (**Figure 5.10**b), and it contributes to the abnormal hysteresis behavior where the hysteresis directions of the I-V and C-V curves do not coincide.

In the previous study, in the case of a SnO/SiO_2 (35nm) device without an Al_2O_3 layer, it was confirmed that I_G with a value as low as 10^{11}~10^{12} A showed only the current characteristics by capacitive charging without a displacive current. At the same time, the mechanism suggested in this study can be supported through the result of coincidence of the hysteresis directions of I-V and C-V in the SnO depletion region (**Figure 5.16**).

Unlike Region A, which occurs in the depletion region of the SnO channel layer, Region B is an abnormal hysteresis that occurs in the accumulation region. This indicates the involvement of hole carriers, and the AC reactivity of the hole carriers to the E_{VO}, which is described as the charge effect (3) in **Figure 5.11**. This may be reflected in the capacitance characteristics.

Figure 5.17a, b are the C-V curve depending on the frequency, showing three types of characteristics. The first is the decrease of curve slope with increasing frequency, unlike typical C-V curves. The second is higher capacitance value at 1 kHz comparing to that at frequency above 5 kHz over the entire bias range. Finally, additional capacitance value (ΔC) is mainly observed in the BW sweep

compared to the FW sweep, and the range of ΔC decreases as the frequency increases.

The first characteristic is related to the high sub-gap DOS of the oxide semiconductor. Unlike traditional semiconductors, the oxide semiconductors have high bulk trap density comparable to the interface trap density, highly affecting C-V performance. As a result of ATLAS simulation with parameters in **Table 5.1**, it was confirmed that the carrier trapping/de-trapping (capture-emission) process through the donor-like band-tail states among several sub-gap states in the SnO had a major influence on the frequency dependence (**Figure 5.18-20**). However, this is a C-V characteristic due to the bulk trap of the SnO channel, and is a subject that deviates from the $V_O^{\cdot\cdot}$ migration effect in Al_2O_3 layer. Therefore, this phenomenon will not be covered in this discussion.

The second phenomenon reflects the slow states in the band gap of SnO resulted from the defective SnO/Al_2O_3 interface. On the other hand, the third phenomenon proves the formation of ΔC when hole trapping/de-trapping occurs by AC stimulus. It can be deduced that the E_{VO} in the SnO band gap is placed near valence band. Therefore, whether or not E_{VO} is activated depends on the distribution of $V_O^{\cdot\cdot}$'s, and it affects the capacitance value in a specific voltage region. The detailed mechanism for this is expected to be as follows (**Figure 5.21**).

The $V_O^{\cdot\cdot}$'s are placed at the Al_2O_3/SiO_2 interface when the large $-V_G$ (or $-V_{BE}$) during FW sweep, hence the hole trapping/de-trapping at E_{VO} state are

inactivated even under AC stimulus. Therefore, the capacitance value of FW sweep remains constant (**Figure 5.17**a). However, the hole trapping/de-trapping are activated as $V_O^{\cdot\cdot}$'s move toward SnO/Al_2O_3 interface by applying $+V_G$ (or $+V_{BE}$) when FW sweep is proceeded. This trend is maintained even during the BW sweep and the ΔC is observed in the significant negative voltage region. Subsequently, as it comes back around –15 V, $V_O^{\cdot\cdot}$'s move back towards the SiO_2 interface by a large negative voltage. Therefore, the ΔC disappears which was induced by hole trapping (**Figure 5.17**b).

Consequently, the difference in capacitance value according to the sweep direction is observed in region B of the C-V curve of **Figure 5.10**b, and abnormal hysteresis occurs. The reduction of ΔC is noticed because the extent the reaction of hole to the trapping/de-trapping is diminished as the frequency increases. Hence, the abnormal hysteresis behavior depending on the sweep direction is not observed when the frequency is as high as 100 kHz.

Meanwhile, the ΔC is also detected in the range of 1 kHz – 5 kHz of FW sweep. This is because $V_O^{\cdot\cdot}$'s, which were aligned at the Al_2O_3/SiO_2 interface, becomes somewhat distant from the interface and can react to AC stimulation with a relatively low frequency. However, since the distribution center (charge centroid) of $V_O^{\cdot\cdot}$'s in Al_2O_3 compared to BW sweep is relatively located near the Al_2O_3/SiO_2 interface, the ΔC effect by FW sweep is not significant, and can be observed only at low frequency.

Similar results have been reported in ion gel-based capacitor devices for the

ΔC in a specific voltage region due to ionic migration in the gate dielectric [24], but it is considered that this is not a commonly observed phenomenon. The reason is that, the phenomenon can be observed only when the conduction band or valence band of the channel material and the defect energy level in the dielectric are properly aligned, as discussed above. Therefore, such a result is not a phenomenon that can be commonly caused by using a gate dielectric layer having $V_O^{\cdot\cdot}$'s in a thin film. This is the abnormal behavior under special conditions observed in the device of the structure ($SnO/Al_2O_3/SiO_2$ gate-stacked) in which the Al_2O_3 gate dielectric layer including $V_O^{\cdot\cdot}$ and the SnO channel layer are in contact.

5.2.1. Summary

In conclusion, the $SnO/Al_2O_3/SiO_2$ gate-stack is an excellent gate capacitor structure with small dielectric loss. Therefore, in most of the V_G range, $SnO/Al_2O_3/SiO_2$ gate-stacked TFTs are normally driven by the channel current caused by the capacitive charging effect.

Nevertheless, abnormal behaviors are observed in the region A and B due to the field-induced $V_O^{\cdot\cdot}$ migration inside the Al_2O_3 layer.

In the case of SnO depletion region (region A), the change of $E_{int.}$ due to the alignment of $V_O^{\cdot\cdot}$'s in Al_2O_3, the gate leakage is dominant compared to channel current in a specific voltage region. This leads to the abnormal behavior in

which the direction of C-V hysteresis and that of I-V hysteresis do not coincide.

In the case of SnO accumulation region (region B), due to the change in the E_{VO} activation induced by $V_O^{\cdot\cdot}$'s alignment in the Al_2O_3 layer, the AC reactivity of hole trapping/de-trapping for the corresponding defect level are varied. This leads to the abnormal behavior which occurs the generation/disappearance of the additional capacitance. Through this study, it was demonstrated that it is important to consider the SnO channel characteristics and charge defects that are capable of field-induced migration such as $V_O^{\cdot\cdot}$ in the gate dielectric when evaluating the stability properties of the device. In addition, it is believed that it has contributed to improving the understanding of abnormal characteristics caused by the mobile charge effect.

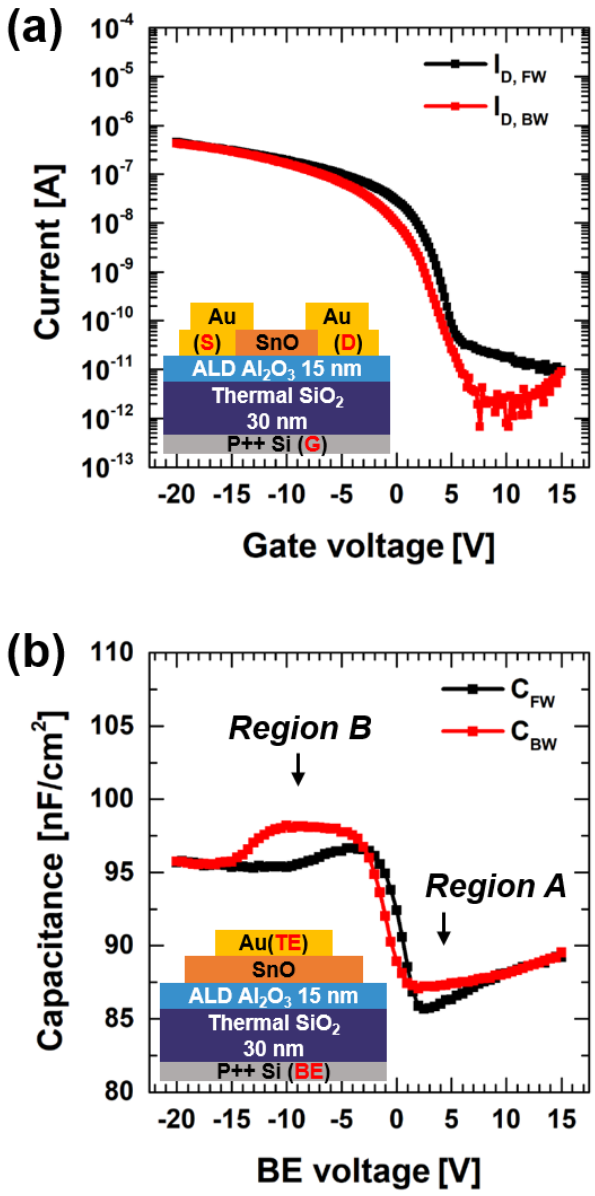


Figure 5.10. (a) The transfer characteristic of the TFT device, and (b) the capacitance voltage characteristic of MOSCAP device. The insets in (a) and (b) show the schematic diagrams of the TFT and MOSCAP structures used in this study, respectively.

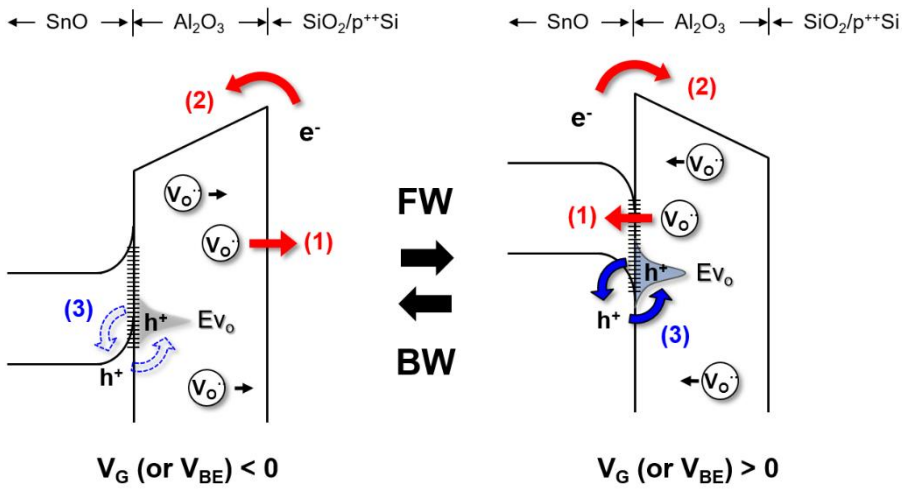


Figure 5.11. The schematic band diagrams summarizing the possible charge effects due to $V_O^{\cdot\cdot}$ migration in $SnO/Al_2O_3/SiO_2$ gate-stacked devices. The red and blue arrows indicate charge behaviors induced by DC and AC stimulus, respectively.

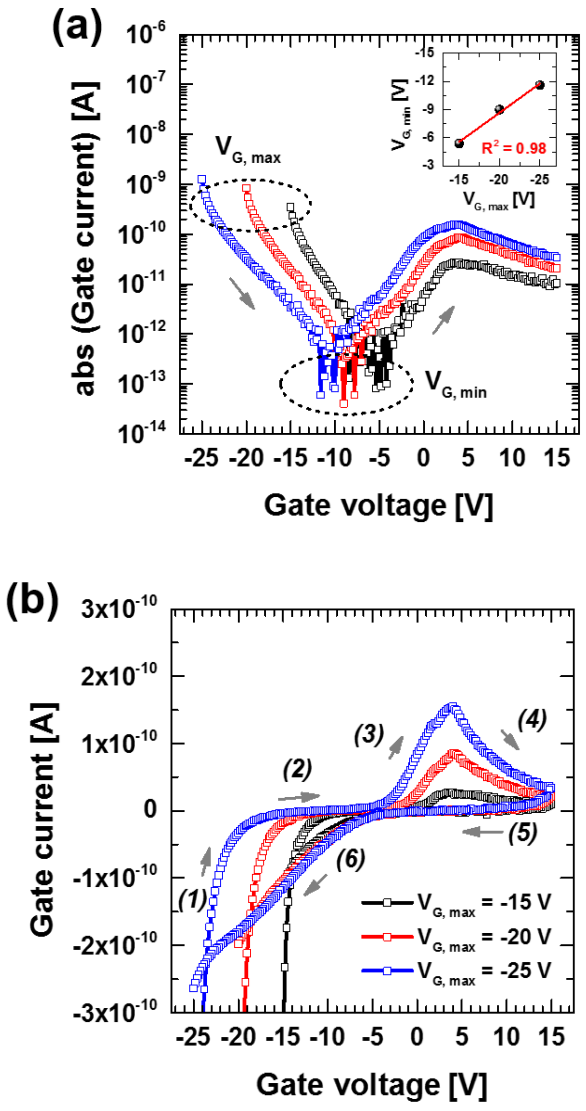


Figure 5.12. The gate current characteristics in (a) log- and (b) linear-scale of the TFT devices. (a) Variation of the voltage position for a minimum current ($V_{G,\,min}$) in the FW sweep as a function of the maximum gate voltage ($V_{G,\,max}$), where inset exhibits a linear relationship of $V_{G,\,min} - V_{G,\,max}$ curve. (b) Variation of the peak values of the current, and the arrows indicate the curve direction.

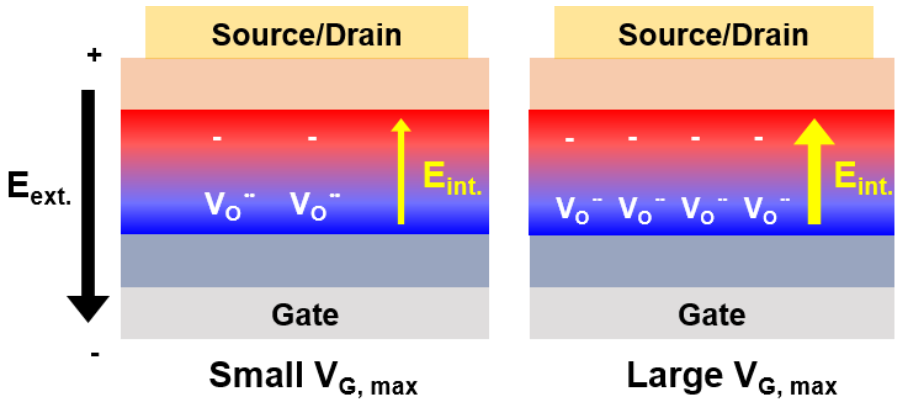


Figure 5.13. A schematic diagram of the change of $E_{int.}$ intensity depending on the $V_{G,\,max}$.

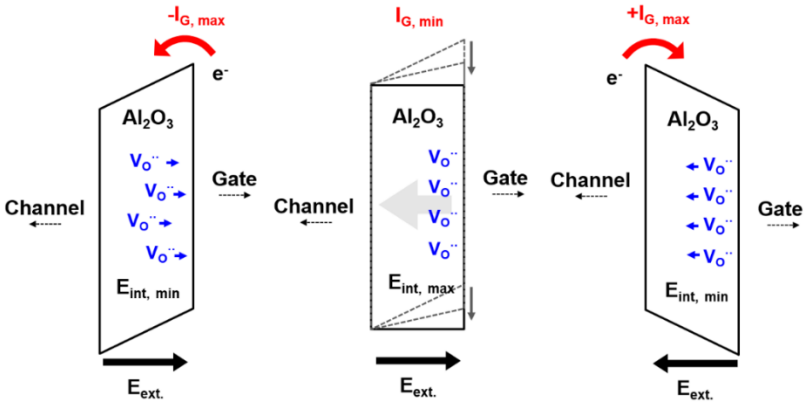


Figure 5.14. The schematic diagram of changes in the amount of electrons flowing into/out of the gate (or BE) by forming $E_{int.}$ by $V_O^{\cdot\cdot}$.

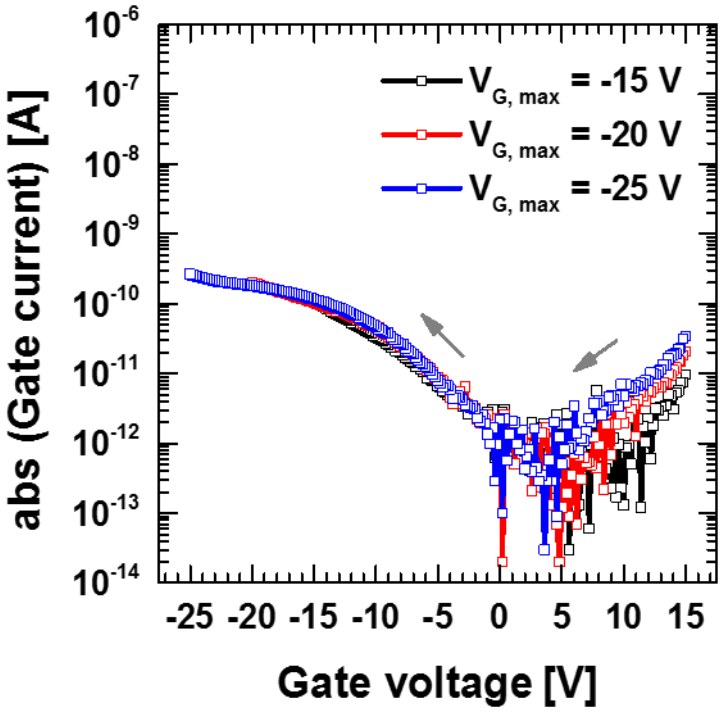


Figure 5.15. The gate current characteristics of BW sweep depending on the $V_{G,\,max}$.

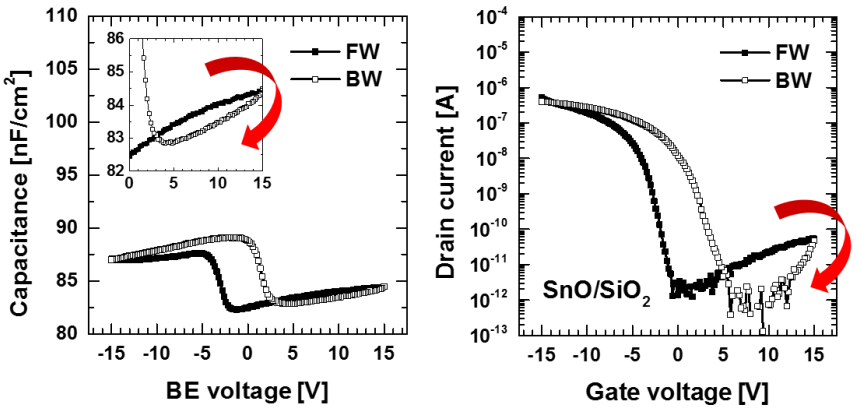


Figure 5.16. (a) The capacitance-voltage characteristic of SnO/SiO_2 stacked MOSCAP device, and (b) the transfer characteristic of the SnO/SiO_2 stacked TFT device. The insets in (a) and (b) show the schematic diagrams of the MOSCAP and TFT structures, respectively.

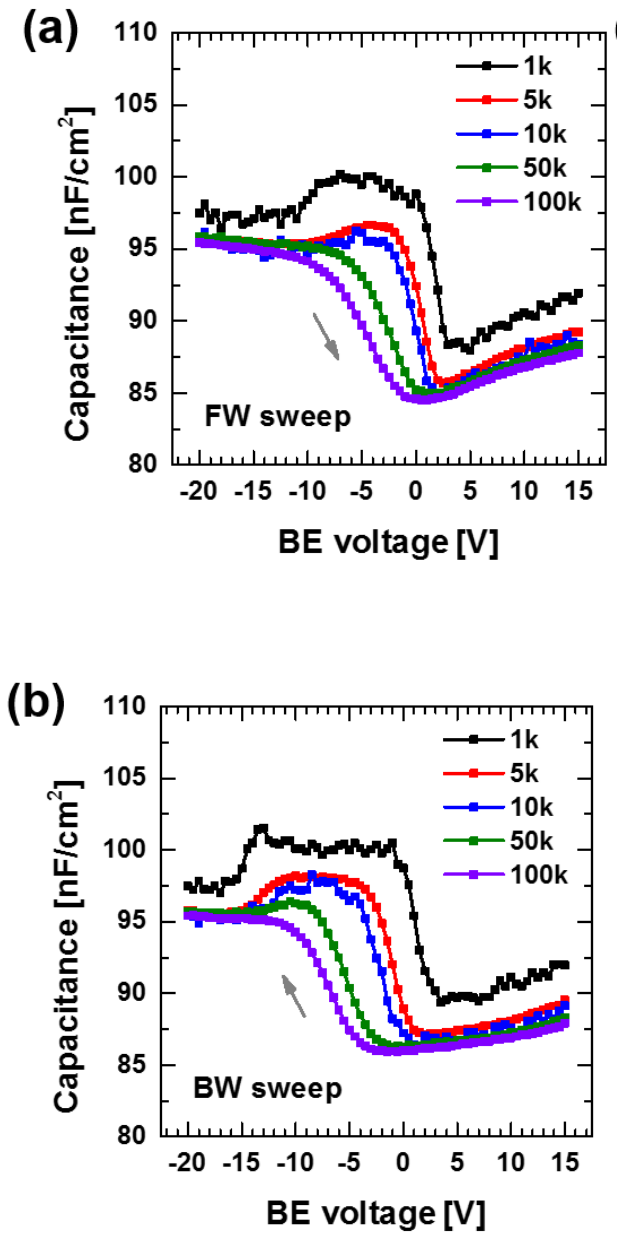


Figure 5.17. Multi-frequency C-V characteristics for a MOSCAP devices measured in (a) FW sweeps and (b) BW sweeps.

Symbols	Units	SnO TFT
N_C	cm^{-3}	2.41×10^{18}
N_V	cm^{-3}	9.13×10^{19}
N_{TA}	$cm^{-3}\ eV^{-1}$	2.43×10^{20}
N_{TD}	$cm^{-3}\ eV^{-1}$	$5 \times 10^{20} \sim 5 \times 10^{21}$
W_{TA}	meV	30
W_{TD}	meV	70
E_g	eV	0.9
χ_e	eV	3.7
ε_r		15
W_{GA}	eV	0.1
E_{GA}	eV	0.52
E_{GD}	eV	0.9
W_{GD}	eV	0.2
N_{GD}	$cm^{-3}\ eV^{-1}$	0.7×10^{17}
N_{GA}	$cm^{-3}\ eV^{-1}$	0.1×10^{19}
μ_P	$cm^{-3}/V-s$	4.8

Table 5.1 Simulation parameters in DOS model for SnO 7 nm / SiO_2 35 nm TFTs with Au source/drain electrode for C-V results.

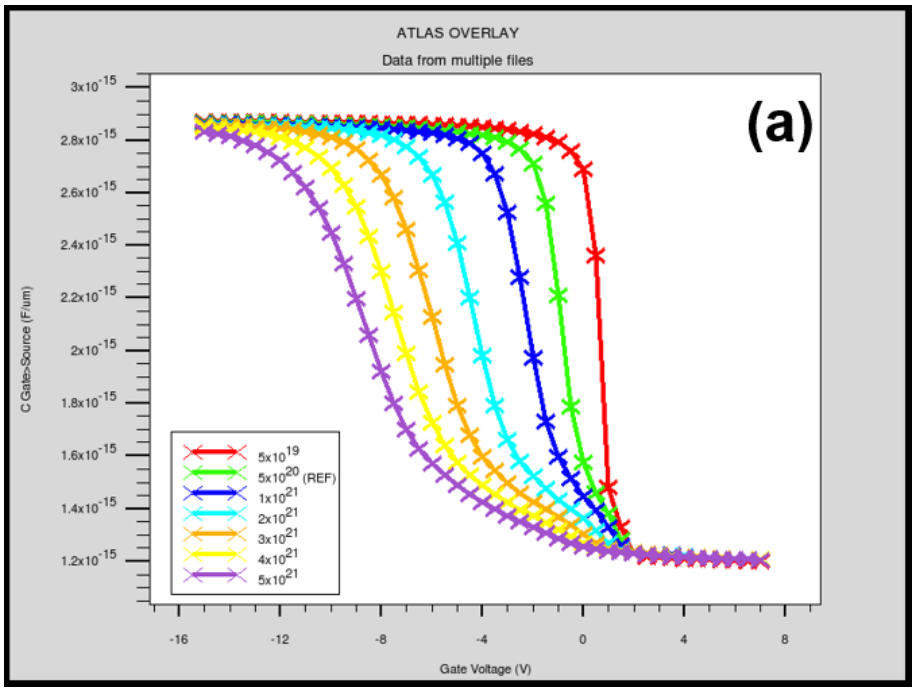


Figure 5.18. The results of ATLAS simulation or C-V characteristics of ALD SnO devices. Figure shows the C-V results according to the density of donor-like band-tail state at frequency of 1 MHz. The unit of density in Figure is [cm^{-3}].

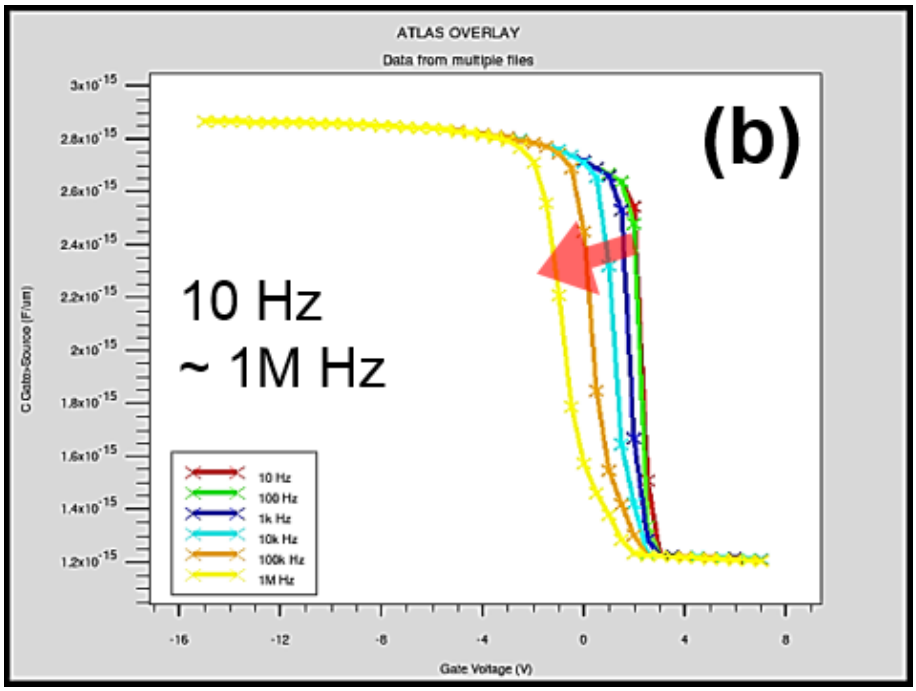


Figure 5.19. The results of ATLAS simulation or C-V characteristics of ALD SnO devices. Figure shows the C-V results according to the frequency from 10 Hz to 1 MHz with density of donor-like band-tail state of 5×10^{20} cm^{-3}.

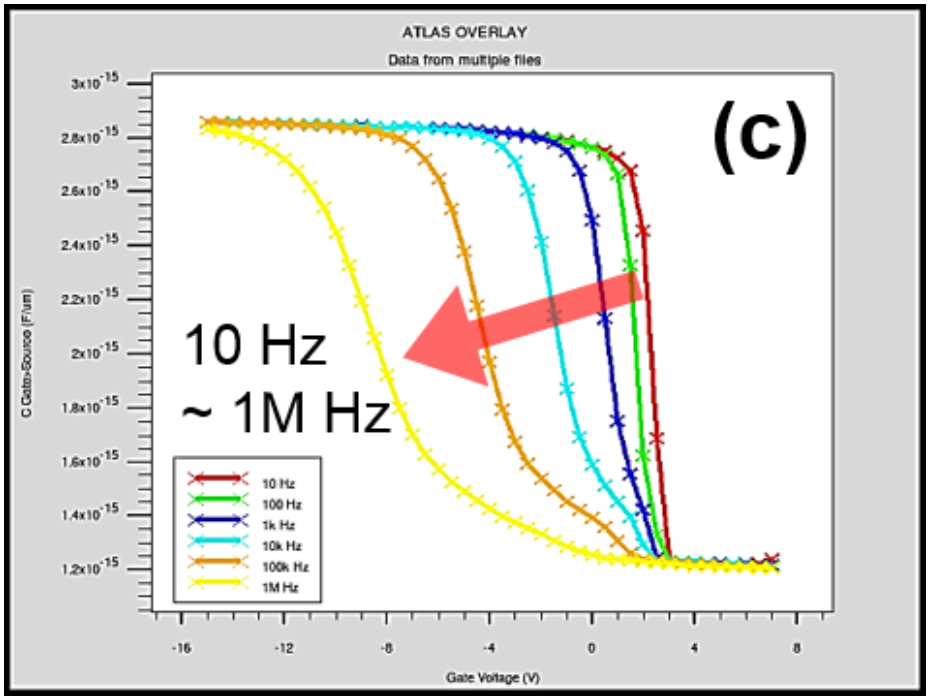


Figure 5.20. The results of ATLAS simulation or C-V characteristics of ALD SnO devices. Figure shows the C-V results according to the frequency from 10 Hz to 1 MHz with density of donor-like band-tail state of 5×10^{21} cm^{-3}.

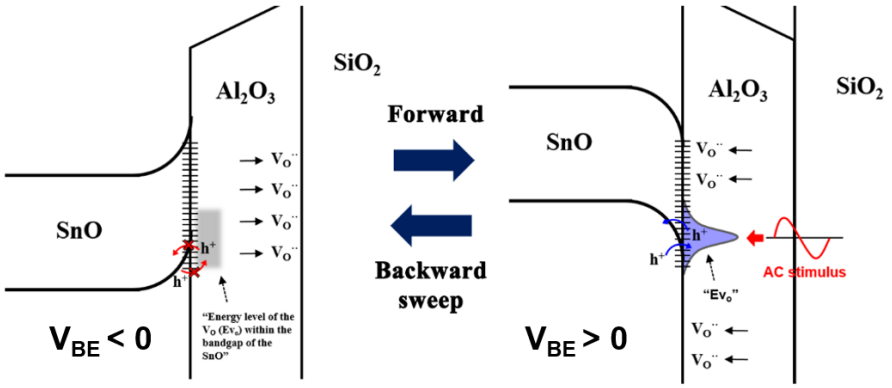


Figure 5.21. The schematic diagram of changes in the AC reactivity of holes to the E_{VO} according to the $V_O^{\cdot\cdot}$ position.

5.3. Bibliography

[1] Y. Li, J. Zhang, J. Yang, Y. Yuan, Z. Hu, Z. Lin, A. Song, Q. Xin, *IEEE Trans. Electron Devices* **2019**, *66*, 950.

[2] Z. Wang, P. K. Nayak, A. Albar, N. Wei, U. Schwingenschlögl, H. N. Alshareef, *Adv. Mater. Interfaces* **2015**, *2*, 1500374.

[3] Z. Wang, X. He, X.-X. Zhang, H. N. Alshareef, *Adv. Electron. Mater.* **2017**, *3*, 1700396.

[4] H. Peng, A. Bikowski, A. Zakutayev, S. Lany, *APL Mater.* **2016**, *4*, 106103.

[5] X. Guan, Z. Wang, M. K. Hota, H. N. Alshareef, T. Wu, *Adv. Electron. Mater.* **2019**, *5*, 1800538.

[6] M. K. Hota, J. A. Caraveo-Frescas, M. A. McLachlan, H. N. Alshareef, *Appl. Phys. Lett.* **2014**, *104*, 152104.

[7] J. A. Caraveo-Frescas, M. A. Khan, H. N. Alshareef, *Sci. Rep.* **2014**, *4*, 5243.

[8] Y. Jang, I. W. Yeu, J. S. Kim, J. H. Han, J.-H. Choi, C. S. Hwang, *Adv. Electron Mater.* **2019**, *5*, 1900371.

[9] I.-C. Chiu, I.-C. Cheng, *IEEE Electron Device Lett.* **2014**, *35*, 90.

[10] J.-H. Lee, Y.-J. Choi, C.-Y. Jeong, D.-K. Jung, S. Ham, H.-I. Kwon, *IEEE Electron Device Lett.* **2016**, *37*, 295.

[11] Y.-J. Han, Y.-J. Choi, C.-Y. Jeong, D. Lee, S.-H. Song, H.-I. Kwon, *IEEE Electron Device Lett.* **2015**, *36*, 466.

[12] J.-H. Lee, Y.-J. Choi, C.-Y. Jeong, C.-W. Lee, H.-I. Kwon*, J. Vac. Sci.Technol. B* **2016**, *34*, 041210.

[13] G. Ghibaudo, *Electron. Lett.* **1988**, *24*, 543.

[14] W. Fikry, G. Ghibaudo, H. Haddara, S. Cristoloveanu, M. Dutoit, *Electron. Lett.* **1995**, *31*, 762.

[15] M. Egginger, S. Bauer, R. Schwodiauer, H. Neugebauer, N. S. Sariciftci, Monatsch. *Chem.* **2009**, *140*, 735.

[16] M. Y. Yang, K. Kamiya, B. Magyari-Kope, M. Niwa, Y. Nishi, K. Shiraishi, *Appl. Phys. Lett.* **2013**, *103*, 093504.

[17] N. J. Chou, *J. Electrochem. Soc.* **1971**, *118*, 601.

[18] J. R. Davis, *Instability in MOS Devices*, Gordon and Breach, New York **1981**.

[19] S. Thiemann, S. J. Sachnov, M. Gruber, F. Gannott, S. Spallek, M. Schweiger, J. Krückel, J. Kaschta, E. Spiecker, P. Wasserscheid, J. Zaumseil, *J. Mater. Chem. C* **2014**, *2*, 2423.

[20] T. N. Ng, J. H. Daniel, S. Sambandan, A.-C. Arias, M. L. Chabinyc, R. A. Street, *J. Appl. Phys.* **2008**, *103*, 044506.

[21] G. Wang, J.-H. Lee, Y. Yang, G. Ruan, N. D. Kim, Y. Ji, J. M. Tour, *Nano Lett.* **2015**, *15*, 6009.

[22] A. Daus, C. Vogt, N. Münzenrieder, L. Petti, S. Knobelspies, G. Cantarella, M. Luisier, G. A. Salvatore, G. Tröster, *J. Appl. Phys.* **2016**, *120*, 244501.

[23] P. B. Pillai, A. Kumar, X. Song, M. M. De Souza, *ACS Appl. Mater. Interfaces* **2018**, *10*, 9782.

[24] J. H. Cho, J. Lee, Y. He, B. Kim, T. P. Lodge, C. D. Frisbie, *Adv. Mater.* **2008**, *20*, 686.

6. Improvement of Electrical Properties in SnO TFTs with HfO_2-based interfacial layer

6.1. A Study on the factors that determine the performance of SnO TFTs adopting a high-k Al:HfO_2 IL

6.1.1. Introduction

In this chapter, an material for the IL that could replace Al_2O_3 was searched. This is because the gate capacitance deteriorates due to the use of a fairly thick IL in the previous study, resulting in a rather large SS value. Therefore, an HfO_2-based material having a high k value (i.e. dielectric constant) is adopted as a IL to improve the gate capacitance. However, HfO_2 has the disadvantage that the crystallization temperature is considerably low even though the dielectric constant is high [1–3]. When crystallization of the HfO_2 thin film occurs, elements that contribute to device deterioration, such as Sn diffusion or leakage current, can be created as already explained in part 4. Therefore, in order to overcome this problem, an experiment was conducted to introduce an Al-doped HfO_2 (Al:HfO_2) thin film as an alternative IL. The reason is that the Al:HfO_2 thin film has the advantages of a large k-value HfO_2 while simultaneously having the Al_2O_3 property of maintaining an amorphous structure even at high temperatures [4-6]. It has been reported that Al:HfO_2 has a high dielectric

constant in a specific structure, that is, a meso-structure, and has a very low gate leakage [6]. In the case of the meso HfO_2 thin film, it is in a state where amorphous and monoclinic phases are mixed. On the other hand, in the case of the Al:HfO_2 thin film, it is in a state where amorphous and tetragonal or cubic images are mixed, thereby having a higher dielectric constant. The principle that the HfO_2 thin film maintains the amorphous state by Al doping to a higher temperature is that the Hf–Al–O bond is formed and the crystallization temperature rises. Therefore, by introducing an Al:HfO_2 thin film as an IL, it is intended to obtain superior IL properties at an annealing temperature lower than 1000 ℃.

6.1.2. Experimental procedure

To improve SS, the experiment was conducted by reducing the SiO_2 thickness from 30 nm to 15 nm. For the deposition of the Al:HfO_2 thin film, Tetrakis(ethylmethylamido)hafnium(IV) (TEMAHf) and TMA were used as Hf and Al sources, respectively, and ozone was used as the oxygen source for both. For HfO_2 deposition, TEMAHf feeding (2 s)-Ar purge (20 s)-O_3 feeding (3 s)-Ar purge (10 s) sequence was used. On the other hand, for Al_2O_3 deposition, a sequence of TMA feeding (2 s)-Ar purge (10 s)-O_3 feeding (3 s)-Ar purge (20 s) was used. Two cycle of ALD Al_2O_3 was inserted between HfO_2 thin films to change the Al doping concentration. The deposition temperature is 280 ℃, and

the growth per rate of the HfO_2 thin film at this time is 0.9A/cy. For comparison with the optimum conditions of the Al_2O_3 thin film, the Al:HfO_2 thin film was also applied with a thickness of 15 nm. In the case of Al doping only in the middle of the HfO_2 thin film, deposition was performed in the HfO_2 52 cy. - Al_2O_3 2 cy. - HfO_2 52cy. sequence (**Figure 6.1**). That is, the ALD cycle ratio of HfO_2 and Al_2O_3 is 52:1. On the other hand, in the case of Al doping alternately with the HfO_2 thin film, the HfO_2 21 cy. -Al_2O_3 2 cy. sequence was repeated 4 times, and the HfO_2 21cy. sequence was additionally deposited. That is, the ALD cycle ratio of HfO_2 and Al_2O_3 is specified as 13:1. Due to the characteristics of the HfO_2 thin film where crystallization occurs relatively easily, high-temperature heat treatment was performed within 2 minutes through the RTA method. Like the heat treatment of the Al_2O_3 thin film, it was carried out in an oxygen atmosphere to remove V_O, which is a native defect of the oxide thin film. RTA treatment was performed from 300 to 800 ℃.

6.1.3. Results and discussion

As a result of Al doping in the middle of the HfO_2 thin film (ALD cycle ratio of HfO_2 : Al_2O_3 = 52 : 1), a problem was found that crystallization occurs more easily than expected. Through GAXRD analysis of the RTA-treated Al:HfO_2 thin film, it was confirmed that crystallization proceeded under all heat treatment conditions from 30 seconds to 2 minutes in a temperature range of

400 to 800 ℃. All of the thin films were crystallized mainly as a monoclinic phase (**Figure 6.2**). On the other hand, when the Al:HfO_2 thin film was RTA-treated at 300 ℃, an amorphous phase was observed (**Figure 6.3**). However, the density of the thin film was not improved due to the problem that there is no significant difference between the RTA treatment temperature and the deposition temperature of the thin film (**Figure 6.4**). Therefore, in order to increase the suppression efficiency against crystallization, a method of alternately Al doping between HfO_2 thin films was introduced (**Figure 6.5**). It was observed that all the thin films treated with RTA at 500 °C were crystallized into a monoclinic phase. However, it was confirmed that the amorphous matrix was maintained at about 495 ℃ in the case of the Al:HfO_2 thin film with the ALD cycle ratio of HfO_2 and Al_2O_3 of 13:1. Based on the GAXRD results, an Al:HfO_2 15 nm thin film was heat-treated at 480 °C and 495 °C, which are the conditions for maintaining amorphous, and adopted as the ILs for the SnO TFTs (**Figure 6.6**).

Among the two heat treatment conditions of the Al:HfO_2 15 nm IL, 480 °C and 495 °C, the TFT device in which the IL was heat-treated at 495 °C showed better transfer characteristics. However, compared to the optimal Al_2O_3 IL conditions obtained through previous studies, it showed significantly deteriorated electrical characteristics in all aspects such as on current, SS, and V_{hy} (**Figure 6.7**). As shown in the I_{GS}-V_{GS} curve, the current level rapidly

increases by ~2 order at high V_{GS} (**Figure 6.8**). In addition, it was observed that the TFT device did not turn on at the low V_{DS} of the output curve. This is analyzed because of the high leakage current characteristics of Al:HfO_2 thin films based on the simulation model of leakage current in a TFT [7]. In other words, V_{DS} and I_{DS} decrease due to the $R_{Drain\text{-}Gate}$ factor due to the large current generation between drain and gate.

The origin of the Al:HfO_2 thin film showing poor leakage characteristics is determined based on the XRR results (**Figure 6.9**). The thin film specified as 100:0 as the ALD cycle ratio of HfO_2: Al_2O_3 is a thin film without Al doping. As the degree of Al doping increases, the thin film density decreases at the same thickness (15 nm). Al doping can suppress the crystallization of HfO_2 thin film, but it acts as an obstacle to the thin film density, greatly deteriorating the performance of the SnO TFT device. It can be analyzed that the effect of increasing the density by the heat treatment does not appear significantly even when the maximum heat treatment temperature (RTA 495 ℃) to maintain the amorphous phase is applied.

In the subsequent experiment, the effect of high density and high dielectric constant was to be confirmed, taking the problem of crystallinity of the Al:HfO_2 thin film. Therefore, an Al:HfO_2 thin film subjected to RTA treatment at 800 ℃ for 30 seconds in an oxygen atmosphere was adopted as IL of SnO TFT (**Figure 6.10**). As a result of the C-V measurement, the total capacitance-equivalent thickness (CET) was 16.3 nm, and the dielectric constant of the Al:HfO_2 thin

film heat-treated at 800 ℃ was calculated as 26.1. The origin of the high dielectric constant was confirmed by GAXRD analysis because the monoclinic phase and the tetragonal phase were mixed (**Figure 6.11**). In addition, as shown in the XRR results, the Al:HfO_2 thin film heat-treated at 800 ℃ can be confirmed to increase the density of the thin film through a critical angel shift compared to the as-depositon thin film and the thin film heat treated at 495 ℃ (**Figure 6.12**).

Therefore, when using the crystallized Al:HfO_2 IL instead, extremely high performance of the SnO TFT was obtained due to the high dielectric constant and improved film density. The SnO TFT with the Al:HfO_2 IL annealed at 800 ^oC showed a V_{hy} of 6.4 V with a μ_{FE} of 5.7 $cm^2/V{\cdot}s$, an SS of 0.39 V/decade, and an I_{on}/I_{off} ratio of 5.6×10^5. Nevertheless, since the characteristics between amorphous and crystallized thin films are markedly different, the process window in which all parameters are optimal is expected to be quite narrow.

The SnO TFTs has been evaluated for its applicability as a memory device by utilizing the large V_{hy} while having excellent transfer characteristics. The V_{GS} stress was applied in the dark box for up to 1000 s, and 0 V was applied to the source and drain electrodes. The programming/erasing (PGM/ERS) characteristics of the TFT memory devices are shown in **Figure 6.13** and **6.14**. The measurement results of the PGM→ERS operation on the memory device are shown in Figure **6.13**. When a negative bias of –12 V was applied for 1000

s on the gate, the device was switched from original state to programmed state, as shown by the blue arrow. When a positive gate bias of +12 V was applied for 1000 s, the resulting I_{DS}-V_{GS} curve returned to the original state corresponding to the pristine device, shown by the green arrow. Meanwhile, the measurement results of the ERS→PGM operation on the memory device are shown in **Figure 6.14**. When a positive bias of +12 V was applied for 1000 s on the gate, the device was switched from original state to erased state, as shown by the red arrow. When a negative gate bias of –12 V was applied for 1000 s, the resulting I_{DS}-V_{GS} curve returned to the original state corresponding to the pristine device, shown by the green arrow. This indicates that the programmed or erased state can be initialized to its original state by an electrical bias, demonstrating an the possibility of memory operation. In other words, it shows the switching ability between pragrammed, erased and original states of SnO TFT devices with Al:HfO_2 IL adopted.

The memory operation of SnO/Al:HfO_2/SiO_2 stacked TFTs can be conducted by the small electrical band gap (~0.7 eV) and ambipolar characteristics of SnO [8–13]. It has been reported that the ERS operation is not properly performed in most of the n-type oxide semiconductor based charge trap memory devices [14–16]. The reason is that most oxide semiconductors have electrical band gaps as high as ~ 3 eV [17,18]. There are few source and drain electrodes that have a work function suitable for hole injection for ERS operation [16]. On the other hand, SnO has higher electron affinity (3.7 eV) and lower ionization

potential (4.4 eV) than general p-type oxide [11]. In addition, unlike general n-type oxide semiconductors, the effective mass of electrons does not significantly differ from the effective mass of holes [19]. Therefore, it has been reported that SnO has ambipoloar properties, which are capable of both hole and electron conduction. For these reasons, SnO materials have the unique feature that electrons and holes are relatively easy to inject into the channel layer, which has contributed to the switching characteristics of SnO TFTs as shown in **Figures 6.13** and **6.14**.

Figure 6.15 shows the data retention characteristics of the memory devices in original state, programmed state and erased state, respectively, at room temperature. For the device in original state in FW and BW sweep, the V_{th} exhibited a negligible change with retention time. For the device programmed at –12 V for 1000 s, the memory window relative to the original state of a pristine device gradually decreased to 0.57 V with an increase in the retention time of up to 10^3 s. For the device erased at +12 V for 1000 s, the window relative to the initial state decreased to 1.01 V at a retention time of 10^3 s. The degradation can be attributed to the leakage of charges stored in Al:HfO_2 IL. Even without inserting a tunneling oxide and a charge trap layer (e.g. SiN_X) in the TFT device, the memory window relative to original state of a pristine device was maintained for programmed and erased state up to 10^5 s and 10^7 s, respectively. Although it was necessary to apply bias stress for a long time for switchin operation between original, PGM and ERS states, the

SnO/Al:HfO_2/SiO_2 stacked TFTs demonstrated electrical programmable and erasable characteristics as well as data retention capability.

Therefore, it is expected that the memory performance can be improved through additional adopting of tunneling oxide or controlling the thickness or crystallinity of the Al:HfO_2 layer.

6.1.4. Summary

Although it was not possible to obtain low V_{hy} by using HfO_2-based IL, there were remarkable advantages in μ_{FE} and SS characteristics. Taking advantage of this, SnO TFT devices can be used for memory devices as well as electronic circuits according to IL materials with different hysteresis characteristics. In other words, a SnO TFT device with a low V_{hy} by adopting an Al_2O_3 IL can be applied as a logic device for CMOS circuit. On the other hand, a SnO TFT device with a large V_{hy} by adopting an Al:HfO_2 IL is expected to be applied as a memory device.

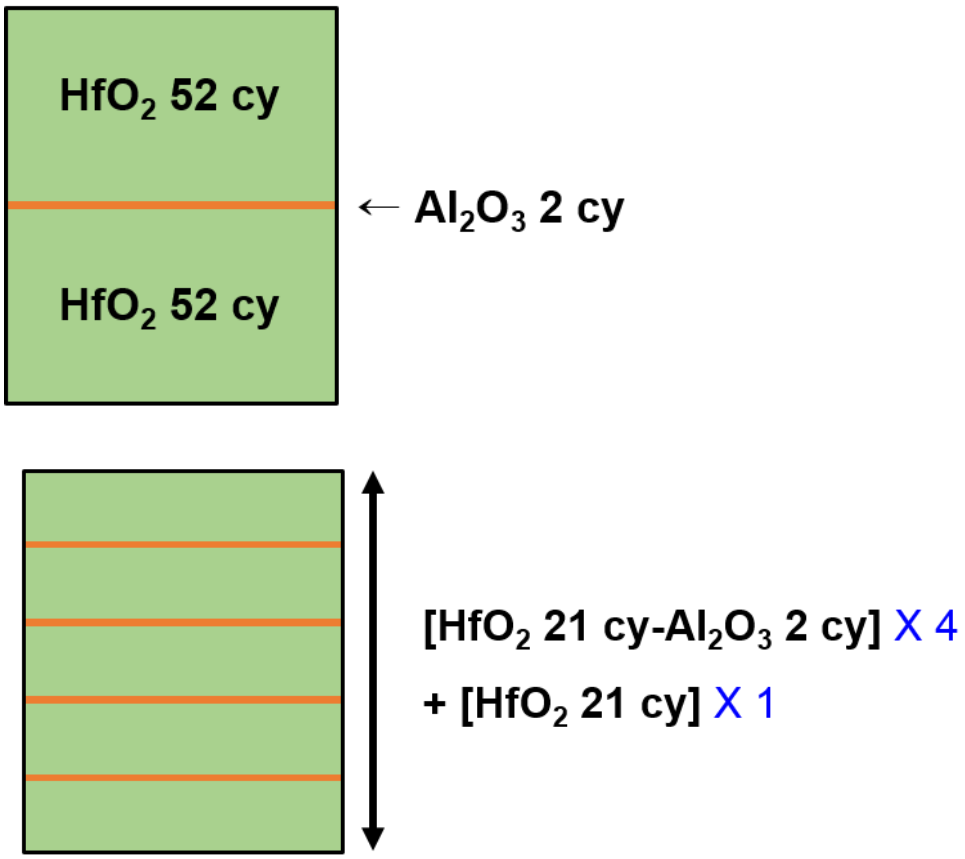


Figure 6.1. The schematic diagram of Al doping into HfO_2 film using the ALD method.

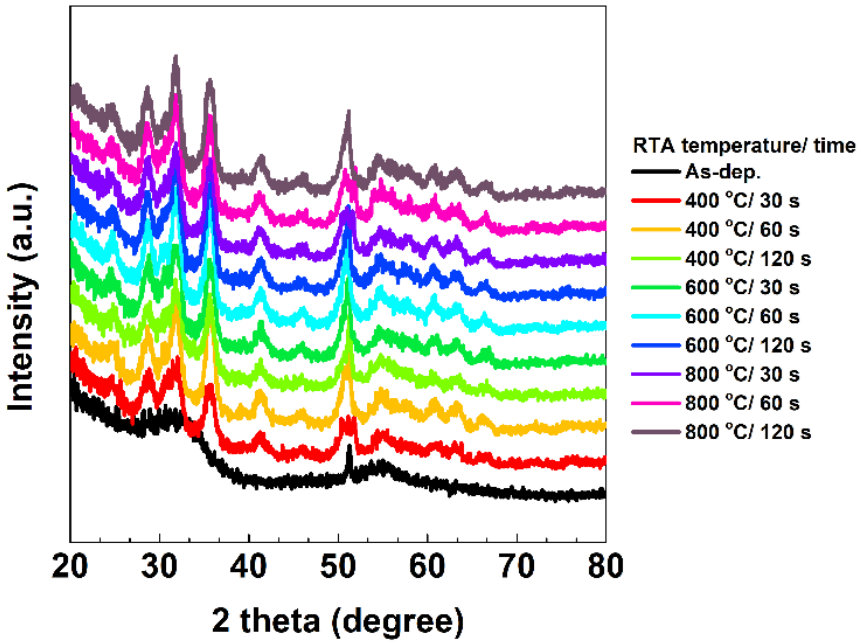


Figure 6.2. GAXRD results of Al-doping in the center of HfO_2 film according to the RTA temperature (400 – 800 ℃) and process time (30 s – 120 s).

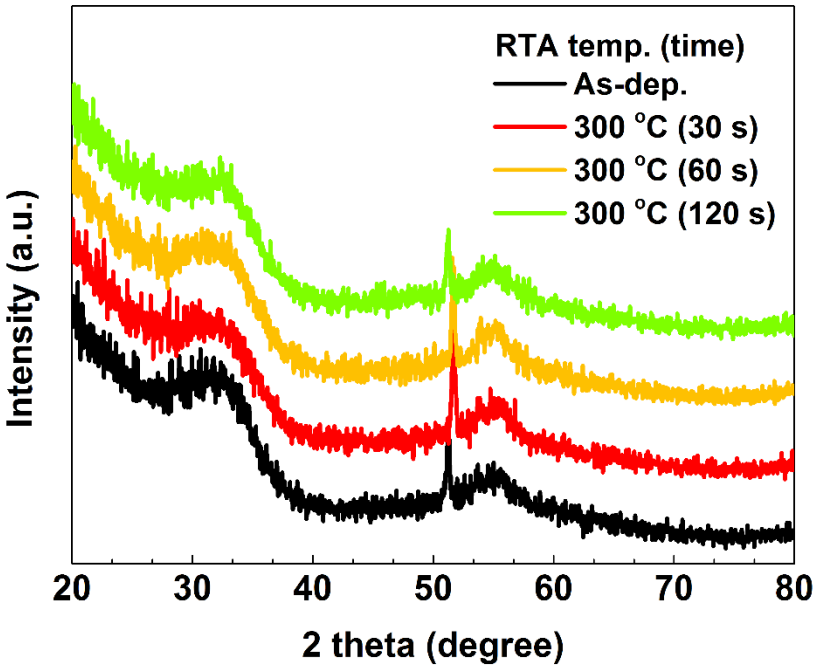


Figure 6.3. GAXRD results of Al-doping in the center of HfO_2 film according to the RTA temperature at 300 ℃ and process time (30 s – 120 s).

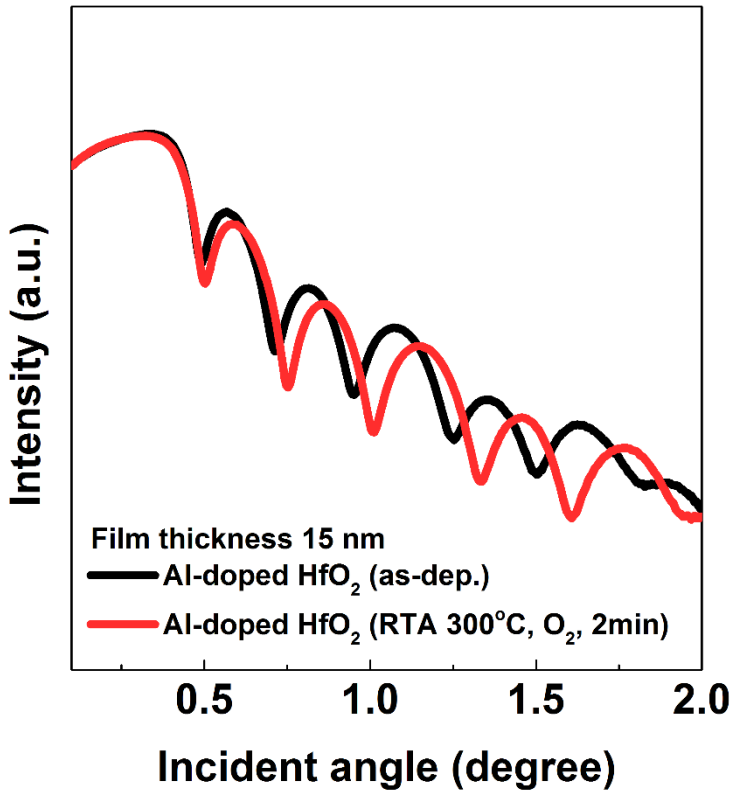


Figure 6.4. XRR results of Al-doping in the center of HfO_2 film according to the RTA temperature at 300 ℃ for process time of 120 s.

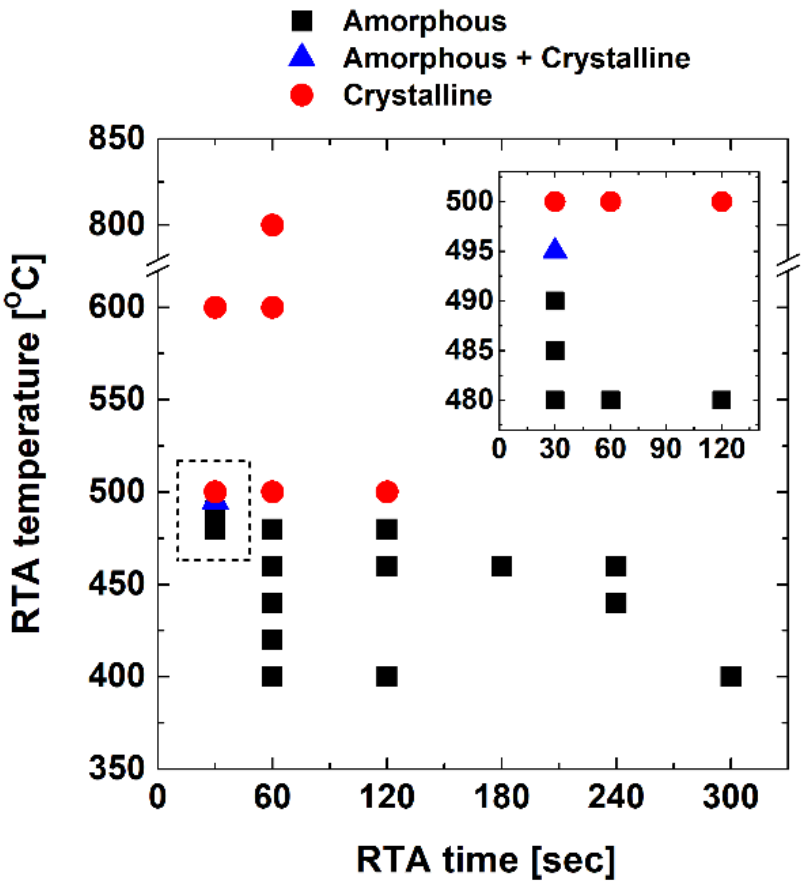


Figure 6.5. The phase mapping based on GAXRD results of alternate doping of Al with HfO_2 film according to the RTA temperature and process time.

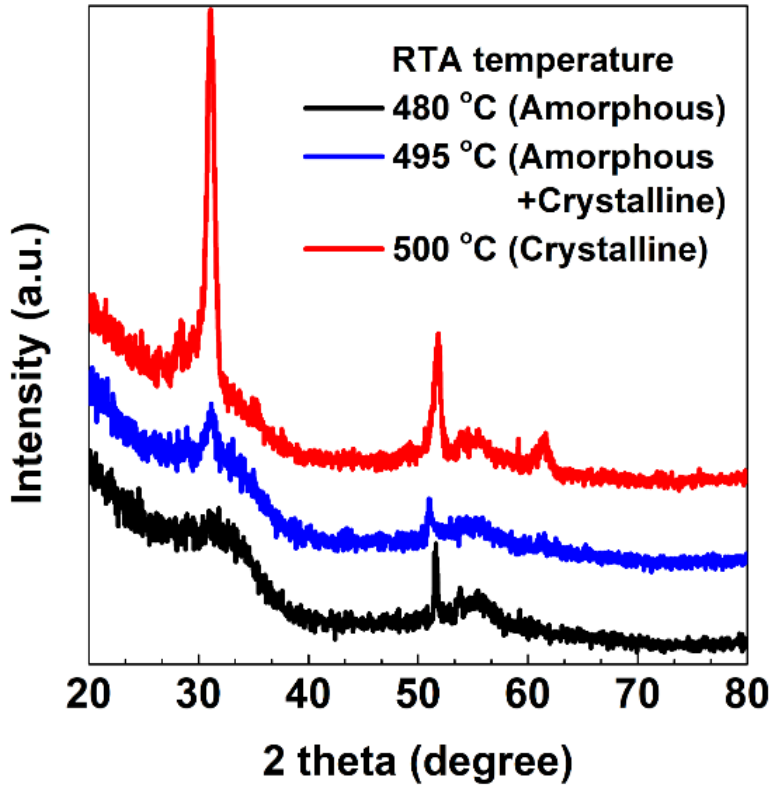


Figure 6.6. GAXRD results of alternate doping of Al with HfO_2 film according to the RTA temperature with process time of 30 s.

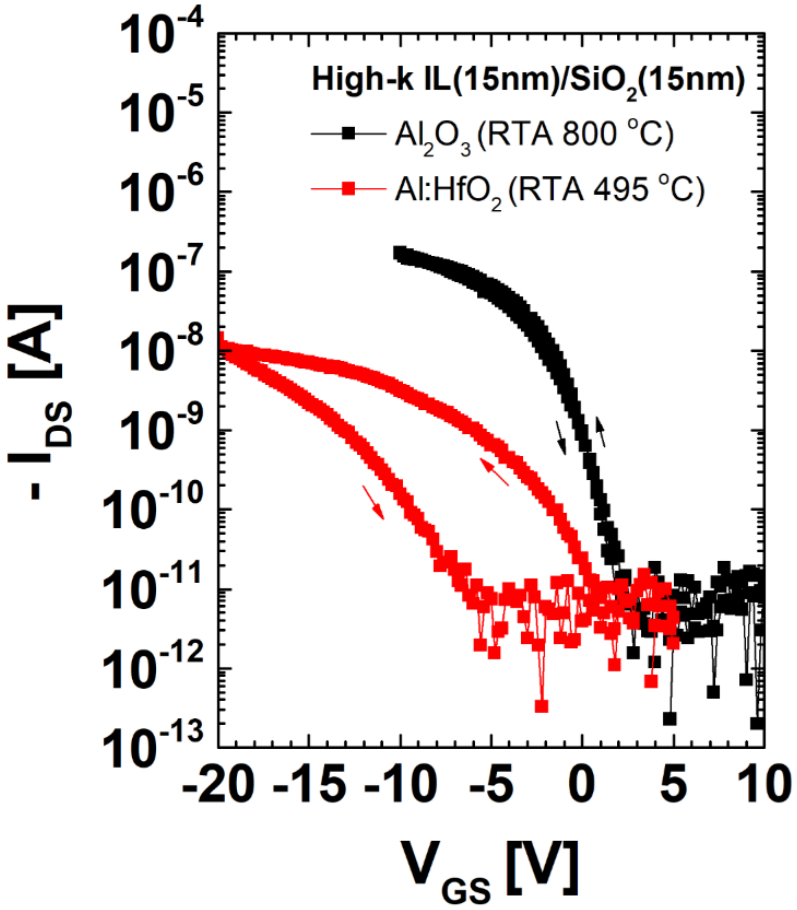


Figure 6.7. The transfer characteristics of SnO TFT with Al_2O_3 IL and Al:HfO_2 IL. The Al_2O_3 IL was underwent RTA at 800 ℃ and the Al:HfO_2 IL was underwent RTA at 495 ℃.

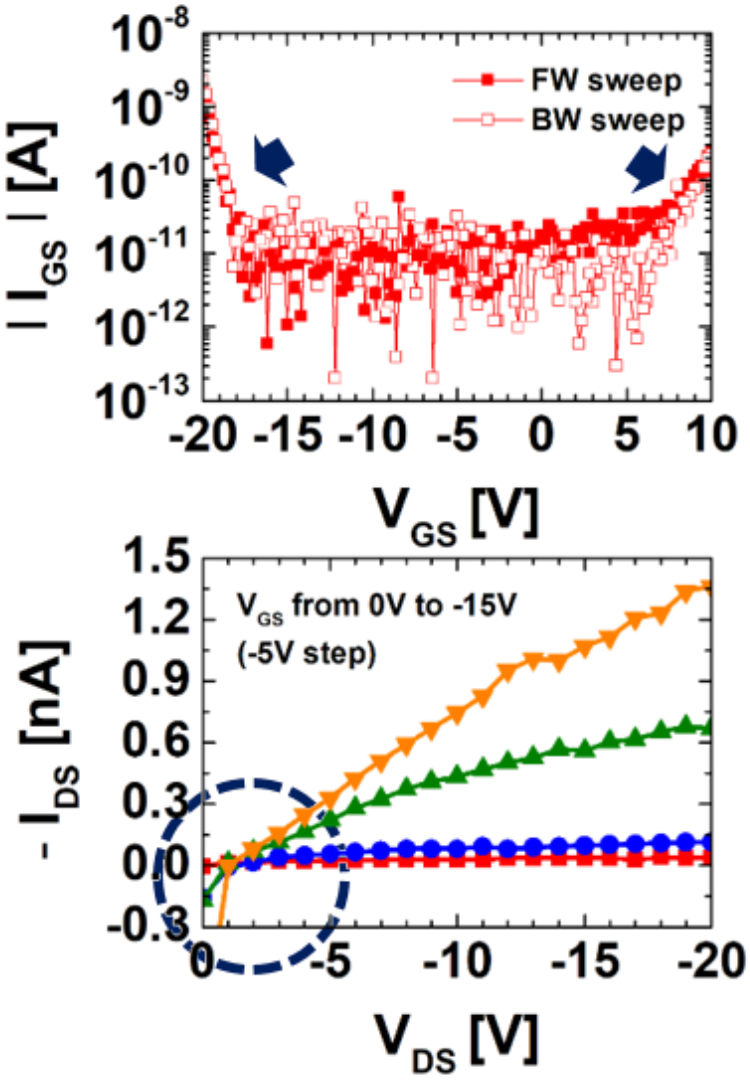


Figure 6.8. The gate current and output characteristics of SnO TFT with Al:HfO_2 IL. The Al:HfO_2 IL was underwent RTA at 495 ℃.

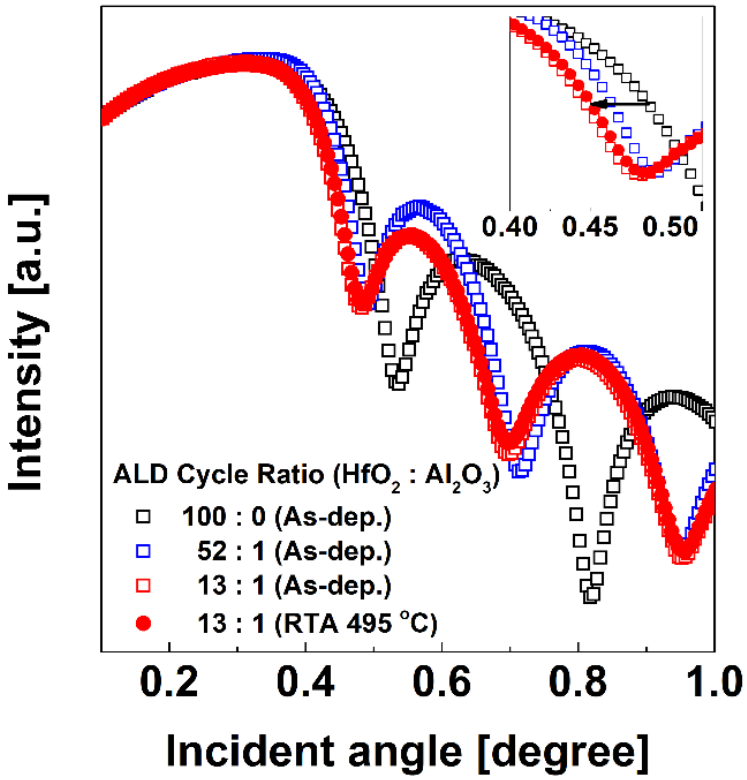


Figure 6.9. The XRR results of Al:HfO_2 film according to ALD cycle ratio between HfO_2 and Al_2O_3.

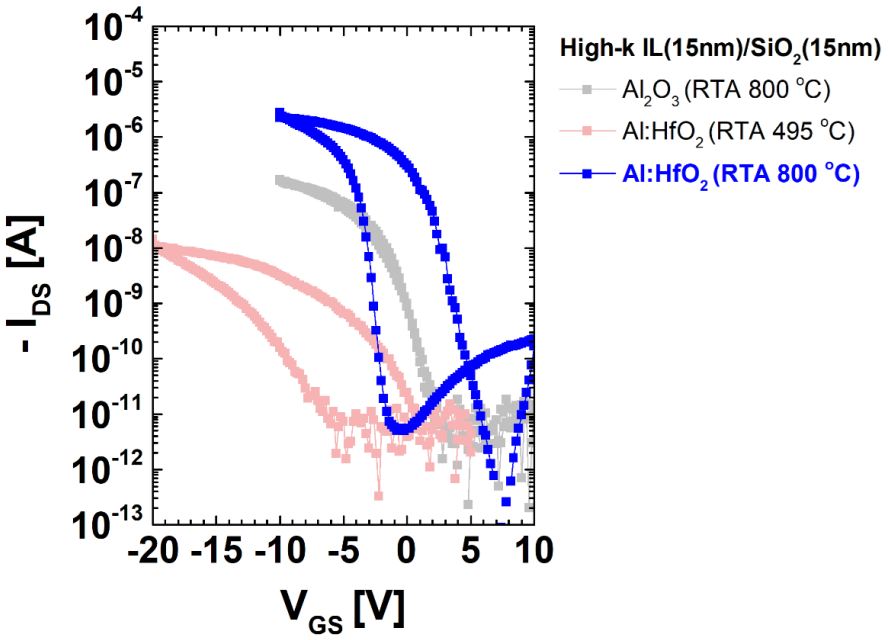


Figure 6.10. The transfer characteristics of SnO TFT with different condition of IL. The Al_2O_3 IL was underwent RTA at 800 ℃ and the Al:HfO_2 IL was underwent RTA at 495 and 800 ℃, respectively.

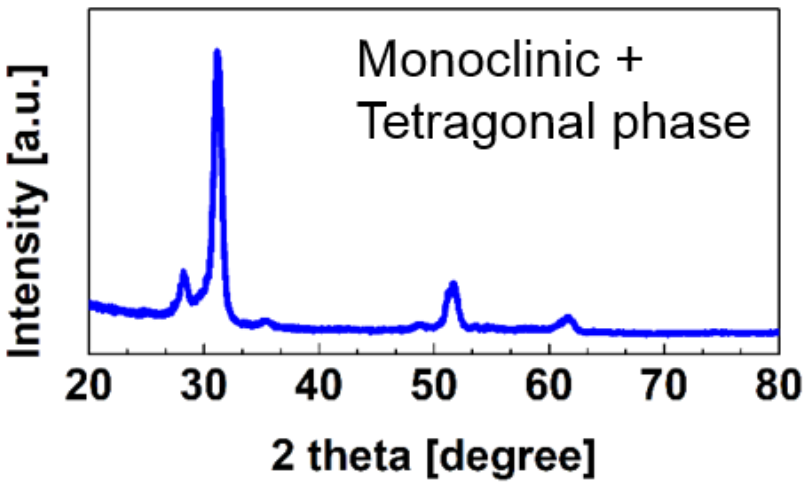


Figure 6.11. The GAXRD results of Al:HfO_2 IL underwent RTA at 800 ℃.

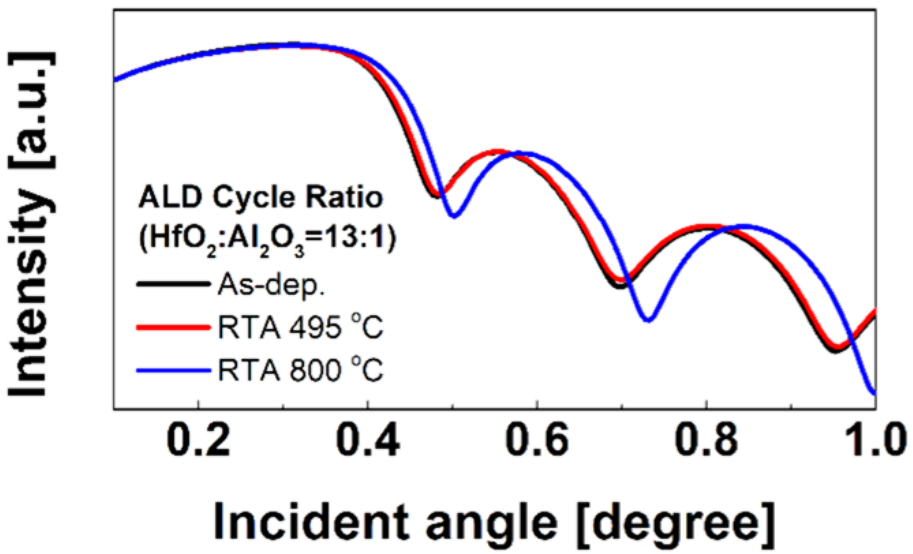


Figure 6.12. The XRR results of Al:HfO_2 film according to RTA temperature.

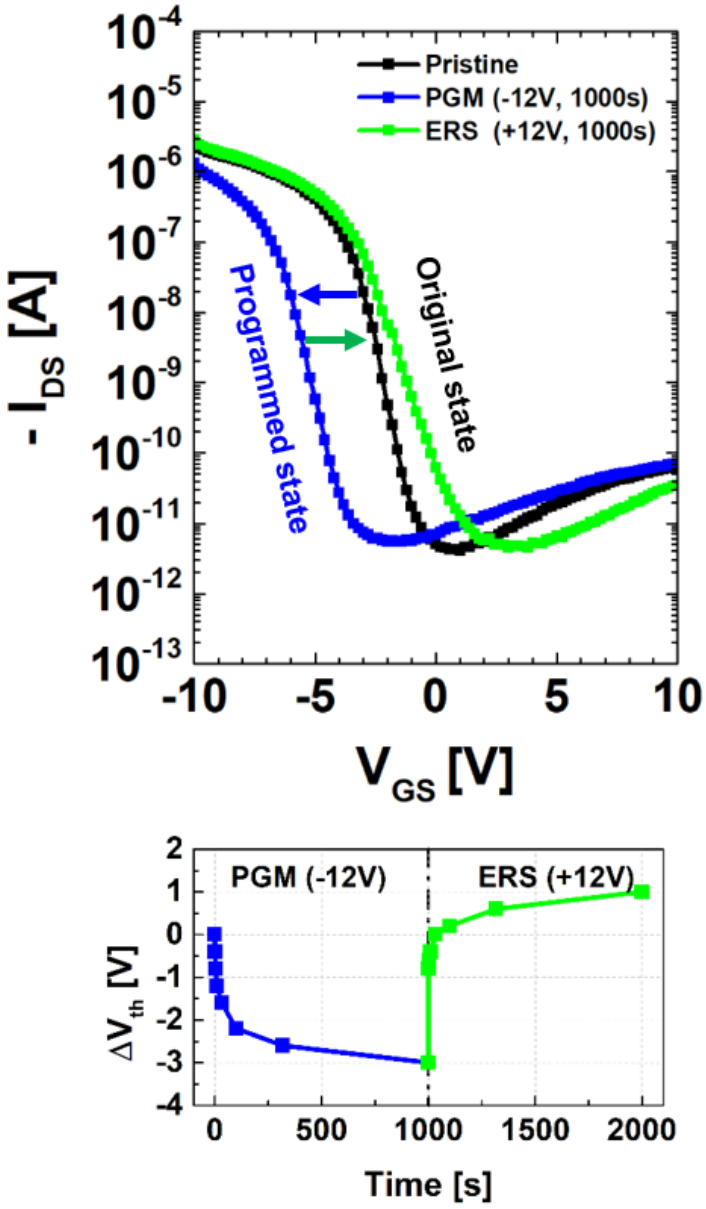


Figure 6.13. The memory characteristics of programming operation for the SnO/Al:HfO_2 (RTA 800 ℃)/SiO_2 stacked TFTs.

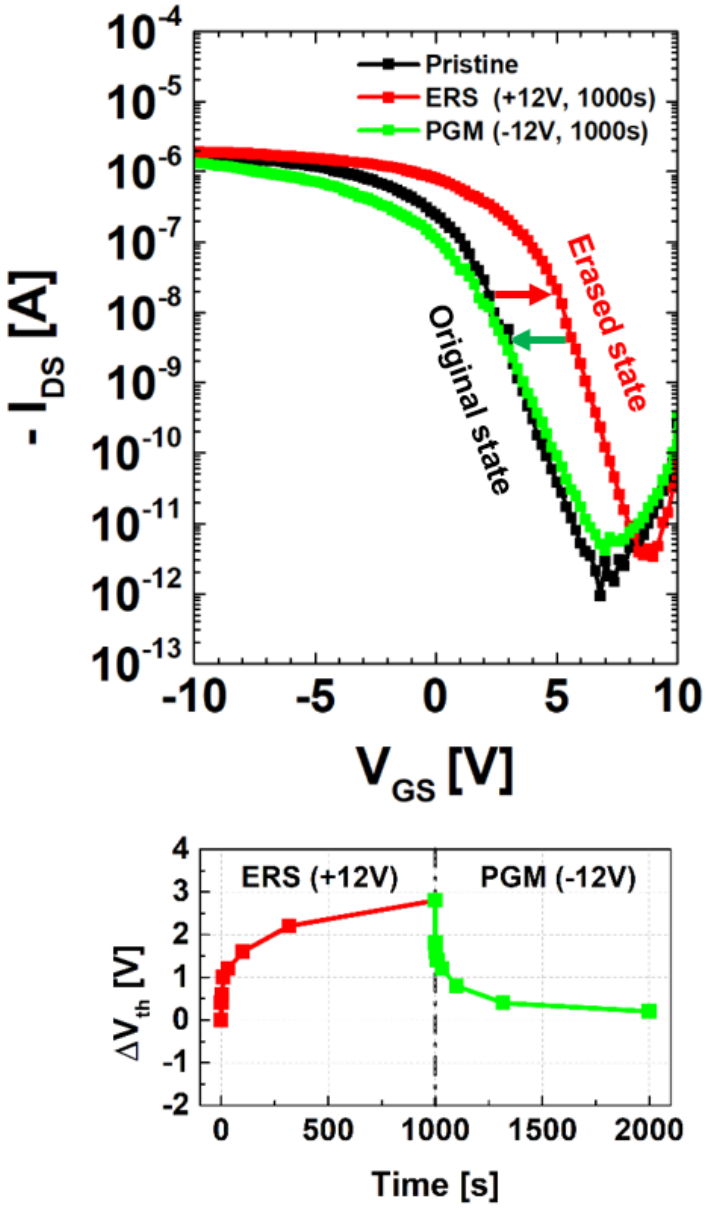


Figure 6.14. The memory characteristics of erase operation for the SnO/Al:HfO_2 (RTA 800 ℃)/SiO_2 stacked TFTs.

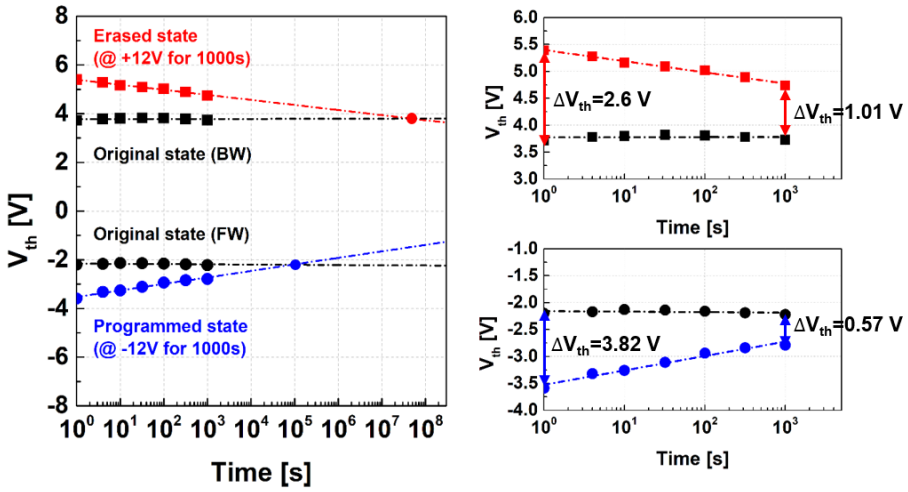


Figure 6.15. The retention characteristics of programming and erase operation for the SnO/Al:HfO_2 (RTA 800 ℃)/SiO_2 stacked TFTs.

6.2. Bibliography

[1] H. Kim, P. C. McIntyre, K. C. Saraswat, *Appl. Phys. Lett.* **2003**, *82*, 106.

[2] D. Triyoso, R. Liu, D. Roan, M. Ramon, N. V. Edwards, R. Gregory, D. Werho, J. Kulik, G. Tam, E. Irwin, X.-D. Wang, L. B. La, C. Hobbs, R. Garcia, J. Baker, B. E. White, Jr., P. Tobin, Journal of The Electrochemical Society **2004**, *151*, F220.

[3] H. -S. Jung, J. H. Jang, D. -Y. Cho, S. -H. Jeon, H. K. Kim, S. Y. Lee, C. S. Hwang, *Electrochem. Solid-State Lett.* **2011**, *14*, G17

[4] X. Liu, L. Yao, Y. Cheng, B. Xiao, *Jpn. J. Appl. Phys.* **2019**, *58*, 090903.

[5] W. Zhu, T. P. Ma, T. Tamagawa, Y. Di, J. Kim, R. Carruthers, M. Gibson, T. Furukawa, *IEEE International Electron Device Meeting* **2001**, *01*, 463.

[6] Y. Lee, W. Jeon, Y. Cho, M. -H. Lee, S. -J. Jeong, J. Park, S. Park, *ACS Nano* **2016**, *10*, 6659.

[7] P. Stallinga, *Electrical Characterization of Organic Electronic Materials and Devices*, John Wiley and Sons, Ltd, **2009**.

[8] Y. Ogo, H. Hiramatsu, K. Nomura, H. Yanagi, T. Kamiya, M. Kimura,

M. Hirano, H. Hosono, *Phys. Status Solidi A* **2009**, *9*, 2187.

[9] H. Hosono, Y. Ogo, H. Yanagi, and T. Kamiya, *Electrochem. Solid-State Lett.* **2011**, *14*, H13.

[10] J. Wang, N. Umezawa, H. Hosono, *Adv. Energy Mater.* **2016**, *6*, 150119.

[11] N. F. Quackenbush, J. P. Allen, D. O. Scanlon, S. Sallis, J. A. Hewlett, A. S. Nandur, B. Chen, K. E. Smith, C. Weiland, D. A. Fischer, J. C. Woicik, B. E. White, G. W. Watson, L. F. J. Piper, *Chem. Mater.* **2013**, *25*, 3114.

[12] L. Y. Liang, H. T. Cao, X. B. Chen, Z. M. Liu, F. Zhuge, H. Luo, J. Li, Y. C. Lu, W. Lu, *Appl. Phys. Lett.* **2012**, *100*, 263502.

[13] H. Luo, L. Liang, H. Cao, M. Dai, Y. Lu, M. Wang, *ACS Appl. Mater. Interfaces* **2015**, *7*, 17023.

[14] S. Chen, W. P. Zhang, X. M. Cui, S. J. Ding, Q. Q. Sun, W. Zhang, *Appl. Phys. Lett.* **2014**, *104*, 103504.

[15] Y. Li, Y. Pei, R. Hu, Z. Chen, Y. Ni, J. Lin, Y. Chen, X. Zhang, Z. Shen, J. Liang, B. Fan, G. Wang, H. Duan, IEEE Trans. Electron Devices 2015, 62, 1184

[16] J. S. Kim, S. Kang, Y. Jang, Y. Lee, K. Kim, W. Kim, W. Lee, C. S.

Hwang, *Phys. Status Solidi RRL* **2021**, 2000549

[17] J. Kim, J. Bang, N. Nakamura, H. Hosono, *APL Mater.* **2019**, *7*, 022501.

[18] K. Ide, K. Nomura, H. Hosono, T. Kamiya, *Phys. Status Solidi A* **2019**, 5, 1800372

[19] Kenji Nomura, *SID Symposium Digest of Technical Papers*, **2015**, *1*, 591.

7. Conclusion

In this dissertation, SnO TFTs with SiO_2 GI exhibit a large V_{hy} due to the trap state density near the interface between the SnO active layer and the SiO_2 GI. Both experimental results and theoretical calculations show that the origin of border traps is the Sn_{Si}^{+0} gap states in SiO_2, which is induced by the Sn diffusion into the SiO_2 layer. The maintenance of the amorphous phase, thickness, and density of the Al_2O_3 ILs was identified to have crucial effects on hysteresis reduction. This is the first report to propose a method to reduce hysteresis by suppressing Sn diffusion.

For in-depth analysis, influence of the ionic-charge ($V_O^{\cdot\cdot}$) effect within the Al_2O_3 layer on the p-type SnO based device performance was evaluated. Reduced V_{hy} and stable V_{th} of SnO TFTs could be obtained by effects on V_{GS} dependence of $V_O^{\cdot\cdot}$. The introduction of an Al_2O_3 layer suppresses the electron and hole trapping at the channel/dielectric interface and contains mobile $V_O^{\cdot\cdot}$ that counteract the hole trapping effect. A large displacive current was measured by effects on I_G characteristics. It was confirmed that charge transfer through the gate dielectric is affected by the $E_{int.}$ created by $V_O^{\cdot\cdot}$. Additional capacitance in BW sweep was revealed that the results from the effects of $V_O^{\cdot\cdot}$ migration. The hole trapping/de-trapping is active or inactive for AC stimulus according to dragged $V_O^{\cdot\cdot}$'s position. By understanding the abnormal electrical properties induced by ILs, a new perspective on IL insertion mechanism through various

in-depth analysis.

By adopting an Al:HfO_2 film as ILs, extremely high μ_{FE} and low SS of SnO TFTs was obtained due to high dielectric constant of high-k-based IL. Although a large V_{hy} (6.4 V) was shown when the crystallized Al:HfO_2 IL was adopted, it demonstrated electrical programmable and erasable characteristics as well as data retention capability. This result shows the possibility of expanding application fields according to IL materials of SnO TFTs.

Abstract (in Korean)

본 학위논문에서는 차세대 반도체 채널 및 유전막 물질에 대한 연구 기술 확보를 목표로, 단원자 증착법 (Atomic Layer Deposition, ALD) 기반 고품질의 p형 산화 주석 (SnO) 박막을 적용한 박막 트랜지스터 (Thin-Film Transistor, TFT) 소자의 전기적 특성 향상에 관한 연구를 수행하였다. 이를 위해, 열화 현상 평가와 원인 규명을 통한 소자의 전기적 안정성 분석 및 특성 개선 방안에 관한 연구를 진행하였다.

첫째로, ALD p형 SnO TFT소자 구동 시 확인되는 히스테리시스 (hysteresis) 거동의 원인 분석을 위해, 계면층 (interfacial layer, IL) 삽입 실험을 진행하였다. 열산화 SiO_2 게이트 절연막 (gate insulator, GI)과 SnO 채널막 간의 계면 반응과 원자의 상호 확산을 억제하기 위해, IL로서 ALD Al_2O_3 박막을 두 물질 사이에 삽입하였다. 계면층이 없는 SnO TFT 소자의 경우 큰 GI과 SnO 채널막 계면에서의 트랩 밀도에 의해 높은 히스테리시스 전압 (V_{hy})을 보였다. 실험 결과 및 이론적 계산을 통해, 이러한 계면 트랩은 GI으로의 Sn 확산에 따라 절연막 내 Sn_{Si}^{+0} 갭 상태에 의한 것으로 확인하였다. Al_2O_3를 IL로 채택하면서 Sn의 확산 방지층으로서 사용되었으며, IL의 두께, 결정성, 밀도에 따라 그 효력이 달라졌다. 연구 결과, 급속 열처리 (rapid thermal annealing, RTA) 후 Al_2O_3 IL의 비정질 구조가 유지되는 한, IL의 두께와 밀도가 증가할 때 SnO TFT의 V_{hy}는 감소하였다. 그리고 결정성 IL의 경우 Sn 확산 억제 특징을 잃어버렸다. p형 ALD SnO TFT에 최적 조건의 IL을 도입한 경우 히스테리시스 전압을 0.2 V까지 크게 낮춤과 동시에 on/off 전류비(1.2×10^5), 전계 이동도 ($1.6\ cm^2 V^{-1}s^{-1}$) 측면에서도 우수한 TFT 소자 성능을 확보할 수 있었다.

둘째로, SnO TFT 소자의 Al_2O_3 IL 삽입 시 나타나는 비정상적 전기적 특성을 조사하였다. IL 내부의 이동성 산소 공공(oxygen vacancy,

V_O)이 게이트 전압 의존성, 게이트 전류 특성 및 커페시턴스 특성에 미치는 영향에 대해 분석하였다. SnO TFT 소자의 동작 특성 중 V_{hy} 및 문턱 전압 (threshold voltage, V_{th})는 스윕 범위와 게이트 전압 속도에 의존하였다. Al_2O_3 IL을 삽입한 TFT 소자의 경우, 이전보다 V_{hy}를 낮출 수 있었으며 안정적인 V_{th}를 나타냈다. SnO 채널막과 GI 사이에 IL을 도입하여, 계면에서 전자 트랩핑을 막아줄 뿐 아니라 IL 내부에 존재하는 V_O가 정공 트랩핑에 대응하는 효과 때문이다.

Al_2O_3 IL 내부의 V_O로부터 또 하나의 비정상적 거동을 보이는 게이트 전류가 비롯된다. IL 내부의 V_O의 전계 유도 이동으로 매우 큰 I_{GS}가 관찰된다. V_O는 외부 전기장과 균형을 이루는 내부 전기장을 형성할 수 있다. 이로써 게이트 유전체를 통한 전하 전달이 영향을 받아, 공핍 영역에서의 채널 전류보다 게이트 누설이 우세해질 수 있는 것이다. 결과적으로 I-V와 C-V의 히스테리시스 방향은 서로 일치하지 않는다.

Al_2O_3 IL 내부 V_O로부터 비롯되는 마지막 비정상적 특성은 커페시턴스 특성에 반영되는데, 이는 특정 전압에서 추가적인 커페시턴스가 관찰되는 것이다. 충분히 음의 게이트 전압인가 시, V_O는 Al_2O_3/SiO_2 계면으로 끌려가, 축적 영역에서 AC 자극에의 반응성 (정공 트랩핑/디트랩핑) 비활성화 상태가 된다. SnO 밴드갭 내 V_O의 에너지 준위가 가전자대에 인접하여, 축적 영역에서 정공 트랩핑에 의해 추가적인 커페시턴스가 발생하는 것으로 보인다. 하지만 게이트 전압이 더욱 감소하면, V_O가 Al_2O_3/SiO_2 계면으로 다시 이동하게 되어 추가 커페시턴스 효과를 없애게 된다.

셋째로, TFT 소자의 전달 특성 향상을 확보하고자 Al_2O_3 박막을 대체하는 고유전율의 Al 도핑된 HfO_2 박막을 IL로 적용하고, 해당 소자의 전기적 특성을 평가하였다. Al 도핑 시 HfO_2 박막의 결정화를 억제할 수 있으나, 박막 밀도에 방해가 되어 SnO TFT 소자 성능을 악화시킨다. 반면, 결정성의 Al 도핑된 HfO_2 박막을 IL로 도입 시, 큰 V_{hy}를 보이지만 높은 유전 상수 (ε_r=26) 덕분에 우수한 TFT 소자

성능을 보인다 (μ_{FE}= 5.7 $cm^2/V{\cdot}s$, SS= 0.39 V/dec., I_{on}/I_{off}= 5.6×10^5). 이러한 특성으로 이용하여 SnO/Al:HfO_2/SiO_2 적층 TFT의 메모리 소자로서의 동작 가능성을 평가한 결과, 프로그래밍 된 상태 (또는 지워진 상태)와 원래 초기 상태 사이의 전환 특성을 관찰할 수 있었다. 이를 통해, 다른 계면층 물질에 따라 다른 히스테리시스 특성을 보이는 SnO 박막 트랜지스터를 전자 회로 소자뿐 아니라 메모리 소자로도 적용할 수 있을 것으로 기대된다.

주요어: p형 주석 산화물 (SnO), 단원자 증착법, 산화물 박막 트랜지스터, 계면층 삽입, 확산 방지층, 고유전체 절연막, 히스테리시스 전압, 문턱 전압, 계면 결함, 전하 트래핑, 산소 공공, 이온 전하 효과

학번: 2014-21554

장 윤 진