Ph.D. DISSERTATION

Nano-wedge RRAM Cross-point Array with Nickel Silicide Bottom Electrode as a Synaptic Device for Neuromorphic Computing Applications

시냅스 소자 적용을 위한 니켈 실리사이드 웨지구조를 가지는 저항변화 메모리 어레이

BY

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이 논문을 공학박사 학위논문으로 제출함

2021 년 2 월

서울대학교 대학원

전기정보공학부

이 동 근

이동근의 공학박사 학위논문을 인준함

2021 년 2 월

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Abstract

Advancement of Internet of Things (IoT) and artificial intelligence (AI) boosted the development of next-generational computing system – neuromorphic computing. Also referred to as brain-inspired computing, unlike currently used von Neumann architecture that processes data sequentially, this technology is able to handle huge amount of data in parallel by integrating the role of processor and memory simultaneously. Not limited to the parallel processing capability, utilizing the neuromorphic computing system would pave the way for efficient solutions to the field of automotive, healthcare and consumer electronics industries. In order to meet an expectation of next-generation in-memory computing technology, numerous research facilities deal with state-of-the-art devices that could be implemented with a hardware-driven architecture. Resistive Random Access Memory (RRAM) has been widely investigated as one of possible candidates for synaptic devices by taking advantages of its scalability, CMOS compatibility and simple structure. Using various switching materials make RRAM device attractive

in terms of optimizing the energy efficiency for neural network application. Conventional metal-insulator-metal (MIM) structure has higher reliabilities to function as the synaptic device, yet comparatively high current level reaching a few mA limits RRAM to expand to large size cross-point array. To solve this problem, metal-insulator-silicon (MIS) structured RRAM device has been given attention for its relatively low current level, which suits for low power operation of neuromorphic computing system.

In this dissertation, Nickel silicided (NiSi) nano-wedge RRAM array was fabricated for potential application as a synaptic device. Instead of having highly-doped Si bottom electrode (BE), NiSi has relatively lower resistivity which lead to decreased switching power consumption. Performing neural network requires a large size cross-point array operating at low energy. Utilizing NiSi BE nano-wedge RRAM not only reduce the total power, but metallic BE improves the switching reliability issues. Furthermore, NiSi BE wire in the cross-point array has largely reduced a wire resistance, which is essential during a vector-matrix multiplication (VMM) to guarantee high accuracy of data recognition. Based on fabricated nano-

wedge RRAM array having both Si and NiSi BE, we performed a current summation and obtained improved results with less current loss from NiSi BE array. In addition, SPICE simulation was carried out to analyze the optimized ratio between the cell and wire resistance in order to minimize the current loss. Reduction of wire resistance by using NiSi BE on nano-wedge RRAM array not only achieved an improvement of switching parameters, it showed a feasibility of hardware implemented synaptic device for neuromorphic computing application.

Keywords: Synaptic devices, resistive random access memory, in-memory computing, NiSi nano-wedge RRAM array, wire resistance, vector-matrix multiplication

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Contents

List of Figures

List of Tables

Chapter 1
Introduction

1.1 Background

Growing demand for fast and connected communication accelerates a transformation from the von-neumann architecture to parallel in-memory computing as the capacity of data utilization is explosively reaching its limitation [1]. Since a sequential computing system that exchanges data between cpu and memory has confronted with scaling issues of CMOS transistors, next-generation memory is under the extensive research to replace the current CMOS logic [2]. One of rising technologies to replace the current computing system is biomimetic neural network that processes the data in parallel. This does not only

take advantages of areal overheard issues, huge amount of data from Internet of Things (IoT) and artificial intelligence (AI) applications could be handled in fast speed without bottleneck. In order to achieve this state-of-the-art system, synapse devices implemented between pre- and post-neurons are essential to carry out the parallel operations. Resistive random access memory (RRAM) has been received as one of promising candidates to replace current sequential logic processors for the synaptic device applications due to its simple structure, CMOS compatibility and fast speed [3-8]. Fig. 1.1 illustrates the biological neural network and principles of electronic synaptic device, respectively. The purpose of synaptic device utilization is to achieve target weights of synapse array by controlling its conductance. Conventional metal-insulator-metal (MIM) structure is the well-known stack which have been reported for synaptic device applications [9-11]. Fig. 1.2 shows RRAM-based cross-point array optimized for neural network systems. As depicted in the Fig. 1.3, input pulses are applied to each word line of the RRAM cross-point array with pre-transferred weights

from the software training, thereby measuring the output current from bit line through vector-matrix multiplication (VMM). The VMM is simply the multiplication of input voltage and conductance of RRAM

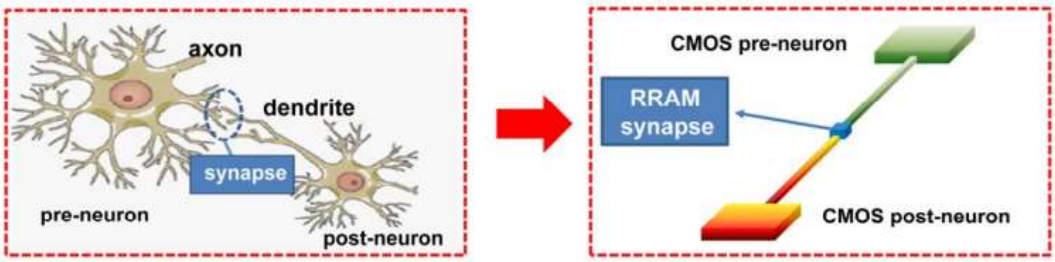


Fig. 1.1. Biological synapse between pre- and post- neurons (left) and electronic synaptic device using an RRAM device (right) [12].

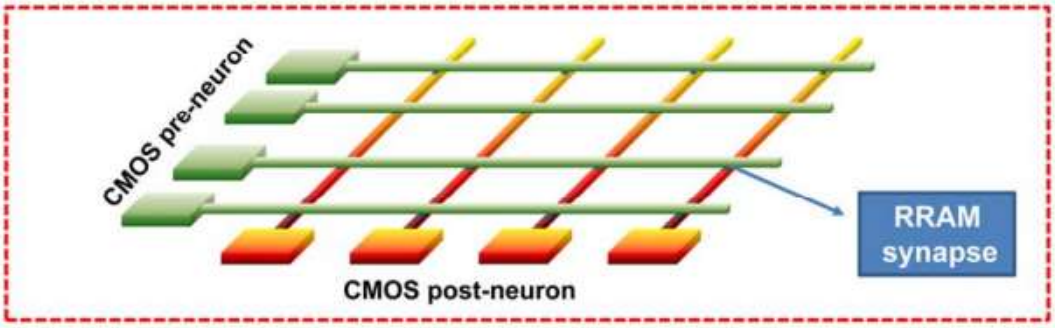


Fig. 1.2. Schematic of RRAM based cross-point array [12].

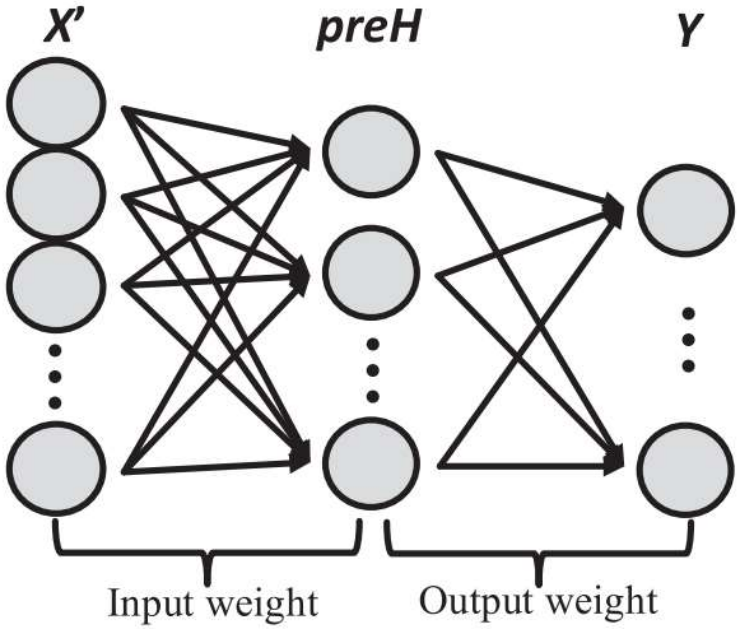


Fig. 1.3. Schematic of synapse based neural network. Input signals from X' are multiplied with pre-transferred synaptic weights, which are then transferred to the output Y to compare with the actual values [13].

array to achieve the current summation [14-16]. Yet, one of intrinsic issues of the MIM RRAM devices is its high current level that prohibit its expansion to the ultra-high density cross-point array. According to Fig. 1.4, average current

level of MIM RRAM devices reaches up to a few mA, which is unrealistic for low power operation of neuromorphic computing application. Reliability issues are another key factors that limiting the commercialization of RRAM devices [17, 18].

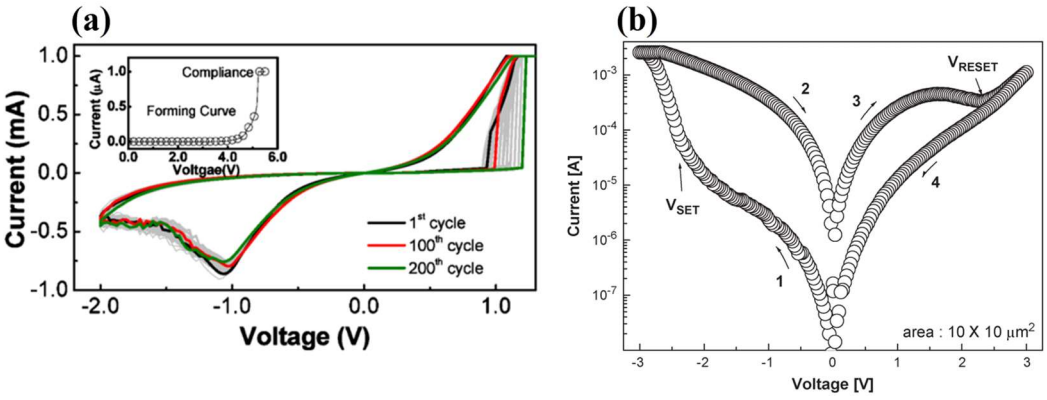


Fig. 1.4. DC I-V curves of the Al/TiO_x/TiO_2/Al (a) and Ti/TiO_2/Pt (b) RRAM where both stacks have metal electrodes [19, 20].

1.2 Silicon BE RRAM as a synaptic device

In order to solve typical issues of MIM RRAM device, metal-insulator-silicon (MIS) RRAM devices have been introduced by Kim. *et. al.* [21-25]. According to reported literatures, Si bottom electrode (BE) not only exhibits low current and thus reducing the switching power, the fabrication process of MIS RRAM device has full compatibility with existing CMOS logic, indicating that there is not necessary for extra cost. Conduction mechanism as well as switching characteristics of Si BE RRAM device proved its superiorities to fit in as large-size cross-point array. Another important aspect when considering RRAM device for hardware-implemented synaptic device is the gradual properties [26-28]. This features are required when operating analog tuning of RRAM based synaptic devices in order to maximize the accuracy of data recognition rates such as MNIST and CIFAR-10. As demonstrated in [29], a highly-doped n^+-Si showed gradual switching characteristics in both DC and

pulse measurement. It has shown that the gradual switching characteristics are also depending on pulse widths and amplitudes [30].

Chapter 2
Si nano-wedge RRAM device

2.1. Electrical characteristics of planar RRAM device with Si bottom electrode

For thorough analysis of metal-insulator-silicon (MIS) RRAM device, we fabricated the Si bottom electrode (BE) RRAM device with the structure of TiN/HfO_2/SiO_2/p^+-Si. Prior to scale down the device size, simple planar RRAM device with the size of 100 μm × 100 μm was fabricated as depicted in Fig. 2.1.

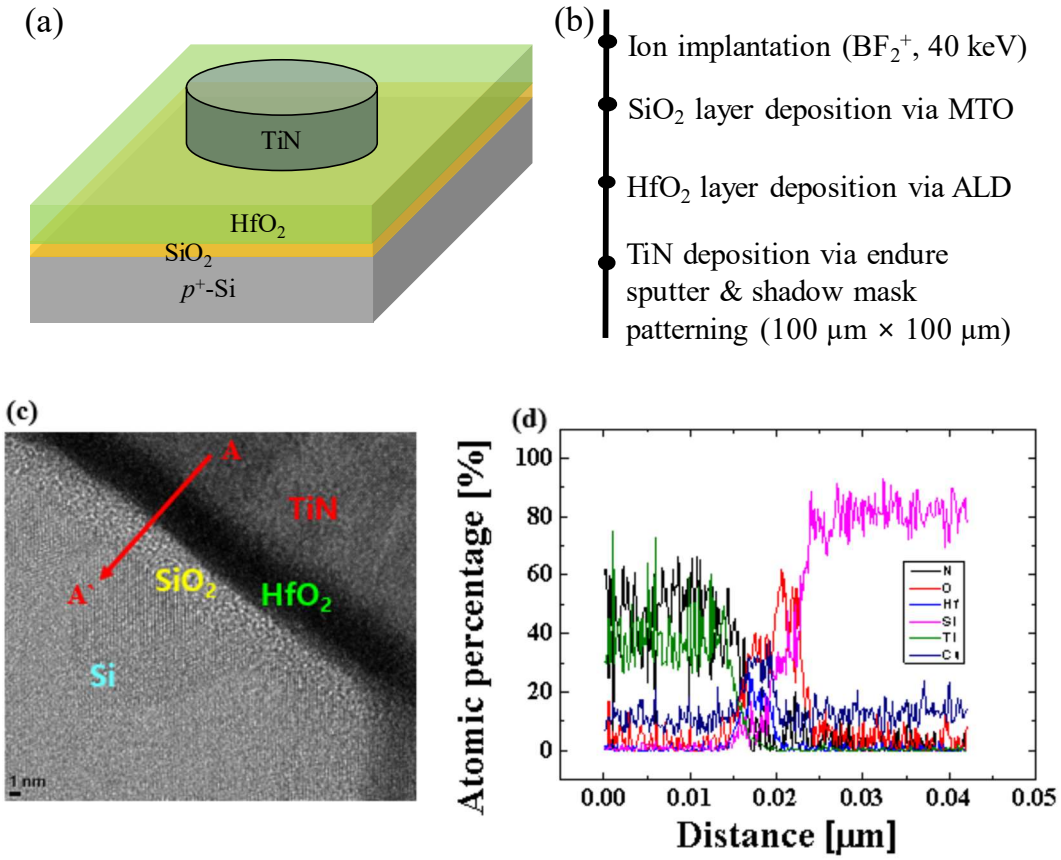


Fig. 2.1. (a) Schematic of the fabricated RRAM device with tunneling barrier layer (SiO_2) insertion and (b) process flow of TiN/HfO_2/SiO_2/p^+-Si RRAM device fabrication. Cross-sectional TEM image of the fabricated device (c) and Energy Dispersive Spectroscopy (EDS) analysis of taken TEM image (d).

The schematic of fabricated RRAM device consists of TiN (top electrode, TE), HfO_2 (switching layer), SiO_2 (tunneling barrier layer) and boron doped Si BE. The purpose of tunneling barrier layer insertion is to increase the nonlinearity of the I-V curve, thus leakage current under the low bias could be suppressed [31, 32]. As shown in the Fig. 2.1 (b), the process flow of the planar RRAM device fabrication is as follow: implantation of BF_2^+ ions with dose of 5×10^{15} cm^{-2} and energy of 40 keV was carried out, which is followed by deposition of SiO_2 layers using Medium Temperature Oxidation (MTO) equipment. The thicknesses of SiO_2 were split into three: 1.5 nm, 1.9 nm and 2.4 nm for the comparison of nonlinearities. The RRAM device without the SiO_2 layer was also fabricated as the control one. Next, HfO_2 (4.4 nm) as the switching layer was deposited by the Atomic Layer Deposition (ALD). For the TE, TiN with the thickness of 100 nm was deposited via the Endura Sputter. The pattern of circular RRAM was acquired by the insertion of shadow mask right before the TE deposition. Fig. 2.1 (c) represents the taken TEM image of the

fabricated RRAM device and EDS component analysis is shown in (d). It is clear that each component is located at its corresponding spot.

In order to investigate the electrical characteristics of the fabricated device, DC measurement was carried out and the results are illustrated in the Fig. 2.2. For the purpose of comparison, electrical characteristics of the RRAM devices with and without the tunneling barrier layer were measured. The compliance current (I_{CC}) applied to the RRAM devices were 1 mA and 300 μA. Fig. 2.2 (a) shows the I-V curves of TiN/HfO_2/p^+-Si while Fig. 2.2 (b) is the I-V curve of TiN/HfO_2/SiO_2/p^+-Si. It is clearly seen that the leakage current (during the initial forming process) is much lower in the RRAM device with the SiO_2 layer insertion. This is attributed to an effect of higher bandgap of SiO_2 (~ 9.2 eV) compared to that of HfO_2 (~ 5.5 eV), making electrons difficult to jump over the barrier of SiO_2. This led to an increased nonlinearity of SiO_2-inserted RRAM device which is defined below:

$$\frac{\mathrm{I@V_{READ}}}{\mathrm{I@\frac{1}{2}V_{READ}}}$$

where ‘I’ represents the current at the applied read voltage (1 V).

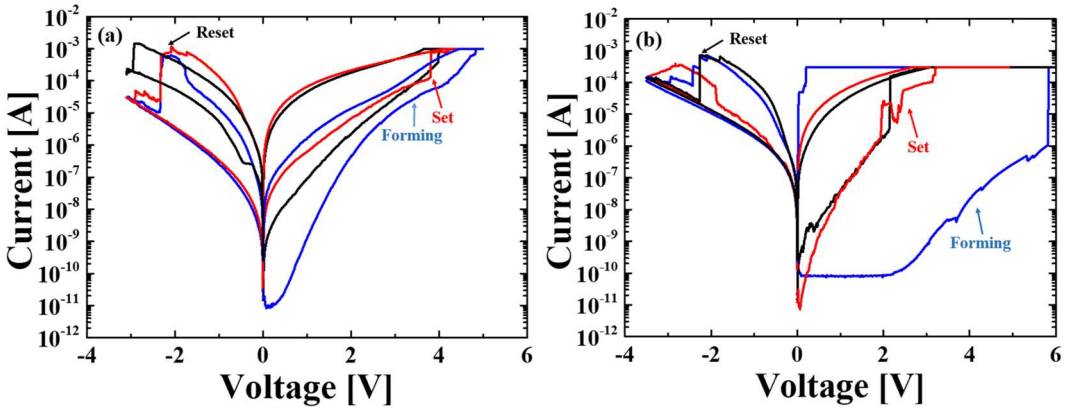


Fig. 2.2. (a) Measured DC I-V characteristics of TiN/HfO_2/p^+-Si and (b) TiN/HfO_2/SiO_2/p^+-Si, respectively.

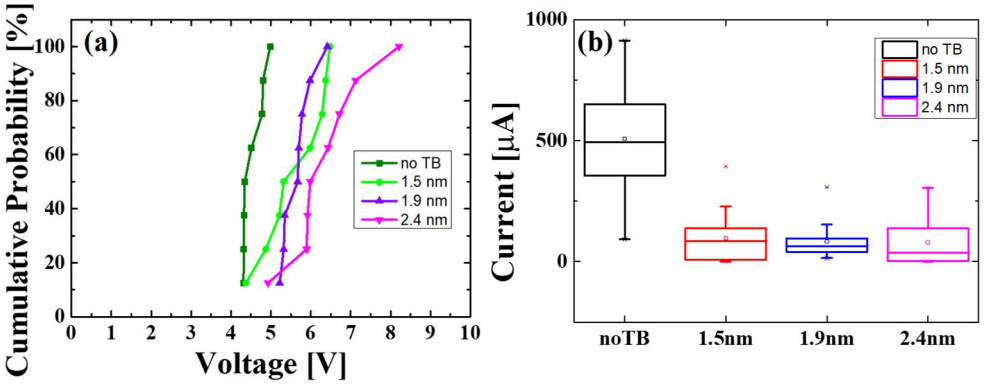


Fig. 2.3. (a) Distribution of $V_{FORMING}$ and (b) I_{ON} at V_{READ} = 1 V.

In order to compare the forming voltage among the fabricated RRAM devices with and without the SiO_2 layers, statistical distribution of $V_{FORMING}$ and on current (I_{ON}) during the low resistance state (LRS) were plotted in Fig. 2.3. Data in the Fig. 2.3 (a) show that the forming voltage increases as the thicknesses of SiO_2 layer increases, indicating more electric field is required to breakdown the tunneling barrier layers. Furthermore, on current in LRS is getting lower as the SiO_2 layer thicknesses increase (Fig. 2.3 (b)) which concludes that electron tunneling distance increased. Nonlinear factors were calculated according to the definition mentioned above and plotted in Fig. 2.4. Compared to the RRAM device with the tunneling barrier layer, the one without it has the lowest nonlinearity, suggesting the inability of single switching layer (HfO_2) to inhibit the current levels at low bias. Thicker SiO_2 layer may increase the nonlinear factors, but there needs an optimized thickness since larger switching voltages may be required in case the TB is deposited as thick as the switching layer.

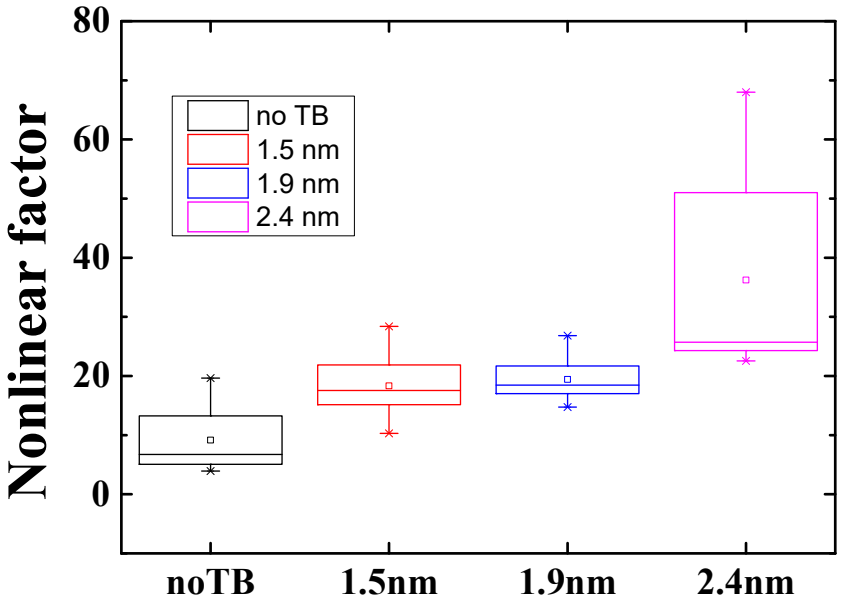


Fig. 2.4. (a) Nonlinear factors of the planar Si BE RRAM device with and without the tunneling barrier (TB) layers. As the thickness of TB increases, the value of nonlinearity also increases.

2.2. Novelty of wedge-structure

2.2.1. Scaling effect

One of critical issues arising from the planar RRAM device is its high current from unexpected path within the switching layer [33-35]. As shown in Fig. 2.5, it represents the typical DC I-V characteristics of RRAM device with Ni/HfO_2/p^+-Si structure. By setting the compliance current to 100 μA, the maximum current level goes beyond the mA, which is a huge current level to apply for the synaptic device application [36-39]. Fig. 2.6 reveals the transient effect of set (a) and reset (b) pulses during the switching processes. Although the switching speeds are fast enough compared to existing NAND Flash memories [40], the maximum current reaches to 1.5 mA which is not practical solution for hardware-implemented neuromorphic computing architecture. To solve this issue, it is essential to fabricate RRAM devices with low current operating at reliable conditions. Fig. 2.7 depicts the effect of RRAM cell scaling. $V_{FORMING}$ has been increased from 1 V to 2.8 V as the cell size scales from 10^{-8}

m^2 to 10^{-14} m^2.

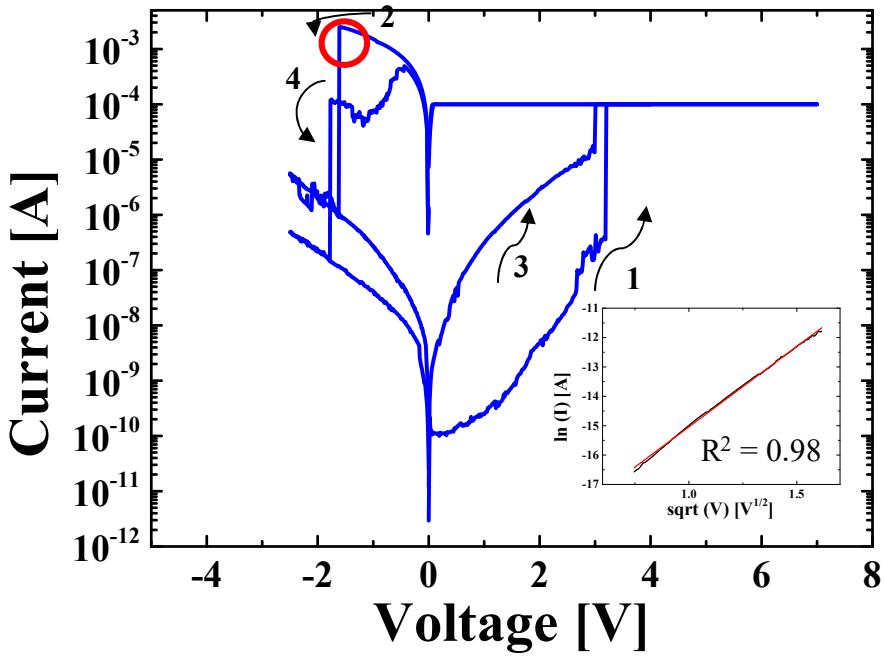


Fig. 2.5. DC I-V of Ni/HfO_2/p^+-Si. Indicators are the sequences of forming, reset and set switching process. The maximum current level reaches up to a few mA. Inset figure is the fitting of schottky emission during the HRS conduction.

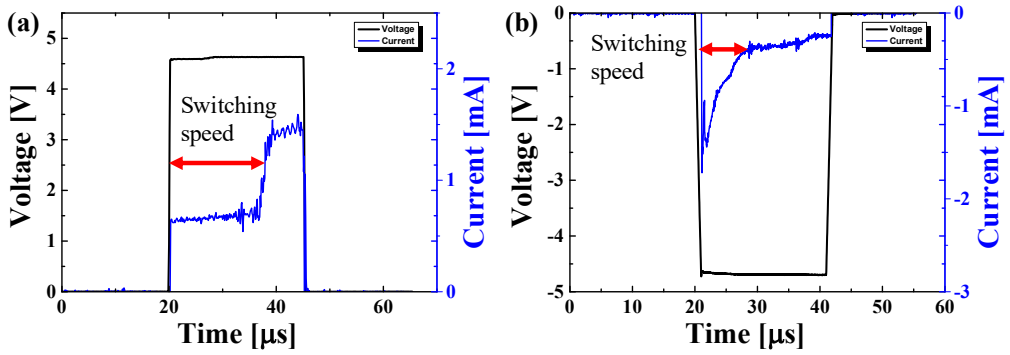


Fig. 2.6. Pulse characteristics of the fabricated Ni/HfO_2/p^+-Si. (a) is the set switching transient while (b) represents the reset switching. The switching speed is around a few microseconds.

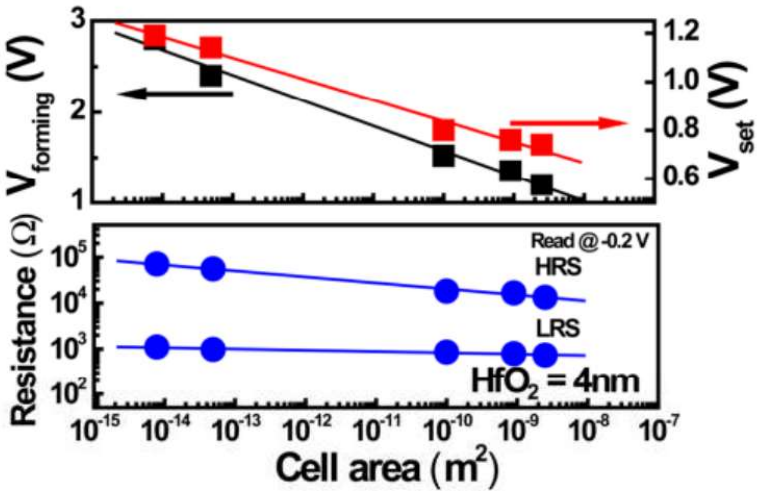


Fig. 2.7. Change of $V_{forming}$, V_{set} and cell resistance with respect to the scaling of RRAM cell area [41].

V_{set} has also been increased 0.7 V to 1.2 V. This is attributed to higher electric field required to induce vacancies within the switching layer of RRAM devices, where the vacancies eventually form the conductive filament to flow electrons. For the cell resistance, scaling the cell size reduces the current level or increases the resistive states. Fig. 2.7 proves the increase of cell resistance. This demonstrates the current level decreases as the cell size scales down and deemed as the key factor to utilize RRAM device as electronic synapses [42].

Scaling method of MIM RRAM device is difficult in a sense that metal is not suitable for CMOS fabrication. To solve this problem, scaling Si BE has been regarded as an alternative to replace MIM RRAM device. Existing scaling method includes sidewall etching or e-beam lithography that could scales the Si down to sub 100 nm. Yet, sidewall etching has complicated fabrication process that costs much. E-beam lithography also has issues of mix and match process, which plays as a bottleneck between the cell scaling and pad lithography. It is also an expensive process that may not be ideal for massive production.

2.2.2. Fabrication process of Si nano-wedge RRAM

In alternative to mentioned scaling technologies, wet-etching of Si fin using an anisotropic wet etchant is deemed to be a simple fabrication process. In detail, Tetramethylammonium hydroxide (TMAH) with 25% solution is an anisotropic wet-etchant that etches the Si fin. Fig. 2.8 illustrates the distance etched (left) and temperature-dependent etch rate (right). Fig. 2.9 is the taken Scanning Electron Microscopy (SEM) image after formation of Si fin structure with a width of 500 nm (± 10% error). The left side of Fig. 2.9 is the wedge structure that has been obtained by dipping the wafer into the TMAH solution for 9 minutes while the one in the right has been dipped for 9.5 minutes. It could be known that, as the wet etching time increases, direction-dependent Si fin could be shaped into tip structure.

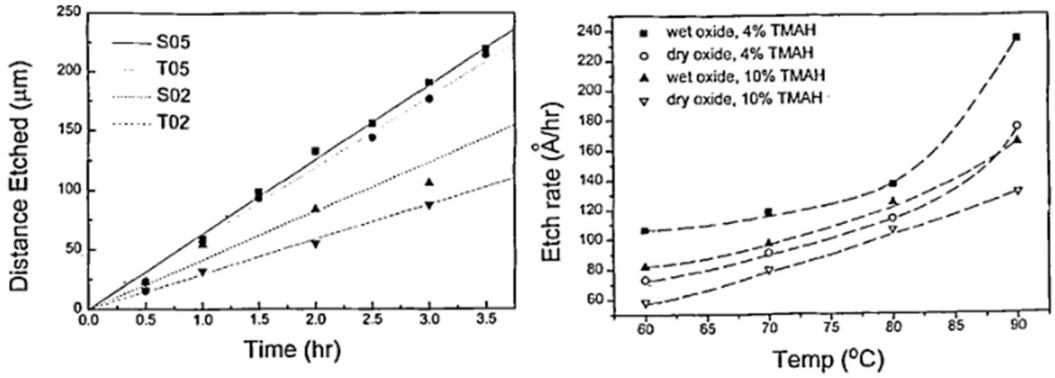


Fig. 2.8. Relation between distance etched vs. time (left) and etch rate vs. temperature of TMAH anisotropic wet etching process (right) [43].

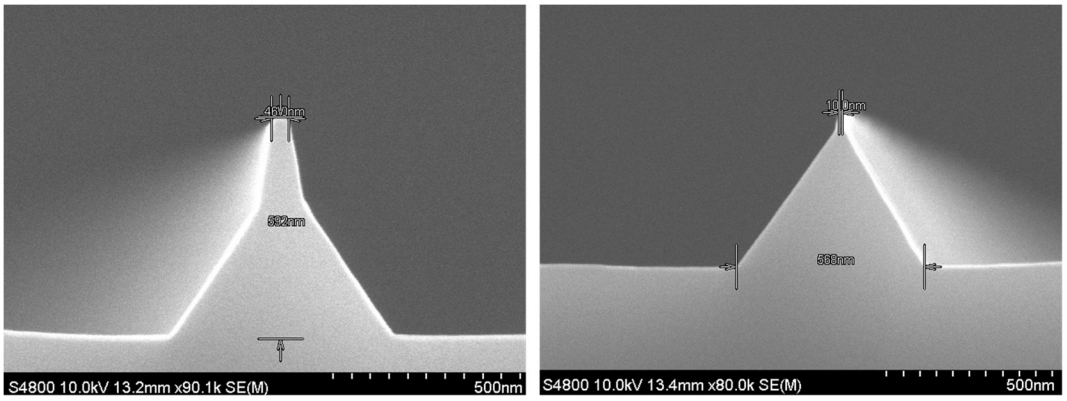


Fig. 2.9. SEM image of the fabricated Si nano-wedge structure. The initial fin width started at 500 nm. The figure in the left has been wet-etched for 9 minutes while the one in the right for 9.5 minutes. The tip size scaled from 46 nm down to 10 nm, proving the direction and time dependent crystalline silicon.

Before fabricating the Si BE nano-wedge RRAM device, we cleaned the 6-inch wafers to remove possible contaminants such as organic matters and metallic as well as non-metallic particles. Fig. 2.10 shows the full schematics of Si BE nano-wedge RRAM fabrication. Si fin patterning and etch using a poly-etcher is processed to form the fin width of 500 nm (Fig. 2.10 (a)). Then, the wafer is dipped into the TMAH wet etchant for 10 minutes and 15 seconds to minimize the tip of Si and form the wedge structure (Fig. 2.10 (b)). This structure is obtained by different etch rate on different direction of the crystalline Si (Fig.2.12 (d)). In detail, the silicon is direction-dependent while dipped into the TMAH solution where the etch rate of <100> and <110> direction with respect to <111> is 37 and 68 times faster, respectively. Isolation layer consists of Tetra-ethyl-ortho-silicate (TEOS) is deposited on top of the Si wedge, which is followed by chemical mechanical planarization (CMP) and hydro-fluro (HF) cleaning to planarize the layer and expose the Si wedge for the next process (Fig. 2.10 (c)). Ion implantation using As^+ ions with the energy of

40 keV and dose of 5×10^{15} cm^{-2} was carried out. After fully activating the active bottom electrode Si wedge, TiO_x as a switching layer is deposited on top of the wedge by using a sputtering process (Fig. 2.10 (d)), which is followed by deposition of Ti as a top electrode (TE) as shown in the Fig. 2.10 (e). Photolithography of TE patterning is processed, and 300 nm thick SiO_2 is deposited on top of the Ti TE for hole etching. The purpose of creating holes is to fill the metal stack of Ti/TiN/Al/TiN with the total thickness of 490 nm. Final nano-wedge RRAM device is obtained after patterning the pad as illustrated in the Fig. 2.10 (f). For comparison purpose, nano-wedge RRAM device with HfO_x switching layer was equally fabricated.

Fig. 2.11 shows the TEM image and EDS analysis of fabricated TiO_x-based nano-wedge RRAM device while Fig. 2.12 (a, b and c) are those of HfO_x-based device. Both images clearly formed the nano-wedge structure, where the width has been scaled down to sub 4 nm.

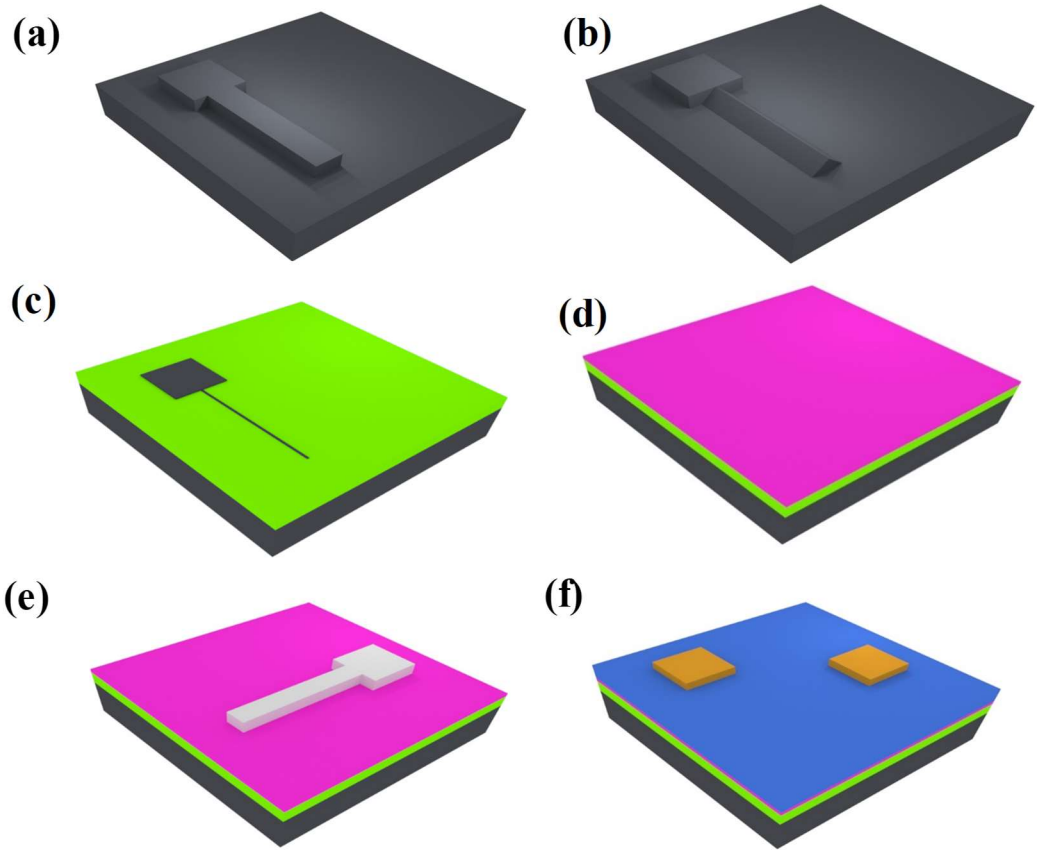


Fig. 2.10. Schematic of process flow for the fabrication of nano-wedge structured RRAM. Patterning and dry-etching the active bottom electrode (a) followed by TMAH anisotropic wet-etching to form the wedge structure of BE (b). Deposition of TEOS layer and CMP process is accompanied in order to expose the tip of BE, where As^{+} ions with the energy of 40 keV and dose amount of 5×10^{15} cm^{-2} are injected to allow it conductivity (c). (d) 15 nm-thick

switching layer (TiO_x) is deposited using a sputter. Top electrode (Ti) patterning (e) and pad photolithography (f) are sequentially processed, where the contact hole etching connects the pads with BE and TE, respectively.

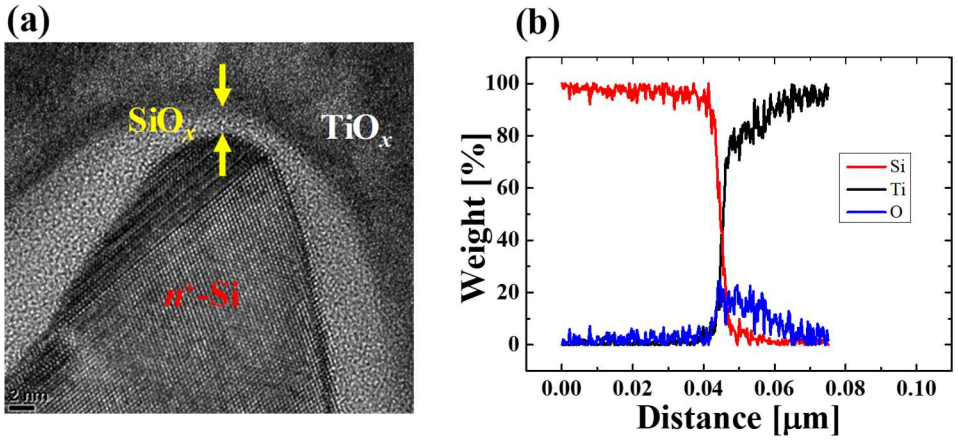


Fig. 2.11. Cross-sectional TEM image of highly doped Si BE nano-wedge RRAM device (a). Capacitive dividing during the voltage application (VTE and gnd) is shown between TiOx and SiO2 (interfacial layer, formed in-between red-dotted lines). EDS analysis of taken TEM image is depicted in (b). Light green area represents the interfacial layer formation.

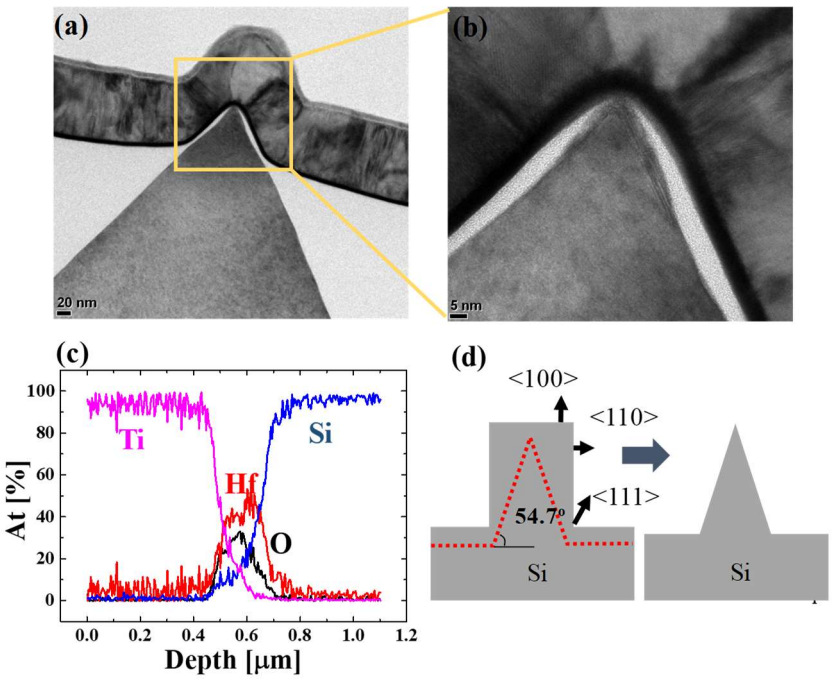


Fig. 2.12. TEM images of the fabricated nano-wedge RRAM device (a) and enlarged wedge-structure (~ 4 nm, (b)). Energy-Dispersive Spectroscopy (EDS) analysis of the take TEM image (c) and the direction of the anisotropic wet etching of silicon fin while dipping it into the TMAH wet etchant.

2.3. DC characteristics

2.3.1. HfO_x-based nano-wedge RRAM

In order to analyze the basic electrical properties of the fabricated HfO_x-based wedge RRAM device, we applied DC bias scheme to switch the device. In order to investigate the gradual switching characteristics, lower I_{cc} with 10 μA was applied. The current compliance prevents current overshoot, which can be further inhibited by setting lower I_{cc}. Fig. 2.13 demonstrates the gradual reset switching for both planar (a, b) and nano-wedge (c,d) RRAM device under the low compliance current. Clearly, in the Fig. 2.13 (a) and (c) which present DC I-V curves for the planar and nano-wedge with I_{cc} = 10 μA, less than an order increase in current level is seen right after the set switching. This stands in contrast with the abrupt set switching in Fig. 2.13 (b) and (d) with I_{cc} = 100 μA. Not limited to inhibited current overshoot in Fig. 2.13 (a) and (c), gradual reset switching processes from both devices indicate the gradual rupturing of the filament from the lower current level after set switching process. As a result,

there is not much current drop during the reset switching. From the Fig. 2.13 (d), a conductive filament is formed around 6 V and the nano-wedge RRAM becomes low resistance state (LRS). Negative bias is applied to reset the device to high resistance state (HRS) which is occurred around – 3 V. Reset process is done by rupturing part of the filament near the top electrode. Several cycles of set-reset switching processes with the abrupt switching are shown in the Fig. 2.13 (b) and (d). By comparing the DC switching characteristics of the planar and nano-wedge RRAM devices as illustrated in the Fig. 3 (b) and (d), both figures show the abrupt switching without an exception. However, the current level of the planar device (Fig. 2.13 (b)) is higher than that of the nano-wedge (Fig. 2.13 (d)) due to reduced area of the switching layer in which the oxygen vacancies are formed, contributing to decreased number of electrons flow. Larger area may have higher number of defects, thus denser (thicker) oxygen vacancies may form that lead to higher current levels.

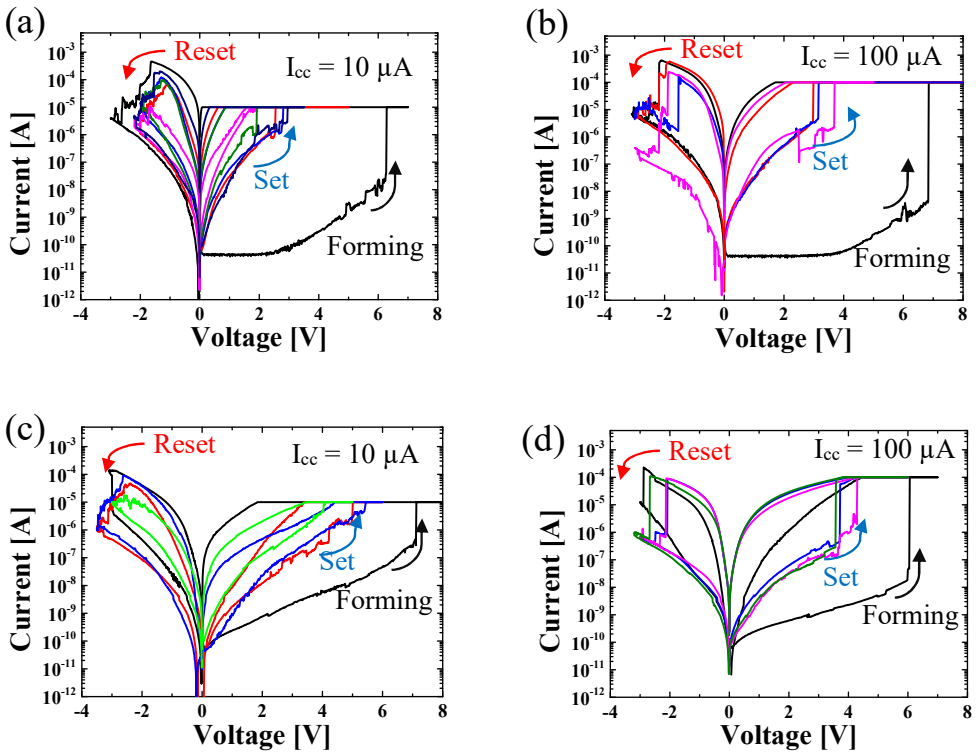


Fig. 2.13. DC I-V characteristics of the fabricated RRAM devices for the 4.9 × 10^5 nm^2 planar (a,b) and 4 × 500 nm^2 nano-wedge (c,d) structure under the compliance current (I_{cc}) of 10 μA and 100 μA.

Underlying switching mechanism of the nano-wedge RRAM is graphically shown in the Fig. 2.14. From the DC I-V curve, memory window of at least an order difference clearly demonstrates the device's switching mechanism is based on the oxygen vacancy movement, causing an abrupt FORMING switching. Once the filament is formed, both LRS and HRS conduction mechanism fits well with trap-controlled Space Charge Limited Conduction (SCLC) with three distinct slope regions, as observed in the Fig. 2.15. From high bias 'III' region in HRS and LRS, high slopes are seen where the current rapidly increases due to positively charged vacancies excited toward Ti top electrode.

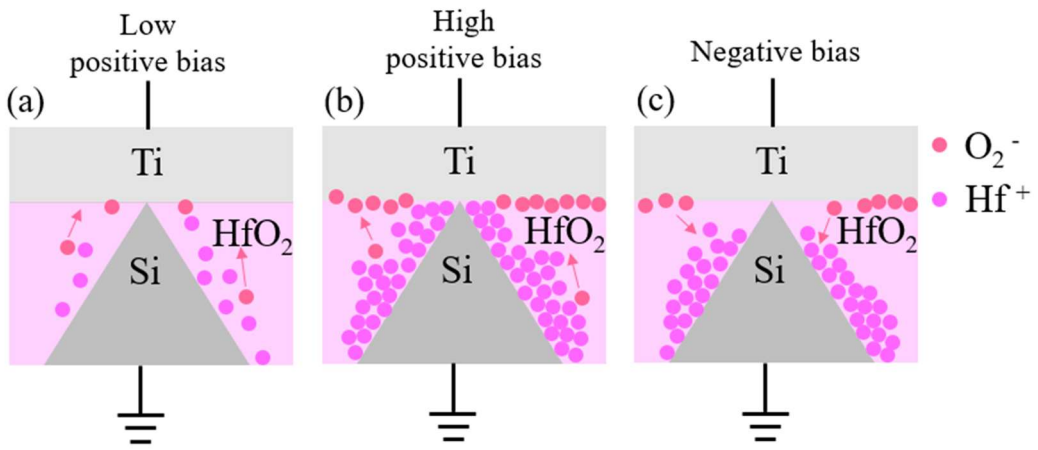


Fig. 2.14. Oxygen vacancy movement under different voltage polarities. (a) At low positive bias, oxygen ions start evacuating within the HfO_2 layer and leave behind the oxygen vacancies (also known as hafnium ions). (b) As the bias becomes higher, denser oxygen vacancies form a conductive filament through which current flows. Oxygen ions are scavenged below the top electrode. (c) Applying negative bias on the top electrode causes reduction of oxygen ions which lead to re-combine with hafnium ions to break the filament and limiting the current back to HRS.

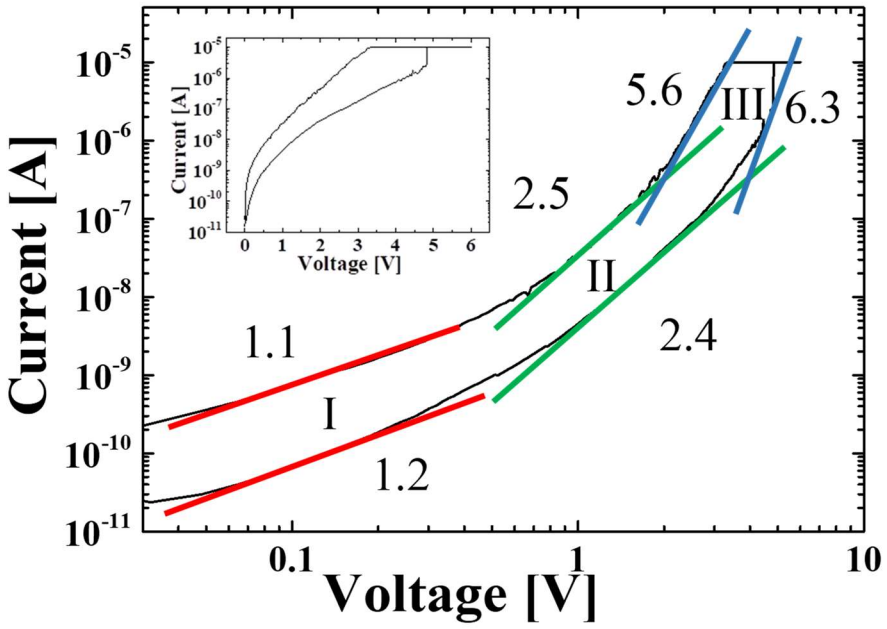


Fig. 2.15. Double-logarithm I-V plot. Inset shows the original set transition of nano-wedge RRAM device under the I_{cc} of 10 μA, used to express the double-logarithm I-V plot. Three distinct slope regions are marked with values of slope above each colored line. 'I' region follows the ohmic conduction behavior following $I \propto V$ (< 1 V region) regions while 'II' and 'III' regions follow Child's Law ($I \propto V^2$). Third 'III' region (blue line) also belongs to SET transition from HRS to LRS.

2.3.2. TiO_x-based nano-wedge RRAM

DC characteristics of TiO_x-based wedge RRAM device are depicted in Fig. 2.16. Initial forming process is occurred above 6 V, which is large enough compared to reported MIM structures [44, 45]. Not limited to this, cycle-to-cycle variations are huge that distribution range is 4 orders of magnitude (Fig. 2.17), indicating the issues of uniform conductance (weight) requirement for the synaptic device application.

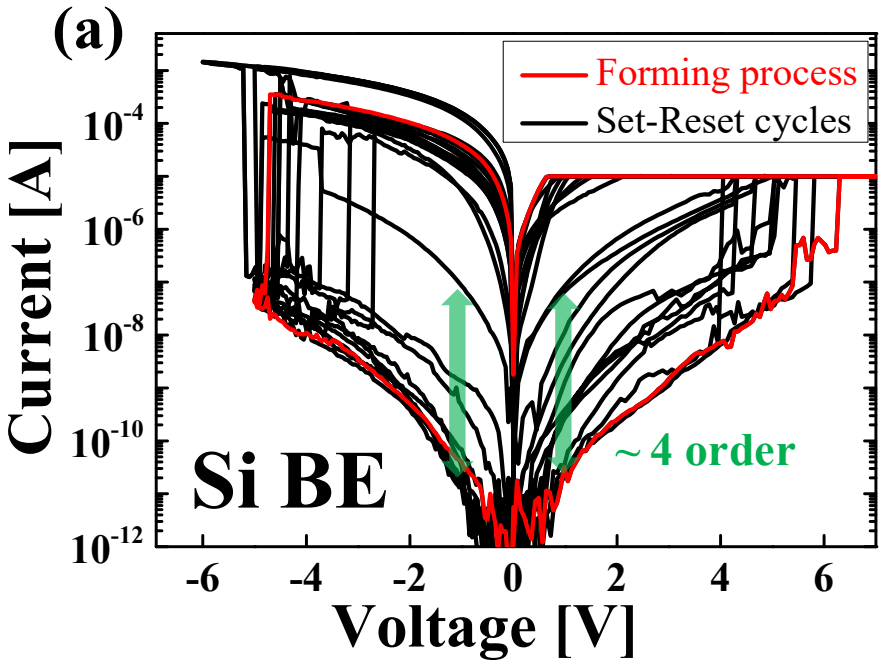


Fig. 2.16. DC I-V characteristics of Si BE nano-wedge RRAM device. HRS variations are distributed over 4 orders of magnitudes.

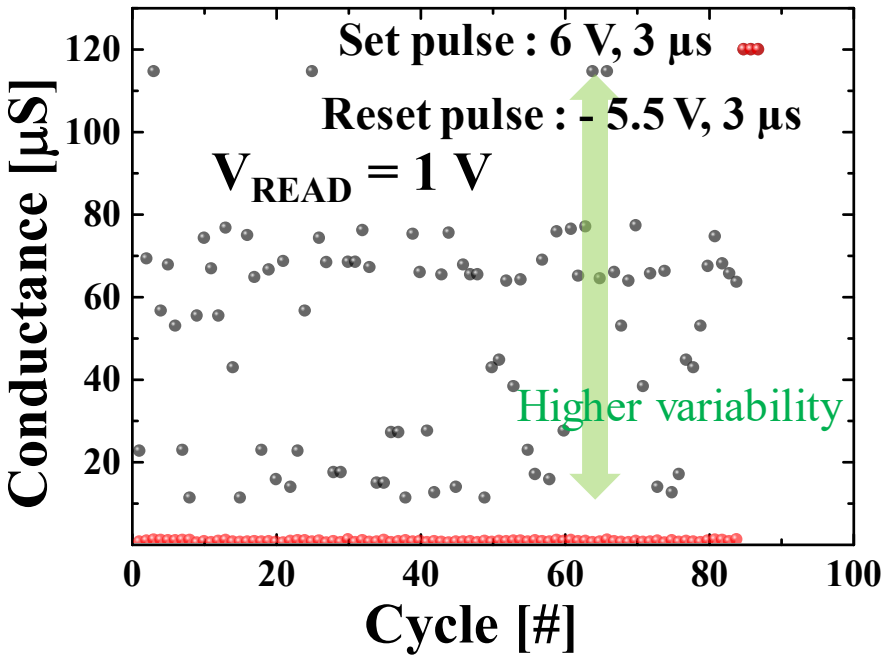


Fig. 2.17. Endurance of Si BE nano-wedge RRAM device. detailed switching conditions are stated in the databox, and larger variations among conductance values are illustrated.

2.4. Pulse characteristics

For neuromorphic computing application, a pulse switching is practical solution, which is the reason for the need of analysis of pulse switching characteristics. As shown in Fig. 2.18, a pulse scheme with 6 V for set (potentiation) and - 4 V for reset (depression) switching was applied with 100 μs pulse width for both cases. The abrupt change in conductance variation is seen from the planar device (Fig. 2.18 (a)) while that is gradually increasing for both set and reset switching process of the nano-wedge RRAM device (Fig. 2.18 (b)). Gradual set and reset from the nano-wedge RRAM under the low I_{cc} (10 μA) indicates the smaller number of oxygen vacancies existing within the HfO_x layer, preventing an abrupt current level drop by gradual rupturing of the conductive filament. This is significant to perform hardware implemented neural network with fine weight tuning and high accuracy achievement. Further pulse width modulation under certain threshold could not be able to set the nano-wedge RRAM, leading to inability of switching process. The conductance level

after the device being potentiated was 30.1 μS while that for the largest device is 469 μS, achieving more than an order reduction in current level

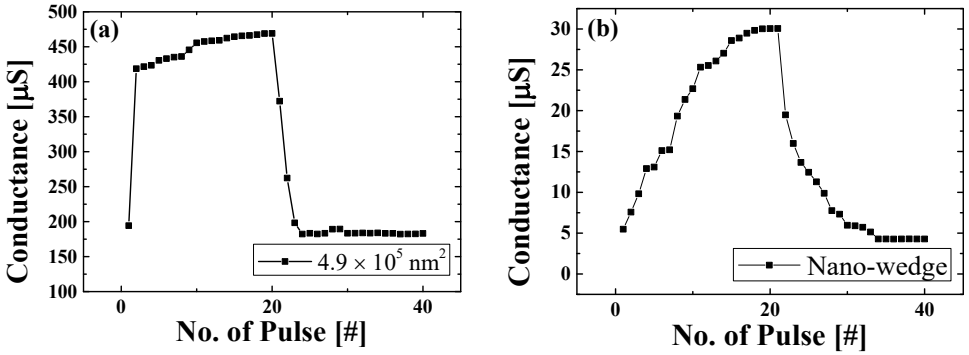


Fig. 2.18. Pulse measurement for investigating the potentiation (set) and depression (reset) of the fabricated planar (a) and nano-wedge (b) RRAM devices.

2.5. Limitation of Si BE RRAM device

Although Si bottom electrode (BE) nano-wedge RRAM device proved to be suitable for low power operation of hardware-implemented synaptic device application, there exists number of drawbacks that prevent MIS RRAM to be commercialized. First, switching power is still large due to unexpected overshoot current while forming and set switching process. Fig. 2.16 shows he severity of current overshoot, and large cycle-to-cycle and device-to-device variations are another non-ideal aspects of Si BE RRAM device. These issues eventually limit the RRAM device to be implemented as synaptic devices, and the reliability of the system may be exacerbated.

According to the measured DC I-V curves in Fig. 2.19 (b), Si BE nano-wedge RRAM with the width of 50 nm is suffering from the current overshoot with more than 2 orders of magnitude. During the reset switching process, the current level drops from 100 μA to a few pico-amperes, indicating the seriousness of bottlenecks for multilevel conductance acquirement.

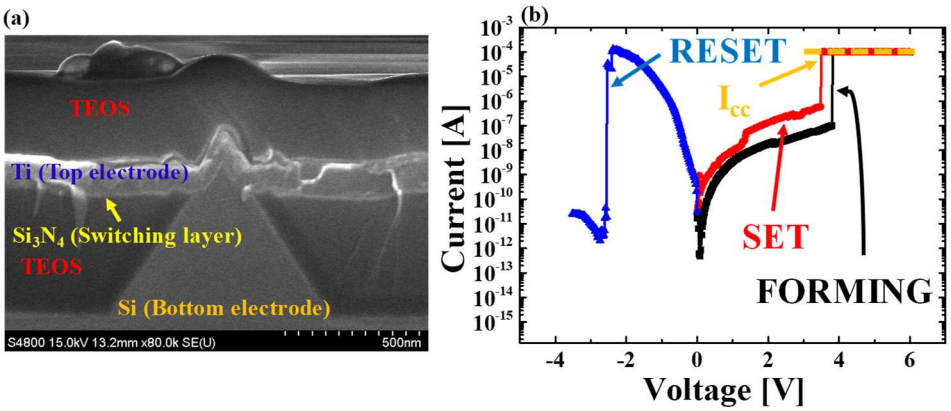


Fig. 2.19. (a) is the fabricated Si_3N_4-based nano-wedge RRAM device with the wedge width of 50 nm and (b) is the I-V characteristics of the device.

From the above results, it is undeniable that Si BE RRAM device still prevents itself from becoming the ideal synaptic device. Thus, it is required to search for other materials that are necessary to reduce non-idealities and make the scaled nano-wedge RRAM practical for neural network application.

2.6. Nickel silicidation to the bottom electrode

The biggest advantages of using MIM RRAM is its uniform switching cycles and highly reliable electrical properties. Yet, high current levels from the existing MIM RRAM device hinder its practical application to synaptic devices. As a result, we suggest a novel application of Nickel (Ni) silicidation to a highly-doped Si bottom electrode (BE) to achieve current levels lower than those of MIM RRAM devices but still with reliable and uniform parameters. The silicidation technique is used to reduce contact resistance of source/drain regions as devices scale down. We used this technique to make the Si BE metallic, thereby reducing the resistance of Si BE and the voltage drop across the fabricated RRAM device.

The fabrication process of single NiSi BE RRAM device is exactly equal to that of TiO_x-based Si nano-wedge RRAM device, except for deposition of Ni (10 nm) and TiN (as a capping layer, 30 nm) followed by annealing at 450 ℃ for 60 seconds. Fig. 2.20 shows the TEM and component of each element for

the fabricated NiSi BE RRAM device.

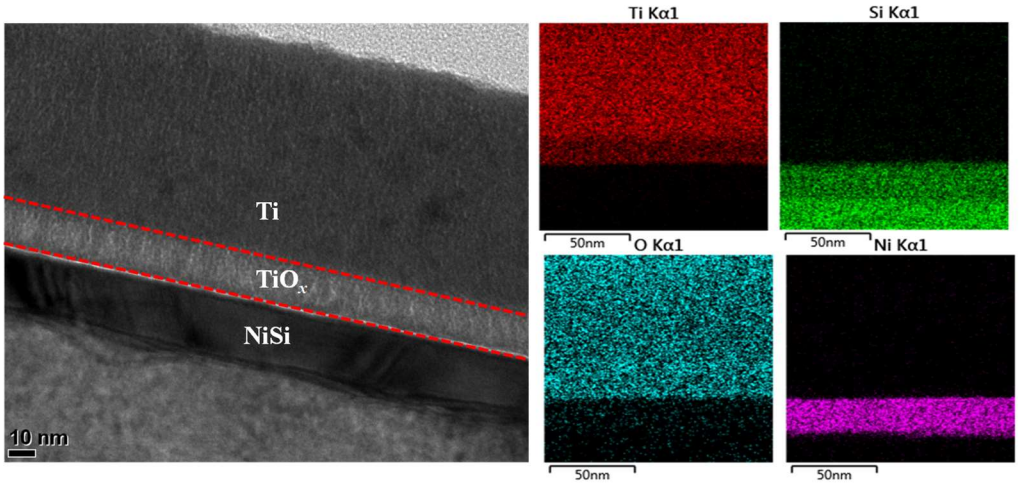


Fig. 2.20. TEM image of fabricated NiSi BE RRAM device (left) and color mapping analysis of the taken image (right).

2.6.1. Effect of NiSi on its resistivity

In order to analyze the resistance of fabricated NiSi BE RRAM device, we prepared a sample with Ni silicidation on top of highly-doped n^+-Si. The measured resistivity is shown in Fig. 2.21. The device for resistivity measurement is 4-point probe, which measures the sheet resistance then calculate the resistivity. As illustrated in the Fig. 2.21, the average resistivity is 1.25 μΩ·cm, which is uniform throughout the 6-inch wafer. This also indicates the uniform formation of Ni silicidation, proving the stability of this specific fabrication process.

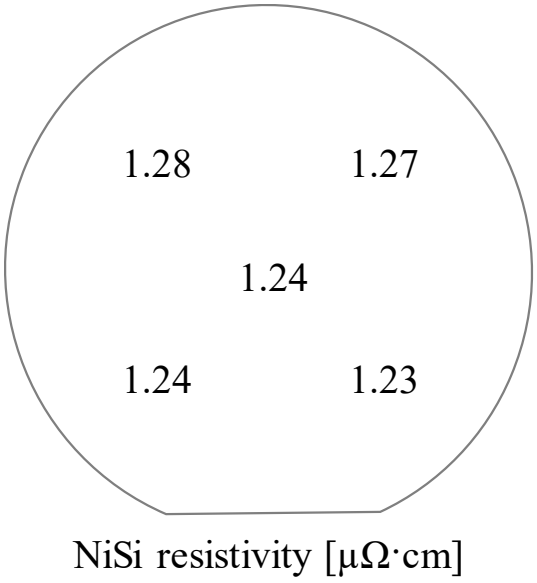


Fig. 2.21. Measured resistivity of fabricated NiSi BE RRAM device.

2.6.2. Comparison of NiSi and TiSi

Silicidation is not necessarily limited to Nickel. Instead, Titanium is another good candidate for the silicidation. As a result, we fabricated planar TiSi BE RRAM device. The measured resistivity of TiSi and NiSi are illustrated in Fig. 2.22. The average resistivity of TiSi was higher than that of NiSi by 22 %.

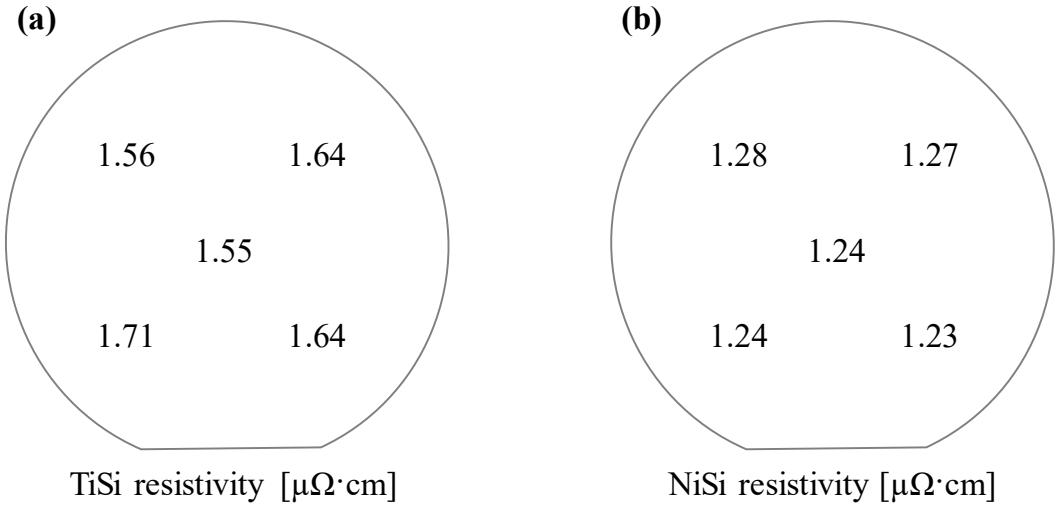


Fig. 2.22. Measured resistivity of TiSi (a) and NiSi (b) on the 6-inch wafer.

The fabrication condition of TiSi is to deposit 10 nm of Ti and 30 nm of TiN (to prevent oxidation of Ti during the annealing process), which is followed

by annealing at 800 ℃ for 240 seconds. Fig. 2.23 shows the full process flow of TiSi BE RRAM device, its schematic and the TEM image. As stated in the Fig. 2.23, after Ti silicidation the residual TiN and Ti is being stripped using H_2SO_4 which is acidic solution. 15 nm TiO_x and 100 nm Ti is sequentially deposited using the sputter and electron beam gun (e-gun) respectively.

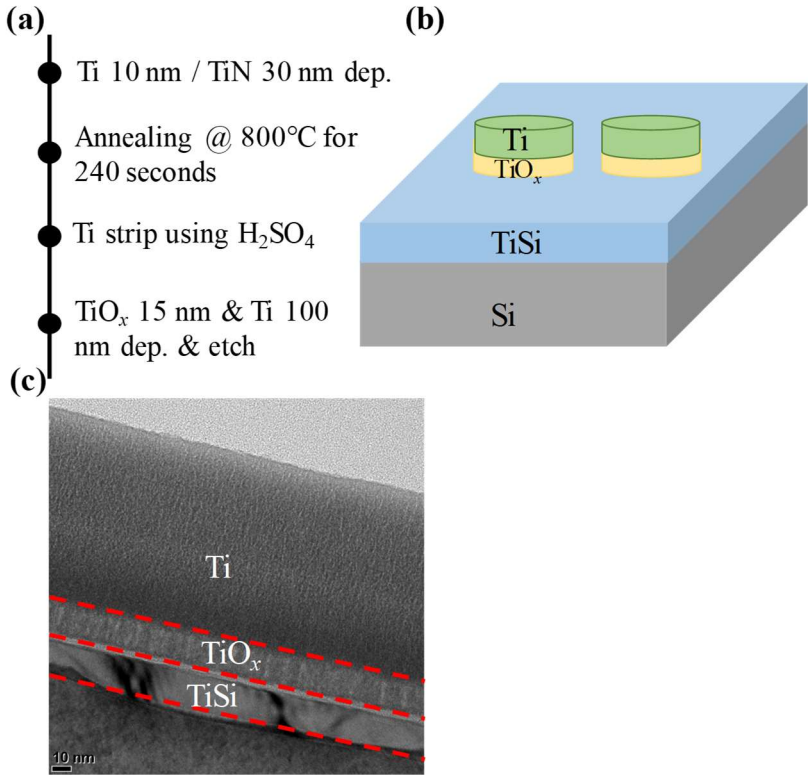


Fig. 2.23. (a) Process flow of the TiSi BE RRAM device, (b) a schematic of the fabricated device and (c) taken TEM image of the TiSi RRAM device.

The electrical characteristics of TiSi and NiSi BE RRAM device using DC bias were measured to compare each other. Fig. 2.24 (a) shows the I-V curve of TiSi BE RRAM where the red cycle indicates the initial switching at 3 V under the I_{cc} of 200 μA. For the grey cycles the I_{cc} have been changed from cycle to cycle since the device was sometimes un-switched at specific I_{cc}. Equally, NiSi BE RRAM also showed similar DC switching characteristics (Fig. 2.24 (b)) compared to TiSi BE, except for slightly increased range of I_{cc} up to 500 μA. To make as accurate comparison as possible, we made statistical distribution of switching parameters (forming/set/reset voltages) as well as resistive states (both LRS and HRS). Fig. 2.25 (a) fully shows the distribution of measured data from the Fig. 2.24. $V_{FORMING}$ of both devices are around 3 V while average V_{SET} of TiSi BE RRAM device (1.8 V) is slightly higher than that of NiSi BE RRAM device (2.1 V). For V_{RESET}, NiSi BE RRAM device exhibits at lower bias (-1.5 V) than TiSi RRAM device (1.65 V). It is interesting that, however, the variation of switching parameters in TiSi BE RRAM device is less

than that of NiSi BE RRAM device, suggesting the irrelevance of resistivity on switching parameter improvement. Fig. 2.25 (b) depicts the measured LRS and HRS of both devices. Equally, variations of TiSi BE are better than those of NiSi BE RRAM device.

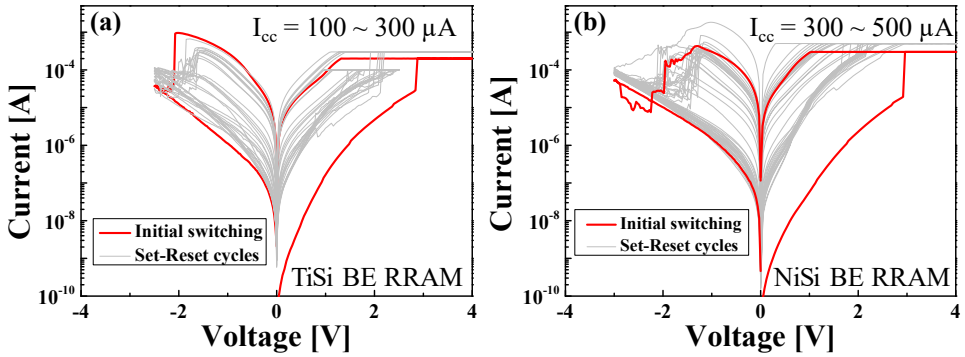


Fig. 2.24. DC characteristics of TiSi BE RRAM (a) and NiSi BE RRAM (b) for the compliance current (I_{cc}) range of 100 ~ 300 µA and 300 ~ 500 µA, respectively. Various I_{cc} were applied to allow the device for full operation until it reaches the stage of un-switchable state.

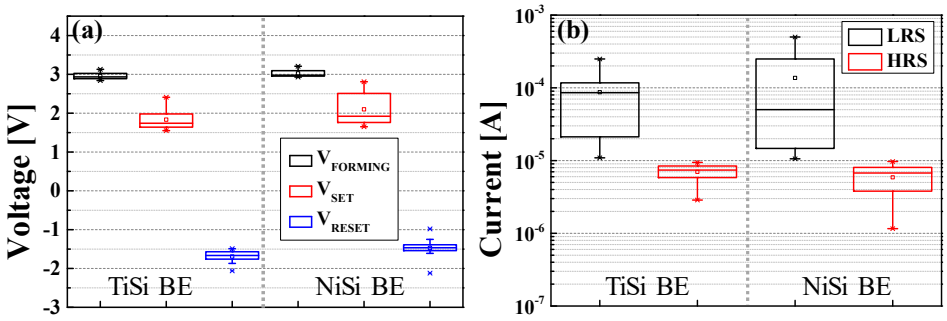


Fig. 2.25. Statistical distribution of $V_{FORMING}$, V_{SET} and V_{RESET} of TiSi and NiSi BE RRAM device (a). Current levels at LRS and HRS of both devices are plotted in (b).

2.6.3. Process flow of single NiSi BE nano-wedge RRAM device

For the application of Ni silicidation to the highly-doped n^+-Si bottom electrode, we fabricated another Si wedge structure RRAM device. The process flow of the single NiSi BE RRAM device fabrication is fully shown in Fig. 2.26 and Fig. 2.27. Fig. 2.26 (a) is the schematic of Si wedge-structure and (b) shows right after the deposition of TEOS SiO_2 layer for the isolation. After a formation of 500 nm width fin through dry etching process, the wafer is dipped into an anisotropic wet etchant TMAH for 10 minutes. Based on different etch rate of <100> and <110> with respect to <111> direction, the Si wedge structure is obtained. Tetra-Ethyl-Ortho-Silicate (TEOS) layer is deposited via PECVD to isolate the device. Planarization of TEOS layer through Chemical Mechanical Polishing (CMP) process and hydro-Fluoro (HF) cleaning is done to expose the tip of Si BE. In order to activate the Si BE, ion implantation with an energy of 40 keV and dose of 5×10^{15} cm^{-2} were executed after growing a screen oxide

layer (~ 10 nm) as illustrated in the Fig. 2.26 (c). Ni (10 nm) and TiN (30 nm) were sequentially sputtered on top of Si tip after the removal of screen oxide. N_2 gas annealing at 450 ℃ for 60 seconds was carried out to silicide the Ni into NiSi (Fig. 2.26 (d)). TiN was used as a capping layer to prevent oxidation of Ni during the silicidation. After etching the TiN using a Sulfuric acid, 15 nm thick TiO_x switching layer was sputtered onto the surface of NiSi, which is followed by top electrode formation through depositing the Ti (~ 100 nm) as depicted in the Fig. 2.27. the cross-sectional view of the fabricated NiSi and Si BE nano-wedge RRAM devices are shown in the Fig. 2.27 (b). The fabricated RRAM device size is 4 nm × 500 nm. TEM image of the fabricated NiSi BE nano-wedge RRAM is shown in the Fig. 2.28 and energy-dispersive spectroscopy (EDS) component analysis is plotted in the Fig. 2.28 (d). For comparison, a highly-doped n^+-Si BE nano-wedge RRAM device was fabricated as the reference device.

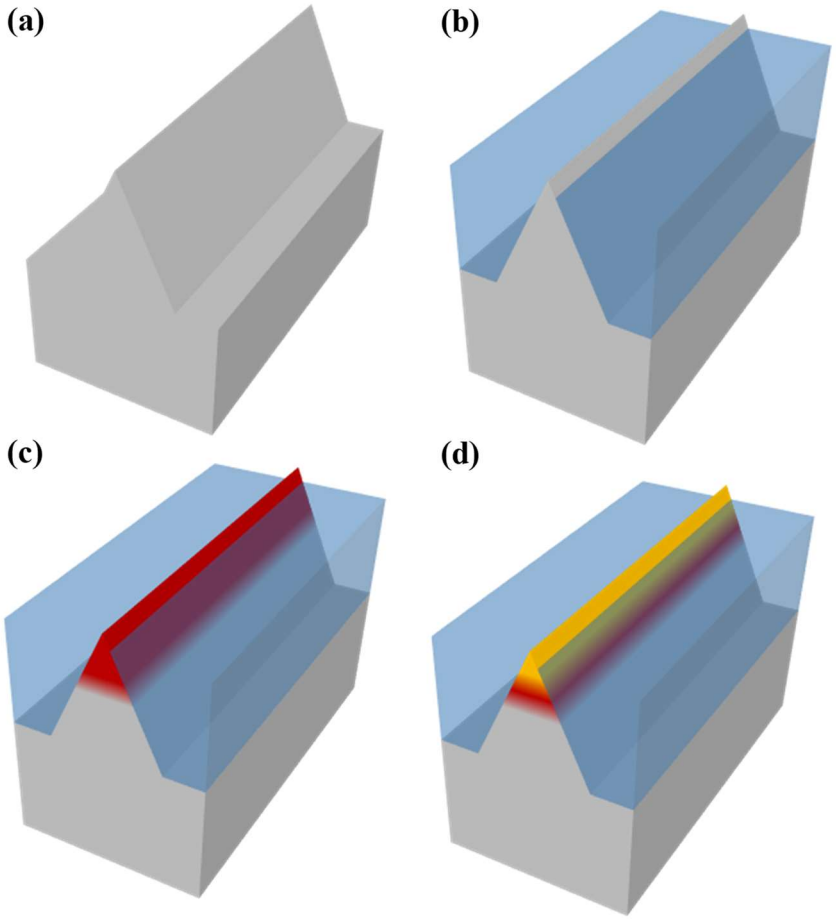


Fig. 2.26. Process flow of NiSi BE nano-wedge RRAM device. (a) is after TMAH wet etching of Si fin, which is followed by deposition of TEOS SiO2 layer for the isolation (b). Activation of bottom electrode (c) is necessary before Ni silicidation to the active (d).

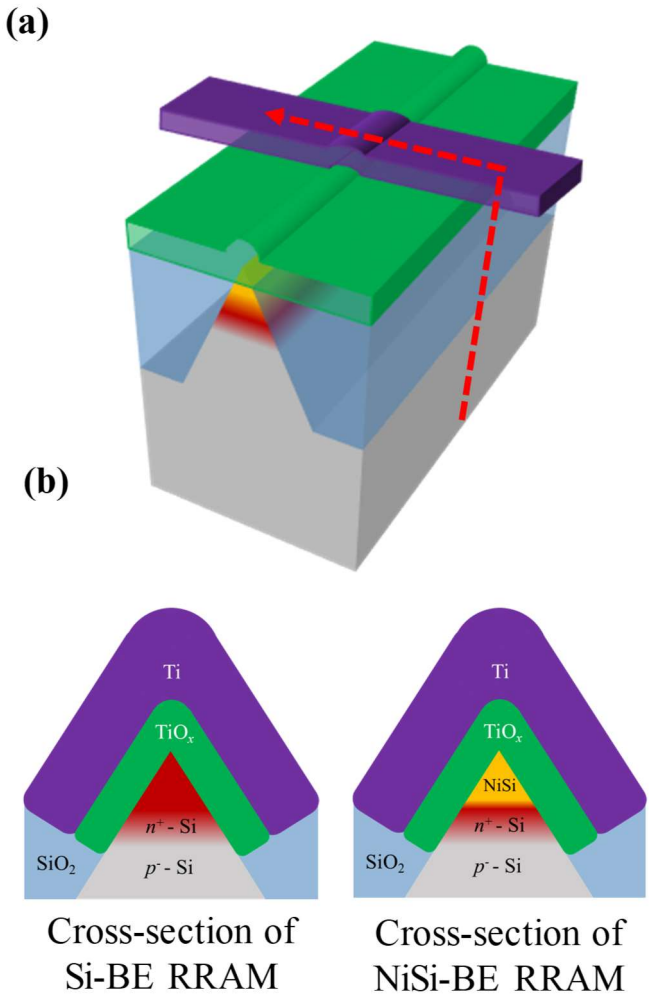


Fig. 2.27. Full schematic of the fabricated single NiSi BE nano-wedge RRAM device (a). cross-section of the fabricated Si and NiSi BE RRAM devices are shown in (b).

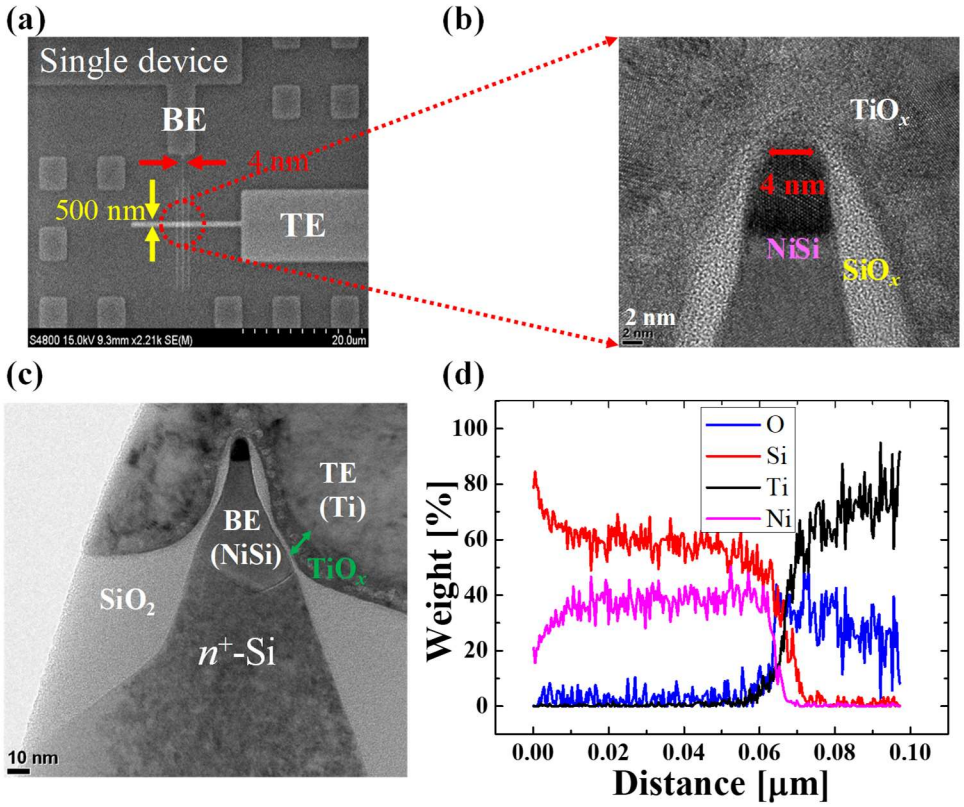


Fig. 2.28. Top SEM image of the fabricated NiSi BE RRAM single device (a) and enlarged wedge structure of NiSi BE (b). TEM image of full cross-section of the fabricated device (c) with EDS analysis (d).

2.7. Improvement of switching parameters in NiSi BE RRAM device

Electrical characteristics of both highly-doped n^+-Si and NiSi BE nano-wedge RRAM devices were analyzed in order to demonstrate the improvement of switching parameters and reliability properties. All DC and pulse switching measurements were carious out using B1500A Agilent Electrical Analyzer and WGFMU ultra-fast IV measurement unit.

First, DC characteristics of Si and NiSi BE nano-wedge RRAM devices' cycle-to-cycle variations are illustrated in Fig. 2. 29. The larger variation among the cycles of Si BE device is seen, in the Fig. 2.29 (a), with HRS variations of 4 orders of magnitude. In contrast, cycle variations are minimized and LRS are uniform except for the initial forming process of NiSi BE device (red curve, Fig. 2.29 (b)). Uniformity of conductance is statistically illustrated in the Fig. 2.29 (c). Si BE LRS shows a wider distribution within 1 order of magnitude, while

both high and low conductance are tightly distributed over 200 cycles as demonstrated in the Fig. 2.29 (d). HRS of Si BE device exist over the span of 4 orders of magnitude, but linear scale (Fig. 2.29 (c) and (d)) plot the data near zero conductance value. From the cumulative data shown in the Fig. 2, average LRS and HRS value for NiSi BE nano-wedge RRAM device are 3.48 μS and 352 nS, while those of Si BE nano-wedge RRAM device is 45.6 μS and 711 nS, respectively. We found the major factor contributing to increased conductance level in Si BE device is due to high switching voltages.

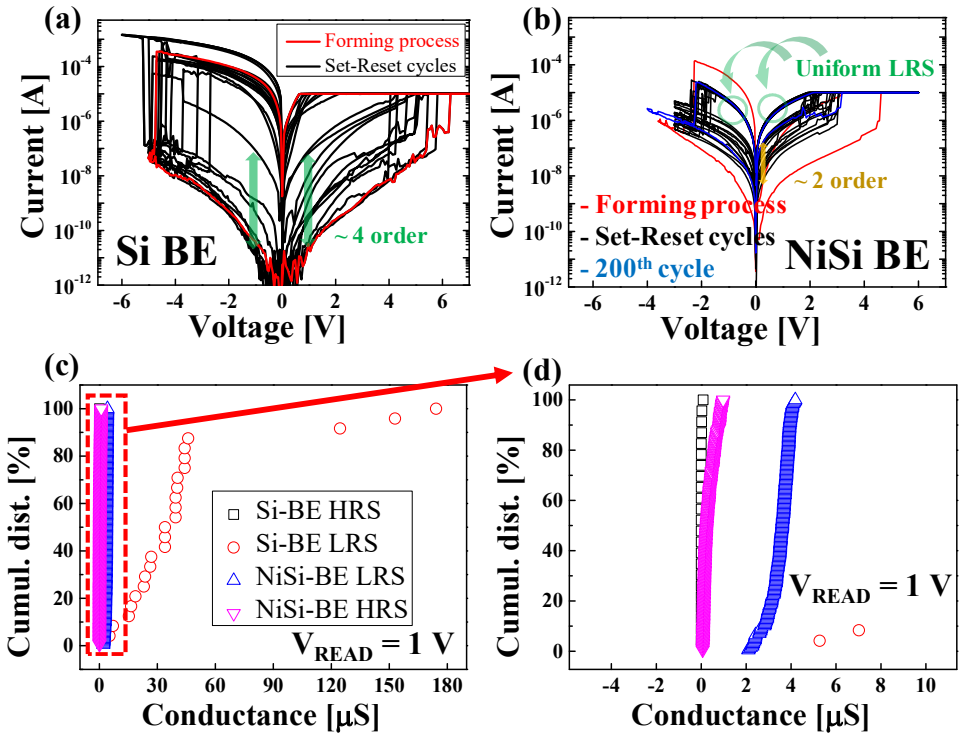


Fig. 2.29. DC I-V characteristics of Si BE (a) and NiSi BE (b) nano-wedge RRAM device. Compliance current (I_{cc}) is applied at 10 μA. (c) Cumulative distributions of LRS and HRS within a single device and (d) enlarged parameter distributions of NiSi BE RRAM at V_{READ} = 1 V.

Device-to-device variations of fabricated nano-wedge RRAM devices are shown in Fig. 2.30. After measuring 100 different devices, an average $V_{FORMING}$ of NiSi BE device is reduced to 4.37 V, which is a 17% reduction from that of Si BE device (5.28 V) as depicted in the Fig. 2.30 (a). Both average V_{SET} and V_{RESET} of NiSi BE device were reduced from 5.13 V and -3.94 V to 2.34 V and -1.61 V after the silicidation, respectively, as plotted in the Fig. 2.30 (b, c). Smaller relative standard deviation (σ/μ) of NiSi BE device indicates that the data are tightly distributed with less device-to-device variations. Main Contribution of reduction of switching parameters comes from the Ni silicidation of Si, which reduced the resistance of BE and thus a total voltage-drop across the nano-wedge RRAM device decreased.

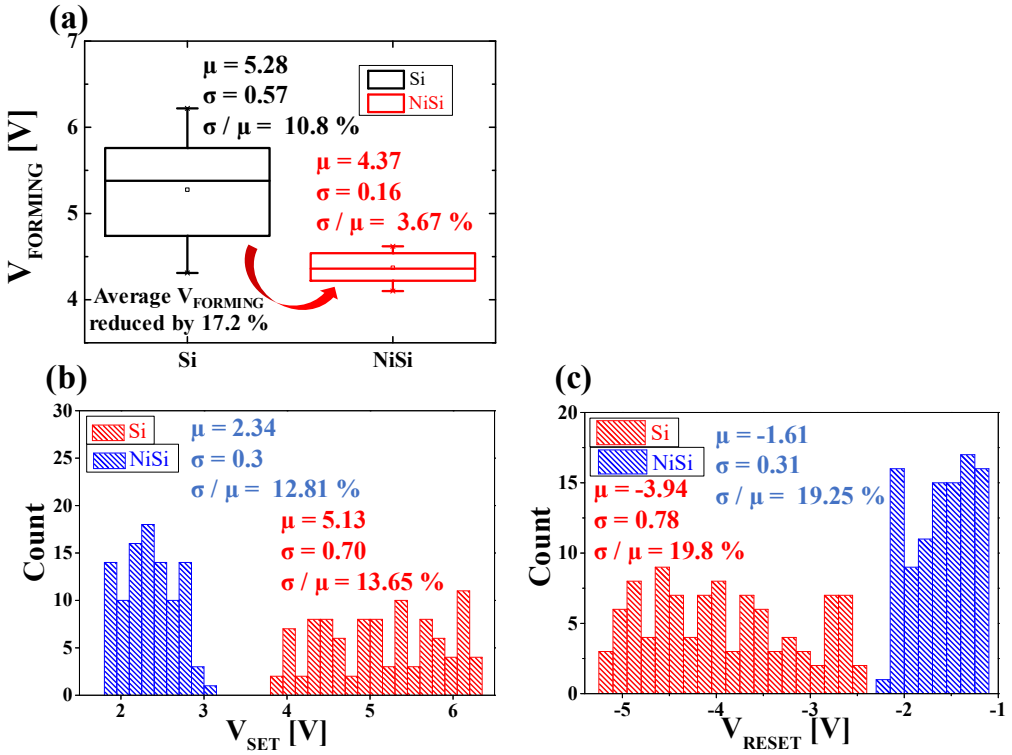


Fig. 2.30. Device-to-device variations of forming (a), set (b) and reset (c) voltages from 100 Si and NiSi BE nano-wedge RRAM devices.

Retention test as illustrated in the Fig. 2.31 (a) shows that both Si and NiSi BE nano-wedge RRAM single device keeps stable states under the temperature of 85 ℃ for 10^4 seconds. A set of pulses was applied to switch the NiSi BE nano-wedge RRAM single device and detailed pulse conditions are stated in the data box of Fig. 2.31 (b). Note that the endurance test result of Si BE RRAM device is illustrated in the Fig. 2.17. Unlike larger cycle-to-cycle variability of Si BE RRAM device in the Fig. 2.17, the endurance of NiSi BE RRAM device, in linear scale, showed uniform conductance over 40k cycles.

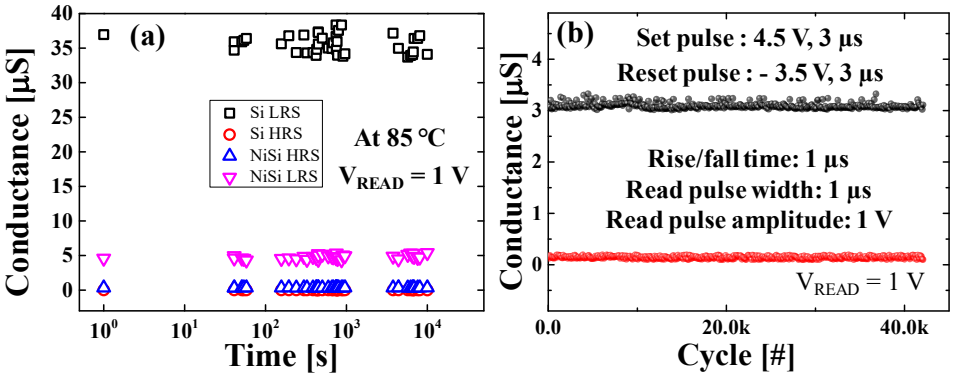


Fig. 2.31. Reliability data showing the retention characteristics (a) of Si and NiSi BE nano-wedge RRAM devices at 85 ℃ for 10^4 seconds and endurance of NiSi BE nano-wedge RRAM single device (b).

A single pulse was applied to show transient characteristics of the fabricated devices as depicted in Fig. 2.32. Red arrows show the fast switching speed (a few nanoseconds) for both types of nano-wedge RRAM devices, demonstrating the independence of switching speed on device types. (a) ~ (c) and (d) ~ (f) respectively represent forming/reset/set switching transients of Si and NiSi BE nano-wedge RRAM device.

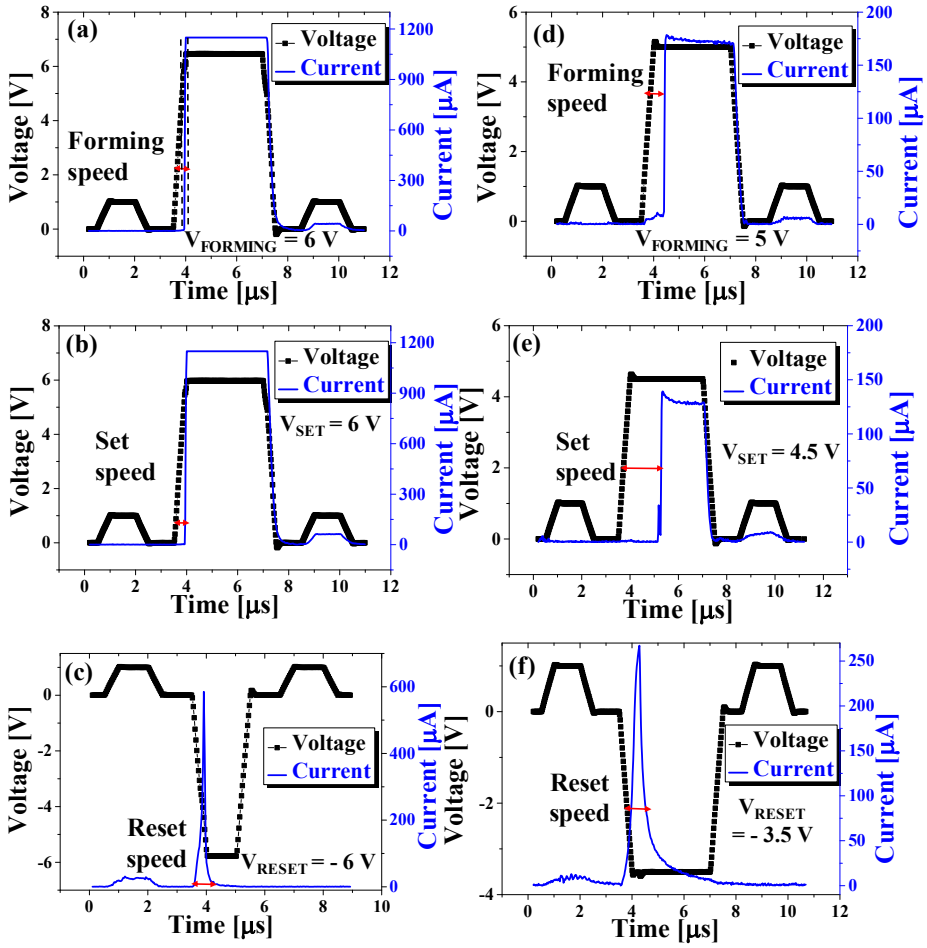


Fig. 2.32. Transients of Si (a ~ c) and NiSi BE (d ~ f) nano-wedge RRAM device. Peak current levels of Si BE reach higher than those of NiSi BE device. Red arrows represent the switching speed, which is independent from device types. Values of the switching parameters are stated within each data box.

Switching speed of the fabricated devices ranges from 30 ns to a few μs, depending on the level of pulse amplitude as illustrated in Fig. 2.33. The peak current during the forming process of Si BE reaches to 1.1 mA (Fig. 2.32 (a)) while that of NiSi BE is kept to 160 μA. Equally, maximum current levels of NiSi BE device during the reset and set switching are decreased to 250 μA and 150 μA. These values reduced by 58 % (from 600 μA) and 87.5 % (from 1.2 mA) compared to current levels of Si BE device. Decreased peak current levels of NiSi BE nano-wedge RRAM device are attributed to reduction of switching voltages as shown in each data box of Fig. 2.32.

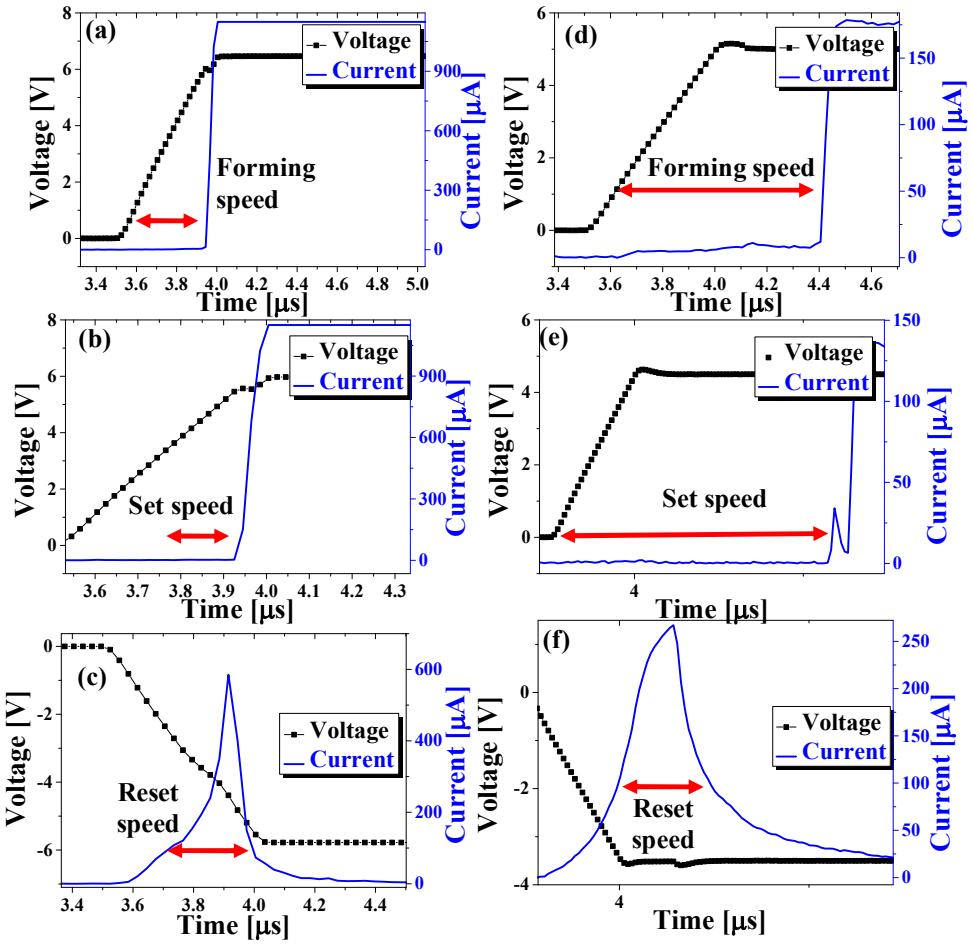


Fig. 2.33. Enlarged pulse transients from the Fig. 2.32 to show the switching speed of Si (a ~ c) and NiSi (d ~ f) nano-wedge RRAM device. Switching speed distributes from tens of nanoseconds to a few microseconds, depending on the value of pulse amplitudes.

To further analyze the reduction of switching parameters (forming/set/reset voltages) of NiSi BE nano-wedge RRAM device, a TEM image of highly doped Si BE nano-wedge RRAM device was taken as shown in Fig. 2.34 (a). During the sputtering of TiO_x, oxygen may have reacted with n^+-Si to form the SiO_2 interfacial layer (IL). EDS analysis in the Fig. 2.34 (b) confirms the existence of oxygen and silicon between TiO_x and n^+-Si (light green region). This IL, along with deposited TiO_x, increases the effective thickness of switching layer. From the Fig. 2.34 (a), a capacitive divider is drawn to show the effect of capacitive dividing during the voltage application (V_{TE}, Top Electrode voltage).

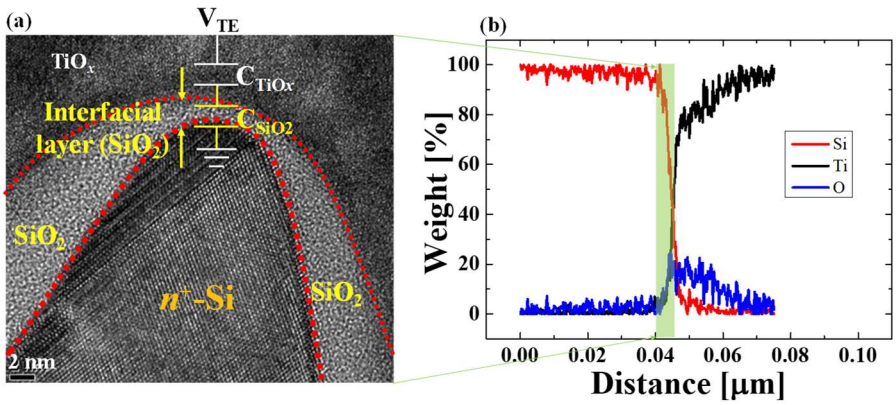


Fig. 2.34. Cross-sectional TEM image of highly doped Si BE nano-wedge RRAM device (a). Capacitive dividing during the voltage application (V_{TE} and gnd) is shown between TiO_x and SiO_2 (interfacial layer, formed in-between red-dotted lines). EDS analysis of taken TEM image is depicted in (b). Light green area represents the interfacial layer formation.

Material	**Dielectric Constant (k)**	**Thickness (nm)**	**Device Area (nm^2)**	**Capacitance per unit area (aF/nm^2)**
TiO_x	80 ~ 170	15	4 × 500	0.1 ~ 0.47
SiO_2	3.9	1 ~ 2	4 × 500	0.017 ~ 0.035

Table 2.1. Calculated capacitance of switching layer.

In order to demonstrate the effect of capacitance on switching parameters of Si BE nano-wedge RRAM device, capacitance per unit area of SiO_2 and TiO_x was calculated as shown in the Table 2.1. Commonly known dielectric constant (k) of SiO_2 is 3.9, while that of TiO_x ranges from 80 to 170. From the TEM image in the Fig. 2.34 (a), the thickness of interfacial layer is around 1~2 nm. Thus, capacitances of two different dielectric layers were calculated and divided by the fabricated device area (4×500 nm^2). From the Table 2.1, capacitance of TiO_x ranges from 0.1 to 0.47 by taking different k values into account, and these capacitances are larger than those of SiO_2 (0.017 ~ 0.035 aF/nm^2). From the principle of capacitive voltage dividing rule, higher voltage drop occurs in SiO_2 than does in TiO_x, which has higher capacitive value. This ultimately breaks down the SiO_2 interfacial layer prior to TiO_x breakdown. At the moment of IL breakdown, the higher voltage is applied between Si BE and Ti top electrode, resulting in switching layer (TiO_x) breakdown. Compared to NiSi BE nano-wedge RRAM device, the higher voltage-drop across Si BE

device induces higher current levels (Fig. 2.29 (a)), which is the main contribution to high power consumption of Si BE device. Furthermore, higher current overshoot from the Si BE RRAM device degrades its reliability, resulting in lower endurance test as demonstrated in the Fig. 2.17.

Another essential functions of synaptic device are to realize gradual and multiple conductance levels, thereby improving the accuracy of neural network processing [46-48]. Both bias ramp up and pulse were applied to NiSi BE nano-wedge RRAM device to demonstrate the multiple conductance levels as illustrated in Fig. 2.35. Fig. 2.35 (a) shows different read voltages by applying different compliance currents from 10 ~ 11 μA with 0.1 μA step. Conductance levels are sequentially increased from 400 nS to 9 μS, indicating more electrons flow through thicker conductive filament. A set of pulse application was also applied to acquire multiple conductance states in the Fig. 2.35 (b). In order to set the NiSi BE RRAM device, initial pulse amplitude of 4.5 V with 80 mV incremental steps was applied for the single pulse duration of 3 μs. A set of

pulse with negative voltage amplitude was also applied for the purpose of depression. During the potentiation (or set switching cycle), conductance increased from 0.3 μS to 4 μS while it diminished to 900 nS during the depression (or reset switching cycle). Demonstration of gradual switching for the NiSi BE nano-wedge RRAM device is attributed to reduced current overshoot during the set switching and prevention of the interfacial layer formation during the sputtering of TiO_x.

In order to analyze the conduction mechanism of the fabricated device, linear fitting curve of hopping (LRS) and Space-Charge-Limited Conduction (SCLC, HRS) conduction mechanism of the NiSi BE nano-wedge RRAM device is illustrated in Fig. 2.36 (a) and (b). These mechanisms are commonly reported mechanisms of MIS structures, indicating the conduction is similar to other reported devices

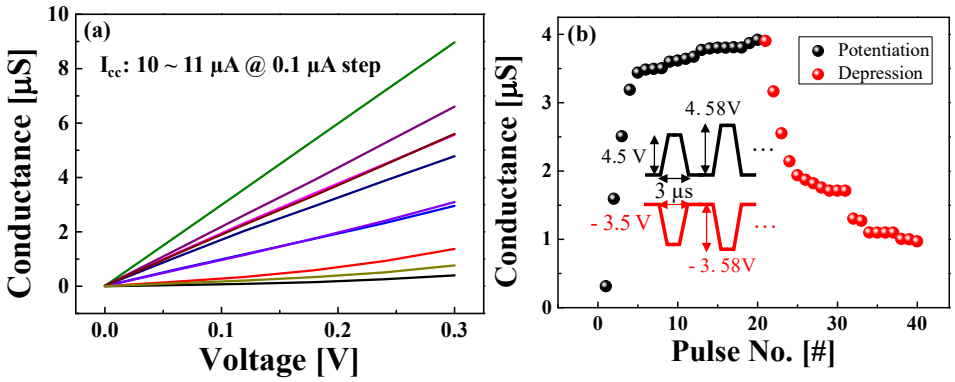


Fig. 2.35. Cross-sectional TEM image of highly doped Si BE nano-wedge RRAM device.

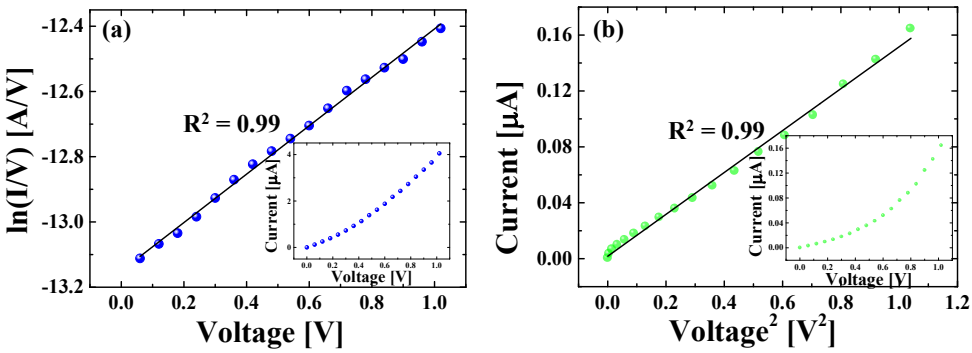


Fig. 2.36. Linear fitting curve of conduction mechanism of NiSi based nano-wedge RRAM device during the low resistance state (a) and high resistance state (b). Insets are linear IV curves.

Average switching power consumption of the fabricated nano-wedge RRAM devices were statistically analyzed. As demonstrated in Fig. 2.37 (a), pulse switching required higher biases than those for DC switching, indicating the higher fields are necessary to switch the device within short period of time (~ μs). The Fig. 2.37 (b) shows the average energy consumed during the set switching of both devices. The average value of energy consumption for NiSi BE nano-wedge RRAM device is 103.1 pJ, which is less than half of Si BE device. This proves the lower resistivity of NiSi active induced lower switching biases needed, leading to reduction of switching power consumption.

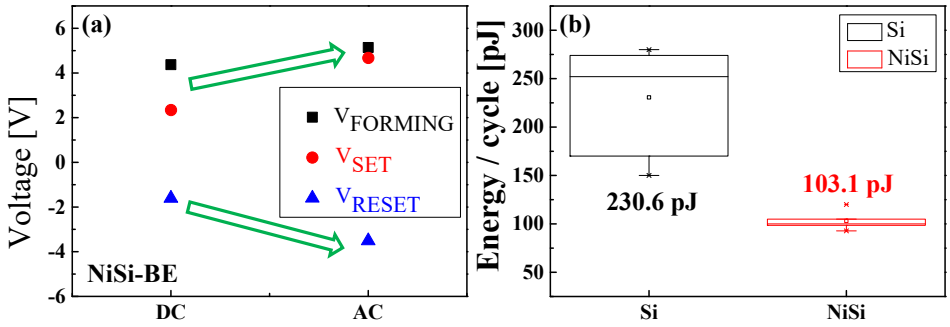


Fig. 2.37. Average forming/set/reset voltages of NiSi BE nano-wedge RRAM device (a) and statistics of energy consumption of 50 different devices for both Si and NiSi active.

Chapter 3

NiSi BE nano-wedge RRAM Cross-Point Array

Operation of neural network requires hardware-implemented synaptic devices in the cross-point array structure [49]. Prior to application of Ni silicidation to the bit-line of cross-point array, we thoroughly investigated the applicability of it in the previous chapter. From numerous data it was proved that the application of NiSi not only helped the nano-wedge RRAM device to

reduce switching parameters ($V_{FORMING}/V_{SET}/V_{RESET}$) but to improved reliability properties such as endurance and retention. Due to the unavoidable wire resistance the current summation could be reduced, however, measured resistivity demonstrated that NiSi has lower value compared to that of Si. Results further support that decreased resistivity is able to contribute to reduction of current summation during the vector-matrix multiplication process.

In this chapter, we introduce the characterization of $TiO_{\underline{x}}$ based NiSi BE nano-wedge RRAM cross-point array with the size expansion of 8 × 8 and 16 × 16. Deep analysis of fabricated RRAM array with two different sizes as well as different active materials (highly-doped n^+-Si and NiSi) are going to be treated.

3.1 Device structure and fabrication process

Fabrication process of Si and NiSi BE nano-wedge RRAM array has been gone through exactly the same with that of single device, except for the different layout we used. Fig. 3.1 depicts the layout of 8 × 8 and 16 × 16 cross-point nano-wedge RRAM array. Fig. 3.1 (a) is 8 × 8 array which is integrated in two while Fig. 3.1 (b) is 16 × 16 array. For both array size the pink layout is the active used for bit-line while green layout is word-lines. The blue part is a screen layer layout for preventing a peripheral area from getting ion implantation, which may short the device. The Fig. 2.26 and Fig. 2.27 is the basic process flow of NiSi BE nano-wedge RRAM single device which follow exactly the same when fabricating the cross-point array. Fig. 3.2 is the top view of the Scanning Electron Microscopy (SEM) image taken after the wedge arrays were fabricated. It is noticeable that there are two 8 × 8 arrays integrated due to remove the residual area left within the die.

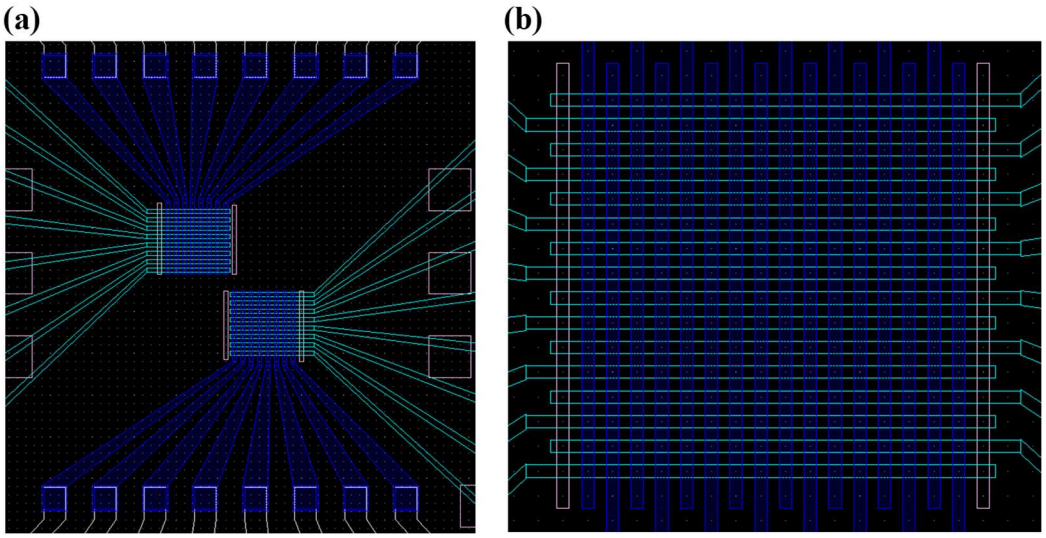


Fig. 3.1. Layout of the fabricated cross-point nano-wedge RRAM array. (a) is 8 × 8 array which is integrated two arrays within the equal die thanks to the areal utilization and (b) shows 16 × 16 passive array layout. Bit-line active bottom electrode is located in a vertical direction while word-line top electrode in the horizontal direction.

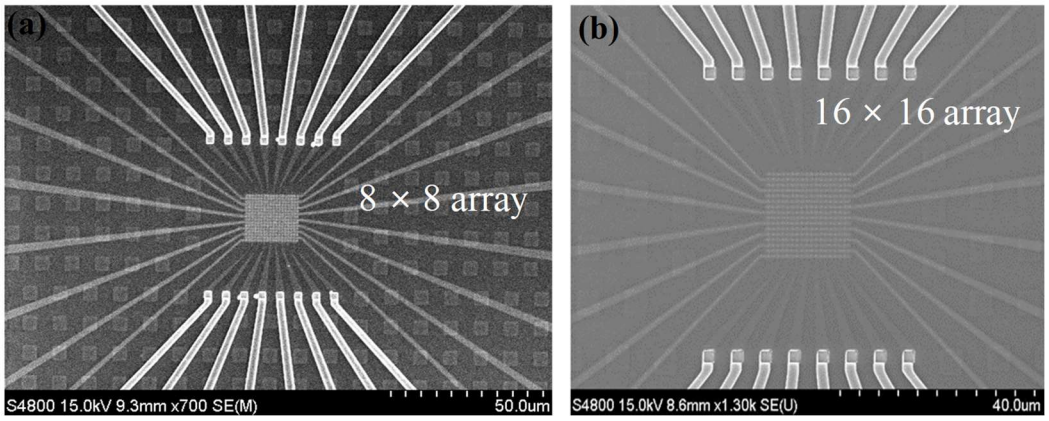


Fig. 3.2. Top view of SEM images for 8 × 8 array (a) and 16 × 16 nano-wedge RRAM array (b).

Due to the non-automatic wet-etching process through TMAH wet etchant, it is difficult to minimize all the wedge tip size to equal width. The minimum width of wedge structure we achieved is around 4 nm (Fig. 2.28 (b)), but there still exists variations among them. Fig. 3.3 illustrates the cross-sectional view of TEM images taken after FIB sample is prepared. As seen from the figure, it is confirmed that each bit-line of array is well-formed with wedge structures.

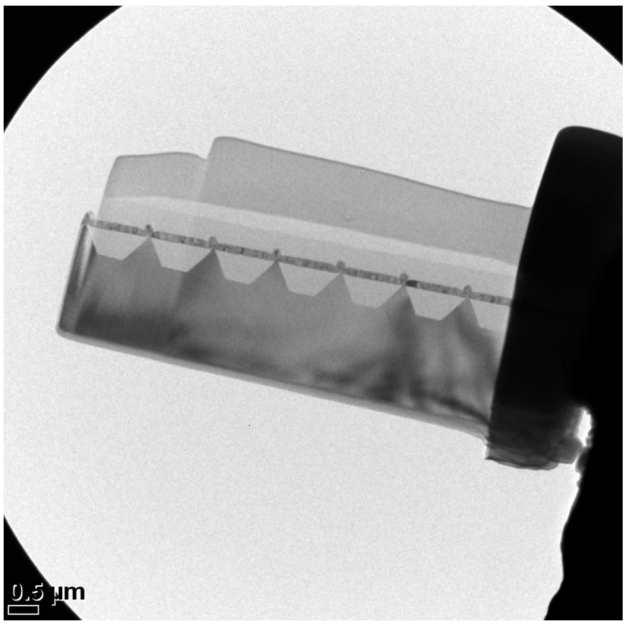


Fig. 3.3. Cross-sectional Transmission Electron Microscopy (TEM) image of the fabricated nano-wedge RRAM array. Clear wedge-structure with the pitch of 1 μm is confirmed while TEOS layer (SiO_2) isolation is deposited in-between.

3.2 Electrical characteristics

Switching characteristics of the fabricated nano-wedge RRAM array is different from those of single RRAM device due to the existence of wire resistance. Unlike metal bottom electrode RRAM array with almost no wire resistance, silicon BE RRAM array suffers from current output reduction by the wire resistance. Fig. 3.4 shows the DC IV of 8 × 8 array for NiSi BE (a) and highly-doped Si BE (b) nano-wedge RRAM array. From the Fig. 3.4 (a), current levels rise over hundreds of μA due to the addition of sneak path current. This result is attributed to the worst case situation as depicted in Fig. 3.5. Each array cell in red color indicates the switched ON state, where current flows through every path and lead to sneak current addition while reading the selected cell (SC). In order to prevent the sneak current issue, it is imperative to add a diode or selector that prevents reverse-biased current flow. Yet, the fabricated nano-wedge RRAM array has no such reverse current prevention function, thus it is inevitable to apply a scheme to minimize the sneak path current. The Fig. 3.4

(b) is the IV of Si BE 8 × 8 wedge RRAM array. Current levels range from a few μA to sub-nA indicate some un-switchable cells exist. Due to a large wire resistance of highly-doped Si BE RRAM device and an interfacial layer (IL) formed above the wedge Si (as explained in the Fig. 2.11 (a)), un-switchable RRAM cells are regarded as dead cells, leading to a reduction of array size. Cells with a few μA may have lower resistance than the measured current level, however, the reduction of current may be attributed to the existence of wire resistance which is not negligible.

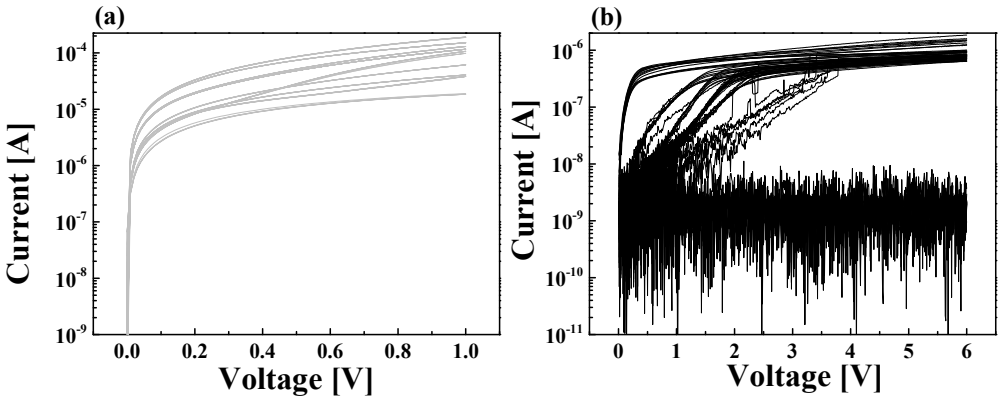


Fig. 3.4. DC switching characteristics of NiSi BE (a) and highly-doped Si BE (b) nano-wedge RRAM array for the size of 8 × 8 array. Due to the existence of wire resistance, the IV curve exhibits at lower current level compared to that of single device. Sneak path current from NiSi BE array affects the current level, leading to increased output current.

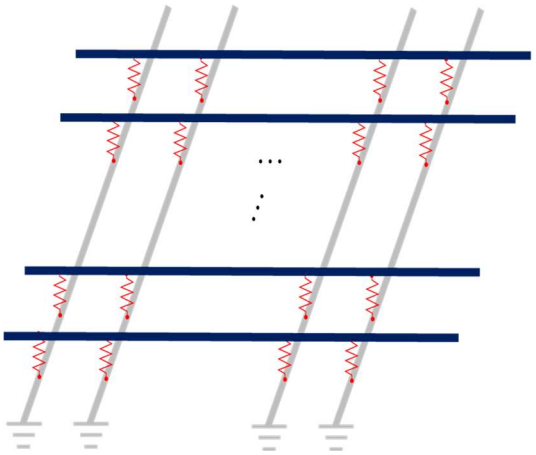


Fig. 3.5. Worst case passive RRAM array with all cells switched ON. Sneak path current flows through every single cell when measuring the selected cell (SC), leading to the current overflow.

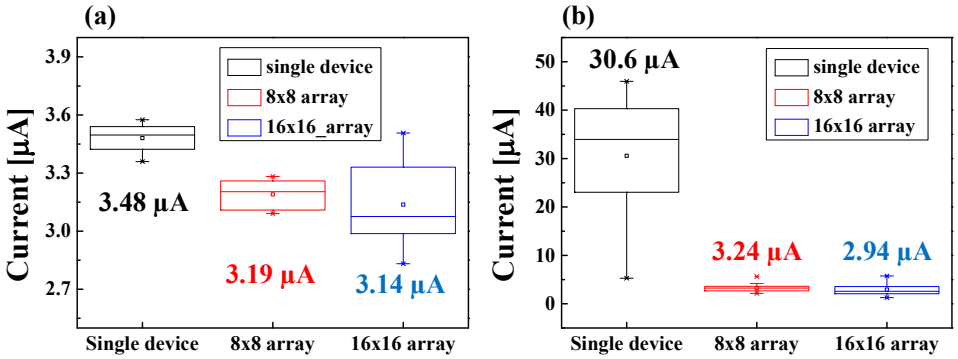


Fig. 3.6. Distribution of current level measured from single device, 8 × 8 and 16 × 16 nano-wedge cross-point arrays. The average value measured from each type of device is stated in the databox. (a) is the current values of NiSi BE RRAM and (b) is those of highly-doped Si BE RRAM.

Fig. 3.6 illustrates the distribution of current level from single and array level RRAM device. Fig. 3.6 (a) is the current level distribution of NiSi BE while the Fig. 3.6 (b) is that of highly doped Si BE RRAM device. When the bottom electrode consists of NiSi, the current reduction level is minimized with difference of 9.7 %. In contrast, Si BE RRAM device exhibits in large difference between single and array level cell. The average current level of Si BE single RRAM device is 30.6 μA while that of 8 × 8 and 16 × 16 array is 3.24 μA and 2.94 μA, respectively. These values are more than 90% reduction from those of single RRAM device, pointing out the huge current loss by large voltage drop occurred in Si bit-lines.

Chapter 4

Hardware implementation as a synaptic device

Once the material and structural analysis of the optimized RRAM synaptic array have been demonstrated from previous chapters, it is necessary to operate the vector-matrix multiplication (VMM) to verify the feasibility of the fabricated NiSi BE nano-wedge RRAM array. As suggested in the Chapter 1, one of critical requirement of synaptic devices is to operate at low power. Unless diminished switching power is guaranteed, it is unable to implement in large size cross-point array because of high energy load. As indicated in Fig. 4.1 (a), the biological function of synapse is achieved by transmitting chemicals

while the electronic synaptic device works by receiving and transmitting spikes (b). Furthermore, there are more than 10^{11} neurons and 10^{14} synapses in human neural network. As such, total energy consumption within the network is only about 20 W which is part of keeping human cognitive system. Similar to the parallel computing system, it is imperative to keep the energy consumption as low as possible to stabilize the neural network.

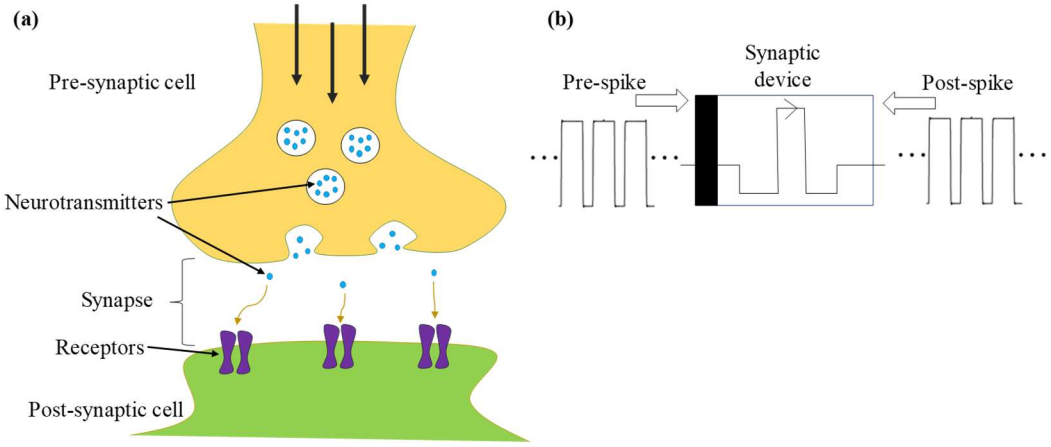


Fig. 4.1. Schematic of biological synapse (a) and electronic synapse device with pre- and post-spike used for input and output signal, respectively (b).

In this chapter, we performed the VMM on the fabricated highly-doped n^+-Si and NiSi BE nano-wedge RRAM array to compare each other and confirm the improvement achieved by Nickel Silicidation. Not limited to the measurement, we made an effort to measure the approximate wire resistance of the fabricated RRAM array. Spice simulation confirmed us to search for the optimized ratio between cells and wire resistance to minimize the current reduction during the VMM operation.

4.1 Vector-matrix multiplication

Fig. 4.2 illustrates the schematic of the array we used for the vector-matrix multiplication. We kept the unselected cells (USCs) in high resistance states (HRS) while turning the selected cell (SC) in low resistance state (LRS) to measure the current flow. For the biasing scheme, 1 V was applied to the word-line (WL) while grounding the bit-line (BL). As explained in the Fig. 4.2, $G_{1,1}$ is the conductance of the SC while I_1 is the multiplication of the applied bias (1 V) and the $G_{1,1}$. This is how the VMM is performed in the synaptic array. By measuring each SCs in the selected BL while grounding all the rest unselected WLs and BLs, we compared the current output when accessing the WLs simultaneously as depicted in the leftist schematic in the Fig. 4.2. This way we can calculate the current reduced ($I_{REDUCTION}$) compared to the summation of individual cells, as defined in the equation 4.1.

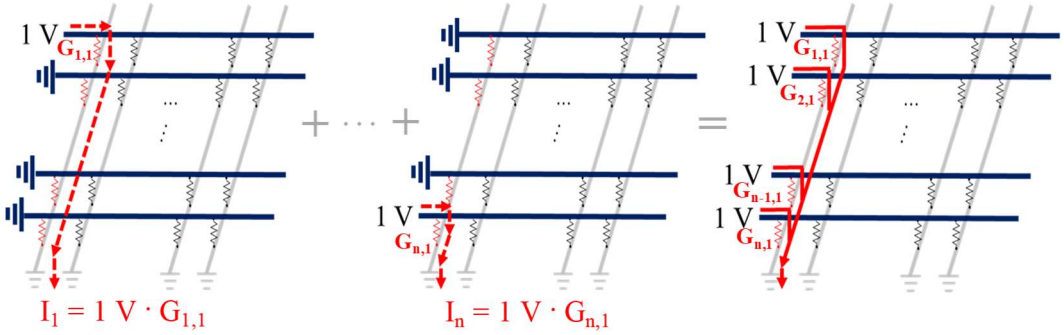


Fig. 4.2. Schematic of the VMM operation on the fabricated nano-wedge RRAM array. While keeping the unselected cells (USCs) in high resistive states, we performed application of 1 V on the selected word-line (WL) while grounding the bit-line (BL) to measure the single cell within the array and inhibit the sneak current paths.

$$I_{REDUCTION}\,[\%] = \frac{\Sigma I_{Individual\ access} - \Sigma I_{Simultaneous\ access}}{\Sigma I_{Individual\ access}} \times 100$$

Equation 4.1. Definition of $I_{REDUCTION}$ during the vector-matrix multiplication operation.

Above equation 4.1 is the definition of the $I_{REDUCTION}$, which is a result of wire resistance. Existence of BL resistance lead to the series resistor connected with the selected cell (SC), which forcefully induce the voltage dividing effect and current reduction as a result of increased total resistance. Only solution to this issue is to remove or minimized the BL resistance. As shown in Fig. 4.3, the cells within the array were switched as applied to single devices. Fig. 4.4 and Fig. 4.5 are data plotted for current measured on the selected BL and simultaneous access of 8 × 8 and 16 × 16 size array, respectively. In the Fig. 4.4, a variation of current levels is clear as the cell location approaches to the BL (which is biased to ground, gnd). Due to the reduction of BL length as the cell is getting nearer to the gnd, less current reduction is measured as the total series resistance decreases. The difference of smallest and biggest current levels is around 1 μA while nearly all cells have identical current levels in NiSi BE nano-wedge RRAM array. The $I_{REDUCTION}$, which is achieved by simultaneous access to all the WLs as shown in the Fig. 4.2, has a value of

42.7 % and 4.3 % for the highly-doped Si BE and NiSi BE cross-point array (Fig. 4.4). The reduction level gets worse when the array size is expanded to 16 × 16 for both types of arrays, indicating the rise of wire resistances. In the Fig. 4.5, the reduction rate increases to 65.8 % and 19.1 %, respectively. Although it is unavoidable to prevent wire resistances, we demonstrated the reduction of current becomes significant with Si bottom electrode and large size array. This also indicates that the NiSi BE nano-wedge RRAM array performed with less current reduction which paves a way for application of synaptic device in the hardware-implemented neuromorphic computing.

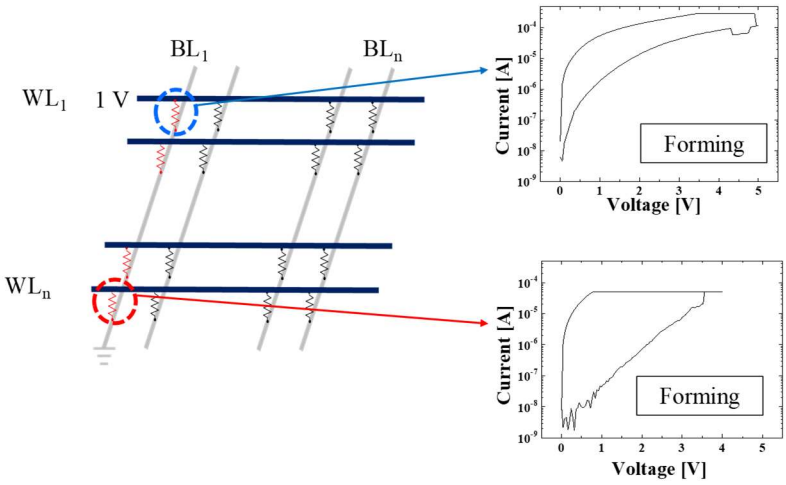


Fig. 4.3. Forming process of the selected cells in the selected BL.

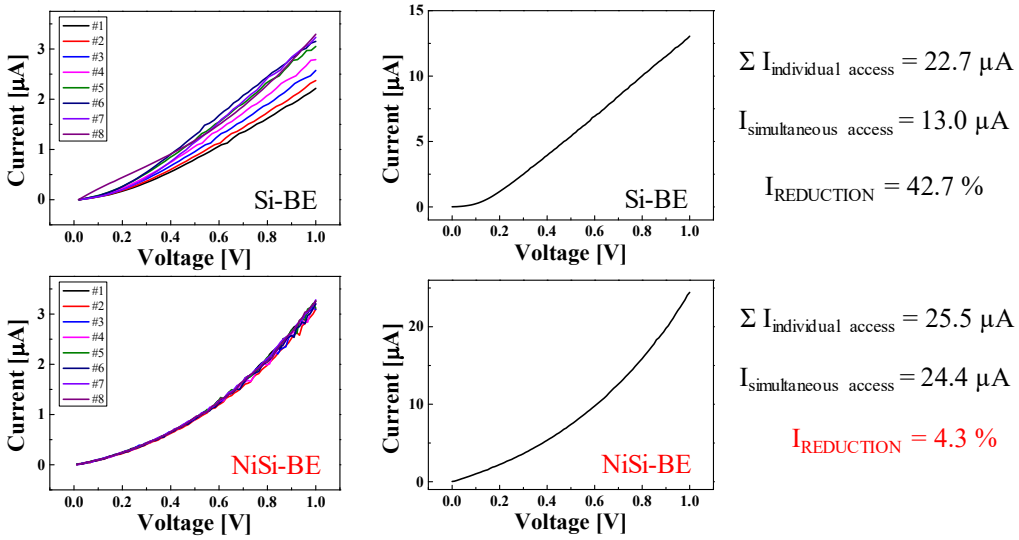


Fig. 4.4. Data showing the cell measurement of 8 × 8 nano-wedge RRAM array in the selected BL individually and simultaneously. $I_{REDUCTION}$ values are stated beside.

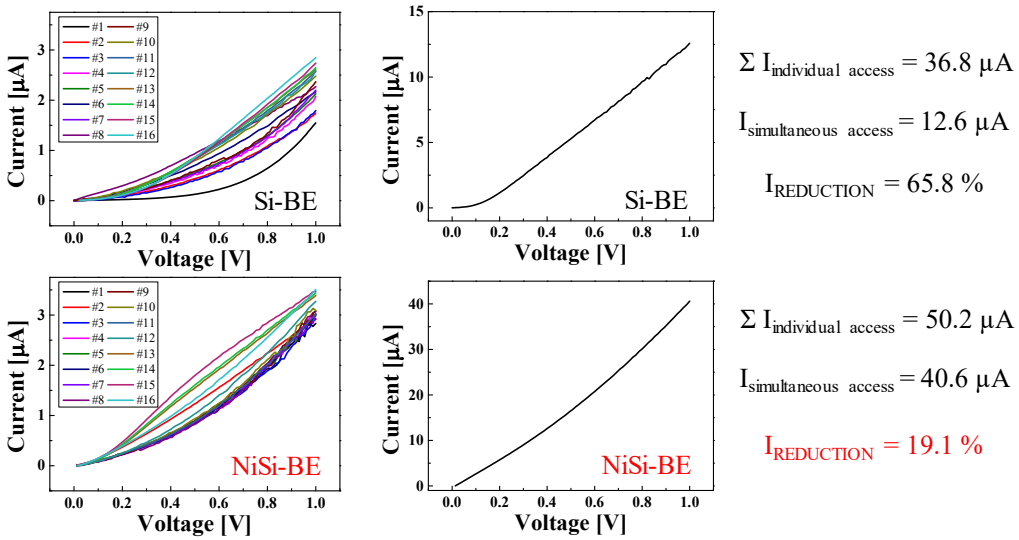


Fig. 4.5. Data showing the cell measurement of 16 × 16 nano-wedge RRAM array in the selected BL individually and simultaneously. $I_{REDUCTION}$ values are stated beside.

Based on the current summation of selected BL as shown in the Fig. 4.4 and 4.5, $I_{REDUCTION}$ has been further measured by expanding to rest BLs of 8 × 8 and 16 × 16 wedge RRAM array as depicted in Fig. 4.6 and 4.7, respectively. Bit-line # indicates the order of selected BL from the left to right side of the array. In the Fig. 4.6 (a), larger differences between the summation of individual access and simultaneous access are seen while those from the Fig. 4.6 (b) are nearly negligible. This demonstrates that less current reduction occurs while VMM is measured from NiSi BE wedge RRAM array. Similarly, for 16 × 16 wedge RRAM array the data of individual and simultaneous access are plotted in the Fig. 4.7. Although both Fig. 4.7 (a) and (b) seem to have no large difference in current summation amount, average $I_{REDUCTION}$ of NiSi BE wedge RRAM array is only 18%, while that of n^+-Si BE array reaches above 66%.

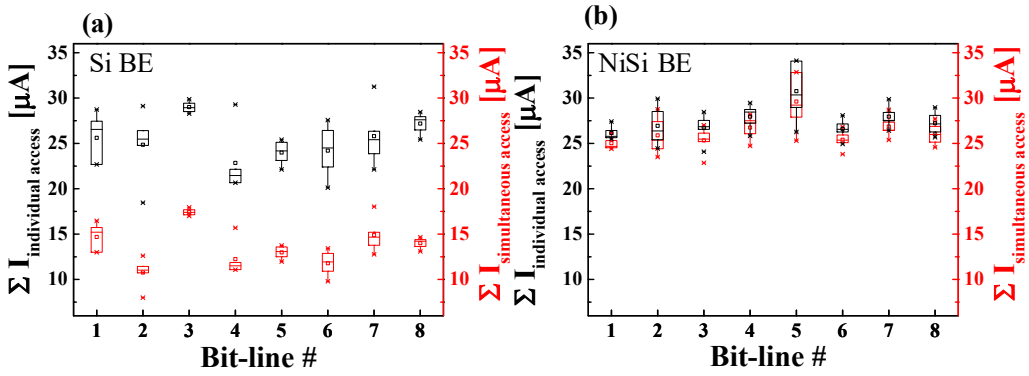


Fig. 4.6. Comparison of the VMM of individual (black) and simultaneous (red) access for 8 × 8 wedge RRAM array with Si BE (a) and NiSi BE (b).

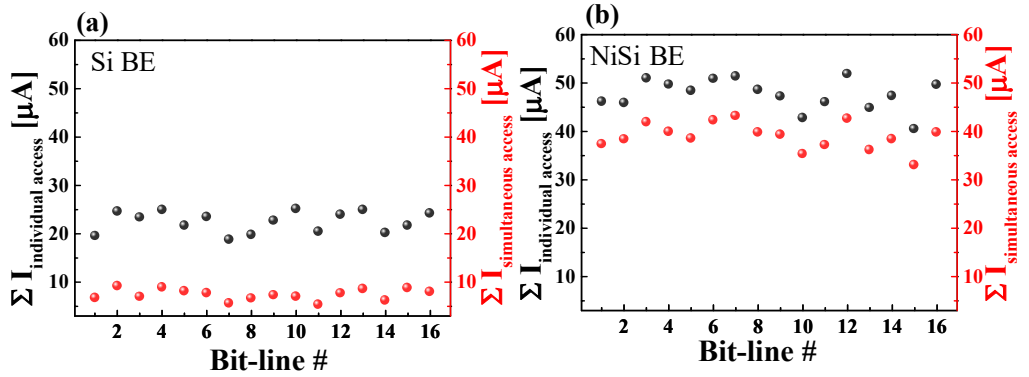


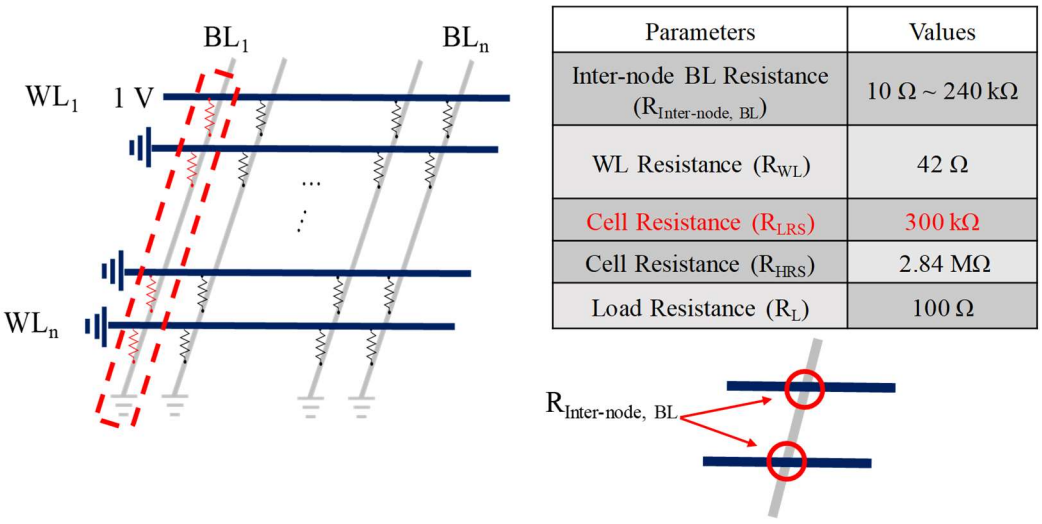
Fig. 4.7. Comparison of the VMM of individual (black) and simultaneous (red) access for 16 × 16 wedge RRAM array with Si BE (a) and NiSi BE (b).

4.2 Spice simulation for optimization of cell to wire resistance

It is essential to keep the wire resistance of RRAM array minimum while keeping the array cell resistance in its high state. In other words, the ratio of wire resistance (R_{BL}) and cell resistance (R_{LRS}) determines the current reduction during the vector-matrix multiplication. In Fig. 4.6, parameters used for SPICE circuit simulation are written with the range of values for inter-node BL resistance. We multiplied the $R_{Inter\text{-}node,\ BL}$ with 8 and 16 depending on the target array size. Cell resistance was fixed at 300 kΩ and 2.84 MΩ for low and high resistance state, respectively. Fig. 4.7 is the simulation result of current as the location is changing. As shown in the Fig. 4.7, the selected cells in blue and red color indicate the one located at the farthest and nearest with respect to the ground on the selected BL. This location dependent current level is plotted at the right side of the Fig. 4.7, where the value is decreasing as both the location and $R_{inter\text{-}node,\ BL}$ increases. ΔI is the current difference between the nearest (red)

and the farthest (blue) cell. As the wire resistance increases, the ΔI also increases. This proves that the current reduction exacerbates as the wire resistance rises.

In order to search for the optimized ratio between cell and wire resistance, we simulated the current summation by changing the wire and cell resistance as well as the cell size. Fig. 4.8 depicts the simulated data of $I_{REDUCTION}$ during the VMM operation. It is confirmed that the reduction rate in kept below 2 % when the cell to wire resistance (R_{LRS} / R_{BL}) is kept above 2 orders of magnitude.



Parameters	Values
Inter-node BL Resistance ($R_{Inter\text{-}node,\ BL}$)	10 Ω ~ 240 kΩ
WL Resistance (R_{WL})	42 Ω
Cell Resistance (R_{LRS})	300 kΩ
Cell Resistance (R_{HRS})	2.84 MΩ
Load Resistance (R_L)	100 Ω

Fig. 4.8. Parameters and values used for SPICE circuit simulation.

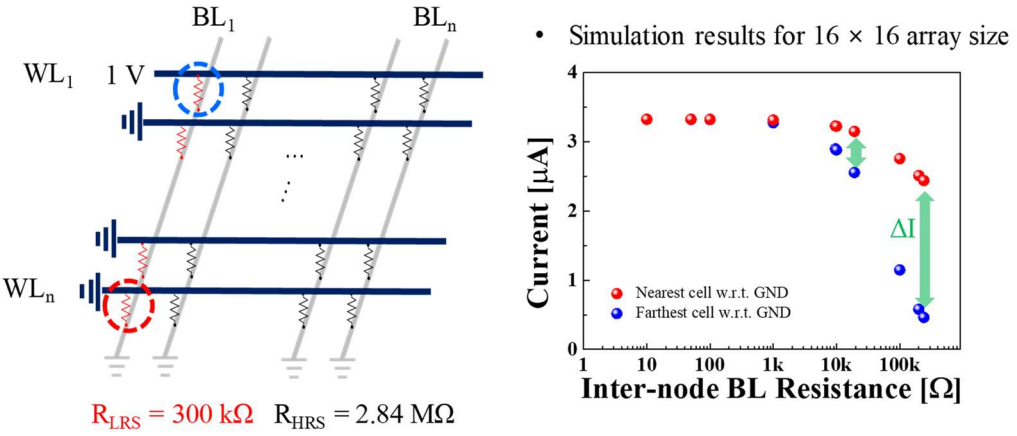


Fig. 4.9. Simulation results for reduction of the selected cell current as the bit-line (BL) resistance increases. The R_{LRS} and R_{HRS} values are also stated.

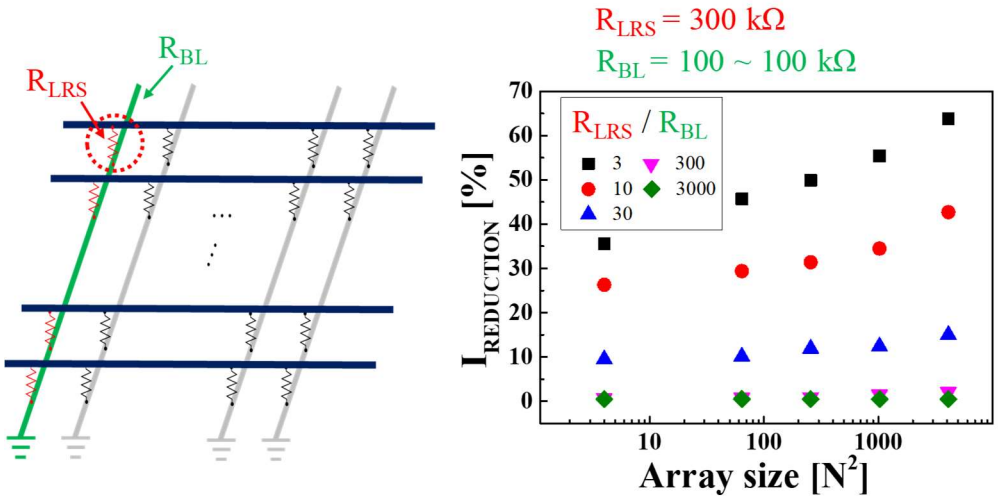


Fig. 4.10. Simulation results for the $I_{REDUCTION}$ as the array size increases. R_{LRS} and R_{BL} indicate the low resistance state of the selected bit-line (BL) and resistance of BL. The reduction rate becomes significant as R_{LRS}/R_{BL} ratio is reduced.

4.3 Estimation of NiSi BE wire resistance

It is of utmost importance to utilized bi-lines with minimized resistance so that the read current of the SC in the array is not reduced during the VMM. In order to measure the accurate bit-line (BL) resistance of the fabricated NiSi BE wedge RRAM array, read current (I_{READ}) through the SC was measured as shown in Fig. 4.11. Left side illustrates the cell (R_{cell}) and inter-node cell ($R_{inter-cell}$) that form a single wire while reading the current by biasing the selected WL. According to the Ohm's Law, I_{READ} is determined by dividing the summation of series connection of R_{cell} and $R_{inter-node}$ by 1 V (read voltage). Array size (n) indicates the number of nodes so that the I_{READ} depends on the position of the selected cell with respect to the ground (gnd).

Fig. 4.12 and 4.13 depict the measured resistance of the SC in the fabricated 8 × 8 and 16 × 16 nano-wedge RRAM array, respectively. As the location of cell gets close to the gnd, the resistance decreases. This proves the reduction of the BL effect as the cell is getting nearer to the gnd. Offset is the

resistance of $R_{inter\text{-}node}$. Compared to Si BE array, NiSi BE array has uniform cell resistance (R_{cell}) regardless of the cell position with respect to the gnd, demonstrating the low resistivity of the NiSi.

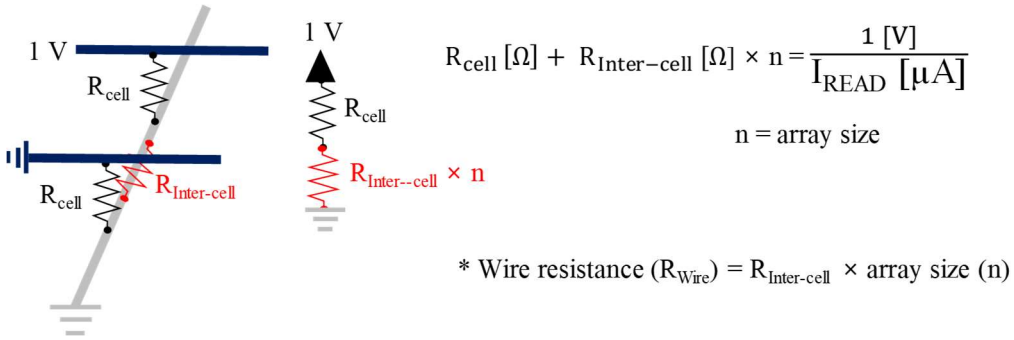


Fig. 4.11. Schematic of the read current measurement according to the Ohm's Law. Wire resistance of the selected cell depends on the value of array size (n).

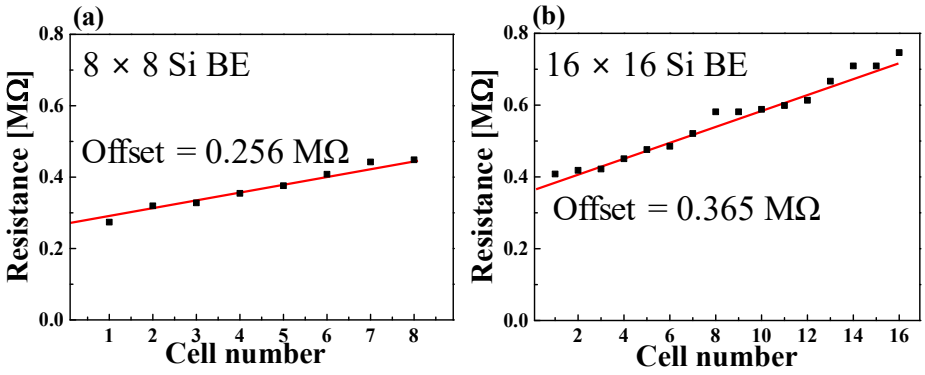


Fig. 4.12. Resistance of the selected cell (SC) of n^+-Si BE array with respect to the gnd position. As the cell gets close to the gnd, the resistance also decreases, indicating the reduction of BL effect on the SC.

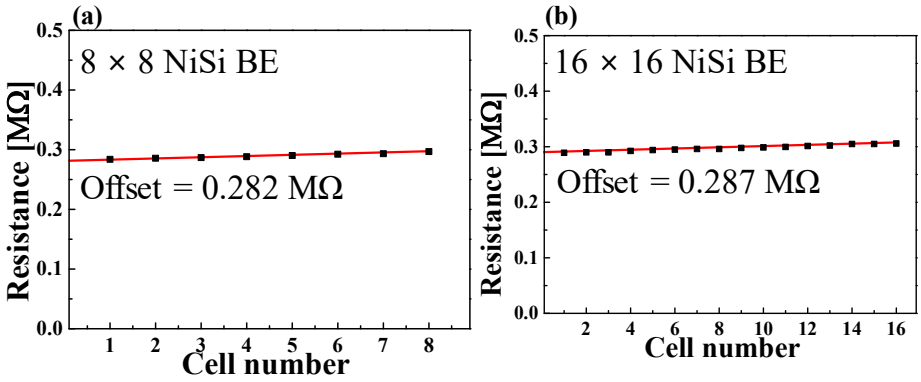


Fig. 4.13. Resistance of the selected cell (SC) of NiSi BE array with respect to the gnd position. As the cell gets close to the gnd, the resistance also decreases, indicating the reduction of BL effect on the SC.

For all 8 BLs of the 8 × 8 wedge RRAM array, $R_{inter\text{-}cell}$ has been measured for both types of BL and results are plotted as shown in the Fig. 4.14. In average, wire resistance of NiSi BE array is reduced by more than 1 order of magnitude compared to that of Si BE RRAM array, indicating the purpose of wire resistance reduction has been achieved by Ni silicidation of the highly doped Si BE.

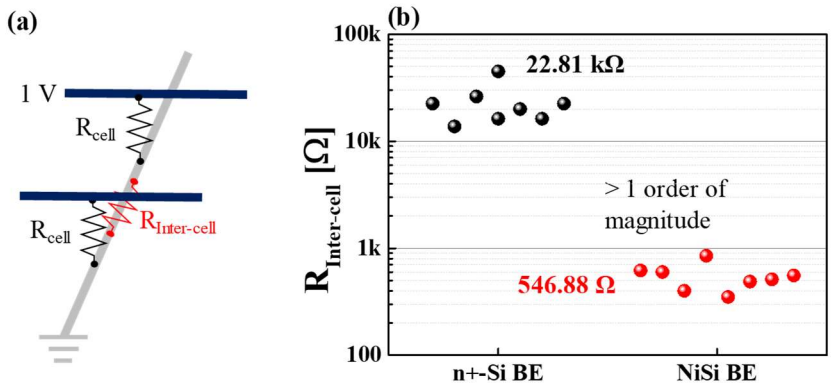


Fig. 4.14. Schematic of the cell measurement (a) and comparison of n^+-Si and NiSi BE array (b).

Chapter 5

Conclusion

In this thesis dissertation, we investigated the electrical characteristics of nano-wedge RRAM array with Ni silicided bottom electrode. Although conventional Si BE proved several advantages over those of metal-insulator-metal RRAM such as low current level and switching power, device-to-device and cycle-to-cycle variations still hindered metal-insulator-silicon RRAM from practically applied as synaptic devices. By silicidation process of Si BE, not only resistance of the active reduced but the uniformity and gradual characteristics were also improved. Current overshoot issue from the Si BE

RRAM device was also relieved with silicided BE by applying the pulse switching operation. We carried out SPICE simulation to optimize the resistance ratio of cell and wire to reduce the current reduction.

First, the NiSi BE RRAM in single device was fabricated to analyze the basic properties of DC and pulse switching characteristics. Anisotropic wet etching via TMAH solution was processed to form the wedge structure of Si, thereby minimizing the width of BE. Measurement results showed the reduction of switching voltages and power consumption compared to those of Si BE RRAM device.

Next, cross-point array was fabricated to operate the vector-matrix multiplication. By reducing the wire resistance of NiSi bit-line by 3 orders of magnitude, less current reduction was achieved during the current summation operation. Low ON current as a result of overshoot current suppression proved the validity of NiSi BE RRAM as a synaptic device application for neuromorphic computing.

Bibliography

[1] R. Bez and P. Cappelletti, "Flash memory and beyond," in *IEEE VLSI-TSA International Symposium on VLSI Technology, 2005. (VLSI-TSA-Tech).* 25-27 April 2005 2005, pp. 84-87, doi: 10.1109/VTSA.2005.1497090.

[2] J. A. Kittl *et al.*, "High-k dielectrics for future generation memory devices (Invited Paper)," *Microelectronic Engineering,* vol. 86, no. 7, pp. 1789-1795, 2009/07/01/ 2009, doi: https://doi.org/10.1016/j.mee.2009.03.045.

[3] H. P. Wong *et al.*, "Metal–Oxide RRAM," *Proceedings of the IEEE,* vol. 100, no. 6, pp. 1951-1970, 2012, doi: 10.1109/JPROC.2012.2190369.

[4] Y. Fang *et al.*, "Improvement of HfO x-Based RRAM Device Variation by Inserting ALD TiN Buffer Layer," *IEEE Electron Device Letters,* vol. 39, no. 6, pp. 819-822, 2018.

[5] S. Larentis, F. Nardi, S. Balatti, D. C. Gilmer, and D. Ielmini, "Resistive Switching by Voltage-Driven Ion Migration in Bipolar RRAM—Part II: Modeling," *IEEE Transactions on Electron Devices,* vol. 59, no. 9, pp. 2468-2475, 2012, doi: 10.1109/TED.2012.2202320.

[6] H. Wang and X. Yan, "Overview of resistive random access memory (RRAM): Materials, filament mechanisms, performance optimization, and prospects," *physica status solidi (RRL)–Rapid Research Letters,* vol. 13, no. 9, p. 1900073, 2019.

[7] S. Kim, J. Zhou, and W. D. Lu, "Crossbar RRAM arrays: Selector device requirements during write operation," *IEEE Transactions on Electron Devices,* vol. 61, no. 8, pp. 2820-2826, 2014.

[8] W. Liu, K.-L. Pey, N. Raghavan, and C. M. Ng, "Fabrication of RRAM Cell Using CMOS Compatible Processes," ed: Google Patents, 2012.

[9] K. Moon *et al.*, "RRAM-based synapse devices for neuromorphic systems," *Faraday discussions,* vol. 213, pp. 421-451, 2019.

[10] D. Ielmini, "Brain-inspired computing with resistive switching memory (RRAM): Devices, synapses and neural networks," *Microelectronic Engineering,* vol. 190, pp. 44-53, 2018/04/15/ 2018, doi: https://doi.org/10.1016/j.mee.2018.01.009.

[11] S. Ambrogio *et al.*, "Neuromorphic learning and recognition with one-transistor-one-resistor synapses and bistable metal oxide RRAM," *IEEE Transactions on Electron Devices,* vol. 63, no. 4, pp. 1508-1515, 2016.

[12] S. Park *et al.*, "RRAM-based synapse for neuromorphic system with pattern recognition function," in *2012 International Electron Devices Meeting*, 10-13 Dec. 2012 2012, pp. 10.2.1-10.2.4, doi: 10.1109/IEDM.2012.6479016.

[13] L. Ni, H. Huang, Z. Liu, R. V. Joshi, and H. Yu, "Distributed In-Memory Computing on Binary RRAM Crossbar," *J. Emerg. Technol. Comput. Syst.,* vol. 13, no. 3, p. Article 36, 2017, doi: 10.1145/2996192.

[14] L. Ni, Y. Wang, H. Yu, W. Yang, C. Weng, and J. Zhao, "An energy-efficient matrix multiplication accelerator by distributed in-memory computing on binary RRAM crossbar," in *2016 21st Asia and South Pacific Design Automation Conference (ASP-DAC)*, 2016: IEEE, pp. 280-285.

[15] Y. Liao *et al.*, "Novel in-memory matrix-matrix multiplication with resistive cross-point arrays," in *2018 IEEE Symposium on VLSI Technology*, 2018: IEEE, pp. 31-32.

[16] M. Hu *et al.*, "Dot-product engine for neuromorphic computing: Programming 1T1M crossbar to accelerate matrix-vector multiplication," in *2016 53nd ACM/EDAC/IEEE Design Automation Conference (DAC)*, 2016: IEEE, pp. 1-6.

[17] S. Z. Rahaman *et al.*, "Scalability and reliability issues of Ti/HfO x-based 1T1R bipolar RRAM: Occurrence, mitigation, and solution,"

Applied Physics Letters, vol. 110, no. 21, p. 213501, 2017.

[18] L. Zhang *et al.*, "Experimental investigation of the reliability issue of RRAM based on high resistance state conduction," *Nanotechnology,* vol. 22, no. 25, p. 254016, 2011/05/16 2011, doi: 10.1088/0957-4484/22/25/254016.

[19] J.-J. Huang, C.-W. Kuo, W.-C. Chang, and T.-H. Hou, "Transition of stable rectification to resistive-switching in Ti/TiO 2/Pt oxide diode," *Applied Physics Letters,* vol. 96, no. 26, p. 262901, 2010.

[20] S. Kim and Y. Choi, "A Comprehensive Study of the Resistive Switching Mechanism in $\hbox{Al/TiO}_{x}/\hbox{TiO}_{2}/\hbox{Al}$-Structured RRAM," *IEEE Transactions on Electron Devices,* vol. 56, no. 12, pp. 3049-3054, 2009, doi: 10.1109/TED.2009.2032597.

[21] S. Kim, Y.-F. Chang, M.-H. Kim, and B.-G. Park, "Improved resistive switching characteristics in Ni/SiN x/p++-Si devices by tuning x," *Applied Physics Letters,* vol. 111, no. 3, p. 033509, 2017.

[22] S. Kim, S. Cho, K.-C. Ryoo, and B.-G. Park, "Effects of conducting defects on resistive switching characteristics of SiN x-based resistive random-access memory with MIS structure," *Journal of Vacuum Science & Technology B, Nanotechnology and Microelectronics: Materials, Processing, Measurement, and Phenomena,* vol. 33, no. 6, p. 062201, 2015.

[23] S. Kim *et al.*, "Scaling effect on silicon nitride memristor with highly doped Si substrate," *Small,* vol. 14, no. 19, p. 1704062, 2018.

[24] S. Kim *et al.*, "Nano-cone resistive memory for ultralow power operation," *Nanotechnology,* vol. 28, no. 12, p. 125207, 2017.

[25] S. Kim, S. Cho, and B.-G. Park, "Fully Si compatible SiN resistive switching memory with large self-rectification ratio," *AIP Advances,* vol. 6, no. 1, p. 015021, 2016.

[26] Z. Wang *et al.*, "Memristors with diffusive dynamics as synaptic emulators for neuromorphic computing," *Nature materials,* vol. 16, no.

1, pp. 101-108, 2017.

[27] S. Yu, B. Gao, Z. Fang, H. Yu, J. Kang, and H.-S. P. Wong, "A neuromorphic visual system using RRAM synaptic devices with sub-pJ energy and tolerance to variability: Experimental characterization and large-scale modeling," in *2012 International Electron Devices Meeting*, 2012: IEEE, pp. 10.4. 1-10.4. 4.

[28] J. Woo *et al.*, "Improved synaptic behavior under identical pulses using AlO x/HfO 2 bilayer RRAM array for neuromorphic systems," *IEEE Electron Device Letters,* vol. 37, no. 8, pp. 994-997, 2016.

[29] S. Kim *et al.*, "Neuronal dynamics in HfO x/AlO y-based homeothermic synaptic memristors with low-power and homogeneous resistive switching," *Nanoscale,* vol. 11, no. 1, pp. 237-245, 2019.

[30] M.-H. Kim *et al.*, "Pulse area dependent gradual resistance switching characteristics of CMOS compatible SiNx-based resistive memory," *Solid-State Electronics,* vol. 132, pp. 109-114, 2017.

[31] J. Woo *et al.*, "Multi-layer tunnel barrier (Ta2O5/TaOx/TiO2) engineering for bipolar RRAM selector applications," in *2013 Symposium on VLSI Technology*, 11-13 June 2013 2013, pp. T168-T169.

[32] U. Chand, K. Huang, C. Huang, and T. Tseng, "Mechanism of Nonlinear Switching in HfO2-Based Crossbar RRAM With Inserting Large Bandgap Tunneling Barrier Layer," *IEEE Transactions on Electron Devices,* vol. 62, no. 11, pp. 3665-3670, 2015, doi: 10.1109/TED.2015.2471835.

[33] G. Bersuker *et al.*, "Metal oxide RRAM switching mechanism based on conductive filament microscopic properties," in *2010 International Electron Devices Meeting*, 6-8 Dec. 2010 2010, pp. 19.6.1-19.6.4, doi: 10.1109/IEDM.2010.5703394.

[34] A. Fantini *et al.*, "Intrinsic switching variability in HfO2 RRAM," in *2013 5th IEEE International Memory Workshop*, 26-29 May 2013 2013, pp. 30-33, doi: 10.1109/IMW.2013.6582090.

[35] D. C. Gilmer *et al.*, "Effects of RRAM Stack Configuration on Forming Voltage and Current Overshoot," in *2011 3rd IEEE International Memory Workshop (IMW)*, 22-25 May 2011 2011, pp. 1-4, doi: 10.1109/IMW.2011.5873225.

[36] K. Beckmann, J. Holt, H. Manem, J. Van Nostrand, and N. C. Cady, "Nanoscale Hafnium Oxide RRAM Devices Exhibit Pulse Dependent Behavior and Multi-level Resistance Capability," *MRS Advances,* vol. 1, no. 49, pp. 3355-3360, 2016/10/01 2016, doi: 10.1557/adv.2016.377.

[37] H. García, O. G. Ossorio, S. Dueñas, and H. Castán, "Controlling the intermediate conductance states in RRAM devices for synaptic applications," *Microelectronic Engineering,* vol. 215, p. 110984, 2019/07/15/ 2019, doi: https://doi.org/10.1016/j.mee.2019.110984.

[38] D. Ielmini and H. S. P. Wong, "In-memory computing with resistive switching devices," *Nature Electronics,* vol. 1, no. 6, pp. 333-343, 2018/06/01 2018, doi: 10.1038/s41928-018-0092-2.

[39] J. Liu *et al.*, "An electronic synaptic device based on HfO2TiOx bilayer structure memristor with self-compliance and deep-RESET characteristics," *Nanotechnology,* vol. 29, no. 41, p. 415205, 2018.

[40] G. Jurczak, "Advances and trends of RRAM technology," in *Proc. SEMICON*, 2015, pp. 1-31.

[41] J. Lee, J. Park, S. Jung, and H. Hwang, "Scaling effect of device area and film thickness on electrical and reliability characteristics of RRAM," in *2011 IEEE International Interconnect Technology Conference*, 8-12 May 2011 2011, pp. 1-3, doi: 10.1109/IITC.2011.5940297.

[42] B. Govoreanu *et al.*, "10×10nm2 Hf/HfOx crossbar resistive RAM with excellent performance, reliability and low-energy operation," in *2011 International Electron Devices Meeting*, 5-7 Dec. 2011 2011, pp. 31.6.1-31.6.4, doi: 10.1109/IEDM.2011.6131652.

[43] J. Thong, W. Choi, and C. Chong, "TMAH etching of silicon and the interaction of etching parameters," *Sensors and Actuators A: Physical,*

vol. 63, no. 3, pp. 243-249, 1997.

[44] Z. Lijie, H. Ru, A. Z. H. Wang, W. Dake, W. Runsheng, and K. Yongbian, "The parasitic effects induced by the contact in RRAM with MIM structure," in *2008 9th International Conference on Solid-State and Integrated-Circuit Technology*, 20-23 Oct. 2008 2008, pp. 932-935, doi: 10.1109/ICSICT.2008.4734687.

[45] S. Dueñas *et al.*, "Memory maps: reading RRAM devices without power consumption," *ECS transactions,* vol. 85, no. 8, p. 201, 2018.

[46] Y. Wu *et al.*, "AlOx-Based Resistive Switching Device with Gradual Resistance Modulation for Neuromorphic Device Application," in *2012 4th IEEE International Memory Workshop*, 20-23 May 2012 2012, pp. 1-4, doi: 10.1109/IMW.2012.6213663.

[47] B. Sarkar, B. Lee, and V. Misra, "Understanding the gradual reset in Pt/Al2O3/Ni RRAM for synaptic applications," *Semiconductor Science and Technology,* vol. 30, no. 10, p. 105014, 2015.

[48] Y. Wu, S. Yu, B. Lee, and P. Wong, "Low-power TiN/Al2O3/Pt resistive switching device with sub-20 μA switching current and gradual resistance modulation," *Journal of Applied Physics,* vol. 110, no. 9, p. 094104, 2011.

[49] J. Kim, S. Cho, T. Kim, and J. J. Pak, "Mimicking Synaptic Behaviors with Cross-Point Structured TiO x/TiO y-Based Filamentary RRAM for Neuromorphic Applications," *Journal of Electrical Engineering & Technology,* vol. 14, no. 2, pp. 869-875, 2019.

초 록

인류사회에서 급속도로 성장하는 사물인터넷 시대에서 지속적으로 증가하는 방대한 양의 데이터를 처리하기 위한 뇌신경망을 모방한 하드웨어에 대한 연구가 활발히 진행되고 있다. 기존에 폰 노이만 방식은 순차적으로 데이터를 처리하여 메모리 및 CPU 간의 병목현상으로 인한 실시간 패턴 인식의 정확도 및 속도의 한계에 부딪치고 있으며, 계속해서 발전하는 시대적 요구에 부응하기 위해 효율성을 극대화한 병렬 처리방식이 가능한 뉴로모픽 칩의 개발이 절실해 지고 있다. 기존의 반도체 소자 기술을 활용하여 뉴런 회로 및 시냅스 소자의 구현을 목표로 궁극적이며 신개념의 시스템반도체 개발을 목적으로 두고 있으며, 소리 및 이미지 처리 등 빅데이터를 사람의 뇌처럼 적은 에너지원으로 실시간으로 정밀한 연산 능력을 갖춘 뉴럴 네트워크 창출을 위해 글로벌 Big Tech 업계들간의 협업이 중요해지고 있다.

본 논문에서는 니켈 실리사이드 하부전극을 가지는 웨지구조의 저항 변화 메모리 어레이를 제작하여, 전기적 특성은 물론 시냅스 소자로서의 가소성에 대한 분석을 진행하였다.

먼저, 평면 저항 변화 메모리 소자를 제작하여 기본적인 전기적

특성에 대한 측정을 확인한 후, 실리콘 하부전극에 대한 비등방성 식각을 통해 소자에 대한 스케일링을 진행하였다. 간단한 공정 과정인 습식 식각방식을 통해 수 나노 미터의 폭을 가지는 실리콘 웨지 구조를 구현하였으며, 셀의 스케일링에 따른 동작 전압, 전류 및 저항 변화를 통계적으로 검증하였다.

높은 도핑 농도를 가지는 실리콘 하부 전극의 경우 저항 변화 메모리 적용에 있어 신뢰성에 다소 취약한 현상을 발견하였다. 이를 개선하기 위해 니켈 실리사이드 공정을 추가적으로 진행하여 전극의 비저항을 감소시키고, 이에 따른 소자의 스위칭 파라미터 및 신뢰성의 개선은 물론 시냅스 소자의 가소성도 구현됨을 확인하였다.

마지막으로 웨지구조 저항 변화 메모리 어레이를 제작하여 벡터-행렬 연산을 진행하였다. 단순 도핑된 하부전극 대비, 실리사이드 전극을 활용한 어레이의 낮은 라인저항으로 인해 동일한 비트라인의 전류 합산 연산시 더 낮은 전류감소를 확인하였다. 이로 인해 저전력 및 고효율 하드웨어 기반 뉴로모픽 컴퓨팅 체계의 실현 가능성에 발전을 가져올 것으로 기대한다.

주요어 : 시냅스 소자, 니켈 실리사이드, 웨지구조 저항 변화 메모리 어레이, 라인저항, 뉴로모픽 컴퓨팅.

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