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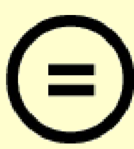

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Ph.D. DISSERTATION

SiGe Nanosheet Tunnel Field-Effect Transistor with High Current Drivability

높은 전류 구동능력을 가지는 SiGe 나노시트 구조의 터널링 전계효과 트랜지스터

BY

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February 2021

DEPARTMENT OF ELECTRICAL AND
COMPUTER ENGINEERING
COLLEGE OF ENGINEERING
SEOUL NATIONAL UNIVERSITY

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이 논문을 공학박사 학위논문으로 제출함

2021년 2월

서울대학교 대학원

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Abstract

The development of very-large-scale integration (VLSI) technology has continuously demanded smaller devices to achieve high integration density for faster computing speed or higher capacity. However, in the recent complementary-metal-oxide-semiconductor (CMOS) technology, simple downsizing the dimension of metal-oxide-semiconductor field-effect transistor (MOSFET) no longer guarantees the boosting performance of IC chips. In particular, static power consumption is not reduced while device size is decreasing because voltage scaling is slowed down at some point. The increased off-current due to short-channel effect (SCE) of MOSFET is a representative cause of the difficulty in voltage scaling. To overcome these fundamental limits of MOSFET, many researchers have been looking for the next generation of FET device over the last ten years. Tunnel field-effect transistor (TFET) has been intensively studied for its steep switching characteristics. Nevertheless, the poor current drivability of TFET is the most serious obstacle to become competitive device for MOSFET.

In this thesis, TFET with high current drivability in which above-mentioned problem is significantly solved is proposed. Vertically-stacked SiGe nanosheet channels are used to boost carrier injection and gate control. The fabrication technique to form highly-condensed SiGe nanosheets is introduced. TFET is fabricated with MOSFET with the same structure in the CMOS-compatible process. Both technology-computer-aided-design (TCAD)

simulation and experimental results are utilized to support and examine the advantages of proposed TFET. From the perspective of the single device, the improvement in switching characteristics and current drivability are quantitatively and qualitatively analyzed. In addition, the device performance is compared to the benchmark of previously reported TFET and co-fabricated MOSFET. Through those processes, the feasibility of SiGe nanosheet TFET is verified. It is revealed that the proposed SiGe nanosheet TFET has notable steeper switching and low leakage in the low drive voltage as an alternative to conventional MOSFET.

Keyword : SiGe channel, Tunnel field-effect Transistor, Multi- nanosheet FET, Low-power device, Steep-switching CMOS device, Subthreshold swing, Ge condensation, Band-to-band tunneling

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Chapter 1

Introduction

1.1. Power Crisis of Conventional CMOS Technology

Since the invention of MOSFET in late 1950s, semiconductor electronics have been dramatically developed. The density of devices in the integrated circuit (IC) chip sharply increases every year and the increase in integration has been directly reflected in the computing speed. Over the four decades, Moore's law [1] and Dennard's scaling theory [2] had effectively predicted the growth of very-large scale integration (VLSI) technology. However, these classical scaling methods for integration trend faced the limitation, such as increasing leakage current caused by thin gate oxide thickness [3]. A simple downsizing did not guarantee further performance improvement of IC chip. In these circumstances, one has begun to find structural and material innovations to enhance gate controllability and achieve high on/off ratio. As a result, strained Si, high-κ/metal gate, and FinFET technology [4] is developed to overcome the limitation of complementary-metal-oxide-semiconductor (CMOS) device scaling. Eventually, device scaling has been continuously maintained by the 2010's, as shown in Figure 1.1.

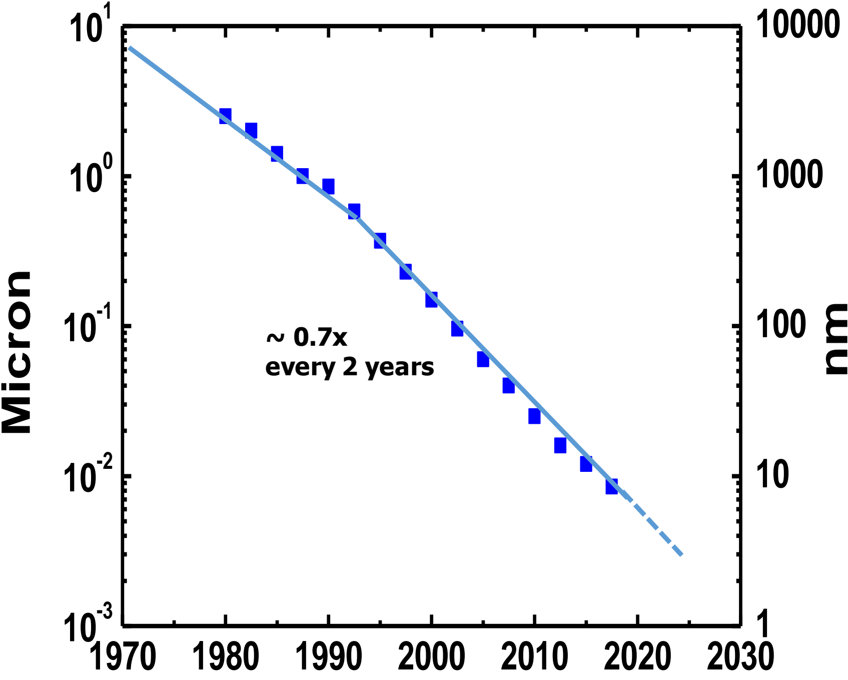


Figure 1.1. CMOS device scaling trends are lasted by using various technologies [4].

However, CMOS technology is facing more fundamental limitations in the 2010's, which is not solved by the previous technologies. One of the serious problems with device size scaling is that power consumption is exponentially increased in the highly-integrated IC chips [5] (Figure 1.2). To explain in detail, one should understand the concept of dynamic and static power. The amount of power dissipation in the CMOS devices can be expressed as below.

$$P = ACV_{DD}{}^{2}f + V_{DD}I_{OFF}$$

where A denotes fraction of switching and C is the total load capacitance. The first term of this expression means dynamic power and second term implies static power. In general, the density and speed of the devices inevitably increase the dynamic power density. Thus, lower V_{DD} is essential to minimize total power dissipation. According to the formula, V_{DD} scaling can be a great help to reduce both dynamic and static power. In fact, the increase in dynamic power shows some slowdown in the advanced technology node with low V_{DD}. Nonetheless, it is noteworthy that the portion of static power becomes gradually higher [5].

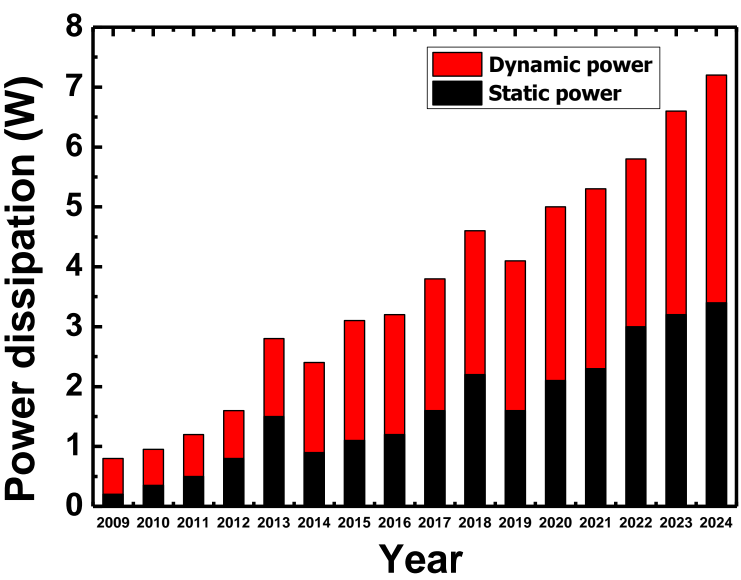


Figure 1.2. Power consumption trends according to the times [5].

Figure 1.2 also shows the ratio between static and dynamic power dissipation in the IC chip according to the times. The main reason for the abrupt increase of static power is the I_{OFF} increase as opposed to the voltage

scaling of MOSFET. As devices have been scaled down, supply voltage (V_{DD}) of CMOS devices has also been continuously decreased to reduce power dissipation. However, the fundamental problem is that voltage scaling encounters an obstacle in the nanoscale MOSFET because short channel effect (SCE) worsens the leakage current, which mainly contributes the static power [6]. In fact, V_{DD} is rarely reduced under 1.0 V, due to threshold voltage (V_t) scaling is limited at 0.2 V [7], as shown in Figure 1.3. In conventional MOSFET, V_t scaling above the allowable range (0.2 V) only increases the leakage component. To prevent leakage current, steep subthreshold swing (SS) is required to achieve higher on/off ratio (I_{ON}/I_{OFF}) (See Figure 1.4). Nevertheless, the Boltzmann limit (kT/q) originating from thermal carrier injection limits SS of MOSFET to 60 mV/dec or less. Therefore, devices with a superior switching capability beyond MOSFETs are necessary for stable driving voltage scaling in the future technology nodes.

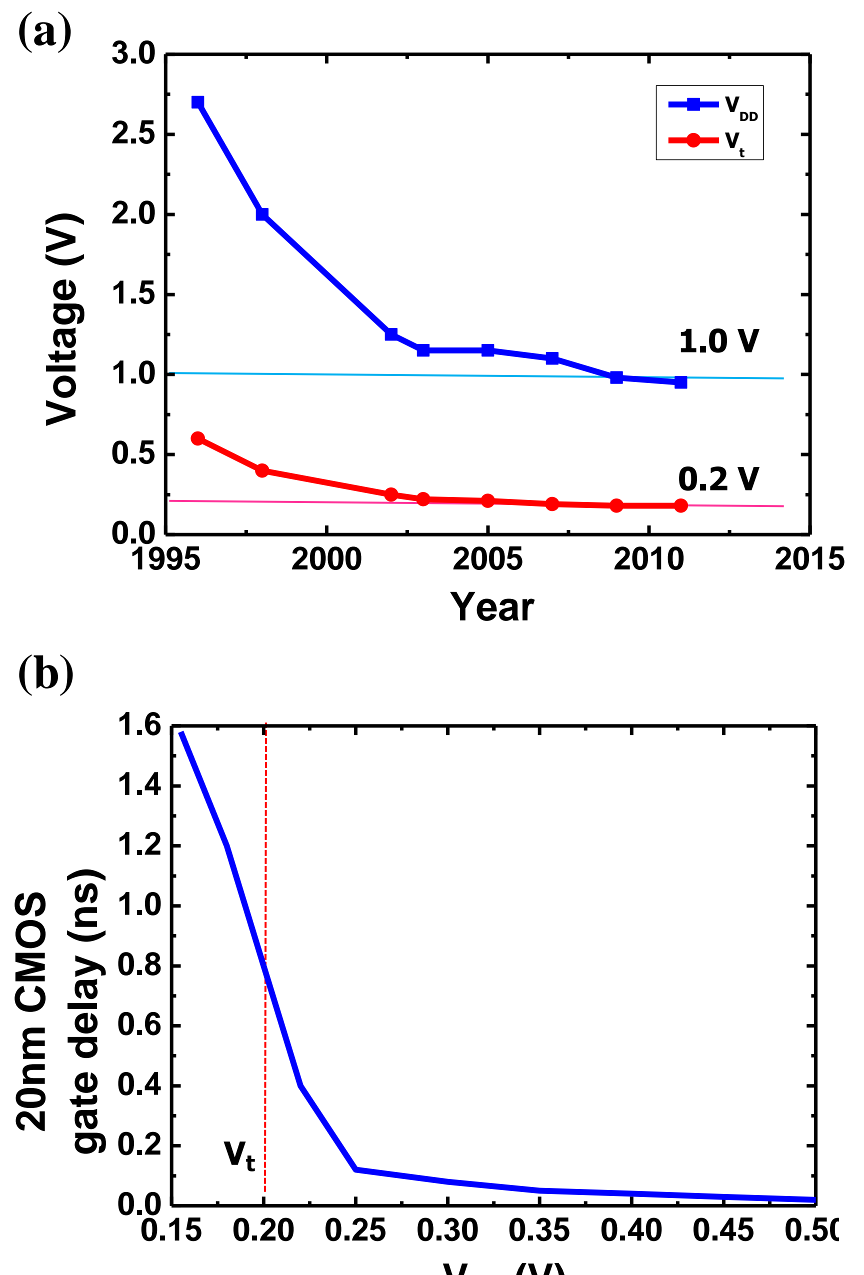


Figure 1.3. (a) Scaling trends of supply voltage (V_{DD}) and threshold voltage (V_t) of CMOS devices. (b) Relation between V_{DD} and gate delay [7].

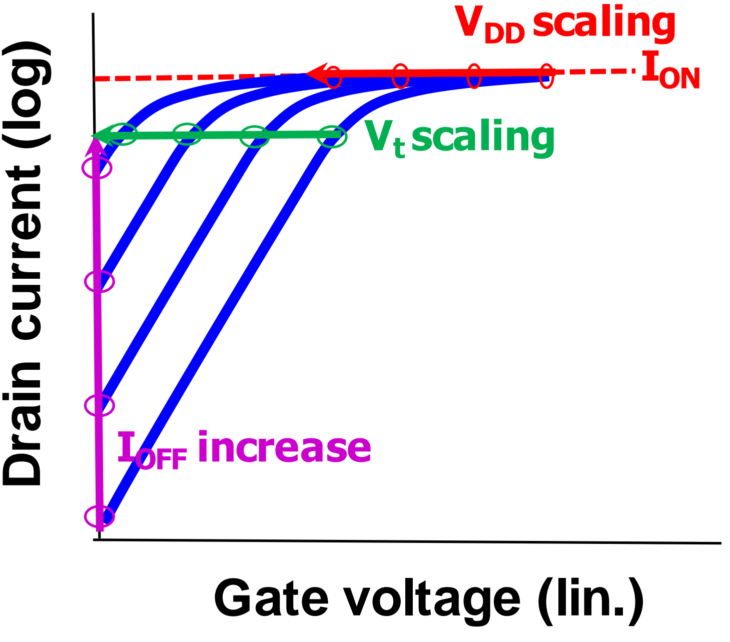


Figure 1.4. Increased I_{OFF} caused by voltage scaling of MOSFET.

1.2. Tunnel Field-Effect Transistor (TFET)

For ultralow voltage operation, a new type of steep-switching device has been researched, such as tunnel FET [8, 9], ferroelectric FET [10], and feedback FET [11]. Among these alternate switching devices, TFET is intensively studied as a promising candidate due to its CMOS-compatible fabrication process and superior SS below 60 mV/dec. TFET utilizes band-to-band tunneling (BTBT) to inject carrier into channel, which enables to overcome Boltzmann limit caused by thermal carrier injection and reduces off-current (I_{OFF}) caused by SCE. Figure 1.5. indicates the basic structure of TFET. The doping junction is quite similar to conventional MOSFET. In n-type devices, p-i-n doping junction is formed as source-channel-drain,

respectively. On the contrary, source and drain are doped with n- and p-type in pTFETs. Figure 1.6 explains the current flowing mechanism of TFET. At the off state ($V_{GS} = V_{DS} = 0$), carrier injection from source is blocked by thick energy barrier. When the gate bias is applied, the energy band at the channel region moves down. As a result, the energy barrier becomes thinner, which enables carriers (electrons or holes) to tunnel source to channel. The representative advantages of TFET are remarkable low I_{OFF} and steep SS, because carrier injection is effectively controlled at the OFF state and BTBT occurs abruptly in the applied electric field. Figure 1.7. summarizes the remarkable switching capability of TFET. The transfer curve of TFET is more similar to ideal switch and drive voltage is more easily scaled.

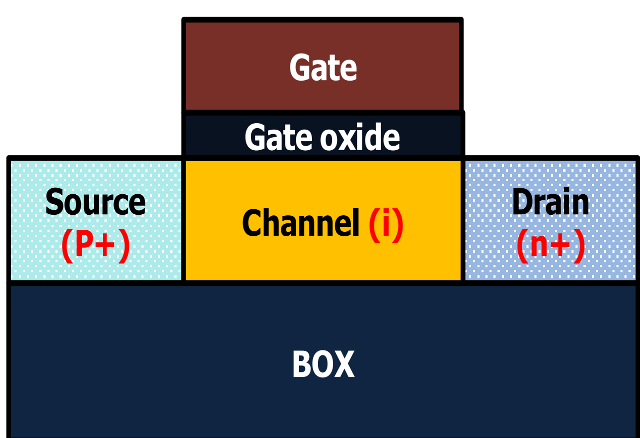


Figure 1.5. Basic structure of n-type TFET.

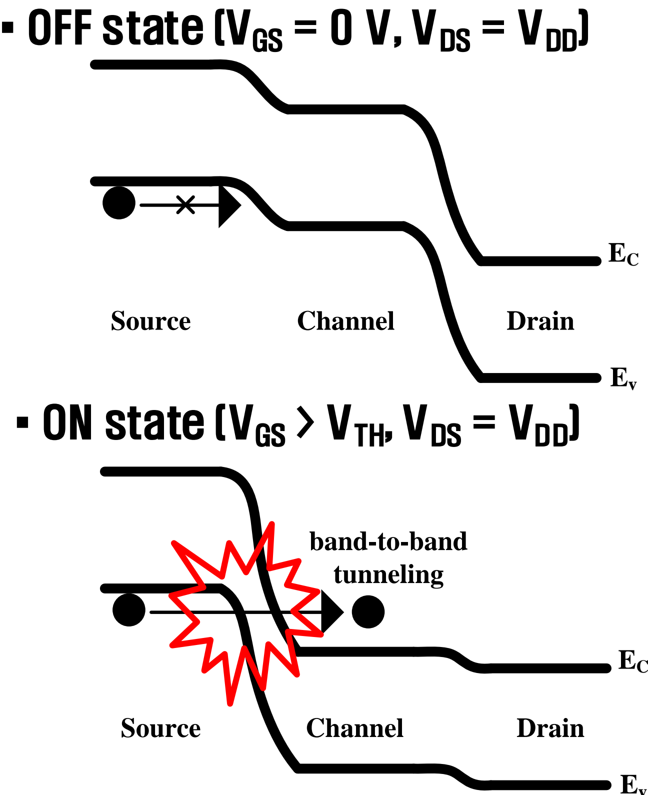


Figure 1.6. Schematic diagram of operation mechanism of TFET.

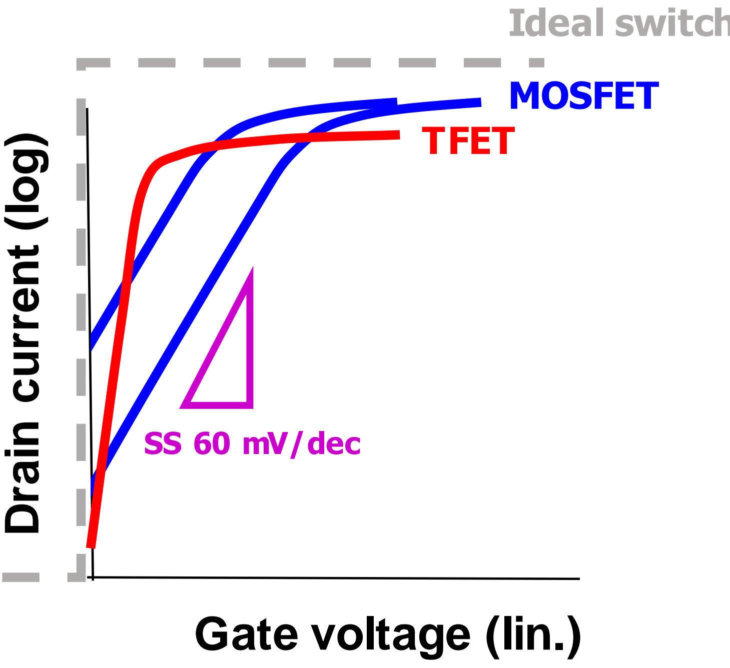


Figure 1.7. Switching characteristic of TFET compared to MOSFET.

1.3. Feasibility and Challenges of TFET

After notable reports dealing with TFETs [12-14] in mid-2000's, TFET have been intensively studied for its feasibility and performance optimization. In consequence, the common major issues for TFET are summarized as follow. 1) low I_{ON} 2) unintended ambipolar current 3) poor AC performance. On problem 2) and 3), there have been several attempts and they had some degree of effectiveness: symmetricity between source and drain [15] or drain doping modulation [16]. Nevertheless, the most serious problem is low I_{ON} (problem 1). Basically, BTBT mechanism of TFET leads to low I_{ON} due to large tunnel resistance in source/channel junction. As Si has relatively large bandgap (1.12 eV at 300K), previously reported Si-based TFET have had poor current

drivability. To reduce large tunnel resistance, narrow bandgap and direct BTBT materials including III-V [17-19] and Ge [20, 21] have been researched for the future channel material of TFET. However, their difficulty for fabrication and CMOS incompatibility are a large obstacle to apply to conventional CMOS technology. Furthermore, abrupt doping junction between source and channel in which electric field can be enhanced have been actively researched to boost BTBT [22]. If the chronic low I_{ON} of TFET is overcome, it is eventually expected that the performance of TFET is going to be surpass that of MOSFET under 0.5V V_{DD} [23] (see Figure 1.9.).

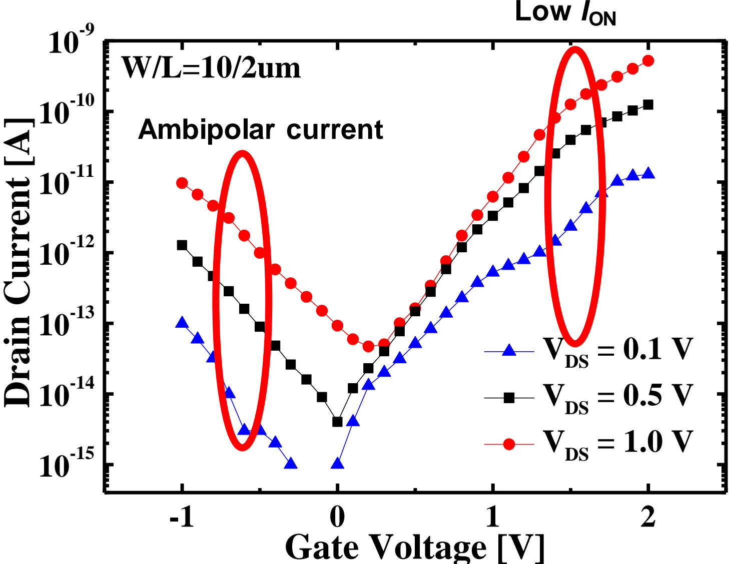


Figure 1.8. Major issues of TFET found in transfer curves.

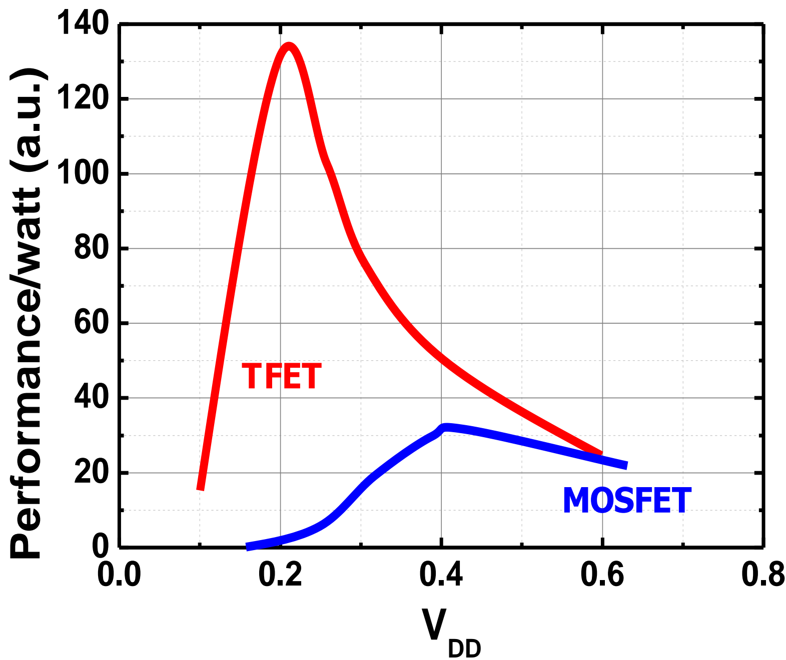


Figure 1.9. Performance per power according to supply voltage. The performances of TFET and MOSFET are compared. [23]

1.4. Scope of Thesis

This thesis focuses on the design and fabrication of TFET with high current drivability, steep SS, and excellent CMOS compatibility. Among the approaches dealt in the previous section, channel material with narrow bandgap, enhanced gate controllability, and doping junction optimization are utilized. First, in Chapter 2, the strategies of improve TFET performance are proposed. After that, the structural and narrow bandgap effects of SiGe channel are investigated. The performance improvement with enhanced gate controllability is also confirmed. To give the TCAD simulations results credibility, the measurement data is compared with TCAD simulation data

and the model parameters are extracted. After that, the fabrication process flow is presented. In specific, the three key processes to achieve the concept of the proposed TFET are introduced and its optimization process is explained in Chapter 3. The measurement results are presented in Chapter 4. The basic characteristics for CMOS devices are estimated. The superiority of device performance is also demonstrated with various experiments. Comparison with ITRS benchmark, previously fabricated TFET, and co-fabricated MOSFET is going to be helpful to verify the feasibility of proposed TFET. Furthermore, simple inverter characteristics are investigated for AC performance. Lastly, the additional optimization options to complement the problems of current devices are discussed.

Chapter 2

Device Characterization

In Chapter 2, the designing process of SiGe nanosheet TFET is mainly addressed. The basic structure and features of SiGe nanosheet TFET are initially discussed. Second, the strategy and propose of the device for the performance improvement of TFETs are explained by each device concept. Through calibrated TCAD simulation, the advantages of proposed device are confirmed by the physical analysis.

2.1. SiGe Nanosheet TFET

The device structure of the proposed SiGe nanosheet TFET is shown in Figure. 2.1. On the silicon-on-insulator (SOI) substrate, active region consists of source/drain with Si/SiGe layers and two SiGe nanosheets (NSs) are vertically stacked. The pattern is generally considered as nanosheet when the width is far larger than the thickness. The number of stacks can be further increased. The Ge ratio of SiGe nanosheets is designed to be higher than that of SiGe source/drain. The maximum Ge fraction in the SiGe channel is up to 0.8, while Ge ratio is 0.3 at the SiGe source and drain, respectively. Figure 2.2(a) shows the cross-section along the gate direction. Each nanosheet is surrounded by high-κ/metal gate, which allows gate-all-around (GAA) structure. is The cross-section along the channel direction is presented in

Figure 2.2(b). In order to form TFET doping junction, source and drain are inversely doped.

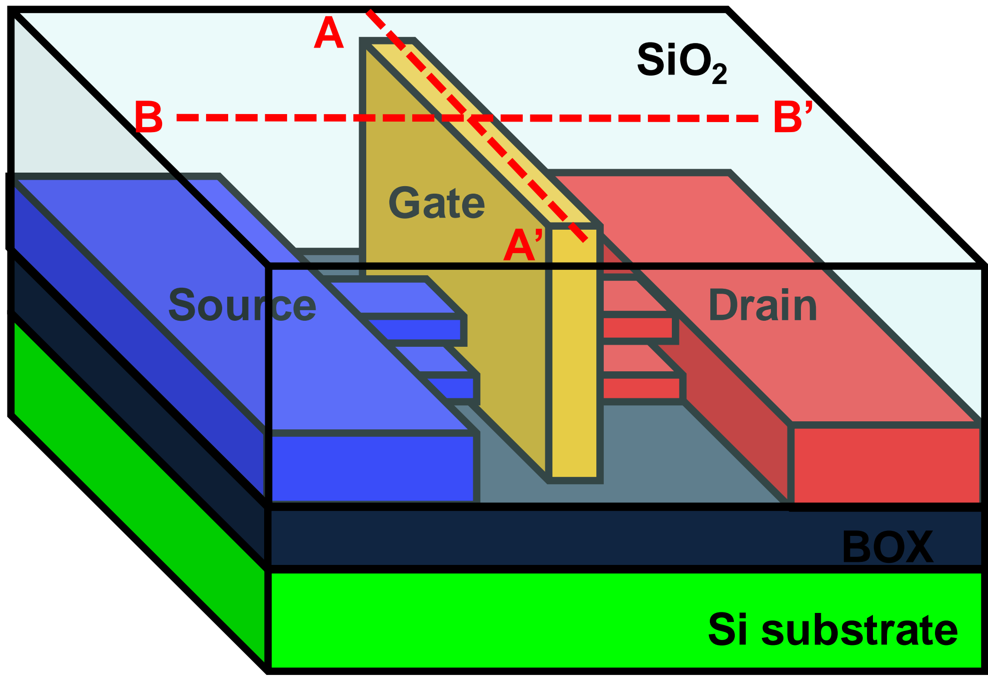


Figure 2.1. Schematic diagram of proposed SiGe nanosheet TFET.

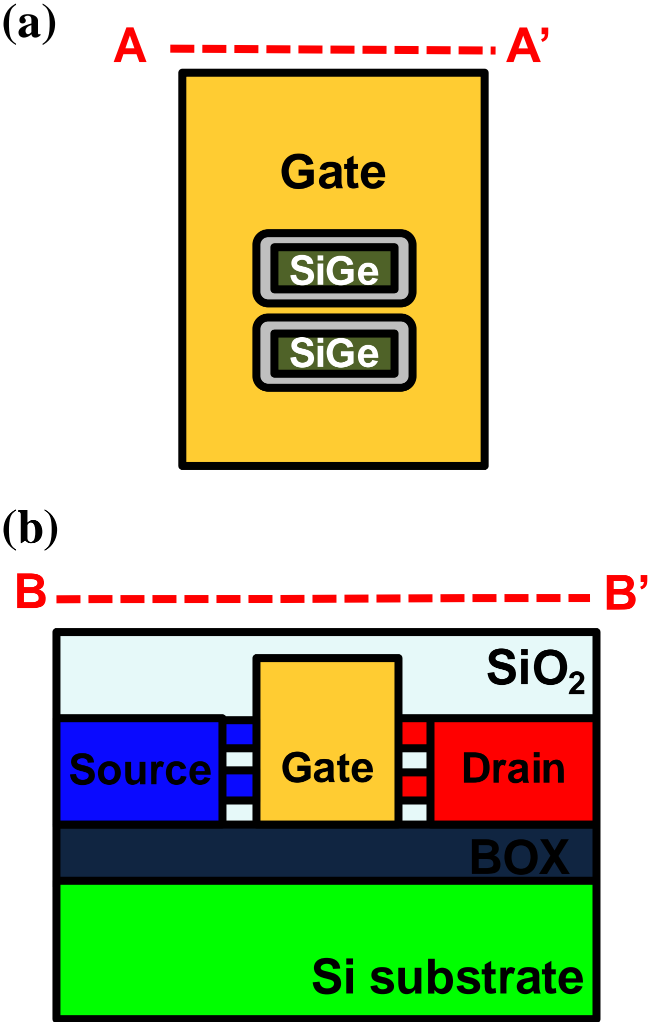


Figure 2.2. Cross-sectional view of (a) along the gate and (b) the channel direction of SiGe nanosheet TFET.

2.2. Device Concept

The objective of proposed SiGe nanosheet TFET summarizes as four parts. 1) high I_{ON} 2) steep SS, 3) low I_{OFF}, and 4) CMOS compatibility. For objective 1) and 2), BTBT should be maximized. There are three representative things to amplify BTBT: narrow bandgap for thinning

tunneling barrier, high electric field between source and channel, and maximizing tunneling area. In this dissertation, SiGe channel is used for thinning tunneling barrier. In addition to SiGe layer deposition, the additional technique to raise Ge ratio, Ge condensation is utilized. High Ge ratio in SiGe channel enables to narrow bandgap and increase the amount of direct BTBT [24]. For the stronger electric field between source and channel, doping junction optimization and superior gate control should be fulfilled. Nanosheet channel presents GAA structure, in which electric field is concentrated on the thin channel. Moreover, the effective channel width can be increased in nanosheet channel within the same feature size. Consequently, tunnel injection and current flow can be maximized in the nanosheet channel. Additionally, high-κ/metal gate with low equivalent oxide thickness (EOT) is applied to strengthen gate control.

To reduce I_{OFF}, it is important to minimize other current flowing mechanism which is irrelevant to BTBT, such as Shockley-Read-Hall (SRH) recombination and trap-assisted-tunneling (TAT) [25]. Good interface quality is required between source and channel (bulk trap) or channel and gate oxide (interface trap), respectively. In proposed TFET, the interface trap density (D_{it}) of gate oxide is closely estimated and the most optimal gate formation condition is selected. Moreover, ambipolar current from drain to channel needs to be suppressed. The drain region is underlapped with gate in order to attenuate electric field between drain and channel. Besides, surface-rich Ge profile [26] in SiGe channel also helps to prevent junction leakage caused by

narrow bandgap in the channel.

Lastly, CMOS compatibility is considered as much as possible in the design of the fabrication process. As SiGe channel is widely accounted to suit both MOSFET and TFET due to high hole mobility, narrow bandgap, and CMOS-compatibility [27], MOSFET and TFET are co-fabricated in the same process. The intrinsic advantage of TFET, which has similar fabrication procedure to that of MOSFET, is constructively utilized.

2.3. Calibration Procedure for TCAD Simulation

Before the investigation of device concept using TCAD simulation, Simulation setup should be preceded to get reliable simulation data. First of all, the core model parameters are extracted from the experimental data of fabricated planar SiGe TFET. Figure 2.3. displays the fabricated planar $Si_{0.2}Ge_{0.8}$ TFET using SOI substrate. The planar TFET is fabricated with the main SiGe nanosheet TFET in the almost same dimension and implant condition (The detailed fabrication process is going to be described in Chapter 3). The gate length and channel width is 1 μm, respectively. The SiGe channel is thinned to 25 nm. EOT is estimated about 2.1 nm and the thickness of TiN gate is 180 nm. As it is a pTFET device, source is doped with arsenic, whereas drain is doped with boron, respectively. Implant dose of each source and drain is 3×10^{15} cm^{-2}.

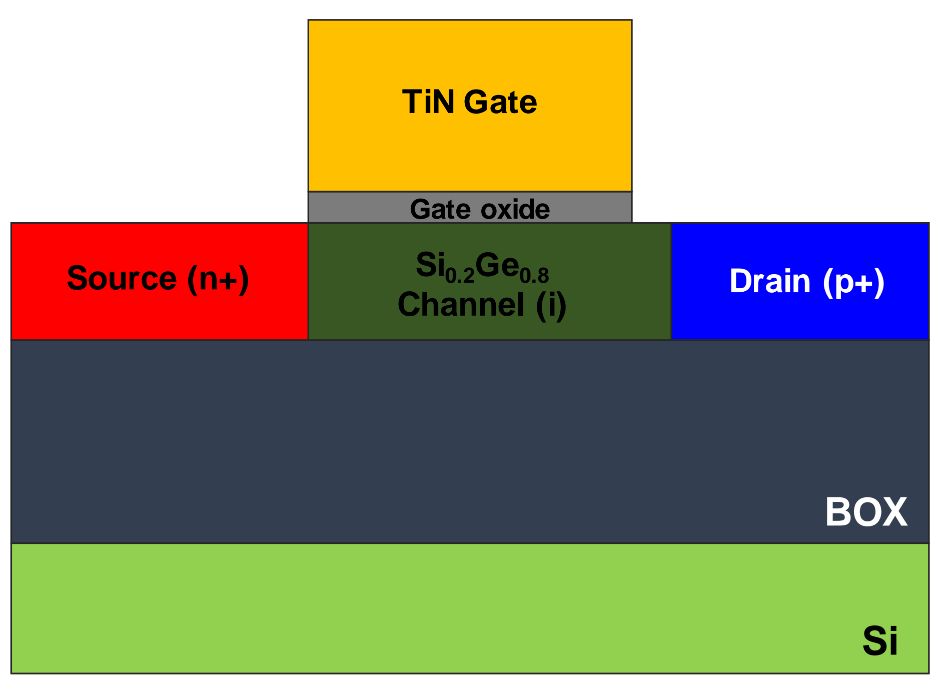


Figure 2.3. Schematic diagram of fabricated p-type $Si_{0.2}Ge_{0.8}$ TFET used in the calibration process.

To fit the measurement data of planar TFET and TCAD simulation data of the same device structure, one should know accurate tunneling coefficients in Kane's model [28, 29]. The nonlocal Kane's model is the most popular model to describe BTBT generation because it automatically reflects the contribution of the direct and indirect tunneling well [30]. The formula of BTBT generation rate in a given electric field is represented as below:

$$G = A(\frac{F}{F_0})^P \exp(-\frac{B}{F})$$

Where F_0 = 1 V/cm, P = 2 for the direct tunneling process, and P = 2.5 for the indirect tunneling process. A and B are the fitting coefficients of nonlocal BTBT model. In general, Si and Ge has each intrinsic value for A

and B for direct and indirect tunneling, respectively. As Ge has narrower bandgap and higher direct and indirect tunneling rate, the values of Ge is bigger than those of Si. The A and B of $Si_{1-x}Ge_x$ channel is determined between the values of Si and those of Ge, in proportion to mole fraction ratio x. Since BTBT dominates the current flowing mechanism of TFET, it is most important to obtain the accurate values A and B for the exact simulation of drain current. In $Si_{1-x}Ge_x$ channel, indirect BTBT mainly contributes to carrier injection when Ge ratio (x) is under 0.8. Thus, the values of A_{ind} and B_{ind} are important. On the other hand, when Ge ratio is over 0.8, the amount of direct BTBT becomes almost similar to that of indirect BTBT [24]. Thus, A_{dir} and B_{dir} should be included in the BTBT simulation.

Figure 2.4. indicates the simulated structure for $Si_{0.2}Ge_{0.8}$ planar TFET. All the dimension parameters used in the simulation are same as the fabricated $Si_{0.2}Ge_{0.8}$ TFET. Simulation is performed by the Sentaurus™ simulator (Ver. 2015. 06) of Synopsys Inc [31]. Non-local BTBT, drift-diffusion carrier transport, band-gap narrowing and Shockley-Read-Hall (SRH) recombination models are used. Gate leakage or interface trap density are ignored in this simulation. Tunnel parameters are modulated referring the previous reports [24, 32] for the values of Si and Ge. Figure 2.5. shows the fitting result between the fabricated and simulated TFETs. It is easily confirmed that the I_{ON} and SS are fitted well in both the linear and log scale. The final extracted tunneling coefficients for Si and Ge are in Table. 2.1.

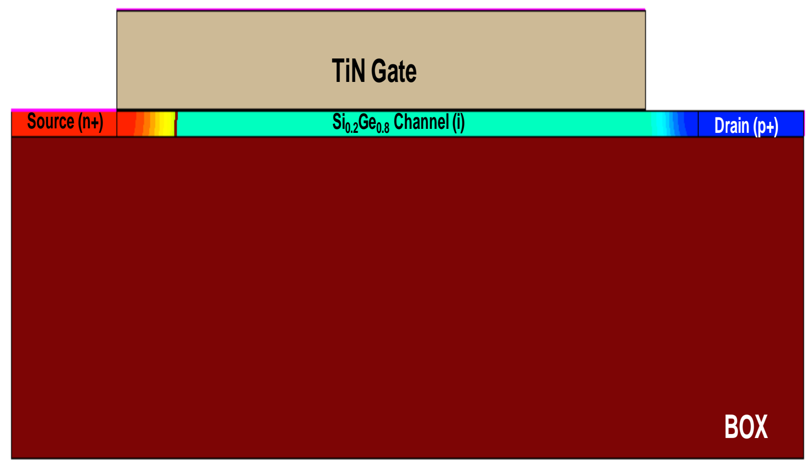


Figure 2.4. Simulated structure of $Si_{0.2}Ge_{0.8}$ planar TFET used in the TCAD simulation.

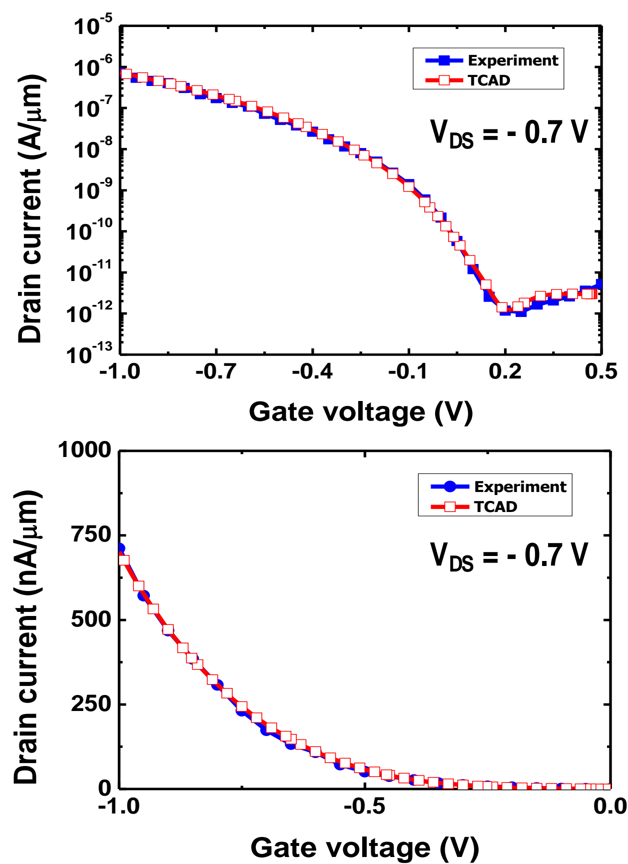


Figure 2.5. Result of calibrated TCAD simulation with the experimental data.

Parameters		
F_0		1 V/m
P		2 for direct BTBT, 2.5 for indirect BTBT
Si	A_{ind}	1.00×10^{15} $cm^{-1}\cdot S^{-1}$
	B_{ind}	21.0 MV/cm
Ge	A_{ind}	1.70×10^{15} $cm^{-1}\cdot S^{-1}$
	B_{ind}	6.20 MV/cm
	A_{dir}	1.46×10^{20} $cm^{-1}\cdot S^{-1}$
	B_{dir}	6.04 MV/cm

Table 2.1. Calibrated BTBT parameters of Si and Ge.

2.4. Device Verification with TCAD Simulation

The three-dimensional simulated structure for SiGe nanosheet TFET is exhibited as shown in Figure. 2.6. The overall shape is quite similar to Figure. 2.1. The height of source and drain is 110 nm. In the nanosheet part, the space between SiGe layers is 30 nm, which is filled with high-κ/metal gate. The width of each nanosheets is defined from 40 nm to 300 nm. P-i-n or n-i-p doping junction is formed for n or p TFETs. The detailed simulation condition is organized in Table. 2.2. Ge concentration is varied from 0.3 to 0.8 to reflect Ge condensation effect. The cross-sectional views along the gate and channel

are also presented.

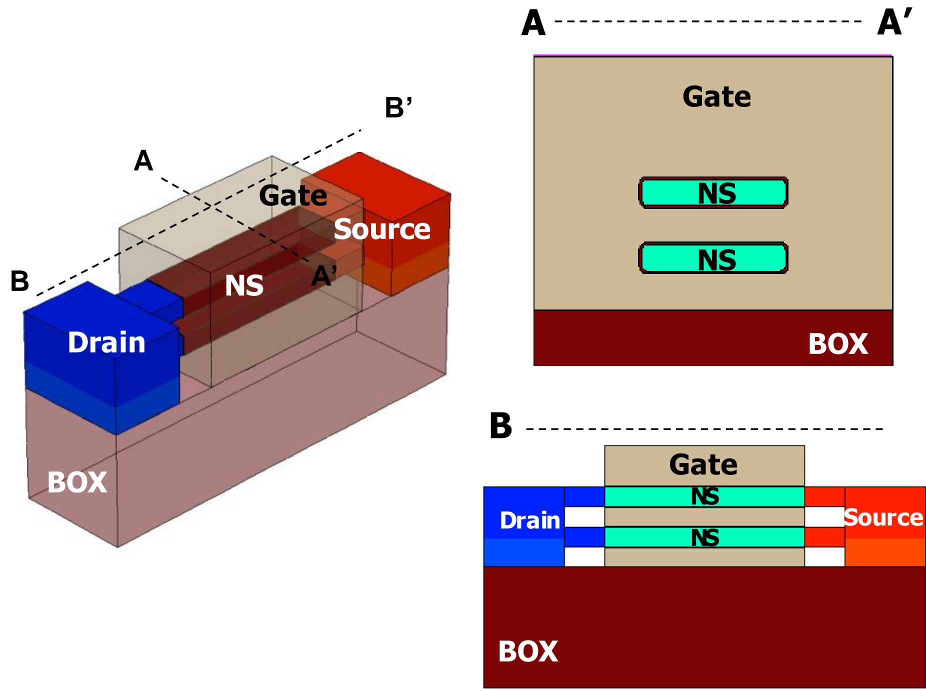


Figure 2.6. Simulated structure of the proposed SiGe nanosheet TFET.

Simulation Parameters	
Channel length	100 ~ 500 nm
NS width/height	40 ~ 200 nm
Source/drain height	120 nm
Space between NSs	40 nm
Gate underlap	100 nm
Equivalent oxide thickness	2.1 nm
BOX thickness	300 nm
Source doping	Arsenic 3×20 cm^{-3}
Drain doping	Boron 2×20 cm^{-3}
Channel doping	Boron 1×15 cm^{-3}

Table 2.2. Parameters used in the TCAD simulation of SiGe nanosheet TFET.

In this simulation, the effects of channel structure are analyzed first. Figure 2.7. shows transfer curves of the simulated SiGe TFETs. Drain voltage (V_D) is -0.7 V. The performances of FinFET and single-nanosheet GAA TFET with the same mask layout and same Ge fraction ratio are compared with the proposed TFET nanosheet structure. As a result, both I_{ON} and SS are improved in nanosheet structure. This result can be explained by the fact that the effective channel width and gate controllability becomes larger in the stacked-nanosheet channel. The enhanced gate controllability enables energy bands at the entire area of the channel are bent more sharply and tunneling barrier is thinner in the GAA structure. Thus, the amount of BTBT generation is higher and the activated area with the holes is wider in nanosheet channel, as shown

in Figure. 2.8.

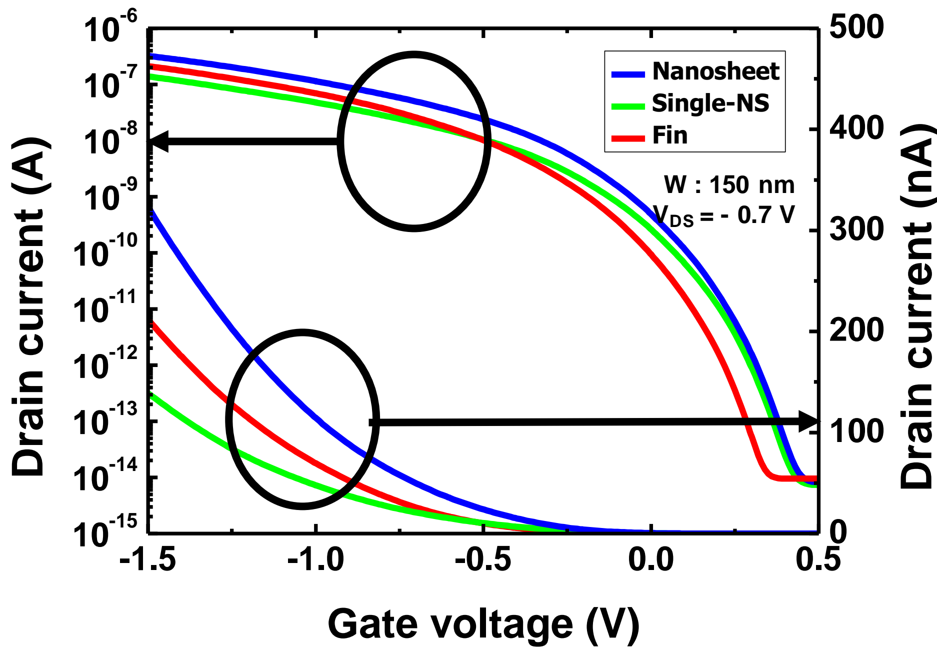


Figure 2.7. Simulated transfer curves of SiGe two-nanosheets, single-nanosheet, and Fin channel TFET.

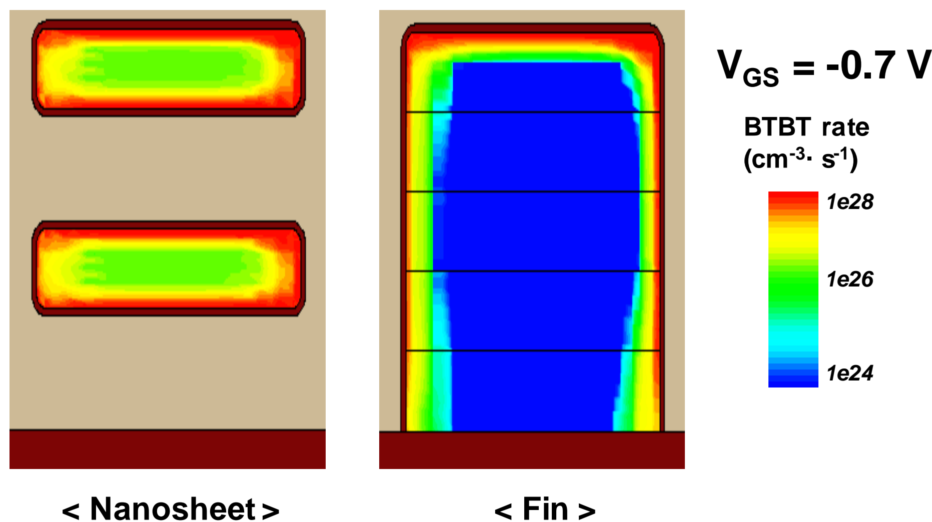


Figure 2.8. BTBT rate at the cross-section of SiGe channel TFET.

Furthermore, Ge condensation process [33, 34] on SiGe channel can mainly boost the performance of SiGe nanosheet TFET. Ge condensation process is a technique originated from thermal oxidation, which enables to raise Ge content in the SiGe nanosheet (see Figure 2.9.). The detailed procedure of Ge condensation will be discussed in Chapter 3. As a consequence of Ge condensation, three changes take place to SiGe nanosheet. 1) Ge ratio on the surface of nanosheet increases, 2) the size of nanosheet becomes smaller as Si in the SiGe nanosheet is consumed, and 3) diffused Ge atoms are gradually distributed from the surface. Figure 2.10. displays the impact of Ge ratio (x) in the $Si_{1-x}Ge_x$ channel. As Ge component becomes higher, the bandgap of SiGe is narrower as Ge has a smaller bandgap than Si. Due to narrower bandgap of SiGe with higher Ge content, BTBT increases in $Si_{0.2}Ge_{0.8}$ channel compared to $Si_{0.7}Ge_{0.3}$, $Si_{0.6}Ge_{0.4}$, and $Si_{0.4}Ge_{0.6}$ channel. However, I_{OFF} also increases in the SiGe channel with higher Ge content due to increased leakage component by narrow bandgap. Channel size shrink during condensation also helps to reduce SS and I_{OFF}. Reduced channel size, especially thin body helps to improve gate controllability in the GAA structure [35]. Therefore, increase in I_{OFF} can be prevented because tunneling is well controlled by enhanced electric field in the smaller nanosheet.

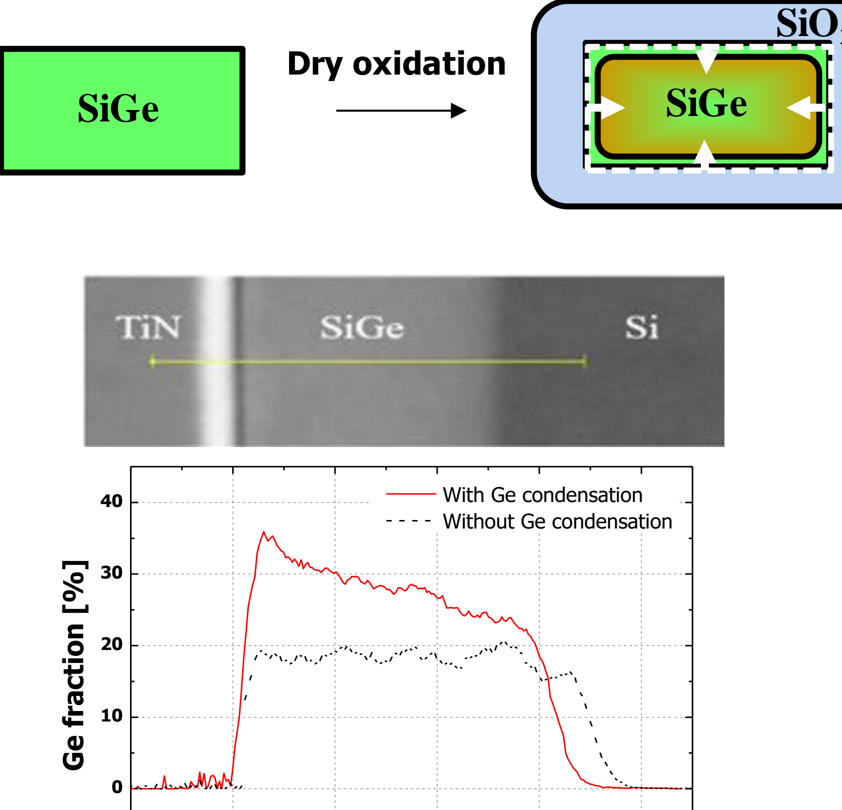


Figure 2.9. Schematic diagram of Ge condensation process on SiGe nanosheet and the raised Ge ratio of SiGe channel during Ge condensation [26].

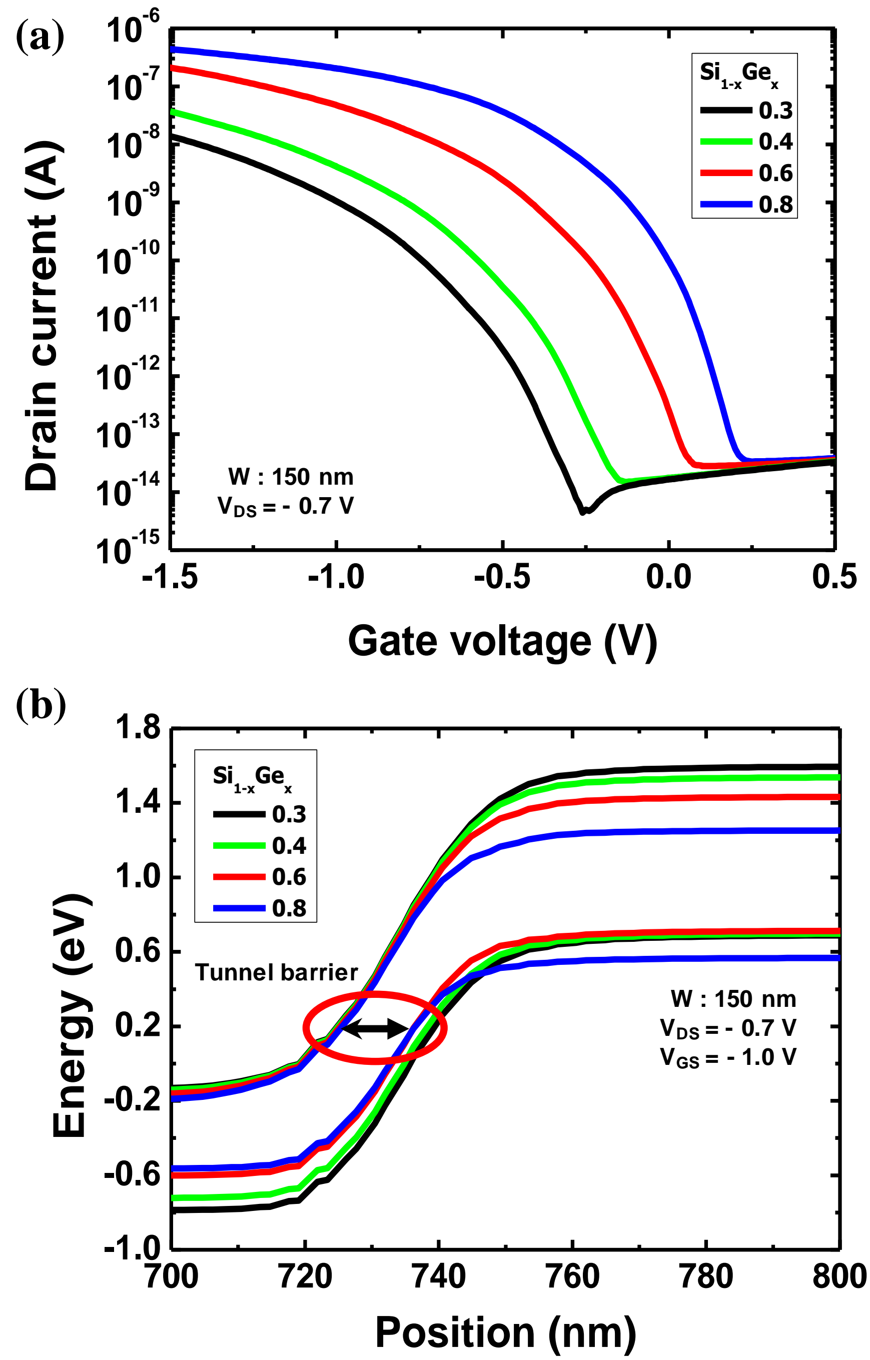


Figure 2.10. (a) Transfer curves and (b) energy band diagrams according to Ge ratio (x) in the $Si_{1-x}Ge_x$ channel

Meanwhile, one can wonder that how far Ge condensation process should be done. Even though the size shrink has the advantage of gate control, oxidation under too high temperature and too long time reduces the size of nanosheet excessively and the advantages of condensed SiGe (large BTBT current due to narrow bandgap) will disappear. Thus, size shrink should be minimized to prevent reducing the effective channel width. When the minimal oxidation proceeds for the Ge condensation, gradual Ge profile is formed, as shown in Figure 2.11. Due to optimized Ge condensation, the Ge fraction at the surface is 0.8 and Ge ratio at the center is 0.3, respectively. The detailed setup procedure of oxidation condition is discussed in Chapter 3. To find out the influence of Ge profile, the simulated gradual Ge profile is fitted with experimental result. The transfer characteristics of SiGe TFET with the constantly distributed Ge profile and the gradual Ge profile are compared. As a consequence, Figure 2.12. indicates the current drivability of each device does not have a big difference. Accordingly, it is proven that the Ge content at the channel surface is most important. Figure 2.13. summarizes the impact of Ge condensation. It is shown that I_{ON} increases remaining I_{ON}/I_{OFF} ratio in the condensed SiGe channel under the optimized process condition [36].

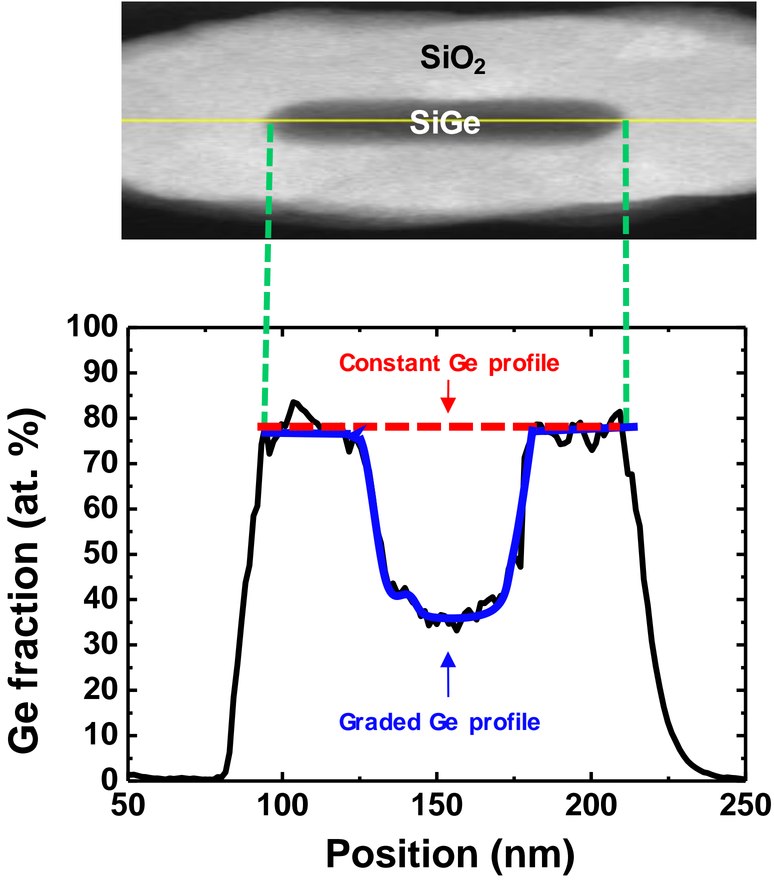


Figure 2.11. Obtained Ge profile from the Ge condensation process and the constant and gradual Ge profile used in the simulation.

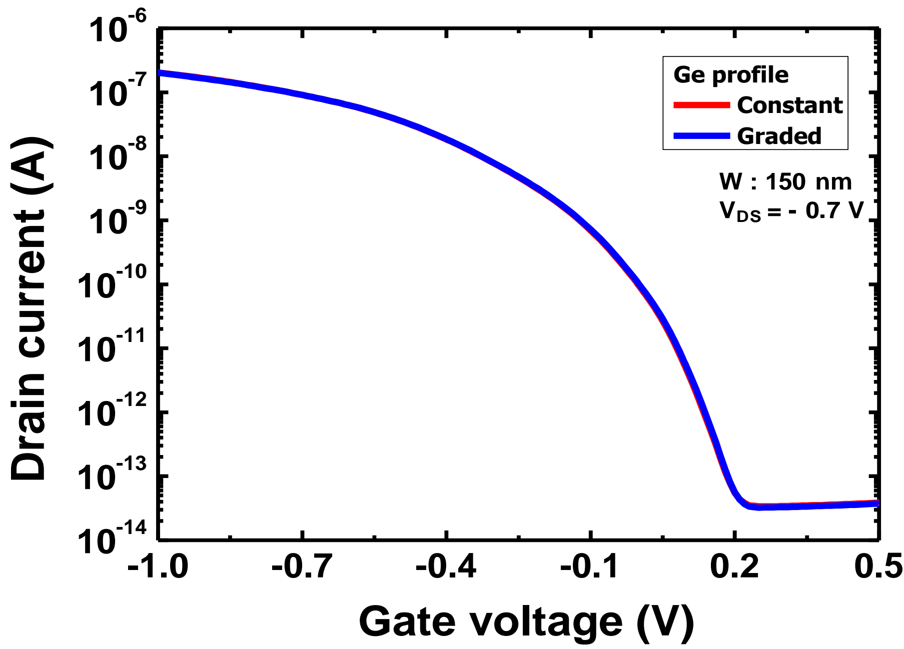


Figure 2.12. Transfer curves of the SiGe TFET according to the various Ge profile

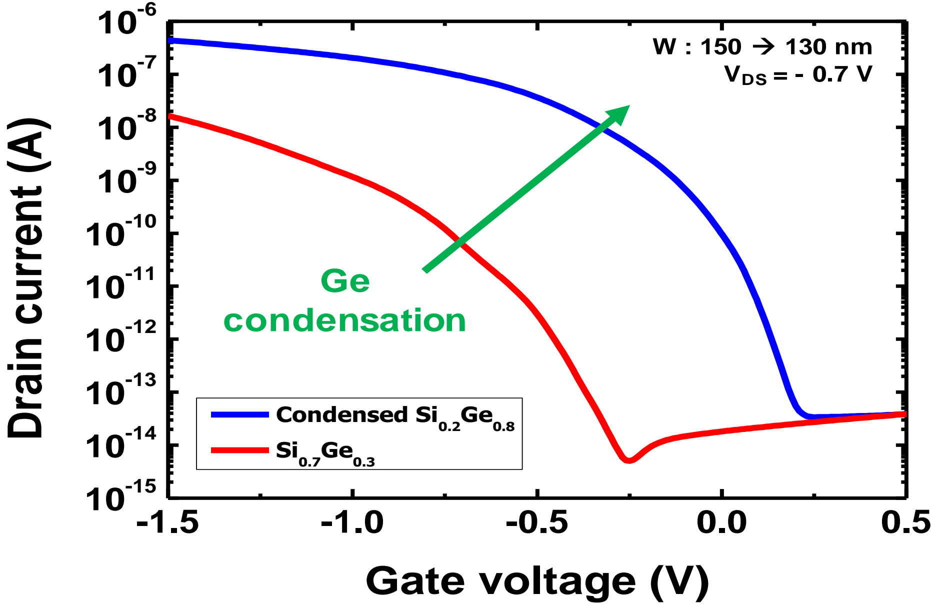


Figure 2.13. Comprehensive effect of Ge condensation process confirmed by the transfer curves of SiGe nanosheet TFET.

Chapter 3

Device Fabrication

In this chapter, the device fabrication procedure of SiGe nanosheet TFET is covered in detail. The whole fabrication process is briefly presented earlier. The detailed explanation and the setup processes are described based on the key processes.

3.1. Fabrication Process Flow

The entire fabrication process flow for SiGe nanosheet TFET is proposed in Figure 3.1. Nanosheet MOSFET is also co-fabricated with TFET. The fabrication starts with the preparation of 100-nm SOI wafer. First, top silicon layer is thinned to 30 nm by wet oxidation [37]. During the thermal oxidation, Si layer is consumed to 45% of the entire SiO_2 layer. Then. SiGe, Si, and SiGe layer are alternatively deposited by epitaxial growth. The layer thickness of each layer is 30 nm. After that, active region is defined by electron beam lithography (e-beam) mix-and-match process with conventional photolithography. At this moment, channel implant is performed on the MOSFET channel with boron and phosphorus. To form fin pattern, Si/SiGe layer is etched by anisotropic Si inductively coupled plasma (ICP) dry etch. Next step is SiGe nanosheet formation. Following 100:1 HF dip in 60 seconds, Si sacrificial layers are selectively removed in

tetramethylammonium hydroxide (TMAH) solution. After nanosheet formation, Ge condensation process is conducted by dry oxidation for 20 minutes in 850°C oxygen atmosphere. Next, dummy gate stack consisted of poly Si and silicon nitride is formed by low-pressure chemical vapor deposition (LPCVD). The thickness of poly-Si and Si_3N_4 is 350 nm and 50 nm, respectively. Then, arsenic (3×10^{15} dose, 80 keV energy) and BF_2 (3×10^{15} dose, 60 keV energy) are implanted to source/drain region and rapid thermal annealing is carried out in 950℃, N_2 ambient for 30 seconds. Interlayer dielectric (ILD) is deposited through high-density plasma CVD (HDPCVD) and chemical-mechanical polishing (CMP) is implemented until nitride dummy gate is exposed. Gate last process [38] is adopted for the gate formation. Dummy gate is removed by wet etch using H_3PO_4, ICP Si dry etch, and CH_3COOH-based poly Si wet etch. To deposit high-κ gate stack, 9-cycles Al_2O_3 and 28-cycles HfO_2 layer are grown and 160-nm TiN gate is deposited by atomic layer deposition (ALD) and sputter process. Finally, conventional back-end-of-line (BEOL) process is done to form metal pad.

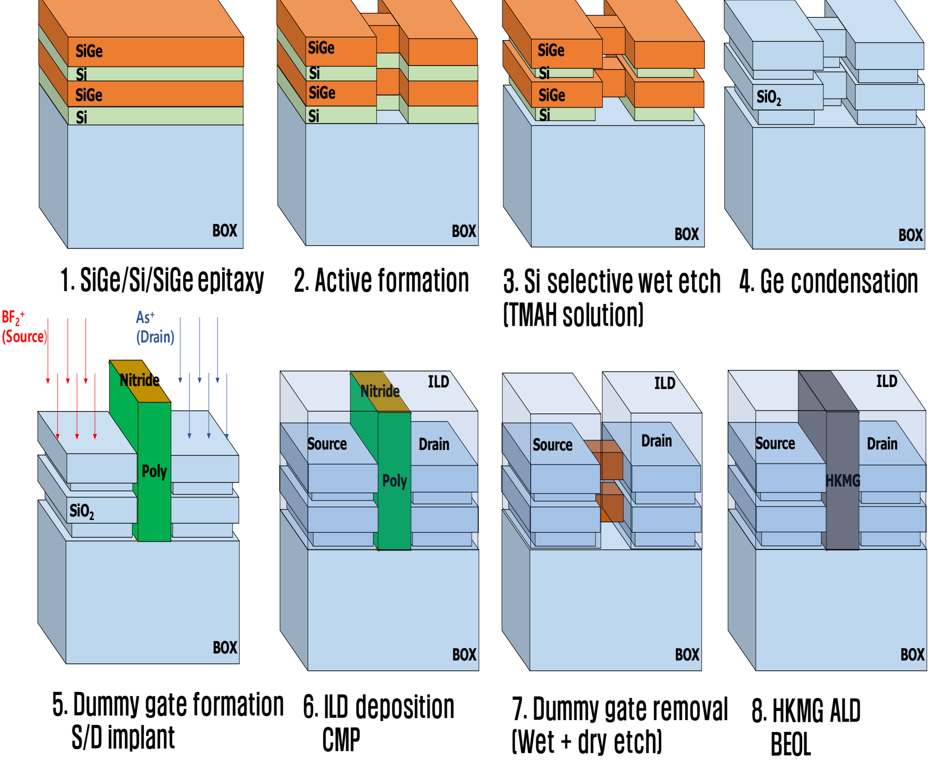


Figure 3.1. Entire fabrication process flow of SiGe nanosheet TFET.

3.2. Key processes for SiGe nanosheet TFET

For the maximization of the concept of proposed TFET, there are three key processes to implement designed structure. First, the formation of SiGe nanosheets. Nanosheet formation implies nanosheet release through Si selective wet etch and Ge condensation. Second, the implantation of source and drain for the BTBT junction formation. Last, high-κ/metal gate formation for the optimization of gate controllability, such as low EOT and D_{it}. As the proposed TFET uses gate-last process, gate formation process in this device includes from dummy gate removal to high-κ/metal gate ALD.

3.2.1. Key Process 1 : SiGe Nanosheet Formation

The most important process in this fabrication is SiGe nanosheet formation. Figure 3.2. displays the fabrication steps of SiGe nanosheet formation from the cross-sectional view of nanosheet. The first step is fin patterning consisted of Si and SiGe layers. Figure 3.3. shows the successfully formed 80-nm width fin by using e-beam lithography and ICP Si dry etch.

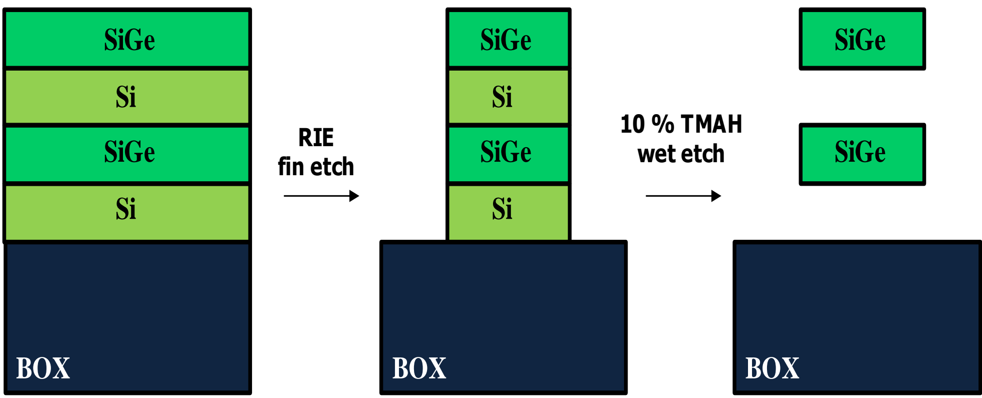


Figure 3.2. Process flow of the SiGe nanosheet release.

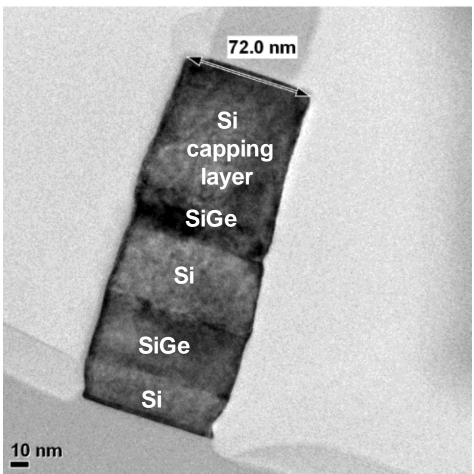


Figure 3.3. 80 nm-width formed by ICP dry etch process.

Next, the core technique is Si wet etch by dipping in TMAH solution. It is a well-known fact that TMAH solution is good etchant for Si [39]. In addition, TMAH solution has high selectivity between Si and SiGe [40]. However, anisotropic etching characteristics [41, 42] of TMAH can be a weakness in nanosheet release process, because residual Si between SiGe nanosheets could not be perfectly removed. In general, the plane direction of conventional channel is <110>. The most problematic part is the lowest etch rate at the <111> plane. At the beginning of the wet etching, <110> Si plane is etched. However, the plane direction in contact with the TMAH solution is continuously changed due to anisotropic etch. Thus, one should consider the bottleneck effect at the <111> direction. Since the anisotropy of Si etch varies with temperature and solution concentration of TMAH, it is essential to find the optimal etch condition for preventing imperfect Si etching. Referring previous report about TMAH solution [39], 10% TMAH solution is used for etch test. In 70 ℃ TMAH solution, the Si/SiGe/Si/SiGe fin pattern is dipped for 3 minutes. In Figure 3.4., it is clearly revealed that Si is etched about 65 nm from each side. In fact, the etch rate for residue Si cannot be linearly calculated because its crystal orientation is continuously changed during wet etch [43]. In the main process, the Si/SiGe fin is dipped for 5 minutes in 70 ℃, 10 % TMAH solution. Results can be confirmed in Figure 3.5. that two vertically stacked SiGe nanosheets are successfully formed. The top, side, and cross sectional views are presented. It is shown that nanosheets are bended, since stress is induced to during the nanosheet release. That problem can be

overcome at the shorter nanosheets, as presented Figure 3.6.

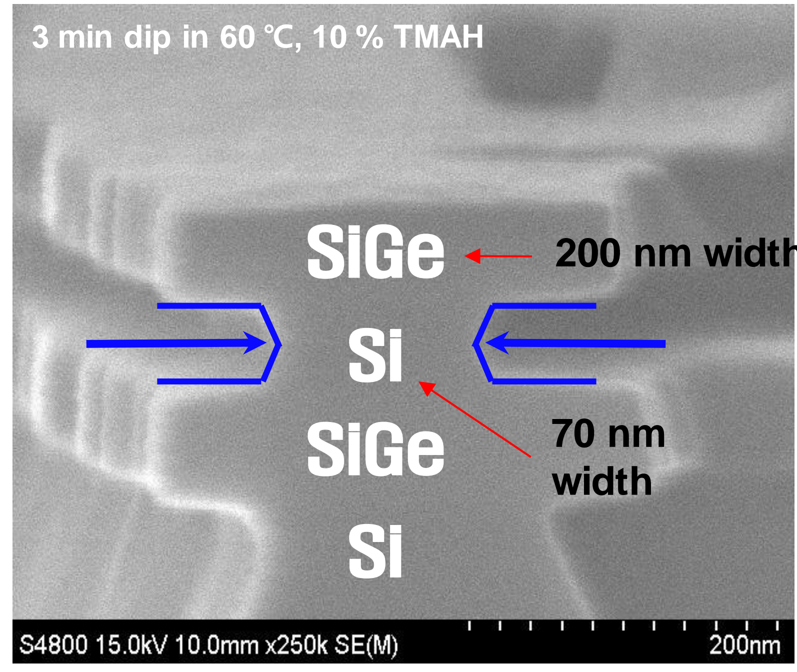
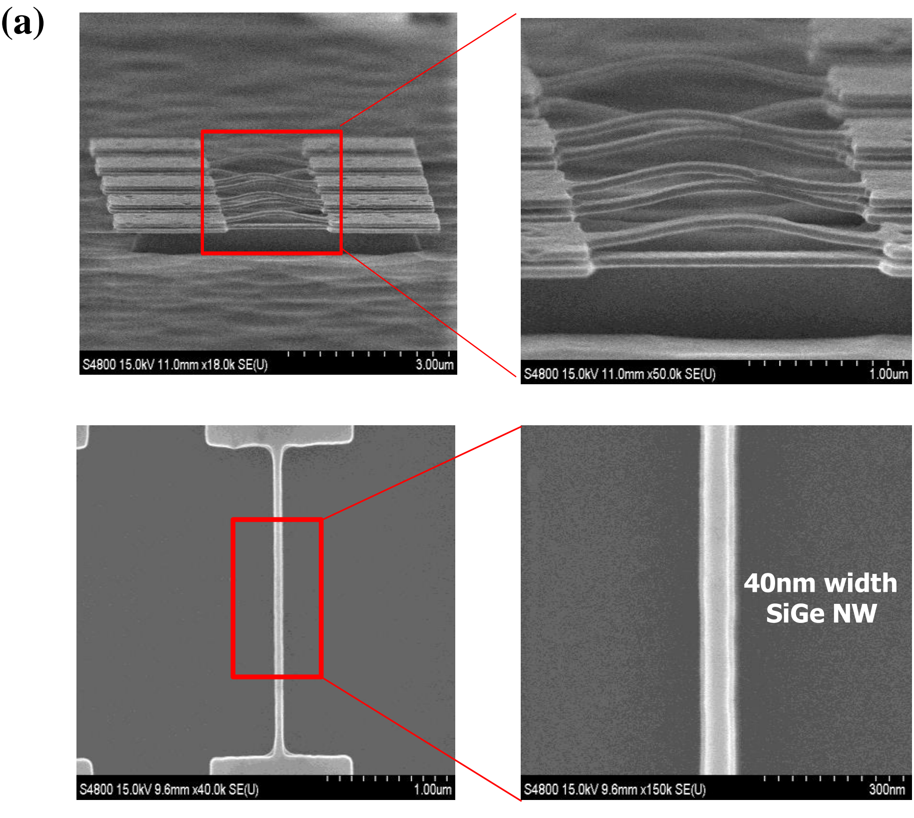


Figure 3.4. Result of <110> Si wet etch in TMAH solution.

(a)



(b)

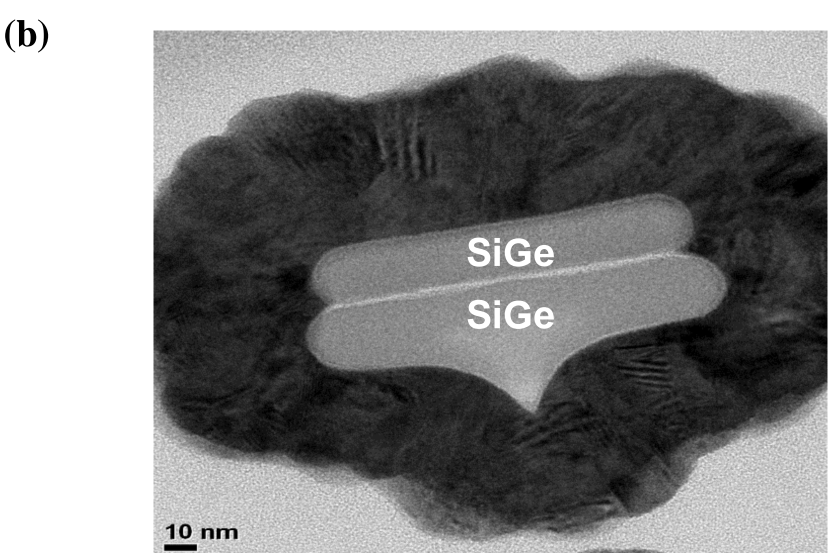


Figure 3.5. Released SiGe nanosheets using TMAH wet etch. (a) Side, Top, and (b) cross-sectional view of SiGe nanosheets

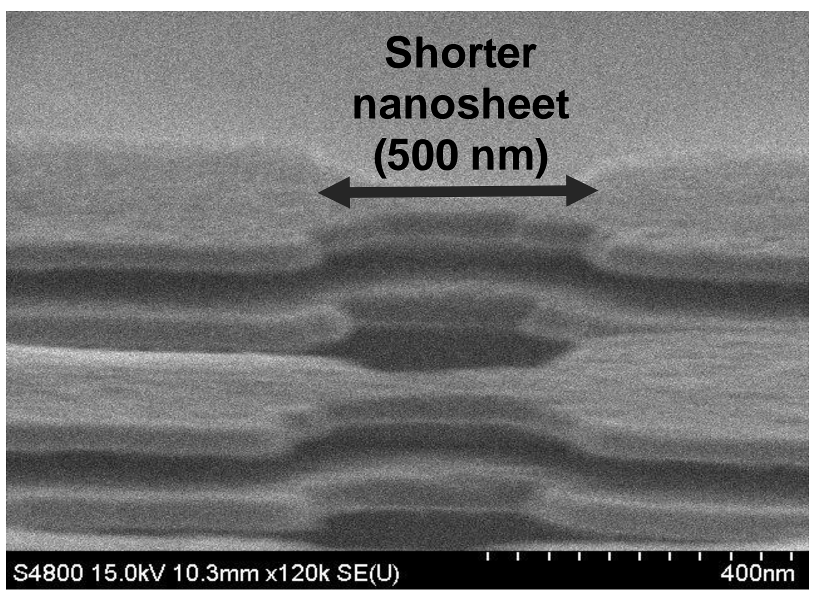


Figure 3.6. Successfully formed SiGe nanosheets with shorter length.

The second process is Ge condensation. During dry oxidation on SiGe substrate, Si atoms are oxidized and thus consumed. Whereas, Ge atoms are not oxidized as Si atoms due to activation energy difference of oxidation [44]. Ge atoms receives thermal energy from oxidation process and diffuses into bulk of the SiGe layer. As a result, the relative Ge ratio in $Si_{1-x}Ge_x$ channel increases from the surface. The adjustable variables for dry oxidation is two: oxidation temperature and time. In them, temperature has dominance due to it directly affects the thermal energy of Ge to diffuse [45]. In Chapter 2, it is verified that the desirable Ge content in SiGe channel is surface-rich gradual profile. We have to find out the optimal temperature for Ge condensation to acquire appropriate Ge profile. Accordingly, oxidation condition is examined. Temperature is splitted from 750 ℃ to 950 ℃ and oxidation is performed for 60 minutes. Figure 3.7. shows the result of temperature dependence

experiment. As temperature rises, the diffusivity increases and Ge atoms move deeper into bulk. At 750 ℃, surface-rich Ge content is achieved but the Ge ratio at the surface is not high due to low Ge diffusivity. It is necessary to raise temperature. However, at 950 ℃, Ge atoms diffuses too much into bulk and overall Ge profile has even distribution. In fact, the Ge profile closest to the desirable distribution can be found at 850 ℃. Surface-rich Ge content is attained and Ge ratio is higher at the surface compared to ratio in other temperature. Moreover, the thickness of surface-rich layer is thick enough to activate BTBT. Meanwhile, the oxidation time is decided considering the thickness of consumed Si and grown SiO_2 layer. As the thickness of grown SiGe nanosheet is about 35 nm, the total reduced thickness during condensation is set to 10 nm. In the main process, Ge condensation carried out in 850 ℃, O_2 ambient for 20 minutes and obtained gradual Ge profile, as shown in Figure 3.8., Surface-rich (over 80 %) Ge profile is obtained.

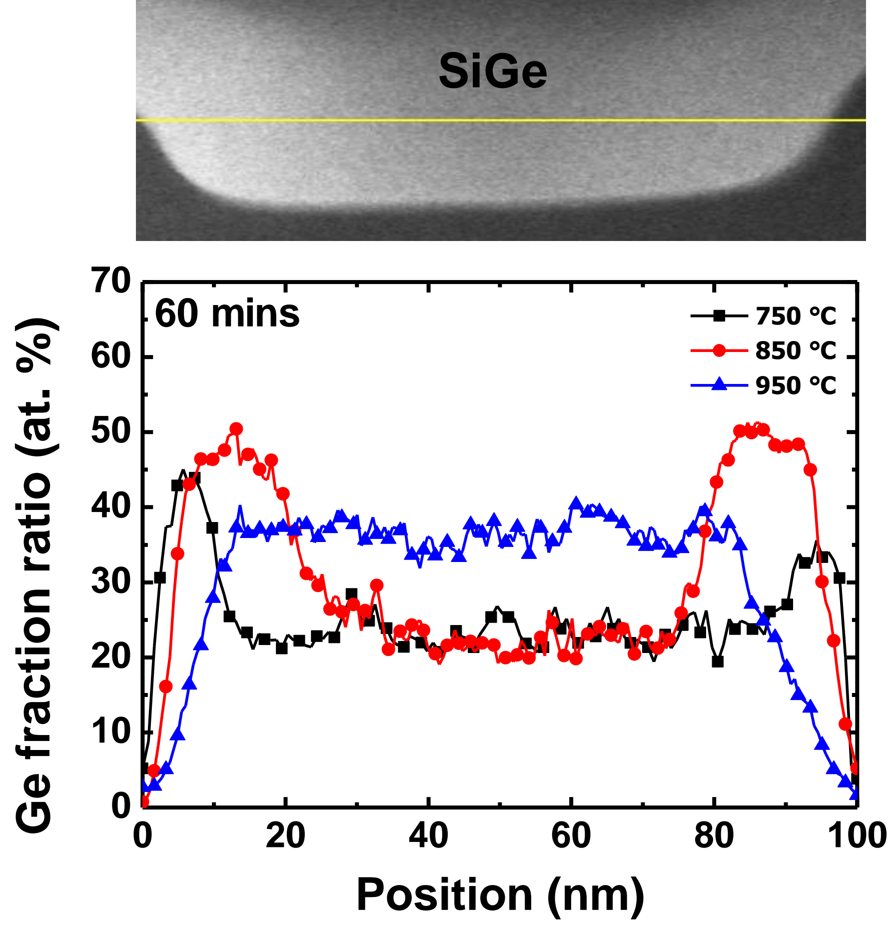


Figure 3.7. Lateral Ge profile in the SiGe channel according to various condensation temperature.

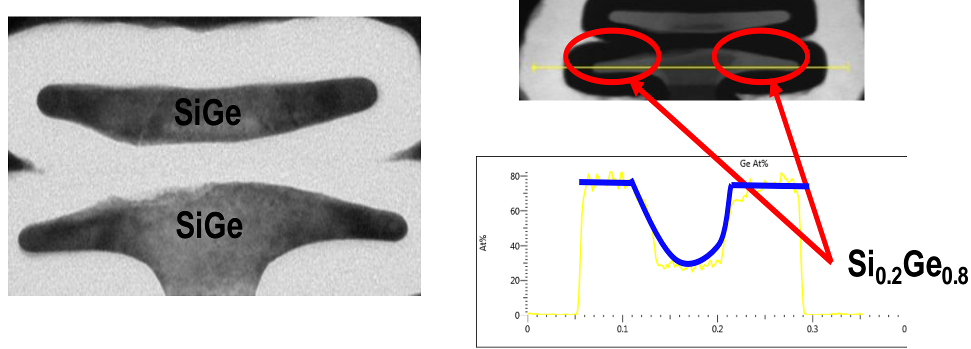


Figure 3.8. Successfully fabricated $Si_{0.2}Ge_{0.8}$ nanosheets through optimized Ge condensation process.

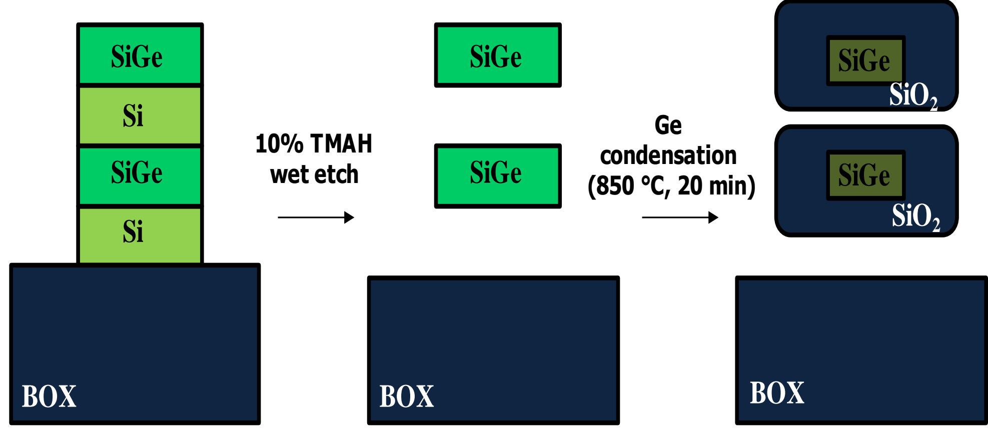


Figure 3.9. Final process steps of SiGe nanosheets formation.

3.2.2. Key Process 2 : Source/Drain Implantation

The second key process is the ion implantation of source and drain. As mentioned in previous chapters, the doping junction formation is one of the most important parts in the fabrication of TFET. In this SiGe nanosheet TFET, the implantation process is more difficult than conventional TFETs due to large height. As the depth of source and drain is deeper during nanosheet stack, the implant energy and dose should be larger enough. Especially, the underlap region between source and channel (Figure 3.10.) also should be doped well because there is the actual starting point for BTBT. However, beneath underlap region, SiO_2 and SiGe layers are alternatively formed as shown in Figure. 3.10. One need to consider whether the implanted ions can penetrate through SiO_2 layer between SiGe nanosheets. For the accurate verification of ion implantation, secondary-ion-mass-spectrometry (SIMS) analysis is performed. On alternatively grown SiGe and SiO_2 layers, ion implant is performed. For the p+ source (drain), BF_2+ ions are implanted. Implant

energy is 60 keV and dose is 3×10^{15} cm^{-2}. In n+ source (drain), implant energy is 80 keV and dose is also 3×10^{15} cm^{-2}. Lastly, RTA is carried out for 10 seconds in 950 °C N_2 ambient. Figure 3.11. shows the SIMS profile after RTA. In the case of BF_2+, boron is penetrated deeply and reached almost the end of SiGe channel. whereas, arsenic ions are heavier than BF_2 ions. Accordingly, it is revealed that arsenic ions are not diffused deeply but the doping junction is successfully formed even in the lower nanosheet.

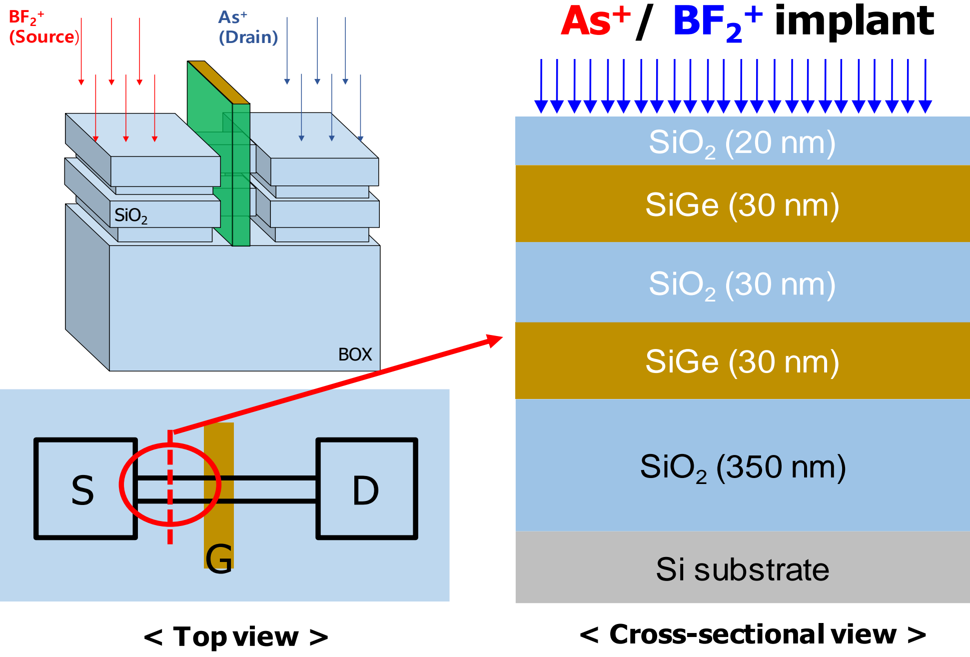


Figure 3.10. Top view and cross-sectional view at the underlapped region between source and gate.

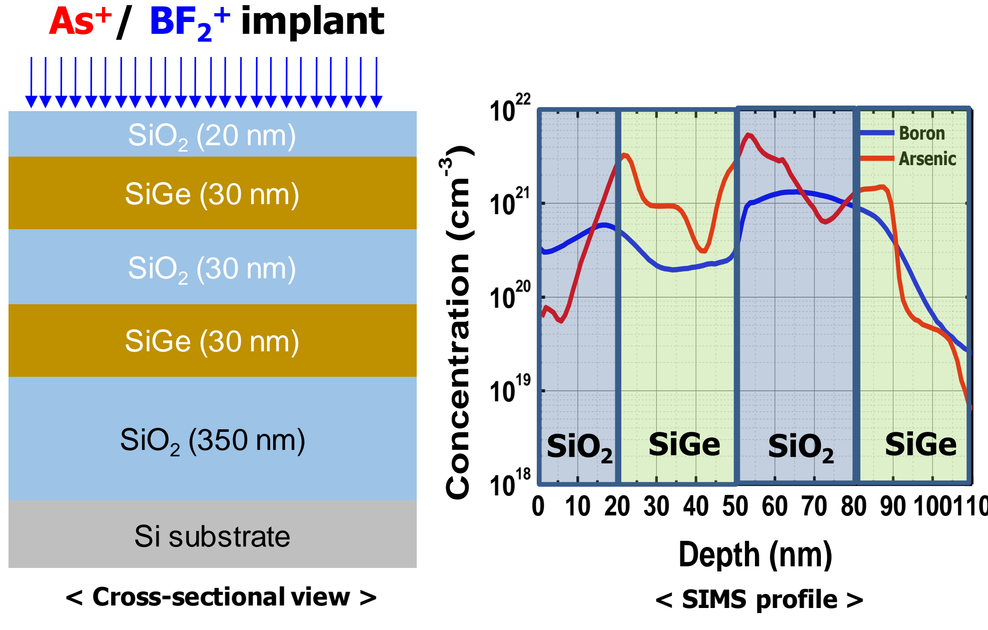


Figure 3.11. SIMS profile extracted from the underlapped region between source and gate.

3.2.3. Key Process 3 : High-κ/Metal gate Formation

The last key process is gate formation. As mentioned in the previous section, gate-last formation process includes dummy gate removal and high-κ/metal gate ALD. Figure 3.12. indicates the schematic diagram of dummy gate removal process. At the dummy gate formation step, poly-Si and Si_3N_4 is deposited. Poly-Si is material that it is easy for ICP dry etch because of high selectivity to SiO_2. Si_3N_4 plays a role of etch stop layer at CMP process. Without S_i3N_4 layer, the uniformity of wafer surface is seriously deteriorated [46]. After ILD process, SiO_2 CMP is executed for planarization of wafer surface. The planarization is done until slurry faces the Si_3N_4 surface. Figure 3.13. shows the result of the successful planarization after 100 seconds CMP.

When the Si_3N_4 surface is exposed, Nitride is etched in 98% H_3PO_4 solution. As the etch rate of 98% H_3PO_4 is about 3 nm/min [47], wet etch is executed for 20 min to remove 50 nm Si_3N_4 layer perfectly. The residual layer of dummy gate is 250 nm poly-Si. To etch the poly-Si layer roughly, ICP dry etch is proceeded earlier. Even though Si dry etch is finished, poly-Si can still remain, especially at the sidewall of active region. In Figure 3.14., it is shown that the residual poly-Si sidewall is formed next to fin. To remove residual poly-Si sidewall, isotropic wet etch is necessary. Among the variety of wet etchants, the mixed solution consisted of CH_3COOH, HNO_3, and HF is used [48]. The composition ratio of the three solutions is 80 (CH_3COOH):80 (HNO_3): 1 (HF), respectively. As there are only two materials SiO_2 and poly-Si exposed to the surface at this step, the selectivity between SiO_2 and poly-Si should be examined. Figure 3.15., indicates the thickness of remaining SiO_2/poly-Si layer according to wet etch time. The revealed etch rate for poly-Si is 9 A/sec. As a result, it is disclosed that the selectivity between SiO_2 and poly-Si in this solution is over 15:1. Consequently, the main wet etch is performed for 80 sec. For the last step of dummy gate removal, the wafer is dipped in 100:1 HF solution for 390 seconds. The objective of this step is to removed SiO_2 grown during condensation process. Figure presents the etch rate of 100:1 HF solution for SiO_2 etch. Finally, the SiGe channels are exposed, as shown in Figure 3.16.

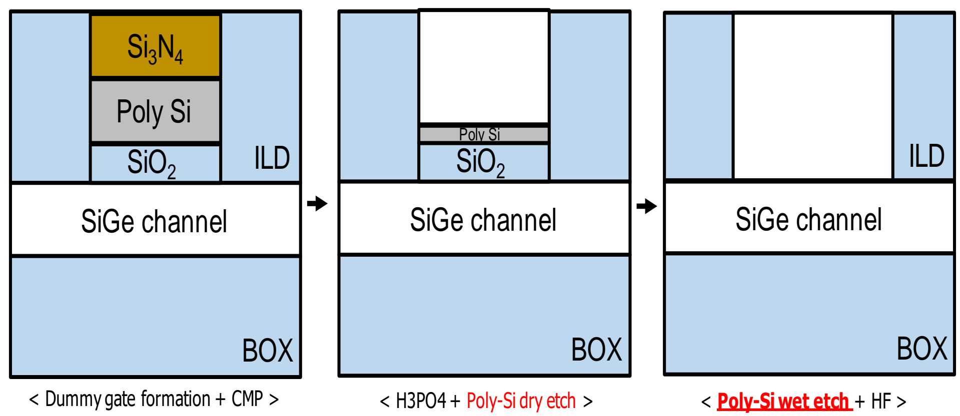


Figure 3.12. Process steps of dummy gate removal.

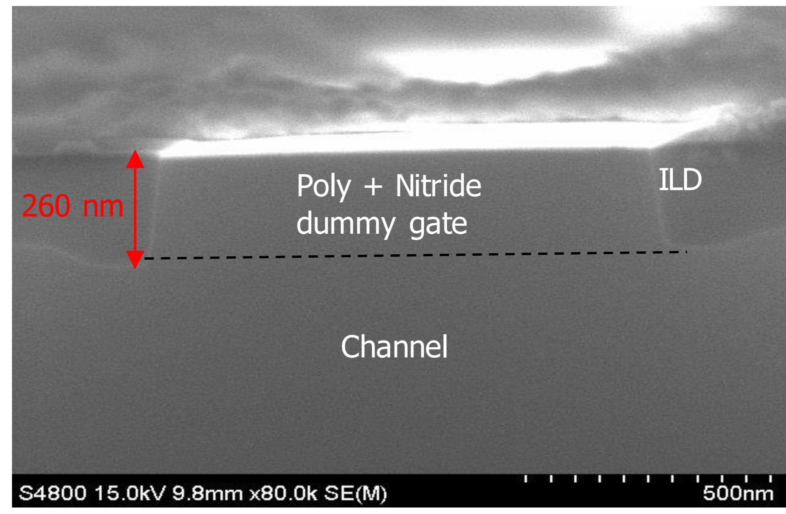


Figure 3.13. Exposed dummy gate after the CMP process.

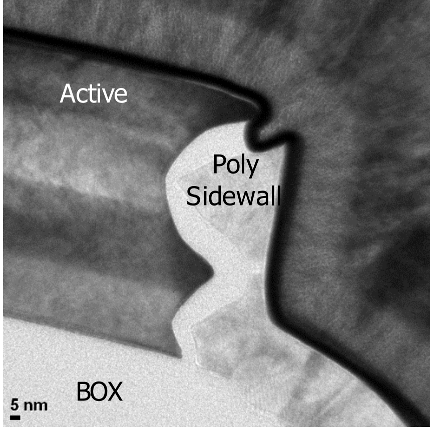


Figure 3.14. Residual poly-Si sidewall next to the active region.

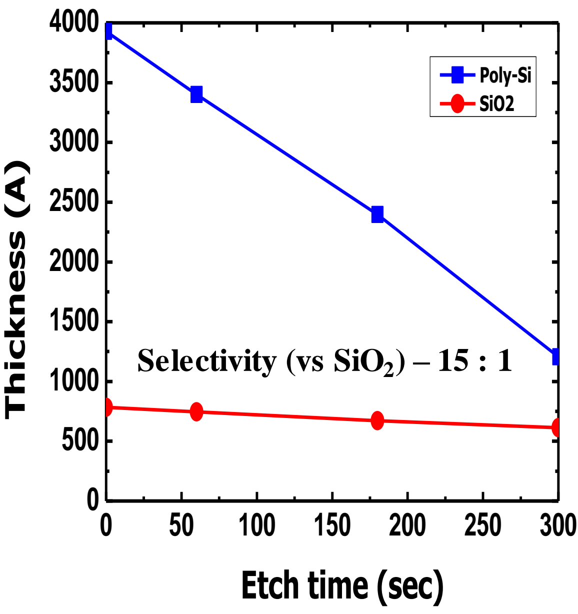


Figure 3.15. Si etch rate and selectivity compared to SiO_2 during poly-Si wet etch.

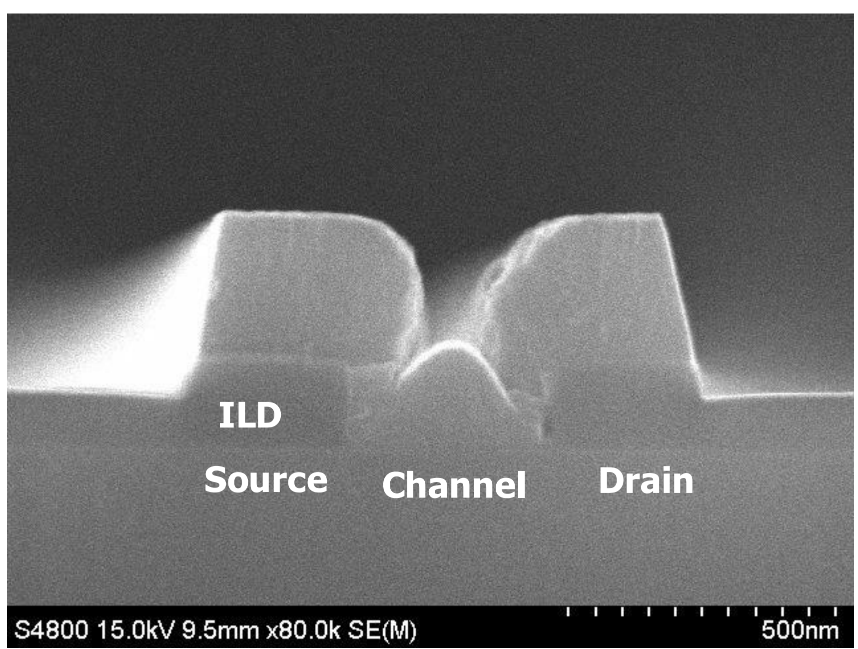


Figure 3.16. Exposed SiGe channel after the dummy gate removal.

From this time, gate-last process is started in earnest. After get rid of native oxide on the SiGe channel, high-κ materials are deposited by ALD. Al_2O_3 and HfO_2 layer is grown for the gate oxide. There have been a variety of reports dealing with the roles of Al_2O_3 and HfO_2 layers [49, 50]. It is known that Al_2O_3 has excellent leakage protection [51] to be appropriate interfacial layer for SiGe channel. On the other hand, HfO_2 is the most actively used for high-κ material due to its superior dielectric constant and CMOS compatibility. So then, we should investigate the detailed deposition condition for each high-κ material. In other words, the thickness of each layer should be precisely determined for optimal gate controllability of TFET. At this time, the three combinations for the gate stack is suggested with reference: Ref [26]) Al_2O_3 9 cycles, HfO_2 32 cycles, 1) Al_2O_3 6 cycles, HfO_2 32 cycles, 2) Al_2O_3 9 cycles, HfO_2 28 cycles. Electrical analysis is essential to estimate each combination of gate dielectric. Therefore, three metal-insulator-semiconductor (MIS) capacitors are fabricated. The schematic diagram of each dielectric is shown in Figure 3.17. On the SiGe layer, ALD is performed and sample is annealed in 450 °C H_2 ambient for 20 minutes. First, capacitance-voltage (C-V) characteristics are measured by using HP 4284A precision LCR meter. Dual-frequency C-V extraction method [52, 53] is used in this experiment. Figure 3.18. summarizes the C-V measurement results. In ideal case, the dielectric constant of Al_2O_3 (9) is much lower than HfO_2 (25). For this reason, case 1) seems to have largest capacitance-equivalent-thickness (CET). However, there is not big difference in the actual

capacitance between case 1 and 2. The extracted CET is 2.08 and 2.16 nm, respectively. Besides, the leakage current is also investigated. Figure 3.19. shows the leakage current according to gate voltage. It is revealed that leakage current is prevented more when physical thickness of gate oxide is thicker (case 1). Nevertheless, that difference is not that meaningful because leakage current become noticeable over -2.5 V gate voltage. The last factor to consider is interface trap density. D_{it} is extracted by conductance method [54, 55]. As a consequence, in Figure 3.20., it is indicated that D_{it} is largest in the case 1. The reason for poor interface trap in case 1 can be explained by the fact that the quality of Al_2O_3 layer is proportional to the number of ALD cycles [56]. In the earlier ALD cycles, the oxygen atoms tend to be attached to interfacial Si atoms. Thus, the composition ratio of oxygen in Al_2O_3 becomes low and the interface quality becomes worse. When additional oxygen is supplied by later cycles, the oxygen ratio is stabilized and the overall quality of Al_2O_3 is improved. To examine the effect of each gate dielectric, TCAD simulation which applies the EOT and D_{it} condition is conducted, eventually. As a result, the best performance is implemented for SS and I_{ON} in case 2 (See Figure 3.21.). Based on the verified results, the thicknesses of Al_2O_3 and HfO_2 are determined as 1 nm (9 cycles) and 3.5 nm (32 cycles), respectively. After high-κ ALD, TiN ALD is also performed with 160 nm thickness. Figure 3.22. displays the final gate stacking situation.

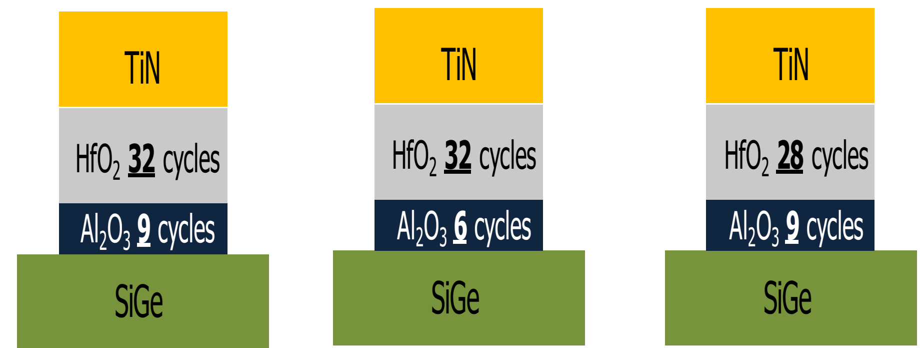


Figure 3.17. Dielectric stack conditions used in the experiment.

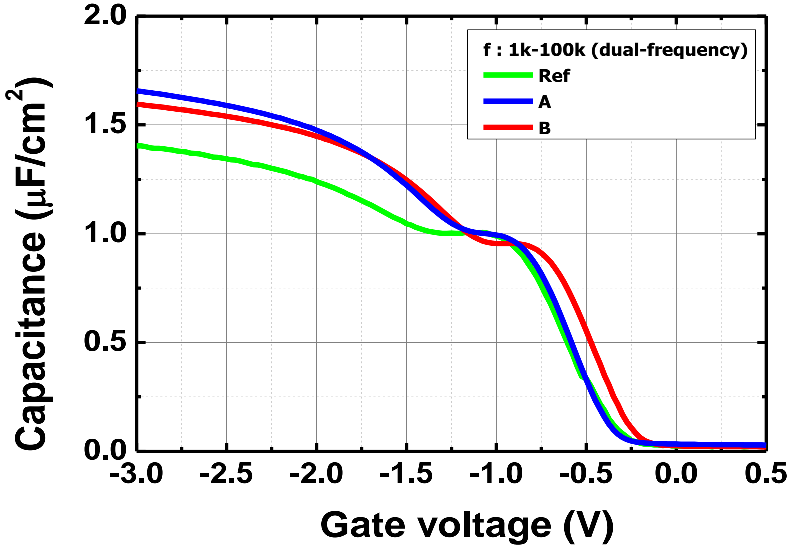


Figure 3.18. Capacitance-voltage measurement result of MIS capacitor extracted by dual-frequency method.

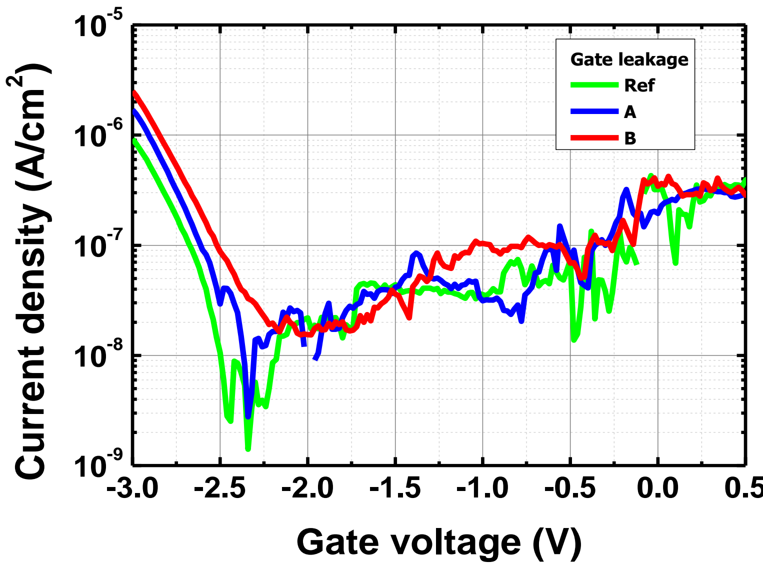


Figure 3.19. Gate leakage current of MIS capacitor during gate sweep.

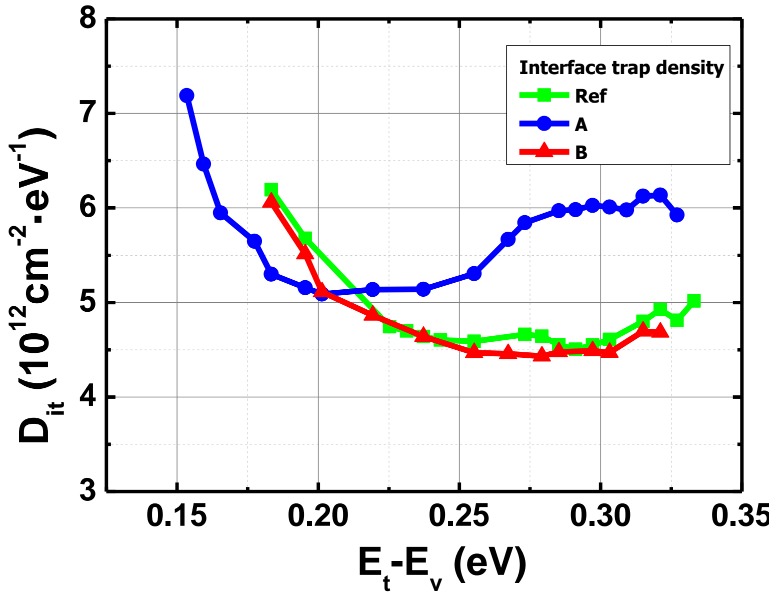


Figure 3.20. D_{it} of each gate dielectric along the trap energy level.

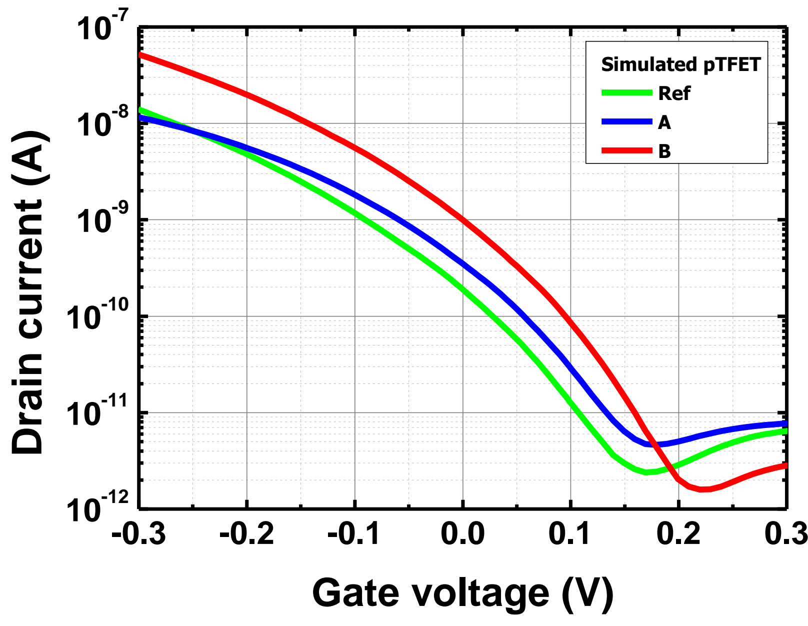


Figure 3.21. Simulated transfer curves of each gate dielectric reflecting CET and the interface trap density.

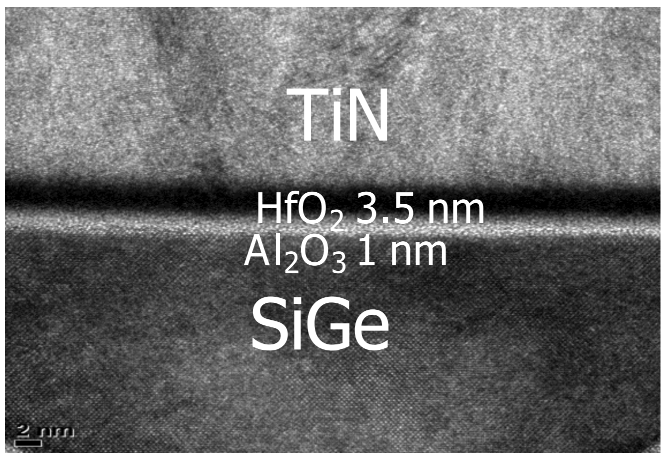


Figure 3.22. Final gate stack used in the main process.

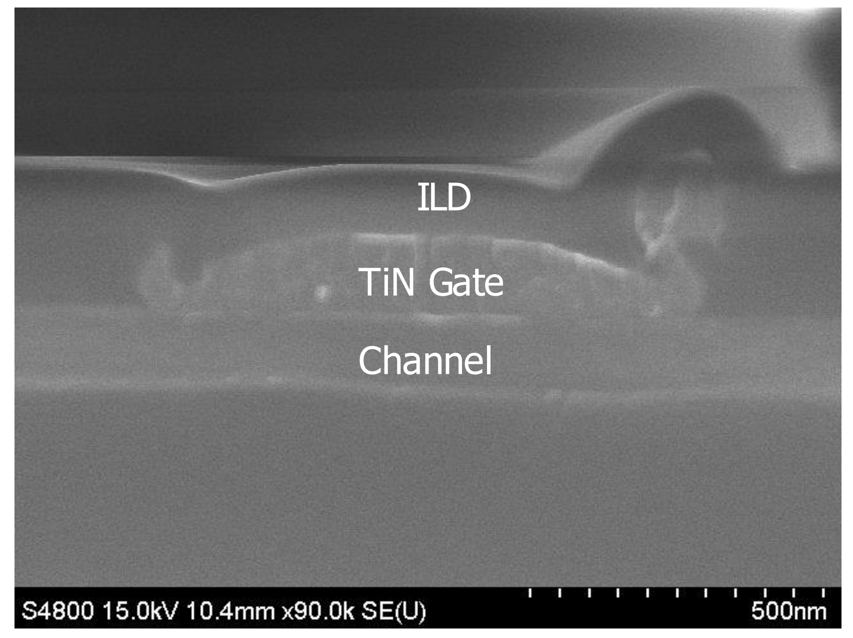


Figure 3.23. SEM image of high-κ/metal gate deposited on the channel.

Chapter 4

Results and Discussion

The measurement results from the fabricated SiGe nanosheet TFET are presented in this chapter. The basic transfer and output characteristics are reported. Then, the performance comparison with previously fabricated surface-rich SiGe TFET is done. In addition, the performance of SiGe nanosheet TFET and the co-fabricated SiGe nanosheet MOSFET is also compared. Inverter performance is examined by calibrated TCAD simulation. In discussion section, the superiority of proposed SiGe nanosheet TFET is examined closely through the performance benchmarks of the reported TFETs. Lastly, the improvement points of proposed TFET are investigated.

4.1. Measurement Results

First of all, the diode characteristic should be checked to confirm the formation of p-i-n or n-i-p doping junction. Without gate bias, the anode current is measured according to anode voltage. Through Figure 4.1., one can assert that the anode current is successfully rectified by both p-i-n and n-i-p junctions. As the focus of TFET is low power operation. In Figure 4.2., transfer curves of the fabricated SiGe nanosheet TFETs are presented. Both nTFETs and pTFETs are measured. $|V_{DS}|$ is applied for 0.1 V and 0.7 V,

respectively. The I_{ON} is defined as I_{DS} when gate overdrive voltage (V_{GS}-V_t) equals the V_{DS}. I_{ON} of pTFET is measured as 0.35 μA/μm at the -0.7 V of V_{DS}. Whereas, I_{ON} of nTFET is 0.22 μA/μm. Figure 4.3. shows the point SS according to drain current (I_{DS}). For the pTFET, the minimum SS is 50 mV/dec and the average SS, which is calculated as the slope from 10^{-12} A to 10^{-9}A of drain current is 70 mV/dec. For the nTFET, the minimum SS is 55 mV/dec and the average SS is 82 mV/dec, respectively. Output curves are exhibited in Figure. 4.4. It is found out that the current drivability of pTFET is better than nTFET.

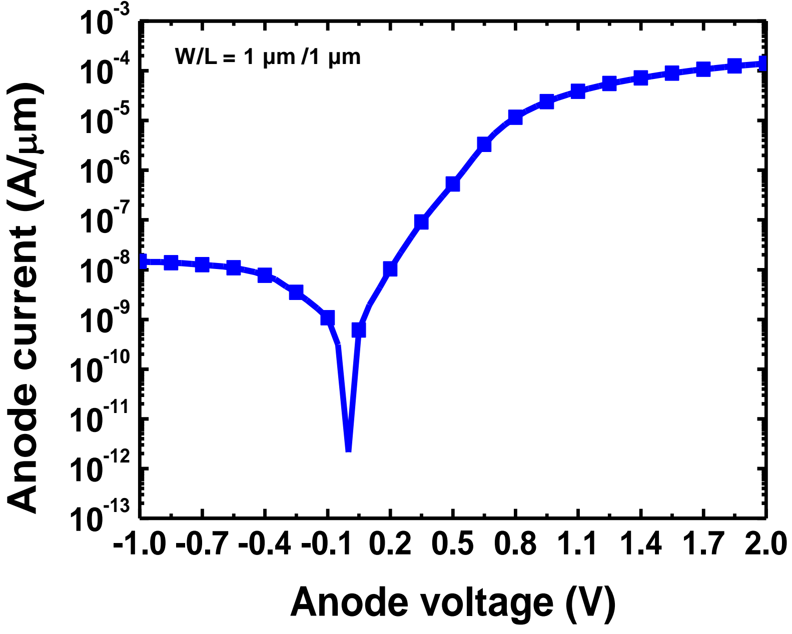


Figure 4.1. Diode characteristic of the fabricated SiGe nanosheet TFET.

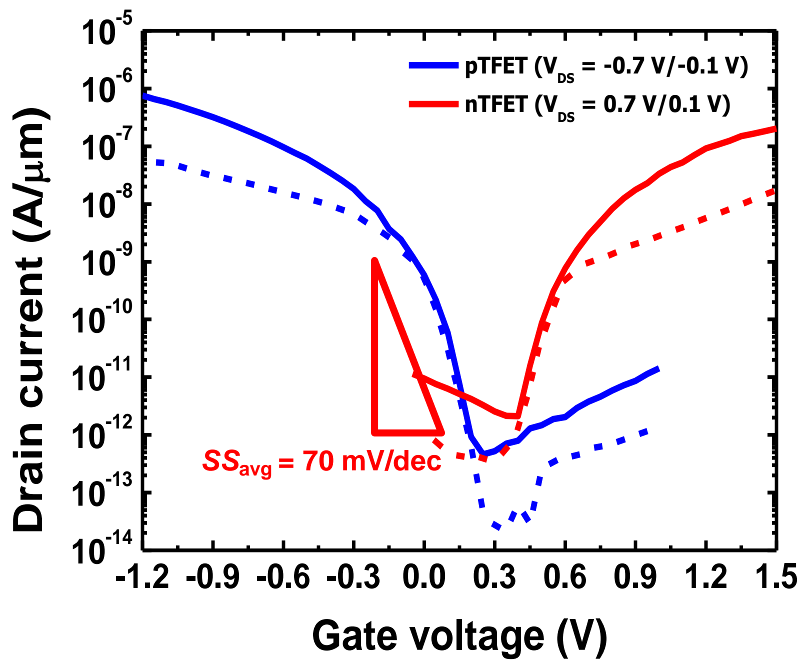


Figure 4.2. Transfer curves of the fabricated SiGe nanosheet TFET.

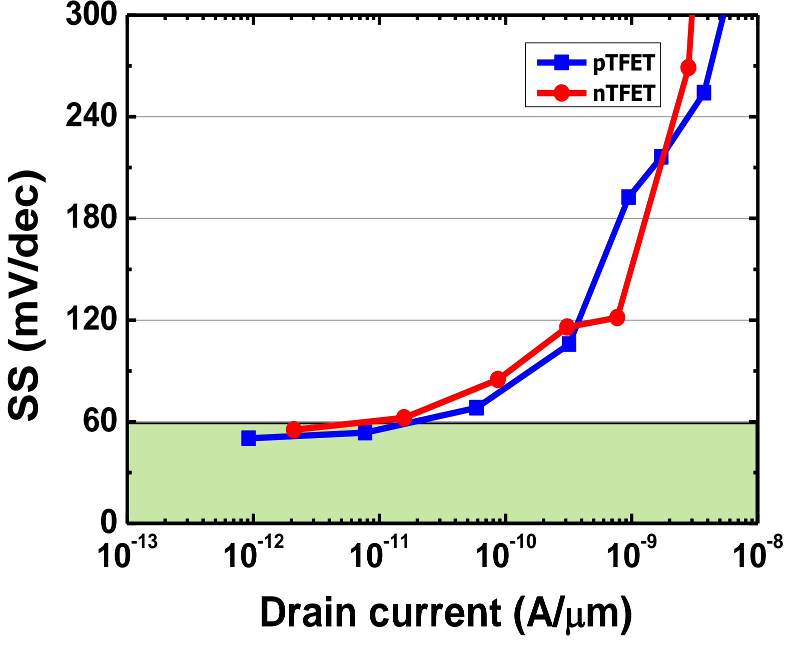


Figure 4.3. Extracted point SS according to drain current.

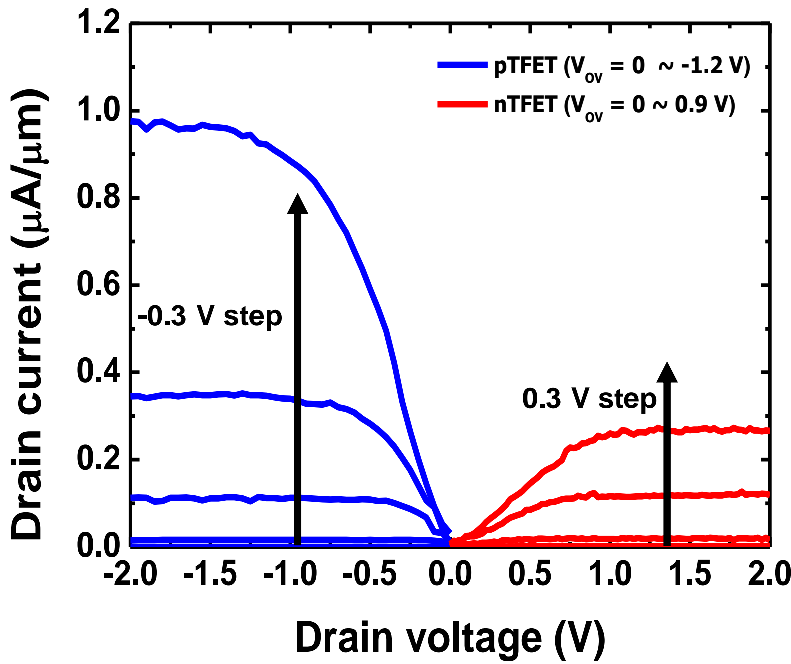


Figure 4.4. Output characteristics of the fabricated SiGe nanosheet TFET.

4.2. Analysis of Device Characteristics

4.2.1. Improved Factors to Performance in SiGe nanosheet TFET

Later, the fabricated SiGe nanosheet TFET is compared to previous fabricated surface Ge-rich $Si_{0.6}Ge_{0.4}$ TFET [26]. Surface Ge-rich SiGe TFET features higher Ge ratio at the surface through Ge condensation, as similar as proposed SiGe nanosheet TFET. For the precise comparison, the cross-section views of SiGe nanosheet TFET and surface Ge-rich SiGe TFET are compared in Figure 4.5. The maximum Ge ratio at the surface is about 0.4, remarkably smaller Ge ratio than that of SiGe nanosheet TFET. The $Si_{0.6}Ge_{0.4}$ TFET has

fin structure, while SiGe nanosheet TFET has GAA structure. As the overall performance of pTFETs is better than nTFETs, transfer curves are compared among pTFETs. Figure 4.6. shows the results of transfer curves. V_{DS} is -0.7 V and -0.1 V, respectively. When V_{DS} = -0.7 V, both I_{ON} and SS are higher in SiGe nanosheet TFET. As mentioned in Chapter 2, current increase and steeper SS are the representative effects in TFETs resulted from narrow bandgap. Moreover, the effect of Ge content can be clearly confirmed in the difference in V_t. The V_t is significantly reduced in the SiGe nanosheet TFET. This result is quite similar to the trend shown in Figure 2.10. The enhanced BTBT efficiency of $Si_{0.2}Ge_{0.8}$ channel can be verified through temperature dependence of each TFET. The measurement is performed at 298K, 323K, and 348K temperature. Figure 4.7(a). shows the transfer curves of $Si_{0.2}Ge_{0.8}$ nanosheet TFET according to temperature. It is revealed that the subthreshold current under V_t is mainly changed, while I_{ON} is almost remained. This trend is quite the typical temperature dependence of conventional TFETs [57]. The activation energy (E_a) extracted from the transfer curves of each TFET device is presented in Figure 4.7(b). the data of $Si_{0.6}Ge_{0.4}$ TFET is also compared in this graph. In the conventional TFETs, the region where E_a is under 0.1 eV is considered as BTBT-dominating region, because BTBT does not depend on the temperature. From 0.1 eV to the half of bandgap, TAT dominates the current flow of TFET. Over the half of bandgap of E_a, it is considered that SRH recombination is the main mechanism of drain current [57]. In $Si_{0.2}Ge_{0.8}$ nanosheet TFET, the overall E_a is low due to narrower bandgap of $Si_{0.2}Ge_{0.8}$.

It is observed that BTBT-dominating region is far larger than in $Si_{0.6}Ge_{0.4}$ TFET. Also, transition from TAT to BTBT is done in the relatively small gate voltage window in SiGe nanosheet TFET. These results imply that the contribution of BTBT to current flow is high. Meanwhile, the CET is thinner in SiGe nanosheet TFET. The gate stack condition of surface-rich SiGe TFET is Al_2O_3 9 cycles and HfO_2 32 cycles, which is the same condition of the reference sample in Chapter 3.2.3. Therefore, the gate controllability of SiGe nanosheet is better than SiGe fin TFET and the result is revealed with difference between SS.

To examine the AC performance of SiGe nanosheet TFET, the inverter characteristics are investigated through TCAD mixed-mode simulation. The basic electric properties of each device are reflected from the experimental results in the TCAD simulation [26]. Figure 4.8(a). shows the basic transient characteristic of SiGe nanosheet and $Si_{0.6}Ge_{0.4}$ TFET, respectively. V_{DD} is set to 0.6 V, which is regarded as low supply voltage for CMOS devices. The rising/falling time is 1 ns and the holding time is 1 µs. Load capacitance (C_L) is 1 fF. In fact, one can find out that only the $Si_{0.2}Ge_{0.8}$ nanosheet TFET plays a role as a CMOS device for the inverter. The propagation delay of each inverter is extracted in Figure 4.8(b). In the inverter with $Si_{0.2}Ge_{0.8}$ nanosheet TFET, delay is quite small as 14 ns. This can be explained by the fact that the high I_{ON} of SiGe nanosheet TFET remarkably reduces the resistance of each device.

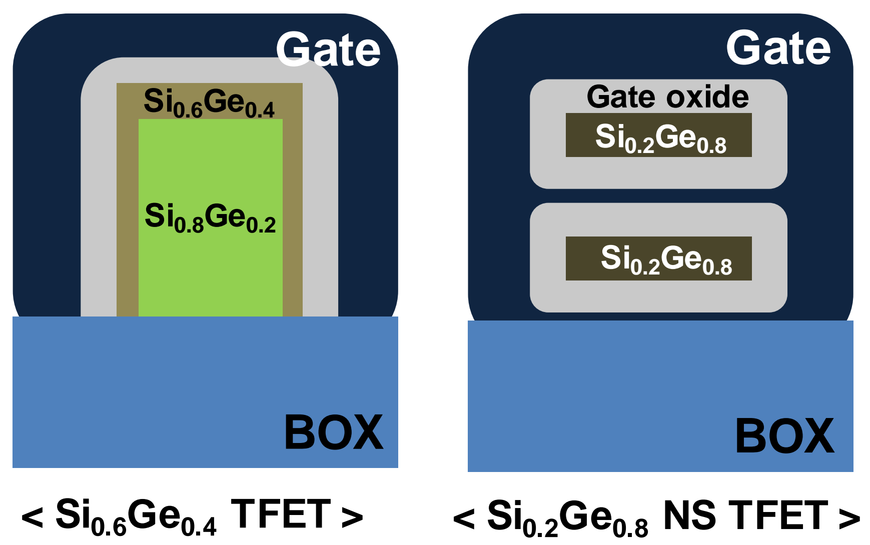


Figure 4.5. Cross-sectional views of $Si_{0.6}Ge_{0.4}$ surface Ge-rich TFET and $Si_{0.2}Ge_{0.8}$ nanosheet TFET.

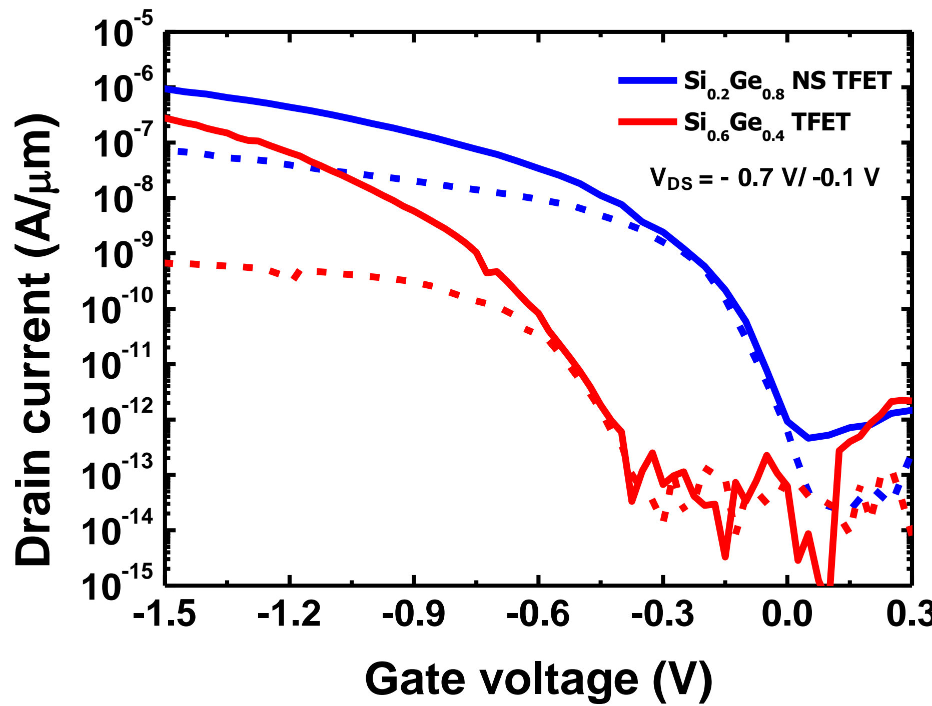


Figure 4.6. Transfer curves of p-type $Si_{0.6}Ge_{0.4}$ and $Si_{0.2}Ge_{0.8}$ nanosheet TFET.

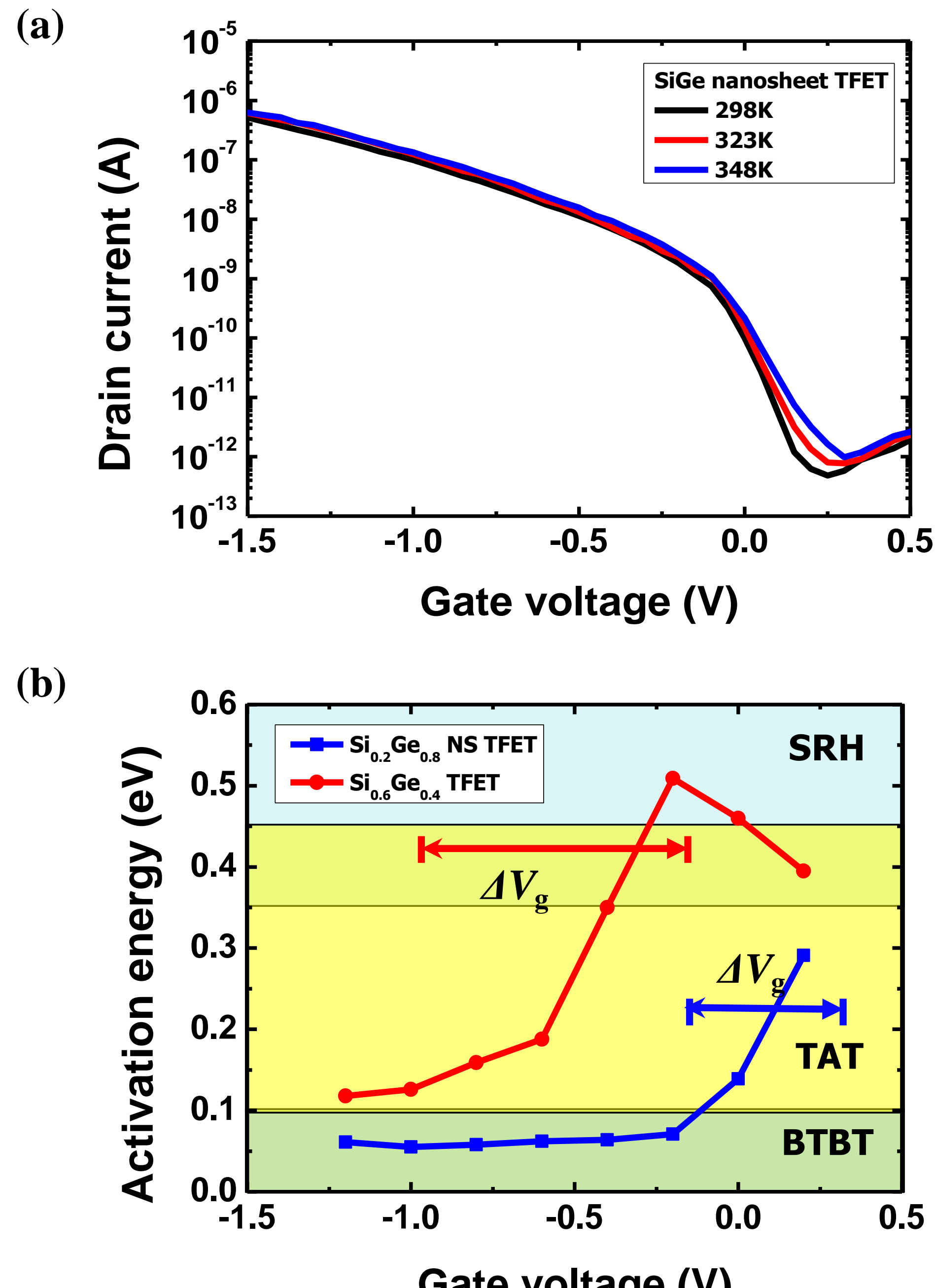


Figure 4.7. (a) Transfer curves at the various temperature and (b) extracted E_a from the temperature measurement data according to the gate voltage.

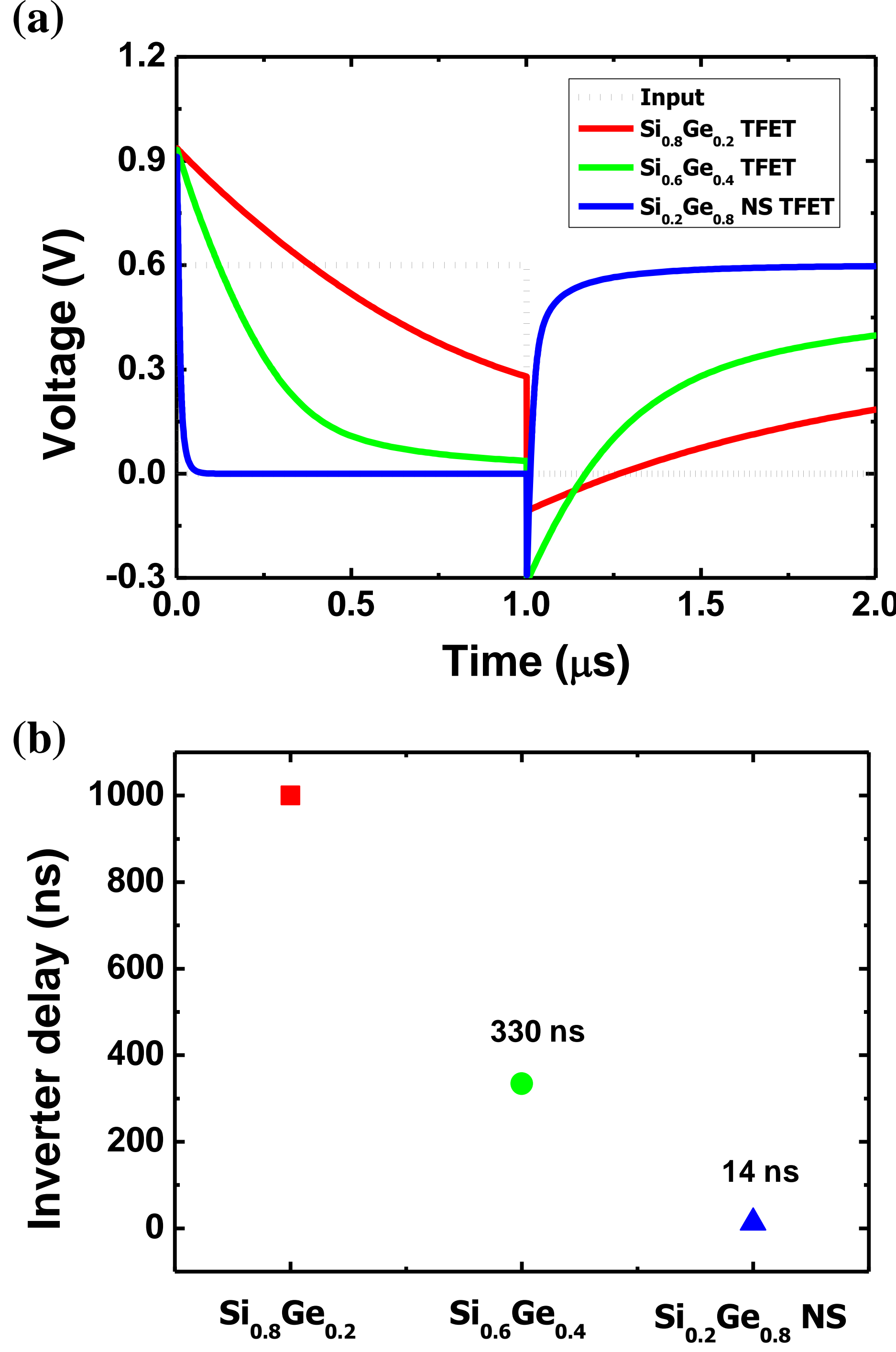


Figure 4.8. (a) Simulated transient characteristics and (b) extracted propagation delay of SiGe TFET inverter.

4.2.2. Performance Comparison with SiGe nanosheet MOSFET

The device performance of SiGe nanosheet pTFET is also compared to SiGe nanosheet pMOSFET which is fabricated at the same time, same process. Only simply changing the mask layout for ion implant can fabricate MOSFETs with the same design. Figure 4.9(a) shows the transfer curves and Figure 4.9(b) shows the output curves of each TFET and MOSFET. As is well known, the I_{ON} of MOSFET is higher than TFET. However, the gap of I_{ON} is relatively small. The poor hole mobility [58] caused by defects at the $Si_{0.2}Ge_{0.8}$ surface is cited as the cause of this phenomenon. Nonetheless, the SS and I_{ON}/I_{OFF} ratio is higher in TFET. V_t is relatively small. Moreover, it is shown that the I_{ON}/I_{OFF} ratio is maximized at the low V_{DS}, -0.1 V. Based on these results, SiGe nanosheet TFET is the better option for low power application, as explained in Chapter 1.

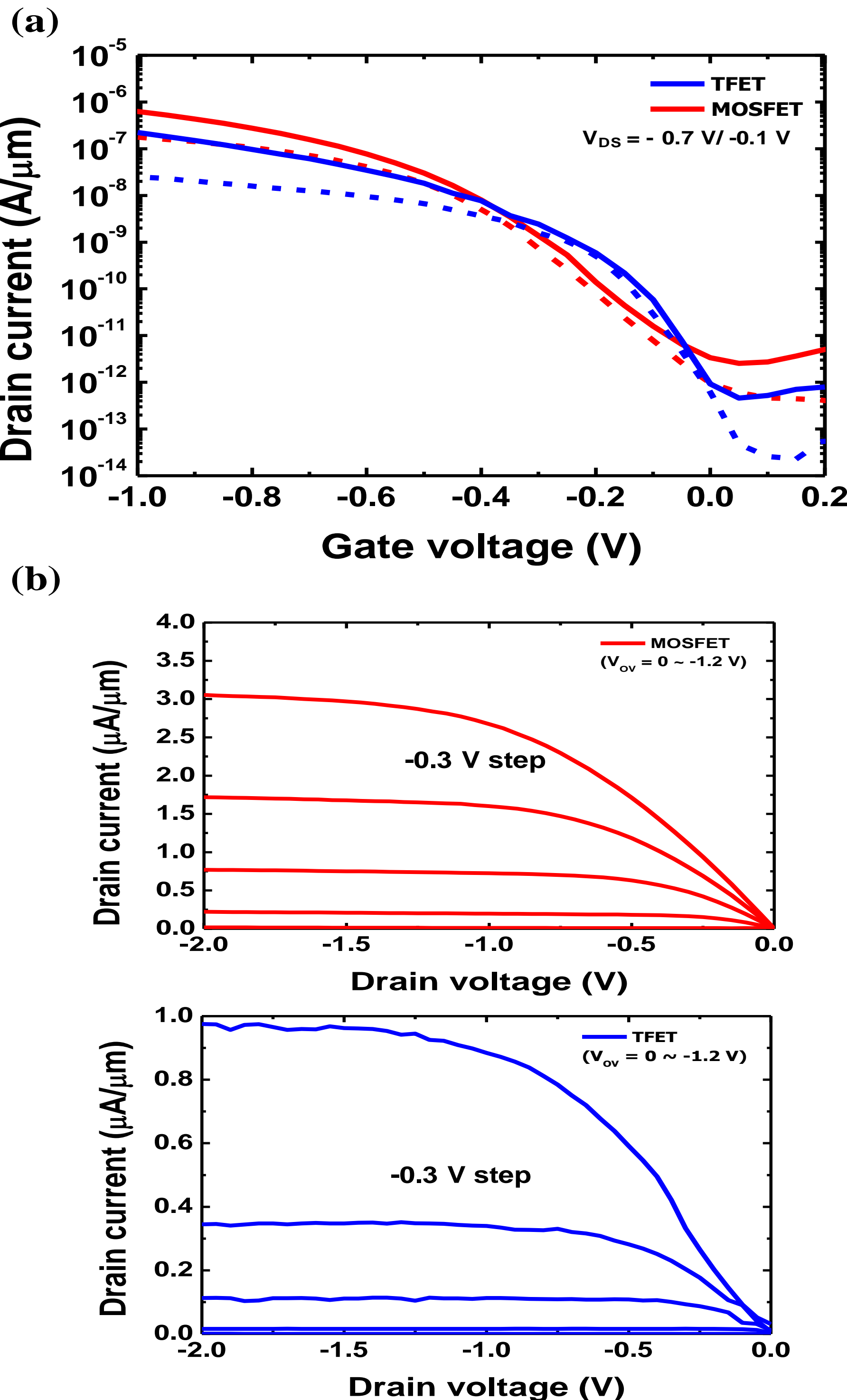


Figure 4.9. (a) Transfer curves and (b) output curves of p-type SiGe nanosheet TFET and MOSFET which are co-fabricated.

4.3. Performance Evaluation through Benchmarks

The DC performance of the fabricated SiGe nanosheet TFET is compared to the variety of reported TFETs [21, 26, 60-72] with superior records. Figure 4.10(a) shows the SS-I_{ON} benchmark of the reported TFETs. The device performance of each device is examined at the 0.3~0.9 V of V_{DD}. The red dots indicate the benchmarks of III-V TFETs, while green dots show the benchmarks of Si or Ge-based TFETs. Blue dots represent the device performance of SiGe nanosheet TFET. It is shown that the overall SS is steep in SiGe nanosheet TFET. I_{ON} is above average in the compared group. Furthemore, I_{ON}/I_{OFF} ratio – I_{ON} benchmarks are also presented in Figure 4.10(b). Especially in the low V_{DD} (0.1 V), the I_{ON}/I_{OFF} ratio of the SiGe nanosheet TFET stands out more. With the comparison to the reported TFETs, it is concluded that the additional I_{ON} improvement is necessary.

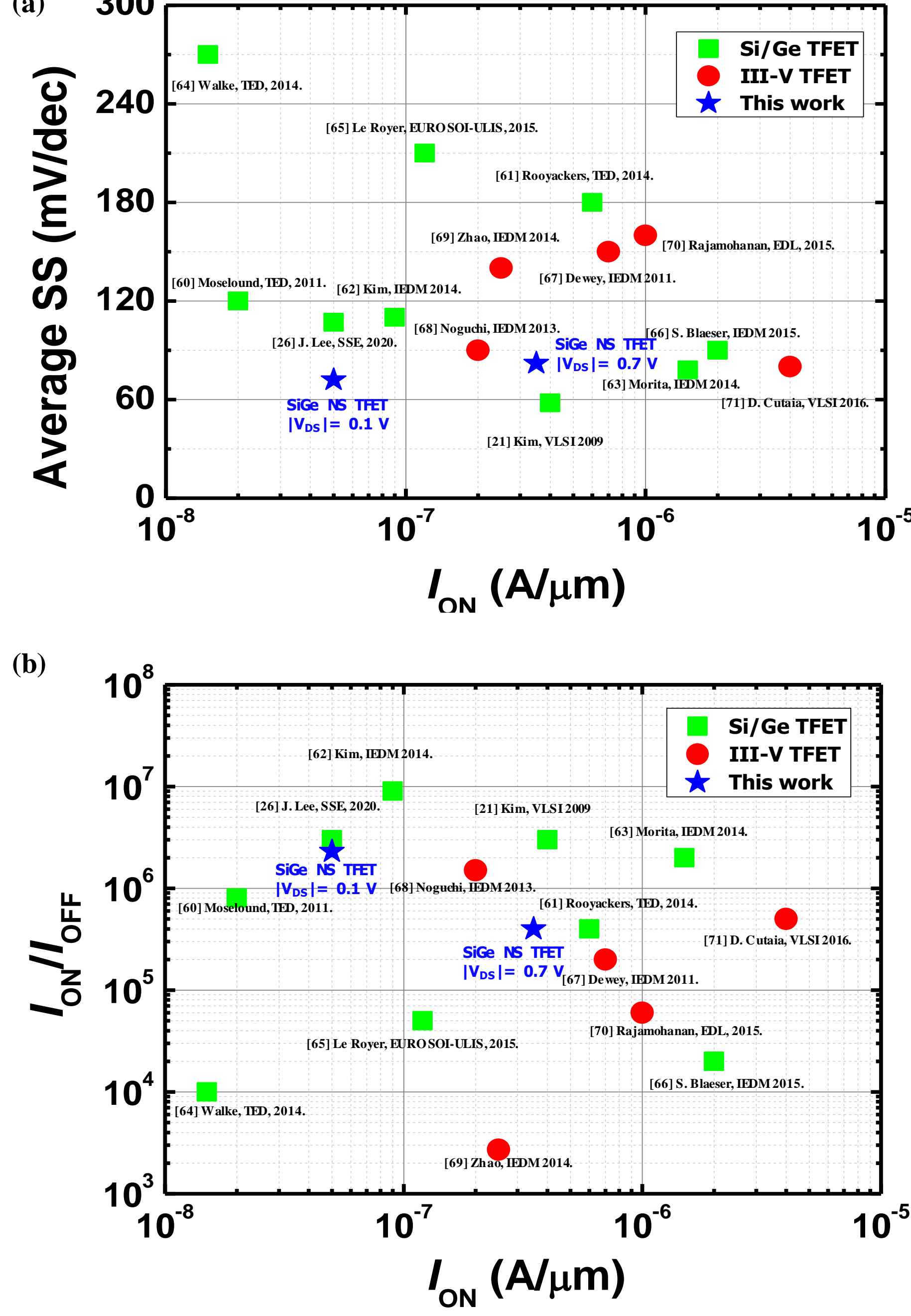


Figure 4.10. Summarized device performance of SiGe nanosheet TFET compared to the performance benchmarks.

4.4. Optimization Plan for SiGe nanosheet TFET

In the previous sections, we look into the measurement results of SiGe nanosheet TFET. Although the performance is remarkable, the problems still exist due to the limitation of the fabrication process and the device design. To summarize, there are two kinds of improvement points. 1) the quality of the gate oxide on SiGe nanosheet and 2) doping junction formed by source/drain implantation, and. In this section, these issues are addressed and the solutions are presented. After that, the optimized performance through each solution is examined.

4.4.1. Improvement of Quality of Gate Dielectric

There is room for improvement on the quality of gate dielectric. On the SiGe channel, GeO_x layer is formed during the Ge condensation and high-κ ALD process [73]. As GeO_x is very unstable material formed by the dangling bond at the SiGe surface, it can have the adverse effects on the gate oxide. Both D_{it} and EOT can be deteriorated by GeO_x layer on the SiGe. The formation of GeO_x can be prevented by sulfur passivation by forming –S bonds to the surface Si or Ge atoms [74]. In this section, the improvement point through reducing D_{it} and scaling EOT is investigated by TCAD simulation. Figure 4.11(a). shows the effect of scaled EOT. In the current condition of gate oxide formation, EOT is 2.1nm, as discussed in Chapter 3. When EOT is scaled to 1.5 nm, I_{ON} of SiGe nanosheet pTFET can increase to

3 times and *SS* becomes steeper to 62 mV/dec.

The influence of interface trap density can be confirmed in Figure 4.11(b). It is observed that the I_{OFF} is dramatically changed by D_{it}. As TAT and SRH recombination has a great influence on subthreshold current, interface traps mainly worsen I_{OFF}. In the same way, *SS* can be also increased by the interface trap. If the interface trap density can be adjusted, I_{ON}/I_{OFF} ratio can be improved up to 10 times, as shown in the Figure 4.11(b).

4.4.2. Optimization of Doping Junction at Source

The doping profiles used in this device can be improved further. First of all, the abrupt junction from the steeper lateral doping profile can enhance the electric field between source and channel. In n+ source, arsenic concentration decreases with the slope of 150 nm/dec [75]. Meanwhile, boron concentration is reduced with the slope of 50 nm/dec in p+ source [76]. With the help of the advanced RTA process [77] or in-situ source epitaxy process [78], The steepness of the doping junction can be improved. According to [78], the junction can be abrupt with the few nanometers per decade of steepness. Figure. 4.12. summarizes the improved device performance of the optimized SiGe nanosheet TFET. Adopting modified process condition, *SS* and current drivability, especially I_{ON} can be additionally supplemented. Moreover, SiGe nanosheet TFET shows a desirable performance improvement compared to the performance benchmark. It is expected that over-micron I_{ON} and near 60

mV/dec *SS* can be achieved with the improved SiGe nanosheet TFET.

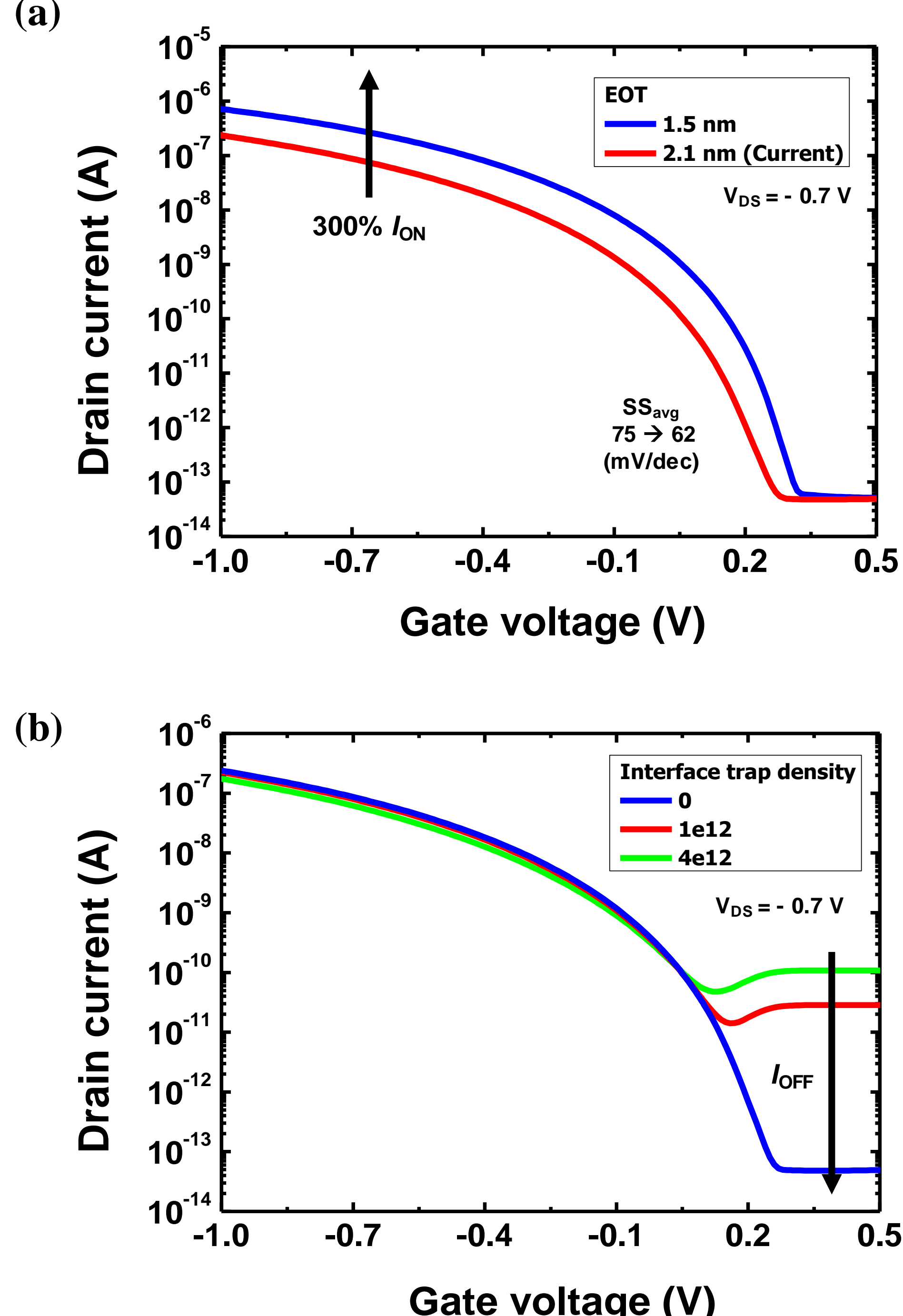


Figure 4.11. Simulated transfer curves of SiGe nanosheet TFETs according to the various conditions of (a) EOT and (b) D_{it}.

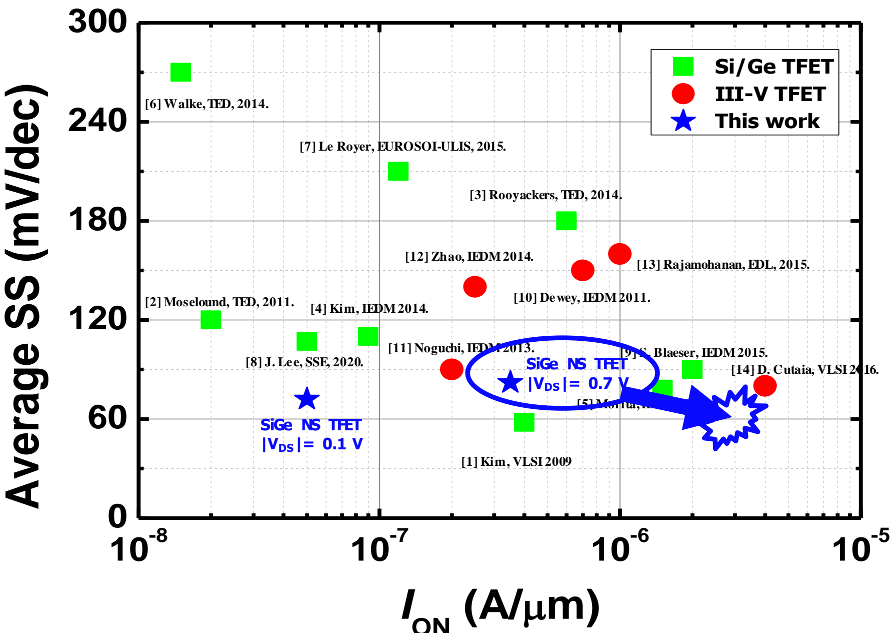


Figure 4.12. Expected device performance of SiGe nanosheet TFET with the optimized process condition.

Chapter 5

Conclusion

In this dissertation, vertically-stacked SiGe nanosheet TFET which is compatible with the state-of-the-art CMOS devices is proposed. The objective of proposed TFET is to solve the limitations of conventional TFETs : high I_{ON}, reducing ambipolar current, and CMOS compatibility. To achieve these goals, Ge-condensed multi SiGe nanosheets structure is suggested.

Through TCAD simulation, each concept of SiGe nanosheet TFET is verified. It features high current drivability, high I_{ON}/I_{OFF} ratio, and smaller SS than conventional Fin and single-GAA TFET. SiGe channel with high Ge content enables to obtain narrow bandgap and boost BTBT. Nanosheet structure has an advantage of maximizing effect channel width and gate controllability. Drain underlapping reduces ambipolar current.

In the fabrication process, the excellent formation process of SiGe nanosheets with high Ge content is proposed. Two $Si_{0.2}Ge_{0.8}$ nanosheets are successfully formed by optimized Ge condensation. To produce the devices as close as possible to the designed conditions, gate stack and ion implantation test are performed. As a result, the combination of Al_2O_3 and HfO_2 high-κ layers is determined and the EOT and D_{it} are optimized. In ion implantation test, the penetration of boron and arsenic is confirmed by SIMS analysis, respectively. Finishing the fabrication, the performance of the SiGe

nanosheet TFET is investigated. Under 60 mV/dec SS is successfully achieved. Through the comparison with the previously reported SiGe and Si TFETs, it is clearly affirmed that SiGe nanosheet TFET has higher I_{ON}, I_{ON}/I_{OFF} and steeper average SS. the factors of the improvement, such as higher Ge content and enhance gate control are also precisely analyzed.

Even though it is confirmed that the proposed concepts are generally well realized in the fabricated SiGe nanosheet TFET, there are still a few problems that have not been resolved. If the junction profile at the source becomes abruptly, using the in-situ-doped source epitaxy, the overall electrical performance can be certainly boosted. Moreover, alleviating D_{it} helps the reducing I_{OFF} and other leakage components. Well-scaled EOT also contributes steeper *SS* and higher I_{ON}. Lastly, the defects generated in the SiGe channel with high Ge ratio can deteriorate the electrical characteristic of proposed TFET. The accurate analysis which can quantify the adverse effects of defect is necessary. In addition, C_{GD} issue should be resolved to improve AC performance. With this SiGe nanosheet structure, both MOSFET and TFET devices can make good progress in the future logic applications.

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초 록

초고밀도 집적회로 기술의 발전은 고집적도 달성을 통해 단위 칩의 연산 속도 및 용량 향상에 기여할 소형의 소자를 끊임없이 요구하고 있다. 하지만 최신의 상보형 금속-산화막-반도체 (CMOS) 기술에서 금속-산화막-반도체 전계 효과 트랜지스터 (MOSFET) 의 단순한 소형화는 더 이상 집적회로의 성능 향상을 보장해 주지 못하고 있다. 특히 소자의 크기가 줄어드는 반면 정적 전력 소모량은 전압 스케일링의 둔화로 인해 감소되지 않고 있는 상황이다. MOSFET의 짧은 채널 효과로 인해 증가된 누설 전류가 전압 스케일링의 어려움을 주는 대표적 원인으로 꼽힌다. 이러한 근본적인 MOSFET의 한계를 극복하기 위하여 지난 10여년간 새로운 단계의 전계 효과 트랜지스터 소자들이 연구되고 있다. 그 중 터널 전계 효과 트랜지스터(TFET)은 그 특유의 우수한 전원 특성으로 각광받아 집중적으로 연구되고 있다. 많은 연구에도 불구하고, TFET의 부족한 전류 구동 능력은 MOSFET의 대체재로 자리매김하는 데 가장 큰 문제점이 되고 있다.

본 학위논문에서는 상기된 문제점을 해결할 수 있는 우수한 전류 구동 능력을 가진 TFET이 제안되었다. 반송자 유입과 게이트 컨트롤을 향상시킬 수 있는 수직 적층된 실리콘저마늄(SiGe) 나노시트 채널이 사용되었다. 또한, 제안된 TFET은 CMOS 기반 공정을 활용하여 MOSFET과 함께 제작되었다. 테크놀로지 컴퓨터 지원 설계(TCAD) 시뮬레이션과

실제 측정 결과를 활용하여 제안된 소자의 우수성을 검증하였다. 단위 CMOS 소자의 관점에서, 전원 특성과 전류 구동 능력의 향상을 정량적, 정성적 방법으로 분석하였다. 그리고, 제작된 소자의 성능을 기존 제작 및 보고된 TFET 및 함께 제작된 MOSSFET과 비교하였다. 이러한 과정을 통해, 실리콘저마늄 나노시트 TFET의 활용 가능성이 입증되었다. 제안된 실리콘저마늄 나노시트 소자는 주목할 만한 전원 특성을 가졌고 저전압 구동 환경에서 한층 더 낮은 누설 전류를 가짐으로써 향후 MOSFET을 대체할만한 충분한 가능성을 보여주었다.

주요어 : 실리콘저마늄(SiGe) 채널, 터널 전계 효과 트랜지스터,다층 나노시트 전계 효과 트랜지스터, 저전압 소자, 우수한 전원 특성을 가진 CMOS 소자, 문턱 전압 이하 기울기, Ge 응축 기술, 밴드 간 터널링

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List of Publications

International Journal

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