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Capacitive Isolated Class E Converter Design Considering Touch Current and Electromagnetic Interference

접촉 전류와 전자파 방해를 고려한 정전식 절연형 클래스 E 컨버터 설계

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이 논문을 공학박사 학위논문으로 제출함
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Abstract

This dissertation studies a method to reduce the common-mode current in capacitive isolated class E converter. Removing a transformer from a galvanically isolated converter has been researched a lot to design a high power density DC/DC converter. One way to remove the transformer is to use a capacitor instead of a transformer for galvanic isolation. However, using a capacitor increases the common-mode current, which can cause high touch current and conduction EMI (Electromagnetic Interference). Due to a user's safety and compatibility with other electronic devices, all electronic devices' touch current and EMI are strictly regulated. Therefore, methods to reduce a common-mode current in a capacitive isolated DC/DC converter are studied in this dissertation.

In this dissertation, common-mode current in the grid frequency band and switching frequency band are analyzed separately. A common-mode current in the grid frequency band is related to touch current, while the switching frequency component of a common-mode current is responsible for conduction EMI. Since grid frequency is relatively low-frequency, the impedance of a capacitor is high at this frequency range. This dissertation, thus, calculates a maximum capacitance allowed to meet the touch current regulation. For DC/DC converter topology, a class E converter is chosen since this topology is suitable for operating in high frequency and reduce the capacitor to block touch current. A balanced class E converter is proposed for lowering the common-mode current in the switching frequency band. The converter's balanced structure can eliminate the common-mode voltage and thus decrease the common-mode current. A common-mode current in class E DC/DC converter with LC series network and T-network is analyzed in this dissertation. T-network is used to set the voltage gain between input and output voltage of the DC/DC converter, and the design method for this network is also

written in this dissertation. The common-mode current in a conventional and a balanced class E converter is compared. The effect of parameter error on a common-mode current in a balanced class E converter is also analyzed. Lastly, a self-powered gate driver circuit for providing power to gate drive is presented. Since a high side switch needs to be placed to operate a balanced class E converter, a circuit providing stable power to a gate driver is necessary. Therefore, a self-powered gate driver circuit that can draw power from the voltage across the switch is proposed.

Conduction EMI and touch current are measured using 40W 7cm by 3cm converter prototype. From the experiment, the proposed balanced class E converter has lower EMI noise compare to the conventional class E converter. Also, the measured touch current satisfies the regulation ensuring the safety of a proposed capacitive isolated converter.

Keywords : Capacitive Isolation, High-Frequency Converter, Touch Current, Electromagnetic Interference, Common-mode Current
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1. Introduction

1.1 Research Background

Designing a high power density isolated converter is being widely researched with advanced high bandgap devices such as GaN (Gallium Nitride) and SiC (Silicon Carbide) [1] – [4]. GaN devices, in particular, have higher saturated velocity and electron mobility compared to Si (Silicon) and SiC devices allowing high-frequency switching. Therefore, with the help of these devices, the switching frequency of the DC/DC converter can be increased up to a few MHz increasing the power density of the converter.

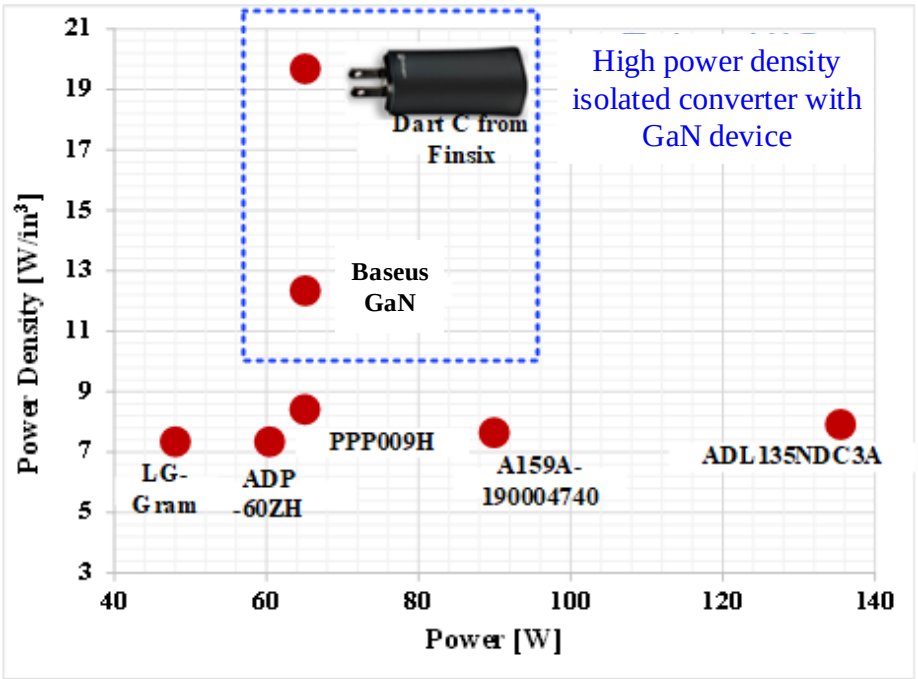


Fig. 1-1. The power density of commercial laptop chargers. Recently, high power density laptop chargers such as Dart C from Finsix [5] is being developed.

Fig. 1−1 shows the power density of commercial laptop chargers. In this figure, the galvanically isolated converter with the highest power density is Dart C from Finsix. It has a power density of 19.5 W/in^3 with a nominal output power of 65W. A laptop charger from Baseus also has a high power density, with a power density of 12.2 W/in^3. The reason for the high power density for both chargers is the use of a GaN switching device, allowing high switching frequency operation. With such high power density laptop chargers in the market, interest in designing galvanically isolated converters with high power density increases.

Most DC/DC converter uses magnetic coupling for galvanic isolation. Therefore, DC/DC converter topologies that use transformers such as flyback converter and LLC converter are widely used. For example, Fig. 1−2 shows a tear−down image

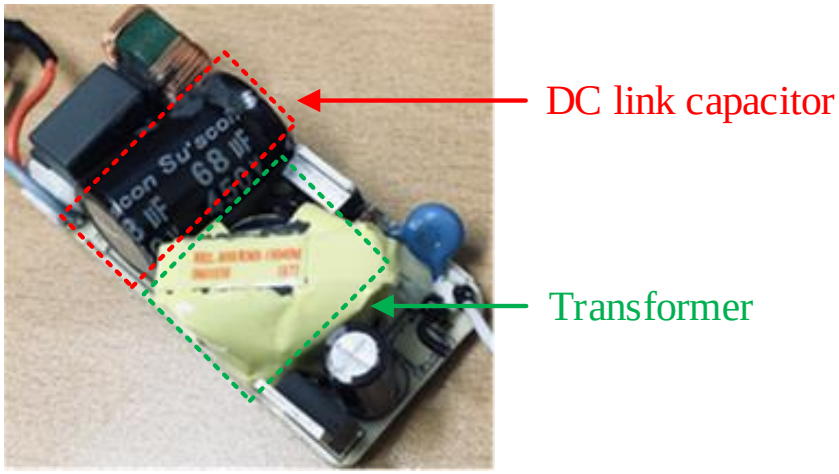


Fig. 1−2. Inside of the commercial laptop charger. Passive elements such as DC−link capacitor and transformer take up most spaces.

of a commercial laptop charger. This charger is a flyback converter with 40W nominal output power. In this image, passive elements such as DC-link capacitor and transformer take most of the DC/DC converter space. Therefore, reducing the size of these passive elements, especially a transformer, is key to increasing an isolated converter's power density. This dissertation uses capacitive isolation to remove the transformer from a DC/DC converter to achieve galvanic isolation. Most importantly, regulations for an isolated converter such as touch current [6]-[9] and conduction EMI (Electromagnetic Interference) [10]-[17] are studied to design a safe and compatible DC/DC converter.

When working with IT equipment, the safety of users is one of the most important factors to be considered when designing electronic devices. Therefore, many restrictions are placed to limit the touch current to ensure the safety of users from electric shock. Fig.1-3 shows the effect of touch current on the human body according to the current flow's current magnitude and duration. It can be seen that the human body can perceive current with a magnitude higher than 0.5 mA. Therefore, standard such as IEC 60950 restricts the magnitude of touch current. Table 1-

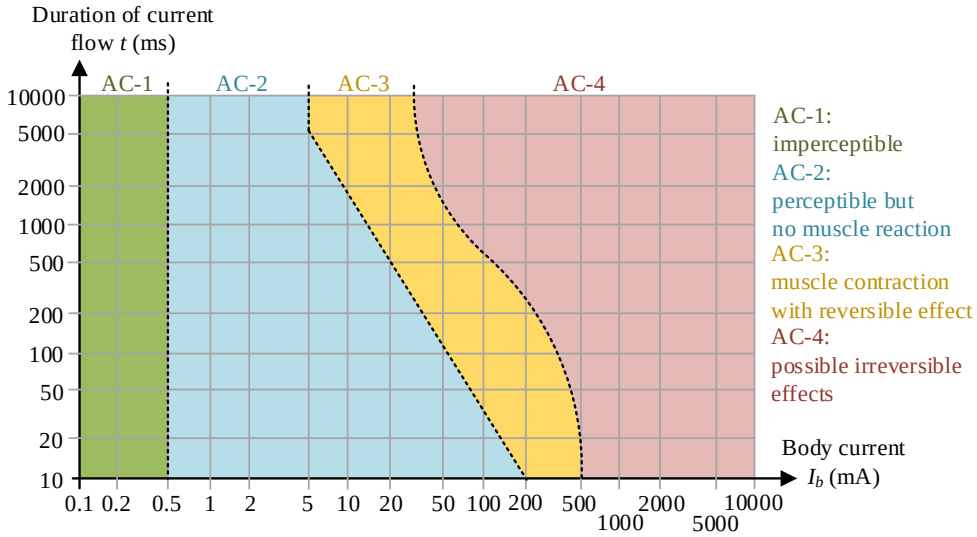


Fig.1−3. Effect of touch current to human body.

TABLE 1−1. IEC 60950 STANDARD[6]

Equipment	Condition	Leakage current limit (mA_{rms})
All equipment	No protective ground	0.25
Handheld	Protective ground is present	0.75
Portable		3.5
Stationary		3.5

1 shows the maximum leakage current allowed according to the standard IEC60950. It can be seen that the touch current is limited to 0.25 mA for the equipment without any protective ground connected to accessible parts. In medical equipment, stricter regulation is in place to protect patients from an electric shock. The standard for medical electrical equipment is IEC60601−1 [8]. In this standard, patient leakage current is restricted to 100 μA in AC and 10 μA in DC. Therefore, when

building medical equipment, limiting a leakage current is a highly critical issue. A more detailed explanation of IEC60601 is written in Appendix 1.

In conventional devices using magnetic coupling, the primary and secondary sides are electrically disconnected. Therefore, ideally, the touch current should be zero when the transformer is in place. However, the capacitor is often added between primary and secondary sides in many cases, as shown in Fig. 1-4, increasing the touch current. This capacitor is added to create a high-frequency current path and reduce the converter's EMI (Electromagnetic Interference). A Y-rated capacitor with more than 300 V rated voltage, and 5 kV instantaneous voltage is used for the user's safety since the failure of this capacitor may lead to an electric shock.

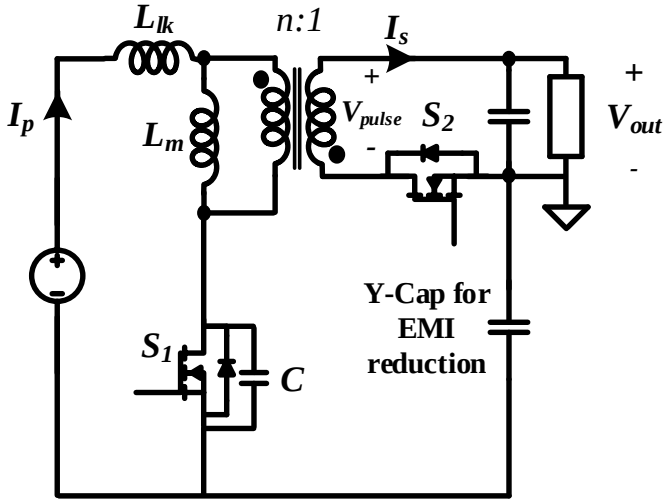
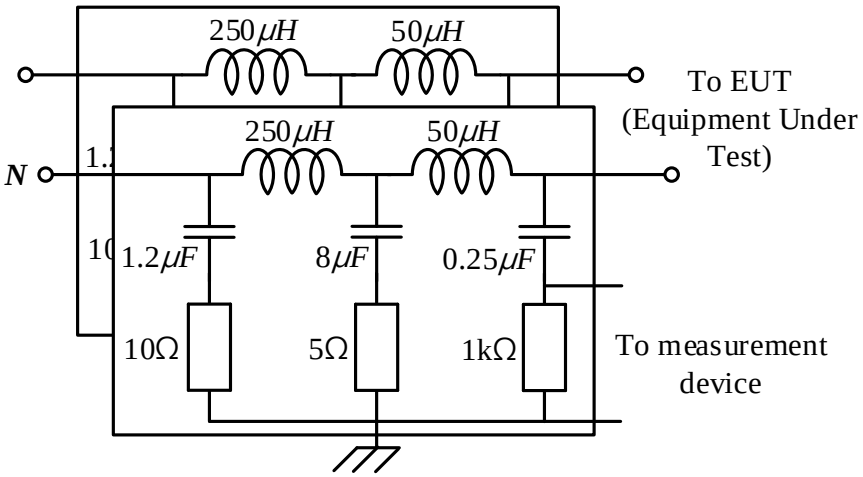


Fig. 1-4. Flyback converter with a Y-capacitor. The capacitor is used for reducing EMI of the converter.

(a)



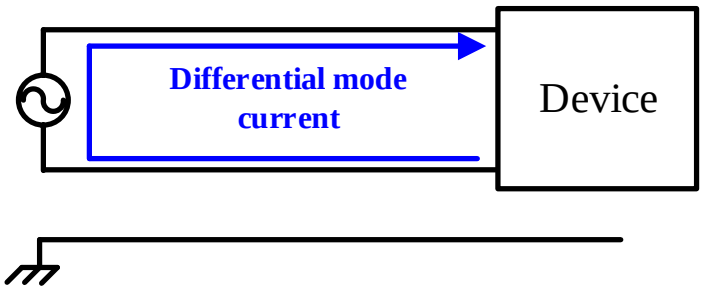
(b)

Fig. 1−5. Line Impedance Stabilization Network used for measuring conduction EMI (a) photo of LISN (b) circuit diagram.

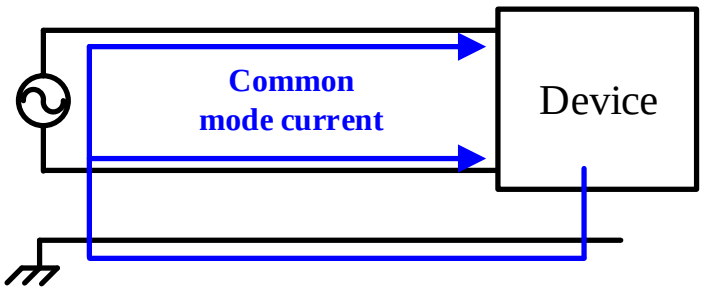
EMI regulations are also crucial when designing electronic devices connected to the AC grid. Every electronic device can radiate electromagnetic power that can impede other electronic devices from operating normally. Therefore, regulations such as

CISPR 22 restricts EMI caused by an electronic device. There are two different types of EMI to be considered. One is conduction EMI caused by high-frequency current traveling along the power line. This EMI is measured using LISN (Line Impedance Stabilization Network) shown in Fig 1-5, and frequency components between 150 kHz and 30 MHz are measured. This conduction EMI should not exceed the value shown in Fig. 1-6, where Class A is for a non-residential application, and Class B is for a residential application. Here both QP (quasi-peak) and AVG (average) values of EMI noise are restricted. Another type of EMI is radiated EMI measured using a radiation measuring probe. In most applications, radiated EMI is measured above 30 MHz. However, in some applications such as induction cooking equipment or wireless power transfer for an electric vehicle, where high radio-frequency energy is radiated, radiation EMI is also measured in frequency between 9 kHz and 30 MHz.

In most cases, the EMI filter is often designed using passive components to meet the EMI regulation. Since different EMI filter types are used for different EMI noises, the types and magnitude of EMI sources must be thoroughly analyzed. There are two EMI sources, a common-mode EMI and differential mode EMI, as shown in Fig. 1-7. It can be seen that differential-mode EMI is caused by a high-frequency current that flows on the same path as the supply current, while the high-frequency current across the Earth causes common-mode EMI. A typical EMI filter used in electronic devices is shown in Fig. 1-8. Each component has



(a)



(b)

Fig. 1-7. Current path of (a) Differential-mode current (b) Common-mode current.

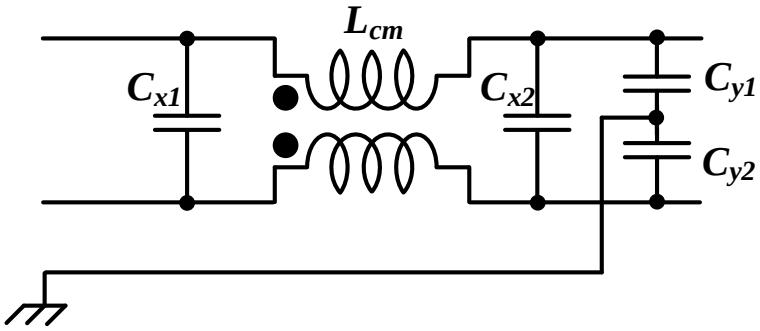


Fig. 1−8. Circuit of a typical EMI filter.

a different purpose for reducing overall EMI noises. Capacitor C_{x1} and C_{x2} are placed between two power supply lines and implemented to reduce the differential−mode EMI noise by creating a differential noise path. Typically, a capacitor with type X safety classification is placed between line−to−line. In order to mitigate common−mode EMI noise, common−mode choke L_{cm} is placed at a power supply line, and capacitors C_{y1} and C_{y2} are placed between the power supply line and Earth. A common−mode choke increases the impedance at the common−mode side, reducing the common−mode current. Capacitors across the power line and Earth create an additional common−mode noise path reducing the common−mode current flowing to the grid. Typically, a capacitor with type Y safety classification is placed between line−to−earth. For a two−wire system, a different EMI filter should be used since earth reference is not available. Therefore, instead of connecting a capacitor to Earth, Y−

capacitor is connected between DC/DC converter grounds, as shown in Fig. 1-4.

However, the addition of this Y-capacitor harms touch current. High-frequency current flows through the Y-capacitor instead of traveling to the power line, thereby reducing the conduction EMI of the electronic device. However, the addition of a Y-capacitor creates a touch current path and therefore increases the touch current. Thus, careful Y-capacitor selection is needed to reduce the EMI noises while ensuring leakage current is beyond the limit [11], [12]. Typically, few nano-Farad capacitors are used. Although this conventional method allows mitigation of both touch current and EMI noise, it also has some disadvantages. The most critical issue is the bulky size of magnetic components, especially in high switching frequency. Since high magnetic coupling between the primary and secondary sides is essential to transfer power efficiently, a large magnetic component is used, becoming a bottleneck for designing a high power density converter. Increasing switching frequency can reduce the size of the transformer; however, it has a limit due to a lack of a high-frequency magnetic component. In fact, at a frequency higher than 10 MHz, increasing the switching frequency increases the inductor's size since a larger size is

needed to dissipate the heat caused by core loss [21]. Air core inductor can be used instead, but it isn't easy to create high magnetic coupling with air core. Therefore, other means of isolation methods should be researched for high frequency and high-power density converter design.

1.2 Research Objective

In this research, isolated converter design using capacitive coupling is used to design high frequency and high-power density converters. A capacitor has an advantage in volume compared to a transformer, especially at the high switching frequency. In fact, many commercially available capacitors have high energy density compared to commercial air-core inductors [23].

A capacitive isolated converter is researched to replace the transformer in an isolated converter [24]-[28]. Most of the research, however, implements capacitive isolation where leakage current standard is not considered. Many researches focus on using capacitive isolation for stacking and building input parallel output series (IPOS) converter [24] – [26]. In these applications, a capacitor as large as a few μF is used, which is beneficial for transferring high power efficiently but cannot be

used in an application where leakage current standard should be met. Some research has also considered the safety and touch current limitation of capacitive isolated converter [27], [28]. In these researches, Y-capacitor is used for isolation to meet isolation voltage standards. However, the high-frequency common-mode current responsible for conduction EMI noise is not seriously considered in previous researches. Instead, a simple common-mode filter is added to remove common-mode noise. Therefore, this paper analyzes sources of common-mode current and proposes the common-mode current mitigation method in the capacitive isolated converter to meet the touch current and conduction EMI regulation.

1.3 Thesis Composition

In this paper, common-mode current in the capacitive isolated converter is studied. In section 2, capacitive isolated converter design to regulate touch current is studied. Maximum allowed capacitance is defined to restrict a touch current that satisfies safety regulations. Also, the class E inverter and class E rectifier operation are analyzed to calculate the high-frequency common-mode current. In section 3, common-mode current in capacitive isolated class E converter with LC series

network is calculated, and balanced class E converter is proposed to reduce common-mode current. In section 4, a capacitive isolated class E converter with a T-model-based network for different input to output voltage gain is analyzed. Similarly, the common-mode current is calculated, and the conduction EMI of a balanced class E converter with a T-model-based network is measured. In section 5, a self-powered gate driver circuit to operate a balanced class E converter is proposed.

2. Capacitive Isolated Converter Design

2.1 Modeling of Capacitive Isolated Converter

Three sources create a common mode current in the capacitive isolated converter shown in Fig.2−1. One is AC grid (V_g), and the other two are high−frequency inverter (V_{inv}) and rectifier (V_{rec}) in DC/DC converter. AC grid voltage V_g is low frequency (around 50 – 60 Hz) while frequency of V_{inv} and V_{rec} depends on switching frequency of DC/DC converter, which can go up to a few MHz in high frequency switching converters. Typically, V_g creates touch current, and V_{inv} and V_{rec} are responsible for conduction EMI noise.

First, capacitor values C_{r1} and C_{r2} will be decided by assuring the grid frequency component of the common−mode current to satisfy the touch current standard. Since capacitors C_{r1} and C_{r2}

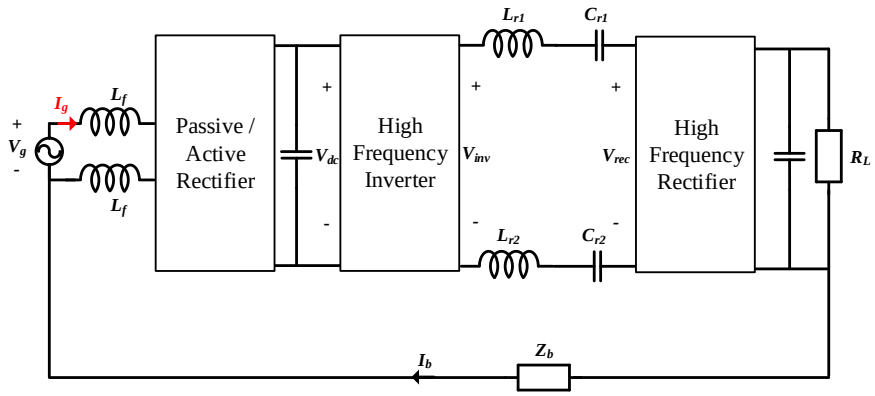


Fig. 2−1. Block diagram of a capacitive isolated DC/DC converter

have high impedance at grid frequency, low-frequency touch current can easily be reduced by adjusting the capacitance value. Then switching frequency f_{sw} is decided that is suitable to transfer power with capacitor C_{r1} and C_{r2}. For a high-frequency common-mode current, the impedance of C_{r1} and C_{r2} is too low and therefore needs an alternative common mode current reduction method. In this paper, a balanced converter design [35]-[39] is implemented to reduce high-frequency common-mode current.

2.2 Grid Frequency Component Analysis

First, the grid frequency component is analyzed. If PFC (Power factor correction) is used as an active rectifier, grid current I_g is a continuous sinusoidal wave. In this case, Fig. 2-1 can be redrawn to Fig. 2-2(a), where other frequency voltage sources V_{inv} and $V_{rec,}$ are set to zero to analyze only low-frequency common-mode current. Since I_g is a sinusoidal wave in phase with grid voltage V_g, V_{ac} is a half-wave sine waveform where the Fourier transform equation is

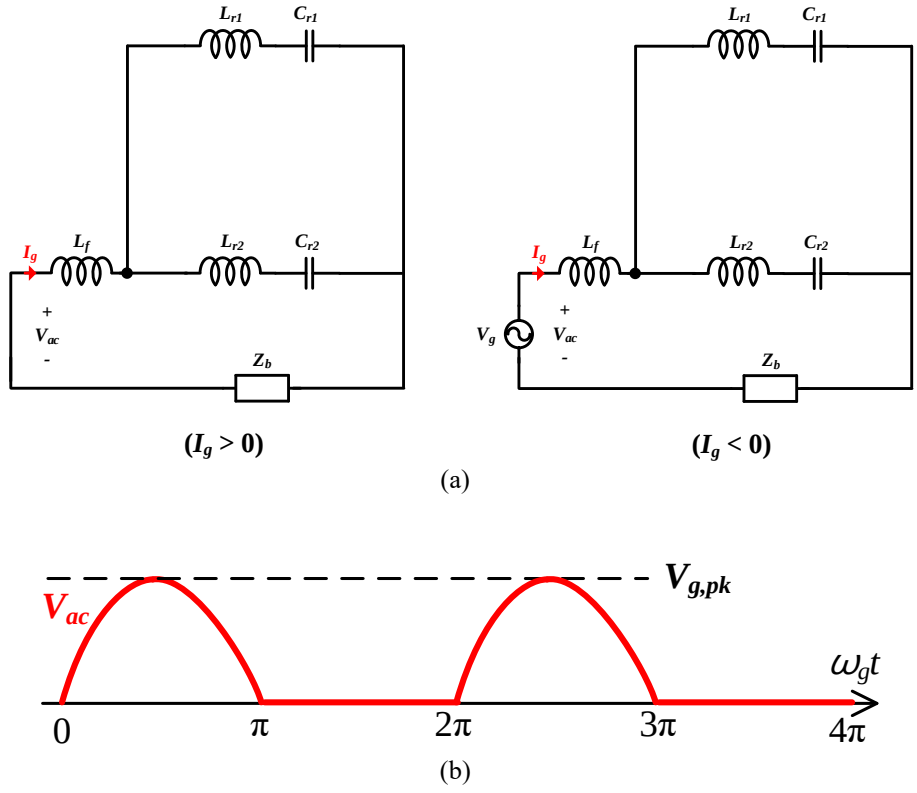
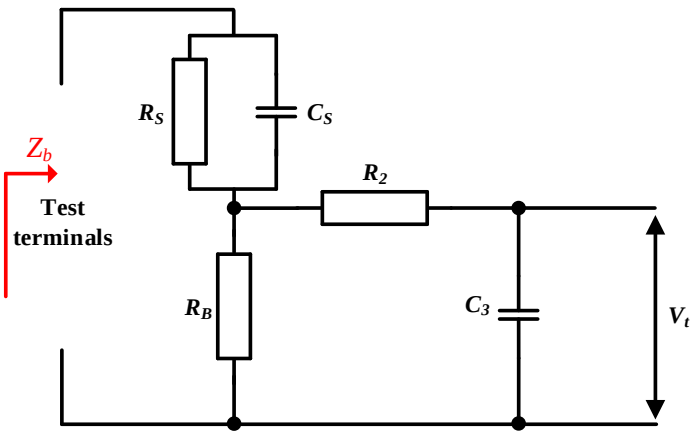


Fig. 2-2. Grid frequency modeling of the capacitive isolated converter (a) equivalent circuit depending on the direction of I_g (b) voltage waveform of V_{ac}

$$V_{ac} = V_{g,pk}\left\{\frac{1}{\pi} + \frac{1}{2}\sin(\omega_g t) - \frac{2}{\pi}\sum_{n=1}^{\infty}\left(\frac{1}{4n^2-1}\cos(2n\omega_g t)\right)\right\}, \quad (2-1)$$

where $V_{g,pk}$ is a peak grid voltage, and ω_g is a grid frequency. To calculate the leakage current with the above V_{ac}, body impedance Z_b is required.

The circuit used to measure the touch current of IT equipment according to the IEC 60990 standard is shown in Fig. 2-3. One side of the test terminal is connected to the load, and the other is connected to the Earth. From the test terminal side, body impedance Z_b is around 2000 Ω at low frequency (<< 480 Hz) and 500 Ω at high frequency (>>480 Hz), as shown in Fig.



R_S = 1500 Ω, R_B = 500 Ω
C_s = 220 nF, C_3 = 22 nF, R_2 = 10000 Ω

Fig. 2-3. Body impedance model circuit diagram in IEC 60990

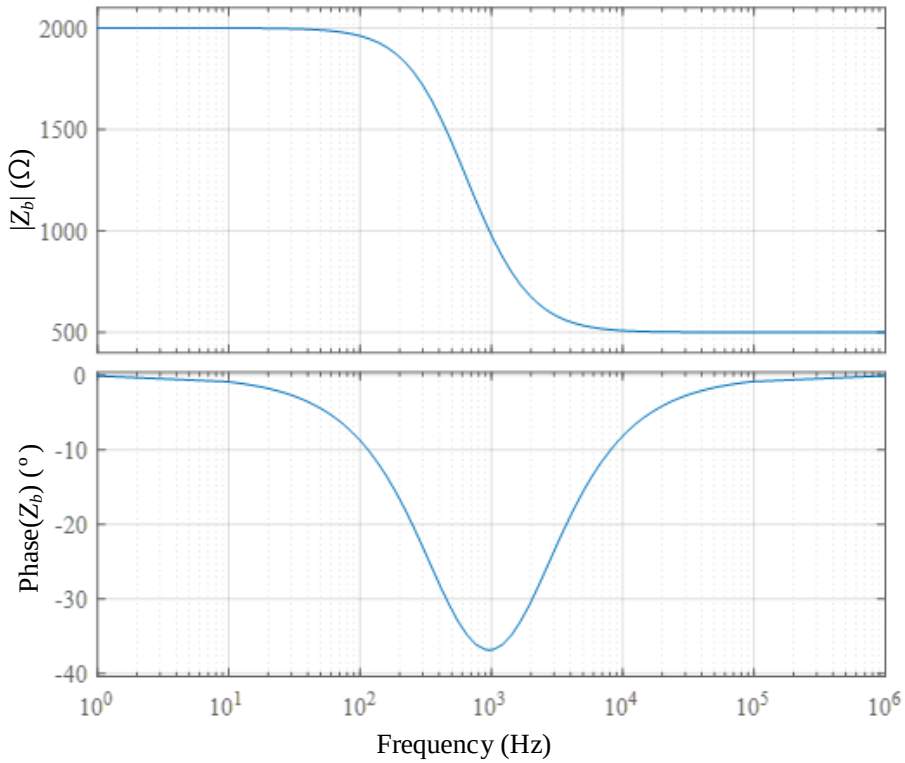


Fig. 2−4. Bode plot of body impedance model.

2−4. The validity of this body impedance model has been widely studied to accurately measure the touch current [39]−[41]. In [41], the body impedance model in IEC 60990 is compared with the impedance of the actual body measured (from hand to foot) using an impedance analyzer. The effect of skin condition (dry or wet), gender (male or female), ground insulation (with shoes or bare feet), and contact with a device (with a finger or fully grasp) are compared. According to work in [41], the impedance of the body is lowest when the impedance of a male body is measured with wet skin and barefoot while fully grasping the measuring device. The measured lowest impedance is compared

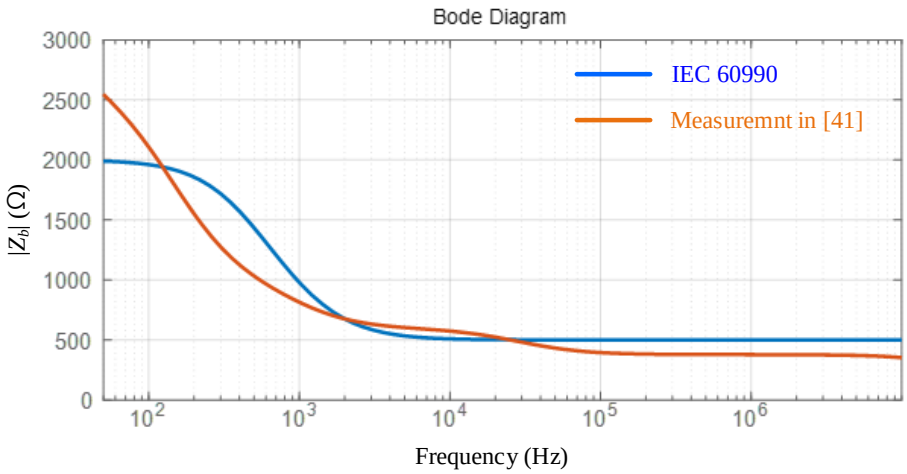


Fig. 2-5. Impedance magnitude comparison between a body impedance model in IEC 60990 and measurement in [41]

with the body impedance model from IEC 60990 in Fig. 2-5. At 50 Hz, the measured body impedance in [41] is 2530 Ω, while the body impedance model from IEC 60990 is 2000 Ω at 50 Hz. At 10 MHz, the measured body impedance is 356 Ω, while the body impedance model from IEC 60990 is 500 Ω. Although the model from IEC 60990 has some errors compared to actual measurement, it is helpful due to its simple structure. A more complex body impedance model is proposed in [40] and [41] if a highly accurate touch current should be measured.

In this paper, the impedance model from IEC 60990 will be used to measure the touch current. Using equation (2-1), leakage current can be calculated. Assuming inductor L_r and L_f have low impedance at low-frequency touch current, I_g can be calculated as

$$|I_{g,rms}|^2 = \frac{V_{g,pk}{}^2(\omega_g C_r)^2}{8}\left[g(1) + \frac{16}{\pi^2}\sum_{n=1}^{\infty}\left\{\left(\frac{2n}{4n^2-1}\right)^2 g(n)\right\}\right], \qquad (2-2)$$

$$g(n) = \left(1 + n^2\omega_g{}^2 C_r{}^2 R_B{}^2 \frac{n^2\omega_g{}^2 C_s{}^2 R_s{}^2}{1 + n^2\omega_g{}^2 C_s{}^2 R_s{}^2}\right)^{-1}.$$

where $C_r = C_{r1} + C_{r2}$. Here touch current $I_{g,rms}$, should be smaller than 0.25 mA_{rms} to meet the standard IEC60950. The condition $I_{g,rms} < 0.25\ mA_{rms}$ is satisfied when C_r is small enough to block leakage current. Using parameters from Fig. 2-3 and setting grid frequency to 60 Hz, it can be seen that $g(n) < 1$ for all n values. Therefore, if C_r satisfies the below inequality equation, touch current standard is satisfied.

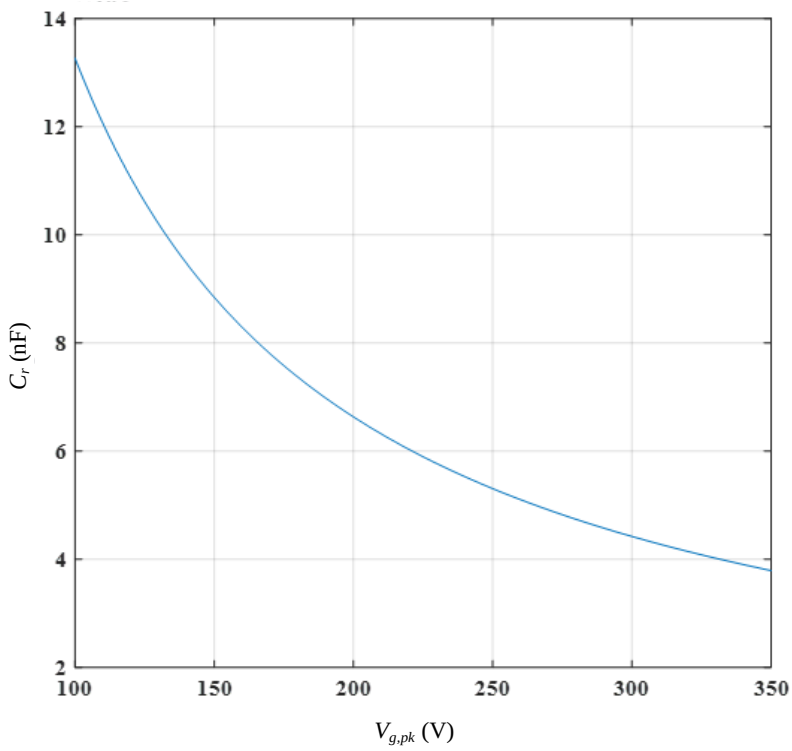


Fig. 2-6. Maximum capacitance allowed for meeting touch current regulation

$$I_{g,rms} < \sqrt{\frac{{V_{g,pk}}^2 \left(\omega_g C_r\right)^2}{8}\left[1+\frac{16}{\pi^2}\sum_{n=1}^{\infty}\left(\frac{2n}{4n^2-1}\right)^2\right]} < I_{TC,\max} . \quad (2-3)$$

$$C_r < \frac{I_{TC,\max}}{\sqrt{\frac{{V_{g,pk}}^2 \omega_g^{\,2}}{8}\left[1+\frac{16}{\pi^2}\sum_{n=1}^{\infty}\left(\frac{2n}{4n^2-1}\right)^2\right]}} \cong \frac{2I_{TC,\max}}{\omega_g V_{g,pk}} \quad (2-4)$$

where $I_{TC,max}$ is a maximum touch current of the system. Setting maximum touch current to 0.25 mA, the maximum value of C_r that satisfies touch current limitation for different AC grid voltage values is shown in Fig. 2-6. When peak AC grid voltage is 350 V, C_r should be smaller than 3.8 nF to reduce the touch current below 0.25 mA.

Next, switching frequency is decided to design a converter that can effectively transfer power with above C_{r1} and C_{r2} value. The capacitor is connected in parallel for common-mode while the capacitor is connected in series in differential mode. Thus, a differential mode equivalent circuit can be drawn as Fig. 2-7(b). Setting C_r = 3.3 nF, the maximum value C_{diff} can have is $C_r/4$ = 825 pF when $C_{r1} = C_{r2}$. Assuming the switching frequency is 1 MHz, the inductance L_{diff} required to set the resonant frequency at 1 MHz is 30 μH, which is too large a value for designing a high

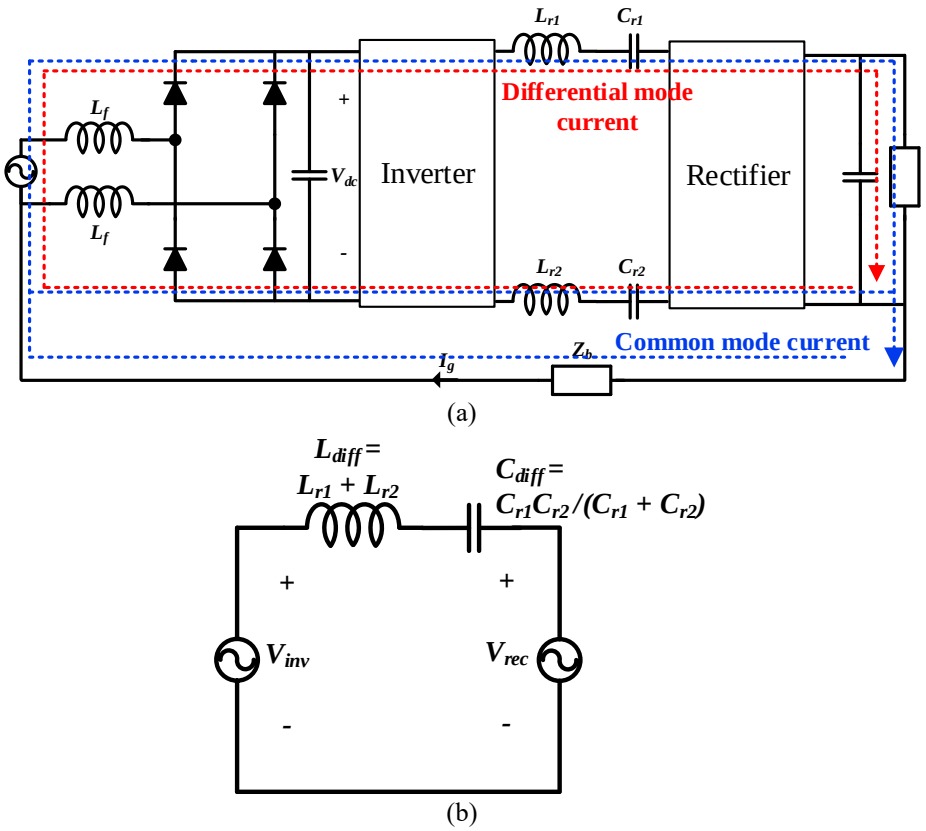


Fig. 2-7. Capacitive isolated converter (a) Direction of differential-mode and common-mode currents (b) Differential-mode equivalent circuit

power density DC/DC converter. In this dissertation, switching frequency is decided considering the volume of the resonant inductor. According to [23], the volume of an inductor has a strong relationship with maximum stored energy defined as $LI_{rms,\max}^{2}$ where L is an inductance and $I_{rms,max}$ is a root mean square value of the rated current of the inductor defined in the datasheets. Fig. 2-8 shows the volume versus maximum stored energy of commercial air-core inductors. An air-core inductor is used due to the high core loss of magnetic core material when switching frequency is higher than a few megahertz [21]. Using

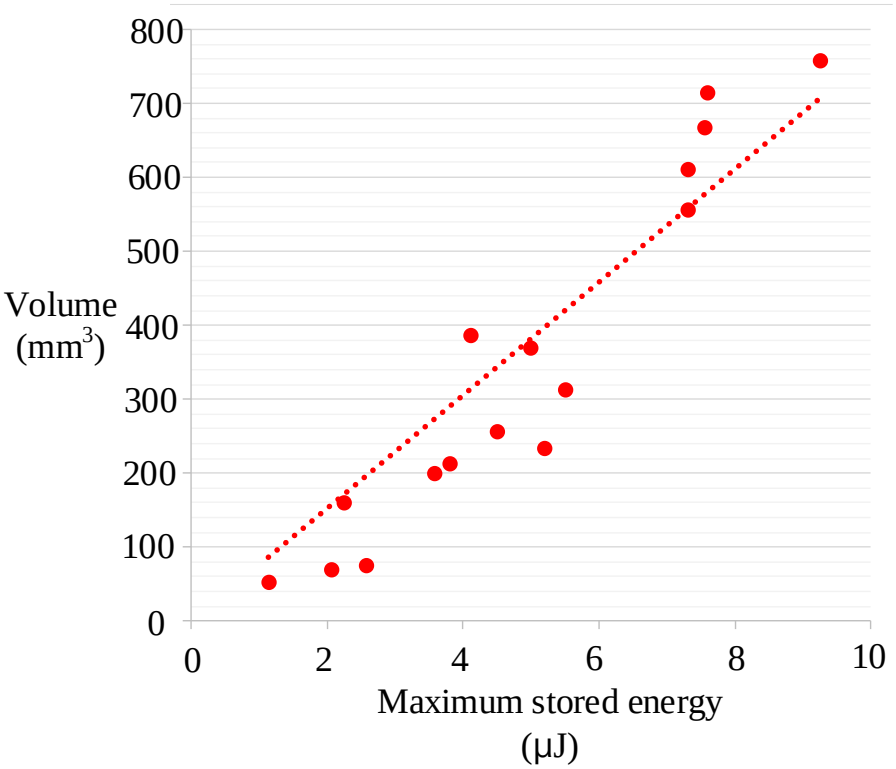


Fig. 2-8. Volume of a commercial air-core inductor depending on the maximum inductor stored energy

this plot, the size of the air-core inductor can be roughly estimated if an inductance and rated current are given. For comparison, the size of the transformer in a laptop charger is found. For the 40 W laptop charger shown in Fig. 1-2, RM 8 size transformer ferrite core is used. The size of this transformer is roughly 4800 mm^3. In a laptop charger from FINSIX, RM 6 size transformer ferrite core is used, which is 2000 mm^3 in size. In a capacitive isolated converter topology, multiple inductors and capacitors are used to create a resonant current. Therefore, the size of the inductor should be much smaller than the conventionally used transformer to design a high power density isolated converter. If the size of the inductor is set to 500 mm^3, then the rough estimation of maximum stored energy is 6.67 μJ. The current rating depends on the nominal output power of the isolated converter, input voltage, and topology of the converter.

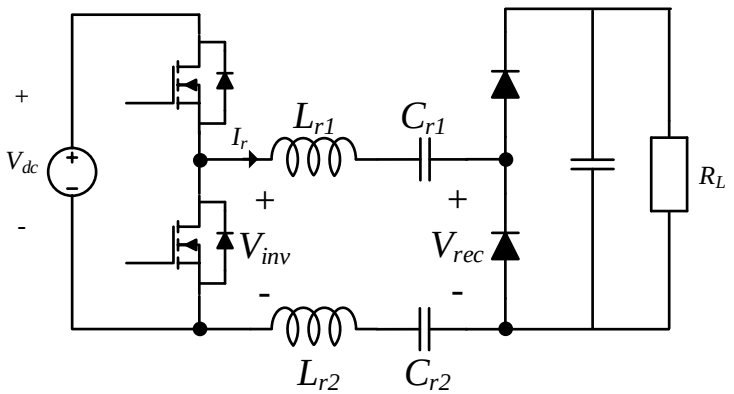


Fig. 2-9. Capacitive isolated series resonant converter.

For instance, assuming a simple 65 W SRC (series resonant converter) with half-bridge inverter and 100 V input voltage (V_{dc}) as shown in Fig. 2-9. Then maximum fundamental input voltage across the series network is $V_{inv,1} = 2V_{dc}/\pi = 64$ V, where $V_{inv,1}$ is a fundamental component of half-bridge inverter output voltage. Then, the resonant current I_r can be calculated as $I_r = 2P_o/V_{inv,1} = 2.04$ A. If this current value is set as a rated current of the inductor, the maximum inductance in the series network considering maximum stored energy can be calculated as $L_{diff,max} = 3.2$ μH. Using this inductance value, the minimum switching frequency required can be calculated as

$$f_{sw} > \frac{1}{2\pi\sqrt{L_{diff}C_{diff}}} = 3.1 \text{ MHz}. \qquad (2-5)$$

Although the maximum inductance value will differ from the converter's topology and rated output power, this value gives a rough estimation. It can be seen from the equation, converter topology suitable for high-frequency switching with more than a few MHz should be used to design a capacitive isolated converter that can satisfy the leakage current standard.

2.3 High-Frequency Converter Topology

For switching frequency higher than few megahertz, switching losses become a dominant cause of efficiency reduction. Therefore, in high frequency, converter topology with low switching losses is often chosen. A resonant converter is one of the most widely used converters for high-frequency switching. A resonant converter can achieve ZVS (zero voltage switching) using resonant current, reducing the switching losses dramatically. There are two types of resonant converter, a bridge-type resonant converter and a single-ended type resonant converter, as shown in Fig. 2-10. A bridge-type uses a half-bridge or full-bridge inverter combined with a resonant network and rectifier. Using a resonant current, the charge stored in the output capacitor C_1 and C_2 of switches are transferred during a dead-time. When charges are fully

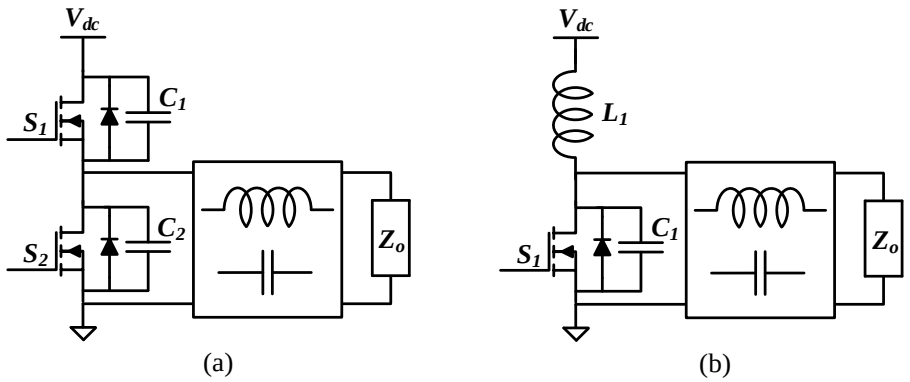


Fig. 2-10. High frequency inverter topology (a) bridge type (b) single-ended type

transferred during a converter, a switch can be turned on when the voltage across the switch is zero achieving ZVS. Therefore, this topology is widely used when switching frequency is around a few hundred kHz to a few MHz. However, this bridge-type resonant converter has some limitations for operating at a higher switching frequency. First, the dead time effects required for achieving ZVS are more severe at high frequency [64]. Since the dead time needed for ZVS is fixed if the resonant current magnitude is unchanged, the proportion of time when both switches are off becoming more prominent as the switching period decreases. This dead time effects result in smaller inverter output voltage affecting the output power. To reduce the dead time, a larger resonant current is required; however, this increases conduction losses. Also, a precise gate signal is required for driving multiple switches in the bridge-type inverter. In order to accurately control the dead time to achieve ZVS, exact gate signaling is necessary. This requires a high resolution and low jitter gate signaling device, making it challenging to operate at high frequency.

For these reasons, a single-ended converter shown in Fig. 2-10 (b) is preferred when the switching frequency is higher than a few MHz. Since it only has one switch, the dead time effect

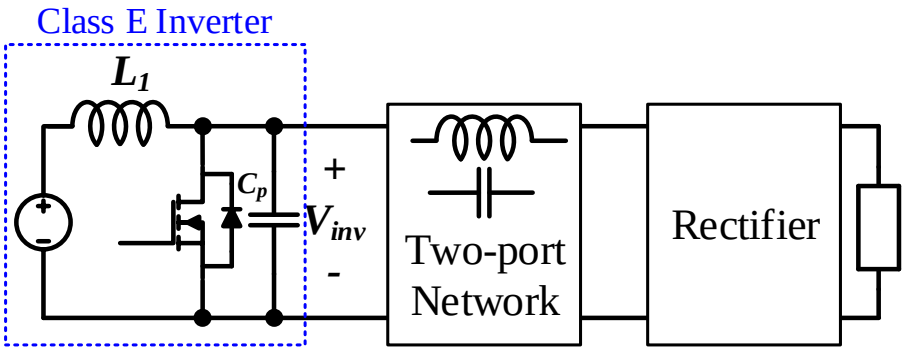


Fig. 2-11. Basic structure of class E DC/DC converter

does not need to be considered, simplifying the gate drive circuit. Also, since it has an inductor placed between the input voltage source and drain of the switch S_1, it can absorb any parasitic inductance between an input voltage source and switch, reducing the possible effect of parasitic components. Due to these advantages, a single-ended type converter, class E converter, in particular, is chosen as a topology for this paper.

The basic structure of a class E converter is shown in Fig. 2-11. Followed by the class E inverter, a two-port network composed of passive components is placed. A simple LC series network is placed for a class E converter with the same input and output voltage value. A rectifier is then connected to transform high-frequency power to DC. Typically, a half-bridge rectifier or class E type rectifier is used, as shown in Fig. 2-12. While a half-bridge rectifier is simple and requires diodes with less

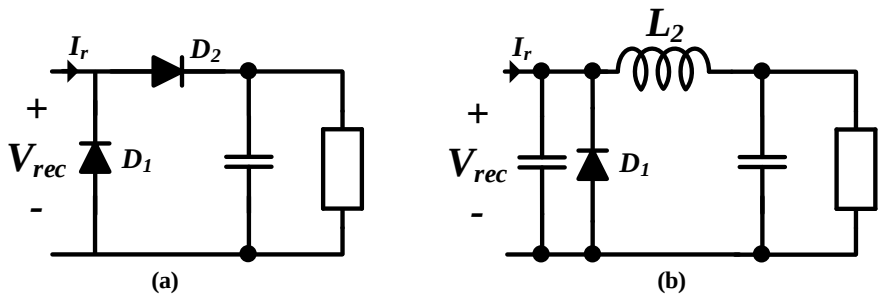


Fig. 2-12. High frequency rectifier topology (a) class D (b) class E

voltage stress, a class E type rectifier creates less EMI noise and less transition loss. In this paper, a class E type rectifier is used to reduce high-frequency common-mode current. The basic operation and analysis of the class E converter are explained in the next section.

2.3.1 Class E Converter Operation

The operation of the class E converter can be divided into two modes, as shown in Fig. 2-13. The voltage and current waveforms at each mode during the steady-state are demonstrated in Fig. 2-14. Here D is the duty ratio of the converter, and T_s is the switching period. It is assumed that the network contains LC series network with high Q, and therefore, current I_r is sinusoidal. In mode I, switch S_1 is turned on, increasing the input current I_s. At this mode, the voltage across the switch S_1 is zero. In mode II, switch S_1 is turned off, increasing the voltage across the switch. At this mode, input current I_s stored at inductor L_1 charges capacitor C_1 placed across the switch. The voltage V_{S1} continually increases until inductor current I_s reaches resonant current I_r. V_{S1} is at its maximum when I_s equals I_r. After this point, resonant current I_r is larger than

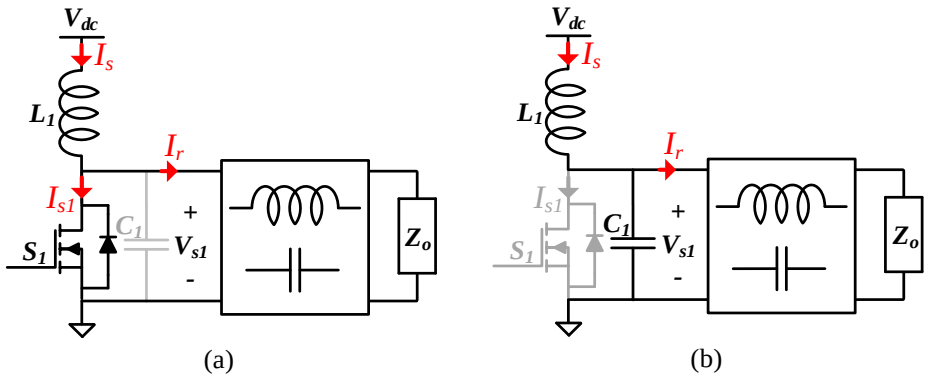


Fig. 2-13. Operation of a class E inverter (a) switch S_1 on (b) switch S_1 off

inductor current I_s, discharging the capacitor C_1. If C_1 is fully discharged before the switch is turned on, ZVS (zero voltage switching) is achieved, eliminating switching loss. In addition to the ZVS condition, the derivative of switch voltage dv/dt at switch turn on is also an essential condition when designing a class E converter. Fig. 2-15 shows the voltage and current waveforms when dv/dt is smaller than zero, and dv/dt equals zero. When dv/dt

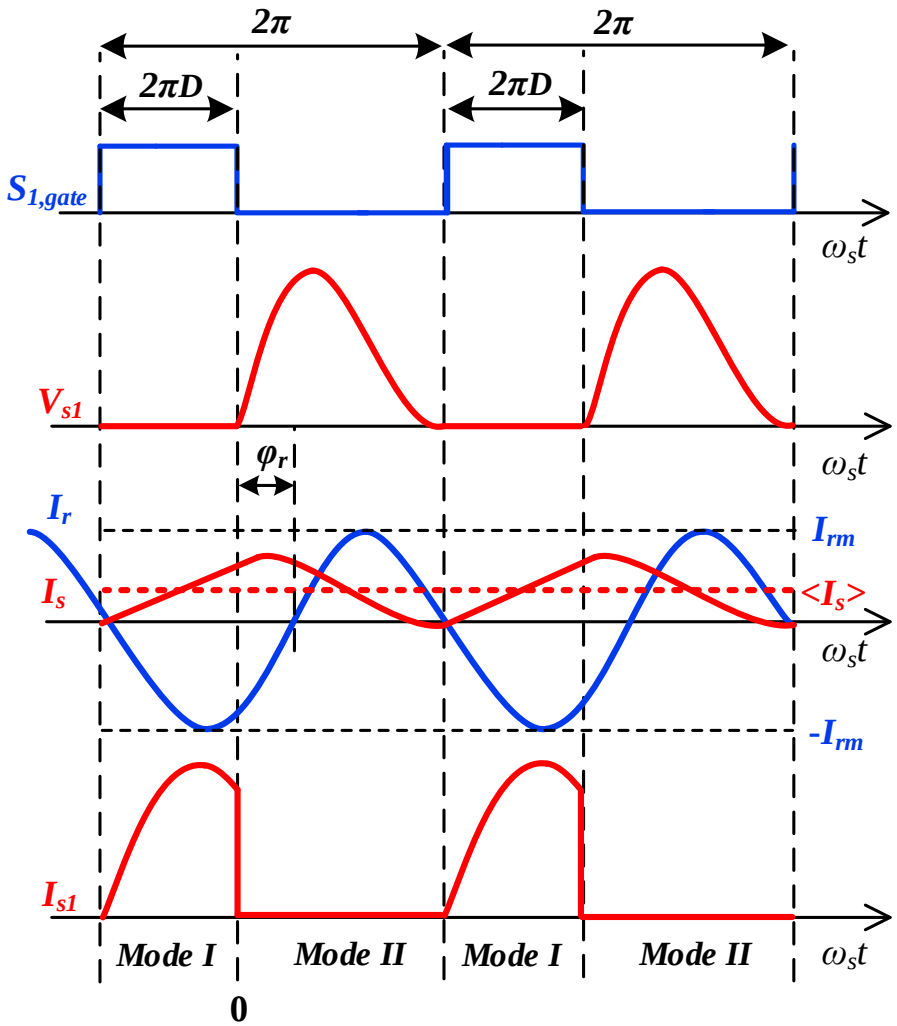


Fig. 2-14. Voltage and current waveforms of a class E inverter

is smaller than zero, negative current flows through the switch S_1. At this point, the body diode of switch S_1 starts conducting. Since the body diode of GaN MOSFET typically has poor conduction performance, reducing time when the body diode is conducting is vital for increasing the efficiency of the class E converter. Thus, many class E converter is designed to achieve ZVS, and dv/dt equals zero.

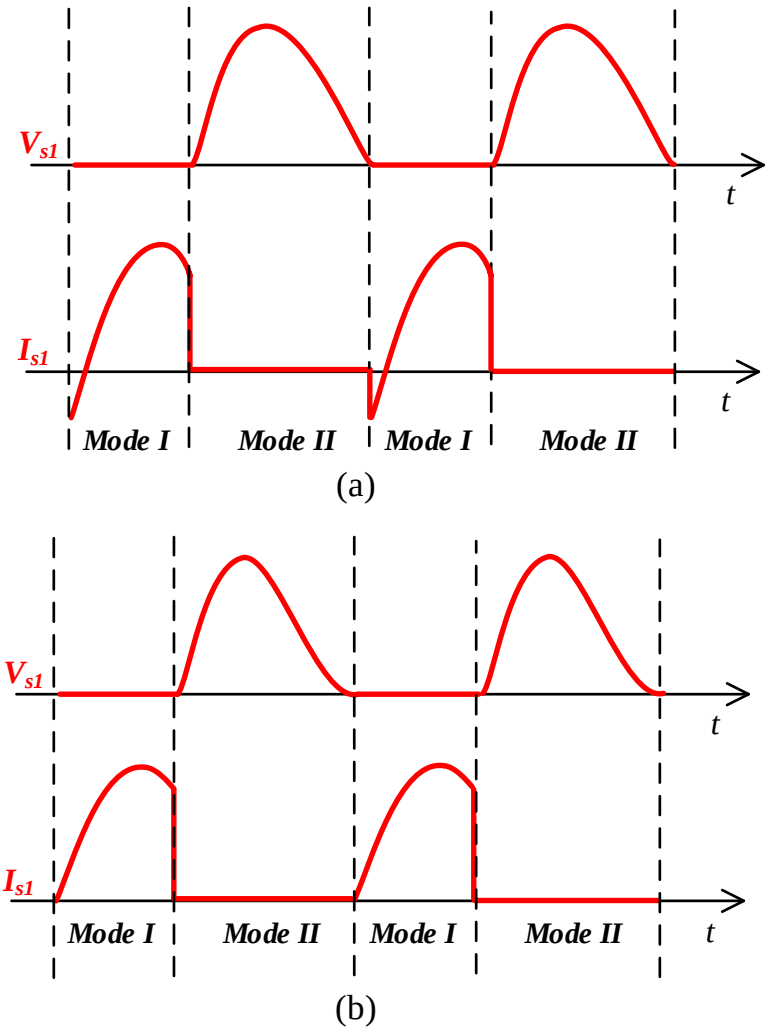


Fig. 2-15. Class E inverter voltage and current waveforms when (a) $dv/dt < 0$ (b) $dv/dt = 0$

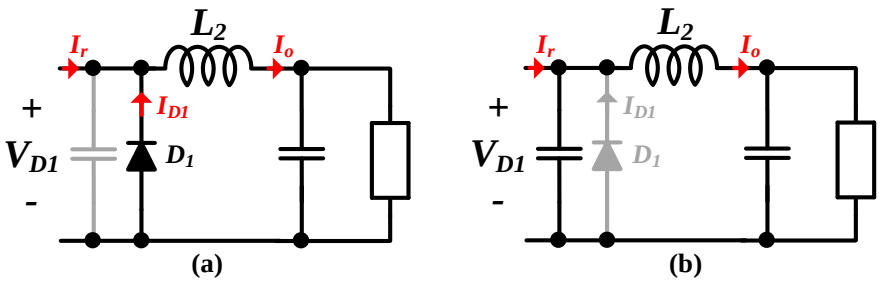


Fig. 2-16. The operation of class E rectifier (a) Mode I diode D_1 turn on (b) Mode II diode D_1 turn off.

The operation of the class E rectifier is also divided into two modes, as shown in Fig. 2-16. In mode I, the diode conducts the current reducing the current I_o. When diode current I_{D1} reaches zero, the diode stops conducting, increasing the voltage across the diode V_{D1}. The voltage and current waveforms of the

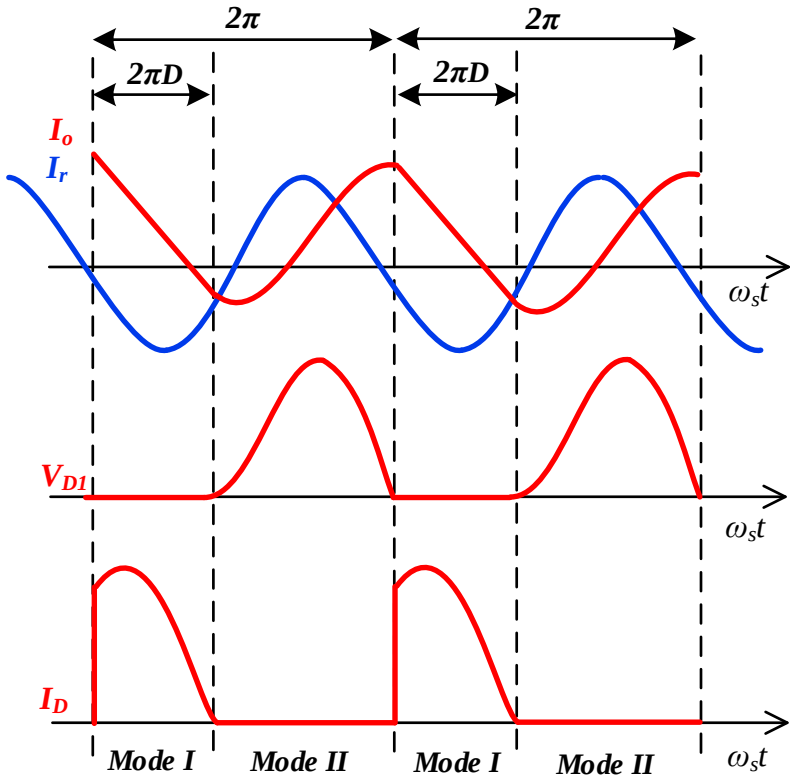


Fig. 2-17. Voltage and current waveforms of class E rectifier

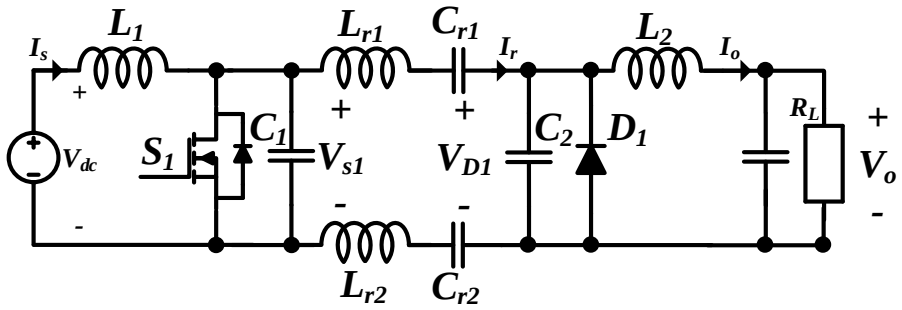


Fig. 2-18. Capacitive Isolated class E DC/DC converter

class E diode are shown in Fig. 2-17. A class E converter with both class E inverter and class E rectifier with a simple LC series network is shown in Fig. 2-18.

2.3.2 Inverter and Rectifier Voltage Analysis

In this section, the voltage across the active component of the converter V_{S1} and V_{D1} are calculated. These values will be later used to estimate the common-mode current. Since many factors affect the switch voltage V_{S1}, some constraints are made to analyze the switch voltage according to duty ratio. First, to simplify the calculation, it is assumed that resonant current I_r is sinusoidal, and other harmonic terms are neglected.

$$I_r = I_{rm}\sin(\omega_s t + \varphi_r)\,. \qquad (2-6)$$

Here I_{rm} is the magnitude, and φ_r is a phase of resonant current as depicted in Fig. 2-14. Also, switch voltage when ZVS and dv/dt equals zero conditions are both satisfied will be calculated.

In mode II, V_{S1} and I_s can be written as

$$\begin{cases} L_1\dfrac{dI_s}{dt} = V_{dc} - V_{S1} \\ C_1\dfrac{dV_{S1}}{dt} = I_s - I_{rm}\sin(\omega_s t + \varphi_r) \end{cases} \qquad 0 < \omega_s t \le 2\pi(1-D)\,. \quad (2-7)$$

After solving the above differential equations, V_{S1} can be rewritten as

$$V_{S1} = V_{dc} - V_{dc}\cos(\omega_1 t) - \frac{Z_1 I_{rm}(\omega_1/\omega_s)\sin(\varphi_r)}{1+(\omega_1/\omega_s)}\sin(\omega_1 t) + Z_1 I_s(0)\sin(\omega_1 t) + \frac{Z_1 I_{rm}(\omega_1/\omega_s)}{1-(\omega_1/\omega_s)^2}\{\cos(\omega_s t + \varphi_r) - \cos(\omega_1 t + \varphi_r)\}\,, \quad (2-8)$$

where $\omega_1 = 1/\sqrt{L_1 C_1}$ and $Z_1 = \sqrt{L_1/C_1}$. Using equations (2-7) and (2-8), I_s can be expressed as

$$I_s = \frac{V_{dc}}{Z_1}\sin(\omega_1 t) - \frac{(\omega_1/\omega_s) I_{rm}\sin(\varphi_r)}{1+(\omega_1/\omega_s)}\cos(\omega_1 t) + I_s(0)\cos(\omega_1 t) + \frac{I_{rm}(\omega_1/\omega_s)}{1-(\omega_1/\omega_s)^2}\{\sin(\omega_1 t+\varphi_r) - (\omega_1/\omega_s)\sin(\omega_s t+\varphi_r)\} \quad , \quad (2-9)$$

To achieve zero voltage switching (ZVS) and $dv/dt = 0$ conditions, V_{S1} should be zero, and I_s should equal to I_r at switch turn-on. Then following equations can be derived

$$1-\cos(B) - \frac{\omega_{1,n} K\sin(\varphi_r)}{1+\omega_{1,n}}\sin(B) + \frac{Z_1 I_s(0)}{V_{dc}}\sin(B) + \frac{K\omega_{1,n}}{1-\omega_{1,n}^2}\{\cos(A+\varphi_r) - \cos(B+\varphi_r)\} = 0 \quad , \quad (2-10)$$

$$\sin(B) - \frac{\omega_{1,n} K\sin(\varphi_r)}{1+\omega_{1,n}}\cos(B) + \frac{Z_1 I_s(0)}{V_{dc}}\cos(B) + \frac{K\omega_{1,n}}{1-\omega_{1,n}^2}\{\sin(B+\varphi_r) - \omega_{1,n}\sin(A+\varphi_r)\} = 0 \quad , \quad (2-11)$$

where $\omega_{1,n} = (\omega_1/\omega_s), A = 2\pi(1-D), B = 2\pi\omega_{1,n}(1-D), K = Z_1 I_{rm}/V_{dc}$.

At mode I, the switch is turned on, and the voltage across the switch equals zero if the ideal switch is assumed. Therefore, V_{S1} and I_s can be written as

$$\begin{cases} L_1 \dfrac{dI_s}{dt} = V_{dc} \\ V_{S1} = 0 \end{cases} \qquad 2\pi(1-D) < \omega_s t \le T_s . \quad (2-12)$$

Solving the above differential equation, I_s can be expressed as

$$I_s = \frac{V_{dc}}{\omega_1 L_1}(\omega_1 t - B) + I_{rm}\sin(A+\varphi_r) \qquad (2-13)$$

where it is assumed that I_s is equals to $I_{rm}\sin(A+\varphi_r)$ at $\omega_s t = 2\pi(1\text{-}D)$ to achieve dv/dt = 0 condition. Also, assuming a steady-state operation, $I_s(T_s)$ should be equals to $I_s(0)$. Therefore, according to equation (2-13)

$$I_s(0) = \frac{V_{dc}}{Z_1}(2\pi\omega_{1,n} - B) + I_{rm}\sin(A+\varphi_r)\,. \qquad (2-14)$$

Using above equations (2-10), (2-11) and (2-14), φ_r and K according to D and $\omega_{1,n}$ can be calculated as

$$\tan(\varphi_r) = -\frac{n(D,\omega_{1,n})}{d(D,\omega_{1,n})} \qquad (2-15)$$

$$n(D,\omega_{1,N}) =$$
$$\left(\sin(B) + (2\pi\omega_{1,N} - B)\cos(B)\right)\left[\sin(A)\sin(B) - \frac{\omega_{1,N}\left(\cos(A)-\cos(B)\right)}{1-{\omega_{1,N}}^2}\right] -$$
$$\left(1-\cos(B) + (2\pi\omega_{1,N} - B)\sin(B)\right)\left[\sin(A)\cos(B) - \frac{\sin(A)-\omega_{1,N}\sin(B)}{1-{\omega_{1,N}}^2}\right]$$

$$d(D,\omega_{1,N}) =$$
$$\left(\sin(B) + (2\pi\omega_{1,N} - B)\cos(B)\right)\left[\cos(A)\sin(B) - \frac{\omega_{1,N}\sin(B)}{1+\omega_{1,N}} - \frac{\omega_{1,N}\left(\sin(A)-\sin(B)\right)}{1-{\omega_{1,N}}^2}\right] -$$
$$\left(1-\cos(B) + (2\pi\omega_{1,N} - B)\sin(B)\right)\left[\cos(A)\cos(B) - \frac{\omega_{1,N}\cos(B)}{1+\omega_{1,N}} - \frac{\cos(A)-\omega_{1,N}\cos(B)}{1-{\omega_{1,N}}^2}\right]$$

$$K = \frac{-\left(\sin(B) + 2\pi\omega_{1,N} D\cos(B)\right)}{\sin(A+\varphi_r)\cos(B) - \frac{\omega_{1,N}\cos(B)\sin(\varphi_r)}{1+\omega_{1,N}} - \frac{\sin(A+\varphi_r) - \omega_{1,N}\sin(B+\varphi_r)}{1-{\omega_{1,N}}^2}} \qquad (2-16)$$

Using the above equations, fundamental and harmonic components of the output voltage of class E inverter V_{S1} can be

calculated. Here $V_{S1,n}$ is defined as an n^{th} harmonic term of V_{S1}. Then $V_{S1,n}$ can be written as

$$\begin{aligned} V_{S1,n}(t) &= \left|V_{S1,n}\right| \sin(n\omega_s t + \varphi_r + \psi_n) \\ &= \left|V_{S1,n}\right|_{\sin} \sin(n\omega_s t + \varphi_r) + \left|V_{S1,n}\right|_{\cos} \cos(n\omega_s t + \varphi_r) \end{aligned} \quad (2-17)$$

where $\left|V_{S1,n}\right| = \sqrt{\left|V_{S1,n}\right|_{\cos}^{\ 2} + \left|V_{S1,n}\right|_{\sin}^{\ 2}}$ and $\tan(\psi_n) = \left|V_{S1,n}\right|_{\sin} / \left|V_{S1,n}\right|_{\cos}$. Using a Fourier series, $|V_{S1,n}|_{\cos}$ and $|V_{S1,n}|_{\sin}$ can be calculated as

$$\left|V_{S1,n}\right|_{\cos} = \frac{1}{\pi}\int_0^{2\pi} V_{S1}(t)\cos(n\omega_s t + \varphi_r) d(\omega_s t)\,, \quad (2-18)$$

$$\left|V_{S1,n}\right|_{\sin} = \frac{1}{\pi}\int_0^{2\pi} V_{S1}(t)\sin(n\omega_s t + \varphi_r) d(\omega_s t)\,. \quad (2-19)$$

Utilizing inverter output voltage V_{S1} equation (2-8), the solution for the above Fourier series equations can be calculated as

$$\begin{aligned} \frac{\left|V_{S1,n}\right|_{\sin}}{V_{dc}} &= \frac{1}{n\pi}\{\cos(\varphi_r) - \cos(nA + \varphi_r)\} - K_{p1,n} \\ &+ K_{p2,n}\left\{K\sin(A + \varphi_r) + 2\pi\omega_{1,N} D - \frac{K\omega_{1,N}\sin(\varphi_r)}{1+\omega_{1,N}}\right\} + \frac{K\omega_{1,N}}{1-\omega_{1,N}^{\ 2}}(K_{p3,n} - K_{p4,n}) \end{aligned} \quad (2-20)$$

$$2\pi K_{p1,n} = \frac{\cos(\varphi_r) - \cos(nA + B + \varphi_r)}{n + \omega_{1,N}} + \frac{\cos(\varphi_r) - \cos(nA - B + \varphi_r)}{n - \omega_{1,N}}$$

$$2\pi K_{p2,n} = -\frac{\sin(nA + B + \varphi_r) - \sin(\varphi_r)}{n + \omega_{1,N}} + \frac{\sin(nA - B + \varphi_r) - \sin(\varphi_r)}{n - \omega_{1,N}}$$

$$2\pi K_{p3,n} = \frac{\cos(2\varphi_r) - \cos((n+1)A + 2\varphi_r)}{n+1} + \frac{\cos((n-1)A) - 1}{n-1}$$

$$2\pi K_{p4,n} = \frac{\cos(2\varphi_r) - \cos(nA + B + 2\varphi_r)}{n + \omega_{1,N}} + \frac{\cos(nA - B) - 1}{n - \omega_{1,N}}$$

$$\frac{\left|V_{s1,n}\right|_{\cos}}{V_{dc}}=\frac{1}{n\pi}\left\{\sin(nA+\varphi_r)-\sin(\varphi_r)\right\}-K_{q1,n}$$
$$+K_{q2,n}\left\{K\sin(A+\varphi_r)+2\pi\omega_{1,N}D-\frac{K\omega_{1,N}\sin(\varphi_r)}{1+\omega_{1,N}}\right\}+\frac{K\omega_{1,N}}{1-\omega_{1,N}{}^2}(K_{q3,n}-K_{q4,n})$$

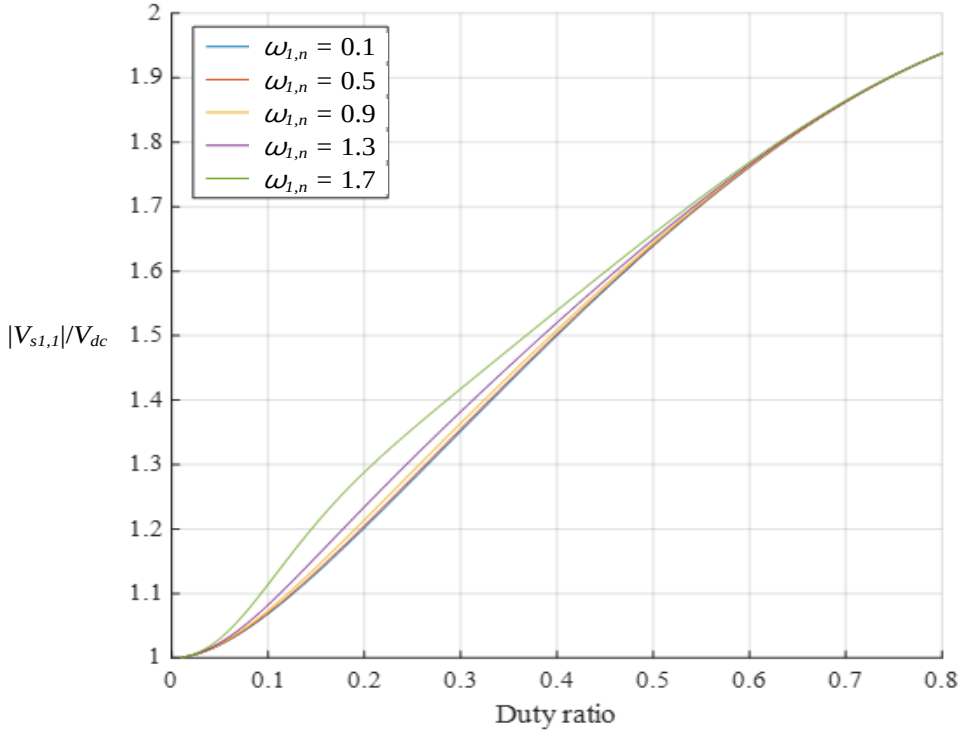
(2-21)

$$2\pi K_{q1,n}=\frac{\sin(nA+B+\varphi_r)-\sin(\varphi_r)}{n+\omega_{1,N}}+\frac{\sin(nA-B+\varphi_r)-\sin(\varphi_r)}{n-\omega_{1,N}}$$

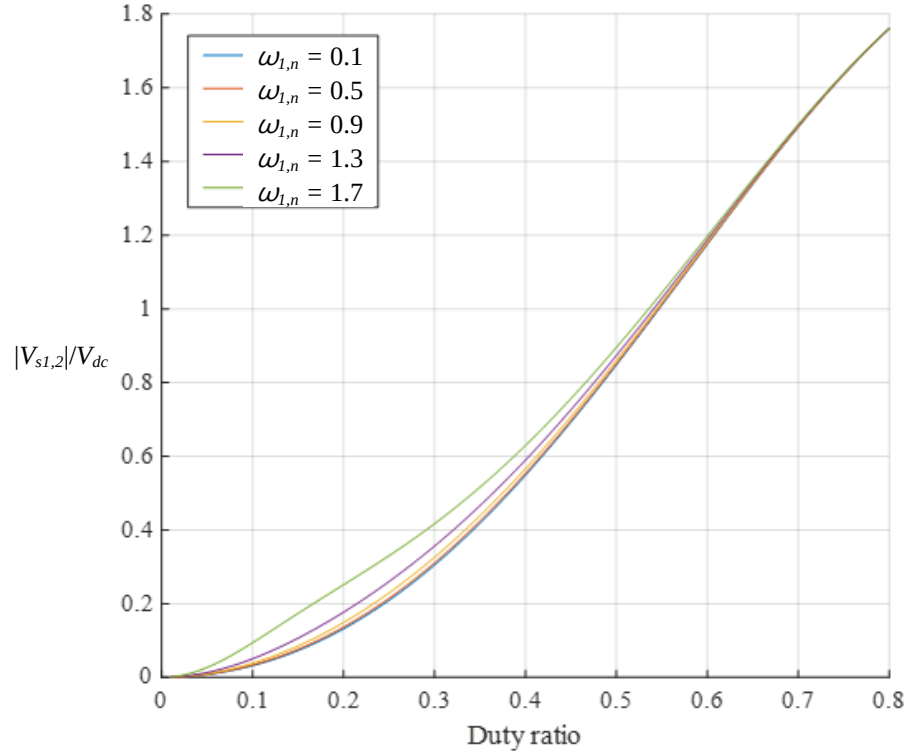
$$2\pi K_{q2,n}=\frac{\cos(\varphi_r)-\cos(nA+B+\varphi_r)}{n+\omega_{1,N}}-\frac{\cos(\varphi_r)-\cos(nA-B+\varphi_r)}{n-\omega_{1,N}}$$

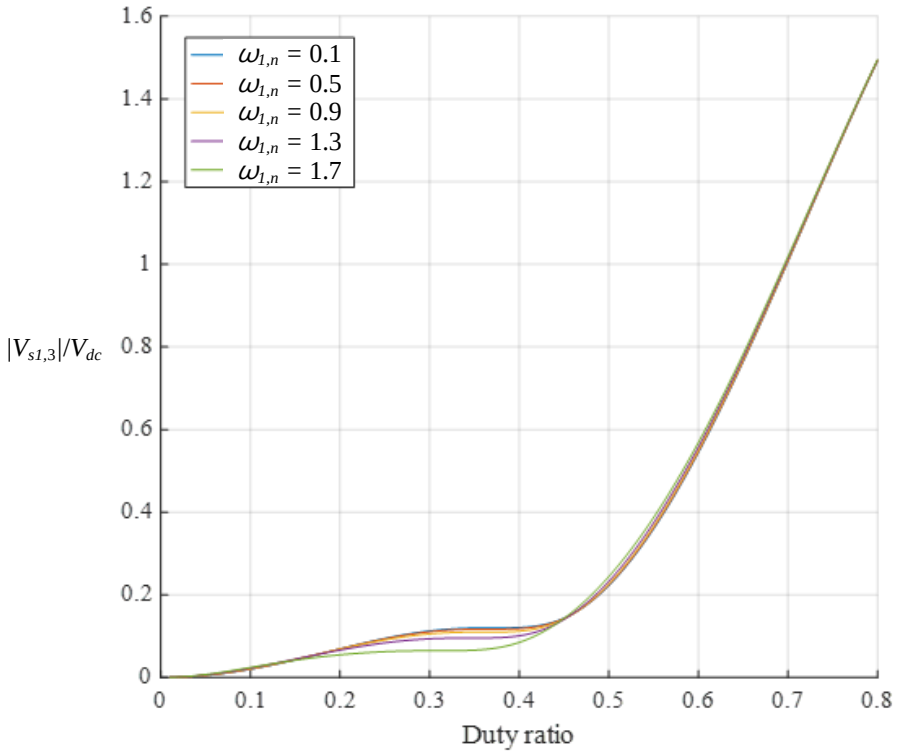
$$2\pi K_{q3,n}=\frac{\sin((n+1)A+2\varphi_r)-\sin(2\varphi_r)}{n+1}+\frac{\sin((n-1)A)-1}{n-1}$$

$$2\pi K_{q4,n}=\frac{\sin(nA+B+2\varphi_r)-\sin(2\varphi_r)}{n+\omega_{1,N}}+\frac{\sin(nA-B)}{n-\omega_{1,N}}$$


$\omega_{1,n}$ = 0.1
$\omega_{1,n}$ = 0.5
$\omega_{1,n}$ = 0.9
$\omega_{1,n}$ = 1.3
$\omega_{1,n}$ = 1.7
$|V_{s1,1}|/V_{dc}$
Duty ratio

(a)


$\omega_{1,n}$ = 0.1
$\omega_{1,n}$ = 0.5
$\omega_{1,n}$ = 0.9
$\omega_{1,n}$ = 1.3
$\omega_{1,n}$ = 1.7
$|V_{s1,2}|/V_{dc}$
Duty ratio



(c)

Fig. 2−19. Class E inverter output voltage magnitude (a) fundamental term (b) 2nd harmonic term (c) 3rd harmonic term

Using these equations, the fundamental term and harmonic terms of the inverter output voltage can be calculated. Fig. 2−19 shows the fundamental, 2nd harmonic, and 3rd harmonic terms of inverter output voltage for different $\omega_{1,n,}$ and duty ratio. It can be seen that both fundamental and harmonic terms increase as the duty ratio

increases. Fig. 2−20 shows the 2nd, 3rd, and 4th harmonic terms compared to fundamental components when $\omega_{1,n}$ = 1.4. In this figure, 3rd and 4th harmonic terms have small values when the duty ratio is below 0.5. Compared to the 2nd harmonic term, higher harmonic terms are more than five times smaller in most duty ratios below 0.5. However, at a high duty ratio, higher harmonic terms are comparable to 2nd harmonic and cannot be ignored. Nonetheless, in most class E converter designs, a high duty ratio above 0.5 is often not used since the maximum voltage across the switch S_1 increases as the duty ratio increases, shown

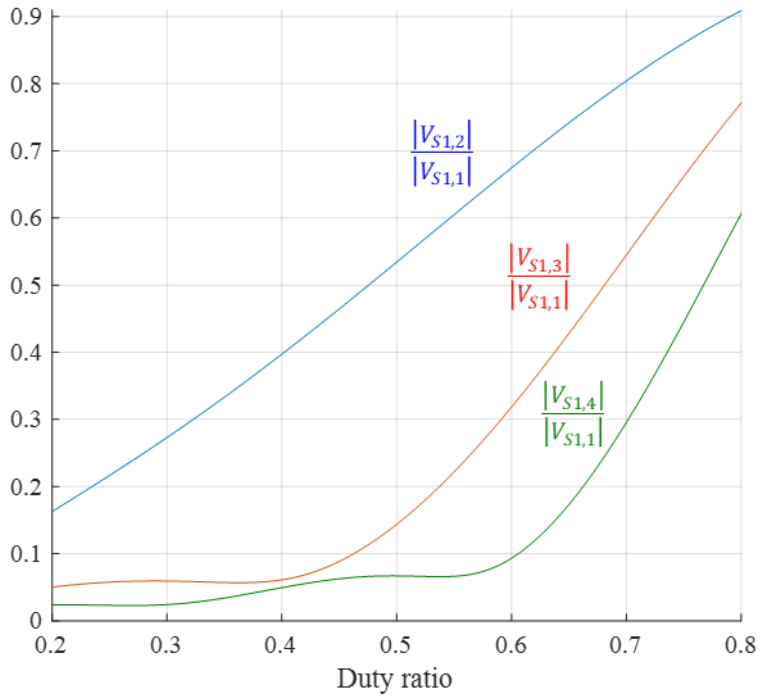


Fig. 2−20. 2nd, 3rd and 4th harmonic terms of a class E inverter output voltage normalized by fundamental term.

in Fig. 2−21. Here $V_{S1,max}$ is a peak voltage across the switch S_1 during steady−state operation. According to this figure, when the duty ratio equals 0.5, the maximum voltage across switch S_1 is 3.6 times the DC−link input voltage V_{dc}. When the duty ratio equals 0.6, the maximum voltage is more than 4.5 times the DC input voltage. Therefore, to reduce the voltage stress of the switch S_1, a class E converter is designed to operate at lower duty. Thus, in this paper, fundamental and 2nd harmonic terms are primarily analyzed since these terms are dominant compared to other harmonic terms in low duty ratio. The phase of the

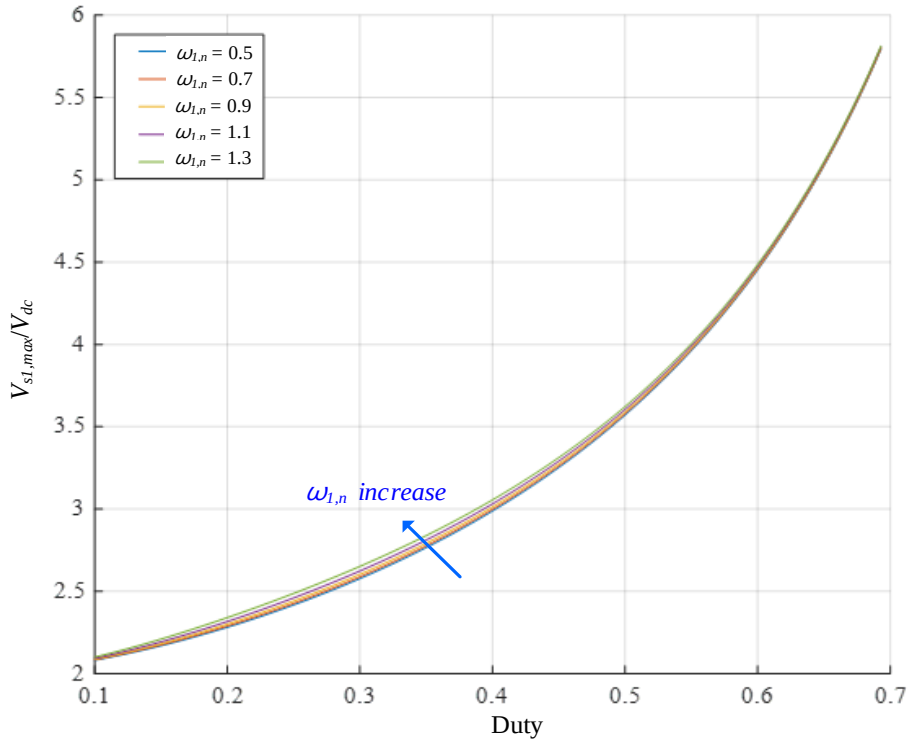
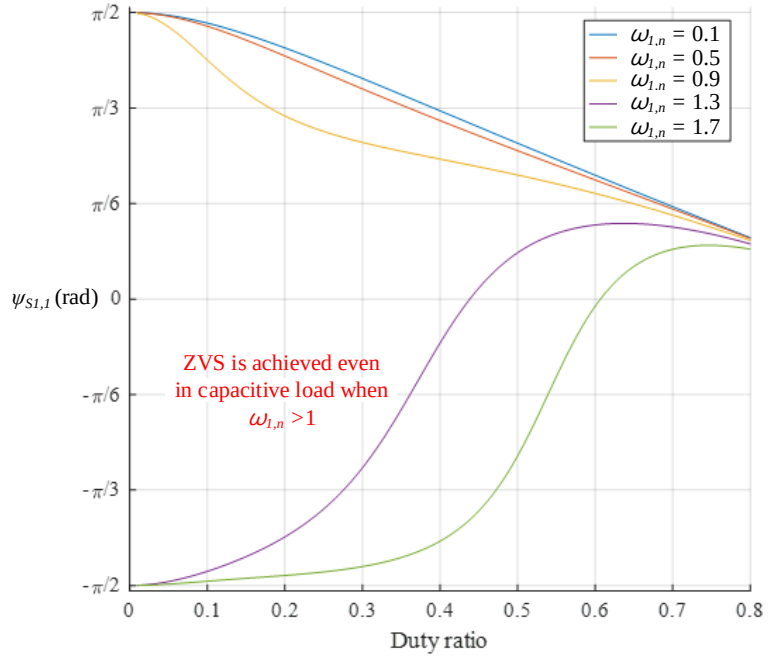


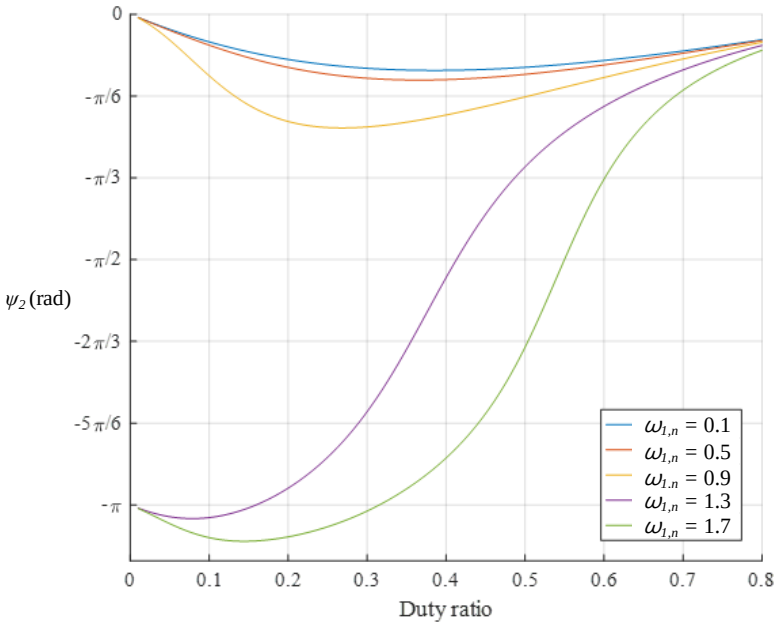
Fig. 2− 21. Maximum voltage across switch S_1 during steady−state operation at different duty ratio.

inverter output voltage $\Psi_{S1,1}$ and $\Psi_{S1,2}$ is shown in Fig. 2−22. From the figure, if $\omega_{1,n}$ is designed below one, $\Psi_{S1,1}$ is consistently between zero and $\pi/2$. This means a resonant current I_r should be lagging compared to $V_{S1,1}$ to achieve ZVS. If $\omega_{1,n}$ is above one, however, there is a region where $\Psi_{S1,1}$ lies between zero and $-\pi/2$. This means that ZVS can still be achieved at some duty ratios even if I_r is leading compared to $V_{S1,1}$. The reason for this result is due to a small inductance of L_1 at large $\omega_{1,n}$. At large $\omega_{1,n}$ inductor L_1 is small and resonates with capacitor C_1 creating resonant current in I_s. These currents help the class E converter achieve ZVS and set the phase of the voltage $V_{S1,1}$ between zero and $-\pi/2$.

A class E rectifier works in duality with a class E inverter [65]. Assuming diode forward voltage drop is small, the magnitude of rectifier voltage V_{D1} can be calculated with the same result with an inverter by replacing parameters L_1, C_1, and V_{dc} in



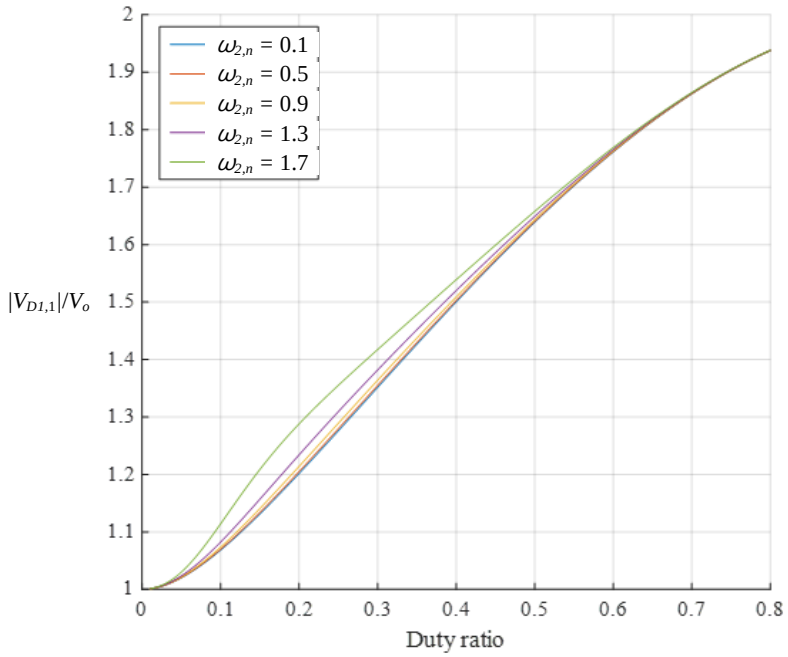
(a)



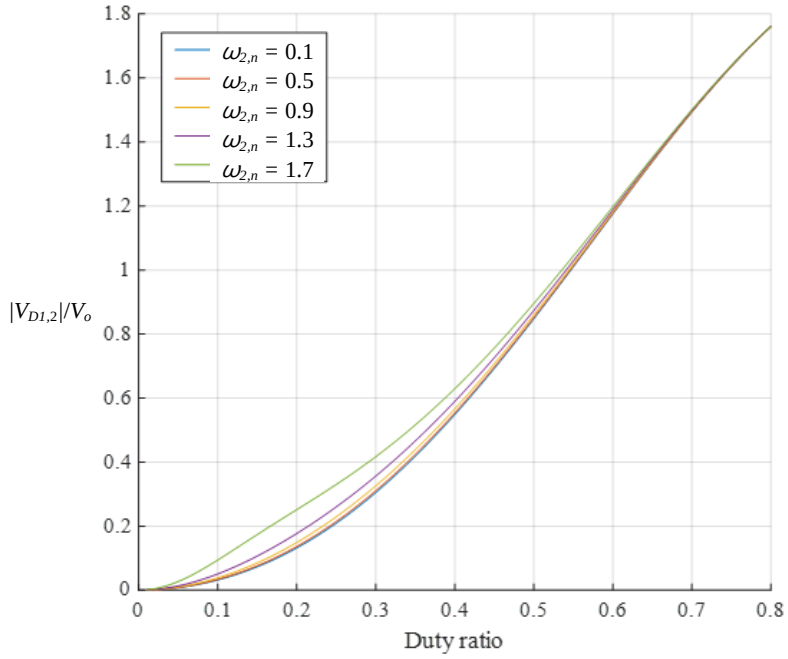
(b)

Fig. 2-22 Phase of the inverter output votlage (a) fundamental (b) 2nd harmonic term

equations (2-7) - (2-21) with L_2, C_2, and V_o. Let $\omega_{2,N} = \left(\omega_s \sqrt{L_2 C_2}\right)^{-1}$, Fig. 2-23 shows the magnitude of fundamental



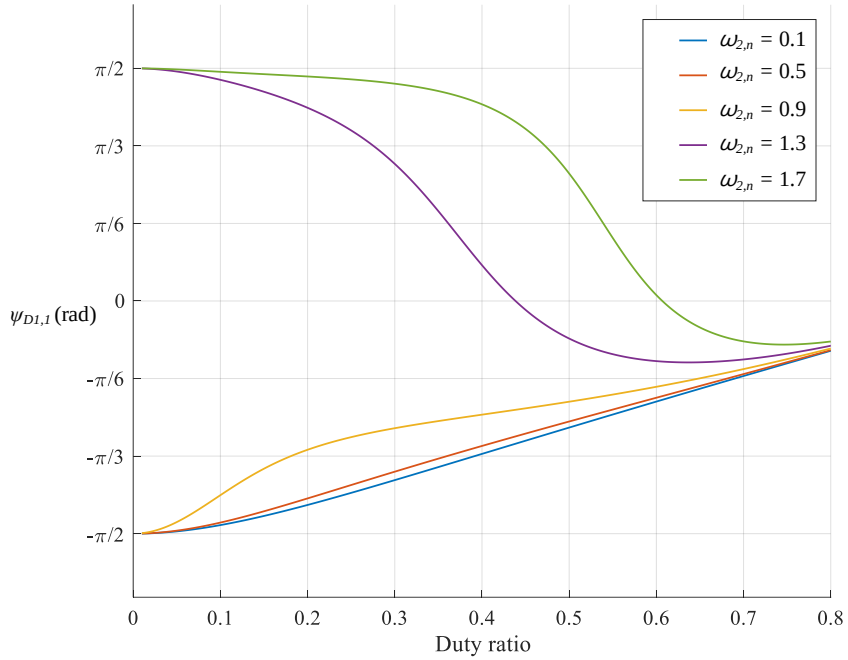
(a)



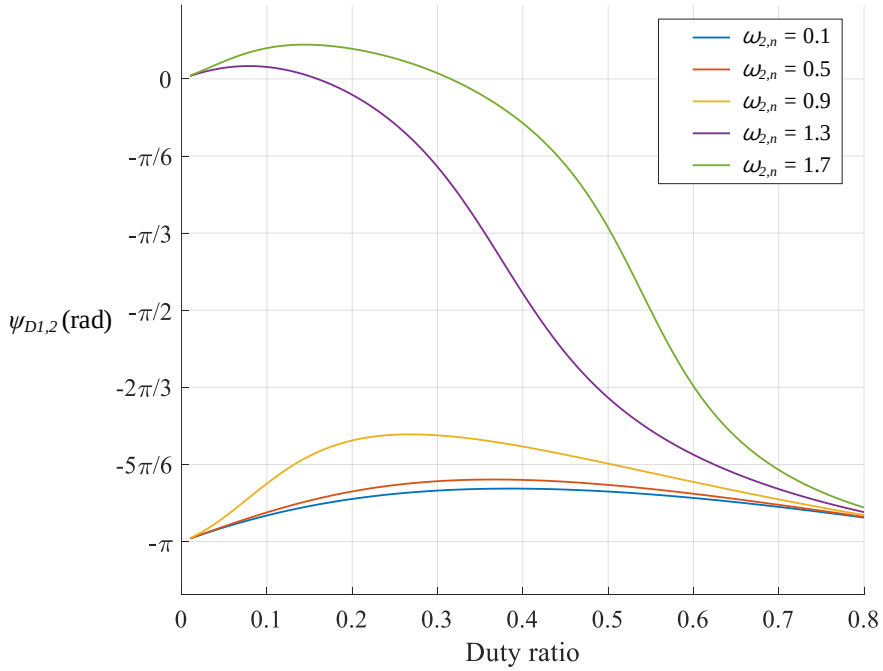
(b)

Fig. 2-23. Magnitude of rectifier voltage (a) fundamental (b) 2nd harmonic term

$|V_{D1,1}|$ and 2nd harmonic term $|V_{D1,2}|$ of rectifier voltage, and Fig. 2-24 shows the phase of fundamental $\Psi_{D1,1}$ and second harmonic



(a)



(b)

Fig. 2-24. Phase of rectifier voltage (a) fundamental (b) 2nd harmonic term

$\Psi_{D1,2}$ term of rectifier voltage. The forward drop of diode D_1 is neglected in this equation. If $\omega_{1,n} = \omega_{2,n}$, the relationship between

class E inverter output voltage and class E rectifier output voltage can be simplified. The magnitude and phase V_{S1} and V_{D1} satisfies the below equation when $\omega_{1,n} = \omega_{2,n}$

$$\frac{|V_{S1,n}|}{V_{dc}} = \frac{|V_{D1,n}|}{V_o} \tag{2-22}$$

$$\psi_{S1,1} = -\psi_{D1,1}, \ \psi_{S1,2} = -\psi_{D1,2} + \pi \tag{2-23}$$

These results will be used to analyze the fundamental and harmonic terms of common-mode current in the class E converter.

3. Class E Converter with LC Series Network

3.1 Common Mode Current in Class E Converter with LC Series Network

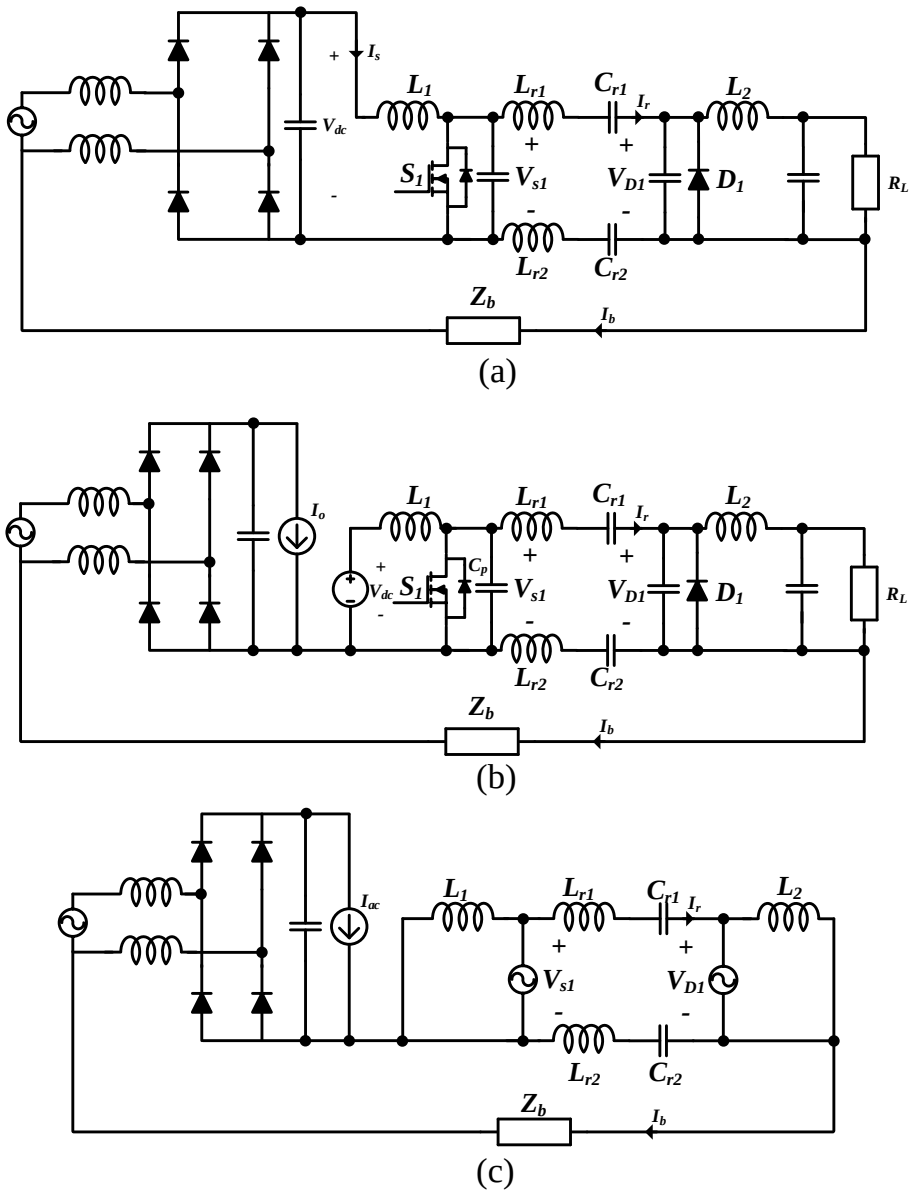


Fig. 3-1. Modeling procedure of class E capacitive isolated converter (a) capacitive isolated converter with LC series network (b) dividing AC/DC rectifier part and DC/DC converter part (c) active components modeling for common mode current estimation

In order to analyze the common-mode current in the class E DC/DC converter, the circuit model shown in Fig. 3-1 is used. First, AC/DC rectifier part and DC/DC converter part are divided as shown in Fig. 3-1(b). Next, assuming common mode current is small compared to the differential mode current, active components are modeled as a voltage source where V_{S1} and V_{D1} are a voltage across the switch S_1 and diode D_1. Also, since DC voltage sources do not contribute to common mode current, input and output of the DC/DC converter are shorted to simplify the model, as shown in Fig. 3-1(c).

Using this model, a high-frequency common mode current can be calculated. Simplifying Fig. 3-1(c) such that only the high-frequency component remains, Thevenin and Norton equivalent circuit seen from the common-mode side can be drawn. Fig. 3-2 shows the process of drawing a common-mode equivalent circuit. The resulting Thevenin and Norton equivalent circuit is shown in Fig. 3-3. where open circuit voltage $V_{cm,oc,}$ and short circuit current $I_{cm,sc}$ can be calculated as

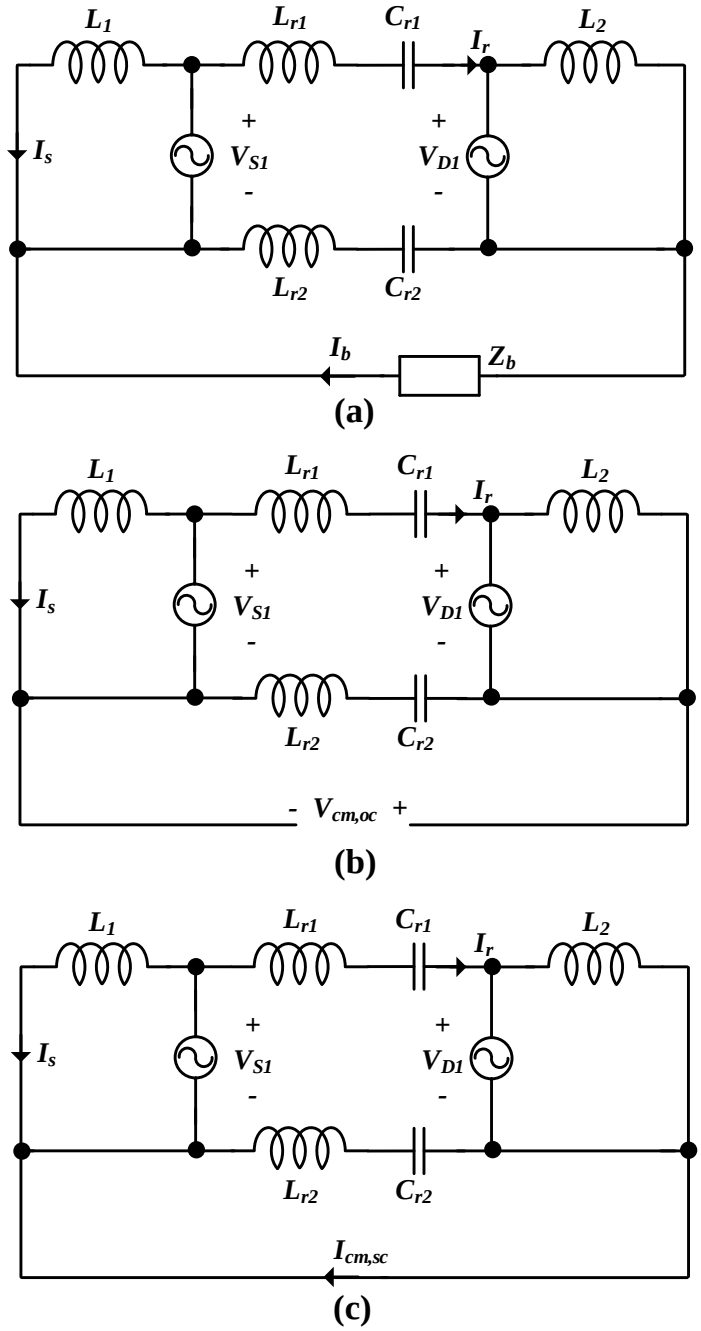


Fig. 3-2. Calculating common-mode Thevenin equivalent circuit (a) common-mode modeling (b) open circuit voltage calculation (c) short circuit current calculation

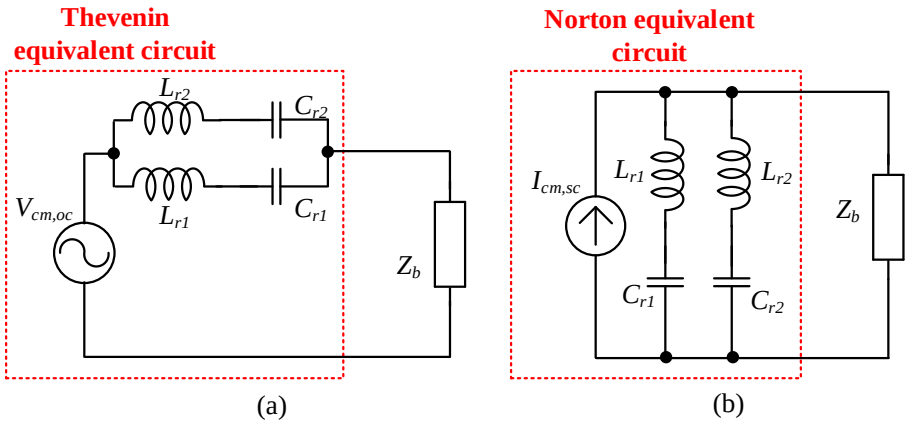


Fig. 3-3. Common-mode equivalent circuit (a) Thevenin equivalent circuit (b) Norton equivalent circuit

$$V_{cm,oc}(s)=\frac{\left(sL_{r2}+1/(sC_{r2})\right)\left(V_{s1}(s)-V_{D1}(s)\right)}{s(L_{r1}+L_{r2})+(C_{r1}+C_{r2})/(sC_{r1}C_{r2})} \tag{3-1}$$

$$I_{cm,sc}(s)=\frac{V_{s1}(s)-V_{D1}(s)}{sL_{r1}+1/(sC_{r1})}. \tag{3-2}$$

Applying results from Fig. 2-19 – Fig. 2-24, the common-mode current at each frequency can be calculated. The magnitude of $I_{cm,sc}$ at switching frequency ω_s and $2\omega_s$, can be written as

$$\left|I_{cm,sc}(j\omega_s)\right|=\left|\frac{|V_{S1,1}|\angle\psi_{S1,1}-\left|V_{D1,1}\right|\angle\psi_{D1,1}}{\{\omega_s L_{r1}-1/(\omega_s C_{r1})\}}\right| \tag{3-3}$$

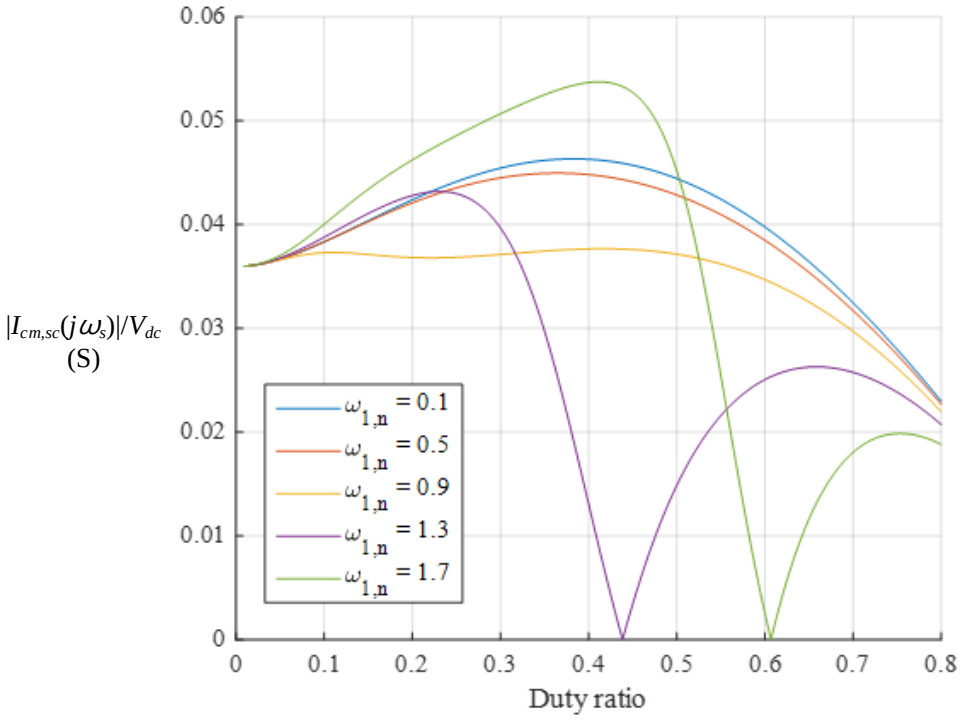
$$\left|I_{cm,sc}(j2\omega_s)\right|=\left|\frac{|V_{S1,2}|\angle\psi_{S1,2}-\left|V_{D1,2}\right|\angle\psi_{D1,2}}{\{2\omega_s L_{r1}-1/(2\omega_s C_{r1})\}}\right| \tag{3-4}$$

If L_1 is equal to L_2 and C_1 is equal to C_2, both inverter and rectifier operate in the same duty ratio and $\omega_{1,n} = \omega_{2,n}$. Also, the inverter and rectifier's fundamental and harmonic voltage magnitude becomes the same. At this condition, the equation (3-3) and (3-4) then can be rewritten as

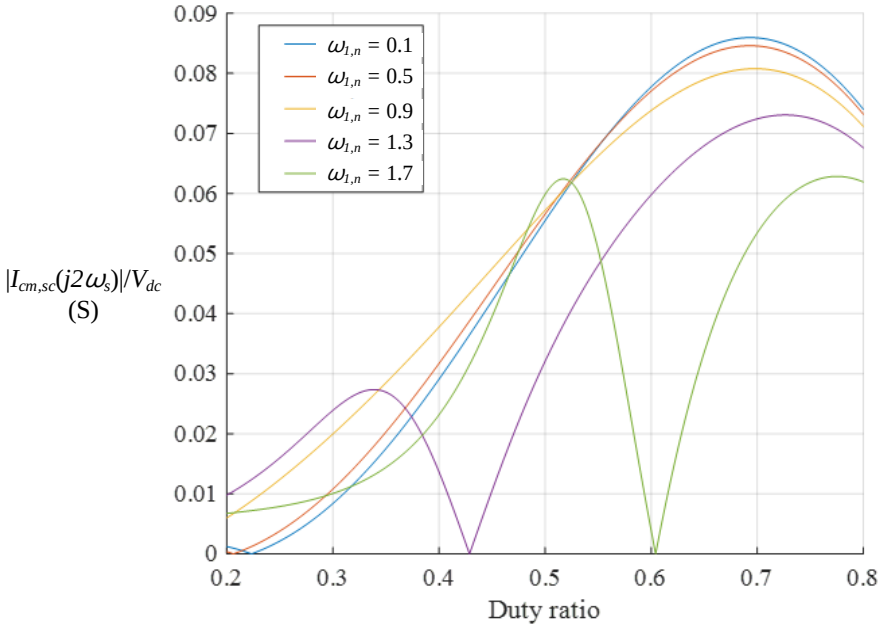
$$\left|I_{cm,sc}(j\omega_s)\right| = \frac{\left|V_{S1,1}\right|\sqrt{2(1-\cos(2\psi_{S1,1}))}}{\left|\omega_s L_{r1} - 1/(\omega_s C_{r1})\right|} \quad (3-5)$$

$$\left|I_{cm,sc}(j2\omega_s)\right| = \frac{\left|V_{S1,2}\right|\sqrt{2(1+\cos(2\psi_{S1,2}))}}{\left|2\omega_s L_{r1} - 1/(2\omega_s C_{r1})\right|} \quad (3-6)$$

Fig. 3-4 shows the plot of the transconductance of common-mode current magnitude $|I_{cm,sc}|/V_{dc}$ at frequency ω_s and $2\omega_s$ when L_{r1} = 0 and C_{r1} = 220 pF. From the figure, there exists a point where $I_{cm,sc}$ is equal to zero. $I_{cm,sc}(j\omega_s)$ is equal to zero when $\Psi_{S1,1}$ is equal to zero and $I_{cm,sc}(j2\omega_s)$ is equal to zero when $\Psi_{S1,2}$ is equal to $\pi/2$. This point can only exist when class E inverter and rectifiers are designed such that both $\omega_{1,n,}$ and $\omega_{2,n}$ are greater than one, as mentioned in the previous section.



(a)



(b)

Fig. 3-4. Transconductance of common-mode current (a) fundamental (b) 2nd harmonic term

Using Norton equivalent circuit in Fig. 3-3, the common-mode current I_{cm} can be calculated using a short circuit common-mode current $I_{cm,sc}$ value using the equation below

$$\left|I_{cm}(jn\omega_s)\right| = \left|\frac{I_{cm,sc}(jn\omega_s)\{Z_b(jn\omega_s) \| jX_{th}(jn\omega_s)\}}{Z_b(jn\omega_s)}\right|, \quad (3-7)$$

where jX_{th} is a Thevenin impedance, also equal to Norton impedance, calculated as $V_{cm,oc}/I_{cm,sc}$. In capacitive isolated class E converter with LC series network in Fig. 3-1, X_{th} is equal to a parallel of two LC series as shown in equivalent circuit in Fig. 3-3. Following impedance X_{th} can be calculated as

$$X_{th}(jn\omega_s) = \frac{(n\omega_s)^2 L_{r1}L_{r2} + \dfrac{1}{(n\omega_s)^2 C_{r1}C_{r2}} - \dfrac{L_{r1}C_{r1} + L_{r2}C_{r2}}{C_{r1}C_{r2}}}{(n\omega_s)(L_{r1} + L_{r2}) - \dfrac{C_{r1} + C_{r2}}{(n\omega_s)C_{r1}C_{r2}}}. \quad (3-8)$$

Z_b is an impedance of a common-mode current path. It is different depending on how the load is connected to the ground. For example, if the load and ground have no physical connection, Z_b has a very high impedance and vice versa. Also, if a common-

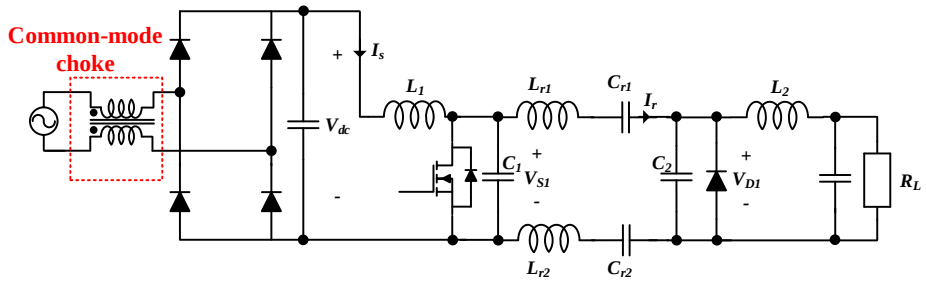
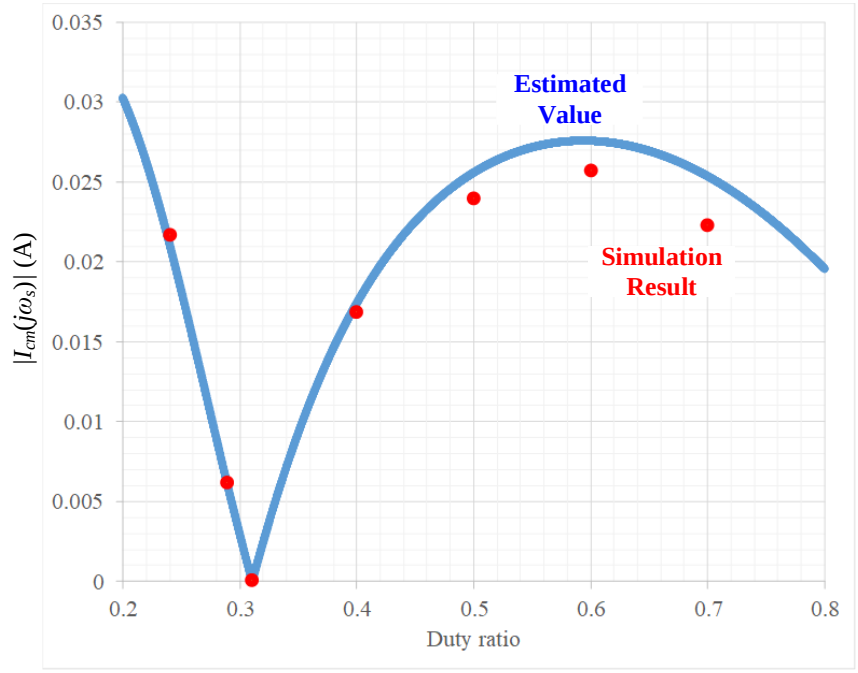


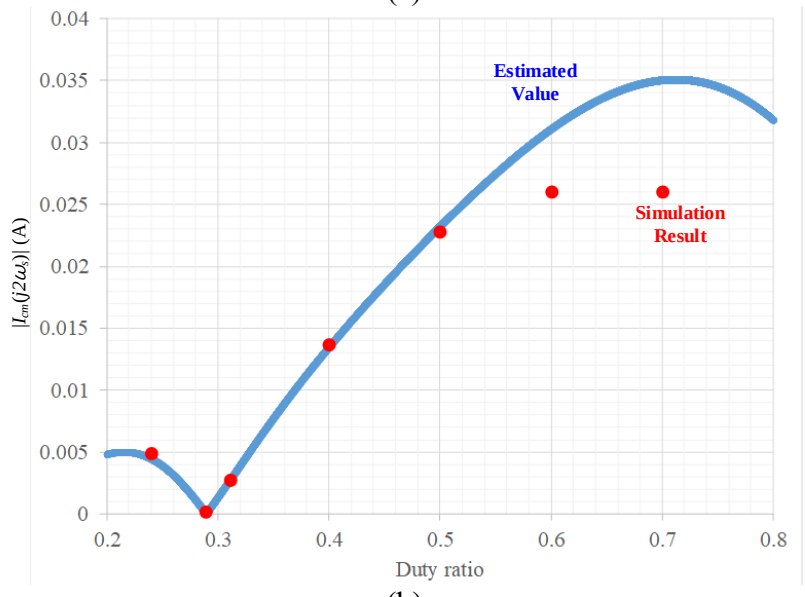
Fig. 3-5. Common-mode choke placed between AC input and AC/DC converter

mode choke filter is placed between AC input and AC/DC converter, as shown in Fig. 3−5, the impedance of the common−mode choke is included in Z_b.

Fig. 3−6 compares the estimated common mode current using equation (3−5) – (3−7) and simulation result value. In this figure, fundamental $|I_{cm}(j\omega_s)|$ and second harmonic term $|I_{cm}(j2\omega_s)|$ when $\omega_{1,n}$ = $\omega_{2,n}$ = 1.14 and Z_b = 3000 Ω are compared. The capacitor value C_{r1} and C_{r2} is set to 220 pF, and inductor L_{r1} and L_{r2} are set such that ZVS and dv/dt equals zero condition is satisfied. The estimated and simulated results are almost identical, but errors increase as the duty ratio increases. This error is caused by the increase in harmonic current in I_r as the duty ratio increases. In section 2, the output voltage equation of the class E inverter is calculated assuming resonant current I_r is sinusoidal with no harmonic component. However, as the duty ratio increases, the harmonic current appears in I_r due to the high−frequency component of inverter output voltage, increasing the estimation error. Fig. 3−7 shows the change in estimation and simulation value when small C_{r1} and C_{r2} is used for high−quality factor LC series circuit. In this result, C_{r1} and C_{r2} are set to 50 pF. From the figure, the estimation and simulation value is very close even in



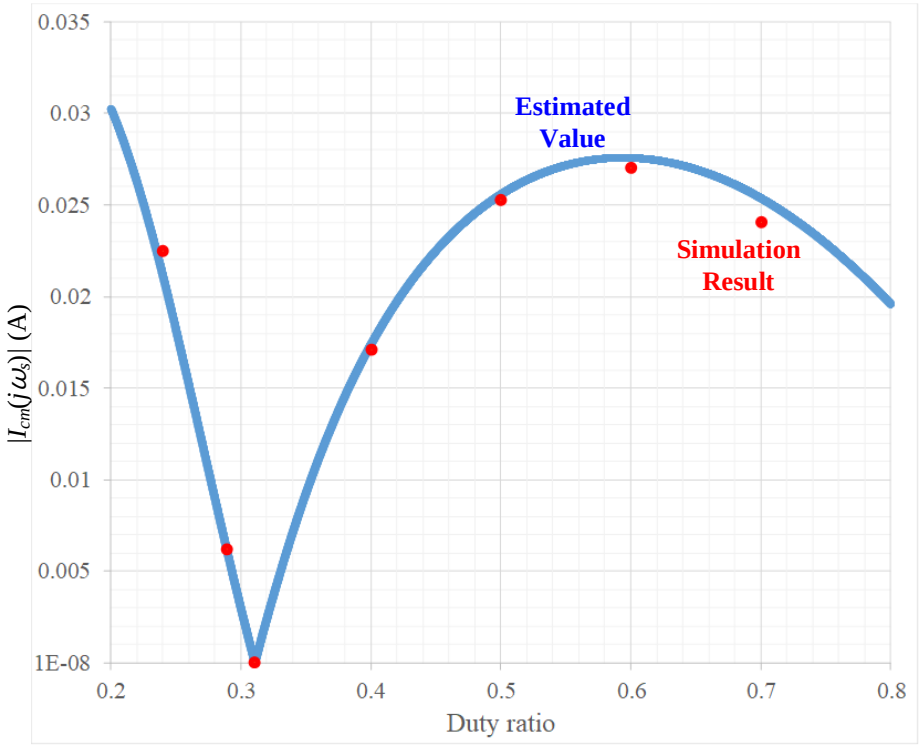
(a)



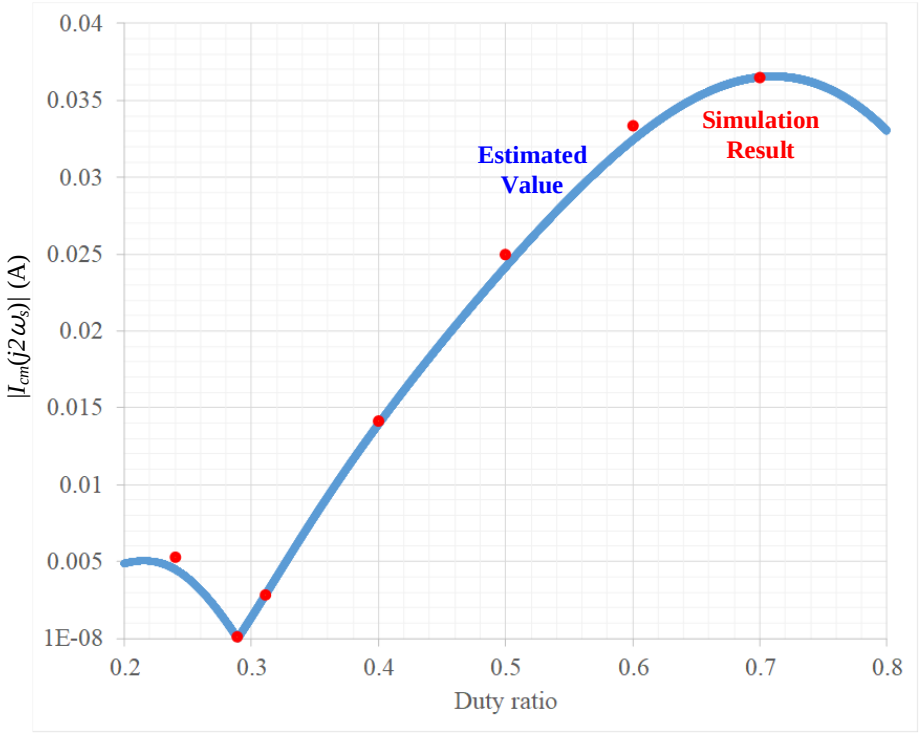
(b)

Fig. 3-6. Comparison between estimated common-mode current and simulated value (a) fundamental (b) 2nd harmonic term

a high duty ratio. However, such a high-quality factor LC series circuit requires a large inductor, and therefore, is not always a feasible option.



(a)



(b)

Fig. 3-7. Comparison between estimated common-mode current and simulated value with small C_r (a) fundamental (b) 2nd harmonic term

When the duty ratio is around 0.3, a common-mode current is almost zero. This is possible because the common-mode current is proportional to the difference between inverter output voltage V_{S1} and rectifier voltage V_{D1}. Therefore, if V_{S1} and V_{D1} can negate each other in a common-mode voltage, common-mode current can be eliminated. In fundamental component, a common-mode current is zero when $\Psi_{S1,1} = \Psi_{D1,1} = 0$. In 2nd harmonic term, a common-mode current is zero when $\Psi_{S1,2} - \Psi_{D1,2} = \pi$. However, these two points are not the same, and therefore, other frequency components of common-mode current still remain, so reducing this common-mode current is necessary.

3.2 Balanced Class E Converter Design and Analysis

In this paper, the balanced class E converter shown in Fig. 3-8 is proposed to reduce the high-frequency common-mode

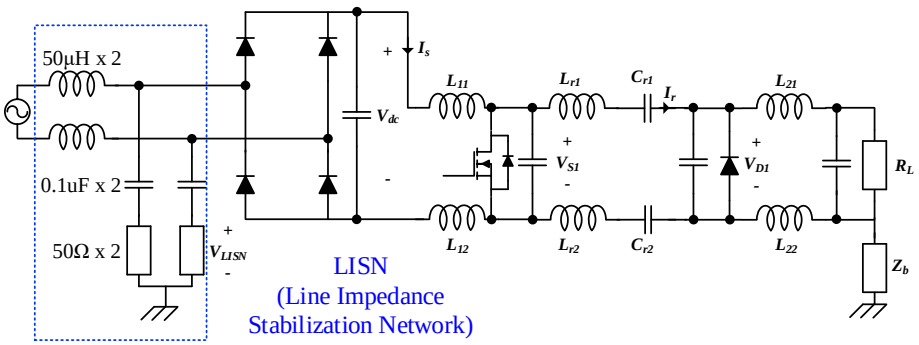


Fig. 3-8. Circuit diagram of balanced class E converter

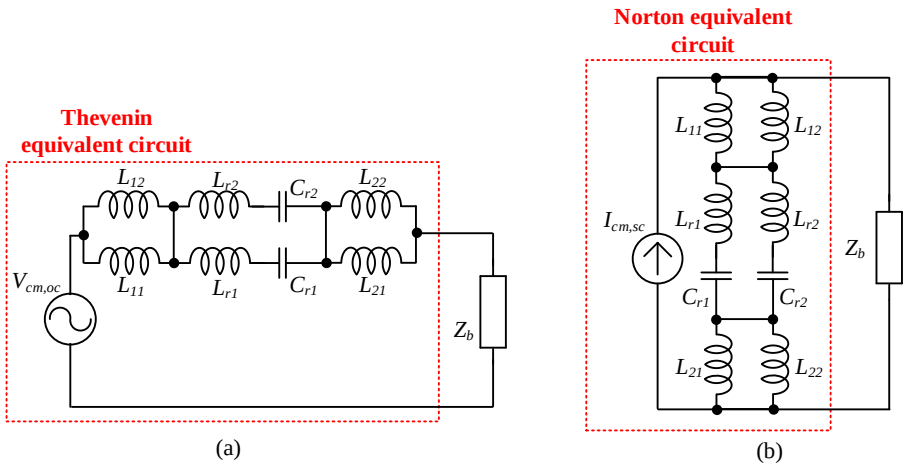


Fig. 3-9. Common-mode equivalent circuit (a) Thevenin equivalent circuit (b) Norton equivalent circuit

current. In order to estimate and analyze the common mode current of balanced class E converter, the same modeling method is used that analyzes common mode current in conventional capacitive isolated class E converter. Thevenin and Norton equivalent circuit is drawn as shown in Fig. 3-9. The calculated $V_{cm,oc,}$ and $I_{cm,sc}$ is

$$V_{cm,oc}(s)=\left\{\frac{sL_{r2}+1/(sC_{r2})}{s(L_{r1}+L_{r2})+(C_{r1}+C_{r2})/(sC_{r1}C_{r2})}-\frac{L_{12}}{L_{11}+L_{12}}\right\}V_{S1}(s)$$
$$-\left\{\frac{sL_{r2}+1/(sC_{r2})}{s(L_{r1}+L_{r2})+(C_{r1}+C_{r2})/(sC_{r1}C_{r2})}-\frac{L_{22}}{L_{21}+L_{22}}\right\}V_{D1}(s) \quad (3-9)$$

$$I_{cm,sc}(s)=\left(\frac{sL_{11}L_{12}}{L_{11}+L_{12}}+\frac{sL_{21}L_{22}}{L_{21}+L_{22}}+\frac{(sL_{r1}+1/(sC_{r1}))(sL_{r2}+1/(sC_{r2}))}{s(L_{r1}+L_{r2})+(C_{r1}+C_{r2})/sC_{r1}C_{r2}}\right)^{-1}V_{cm,oc}(s) \quad (3-10)$$

It can be seen from equations (3-9) and (3-10), common-mode

current is completely removed for all frequency components if converter is perfectly balanced, meaning $L_{11} = L_{12}$, $L_{21} = L_{22}$, $L_{r1} = L_{r2}$ and $C_{r1} = C_{r2}$.

A common-mode current can be eliminated if an exact parameter value can be used to design a balanced class E converter. However, it is impossible to develop a perfectly balanced converter in the real world due to the manufacturing error of each passive element and parasitic inductor and capacitor. Due to manufacturing errors, commercial inductors and capacitors have slightly different parameter values even if bought from the same manufacturer. For instance, the air core inductor from coil craft [46] has a minimum stock tolerance of 2%. Although it is still possible to put a special order to buy elements with lower tolerance value, such an order is much more expensive and requires a longer shipping time. Also, parasitic inductance and capacitance depending on PCB layout [47]-[51] also contribute to parameter difference in balanced class E converter. Therefore, effects of parameter error to common mode current in balanced class E converter should be analyzed

Monte-Carlo simulation is done to examine the effects of parameter error on common-mode current. Fig 3-10 shows a

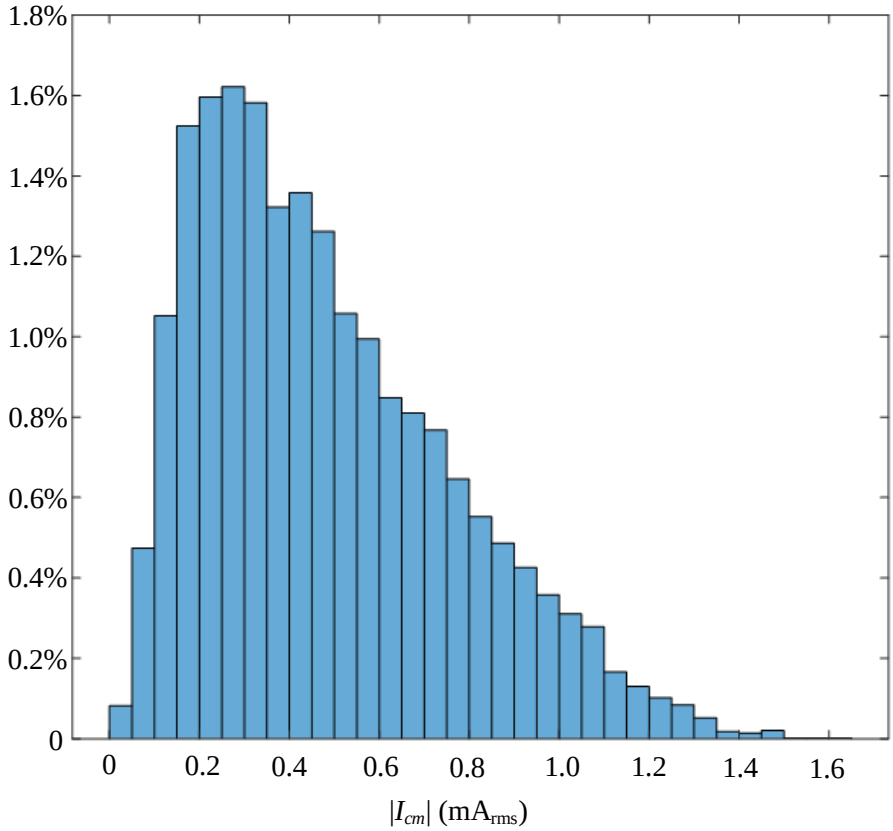


Fig. 3-10. Histogram of root mean square value of common-mode current

TABLE 3-1. CLASS E CONVERTER WITH LC SERIES NETWORK PARAMETERS USED IN SIMULATION AND EXPERIMENTS

Parameters	Value	Parameter Tolerance
L_{11} & L_{12}	300 [nH]	±2%
L_{r1} & L_{r2}	798 [nH]	±2%
C_{r1} & C_{r2}	220 [pF]	±10%
L_{21} & L_{22}	300 [nH]	±2%
C_1 & C_2	200 [pF]	
f_s	12.14 [MHz]	
R_L	300 [Ω]	

histogram of the root mean square value of common-mode current when the simulation is run 10,000 times. Parameters and their tolerance used in the simulation are shown in Table 3-1.

Here inductors have 2% parameter tolerance, and capacitors have 10% parameter tolerance based on the actual parameter tolerance value stated in the datasheet [46] and [60]. This simulation parameter is assumed to be uniformly distributed among parameter tolerance values, and common-mode current path impedance is set to 3000 Ω. The maximum common-mode current caused by parameter tolerance is 1.62 mA, while the most probable common-mode current value is between 250 μA and 300 μA from the histogram.

In order to mathematically estimate the effect of parameter error in a balanced converter, the maximum common-mode current of a balanced class E converter within a given parameter tolerance range is calculated. It is assumed that parameter error is small such that it does not affect voltage V_{S1} and V_{D1}. Then using parameters $|V_{S1,n}|$, $|V_{D1,n}|$, $\Psi_{S1,n}$ and $\Psi_{D1,n}$ calculated in previous section, equation (3-9) can be rewritten as

$$\left|V_{cm,oc}(jn\omega_s)\right|^2 = \left(K(jn\omega_s) - \frac{L_{12}}{L_{11}+L_{12}}\right)^2 |V_{S1,n}|^2 + \left(K(jn\omega_s) - \frac{L_{22}}{L_{21}+L_{22}}\right)^2 |V_{D1,n}|^2$$
$$-2|V_{S1,n}||V_{D1,n}|\left(K(jn\omega_s) - \frac{L_{12}}{L_{11}+L_{12}}\right)\left(K(jn\omega_s) - \frac{L_{22}}{L_{21}+L_{22}}\right)\cos(\psi_{S1,n} - \psi_{D1,n}) \quad (3-11)$$

$$K(jn\omega_s) = \frac{1-(n\omega_s)^2 C_{r2}L_{r2}}{(1+C_{r2}/C_{r1})-(n\omega_s)^2 C_{r2}(L_{r1}+L_{r2})}$$

If both inverter and rectifier operates in same duty ratio and $\omega_{1,n}$ equals $\omega_{2,n}$, $|V_{S1,n}|$ is equal to $|V_{D1,n}|$.

$$\frac{|V_{cm,oc}(jn\omega_s)|^2}{|V_{S1,n}|^2} = \left(\frac{X_{r2}}{X_{r1}+X_{r2}} - \frac{L_{12}}{L_{11}+L_{12}}\right)^2 + \left(\frac{X_{r2}}{X_{r1}+X_{r2}} - \frac{L_{22}}{L_{21}+L_{22}}\right)^2 - 2\left(\frac{X_{r2}}{X_{r1}+X_{r2}} - \frac{L_{12}}{L_{11}+L_{12}}\right)\left(\frac{X_{r2}}{X_{r1}+X_{r2}} - \frac{L_{22}}{L_{21}+L_{22}}\right)\cos(\psi_{S1,n} - \psi_{D1,n}) \quad (3-12)$$

where $X_{r1} = \omega L_{r1} - 1/(\omega C_{r1})$ and $X_{r2} = \omega L_{r2} - 1/(\omega C_{r2})$. To observe the parameter error effect on $V_{cm,oc}$, each parameter is rewritten as below

$$L_{11} = L_1(1+\lambda_{11}), L_{12} = L_1(1+\lambda_{12}), L_{21} = L_2(1+\lambda_{21}), L_{22} = L_2(1+\lambda_{22})$$
$$X_{r1} = X_r(1+\lambda_{r1}), X_{r2} = X_r(1+\lambda_{r2}) \quad (3-13)$$

where λ is a parameter error tolerance often with a few hundredths value. Then using polar coordinates, the parameter tolerance value is altered to

$$\lambda_k = \sqrt{\lambda_{k1}{}^2 + \lambda_{k2}{}^2}, \tan(\theta_k) = \frac{\lambda_{k2}}{\lambda_{k1}} (k = 1, 2, r) \quad (3-14)$$

Using equation (3−13) and (3−14), $V_{cm,oc}$ equation (3−12) can be rewritten as

$$\frac{\left|V_{cm,oc}(jn\omega_s)\right|^2}{|V_{S1,n}|^2}=\left(\frac{1+\lambda_r\sin(\theta_r)}{2+\lambda_r(\sin(\theta_r)+\cos(\theta_r))}-\frac{1+\lambda_1\sin(\theta_1)}{2+\lambda_1(\sin(\theta_1)+\cos(\theta_1))}\right)^2$$
$$+\left(\frac{1+\lambda_r\sin(\theta_r)}{2+\lambda_r(\sin(\theta_r)+\cos(\theta_r))}-\frac{1+\lambda_2\sin(\theta_2)}{2+\lambda_2(\sin(\theta_2)+\cos(\theta_2))}\right)^2$$
$$-2\left(\frac{1+\lambda_r\sin(\theta_r)}{2+\lambda_r(\sin(\theta_r)+\cos(\theta_r))}-\frac{1+\lambda_1\sin(\theta_1)}{2+\lambda_1(\sin(\theta_1)+\cos(\theta_1))}\right)$$
$$\left(\frac{1+\lambda_r\sin(\theta_r)}{2+\lambda_r(\sin(\theta_r)+\cos(\theta_r))}-\frac{1+\lambda_2\sin(\theta_2)}{2+\lambda_2(\sin(\theta_2)+\cos(\theta_2))}\right)\cos(\psi_{S1,n}-\psi_{D1,n})$$

(3−15)

Then calculating the derivative of equation (3−15) with θ_k yields

$$\frac{d(|V_{cm,oc}|^2/|V_{S1,n}|^2)}{d\theta_1}$$
$$\cong 2\frac{-\lambda_1(\cos(\theta_1)+\sin(\theta_1)+\lambda_1)}{\{2+\lambda_1(\sin(\theta_1)+\cos(\theta_1))\}^2}\left\{\left(\frac{1+\lambda_r\sin(\theta_r)}{2+\lambda_r(\sin(\theta_r)+\cos(\theta_r))}-\frac{1+\lambda_1\sin(\theta_1)}{2+\lambda_1(\sin(\theta_1)+\cos(\theta_1))}\right)\right.$$
$$\left.-\left(\frac{1+\lambda_r\sin(\theta_r)}{2+\lambda_r(\sin(\theta_r)+\cos(\theta_r))}-\frac{1+\lambda_2\sin(\theta_2)}{2+\lambda_2(\sin(\theta_2)+\cos(\theta_2))}\right)\cos(\psi_{S1,n}-\psi_{D1,n})\right\}$$

(3−16)

$$\frac{d(|V_{cm,oc}|^2/|V_{S1,n}|^2)}{d\theta_2}$$
$$=2\frac{-\lambda_2(\cos(\theta_2)+\sin(\theta_2)+\lambda_2)}{\{2+\lambda_2(\sin(\theta_2)+\cos(\theta_2))\}^2}\left\{\left(\frac{1+\lambda_r\sin(\theta_r)}{2+\lambda_r(\sin(\theta_r)+\cos(\theta_r))}-\frac{1+\lambda_2\sin(\theta_2)}{2+\lambda_2(\sin(\theta_2)+\cos(\theta_2))}\right)\right.$$
$$\left.-\left(\frac{1+\lambda_r\sin(\theta_r)}{2+\lambda_r(\sin(\theta_r)+\cos(\theta_r))}-\frac{1+\lambda_1\sin(\theta_1)}{2+\lambda_1(\sin(\theta_1)+\cos(\theta_1))}\right)\cos(\psi_{S1,n}-\psi_{D1,n})\right\}$$

(3−17)

$$\frac{d(|V_{cm,oc}|^2/|V_{S1,n}|^2)}{d\theta_r}=2\frac{\lambda_r\{(\sin(\theta_r)+\cos(\theta_r))+\lambda_r\}}{\{2+\lambda_r(\sin(\theta_r)+\cos(\theta_r))\}^2}$$
$$\left\{\left(2\frac{1+\lambda_r\sin(\theta_r)}{2}-\frac{1+\lambda_2\sin(\theta_2)}{2}-\frac{1+\lambda_1\sin(\theta_1)}{2}\right)(1-\cos(\psi_{S1,n}-\psi_{D1,n}))\right\}$$

(3−18)

It can be seen that $|V_{cm,oc}|$ has a maximum value when $\cos(\theta_k)+\sin(\theta_k)+\lambda_k=0$ for $k=1, 2,$ and r. Since λ_k is a small value, around a few hundredth, it can be estimated that common-mode open circuit voltage $|V_{cm,oc}|$ has a maximum when $\cos(\theta_k)+\sin(\theta_k)\cong 0$ for $k=1,2$ and r. It means that the condition for maximum common-mode open circuit voltage is when $\sin(\theta_k)=\pm 1/\sqrt{2}$ and $\cos(\theta_k)=\mp 1/\sqrt{2}$. To simplify the equation, applying condition $\cos(\theta_k)+\sin(\theta_k)\cong 0$ for k = 1, 2, and r, equation (3-15) can be rewritten to

$$\frac{\left|V_{cm,oc}(jn\omega_s)\right|^2}{|V_{S1,n}|^2}=\frac{1}{4}\Big\{\big(\lambda_r\sin(\theta_r)-\lambda_1\sin(\theta_1)\big)^2+\big(\lambda_r\sin(\theta_r)-\lambda_2\sin(\theta_2)\big)^2$$
$$-2\big(\lambda_r\sin(\theta_r)-\lambda_1\sin(\theta_1)\big)\big(\lambda_r\sin(\theta_r)-\lambda_2\sin(\theta_2)\big)\cos(\psi_{S1,n}-\psi_{D1,n})\Big\} \quad (3-19)$$

Let parameter error tolerance range $0\le\lambda_k\le\lambda_{k,\max}$ where $\lambda_{k,max}$ is a maximum parameter error tolerance. Substituting $\lambda_{k,max}$ to equation (3-19), the equation is rewritten as

$$\frac{|V_{cm,ov}(j\omega_s)|^2}{|V_{S1,1}|^2}$$
$$=\frac{1}{8}\Big\{\lambda_{1,\max}{}^2+\lambda_{2,\max}{}^2+2(1-\cos(2\psi_{S1,1}))\lambda_{r,\max}{}^2-2(-1)^{\eta_{12}}\lambda_{1,\max}\lambda_{2,\max}\cos(2\psi_{S1,1})$$
$$-2\lambda_{r,\max}\big((-1)^{\eta_{r1}}\lambda_{1,\max}+(-1)^{\eta_{r2}}\lambda_{2,\max}\big)(1-\cos(2\psi_{S1,1}))\Big\} \quad (3-20)$$

$$\frac{|V_{cm,ov}(j2\omega_s)|^2}{|V_{S1,2}|^2}$$
$$= \frac{1}{8}\Big\{{\lambda_{1,\max}}^2 + {\lambda_{2,\max}}^2 + 2(1+\cos(2\psi_{S1,2}))\lambda_{r,\max}{}^2 + 2(-1)^{\eta_{12}}\lambda_{1,\max}\lambda_{2,\max}\cos(2\psi_{S1,2})$$
$$-2\lambda_{r,\max}((-1)^{\eta_{r1}}\lambda_{1,\max} + (-1)^{\eta_{r2}}\lambda_{2,\max})(1+\cos(2\psi_{S1,2}))\Big\}$$

(3-21)

where η_{12}, η_{r1}, and η_{r2} satisfy below equation

$$\eta_{ab} = \begin{cases} 1 & (\sin(\theta_a)\sin(\theta_b) = -0.5) \\ 2 & (\sin(\theta_a)\sin(\theta_b) = 0.5) \end{cases}. \qquad (3-22)$$

In equations (3-20) and (3-21), four solutions are possible depending on the sign of $\sin(\theta_1)$, $\sin(\theta_2)$, and $\sin(\theta_r)$. Calculating all possible solutions, the maximum value of $|V_{cm,oc}|$ is

$$\left.\frac{|V_{cm,oc}(j\omega_s)|^2}{|V_{S1,1}|^2}\right|_{\max} \cong \frac{1}{8}\Big\{{\lambda_{1,\max}}^2 + {\lambda_{2,\max}}^2 + 2(1-\cos(2\psi_{S1,1}))\lambda_{r,\max}{}^2 +$$
$$2\max(-\lambda_{1,\max}\lambda_{2,\max}\cos(2\psi_{S1,1}) + \lambda_{r,\max}(\lambda_{1,\max}+\lambda_{2,\max})(1-\cos(2\psi_{S1,1})),$$
$$\lambda_{1,\max}\lambda_{2,\max}\cos(2\psi_{S1,1}) + \lambda_{r,\max}|\lambda_{1,\max}-\lambda_{2,\max}|(1-\cos(2\psi_{S1,1})))$$

(3-23)

$$\left.\frac{|V_{cm,oc}(j2\omega_s)|^2}{|V_{S1,2}|^2}\right|_{\max} \cong \frac{1}{8}\Big\{{\lambda_{1,\max}}^2 + {\lambda_{2,\max}}^2 + 2(1+\cos(2\psi_{S1,2}))\lambda_{r,\max}{}^2 +$$
$$2\max(\lambda_{1,\max}\lambda_{2,\max}\cos(2\psi_{S1,2}) + \lambda_{r,\max}(\lambda_{1,\max}+\lambda_{2,\max})(1+\cos(2\psi_{S1,2})),$$
$$-\lambda_{1,\max}\lambda_{2,\max}\cos(2\psi_{S1,2}) + \lambda_{r,\max}|\lambda_{1,\max}-\lambda_{2,\max}|(1+\cos(2\psi_{S1,2})))$$

(3-24)

If $\lambda_{1,max}$, $\lambda_{2,max}$ and $\lambda_{r,max}$ have all the same value equal to λ_{max}, equation (3-23) and (3-24) can be rewritten as

$$\left.\frac{|V_{cm,oc}(j\omega_s)|^2}{|V_{S1,1}|^2}\right|_{\max} \cong \frac{\lambda_{\max}{}^2}{4}\left\{\begin{array}{l}2-\cos(2\psi_{S1,1})+\\ \max\left(2-3\cos(2\psi_{S1,1})),\cos(2\psi_{S1,1})\right)\end{array}\right\}$$
$$=\begin{cases}\dfrac{\lambda_{\max}{}^2}{2} & \left(-\dfrac{\pi}{6}<\psi_{S1,1}<\dfrac{\pi}{6}\right)\\ \lambda_{\max}{}^2(1-\cos(2\psi_{S1,1})) & elsewhere\end{cases} \quad (3-25)$$

$$\left.\frac{|V_{cm,oc}(j2\omega_s)|^2}{|V_{S1,2}|^2}\right|_{\max} \cong \frac{\lambda_{\max}{}^2}{4}\left\{\begin{array}{l}2+\cos(2\psi_{S1,2})+\\ \max\left(2+3\cos(2\psi_{S1,2})),-\cos(2\psi_{S1,2})\right)\end{array}\right\}$$
$$=\begin{cases}\dfrac{\lambda_{\max}{}^2}{2} & elsewhere\\ \lambda_{\max}{}^2(1+\cos(2\psi_{S1,2})) & \left(-\dfrac{\pi}{3}<\psi_{S1,2}<\dfrac{\pi}{3}\right)\end{cases} \quad (3-26)$$

According to above equations, the common-mode open-circuit voltage of a balanced class E converter is proportional to the voltage across the switch $|V_{S1,n}|$ and parameter error tolerance λ_{max}.

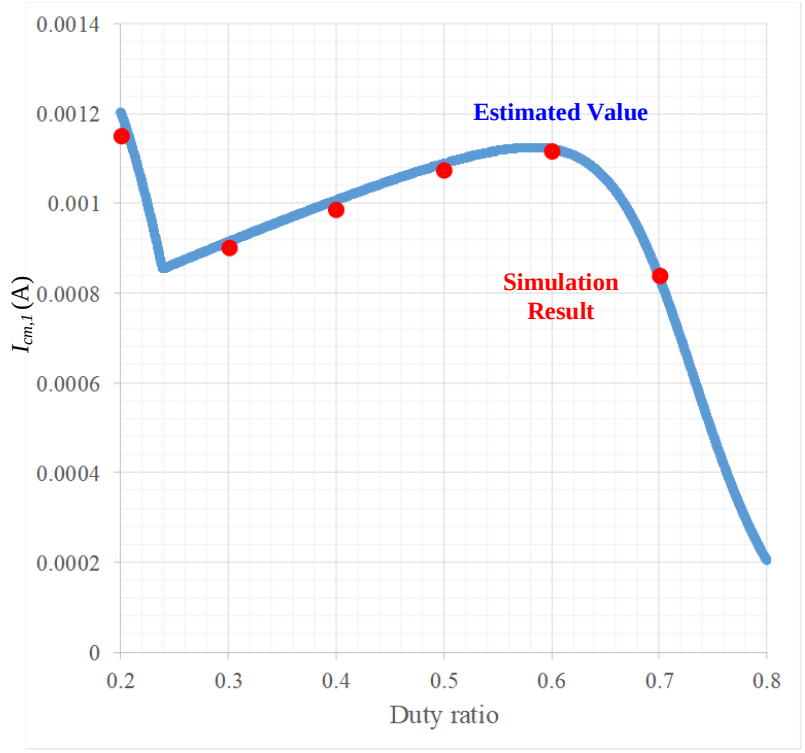
Common-mode open circuit voltage $V_{cm,oc}$ can be used to calculate the common-mode current using the equation below

$$\left|I_{cm}(jn\omega_s)\right| = \left|\frac{V_{cm,oc}(jn\omega_s)}{Z_b(jn\omega_s)+jX_{th}(jn\omega_s)}\right| \quad (3-27)$$

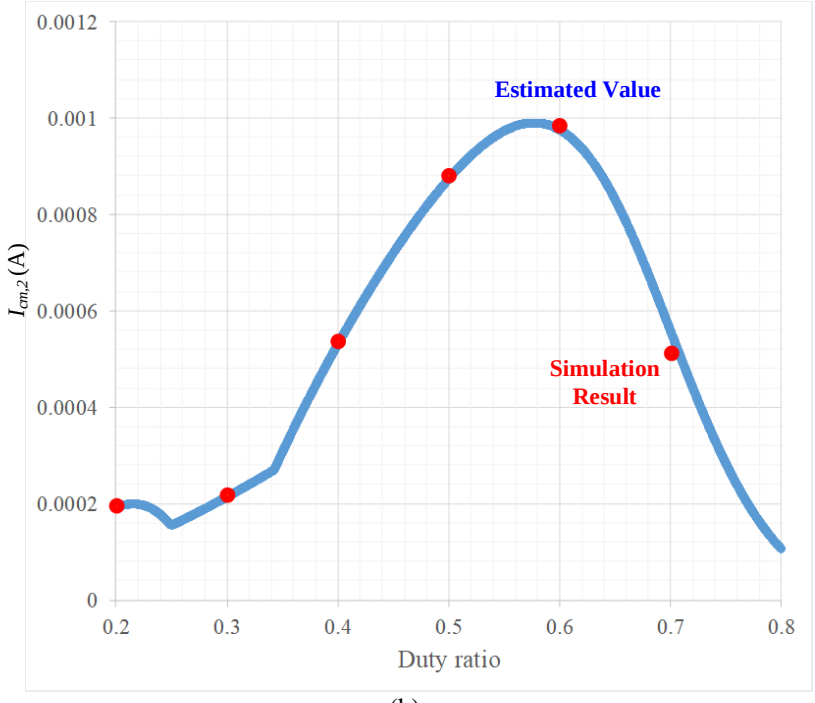
where X_{th} in a balanced class E converter is calculated as

$$X_{th}(jn\omega_s) = (n\omega_s)\left(\frac{L_{11}L_{12}}{L_{11}+L_{12}}+\frac{L_{21}L_{22}}{L_{21}+L_{22}}\right)+\frac{\left(n\omega_s L_{r1}-1/(n\omega_s C_{r1})\right)\left(n\omega_s L_{r2}-1/(n\omega_s C_{r2})\right)}{(n\omega_s)(L_{r1}+L_{r2})-(C_{r1}+C_{r2})/(n\omega_s C_{r1}C_{r2})} \quad (3-28)$$

The estimated maximum common-mode current value plot using equations (3-25) – (3-27) is shown in Fig. 3-10. Similar to Fig. 3-6, Z_b is set to 3000 Ω, $\omega_{1,n}$ equals 1.14, and the input voltage is 100V. The estimation is compared with the simulation.



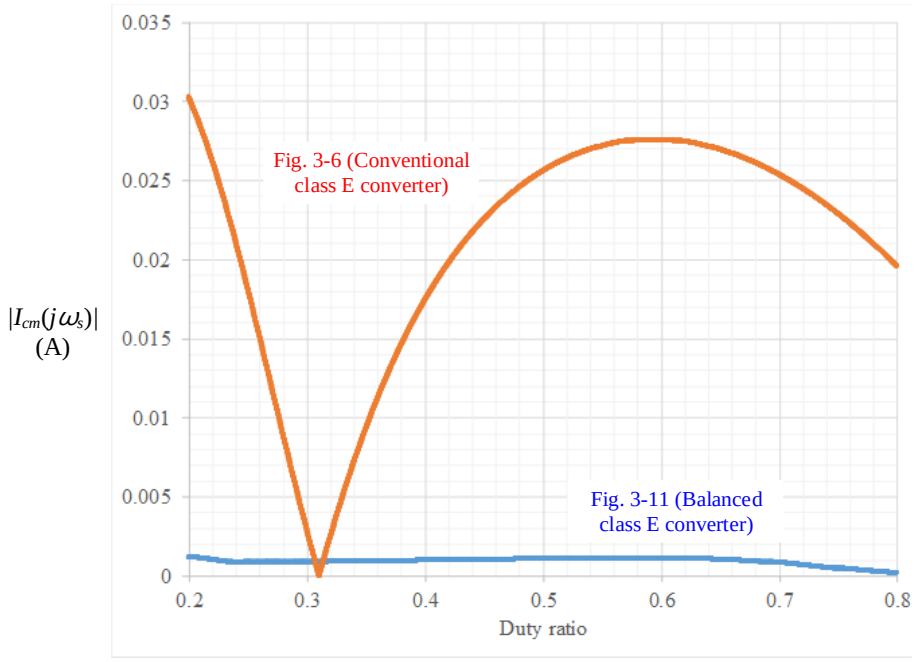
(a)



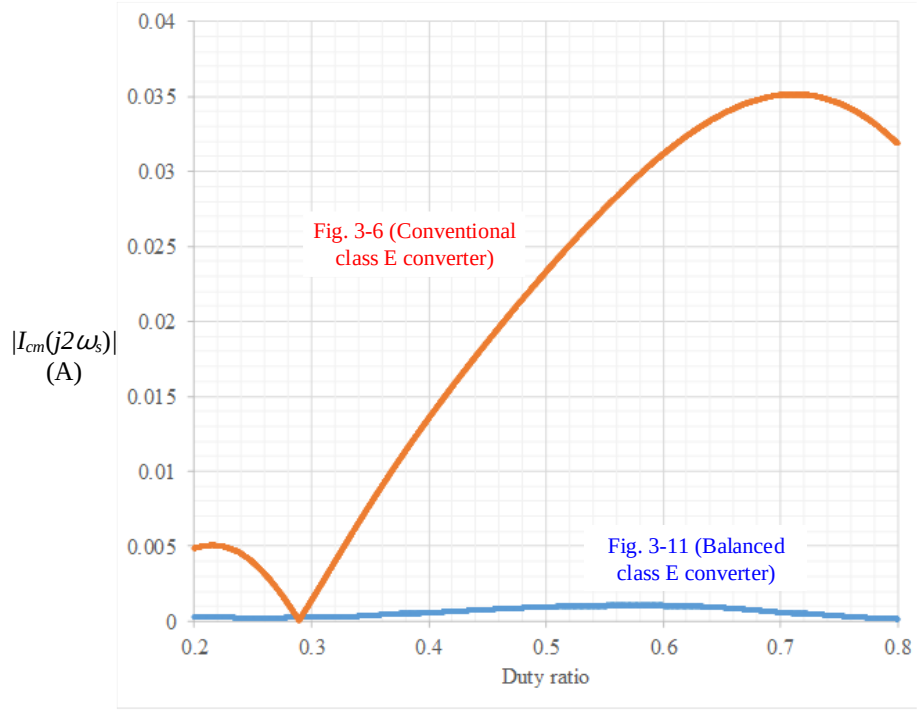
(b)

Fig. 3-11 Estimation and simulated value of a maximum common-mode mode current with parameter tolerance of ±2% (a) fundamental (b) 2nd harmonic

Comparing Fig. 3-11 to Fig. 3-6, in most regions, the maximum common-mode current in a balanced converter is more than ten times smaller than a common-mode current in a conventional class E converter. Fig. 3-12 shows the estimation of a common-mode current in a conventional class E converter and a balanced class E converter. When the duty ratio is close to 0.3, a conventional capacitive isolated converter has a smaller common-mode current compared to a balanced converter. However, parameter error is not considered when analyzing common-mode current in a conventional class E converter. Suppose a parameter error is included in a conventional class E converter. In that case, the common-mode current will no longer be eliminated at the point where the common-mode current is minimum. Therefore, designing a balanced class E converter is the best option for mitigating common-mode current in a capacitive isolated converter.



(a)



(b)

Fig. 3-12 Comparison of an estimated common-mode current in a conventional class E converter and a balanced class E converter (a) fundamental (b) 2nd harmonic

3.2.1 Common-Mode Filter

A common-mode filter can be placed in the converter to mitigate the common-mode current caused by parameter error. Generally, common-mode filters using class Y capacitor and common-mode choke are used, as shown in Fig. 3-13. In addition, Thevenin and Norton equivalent circuit is redrawn with common-mode filters in Fig. 3-14.

A common-mode filter using a class Y capacitor is placed between the DC link input and the load. This filter helps reduce the common-mode current by creating another path for high frequency current to flow. If the capacitance of C_Y is increased, the impedance of the class Y capacitor is reduced, redirecting more current to the class Y capacitor instead of flowing to the ground reducing conduction EMI. However, increasing C_Y can increase the touch current of the converter since impedance at

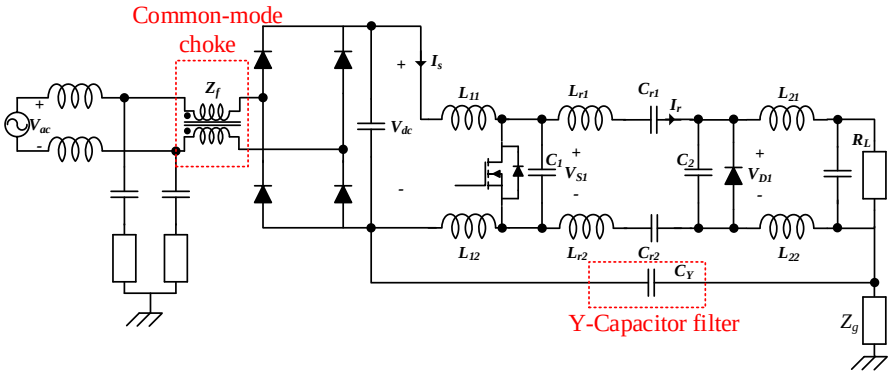


Fig. 3-13. Balanced class E converter with common-mode filter. Y-capacitor filter and common-mode choke are placed.

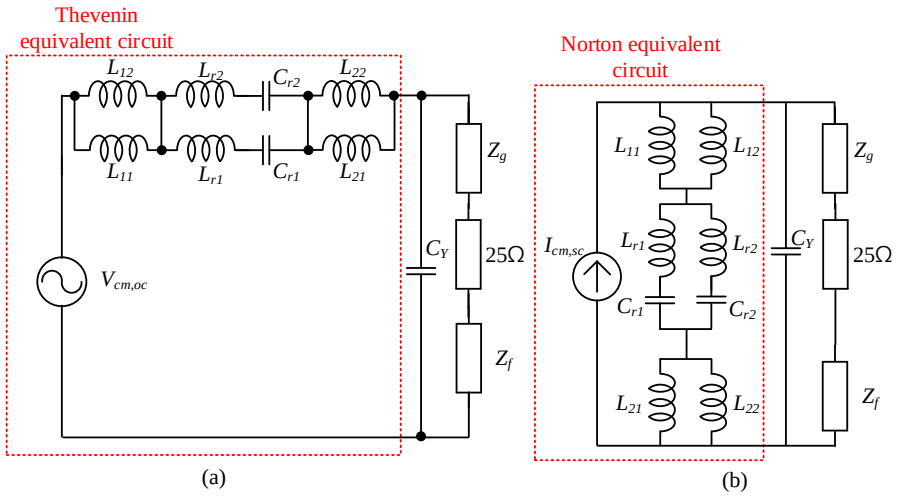


Fig. 3-14. Common-mode equivalent circuit with common mode filter (a) Thevenin equivalent circuit (b) Norton equivalent circuit

grid frequency also decreases. Thus the careful selection of C_Y is required to meet both touch current and conduction EMI regulations. The addition of class Y capacitor filter changes common-mode current to

$$\begin{aligned} &|I_{cm}(jn\omega_s)| \\ &= \left| \frac{I_{cm,sc}(jn\omega_s)}{Z_b(jn\omega_s)} \left\{ Z_b(jn\omega_s) \| j\frac{X_{th}(jn\omega_s)}{n\omega_s C_Y X_{th}(jn\omega_s)-1} \right\} \right| \\ &= \left| \frac{V_{cm,oc}(jn\omega_s)}{X_{th}(jn\omega_s)Z_b(jn\omega_s)} \left\{ Z_b(jn\omega_s) \| j\frac{X_{th}(jn\omega_s)}{n\omega_s C_Y X_{th}(jn\omega_s)-1} \right\} \right| \end{aligned} \quad . (3-27)$$

From the equation, common-mode current can be significantly reduced if $n\omega_s C_Y X_{th}(jn\omega_s) >> 1$. If $n\omega_s C_Y X_{th}(jn\omega_s) << 1$ $|I_{cm}|$ is close to the case where there is no C_Y filter and if $n\omega_s C_Y X_{th}(jn\omega_s)$ is close to one, a common-mode current is greater than when there is no capacitor filter in place. Fig. 3-15 shows the maximum common-mode current value of a balanced class E

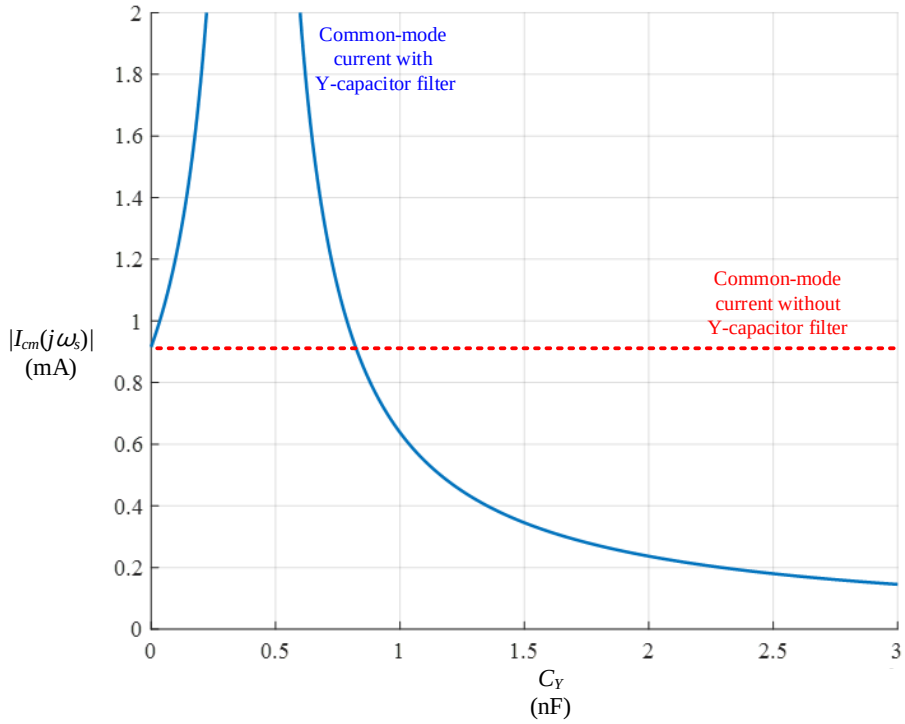


Fig. 3-15. Estimated common-mode current with different Y-capacitor C_Y.

converter with parameter error depending on the C_Y value when $\omega_{1,n}$ = 1.14, and duty ratio equals 0.3. The red line shows the maximum common-mode current value when no C_Y filter is in place, as estimated in Fig. 3-11. The equivalent impedance of the converter $X_{th}(j\omega_s)$ is equal to 32 Ω, and therefore the common-mode current is at maximum when $C_Y = 1/(\omega_s X_{th}(j\omega_s))$ = 410 pF. The converter's common-mode current becomes smaller than when there is no class Y capacitor filter if C_Y is higher than 800 pF. Therefore, in this case, C_Y should be larger than 800 pF to reduce the EMI noise.

A common-mode choke reduces the common-mode current

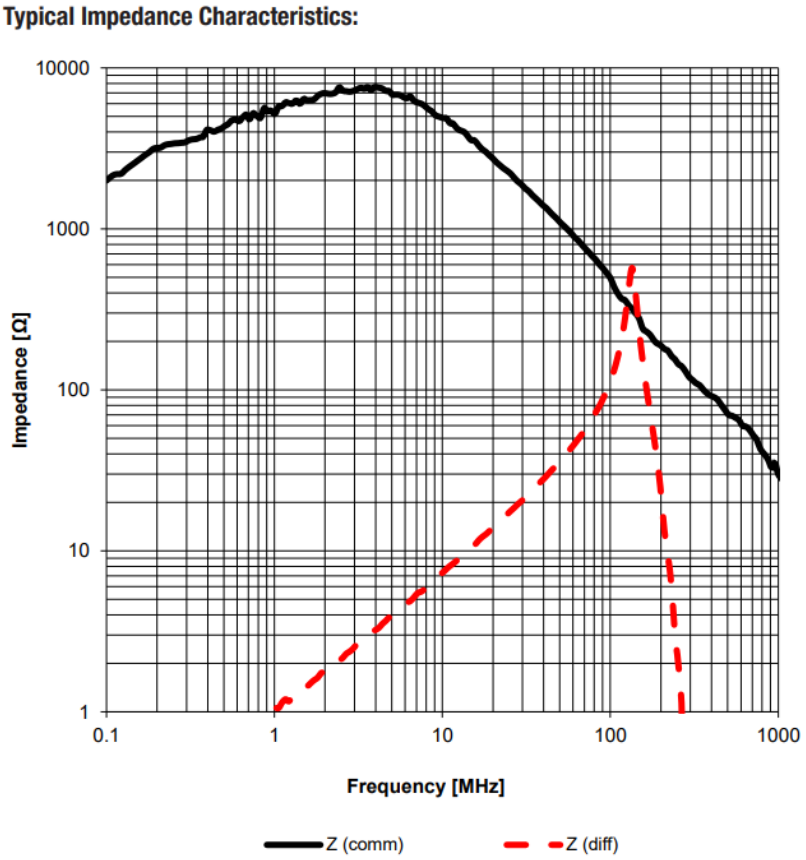


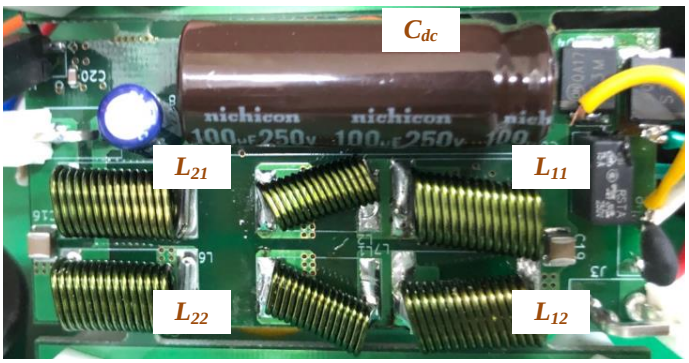
Fig. 3-16. Impedance of common mode filter WE-SL5 from Wuerth Electronik[54]

by increasing the common-mode current path impedance. Common-mode choke impedance is ideally inductive, but due to a parasitic component, measuring the common-mode impedance of commercially available common mode choke may result in resistive or even capacitive impedance value at high frequency [54]-[57]. Fig. 3-16 shows the impedance of common-mode choke WE-SL5 from Wuerth Electronik. At 12.14 MHz, the filter impedance is around 4 kΩ and about 2 kΩ at 24.28 MHz. The impedance of the common-mode choke is capacitive at a

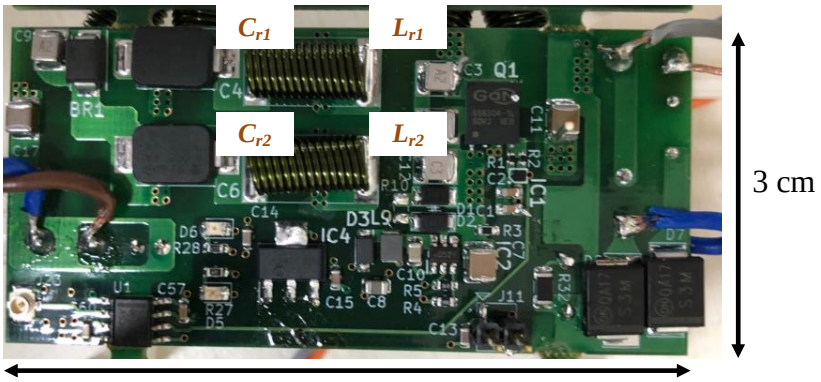
frequency higher than 10 MHz, meaning parasitic components are dominant at this frequency range.

3.3 Experimental Results

The experiment is done with class E DC/DC converter design shown in Fig. 3−17. The same parameter values, shown in Table 3−1, are used. DC/DC converter is shielded, as shown in Fig. 3−18, such that radiated noise causes a small impact to the result, and the most common mode current flows from the path created by load and Earth. In this case, the shield is



(a)



(b)

Fig. 3−17. Experimental prototype (a) front side (b) back side

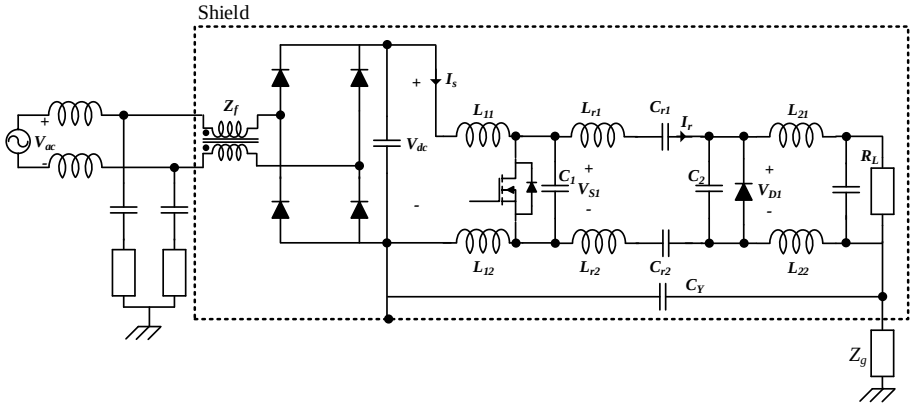
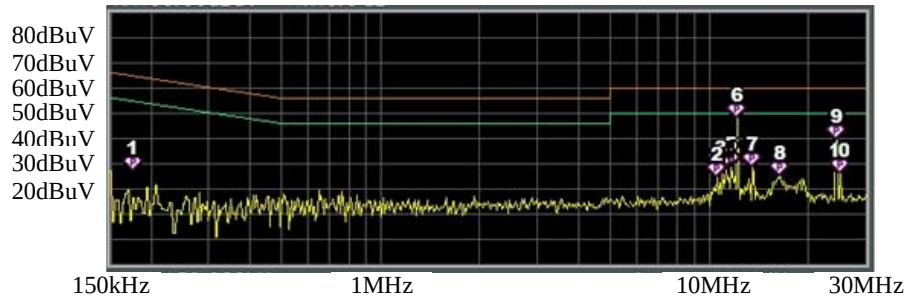


Fig. 3-18. Balanced class E converter with common-mode filter. Y-capacitor filter and common-mode choke are placed.

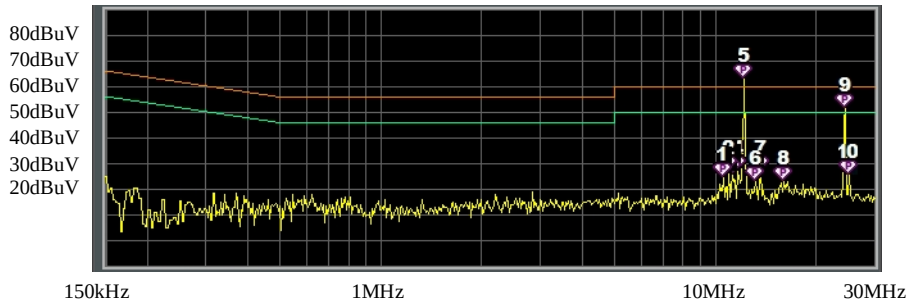
connected to the negative side of the DC-link voltage. Therefore, from the Earth side, only low-frequency grid frequency component radiation remains. For switch S_1, GaN transistor GS-065-004-1-L from GaN Systems [58] is used as a high-frequency switch with high-speed gate driver UCC27611DRVT from Texas Instrument [59]. Gate driver power is provided by the proposed self-powered circuit, which will be explained in section V of this paper. For C_{r1} and C_{r2}, Y-rated capacitor DK1B3EA221K86RAH01 from Murata Electronics [60] is used for capacitive isolation. A Y-rated capacitor is used to satisfy the voltage isolation standard IEC 60950 and IEC 61800-1. A detailed explanation of isolation voltage standard and capacitor rating is stated in Appendix 2. Also, Y-capacitor filter C_Y = 2.5 nF is added in the experiment. EM5040B from Cybertek is a line impedance stabilization network with (50 μH + 5 Ω)/ 50 Ω circuit

network. This LISN is capable of measuring common mode and differential mode conduction EMI noise separately. Only common mode noise will be measured in this experiment since reducing differential noise EMI is a separate issue. Using this LISN, conduction EMI is measured using a spectrum analyzer (GSP – 9330) from Gwinstek.

Fig. 3–19 and 3–20 show the conduction EMI measurement using a spectrum analyzer where V_{dc} = 100 V, P_o = 40 W. Conduction EMI is measured on two occasions for each circuit, one when the load has no physical connection with the Earth and another when one side of the load is directly connected to the

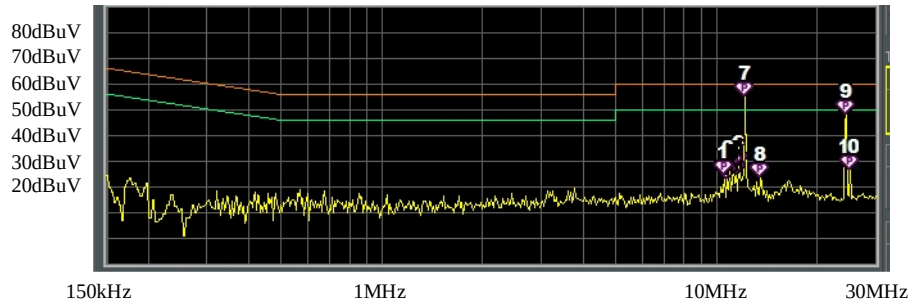


(a)



(b)

Fig. 3-19. Conduction EMI when Z_b is high impedance (a) balanced class E converter (b) conventional class E converter



(a)

(b)

Fig. 3-20. Conduction EMI when load is shorted to Earth (a) balanced class E converter (b) conventional class E converter

Earth. When the load has no physical contact, a parasitic capacitor is formed between the load and the Earth, and common mode current flows through this parasitic capacitor. Table 3-2 and Table 3-3 show the voltage across the LISN (V_{LISN}). Using a spectrum analyzer, quasi-peak of V_{LISN} is measured. Then common-mode current (I_{cm}) is calculated by dividing V_{LISN} by 25 Ω at both switching frequency (12.14 MHz) and 2nd harmonic term (24.28 MHz). From the result, it can be observed that common-mode current increases dramatically when the load is connected to the Earth. This means that other EMI noise source is small compare to common mode current path through the load

TABLE 3-2. EXPERIMENTAL RESULT WHEN ZB = HIGH IMPEDANCE

	Balanced Class E Converter		Conventional Class E Converter	
	Fundamental	2nd Harmonic	Fundamental	2nd Harmonic
V_{LISN} (dBuV)	47.8 dBμV	39.41 dBμV	54.6 dBμV	47.67 dBμV
V_{LISN} *(V)*	245 μV	93.4 μV	537 μV	242 μV
I_{cm} *(A)*	9.8 μA	3.7 μA	21.48 μA	9.68 μA

TABLE 3-3. EXPERIMENTAL RESULT WHEN ZB = 0

	Balanced Class E Converter		Conventional Class E Converter	
	Fundamental	2nd Harmonic	Fundamental	2nd Harmonic
V_{LISN} (dBuV)	65.6 dBμV	54.5 dBμV	75.89 dBμV	82.33 dBμV
V_{LISN} *(V)*	1.9 mV	530 μV	6.232 mV	13.07 mV
I_{cm} *(A)*	76.14 μA	21.2 μA	249.6 μA	531 μA

and therefore, most of the common-mode current in Table 3-3 is from the load path analyzed in previous sections. Comparing this to estimation and simulation value is shown in Table 3-4. It can be seen that the common-mode current in an experiment is relatively small compare to the estimated and simulated value. This is because the exact impedance in the common-mode path is hard to estimate. In estimation and simulation results, it is assumed that the impedance between the load and the input of

TABLE 3-4. COMPARISON BETWEEN ESTIMATION, SIMULATION AND EXPERIMENTAL RESULT WHEN ZB = 0

	Balanced Class E Converter		Conventional Class E Converter	
	Fundamental	2nd Harmonic	Fundamental	2nd Harmonic
Estimation	277 μA	103 μA	613.2 μA	900 μA
Simulation	306 μA	106 μA	603.2 μA	895 μA
Experiment	76.14 μA	21.2 μA	249.6 μA	531 μA

the DC/DC converter is around 3000 Ω, which is the impedance of the common-mode filter. However, due to the parasitic component, this impedance value is not exact. Therefore, in reality, the impedance may be larger than anticipated and more studies are required to estimate the common-mode current correctly in the real world.

Touch current is also measured using a body impedance model. Fig. 2-3 shows the body impedance circuit used in the experiment, and Fig. 3-21 shows the voltage waveforms of input grid voltage V_g and touch current measurement V_t. It can be seen that the peak V_t value is 45 mV which results in a touch current of 90 μA. The root means square value of V_{tc} is 18.8 mV_{rms}, which is 37.4 μA_{rms} touch current. From equation (3-28), the root mean square of the touch current equation is

$$I_{TC,rms} = \frac{\omega_g C_Y V_{g,pk}}{2} \qquad (3-28)$$

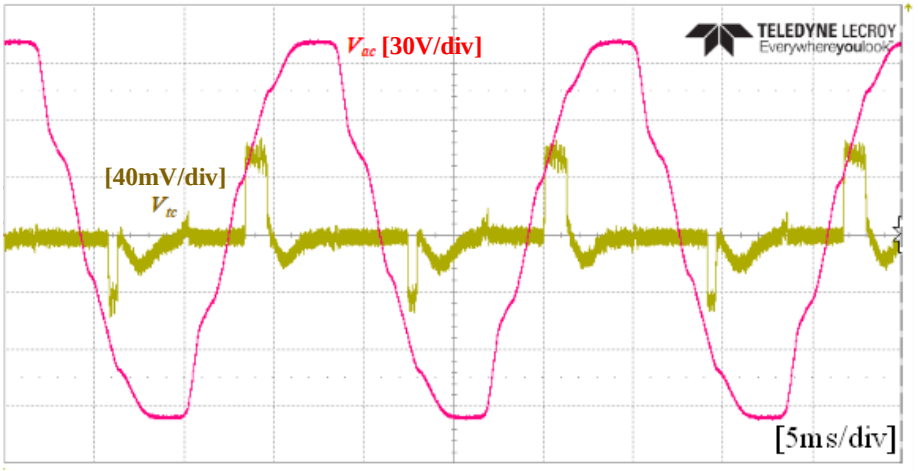


Fig. 3-21. Touch current waveforms

Taking C_Y = 2.9 nF, $V_{g,pk}$ = 100 V and ω_g = 2π60 rad/s, touch current calculation result is 54.6 μA_{rms}. The experimental result is smaller than the calculated result since a passive diode rectifier is used instead of PFC, reducing the grid voltage seen from the common mode.

4. Common Mode Current in Class E Converter with T-model Network

4.1 Two-port Network Design

In a conventional magnetically isolated converter, the turn-ratio of the transformer is used to set DC/DC converter conversion gain. Since the transformer is absent from the capacitive isolated converter, an alternative method to set the conversion gain is required. A two-port passive network is used in a resonant converter for impedance conversion [42]-[45]. This network will be used to set the conversion gain, and the design method for a two-port passive network for a capacitive isolated converter is proposed.

Assuming the network is lossless, a two-port network satisfies the following equation

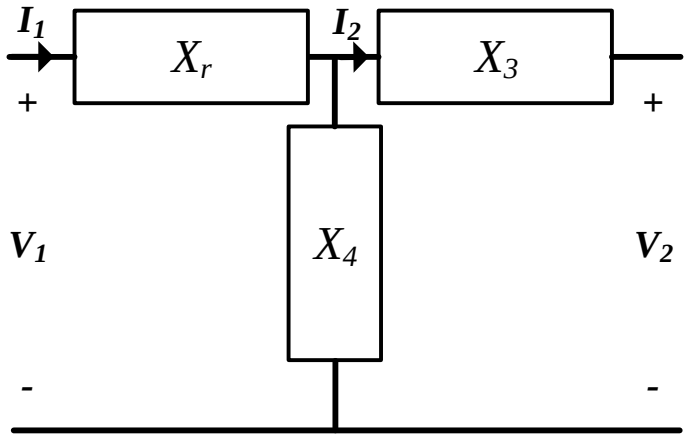


Fig. 4-1. T-model based two-port network.

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = j \begin{bmatrix} X_{11} & X_{12} \\ X_{12} & X_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ -I_2 \end{bmatrix}, \quad (4-1)$$

where V_1 and I_1 are the input voltage and current and V_2 and I_2 are output voltage and current. The value of $X_{11}, X_{12,}$ and X_{22} depends on the type of two-port passive network. The T-equivalent model shown in Fig. 4-1 is often used, and the impedance value of each branch can be calculated as

$$\begin{aligned} X_r &= X_{11} - X_{12} \\ X_3 &= X_{22} - X_{12} \\ X_4 &= X_{12} \end{aligned} . \quad (4-2)$$

Using the above equation, impedance conversion can be calculated. If an output impedance is $V_2/I_2 = R_o + jX_o$ then input impedance $V_1/I_1 = R_i + \mathrm{j}X_i$ becomes

$$\begin{aligned} R_i &= \frac{X_4{}^2 R_o}{R_o{}^2 + (X_3 + X_4 + X_o)^2}, \\ X_i &= X_r + X_4 - \frac{X_4{}^2 (X_3 + X_4 + X_o)}{R_o{}^2 + (X_3 + X_4 + X_o)^2} \end{aligned} \quad (4-3)$$

where R_i is a resistive part of the input impedance and X_i is a reactance part of the input impedance. Setting converter conversion gain $m = V_1/V_{2,}$ the above equations can be rewritten to

$$R_i = m^2 R_o = \frac{X_4{}^2 R_o}{R_o{}^2 + (X_3 + X_4 + X_o)^2}, \quad (4-4)$$

$$X_i = -\frac{X_o}{R_o} R_i = \frac{-X_4{}^2 X_o}{R_o{}^2 + (X_3 + X_4 + X_o)^2} \\ = X_r + X_4 - \frac{X_4{}^2 (X_3 + X_4 + X_o)}{R_o{}^2 + (X_3 + X_4 + X_o)^2} \quad , \qquad (4-5)$$

Then following equations can be derived

$$m^2 = \frac{X_4{}^2}{R_o{}^2 + (X_3 + X_4 + X_o)^2} \qquad (4-6)$$

$$X_r + X_4 = m^2 (X_3 + X_4) \qquad (4-7)$$

Since there are three unknown variables and only two equations, there is one degree of freedom to design a two-port network. In this paper, this degree of freedom will be used to minimize the size of the network. The index often used to determine a network's physical size is the ratio of total reactive power to active power [23], as shown in the equation below

$$g_Q = \frac{\sum |Q_{Ln}| + \sum |Q_{Cn}|}{P_i} = \frac{\sum |X_{Ln}||I_{Ln}|^2 + \sum |X_{Cn}||I_{Cn}|^2}{P_i} \qquad (4-8)$$

where P_i is an active power, X_{Ln} and I_{Ln} are impedance, and current of an n^{th} inductor in the network, and X_{Cn} and I_{Cn} are impedance and current of n^{th} capacitor in the network.

Fig. 4-2 shows two possible T-model-based network designs for class E DC/DC converter. First, LC series in a branch X_1 is needed to create resonant current to operate class E converter. Then, to minimize the network size, X_3 and X_4 are

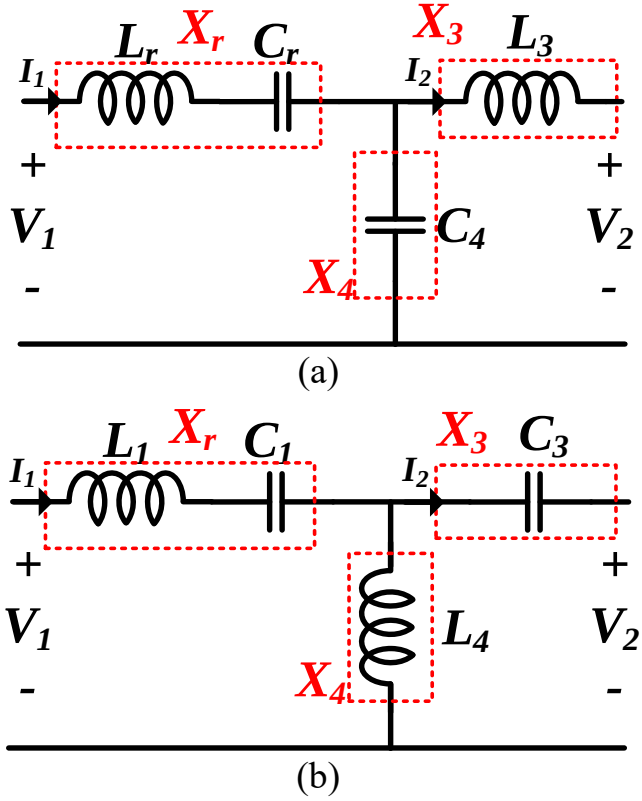


Fig. 4-2. Possible two-port network design

chosen to have a single component. However, it is not possible for X_3 and X_4 to either be both inductors or both capacitors. If X_3 and X_4 are both inductors, high DC current will flow to X_3 and X_4, while if X_3 and X_4 are both capacitors, high frequency circulating current will exist. Therefore, possible combinations are circuit shown in Fig.4-2.

Using Fig. 4-2 and equation (4-8), the physical size index g_Q of the network is

$$g_Q = \left\{ \left(\omega L_1 + \frac{1}{\omega C_1} \right) | I_1 |^2 + | X_4 | | I_1 - I_2 |^2 + | X_3 | | I_2 |^2 \right\} P_i^{-1} \quad (4-9)$$

where ω is a frequency where the network will be operated. If output impedance is set to $R_o + jX_o$ then I_1 and I_2 satisfies

$$I_1 = \left(\frac{X_o + X_3 + X_4 - jR_o}{X_4} \right) I_2 . \quad (4-10)$$

Substituting equations (4-6), (4-7), and (4-10) to equation (4-9), the index is simplified to

$$\frac{g_Q P_i}{|I_2|^2} = \frac{1}{m^2} \left\{ \left(\omega L_1 + \frac{1}{\omega C_1} \right) + \text{sign}(X_4) \left(\omega L_1 - \frac{1}{\omega C_1} \right) \right\} - 2\text{sign}(X_4)(X_3 + X_o) \quad (4-11)$$

where sign(X_4) is a plus-minus sign of reactance X_4. In this equation, sign(X_4) is a negative one in Fig. 4-2(a), and sign(X_4) is a positive one in Fig. 4-2(b). Therefore, equation (4-11) for Fig. 4-2 (a) and (b) can be calculated as

$$\frac{g_Q P_i}{|I_2|^2} = \begin{cases} 2\left\{ \dfrac{1}{m^2 \omega C_1} + (X_3 + X_o) \right\} & Fig.4-2(a) \\ 2\left\{ \dfrac{1}{m^2} \omega L_1 - (X_3 + X_o) \right\} & Fig.4-2(b) \end{cases} \quad (4-12)$$

Here $|I_2|$ is decided by the output power, and the LC tank's quality factor determines L_1 and C_1 value. Thus, the physical size index g_Q depends on $|X_3 + X_o|$. X_3 should satisfy equation (4-6) which can be rewritten as

$$\left(1-\frac{1}{m^2}\right)X_4{}^2+2(X_o+X_3)X_4+X_3{}^2+2X_oX_3+R_o{}^2+X_o{}^2=0$$

(4−13)

Since X_3 is a real value, the discriminant of equation (4−13) should be positive. Therefore, following inequality must hold

$$(1-m^{-2})(1+\frac{R_o{}^2}{(X_o+X_3)^2})\le 1. \qquad (4-14)$$

Using the above inequality, the minimum value of $|X_2|$ depending on the conversion gain m is

$$|X_3+X_o|_{\min}=\begin{cases}\sqrt{m^2-1}R_o & (m\ge 1)\\ 0 & (m<1)\end{cases}, \qquad (4-15)$$

where $|X_3+X_o|_{\min}$ is a minimum value of $|X_3+X_o|$. $|X_3+X_o|$ is positive when the network in Fig. 4−2 (a) is used and negative when the network in Fig. 4−2(b) is used. The network elements value X_3, X_4 and X_r are calculated for each network design. First, solutions are divided for a different range of output reactance X_o. Then network elements value for each network at Fig. 4−2(a) and (b) will be calculated as below

Network Fig.4−2 (a)

Condition 1: $m\ge 1$, $X_o\ge\sqrt{m^2-1}R_o$

In this condition, the value of X_3 where $|X_3+X_o|$ is minimum is zero for the network in Fig. 4−2(a). Therefore, substituting X_3 =

0 in equations (4−6) and (4−7) X_r and X_4 can be calculated as

$$X_3 = 0, X_4 = \frac{-m^2 X_o + m\sqrt{X_o{}^2 - R_o{}^2(m^2-1)}}{m^2-1}, \qquad (4-16)$$
$$X_r = -m^2 X_o + m\sqrt{X_o{}^2 - R_o{}^2(m^2-1)}$$

Condition 2: $m \geq 1$, $X_o < \sqrt{m^2-1}R_o$

In this condition, the value of X_3 where $|X_3 + X_o|$ is minimum is $\sqrt{m^2-1}R_o - X_o$. Therefore, substituting X_2 to equations (4−6) and (4−7) yields

$$X_3 = \sqrt{m^2-1}R_o - X_o, X_4 = \frac{-m^2 R_o}{\sqrt{m^2-1}}, \qquad (4-17)$$
$$X_r = -m^2 X_o$$

Network Fig.4−2 (b)

Condition 1: $m \geq 1$, $X_o < -\sqrt{m^2-1}R_o$

In this condition, the value of X_3 where $|X_3 + X_o|$ is minimum is zero. Therefore, substituting X_3 to equations (4−6) and (4−7) becomes

$$X_3 = 0, X_4 = \frac{-m^2 X_o - m\sqrt{X_o{}^2 - R_o{}^2(m^2-1)}}{m^2-1}, \qquad (4-18)$$
$$X_r = -m^2 X_o - m\sqrt{X_o{}^2 - R_o{}^2(m^2-1)}$$

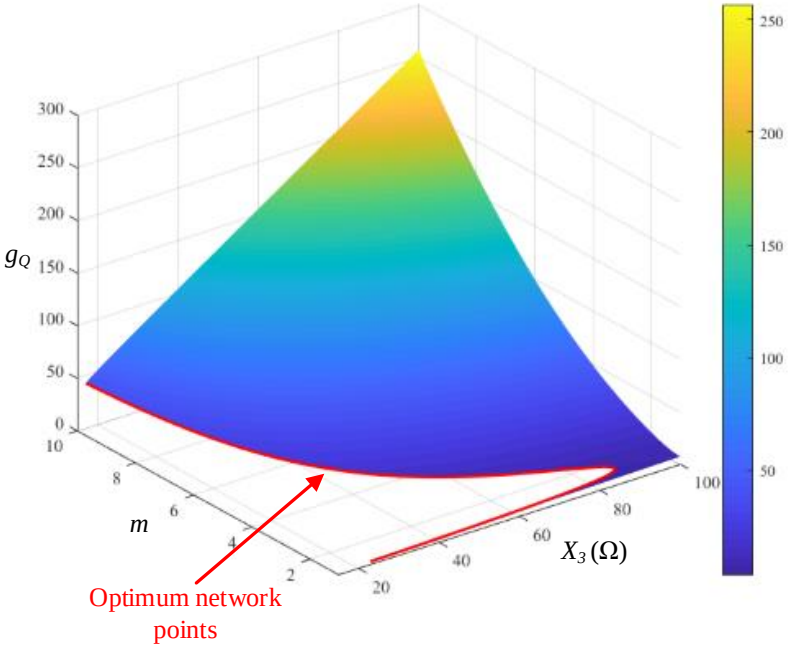
Condition 2: $m \geq 1$, $X_o \geq -\sqrt{m^2-1}R_o$

In this condition, the value of X_3 where $|X_3 + X_o|$ is minimum is $\sqrt{m^2-1}R_o - X_o$. Therefore, substituting X_3 to equations (4−6) and

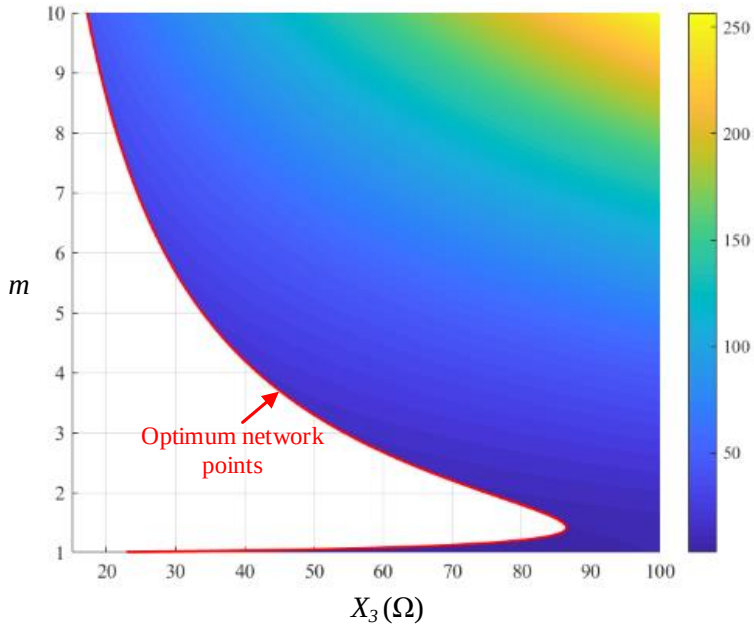
(4−7) yields

$$X_3 = -\sqrt{m^2 - 1}R_o - X_o, X_4 = \frac{m^2 R_o}{\sqrt{m^2 - 1}}, \qquad (4-19)$$
$$X_r = -m^2 X_o$$

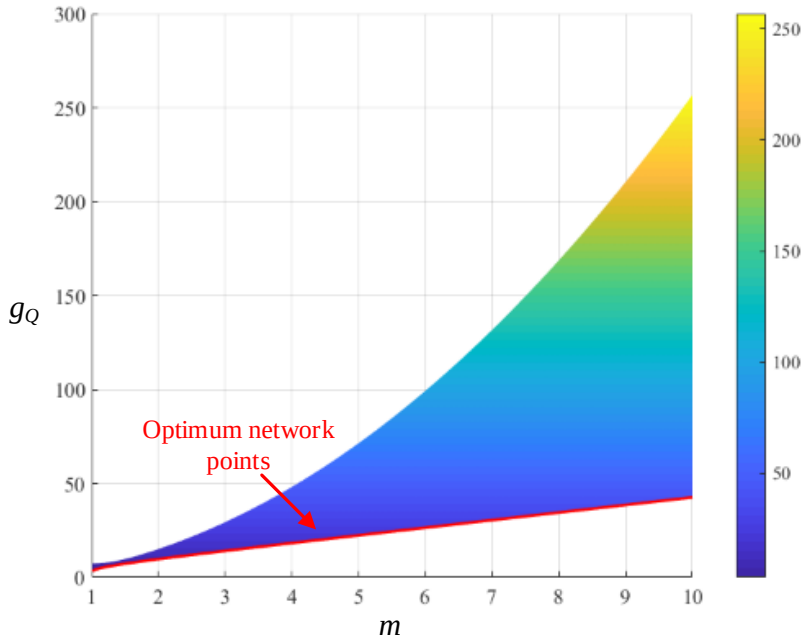
To see above condition has minimum g_Q, all g_Q value is calculated for all different conversion gain m. Fig. 4−3 shows the size index value g_Q of the network shown in Fig. 4−2(a) for different conversion gain m and reactance X_3. In this figure, fixed values are input power P_i = 65 W and peak AC input voltage V_I = 150 V. Also, for simplicity, output reactance is set to zero. Then input and output resistance can be calculated as $R_i = m^2 R_o$ = 175 Ω. In this condition, if reactance X_3 and conversion gain m are decided, reactance X_r and X_4 can be calculated using equations (4−6) and (4−7). The size index g_Q for all these networks is plotted in Fig. 4−3(a). The red line in the figure is the two−port network design using equations (4−17). Fig. 4−3(b) shows the plot of Fig.4−3(a) seen from the z−axis. The area in white is where X_4 has no real solution in equation (4−13); therefore, no real two−port network design is possible. Here the optimum network design plotted as redline lies on the boundary.


g_Q
300
250
200
150
100
50
0
10
8
6
4
2
m
20
40
60
80
100
$X_3\,(\Omega)$
250
200
150
100
50
Optimum network points

(a)

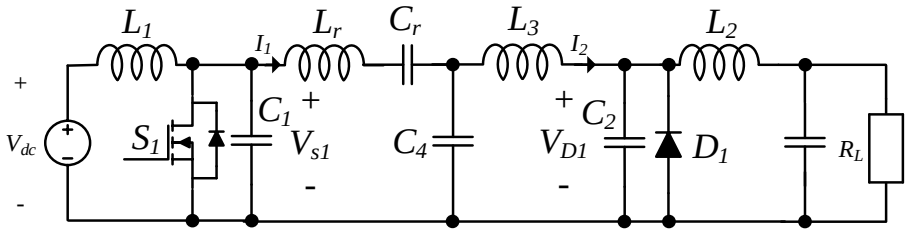

m
10
9
8
7
6
5
4
3
2
1
20
30
40
50
60
70
80
90
100
$X_3\,(\Omega)$
250
200
150
100
50
Optimum network points

(b)

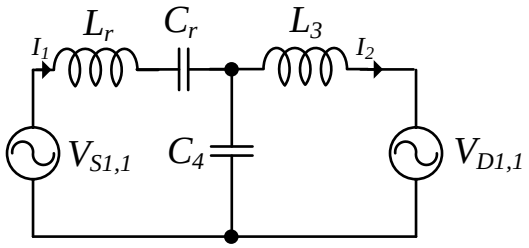


(c)

Fig. 4-3. Size index g_Q for different conversion gain m and X_3 branch reactance (a) x-axis is set to X_3, y-axis is set to m and z-axis is set to g_Q (b) plot seen from z-axis (c) plot seen from x-axis



(a)



(b)

Fig. 4-4. (a) A class E converter with two-port network (b) the fundamental term modeling of (a).

Fig. 4-3(c) shows the plot from the angle where network size index g_Q for different conversion gain m can be seen. The network in redline calculated with equation (4-13) has the smallest size index value for all m values and is, therefore, an optimum network. It can also be seen that the optimum physical size index g_Q increase linearly as the conversion ratio m increases. If the maximum physical index of the network is set, the maximum conversion ratio m possible can be calculated.

A class E converter with a two-port network is shown in Fig. 4-4. Fig. 4-4(b) shows the model of only the fundamental component of the class E converter with a two-port network. Both currents, I_1 and I_2 are assumed to be sinusoidal, as shown in the equation below

$$I_1 = I_{rm,1}\sin(\omega_s t + \varphi_1), I_2 = I_{rm,2}\sin(\omega_s t + \varphi_2) \qquad (4-20)$$

where φ_1 and φ_2 are the phases of the currents I_1 and I_2. Then the voltage equation of the fundamental component of V_{S1} and V_{D1} can be written as

$$\begin{aligned} V_{S1,1} &= |V_{S1,1}|\sin(\omega_s t + \varphi_1 + \varphi_{S1,1}), \\ V_{D1,1} &= |V_{D1,1}|\sin(\omega_s t + \varphi_2 + \varphi_{D1,1}) \end{aligned} \qquad (4-21)$$

where $|V_{S1,1}|$ and $|V_{D1,1}|$ are the magnitude of a fundamental component of class E inverter and rectifier voltage, $\Psi_{S1,1}$ is a phase difference compared to current I_1, and $\Psi_{D1,1}$ is a phase

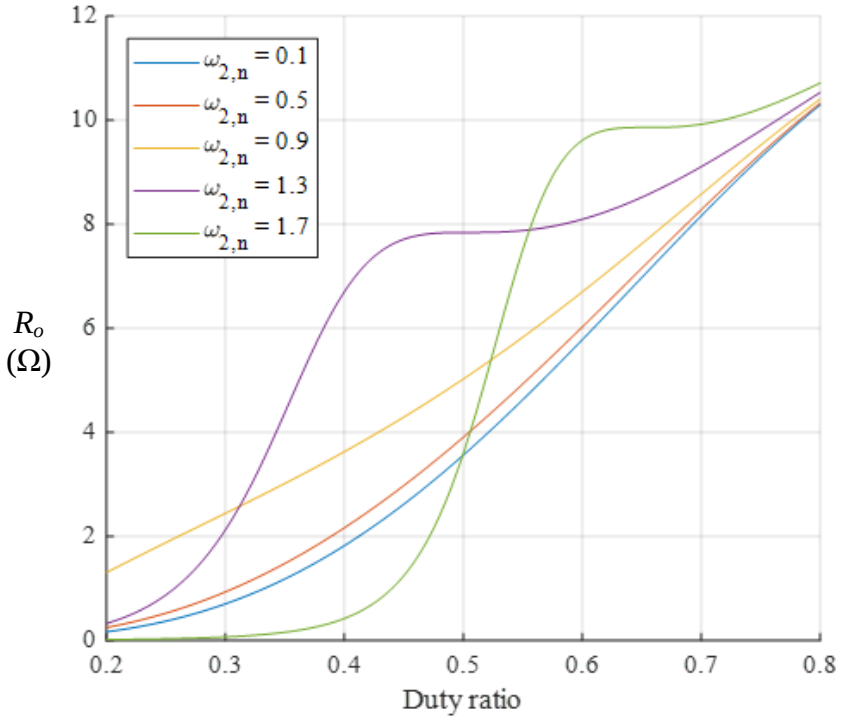
difference compare to current I_2. The magnitude and phase of the inverter and rectifier voltage depending on L_1, C_1 L_2, C_2 and duty ratio can be calculated using Fig. 2-22 – Fig. 2-24. If the conversion gain of the network is set to m, then the inverter and rectifier voltage satisfies below equation

$$|V_{S1,1}| = m|V_{D1,1}|. \quad (4-22)$$

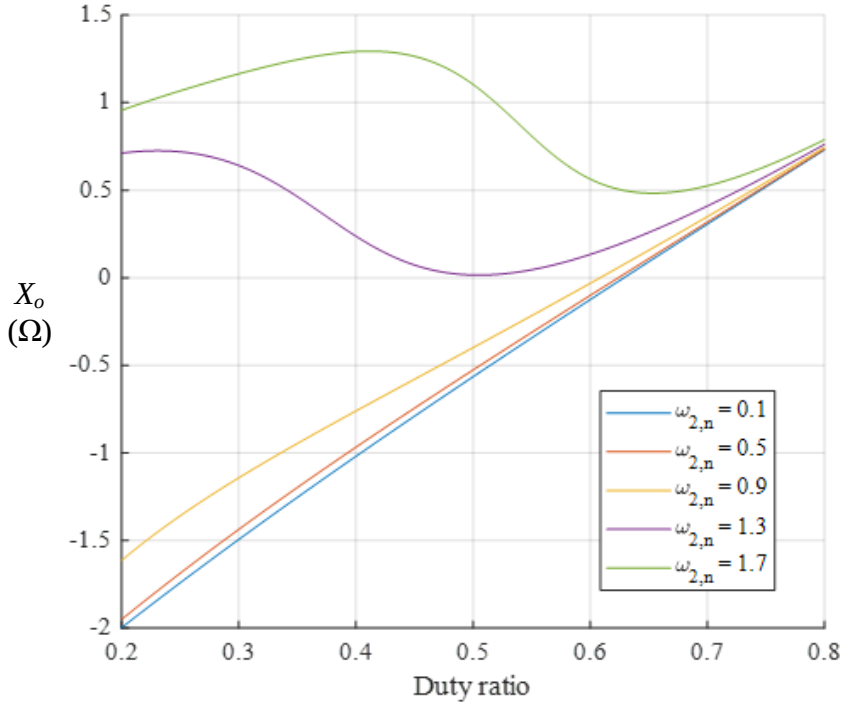
If both inverter and rectifier have the same duty ratio and $\omega_{1,n} = \omega_{2,n}$, then

$$\frac{|V_{S1,1}|}{V_{dc}} = \frac{|V_{D1,1}|}{V_o} \quad (4-23)$$

where V_{dc} is an input voltage and V_o is an output voltage of class E DC/DC converter. According to equations (4-22) and(4-23), if the inverter and rectifier are designed with the same duty ratio and $\omega_{1,n} = \omega_{2,n}$ then V_{dc}/V_o equals m when two-port network is designed with conversion gain m.



(a)



(b)

Fig. 4-5. Output impedance of the class E rectifier (a) resistance (b) reactance

The output impedance $Z_o = V_{D1,1}/I_2 = R_o + jX_o$ of the network used in the class E converter at switching frequency should be known to design the network. Assuming rectifier is lossless, output resistance R_o should satisfy below equation,

$$\frac{R_o I_{rm,2}^{\ 2}}{2} = \frac{V_o^{\ 2}}{R_L}. \qquad (4-24)$$

Using $K = Z_2 I_{rm,2} / V_o$ calculated at equation (2−16) where Z_2 is equal to $\sqrt{L_2 / C_2}$ the output resistance R_o can be calculated as

$$R_o = \frac{1}{R_L}\frac{2Z_2^{\ 2}}{K^2}. \qquad (4-25)$$

The output reactance X_o then can be calculated using phase difference $\Psi_{D1,1}$ between current I_2 as shown in the equation below

$$X_o = R_o \tan(\psi_{D1,1}). \qquad (4-26)$$

Using these equations, the output impedance of the class E rectifier in fundamental frequency can be calculated. Fig. 4−5 shows the resulting R_o and X_o value of class E rectifier for different $\omega_{2,n,}$ and duty ratio values. Here V_o = 20 V and P_o = 65 W. It can be seen that the resistance of output impedance R_o increases as the duty ratio of the rectifier increases. If $Z_i = R_i + jX_i = m^2(R_o - jX_o)$ as stated in equation (4−4) and (4−5) then

$$R_i = m^2 R_o = \frac{2m^2 Z_2^{\ 2}}{K^2 R_L} \qquad (4-27)$$

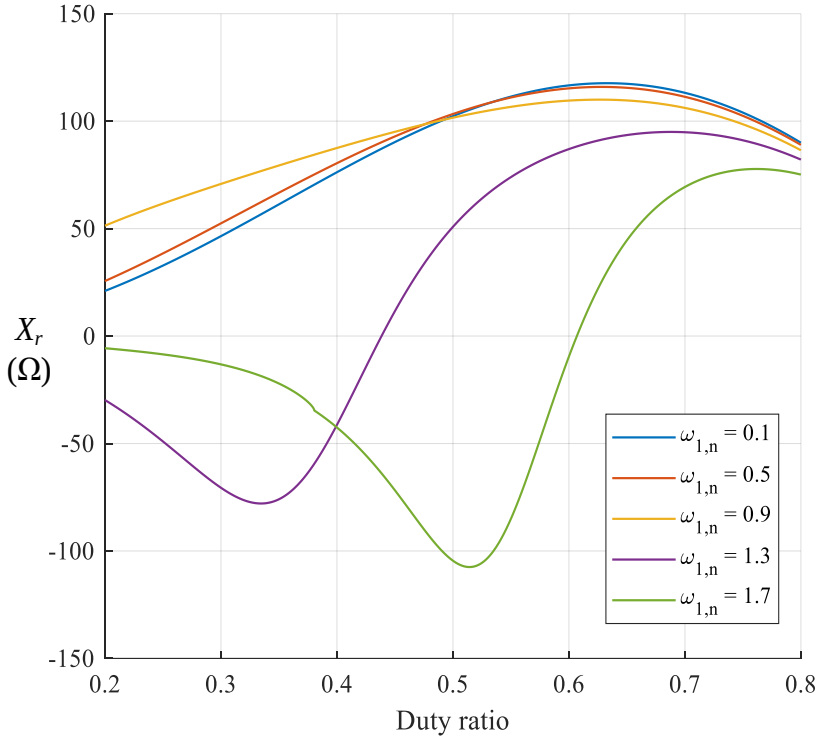
$$X_i = -m^2 R_o \tan(\psi_{D1,1}) \qquad (4-28)$$

Assuming network in Fig.4−2 (a) is used, the calculated result for X_r, X_3, and X_4 are shown in Fig. 4−6 where V_o = 20 V, m = 5, and P_o = 65 W. The phase difference between current I_1 and I_2 $\varphi_1 - \varphi_2$ can also be calculated using equations (4−10). The phase difference between I_1 and I_2 is

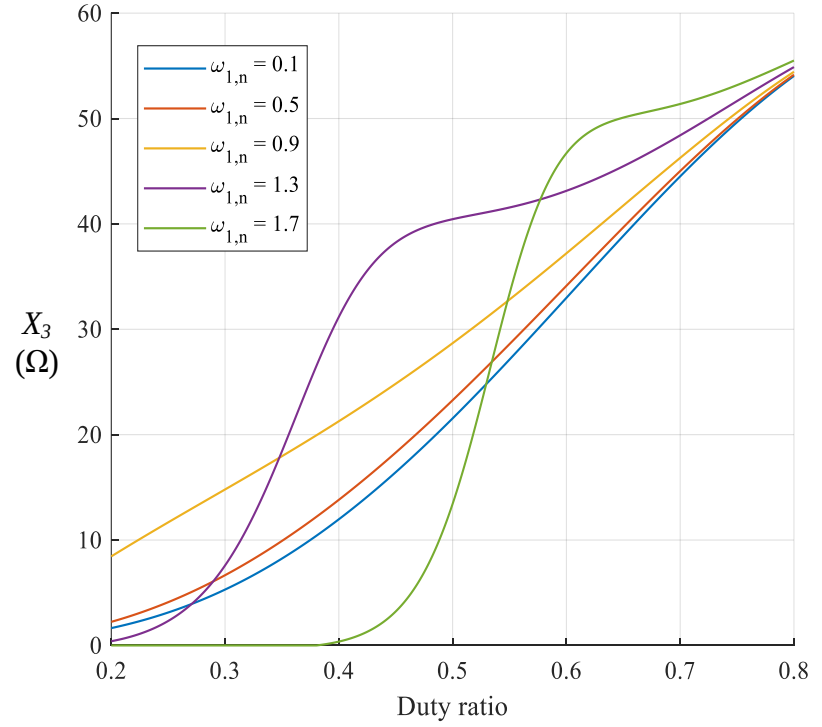
$$\tan(\varphi_1 - \varphi_2) = \frac{-R_o}{X_o + X_3 + X_4}. \qquad (4-29)$$

Using equations (4−16) – (4−19), the above equations can be rewritten using conversion gain value m and output impedance R_o and X_o. When the network in Fig. 4−2(a) is used, the equation (4−29) can be rewritten as

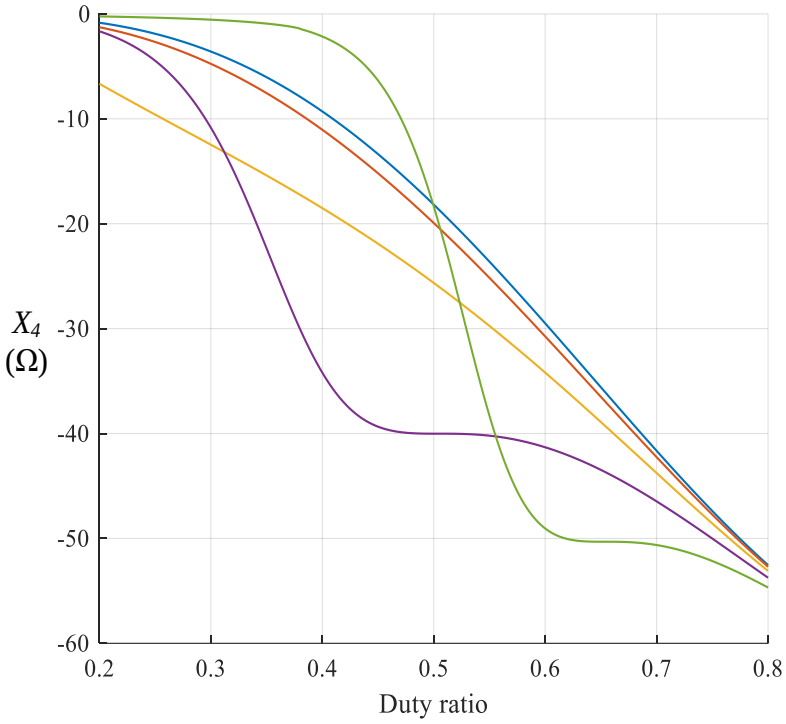
$$\tan(\varphi_1 - \varphi_2) = \begin{cases} \dfrac{(m^2-1)R_o}{X_o - m\sqrt{X_o{}^2 - (m^2-1)R_o{}^2}} & \left(m \geq 1, X_o \geq \sqrt{m^2-1}R_o\right) \\ \sqrt{m^2-1} & \left(m \geq 1, X_o < \sqrt{m^2-1}R_o\right) \end{cases}. \qquad (4-30)$$


150
100
50
0
-50
-100
-150
X_r
(Ω)
0.2
0.3
0.4
0.5
0.6
0.7
0.8
Duty ratio
$\omega_{1,n}$ = 0.1
$\omega_{1,n}$ = 0.5
$\omega_{1,n}$ = 0.9
$\omega_{1,n}$ = 1.3
$\omega_{1,n}$ = 1.7

(a)


60
50
40
30
20
10
0
X_3
(Ω)
0.2
0.3
0.4
0.5
0.6
0.7
0.8
Duty ratio
$\omega_{1,n}$ = 0.1
$\omega_{1,n}$ = 0.5
$\omega_{1,n}$ = 0.9
$\omega_{1,n}$ = 1.3
$\omega_{1,n}$ = 1.7

(b)



(c)

Fig. 4-6. Calculation of the reactance for two-port network elements placed in each branch (a) X_r (b) X_3 (c) X_4

4.2 Common Mode Current in Class E Converter

In this paper, the network, shown in Fig. 4-2(a), will be used to design a class E converter with a two-port network. Here two-port network with the conversion gain greater than one will be used, meaning the input voltage of the class E DC/DC converter is larger than the output voltage. The resulting class E converter is shown in Fig. 4-7.

The common-mode current of the class E converter with the two-port network is analyzed similarly to section 3.1. Using Kirchhoff's circuit law, $V_{cm,oc,}$ and $I_{cm,sc}$ can be calculated as

$$V_{cm,oc}(s) = \frac{X_{th}\{(X_3+X_4)V_{S1}(s) - X_4 V_{D1}(s)\}}{(X_3+X_4)X_{r1} + X_3X_4} \qquad (4-31)$$

$$I_{cm,sc}(s) = \frac{(X_3+X_4)V_{S1}(s) - X_4 V_{D1}(s)}{(X_3+X_4)X_{r1} + X_3X_4} \qquad (4-32)$$

$$X_{th} = \frac{X_{r2}\left(X_{r1} + \dfrac{X_3X_4}{X_3+X_4}\right)}{X_{r1} + X_{r2} + \dfrac{X_3X_4}{X_3+X_4}}$$

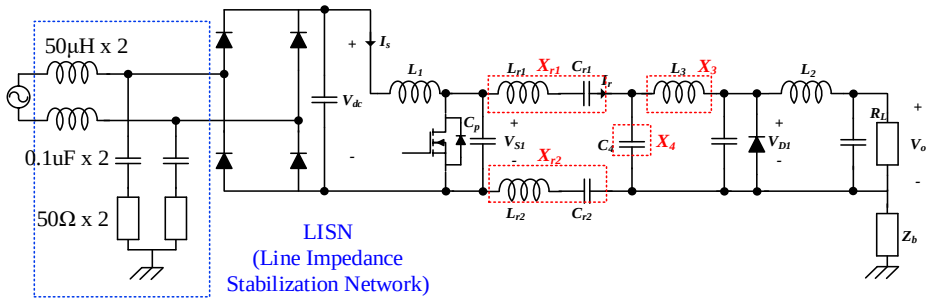


Fig. 4-7. Capacitive Isolated Class E Converter with two-port network

where X_{r1}, X_{r2}, X_3 and X_4 are reactance of each network elements as shown in Fig.4−7 and $X_r = X_{r1} + X_{r2}$. Using these equations, $I_{cm,sc}$ at each frequency will be calculated. The resulting Thevenin and Norton equivalent circuit is shown in Fig.4−8. The calculated magnitude of $I_{cm,sc}$ is

$$|I_{cm,sc}(j\omega_s)| = \left| \frac{(X_3 + X_4)|V_{S1,1}|\angle(\psi_{S1,1} + \varphi_1) - X_4 |V_{D1,1}| \angle(\psi_{D1,1} + \varphi_2)}{(X_3 + X_4)X_{r1} + X_3 X_4} \right| \quad (4-33)$$

$$|I_{cm,sc}(j2\omega_s)| = \left| \frac{(X_3 + X_4)|V_{S1,2}|\angle(\psi_{S1,2} + 2\varphi_1) - X_4 |V_{D1,2}| \angle(\psi_{D1,2} + 2\varphi_2)}{(X_3 + X_4)X_{r1} + X_3 X_4} \right| \quad (4-34)$$

In this paper, the duty ratios of the inverter and rectifier are the same, and $\omega_{1,n} = \omega_{2,n}$. Also, the two−port network is designed with a conversion gain m. Then $|V_{s1,n}| = m|V_{D1,n}|$ and therefore above equations can be rewritten as

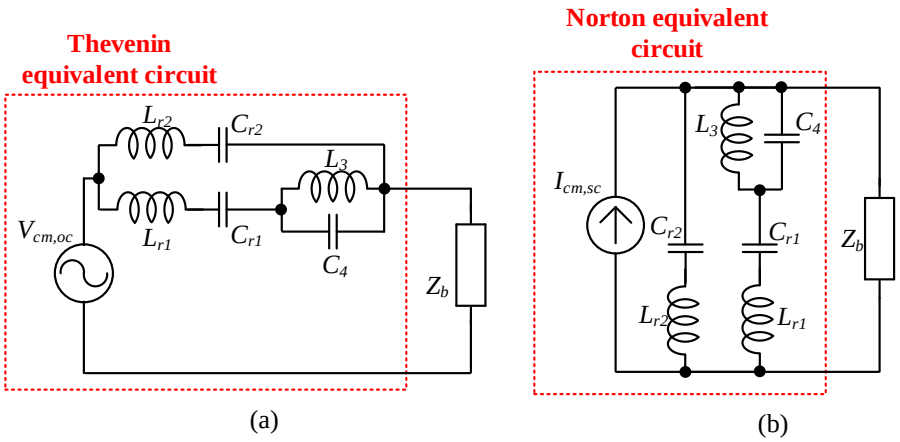
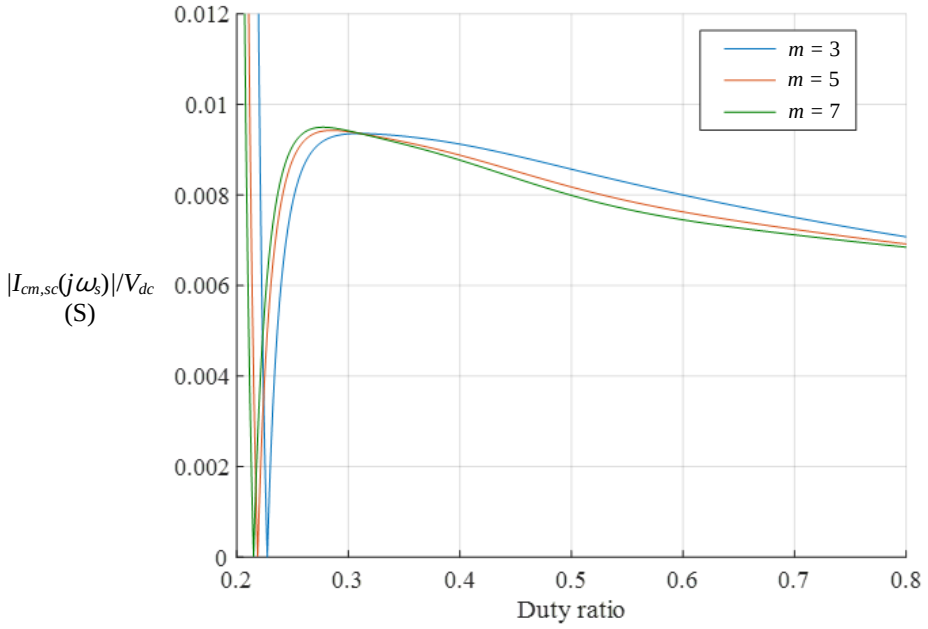


Fig. 4−8. Common mode equivalent circuit (a) Thevenin equivalent circuit (b) Norton equivalent circuit

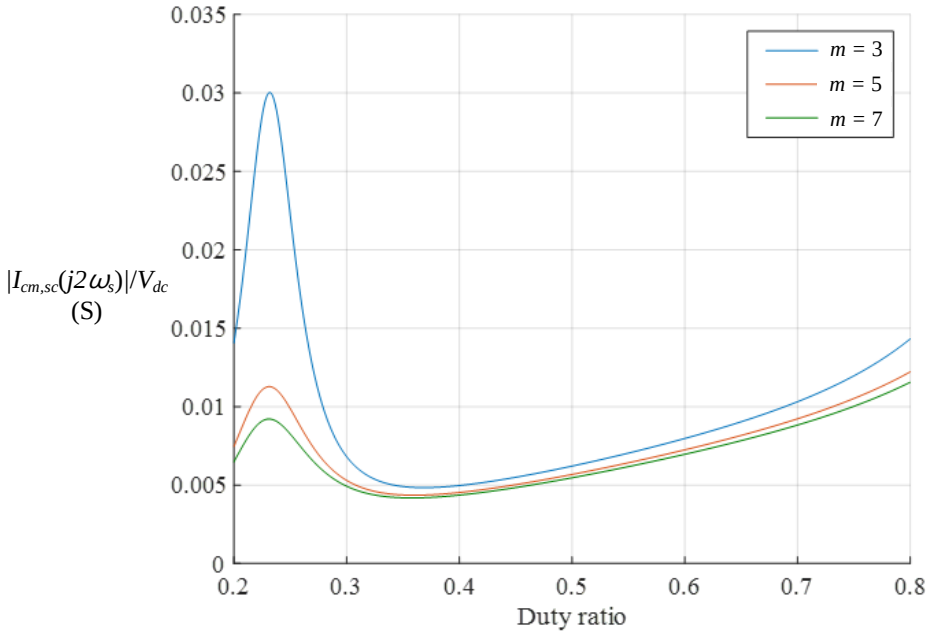
$$\frac{|I_{cm,sc}(j\omega_s)|}{|V_{S1,1}|} = \frac{\sqrt{(X_4+X_3)^2 + \frac{X_4^{\,2}}{m^2} - \frac{2}{m}X_4(X_4+X_3)\cos(2\psi_{S1,1}+\varphi_1-\varphi_2)}}{\left|(X_3+X_4)X_{r1}+X_3X_4\right|} \quad (4-35)$$

$$\frac{|I_{cm,sc}(j2\omega_s)|}{|V_{S1,2}|} = \frac{\sqrt{(X_4+X_3)^2 + \frac{X_4^{\,2}}{m^2} + \frac{2}{m}X_4(X_4+X_3)\cos(2\psi_{S1,2}+2\varphi_1-2\varphi_2)}}{\left|(X_3+X_4)X_{r1}+X_3X_4\right|} \quad (4-36)$$

Fig.4-9 shows the ratio of common-mode short-circuit current divided by input voltage $|I_{cm,sc}(jn\omega_s)|/V_{dc}$ value depending on the duty ratio. Different network element is used for each duty ratio while $(V_{dc})^2/P_o = 150\,\Omega$ and $\omega_{1,n} = 1.14$. Like a class E converter with an LC series network, there is a point where the fundamental term of $I_{cm,sc}$ is equal to zero. This point is where the nominator of equation (4-35) is equal to zero.



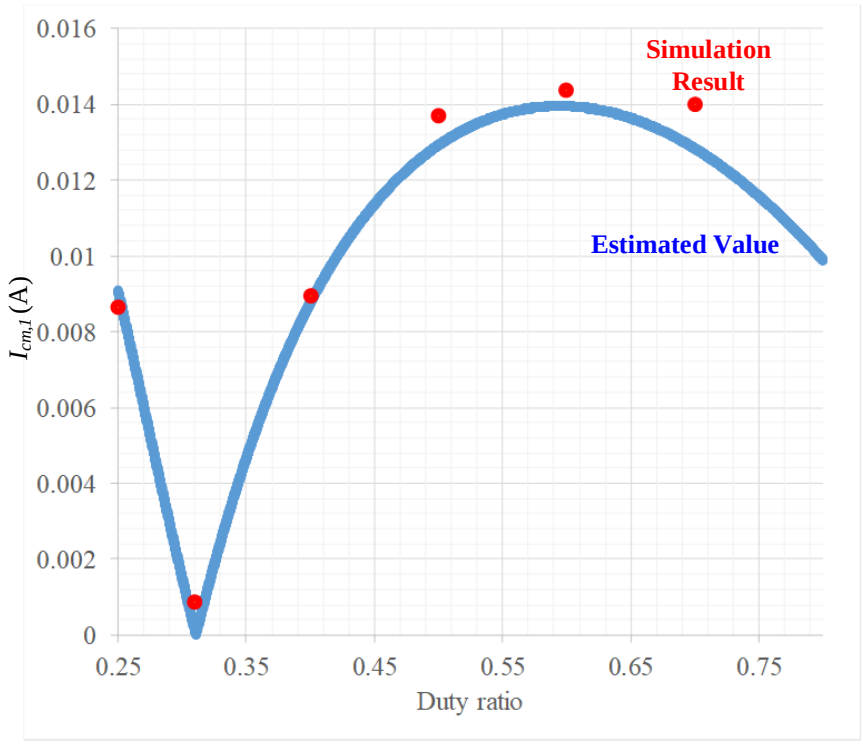
(a)



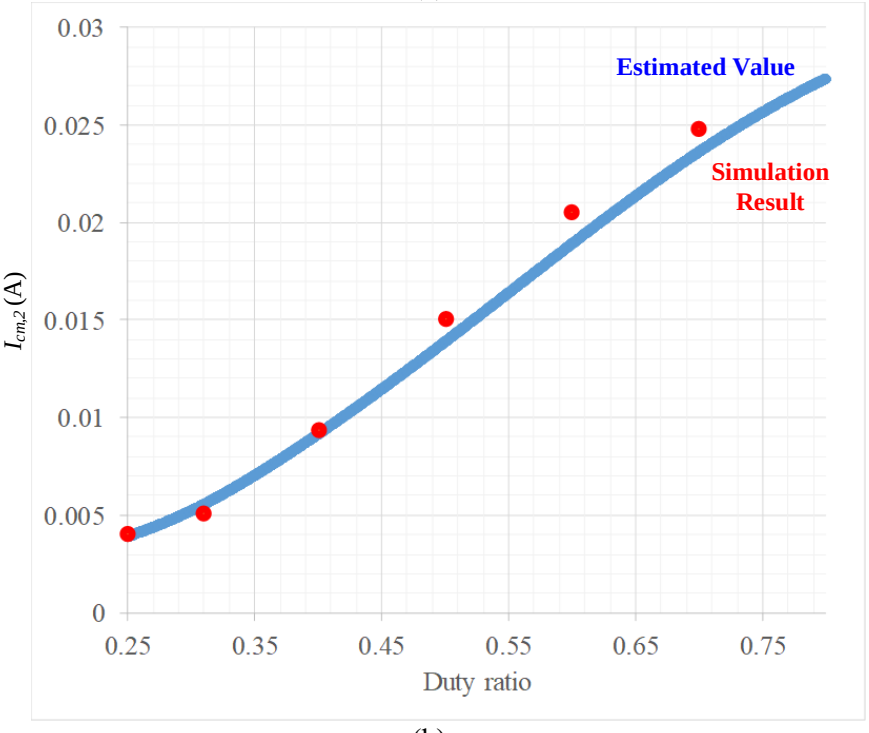
(b)

Fig. 4-9. Common-mode short circuit current in class E converter with two-port network (a) fundamental (b) 2nd harmonic

Using equation (3-7), a common-mode current can be calculated using a common-mode short circuit current. Fig. 4-10 shows the value of fundamental and second harmonic common-mode current when Z_b equals 3000 Ω. The blue line represents the estimated common-mode current value using equations (4-35) and (4-36), and red dots represent the measurement of common-mode current using simulation. The error between the estimated and simulation values increases as the duty ratio increases, similar to Fig. 3-6 due to harmonic currents to class E converter operation.



(a)



(b)

Fig. 4-10. Common-mode current in class E converter with two-port network (a) fundamental (b) 2nd harmonic

4.3 Common-Mode Current in a Balanced Class E Converter

The two-port network should also be balanced when designing a balanced class E converter to reduce the high-frequency common-mode current. Therefore, T-model based network should be modified, as shown in Fig. 4-11. This network divides branches and therefore shares the same physical size

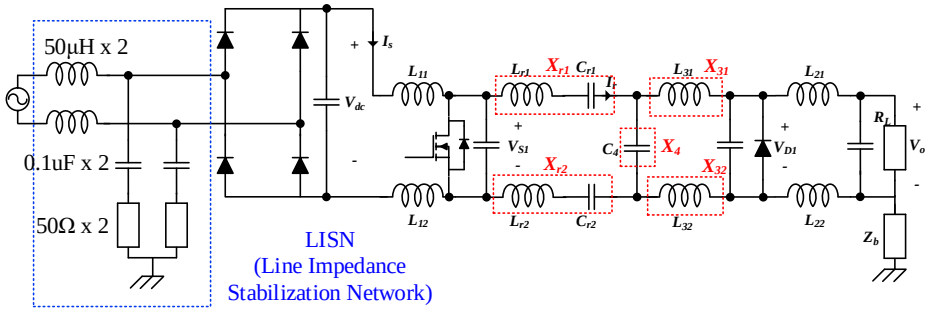


Fig. 4-11. Balanced class E converter with two-port network

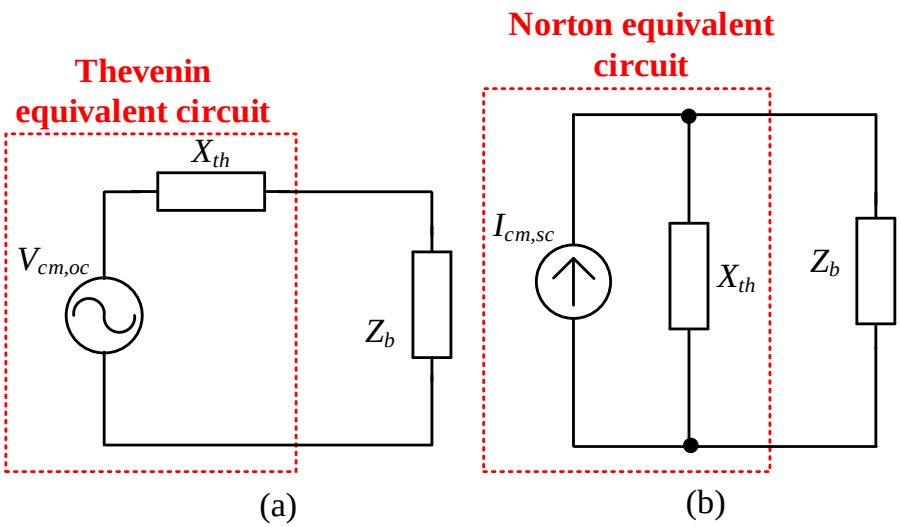


Fig. 4-12. Common-mode equivalent circuit of a balanced class E converter with two-port network. Xth is calculated in equation (4-39) (a) Thevenin equivalent circuit (b) Norton equivalent circuit

index g_Q with T-model based network. When this network is implemented, Thevenin and Norton equivalent circuits are redrawn to Fig. 4-12. Here $V_{cm,oc}$, $I_{cm,sc,}$ and X_{th} are calculated as

$$V_{cm,oc}(s) = \left(\frac{X_{r2}X_{33} + (X_{r2} + X_{32})X_4}{X_{r3}X_{33} + (X_{r3} + X_{33})X_4} - \frac{L_{12}}{L_{11} + L_{12}} \right) V_{S1}(s) - \left(\frac{X_{r3}X_{32} + (X_{r2} + X_{32})X_4}{X_{r3}X_{33} + (X_{r3} + X_{33})X_4} - \frac{L_{22}}{L_{21} + L_{22}} \right) V_{D1}(s) \quad (4-37)$$

$$I_{cm,sc}(s) = \frac{1}{X_{th}} V_{cm,oc}(s) \quad (4-38)$$

$$X_{th} = \frac{X_{r1}X_{r2}X_{33} + X_{r3}X_{31}X_{32} + (X_{r2} + X_{32})(X_{r1} + X_{33})X_4}{X_{r3}X_{33} + (X_{r3} + X_{33})X_4} \quad (4-39)$$

where $X_{r3} = X_{r1} + X_{r2}$ and $X_{33} = X_{31} + X_{32}$. It can be seen from above equation, $I_{cm,sc}$ is zero when $L_{11} = L_{12}$, $L_{r1} = L_{r2}$, $C_{r1} = C_{r2}$, $L_{31} = L_{32}$ and $L_{21} = L_{22}$.

Monte-Carlo simulation is used to analyze the effect of

TABLE 4-1. CLASS E CONVERTER WITH TWO-PORT NETWORK PARAMETERS USED IN SIMULATION AND EXPERIMENTS

Parameters	Value	Parameter tolerance
L_{11} & L_{12}	300 [nH]	±2%
L_{r1} & L_{r2}	798 [nH]	±2%
C_{r1} & C_{r2}	220 [pF]	±10%
L_{21} & L_{22}	47 [nH]	±2%
C_4	220 [pF]	±2%
L_{31} & L_{32}	300 [nH]	±2%
C_1	200 [pF]	
C_2	1.3 [nF]	
f_s	12.14 [MHz]	
R_L	6.25 [Ω]	

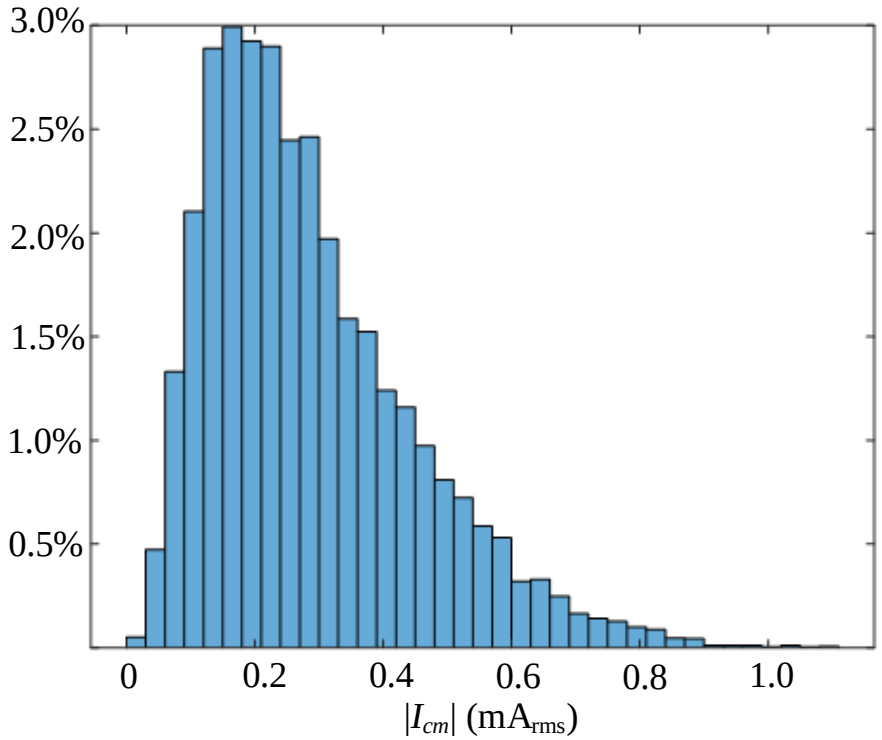


Fig. 4-13. Histogram of common-mode current in a balanced class E converter with two-port network when parameter tolerance is considered

parameter error in a common-mode current. The simulation parameter and parameter tolerance are shown in Table 4.1. Inductors have a tolerance of 2%, while capacitors have a tolerance of 10%, chosen based on parameter tolerance of commercial components. The simulation is run 10,000 times, and the histogram of the root mean square value of a common-mode current is shown in Fig. 4-13. The maximum common-mode current is 1.12 mA, while the most probable common-mode current value is between 150 μA and 180 μA.

The maximum common-mode current considering

parameter error is also calculated. Each parameter considering parameter error rewritten as below

$$L_{11} = L_1(1+\lambda_{11}), L_{12} = L_1(1+\lambda_{12}), L_{21} = L_2(1+\lambda_{21}), L_{22} = L_2(1+\lambda_{22})$$
$$X_{r1} = X_r(1+\lambda_{r1}), X_{r2} = X_r(1+\lambda_{r2}), L_{31} = L_3(1+\lambda_{31}), L_{32} = L_3(1+\lambda_{32})$$

(4−40)

where λ is a parameter error tolerance value with a few hundredths value. This parameter error tolerance value is then rewritten as a polar coordinate value using equations (3−12). Then the equation (4−37) can be rewritten as

$$\frac{|V_{cm,oc}(jn\omega_s)|^2}{|V_{S1,1}|^2}$$
$$= \left(K_1(jn\omega_s) - \frac{1+\lambda_1 \sin\theta_1}{2+\eta_1} \right)^2 + \frac{1}{m^2}\left(K_2(jn\omega_s) - \frac{1+\lambda_2 \sin\theta_2}{2+\eta_2} \right)^2$$
$$- \frac{2}{m}\left(K_1(jn\omega_s) - \frac{1+\lambda_1 \sin\theta_1}{2+\eta_1} \right)\left(K_2(jn\omega_s) - \frac{1+\lambda_2 \sin\theta_2}{2+\eta_2} \right)$$
$$\cos(2\psi_{S1,n} + n(\varphi_1 - \varphi_2) + (n-1)\pi)$$

(4−41)

$$K_1 = \frac{X_r X_3\{2+2\lambda_r \sin\theta_r + \eta_3\} + X_4\{(X_r + X_3) + X_r\lambda_r \sin\theta_r + X_3\lambda_3 \sin\theta_3\}}{2X_r X_3\{2+\eta_r+\eta_3\} + X_4\{2(X_r+X_3) + X_r\eta_r + X_3\eta_3\}}$$

$$K_2 = \frac{X_r X_3\{2+\eta_r+2\lambda_3 \sin\theta_3\} + X_4\{(X_r + X_3) + X_r\lambda_r \sin\theta_r + X_3\lambda_3 \sin\theta_3\}}{2X_r X_3\{2+\eta_r+\eta_3\} + X_4\{2(X_r+X_3) + X_r\eta_r + X_3\eta_3\}}$$

where $\eta_k = \lambda_k(\sin\theta_k + \cos\theta_k)$ for k = 1, 2, 3 and r. It is assumed that λ_k values are all small, typically a few hundredth values, and therefore, to simplify the equation, λ_k^l, where l is greater than one,

is approximated to zero. To find out the worst scenario for the largest common mode current caused by parameter error, derivatives of equation (4-41) are then calculated as

$$\frac{d(|V_{cm,oc}|^2/|V_{S1,n}|^2)}{d\theta_1} \cong \frac{2\lambda_1(\sin\theta_1+\cos\theta_1)}{\{2+\eta_1\}^2}\left\{\left(K_1-\frac{1+\lambda_1\sin(\theta_1)}{2+\eta_1}\right) -\frac{1}{m}\left(K_2-\frac{1+\lambda_2\sin(\theta_2)}{2+\eta_2}\right)\cos(2\psi_{S1,n}+n(\varphi_1-\varphi_2)+(n-1)\pi)\right\} \quad (4-42)$$

$$\frac{d(|V_{cm,oc}|^2/|V_{S1,n}|^2)}{d\theta_2} \cong \frac{2\lambda_2(\sin\theta_2+\cos\theta_2)}{\{2+\eta_2\}^2}\left\{\frac{1}{m^2}\left(K_2-\frac{1+\lambda_2\sin(\theta_2)}{2+\eta_2}\right) -\frac{1}{m}\left(K_1-\frac{1+\lambda_1\sin(\theta_1)}{2+\eta_1}\right)\cos(2\psi_{S1,n}+n(\varphi_1-\varphi_2)+(n-1)\pi)\right\} \quad (4-43)$$

$$\frac{d(|V_{cm,oc}|^2/|V_{S1,n}|^2)}{d\theta_3} \cong \frac{2X_3\lambda_3(2X_rX_3+X_4(X_r+X_3))(\cos\theta_3+\sin\theta_3)}{\left[2X_rX_3(2+\eta_r+\eta_3)+X_4\{2(X_r+X_3)+X_r\eta_r+X_3\eta_3\}\right]^2} \left\{\left(\frac{X_4}{m^2}-\frac{2X_r+X_4}{m}\cos(2\psi_{S1,n}+n(\varphi_1-\varphi_2)+(n-1)\pi)\right)\left(K_2-\frac{1+\lambda_2\sin(\theta_2)}{2+\eta_2}\right) +\left(2X_r+X_4-\frac{X_4}{m}\cos(2\psi_{S1,n}+n(\varphi_1-\varphi_2)+(n-1)\pi)\right)\left(K_1-\frac{1+\lambda_1\sin(\theta_1)}{2+\eta_1}\right)\right\} \quad (4-44)$$

$$\frac{d(|V_{cm,oc}|^2/|V_{S1,n}|^2)}{d\theta_r}$$

$$\cong \frac{2X_r\lambda_r\{2X_rX_3+X_4(X_r+X_3)\}(\cos\theta_r+\sin\theta_r)}{\left[2X_rX_3(2+\eta_r+\eta_3)+X_4\{2(X_r+X_3)+X_r\eta_r+X_3\eta_3\}\right]^2}$$

$$\left\{\left(\frac{X_4}{m^2}-\frac{2X_3+X_4}{m}\cos(2\psi_{S1,n}+n(\varphi_1-\varphi_2)+(n-1)\pi)\right)\left(K_2-\frac{1+\lambda_2\sin(\theta_2)}{2+\eta_2}\right)\right.$$

$$\left.+\left(2X_3+X_4-\frac{X_4}{m}\cos(2\psi_{S1,n}+n(\varphi_1-\varphi_2)+(n-1)\pi)\right)\left(K_1-\frac{1+\lambda_1\sin(\theta_1)}{2+\eta_1}\right)\right\}$$

(4−45)

It can be seen that derivatives are all zero when $\cos(\theta_k)+\sin(\theta_k)=0$ for all $k=1, 2, 3$ and r. Therefore, substituting $\cos(\theta_k)+\sin(\theta_k)=0$ to equation (4−41) yields

$$\frac{|V_{cm,oc}(jn\omega_s)|^2}{|V_{S1,n}|^2}$$

$$=\left(K_{1,m}(jn\omega_s)-\frac{\lambda_1\sin\theta_1}{2}\right)^2+\frac{1}{m^2}\left(K_{2,m}(jn\omega_s)-\frac{\lambda_2\sin\theta_2}{2}\right)^2$$

$$-\frac{2}{m}\left(K_{1,m}(jn\omega_s)-\frac{\lambda_1\sin\theta_1}{2}\right)\left(K_{2,m}(jn\omega_s)-\frac{\lambda_2\sin\theta_2}{2}\right)$$

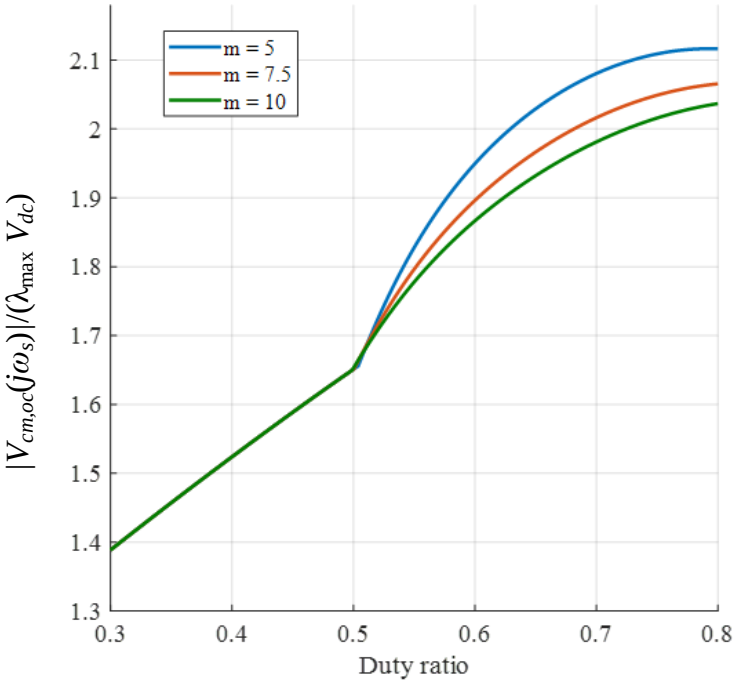
$$\cos(2\psi_{S1,n}+n(\varphi_1-\varphi_2)+(n-1)\pi)$$

(4−46)

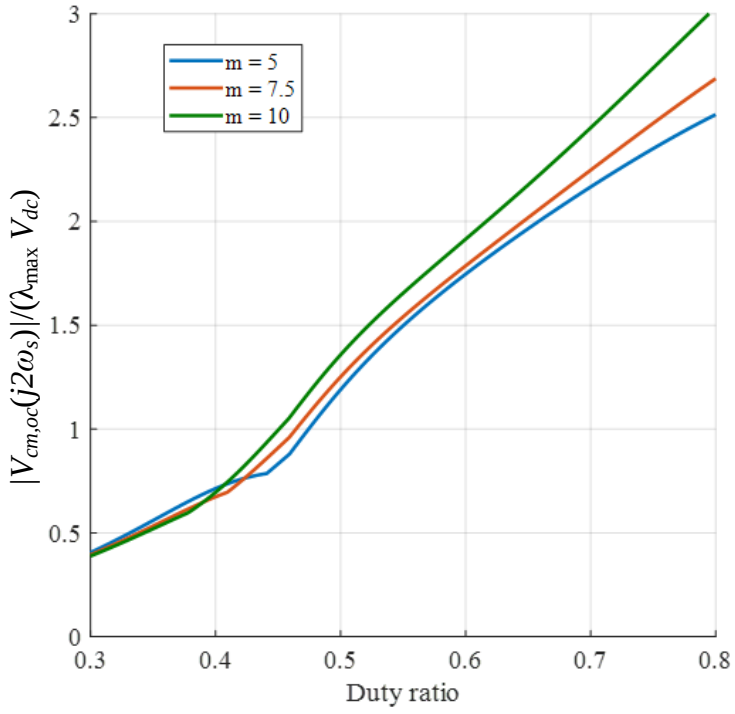
$$K_{1,m}=\frac{2X_rX_3\lambda_r\sin\theta_r+X_4\left(X_r\lambda_r\sin\theta_r+X_3\lambda_3\sin\theta_3\right)}{4X_rX_3+2X_4(X_r+X_3)}$$

$$K_{2,m}=\frac{2X_rX_3\lambda_3\sin\theta_3+X_4\left(X_r\lambda_r\sin\theta_r+X_3\lambda_3\sin\theta_3\right)}{4X_rX_3+2X_4(X_r+X_3)}$$

In equation (4−39), 16 possible solutions are available depending on the sign of $\sin(\theta_k)=\pm1/\sqrt{2}$ for every k = 1, 2, 3



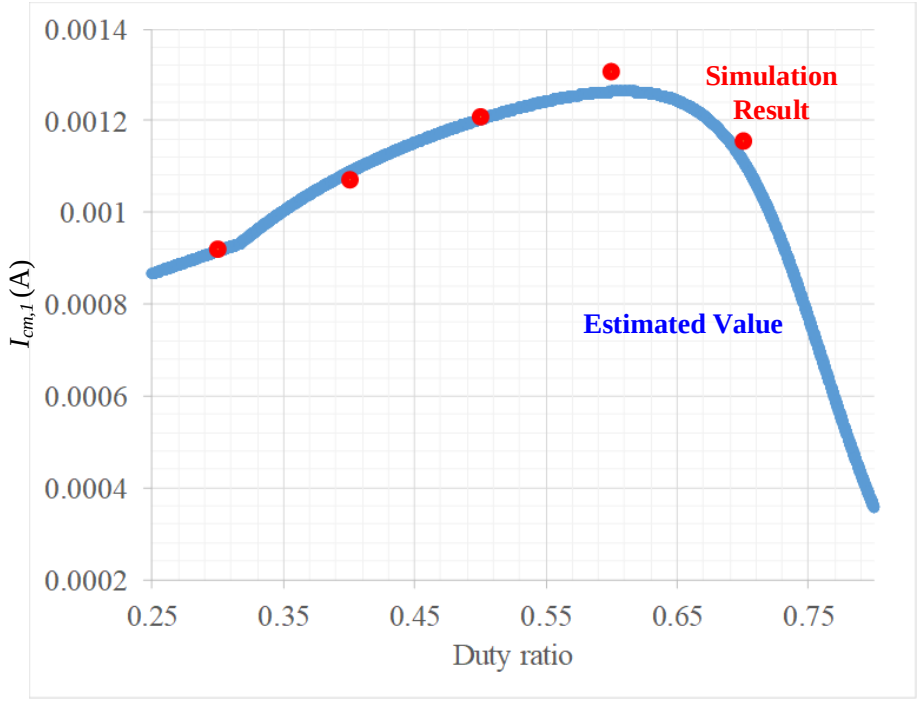
(a)



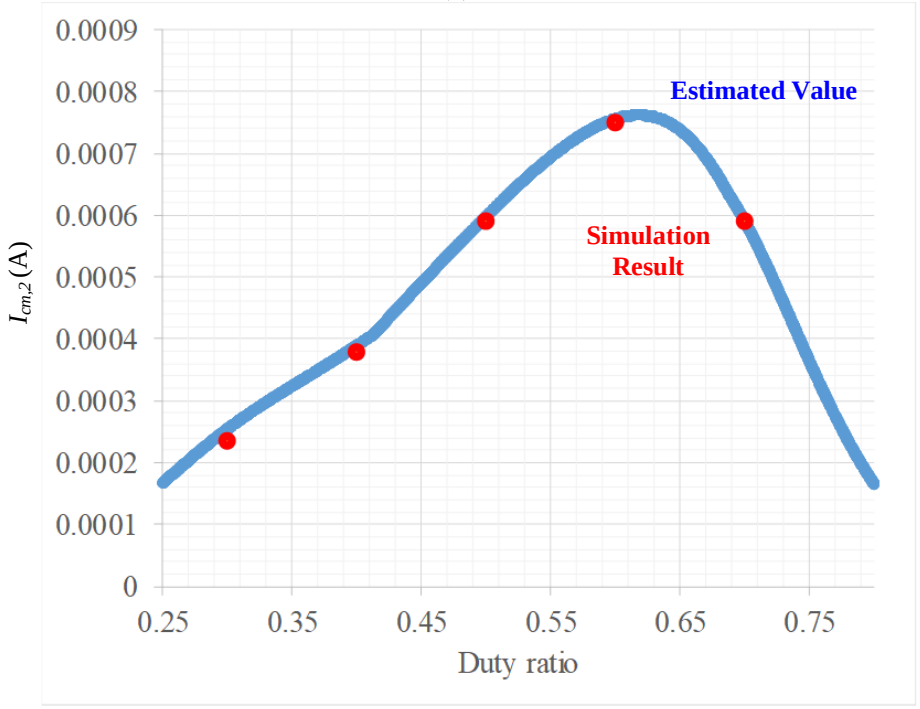
(b)

Fig. 4-14. Maximum common-mode open circuit voltage in a balanced class E converter with two-port network (a) fundamental (b) 2nd harmonic

and r. Calculating all possible solutions and comparing the value of equation (4-46), the maximum value of $|V_{cm,oc}|$ can be found. Fig. 4-14 shows the maximum common-mode open circuit voltage $|V_{cm,oc}|$ for different conversion gain values m. This common-mode open circuit voltage value can be used in equations (3-25) to calculate the maximum common-mode current of the converter caused by the parameter error. Fig. 4-15 shows the estimated and simulated common-mode current value when impedance between the load and ground Z_b is set to 3000 Ω. Comparing to the common-mode current of a conventional class E converter shown in Fig. 4-3, the maximum common-mode current of a balanced class E converter is ten times smaller than the conventional one in most regions. However, when the duty ratio is around 0.3, the fundamental common-mode current of a conventional class E converter is almost zero. It, therefore, is smaller than the maximum common-mode current of a balanced class E converter. This is due to canceling a common-mode voltage by a class E inverter and rectifier voltage. Although the fundamental term of common-mode current can be eliminated, 2^{nd} harmonic term is still larger



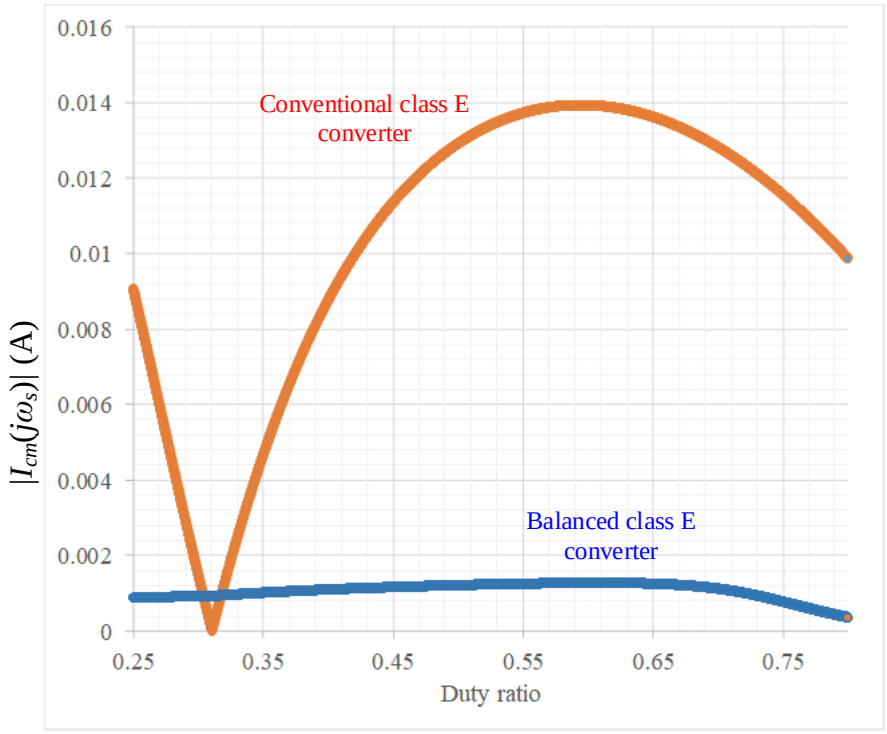
(a)



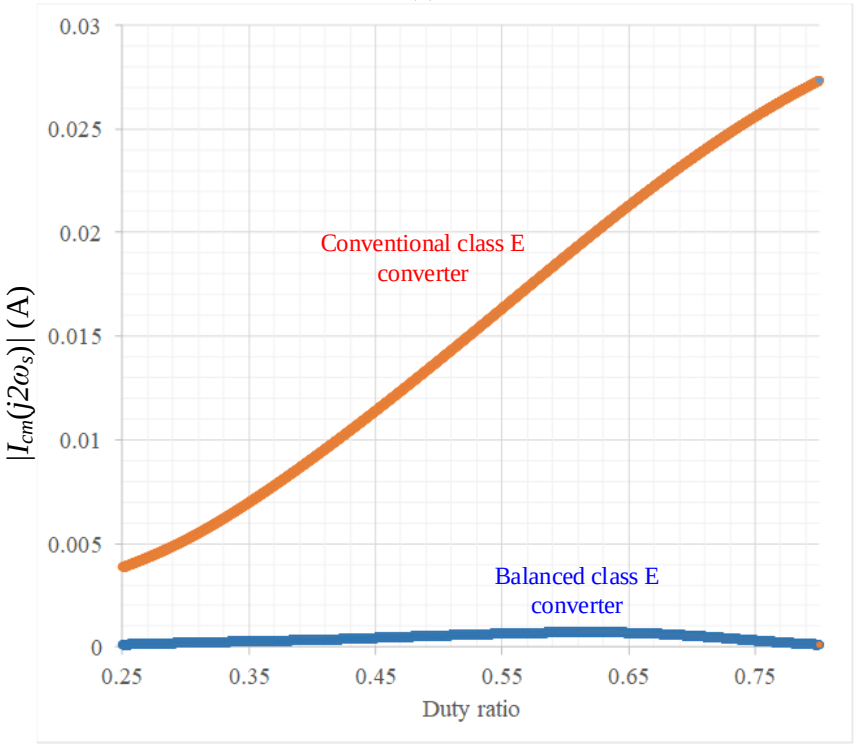
(b)

Fig. 4-15. Common-mode current in a balanced class E converter with two-port network (a) fundamental (b) 2nd harmonic

than the maximum common-mode current of a balanced class E converter. Also, parameter error is not considered in a conventional class E converter, altering the point where fundamental common-mode current can be eliminated. Therefore, in the common-mode current perspective, a balanced class E converter is more advantageous in removing a conduction EMI.



(a)



(b)

Fig. 4-16. Comparison of an estimated common-mode current in a conventional class E converter and a balanced class E converter (a) fundamental (b) 2nd harmonic

4.4 Experimental Results

The experiment is done using a balanced class E converter, similarly as in section 3. The same parameters are used with simulation. Conduction EMI of balanced class E converter with and without Y-rated capacitor is measured as shown in Fig. 4-17 and 4-18. Table 4-2 and 4-3 show the EMI conduction result when Z_b is high impedance, and the load is shorted to Earth. It can be seen that connecting C_Y capacitor between input and output helps reduce 2nd harmonic common-mode current

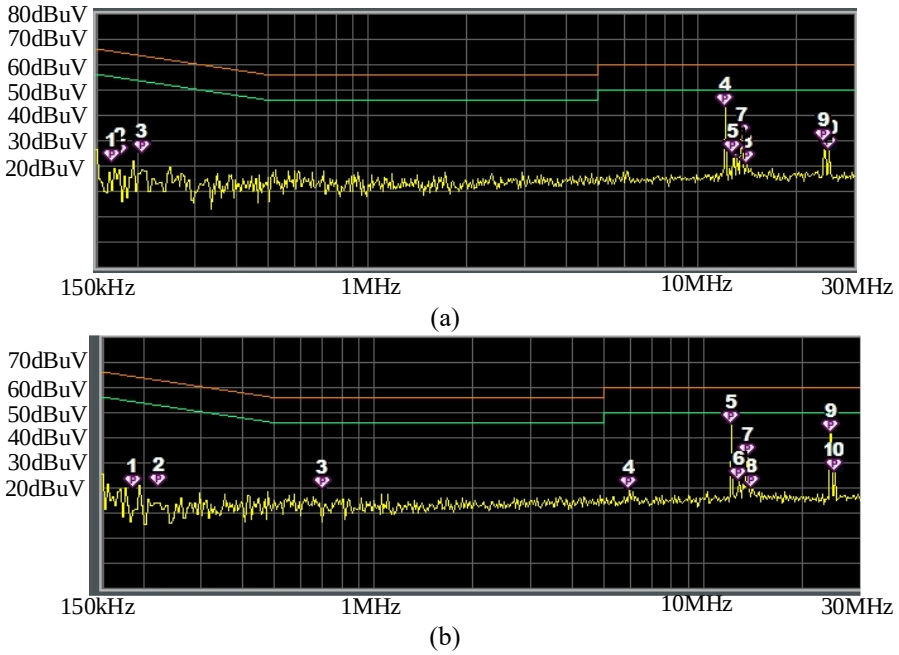


Fig. 4-17. Conduction EMI measurement of a balanced class E converter when Z_b = high impedance (a) with Y-capacitor (b) without Y-capacitor

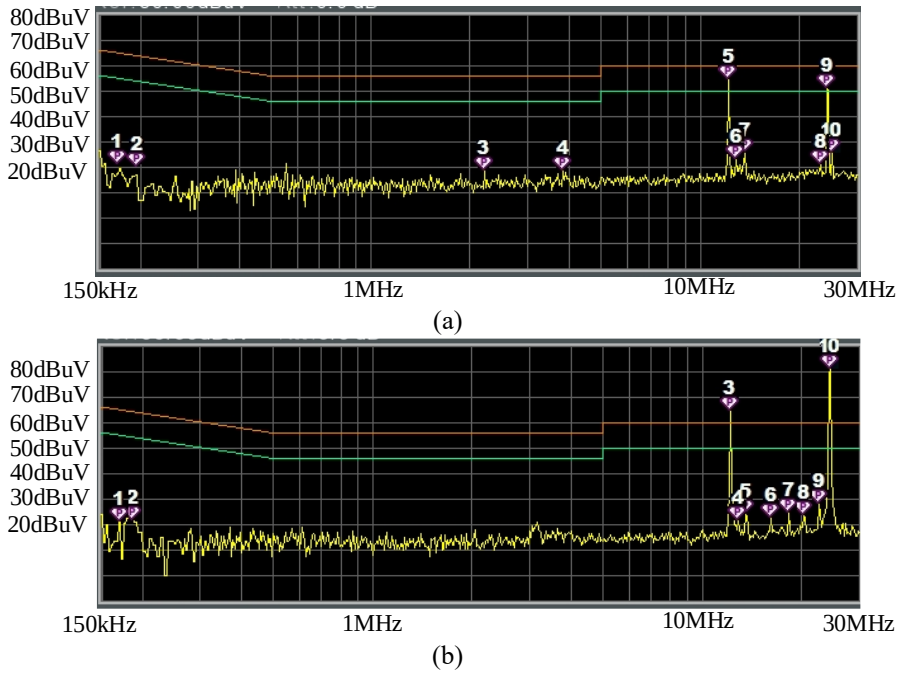


Fig. 4-18. Conduction EMI measurement of a balanced class E converter when Z_b = 0 (a) with Y-capacitor (b) without Y-capacitor

substantially.

The comparison between estimation and simulation value is shown in Table 4-4. The estimation and simulation value is when the parameter value is in its worst case. Therefore, estimation and simulation results are a lot larger than the experimental

TABLE 4-2. EXPERIMENTAL RESULT WHEN ZB = HIGH IMPEDANCE

	Balanced Class E Converter Without C_Y		Balanced Class E Converter with C_Y	
	Fundamental	2nd Harmonic	Fundamental	2nd Harmonic
V_{LISN} (dBuV)	50 dBμV	47.2 dBμV	48.6 dBμV	34.6 dBμV
V_{LISN} (V)	340 μV	228 μV	270 μV	54.2 μV
I_{cm} (A)	13.6 μA	9.12 μA	10.8 μA	2.17 μA

result.

TABLE 4-3. EXPERIMENTAL RESULT WHEN ZB = 0

	Balanced Class E Converter Without C_Y		Balanced Class E Converter with C_Y	
	Fundamental	2nd Harmonic	Fundamental	2nd Harmonic
V_{LISN} (dBuV)	68.1 dBμV	82.3 dBμV	60.3 dBμV	56.6 dBμV
V_{LISN} *(V)*	2.54 mV	13 mV	1.03 mV	676 μV
I_{cm} *(A)*	101 μA	520 μA	41.2 μA	27.04 μA

TABLE 4-4. COMPARISON BETWEEN ESTIMATION, SIMULATION AND EXPERIMENTAL RESULT WHEN ZB = 0

	Balanced Class E Converter without C_Y		Balanced Class E Converter with C_Y	
	Fundamental	2nd Harmonic	Fundamental	2nd Harmonic
Estimation	1.2 mA	592 μA	525 μA	106 μA
Simulation	1.2 mA	589 μA	523 μA	109 μA
Experiment	101 μA	520 μA	41.2 μA	27.04 μA

5. Self-powered Gate Driver Circuit Design

In order to operate a balanced class E converter proposed in this paper, the method to drive a high side switch needs to be considered. It is possible to place an isolated DC/DC converter to power the gate driver circuit. However, an isolated converter is often bulky, decreasing the overall power density. Also, adding an isolated DC/DC converter can add a common-mode noise path disturbing gate signal, especially in high switching frequency converter [62], [64].

In order to drive this system, a self-charge pump topology for a high-side power supply for a balanced class E converter shown in Fig. 5-1 is proposed. When the switch is turned off, the voltage across the switch rises, and this voltage will be used

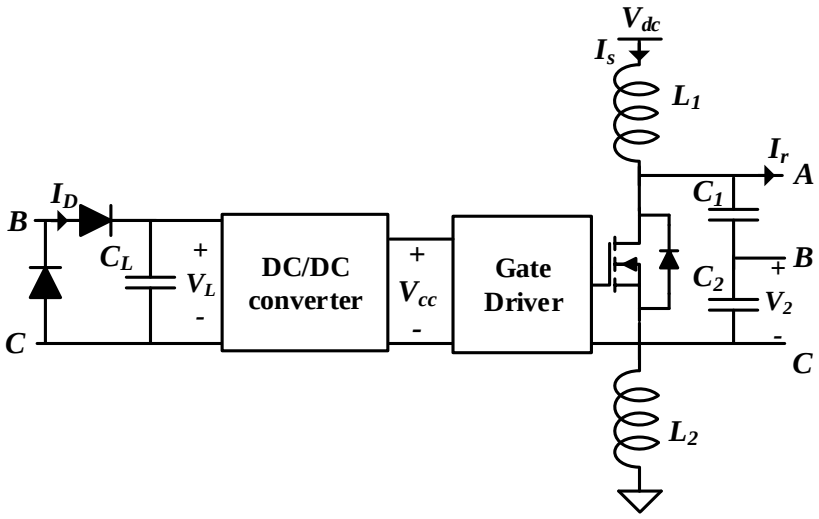


Fig. 5-1. Self-powered gate driver circuit topology

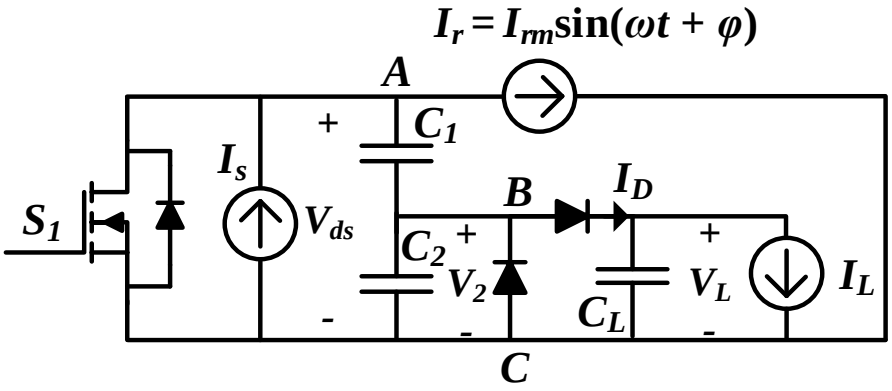


Fig. 5-2. Simplified model of self-powered gate driver circuit

to draw the power for the gate driving circuit. Fig. 5-2 shows the simplified model of the self-powered circuit. Here it is assumed that the self-powered circuit does not intervene with the regular operation of a class E converter. Therefore, I_r and I_s are considered a current source that satisfies equations (2-6) and (2-9). The power drawn from the gate driver circuit is also redrawn as a constant current source I_L since V_L is almost constant, assuming C_L is large. A capacitor is generally connected in parallel to the switch in a class E converter, and therefore the effects of drawing power for gate driving are minor. In this paper, the operation of the proposed circuit is analyzed, and conditions

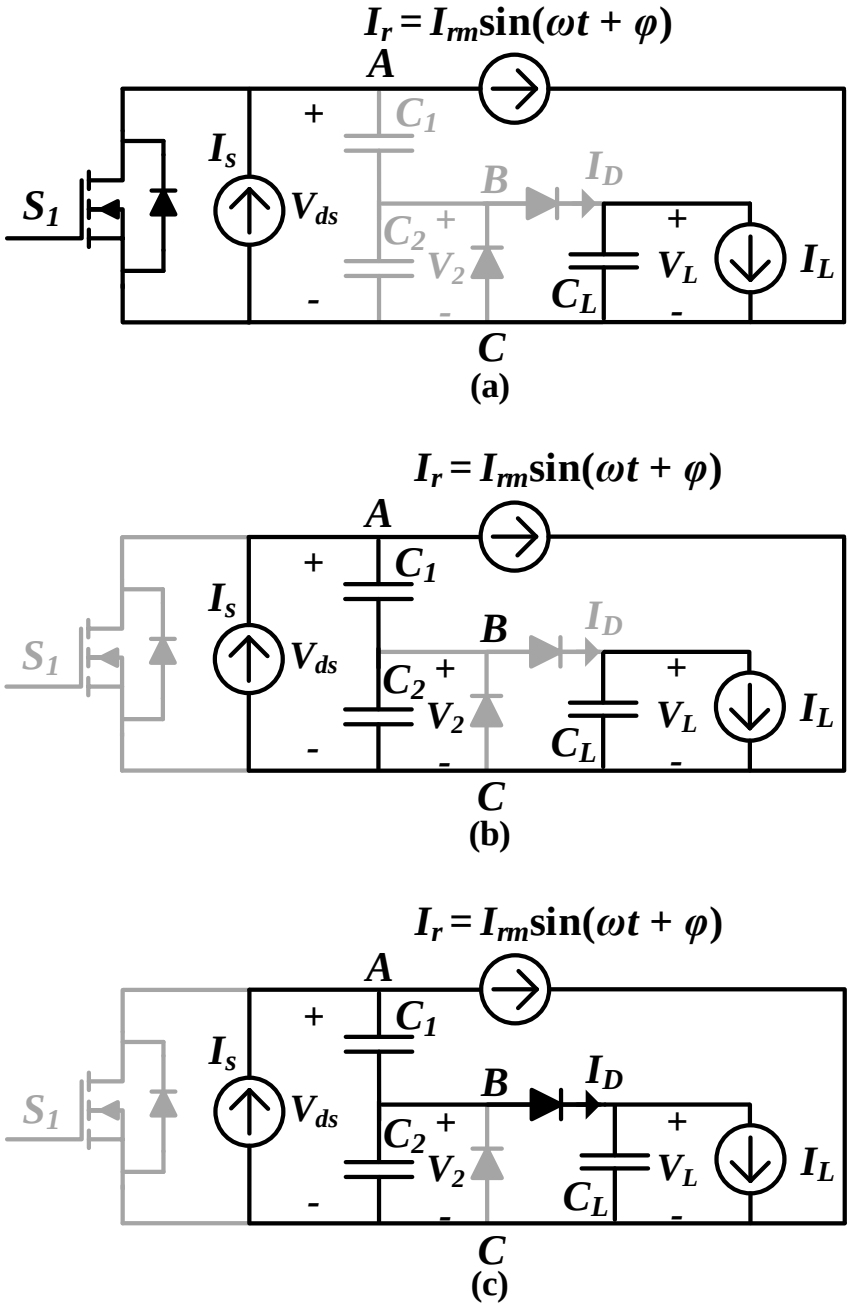


Fig. 5-3. Operation mode of self-powered gate driver circuit (a) Mode I when switch is turned on (b) Mode II switch is turned on but diode is turned off (c) Mode III diode is turned on.

for the self-powered pump circuit to operate properly will be found.

Fig. 5-3 shows the operation at each mode and Fig. 5-4

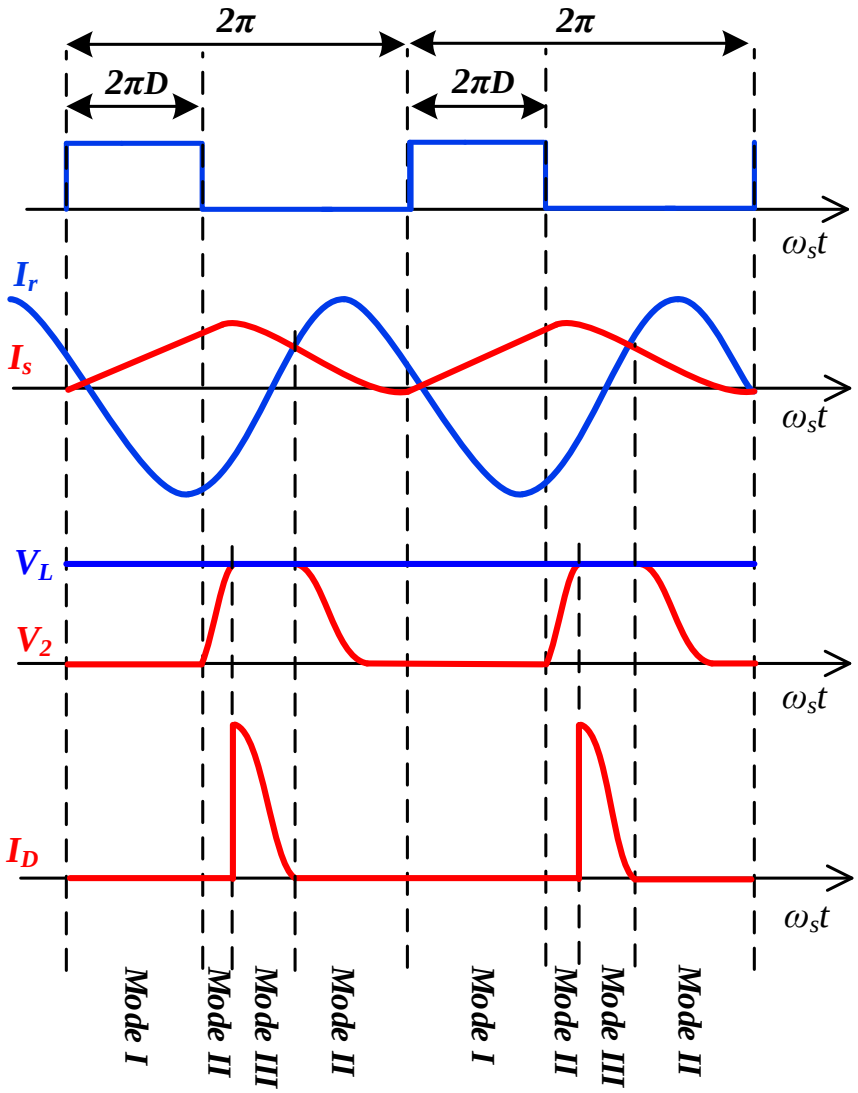


Fig. 5-4. Voltage and current waveforms of self-powered gate driver circuit

shows the voltage waveforms of the self-power circuit. At mode I, switch S_1 is turned on, and the voltage across the capacitor C_2 is zero. Therefore, diodes are turned off in this period, and no power is transferred to capacitor C_L. The switch is turned off in mode II, and capacitor C_2 charges until it reaches voltage V_L. At this moment, diodes are still off, and therefore current I_D is still

zero. Using the voltage equation of V_{S1} from equation (2-8), the voltage V_2 can be calculated as

$$V_2 = \frac{C_1 V_{s1}}{C_1 + C_2} = \frac{C_1}{C_1 + C_2}[V_{dc} - V_{dc}\cos(\omega_1 t) + Z_1 I_s(0)\sin(\omega_1 t)$$
$$- \frac{(\omega_1/\omega_s) Z_1 I_{rm}\sin(\varphi_r)}{1+(\omega_1/\omega_s)}\sin(\omega_1 t) + \frac{Z_1 I_{rm}(\omega_1/\omega_s)}{1-(\omega_1/\omega_s)^2}\{\cos(\omega_s t + \varphi_r) - \cos(\omega_1 t + \varphi_r)\}] \quad (5-1)$$

At mode III, diode D_1 starts conducting, and therefore voltage V_2 is fixed to V_L. In this mode, current I_D flows and charges capacitor C_L. The current $I_{D,}$ according to equations (2-9), becomes

$$I_D = I_s - I_r$$
$$= \frac{V_{dc}}{Z_1}\sin(\omega_1 t) - \frac{(\omega_1/\omega_s) I_{rm}\sin(\varphi_r)}{1+(\omega_1/\omega_s)}\cos(\omega_1 t) + I_s(0)\cos(\omega_1 t) \quad (5-2)$$
$$+ \frac{I_{rm}}{1-(\omega_1/\omega_s)^2}\{(\omega_1/\omega_s)\sin(\omega_1 t + \varphi_r) - \sin(\omega_s t + \varphi_r)\}$$

The circuit operates in mode III until the current I_D reaches zero and diode D_1 is turned off.

In order to design a self-powering circuit, the average current of I_D needs to be calculated. At a steady-state, the average current of I_D should be equals to I_L. Therefore, voltage V_L according to different output power can be calculated to design the circuit. The average current of I_D can be calculated as

$$I_{D,avg} = \frac{1}{T_s}\int_{t_1}^{t_2}\left(I_s - I_r\right)dt\,, \qquad (5-3)$$

where t_1 is when mode III starts, and t_2 is when mode III stops. Assuming C_2 is sufficiently larger than C_1 such that $V_{S1} >> V_2$, then the above equation can be rewritten,

$$I_{D,avg} = \frac{1}{T_s}\int_{t_1}^{t_2}\left(I_s - I_r\right)dt = \frac{C_1}{T_s}(V_{s1}(t_2) - V_{s1}(t_1)) \qquad (5-4)$$

At time t_1, voltage V_2 is equal to V_L, and therefore $V_{S1}(t_1)$ can be calculated

$$V_{S1}(t_1) = \frac{C_1 + C_2}{C_1}V_L\,. \qquad (5-5)$$

At time t_2, I_r is equal to I_s. At this point, $\mathrm{d}V_{S1}/dt = 0$, meaning that $V_{S1}(t_2)$ is a maximum switch voltage. The maximum switch voltage $V_{S1,max}$ is calculated numerically and plotted in Fig.5-5, where duty versus maximum switch voltage is divided by input voltage $V_{S1,max}/V_{dc}$. It can be seen that changes in $\omega_{1,n}$ has a negligible effect on maximum switch voltage. The average I_D then becomes

$$I_{D,avg} = \frac{1}{T_s}(C_1 V_{S1,\max} - (C_1 + C_2)V_L)\,. \qquad (5-6)$$

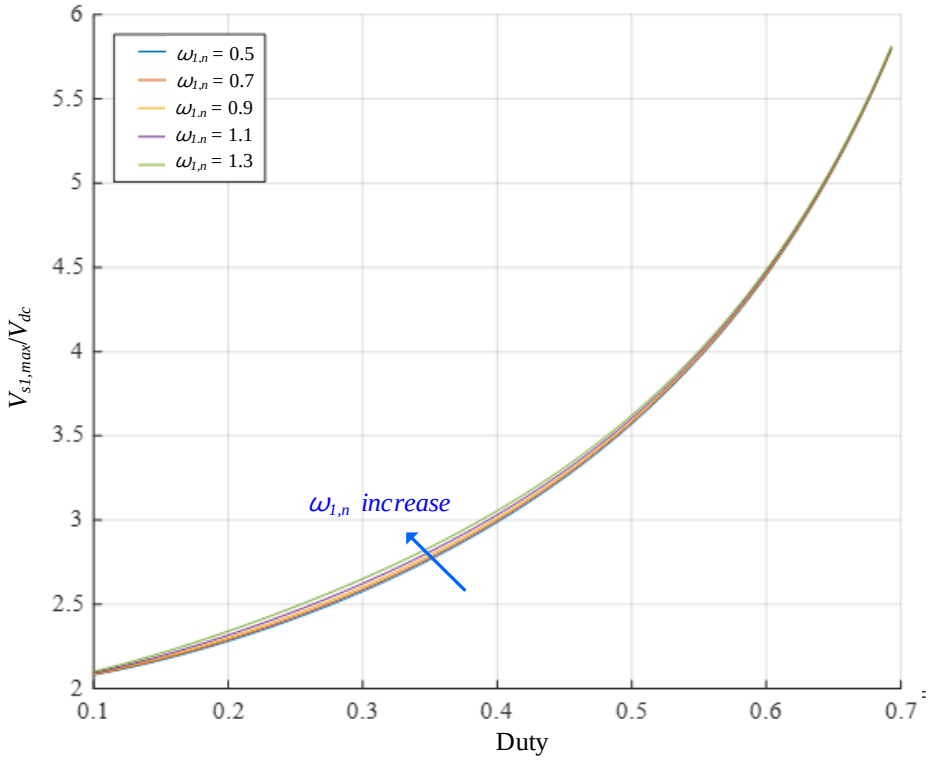


Fig. 5-5. Maximum switch voltage versus duty ratio

Now let $I_{D,avg} = I_{L,}$ then the following equation can be derived.

$$V_L I_L = \frac{1}{T_s}(C_1 V_{s1,\max} - (C_1 + C_2)V_L)V_L = P_o \qquad (5-7)$$

where P_o is the output power of this self-powering circuit. Solving the above quadratic equation V_L can be found as

$$V_L = \frac{C_1 V_{s1,\max}}{2(C_1 + C_2)}\left(1 + \sqrt{1 - \frac{8\pi(C_1 + C_2)P_o}{\omega_s (C_1 V_{s1,\max})^2}}\right) \qquad (5-8)$$

Fig. 5-6 shows the plot of duty ratio versus V_L divided by input voltage for different values of $\omega_{1,n}$ when C_1 = 100 pF, C_2 = 1.2 nF, f_s = 13 MHz, V_{dc} = 150 V and P_o = 1 W. Fig. 5-7 shows the same plot with the same condition except for fixed $\omega_{1,n}$ = 1.3 and

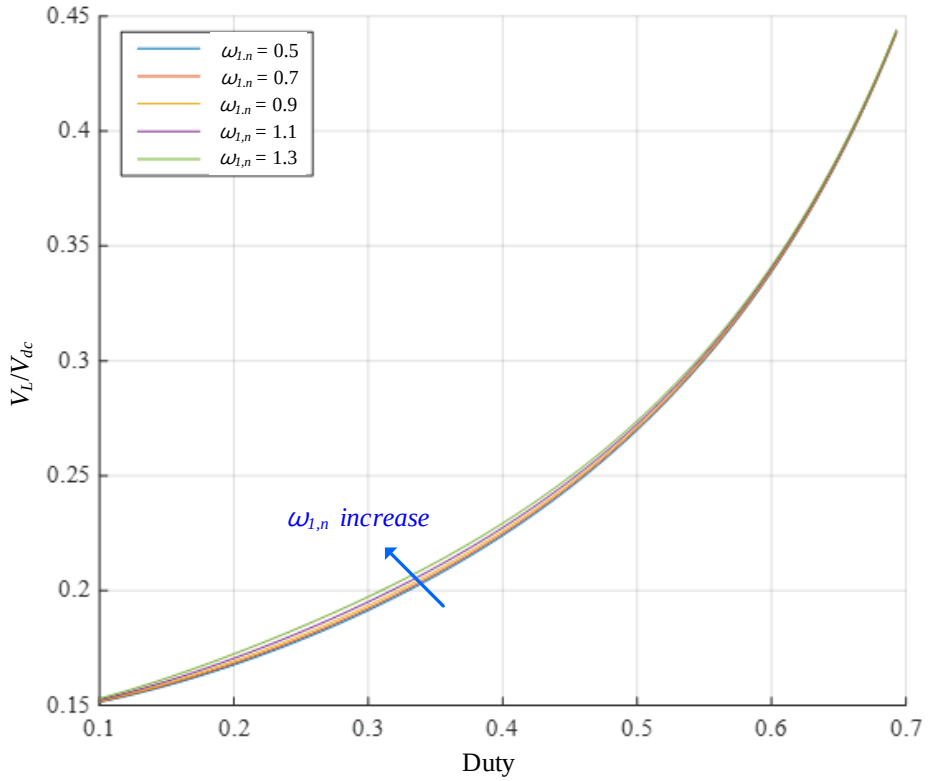


Fig. 5-6. DC/DC converter input voltage versus duty ratio when P_o = 1W

different output power P_o at 0.2 W, which is a maximum power to operate gate driver IC and 1 W, which is a maximum power to operate gate driver IC and DSP (Digital Signal Processor). It can be seen that as output power increases, the voltage V_L decreases.

The proposed circuit cannot provide enough power when the output power is too high or $V_{S1,max}$ is too low. This condition is when quadratic equation (5-7) has no real solution. The condition for the self-powering circuit to function properly can be written as an inequality function below

$$1-\frac{8\pi(C_1+C_2)P_o}{\omega_s(C_1V_{s1,\max})^2}>0. \qquad (5-9)$$

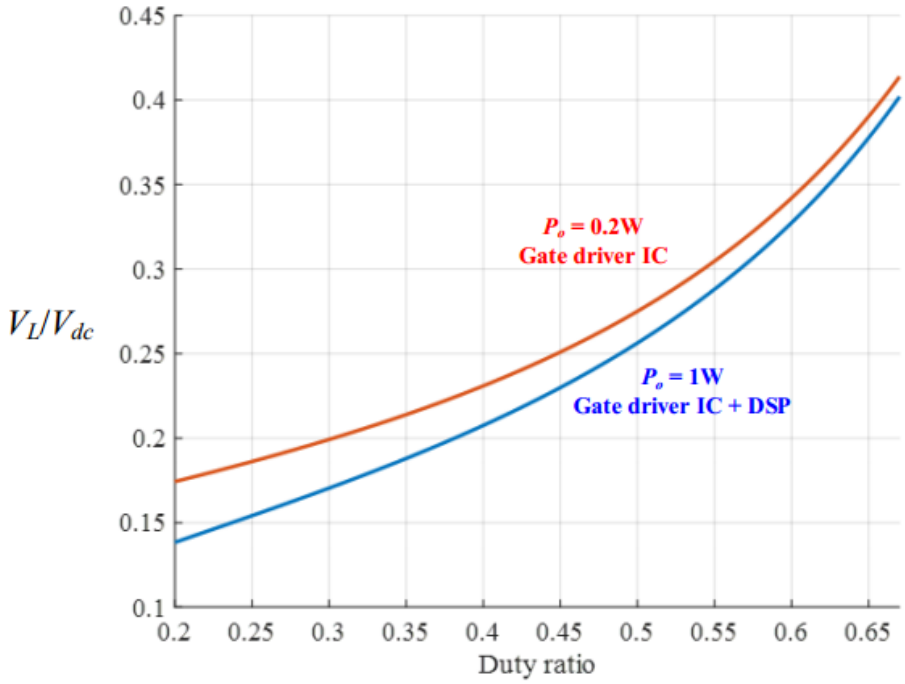


Fig. 5-7. DC/DC converter input voltage versus duty ratio when $\omega_{1,n}$ = 1.3

Rearranging the above inequality function makes it possible to calculate the minimum input voltage required to operate the proposed self-powering circuit.

$$V_{dc} > \frac{1}{C_1(V_{s1,\max}/V_{dc})}\sqrt{\frac{8\pi(C_1+C_2)P_o}{\omega_s}}. \qquad (5-10)$$

Fig.5-8 shows the duty ratio versus minimum input voltage $V_{dc,min}$ plot for different output power with the same conditions as Fig. 5-6. It can be seen that higher input voltage is required for higher output power.

The capacitors C_1 and C_2 are chosen by setting a maximum and minimum value of V_L. If V_L is too large, DC/DC converter or linear regulator with a high step-down gain is required. If V_L is too low, the current I_D should be large, thus reducing the efficiency of the circuit. Therefore, C_1 and C_2 should be chosen carefully. The proportion of two capacitors C_2/C_1 can be used to set the value of V_L versus the DC-link voltage of the class E converter. Rewriting equation (5-8),

$$V_L = \frac{V_{s1,\max}}{2(1+C_2/C_1)}\left(1+\sqrt{1-\frac{8\pi(1+C_2/C_1)P_o}{\omega_s C_1 (V_{s1,\max})^2}}\right) \qquad (5-11)$$

First, C_1 is chosen that normal operation of a class E converter

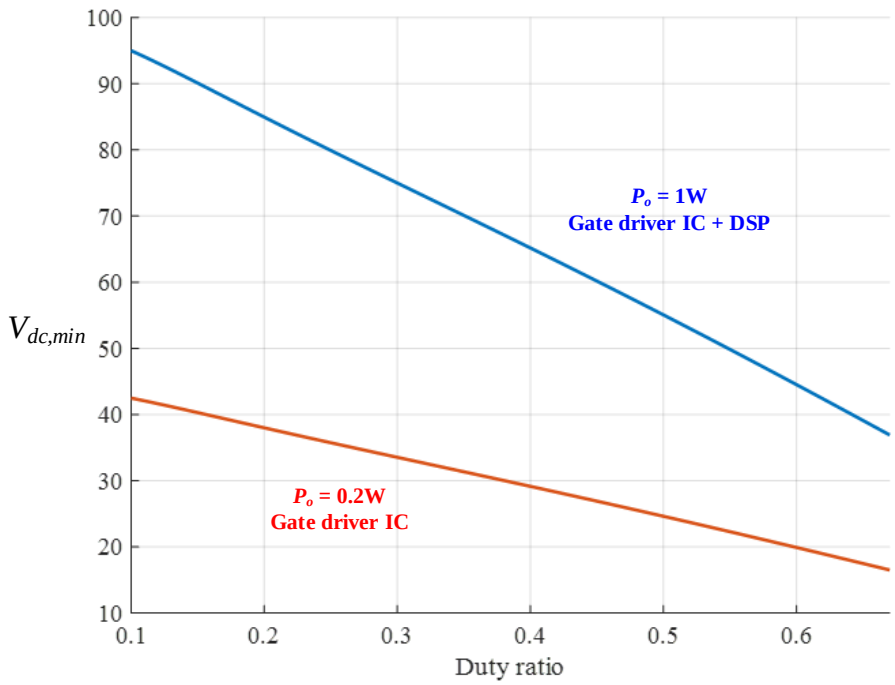


Fig. 5-8. Minimum DC-link input voltage required to operate self-powered gate driver cituit when ω_{1n} = 1.3

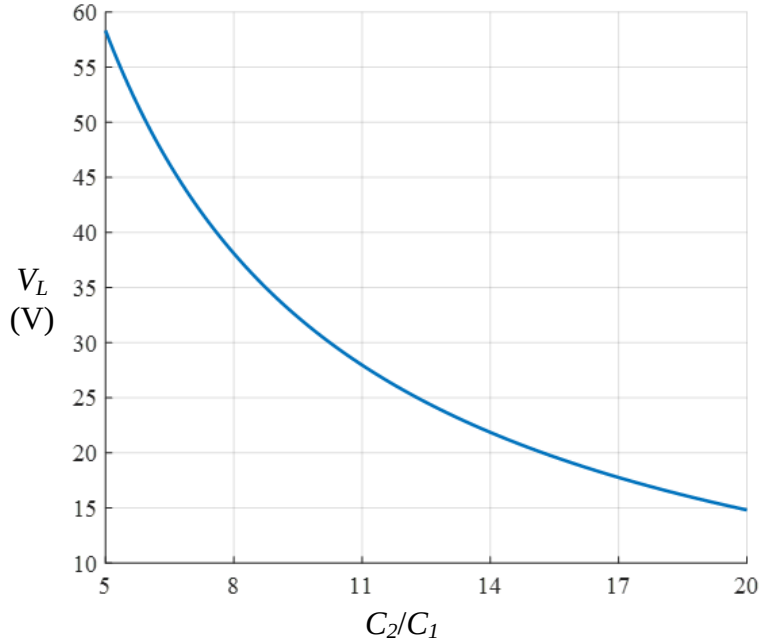


Fig. 5-9. DC/DC converter input voltage V_L versus C_2/C_1

is possible while achieving ZVS. Then, using equation (2-16), $K = Z_1 I_{rm}/V_{dc}$ can be calculated where Z_1 = $\sqrt{L_1/C_1}$. Using this value with $\omega_{1,n} = \omega_s(\sqrt{L_1 C_1})^{-1}$, C_1 can be calculated. Then C_2 is chosen, which is large compare to C_1 such that the impedance of C_2 is more than five times smaller than the impedance of C_1. This is to make sure that the self-powered gate drive circuit has a minimal effect on the operation of the class E converter. The value of V_L is then calculated for different values of C_2/C_1. Fig. 5-9 shows the plot of V_L versus C_2/C_1 where C_1 = 100 pF, $\omega_{1,n}$ = 1.3, V_{dc} = 100 V, P_o = 1 W and duty ratio equals 0.5. If C_2/C_1 = 6 and gate driver IC input voltage is 5 V, DC/DC converter with a step-

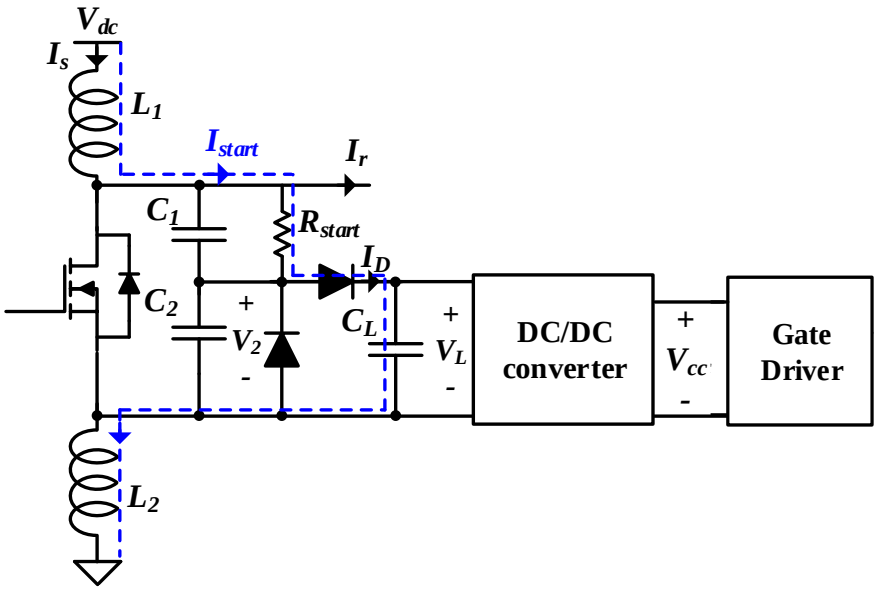
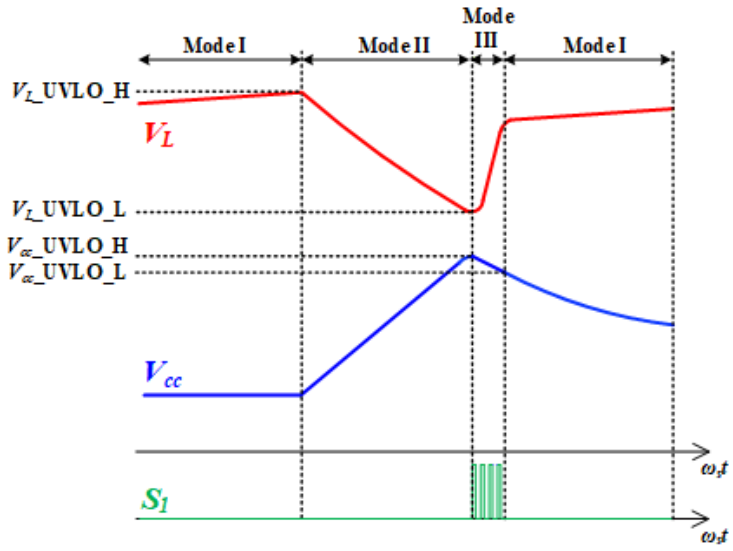


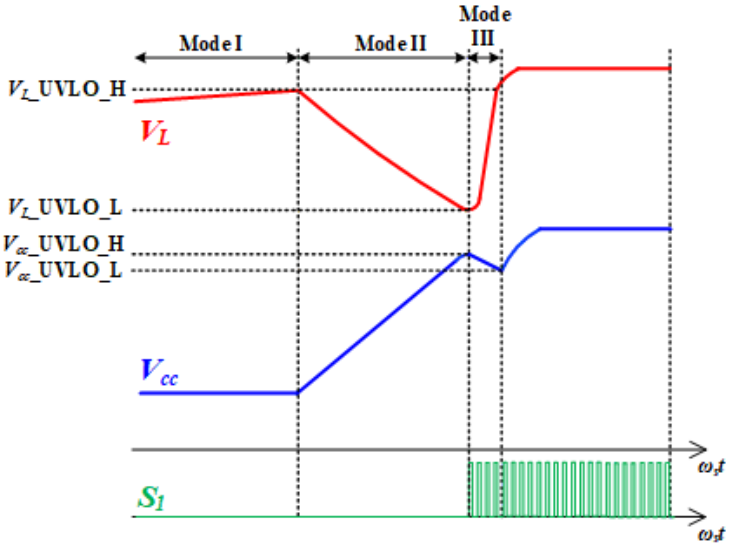
Fig. 5-10. Start-up resistor placed in the proposed self-powered gate driving circuit.

down gain of 10 is needed to provide IC power. In this paper, C_2/C_1 is set to 20 (C_1 = 100 pF and C_2 = 2 nF) due to the lack of a small-sized buck converter IC capable of high step-down gain and high input voltage.

The start-up circuit is required to begin the operation of self-powered gate driving at the beginning. In the proposed self-powered gate driver circuit, a resistor is placed, as shown in Fig. 5-10, to draw power from the input voltage to charge the capacitor C_L. The voltage waveforms during start-up are demonstrated in Fig. 5-11. Fig. 5-11(a) shows when the proposed circuit fails to start up, and Fig. 5-11 (b) shows when the proposed circuit succeeds to start operating. In mode I, the



(a)



(b)

Fig. 5-11. The voltage waveforms during start-up operation of the self-powered gate drivier (a) start-up fails (b) start-up successful

voltage V_L starts rising due to start-up current flowing through resistor R_{start}. After V_L reaches the rising threshold of the DC/DC converter, the DC/DC converter starts operating and charges voltage V_{cc} in mode II. If V_{cc} reaches a rising threshold of the gate

driver IC, gate driver starts switching in Mode III. During this mode, through a proposed self-powered gate driver circuit, the voltage V_L starts increasing. If the voltage V_L reaches the DC/DC converter threshold's rising threshold during mode III, the self-powered gate driving circuit can operate steadily. However, if the voltage V_{cc} is reduced below the negative threshold of the gate driver IC and therefore stops switching before voltage V_L reaches the rising threshold, a self-powered gate driving circuit fails to start.

Fig. 5-12 shows voltage waveforms of V_L and V_2 when the gate driver circuit is operating in a steady state. Here V_L reaches 16 V when measured gate driver power is 0.2 W. Fig. 5-13 shows the voltage waveforms during start-up time. The voltage V_L and V_{cc} are demonstrated at each mode. The exact time the start-up is successful is hard to capture since the self-powered

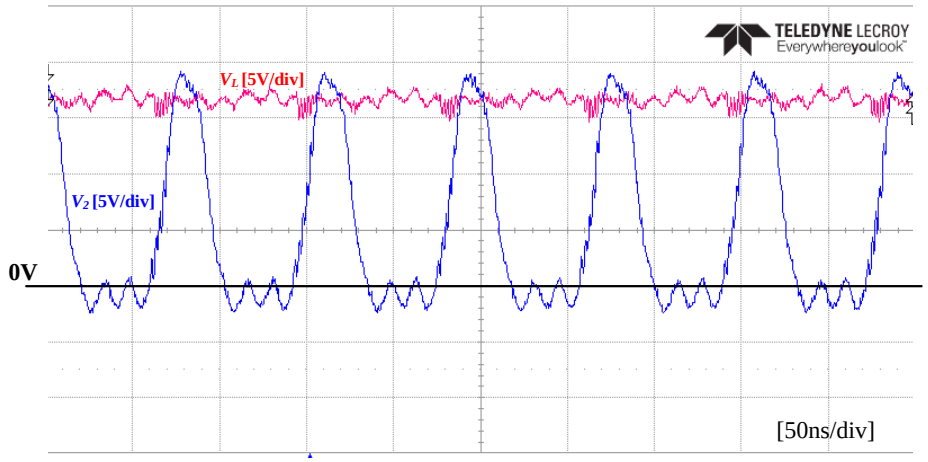


Fig. 5-12. Voltage waveforms of self-powered gate driver circuit during steady state operation

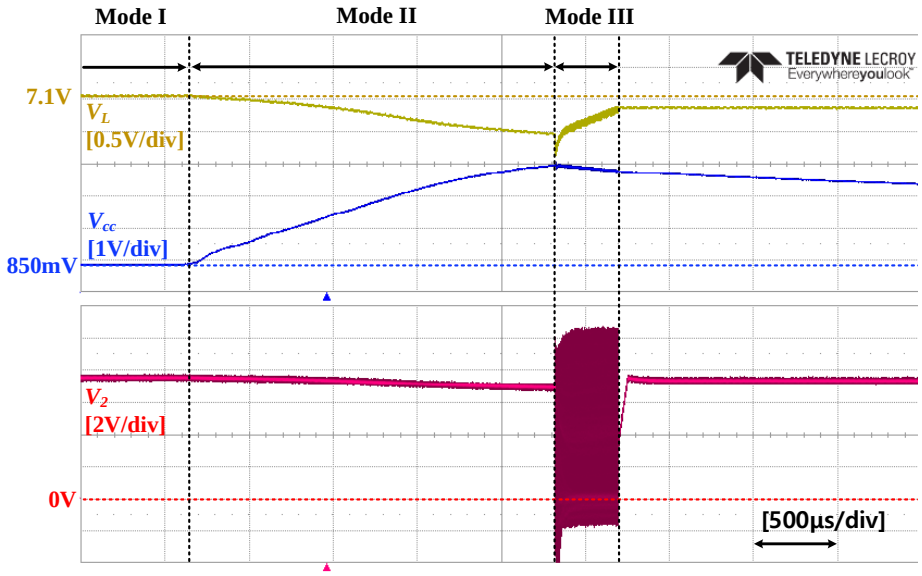


Fig. 5-13. Voltage waveforms of self-powered gate driver circuit during start-up operation.

gate driver starts operating after few start-up failures. Therefore, Fig. 5-13 only shows the voltage waveforms when the self-powered gate driver fails to start up initially. It can be seen that the voltage V_L fails to reach the rising threshold of 7.1 V during Mode III.

6. Conclusion and Future Research

6.1 Conclusion

This dissertation proposes a capacitive isolated converter design mitigating common-mode current to consider touch current and electromagnetic interference. The transformer takes a lot of space in the converter, becoming a bottleneck for designing a high power density isolated converter. A capacitor can be utilized instead of a transformer to create a high power density isolated converter since it has a high energy density in a high switching frequency converter. A capacitive isolated converter, however, has a common-mode current path through capacitors. This common-mode current can cause safety and compatibility issues by increasing touch current and conducted electromagnetic interference. Therefore, this dissertation analyzed the common-mode current in a capacitive isolated converter and proposes a method to reduce a common-mode current.

The common-mode current in a capacitive isolated converter is analyzed by dividing them into grid frequency bands and switching frequency bands. The common-mode current in grid frequency bands is caused by grid voltage and is responsible

for touch current. In contrast, common-mode current in switching frequency bands is caused by a high-frequency inverter and is accountable for conducted electromagnetic interference. This dissertation proposes setting a maximum capacitor value and designing a balanced class E converter to reduce a common-mode current. The proposed method is tested with simulation and experiment, and these results show the reduction in common-mode current.

The dissertation is summarized as follows.

1) In grid frequency bands, the impedance of the capacitor is high. Therefore, reducing the capacitance of the capacitive isolated converter can limit the common-mode current in grid frequency bands. In this dissertation, maximum allowed capacitance is calculated to satisfy the touch current regulation of electronic devices. To reduce the capacitance, a class E converter topology, which is suitable for high switching frequency, is chosen. The touch current is measured in the experiment, and it was observed that the measured touch current is below the regulation limit.
2) The common-mode current in switching frequency bands is reduced using a balanced class E converter topology.

The proposed balanced class E converter reduces the common-mode current in switching frequency bands by canceling the voltage seen from the common-mode side. A balanced structure can, ideally, eliminate the common-mode current in switching frequency bands. However, the converter cannot be balanced completely in the real world due to a parameter error. Therefore, this dissertation analyzes the effect of common-mode current on parameter error of a proposed balanced class E converter. The analysis shows that the proposed class E converter has a lower common-mode current than the conventional capacitive isolated converter. The simulation and experimental results also show the same conclusion.

3) The role of the transformer is not only to isolate the primary and secondary sides but also to adjust voltage gain between input and output using turn ratio. In a proposed capacitive isolated converter, a two-port network is used to set the voltage gain. The optimal network design to minimize the network size is also written in this dissertation.

4) In a balanced class E converter, the switch is placed on a high side. Therefore, a circuit to provide power to a gate

driver circuit is needed to operate the proposed balanced class E converter. A self-powered gate driving circuit that draws power from a voltage across the switch is presented in this dissertation. The operation condition of this circuit is analyzed. The circuit is used to provide power to a gate driver in the prototype used in the experiment.

6.2 Future Research

There are many more challenges to overcome as future research. First, the lack of a high-frequency common mode choke filter is a problem when designing a high-power capacitive isolated converter. Due to parasitic capacitance, common mode choke has typically low impedance at high frequency, especially for the high power converter. Therefore, an alternative design for high-frequency EMI filter design should be studied to reduce conduction EMI in a high-power capacitive isolated converter. Also, due to the voltage limit of the GaN switch (650V maximum for commercially available GaN transistor), the current topology cannot operate in universal input voltage. Therefore, alternative topology for capacitive isolation converter needs to be further studied to work in broader input voltage.

Appendix

A.1 Safety Requirements for Medical Electrical Equipment

The safety standard for medical electrical equipment is a lot stricter than other IT equipment for patient safety. The leakage current of medical electrical equipment is restricted by the standard IEC 60601 [8]. The standard also includes the circuit implemented to measure the leakage current shown in Fig. A−1. This circuit is used to measure the leakage current by connecting one end of the test terminal to the medical equipment and the other end to the ground. The voltage V_t is measured, and the leakage current I_{lk} is calculated as

$$I_{lk} = V_t / R_2 \qquad \text{(A−1)}$$

where R_2 is 1000 Ω.

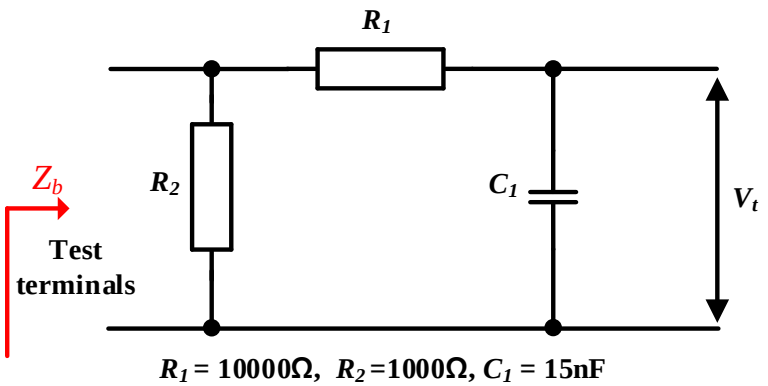


Fig. A−1. Leakage current measuring circuit in IEC 60601.

The maximum leakage current depends on the type of applied part, part of the equipment that comes into contact with a patient, used in medical equipment. There are three types of applied parts defined in the standard: Type B (Body), Type BF (Body Floating), and Type CF (Cardiac Floating). Type B is the least stringent one where the contact of the equipment is not conductive. The example of such equipment is MRI scanner and medical laser. Type BF is designed to be safer than Type B since the contact is conductive but not enough to be used directly to the heart. Type CF is the most stringent one and is thus used in applications such as dialysis machines where direct contact with the heart is required. The leakage current standard for each type of applied part is shown in Table A-1.

TABLE A-1. IEC 60601 LEAKAGE CURRENT STANDARD FOR MEDICAL EQUIPMENT

		Type B		**Type BF**		**Type CF**	
		NC	SFC	NC	SFC	NC	SFC
Patient Auxiliary Current	DC	10μA	50μA	10μA	50μA	10μA	50μA
	AC	100μA	500 μA	100μA	500μA	10μA	50μA
Patient Leakage Current	DC	10μA	50μA	10μA	50μA	10μA	50μA
	AC	100μA	500μA	100μA	500μA	10μA	50μA
Total Leakage Current	DC	50μA	100μA	50μA	100μA	50μA	100μA
	AC	500μA	1mA	500μA	1mA	50μA	100μA

Here NC stands for normal condition, and SFC stands for a single fault condition. Also, from the table above, there are three different types of leakage current: a patient auxiliary current, patient leakage current, and total leakage c-urrent. A patient auxiliary current and patient leakage current direction are shown in Fig. A-2. The patient leakage current flows from applied parts to earth through the patient, as shown in Fig. A-2(a). The patient auxiliary current flows between different applied parts via the patient, as shown in Fig. A-2(b). The total leakage current is measured when there are multiple applied parts in the medical

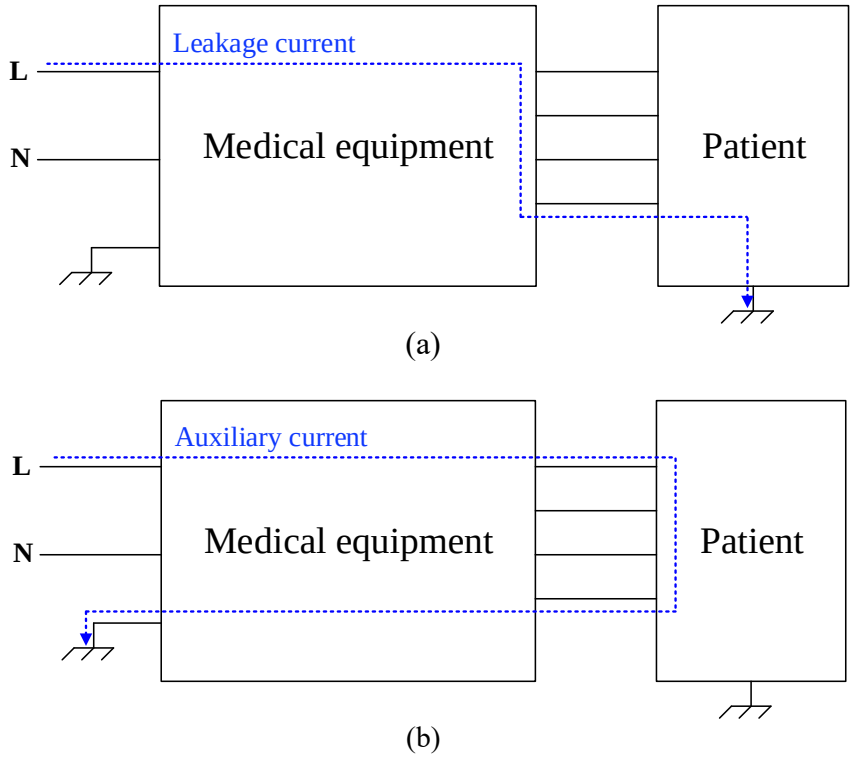


Fig. A-2. Typical current direction of (a) leakage current (b) auxiliary current between medical equipment and patient.

equipment. The summation of leakage current measured for each applied part should not exceed the total leakage current value in Table A-1. The leakage current of medical equipment with Type B and Type BF is limited to 10 μA DC and 100 μA AC, lower than 250 μA leakage current restriction in IEC 60950. In the medical equipment with Type CF applied part, the leakage current is restricted to 10 μA both in DC and AC. Therefore, the capacitor should be chosen more carefully when designing a capacitive isolated converter for medical equipment.

A.2 Rating of a Safety Capacitor

In this paper, Y-capacitor is used to achieve galvanic isolation instead of a transformer. This is due to a withstand voltage and impulse voltage standard for isolated converter written in IEC 60950-1 [6] and IEC 61800-1 [65]. All electric equipment must undergo voltage stress tests to make sure safe and stable operation. The withstand voltage test induces 50/60 Hz or DC voltage between the primary and secondary sides of an isolated converter. The induced voltage is slowly escalated, below 150 V/s, until it reaches test voltage. If an isolated converter can withstand the test voltage for 60 seconds, it passes the withstand voltage test. The test voltage of the converter is different depending on the type of isolation and peak operating voltage. Table A-2 shows the withstand test voltage across the primary and secondary sides for each isolation type. Here U refers to the peak operating voltage of the electronic

TABLE A-2. WITHSTAND VOLTAGE TEST ACCORDING TO IEC 60950-1

	Test Voltage				
	$U \leq 184\ V_{pk}$	$184\ V_{pk} < U \leq 354 V_{pk}$	$364\ V_{pk} < U \leq 1.41\ kV_{pk}$	$1.41\ kV_{pk} < U \leq 10\ kV_{pk}$	$10\ kV_{pk} < U \leq 50\ kV_{pk}$
Functional Isolation	$1000\ V_{rms}$	$1500\ V_{rms}$	V_a	V_a	$1.06U$
Basic Isolation	$1000\ V_{rms}$	$1500\ V_{rms}$	V_a	V_a	$1.06U$
Reinforced Isolation	$2000\ V_{rms}$	$3000\ V_{rms}$	$3000\ V_{rms}$	V_b	$1.06U$

device. There are four different types of isolation: functional isolation, basic isolation, double isolation, and reinforced isolation. Functional isolation does not provide any protection against electric shock and therefore is least stringent. Basic isolation offers some protection against electric shock but is not as safe and is typically used when most accessible parts are connected to the earth. Double isolation has, in addition to basic isolation, a supplementary insulation layer to provide additional protection. Lastly, reinforced isolation offers the same protection level as double isolation with only a single layer. From the table, electronic devices with reinforced isolation should withstand 2000 V_{rms} voltage if operating voltage is below 184 V_{pk} and 3000 V_{rms} if operating voltage is between 184 V_{pk} and 354 V_{pk}.

The rating of the safety capacitor is used to find the capacitor that can pass the withstand voltage test. According to the

TABLE A-3. CAPACITOR RATING ACCORDING TO IEC 60384

Capacitor Rating	Rated Voltage	Impulse Test Voltage	Withstand Test Voltage
Y1	Max. 500 V_{rms}	8 kV	4 kV_{rms}
Y2	Min. 150 V_{rms} Max. 300 V_{rms}	5 kV	1.5 kV_{rms}
Y4	Max. 150 V_{rms}	2.5 kV	900 V_{rms}
X1	Max. 760 V_{rms}	4 kV	4.3 times rated voltage
X2	Max. 760 V_{rms}	2.5 kV	4.3 times rated voltage

standard IEC 60384 [61], safety capacitors are rated according to their rated voltage, impulse test voltage, and withstand voltage. Table A-3 shows the requirement for each rating of safety capacitors. Here rated voltage is defined as a voltage level that can be applied continuously without exceeding the operating temperature range. From the table, only Y1 rated capacitor can pass the withstand voltage for the reinforced isolation with operation voltage smaller than 1.41 kV_{pk}. The withstand voltage test of a proposed capacitive isolated converter is shown in Fig. A-3. Since inductors have small impedance at low frequency, DC or 50/60 Hz, most of the withstand voltage is applied to capacitors C_{r1} and C_{r2}. Therefore, in the proposed capacitive isolated converter, Y1 rated safety capacitor is used to pass the withstand voltage test.

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초 록

본 논문은 정전식 절연형 클래스 E 컨버터에서 발생하는 공통모드 전류를 분석하고 줄이는 방식을 제안한다. 고전력 밀도의 DC/DC 컨버터 설계를 위해 절연형 컨버터의 변압기를 제거하는 연구가 많이 진행되어 왔다. 변압기를 제거하는 한 방법은 변압기 대신에 커패시터를 이용해 갈바닉 절연을 달성하는 방법이다. 그러나 커패시터를 사용하게 되면 커패시터를 통해 공통모드 전류가 흐르게 되고 이는 접촉 전류와 전도 전자 방해 노이즈를 발생시킨다. 모든 전자기기는 사용자의 안전과 다른 전자기기와의 전자 적합성을 위해 공통모드 전류로 인해 발생하는 접촉 전류와 전도 전자 방해 노이즈를 제한하고 있다. 그러므로 본 논문에서는 정전식 절연형 클래스 E 컨버터에서 발생하는 공통모드 전류를 분석하고 이를 줄이는 방법을 연구한다.

먼저 계통 주파수 대역의 공통모드 전류를 먼저 분석하였다. 이 저주파수 대역의 공통모드 전류는 사용자의 안전을 위협하는 접촉 전류와 관련이 있다. 저주파수 대역에서는 커패시터가 높은 임피던스를 가지기 때문에 최대 커패시터 값을 설정해서 접촉 전류를 규정에 만족하도록 설정할 수 있다. DC/DC 컨버터의 토폴로지로는 클래스 E 컨버터를 선정하였다. 이 토폴로지는 영전압 스위칭을 통해 고주파 스위칭이 가능하다는 장점이 있어 절연을 위해 사용하는 커패시터 값을 접촉 전류 규정에 맞게 줄일 수가 있다. 전도 전자 방해 노이즈를 발생시키는 고주파의 공통모드 전류를 제거하기 위해서는 컨버터를 대칭형으로 설계하는 방식을 사용한다. 본 논문에서는 LC 직렬 네트워크를 사용하는 정전식 클래스 E 컨버터와 T-네트워크를 사용하는 정전식 클래스 E 컨버터의 공통모드 전류를 분석하였다. 여기서 T-네트워크는 컨버터의 입출력비를 설정할 수 있도록 설계되었고 논문에서 이 네트워크를 설계 방식도 같이 제시하였다. 기존의 클래스 E 컨버터와 대칭형 클래스 E 컨버터의 공통모드 전류를 비교하였고 대칭형 컨버터에서 파라미터 오차에 의한 공통모드 전류도 본 논문에서 분석하였다. 마지막으로 대칭형 클래스 E 컨버터를 설계하기 위해서는 스위치가 상측에 배치되어야 하는데 이를 위해서는 스위치의 게이트 드라이버의 전원을 공급해주는 회로가 추가로 필요하다. 본 논문에서는 스위치에 인가되는 전압을 이용해

게이트 구동기의 전원을 공급해주는 회로를 제시한다.

제안한 컨버터는 40W급의 7cm x 3cm 크기의 프로토타입을 이용해 실험을 진행했다. LC 직렬 네트워크를 사용하는 정전식 절연형 클래스 E 컨버터와 T-네트워크를 사용하는 정전식 절연형 클래스 E 컨버터를 실험했고 접촉 전류와 전도 전자 방해 노이즈를 측정했다. 제안한 정전식 절연형 컨버터가 기존의 컨버터에 비해 전도 전자 방해 노이즈를 감소시킬 수 있었고 접촉 전류 또한 규정에 맞게 제한되어 제안하는 정전식 절연형 컨버터의 안정성을 확인하였다.

주요어 : 정전식 절연, 고주파 컨버터, 접촉 전류, 전도 전파 장해
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