Ph. D. DISSERTATION

Defect-engineering of Atomic Layer Deposited Hafnium Oxide layer for Neural Network Application and 1-Transistor – 1-Resistor (1T-1R) array

by

Gil Seop Kim

February 2022

Department of Materials Science and Engineering
College of Engineering
Seoul National University

Defect-engineering of Atomic Layer Deposited Hafnium Oxide layer for Neural Network Application and 1-Transistor – 1-Resistor (1T-1R) array

Advisor: Prof. Cheol Seong Hwang

By
Gil Seop Kim

A thesis submitted to the Graduate Faculty of Seoul National University in partial fulfillment of the requirements for the
Degree of Doctor of Philosophy
Department of Materials Science and Engineering

February 2022

Approved
by

Chairman of Advisory Committee: Jin Young Kim

Vice-chairman of Advisory Committee: Cheol Seong Hwang

Advisory Committee: Min Hyuk Park

Advisory Committee: Kyung Min Kim

Advisory Committee: Jung Ho Yoon

Abstract

The next-generation non-volatile memories (NVMs), the ReRAM, has been under great attention for its relatively simple structure, high scalability, low power, high speed, good reliability, and CMOS compatibility. Among the various materials and device candidates, metal-oxide-based ReRAM has been investigated for mechanism analysis and device implementation in the past several decades. The extensive chemical, structural, and electrical characterizations disclosed that the repeated formation and annihilation of the conduction filament (CF), mainly composed of oxygen vacancy (V_O), is responsible for the resistive switching (RS) mechanism. The HfO_2 is one of the most extensively studied materials in this field, where the V_O-induced CF mechanism also controls RS. Despite the significant improvement in the material property understanding and integration processes, there are still several critical hurdles to be overcome for commercialization, such as poor retention performance and switching non-uniformity. Since the CF involved in the resistive switching in HfO_2-based ReRAM consists of V_O's, it is essential to control V_O in the RS layer to achieve improved and desired switching performance.

As the first part of this work, the unusual retention failure mechanism of a HfO_2-based ReRAM device with an ultra-thin HfO_2 RS layer was elucidated. A 1-nm-thick HfO_2 thin film grown via thermal atomic layer deposition (ALD)

was employed as the RS layer. The test device structure was integrated on a 300-mm-diameter wafer using state-of-the-art fabrication technology in a commercial research facility in SK Hynix. Unlike the retention failure reported in other thicker oxide-based resistance switching memories, the current of both the low resistance (LRS) and high resistance (HRS) states suddenly increased at a particular time, causing retention failure. As a result of the retention analysis on the devices proceeded different program processes, it was determined that the involvement of the reset step induced the retention failure. The pristine device contained a high portion of the V_O-rich region, and the location of the border between the V_O-rich and V_O-free regions played a critical role in governing the retention performance. This borderline moves towards the Ta electrode during the reset step, but it moves back to the original location during the retention period, which eventually causes the reconnection of the disconnected conducting filament or strengthens the connected weak portion. The activation energy for the retention failure mechanism was 0.15 eV, which is related to the ionization of neutral V_O to ionized V_O.

Based on the switching mechanism and similar material stack of structure, Ta/HfO_2/RuO_2 ReRAM device was adopted to improve the system performance of the fully connected neural network in identifying the black-and-white characters (MNIST data set). The optimized Ta top electrode (TE) and RuO_2 bottom electrode (BE) conditions were considered referring to previous researches. The HfO_2 thickness was controlled to ~3.0 nm, which is thin enough

to ensure the electroforming (EF)-free behavior but still thick enough to maintain a useful on-to-off ratio. For comparison, a thicker HfO_2 layer (~4.5 nm) device with an identical material stack was fabricated, which obviously required the EF process to induce proper switching functionality. As a reference device, the conventional Ta/HfO_2/TiN ReRAM with a ~4.5-nm-thick HfO_2 layer was also fabricated, and their device characteristics were compared. Along with the EF-free characteristic, the optimized Ta/3.0 nm–HfO_2/RuO_2 ReRAM showed improved retention and uniformity. In addition, it showed improved analog switching behaviors and synaptic performances. The chemical analysis of the layer stack provided several clues to identifying the reasons for such improvements, and a related switching model was suggested. Finally, its application to the neuromorphic neural network was inspected by computer simulation using the experimentally estimated potentiation–depression curves. The use of such an improved synapse device improved MNIST dataset recognition.

Vertical-string 1T-1R array called ‘V-TFT-ReRAM’ has been under great interest as a successor of V-NAND flash. As prior research to the next-generation V-TFT-ReRAM, the HfO_2-based planar structure 1T-1R device was investigated as follows. Since the fabrication variable that can control the RS behavior was limited to the properties of the RS layer because of the inherently symmetric device structure, it was crucial to engineering the defect like V_O in the resistor to achieve the planar-direction NVM behavior and compatibility

with 1T. From the MIM leakage current analysis of HfO_2 deposited under different ALD conditions, it was confirmed that the defect properties of HfO_2 can be controlled by deposition conditions like substrate temperature and O_2-plasma power. Next, The large-scale 1T-1R with HfO_2 resistor was investigated, in which the most stoichiometric PEALD-HfO_2 and the most O-deficient THALD-HfO_2 were applied as RS layers. For the planar-direction NVM behavior between source and drain electrode, scaled-1R with a 20nm of switching-length using e-beam lithography process was evaluated. In the scaled-1R with stoichiometric PEALD-HfO_2, repetitive planar-direction NVM behavior was observed, and compatibility with 1T for stable operation in merged 1T-1R was achieved. Finally, the experimental data-based cell-string number simulation was examined, and it was concluded that more than 200 cell-string of 1T-1R is possible.

Keywords: resistance random access memory, ReRAM, conduction filament, resistive switching, RS, oxygen vacancy, V_O, HfO_2, atomic layer deposition, ALD, low resistance state, high resistance state, LRS, HRS, electroforming, retention, uniformity, synapse, potentiation, depression, LTP, LTD, neuromorphic, Vertical, non-volatile-memory, NVM

Student ID: 2017 – 23054

Gil Seop Kim

Table of Contents

(1) Kim, G. S.; Park, T. H.; Kim, H. J.; Ha, T. J.; Park, W. Y.; Kim. S. G.; Hwang, C. S. Investigation of the retention performance of an ultra-thin HfO_2 resistance switching layer in an integrated memory device. *J. Appl. Phys.* **2018**, 124, 024102.

(2) Kim, G. S.; Song, H.; Lee, Y. K.; Kim, J. H.; Kim, W.; Park, T. H.; Kim, H. J.; Kim, K. M.; Hwang, C. S. Defect-Engineered Electroforming-Free Analog HfO_x Memristor and Its Application to the Neural Network. *ACS Appl. Mater. Interfaces* **2019**, 11 (50), 47063-47072.

(3) Kim, G. S. HfO_2-based planar 1T-1R device and Resistive switching behavior for Next-generation Vertical-string 1T-1R array. Preparing for submission

List of Figures

after the deposition. During XPS measurement, each sample is etched by Ar^+ plasma. In the XPS data, the Hf-line of etching time from the 30s to 300s is from the surface region (30s) to RuO_2(or TiN) / HfO_2 interfacial region (300s) in HfO_2 layer. (a) show XPS experimental data of the Hf *4f* with depth profile, deconvolution results of etching time (b) 30s (most surface region), (c) 150s (middle portion of the film), and (d) 300s (near RuO_2/HfO_2 interfacial region) in RuO_2/HfO_2 30 ALD-cycled sample. (e) show XPS experimental data of the Hf *4f* with depth profile, deconvolution results of etching time (f) 30s (most surface region), (g) 150s (middle portion of the film), and (h) 300s (near TiN/HfO_2 interfacial region) in TiN/HfO_2 30 ALD-cycled sample. The black dot and red lines are the experimental results and deconvolution results, and the blue dot and green dot are the Hf-oxide curve and metallic-Hf curve, respectively.

Figure 3-5. XPS spectra of the O *1s*, Ru *3d*, and Ti *2p* region with depth profile and fitting results for the RuO_2/HfO_2 30 ALD-cycled sample and TiN/HfO_2 30 ALD-cycled sample. Each sample was measured right after as-deposition. During XPS measurement, each sample is etched by Ar^+ plasma.

Figure 3-6. Schematics of the oxygen vacancy distribution of (a) T-45, (b) R-45, and (c) R-30 devices. The left, middle, and right panels in each figure show the initial state (before the electro-forming), the as-

plasma, 280°C) in Figure 4-2, respectively. And (d-f) show the output curve of the device measured in (a-c), respectively.

Figure 4-4. (a) The resistive switching behavior of PEALD-HfO_2 deposited 1T-1R with stable channel-on and -off operations. In the measurement, the channel-length and -width(= switching-length and -width) are 0.5**μm** and 10.0**μm**, respectively. (b) and (c) show the output current flow of PEALD-HfO_2 deposited 1T-1R device in the case of channel-off and –on state, respectively.

Figure 4-5. (a) The fabrication flow of etch-stop-layer(ESL)-type 1T-1R device. The inserted SiO_2 passivation is deposited 100nm using plasma-enhanced-chemical-vapor-deposition (PECVD) and dry-etched. (b) ESL-type 1T-1R device; the PECVD-SiO_2 passivation layer is inserted between the channel and source/drain electrode. In the structure, the channel length is determined by the length of PECVD-SiO_2 passivation, and switching length is determined by the pattern distance of the source and drain electrode.

Figure 4-6. The transfer behavior of 1T-reference structure (a, channel-length/width 5.0/10.0**μm**), SiO_2-passivated 1T-reference structure (b, channel-length/width 5.0/10.0 **μm**). The transfer behavior of SiO_2-passivated ESL-type 1T structure (c, channel-length/width 5.0/10.0 **μm** and switching-length/width 0.5/10.0 **μm**), and SiO_2-passivated ESL-type 1T-1R structure (d, channel-length/width 5.0/10.0 **μm** and switching-length/width

0.5/10.0 **μm**), respectively. The inset shows the top and cross-section scheme of each device structure.

Figure 4-7. The I-V curve of SiO_2-passivated ESL-type 1T device in the condition of channel-off state (V_{gate} -10V). In the measurement, V_{drain} **±20V** and **±40V** are applied between the source and drain electrode as shown in (a) and (b). The I-V curve of SiO_2-passivated ESL-type 1T-1R in the condition of channel-off state (V_{gate} -10V) and V_{drain} **±20V** and **±30V** are applied between source and drain as shown in (c) and (d), respectively.

Figure 4-8. The I-V curve of scaled-1R devices using (a) PEALD-HfO_2 and (b) O-deficient THALD-HfO_2, respectively. (c) SEM top view image and scheme of scaled-1R, and each device has 20nm and 50nm of switching-length and -width, respectively. (d) The resistance change according to switching number of scaled-1R with PEALD-HfO_2 in the condition of I_{CC} 3**μA**, V_{set} ~1.2V, and V_{reset} ~-0.8V. (e) The retention performance of the scaled-1R device with PEALD-HfO_2 at 298K.

Figure 4-9. (a) The overlapped curve of output curve of ESL-type 1T and I-V curve of scaled-1R. (b) The read current (at $V_{BL,\ read}$ 0.4V) of selected device flowing through bit-line (BL) depending on the cell-string number in the worst case of the read operation in (d). (c) The programming voltage of BL for resistive-switching in the

resistor of the selected device depending on the cell-string number considering the worst case of the write operation in (e).

List of Abbreviations

AC	Alternating Current
ALD	Atomic Layer Deposition
ALD	Atomic Layer Deposition
BE	Bottom Electrode
BRS	Bipolar Resistive Switching
BL	Bit Line
CBA	Cross Bar Array
CF	Conducting Filament
CMOS	Complementary Metal Oxide Semiconductor
CV	Coefficient of Variation
CVD	Chemical Vapor Deposition
CVS	Constant Voltage Stress
DC	Direct Current
EF	Electro-Forming
ESL	Etch Stop Layer
GPC	Growth Per Cycle
G-V	Conductance-Voltage
HRS	High Resistance State
I_{CC}	Current Compliance
ICP	Inductively Coupled Plasma
I-V	Current-Voltage
LRS	Low Resistance State
LTD	Long Term Depression
LTP	Long Term Potentiation

MIM	Metal-Oxide-Metal
NVM	Non Volatile Memory
QPC	Quantum Point Contact
ReRAM	Resistance Random Access Memory
RF	Radio Frequency
RS	Resistance Switching
SEM	Scanning Electron Microscope
TE	Top Electrode
TFT	Thin Film Transistor
URS	Unipolar Resistive Switching
V_{drain}	Drain Voltage
V_{gate}	Gate Voltage
V-NAND	Vertical-NAND
V_O	Oxygen Vacancy
V_{reset}	Reset Voltage
V_{set}	Set Voltage
WL	Word Line
XPS	X-ray Photoelectron Spectroscopy
XRD	X-ray Diffraction
1T-1R	1-Transistor-1Resistor

1. Introduction

1.1. Oxide-based Resistive Random Access Memory

Metal-oxide-based resistance random access memory (ReRAM) has been examined in the past several decades for both mechanism analysis and device implementation. The extensive chemical, structural, and electrical characterizations revealed that oxygen vacancy (V_O) generation and the repeated formation and rupture of the percolation path mainly composed of V_O's, which is called "conducting filament (CF)," is responsible for the resistance switching (RS) mechanism.[1-5] ReRAM has a metal-insulator-metal (MIM) capacitor-like structure in which an insulator is sandwiched between two metal electrodes, the top electrode (TE) and the bottom electrode (BE), and can be categorized into unipolar (URS) and bipolar resistive switching (BRS). When a bias stimulus is applied to the electrode, the V_O formed or already existed in the RS layer forms CF. If the filament consist of V_O's connects both electrodes, current flows through the filament, and the device is switched from high resistance (HRS) to low resistance (LRS); called set-switching. If the filament connecting both electrodes is ruptured due to the bias stimuli and joule-heating, the current flowing through the filament is decreased, and the device is switched from low resistance (LRS) to high resistance (HRS); called reset-switching. The URS shows that set/reset is independent of bias polarity,

and the BRS shows that set/reset depends on bias polarity. HfO_2 is one of the most extensively studied materials in this field, where the V_O-induced CF mechanism also controls RS. Since the CF involved in resistive switching in HfO_2-based ReRAM consists of V_O, it is important to control V_O in the RS layer to improve switching performance. There are several researches that improve the switching performance of ReRAM by V_O-control in the RS layer. Among them, the electrode is a crucial ingredient that might improve the device's performance. For many ReRAMs using an oxide switching layer, the electrodes must play the role of oxygen reservoir or oxygen transport layer.[6-11] In several cases, an additional oxygen reservoir layer has been adopted, especially in cases where the electrodes can hardly take the role, such as TiN.[11] On the other hand, stable operation of the resistance switching upon repeated pulse-switching, i.e., involving invariable R_{LRS}, R_{HRS}, V_{set}, and V_{reset}, which are the LRS and HRS resistance, and the set and reset voltages, respectively, is essential but has remained rather challenging. As the repeated operation of the resistance switching is usually accompanied by the gradual loss of oxygen from the limited memory cell volume, confirming the stability of the above-mentioned parameters is generally challenging.

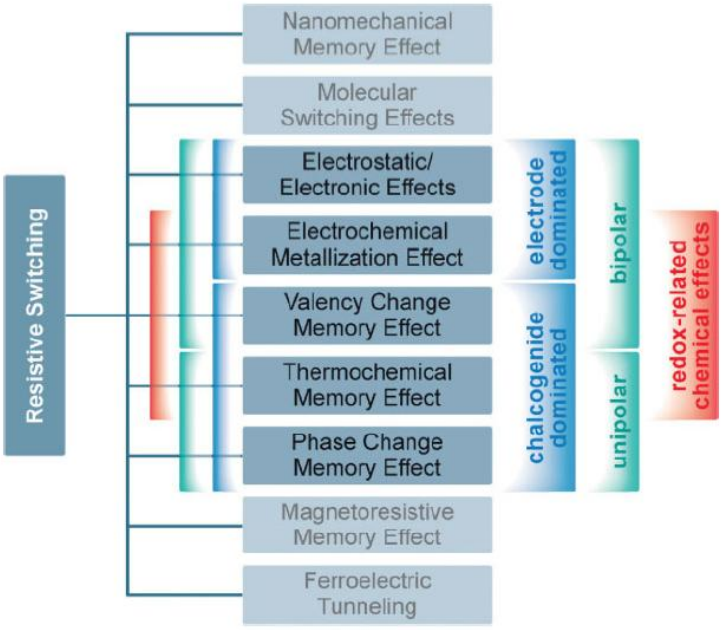


Figure 1-1. Classification of the resistive switching effects which are considered for non-volatile-memory applications.[2]

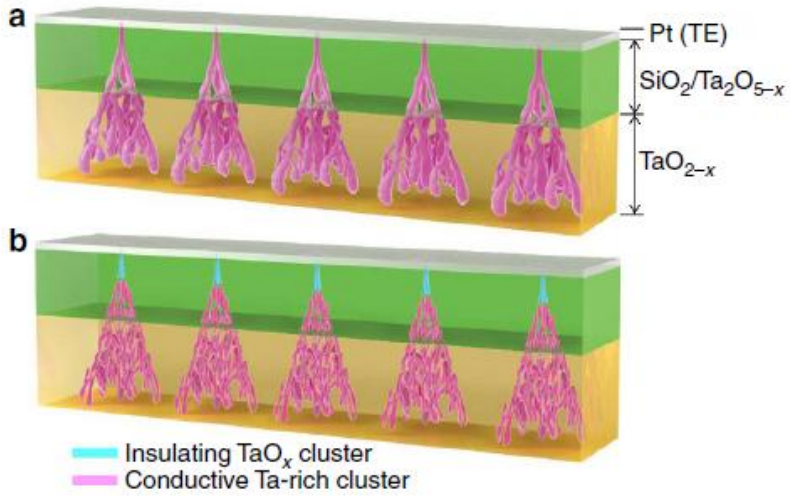


Figure 1-2. Schematic diagram illustrating resistance-switching mechanism in the Ta_2O_{5-x}/TaO_{2-x} device. Formation and annihilation of conducting channel during the (a) set and (b) reset state are shown.[5]

1.2. Switching reliability issue in Oxide-based ReRAM

In the metal-oxide-based ReRAM research, despite the significant improvement in the material property understanding and integration processes, there are still several critical hurdles to be overcome for commercialization.[12-15] Among them, the poor retention performance of the V_O-related CF mechanism is critical.[16-18] Here, retention means retaining the resistance values of the LRS and HRS over time with or without small read voltage application. As a reliable non-volatile memory, the values should be invariant for 10 years at an operation temperature of 85ºC, but many of the oxide-based ReRAMs fail to meet such criteria. This is understandable because the V_O percolation path (CF) is thermodynamically unstable — i.e., it is a type of kinetic memory and thus must be prone to thermal disturbance. Therefore, the LRS resistance suddenly increases to a high value at a particular time. In contrast, HRS usually suffers from the loss of a high resistance value, which is related to the diffusion of V_O's into the CF-ruptured region during the retention period. Under this circumstance, the HRS resistance decreases gradually or abruptly.[16, 17]

Another critical issue is the switching non-uniformity between different ReRAM devices in a given ReRAM array and different switching cycles for a given ReRAM device. This is understandable from the inherently random nature of defect (V_O) generation in oxide materials, and their percolation and annihilation must be even more random, making their sufficient control highly challenging.[19-21] Most of the MIM-structured ReRAM are highly insulating at

the as-fabricated state, which requires an electroforming (EF) step to operate them as a feasible memory or synapse. EF corresponds to a soft-breakdown of the insulating layer, which usually induces several CFs in the insulating matrix, such as HfO_2, as in this work. In insulating oxides, the CFs are usually composed of oxygen (O)-deficient phases, such as Magnéli in TiO_2,[22-26] or V_O clusters, as in HfO_2 and Ta_2O_5.[5-8, 27] However, such EF process also induces several undesired side effects, which largely degrade the ReRAM performances of uniformity, endurance, and retention. In addition, from the driving circuit point of view, incorporating an EF control circuit into the system is highly undesirable. EF of all the components in a system using a test process before chip shipping is also very burdensome. Therefore, exploiting an EF-free ReRAM could be an achievable solution to the numerous issue mentioned above.

1.3. Synaptic performance of Oxide-based ReRAM

Since the analog switching characteristics of a ReRAM were identified as mimicking the functions of a synapse, ReRAM-based neuromorphic computing technology utilizing the ReRAM as a synapse has been widely researched.[28-36] The ReRAM synapse can be integrated into a two-terminal MIM structure, which is suitable as the memory element in a passive crossbar array (CBA). Since the CBA structure has the smallest feature size and the highest integration density, it can be a feasible building block for the ReRAM-based neural network. One of the ReRAM synapse challenges is its non-ideal analog characteristic and inherent resistance variability that originates from its stochastic resistance switching nature.[37-41] For example, for an ideal artificial neural network, it is desirable for a ReRAM to have a constant conductance change rate upon the application of a given voltage stimulus over the entire conductance range, which is termed 'linearity', and the same conductance change rate during potentiation and depression, which is termed 'symmetry'. Potentiation and depression mean the increase and decrease in the electrical conductance, respectively, with the repeated electrical voltage pulse application. These features can be obtained by measuring the long-term potentiation and depression (LTP and LTD) characteristics and plotting the conductance values as a function of the number of the set (switching from the HRS to LRS) and reset (switching from the LRS to HRS) voltage pulses, respectively. If the LTP and LTD curves of a given ReRAM are linear and symmetric, it corresponds to

an ideal synaptic device. However, due to the drift- and diffusion-based kinetics in the ReRAM switching phenomena, where the variation is usually faster at the beginning of the potentiation and depression processes, compared with that after the process, the synaptic performance of the ReRAM is usually relatively remote from the ideal behavior.[42-45] Another critical issue is the involvement of the random variation in the device characteristics between the cells and switching operations, which certainly impacts the network's performance.[43, 44] Such variations can be quantified by adopting a coefficient of variation (CV) that defines the ratio of the standard deviation (σ) to the mean value (μ). In addition to these synaptic performances, conventional memory performance indicators, such as the retention and endurance of the memory cell, are still the crucial factors for the ReRAM to have in the neural network.[1-4, 20, 21, 45]

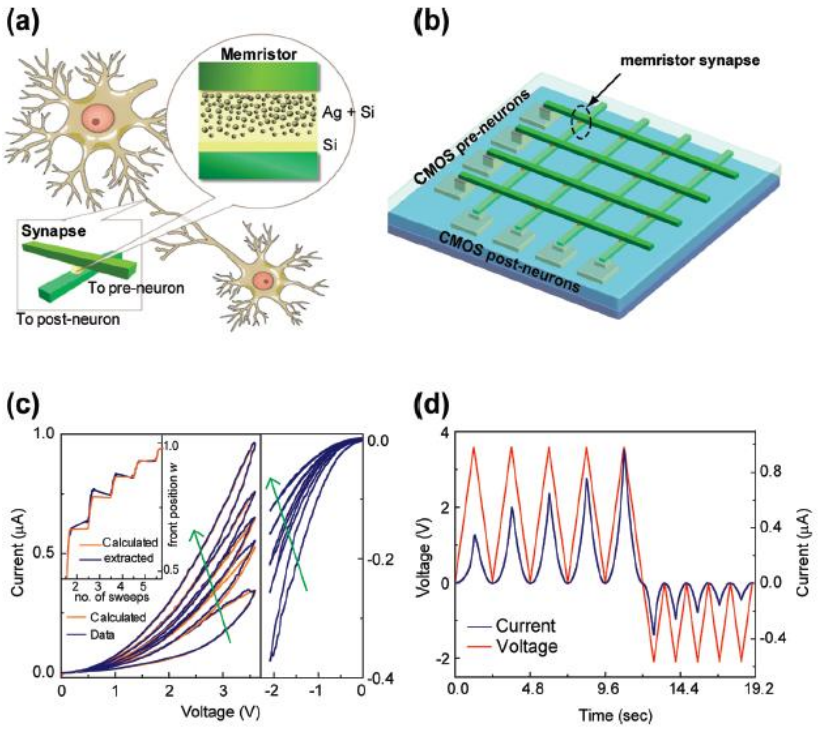


Figure 1-3. Nanoscale memristor characteristics and its application as a synapse. (a) schematic illustration of the concept of using memristors as synapses between neurons. (b) Schematic of a neuromorphic with CMOS neurons and memristor synapses in a crossbar configuration. (c) Measured and calculated I-V characteristics of the memristor (d) The current and voltage data versus time for the device.[32]

1.4. Vertical-array structure of Oxide-based ReRAM

At present, the main non-volatile storage memory is NAND flash memory, which has faced limitations because of parasitic effects by scaling down. 2-dimensional NAND flash has encountered physical limitations to cell size reduction, such as cell to cell interference and cell uniformity.[46-51] Although 3-dimensional stacked vertical-NAND flash (V-NAND flash) proposes higher density than planar type, V-NAND flash has other issues like technical difficulties in the hole etching process as the aspect ratio increases, charge loss in the lateral direction, and word plane parasitic capacitance as each oxide gets thinner.[52-57] The next-generation NVMs, the ReRAM, has been widely studied because of its relatively simple MIM structure, high scalability, low power, high speed, good reliability, and complementary metal-oxide-semiconductor (CMOS) compatibility. Representative commercialization of RS memory is Intel's '3D Xpoint', named by the 'Optane' brand. 3D Xpoint has a unit cell size of $4F^2$ in the form of a CBA using phase-change memory. However, as the number of vertical stacks increases, the fabrication cost is exponentially increased because functional line process such as photolithography and etching is increased. In addition, a two-terminal structure did not fit the existing CPU design. Other structures for stacking ReRAM can be divided into a side-wall-type and a hole-type vertical structure.[12, 58-60] The hole-type vertical structure stacks word lines and isolation layers alternately, then etch holes and deposits

thin-film-transistors (TFT, T) and resistors (R) on the wall. The hole-type vertical structure can suppress sneak path current efficiently, as TFT can play a selector role. In the hole-type vertical structure, TFT for device selection and the resistor for storing the memory are connected in parallel as unit devices, and the unit devices are connected in serial. Such vertical-string 1T-1R array is called 'V-TFT-ReRAM,' and the conditions required for operation are as follows.[58]

In "V-TFT-ReRAM", an oxide-based RS layer is deposited inside the hole after the transistor fabrication. In this structure, the RS layer and channel are in direct contact forming an effective parallel circuit structure. V-TFT-ReRAM can be operated by turning off the corresponding TFT parallel to the selected device in writing and reading modes. For the fluent operation of the V-TFT-ReRAM device, the following conditions must be satisfied. The sum of all the on-TFTs (R_S^T) on-resistances must be low to provide proper voltage to the selected 1T-1R unit cell. Also, the off-resistance of the TFT (R_{off}^T) of the selected cell must be high compared with the on- and off-resistance of the selected memory cell (R_{on}^m and R_{off}^m) to efficiently apply the operating current to the memory cell, which must be supplied through the TFT channel string.[58]

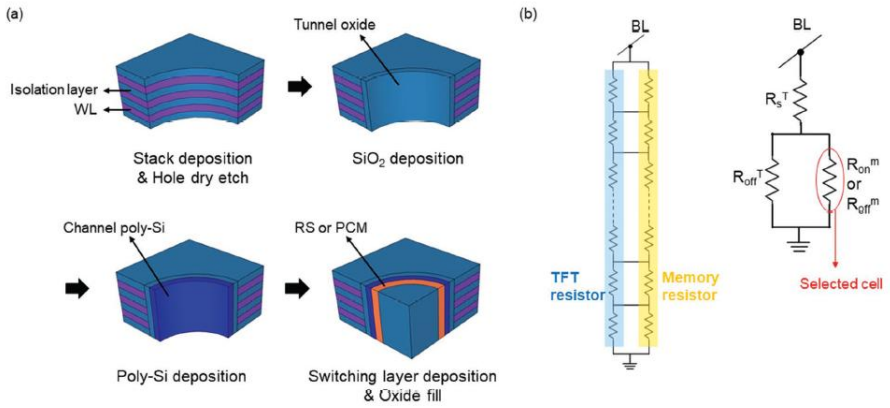


Figure 1-4. (a) Schematic figures of the process sequence for V-TFT-ReRAM fabrication and (b) Circuit diagram of the V-TFT-ReRAM and simplification of the circuit.[58]

1.5. Research Scope and Chapter Overview

The objective of the present thesis is to study the defect-engineering of atomic-layer-deposited HfO_2 resistive switching layer to improve resistive switching performance and achieve planar-direction resistive switching behavior for neural network and V-TFT-ReRAM (1T-1R) applications.

Chapter 2 presents the retention behavior of a HfO_2 resistive switching memory device with a 28 nm diameter and an ultra-thin (1 nm) HfO_2 layer as the switching layer. Unlike the retention failure phenomenon reported in other thicker oxide-based ReRAM, the current of both the low and high resistance states suddenly increased at a certain time, causing retention failure. Through the retention tests of the devices under different resistance states, it was concluded that the involvement of the reset step induced the retention failure. The pristine device contained a high portion of the V_O-rich region, and the location of the border between the V_O-rich and V_O-free regions played a critical role in governing the retention performance. During the reset step, this borderline moves towards the Ta electrode, but it moves back to the original location during the retention period, which eventually induces the reconnection of the disconnected conducting filament or strengthens the connected weak portion. Finally, the activation energy for the retention failure mechanism, 0.15 eV, was obtained through temperature dependency analysis of retention failure, which is related to the ionization of neutral V_O to ionized V_O.

Chapter 3 suggests $Ta/HfO_2/RuO_2$ ReRAM device to improve the switching

characteristics and the system performance of the fully connected neural network in identifying the black-and-white characters (MNIST data set). The HfO_2 thickness was controlled to ~3.0 nm, which is just thin enough to ensure the EF-free behavior but still thick enough to maintain a useful on-to-off ratio. For comparison, a similar material stack, but with thicker HfO_2 film (~4.5 nm), was also fabricated, which obviously required the EF process to induce useful switching functionality. As a reference device, the conventional Ta/HfO_2/TiN ReRAM cell with a ~4.5-nm-thick HfO_2 film was also fabricated, and their device characteristics were compared. Along with the EF-free characteristic, the optimized Ta/3.0 nm–HfO_2/RuO_2 ReRAM showed improved retention and uniformity. Also, it showed improved analog switching behaviors and synaptic performances (improved linearity and symmetry factors). The chemical analysis of the film stack provided several clues to identifying the reasons for such improvements. Finally, its application to the neuromorphic neural network was examined by computer simulation using the experimentally estimated potentiation–depression curves. And it is shown that the use of such an improved synapse device improved MNIST dataset recognition.

Chapter 4 covers the HfO_2-based planar structure 1T-1R device as prior research to the V-TFT-ReRAM for replacing V-NAND-flash. Since the fabrication variable that can control the resistive switching behavior was limited to the properties of the RS layer because of the inherently symmetric device structure, it was essential to engineer the defect like V_O in the resistor to obtain the planar-direction NVM behavior and compatibility with 1T. From the

MIM leakage current analysis of HfO_2 deposited under different ALD conditions, it was confirmed that the defect properties of HfO_2 can be controlled by deposition conditions like substrate temperature and O_2-plasma power. Next, the large-scale 1T-1R with HfO_2 resistor was investigated, in which the most stoichiometric PEALD-HfO_2 and the most O-deficient THALD-HfO_2 were used. For the planar-direction NVM behavior between source and drain electrode, scaled-1R with a 20nm of switching-length using e-beam lithography process was evaluated. In the scaled-1R with stoichiometric PEALD-HfO_2, repetitive planar-direction NVM behavior was observed, and compatibility with 1T for stable operation in merged 1T-1R was achieved. Finally, it was confirmed that more than 200 cell-string of 1T-1R is possible as s result of the experimental data-based cell-string number simulation.

Finally, in chapter 5, the conclusion of the thesis is made.

1.6. References

(1) Kim, K. M.; Jeong, D. S.; Hwang, C. S. Nanofilamentary resistive switching in binary oxide system; a review on the present status and outlook. *Nanotechnol.* **2011,** *22*, No. 254002.

(2) Waser, R.; Dittmann, R.; Staikov, G.; Szot, K. Redox-Based Resistive Switching Memories -Nanoionic Mechanisms, Prospects, and Challenges. *Adv. Mater.* **2009,** *21*, 2632-2663.

(3) Yang, J. J.; Zhang, M.-X.; Strachen, J. P.; Miao, F.; Pickett, M.; Kelley, R. D.; Medeiros-Ribeiro, G.; Williams, R. S. High switching endurance in TaO_x memristive devices. *Appl. Phys. Lett.* **2010,** *97*, No. 232102.

(4) Miao, F.; Strachen, J. P.; Yang, J. J.; Zhang, M.-X.; Goldfarb, I.; Torrezan, A. C.; Eschbach, P.; Kelley, R. D.; Medeiros-Ribeiro, G.; Williams, R. S. Anatomy of a Nanoscale Conduction Channel Reveals the Mechanism of a High-Performance Memristor. *Adv. Mater.* **2011,** *23*, 5633-5640.

(5) Park, G.-S.; Kim, Y. B.; Park, S. Y.; Li, X. S.; Heo, S.; Lee, M.-J.; Chang, M.; Kwon, J. H.; Kim, M.; Chung, U.-I.; Dittmann, R.; Waser, R.; Kim, K. *In Situ* Observation of Filamentrary Conducting Channels in an Asymmetric Ta_2O_{5-X} / TaO_{2-X} Bilayer Structure. *Nat. Commun.* **2013,** *4*, No. 2382.

(6) Park, T. H.; Song, S. J.; Kim, H. J.; Kim, S. G.; Chung, S.; Kim, B. Y.; Lee, K. J.; Kim, K. M.; Choi, B. J.; Hwang, C. S. Thickness effect of ultra-thin Ta_2O_5 resistance switching layer in 28 nm-diameter memory cell. *Sci. Rep.* **2015,** *5*, No. 15965.

(7) Park, T. H.; Kim, H. J.; Park, W. Y.; Kim, S. G.; Choi, B. J.; Hwang, C. S. Roles of conducting filament and non-filament regions in the Ta_2O_5 and HfO_2 resistive switching memory for switching reliability. *Nanoscale* **2017,** *9*, 6010-

6019.

(8) Park, T. H.; Kwon, Y. J.; Kim, H. J.; Woo, H. C.; Kim, G. S.; An, C. H.; Kim, Y.; Kwon, D. E.; Hwang, C. S. Balancing the Source and Sink of Oxygen Vacancies for the Resistive Switching Memory. *ACS Appl. Mater. Interfaces.* **2018,** *10*, 21445-21450.

(9) Xue, W. H.; Xiao, W.; Chen, X. X.; Zhu, X. J.; Shang, J.; Pan, L.; Tan, H. W.; Zhang, W. B.; Ji, Z. H.; Liu, G.; Xu, X.-H.; Ding, J.; Li, R.-W. Intrinsic and Interfacial Effect of Electrode Metals on the Resistive Switching Behaviors of Zinc Oxide Films. *Nanotechnology* **2014,** *24*, No. 425204.

(10) Ge, N.; Zhang, M.-X.; Zhang, L.; Yang, J. J.; Li, Z.; Williams, R. S. Electrode-Material Dependent Switching in TaO_x Memristors. *Semicond. Sci. Technol.* **2014,** *29*, No. 104003.

(11) Lee, M.-J.; Lee, C. B.; Lee, D.; Lee, S. R.; Chang, M.; Hur, J. H.; Kim, Y.-B.; Kim, C.-J.; Seo, D. H.; Seo, S.; Chung, U.-I.; Yoo, I.-K.; Kim, K. A fast, high-endurance and scalable non-volatile memory device made from asymmetric Ta_2O_{5-X}/TaO_{2-X} bilayer structures. *Nat. Mater.* **2011,** *10*, 625-630.

(12) Yoon, J. H.; Song, S. J.; Yoo, I.-H.; Seok, J. Y.; Yoon, K. J.; Kwon, D. E.; Park, T. H.; Hwang. C. S. Highly Uniform, Electroforming-Free, and Self-Rectifying Resistive Memory in the Pt/Ta_2O_5/HfO_{2-X}/TiN Structure. *Adv. Funct. Mater.* **2014,** *24*, 5086-5095.

(13) Lee, H. T.; Chen, P. S.; Wu, T. Y.; Chen, Y. S.; Wang, C. C.; Tzeng, P. J.; Lin, C. H.; Chen, F.; Lien, C. H.; Tsai, M, -J. Low Power and High Speed Bipolar Switching with a Thin Reactive Ti Buffer Layer in Robust HfO_2 Based RRAM. *IEEE International Electron Devices Meeting. Technical Digest*, San Francisco, CA, USA,15-17 December 2008.

(14) Lee, B.; Wong, H. -S. P. NiO Resistance Change Memory with a Novel Structure for 3D integration and Improved Confinement of Conduction Path. *IEEE Symp. on VLSI Technology,* Honolulu, Hawaii, USA, June, 2009.

(15) Chen, Y. S.; Lee, H. Y.; Chen, P. S.; Gu, P. Y.;Chen, C. W.; Lin, W. P.; Liu, W. H.; Hsu, Y. Y.; Sheu, S. S.; Chiang, P. C.; Chen, W. S.; Chen, F. T.; Lien, C. H.; Tsai, M. -J. Highly Scalable Hafnium Oxide Memory with Improvements of Resistive Distrubution and Read Disturb Immunity. *IEEE International Electron Devices Meeting. Technical Digest*, Baltimore, MD, USA, 7-9 December 2009.

(16) Ninomiya, T.; Muraoka, S.; Wei, Z.; Yasuhara, R.; Katayama, K.; Takagi, T. Improvement of Data Retention During Long-Term Use by Suppressing Conductive Filament Expansion in TaO_x Bipolar-ReRAM. *IEEE Electron Device Lett*. **2013,** *34*, 762-764.

(17) Gao, B.; Zhang, H.; Chen, B.; Liu, L.; Liu, X.; Han, R.; Kang, J.; Fang, Z.; Yu, H.; Yu, B.; Kwong, D. L. Modeling of Retention Failure Behavior in Bipolar Oxide-Based Resistive Switching Memory. *IEEE Electron Device Lett*. **2011,** *32*, 276-278.

(18) Wei, Z.; Takagi, T.; Kanazawa, Y.; Katoh, Y.; Ninomiya, T.; Kawai, K.; Muraoka, S.; Mitani, S.; Katayama, K.; Fujii, S.; Miyanaga, R.; Kawashima, Y.; Mikawa, T.; Shimakawa, K.; Aono, K. Retention Model for High-density ReRAM. *IEEE Int. Memory Workshop,* Milan, Italy, May, 2012.

(19) Kwon, D.-H.; Kim, K.; Jang, J.; Jeon, J.; Lee, M.; Kim, G.; Li, X.-S.; Park, G.-S.; Lee, B.; Han, S.; Kim, M.; Hwang, C. S. Atomic Structure of Conducting Nanofilaments in TiO_2 Resistive Switching Memory. *Nat. Nanotechnol*. **2010,** *5*, 148-153.

(20) Choi, B. J.; Jeong, D. S.; Kim, S. K.; Rohde, C.; Choi, S.; Oh, J. H.; Kim, H.

J.; Hwang, C. S.; Szot, K.; Waser, R.; Reichenberg, B.; Tiedke, S.; Resistive Switching Mechanism of TiO_2 Thin Films Frown by Atomic-Layer Deposition. *J. Appl. Phys*. **2005,** *98*, No. 033715.

(21) Park, G.-S.; Li, X.-S.; Kim, D.-C.; Jung, R.-J.; Lee, M.-J.; Seo, S. Observation of electric-field induced Ni filament channels in polycrystalline NiO_x film. *Appl. Phys. Lett*. **2007,** *97*, No. 222103.

(22) Kim, G. H.; Lee, J. H.; Seok, J. Y.; Song, S. J.; Yoon, J. H.; Yoon, K. J.; Lee, M. H.; Kim, K. M.; Lee, H. D.; Ryu, S. W.; Park, T. J.; Hwang, C. S. Improved endurance of resistive switching TiO_2 thin film by hourglass shaped Magneli filaments. *Appl. Phys. Lett*. **2011,** *98*, No. 262901.

(23) Kim, K. M.; Park, T. H.; Hwang, C. S. Dual Conical Conducting Filament Model in Resistance Switching TiO_2 Thin Films. *Sci. Rep*. **2015,** *5*, No. 7844.

(24) Yoon, K. J.; Song, S. J.; Seok, J. Y.; Yoon, J. H.; Kim, G. H.; Lee, J. H.; Hwang, C. S. Ionic bipolar resistive switching modes determined by the preceding unipolar resistive switching reset behavior in Pt/TiO_2/Pt. *Nanotechnology* **2013,** *24*, No. 145201.

(25) Song, S. J.; Seok, J. Y.; Yoon, J. H.; Kim, K. M.; Kim, G. H.; Lee, M. H.; Hwang, C. S. Real-time identification of the evolution of conducting nano-filaments in TiO_2 thin film ReRAM. *Sci. Rep*. **2013,** *3*, No. 3443.

(26) Kim, K. M.; Lee, M. H.; Kim, G. H.; Song, S. J.; Seok, J. Y.; Yoon, J. H.; Hwang, C. S. Understanding structure-property relationship of resistive switching oxide thin films using a conical filament model. *Appl. Phys. Lett.* **2010,** *97*, No. 162912.

(27) Li, C.; Gao, B.; Yao, Y.; Guan, X.; Shen, X.; Wang, Y.; Huang, P.; Liu, L.; Lie, X.; Li, J.; Gu, C.; Kang, L.; Yu, R. Direct Observations of Nanofilament

Evolution in Switching Processed in HfO_2-Based Resistive Random Access Memory by In situ TEM studies. *Adv. Mater.* **2017,** *29*, No. 1602976.

(28) Waldrop, M. M. The Chips are down for Moore's law. *Nature* **2016,** *530*, 144-147.

(29) Di Ventra, M.; Pershin, Y. V. The parallel Approach. *Nat. Phys*. **2013,** *9*, 200-202.

(30) Yang, J. J.; Strukov, D. B.; Stewart, D. R. Memristive devices for computing. *Nat. Nanotechnol*. **2013,** *8*, 13-24.

(31) Yang, R.; Terabe, K.; Liu, G.; Tsuruoka, T.; Hasegawa, T. On-demand nanodevice with electrical and neuromorphic multifunction realized by local ion migration. *ACS Nano* **2012,** *6*, 9515-9521.

(32) Jo, S. H.; Chang, T.; Ebong, I.; Bhavitavya, B.; Mazumder, P.; Lu, W. Nanoscale memristor device as synapse in neuromorphic systems. *Nano Lett.* **2010,** *10*, 1297-1301.

(33) Feldman, D. E. The Spike-Timing Dependence of Plasticity. *Neuron*. **2012,** *75*, 556-571.

(34) Abbott, L. F.; Nelson, S. B. Synaptic plasticity: taming the beast. *Nat. Neurosci.* **2000,** *3*, 1178-1183.

(35) Li, Y.; Zhong, Y. P.; Zhang, J. J.; Xu, L.; Wang, Q.; Sun, H. J.; Tong, H.; Cheng, X. M.; Miao, X. S. Activity-Dependent Synaptic Plasticity of a Chalcogenide Electronic Synapse for Neuromorphic Systems. *Sci. Rep*. **2014,** *4*, No. 4906.

(36) Chang, T.; Jo, S.-H.; Lu, W. Short-Term Memory to Long-Term Memory Transition in a Nanoscale Memristor. *ACS Nano* **2011,** *5*, 7669-7676.

(37) Kim, S.; Du, C.; Sheridan, P.; Ma, W.; Choi, S.; Lu, W. D. Experimental

Demonstration of a Second-Order Memristor and Its Ability to Biorealistically Implement Synaptic Plasticity. *Nano Lett.* **2015,** *15*, 2203-2211.

(38) Wang, I. T.; Lin, Y. C.; Wang, Y. F.; Hsu, C. W.; Hou, T. H. 3D Synaptic Architecture with Ultralow Sub-10 FJ Energy per Spike for Neuromorphic Computation. *IEEE International Electron Devices Meeting,* San Francisco, USA, Dec 15-17, 2014.

(39) Jeong, Y.; Kim, S.; Lu, W. D. Utilizing Multiple State Variables to Improve the Dynamic Range of Analog Switching in a Memristor. *Appl. Phys. Lett.* **2015,** *107*, No. 173105.

(40) Woo, J.; Moon, K.; Song, J.; Lee, S.; Kwak, M.; Park, J.; Hwang, H. Improved Synaptic Behavior under Identical Pulses Using AlO_x/HfO_x Bilayer RRAM Array for Neuromorphic Systems. *IEEE Electron Device Lett*. **2016,** *37*, 994-997.

(41) Wang, Z.; Yin, M.; Zhang, T.; Cai, Y.; Wang, Y.; Yang, Y.; Huang, R. Engineering Incremental Resistive Switching in TaO_x Based Memritors for Brain-Inspired Computing. *Nanoscale* **2016,** *8*, 14015-14022.

(42) Woo, J.; Padovani, A.; Moon, K.; Kwak, M.; Larcher, L.; Hwang, H. Linking Conductive Filament Properties and Evlution to Synaptic Behavior of RRAM Devices for Neuromorphic Applications. *IEEE Electron Device Lett*. **2017,** *38*, 1220-1223.

(43) Kim, S.; Choi, B.; Lim, M.; Yoon, J.; Lee, J.; Kim, H.-D.; Choi, S.-J. Pattern Recognition Using Carbon Nanotube Synaptic Transistor with an Adjustable Weight Update Protocol. *ACS Nano* **2017,** *11*, 2814-2822.

(44) Yu, S.; Gao, B.; Fang, Z.; Yu, H.; Kang, J.; Wong, H.-S. P. A Low Energy Oxide-Based Electronic Synaptic Device for Neuromorphic Visual Systems with

Tolerance to Device Variation. *Adv. Mater*. **2013,** *25*, 1774-1779.

(45) Kim, K. M.; Choi, B. J.; Hwang, C. S. Localized Switching Mechanism in Resistive Switching of Atomic-Layer-Deposited TiO_2 Thin Films. *Appl. Phys. Lett*. **2007,** *90*, No. 242906.

(46) Fukuzumi, Y.; Matsuoka, Y.; Kito, M.; Kido, M.; Sato, M.; Tanaka, H.; Nagata, Y.; Iwata, Y.; Aochi, H.; Nitayama, A. Optimal Integration and Characteristics of Vertical Array Devices for Ultra-High Density, Bit-Cost Scalable Flash Memory, Proc. *IEEE Int. Electron Devices Meeting*, Washington, DC, USA. 10-12 Dec. **2007**, 449.

(47) Asenov, A.; Brown, A. R.; Davies, J. H.; Kaya, S.; Slavcheva, G. Simulation of intrinsic parameter fluctuations in decananometer and nanometer-scale MOSFETs, *IEEE Trans. Electron Devices.* **2003**, *50*, 1837.

(48) Lee, S. H.; Zhu, X.; Lu, W. D. Nanoscale resistive switching devices for memory and computing applications, *Nano Res*. **2020**, *13*, 1228–1243.

(49) Taur, Y.; Buchanan, D. A.; Chen, W.; Frank, D. J.; Ismail, K. E.; Lo, S. H.; Sai-Halasz, G. A.; Viswanathan, R. G.; Wann, H. -J. C.; Wind, S. J. CMOS scaling into the nanometer regime, *Proc. IEEE*. **1997**, *85*, 486–504.

(50) Frank, D. J.; Dennard, R. H.; Nowak, E.; Solomon, P. M.; Taur, Y.; Wong, H. -S. P. Device scaling limits of Si MOSFETs and their application dependencies. *Proc. IEEE*. **2001**, *89*, 259–288.

(51) Khan, H. N.; Hounshell, D. A.; Fuchs, E. R. H. Science and research policy at the end of Moore'S law. *Nat. Electron*. **2018**, *1*, 14–21.

(52) Omura, M.; Hashimoto, J.; Adachi, T.; Kondo, Y.; Ishikawa, M.; Abe, J.; Sakai, I.; Hayashi, H.; Sekine, M.; Hori, M. Formation mechanism of sidewall striation in high-aspect-ratio hole etching, *Jpn. J. Appl. Phys*. **2019**, *58*,

SEEB02.

(53) Sakamori, S.; Fujiwara, N.; Miyatake, H.; Oikawa, K.; Yamanaka, M.; Sasaki, T. Transformation of Dense Contact Holes during SiO2 Etching, *Jpn. J. Appl. Phys*, **2003**, *42* 3962.

(54) Izawa, M.; Negishi, N.; Yokogawa, K.; Momonoi, Y. Investigation of Bowing Reduction in SiO_2 Etching Taking into Account Radical Sticking in a Hole, *Jpn. J. Appl. Phys*, **2007**, *46* 7870.

(55) Miyake, M., Negishi, N.; Izawa, M.; Yokogawa, K.; Oyama, M.; Kanekiyo, T. Effects of Mask and Necking Deformation on Bowing and Twisting in High-Aspect-Ratio Contact Hole Etching, *Jpn. J. Appl. Phys*, **2009**, *48* 08HE01.

(56) Kim, J. K.; Lee, S. H.; Cho, S. I.; Yeom, G. Y. Study on contact distortion during high aspect ratio contact SiO_2 etching, *J. Vac. Sci. Technol. A*, **2015**, *33*, 021303.

(57) Negishi, N.; Miyake, M.; Yokogawa, K.; Oyama, M.; Kanekiyo, T.; Izawa, M. Bottom profile degradation mechanism in high aspect ratio feature etching based on pattern transfer observation, *J. Vac. Sci. Technol. B*, **2017**, *35*, 051205.

(58) Yoon, K. J.; Kim, Y.; Hwang, C. S. What Will Come After V-NAND—Vertical Resistive Switching Memory?, *Adv. Electron. Mater*. **2019**, 1800914.

(59) Kim, K. M.; Zhang, J.; Graves, C.; Yang, J. J.; Choi, B. J.; Hwang, C. S.; Li, Z.; Williams, R .S. Low-Power, Self-Rectifying, and Forming-Free Memristor with an Asymmetric Programing Voltage for a High-Density Crossbar Application, *Nano Lett*. **2016**, *16*, 11, 6724–6732.

(60) Bai, Y.; Wu, H.; Wu, R.; Zhang, Y.; Deng, N.; Yu, Z.; Qian, H. Study of Multi-level Characteristics for 3D Vertical Resistive Switching Memory, *Sci Rep 4*, **2014**, 5780

2. Investigation of retention performance of a 1-nm-thick HfO_2 resistance switching layer in a 28-nm-diameter memory device

2.1. Introduction

Metal-oxide-based resistance random access memory (ReRAM) has been examined in the past several decades for both mechanism analysis and device implementation. The extensive chemical, structural, and electrical characterizations revealed that oxygen vacancy (V_O) generation and the repeated formation and rupture of the percolation path mainly composed of V_O's, which is called "conducting filament (CF)," is responsible for the resistance switching (RS) mechanism.[1-5] HfO_2 is one of the most extensively studied materials in this field, where RS is also controlled by the V_O-induced CF mechanism. Despite the great improvement in the material property understanding and integration processes, there are still several critical hurdles to be overcome for commercialization.[6-9] Among them, the insufficient retention performance of the V_O-related CF mechanism is critical.[10-17] Here, retention means retaining the resistance values of the low resistance state (LRS) and high resistance state (HRS) over time with or without small read voltage application. As a reliable non-volatile memory, the values should be invariant

for 10 years at an operation temperature of 85ºC, but many of the oxide-based ReRAMs fail to meet such criteria. This is understandable because the V_O percolation path (CF) is thermodynamically unstable — i.e., it is a type of kinetic memory and thus must be prone to thermal disturbance. Therefore, the LRS resistance suddenly increases to a high value at a certain time. In contrast, HRS usually suffers from the loss of a high resistance value, which is related to the diffusion of V_O's into the CF-ruptured region during the retention check period. Under this circumstance, the HRS resistance decreases gradually or abruptly.[10-11]

Another critical issue is the switching non-uniformity between different memory cells in a given memory array and different switching cycles for a given memory cell. This is also understandable from the inherently random nature of defect (V_O) generation in oxide materials, and their percolation and rupture must be even more random, making their sufficient control highly challenging.[18-20] Such random behavior becomes even worse when the RS memory cells are integrated into the passive cross-bar array (CBA) architecture. In the pristine state or HRS of the CBA, the metal-insulator-metal structures of the ReRAM cell constitute a large capacitor structure (the line length in CBA is very high), whose stored charge bursts into the CF when any of the connected cells is electroformed. Depending on the resistance state of the cells within a CBA, different cells must be under different environments during electroforming (EF) or set (switching from HRS to LRS) and reset (switching

from LRS to HRS) switching. This effect must be most influential to the device uniformity at the EF step because the EF step establishes the CF size and shape in each cell, which subsequently governs the switching performances.[1,21] In this regard, the EF-free ReRAM is very desirable for improving the uniformity of the ReRAM performance. The EF-free property also has a critical influence on the retention performance, as shown in this work.

As all these reliability and uniformity issues are closely related with the defect generation and their percolation path formation, one of the best ways to mitigate the problems is to use a smaller volume of oxide materials that must have a lower chance of involving large variations in V_O behaviors. Smaller dimension means a smaller lateral size of the memory cell as well as a low thickness of the switching oxide layer. Indeed, the authors reported the greatly enhanced switching uniformity and endurance performance from the ReRAM cell with a 28 nm lateral dimension and extremely thin switching oxides - Ta_2O_5 or HfO_2 (0.5-2 nm).[22-24] Interestingly enough, in both device types with Ta_2O_5 or HfO_2 as the switching layers (Ta as the V_O-source electrode layer and TiN as the inert counter electrode), the thinnest oxide film devices showed the best performance, which is partly related with the EF-free behavior of such thinnest film devices.[22-24] It was concluded that the devices have hourglass-shaped CFs; as such, the weakest portion near the middle region of the film, albeit its low thickness, is responsible for the RS performance. In fact, the set and reset processes under different bias polarities (a positive bias to the Ta electrode sets

the cell, and a negative bias to the Ta electrode resets the cell) were understood from the relative movement of the two portions of the CF (upper and lower portions). During the set process, the growth speed of the upper portion near the Ta electrode was faster than the retracting speed of the lower portion near the TiN; as such, they are connected. In contrast, the reset process was accomplished by the faster retracting speed of the upper portion than the growing speed of the lower portion, which eventually disconnects the two portions.[23,24] As these set and reset processes involve the complicated motions of the two portions of the CF, it was understandable that the switching uniformity and reliability could hardly be achieved. The EF-free behavior and improved uniformity and endurance of the thinnest (<1nm) film devices were understood from the more conical-shaped CF, where the above-mentioned competition between the two portions are not involved. A simple extension and retraction of a V_O-rich portion (CF) near the Ta electrode, which is already formed even at the pristine state by the chemical reduction effect of the Ta electrode, can induce the reliable RS performances.[23]

Low thickness is also beneficial considering the expectation that the most feasible application of the high-density ReRAM CBA is as the successor to the vertical NAND flash. In this case, the extremely narrow hole must be filled with an RS/selector layer and the top electrode.[25-28] When the hole diameter is ~10 nm or less, the physical space allowable for the RS layer is only ~1 nm. Therefore, the evaluation of other performances, such as retention, as in this

work, of such extremely thin film device is critically important.[29] As shown in this work, however, the retention performance is generally unsatisfactory, and an even worse problem is the highly different trend of retention failure mode from the conventional cases[10,11] (i.e., both LRS and HRS showed a sudden resistance drop at a certain time during the retention test). Therefore, this work was conducted to elucidate the mechanism for such unusual failure mechanism and to suggest a possible solution to the problem. In this work, a 1-nm-thick HfO_2 thin film grown via thermal atomic layer deposition (ALD) was employed as the RS layer, and the test device structure was integrated on a 300-mm-diameter wafer using the state-of-the-art fabrication technology in a commercial research facility in SK Hynix.

2.2. Experimental

The details of the test device fabrication process can be found elsewhere. Only a summary is provided in this section. After patterning a W layer for the word lines, the SiO_2 layer was deposited via chemical vapor deposition (CVD). Then a contact hole with a 20 nm diameter to the W word line was made within the CVD SiO_2, and was filled with the TiN layer, which constituted the bottom electrode (BE) of the memory cell. After the chemical mechanical polishing of the TiN layer to isolate the contacts, a HfO_2 layer with a 1 nm thickness was deposited via ALD, followed by the sequential formation of a 10-nm-thick Ta layer, which worked as a V_O-source layer and an additional 10-nm-thick TiN layer deposited through reactive sputtering. The top Ta/TiN layer constitutes the top electrode (TE). The TiN/Ta/HfO_2/TiN stack layers were dry-etched with a 28 nm cell diameter. The fabricated structure was passivated with a 7-nm-thick CVD Si_3N_4 spacer, and the SiO_2 interlayer dielectric layer was deposited. TE contact was achieved via the W bit line, which ran in an orthogonal direction to the word line direction. Al pads were used to contact the bit and word lines.

Direct current (DC) voltage sweep was performed using a Hewlett Packard 4155B semiconductor parameter analyzer with the TE (bit line) biased and the BE (word line) grounded. The retention measurements were performed under constant voltage stress mode (CVS mode, with a ±0.2 V read voltage), which continuously applies constant read voltage stress to the device, and under

the pulse mode (non-CVS mode, with a ±0.2 V read pulse voltage), which reads the device resistance state at specific time intervals with the read pulse voltage. Before the retention measurement, the “EF,” “set,” and “reset” processes of the pristine devices proceeded using the DC double-sweep mode.

2.3. Results and Discussions

Figure 2-1(a) shows the typical switching current-voltage (I-V) curve of the 1-nm-thick HfO_2-ReRAM device under the conditions of compliance current (I_{CC}) 300μA through the DC measurement mode. The EF, 1st reset, and 1st set operation results (blue symbol for EF, black symbol for 1st reset, and red symbol for 1st set) are shown in the figure. As can be seen in Figure 2-1 (a), the pristine device showed high resistance, with an EF voltage of ~0.92 V (the tests with more than 20 cells showed an average EF voltage of 0.92±0.04 V), which is similar to the set voltage of ~0.78 V (the tests with more than 20 cells showed an average set voltage of 0.78±0.02 V). This finding means that this device showed an EF-free performance. However, for the sake of convenience, the first sweep into the positive bias direction was referred as the EF in this paper. The EF and set processes occur in the positive bias direction, whereas the reset process occurs at the negative bias direction, which is consistent with the previous report.[23] The positive bias voltage drives the V_O's, which were already formed near the Ta TE interface in the pristine state, towards the TiN BE, making the CF connected. The negative bias drives back a certain portion of the V_O's within the connected CF towards the Ta TE direction. What really occurs, however, is much more complicated than this simple RS picture, which is the reason behind the unusual retention performance, as shown below. Another interesting and critical finding is that the current in the reset state is lower than that in the pristine state, as can be seen in the comparison of the blue

and red curves in Figure 2-1 (a), which provides a critical clue to understanding the unusual retention properties in this work. Figure 2-1 (b) shows a double logarithm plot of the I-V curves in the negative-voltage region of Figure 2-1 (a) after the EF, meaning that the sample is in LRS (upper portion), and after the reset (lower portion, HRS), with the maximum reset voltage of -1.2 V. The LRS of the device shows linearity in the I-V relationship, and the slope of the plot is ~1, indicating that Ohmic conduction through the CF is dominant. For the HRS of the device, Ohmic conduction was observed at a lower voltage, but the slope increased to ~2, indicating that the space-charge-limited conduction (SCLC) through the disconnected portion of the CF predominates at a higher-voltage region. These conduction behaviors of the LRS and HRS are also consistent with those in the previous report.[23,24]

Figure 2-1 (c) shows the results of the retention measurement of the device with LRS after the "EF-reset-set" process (blue data) and the device with HRS after the "EF-reset" process (red data), with an I_{CC}=300μA condition. Retention measurements of LRS and HRS were carried out in CVS mode, where +0.2 and -0.2 V were applied to the LRS and HRS devices, respectively, to help improve their retention performance. For better understanding, the read voltage application schemes are shown in the inset of Figure 2-1 (c). Despite these favorable CVS conditions, the devices retained their HRS and LRS up to only ~10^3 and ~10^4 sec, respectively, and they showed a high leakage current after the retention failure. While the retention failure behavior of the HRS (i.e.,

sudden current increase) is consistent with other reports,[11-13] that of the LRS shows an opposite trend. Similar trends have been confirmed by testing more than 20 devices, and the average retention times of HRS and LRS were only ~10^3 and ~10^4 sec, respectively, at room temperature, which are very insufficient for this memory to be regarded as a suitable non-volatile memory.

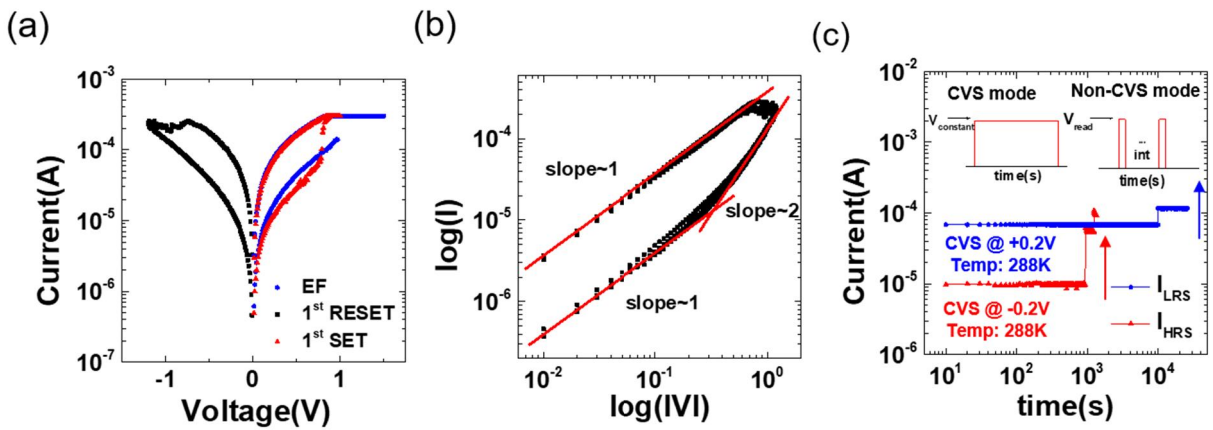


Figure 2-1. (a) I-V curve of the 0.9-nm-thick HfO_2 ReRAM device under the condition of compliance current (I_{CC}) 300**μA** through direct current (DC) measurement mode. (b) Double logarithm plot of I-V curves in the negative-voltage region after EF (c) Results of the retention measurement of the device with LRS after the "EF-reset-set" process, and the device with HRS after the "EF-reset" process with an I_{CC}=300**μA** condition

To examine the mechanisms of such unusual and unsatisfactory retention, more systematic tests were performed, as shown in Figure 2-2. Here, four different device states (five-cell per each state) were prepared for the retention tests under the CVS and non-CVS modes, meaning that a total of eight different conditions (total of forty-cell) were tested. The four different states were EF-only, EF-reset-set, EF-reset, and reset-only under the CVS and non-CVS modes, respectively. Here, the reset-only device corresponds to the device state after the first I-V sweep down to -1.2 V without EF. As can be conjectured from Figure 2-1(a), this reset-only operation further decreased the current of the HRS in the positive-bias-voltage region (see Figure 2-2 (a)). This means that the factors that contributed to the leakage current of the pristine state, which must have diffused V_O from the Ta TE, were partly removed during this first reset operation. The results shown in Figure 2-1 (a) and 2-2 (a) indicate that the device under HRS is more insulating than the pristine state, which is normally not the case in other oxide-based ReRAMs, which have a much thicker switching RS layer. This finding provided the authors with a critical clue to understanding the retention failure mechanism in this device, as will be discussed later in this paper.

Among the four configurations of the test device, the first two correspond to LRS, and the last two correspond to HRS. Among them, the EF-only configuration did not undergo the reset operation, whereas the other three configurations underwent the reset process. As shown in Figure 2-2, the EF-

only device did not show retention failure, but all the other devices showed clear retention failure behavior under both CVS and non-CVS conditions, suggesting that the reset operation induced a certain common reason for the retention failure. Figure 2-2 (a) and (b) show the retention test results under the CVS and non-CVS conditions, respectively, where the bias direction was chosen to enhance the retention performance (i.e., +0.2 V for LRS and -0.2 V for HRS). Although the CVS slightly improved the retention characteristics, as intended, insufficient retention performance was confirmed for the three reset-involved devices (EF-reset-set, EF-reset, and reset-only), whereas the EF-only sample did not show retention failure up to $3x10^4$ sec. $3x10^4$ sec is not a sufficiently long time to confirm the device reliability in the mass-production level, but it is enough for the purposes of this work. As discussed above, the reset-only sample showed the lowest current and retention failure times of $\sim10^4$ sec for the CVS condition and $\sim5x10^3$ sec for the non-CVS condition, which is longer than those of the EF-reset devices by approximately one order of magnitude. This finding implies that what occurred during the EF (typically remaining CF portion) in the EF-reset device also contributed to the retention failure.

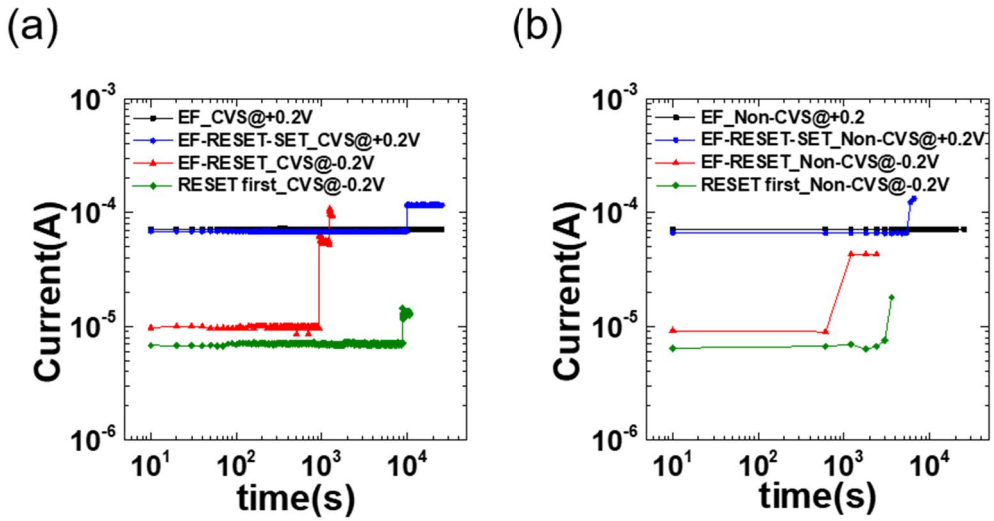


Figure 2-2. (a) Results of the retention measurement of the device with EF-only, EF-reset-set, EF-reset, and reset-only under the CVS condition and non-CVS condition in (b), respectively, where the bias direction was chosen to enhance the retention performance (i.e., +0.2 V for LRS and -0.2 V for HRS)

Next, the conductance-voltage (G-V) plots are shown in Figure 2-3 for the elucidation of the current conduction path for the retention-failed devices. In the authors' previous works on similar devices, it was confirmed that the current flow along the CF in these nanoscale devices is made through quantum point contact (QPC) behavior, where the G of a single QPC is 2 e^2/h (G_0=7.748 x 10^{-5} S) (e and h are the elementary charges and Planck constant, respectively).[24] Figure 2-3 (a) shows the typical G-V plots (three G-V scans are overlapped) of the LRS cell before retention failure occurs (EF-reset-set device). Due to the complicated contact nature of the CF and electrode or within the CF, half- or even quarter-integer G_0 values of CF have been observed,[24] and this was also the case for V < ~0.2 V (G ~5.5 G_0, not shown here). It has been well understood that the most critical feature of QPC is the independence of G on the applied voltage, which was demonstrated only in the low-voltage region in this device. At higher voltages (> ~0.2 V), G increases almost linearly with V, and this abnormal behavior has been identified as a proof of the leakage current flow through the non-CF region within the cell, whose conduction is mostly governed by the SCLC mechanism.[24] Detailed discussions of this interpretation can be found elsewhere,[24] and it is sufficient to remark that the invariant G with V indicates the current conduction through CF, and that increasing G with V causes leakage current through the non-CF region in this case. Figure 2-3 (b) is provided to elucidate this circumstance; in the low-V region, the current flows

mostly via the CF, but in the high-V region, the current flow through the non-CF region dominates.

Figure 2-3 (c) shows the G-V plots or normal cells (before retention failure) of HRS and LRS (black curves at the lowest portion). The data were collected in the negative-voltage region, and as such, the x-axis of the graph corresponds to the absolute value of the voltage. HRS and LRS show ~0.5×10^{-4} S and ~4.0×10^{-4} S up to 0.2 V, which slightly increased to ~0.8×10^{-4} S and ~4.3×10^{-4} S at 0.7 V, respectively, suggesting that the current flow was accomplished through the remaining weak CF in HRS and well-established CF in LRS. The retention-failed devices, however, demonstrated disparate behaviors, as shown by the curves indicated by "case 1" and "case 2" in the figure, which were achieved from the EF-reset device. When the device showed retention failure (i.e., the device current suddenly increased from HRS), it could not be returned to HRS (set-stuck), which is very detrimental to the CBA operation. Case 1 shows the slight recovery of the insulating properties by the repeated reset I-V sweep, as indicated more clearly in Figure 2-3(d), but it never went back to the genuine HRS or pristine state even after the repeated reset I-V sweeps. The most characteristic feature of case 1 is that the device did not show a constant G value across the entire voltage region, suggesting that the non-CF region dominated the current conduction in this case.

Case 2 corresponds to an even worse case; here, the repeated reset sweep did not change the too conductive state at all. As shown by the purple curve in the uppermost portion of Figure 2-3 (d), the conductance slightly decreased with the increasing absolute V, which could be induced by the thermal scattering of the carriers through the highly conducting metallic CF formed in this case. This means that the almost entire memory cell region was completely filled with an overly high density of V_O, which cannot be recovered to HRS.

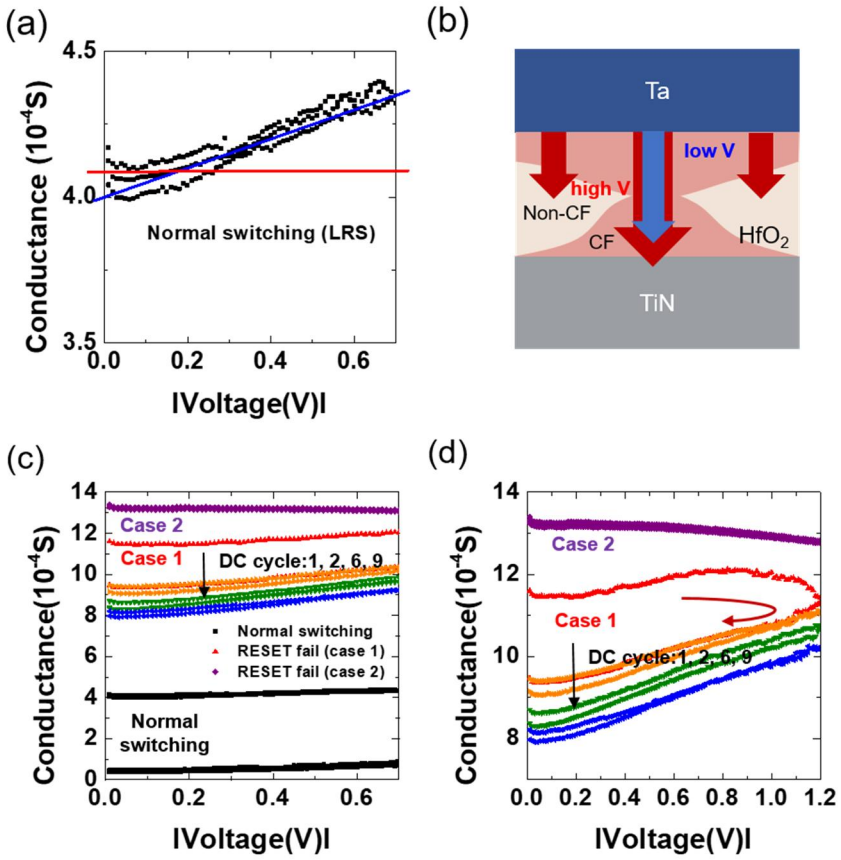


Figure 2-3. (a) Typical conductance-voltage (G-V) plots of the LRS device before the occurrence of retention failure. (b) Schematic elucidating the current conduction path in the LRS device; in the low-V region, the current flows mostly via the CF, but in the high-V region, the current flow through the non-CF region dominates. G-V plots showing the conductance-voltage relation of the normal device and the retention-failed devices in the negative-voltage region during a 10 DC cycle. (c) G-V plots of two cases of the retention-failed device: cases 1 and 2, respectively

From these findings, the following retention failure mechanism can be suggested. Figure 2-4 (a) shows the schematic cross-section of the device in the pristine state. As discussed previously, the Ta TE played the role of a fluent V_O supplier to the thin HfO_2 switching layer, and half of the 1-nm-thick HfO_2 film was assumed to be already filled with V_O's in this diagram. It was also elucidated that the ionization rate of the V_O in the RS oxide determined the EF when the RS oxide was Ta_2O_5,[22] which must also be the case in this HfO_2 cell. In this case, the current flow through the lower portion of the V_O-free region constitutes the leakage current under the bias application. Figure 2-4 (b) shows the schematic cross-section of the device after the EF. Here, an integral portion of the V_O's was ionized and migrated towards the TiN BE, eventually making the connected CF either conical- or hourglass-shaped. Here, the forefront of the original V_O-enriched region of the pristine cell outside the CF could slightly move towards the TiN electrode. This structure can flow current fluently through the formed CF, making the cell remain in LRS. When reset I-V sweep is performed, the CF will be ruptured, but a small portion of it will remain near the BE, which may act as the seed for the CF regrowth during the subsequent set. The most notable assumption that could be made, however, is the retraction of the forefront of the V_O-enriched region behind the original location at the pristine state, as shown in Figure 2-4 (c). As the original location of the forefront (or the boundary between the V_O-rich and V_O-free regions) must be governed by the thermodynamic equilibrium of the memory cell when it was

fabricated, its location must eventually be regained when the reset bias voltage was removed. Figure 2-4 (d) shows this circumstance. Due to the moving back of the forefront towards the TiN BE, the V_O-enriched region may have been connected to the remaining CF portion near the TiN BE, which caused the reset failure (retention failure). The authors have also reported that the repetition of the switching process inevitably increases the overall V_O concentration within the memory cell due to the involvement of the lateral diffusion of V_O, stimulated by the thermal energy related with the Joule heating.[23,24] Therefore, the reconnected CF can be even more conductive than that of the EF state, which can explain the even higher current of the reset-failed EF-reset device shown in Figure 2-1 (c) and 2-2 (a). However, in the case of an EF-only device which is without reset process in Figure 2-4 (b), there is not a retraction of the forefront of the Vo-enrich region behind the original location at the pristine state. Therefore there is not moving back to the forefront towards the TiN BE which caused the retention failure during retention times, as shown in Figure 2-2 (a) and (b).

A similar idea can be applied to the reset-only device. Figure 2-4 (e) shows the schematic cross-section of the reset-only device immediately after the reset I-V sweep. The reset voltage moves the forefront towards the Ta TE, and as such, the thickness of the V_O-free region increases, which induces an even lower leakage current than that in the pristine device. A similar effect was observed for the EF-reset device. When the reset-only device was retained

under the retention test conditions, the forefront moved back to its original stable position. In the meantime, there could be some V_O generation near the TiN BE interface because TiN is not perfectly immune to oxidation, and such minute amount of V_O can induce small nuclei of CF during the first reset I-V sweep or the retention test (especially with the CVS condition). When the moved-back forefront touches these nuclei of the CF from the TiN BE (Figure 2-4 (f)), it will set the device weakly, which is observed in Figure 2-2 (a) and (b). The even higher current after the retention failure of the EF-reset-set device can be understood similarly, as shown in Figure 2-4 (g). In this case, the already-connected region between the upper and lower portions of the CF during the set I-V sweep could be further strengthened by the forwardly moving forefront during the retention time. In this case, the forefront may be retracted to the position near the Ta TE after the reset I-V. This retracted forefront, however, may not be moved back to the original position during the subsequent set I-V sweep because most of the V_O migration is concentrated within the recovering CF region. With the help of the lateral diffusion of V_O's during the I-V sweeps, and a much longer retention test time, the forefront that moved back to the original position may induce an even higher current than that in the EF or just-set state, which was experimentally observed in Figure 2-2 (a) and (b).

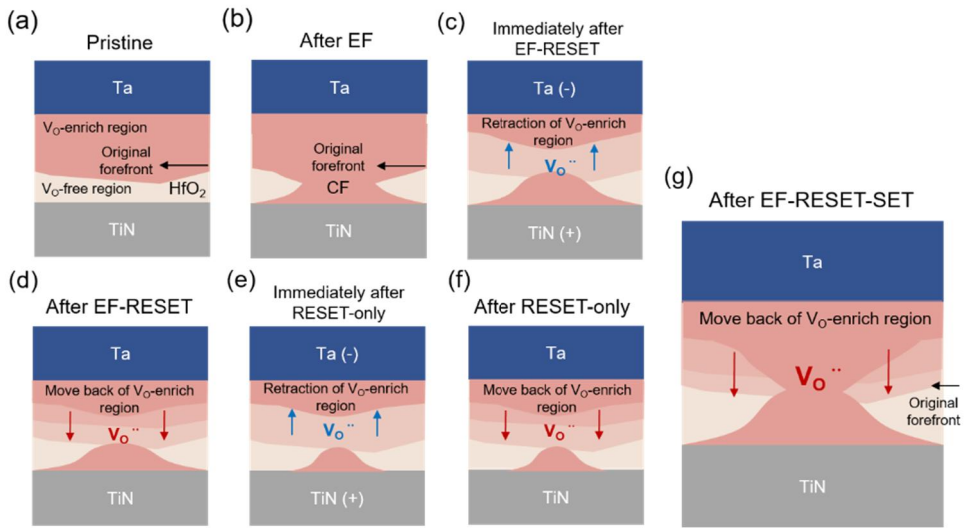


Figure 2-4. (a) Schematic cross-section of the pristine device, (b) the device after the EF, (c) the device with the EF-reset immediately after the reset I-V sweep, (d) the device after the EF-reset when the reset bias is removed, (e) the reset-only device immediately after the reset I-V sweep, (f) the reset-only device when the reset bias is removed, and (g) the device after the EF-reset-set process

Finally, the activation energy of the retention failure of the LRS was estimated by measuring the retention failure time of the EF-reset-set device (LRS) as a function of temperature (288-348 K) under the CVS mode (+0.2 V). The results are plotted according to the Arrhenius format in Figure 2-5. As expected, retention failure occurs at an earlier time as the temperature increases, suggesting that the movement of the forefront towards the TiN BE direction is thermally activated. From the slope of the best linear fit of the data, 0.152 eV activation energy was estimated. This value is similar to the value achieved as the activation energy of EF in Ta_2O_5 and HfO_2, which corresponds to the ionization energy of V_O in these oxides.[5,6,22] Therefore, the thermal de-trapping of the trapped electrons at the V_O centers is the rate-determining step of retention failure.

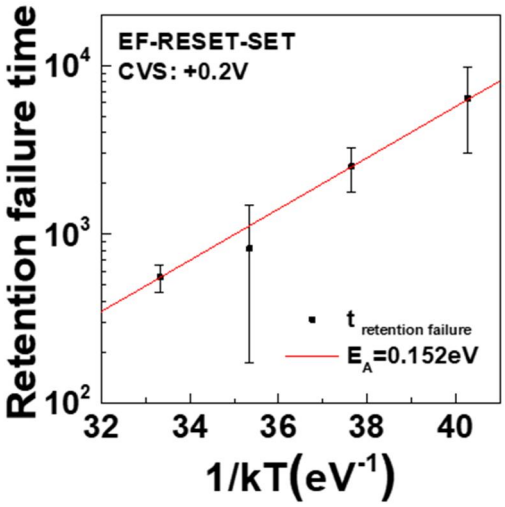


Figure 2-5. Arrhenius plot of the retention failure time of the device after the EF-reset-set process as a function of temperature (288-348K) under the CVS mode (+0.2 V)

From the discussions above, it can be understood that the enrichment of V_O's within the switching oxide layer, either during the switching I-V measurements or the retention test period, is the major reason for retention failure. If the total V_O concentration is kept invariant and is confined within the CF region, such reliability issue may disappear. Recently, the authors demonstrated that adopting RuO_2 as the BE instead of TiN as the V_O sink layer greatly improved the endurance and switching uniformity (both resistance values and switching voltages).[30] This is due to the removal of the excessive V_O included during the repeated switching through the adoption of RuO_2. Therefore, it can be anticipated that adopting RuO_2 will also improve the retention performance as it will remove the excessive V_O included during the retention test period, whose results will be reported separately.

2.4. Conclusion

The retention behaviors of a HfO_2 resistance random access memory device with an ultra-thin (1nm) HfO_2 resistance switching layer were investigated. Unlike the reported retention failure phenomenon, in the 1-nm-thick HfO_2 ReRAM device, both the low-resistance-state and high-resistance-state currents increased at a certain time, which induced retention failure. The retention tests in both the constant voltage stress and non- constant voltage stress modes confirmed that the reset process is the critical step that causes the retention failure of the device. Through the analysis of the conductance-voltage relationship, it was confirmed that the increase of the oxygen vacancy concentration in the RS oxide layer during the retention test period induces the retention failure. The pristine device has an integral portion of the V_O-enriched region near the Ta electrode, whose border with the V_O-free region is recessed from the original position towards the Ta top electrode during the reset process. This recessed region recovers the original location during the retention test period as it is thermodynamically more stable, which can induce the reconnection of the broken conducting filament. This is further facilitated by the increased V_O concentration within the CF and non-electroformed regions in the memory cell. Even at the LRS, which is achieved by the sequential operation of the electroforming, reset, and set processes, the cell current becomes higher after the retention failure due to the strengthening of the CF by the moving back of the border to the original position. The EF-only device did

not show a sudden increase in current. As the main reason for the involvement of such unwanted effect is the overall increase in V_O concentration within the memory cell, the adoption of a V_O sink layer such as RuO_2 as the counter electrode of the V_O-source Ta electrode may improve the retention performance.

2.5. References

(1) Kim, K. M.; Jeong, D. S.; Hwang, C. S. Nanofilamentary resistive switching in binary oxide system; a review on the present status and outlook. *Nanotechnol.* **2011,** *22*, No. 254002.

(2) Waser, R.; Dittmann, R.; Staikov, G.; Szot, K. Redox-Based Resistive Switching Memories -Nanoionic Mechanisms, Prospects, and Challenges. *Adv. Mater.* **2009,** *21*, 2632-2663.

(3) Yang, J. J.; Zhang, M.-X.; Strachen, J. P.; Miao, F.; Pickett, M.; Kelley, R. D.; Medeiros-Ribeiro, G.; Williams, R. S. High switching endurance in TaO_x memristive devices. *Appl. Phys. Lett.* **2010,** *97*, No. 232102.

(4) Miao, F.; Strachen, J. P.; Yang, J. J.; Zhang, M.-X.; Goldfarb, I.; Torrezan, A. C.; Eschbach, P.; Kelley, R. D.; Medeiros-Ribeiro, G.; Williams, R. S. Anatomy of a Nanoscale Conduction Channel Reveals the Mechanism of a High-Performance Memristor. *Adv. Mater.* **2011,** *23*, 5633-5640.

(5) Park, G.-S.; Kim, Y. B.; Park, S. Y.; Li, X. S.; Heo, S.; Lee, M.-J.; Chang, M.; Kwon, J. H.; Kim, M.; Chung, U.-I.; Dittmann, R.; Waser, R.; Kim, K. *In Situ* Observation of Filamentrary Conducting Channels in an Asymmetric Ta_2O_{5-X} / TaO_{2-X} Bilayer Structure. *Nat. Commun.* **2013,** *4*, No. 2382.

(6) Yoon, J. H.; Song, S. J.; Yoo, I.-H.; Seok, J. Y.; Yoon, K. J.; Kwon, D. E.; Park, T. H.; Hwang. C. S. Highly Uniform, Electroforming-Free, and Self-Rectifying Resistive Memory in the Pt/Ta_2O_5/HfO_{2-X}/TiN Structure. *Adv. Funct. Mater.* **2014,** *24*, 5086-5095.

(7) Lee, H. T.; Chen, P. S.; Wu, T. Y.; Chen, Y. S.; Wang, C. C.; Tzeng, P. J.; Lin, C. H.; Chen, F.; Lien, C. H.; Tsai, M, -J. Low Power and High Speed Bipolar Switching with a Thin Reactive Ti Buffer Layer in Robust HfO_2 Based RRAM.

IEEE International Electron Devices Meeting. Technical Digest, San Francisco, CA, USA,15-17 December 2008.

(8) Lee, B.; Wong, H. -S. P. NiO Resistance Change Memory with a Novel Structure for 3D integration and Improved Confinement of Conduction Path. *IEEE Symp. on VLSI Technology,* Honolulu, Hawaii, USA, June, 2009.

(9) Chen, Y. S.; Lee, H. Y.; Chen, P. S.; Gu, P. Y.;Chen, C. W.; Lin, W. P.; Liu, W. H.; Hsu, Y. Y.; Sheu, S. S.; Chiang, P. C.; Chen, W. S.; Chen, F. T.; Lien, C. H.; Tsai, M. -J. Highly Scalable Hafnium Oxide Memory with Improvements of Resistive Distrubution and Read Disturb Immunity. *IEEE International Electron Devices Meeting. Technical Digest*, Baltimore, MD, USA, 7-9 December 2009.

(10) Ninomiya, T.; Muraoka, S.; Wei, Z.; Yasuhara, R.; Katayama, K.; Takagi, T. Improvement of Data Retention During Long-Term Use by Suppressing Conductive Filament Expansion in TaO_x Bipolar-ReRAM. *IEEE Electron Device Lett*. **2013,** *34*, 762-764.

(11) Gao, B.; Zhang, H.; Chen, B.; Liu, L.; Liu, X.; Han, R.; Kang, J.; Fang, Z.; Yu, H.; Yu, B.; Kwong, D. L. Modeling of Retention Failure Behavior in Bipolar Oxide-Based Resistive Switching Memory. *IEEE Electron Device Lett*. **2011,** *32*, 276-278.

(12) Wei, Z.; Takagi, T.; Kanazawa, Y.; Katoh, Y.; Ninomiya, T.; Kawai, K.; Muraoka, S.; Mitani, S.; Katayama, K.; Fujii, S.; Miyanaga, R.; Kawashima, Y.; Mikawa, T.; Shimakawa, K.; Aono, K. Retention Model for High-density ReRAM. *IEEE Int. Memory Workshop,* Milan, Italy, May, 2012.

(13) Wei, Z.; Takagi, T.; Kanazawa, Y.; Katoh, Y.; Ninomiya, T.; Kawai, K.; Muraoka, S.; Mitani, S.; Katayama, K.; Fujii, S.; Miyanaga, R.; Kawashima, Y.; Mikawa, T.; Shimakawa, K.; Aono, K. Demonstraion of High-density

ReRAM Ensuring 10-year Retention at 85°C Based on a Newly Developed Reliability Model. *IEEE Int. Electron Devices Meeting (IEDM),* Washington, DC, USA, December, 2011.

(14) Chen, Y. Y.; Goux, L.; Clima, S.; Govoreanu, B.; Degraeve, R.; Kar, G. S.; Fantini, A.; Groeseneken, G.; Wouters, D. J.; Jurczak, M. Endurance/Retention Trade-off on HfO_2/Metal Cap 1T1R Bipolar RRAM. *IEEE Trans. Electron Devices* **2013,** *60*, 1114-1121.

(15) Chen, Y. Y.; Degraeve, R.; Govoreanu, B.; Clima, S.; Goux, L.; Fantini, A.; Kar, G. S.; Wouters, D. J.; Groeseneken, G.; Jurczak, M. Postcycling LRS Retention Analysis in HfO_2/Hf RRAM 1T1R Device. *IEEE Electron Device Lett*. **2013,** *34,* 626-628.

(16) Koo, Y.; Ambrogio, S.; Woo, J.; Song, J.; Ielmini, D.; Hwang, H. Acceletrated Retention Test Method by Controlling Ion Migration Barrier of Resistive Random Access Memory. *IEEE Electron Device Lett*. **2015,** *36*, 238-240.

(17) Chen, Y. Y.; Komura, M.; Degraeve, R.; Govoreanu, B.; Goux, l.; Fantini, A.; Raghavan, N.; Clima, S.; Zhang, L.; Belmonte, A.; Redolfi, A.; Kar, G. S.; Groeseneken, G.; Wouters, D. J.; Jurczak, M. Improvement of data retention in HfO_2/Hf 1T1R RRAM cell under low operating current. . *IEEE Int. Electron Devices Meeting (IEDM),* Washington, DC, USA, December, 2013.

(18) Kwon, D.-H.; Kim, K.; Jang, J.; Jeon, J.; Lee, M.; Kim, G.; Li, X.-S.; Park, G.-S.; Lee, B.; Han, S.; Kim, M.; Hwang, C. S. Atomic Structure of Conducting Nanofilaments in TiO_2 Resistive Switching Memory. *Nat. Nanotechnol*. **2010,** *5*, 148-153.

(19) Choi, B. J.; Jeong, D. S.; Kim, S. K.; Rohde, C.; Choi, S.; Oh, J. H.; Kim, H. J.; Hwang, C. S.; Szot, K.; Waser, R.; Reichenberg, B.; Tiedke, S.; Resistive Switching Mechanism of TiO_2 Thin Films Frown by Atomic-Layer Deposition.

J. Appl. Phys. **2005,** *98*, No. 033715.

(20) Park, G.-S.; Li, X.-S.; Kim, D.-C.; Jung, R.-J.; Lee, M.-J.; Seo, S. Observation of electric-field induced Ni filament channels in polycrystalline NiO_x film. *Appl. Phys. Lett*. **2007,** *97*, No. 222103.

(21) Kim, K. M.; Choi, B. J.; Hwang, C. S. Localized switching mechanism in resistive switching of atomic-layer-depostied TiO_2 thin films. *Appl. Phys. Lett.* **2007,** *90*, No. 242906.

(22) Park, T. H.; Song, S. J.; Kim, H. J.; Kim, S. G.; Chung, S.; Kim, B. Y.; Lee, K. J.; Kim, K. M.; Choi, B. J.; Hwang, C. S. Thickness-dependent electroforming behavior of ultra-thin Ta_2O_5 resistance switching layer. *Phys. status solidi-Rapid Res. Lett*. **2015,** *9*, 362-365.

(23) Park, T. H.; Song, S. J.; Kim, H. J.; Kim, S. G.; Chung, S.; Kim, B. Y.; Lee, K. J.; Kim, K. M.; Choi, B. J.; Hwang, C. S. Thickness effect of ultra-thin Ta_2O_5 resistance switching layer in 28 nm-diameter memory cell. *Sci. Rep*. **2015,** *5*, No. 15965.

(24) Park, T. H.; Kim, H. J.; Park, W. Y.; Kim, S. G.; Choi, B. J.; Hwang, C. S. Roles of conducting filament and non-filament regions in the Ta_2O_5 and HfO_2 resistive switching memory for switching reliability. *Nanoscale* **2017,** *9*, 6010-6019.

(25) Baek, I. G.; Park, C. J.; Ju, H.; Seong, D. J.; Ahn, H. S.; Kim, J. H.; Yang, M. K.; Song, S. H.; Kim, E. M.; Park, S. O.; Park, C. H.; Song, C. W.; Jeong, G. T.; Choi, S.; Kang, H. K.; Chung, C. Realization of Vertical Resistive Memory (VRRAM) using cost effective 3D Process. *IEEE Int. Electron Devices Meeting (IEDM),* Washington, DC, USA, December, 2011.

(26) Cha, E.; Woo, J.; Lee, D.; Lee, S.; Song, J.; Koo, Y.; Lee, J.; Park, C. G.; Yang,

M. Y.; Kamiya, K.; Shiraishi, K.; Magyari-Köpe, B.; Nishi, Y.; Hwang, H. Nanoscale (~10nm) 3D vertical ReRAM and NbO_2 threshold selector with TiN electrode. *IEEE Int. Electron Devices Meeting (IEDM),* Washington, DC, USA, December, 2013.

(27) Yoon, H. S.; Baek, I. G.; Zhao, H.; Sim, H.; Pakr, M. Y.; Lee, H.; Oh, G. H.; Shin, J. C.; Yeo, I. S.; Chung, U. I. Vertical Cross-point resistance Change Memory for Ultra-High Density Non-volatile Memory Applications. *IEEE Symp. on VLSI Technology,* Honolulu, Hawaii, USA, June, 2009.

(28) Woo, J.; Lee, D.; Cha, E.; Lee, S.; Park, S.; Hwang, H. Vertically Stacked ReRAM Composed of a Bidirectional Selector and CB-RAM for Cross-Point Array Applications. *IEEE Electron Device Lett.* **2013,** *34*, 1512-1514.

(29) Seok, J. Y.; Song, S. J.; Yoon, J. H.; Yoon, K. J.; Park, T. H.; Kwon, D. E.; Lim, H.; Kim, K. H., Jeong, D. S.; Hwang, C. S. A Review of Three-Dimensional Resistive Switching Cross-Bar Array Memories from the Integration and Materials Property Points of View. *Adv. Funct. Mater.* **2014,** *24*, 5316-5339.

(30) Park, T. H.; Kwon, Y. J.; Kim, H. J.; Woo, H. C.; Kim, G. S.; An, C. H.; Kim, Y.; Kwon, D. E.; Hwang, C. S. Balancing the Source and Sink of Oxygen Vacancies for the Resistive Switching Memory. *ACS Appl. Mater. Interfaces.* **2018,** *10*, 21445-21450.

3. Defect Engineered Electroforming-Free Analog HfO_x ReRAM and its Application to the Neural network

3.1. Introduction

Since the analog switching characteristics of a ReRAM were identified as mimicking the functions of a synapse, ReRAM-based neuromorphic computing technology utilizing the ReRAM as a synapse has been widely studied.[1–5] The ReRAM synapse can be integrated into a two-terminal metal-insulator-metal (MIM) structure, which is suitable as the memory element in a passive crossbar array (CBA). Since the CBA structure has the smallest feature size and the highest integration density, it can be a feasible building block for the ReRAM neural network. One of the challenges of the ReRAM synapse is its non-ideal analog characteristic and inherent resistance variability that originates from its stochastic resistance switching nature.[6–10] For example, for an ideal artificial neural network, it is desirable for a ReRAM to have a constant conductance change rate upon the application of a given voltage stimulus over the entire conductance range, which is termed ‘linearity’, and the same conductance change rate during potentiation and depression, which is termed ‘symmetry’. Potentiation and depression mean the increase and decrease in the electrical conductance, respectively, with the repeated electrical voltage pulse

application. These features can be obtained by measuring the long-term potentiation and depression (LTP and LTD) characteristics and plotting the conductance values as a function of the number of set (switching from the high resistance state (HRS) to low resistance state (LRS)) and reset (switching from the LRS to HRS) voltage pulses, respectively. If the LTP and LTD curves of a given ReRAM are linear and symmetric, it corresponds to an ideal synaptic device. However, due to the drift- and diffusion-based kinetics in the ReRAM switching phenomena, where the variation is usually faster at the beginning of the potentiation and depression processes, compared with that at the completion of the process, the synaptic performance of the ReRAMs is usually rather remote from the ideal behavior.[11–15] This has been especially the case where the resistance switching (RS) was mediated by the formation and rupture of conducting filaments (CF).[12–15] In particular, the initiation of the reset process is highly abrupt, compared with the set process. Therefore, there have been several suggestions to alleviate the issues related to such abrupt reset initiation. One of the common methods is to experimentally estimate the potentiation–depression curves, fit the data with the appropriate mathematical formula, and correct the non-linearity using an auxiliary circuit.[16, 17] However, this causes a bulky control circuit, so it is not an ideal method. Another method is to always take the reset state first, and gradually set the ReRAM cell during the training of the network. This method cannot be used for depression, and thus usually, two ReRAM cells are combined together, with one of them being used to

represent depression by converting the applied voltage polarity.[17–19] This also invoked problems of large cell areas and complicated control circuits. Another critical issue is the involvement of the random variation in the device characteristics between the cells and switching operations, which certainly impacts the performance of the network.[20, 21] Such variations can be quantified by adopting a coefficient of variation (CV) that defines the ratio of the standard deviation (σ) to the mean value (μ). Song et al. reported recently that CV of about ~2 % does not impact the system performance, demonstrating the defect-tolerant feature of the artificial neural network.[22] In addition to these synaptic performances, conventional memory performance indicators, such as the retention and endurance of the memory cell, are still the crucial factors for the ReRAM to have in the neural network.[23–29] Most of the MIM-structured ReRAMs are highly insulating at the as-fabricated state, which requires an electroforming (EF) step to operate them as a feasible memory or synapse. EF corresponds to a soft-breakdown of the insulating layer, which usually induces several CFs in the insulating matrix, such as HfO_2, as in this work. In insulating oxides, the CFs are usually composed of oxygen-deficient phases, such as Magnéli in TiO2,[30–35] or oxygen vacancy (V_O) clusters, as in HfO_2 and Ta_2O_5.[36–40] However, such EF process also induces several unwanted side effects, which largely deteriorate the ReRAM performances of uniformity, endurance, and retention. Also, from the driving circuit point of view, incorporating EF control circuit into the system is highly undesirable. EF of all the components in a

system using a test process before chip shipping is also very burdensome. Therefore, exploiting an EF-free ReRAM could be a feasible solution to the numerous problems mentioned above, and indeed there are several works where EF-free characteristics are reported.[41–46] However, in many such reports with the EF-free samples, the on-to-off current ratio was too small, and operation current levels are too high to be used for standard high-density CBA (memory) application. Fortunately, applications of such ReRAMs in the neural network require different characteristics, and thus the low on-to-off ratio and slightly high current level might not be a severe issue. As the EF process is related to the first generation of the CFs, ReRAMs that do not rely upon the distinct CF mechanism could be a feasible option for such purpose. Another crucial ingredient that might contribute to the improvement in device performance is the electrode. For many resistive switching random access memories (ReRAMs) using an oxide switching layer, the electrodes must play the role of oxygen reservoir or oxygen transport layer.[36–38, 47, 48] In several cases, an additional oxygen reservoir layer has been adopted, especially for the cases where the electrodes can hardly take the role, such as TiN.[49] While the standard memory applications can take the industry-standard test protocol, i.e., incremental step pulse programming, to achieve the desired (multiple) target resistance values, it can hardly be used for the neural network, especially when the system was intended to be used for applications requiring online learning or training-intensive tasks. Therefore, stable operation of the resistance

switching upon repeated pulse-switching, i.e., involving invariable R_{LRS}, R_{HRS}, V_{set}, and V_{reset}, which are the LRS and HRS resistance, and the set and reset voltages, respectively, is essential but has remained rather challenging. As the repeated operation of the resistance switching is usually accompanied by the gradual loss of oxygen from the limited memory cell volume, confirming the stability of the above-mentioned parameters is generally challenging. Recently, reports have observed that the adoption of the optimized Ta electrode, which is the source of V_O, and optimized RuO_2, which is the sink of excessive V_O, in the Ta/HfO_2/RuO_2 ReRAM cell can significantly contribute to ensuring stable device operation, compared with the conventional Ta/HfO_2/TiN ReRAM cell.[37, 38] In the conventional Ta/HfO_2/TiN ReRAM cell, the device becomes filled with excessive V_O's as the pulse-switching cycles proceed, inevitably increasing the V_{set}, and V_{reset}, which then induces device failure after only several hundreds of thousand cycles.[37, 38] In contrast, the optimized Ta/HfO_2/RuO_2 ReRAM cell could show almost no change in those critical operation parameters up to tens of million cycles, by taking away the excessive V_O's from the active volume of the memory cell via the high oxygen-supply characteristics of the RuO_2.[38] Therefore, this work adopted a similar Ta/HfO_2/RuO_2 ReRAM cell to improve the system performance of the fully connected neural network in identifying the black-and-white characters (MNIST data set). For such purpose, the previously optimized Ta top electrode (TE) and RuO_2 bottom electrode (BE) conditions were adopted. Also, the HfO_2 thickness was controlled to ~3.0 nm, which is just

thin enough to ensure the EF-free behavior, but still thick enough to maintain a useful on-to-off ratio. For comparison, a similar material stack, but with thicker HfO_2 film (~4.5 nm), was also fabricated, which obviously required the EF process to induce useful switching functionality. As a reference device, the conventional Ta/HfO_2/TiN ReRAM cell with a ~4.5-nm-thick HfO_2 film was also fabricated, and their device characteristics were compared. The test device size was (4 μm × 4 μm). Along with the EF free characteristic, the optimized Ta/3.0 nm–HfO_2/RuO_2 ReRAM showed improved retention and uniformity. Also, it showed improved analog switching behaviors and synaptic performances (improved linearity and symmetry factors). The chemical analysis of the film stack provided several clues to identifying the reasons for such improvements. Finally, its application to the neuromorphic neural network is examined by computer simulation using the experimentally estimated potentiation–depression curves. The use of such an improved synapse device improved MNIST dataset recognition.

3.2. Experimental

Cell Fabrication: The devices were fabricated with a crossbar structure with (4 – 10) μm line width. The device structure consisted of Pt (60 nm)/Ta (20 nm)/HfO_2/RuO_2 (20 nm)/Pt (60 nm), or Pt (60 nm)/Ta (20 nm)/HfO_2/TiN (20 nm)/Pt (60 nm). The Pt layer was added to lower the line resistance. The HfO_2 switching layer was deposited via plasma-enhanced atomic layer deposition (PEALD). The thickness of the HfO_2 layer was varied from (3.0 to 4.5) nm by controlling the number of PEALD cycle numbers. Because the growth per cycle of the HfO_2 film was dependent on the type of bottom electrode (Growth per cycle (GPC) behavior of the PEALD-processed HfO_2 layer depending on the substrates (Si, SiO_2, RuO_2, TiN) are shown in Figure 3-1 (b)), the number of PEALD cycles was carefully controlled based on the data shown in Figure 3-1(b). Tetrakis(ethylmethylamiono)-Hafnium, as the Hf source, was heated to 50 °C, and then supplied to the processing chamber by bubbling through 50 sccm Ar. O_2 plasma (100 W at a 50 sccm flow rate) was applied as an oxygen source. The optimized PEALD sequence was 1 s Hf-precursor pulse – 10 s Ar purge – 7 s O_2 plasma pulse – 10 s Ar purge. RuO_2 BE was deposited through O_2 reactive sputtering using a 3-inch diameter Ru target. The O_2 flow rate was 3.5 sccm, while the Ar flow rate was 30 sccm. The sputtering power was 60 W, and the working pressure was 1.5×10^{-2} torr. The TiN BE was deposited through N_2 reactive sputtering using a 3-inch diameter Ti target. The N_2 flow rate was 1.0 sccm, while the Ar flow rate was 20 sccm.

The sputtering power was 100 W, and the working pressure was 4.0×10^{-3} torr. For the Ta deposition using a 3-inch diameter Ta target, the Ar flow rate was 30 sccm, sputtering power was 100 W, and working pressure was 1.5×10^{-2} torr. Figure 3-1 shows the scanning electron microscope (SEM) top-view image of the fabricated device and the growth per cycle (GPC) behavior of the PEALD processed HfO_2 depending on the substrates (Si, Si/SiO_2, Si/RuO_2, and Si/TiN).

Characterization: The electrical properties were measured using a semiconductor parameter analyzer (Hewlett Packard, 4155B) in the direct sweep (DC) voltage sweep mode. The bottom Pt/RuO_2 (or Pt/TiN) electrode was grounded, while bias was applied to the top Ta/Pt electrode. For the alternating current (AC) measurement, a semiconductor parameter analyzer (Hewlett Packard, 4155B), a pulse generator (Agilent 81110A), and an oscilloscope (Tektronix, TDS 684C) were used. The X-ray photoelectron spectroscopy (XPS) data were acquired on an Axis Supra (Kratos, UK) equipment using a monochromatic Al Kα source. The depth-profile was performed in situ by Ar+ ion etching with an acceleration voltage of 5 kV in the XPS chamber. The binding energies were corrected relative to the C 1s signal at 284.5 eV.

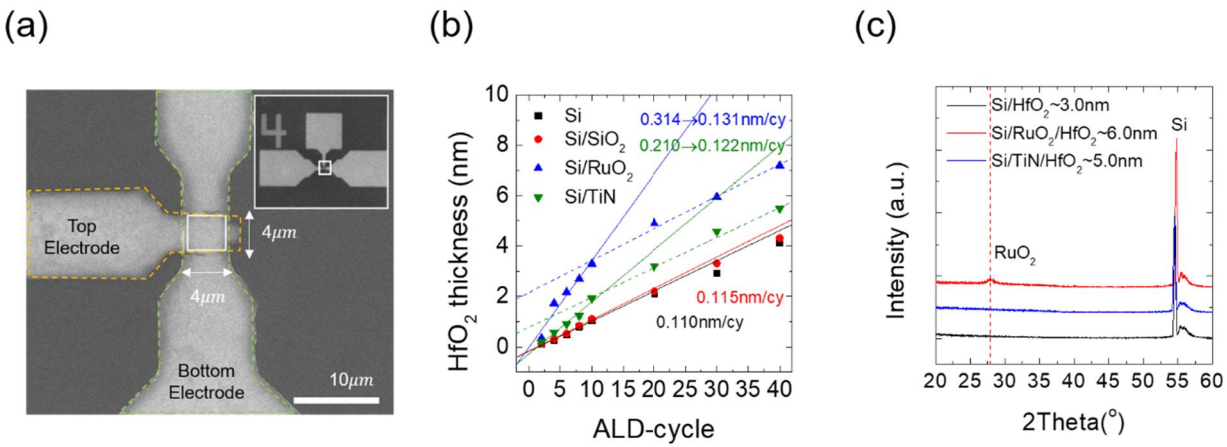


Figure 3-1. (a) Scanning electron microscope (SEM) top-view image of the fabricated device. (b) Growth per cycle (GPC) behavior of the PEALD processed HfO_2 depending on the substrate (Si, SiO_2, Si/TiN, and Si/RuO_2). (c) XRD measurement results of 30 ALD cycles deposited HfO_2 on Si, Si/RuO_2, and Si/TiN substrate

3.3. Results and Discussions

3. 3. 1. Basic switching characteristics

Three crossbar-type HfO_2 resistive switching devices, Ta/4.5 nm-thick-HfO_2/TiN (T-45), Ta/4.5 nm-thick-HfO_2/RuO_2 (R-45), and Ta/3.0 nm-thick-HfO_2/RuO_2 (R-30), were prepared. The HfO_2 switching layers were grown by a plasma-enhanced atomic layer deposition (PEALD), using the $Hf(N(CH_3)C_2H_5)_4$ and plasma-activated O_2 gas as the Hf-precursor and oxygen source, respectively. Figure 3-1 (b) shows the film thickness variation as a function of the PEALD cycle number on various substrates (Si, SiO_2, RuO_2, and TiN), which provided the basic data set to grow the target thickness of the HfO_2 layers in each device. Sputter-deposited Ta was used as the TE for all devices. The TiN and RuO_2 BE layers were grown by the reactive sputtering processes. The details for the fabrication process can be found in the experimental section. Figure 3-1 (a) shows the scanning electron microscope (SEM) top-view image of the fabricated device with 4 μm line width. Figures 3-2 (a–c) show the current–voltage (I–V) characteristics of the T-45, R-45, and R-30 devices, respectively, for the 100 set and reset switching cycles using a direct current (DC) double-sweep mode. Figure 3-2 insets show the schematics of the device structure. During the electrical measurement, the Ta TE was biased, and the TiN or RuO_2 BE was grounded. In each device, the voltage was swept 0 V → V_{set} (1.5 – 3.0) V → 0 V → V_{reset} (-1.3 V) → 0 V. Black and

red curves represent the EF cycles, and a subsequent set and reset switching cycle, respectively. Grey curves represent the $(20–80)^{th}$ set-reset switching cycles per 10 cycles, while the blue curve represents the 100^{th} set-reset switching behavior. During the set switching, the compliance current (I_{CC}) was set to 300 μA. This I_{CC} was the minimum value for guaranteeing a successful EF of the T-45 device; if the I_{CC} was lower than 300 μA, the EF was not achieved. In the T-45 device in Figure 3-2 (a), after the EF occurred at ~2.0 V, the device remained at the LRS during the subsequent sweep to ~-0.7 V, and the device turned into the HRS after the sweep down to -1.3 V. The comparison between the black curve and the other curves shows a peculiar property of the device immediately after the EF. Despite the I_{CC} being controlled as low as possible, the first LRS showed a relatively higher conductance state than the subsequent LRSs, which originates from the capacitive charge effect.[50, 51] Such excess EF behavior should be avoided to achieve longer retention and higher endurance, because it generates excess filaments, causing higher variation of the RS and faster device degradation. As the EF voltage is proportional to the film thickness, one of the most feasible methods to do this is to decrease the HfO_2 thickness.[41] However, the thinner HfO_2 film of (3.0 – 3.5) nm with TiN BE showed a high leakage current, making the EF improbable even at the maximum I_{CC} of 100 mA, which renders the RS improbable too. Such high leakage current originates from the low Schottky barrier at the HfO_2/TiN interface, and the insufficient insulating property of the HfO_2 containing a high

V_O concentration by the oxygen scavenging effect of the TiN BE. This infers that the V_O concentration control, as well as the thickness control, is crucial for achieving EF-free behavior. Therefore, the TiN BE was replaced with the RuO_2 BE, expecting reduced leakage current by its higher work function (5.2 eV vs. 4.5 eV of TiN) and less oxygen scavenging (or even oxygen providing) effect.[38] Figure 1(b) shows the RS characteristic of the R-45 device, where its EF voltage is almost identical to that in the T-45 device (~ 2.0 V). However, the R-45 showed a much higher insulating property than the T-45 device at the pristine state, which matches well with the idea that the HfO_2/RuO_2 interface forms a higher Schottky barrier, and the lower current will be achieved when the positive bias is applied to the Ta TE. Nonetheless, the EF of the R-45 device also induced too much conducting LRS of the device immediately after the EF, as can be seen from the unusually high current of the black curve in LRS, compared with the other curves. Interestingly, when the HfO_2 film becomes as thin as 3.0 nm, the R-30 device showed EF-free switching performance, as shown in Figure 3-2 (c). Moreover, the EF-free R-30 device showed improved switching uniformity, compared with the others. Figure 3-2 (d) shows the average resistance values of the first LRSs and HRSs (red curves in Figures 3-2 (a–c)) collected from 10 devices per type. Here, the R-45 and T-45 devices showed lower R_{LRS} with a higher variation than those of the R-30 device, although their HfO_2 film was thicker. Such variation was caused by 'over-forming' during the EF process.[50, 51] Once the ReRAM cell is over-formed, the

stochasticity of the RS increases, which causes a higher variation in the device uniformity. Figure 3-2 (e) shows the average resistance values of LRSs and HRSs over 100 cycles from one typical cell. Figures 3-3 (a–c) show changes in resistance of the T-45 (left panel), R-45 (middle panel), and R-30 (right panel) devices depending on the cycle number in DC operation from (1.5 to -1.3) V with I_{CC} 300 μA. This confirms that the cycle-to-cycle uniformity of the T-45 and R-45 devices is worse than that of the R-30 device. The inset shows the R_{LRS} variation, which shows the average resistance value was almost the same, but the variation was higher in the T-45 and R-45 devices, compared to the R-30 device. More importantly, the variation of the HRS and LRS values with the increasing number of switching cycles, shown in Figure 3-3, indicates that the overall defect concentration in R-30 remains invariable, whereas that of the other two devices increases (T-45) or fluctuates (R-45). Figure 3-2 (f) shows the V_{set} variations of the devices. Interestingly, unlike the resistance variation of the T-45 and R-45 devices larger than the R-30 device, the V_{set} variation shows insignificant difference between the T-45, R-45, and R-30 devices, which suggests that the resistance variation did not originate from the fluctuation of the V_{set}, but from the inherently stochastic nature of the devices related to the initial vacancy configuration by the EF process. It was noteworthy that the pristine state of the R-30 device does not necessarily correspond to the HRS. When ~20 devices were tested, almost half of them showed an initial semi-LRS, meaning that the pristine resistance was in between the HRS and LRS.

Therefore, it can be inferred that such thin HfO_2 film already had (slightly) conducting path at the pristine state, which is responsible for the EF-free performance.

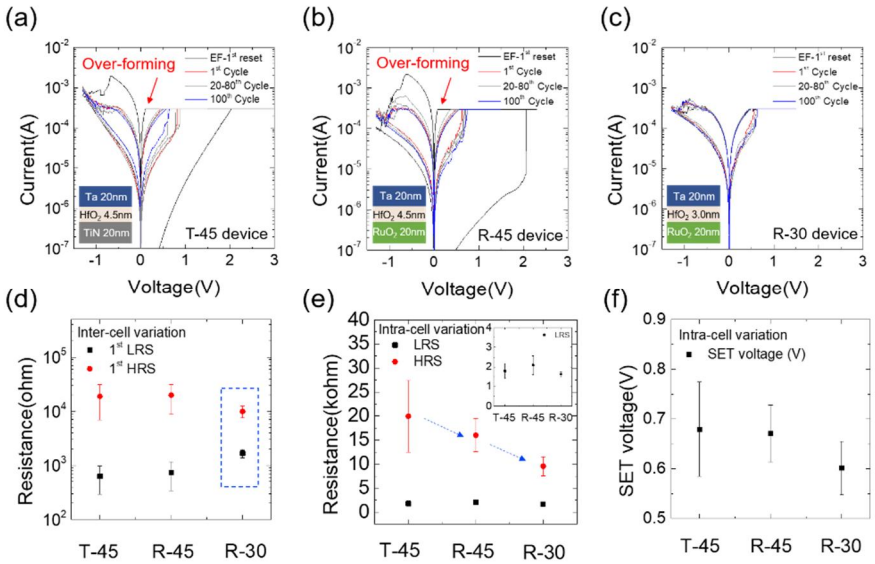


Figure 3-2. The resistive switching I–V curves of (a) T-45, (b) R-45, and (c) R-30 devices. The inset in the left bottom shows each device stack. The compliance current was set to 300 μA. (d) The first LRS and HRS resistance variations from 10 devices. (e) and (f) The resistances (in both LRS and HRS) and the set voltage switching variations from 100 cycles, respectively. The inset in (e) shows a magnified view of the LRS

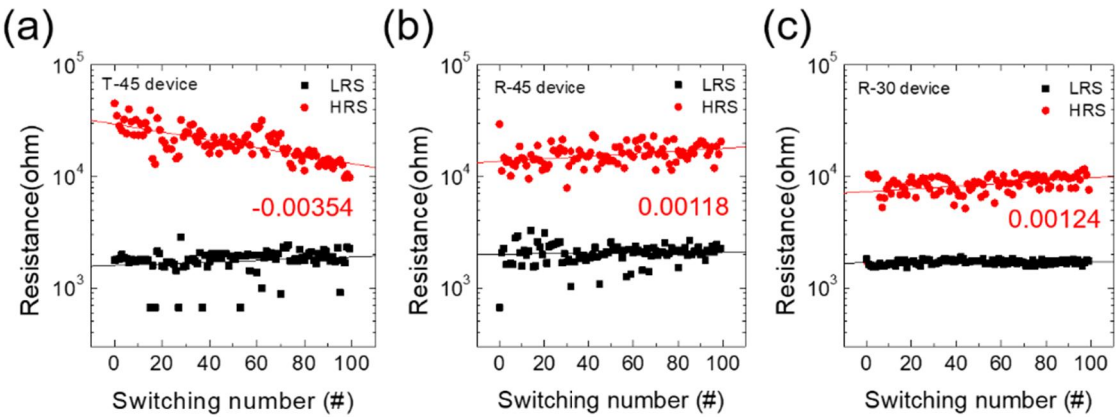


Figure 3-3. (a) Changes in resistance of the T-45 (left), R-45 (middle), and R-30 (right) devices depending on the cycle numbers in DC operation from (1.5 to -1.3) V with 300 μA. The drift of the resistance is indicated as slopes (resistance/cycle) in the upper plots.

3. 3. 2. Vacancy configuration analysis

The variations in the electrical properties of the devices with the TiN or RuO_2 BE could be identified by examining the HfO_2 film's chemical states by the X-ray photoelectron spectroscopy (XPS) analysis. Figure 3-4 shows the XPS depth profile data (high-resolution Hf 4f peak) and the fitting results of (6.0 and 5.0) nm thick HfO_2 films deposited on an (a – d) RuO_2 and (e – h) TiN substrates. (The XPS depth profile data and fitting results of O 1s, Ru 3d, and Ti 2p spectra during the depth profile of RuO_2/HfO_2 and TiN/HfO_2 samples are shown in Figure 3-5.) For the XPS analysis, the two ALD samples were prepared together, to minimize the experiment deviation during the analysis. For both samples, ten XPS spectra were collected, while keeping a constant etching rate. The labels from etching time (30 to 300) s correspond to the spectra from the surface of HfO_2 to the BE interface (HfO_2/RuO_2 or HfO_2/TiN). In the HfO_2/RuO_2 sample, the binding energy of Hf $4f_{7/2}$ peak shifted from 16.5 eV at the film surface to 16.8 eV near the BE interface (etching time increases from (30 to 300) s). [52-54] The binding energy of the Hf $4f_{7/2}$ peak of the stoichiometric HfO_2 is located at (16.7 – 16.8) eV,[55] suggesting that the HfO_2 film has stoichiometric composition near the RuO_2 interface. The Hf $4f_{7/2}$ peaks of the spectra after etching time of 30 s (near film surface), 150 s (at the middle portion), and 300 s (near RuO_2 interface) were deconvoluted as shown in Figures 3-4 (b–d). It can be understood that the peaks were composed of a single component, suggesting that the binding energy shift by ~0.3 eV between near

the interface and surface is due to the Fermi energy shift by the presence of charged defects, such as oxygen vacancy, near the surface. This was corroborated by a similar shift in the binding energy of the O1s XPS peak with the almost identical amount and direction (toward the lower binding energy direction from the interface to the surface), of which data were included in Figure 3-5 (a – d). In contrast, for the HfO_2/TiN sample, the binding energy of the Hf $4f_{7/2}$ peak remained at ~16.4 eV throughout the entire thickness, suggesting that the entire film is under the influence of the Fermi energy shift due to the presence of the charged defects. The variation in the O1s peak position, included in Figure 3-5 (e–h), corroborates this interpretation. Also, there are small shoulder peaks at the binding energy of ~13.9 eV, which emerge near the TiN BE interface. These additional peaks correspond to the metallic Hf, which could be identified by the Hf $4f_{7/2}$ peak deconvolution as shown in Figures 3-4 (f–h). This is due to the preferential etching of oxygen, which must have been compensated by the fluent supply of oxygen in the case of the HfO_2 on RuO_2 BE. Therefore, it can be inferred that the adopted PEALD process generally deposited oxygen-deficient HfO_2 film, but the high oxygen-supply effect of the RuO_2 BE decreased the oxygen vacancy concentration near the interface in case of the HfO_2/RuO_2 sample. It has been reported that the RuO_2 serves as the oxygen source for the ALD of several oxide films, especially when the cation in the growing film has strong oxygen affinity, such as SrO and TiO_2, making the growth rate higher at the initial stage of the ALD.[52, 53] Similarly,

when the PEALD of HfO_2 film was grown on the RuO_2 BE in this work, it showed a significantly higher growth per cycle (GPC) of 0.31 nm/cycle up to 10 PEALD cycles than a normal GPC of 0.13 nm/cycle afterward as shown in Figure 3-1 (b). This is fundamentally due to the much higher oxide formation energy of HfO_2 (980.37 kJ/mol at the PEALD temperature of 200 °C), compared with that of the RuO_2 (224.37 kJ/mol at the same temperature). In fact, there was also an increase in the GPC (0.21 nm/cycle) during the initial stage of the PEALD up to 10 cycles, compared with the saturated GPC (0.12 nm/cycle) afterward for the PEALD of the HfO_2 film on the TiN BE. Such an enhancement could be due to the partial supply of oxygen from the surface TiON layer to the growing HfO_2, or to several other reasons, such as higher surface electrical conductivity or higher active chemical adsorption site density. For any reason, it is obvious that the TiN is not a fluent oxygen supply layer to the HfO_2 film. Therefore, compared with the film on the TiN BE, the HfO_2 film on the RuO_2 BE has a much higher insulating property. Ta TE also takes oxygen from the thin HfO_2 layer, so that the 3.0 nm thick HfO_2 film on the TiN BE cannot be used as a feasible ReRAM, due to the too high leakage current; whereas, the film with a similar thickness on the RuO_2 BE can be feasibly used as the ReRAM. The different switching behaviors of the devices shown in Figure 3-2 can be explained by a model based on the V_O distribution profile shown in Figure 3-6, which shows the schematics of the switching model of each device. In Figure 3-6 (a), the T-45 device initially contains high-density of

V_O's (red spheres) across the entire film thickness, resulting in relatively high leakage current, even at the pristine state (left panel). Once the device is electroformed (middle panel), many of the vacancies are collected (and even more vacancies might be generated) to form the CF (black-line polygon). In the subsequent reset switching (right panel), the CF near the BE interface is partially ruptured (black-dashed line polygon), and some residual filament is left (black-line polygon). Therefore, the subsequent set occurs at a lower voltage compared with the EF voltage. During the repeated switching cycles, the configuration of the residual filaments continuously changes, making the switching non-uniform (Figures 3-2 (d–f)). When the switching cycle increases, V_O could be accumulated at the HfO_2/TiN interface and form hour-glass like filament, which caused the performance degradations of the device using TiN BE.[36, 38, 56] In the R-45 device in Figure 3-6 (b), due to the V_O scavenging effect by the RuO_2 BE, the film near the BE interface could be highly insulating, and thus, the pristine leakage current was much lower than the T-45 device. The similar R_{LRS} of this device to that of the T-45 after the EF suggests that the CF configurations in these devices are similar. This suggests that EF might have induced more V_O generation in this device, and thereby, the subsequent reset and set switching characteristics become similar to those of the T-45 device. The difference with the T-45 device is that V_O could not be accumulated at the HfO_2/RuO_2 interface during repeated switching due to the V_O scavenging effect of RuO_2 electrode. However, the residual filaments formed during the

electroforming process did not disappear, resulting in switching non-uniformity similar to T-45 devices.[38] In the R-30 device of Figure 3-6 (c), the circumstance is quite different. As can be guessed from the involvement of many cases where the pristine resistance is close to the LRS, the integral part of the film thickness might be filled with the V_O's, but the average V_O concentration might not be too high to make the film short. When the V_{set} was applied, some of the V_O's are collected to a local position and form the percolated path (CF), and the film sets. Upon the application of the V_{reset}, the CF was almost completely ruptured recovering the initial state, making the device EF-free. A similar phenomenon was observed from the extremely thin HfO_2 film (~ 1.0 nm), which was grown by a thermal ALD using an identical Hf-precursor as in this work, but using a different oxygen source (O_3), and integrated into a 28 nm-diameter ReRAM device.[36, 56] In the previous work, the ~ (2.0 – 2.5) nm film required EF-process, which suggested the oxygen stoichiometric composition of the HfO_2 film grown by the thermal ALD. Therefore, it can be understood that the detailed chemical condition of the film growth process has a critical influence on the critical thickness where the EF-free performance can be achieved. In fact, the PEALD condition adopted in this work was optimized to produce the HfO_2 films with relatively high V_O concentration, as can be identified from the XPS results in Figure 3-4, to acquire the EF-free performance at a slightly thicker thickness (~3.0 nm).

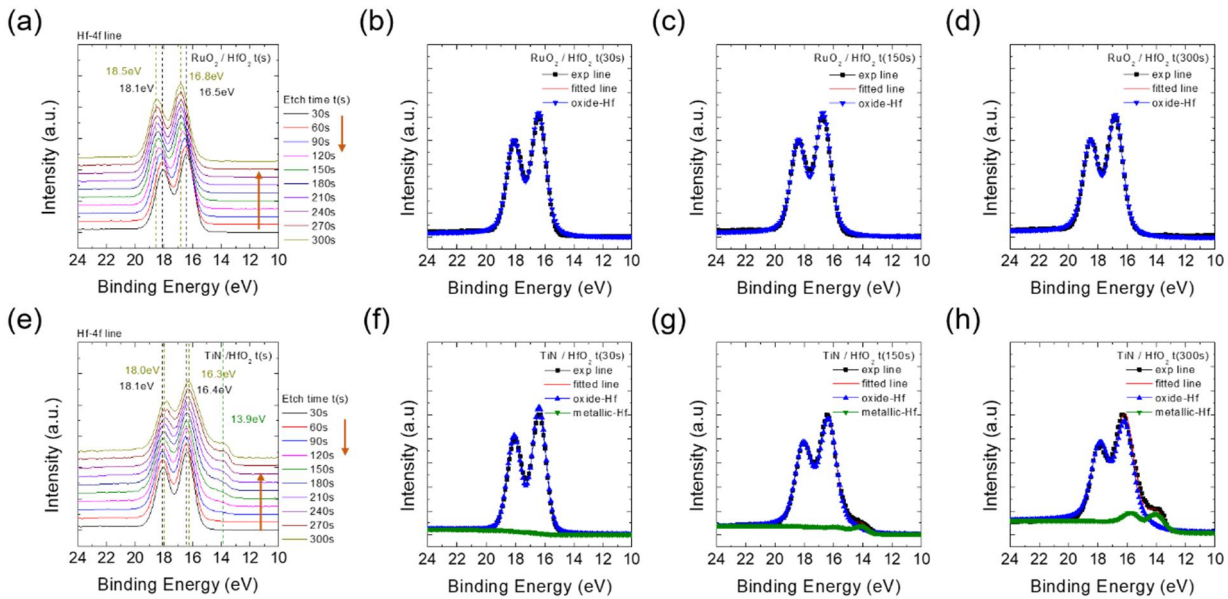


Figure 3-4. XPS spectra of the Hf *4f* region with a depth profile and fitting results for the RuO_2/HfO_2 30 ALD-cycled sample and TiN/HfO_2 30 ALD-cycled sample.

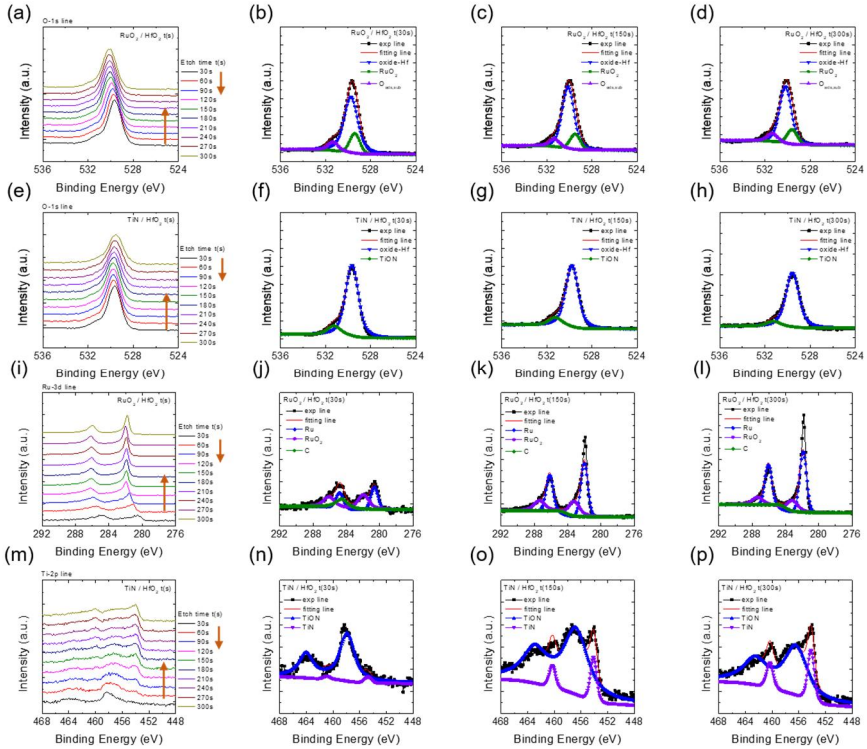


Figure 3-5. XPS spectra of the O *1s*, Ru *3d*, and Ti *2p* region with depth profile and fitting results for the RuO_2/HfO_2 30 ALD-cycled sample and TiN/HfO_2 30 ALD-cycled sample. Each sample was measured right after as-deposition. During XPS measurement, each sample is etched by Ar^+ plasma

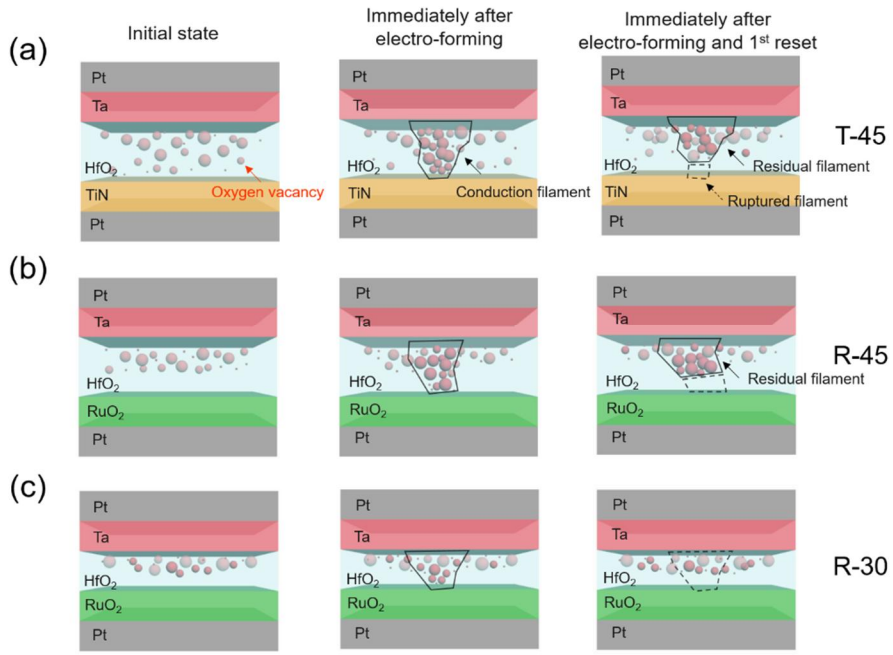


Figure 3-6. Schematics of the oxygen vacancy distribution of (a) T-45, (b) R-45, and (c) R-30 devices. The left, middle, and right panels in each figure show the initial state (before the electro-forming), the as-formed LRS, and the HRS, respectively. The black-solid and black-dash lines indicate the formed filaments and the ruptured filaments, respectively

3. 3. 3. Retention improvement model

Another crucial advantage to the use of RuO_2 BE can be found from the improvement in the retention characteristics. Figures 3-7 (a–c) show the retention performance of T-45, R-45, and R-30 devices, where the read voltage for the LRS and HRS were (+0.2 and -0.2) V, respectively. For this test, five cells from each type of device were selected and settled to the LRS and HRS, respectively, by the appropriate I–V sweep, and retained at 85 °C. In the T-45 device, both the LRS and HRS devices showed abrupt current jump after ~200 s and remained at an abnormally high conductive state. In contrast, both the R-45 and R-30 devices showed a stable retention characteristic up to ~10^5 s. The result with TiN BE is consistent with a previous report by Kim et al., who reported similar abnormal-retention failure phenomena in TiN/Ta/HfO2 (~1.0 nm) /TiN devices with 28-nm device diameter.[56] The retention failure is associated with the continuous oxygen scavenging effect of the TiN BE over time. The possible formation of a thin TiON layer between HfO_2/TiN interfaces due to air exposure during the Ta/HfO_2/TiN device fabrication process cannot be completely disregarded. However, such a thin and non-uniform TiON layer may not block the oxygen ion migration between the TiN BE and HfO_2 switching layers. With the help of electric-field and Joule heating that occurs during the repeated switching, the adverse oxygen ion migration toward the TiN BE from the HfO_2 could not be avoided during the repetitive switching operation or retention period of the device. These adverse effects caused

endurance and retention failure.[36, 38, 56] Figure 3-7 (d) shows a schematic to explain the retention failure mechanism with the TiN BE. The left and right panels of Figure 3-7 (d) show the retention failure in the HRS and LRS, respectively. The black polygons in the HfO_2 layer represent the residual filaments in the HRS and the conducting filaments in the LRS, respectively. In the T-45 device, the TiN BE is not completely inert but tends to attract oxygen from the HfO2 layer to form a TiON interfacial layer over time. This results in an increase in the Vo concentration in the HfO_2 layer, which is indicated by red arrows. Red dash polygons in the HfO_2 layer represent the local increase in the V_O concentration that rejuvenates the broken part of the residual filaments (left panel) or forms additional filaments (right panel), resulting in retention failure. RuO_2 BE can be an oxygen supplier, rather than a scavenger, so such an increase in the V_O concentration and resulting retention failure were not expected. Rather than that issue, it might have been possible to decrease the V_O concentration over time due to the V_O scavenging effect of the RuO_2, which might have induced the retention failure by a current drop. However, this was not the case, suggesting that the optimized condition for the RuO_2 BE growth has produced desirable chemical property of the RuO_2 BE.

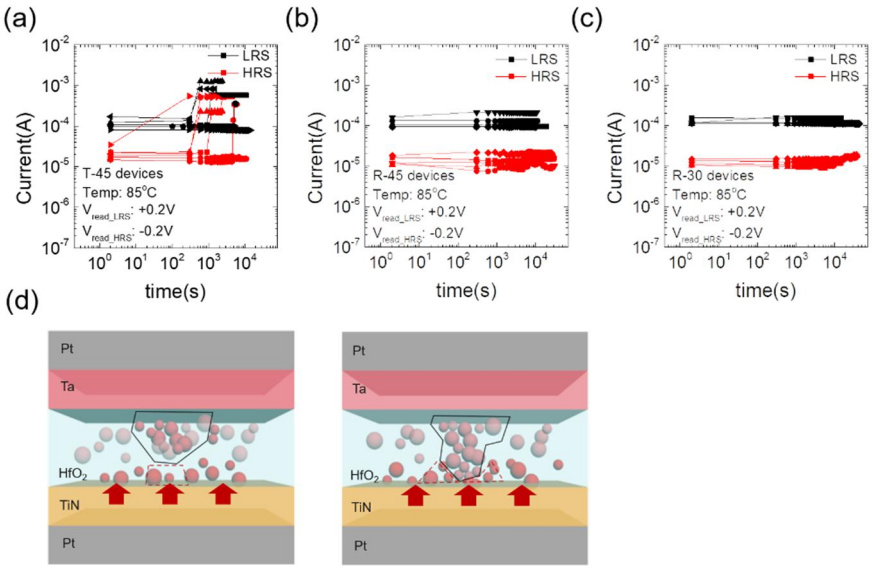


Figure 3-7. Retention performance of the (a) T-45, (b) R-45, and (c) R-30 devices. (d) A schematic vacancy model of HRS (left panel), and LRS (right panel) with the TiN BE. The red arrows indicate the oxygen scavenging effect of the TiN generating the oxygen vacancies. The black polygons and red dashed polygons represent the residual filaments and the rejuvenating filaments by TiN, respectively

3. 3. 4. Analog synapse performance and its neural network application

As discussed in the introduction, one of the main purposes of pursuing the EF-free performance from the R-30 device is to apply it to the analog synapse components of a neuromorphic computing device. Figure 3-8 shows the analog switching characteristic of the devices for the synapse applications. Figures 3-8 (a–c) show the long-term potentiation (LTP) and long-term depression (LTD) characteristics of T-45, R-45, and R-30 devices, respectively. The total number of pulses for LTP or LTD is ^{50}. Figure 3-8 (d) shows an experimental set-up (upper panel) and the pulse sequences (lower panel) for this measurement, where DUT is the device under the measurement (T-45, R-45, and R-30 devices). For this measurement, an identical 50 LTP (or LTD) pulses were applied using a pulse generator (PG), whose amplitude and width was 0.8V and 100ns for LTP mode (-1.0V and 800ns for LTD mode), and the output current was monitored using an oscilloscope (OSC) with two channels (Ch1, Ch2). The interval between pulses was 1.0μs for both LTP and LTD modes. Before the LTP or LTD measurement, each device was programmed to the HRS by DC sweep mode (I_{CC} = 300 μA and V_{reset} = -1.3 V). For the LTP and LTD measurements, identical pulse conditions were applied for the potentiation (pulse height: 0.8 V, pulse width: 100 ns, and pulse interval: 1 μs), and for the depression (pulse height: -1.0 V, pulse width: 800 ns, and pulse interval: 1 μs), for 50 times. The conductance change ($\Delta G = G - G_{HRS}$) was

monitored after every pulse input. These pulse voltage conditions correspond to the minimum voltage amplitudes for operating the T-45, R-45, and R-30 devices for the given pulse length; if the pulse amplitude was lower than 0.7 V and higher than -0.9 V for the set and reset programming, the conductance change was not observed. Figures 3-8 (a–c) show that the R-30 device exhibited relatively gradual and uniform LTP and LTD behaviors, while the R-45 and T-45 devices showed much more abrupt conductance change with a higher variation for both potentiation and depression. Although the maximum value of the conductance change (ΔG) was the smallest in the R-30 device, the ΔG variation of the R-30 device was much more gradual than that of the other devices. Figures 3-8 (e) and (f) show the average linearity factor and symmetry factor extracted from the results of LTP (left dot) and LTD (right dot) data of the T-45 (blue), R-45 (red), and R-30 (black) devices, respectively. The linearity can be quantified by the linearity factor, which is defined by the ratio of minimum conductance change rate to the maximum conductance change rate (Linearity factor = $\min d\ (\Delta G_{set}\ or\ \Delta G_{reset}) / \max d\ (\Delta G_{set}\ or\ \Delta G_{reset})$), of which the ideal value is 1.[20, 57, 58] Similarly, the symmetry factor is defined by the ratio of reset conductance change rate to set conductance change rate (Symmetry factor = $\mathrm{d}(\Delta \mathrm{G}_{\mathrm{reset}})/\mathrm{d}(\Delta \mathrm{G}_{\mathrm{set}})$) when $\mathrm{d}(\Delta \mathrm{G}_{\mathrm{reset}}) > \mathrm{d}(\Delta \mathrm{G}_{\mathrm{set}})$ (or $\mathrm{d}(\Delta \mathrm{G}_{\mathrm{set}})/\mathrm{d}(\Delta \mathrm{G}_{\mathrm{reset}})$ when $\mathrm{d}(\Delta \mathrm{G}_{\mathrm{reset}}) < \mathrm{d}(\Delta \mathrm{G}_{\mathrm{set}})$.) The ideal value of the symmetry factor is also 1.[59] Those factors can be the feasible metrics for the synaptic performances of ReRAMs, and help to estimate its effectiveness for

the neural network.[57–59] As expected, the R-30 device showed the highest linearity factor and the lowest symmetry factor close to the ideal synapse. This is a demonstration that the EF-free performance of a ReRAM can also improve synaptic performance. The following equations were used to fit the potentiation and depression behavior, which were necessary to estimate the influence of the non-ideal factors of the three types of synapses to the performance of a neural network:[60]

$$G(n+1) = G(n) + \alpha_p \exp\left(-\beta_p \frac{G(n) - G_{min}}{G_{max} - G_{min}}\right)$$

$$G(n+1) = G(n) - \alpha_d \exp\left(-\beta_d \frac{G_{max} - G(n)}{G_{max} - G_{min}}\right)$$

where, α_p and β_p are fitting coefficients for potentiation (α_d and β_d are for depression), n is the conductance state number, and G_{max} and G_{min} are the maximum and minimum possible conductance values representing the conductance boundaries of the ReRAM, respectively. Here, the n is set to 50, considering the number of potentiation and depression steps in Figure 3-8. These equations are used to calculate the conductance update rate as a function of the conductance values during the neural network training, of which the configuration is shown in Figure 3-9 (a). In the equation, as the β value decreases to 0, the conductance change rate becomes constant, which is regarded as the ideal synapse. Figure 3-10 (a) shows the fitting example of the R-30 device. Here, the yellow line indicates the exponential fitting curve, and the red lines indicate the upper and lower boundaries related to the coefficient

of variation of the device. Figure 3-10 (b) summarizes the fitting parameters for the T-45, R-45, and R-30 devices. These types of synaptic functions are applied to the synaptic weight update shown in the simple neural network of Figure 3-9 (a), which was composed of only three layers: input, hidden, and output layers, and was used to identify the MNIST data set. Figures 3-9 (b) and (c) show the detailed procedures to perform the neural network simulation. Figure 3-10 (c) shows the estimated MNIST dataset recognition accuracy for the three types of synapses. In the software-based simulation, the recognition accuracy assuming ideal synapse (both linearity factor and symmetric factors are 1) with infinite conductance state (labeled to the ideal (INF)) was 92.1 %, which is not sufficiently high due to the simple network structure assumed, but still comparable to other results with similar network structure.[20, 57–59] Then, the number of conductance states was limited to estimate the experimentally achievable highest accuracy, considering the finite LTP and LTD steps. When the ideal synapse was assumed with a limited number of conductance states of 50 (ideal (50)) which is the number of states in LTP and LTD in Figure 3-8, the accuracy was estimated to be 91.3 %; 0.8 % decreased when compared to the ideal (INF) case. Figure 3-10 (c) shows the estimated accuracy as a function of the number of training epochs. In all cases, even after the accuracy saturation at ~200,000 dataset training, the accuracy fluctuated, due to the stochastic variation of the ReRAM during the training. Figure 3-10 (d) shows an average accuracy after 200,000 samples training. Nevertheless, it was obvious that the

R-30 device showed the least fluctuation. The average estimated accuracies assuming the T-45, R-45, and R-30 devices were (87.96, 86.96, and 88.44) %, respectively. Despite the lower on-to-off ratio of the R-30 device, the improved linearity and symmetry in the R-30 device allow the highest performance of the neural network in the simulation.

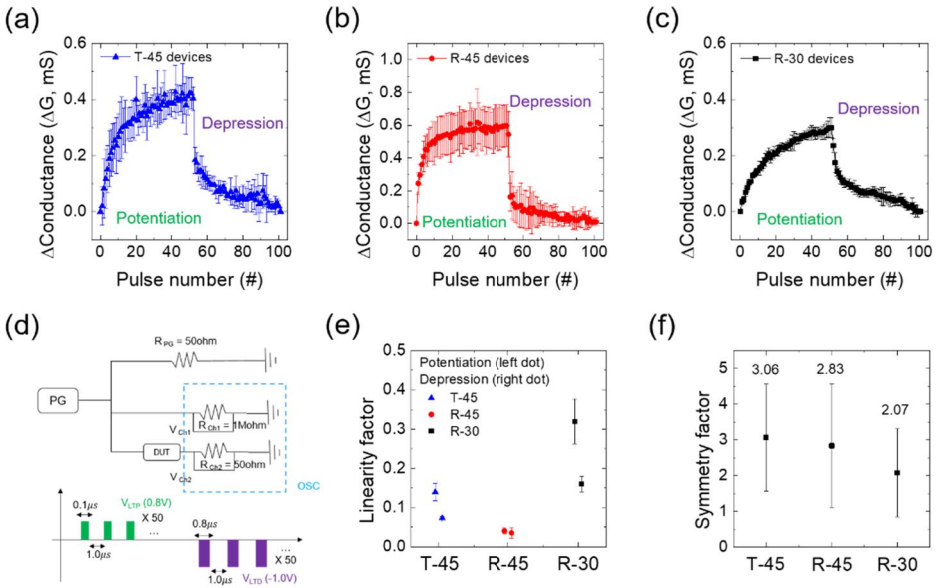


Figure 3-8. Potentiation and depression behavior of (a) T-45 (blue dot), (b) R-45 (red dot), and (c) R-30 (black dot) devices with identical potentiation and depression pulse condition, respectively ($\Delta G = G - G_{HRS}$). (d) The equivalent circuit (top panel) and the pulse sequences (bottom panel) used in this measurement. (e) Linearity factor of the devices, and (f) Symmetry factor of the devices.

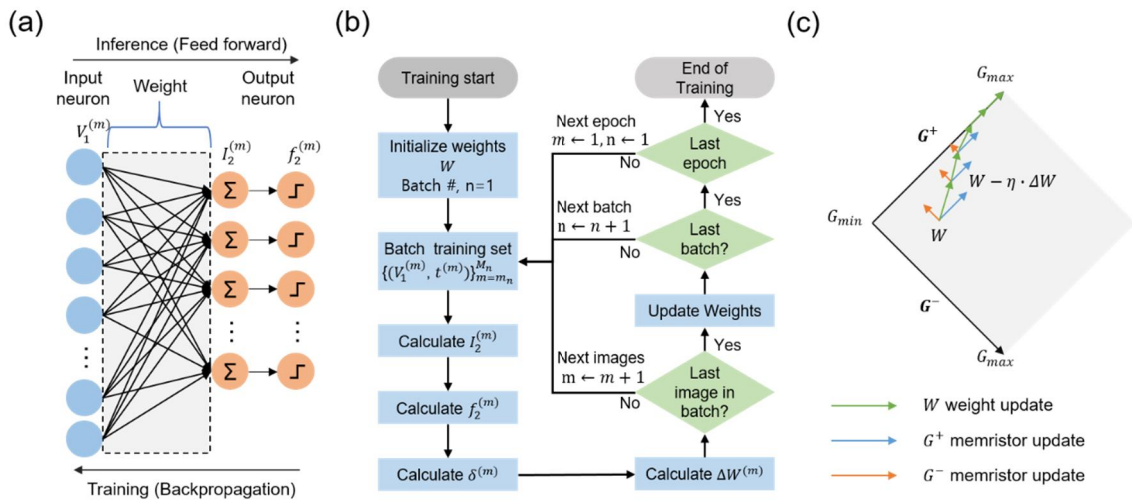
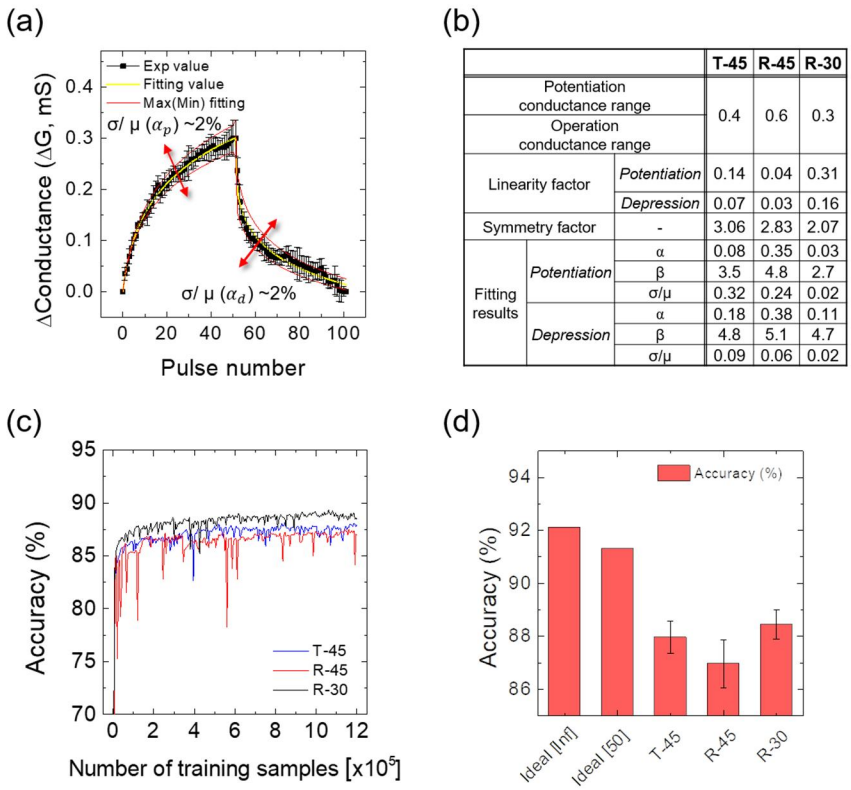


Figure 3-9. Memristive neural network simulation for MNIST digit recognition. (a) A single softmax regression network model. (b) A flowchart of softmax regression training. (c) Weight conductance diamond showing $\boldsymbol{G^+}$ and $\boldsymbol{G^-}$ memristor conductance update magnitude and direction. It also shows the current weight state, and the next one after updating. The green arrow is a weight update vector. The blue and orange arrows are $\boldsymbol{G^+}$ and $\boldsymbol{G^-}$ memristor updates, respectively



		T-45	R-45	R-30
Potentiation conductance range		0.4	0.6	0.3
Operation conductance range				
Linearity factor	*Potentiation*	0.14	0.04	0.31
	Depression	0.07	0.03	0.16
Symmetry factor	-	3.06	2.83	2.07
Fitting results	*Potentiation* α	0.08	0.35	0.03
	Potentiation β	3.5	4.8	2.7
	Potentiation σ/μ	0.32	0.24	0.02
	Depression α	0.18	0.38	0.11
	Depression β	4.8	5.1	4.7
	Depression σ/μ	0.09	0.06	0.02

Figure 3-10. (a) Simulated data using the linearity factor, symmetric factor, and coefficient of variation of experimental data in Figure 5. (b) The fitting parameters for the T-45, R-45, and R-30 devices). (c) The estimated MNIST dataset recognition accuracy for the cases in Figure 3-10 (b). (d) MNIST test dataset recognition accuracy during training

3.4. Conclusion

Resistive switching memory using the PEALD-grown HfO_2 thin film as the switching layer was optimized to use the memory cell as an analog-type synapse in the neuromorphic circuit. Most problems of the ReRAM cell to be used as a feasible synapse, such as high non-linearity, high asymmetry in potentiation and depression, low repeatability and uniformity of the switching performance, and low retention, are related to the uncontrolled formation and rupture of the CFs. Such a problem appeared to be closely related to the electroforming process, which inevitably induced the uncontrollable formation of the CFs. Therefore, electroforming-free ReRAM was necessary, which could fundamentally be achieved by thinning the PEALD-grown HfO_2 film from (4.5 to 3.0) nm. However, for such a thin film, the adoption of RuO_2 bottom electrode, replacing the convention TiN bottom electrode, was essential. Otherwise, the 3.0 nm-thick film showed too high a leakage current to be used as a feasible memory. The optimized $Ta/HfO_2/RuO_2$ stack provided the desirable performances for it to be used as a feasible synapse with improved linearity and symmetry factors. The PEALD HfO_2 film was initially oxygen-deficient, which was actually a prerequisite to induce a useful level of leakage current for it to be used as a feasible ReRAM when it was thicker than ~4.5 nm. The portion of the HfO_2 film in contact with the RuO_2 bottom electrode recovered the stoichiometric composition, making the interface layer highly

insulating, but still thin enough to achieve the electroforming-free performances

3.5. References

(1) Waldrop, M. M. The Chips are down for Moore's law. *Nature* **2016,** *530*, 144-147.

(2) Di Ventra, M.; Pershin, Y. V. The parallel Approach. *Nat. Phys*. **2013,** *9*, 200-202.

(3) Yang, J. J.; Strukov, D. B.; Stewart, D. R. Memristive devices for computing. *Nat. Nanotechnol*. **2013,** *8*, 13-24.

(4) Yang, R.; Terabe, K.; Liu, G.; Tsuruoka, T.; Hasegawa, T. On-demand nanodevice with electrical and neuromorphic multifunction realized by local ion migration. *ACS Nano* **2012,** *6*, 9515-9521.

(5) Jo, S. H.; Chang, T.; Ebong, I.; Bhavitavya, B.; Mazumder, P.; Lu, W. Nanoscale memristor device as synapse in neuromorphic systems. *Nano Lett.* **2010,** *10*, 1297-1301.

(6) Feldman, D. E. The Spike-Timing Dependence of Plasticity. *Neuron*. **2012,** *75*, 556-571.

(7) Abbott, L. F.; Nelson, S. B. Synaptic plasticity: taming the beast. *Nat. Neurosci.* **2000,** *3*, 1178-1183.

(8) Li, Y.; Zhong, Y. P.; Zhang, J. J.; Xu, L.; Wang, Q.; Sun, H. J.; Tong, H.; Cheng, X. M.; Miao, X. S. Activity-Dependent Synaptic Plasticity of a Chalcogenide Electronic Synapse for Neuromorphic Systems. *Sci. Rep*. **2014,** *4*, No. 4906.

(9) Chang, T.; Jo, S.-H.; Lu, W. Short-Term Memory to Long-Term Memory Transition in a Nanoscale Memristor. *ACS Nano* **2011,** *5*, 7669-7676.

(10) Kim, S.; Du, C.; Sheridan, P.; Ma, W.; Choi, S.; Lu, W. D. Experimental

Demonstration of a Second-Order Memristor and Its Ability to Biorealistically Implement Synaptic Plasticity. *Nano Lett.* **2015,** *15*, 2203-2211.

(11) Wang, I. T.; Lin, Y. C.; Wang, Y. F.; Hsu, C. W.; Hou, T. H. 3D Synaptic Architecture with Ultralow Sub-10 FJ Energy per Spike for Neuromorphic Computation. *IEEE International Electron Devices Meeting,* San Francisco, USA, Dec 15-17, 2014.

(12) Jeong, Y.; Kim, S.; Lu, W. D. Utilizing Multiple State Variables to Improve the Dynamic Range of Analog Switching in a Memristor. *Appl. Phys. Lett.* **2015,** *107*, No. 173105.

(13) Woo, J.; Moon, K.; Song, J.; Lee, S.; Kwak, M.; Park, J.; Hwang, H. Improved Synaptic Behavior under Identical Pulses Using AlO_x/HfO_x Bilayer RRAM Array for Neuromorphic Systems. *IEEE Electron Device Lett*. **2016,** *37*, 994-997.

(14) Wang, Z.; Yin, M.; Zhang, T.; Cai, Y.; Wang, Y.; Yang, Y.; Huang, R. Engineering Incremental Resistive Switching in TaO_x Based Memritors for Brain-Inspired Computing. *Nanoscale* **2016,** *8*, 14015-14022.

(15) Woo, J.; Padovani, A.; Moon, K.; Kwak, M.; Larcher, L.; Hwang, H. Linking Conductive Filament Properties and Evlution to Synaptic Behavior of RRAM Devices for Neuromorphic Applications. *IEEE Electron Device Lett*. **2017,** *38*, 1220-1223.

(16) Hu, M.; Graves, C. E.; Li, C.; Li, Y.; Ge, N.; Montgomery, E.; Davila, N.; Jiang, H.; Williams, R. S.; Yang, J. J.; Xia, Q.; Strachan, J. P. Memristor-Based Analog Computation and Neural Network Classification with a Dot Product Engine. *Adv. Mater*. **2018,** *30*, No. 1705914.

(17) Li, C.; Belkin, D.; Li, Y.; Yan, P.; Hu, M.; Ge, N.; Jiang, H.; Montgomery, E.;

Lin, P.; Wang, Z.; Song, W.; Strachen, J. P.; Barnell, M.; Wu, Q.; Williams, R. S.; Yang, J. J.; Xia, Q. Efficient and self-adaptive in-situ learning in multilayer memristor neural networks. *Nat. Commun*. **2018,** *9*, No. 2385.

(18) Burr, G. W.; Shelby, R. M.; Sidler, S.; Nolfo, C.; Jang, J.; Boybat, I.; Shenoy, R. S.; Narayanan, P.; Virwani, K.; Giacometti, E. U.; Kuridi, B. N.; Hwang, H. Experimental Demonstration and Tolerancing of a Large-Scale Neural Network (165 000 Synapses) Using Phase-Change Memory as the Synaptic Weight Element. *IEEE Trans. Electron Devices* **2015,** *62*, 3498-3507.

(19) Jeong, D. S.; Hwang, C. S. Nonvolatile Memory Materials for Neuromorphic Intelligent Machines. *Adv. Mater*. **2018,** *30*, No. 1704729.

(20) Kim, S.; Choi, B.; Lim, M.; Yoon, J.; Lee, J.; Kim, H.-D.; Choi, S.-J. Pattern Recognition Using Carbon Nanotube Synaptic Transistor with an Adjustable Weight Update Protocol. *ACS Nano* **2017,** *11*, 2814-2822.

(21) Yu, S.; Gao, B.; Fang, Z.; Yu, H.; Kang, J.; Wong, H.-S. P. A Low Energy Oxide-Based Electronic Synaptic Device for Neuromorphic Visual Systems with Tolerance to Device Variation. *Adv. Mater*. **2013,** *25*, 1774-1779.

(22) Song, H.; Kim, Y. S.; Park, J.; Kim, M. K. Designed Memristor Circuit for Self-Limited Analog Switching and its Application to a Memristive Neural Network. *Adv. Electron. Mater.* **2019,** *5*, No. 1800740.

(23) Waser, R.; Dittmann, R.; Staikov, G.; Szot, K. Redox-Based Resistive Switching Memories-Nanoionic Mechanisms, Prospects, and Challenges. *Adv. Mater*. **2009,** *21*, 2632-2663.

(24) Miao, F.; Strachen, J. P.; Yang, J. J.; Zhang, M.-X.; Goldfarb, I.; Torrezan, A. C.; Eschbach, P.; Kelley, R. D.; Medeiros-Ribeiro, G.; Williams, R. S. Anatomy of a Nanoscale Conduction Channel Reveals the Mechanism of a High-

Performance Memristor. *Adv. Mater*. **2011,** *23*, 5633-5640.

(25) Kim, K. M.; Jeong, D. S.; Hwang, C. S. Nanofilamentary resistive switching in binary oxide system; a review on the present status and outlook. *Nanotechnol.* **2011,** *22*, No. 254002.

(26) Yang, J. J.; Zhang, M.-X.; Strachen, J. P.; Miao, F.; Pickett, M.; Kelley, R. D.; Medeiros-Ribeiro, G.; Williams, R. S. High switching endurance in TaO_x memristive devices. *Appl. Phys. Lett*. **2010,** *97*, No. 232102.

(27) Choi, B. J.; Jeong, D. S.; Kim, S. K.; Rohde, C.; Choi, S.; Oh, J. H.; Kim, H. J.; Hwang, C. S.; Szot, K.; Waser, R.; Reichenberg, B.; Tiedke, S.; Resistive Switching Mechanism of TiO_2 Thin Films Frown by Atomic-Layer Deposition. *J. Appl. Phys*. **2005,** *98*, No. 033715.

(28) Park, G.-S.; Li, X.-S.; Kim, D.-C.; Jung, R.-J.; Lee, M.-J.; Seo, S. Observation of electric-field induced Ni filament channels in polycrystalline NiO_x film. *Appl. Phys. Lett*. **2007,** *97*, No. 222103.

(29) Kim, K. M.; Choi, B. J.; Hwang, C. S. Localized Switching Mechanism in Resistive Switching of Atomic-Layer-Deposited TiO_2 Thin Films. *Appl. Phys. Lett*. **2007,** *90*, No. 242906.

(30) Kwon, D.-H.; Kim, K.; Jang, J.; Jeon, J.; Lee, M.; Kim, G.; Li, X.-S.; Park, G.-S.; Lee, B.; Han, S.; Kim, M.; Hwang, C. S. Atomic Structure of Conducting Nanofilaments in TiO_2 Resistive Switching Memory. *Nat. Nanotechnol*. **2010,** *5*, 148-153.

(31) Kim, G. H.; Lee, J. H.; Seok, J. Y.; Song, S. J.; Yoon, J. H.; Yoon, K. J.; Lee, M. H.; Kim, K. M.; Lee, H. D.; Ryu, S. W.; Park, T. J.; Hwang, C. S. Improved endurance of resistive switching TiO_2 thin film by hourglass shaped Magneli filaments. *Appl. Phys. Lett*. **2011,** *98*, No. 262901.

(32) Kim, K. M.; Park, T. H.; Hwang, C. S. Dual Conical Conducting Filament Model in Resistance Switching TiO_2 Thin Films. *Sci. Rep*. **2015,** *5*, No. 7844.

(33) Yoon, K. J.; Song, S. J.; Seok, J. Y.; Yoon, J. H.; Kim, G. H.; Lee, J. H.; Hwang, C. S. Ionic bipolar resistive switching modes determined by the preceding unipolar resistive switching reset behavior in Pt/TiO_2/Pt. *Nanotechnology* **2013,** *24*, No. 145201.

(34) Song, S. J.; Seok, J. Y.; Yoon, J. H.; Kim, K. M.; Kim, G. H.; Lee, M. H.; Hwang, C. S. Real-time identification of the evolution of conducting nano-filaments in TiO_2 thin film ReRAM. *Sci. Rep*. **2013,** *3*, No. 3443.

(35) Kim, K. M.; Lee, M. H.; Kim, G. H.; Song, S. J.; Seok, J. Y.; Yoon, J. H.; Hwang, C. S. Understanding structure-property relationship of resistive switching oxide thin films using a conical filament model. *Appl. Phys. Lett.* **2010,** *97*, No. 162912.

(36) Park, T. H.; Song, S. J.; Kim, H. J.; Kim, S. G.; Chung, S.; Kim, B. Y.; Lee, K. J.; Kim, K. M.; Choi, B. J.; Hwang, C. S. Thickness effect of ultra-thin Ta_2O_5 resistance switching layer in 28 nm-diameter memory cell. *Sci. Rep*. **2015,** *5*, No. 15965.

(37) Park, T. H.; Kim, H. J.; Park, W. Y.; Kim, S. G.; Choi, B. J.; Hwang, C. S. Roles of conducting filament and non-filament regions in the Ta_2O_5 and HfO_2 resistive switching memory for switching reliability. *Nanoscale* **2017,** *9*, 6010-6019.

(38) Park, T. H.; Kwon, Y. J.; Kim, H. J.; Woo, H. C.; Kim, G. S.; An, C. H.; Kim, Y.; Kwon, D. E.; Hwang, C. S. Balancing the Source and Sink of Oxygen Vacancies for the Resistive Switching Memory. *ACS Appl. Mater. Interfaces.* **2018,** *10*, 21445-21450.

(39) Park, G.-S.; Kim, Y. B.; Park, S. Y.; Li, X. S.; Heo, S.; Lee, M.-J.; Chang, M.; Kwon, J. H.; Kim, M.; Chung, U.-I.; Dittmann, R.; Waser, R.; Kim, K. *In Situ* Observation of Filamentrary Conducting Channels in an Asymmetric Ta_2O_{5-X} / TaO_{2-X} Bilayer Structure. *Nat. Commun*. **2013,** *4*, No. 2382.

(40) Li, C.; Gao, B.; Yao, Y.; Guan, X.; Shen, X.; Wang, Y.; Huang, P.; Liu, L.; Lie, X.; Li, J.; Gu, C.; Kang, L.; Yu, R. Direct Observations of Nanofilament Evolution in Switching Processed in HfO_2-Based Resistive Random Access Memory by In situ TEM studies. *Adv. Mater.* **2017,** *29*, No. 1602976.

(41) Park, T. H.; Song, S. J.; Kim, H. J.; Kim, S. G.; Chung, S.; Kim, B. Y.; Lee, K. J.; Kim, K. M.; Choi, B. J.; Hwang, C. S. Thickness-dependent electroforming behavior of ultra-thin Ta_2O_5 resistance switching layer. *Phys. status solidi-Rapid Res. Lett*. **2015,** *9*, 362-365.

(42) Kuzmichev, D. S.; Lebedinskii, Y. Y.; Hwang. C. S.; Markeev, A. M. Atomic Layer Deposited Oxygen-Deficient TaO_x Layers for Electroforming-Free and Reliable Resistance Switching Memory. *Phys. status solidi-Rapid Res. Lett*. **2018,** *12*, No. 1800429.

(43) Ku, B.; Abbas, Y.; Sokolov, A. S.; Choi, C. Interface engineering of ALD HfO_2-based RRAM with Ar plasma treatment for reliable and uniform switching behaviors. *J. Alloys Compd.* **2018,** *735*, 1181-1188.

(44) Kim, K. M.; Zhang, J.; Graves, C.; Yang, J. J.; Choi, B. J.; Hwang, C. S.; Li, Z.; Williams, R. S. Low-Power, Self-Rectifying, and Forming-Free Memristor with an Asymmetric Programing Voltage for a High-Density Crossbar Application. *Nano Lett*. **2016,** *16*, 6724-2732.

(45) Yoon, J. H.; Song, S. J.; Yoo, I.-H.; Seok, J. Y.; Yoon, K. J.; Kwon, D. E.; Park, T. H.; Hwang. C. S. Highly Uniform, Electroforming-Free, and Self-Rectifying Resistive Memory in the Pt/Ta_2O_5/HfO_{2-X}/TiN Structure. *Adv. Funct. Mater*.

2014, *24*, 5086-5095.

(46) Kim, K. M.; Kim, G. H.; Song, S. J.; Seok, J. Y.; Lee, M. H.; Yoon, J. H.; Hwang, C. S. Electrically configurable electroforming and bipolar resistive switching in Pt/TiO_2/Pt structures. *Nanotechnology* **2010,** *21*, No. 305203.

(47) Xue, W. H.; Xiao, W.; Chen, X. X.; Zhu, X. J.; Shang, J.; Pan, L.; Tan, H. W.; Zhang, W. B.; Ji, Z. H.; Liu, G.; Xu, X.-H.; Ding, J.; Li, R.-W. Intrinsic and Interfacial Effect of Electrode Metals on the Resistive Switching Behaviors of Zinc Oxide Films. *Nanotechnology* **2014,** *24*, No. 425204.

(48) Ge, N.; Zhang, M.-X.; Zhang, L.; Yang, J. J.; Li, Z.; Williams, R. S. Electrode-Material Dependent Switching in TaO_x Memristors. *Semicond. Sci. Technol.* **2014,** *29*, No. 104003.

(49) Lee, M.-J.; Lee, C. B.; Lee, D.; Lee, S. R.; Chang, M.; Hur, J. H.; Kim, Y.-B.; Kim, C.-J.; Seo, D. H.; Seo, S.; Chung, U.-I.; Yoo, I.-K.; Kim, K. A fast, high-endurance and scalable non-volatile memory device made from asymmetric Ta_2O_{5-X}/TaO_{2-X} bilayer structures. *Nat. Mater.* **2011,** *10*, 625-630.

(50) Kim, K. M.; Song, S. J.; Kim, G. H.; Seok, J. Y.; Lee, M. H.; Zhao, J. S.; Hwang, C. S. Methods of Set Switching for Improving the Uniformity of Filament Formation in the TiO_2 Thin Film. *Electrochem. Solid-State Lett*. **2010**, *13*, G51-G53.

(51) Song, S. J.; Kim, K. M.; Kim, G. H.; Lee, M. H.; Seok, J. Y.; Jung, R.; Hwang, C. S. Identification of the controlling parameter for the set-state resistance of a TiO_2 resistive switching cell. *Appl. Phys. Lett*. **2010,** *96*, No. 112904.

(52) Song, S. J.; Lee, S. W.; Kim, G. H.; Seok, J. Y.; Yoon, K. J.; Yoon, J. H.; Hwang, C. S.; Gatineau, J.; Ko, C. Substrate Dependent Growth Behaviors of Plasma-Enhanced Atomic Layer Deposited Nickel Oxide Films for Resistive Switching

Application. *Chem. Mater.* **2012,** *24*, 4675-4685.

(53) Jeon, W.; Lee, W.; Yoo, Y. W.; An, C. H.; Han, J. H.; Kim, S. K.; Hwang, C. S. Chemistry of Active Oxygen in RuO_x and Its Influence on the Atomic Layer Deposition of TiO_2 Films. *J. Mater. Chem. C*. **2014,** *2*, 9993-10001.

(54) Cho, D.-Y.; Min, C.-H.; Kim, J.; Oh, S.-J. Bond nature of oxygen-deficient HfO_2/Si(100)film. *Appl. Phys. Lett.* **2006**, *89*, No. 253510.

(55) Moudler, J. F.; Stickle, W. F.; Sobol, P. E.; Bomben, K. D. *Handbook of X-ray Photoelectron Spectroscopy*; Perkin-Elmer: Eden Prairie, MN, 1992.

(56) Kim, G. S.; Park, T. H.; Kim, H. J.; Ha, T. J.; Park, W. Y.; Kim, S. G.; Hwang, C. S. Investigation of the retention performance of an ultra-thin HfO_2 resistance switching layer in an integrated memory device. *J. Appl. Phys.* **2018,** *124*, No. 024102.

(57) Kim, S.; Lim, M.; Kim, Y.; Kim, H.-D.; Choi, S.-J. Impact of Synaptic Device Variations on Pattern Recognition Accuracy in a Hardware Neural Network. *Sci. Rep.* **2018,** *8*, No. 2638.

(58) Wang, I.-T.; Chang, C.-C.; Chiu, L.-W.; Chou, T.; Hou, T.-H. 3D $Ta/TaO_x/TiO_x/Ti$ Synaptic Array and Linearity Tuning of Weight Update for Hardware Neural Network Applications. *Nanotechnology* **2016,** *27*, No. 365204.

(59) Yang, C.-S.; Shang, D.-S.; Liu, N.; Fuller, E. J.; Agrawal, S.; Talin, A. A.; Li, Y.-Q.; Shen, B.-G.; Sun, Y. All-Solid-State Synaptic Transistor with Ultralow Conductance for Neuromorphic Computing. *Adv. Funct. Mater*. **2018**, *28*, No. 1804170.

(60) Querlioz, D.; Dollfus, P.; Bichler, O.; Gamrat, C. Learning with Memristive Devices: How Should We Model Their Behavior?, *IEEE/ACM International*

4. HfO_2-based planar 1T-1R device and Resistive switching behavior for Next-generation Vertical-string 1T-1R array

4.1. Introduction

At present, the main non-volatile storage memory is NAND flash memory, which has faced limitations because of parasitic effects by scaling down. 2-dimensional NAND flash has encountered physical limitations to cell size reduction, such as cell to cell interference and cell uniformity.[1-7] Therefore, 3-dimensional stacked vertical-NAND flash (V-NAND flash) stacked in a vertical direction is developed.[8-9] Although V-NAND flash technology suggests higher density than planar type, V-NAND flash has other problems like technical difficulties in the hole etching process as the aspect ratio increases, charge loss in the lateral direction, and word plane parasitic capacitance as each oxide gets thinner.[10-15] Therefore, researches on memory unit for the successor of V-NAND flash are attracting attention.[16-19] Among the next-generation non-volatile memories (NVMs), the resistance random access memory (ReRAM) has been widely studied because of its relatively simple metal-insulator-metal (MIM) structure, high scalability, low power, high speed, good reliability, and complementary metal-oxide-semiconductor (CMOS) compatibility. Representative commercialization of resistive switching (RS) memory is Intel's

‘3D Xpoint’, named by the ‘Optane’ brand. 3D Xpoint has a unit cell size of $4F^2$ in the form of a crossbar array (CBA) using phase-change memory. However, as the number of vertical stacks increases, the fabrication cost is exponentially increased because functional line process such as photolithography and etching is increased. In addition, a two-terminal structure did not fit the existing CPU design. Therefore, Optane, which is only fitted for storage-class-memory, has not been succeeded in the semiconductor market.

There are many kinds of research on the 3D structure of the ReRAM to replace NAND flash’s position.[16-19] In the CBA stacking structure, it has crucial weak points such as sneak path currents, which induce read disturbance and high energy consumption.[20-24] To overcome sneak path current, a good selectivity selector and proper voltage operation scheme are needed.[22-24] However, it is hard to match proper selector and ReRAM devices. So, another study for the 3D structure of the ReRAM is needed to produce next-generation, high-density NVM. Other structures for stacking ReRAM can be divided into a side-wall-type and a hole-type vertical structure.[16,25-27] The side-wall-type has a structure that word lines and isolation layers are alternately stacked, then selectors and resistors are deposited on the sidewalls and then covered by bit lines.[16,25,26] Compared to 3D Xpoint, it has an advantage in the number of process steps and bit line contacts regardless of the increase in the number of layers. However, it requires an excellent operating characteristic of 1-selector (S)-1-resistor (R). Another stacked ReRAM, the hole-type vertical structure

stacks word lines and isolation layers alternately,[16,27] then etches holes and deposits thin-film-transistors (TFT, T) and resistors (R) on the wall. The hole-type vertical structure can suppress sneak path current efficiently, as TFT can play a selector role. In the hole-type vertical structure, TFT for device selection and the resistor for storing the memory are connected in parallel as unit devices, and the unit devices are connected in serial. Such vertical-string 1T-1R array is called 'V-TFT-ReRAM,' and the conditions required for operation are as follows.[16]

In "V-TFT-ReRAM", an oxide-based RS layer is deposited inside the hole after the transistor fabrication. In this structure, the RS layer and channel are in direct contact forming an effective parallel circuit structure. V-TFT-ReRAM can be operated by turning off the corresponding TFT parallel to the selected cell in writing and reading modes. For the fluent operation of the V-TFT-ReRAM device, the following conditions must be fulfilled. The sum of all the on-TFTs (R_S^T) on-resistances must be low to provide proper voltage to the selected 1T-1R unit cell. Also, the off-resistance of the TFT (R_{off}^T) of the selected cell must be high compared with the on- and off-resistance of the selected memory cell (R_{on}^m and R_{off}^m) to efficiently apply the operating current to the memory cell (ReRAM or resistor in this work), which must be supplied through the TFT channel string.[16]

There are many candidates for V-TFT-ReRAM's RS material such as HfO_x, TaO_x, AlO_x, NiO_x, TiO_x, etc. V-TFT-ReRAM's RS material should have some natures like high endurance behavior, enough on-off ratio, good retention for NVM and CMOS compatibility.[28] Among these materials, the HfO_x layer has many advantages such as CMOS compatibility, high speed, moderate on/off ratio, good endurance, good retention, and capability to multi-bit operation.[28-31] Therefore, the HfO_x layer is used for RS material in this work.

In this work, The HfO_2-based planar structure 1T-1R device was investigated as prior research to the next-generation V-TFT-ReRAM. The large-scale 1T-1R with HfO_2 resistor was investigated, in which the most stoichiometric PEALD-HfO_2 and the most O-deficient THALD-HfO_2 were used as RS layers. For the planar-direction NVM behavior between source and drain electrode, scaled-1R with a 20nm of switching-length using e-beam lithography process was evaluated. In the scaled-1R with stoichiometric PEALD-HfO_2, repetitive planar-direction NVM behavior was observed, and compatibility with 1T for stable operation in merged 1T-1R was achieved. Finally, it was confirmed that more than 200 cell-string of 1T-1R is possible as a result of the experimental data-based cell-string number simulation.

4.2. Experimental

Cell Fabrication: 1T-1R device with planar-structure scaled ReRAM on top of bottom-gate IGZO-based thin film transistor was fabricated by the following process steps. The p-type Si substrate was used as the gate electrode. A 100nm-thick SiO_2 layer was thermally grown as the gate dielectric. A 50nm-thick IGZO was sputtered at room temperature using an IGZO target at 50W radio frequency (RF) power and 3mtorr working pressure in the Ar atmosphere. IGZO channel layer was patterned by photolithography and wet etching procedure. 80nm-thick SiO_2 was deposited with a PECVD system using 170sccm 5% SiH_4/N_2 gas and 1000sccm N_2O gas at 20W RF power. Etch-stop-layer was patterned by photolithography and dry etched out with an inductively coupled plasma (ICP) etcher. ITO film, which functions as a TFTs source/drain and ReRAM electrode, was deposited via direct-current sputtering and patterned through lift-off process using photolithography and e-beam lithography, respectively. A JEOL, JBX-6300FS electron-beam lithography tool was used to form sub-50nm patterns. A resist layer of poly-methyl-methacrylate (PMMA, 495K) was spin-coated at 3000 rpm for 45 s to obtain a film thickness of approximately 200nm and subsequently baked at 180℃ for 180 s to remove residual solvent. E-beam lithography was performed with energy, dose, and step size at 100keV, 1000μC/cm^2, and 6nm, respectively. HfO_2 switching layer was deposited via plasma-enhanced atomic layer deposition (PEALD) using Tetrakis(ethylmethylamiono)-Hafnium as the Hf

source with O_2 plasma as an oxygen source at a substrate temperature of 200℃. HfO_2 film on the contact pad of the ITO electrodes was etched out for the electrical contact with the RIE etcher using CF_4 and Ar gas. The post-metallization-annealing was followed in an air atmosphere at 350℃ for an hour after the 1T-1R device was fabricated to improve the electrical characteristics of the IGZO-based TFTs.

Characterization: The electrical characteristics of the TFTs and lateral ReRAM were measured using a semiconductor parameter analyzer (Hewlett Packard, 4155B). The film crystallinity and thickness were measured using X-ray diffraction (XRD, PANalytical, X'Pert PRO MPD) and spectroscopic ellipsometry (SE, J.A. Woolam, ESM-300). Energy-dispersive X-ray fluorescence (EDXRF, Thermo Scientific, Quant'X) was used to measure the composition and layer density of the deposited films. Completed 1T1R device image and enlarged scaled ReRAM electrode image were obtained using FESEM (Hitachi, S-4800).

4.3. Results and Discussions

4. 3. 1. Switching characteristics of large-scale 1T-1R

Figure 4-1 (a) shows HfO_2-based planar structure 1T-1R, and Figure 4-1 (b) shows the fabrication flow of HfO_2-based planar structure 1T-1R. The device is fabricated by manufacturing a bottom-gate-TFT device using an IGZO channel, and the HfO_2 RS layer is deposited on the top of the backchannel. In this research confirming the program and read operations between source and drain electrodes is attempted by applying DC sweep voltage in off-channel conditions. For stable operation of the 1T-1R, the channel-on and -off resistance of 1T should be large enough to cover both low-resistance-state (LRS) and high-resistance-state (HRS) of the resistor.[16] However, prior to the research, there were several issues; First, in previous ReRAM studies, the repetitive NVM behavior in the planar-direction rather than the thickness-direction in the RS layer has not been reported yet. Second, even if the NVM behavior is observed in the RS layer, it is difficult to achieve compatibility between the resistor and the transistor operations in Figure 4-1 (a). Third, because of the inherently symmetric structure, resistive switching behavior cannot be controlled through electrode material selection or bilayer structure as in general ReRAM research.[32-34] Since the fabrication variable that can control the resistive switching behavior is limited to the properties of the RS layer, and it

is essential to engineer the defect like oxygen vacancy (V_O) in the resistor to obtain planar-direction NVM behavior and compatibility with 1T device.

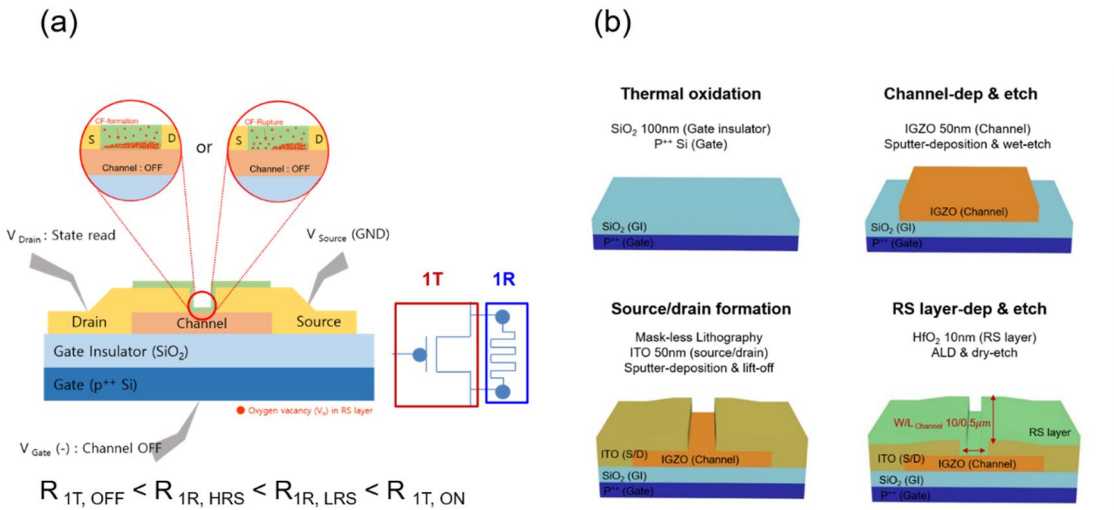


Figure 4-1. (a) the HfO_2-based planar structure 1T-1R and (b) the fabrication flow of HfO_2-based planar structure 1T-1R. The device is fabricated by manufacturing a bottom-gate-TFT device using IGZO-channel, and HfO_2 resistive-switching(RS) layer is deposited on the top of the backchannel

Figure 4-2 shows the MIM leakage-current of the HfO_2 layer depending on the deposition conditions, substrate temperature, and O_2-plasma power. There are several studies that control physical/chemical properties such as density, crystallinity, and chemical composition of the oxide layer by controlling the type of oxidant (or precursor) and deposition conditions in the ALD of oxide.[35-38] In the PEALD-HfO_2, the properties of HfO_2 are analyzed by leakage-current analysis depending on substrate temperature and O_2-plasma power control as shown in Figure 4-2 (a) and (c), respectively. In the measurement, a MIM Cap. with Pt/HfO_2(10nm)/Pt structure in which both the electrode area and the HfO_2 thickness were equally controlled is used. Figure 4-2 (a) and (b) show the leakage results of a PEALD-HfO_2 layer deposited at 200°C, 100W-O_2-plasma power, and a THALD-HfO_2 layer deposited at 280-300°C, 0W-O_2-plasma power. Results show that the HfO_2 layer deposited without plasma is leakier than the PEALD-HfO_2 layer, and the leakage current of the HfO_2 layer increases as the deposition temperature decreases. This means that the lower the deposition temperature and without plasma, the lower the chemical activity of the oxidant form more O-deficient and defective HfO_2 layer.[35-36] Figure 4-2 (c) and (d) show the leakage current of the PEALD-HfO_2 layer depending on the O_2-plasma power at a deposition temperature of 200°C. A more leaky-HfO_2 layer is formed as the O_2-plasma power decrease, but control of the 20W interval does not show a significant difference.

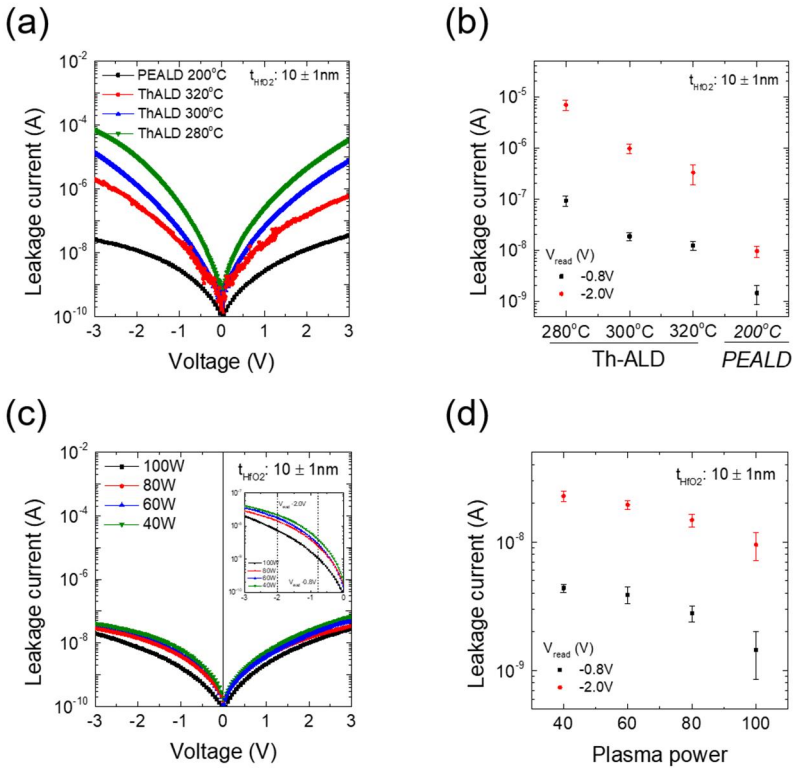


Figure 4-2. MIM leakage-current of HfO_2 layer depending on the deposition conditions, substrate temperature, and O_2-plasma power. (a) and (b) show the leakage results of a PEALD-HfO_2 layer deposited at 200°C, 100W-O_2-plasma power, and a THALD-HfO_2 layer deposited at 280-300°C, 0W-O_2-plasma power. (c) and (d) show the leakage current of the PEALD-HfO_2 layer depending on the O_2-plasma power at a deposition temperature of 200°C

Figure 4-3 shows the transfer curve of the (a) reference-1T (IGZO-TFT), (b) planar structure 1T-1R using stoichiometric PEALD-HfO_2, and (c) planar structure 1T-1R using most O-deficient THALD-HfO_2 (without plasma, 280°C) in Figure 4-2, respectively. Figure 4-3 (d-f) shows the output curve of the device measured in (a-c), respectively. The channel length and -width of each device measured in Figures 4-3 are the same, 0.5μm and 10.0μm, respectively. In figure 4-3 (a), the transfer curve of the reference-1T device shows that the channel is off ($I_{drain} < 10^{-11}$A, V_{drain} 1V) at gate voltage (V_{gate}) -10V, and the channel is on ($I_{drain} >$ 10-5A, V_{drain} 1V) at V_{gate} +20V. The output curve of the reference-1T device in figure 4-3 (d) shows that channel-breakdown is not observed within the drain voltage (V_{drain}) ~+20V, which means that V_{drain} ~±20V can be applied between the source and drains for resistive switching in the HfO_2 resistor. In Figures 4-3 (c) and (f), the degradation of transfer and output behavior is observed in the 1T-1R device with the O-deficient HfO_2 layer. This implies that the IGZO channel is affected by the O-deficiency of the HfO_2 switching layer. The interfacial reaction between the O-deficient HfO_2 and the IGZO-channel layer is expected to cause the carrier density increase in the backchannel. This interfacial reaction between the RS layer and the channel layer will limit material selection and defect-engineering of the RS layer to control switching behavior in the resistor. Unlike 1T-1R device with an O-deficient HfO_2 layer, the transfer and output behavior degradation is not observed in the 1T-1R device with relatively stoichiometric PEALD-HfO_2 layer

in Figure 4-3 (b) and (e). Also, the off-current in figure 4-3 (e) increases as the V_{drain} increases, which means that the contribution of the leakage current through the RS layer appears in the high V_{drain} region.

Figure 4-4 (a) shows the resistive switching behavior of PEALD-HfO_2 deposited 1T-1R with stable channel-on and -off operations. In the measurement, the channel-length and –width (= switching-length and -width) are 0.5μm and 10.0μm, respectively. For the planar-direction resistive switching to the RS layer thickness, DC sweep V_{drain} is applied (0V → 20V →0V → -20V →0V) in the condition of channel-off state by applying V_{gate} -20~-10V (black and red curve in Figure 4-4 (a)). Even though a sufficiently high voltage of V_{drain} ±20V is applied on the RS layer, the volatile-memory (VM) behavior is observed between source and drain electrode (1→2→3→4 arrows in Figure 4-4 (a)). This result is not consistent with the expectation that NVM behavior between source and drain will appear. Also, it is noticed that the output current from the 1T-1R in Figure 4-4 (a) is different depending on the V_{gate}. This can be explained by Figures 4-4 (b) and (c). In the condition of channel-off state (V_{gate} -20~-10V) in Figure 4-4 (b), most of the drain current flows through the HfO_2 resistor because the resistance of the channel layer is very high. Therefore, VM behavior in the resistor is observed (output curve in the condition of V_{gate} -20~-10V in Figure 4-4 (a)). However, in the condition of

channel-on state (V_{gate} 0~20V) in Figure 4-4 (c), some portion of drain current flows through the channel due to the electron accumulation in the channel layer and the resistance of the channel starts to be observed. When the channel is fully turned on, the hysteresis in the HfO_2 resistor is masked by the current flowing through the fully turned on channel (output curve in the condition of V_{gate} 10~20V in Figure 4-4 (a)). From the results of VM behavior of the PEALD-HfO_2 deposited 1T-1R in Figure 4-4, it is confirmed that the switching-length 0.5μm is too large for the HfO_2 resistor to have planar-direction NVM behavior. In order for the resistor to have planar-direction NVM between source and drain electrode, it is conceivable to reduce the length between source and drain down to tens of nm (< 50nm).[34, 39] However, a short-channel of the 1T might be observed in the switching-length scale down because the channel-length and the switching-length are shared, as shown in Figure 4-4 (a). And the interfacial reaction between the channel and resistor, as shown in Figure 4-3 (c), should be prevented for the application of the RS layer with various properties.

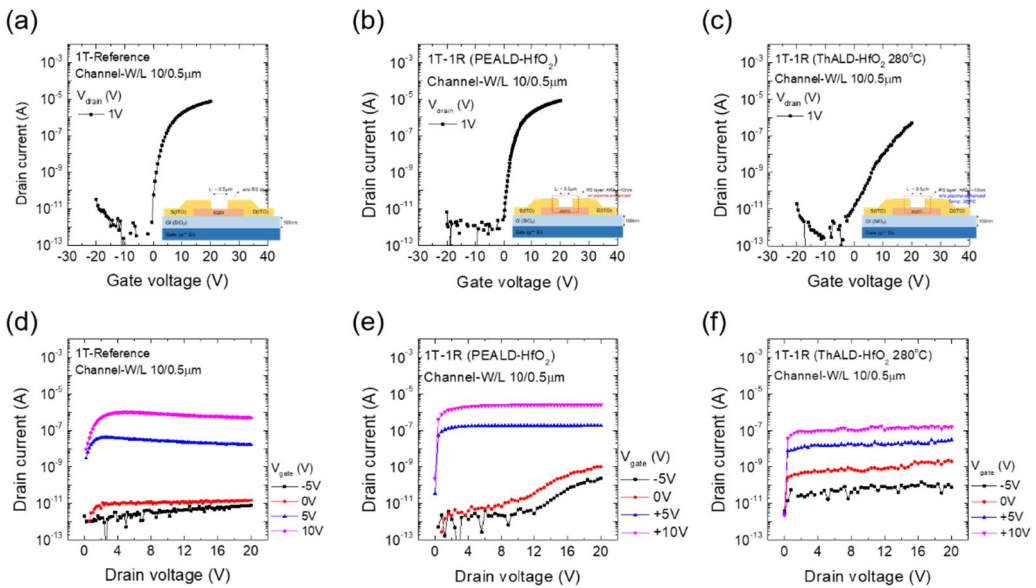


Figure 4-3. The transfer curve of (a) the reference-1T (IGZO-TFT), (b) planar structure 1T-1R using stoichiometric PEALD-HfO_2, and (c) planar structure 1T-1R using most O-deficient THALD-HfO_2 (without plasma, 280°C) in Figure 4-2, respectively. And (d-f) show the output curve of the device measured in (a-c), respectively

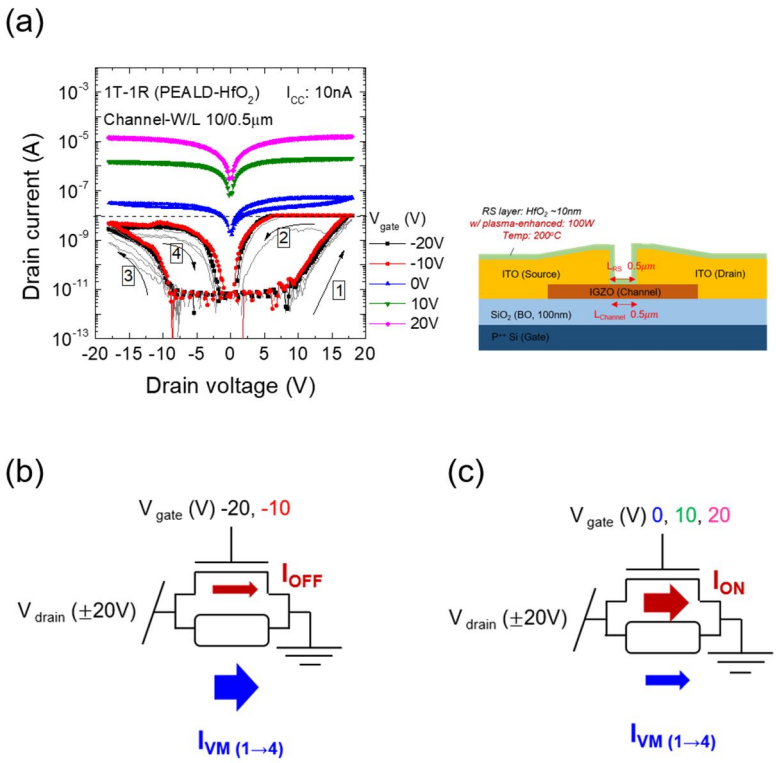


Figure 4-4. (a) The resistive switching behavior of PEALD-HfO_2 deposited 1T-1R with stable channel-on and -off operations. In the measurement the channel-length and -width(= switching-length and -width) are 0.5**μm** and 10.0**μm**, respectively. (b) and (c) show the output current flow of PEALD-HfO_2 deposited 1T-1R device in the case of channel-off and –on state, respectively.

4. 3. 2. Etch-stop-layer (ESL)-type 1T-1R device

To prevent the interfacial reaction between the resistor and channel layer and separate the switching length and channel length, the plasma-enhanced-chemical-vapor-deposition (PECVD)-SiO_2 passivation layer is inserted between the channel and source/drain electrode as shown in Figure 4-5 (b). In the structure shown in Figures 4-5 (b), the channel length and switching length are determined by the length of PECVD-SiO_2 passivation and the pattern distance of the source and drain electrode, respectively. In addition, the interfacial reaction between channel and resistor can be limited by the inserted SiO_2-passivation layer. In the display industry, during the wet-etch process of the indium-tin-oxide (ITO) source and drain electrode, an etch-stop-layer (ESL) is inserted between the channel and electrode due to the low selectivity with IGZO-channel, and this structure is similar to the structure in Figure 4-5 (b).[40-42] So, in the following content, the device structure in Figure 4-5 (b) will be referred to as ESL-type 1T-1R structure. Figure 4-5 (a) shows the fabrication flow of the ESL-type 1T-1R device. The inserted SiO_2 passivation is deposited 100nm using PECVD and dry-etched.

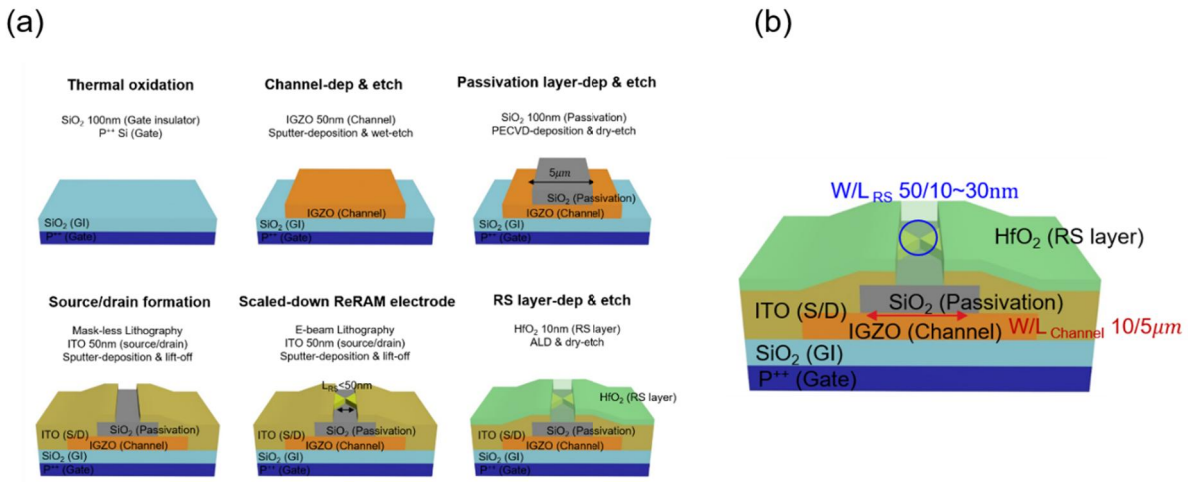


Figure 4-5. (a) The fabrication flow of etch-stop-layer(ESL)-type 1T-1R device. The inserted SiO_2 passivation is deposited 100nm using plasma-enhanced-chemical-vapor-deposition (PECVD) and dry-etched. (b) ESL-type 1T-1R device; the PECVD-SiO_2 passivation layer is inserted between the channel and source/drain electrode. In the structure, the channel length is determined by the length of PECVD-SiO_2 passivation, and switching length is determined by the pattern distance of the source and drain electrode

Figure 4-6 (a) and (b) show transfer behavior of 1T-reference structure (a, channel-length/width 5.0/10.0μm), and SiO_2-passivated 1T-reference structure (b, channel-length/width 5.0/10.0 μm). In this case, channel -length and -width are determined by the pattern distance of source and drain. Figure 4-6 (c) and (d) show transfer behavior of SiO_2-passivated ESL-type 1T structure (c, channel-length/width 5.0/10.0 μm and switching-length/width 0.5/10.0 μm), and SiO_2-passivated ESL-type 1T-1R structure (d, channel-length/width 5.0/10.0 μm and switching-length/width 0.5/10.0 μm), respectively. In this case, channel-length and -width is determined by inserted SiO_2-passivation, and switching-length and -width is determined by pattern distance of source and drain. The inset of Figure 4-6 (a-d) shows the top and cross-section scheme of each device structure, and the most O-deficient HfO_2 layer (deposition temp 280ºC and O_2-plasma power 0W in Figure 4-2 (a)) is used in (d) ESL-type 1T-1R. Through transfer curve analysis of reference-1T and SiO_2-passivated reference-1T devices in Figure 4-6 (a) and (b), it is verified that the PECVD-SiO_2 passivation layer rarely affects the IGZO-channel layer. It can also be seen that the on-current is slightly increased, and sub-threshold swing (S.S) is deteriorated in the SiO_2-passivated 1T device compared to the reference-1T. It is expected to come from the increased carrier concentration in the channel due to the hydrogen contamination during the SiO_2-PECVD process or the decreased charged defect (-OH) on the back-channel[43-45], but it rarely affects this work. Figures 4-6 (b) and (c) show no significant difference in the transfer

curve between SiO_2-passivated reference-1T and SiO_2-passivated ESL-type 1T. The results imply that channel-length and switching-length are physically independent, and the PECVD-SiO_2 passivation determines channel-length. Through transfer curve comparison between ESL-type 1T and ESL-type 1T-1R devices in Figure 4-6 (c) and (d), it is affirmed that the O-deficient HfO_2 and IGZO-channel layer are chemically separated by the PECVD-SiO_2 passivation, and the interfacial reaction is completely restricted.

Figure 4-7 (a) and (b) show the current and voltage (I-V) curve of SiO_2-passivated ESL-type 1T device in the condition of channel-off state (V_{gate} -10V). In the measurement, V_{drain} ±20V and ±40V are applied between source and drain electrode to check whether the resistive switching is observed in the inserted SiO_2-passivation. As a result of analysis of more than ten devices, there is no noticeable resistive switching behavior, with only the charging and discharging between the source and drain observed, as shown in Figures 4-7 (a) and (b). Figures 4-7 (c) and (d) show the I-V curve of SiO_2-passivated ESL-type 1T-1R in the condition of channel-off state (V_{gate} -10V), and V_{drain} ±20V and ±30V are applied between source and drain, respectively. Unlike the ESL-type 1T device in Figure 4-7 (b), VM behavior between source and drain appears by applying V_{drain} over ±20V, and the current gradually increases with repeated switching as shown in Figure 4-7 (d). Through comparison with the I-V results of the ESL-type 1T device, resistive switching is observed in the HfO_2 resistor, not in the SiO_2-passivation or IGZO-channel layer. In the condition of

interfacial reaction between the channel and resistor is restricted, it is expected that NVM behavior would be more easily observed in the V_O-rich THALD-HfO_2 layer, but volatile-switching is observed. Compared to previously reported general ReRAM devices in which resistive switching occurs in the thickness-direction, more than V_{drain} ±300V must be applied for the switching-length 0.5μm device to have stable NVM behavior.[39] Therefore, the switching length is scaled-down under 30nm using an e-beam lithography process to apply sufficient electric field to the resistor and observe stable NVM behavior.

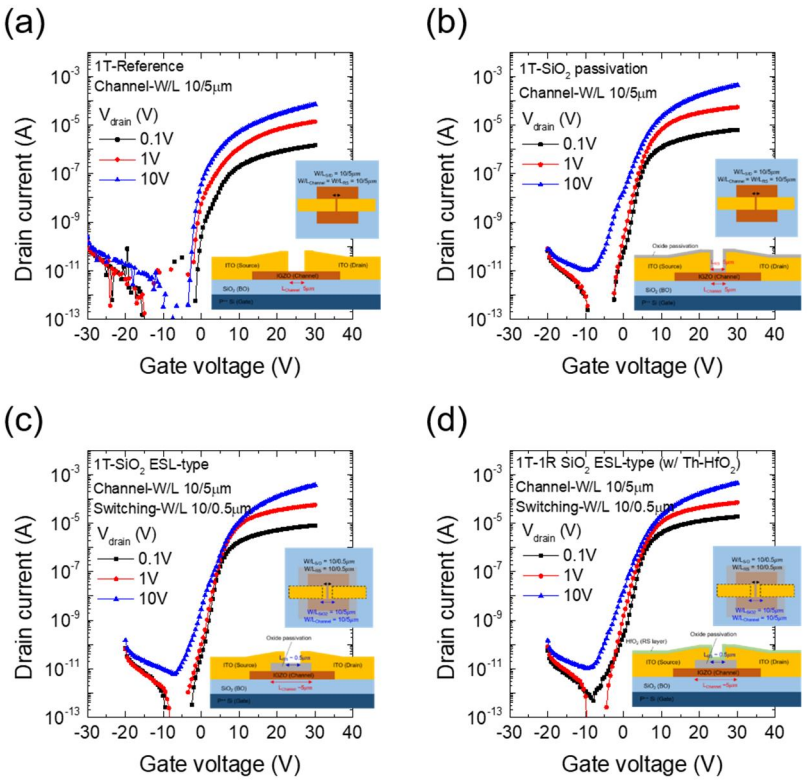


Figure 4-6. The transfer behavior of 1T-reference structure (a, channel-length/width 5.0/10.0**μm**), SiO_2-passivated 1T-reference structure (b, channel-length/width 5.0/10.0 **μm**). The transfer behavior of SiO_2-passivated ESL-type 1T structure (c, channel-length/width 5.0/10.0 **μm** and switching-length/width 0.5/10.0 **μm**), and SiO_2-passivated ESL-type 1T-1R structure (d, channel-length/width 5.0/10.0 **μm** and switching-length/width 0.5/10.0 **μm**), respectively. The inset shows the top and cross-section scheme of each device structure.

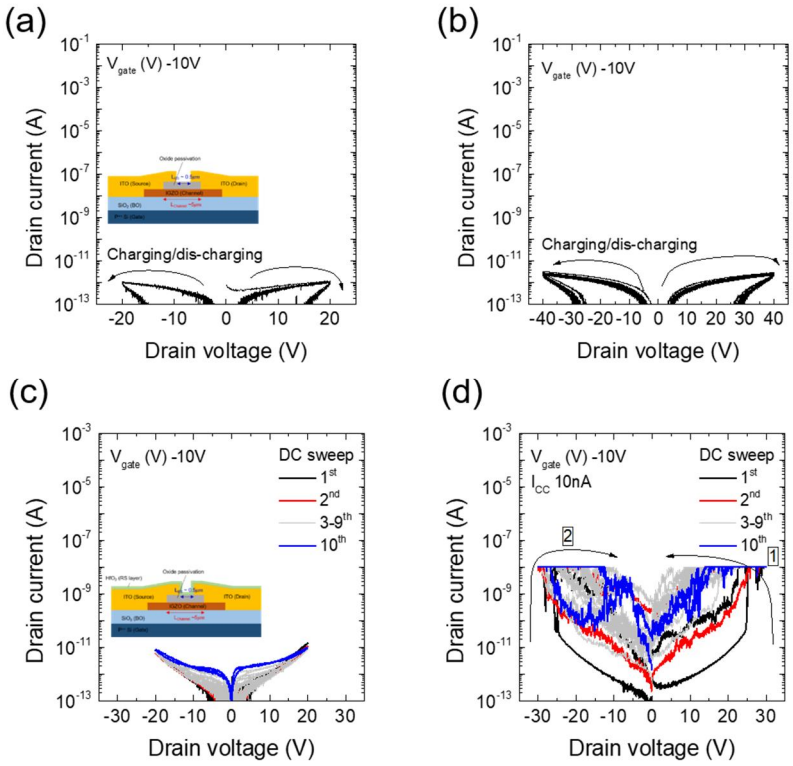


Figure 4-7. The I-V curve of SiO_2-passivated ESL-type 1T device in the condition of channel-off state (V_{gate} -10V). In the measurement, V_{drain} **±20V** and **±40V** are applied between the source and drain electrode as shown in (a) and (b). The I-V curve of SiO_2-passivated ESL-type 1T-1R in the condition of channel-off state (V_{gate} -10V) and V_{drain} **±20V** and **±30V** are applied between source and drain as shown in (c) and (d), respectively.

4. 3. 3. Scaled-1R and NVM switching characteristics

Before merging 1T and scaled-1R devices, a scaled-1R single device is fabricated to confirm the planar-direction NVM behavior to the RS layer. Figure 4-8 (a) and (b) show the I-V curve of scaled-1R devices using PEALD-HfO_2 (deposition temp 200°C, O_2-plasma power 100W) and O-deficient THALD-HfO_2 (deposition temp 280°C, O_2-plasma power 0W), respectively. Figure 4-8 (c) shows SEM top view image and scheme of scaled-1R, and each device has 20nm and 50nm of switching-length and -width, respectively. The scaled-1R should have resistive switching within 50μA of operating current considering the compatibility with 1T as previously explained in Figure 4-1 (a). In the case of the scaled-1R with a relatively insulating PEALD-HfO_2 resistor, the device is electroformed at ~1.6V under the condition of compliance current (I_{CC}) 1μA and switched to LRS as shown in Figure 4-8 (a blue curve). Subsequently, the device is reset at ~-0.8V and switched from LRS to HRS. It is essential to form asymmetric-V_O distribution in HfO_2 resistor through electroforming process for repetitive NVM behavior considering the symmetric-1R structure. 1μA is the minimum current level to form a stable conduction path in the scaled-1R with PEALD-HfO_2 switching layer. After the stable forming-1st reset process, planar-direction NVM behavior (1→2→3→4 arrows in Figure 4-8 (a)) between source and drain is observed, in which the device is set at ~1.2V (black curve) and reset at ~-0.8V (red curve) under the

condition of I_{CC} 3μA. From the comparison of the current flowing the pristine device (blue curve) and the current flowing HRS device after electroforming-1st reset (black curve) in Figure 4-8 (a), an asymmetric-V_O distribution in the HfO_2 resistor is expected to form during the electroforming process. On the other hand, in the case of the scaled-1R with O-deficient THALD-HfO_2 switching layer in Figure 4-8 (b), it is impossible to form a stable conduction path in the HfO_2 switching layer even if the I_{CC} is increased to 10μA or more due to the leakage current through the as-fabricated device. In addition, the results of Figures 4-4 (b) and (c) confirm that the PEALD-HfO_2 switching layer rarely affects the channel compared to the O-deficient HfO_2. Considering the vertical-TFT-ReRAM structure where it is difficult to insert a passivation layer, a less O-deficient PEALD-HfO_2 switching layer will be more suitable. Figure 4-8 (d) shows resistance change according to switching number of scaled-1R with PEALD-HfO_2 in the condition of I_{CC} 3μA, V_{set} ~1.2V, and V_{reset} ~-0.8V and the non-volatile resistive switching is repeated up to 50 times. Figure 4-8 (e) shows the LRS and HRS retention performance of the scaled-1R device with PEALD-HfO_2 in the condition of constant V_{read} (0.2V) stress at 298K. From the retention performance in which both LRS and HRS are maintained up to ~10^4s, it is confirmed that the resistive switching behavior in Figure 4-8 (a) is non-volatile. Figure 4-8 (f) shows the closed-loop-pulsed-switching (CLPS) operation result of the scaled-1R device with PEALD-HfO_2. The CLPS operation, similar to the incremental-step-pulse-programming (ISPP) in

NAND-flash operation, switches the ReRAM device according to the target resistance value with the program and verify method. In the case of LRS, if the resistance verified after the program is lower than the target resistance, it is judged as SET. And if the target resistance is not reached, the pulse height increases, and the SET pulse is applied again. Conversely, in the case of HRS, if the verified resistance is higher than the target resistance, it is judged to have been RESET. If the target resistance is not reached, the RESET pulse is applied again by increasing the pulse height in the RESET polarity. The CLPS analysis of the scaled-1R device confirmed that resistive switching is stable when operated in a target resistance range of 5M ~ 100Mohm. When the target LRS and HRS are set to 5Mohm and 100Mohm, respectively, it shows that repeated switching over 100,000 times is possible.

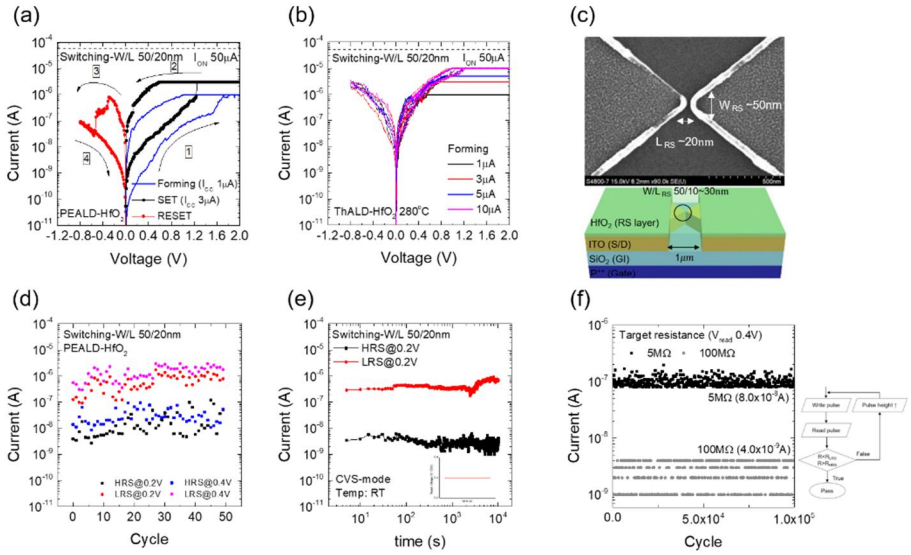


Figure 4-8. The I-V curve of scaled-1R devices using (a) PEALD-HfO_2 and (b) O-deficient THALD-HfO_2, respectively. (c) SEM top view image and scheme of scaled-1R, and each device has 20nm and 50nm of switching-length and -width, respectively. (d) The resistance change according to switching number of scaled-1R with PEALD-HfO_2 in the condition of I_{CC} 3**μA**, V_{set} ~1.2V, and V_{reset} ~-0.8V. (e) The retention performance of scaled-1R device with PEALD-HfO_2 at 298K

4. 3. 4. Data-based Cell-string number simulation

Figure 4-9 (a) shows the overlapped curve of the output curve of ESL-type 1T in Figure 4-6 (c) and I-V curve of scaled-1R in Figure 4-8 (a) to find out the compatibility of 1T and scaled-1R devices. The results in Figure 4-9 (a) confirm that the current range of the LRS and HRS state of scaled-1R is well covered by the current range of the channel-on and -off state of ESL-type 1T. It means that the resistance relation of 1-transistor and 1-resistor is satisfied for stable operation in merged structure 1T-1R. Based on the experimental data of 1T and 1R devices, cell-string number simulation is performed in Figure 4-9 (b) and (c) considering the worst case in both reads and write operations as shown in Figure 4-9 (d) and (e), respectively. For the cell-string number simulation, the resistive-switching behavior of scaled-1R is fitted as shown in Figure 4-9 (a) blue curve. In the case of HRS, it is well fitted by the ohmic conduction model at low voltage (< 0.2V) region and hopping conduction model at high voltage (> 0.2V) region in both set and reset curves. In the case of LRS, it is well fitted by the ohmic conduction model at low voltage (< 0.4V) region and hopping conduction model at high voltage (> 0.4V) region in both set and reset curves. Figure 4-9 (b) shows the read current (at $V_{BL,\ read}$ 0.4V) of the selected device flowing through bit-line (BL) depending on the cell-string number in the worst case of the read operation in Figure 4-9 (d). The black and red curves show the read current flowing through BL when the resistor of the selected device is HRS and LRS, respectively. The worst case of reading operation

occurs when the voltage drop of BL is the smallest in the selected device compared to the un-selected devices, as shown in Figure 4-9 (d). When the $V_{BL,\ read}$ for a read operation of the selected device is 0.4V, the read current flowing through the resistor of the selected device decreases in both LRS and HRS as the cell-string number increases according to the following equation (1).

$$I_{selected} = \frac{V_{BL,read}}{R_{LRS\ or\ HRS}+(N-1)R_{ON}} \quad (R_{HRS} \gg R_{ON}) \qquad (1)$$

$$\frac{V_{BL,read}}{R_{LRS}+(N-1)R_{ON}} = \frac{V_{BL,read}}{R_{HRS}+(N-1)R_{ON}} \cong \frac{V_{BL,read}}{R_{HRS}} \qquad (2)$$

$$N \cong \frac{R_{HRS} - R_{LRS}}{R_{ON}} \qquad (3)$$

Equation (1) confirmed that the read current flowing BL decreases sharply when the resistor of the selected device is LRS compared to HRS. The read margin of the resistor decreases and the cell-string number is limited as the cell-string number increases according to equations (2) and (3). The results of Figure 4-9 (b) suggest that the BL current window is maintained ~4.5 times for 200 cell-strings and ~3.0 times for 500 cells, which means that more than 180 cell-strings of the current V-NAND-flash is possible in the point of view read operation. Figure 4-9 (c) shows the programming voltage of BL for resistive switching in the resistor of the selected device depending on the cell-string number considering the worst case of the write operation in Figure 4-9 (e). The black and red curves show the BL programming voltage for set and reset operations, in which the resistor of the selected device is HRS and LRS,

respectively. The worst case of write operation occurs when the voltage drop of BL is the smallest in the selected device, as shown in Figures 4-9 (e). The programing voltage on BL for the stable resistive switching in the resistor of the selected device increases as the cell-string number increases according to the following equation (4) and (5).

$$V_{BL,reset} = V_{reset} \times \left(1 + \frac{R_{ON}}{R_{LRS}} N\right) \text{ <reset operation>} \quad (4)$$

$$V_{BL,set} = V_{set} \times \left(1 + \frac{R_{ON}}{R_{HRS}} N\right) \text{ <set operation>} \quad (5)$$

Equations (4) and (5) show that the BL programming voltage increases rapidly in the reset operation of the selected device in the LRS state compared to the set operation of the selected device in the HRS state. In Figure 4-9 (c), assuming 200 cell-string numbers, the BL programming voltage for the set and reset operation of the selected resistor are 6.7V and -7.7V, respectively, which are within the programming voltage of the current V-NAND-flash. However, to replace the current commercialized V-NAND-flash and occupy the storage-memory portion in the memory hierarchy, the cell-string number of 180 or more must be considered along with power consumption. In the transistor, it is possible to increase the cell-string number from both reads and write operation points of view and decrease the BL programming voltage for resistive switching in the resistor by reducing the channel-on resistance according to the equations (3-5). In addition, the gate voltage -10V and +20V for device selection

operation in Figure 4-9 (a) are still too high, so it must be reduced by increasing gate-controllability for channel-on/off. In the case of the resistor, it is possible to reduce power consumption from the program point of view by applying a more stoichiometric RS layer and increasing the LRS and HRS according to the equation (4) and (5). To control the O-deficiency of atomic layer deposited HfO_2, deposition temperature control, doping, post-annealing treatment in an oxygen atmosphere, etc., have been applied in several researches.[36-38] However, if the O-deficiency in the resistor is excessively reduced, it is difficult to have a resistive switching behavior in the resistor, and operating voltage might be increased. Therefore, considering these factors, the defect-engineering of the resistive-switching layer will play an essential role in future V-TFT-ReRAM research for replacing the current V-NAND-flash.

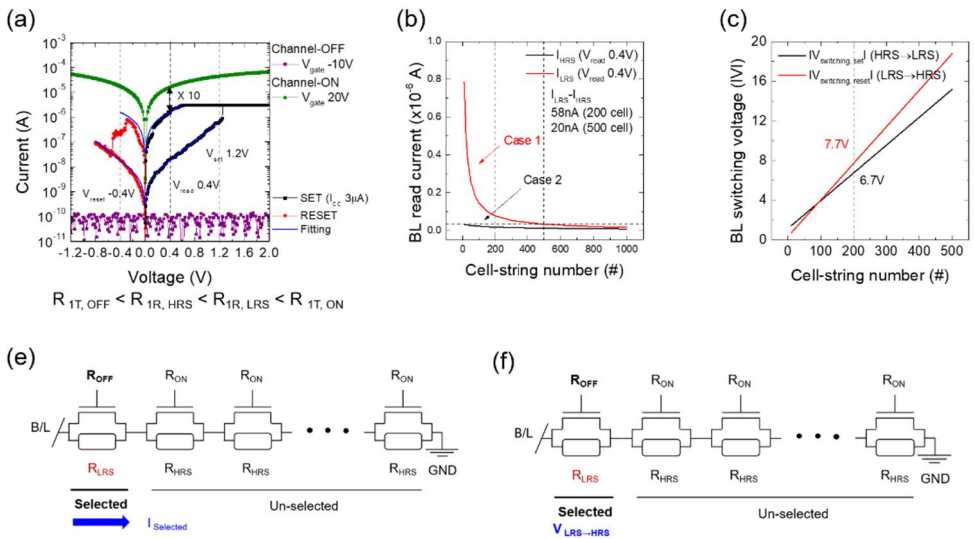


Figure 4-9. (a) The overlapped curve of output curve of ESL-type 1T and I-V curve of scaled-1R. (b) The read current (at $V_{BL,\,read}$ 0.4V) of selected device flowing through bit-line (BL) depending on the cell-string number in the worst case of the read operation in (d). (c) The programming voltage of BL for resistive-switching in the resistor of the selected device depending on the cell-string number considering the worst case of the write operation in (e).

4.4. Conclusion

As prior research to the next-generation vertical-string 1T-1R array (V-TFT-ReRAM) for replacing V-NAND-flash, the HfO_2-based planar structure 1T-1R device was examined. Since the fabrication variable that can control the resistive switching behavior was limited to the properties of the RS layer because of the inherently symmetric device structure, it was essential to engineer the defect like oxygen vacancy (V_O) in the resistor to obtain the planar-direction NVM behavior and compatibility with 1T. From the MIM leakage current analysis of HfO_2 deposited under different ALD conditions, it was confirmed that the defect properties of HfO_2 can be controlled by deposition conditions like substrate temperature and O_2-plasma power. Next, the large-scale 1T-1R with HfO_2 resistor was investigated, in which the most stoichiometric PEALD-HfO_2 and the most O-deficient THALD-HfO_2 were used. In the large-scale 1T-1R investigation, several issues were observed; interfacial reaction between the channel and O-deficient HfO_2 resistor and scale down restriction due to sharing of channel-length and switching-length. These were solved by inserting PECVD-SiO_2 passivation between the channel and source/drain electrode. For the planar-direction NVM behavior between source and drain electrode, scaled-1R with a 20nm of switching-length using e-beam lithography process was evaluated. In the scaled-1R with stoichiometric PEALD-HfO_2, repetitive planar-direction NVM behavior was observed, and compatibility with 1T for stable operation in merged 1T-1R was achieved.

Finally, it was realized that more than 200 cell-string of 1T-1R is possible as a result of the experimental data-based cell-string number simulation. From this work, it was shown that the atomic-layer-deposited HfO_2 layer could be applied as a resistor layer in the V-TFT-ReRAM field and the defect-engineering of the resistor is still essential for the future V-TFT-ReRAM research to occupy storage-memory beyond V-NAND-flash device.

4.5. References

(1) Waser, R.; Dittmann, R.; Staikov, G.; Szot, K. Redox-Based Resistive Switching Memories – Nanoionic Mechanisms, Prospects, and Challenges, *Adv. Mater*. **2009**, *21*, 2632–2663.

(2) Fukuzumi, Y.; Matsuoka, Y.; Kito, M.; Kido, M.; Sato, M.; Tanaka, H.; Nagata, Y.; Iwata, Y.; Aochi, H.; Nitayama, A. Optimal Integration and Characteristics of Vertical Array Devices for Ultra-High Density, Bit-Cost Scalable Flash Memory, Proc. *IEEE Int. Electron Devices Meeting*, Washington, DC, USA. 10-12 Dec. 2007.

(3) Asenov, A.; Brown, A. R.; Davies, J. H.; Kaya, S.; Slavcheva, G. Simulation of intrinsic parameter fluctuations in decananometer and nanometer-scale MOSFETs, *IEEE Trans. Electron Devices.* **2003**, *50*, 1837.

(4) Lee, S. H.; Zhu, X.; Lu, W. D. Nanoscale resistive switching devices for memory and computing applications, *Nano Res*. **2020**, *13*, 1228–1243.

(5) Taur, Y.; Buchanan, D. A.; Chen, W.; Frank, D. J.; Ismail, K. E.; Lo, S. H.; Sai-Halasz, G. A.; Viswanathan, R. G.; Wann, H. -J. C.; Wind, S. J. CMOS scaling into the nanometer regime, *Proc. IEEE*. **1997**, *85*, 486–504.

(6) Frank, D. J.; Dennard, R. H.; Nowak, E.; Solomon, P. M.; Taur, Y.; Wong, H. -S. P. Device scaling limits of Si MOSFETs and their application dependencies. *Proc. IEEE*. **2001**, *89*, 259–288.

(7) Khan, H. N.; Hounshell, D. A.; Fuchs, E. R. H. Science and research policy at the end of Moore'S law. *Nat. Electron*. **2018**, *1*, 14–21.

(8) Tanaka, H.; Kido, M.; Yahashi, K.; Oomura, M.; Katsumata, R.; Kito, M.; Fukuzumi, Y.; Sato, M.; Nagata, Y.; Matsuoka, Y.; Iwata, Y.; Aochi, H.;

Nitayama, A. Bit cost scalable technology with punch and plug process for ultra high density flash memory, *Proc. IEEE Symp. VLSI Technol*. Kyoto, Japan. 12-14 Jun. 2007.

(9) Kim, C.; Kim, D. –H,; Jeong, W.; Kim, H. –J,; Park, I. H.; Park, H. –W.; Lee, J.; Park, J.; Ahn, Y. –L.; Lee, J. Y. A 512-Gb 3-b/Cell 64-Stacked WL 3-D-NAND Flash Memory, *IEEE J. Solid-State Circuit*. **2018**, *53* 7669-7676.

(10) Omura, M.; Hashimoto, J.; Adachi, T.; Kondo, Y.; Ishikawa, M.; Abe, J.; Sakai, I.; Hayashi, H.; Sekine, M.; Hori, M. Formation mechanism of sidewall striation in high-aspect-ratio hole etching, *Jpn. J. Appl. Phys*. **2019**, *58*, SEEB02.

(11) Sakamori, S.; Fujiwara, N.; Miyatake, H.; Oikawa, K.; Yamanaka, M.; Sasaki, T. Transformation of Dense Contact Holes during SiO_2 Etching, *Jpn. J. Appl. Phys*, **2003**, *42* 3962.

(12) Izawa, M.; Negishi, N.; Yokogawa, K.; Momonoi, Y. Investigation of Bowing Reduction in SiO_2 Etching Taking into Account Radical Sticking in a Hole, *Jpn. J. Appl. Phys*, **2007**, *46* 7870.

(13) Miyake, M., Negishi, N.; Izawa, M.; Yokogawa, K.; Oyama, M.; Kanekiyo, T. Effects of Mask and Necking Deformation on Bowing and Twisting in High-Aspect-Ratio Contact Hole Etching, *Jpn. J. Appl. Phys*, **2009**, *48* 08HE01.

(14) Kim, J. K.; Lee, S. H.; Cho, S. I.; Yeom, G. Y. Study on contact distortion during high aspect ratio contact SiO_2 etching, *J. Vac. Sci. Technol. A*, **2015**, *33*, 021303.

(15) Negishi, N.; Miyake, M.; Yokogawa, K.; Oyama, M.; Kanekiyo, T.; Izawa, M. Bottom profile degradation mechanism in high aspect ratio feature etching based on pattern transfer observation, *J. Vac. Sci. Technol. B*, **2017**, *35*, 051205.

(16) Yoon, K. J.; Kim, Y.; Hwang, C. S. What Will Come After V-NAND—Vertical

Resistive Switching Memory?, *Adv. Electron. Mater*. **2019**, 1800914.

(17) Kinoshita, M.; Sasago, Y.; Minemura, H.; Anzai, Y.; Tai, M.; Fujisaki, Y.; Kusaba, S.; Morimoto, T.; Takahama, T.; Mine, T.; Shima, A.; Yonamoto, Y.; Kobayash, T. Scalable 3-D vertical chain-cell-type phase-change memory with $4F^2$ poly-Si diodes, *IEEE/Symp. on VLSI Tech Digest of Technical Papers*, Honolulu, HI, USA, 12-14 June 2012.

(18) Hwang, E. S.; Kim, J. S.; Jeon, S. M.; Lee, S. J.; Jang, Y.; Cho, D. –Y.; Hwang, C. S. $In_2Ga_2ZnO_7$ oxide semiconductor based charge trap device for NAND flash memory, *Nanotechnology*, **2018**, *29*, 155203.

(19) Kim, S. M.; Song, E. B.; Lee, S.; Zhu, J.; Seo, D. H.; Mecklenburg, M.; Seo, S.; Wang, K. L. Transparent and Flexible Graphene Charge-Trap Memory, *ACS Nano*, **2012**, *6*, 9, 7879–7884.

(20) Seok, J. Y.; Song, S. J.; Yoon, J. H.; Yoon, K. J.; Park, T. H.; Kwon, D. E.; Lim, H.; Kim, G. H.; Jeong, D. S.; Hwang, C. S.; A Review of Three-Dimensional Resistive Switching Cross-Bar Array Memories from the Integration and Materials Property Points of View, *Adv. Funct. Mater*. **2014**, *24*, 5316–5339.

(21) Ziegler, M. M.; Stan, M. R. Design and analysis of crossbar circuits for molecular nanoelectronics, *Proceedings of the 2nd IEEE Conference on Nanotechnology*, Washington, DC, USA, 2002.

(22) Kang, B. S.; Ahn, S. –E.; Lee, M. –J.; Stefanovich, G.; Kim, K. H.; Xianyu, W. X.; Lee, C. B.; Park, Y.; Baek, I. G.; Park, B. H. High-Current-Density CuO x/InZnOx Thin-Film Diodes for Cross-Point Memory Applications, *Adv. Mater*, **2008**, *20*, 3066–3069.

(23) . Lee, M. –J.; Kim, S. I.; Lee, C. B.; Yin, H.; Ahn, S. –E.; Kang, B. S.; Kim, K. H.; Park, J. C.; Kim, C. J.; Song, I.; Kim, S. W.; Stefanovich, G.; Lee, J. H.;

Chung, S. J.; Kim, Y. H.; Park, Y. Low-Temperature-Grown Transition Metal Oxide Based Storage Materials and Oxide Transistors for High-Density Non-volatile Memory, *Adv. Funct. Mater*, **2009**, *19*, 1587–1593.

(24) Park, W. Y.; Kim, G. H.; Seok, J. Y.; Kim, K. M.; Song, S. J.; Lee, M. H.; Hwang, C. S. A $Pt/TiO_2/Ti$ Schottky-type selection diode for alleviating the sneak current in resistance switching memory arrays, *Nanotechnology*, **2010**, *21*, 195201.

(25) Kim, K. M.; Zhang, J.; Graves, C.; Yang, J. J.; Choi, B. J.; Hwang, C. S.; Li, Z.; Williams, R .S. Low-Power, Self-Rectifying, and Forming-Free Memristor with an Asymmetric Programing Voltage for a High-Density Crossbar Application, *Nano Lett*. **2016**, *16*, 11, 6724–6732.

(26) Yoon, J. H.; Song, S. J.; Yoo, I. –H.; Seok, J. Y.; Yoon, K. J.; Kwon, D. E.; Park, T. H.; Hwang, C. S. Highly Uniform, Electroforming-Free, and Self-Rectifying Resistive Memory in the $Pt/Ta_2O_5/HfO_{2-x}/TiN$ Structure, *Adv. Funct. Mater*. **2014**, *24*, 5086–5095.

(27) Bai, Y.; Wu, H.; Wu, R.; Zhang, Y.; Deng, N.; Yu, Z.; Qian, H. Study of Multi-level Characteristics for 3D Vertical Resistive Switching Memory, *Sci Rep 4*, **2014**, 5780.

(28) Wong, H. -S. P.; Lee, H. –Y.; Yu, S.; Chen, Y. –S.; Wu, Y.; Chen, P. –S.; Lee, B.; Chen, F. T.; Tsai, M. –J. Metal-Oxide RRAM, *Proc. IEEE*, **June 2012**, *100*, 1951-1970.

(29) Wilk, G. D.; Wallace, R. M.; Anthony, J. M. High-k gate dielectrics: Current status and materials properties considerations, *J. Appl. Phys.*, **2001**, *89*, 5243.

(30) Lee, H. Y.; Chen, P. S.; Wu, T. Y.; Chen, Y. S.; Wang, C. C.; Tzeng, P. J.; Lin, C. H.; Chen, F.; Lien, C. H.; Tsai, M. –J. Low power and high speed bipolar

switching with a thin reactive Ti buffer layer in robust HfO_2 based RRAM, San Francisco, CA, USA, *2008 IEEE International Electron Devices Meeting*, 2008.

(31) Chen, Y. ReRAM: History, Status, and Future, *IEEE Trans. Electron Devices*, **2020**, *67*, 1420.

(32) Kim, Y.; Kwon, Y. J.; Kwon, D. E.; Yoon, K. J.; Yoon, J. H.; Yoo, S.; Kim, H. J.; Park, T. H.; Han, J. –W.; Kim, K. M.; Hwang, C. S. Nociceptive Memristor, *Avd. Mater*. **2018**, *30*, 1704320.

(33) Park, T. H.; Kwon, Y. J.; Kim, H. J.; Woo, H. C.; Kim, G. S.; An, C. H.; Kim, Y.; Kwon, D. E.; Hwang, C. S. Balancing the Source and Sink of Oxygen Vacancies for the Resistive Switching Memory, *ACS Appl. Mater. Interfaces*. **2018**, *10*, 21445-21450.

(34) Kim, G. S.; Song, H.; Lee, Y. K.; Kim, J. H.; Kim, W.; Park, T. H.; Kim, H. J.; Kim, K. M.; Hwang, C. S. Defect-Engineered Electroforming-Free Analog HfO_x Memristor and Its Application to the Neural Network, *ACS Appl. Mater. Interfaces*. **2018**, *11*, 47063-47072.

(35) Kwon, J. –D.; Lee, J. –W.; Nam, K. –S.; Kim, D. –H.; Jeong, Y.; Kwon, S. –H.; Park, J. –S. The impact on in-situ-hydrogen-plasma treatment for zinc oxide plasma enhanced atomic layer deposition, *Curr. Appl. Phys*. **2012**, *12*, 134-138.

(36) Morgan, K.; Huang, R.; Pearce, S.; De Groot. C. H. The effect of atomic layer deposition temperature on switching properties of HfO_x resistive RAM devices, *IEEE Int. Symp. Circuits Syst (ISCAS)*. Melbourne, Australia. Jun. 2014.

(37) Regoutz, A.; Gupta, I.; Serb, A.; Khiat, A.; Borgatti, F.; Lee, T. –L.; Schiueter, C.; Torelli, P.; Gobaut, B.; Light, M.; Carta, D.; Pearce, S.; Panaccione, G.; Prodromakis, T. Role and Optimization of the Active Oxide Layer in TiO_2-based RRAM, *Adv. Funct. Mater*. **2016**, *26*, 507-513.

(38) Das, K. C.; Tripathy, N. Ghosh, S. P.; Mohanta, S. K.; Nakamura, A.; Kar, J. P. Investigation of microstructural and electrical properties of composition dependent co-sputtered $Hf_{1-x}Ta_xO_2$ thin films, *Mater. Res. Express*. **2017**, *4*, 114007.

(39) Park, T. H.; Song, S. J.; Kim, H. J.; Kim, S. G.; Chung, S.; Kim, B. Y.; Lee, K. J.; Kim, K. M.; Choi, B. J.; Hwang, C. S. Thickness-dependent electroforming behaviro of ultra-thin Ta_2O_5 resistance switching layer, *Phys. Status Solidi RRL*. **2015**, *9*, 362-365.

(40) Koretomo, D.; Toda, T.; Matsuda, T.; Kimura, M.; Furuta, M. Anomalus Increase in Field-Effect Mobility in In-Gz-Zn-O Thin-film Transistors Caused by Dry-Etching Damage Through Etch-Stop Layer, *IEEE Trans. Electon Devices*. **2016**, *63*, 2785-2789.

(41) Nag, M.; Steudel, S.; Bhoolokam, A.; Chasin, A.; Rockele, M.; Myny, K.; Mass, J.; Fritz, T.; Trube, J.; Groeseneken, G.; Heremans, P. High performance a-IGZO thin-film transistors with mf-PVD SiO_2 as an etch-stop-layer, *J. Soc. Inf. Disp*. **2014**, *22*, 23-28.

(42) Li, X.; Xin, E.; Chen, L.; Shi, J.; Zhang, J. Effect of etching stop layer on characteristics of amorphous IGZO thin film transistor fabricated at low temperaure, *API Adv*. **2013**, *3*, 032127.

(43) Noh, H. Y.; Kim, J.; Kim, J. –S.; Lee, M. –J.; Lee, H. –J. Role of Hydrogen in Active Layer of Oxide-Semiconductor-Based Thin Film Transistors, *Crystals*. **2019**, *7*, 75.

(44) Cho, D. H.; Yang, S. H.;, Shin, J. –H.; Byun, C. W.; Ryu, M. K.; Lee, J. I.; Hwang, C. S.; Chu. H. Y. Passivation of Bottom-Gate IGZO Thin Film Transistors, *J. Korean Phys. Soc*. **2009**, *54*, 531-534.

(45) Jeong, S. –G.; Jeong, H. –J.; Choi, W. –H.; Kim, K. R.; Park, J. –S. Hydrogen Impacts of PEALD InGaZnO TFTs Using SiO_x Gate Inulators Deposited by PECVD and PEALD, *IEEE Tans. Electon Devices*. **2020**, *67*, 4250-4255.

5. Conclusion

In this dissertation, the defect-engineering of atomic-layer-deposited HfO_2 resistive switching layer was investigated to improve resistive switching performance and achieve planar-direction resistive switching behavior for neural network and V-TFT-ReRAM (1T-1R) applications. Through the systematic analysis, the retention failure model was identified in the ultra-thin HfO_2 and improved by the defect (V_O)-control in the RS layer. The electroforming-free behavior was achieved by HfO_2-thickness and V_O-control utilizing the RuO_2 bottom electrode. The switching uniformity and the synaptic behavior were highly improved in the electroforming-free device. These results elucidate the applicability of the defect-engineered HfO_2-based ReRAM to neural network computing. Furthermore, as prior research to the V-TFT-ReRAM, the HfO_2-based planar structure 1T-1R device was investigated. In the scaled-1R with PEALD-HfO_2, repetitive planar-direction NVM behavior was observed, and compatibility with 1T for the stable operation was achieved. These results demonstrated that the defect-engineered HfO_2 layer could be applied as a resistor in the V-TFT-ReRAM studies.

In the first part of the study, the retention behaviors of a HfO_2-based ReRAM device with an ultra-thin (1 nm) HfO_2 RS layer were investigated. Unlike the reported retention failure phenomenon, in the 1-nm-thick HfO_2 ReRAM device, both the LRS and HRS currents increased at a certain time,

which induced retention failure. The retention tests in both the CVS and non-CVS modes confirmed that the reset process is the critical step that causes the retention failure of the device. Through the analysis of the conductance-voltage relationship, it was confirmed that the increase of the V_O concentration in the RS oxide layer during the retention test period induces retention failure. The pristine device has an integral portion of the V_O-enriched region near the Ta electrode, whose border with the V_O-free region is recessed from the original position towards the Ta top electrode during the reset process. This recessed region recovers the original location during the retention test period as it is thermodynamically more stable, which can induce the reconnection of the broken conducting filament. This is further facilitated by the increased V_O concentration within the CF and non-electroformed regions in the memory cell. Even at the LRS, which is achieved by the sequential operation of the electroforming, reset, and set processes, the cell current becomes higher after the retention failure due to the strengthening of the CF by the moving back of the border to the original position. The EF-only device did not show a sudden increase in current. As the main reason for the involvement of such unwanted effect is the overall increase in V_O concentration within the memory cell, the adoption of a V_O sink layer such as RuO_2 as the counter electrode of the V_O-source Ta electrode may improve the retention performance.

On the basis of the switching behavior and the similar material stack of structure in the first part, the ReRAM device using the PEALD-grown HfO_2

thin film as the switching layer was optimized by V_O-control in the RS layer through electrode replacement ($TiN \rightarrow RuO_2$) to use the memory cell as an analog-type synapse in the neuromorphic circuit. Most problems of the ReRAM cell to be used as a feasible synapse, such as high non-linearity, high asymmetry in potentiation and depression, low repeatability and uniformity of the switching performance, and low retention, are related to the uncontrolled formation and rupture of the CFs. Such a problem appeared to be closely related to the electroforming process, which inevitably induced the uncontrollable formation of the CFs. Therefore, electroforming-free ReRAM was necessary, which could fundamentally be achieved by thinning the PEALD-grown HfO_2 film from (4.5 to 3.0) nm. However, for such a thin film, the adoption of RuO_2 bottom electrode, replacing the convention TiN bottom electrode, was essential. Otherwise, the 3.0 nm-thick film showed too high a leakage current to be used as a feasible memory. The optimized $Ta/HfO_2/RuO_2$ stack provided the desirable performances for it to be used as a feasible synapse with improved linearity and symmetry factors. The PEALD HfO_2 film was initially oxygen-deficient, which was actually a prerequisite to induce a useful level of leakage current for it to be used as a feasible ReRAM when it was thicker than ~4.5 nm. The portion of the HfO_2 film in contact with the RuO_2 bottom electrode recovered the stoichiometric composition, making the interface layer highly insulating but still thin enough to achieve electroforming-free performances. These results demonstrated that defect engineering such as V_O in the RS layer

plays an essential role in improving the switching performance of oxide ReRAM devices and the applicability of HfO_2-based synapse devices to neuromorphic applications.

On the other hand, the attention to V-TFT-ReRAM devices has increased as an effort to overcome the limitations of the CBA structure for high-density ReRAM array and replace currently commercialized V-NAND-flash devices. As prior research to the V-TFT-ReRAM for replacing V-NAND-flash, the HfO_2-based planar structure 1T-1R device was investigated. However, there were several issues. First, in the ReRAM research, the repetitive NVM behavior in the planar-direction rather than the thickness-direction in the RS layer had not been reported yet. Second, even if the NVM behavior is observed in the RS layer, it is difficult to achieve compatibility between the resistor and the transistor operations. Third, because of the inherently symmetric structure, the switching behavior cannot be controlled by electrode material selection or bilayer structure as in general ReRAM research. Since the fabrication variable that can control the resistive switching behavior was limited to the properties of the RS layer because of the inherently symmetric device structure, it was essential to engineer the defect like V_O in the resistor to obtain the planar-direction NVM behavior and compatibility with 1T. From the MIM leakage current analysis of HfO_2 deposited under different ALD conditions, it was confirmed that the defect properties of HfO_2 can be controlled by deposition conditions like substrate temperature and O_2-plasma power. Next, the large-

scale 1T-1R with HfO_2 resistor was investigated, in which the most stoichiometric PEALD-HfO_2 and the most O-deficient THALD-HfO_2 were used. In the large-scale 1T-1R investigation, several issues were observed; interfacial reaction between the channel and O-deficient HfO_2 resistor and scale down restriction due to sharing of channel-length and switching-length. These were solved by inserting PECVD-SiO_2 passivation between the channel and source/drain electrode. For the planar-direction NVM behavior between source and drain electrode, scaled-1R with a 20nm of switching-length using e-beam lithography process was evaluated. In the scaled-1R with stoichiometric PEALD-HfO_2, repetitive planar-direction NVM behavior was observed, and compatibility with 1T for stable operation in merged 1T-1R was achieved. Finally, it was realized that more than 200 cell-string of 1T-1R is possible as a result of the experimental data-based cell-string number simulation. From this work, it was shown that the atomic-layer-deposited HfO_2 layer could be applied as a resistor layer in the V-TFT-ReRAM field and the defect-engineering of the resistor is still essential for the future V-TFT-ReRAM research to occupy storage-memory beyond V-NAND-flash device.

This thesis presents a deeper understanding of the defect-engineering of the ALD deposited HfO_2 switching layer and a pathway to achieve the improved and desired switching performance. Even though the HfO_2-based ReRAM is still far from the replacement of the currently commercialized V-NAND-flash device and the adoption as a universal memory, the results in this

thesis could shed light on this field by suggesting new pathways different from the conventional approach.

Abstract (in Korean)

저항 변화 메모리 (ReRAM)은 단순한 구조, 고집적 가능성, 저전력 및 고속 동작, 우수한 신뢰성 그리고 CMOS 호환성으로 차세대 비-휘발성 메모리 (NVM)로 많은 관심을 받고있다. 다양한 재료, 소자 후보 중 금속 산화물 기반 ReRAM은 지난 수십 년 동안 메커니즘 분석 및 소자 적용을 위해 연구되어왔다. 화학적, 구조적, 그리고 전기적 특성 분석을 통해 산소 결손 (oxygen vacancy, V_O)으로 구성된 전도성 필라멘트의 반복된 성장 및 소멸이 ReRAM 소자의 저항 변화 현상을 유발하는 것을 밝혔다. 한편, HfO_2 박막은 ReRAM 분야에서 연구되고 있는 재료 중 하나로 V_O로 구성된 전도성 필라멘트에 의한 저항 변화 메커니즘이 소자 스위칭 현상을 나타낸다. 하지만 재료적 특성의 이해, 공정 프로세스의 개선에도 불구하고 ReRAM 소자의 불충분한 retention 및 non-uniformity와 같이 ReRAM 소자의 상용화 발목을 잡는 극복해야할 많은 문제들이 존재한다. 이때, HfO_2 박막 기반 ReRAM 소자에서 저항 스위칭에 관여하는 전도성 필라멘트는 V_O로 구성되어 있기 때문에 스위칭 특성을 개선하고 원하는 저항 변화 거동을 확보하기 위해서 저항 변화 층 내 V_O를 제어하는 연구가 필요하다.

본 연구에서는 먼저 초박형 HfO_2 저항 변화 층이 적용된 HfO_2 기반 ReRAM 소자의 비정상적인 retention 거동을 분석하고 열화 메커니즘을 설명한다. 이때 저항 변화 층으로는 열-원자 층 증착 방식 (ALD)을 통해 성장한 1nm 두께의 HfO_2 박막을 사용하였다. 분석에 사용된 소자는 SK 하이닉스 시설의 제조 기술을 이용하여 직경 300mm 웨이퍼에 집적되었다. 분석에 사용된 초박형 HfO_2 기반 ReRAM 소자의 경우, 다른 두꺼운 산화물 기반 ReRAM에서 보고되는 retention 열화 거동과 다르게 특정 시간에 저 저항 (LRS) 및 고 저항 (HRS) 상태의 전류가 증가하는 형태로 retention 열화가

나타났다. 각 프로그램 과정을 거친 소자에 대한 retention 분석을 통해 reset 과정의 개입이 초박형 HfO_2 기반 ReRAM 소자의 retention 열화를 유발하는 것을 확인하였다. 또한 pristine 소자는 Ta/HfO_2 계면 사이에 V_O가 풍부한 영역을 포함하는데, V_O가 풍부한 영역과 V_O가 부족한 영역 사이의 경계 위치가 소자 retention 성능을 제어하는데 중요한 역할을 한다. 이 경계선은 reset 단계에서 소자에 가해진 외부 전압에 의해 Ta 전극 쪽으로 이동하지만, 외부 전압이 해제되거나 약한 retention 기간 동안 원래의 안정한 위치로 다시 되돌아온다. 그 결과 끊어진 전도성 필라멘트가 다시 연결되거나 이미 연결된 필라멘트의 약한 부분이 강화되며 retention 열화 현상이 나타난다. 마지막으로 retention 열화 거동의 온도 의존성 분석을 통해 retention 열화 거동의 활성화 에너지 0.15eV를 도출하였으며, 이는 중성 V_O의 이온화 에너지와 관련이 있는 것을 확인하였다.

앞선 연구를 통해 규명된 소자의 스위칭 메커니즘 및 유사한 재료 구조를 기반으로 Ta/HfO_2/RuO_2 ReRAM 소자에 대한 연구를 진행하였다. Ta/HfO_2/RuO_2 ReRAM 소자를 synapse로 활용한 완전 연결 신경망 시스템을 구성하여 흑백 문자 식별 (MNIST data set) 시험의 성능 향상을 도모하였다. 이전 연구를 참고하여 최적화 된 Ta 상부 전극 및 RuO_2 하부 전극 증착 조건이 소자 제작에 적용되었다. 이때, HfO_2 저항 변화 층 두께는 ~3.0nm로 증착되었으며, 이는 electroforming-free 동작을 갖기 충분히 얇지만 소자 저항 변화를 위한 on-off 비율을 유지하기에 충분히 두꺼운 두께이다. Electroforming-free 소자와 비교를 위해 유사한 구조의 HfO_2 두께 ~4.5nm 소자가 함께 제작되었으며 해당 소자의 경우 안정적 저항 변화 거동을 위해 electroforming 과정이 필요하다. 또한 기준 소자로 Ta/HfO_2 (~4.5nm)/TiN ReRAM 소자도 함께 제작하여 각 소자의 스위칭 특성을 비교하였다. 분석 결과 electroforming-free 거동을

갖는 최적화 된 Ta/HfO_2/RuO_2 ReRAM 소자가 가장 개선된 retention 거동 및 스위칭 uniformity 특성을 나타냈다. 또한 향상된 아날로그 스위칭 동작과 synapse 성능을 갖는 것을 확인하였다. 각 TiN, RuO_2 전극 기판 위에 증착 된 HfO_2 박막의 화학적 분석을 통해, 최적화 된 electroforming-free Ta/HfO_2 (~3.0nm)/RuO_2 ReRAM 소자 동작 특성 개선 원인에 대한 단서를 확인하였으며 각 소자 스위칭 모델을 제시하였다. 마지막으로 실험적으로 확보한 HfO_2 기반 synapse 소자의 신경 연결 potentiation, depression 곡선 결과와 컴퓨터 시뮬레이션 모델링을 통해 뉴로모픽 신경망 모사 연구를 진행하였다. 분석 결과 개선된 synapse 거동을 보이는 electroforming-free Ta/HfO_2 (~3.0nm)/RuO_2 ReRAM 소자에서 가장 높은 MNIST data set 인식 정확도를 갖는 것을 확인하였다. 이는 저항 변화 층 내 V_O와 같은 결함 설계가 ReRAM 소자의 동작 특성 개선에 중요한 역할을 한다는 것을 보여줌과 동시에 HfO_2 기반 synapse 소자의 뉴로모픽 신경망 모사 적용 가능성을 보여준 결과이다.

한편, V-NAND flash 소자를 대체하기 위한 후보로 V-TFT-ReRAM으로 명명되는 수직 연결 1T-1R 어레이가 많은 관심을 받고 있다. 본 연구에서는 차세대 V-TFT-ReRAM 소자에 대한 선행 연구로 HfO_2 기반 평면 구조 1T-1R 소자에 대한 연구를 진행하였다. 본질적으로 대칭적인 소자 구조로 인해 저항 변화를 제어할 수 있는 공정 변수가 저항 변화 층 물성으로 제한되기 때문에 저항 변화층 내 V_O와 같은 결함 설계를 통한 NVM 거동 확보 및 트랜지스터와 호환성을 확보하는 연구가 선행되어야 한다. 먼저 ALD 증착 조건에 따른 HfO_2 박막의 MIM 구조 누설 전류 평가를 통해 HfO_2 박막의 결함 특성이 증착 시 기판 온도 및 산화제의 O_2-플라즈마 전력과 같은 증착 조건에 의해 조절될 수 있음을 확인하였다. 다음으로 PEALD 방식으로 증착된 화학양론적 HfO_2 박막과 THALD 방식으로 증착된 산소 결핍 HfO_{2-x} 박막이 저항

변화 층으로 적용된 1T-1R 소자에 대한 분석을 진행하였으나, 비-휘발성 (NVM)이 아닌 휘발성 메모리 (VM) 거동이 관찰되었다. 소스-드레인 전극 간 평면 방향의 NVM 거동을 위해 이빔-리소그래피 공정을 적용하여 스위칭 길이를 20nm로 축소하였고 축소화-1R 소자에 대한 평가를 진행하였다. 분석 결과 PEALD 방식으로 증착된 HfO_2 박막이 적용된 축소화-1R 소자에서 평면 방향의 반복적 NVM 거동이 관찰되었으며, 병합된 1T-1R 구조에서 안정적 동작을 위한 트랜지스터 소자와 호환성을 만족하는 것을 처음으로 확인하였다. 마지막으로 실험 데이터 기반 소자-연결 시뮬레이션을 진행하였으며, 200개 이상 1T-1R 소자-연결이 가능한 것을 확인하였다. 이는 V-TFT-ReRAM 연구에서 V_O와 같은 결함 설계를 통한 ALD 방식 증착 HfO_2 박막의 저항 변화 층으로 적용 가능성을 보여주는 결과이다.

주요어: 저항 변화 메모리, ReRAM, 전도성 필라멘트, 저항 스위칭, 산소 결손, V_O, HfO_2, 원자 층 증착, 저 저항 상태, 고 저항 상태, electroforming, retention, 산포, non-uniformity, synapse, potentiation, depression, 뉴로모픽 신경망, MNIST, 수직 소자, 비-휘발성 메모리

학 번: 2017 – 23054

김 길 섭