Ph.D. Dissertation

12.8 kHz Energy-Efficient Read-Out IC for High Precision Bridge Sensor Sensing System

고 정밀 브리지 센서 감지 시스템을 위한 12.8 kHz 고 효율 판독 회로

by

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Department of Electrical Engineering and
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이 논문을 공학박사 학위논문으로 제출함

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ABSTRACT

12.8 kHz Energy-Efficient Read-Out IC for High Precision Bridge Sensor Sensing System

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In the thesis, a high energy-efficient read-out integrated circuit (read-out IC) for a high-precision bridge sensor sensing system is proposed. A low-noise capacitively-coupled chopper instrumentation amplifier (CCIA) followed by a high-resolution incremental discrete-time delta-sigma modulator (DTΔΣM) analog-to-digital converter (ADC) is implemented. To increase energy-efficiency, CCIA is chosen, which has the highest energy-efficiency among IA types. CCIA has a programmable gain of 1 to 128 that can amplify the small output of the bridge sensor. Impedance boosting loop (IBL) is applied to compensate for the low input impedance, which is a disadvantage of a CCIA. Also, the sensor offset cancellation technique was applied to CCIA to eliminate the offset resulting from the

resistance mismatch of the bridge sensor, and the bridge sensor offset from -350 mV to 350 mV can be eliminated. In addition, the output data rate of the read-out IC is designed to be 12.8 kHz to quickly capture data and to reduce the power consumption of the sensor by turning off the sensor and read-out IC for the rest of the time. Generally, bridge sensor system is much slower than 12.8 kHz. To suppress 1/f noise, system level chopping and correlated double sampling (CDS) techniques are used. Implemented in a standard 0.13-μm CMOS process, the ROIC's effective resolution is 17.0 bits at gain 1 and that of 14.6 bits at gain 128. The analog part draws the average current of 139.4 μA from 3-V supply, and 60.2 μA from a 1.8 V supply.

Keywords: Smart device, capacitively-coupled chopper instrumentation amplifier (CCIA), wheatstone bridge sensor, 1/*f* noise, system-level chopping, incremental delta-sigma analog-to-digital converter (ADC), sensor offset cancellation, Impedance boosting.

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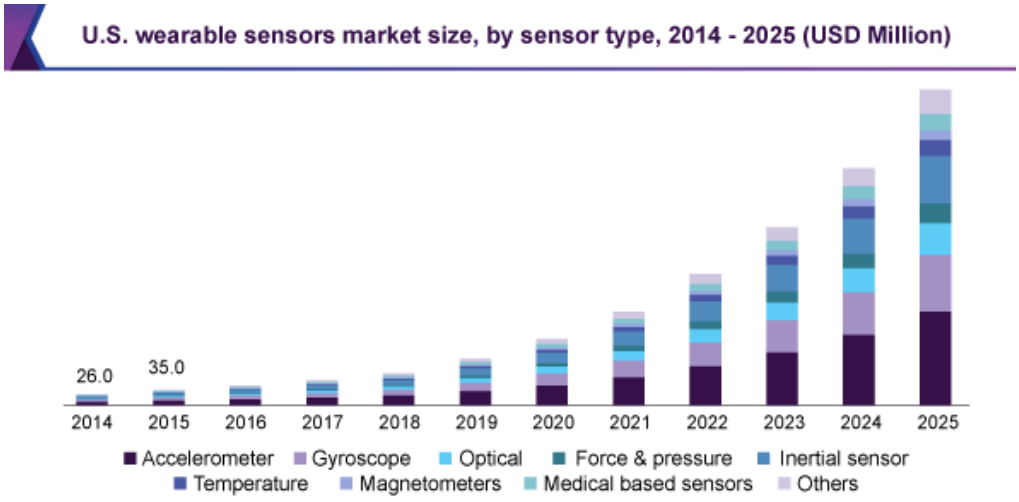
CHAPTER 1

INTRODUCTION

1.1 SMART DEVICES

Fig. 1.1.1 Various sensors in smart phone.

As time goes on, more types of sensors are being installed in small electronic devices such as cell phones. And these sensors allow one small electronic device to be used in various ways and become a means of enhancing competitiveness. Fig. 1 shows countless sensors in one electronic device. The sensors are proximity sensor, Ambient light sensor,



Source: Grand View Research, 2018

Fig. 1.1.2 Forecast of growth in wearable device market.

CMOS imager sensors, GPS sensor, Accelerometer, humidity sensor, temperature sensor, force & pressure sensor, fingerprint sensor, magnetometer, gyroscope, touch sensor, and etc. as shown in Fig. 1.1.1. A typical small electronic device using various sensors is a smartphone. Smart device sensors are built into these devices to improve usability, controllability and manageability. Smartphones are an amazing feat of engineering. Six of more gadgets are packed into a single slab, and many of the coolest functions are performed by a variety of sensors. For example, accelerometers handle axis-based motion detection and can be found on cell phones as well as fitness trackers. These accelerometers are the reason why you can track your steps on your smartphone without having to purchase a separate wearable. The gyroscope helps the accelerometer understand the phone's

orientation. It adds another level of precision to make your 360-degree light sphere look as impressive as possible. In addition, it measures the vertical speed of elevators, pedestrians climbing stairs, and drones using a smartphone pressure sensor. Also, the pressure sensor can remove physical buttons in the smartphone. Therefore, various smart sensors built into smartphones allow you to do many things with one electronic device. Fig. 2 shows the market size of the wearable devices. In 2016, the global wearable sensor market size was valued at USD 149.3 million. Sensors are an important aspect of wearable devices used by consumers due to the growing interest in real-time motion detection activity tracking. This has the potential to boost industry growth during the forecast period. The growing number of health and fitness monitoring applications worldwide is driving the market forward. As we can see above, small smart electronic devices are equipped with numerous smart sensors, and their demand is expected to surge.

1.2 SMART SENSOR SYSTEMS

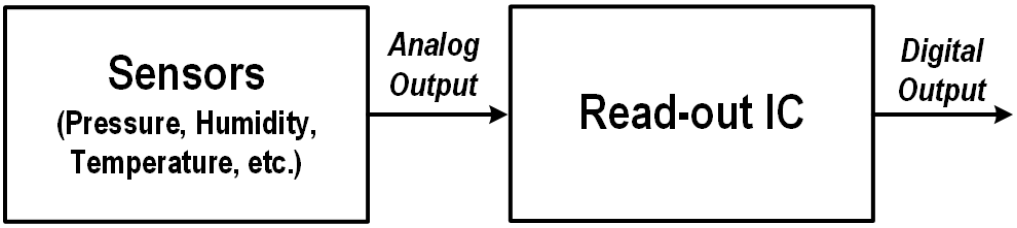


Fig. 1.2.1 Smart sensor systems.

Since most sensors installed in smart devices output analog signals, a suitable read-out Integrated Circuit (IC) is needed to convert analog signals into digital signals for each sensor as shown in Fig. 1.2.1. The converted digital signal is processed by the Microcontroller Unit (MCU). Since there are many sensors and read-out ICs in a small smart device, increasing their power efficiency is one the most important issues.

1.3 WHEATSTONE BRIDGE SENSOR

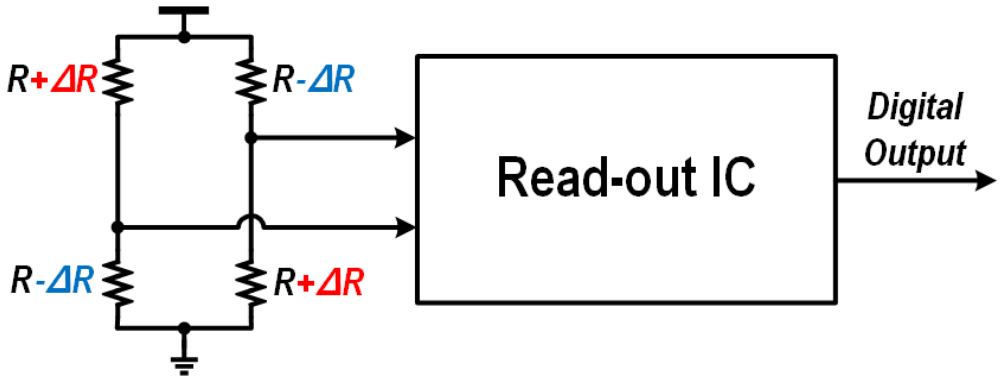


Fig. 1.3.1 Bridge sensor system.

Fig. 1.3.1 shows a Wheatstone Bridge sensor followed by a read-out IC. Because of sensor's simplicity, stability and accuracy, the Wheatstone Bridge sensor is still widely used to measure resistance [1.3.1]-[1.3.3]. Wheatstone Bridge sensors are often used to detect physical quantities such as pressure, force, temperature, and magnetic fields through their effect on resistances of the sensor [1.3.4]-[1.3.6]. Fig. 1.3.2 shows the types of the Wheatstone Bridge Sensors.

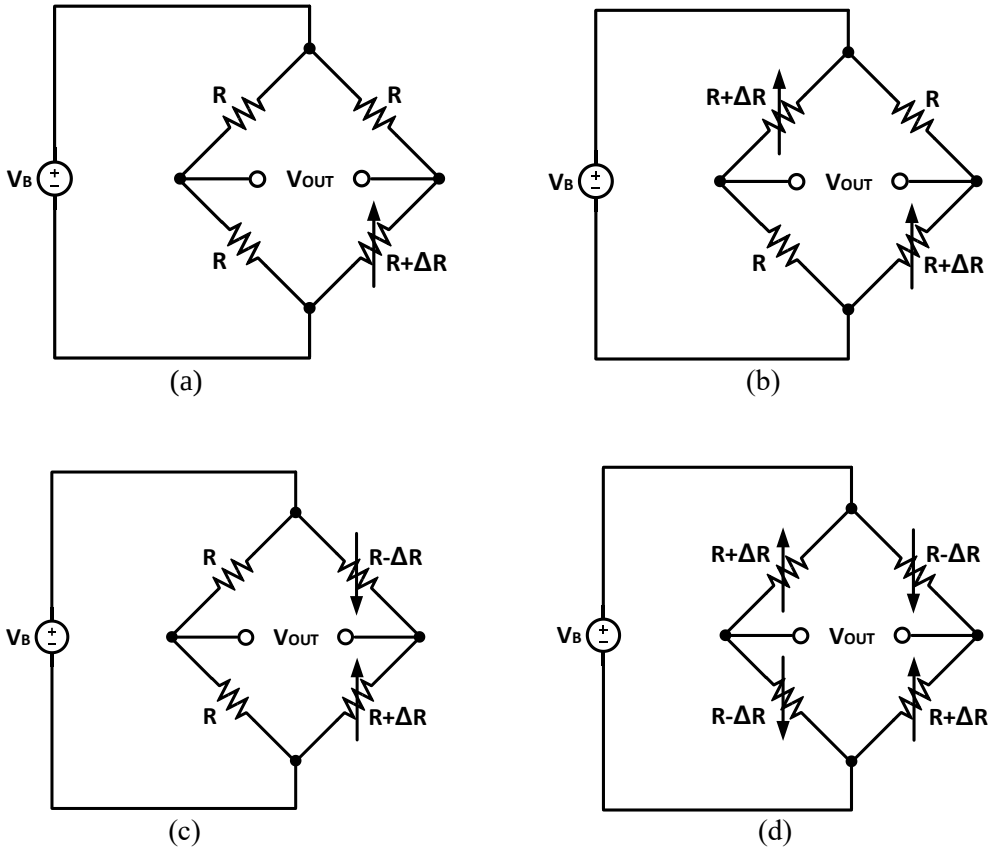


Fig. 1.3.2 Types of Wheatstone bridge sensors [1.3.8].

Figure 1.3.2 (a) is a single-element varying type. The single resistance changes by force or pressure. The resistance changes yield V_{OUT} changes.

$$V_{OUT} = \frac{V_B}{4}\left(\frac{\Delta R}{R + (\frac{\Delta R}{2})}\right) \tag{1.1}$$

Because of the mismatch of the resistors, the linearity error is approximately 0.5 %. Fig. 1.3.2 (b) is the type of two-element varying. The linearity error is same as 1.3.2 (a) but the sensitivity is improved by a factor of two comparing with 1.3.2 (a). Fig. 1.3.2 (c) is also the type of two-element varying. The linearity error is almost zero and the sensitivity is improved by a factor of two comparing with Fig. 1.3.2 (a). Fig. 1.3.3 (d) is the type of four-element varying. The linearity error is almost zero and the sensitivity is improved by a factor of four comparing with Fig. 1.3.2 (a) and it has the best performance but usually more expensive than others.

1.4 MOTIVATION

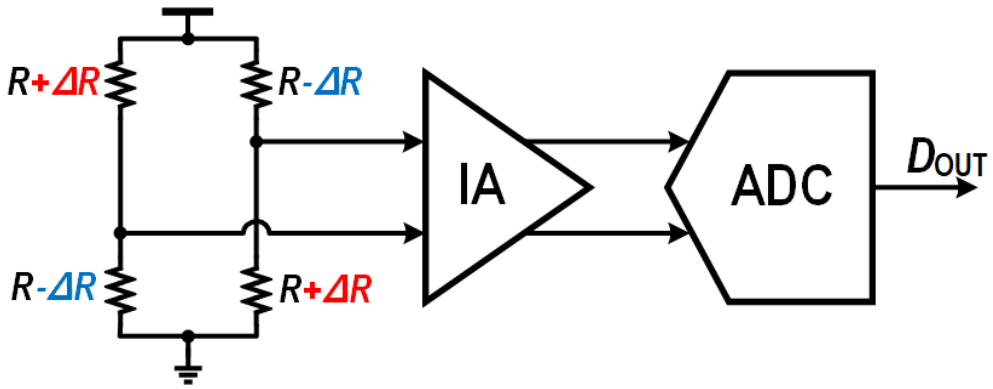


Fig. 1.4.1 Typical block diagram of a bridge-to-digital converter.

Fig. 1.4.1 shows the simplified block diagram of a bridge sensor system. A bridge sensor converts a change in sensor resistance into a digital signal using a read-out IC when a force or pressure is applied to the sensor. In general, a read-out IC consists of an instrumentation amplifier (IA) and an analog-to-digital Converter (ADC) [1.3.3]. Since the output signal of the sensor is small, a programmable gain IA is required to amplify the sensor's output signal, and the IA needs to have a large input impedance to prevent signal loss. In the case of ADC, since the output of the force sensor is DC, a low-bandwidth, high-resolution ADC is generally used [1.4.1].

As we have mentioned in section 1.2, reducing power consumption of a bridge sensor system is crucial in a small smart device. In the case of force sensor system, static

current flows in both the force sensor and the read-out IC. Therefore, the total power consumption of the bridge sensor system can be reduced in the read-out IC or in the sensor. For this purpose, many papers have been researched.

1.5 PREVIOUS WORKS

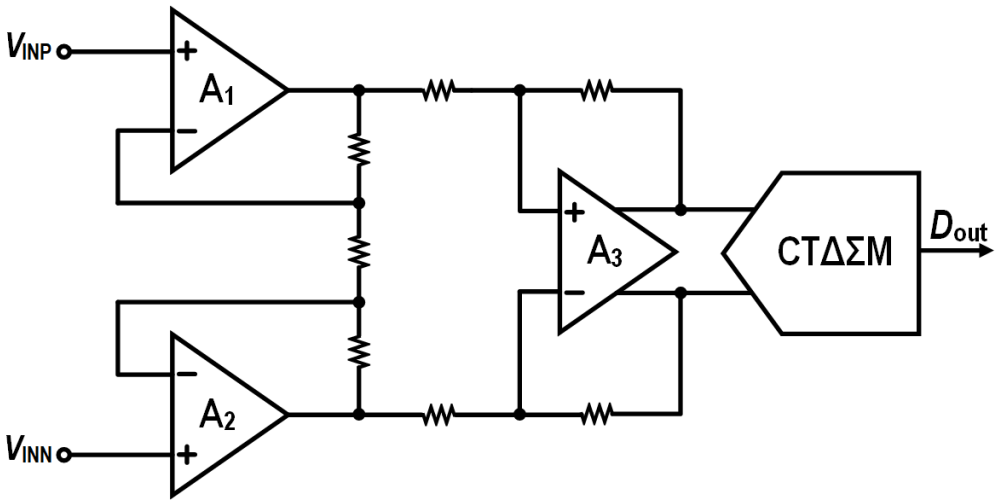


Fig. 1.5.1 Block diagram of the three-opamp IA topology [1.3.4].

Fig. 1.5.1 shows three-opamp topology followed by a continuous delta-sigma ADC [1.3.4]. The three-opamp is the oldest structure among IA types and is the most traditionally used to read resistance type sensors, especially in commercial products. It has an outstanding linearity and has high input impedance. However, the power efficiency is poor because of two low-noise amplifiers. Also, it is hard to achieve bridge sensor's rail-to-rail sensing. In other words, cannot lower bridge sensor's supply voltage to reduce sensor's static power consumption.

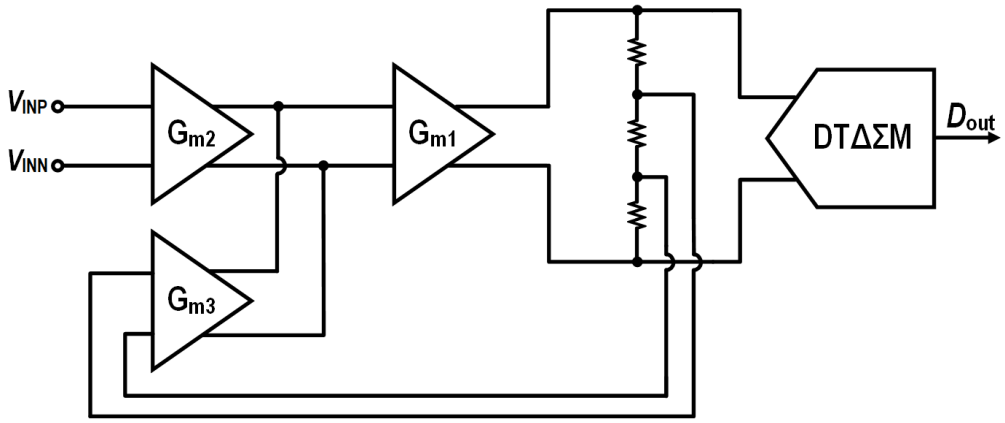


Fig. 1.5.2 Block diagram of the CFIA topology [1.5.1].

Fig. 1.5.2 shows another topology of IAs, Current feedback IA (CFIA), followed by a discrete-time delta-sigma ADC [1.5.1], [1.5.2]. It has high input impedance and it has better power efficiency than three-opamp topology. Also, it has a capability of bridge sensor's rail-to-rail sensing. However, because of the mismatch between the input and feedback transconductances, or because of the resistor mismatch, the gain accuracy is limited. Accordingly, external resistor trimming is required. Also, in addition, achieving both rail-to-rail sensing capability and the high gain accuracy is quite challenging because the mismatch between the input and feedback transconductors is a function of the input CM voltage [1.3.7]. Also, the power efficiency better than three-opamp topology, it is still limited by two input and feedback transonductances. Fig. 1.5.3 shows the simplified block diagram of Capacitively-Coupled Chopper Insturmentation Amplifier (CCIA) [1.3.7], [1.5.3] followed by a discrete-time delta-sigma ADC. CCIA is being researched most

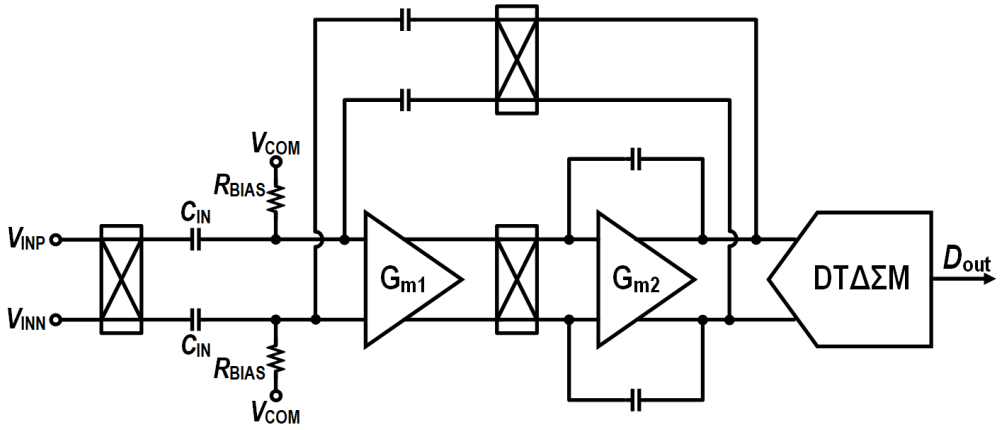


Fig. 1.5.3 Block diagram of the CCIA topology [1.3.7].

actively in recent years due to its high power efficiency [1.5.4], [1.5.5]. The noise of a CCIA is determined by one amplifier [1.3.7], so that the energy efficiency is higher than the three-opamp IA and CFIA. Also, CCIA has the advantage of being suitable for easy use of rail-to-rail sensing without any special techniques because C_{IN} blocks the DC signal. However, the reason why research is active despite high energy efficiency is because the CCIA still suffers from several drawbacks such as low input impedance, output ripples, and output spikes at its chopping transitions [1.3.7], [1.5.5].

On the other hand, in [1.3.2], they emphasized that it is important to lower the sensor's supply voltage to reduce the power consumption of the bridge sensor system. They mention that, recently, many bridge sensors are low impedance devices, complicating the low power design. The surest way to minimize bridge sensor system's power consumption is to limit the drive to the bridge sensor. For instance, if the supply voltage of the bridge

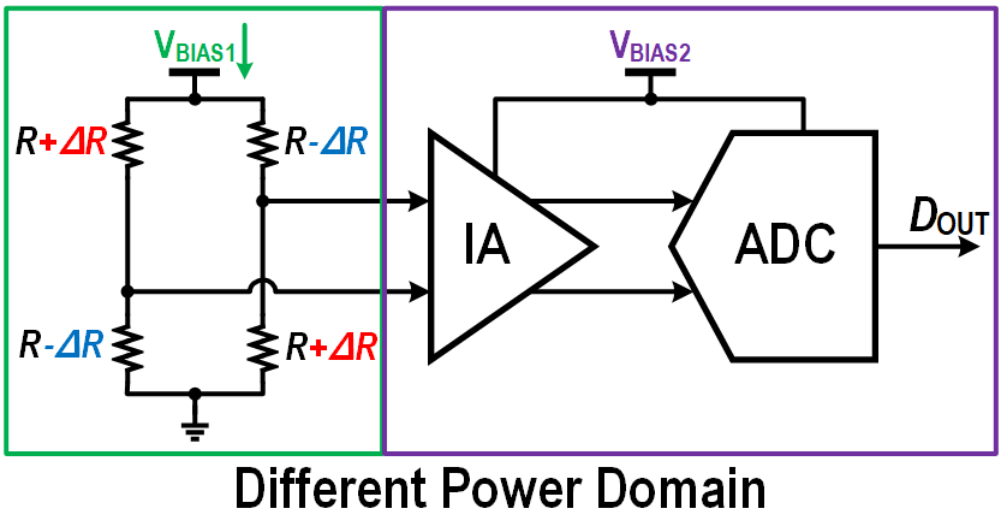
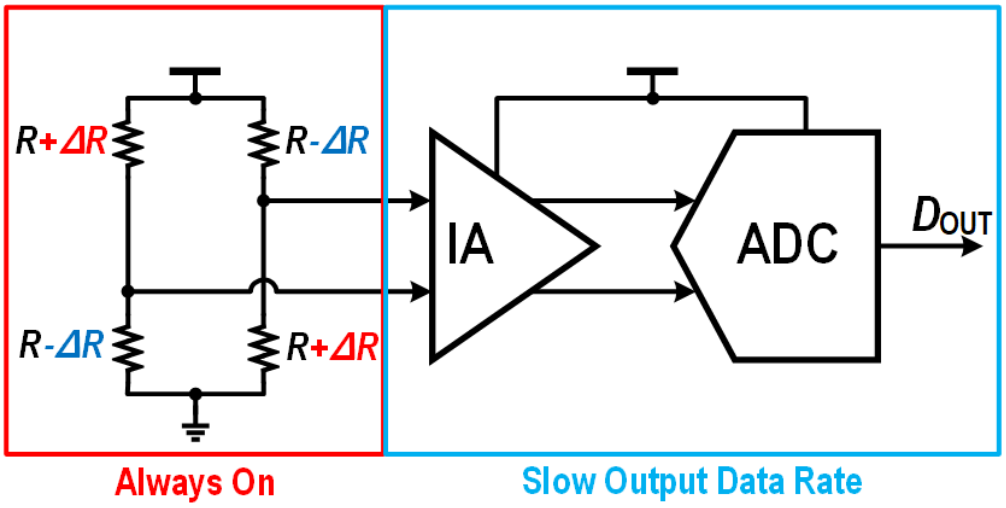


Fig. 1.5.4 Simplified block diagram of the bridge sensor system with different power domain.

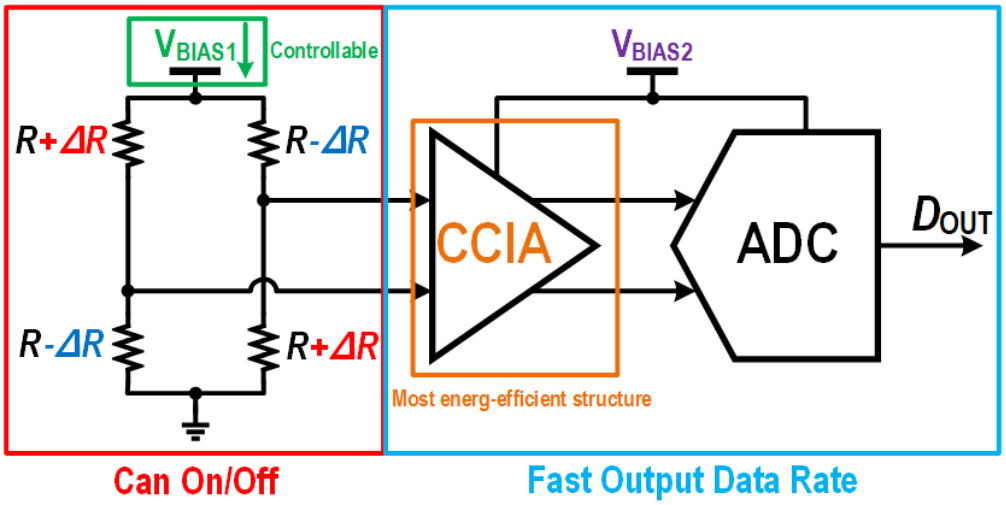
sensor is reduced from 10 V to 1.2 V, the current consumption is reduced from 30 mA to about 3.5 mA. And they emphasize that the remaining circuit consume negligible power compared to this. The trade-off exists for the expense of the bridge's output signal. When the V_{BIAS1} is reduced, the bridge's output signal lower correspondingly, making the noise floor a larger proportion of the signal. Also, In the paper [1.5.6], they use a separate supply voltage for the sensor and the analog front-end, which can reduce the power consumption of the sensor. It can be easily implemented with using CCIA.

1.6 INTRODUCTION OF THE PROPOSED SYSTEM

As we have mentioned so far, there have been many researches to enhance power efficiency. In this paper, we propose a 12.8 kHz energy-efficient force sensor system. To lower the power consumption of the force sensor read-out IC, deformed structure of a CCIA is implemented as the IA topology. And a discrete time delta-sigma ADC with 17-bits effective resolution. The system output data rate is 12.8 kHz. This speed is quite fast compare with previous works. In general, the force sensor's output moves slowly, so there is no need to have a quick output data rate. Nevertheless, the reason for taking the system speed up is to convert the analog signal to a digital signal quickly instead of slow conversion is that the sensor can be turned off for the rest of the time. Due to this, the power consumption of the sensor can be reduced. However, As the speed increases, the input impedance of CCIA decreases, making it unsuitable for a bridge sensor. In order to solve this problem, system chopping is used instead of the demodulating chopper of CCIA to propose a structure that can produce the effect of CCIA while maintaining one opamp, which is the advantage of a CCIA.



(a)



(b)

Fig. 1.6.1 (a) general slow speed of bridge sensor system and (b) proposed 12.8 kHz fast speed bridge sensor system.

1.7 THESIS ORGANIZATION

This paper consists of seven chapters and appendix chapter on the energy-efficient high-resolution bridge sensor sensing system. The first chapter introduces smart sensors and bridge sensor for various DC measurement systems. Also, previous works are introduced to achieve higher energy-efficient bridge sensor systems. Chapter 2 describes the system overview. Chapter 3 describes the proposed CCIA structures and techniques implemented. Chap 4 explains the operation and implementation of an incremental ΔΣ ADC. Chapter 5 describes the system architecture and its clock timing. Finally, chapter 6 introduces the measurement results and performance summary. Chapter 7 concludes the thesis. Appendix A. introduces the high-precision bridge sensor system with doubled-sampling time ΔΣ modulator technique to reduce IA's current consumption to half.

CHAPTER 2

SYSTEM OVERVIEW

2.1 SYSTEM ARCHITECTURE

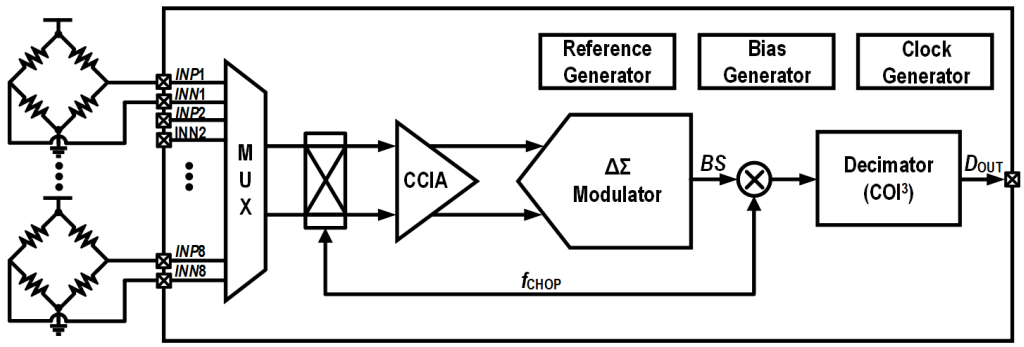


Fig. 1.7.1 Simplified block diagram of the system.

This paper describes a fully integrated read-out integrated circuit (IC) for high-precision DC measurement system. Fig. 2.1.1 shows the simplified block diagram of the entire system. It consists of an input multiplexer (MUX) to receive inputs from 8 different bridge sensors, CCIA, and a high resolution delta-sigma ADC. Low noise and energy-efficient CCIA is used in the system for programmable-gain instrumentation amplifier and

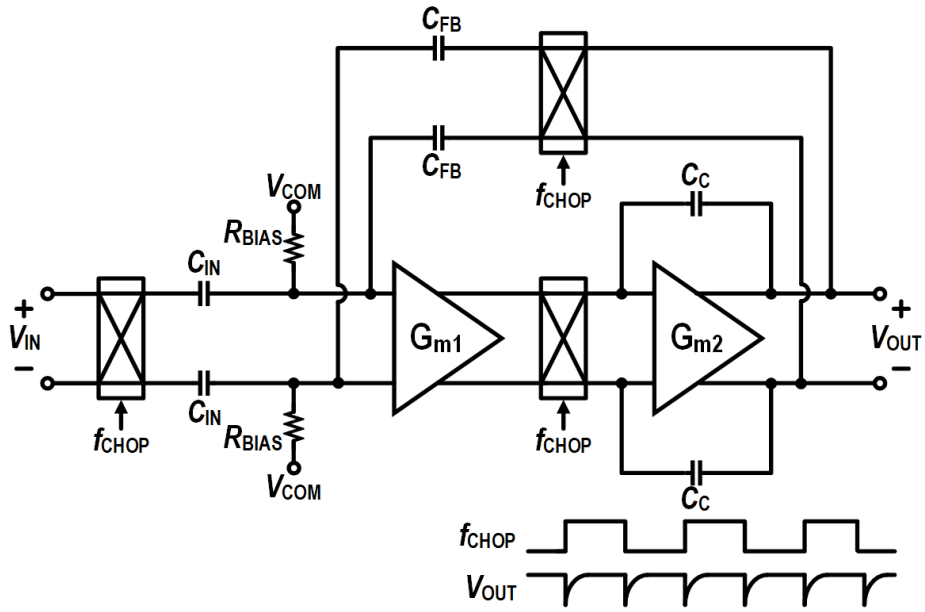
the gains of CCIA are 8, 16, 32, 64, and 128. Third-order incremental delta-sigma ADC is used for high-precision bridge sensor DC applications.

CHAPTER 3

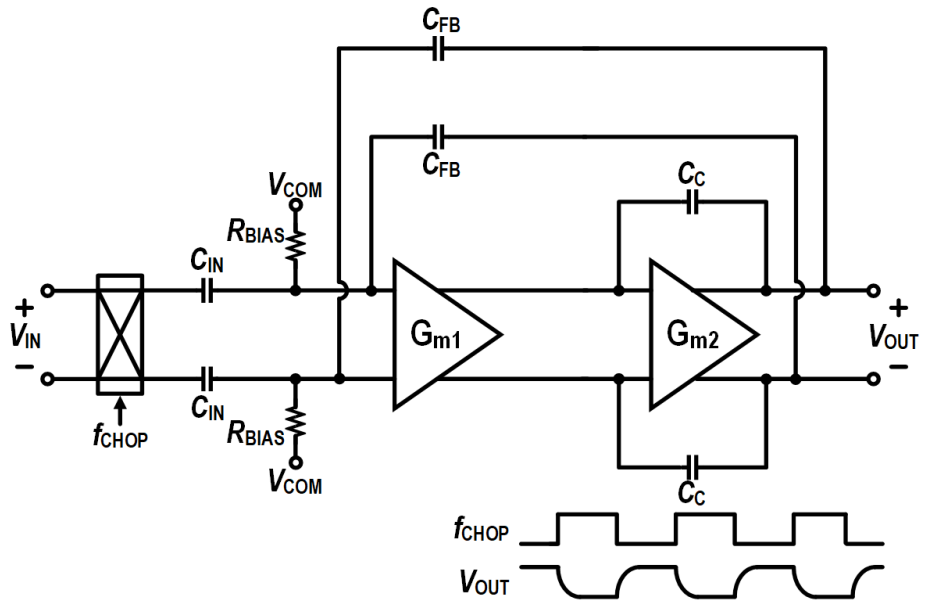
IMPLEMENTATION OF THE CCIA

3.1 CAPACITIVELY-COUPLED CHOPPER INSTRUMENTATION AMPLIFIER

Fig. 3.1.1 (a) shows the simplified block diagram of the conventional CCIA and its timing diagram. It consists of an input modulating chopper, a feedback chopper, and a demodulating chopper between Gm1 and Gm2. 1/*f* noise and offset are inherently quite low because of chopping comparing with other structures of IA [1.3.4], [1.5.1]. However, since the input impedance of CCIA is limited by the chopping frequency, it is not suitable for high-speed systems. As we have mentioned above, to reduce the average current, system's output data rate is 12.8 kHz, and the sampling frequency is 4 MHz when the oversampling ratio (OSR) 128 is used. In the conventional CCIA, the chopping frequency needs to satisfy 2 * ADC's sampling frequency, f_S, which is 8 MHz [1.5.3], [1.5.6]. Then, the input impedance may be too low for use in bridge sensor, which is composed of resistors, and may cause signal loss. Fig. 3.1.1 (b) shows the simplified block diagram of the proposed block diagram. Because



(a)



(b)

Fig. 3.1.1 (a) Simplified block diagram of the conventional CCIA, (b) Simplified block diagram of the proposed CCIA.

demodulating chopper and feedback chopper. Then, we have used 12.8 kHz as an input chopping frequency, which is same as output data rate. Accordingly, the output of the proposed CCIA looks like V_{OUT} as shown in Fig. 3.1.1 (b). The output of the proposed CCIA is once positive voltage and once negative voltage. Then, demodulate negative voltage to positive voltage, when the input is positive voltage, after the analog-to-digital conversion. In the proposed scheme, the conventional CCIA's modulating chopper and demodulating chopper are replaced with system choppers as we can see in Fig. 2.1.1. Through the proposed scheme, it can be used at higher speeds without significant performance degradation than a conventional CCIA. We can still inherently remove 1/*f* noise and amplifier offset, and can maintain better energy-efficiency than 3-opamp or CFIA because only one operational amplifier is a noise source.

3.2 IMPEDANCE BOOSTING

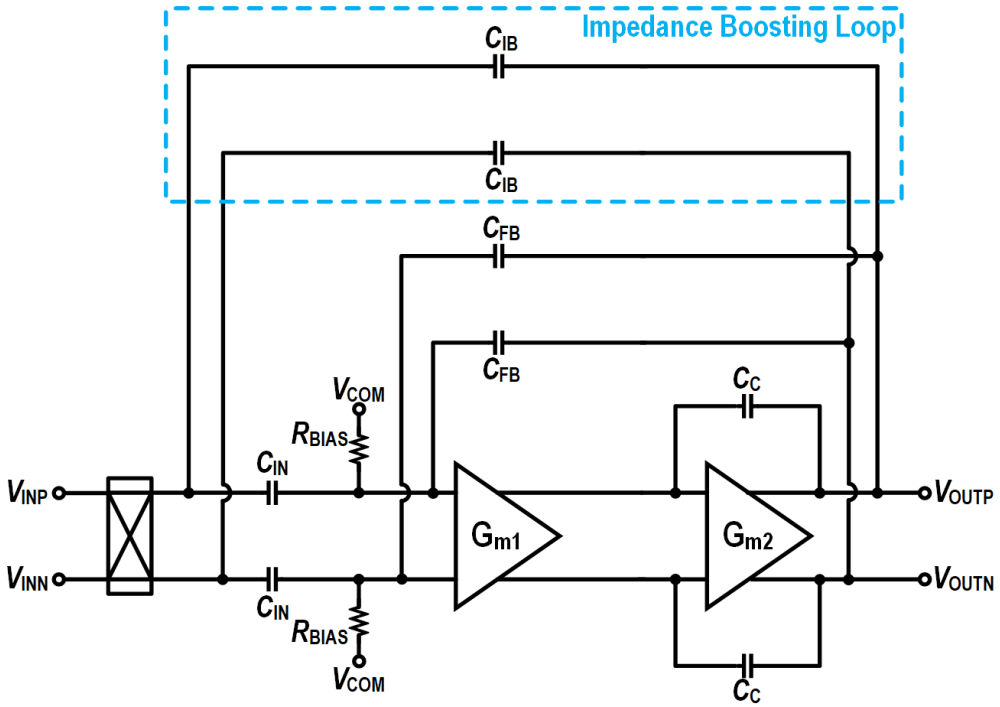


Fig. 3.2.1 Impedance boosting loop in the CCIA.

Although, CCIA is the most energy-efficient structure among IAs, it is still being researched most actively in recent years because it has some disadvantages. Input impedance is a critical drawback of CCIA. In CCIA, to transfer the signal, it is forced to

use input chopping and it lowers the input impedance. Therefore, we need to use some techniques to boost the input impedance. The widely known impedance boosting techniques can be divided into two. The first technique is using impedance boosting loop (IBL) as shown in fig. 3.2.1 [1.3.7]. And the second technique is using auxiliary buffers [3.2.1], [3.2.2]. The auxiliary buffer is a technique to increase the input impedance by momentarily passing through the buffer. Normally, this technique can achieve higher input impedance than the IBL technique. However, it increases design complexity and current consumption. Also, rail-to-rail sensing is not possible, which is a big advantage of a CCIA. On the other hand, in [3.2.3]-[3.2.5], they achieved higher input impedance with modified structure of the IBL technique. Fig. 3.2.1 shows the block diagram of the CCIA with IBL. Two extra feedback capacitors C_{IB} are used for IBL, which provide positive feedback to the CCIA's input. The IBL generates current I_{IB} equal to I_{FB}. Accordingly, the input impedance of the CCIA is infinite because no input current is drawn from the signal source, theoretically. From the equation (3.1), we can find C_{IB} which can make infinite input impedance:

$$I_{IB} = 2(V_{OUT} - V_{IN}) \cdot f_{CHOP} \cdot C_{IB} = 2V_{OUT} \cdot f_{CHOP} \cdot C_{FB} = I_{FB}$$

$$C_{IB} = \frac{C_{IN}}{G-1} \tag{3.2.1}$$

Where G is the closed loop gain. However, C_{IB} cannot be the exact value we have calculated in the equation (3.2.1). Therefore, the boosted input impedance cannot reach infinite. The compromised boosted input impedance can be calculated as follows [1.3.7],

$$Z_{IN\_BOOSTED} = \frac{V_{IN}}{I_{IB}} = \frac{G}{2 f_{CHOP} \cdot C_{IN}} \tag{3.2.2}$$

Then, if we assume, the G is 100, the $Z_{IN\_BOOSTED}$ becomes 100*Z_{IN}, where Z_{IN} is the original input impedance. In addition, the parasitic capacitance in between C_{IN} and ground affects the value of C_{IN} and the $Z_{IN\_BOOSTED}$ from the equation (3.2.2) will be different. In practice, the measured boosted input impedance is much smaller than the calculation from (3.2.2). it is around 5 times to 10times bigger than original input impedance. As the resolution of C_{IB} is smaller, we can make higher boosted input impedance, in practice. In this design, the resolution of 5 bits C_{IB} array is used.

3.3 SENSOR OFFSET CANCELLATION

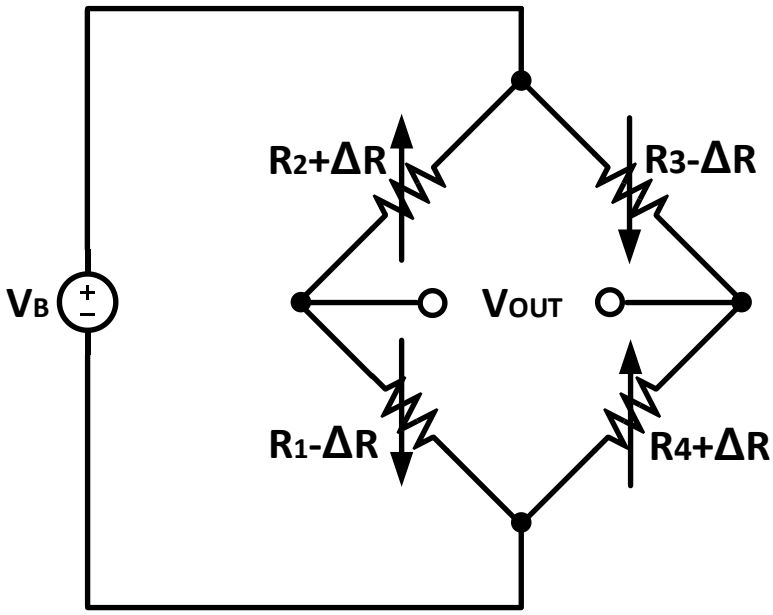


Fig. 3.3.1 Block diagram of the bridge sensor.

Fig. 3.3.1 shows the block diagram of the bridge sensor. Ideally, if the pressure is 0 kPa, ΔR is 0 and the bridge resistances are the same as $R_1 = R_2 = R_3 = R_4$. However, in practice, because of the mismatches, the bridge resistances cannot be the same. Then, the sensor offset, V_{OFFSET}, exists when the pressure is 0 kPa. For example, $R_1 = R_3 = 1100\Omega$ and

$R_2 = R_4 = 1000\Omega$ with $V_B = 5V$, then, V_{OFFSET} can be calculated as follows:

$$V_{OFFSET} = V_B\left(\frac{R_1}{R_1 + R_2} - \frac{R_4}{R_3 + R_4}\right) \tag{3.3.1}$$

Then, V_{OFFSET} is 238 mV. This V_{OFFSET}. From the equation 3.3.1, as resistance mismatch increases of V_B increases, V_{OFFSET} increases. In the bridge sensor, since the offset is quite large often and the IA's output can be saturated. In other words, the offset limits the IA's output range. If we don't remove the offset before amplification, the ADC needs to have a lower input-referred noise and a wider dynamic range. Then, the power consumption increases.

There have been some techniques to remove the bridge sensor offset. The first one is trimming the bridge by an external offset compensation network [3.3.1]. The second one is injecting current into the bridge with a current DAC [3.3.2]. The last one is a ratio-metric offset-compensation scheme by using capacitor DAC (CDAC) [1.5.6]. In this design, a ratio-metric offset-compensation scheme is used to remove bridge sensor's offset. Fig. 3.3.2 shows the simplified block diagram of the CCIA with a ratio-metric offset-compensation CDAC. CDAC2 is used to cancel out bridge sensor's offset and CDAC1 is used to compensate for the input impedance affected by CDAC2. The CDAC2 is a duplication of the input chopper and input capacitor with different capacitance, so that it

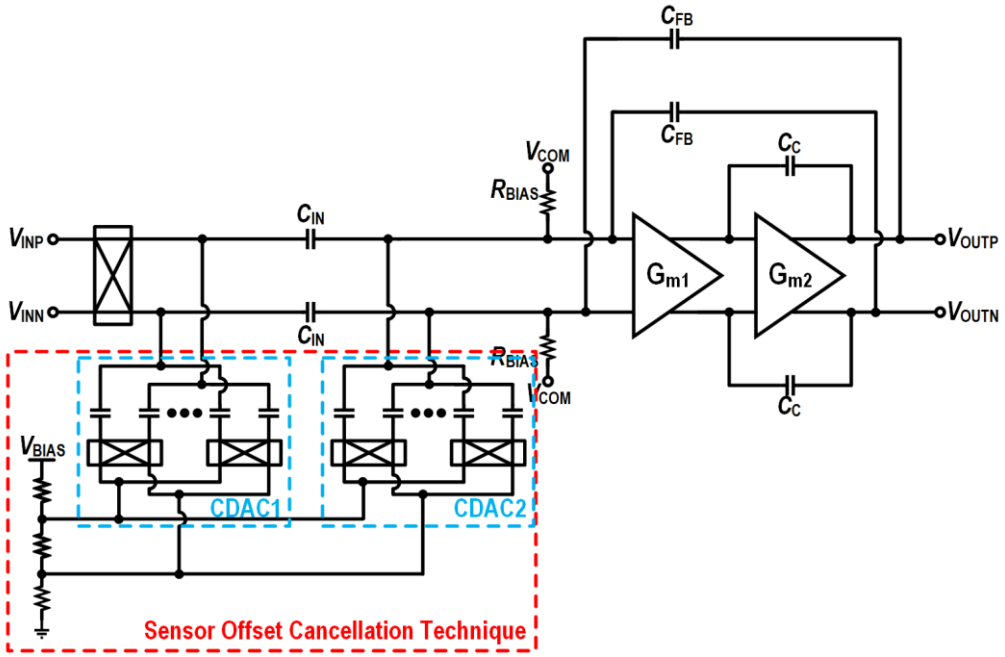


Fig. 3.3.2 Block diagram of the CCIA with sensor offset cancellation technique.

acts like an another input to the CCIA. Therefore, we can cancel out input offset with operating CDAC2 in opposite to the polarity of the input offset. It is 7-bits resolution CDAC with 2.76 mV lsb and +/- 350 mV offset cancellation range. CCIA's output can be calculated by

$$V_{OUT} = \frac{C_{IN}}{C_{FB}}\left(V_{IN} + \frac{C_{SENSOR}}{C_{IN}}\Delta V_{RLADDER}\right)$$

$$= \frac{C_{IN}}{C_{FB}}(V_{SENSOR} + V_{OFFSET} - V_{CAL})$$

(3.3.1)

Where V_{IN} is input from the bridge sensor which is V_{SENSOR} added by V_{OFFSET}, $V_{RLADDER}$ is from resistor ladder, and V_{CAL} is from offset calibration CDAC.

3.4 AMPLIFIER OFFSET CANCELLATION

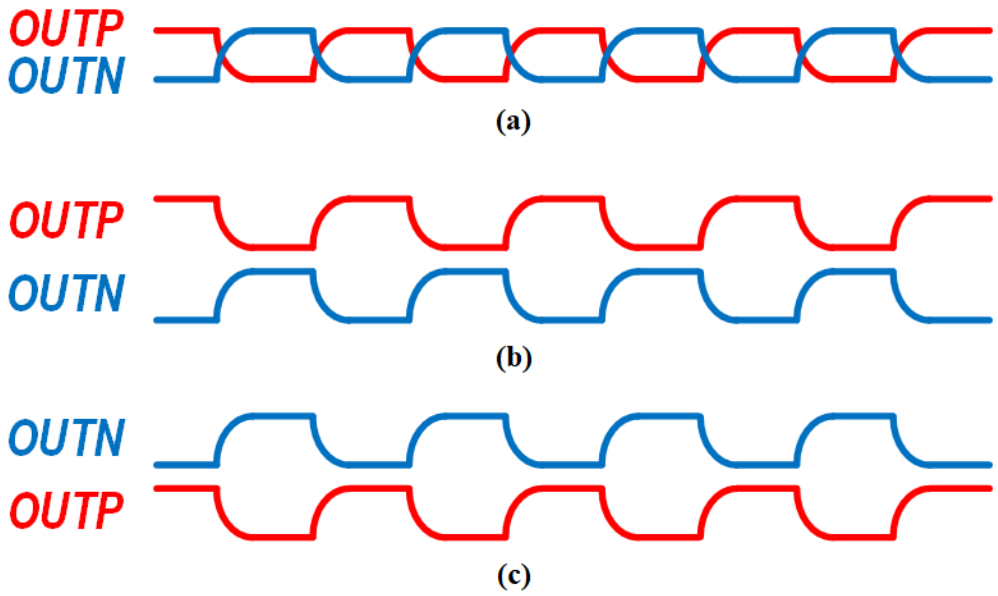


Fig. 3.4.1 (a) Output of the CCIA when amplifier's offset is zero, (b) output of the CCIA when amplifier's offset is positive voltage, and (c) output of the CCIA when amplifier's offset is negative.

Fig. 3.4.1. shows the waveform when amplifier's offset exists. Fig. 3.4.1 (a) shows the output waveform of the proposed CCIA when amplifier's offset does not exist. Fig.

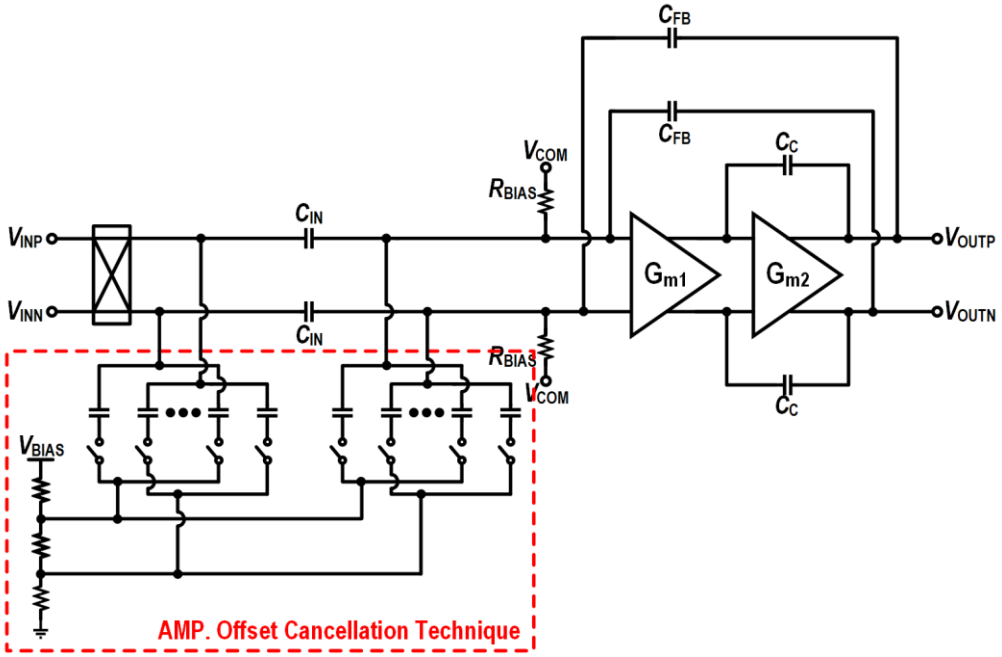


Fig. 3.4.2 Block diagram of the CCIA with amplifier offset cancellation technique.

3.4.1 (b) shows the output waveform of the CCIA when amplifier's offset is positive voltage. Fig. 3.4.1 (c) shows the output waveform of the CCIA when amplifier's offset is positive voltage. In the extreme case, the amplifier's offset can be increased to 100 mV [1.3.7]. A certain amount of amplifier's offset can be solved by system level chopping, but if the amplifier's offset is large with a large input, the CCIA output can be saturated. Fig. 3.4.1 shows the proposed amplifier offset cancellation technique. The operation method is similar to the sensor offset cancellation technique, but in sensor offset cancellation, the polarity of resistor ladder voltage is reversed whenever the input chopper is chopping, but

in amplifier offset cancellation, the polarity of resistor ladder voltage is maintained in the same direction.

$$V_{OUT} = \frac{C_{IN}}{C_{FB}}\left(V_{IN} + \frac{C_{SENSOR}}{C_{IN}}\Delta V_{RLADDER} - \frac{C_{AMP}}{C_{IN}}V_{RLADDER}\right)$$
$$= \frac{C_{IN}}{C_{FB}}\left(V_{SENSOR} + V_{OFFSET} - V_{CAL} - V_{AMP}\right) \quad (3.4.1)$$

Where C_{SENSOR} is the capacitance in sensor offset calibration CDAC and C_{AMP} is the capacitance in amplifier offset calibration CDAC.

3.5 AMPLIFIER IMPLEMENTATION

Fig. 3.5.1 shows the detailed circuit diagram of the main two-stage amplifier in the CCIA. This main amplifier takes up most of the noise in the bridge sensor system. Then, to increase the energy-efficiency, the main amplifier should be carefully designed. The amplifier's first stage is a folded cascode and the second stage is a class-AB. To maximize the unit gain bandwidth (UGBW), a cascade Miller-compensation technique is used. The amplifier is designed to have 130 dB DC gain, 11 MHz UGBW, and 90 ° phase margin. Also, continuous-time common mode feedback (CT-CMFB) is implemented. And the input referred noise of the main amplifier is 33 nV/√Hz.

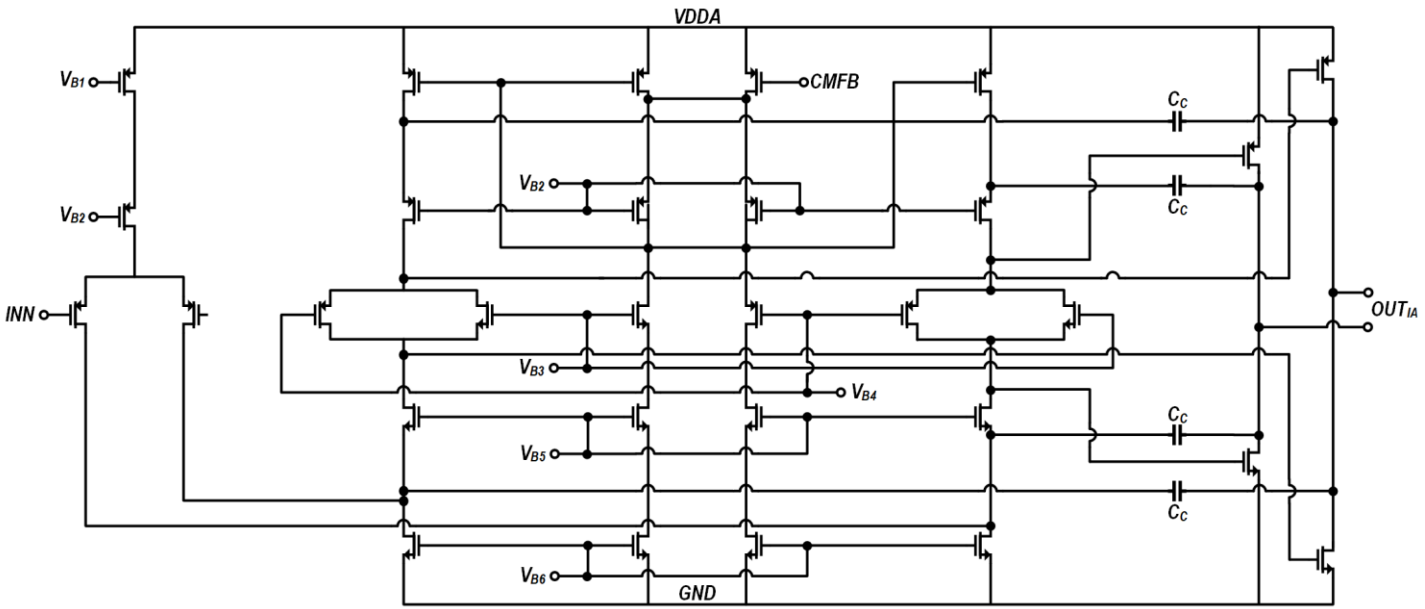


Fig. 3.5.1 The schematic of main amplifier in the CCIA.

3.6 IMPLEMENTATION OF THE CCIA

Fig. 3.6.1 shows the block diagram of the proposed CCIA in the thesis. Input capacitance is 9 pF and feedback capacitances are 0.07, 0.14, 0.28, 0.56, 1.12 pF to produce a closed0loop gain G of 8, 16, 32, 64, and 128, respectively. Impedance boosting loop capacitances are the same as C_{FB}s. When designing CCIA, the noise gain is the one that we need to consider. The equation (3.6.1) shows the noise factor calculated by signal gain, G, and noise gain, NG, [1.3.3].

$$\frac{G}{NG} = \frac{C_{IN} + C_P + C_{FB}}{C_{IN}} \tag{3.6.1}$$

Where C_P is the parasitic capacitance of the input stage. C_{IN} is chosen to have a relatively big capacitance to achieve a low noise factor. As we have mentioned earlier, Impedance boosting, sensor offset cancellation, amplifier offset cancellation techniques are implemented. Also, input chopper exists to transfer the sensor signal to the output.

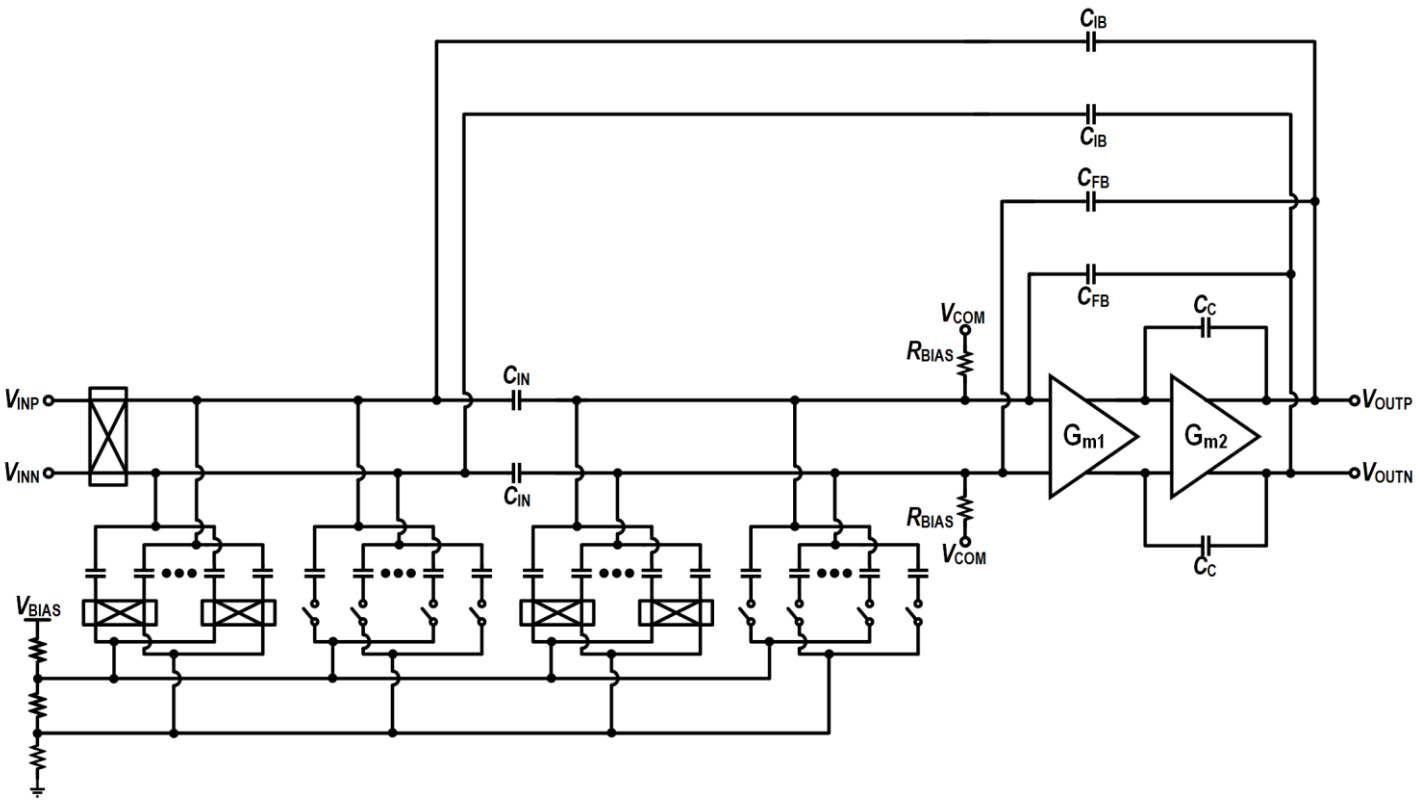


Fig. 3.6.1 Simplified block diagram of the proposed CCIA.

CHAPTER 4

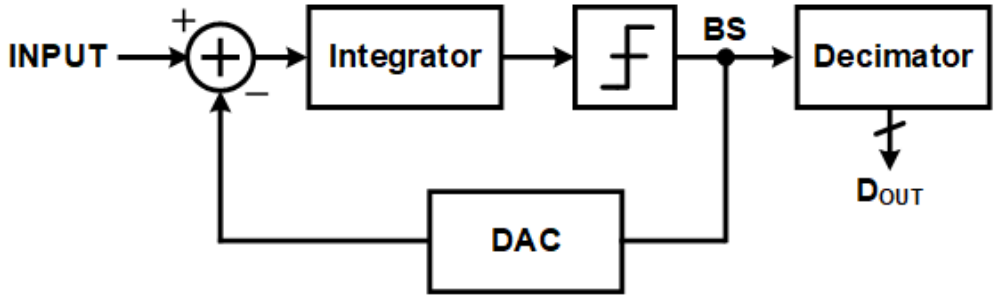
INCREMENTAL ΔΣ ADC

4.1 INTRODUCTION OF INCREMENTAL ΔΣ ADC

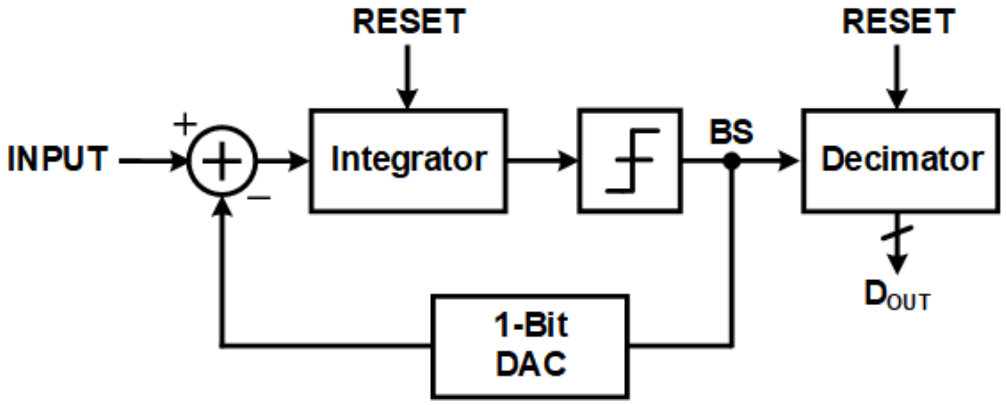
Fig. 4.1.1 shows a first-order incremental ΔΣ ADC. The ΔΣ ADC consists of an analog ΔΣ modulator and a digital decimation filter. The negative feedback loop in Fig. 4.1.1 is called a ΔΣ modulator. The integrator is often referred to as the loop filter. The negative feedback loop is composed of a loop filter, a quantizer or a coarse ADC, and a feedback DAC. The ΔΣ modulator operates with oversampling and noise-shaping. The input signal processes through the signal transfer function (STF) and the quantization noise processes through noise transfer function (NTF). Then, the quantization noise is shaped by the high-pass filter NTF [4.1.1]. On the other hand, a decimation filter low-pass filters the noise-shaped quantization noise and it down samples the oversampled bit-stream of the ΔΣ modulator to the Nyquist rate which is twice the bandwidth.

The incremental ΔΣ ADC has a pretty much similar structure with a conventional ΔΣ ADC [4.1.2]. There are three significant differences. The first one is the incremental converter does not operate continuously. The second one is that the loop filter and digital

decimation filter are reset after each conversion. The last one is that the decimation filter can be realized with a much simpler structure. At the beginning of each conversion, incremental ΔΣ ADC reset all memory elements. Therefore, the incremental ΔΣ ADC is well-suited for DC sensor systems such as temperature, humidity, pressure, etc. Also, because there is a reset for each conversion, it is easy to use in a multiplexed system. In other words, the incremental ΔΣ ADC can process multiple sensor inputs with a single ADC. Therefore, the benefits can be obtained in terms of area and power consumption. Additionally, 1-bit quantizer is inherently linear, making them optimal for sensor applications.



(a)



(b)

Fig. 4.1.1 (a) Block diagram of a first-order ΔΣ ADC and (b) Block diagram of a first-order incremental ΔΣ ADC.

4.2 IMPLEMENTATION OF INCREMENTAL ΔΣ MODULATOR

Fig. 4.2.1 shows a block diagram of the designed incremental ΔΣ modulator with coefficients. The structure is implemented as a cascade of integrators with a feedforward (CIFF). The ΔΣ modulator consists of a third-order loop filter, 1-bit quantizer, and 1-bit DAC followed by a digital decimation filter. Fig. 4.2.2 shows a schematic diagram of the third-order ΔΣ modulator. The values of both sampling capacitor, C_{S1}, and DAC capacitor, C_{DAC}, are is 1.05 pF. C_{S1} samples the inputs V_{INP} and V_{INN} and C_{DAC} samples the reference V_{REFP}. The separate sampling structure is used so that the feedback signal does not interfere with the input signal [4.2.1], [4.2.2]. The DC signal gain can be defined as C_{S1}/C_{DAC}, which is b_1/C_1. 7 pF capacitor is used for C_{FB}. The sampling clock frequency is 4MHz to make ODR 12.8 kHz with OSR 128. The first integrator is the most important block in the ΔΣ modulator. We need to have a low IRN and sampling error [4.2.3]. Accordingly, to reduce 1/*f* noise, CDS technique is applied to the first integrator. Also, bottom-plate sampling with non-overlapping clock is used to reduce the nonlinearities. Passive adder is used to minimize the static current.

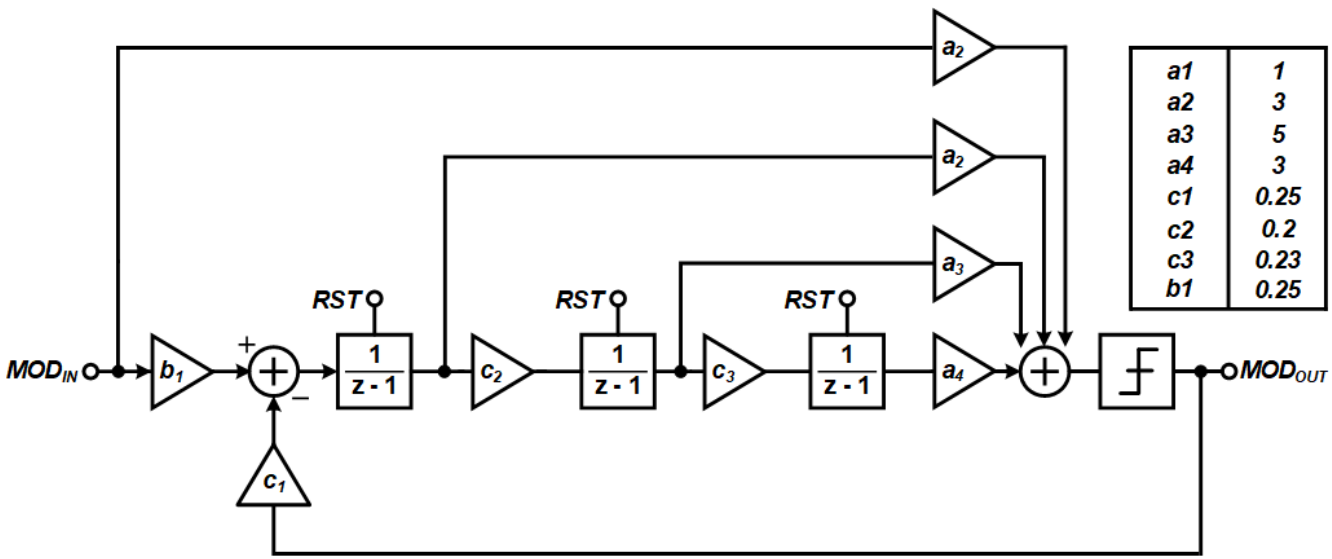


Fig. 4.2.1 Block diagram of the ΔΣ modulator with coefficients.

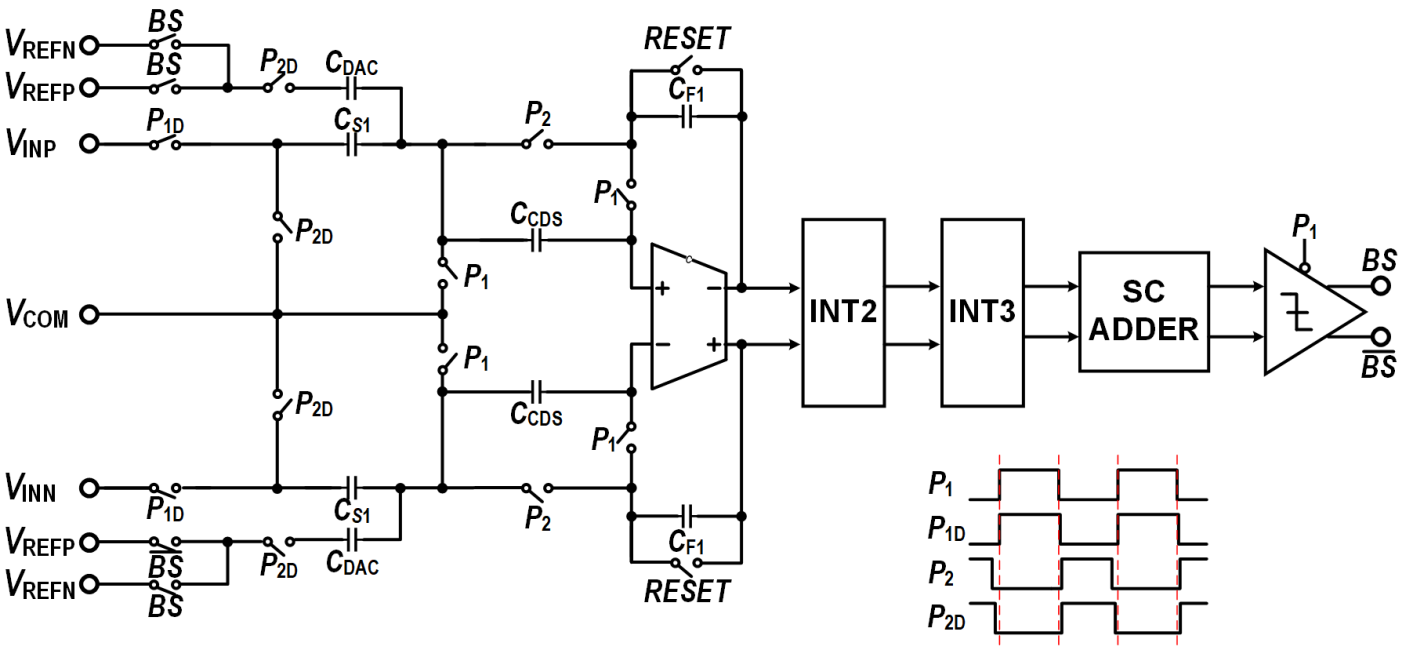


Fig. 4.2.2 Schematic of ΔΣ modulator.

CHAPTER 5

SYSTEM-LEVEL DESIGN

5.1 DIGITAL FILTER

Generally, either a CoI filter or a sinc filter is designed to process the output of the incremental ΔΣ modulator. The sinc filter provides line frequency noise suppression, so that it is the most popular for high precision dc applications. In contrast, this filter topology requires a high N, where we can consider N as an OSR in the conventional ΔΣ modulator, to achieve the same resolution when compared to other topologies. Accordingly, sinc filter is usually used for slow systems. On the other hand, CoI filters do not provide line frequency noise suppression. Nevertheless, it gives a faster response for incremental converters as the values obtained for N are smaller. As a result, an incremental ΣΔ ADC with a CoI filter can reach high bandwidths moderately, making it suitable for multiplexing. However, considering higher-order filtering, the filter coefficients are not the same, which affects the ADC output noise [4.1.2], [5.1.1].

Fig. 5.1.1 shows the block diagram of the proposed system with clock timings. As we have mentioned above, CoI^3 filter is appropriate for our proposed system because the default system speed is 12.8 kSPS, which is faster than general bridge sensor read-out IC and OSR is only 128. Therefore, in the proposed design, CoI^3 decimation filter [4.1.2] is

used followed by a finite impulse response (FIR) filter. The digital filter is programmable for ODR of 12.8 kSPS, 7.04 kSPS, 3.7 kSPS, 2.46 kSPS, and 1.23 kSPS.

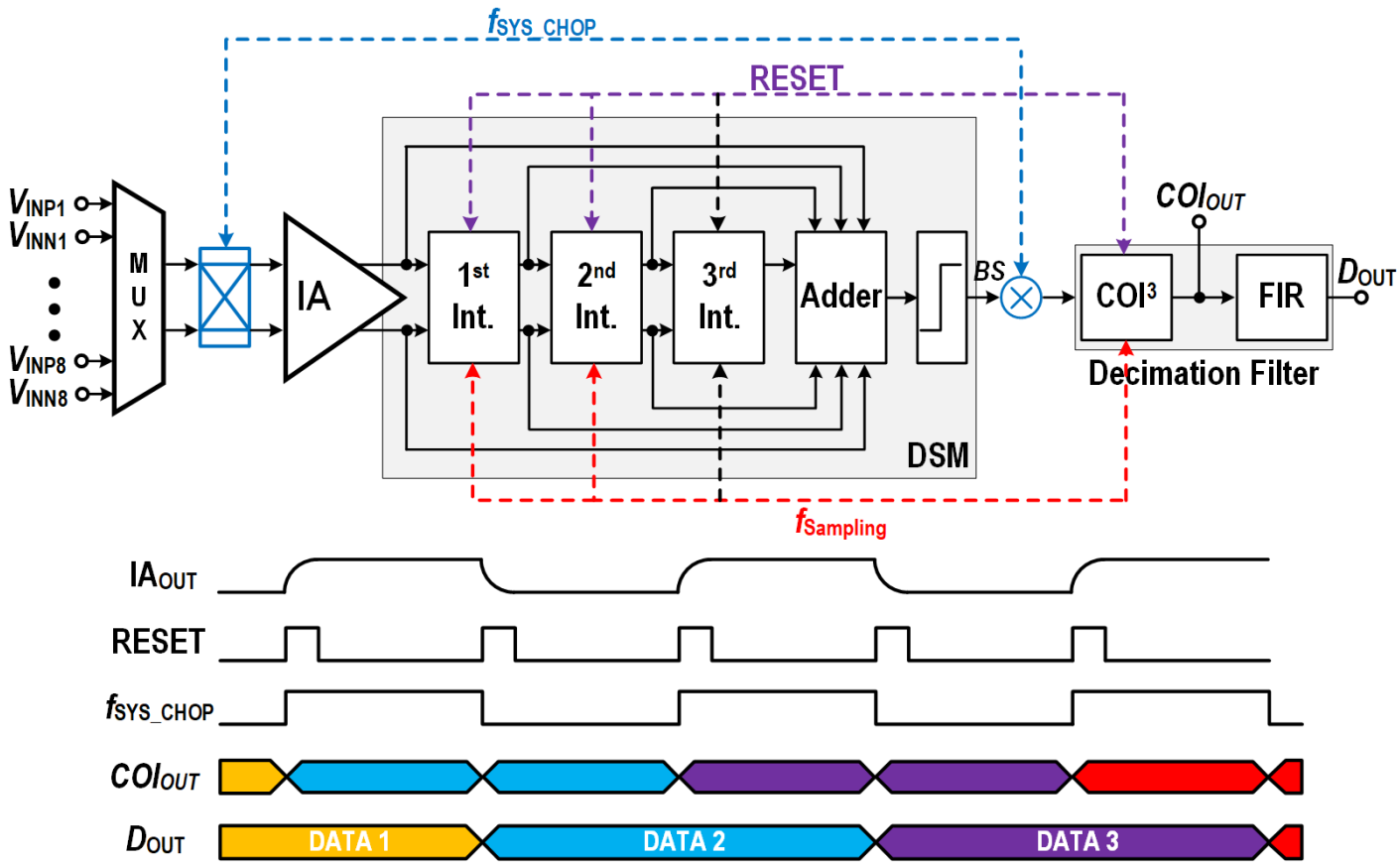


Fig. 5.1.1 Proposed block diagram of the system with clock distribution.

5.2 SYSTEM-LEVEL CHOPPING & TIMING

Fig. 5.1.1 shows the proposed block diagram of the system with clock distribution. In the system, to increase the input impedance, CCIA's input chopping frequency is not $f_{sampling}/2$ which is 2 MHz. And the chopping demodulator is removed in between first and second stage of CCIA's main amplifier. Because there is no chopping demodulator, the output of IA moves up and down and additional ripple reduction loop (RRL) is not necessary. As we can see in Fig. 5.1.1, settling time is required for IA's output. Accordingly, RESET time is 24 * ($1/f_{sampling}$), which is longer than general reset time, $1/f_{sampling}$. And the incremental ΣΔ modulator's conversion time is 128 * ($1/f_{sampling}$). The reset time and conversion time make the ODR 12.8 kSPS. Enough reset time is required for fully settled IA's output. On the other hand, the system level chopping is essential in this structure because the chopping demodulator is removed. The CoI^3 filter's output, COI_{OUT}, is 25.6 kHz. The consecutive COI_{OUT} are averaged out by the FIR filter to make one D_{OUT}. This system chopping can improve system performance by reducing the 1/f noise while removing the offset of the AFE. Although, system level chopping reduces the ODR by a factor of 2, but increase the ER with 0.5 bits. On the other hand, as mentioned in the introduction, the IA is power-hungry block. The current consumption ratio of IA and ADC is 3.6:1 in the proposed system. The current consumption of the IA is 1.37 mA and that of the ΣΔ modulator is 362 μA. The ADC samples the same DC input during one conversion time to create a single ADC output data while eliminating the demodulation chopper of

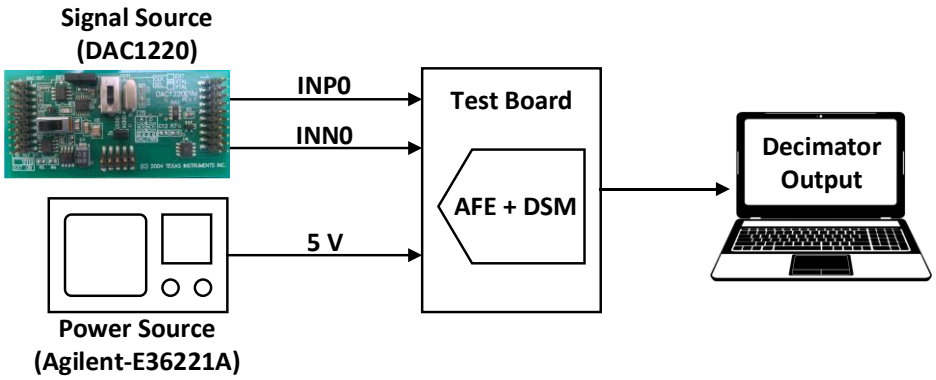
CCIA and replacing it with system chopping. After one conversion is completed, the DC value with the same absolute value and different polarity is output by input system chopping for the next conversion. Accordingly, the ΣΔ modulator's input is the same in terms of dynamic range compared to a conventional CCIA.

CHAPTER 5

MEASUREMENT RESULTS

6.1 MEASUREMENT SUMMARY

The force sensor readout-IC is designed and fabricated in a standard 0.13 μm CMOST process. Fig. 6.1.1 shows the chip microphotograph. The chip's active area is 1.95 mm^2, which consists of the CCIA, incremental ΔΣ modulator, LDO, BGR, POR, and biasing circuits. The AFE occupies 1.32 mm^2. The AFE consumes 1.75 mA from a 3 V supply and the digital circuit (decimator) draws 20 μA from a 1.5 V supply when 12.8 kHz output data rate.



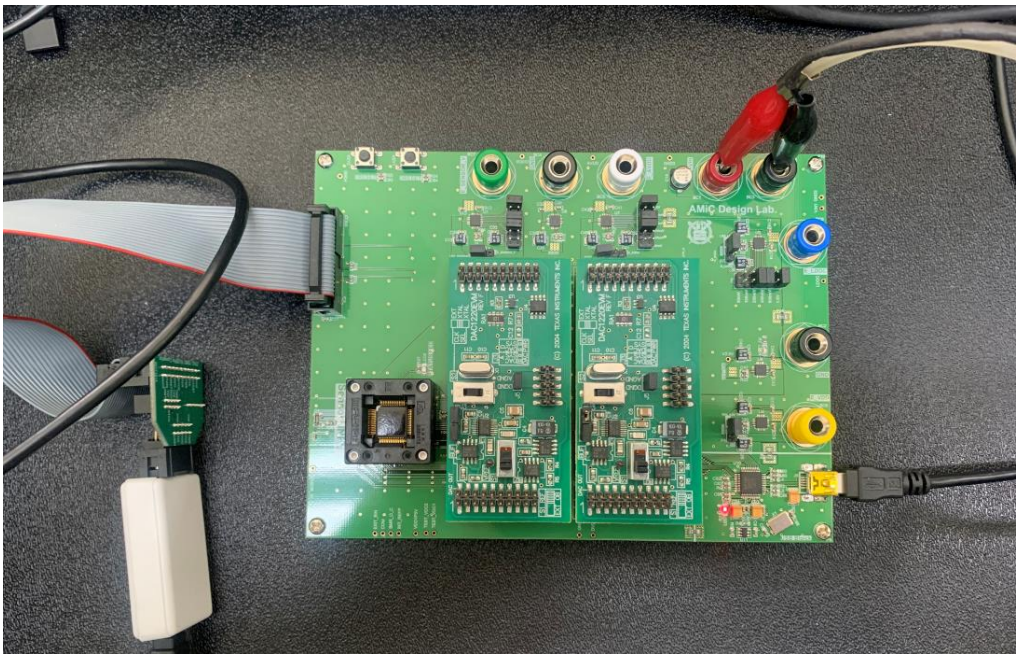


Fig. 6.1.1 Measurement Setup and connected test board.

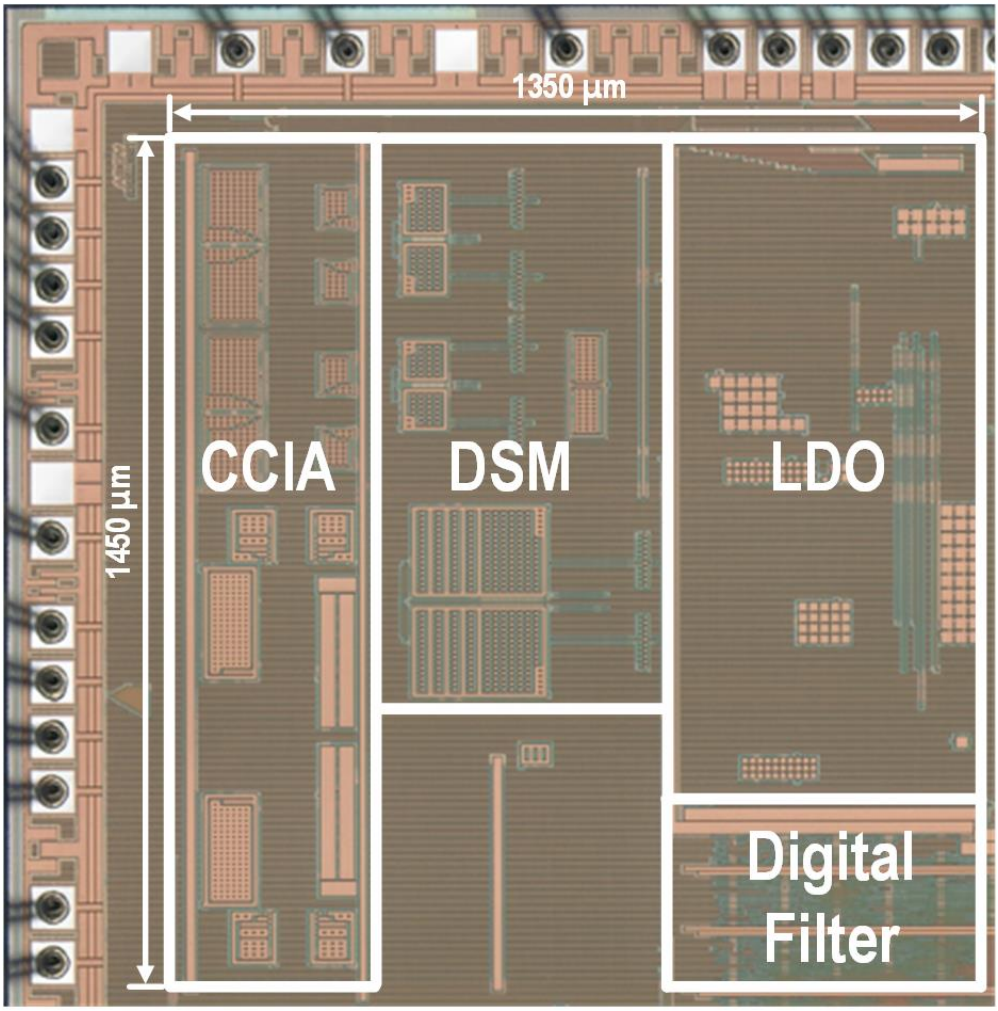


Fig. 6.1.2 Chip microphotograph.

6.2 LINEARITY & NOISE MEASUREMENT

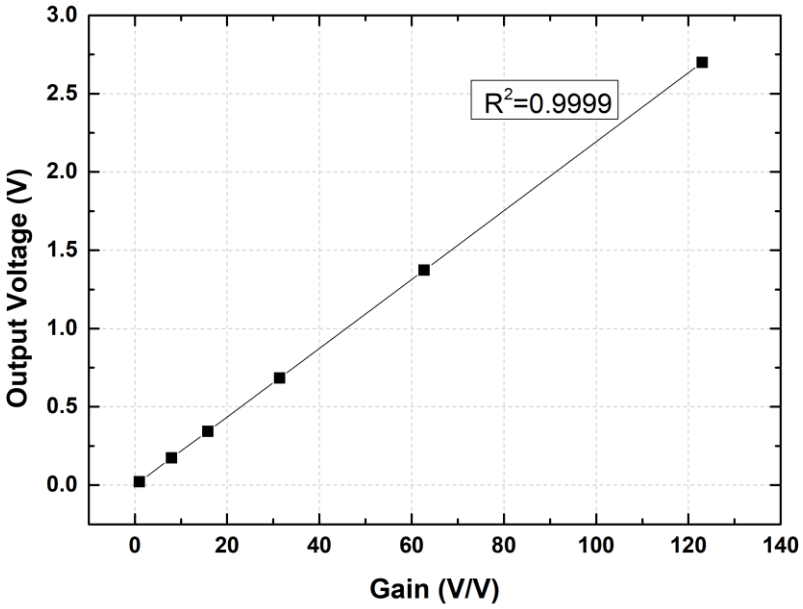
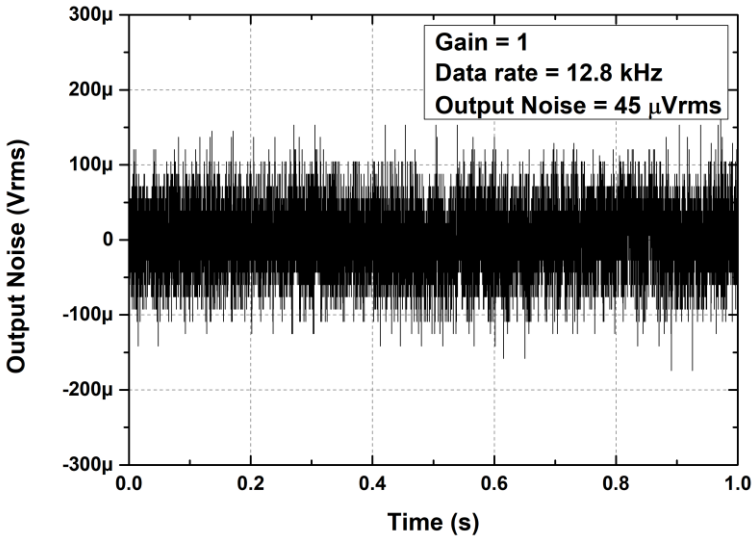
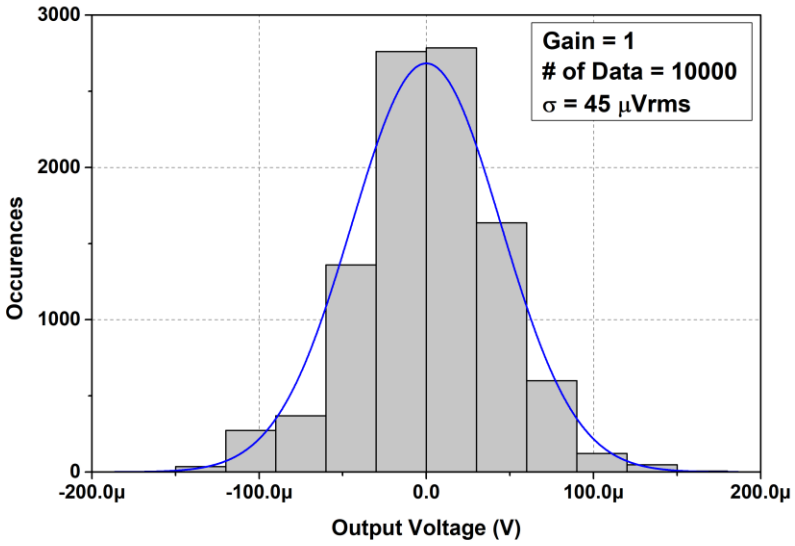


Fig. 6.2.1 Output voltage versus gain.

Fig. 6.21 shows the measured output of the read-out IC versus gain with a fixed 20 mV input. The measured result shows that the output of the read-out IC is highly linear with a coefficient of determination is equal to 0.9999. The measured gains are x1, x7.9, x15.6, x31, x59.4, x111.

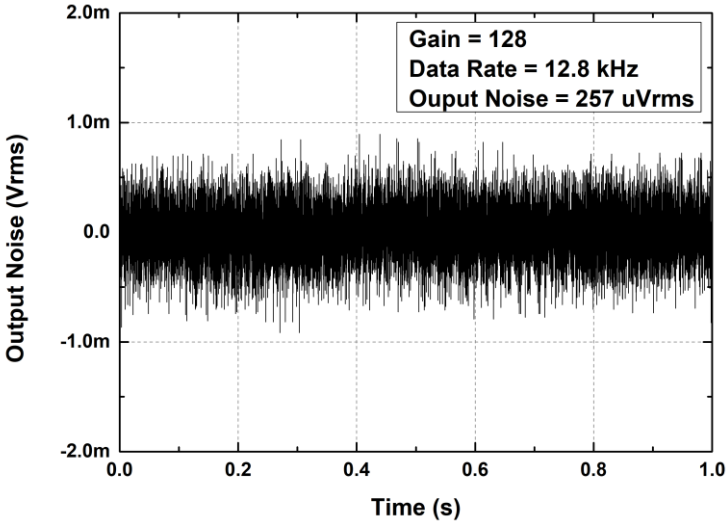


(a)

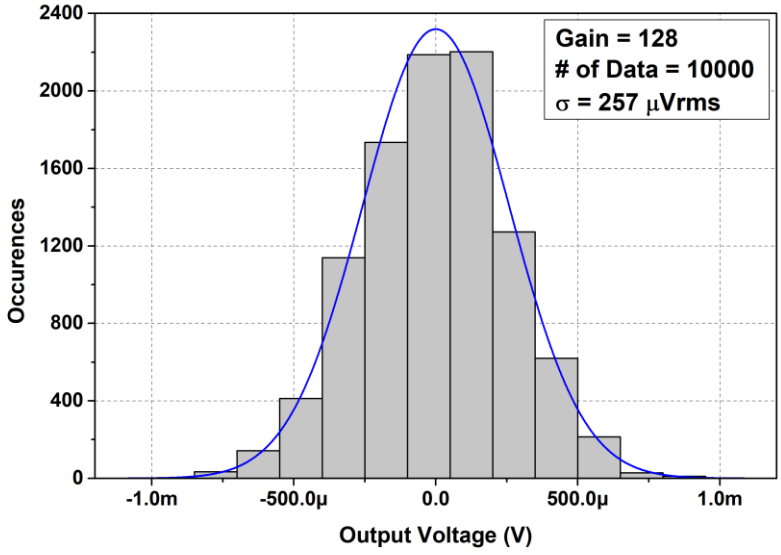


(b)

Fig. 6.2.2 (a) Output noise in time domain at gain 1. (b) Output noise histogram at gain 1.



(a)



(b)

Fig. 6.2.3 (a) Output noise in time domain at gain 128. (b) Output noise histogram at gain 128.

Fig. 6.2.2 (a) shows the measured output data of the read-out IC in the time domain when the gain is 1 at 12.8 kSPS ODR. Fig. 6.2.2 (b) shows the noise histogram when the gain is 1 at 12.8 kHz ODR. In gain 1, IA is bypassed and input is directly connected to the ADC. In other words, Fig. 6.2.2 shows ADC's RMS noise. From Fig. 6.2.2, ADC's input referred noise (IRN) is 45 μVrms and its effective resolution (ER) is 17.0 bits. Fig. 6.2.3 (a) shows the measured output data of the read-out IC in the time domain when the gain is 128 at 12.8 kSPS ODR. Fig 6.2.2 (b) shows the noise histogram when the gain is 1 at 12.8 kSPS ODR. Fig. 6.2.3 shows the system's RMS noise at max gain. In this system, when the gain is 128, the measured output referred noise is 257 μVrms and the input referred noise is 2.0 μVrms. Then, the ER is 14.6 bits.

Fig. 6.2.4 shows the ER versus ODR at each gain. For different conversion time, ODR is adjusted by different over sampling ratio (OSR) in DSM. As can be seen from the theory [4.1.1], the larger the OSR of the DSM, the better the performance of the DSM. From Fig. 6.2.4, it can be seen that the ER of the read-out IC improves as the conversion time becomes slower and the graph is linearly increased as the OSR is doubled. The measured ODRs are 12.8 kSPS, 7.04 kSPS, and 3.7 kSPS and used OSRs are 128, 256, and 512, respectively. In gain 1, the measured ERs are 17.0 bits and 18.0 bits at 12.8 kSPS and 3.7 kSPS, respectively. In gain 8, the measured ERs are 16.9 bits and 17.8 bits at 12.8 kSPS and 3.7 kSPS, respectively. In gain 16, the measured ERs are 16.5 bits and 17.5 bits at 12.8 kSPS and 3.7 kSPS, respectively. In gain 32, the measured ERs are 16.1 bits and 16.9 bits at 12.8 kSPS and 3.7 kSPS, respectively. In gain 64, the measured ERs are 15.5 bits and 16.0 bits at 12.8 kSPS and 3.7 kSPS, respectively. In gain 128, the measured ERs are 14.6

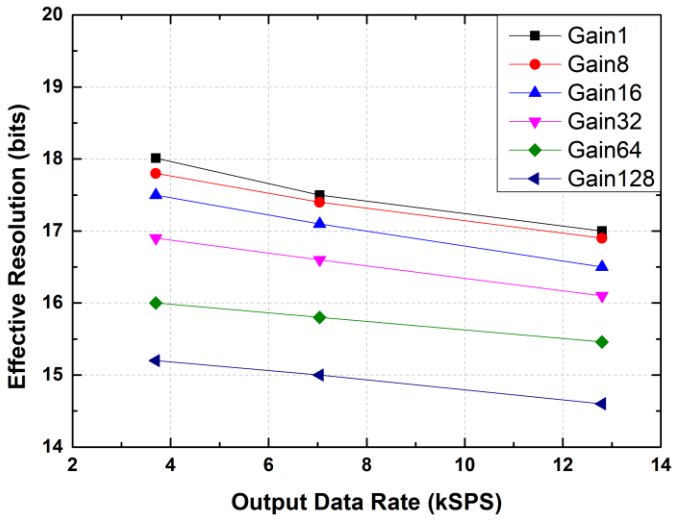


Fig. 6.2.4 Measured ER versus ODR.

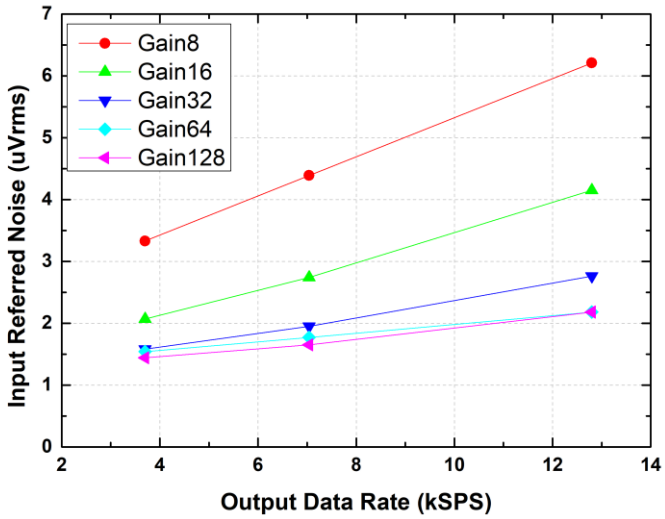


Fig. 6.2.5 Measured IRN versus ODR.

bits and 15.2 bits at 12.8 kSPS and 3.7 kSPS, respectively.

Fig. 6.2.5 shows the IRN versus ODR at each gain. In gain 8, the measured IRNs are 6.21 μVrms and 3.33 μVrms at 12.8 kSPS and 3.7 kSPS, respectively. In gain 16, the measured IRNs are 4.15 μVrms and 2.07 μVrms at 12.8 kSPS and 3.7 kSPS, respectively. In gain 32, the measured IRNs are 2.76 μVrms and 1.58 μVrms at 12.8 kSPS and 3.7 kSPS, respectively. In gain 64, the measured IRNs are 2.18 μVrms and 1.54 μVrms at 12.8 kSPS and 3.7 kSPS, respectively. In gain 128, the measured IRNs are 2.18 μVrms and 1.54 μVrms at 12.8 kSPS and 3.7 kSPS, respectively. The singularity is the IRN at the gain of 64 and the IRN at the gain of 128 are similar. Also, the graph shows that the waveform is linearly increased as OSR is doubled. This is because the DSM noise is almost negligible at a gain larger than a certain amount.

6.3 SENSOR OFFSET CANCELLATION MEASUREMENT

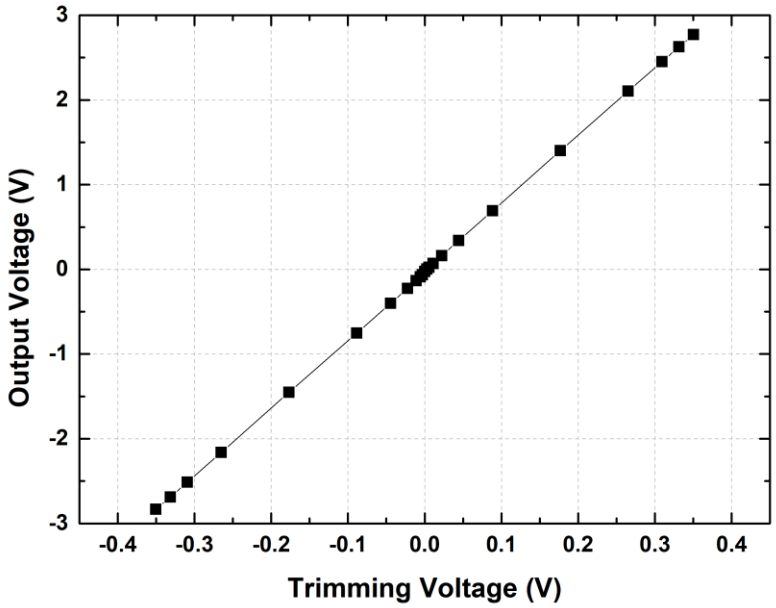


Fig. 6.3.1 Output voltages when sensor offset trimming voltage is applied.

Fig. 6.3.1 shows the offset trimming range that can be removed when an offset exists. To measure this, a common mode voltage was applied to the differential input of the IC in the state of gain x8 (0V input). After that, the +/- offset generated by the IC itself was

swept using the offset trimming cap DAC (X axis). That is, if the offset of the sensor is +350 mV, the offset is canceled by offsetting the -350 mV that the offset trimming cap DAC generates with maximum negative trimming code. If the offset of the sensor is -350 mV, the offset is canceled by offsetting the +350 mV that the offset trimming cap DAC generates with maximum positive trimming code. Then, the sensor offset is completely eliminated. Also, as can be seen from the graph, the offset removal function operates linearly. Offset trimming range is -350mV ~ 350mV, which indicates the range that can remove the offset of the sensor. Through this, Figure 6.3.1 shows that the input dynamic range +/- 370mV is achieved by adding the offset cancellation range and the signal amplitude of 20mV.

6.4 INPUT IMPEDANCE MEASUREMENT

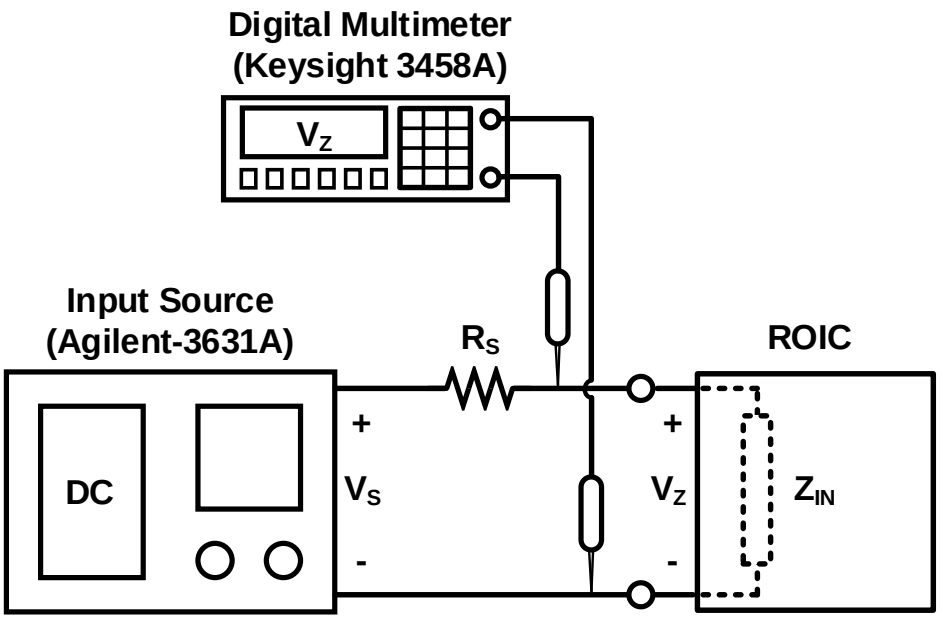


Fig. 6.4.1 Input impedance measurement setup.

Fig. 6.4.1 shows the input impedance measurement setup. Then, we can find the input impedance Z_{IN} with following equation (6.4.1),

$$Z_{IN} = \frac{V_Z}{(V_S - V_Z)} \times R_S \tag{6.4.1}$$

Where V_S is known voltage 200 mV and R_S is known resistance 1 MΩ. Then, we measure

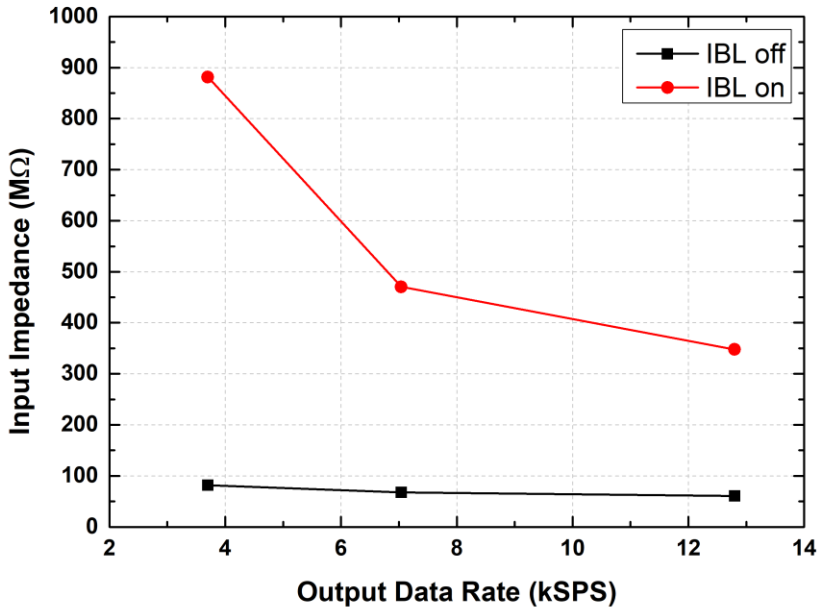


Fig. 6.4.2 Measured input impedance when IBL is on and off.

V_Z with multimeter. Since V_Z is quite small, we need to use highly accurate multimeter to measure precise input impedance of the read-out IC. Fig. 6.4.1 shows the input impedance versus ODR when the IBL is on and off. When IBL is off, the measured input impedances are 60.5 MΩ, 67.7 MΩ, and 82.0 MΩ when ODRs are 12.8 kSPS, 7.04 kSPS, and 3.7 kSPS, respectively. When IBL is on, the measured input impedances are 347.6 MΩ, 470.6 MΩ,

and 881.6 MΩ when ODRs are 12.8 kSPS, 7.04 kSPS, and 3.7 kSPS, respectively. In

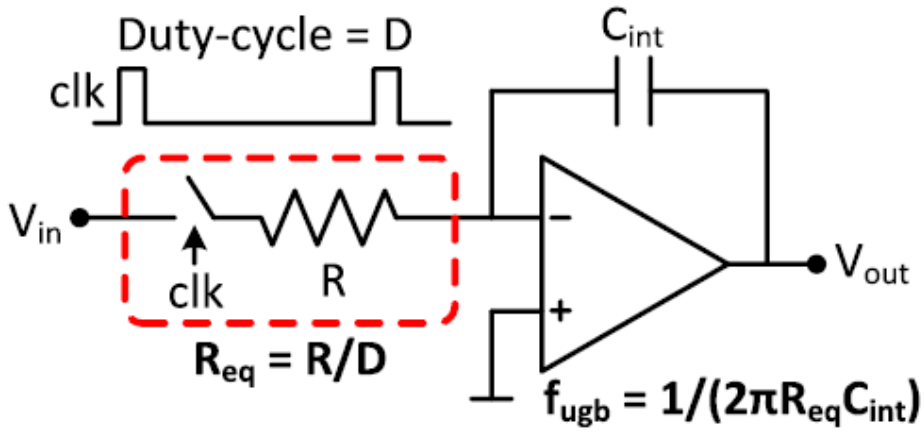


Fig. 6.4.3 Duty-cycled resistor [3.2.1].

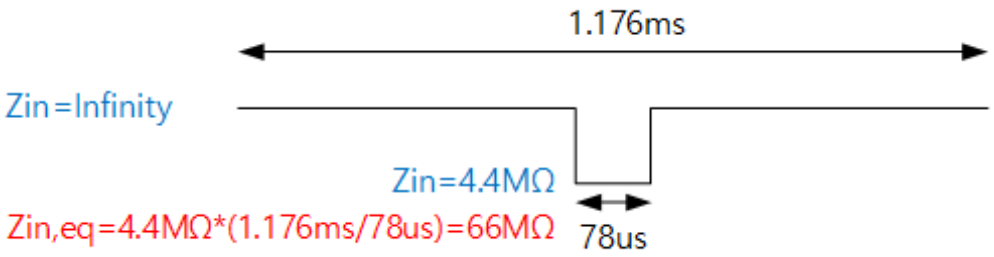


Fig. 6.4.4 Input impedance calculation.

practice, when IBL is on, the input impedance is x5 to x10 times bigger than IBL is off [1.3.7] as we have mentioned in section 3. The measurement results reflect this. On the

other hand, theoretically, CCIA's input capacitance 8.8 pF with chopping frequency 12.8 kHz, the input impedance should be 4.4 MΩ when IBL is off. However, the measured input impedance is 60.5 MΩ when IBL is off in Fig. 6.4.3. This force system turns on the sensor and read-out IC shortly and turns off for the rest of time to reduce sensor's power consumption and it makes the input impedance look like a duty-cycled resistor. Fig. 6.4.3 shows how to increase resistance with duty-cycled resistor in the paper [3.2.1]. Figure 6.4.4 shows that when we measured the read-out IC only turned on 78 μs for 1.176 ms. Then, the calculated input impedance, Z_{eq}, becomes 66 MΩ. It can be seen that this calculated value is close to the actual measured value.

6.5 TEMPERATURE VARIATION MEASUREMENT

Fig. 6.5.1 Temperature sweep measurement setup.

Fig. 6.5.1 shows the temperature drift of the read-out IC measurement setup in the chamber. The temperature is swept from -40 °C to 120 °C. In the bridge sensor system temperature drift is one of the crucial factor [1.5.6].

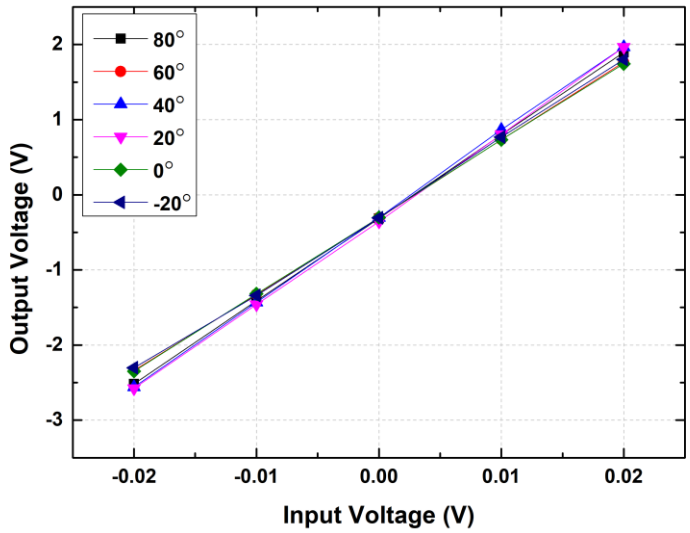


Fig. 6.5.2 Output voltage versus input voltage at each temperature (internal LDO).

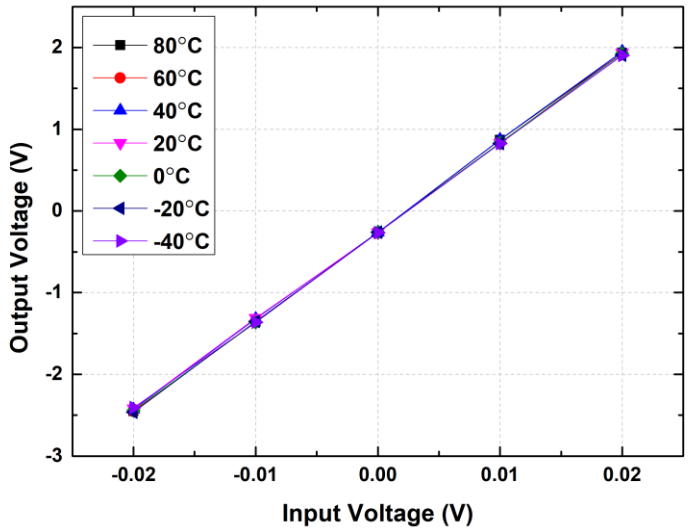


Fig. 6.5.3 Output voltage versus input voltage at each temperature (external LDO).

Fig. 6.5.2 shows the output voltage versus input voltage at each temperature in the gain of x128. In the Fig. 6.5.2, internal LDO is used and there is slight gain change at each temperature. Fig. 6.5.3 shows the same measurement with fig. 6.5.2 with external LDO. It shows that the temperature drift is much more improved compared with using internal LDO. Accordingly, it shows that the designed AFE is stable with temperature drift.

6.6 PERFORMANCE SUMMARY

The performance of the proposed read-out IC for bridge sensor system is summarized in Table 6.6.1. In the Table 6.6.1, this work is compared with other types of high resolution bridge sensor system read-out ICs. In order to quickly capture data and turn off the sensor to reduce the power consumption of the sensor, the conversion time is 0.078 μs, which is much faster than other papers. As the sensor's supply voltage is lowered, the sensor output also becomes smaller, so the gain range is wider than other papers to increase amplification. IRNs are 45 μVrms at gain 1 and 2.0 μVrms at gain 128, respectively. ERs are 17.0 bits at gain 1 and 14.5 bits at gain 128, respectively. The FOM_{MAX} achieved 163. Therefore, in the thesis, 12.8 kHz energy-efficient and high-resolution read-out IC is designed. When the performance of read-out IC is compared, it can be seen that the CCIA of the modified structure proposed in this thesis has better energy-efficient compared to other types of IA structures. The structure of the paper [1.5.3] consists of a CCIA and DT-ΔΣ ADC and it shows better performance. However, the conversion time is slow as 200 ms and because it is slow, there is no benefit to further reducing current consumption by turning off the sensor.

Table 6.6.1 Performance summary.

	This Work	[1.5.6] JSSC'19	[1.5.2] JSSC'12	[1.5.3] JSSC'19	[6.6.1] Sensors'18
Architecture	**CCIA+ DT-ΔΣ ADC**	CCIA+ CT- ΔΣ ADC	CFIA+ DT- ΔΣ ADC	CCIA+ DT- ΔΣ ADC	3OPAMP+ CT- ΔΣ ADC
CMOS Technology (μm)	**0.13**	0.18	0.7	0.13	0.18
Area (mm^2)	**1.23**	0.73	5	0.65	0.24
Supply Voltage (V)	**3 (Analog) 1.5 (Digital)**	1.8	5	3	1.8
Average Current (μA)	**117.5 (Analog) 1.3 (Digital)**	1200	270	142	36
Conversion Time (ms)	**0.078**	0.5	170	200	0.2
Gain Range	**1 ~ 128**	100	>20	1 ~ 64	40 ~ 200
IRN_{MIN} (μV)	**45 (@ gain 1) 2.0 (@gain 128)**	16.9 (@ gain100)	-	1.43 (@ gain1)	6.8 (@ gain200)
ER_{MAX} (bits)	**17.0 (@ gain 1) 14.6 (@ gain 128)**	15.4 (@ gain100)	20	21.9 (@ gain1)	12.5(@ gain 200)
+/- Input Range (V)	**2.8**	0.01	0.04	2.8	No
Sensor Offset Cancellation	**Yes**	Yes	No	No	No
$FOMS_{MAX}$* (dB)	**163**	151.1	155.5	169.3	130.6

* $FOMS_{MAX} = SNR_{MAX}$ (dB) + 10log(1/(2xPowerxConversion time))

CHAPTER 7

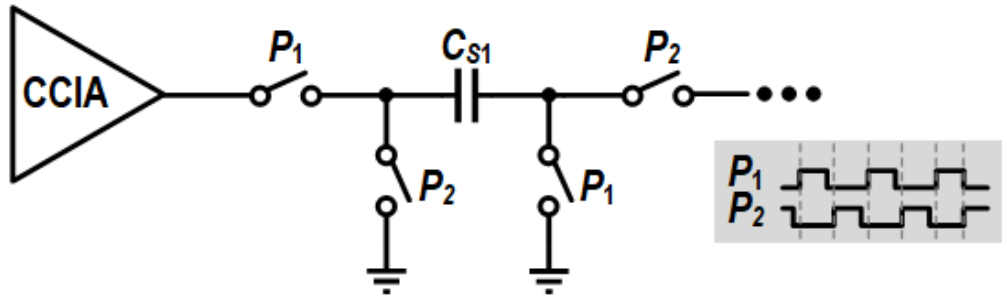
CONCLUSION

A high-precision DC measurement read-out integrated circuit (ROIC) for bridge sensor sensing system is implemented from a low-noise capacitively-coupled chopper instrumentation amplifier (CCIA) followed by a high-resolution incremental discrete-time delta-sigma modulator (DTΔΣM) analog-to-digital converter (ADC). As the small smart devices advances, the demand of high energy-efficiency of a built-in sensor system is increasingly important. The bridge sensor system is used for many sensors in smart devices such as humidity, temperature, pressure, etc. Accordingly, there have been many researches to design higher energy-efficient bridge sensor system. First, there are studies that reduce the power consumption of read-out ICs in terms of the structure of instrumentation amplifier (IA). The second method is to lower the sensor's supply voltage to lower the sensor's power consumption. In this thesis, the read-out IC has an output data rate of 12.8 kSPS, which is faster than the traditional bridge sensor system, to fill data quickly and further reduce the power consumption of the sensor by turning off the system for the rest of the time. The input referred noise, 2.0 μVrms is achieved at the gain of 128 and 14.6 bits ER is achieved.

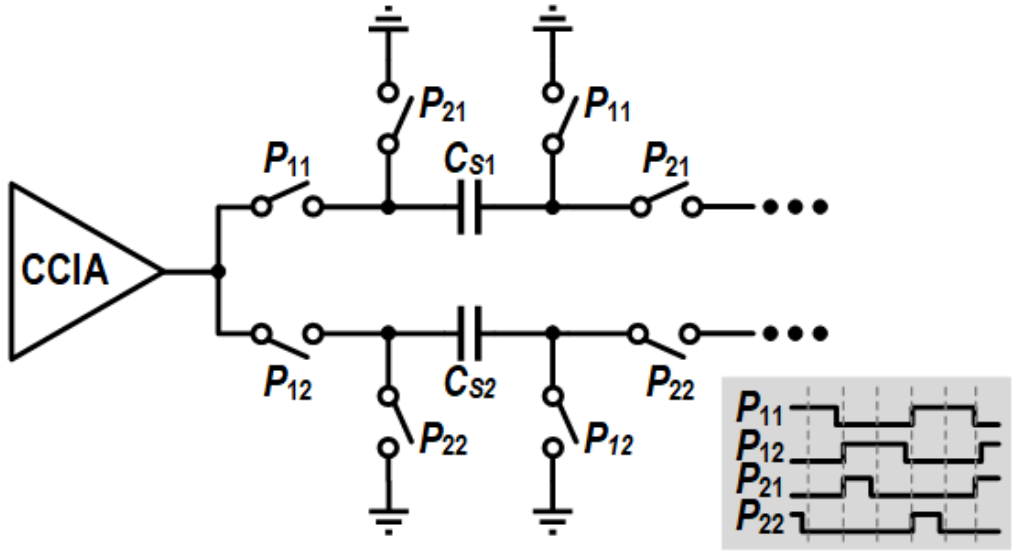
APPENDIX A. ENERGY-EFFICIENT READ-OUT IC FOR HIGH-PRECISION DC MEASUREMENT SYSTEM WITH IA POWER REDUCTION TECHNIQUE

The CCIA is being researched most actively in recent years due to its high power efficiency. The noise of a CCIA is determined by one amplifier, so that the energy efficiency is higher than the three-opamp IA and CFIA. The reason why research is active despite high energy efficiency is because the CCIA still suffers from several drawbacks such as low input impedance, output ripples, and output spikes at its chopping transitions. The output spikes of CCIA at chopping transitions should not be sampled by ADC because it is nonlinear function of the input signal and the chopping frequency is forced to $2f_s$, where f_s is ADC's sampling frequency. Then, the bandwidth is determined by ADC's sampling frequency. For complete settling, the CCIA's bandwidth needs to be wide enough or additional buffer is required, which increases noise aliasing and degrades ROIC's energy efficiency [1.5.6], [A.1].

The [1.5.6] reduces CCIA's bandwidth by using continuous-time delta-sigma modulator (CTΔΣM) instead of using discrete-time delta-sigma modulator (DTΔΣM) which is mostly used in previous papers. The input is connected to common-mode voltage when CCIA's output generates spikes. However, CTΔΣM has an inherent disadvantage of being more sensitive to clock jitter and accuracy [4.1.1] than DTΔΣM. Also, in [A.1], buffer



(a)



(b)

Fig. 0.1 Simplified block diagram of sampling and integrating operation of (a) a conventional DTΔΣM (b) a proposed doubled sampling-time DTΔΣM (single-ended circuit is assumed).

and dynamic filter are introduced to increase energy efficiency by reducing noise aliasing, but this increases design complexity and introduces the need for an additional filter.

In this paper, we describe an energy-efficient high-precision DC measurement ROIC. We propose a CCIA's bandwidth reduction scheme by using a doubled sampling-time (DST) incremental DTΔΣM. Using the proposed technique, the current consumption of the power-hungry CCIA is reduced to half compared to that of an IA followed by a conventional DTΔΣM. The sampling time of the proposed DTΔΣM is effectively doubled, while the output data rate is maintained. As the bandwidth of the CCIA is cut in half, it reduces noise aliasing generated from sampling of the ADC, which compensates for any degradation in system effective resolution and increase the energy-efficiency. In other words, the proposed technique relaxes the power-consumption burden of the IA and it can be applied to any other types of IAs in the DC measurement system.

Fig. 2 (a) shows the simplified sampling and integrating operation of a conventional DTΔΣM and single-ended circuit is assumed. In the P_1 phase, C_{S1} samples the output of the IA; afterwards, in the P_2 phase, the first integrator integrates. Fig. 2 (b) shows a simplified sampling and integrating operation of the DST incremental DTΔΣM. The switched-capacitor shows the sampling capacitors of a first integrator in proposed DTΔΣM. If the circuit is assumed as a single-ended circuit, in phase one, when P_{11} and P_{22} are high, C_{S1} does sampling and C_{S2} does integrating simultaneously. In phase two, when P_{11} is high and P_{22} is low, C_{S1} keeps sampling and C_{S2} is at rest. In phase three, when P_{12} and P_{21} are high, C_{S1} starts integrating and C_{S2} starts sampling. In phase four, P_{12} is high and P_{21} is low, the C_{S1} stops integrating and C_{S2} keeps sampling. The four-phase operation

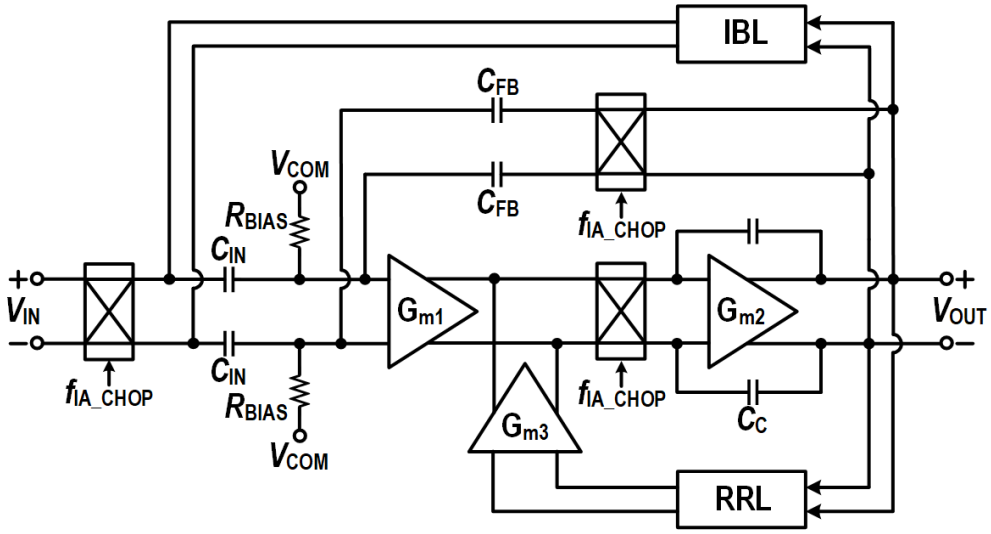


Fig. 0.2 Simplified block diagram of CCIA.

is continuously repeated until the conversion is ended when the incremental DTΔΣM's reset is high.

If the DTΔΣM performs sampling and integrating with the sequences shown in Fig. 2 (b), the sampling time is effectively doubled comparing to that of a conventional DTΔΣM while maintaining the same output data rate. Assuming that CCIA is a single pole system without slew rate limitations, the doubled sampling time halves the bandwidth BW of the CCIA, as shown in equation (A.1) [A.2]

$$BW \geq 2 \cdot (m+1) f_s \cdot \ln 2 \qquad \text{(A.1)}$$

where f_s is the sampling frequency of the DTΔΣM and m is the target resolution. The noise within $\pi/2 \bullet BW$ folds back and it increases the CCIA's in-band noise power density [1.5.6]. Then, the ROIC's energy-efficiency decreases significantly [1.5.3]. By the DST incremental DTΔΣM, the bandwidth and the power of a CCIA are reduced to half, so that the lower noise-aliasing and higher energy-efficiency effects can be obtained.

In order to implement the proposed DST DTΔΣM design, additional area is required to add the extra sampling capacitor. However, in the perspective of a system, the area of a CCIA's main amplifier can be halved, effectively compensating for the additional area of the capacitor. Also, considering the kT/C noise and the half over sampling ratio (OSR) applied to each capacitor, the RMS noise of the proposed DST DTΔΣM is nearly doubled comparing with a conventional DTΔΣM. However, in the perspective of a system, the increased noise of the DTΔΣM is negligible because the input referred noise of a system is strongly determined by the gain of a CCIA as shown in equation (2)

$$V_{n,input-referred} = \sqrt{V_{n,IA}{}^2 + \frac{V_{n,ADC}{}^2}{Gain^2}}$$

(A.2)

where $V_{n,IA}$ is the input referred noise of IA and $V_{n,ADC}$ is the input referred noise of ADC. Finally, the mismatch of two sampling capacitors is not a concern in regards to the performance of the system. Because in the proposed system, the incremental DTΔΣM is

used and the system is designed for DC signals. Therefore, the modulator's output will be averaged out accordingly.

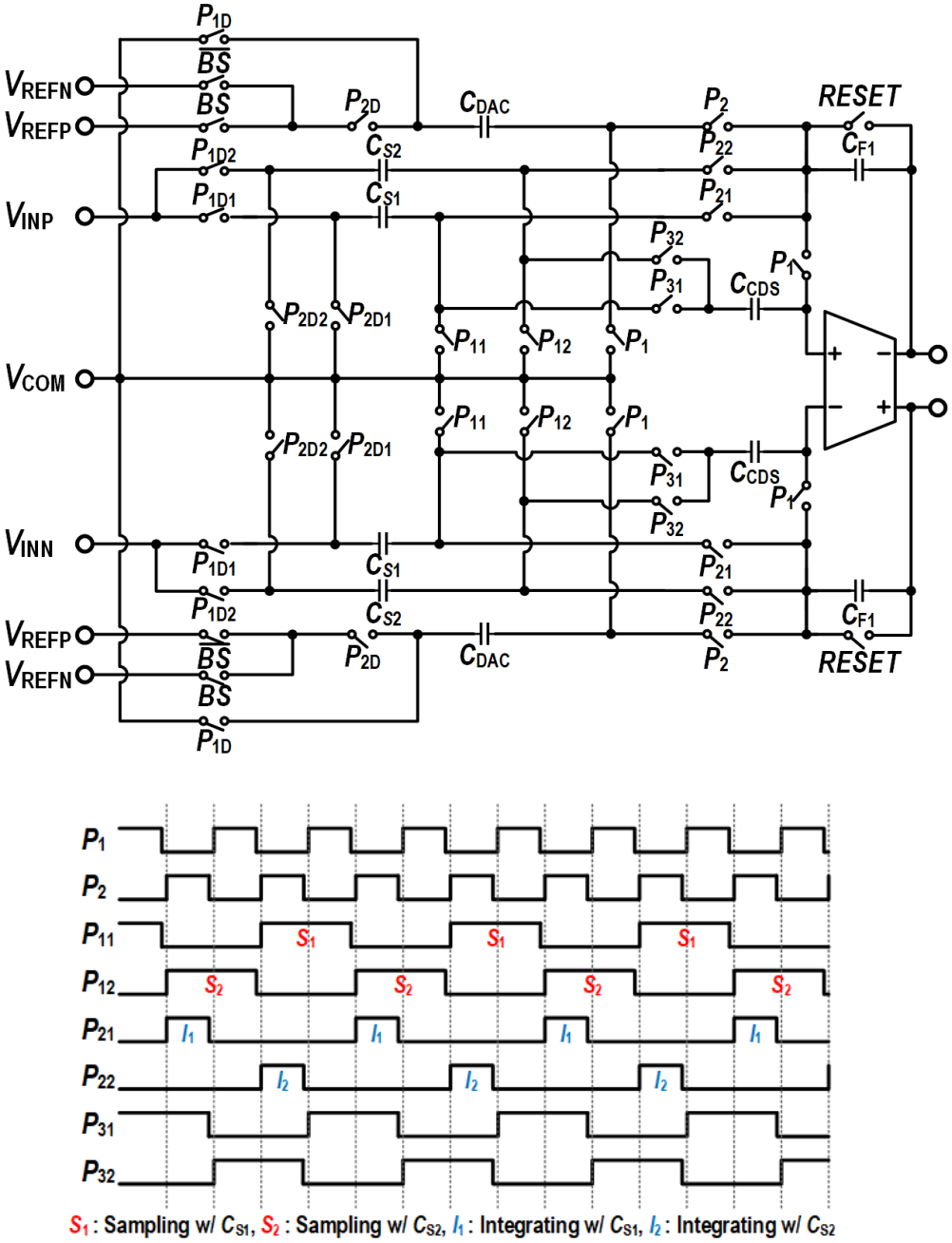


Fig. 0.3 Proposed 1st integrator of the DST DTΔΣM and clock distribution.

The Fig. 4 (a) shows the proposed first integrator in incremental DTΔΣM. The dual capacitors, C_{S1} and C_{S2}, are used as sampling capacitors to double the sampling time. P_1 and P_2 are 61.44kHz sampling and integrating clocks in the conventional DTΔΣM, respectively. Fig. 4 (b) shows the clock timing of the proposed first integrator. In the proposed scheme, the clocks P_{11} and P_{12} act as sampling clocks for C_{S1} and C_{S2}, respectively, which are 30.72 kHz. The clocks P_{21} and P_{22} are integrating clocks for C_{S1} and C_{S2}, respectively. The f_{IA_CHOP} transition occurs right after either P_{11} or P_{12} finishes sampling.

One thing to note here is that the reset and integrating time of the C_{DAC} in proposed DST DTΔΣM is same as those of the C_{DAC} in conventional DTΔΣM, which are P_1 and P_2. In the DTΔΣM, either V_{REFP} or V_{REFN} as an input to C_{DAC} is determined by the comparator's output bit-stream, *BS*, with feedback and it is not a concern with DC input in the proposed scheme. Accordingly, the C_{DAC}'s operation is exactly same as the conventional DTΔΣM.

In many cases, to reduce the $1/f$ noise of the amplifier and the offset, the correlated double sampling (CDS) technique is applied to the first integrator in DTΔΣM [A.3]. In the conventional first integrator, the offset-storage capacitor C_{CDS} stores the offset in the sampling phase and then stored offset is cancelled out in the integrating phase. However, in the proposed first integrator, there is a phase when the sampling and integrating occurs simultaneously. Because the absence of the CDS technique significantly degrades the DTΔΣM's performance, a modified CDS technique for the first integrator of the proposed DST DTΔΣM is implemented, and the effects of the modified CDS are confirmed through simulations. When P_1 is high, the bottom plate of the C_{CDS} is connected to the feedback capacitor, C_{F1}, and input of the amplifier, and the top plate is connected to either C_{S1} or C_{S2}

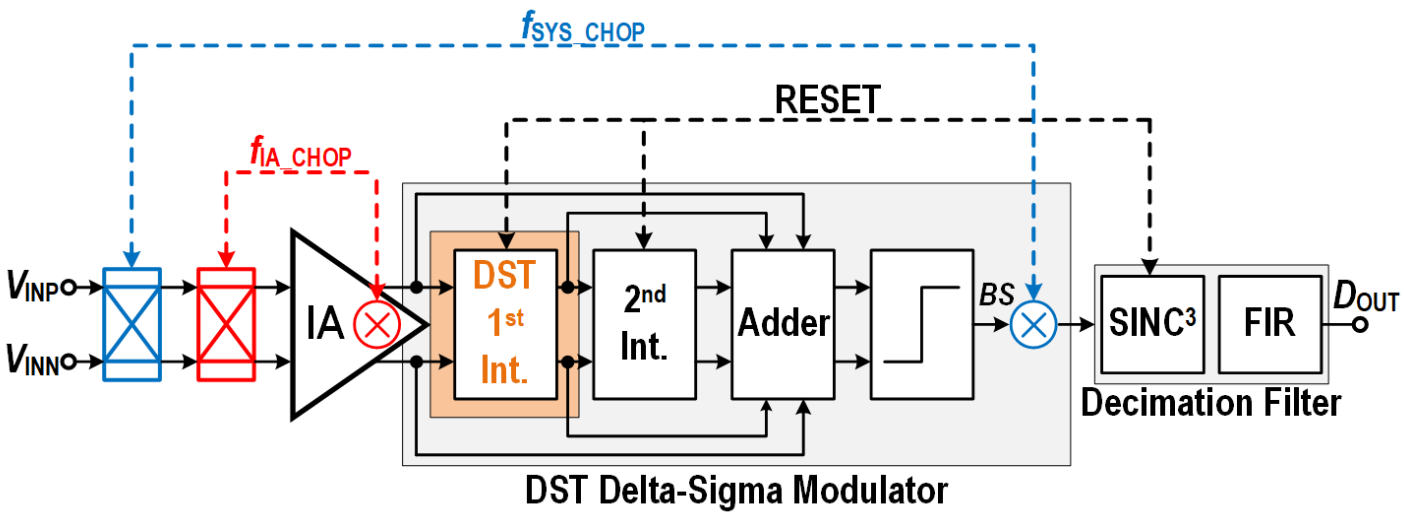


Fig. 0.4 Block diagram of the proposed system.

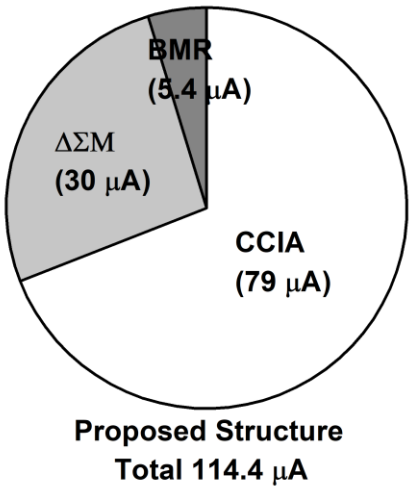


Fig. 0.5 Power distribution of the proposed ROIC.

to store the offset. When P_1 is low, bottom plate of the C_{CDS} is disconnected from C_{F1} and used for integration. The clocks P_{31} and P_{32} connect the top plate of C_{CDS} to C_{S1} and C_{S2}, alternatively. They are 1/4 delayed clocks of P_{11} and P_{12}.

Fig. 5 shows the block diagram of the entire system. It consists of a second-order system chopper, a CCIA, a DTΔΣM, and a decimation filter. The decimation filter consists of a sinc^3 filter followed by a finite impulse response (FIR) filter. Also, to reduce remaining $1/f$ noise and offset, a second-order system-level chopping is applied. The four consecutive outputs of sinc^3 are combined through a moving-average FIR filter [1.5.3].

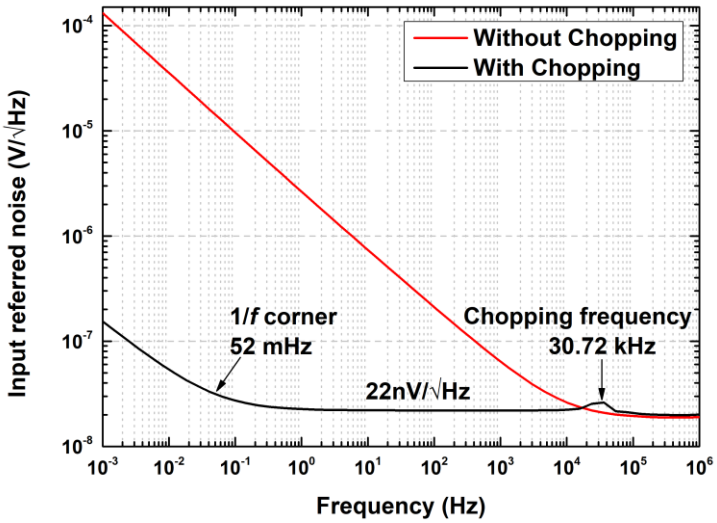


Fig. 0.6 Simulated CCIA's input-referred noise PSD.

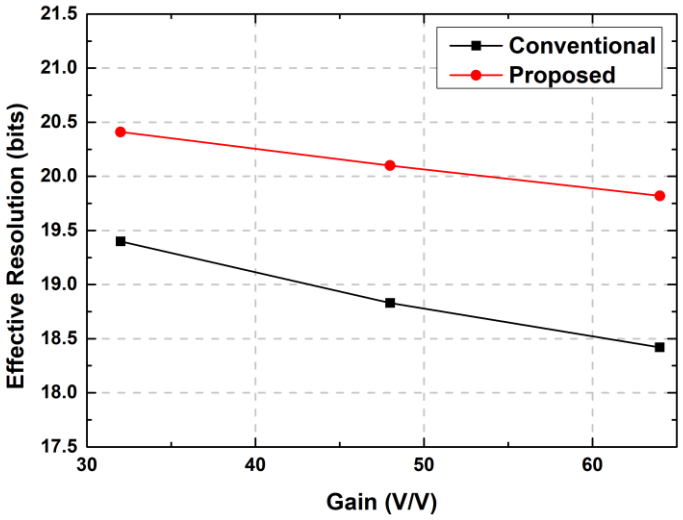


Fig. 0.7 Simulated effective resolution versus gain.

In the high gain DC measurement system, the input-referred noise is dominated by an IA's main amplifier. Accordingly, the IA takes up most of the power in the system. Fig. 6 shows the power distribution of the proposed structure. The system draws only 114.4 μA from 3-V supply. If the system's IA is followed by a conventional DTΔΣM, instead of the DST DTΔΣM, the current consumption of the IA will be increased by a factor of two, raising the total current consumption to approximately 193.4 μA.

Fig. A.6 shows the input-referred noise density of the op-amp and chopped CCIA. The offset and 1/*f* noise of G_{m1} is mitigated by chopping, and G_{m2} noise is mitigated by open-loop gain of G_{m1} from Fig. 3. As shown in Fig. 7, 1/*f* noise is sufficiently suppressed by chopping with 30.72 kHz chopping frequency and 1/*f* corner is 52 mHz. The 1/*f* corner is further decreased through second-order system level chopping. Also, the simulation shows that the CCIA achieves an input-referred noise density of 22 nV/√Hz.

Fig. A.7 shows the effective resolution (ER) of the proposed system. To prove the effects of the proposed DST DTΔΣM, we have designed a conventional DTΔΣM (DST off) and have applied the DST technique to the conventional DTΔΣM (DST on). The ERs of the DST off mode are 19.4, 18.8, and 18.4 bits at the gains of 32, 48, and 64, respectively. The ERs of the DST off mode are 20.4, 20.1, and 19.8 bits at the gains of 32, 48, and 64, respectively. In the DST off mode, the unit gain bandwidth of the CCIA is 7 MHz while that of the DST on mode is 3.5 MHz. As we have explained in section II, at the gain of 1, the ER of the DST off mode is nearly 1 bit higher than that of the DST on mode. However, in the perspective of the system, with half current consumption of the CCIA, the ERs are even higher at the high gains in the DST on mode due to the lower noise-aliasing. The table

I shows that the proposed system shows outstanding performance in the system figure of merit (FOM).

Table A.1 Performance summary.

	This work	**[7] JSSC' 19**	**[13] ISSCC' 18**	**[6] JSSC' 19**
Architecture	CCIA+ DTΔΣM	CCIA+ DTΔΣM	CCIA+ DTΔΣM	CCIA+ CTΔΣM
Technology (μm)	0.13	0.13	0.13	0.18
Supply voltage (V)	3.0	3.0	3.0	1.8
Supply current (μA)	114.4	142	326	1200
Conversion time (ms)	200	200	200	0.5
Gain range	1 ~ 64	1 ~ 128	1 ~ 128	100
+/- Input range (V)	2.8	2.8	2.8	0.01
ER (bits)	19.8 (gain 64)	19.6 (gain 64)	19.0 (gain 64)	15.4 (gain 100)
NEF of IA	7.4	6.6	10.5	4.5
FOM (dB) of read-out IC*	160 (gain 64)	157 (gain 64)	150 (gain 64)	155.5 (gain 100)

*FOM (dB)=SNR+10log(1/(2×Power×Conversion time))

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한글초록

본 논문에서는 고정밀 브리지 센서 센싱 시스템을 위한 에너지 효율이 높은 Read-out Integrated Circuit (read-out IC)를 제안한다. 저 잡음 Capacitively-Coupled Instrumentation Amplifier (CCIA)에 이은 고해상도 Discrete-time Delta-Sigma 변조기(DTΔΣM) 아날로그-디지털 변환기(ADC)를 구현하였다.

에너지 효율을 높이기 위해 IA 유형 중 에너지 효율이 가장 높은 CCIA를 선택하였다. CCIA는 브리지 센서의 작은 출력을 증폭할 수 있는 1 에서 128의 프로그래밍 가능한 전압 이득을 가진다. CCIA의 단점인 낮은 입력 임피던스를 보상하기 위해 Impedance Boosting Loop (IBL)을 적용하였다. 또한 CCIA에 센서 오프셋 제거 기술을 적용하여 브리지 센서의 저항 미스매치로 인한 오프셋을 제거 기능을 탑재하였으며 -350mV에서 350mV까지 브리지 센서 오프셋을 제거할 수 있다. Read-out IC의 출력 데이터 전송률은 12.8kHz로 설계하여 데이터를 빠르게 채고 나머지 시간 동안 센서와 read-out IC를 꺼서 센서의 전력 소비를 줄일 수 있도록 설계하였다. 일반적으로 브리지 센서 시스템은 12.8kHz보다 느리기 때문에 이것이 가능하다. 하지만, 일반적인 CCIA는 입력 임피던스 때문에 빠른 속도에서 설계가 불가능하다. 이를 해결하기 위해 demodulate 차핑을 앰프 내부가 아닌 시스템 차핑을 이용해 해결하였다.

1/*f* 노이즈를 억제하기 위해 시스템 레벨 차핑 및 상관 이중 샘플링(CDS)

기술이 사용되었다. 0.13μm CMOS 공정에서 구현된 read-out IC의 Effective Resolution (ER)은 전압 이득 1에서 17.0비트이고 전압 이득 128에서 14.6비트를 달성하였다. 아날로그 회로는 3 V 전원에서 139.4μA의 평균 전류를, 디지털 회로는 1.8 V 전원에서 60.2μA의 평균 전류를 사용한다.

주요어 : 스마트 장치, capacitively-coupled chopper instrumentation amplifier (CCIA), 휘트스톤 브리지 센서, 1/*f* 잡음, system-level chopping, incremental delta-sigma analog-to-digital converter (ADC), 센서 오프셋, 임피던스 부스팅

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