PH.D. DISSERTATION

A DESIGN OF QUARTER-RATE PAM-4 RECEIVER FOR MEMORY INTERFACES

메모리 인터페이스를 위한 4 레벨 펄스 진폭 변조 쿼터 레이트 수신기 설계

BY

HYUNKYU PARK

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DEPARTMENT OF ELECTRICAL AND
COMPUTER ENGINEERING
COLLEGE OF ENGINEERING
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지도교수 김 수 환

이 논문을 공학박사 학위논문으로 제출함

2022 년 8 월

서울대학교 대학원

전기·정보공학부

박 현 규

박현규의 공학박사 학위논문을 인준함

2022 년 8 월

위 원 장 : 정 덕 균 (印)
부위원장 : 김 수 환 (印)
위 원 : 김 재 하 (印)
위 원 : 최 우 석 (印)
위 원 : 채 주 형 (印)

ABSTRACT

A DESIGN OF QUARTER-RATE PAM-4 RECEIVER FOR MEMORY INTERFACES

HYUNKYU PARK
DEPARTMENT OF ELECTRICAL AND
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A four-level pulse amplitude modulation (PAM-4) receiver, and a quadrature signal corrector (QSC) that generates quadrature clocks for memory interfaces is presented. Increasing IP traffic in data centers has increased the demand for high-speed and low-power memory interfaces. To satisfy this demand, PAM-4 signaling, which can increase data-rate without increasing clock and Nyquist frequency, is considered as one of signalings to be used for next-generation memory interfaces.

PAM- signaling has three-times smaller vertical margin than non-return-to-zero (NRZ) signaling, which makes the clock-to-Q delay of the slicer in the decision feedback equalizer (DFE) increases. This makes the DFE difficult to satisfy the timing constraint. In this paper, by using a DFE with inverter-based summers, the clock-to-Q delay of the slicer can be

reduced without increasing the power consumption of the slicers.

Also, the QSC using an adaptive delay gain controller can correct the skew between the quadrature clock with low skew and short correction time.

The prototype receiver including the DFE with the inverter-based summer and the QSC using the adaptive delay gain controller was fabricated in 65 nm CMOS process. The prototype chip can achieve a bit error rate (BER) of 10^{-12} at 24 Gb/s/pin, and at this time, an eye width of 100 mUI is secured. The efficiency of the receiver is 0.73 pJ/b. In addition, the QSC cna reduce the maximum 21.2 ps of skew between 3 GHz quadrature clocks to 0.8 ps and has a correction time of 76.9 ns. The efficiency of the QSC is 2.15 mW/GHz.

Keywords: Memory interface, four-level pulse amplitude modulation (PAM-4) receiver, inverter-based summer, quadrature signal corrector (QSC).

Student Number: 2014-22560

CONTENTS

LIST OF FIGURES

LIST OF TABLE

CHAPTER 1

INTRODUCTION

1.1 MOTIVATION

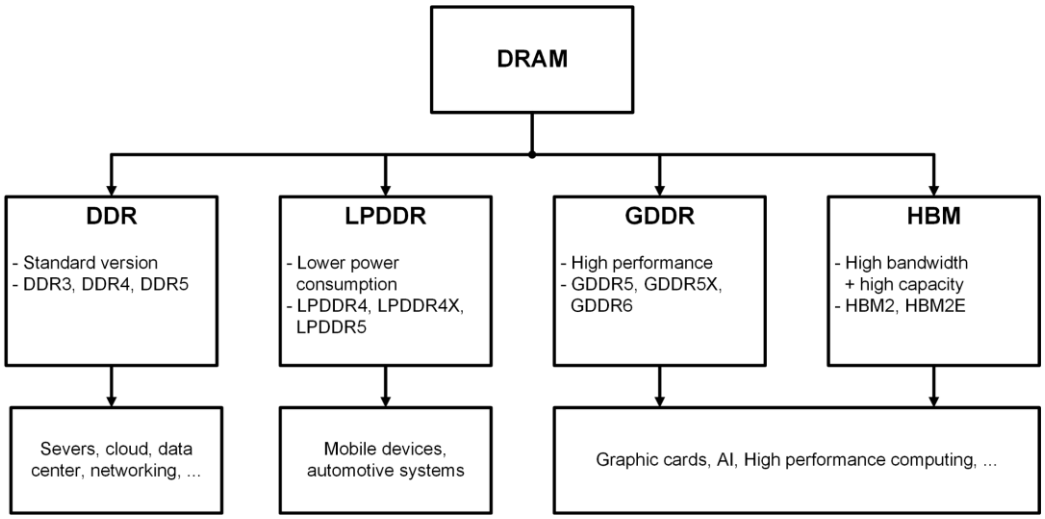


Figure 1.1.1. Four types of DRAM.

Dynamic random-access memory (DRAM) is a type of random-access memory that stores data using cells that are composed of a transistor and capacitors. Figure 1.1.1 shows the type of DRAM. The DRAM is divided into four types depending on the applications: double data rate (DDR) synchronous DRAM (SDRAM) for general purposes, low power

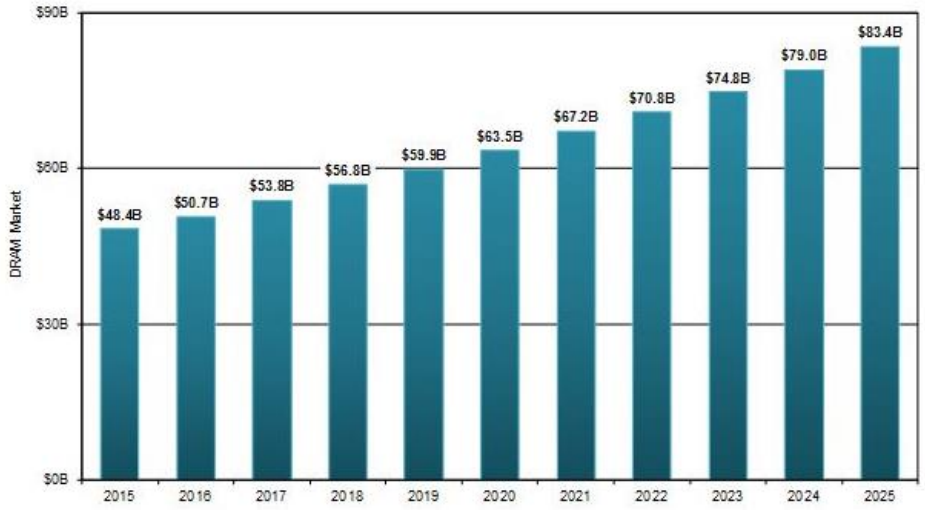


Figure 1.1.2. Growth of DRAM market [1.1.2].

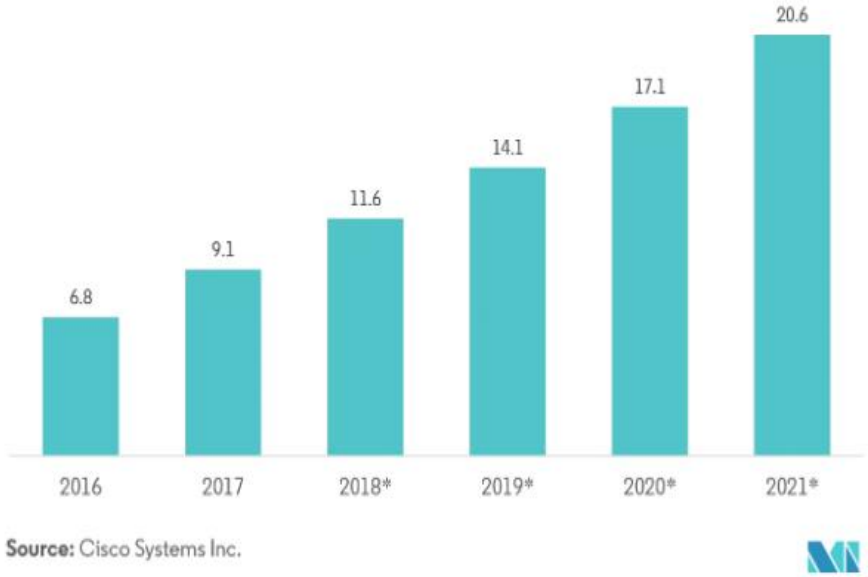


Figure 1.1.3. Growth of IP traffic in data centers.

DDR (LPDDR) SDRAM for low power application such as mobile application, graphics DDR (GDDR) SDRAM for high performance with high data-rate [1.1.1] , and high

bandwidth memory (HBM) for higher throughput [1.1.3]. As shown in figure 1.1.1, DRAMs are used in various applications.

Figure 1.1.2 shows transition in DRAM market from 2015 to 2025 (estimated). This demand is expected to continue to increase as the application of DRAM is expanded. The DRAM market is expected to increase about twice compared to 2015.the growth of IP

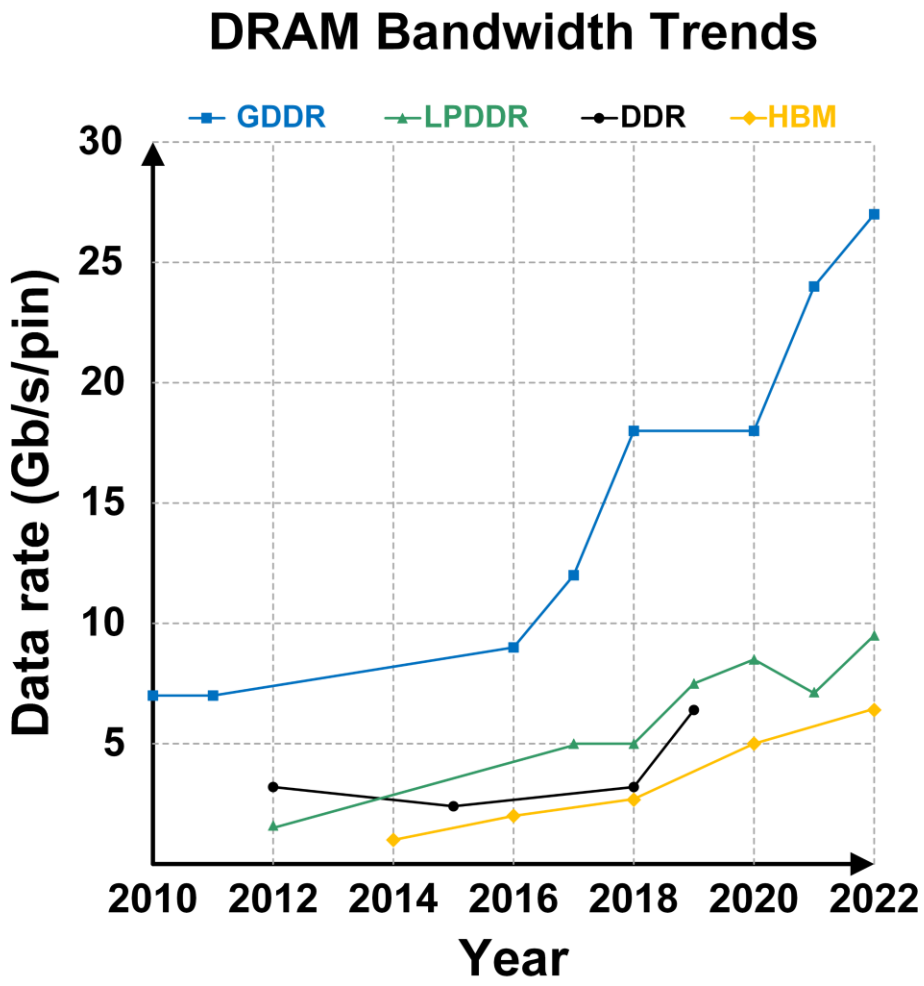


Figure 1.1.2. DRAM bandwidth trends.

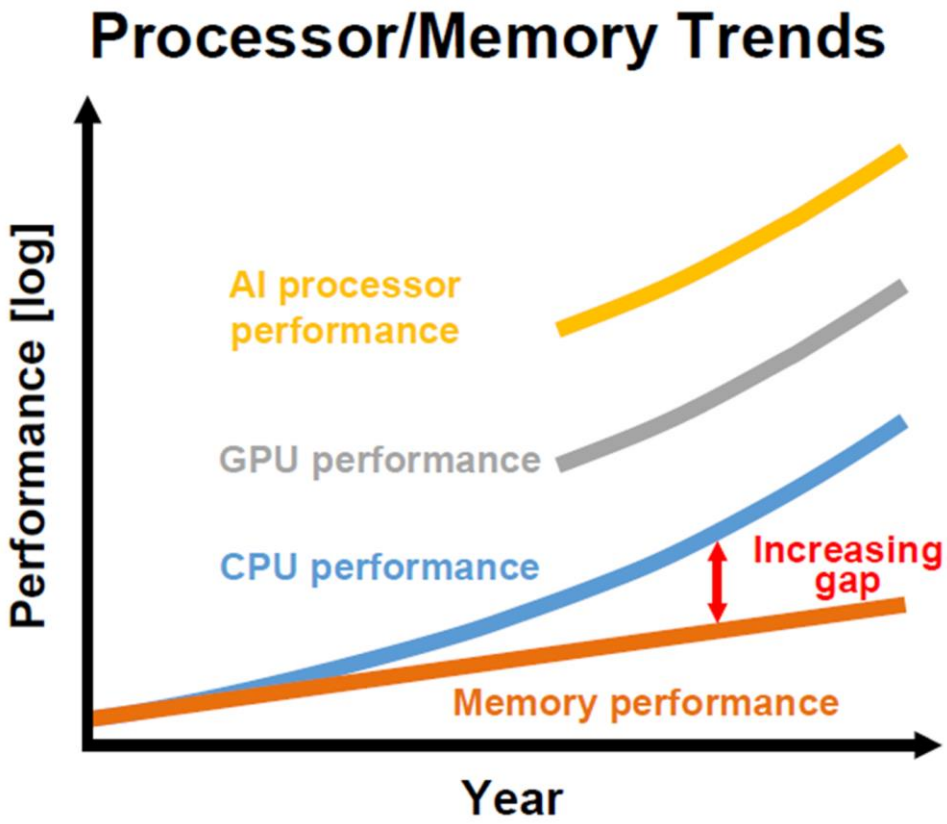


Figure 1.1.3. Performance gap between processor units and memory.

traffic in data center from 2016 to 2021. Fig 1.1.3 shows the change of IP traffic from 2016 to 2021. As demand for internet on things (IoT), cloud platform, artificial intelligence, and autonomous vehicle increases, IP traffic in data centers is increasing, which means that the the amount of data to be processed in DRAM also increase. Considering figure 1.1.2 and figure 1.1.3, the demand is expected to continue to increase. Figure 1.1.4 shows the IO bandwidth of DRAMs since 2010 in previous papers. To satisfy the increasing amount of data to be processed, the bandwidth of DRAM is steadily growing. However, As shown in Figure 1.1.5, the bandwidth of DRAM cannot satisfy the performance of processor. The

performance of DRAM is considered as the bottleneck because of the performance gap between the processors and DRAMs.

The process shrink of DRAM processes has increased the performance of DRAM. Process shrink has advantages of increasing density of the memory cell and bandwidth of DRAM I/O. However, since the speed of process shrink is slowing, there is a limit to improving the bandwidth through process shrink.

Parallelizing I/O is one of the method to improving the bandwidth of DRAMs. This method increases the number of I/O, which can increase throughput of entire memory system without increasing data rate per pin. However, the method inevitably increases the number of pins [1.1.4]. Since the memory interface have the limited number of pin count, this method can be applied to only specific applications.

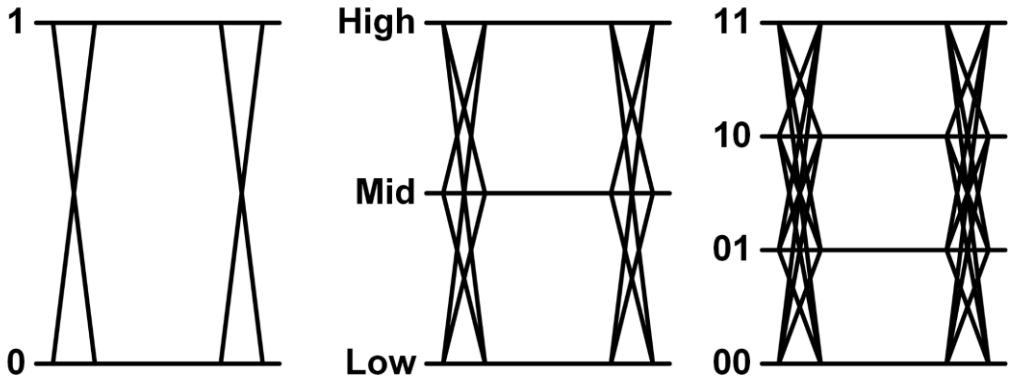
These two methods have improved the performance of DRAM, there is limitation in next generation DRAMs. To improve bandwidth of DRAMs, data-rate per pin has been increased for many years, which is shown as in figure 1.1.4.

The memory interfaces are more vulnerable to channel loss as data-rate is increased. Inter-symbol interference (ISI) caused by channel loss degrades the signal integrity of the interface. In addition, improving data-rate per pin needs to increase clock frequency. However, increasing clock frequency is limited by DRAM process [1.1.5]. To reduce the effect of channel loss and increase data-rate without increasing clock frequency, two methods have been attracting attention: Four-level pulse amplitude modulation (PAM-4), and multi-phase clocking.

To reduce ISI, equalization in transmitters and receivers must be performed. Since the

power efficiency of the transmitter-side equalization is worse than that of receiver-side equalization [1.1.6], we focus on the receiver-side equalization.

1.2 PAM-4 SIGNALING



(a) (b) (c)

Figure 1.2.1. Eye diagram of (a) NRZ, (b) PAM-3 and (c) PAM-4 signaling.

As mentioned in 1.1, data-rate of memory interfaces is increasing steadily. However, the present memory interfaces using non-return-to-zero (NRZ) signaling have limitations in increasing the bandwidth due to low-performances DRAM processes and increased channel loss as the data rate increases [1.1.5], [1.2.1]. To solve the limitation, various signalings have been proposed. Figure 1.2.1 shows eye diagrams of the signals. Figure 1.2.1 (a) shows the eye diagram of NRZ signaling. NRZ signaling transmits and receives one-bit data by using two signal levels in unit interval (UI). Figure 1.2.1 (b) is the eye diagram of PAM-3 signaling. The signaling uses three signal level to transmit and receive three bits in two UI. Compared to NRZ signaling, 1.5 bits in one UI can be contained by using PAM-3 signaling. Figure 1.2.1 (c) shows the eye diagram of PAM-4 signaling. The signal can contain two bits in one UI by using four different signal levels.

Figure 1.2.2 shows an example of comparison between NRZ and PAM-3 signaling.

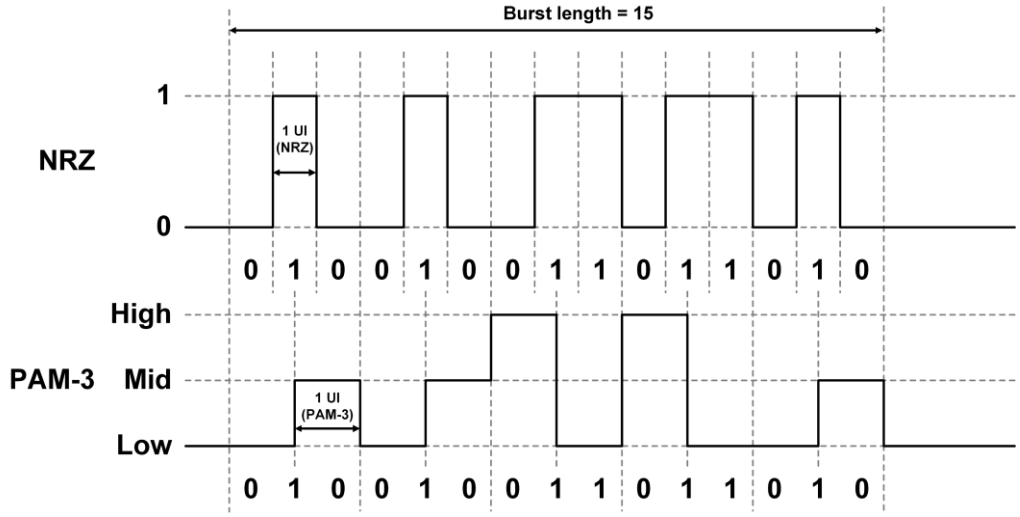


Figure 1.2.2. Comparison between NRZ and PAM-3 signaling.

At the equal data-rate, PAM-3 signaling has 1.5 times wider data width by encoding three bits of data to two UI with three signal levels. Therefore, PAM-3 signaling has 1.5 times lower clock and Nyquist frequency than NRZ signaling. However, in [1.2.2], the encoder and decoder for PAM-3 signaling makes PAM-3 transceivers complex since data in one UI is not integer.

Figure 1.2.3 shows an example of comparison between NRZ and PAM-4 signaling. PAM-4 signaling has two times wider data width than NRZ signaling, which has two times lower clock and Nyquist frequency than NRZ signaling. For PAM-4 signaling, unlike PAM-3 signaling, data contained in one UI is integer (two), PAM-4 transceiver has less complicated structure than PAM-3 transceiver. Also, PAM-4 signaling alleviates the effect of channel loss more than PAM-3 since the Nyquist frequency of PAM-4 signaling is lower than that of PAM-3 signaling [1.2.3]. In summary, PAM-4 signaling is more attractive option than PAM-3 signaling for the memory interfaces in terms of clock and Nyquist

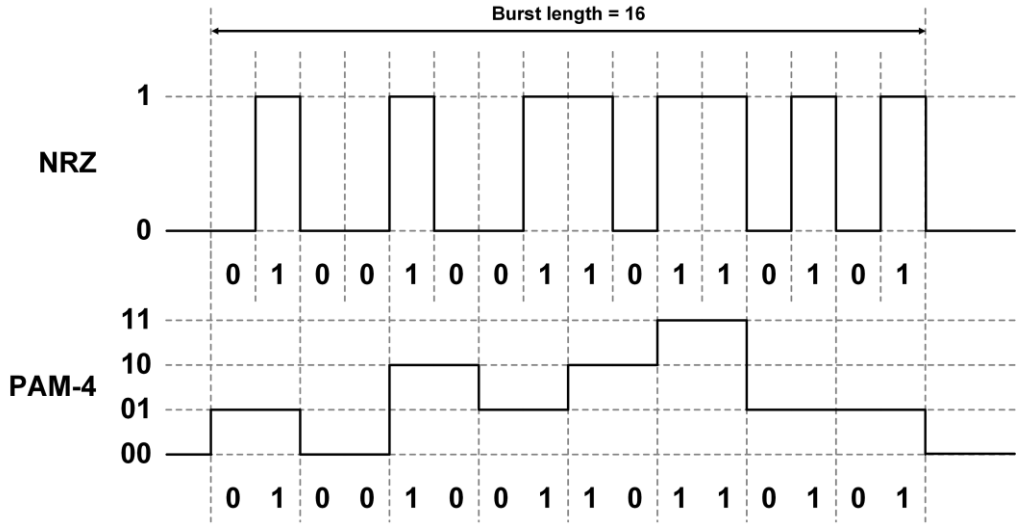


Figure 1.2.3. Comparison between NRZ and PAM-4 signaling.

frequency, complexity of transceiver, and the loss of channel.

Compared to NRZ signaling, PAM-3 and PAM-4 signaling have smaller eye height if the peak-to-peak swings of the signals are the same, as shown in Figure 1.2.1. Especially, PAM-4 signaling has eye height which is three times smaller than NRZ signaling. This means that PAM-4 signaling is more vulnerable to noise and ISI.

1.2.1 DESIGN CONSIDERATIONS ON PAM-4 RECEIVER

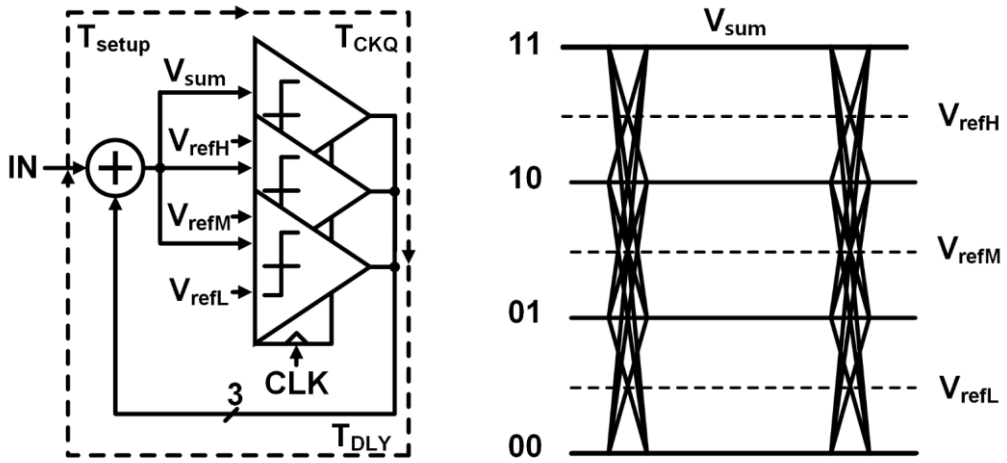


Figure 1.2.1.1. Block diagram of PAM-4 DFE with timing parameter and output of summer.

As mentioned in 1.2, PAM-4 signaling has a disadvantage of vulnerability to noise and ISI. Since decision feedback equalizer (DFE) can compensate for ISI in the signals without amplifying the noise, the DFE is an attractive option for PAM-4 receivers. Figure 1.2.1.1 shows simplified block diagram of the PAM-4 DFE and the timing parameters on the DFE. The PAM-4 DFE consists of a summer to equalize input data, three slicers to decide data. Three reference voltages (V_{refH}, V_{refM}, V_{refL}) are used for the slicers. The timing constraint must be satisfied for the PAM-4 DFE to decide current data based on previous data, which can be expressed as follow:

$$T_{setup} + T_{CKQ} + T_{DLY} < 1 \text{ UI} \quad (1.2.1.1)$$

where T_{setup} is the setup time of the slicers, T_{CKQ} is the clock-to-Q delay of the slicers, and

T_{DLY} is the delay of signal path from the slicer to the summer. As shown in (1.2.1.1), T_{CKQ} is one of the factor that determines the data-rate of the DFE.

The sensitivity is defined as the minimum swing of the input signal which the slicers

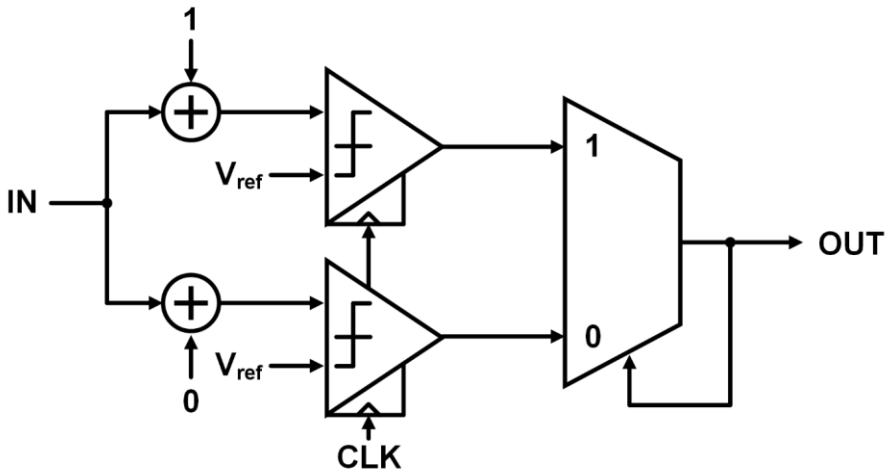


Figure 1.2.1.2. Loop unrolling DFE for NRZ signaling

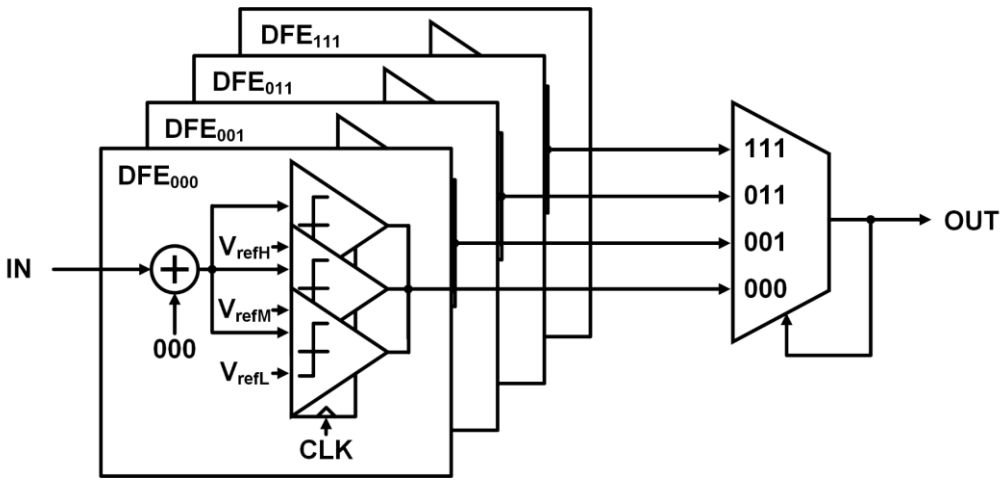


Figure 1.2.1.3. Loop unrolling DFE for NRZ signaling

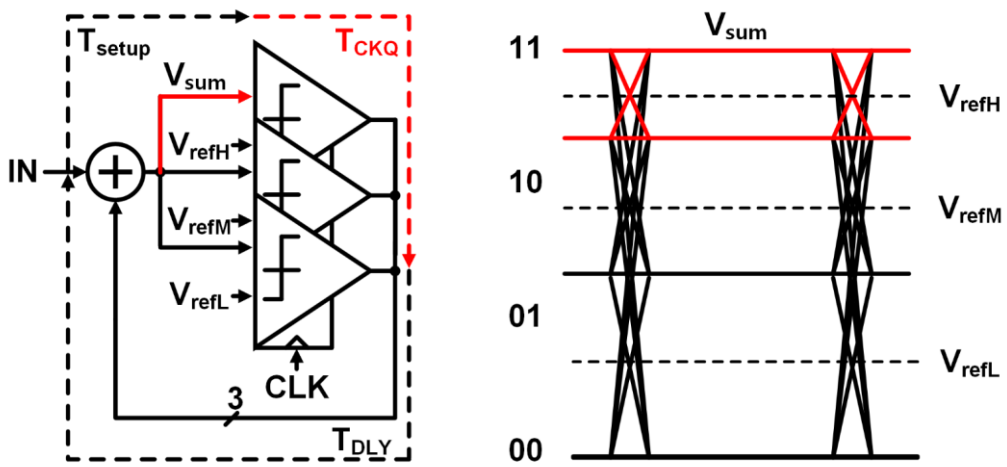


Figure 1.2.1.4. Timing constraint of PAM-4 DFE with non-ideal case.

need to compare data within one UI at specific baud-rate [1.2.1.1]. Since the equalization can be performed after the outputs of all slicers for previous data come out, T_{CKQ} in (1.2.1.1) is determined by the slowest slicer between the slicers. Based on (1.2.1.1), as data-rate increases, the sensitivity which is required for the slicers in the DFE increases. In the previous PAM-4 DFE, the linearity of the summers and clock-to-Q delay of the slicers must be considered simultaneously. However, the linearity limits the clock-to-Q delay.

To reduce the effect of the clock-to-Q delay, DFEs for NRZ signaling have used loop unrolling, as shown in Figure 1.2.1.2. the DFEs equalize current data assuming that the previous data is 0 or 1 and choose the one of the equalizations. Since the equalization can be performed before the decision of previous data, the constraint on the clock-to-Q delay of slicer can be mitigated. However, since previous data has two cases, the number of summer and slicer is doubled. As shown in Figure 1.2.1.3, because PAM-4 signaling has four signal levels, applying the loop unrolling to the PAM-4 DFE increases the number of

the slicers and the summers by four times. The increased slicers and summer increase the area and power consumption of the PAM-4 receiver, which is difficult to apply to the memory interface.

Figure 1.2.1.4 shows the timing constraint of the DFE in ideal non-ideal environment and the output of summer. Compared to figure 1.2.1.1, the clock-to-Q delay of the slicer corresponding to V_{refL} is shorter than that of figure 1.2.1.1. However, clock-to-Q delay of the slicer corresponding to V_{refH} is prolonged, because the height of the lowest eye is smaller. Therefore, overall clock-to-Q delay of the PAM-4 DFE is worsened by non-linearity of the summer in the DFE. The linearity of the summer is an important factor to increase the performance of the DFE.

1.2.2 PRIOR WORKS

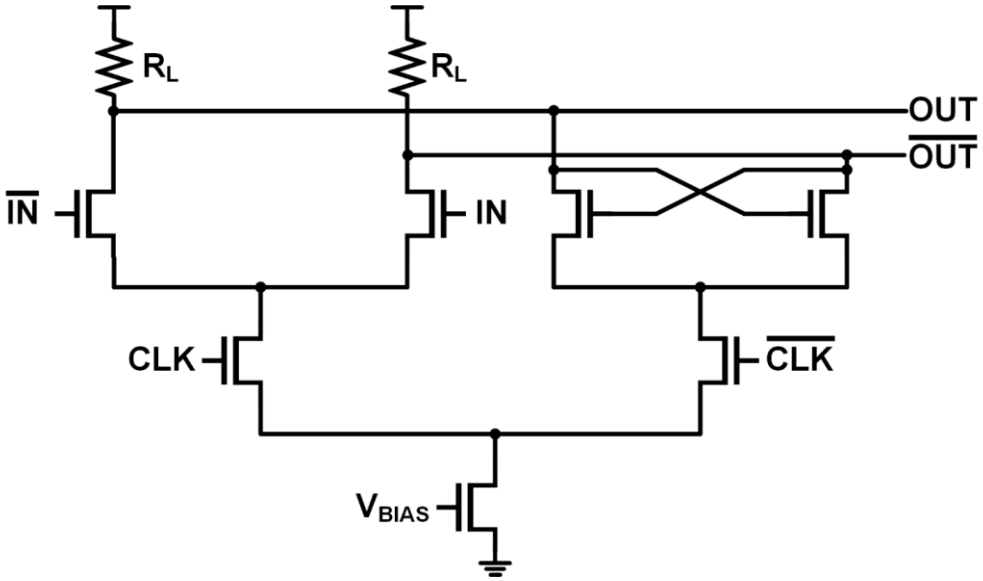
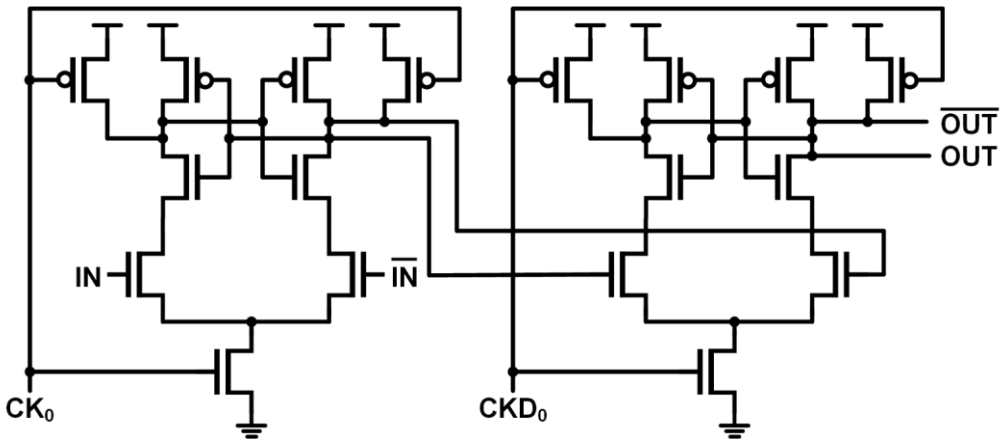


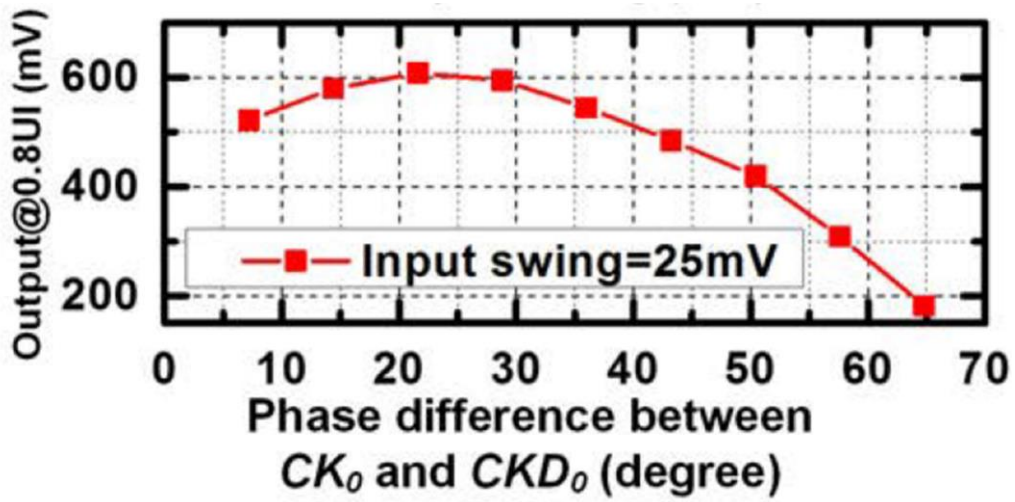
Figure 1.2.2.1. Block diagram of CML slicer.

Some methods have been proposed to solve the problem caused by the reduced eye height. The methods have focused on improving clock-to-Q delays of slicers.

Figure 1.2.2.1 shows a block diagram of current mode logic (CML) slicer [1.2.1.1]. The CML slicer consists of two parts: a part for tracking and the other part for holding. At CLK is high, the slicer tracks the input signal with a gain determined by load resistors (R_L) and the transconductance of input transistors. At CLK is low, the slicer amplifies the output after tracking by using positive feedback. The CML slicer has shorter clock-to-Q delay than the conventional StrongArm slicer. However, since the CML slicer uses a static current source, the slicer consumes more power than the StrongArm slicer. Also, the output swing of the CML slicer is limited, an additional CML-to-CMOS stage is needed, which increases



(a)



(b)

Figure 1.2.2.2. (a) Block diagram of two-stage sense amplifier and (b) relationship between output swing and phase difference between two stages [1.2.2.1].

the power consumption.

Another method is to use two-stage slicers. One of the slicers is two-stage sense amplifiers (TSSAs), used in [1.2.2.1], is shown as figure 1.2.2.2 (a). TSSA is composed of two StrongArm slicers. This method can improve the clock-to-Q delay of the slicers by

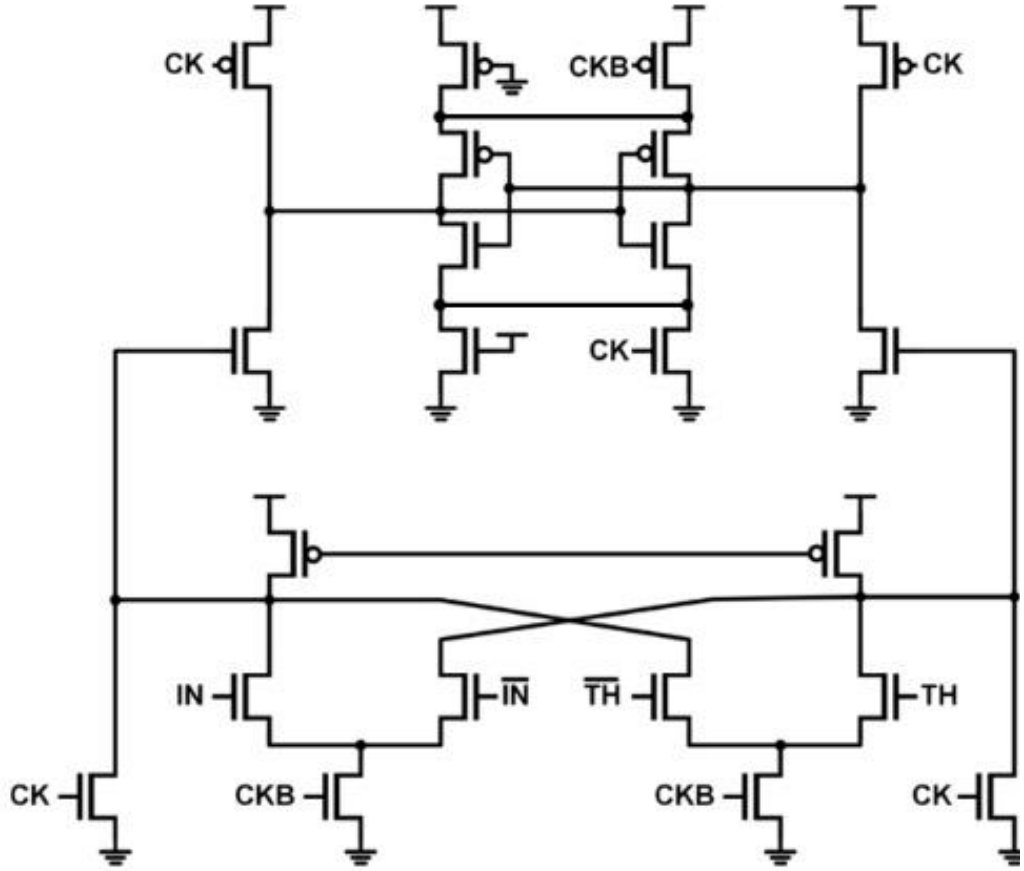


Figure 1.2.2.3. Block diagram of track-and-regenerate slicer.

increasing the gain of the slicer. However, to maximize the gain of the slicer, two clock phases are needed as shown in Figure 1.2.2.2 (b). An additional block for phase adaptation is needed to generate the two clocks, which draws an increase in power consumption.

Fig 1.2.2.3 is a track-and-regenerate slicer used in [1.2.1.1]. The slicer consists of two stages: first stage for tracking the input signal and second stage for regenerating the output of the first stage. Compared to CML slicer, track-and-regenerate slicer has an advantage that the slicer does not use static current source, which reduce power consumption.

However, the slicer has higher power consumption than the conventional StrongArm slicer [1.2.1.1].

As mentioned, previous methods solve the problem of the timing constraint of PAM-4 DFEs by using high-performance slicers. However, the slicers or additional blocks increase the power consumption of the PAM-4 receiver. Also, the clock-to-Q delays of the slicers still depend on the input swing of the slicers, output eye height of the summer in the PAM-4 DFE.

1.3 QUARTER-RATE ARCHITECTURE

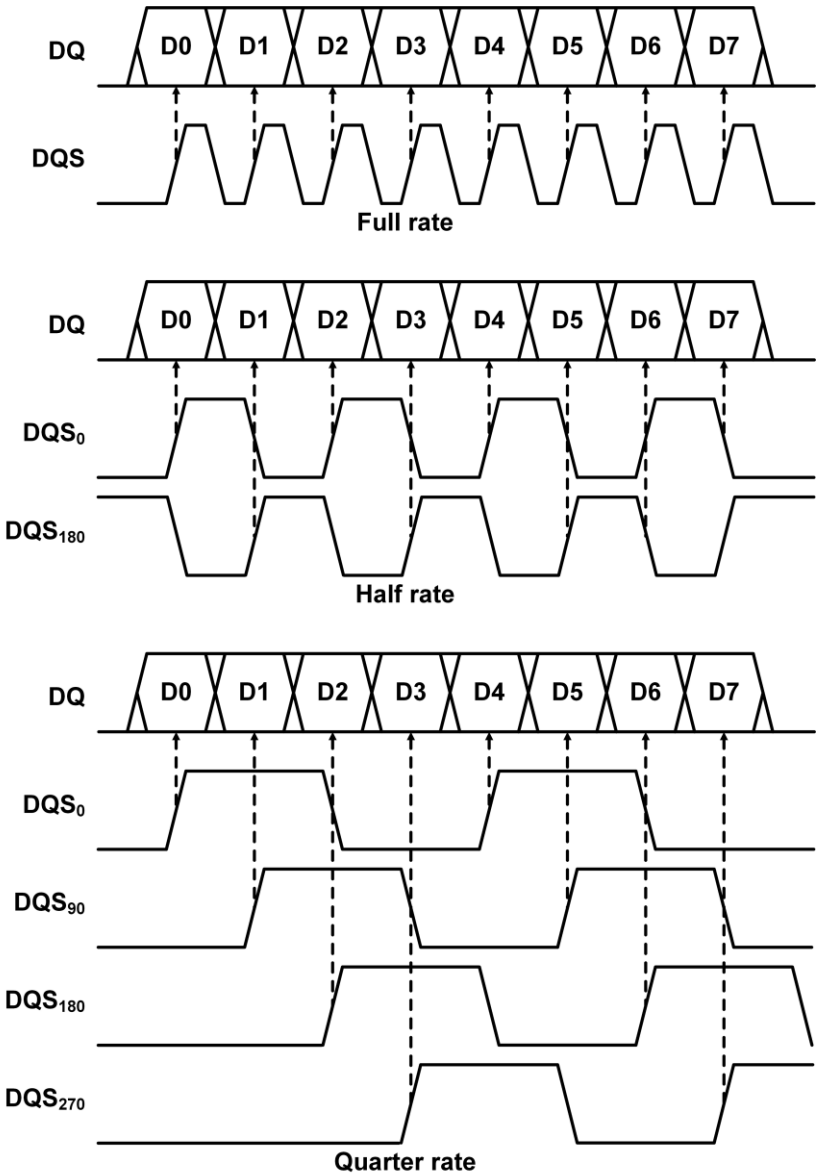


Figure 1.3.1. Relationship between DQ and clock signals in full-rate, half-rate, and quarter-rate architecture.

As described in Chapter 1.1, Increasing data-rate requires higher clock frequency.

However, increasing the clock frequency is limited by low-performance DRAM processes. To increase data-rate without increasing the clock frequency, present memory interfaces use multi-phase clocking. Figure 1.3.1 shows a comparison between full-rate, half-rate and quarter-rate architecture. Compared to other architecture, Although the quarter-rate architecture more phases than other architecture, the clock frequency of the quarter-rate architecture is lower than other architecture. This can relax timing margin and lower power consumption of the clock distribution for memory interfaces [1.3.1], [1.3.2], [1.3.3]. Therefore, the quarter-rate architecture has been used for memory interfaces in recent papers [1.1.1], [1.3.4].

1.3.1 DESIGN CONSIDERATION ON QUARTER-RATE ARCHITECTURE

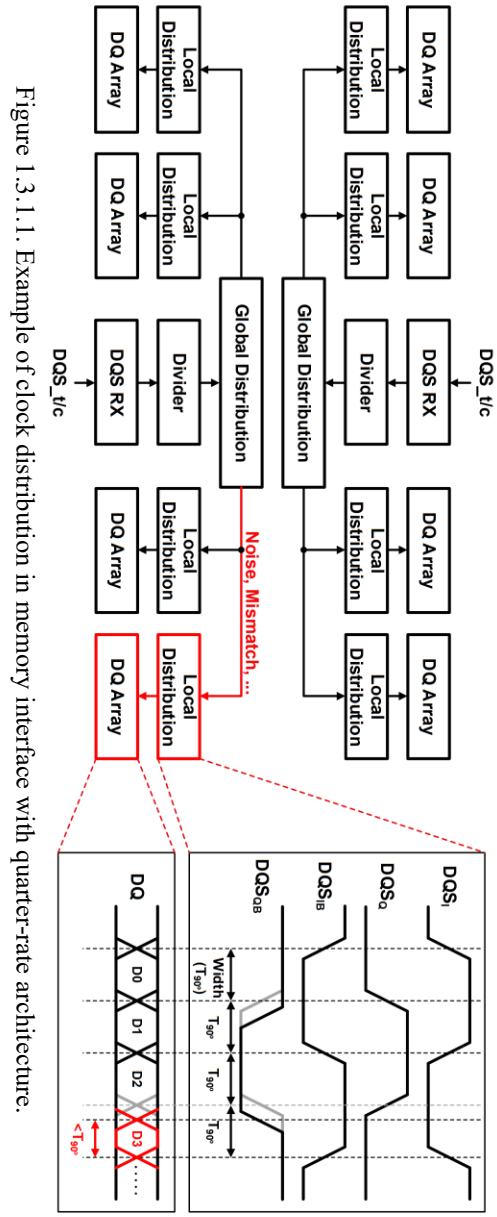


Figure 1.3.1.1. Example of clock distribution in memory interface with quarter-rate architecture.

Figure 1.3.1.1 shows an example of clock distribution in memory interfaces. The clock

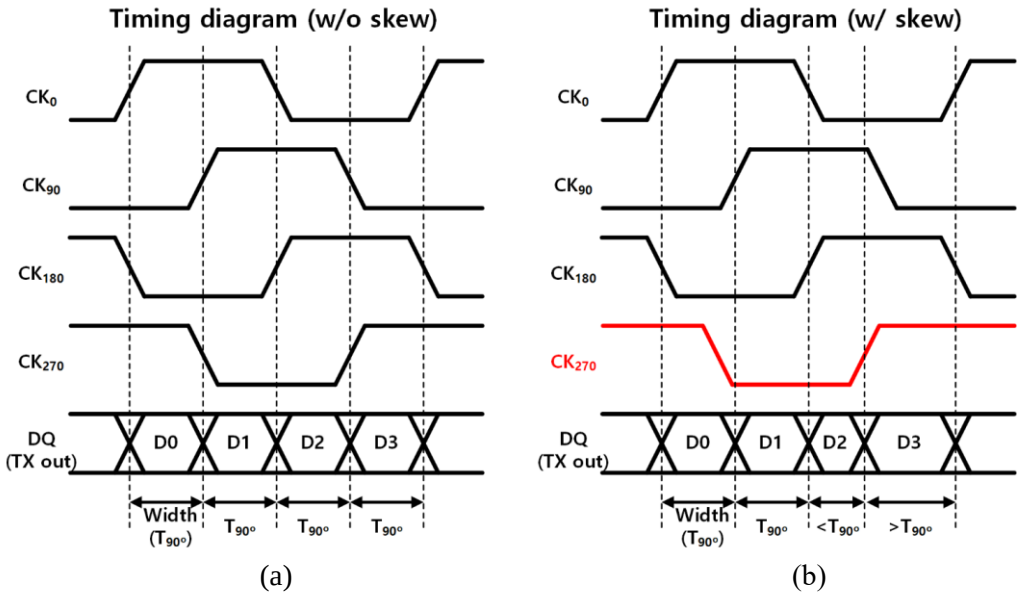


Figure 1.3.1.2. Relationship between clock and data (a) without and (b) with skew in transmitter.

distribution consists of a clock receiver (DQS RX), dividers, global distributions and local network. In the memory interfaces using quarter-rate architecture, quadrature clocks can be created by dividing high-speed clocks by two [1.1.1], [1.3.4]. The quadrature clocks are delivered through the global distributions and the local networks. DQ arrays use the clocks to generate or sample DQ.

However, skew between the quadrature clocks are inserted because of mismatches, noise and process, voltage, and temperature (PVT) variations in the clock path. The skew causes the degradation of performance of the transmitters and receiver in the memory interfaces.

Figure. 1.3.1.2 shows the relationship between the skew and the transmitter in the memory interfaces. The transition of DQ is made based on the edge of the clocks. In ideal

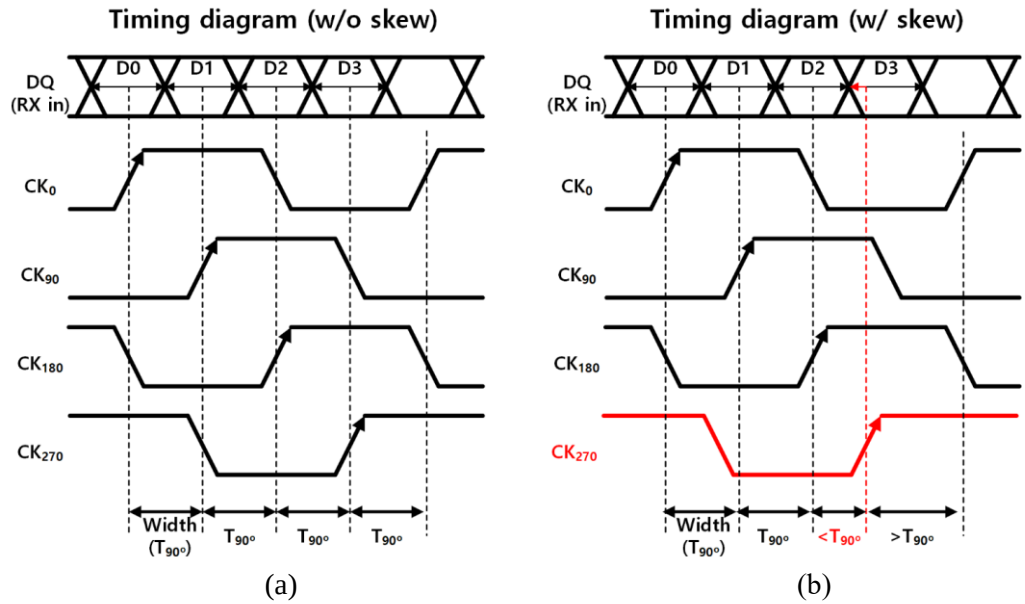


Figure 1.3.1.3. Relationship between clock and data (a) without and (b) with skew in receiver.

case, since the timing differences between the clocks are equal, the width of the output of the transmitter is uniform, as in Figure. 1.3.1.2 (a). In real case, as shown in figure. 1.3.1.2 (b), the skew makes the timing difference between the clocks unequal. Therefore, DQ generated by the transmitter is not uniform.

Figure 1.3.1.3 shows the relationship between skew and the receiver in the memory interfaces. DQ is sampled at the rising edge of the quadrature clocks. Due to the skew between the clocks, the timing of sampling DQ is not regular, which acts like an intrinsic jitter and reduces the effect eye width of DQ.

In summary, the skew between quadrature clocks degrades the performance of DQ array. To reduce the effect of the skew, quadrature signal corrector (QSC) is required for memory interfaces using quarter-rate architecture.

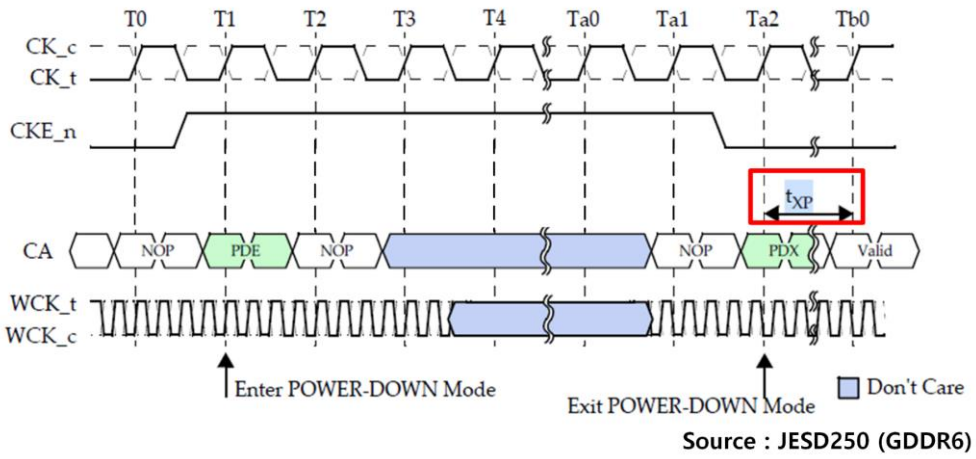


Figure 1.3.1.4. Timing diagram of power down entry and power down mode exit.

One more things to consider is the time needed to correct skew. Figure 1.3.1.4 shows the timing diagram of power down entry and exit in GDDR6 [1.3.1.1]. The memory interface enters power-down mode after power down entry (PDE), and the system remains in no operation (NOP). Valid commands can be applied t_{XP} cycles later after power down mode exit (PDX). t_{XP} is inevitably longer if the time for the skew correction is getting longer. The system must be in standby state until the correction is completed, which increase overall energy consumption of the system without any operations. In addition, the lengthened correction reduces the bandwidth of overall system.

The high-accuracy skew correction and the reduced correction time must be considered in designing the QSC for memory interfaces. However, there is a trade-off between the two factors [1.3.1.2], [1.3.1.3]. Higher resolution of skew correction allows the memory interfaces to generate and sample DQ with enhanced timing windows. However, it can increase the correction time, which degrades the bandwidth of overall

system. Therefore, the QSCs for memory interfaces must be designed to alleviate the trade-off between the accuracy and the correction time.

1.3.2 PRIOR WORKS

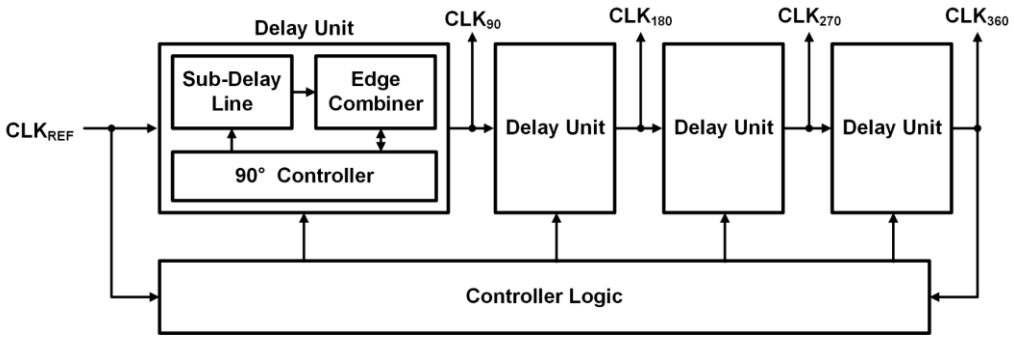


Figure 1.3.2.1. Block diagram of MDLLs.

One of the solution for skew correction is multi-phase delay locked loops (MDLLs) [1.3.2.1], [1.3.2.2]. Figure 1.3.2.1 show the block diagram of the MDLLs. The MDLLs consist of four cascaded delay units to generate the quadrature clocks between a reference clock (CLK_{REF}) and a delayed clock (CLK_{360}), and a controller logic to compare CLK_{REF} and CLK_{360} and adjust the codes of the delay units. The delay units generate clocks by using sub-delay line, edge combiner and 90° controller based on the controller logic. The MDLLs have an advantage of having relatively short correction time because the timing of the quadrature clocks are changed at the same time. However, the architecture has a low accuracy due to the mismatch between the delay lines since the delay units are controlled by the same signals of the controller logic.

Another solution is a QSC with a single loop shown in Figure 1.3.2.2. [1.3.2.3]. It can correct the skew by selecting two adjacent clocks and checking if the interval between the two clocks is equal to a specific timing (t_{quad}). Unlike the MDLLs, since the only one loop is used and the delay lines are controlled separately, the QSC reduce the effect of the

mismatch of delay lines. However, this architecture causes increase in the correction time because only one loop filter is used for the skew correction between four clocks. This makes

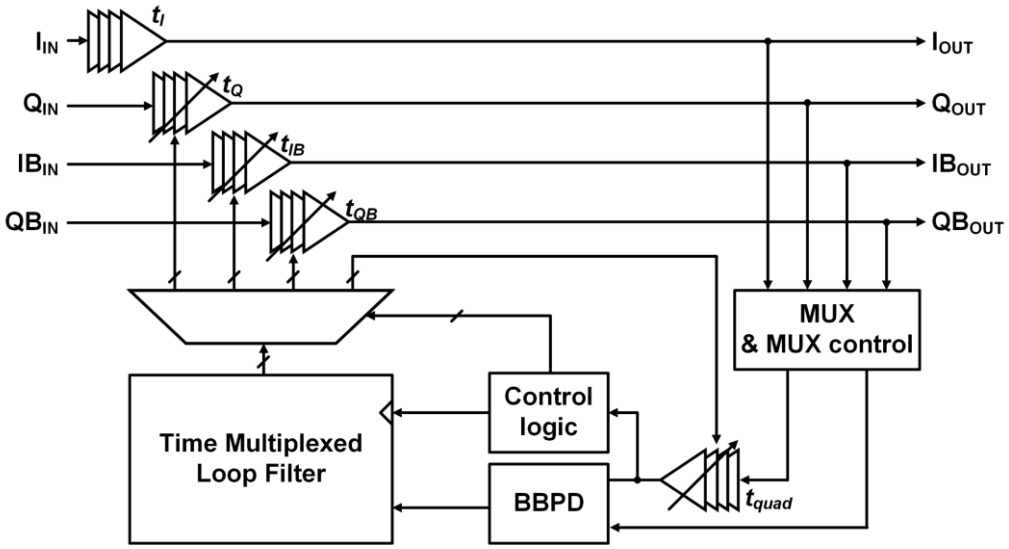


Figure 1.3.2.2. Block diagram of QSC with single loop.

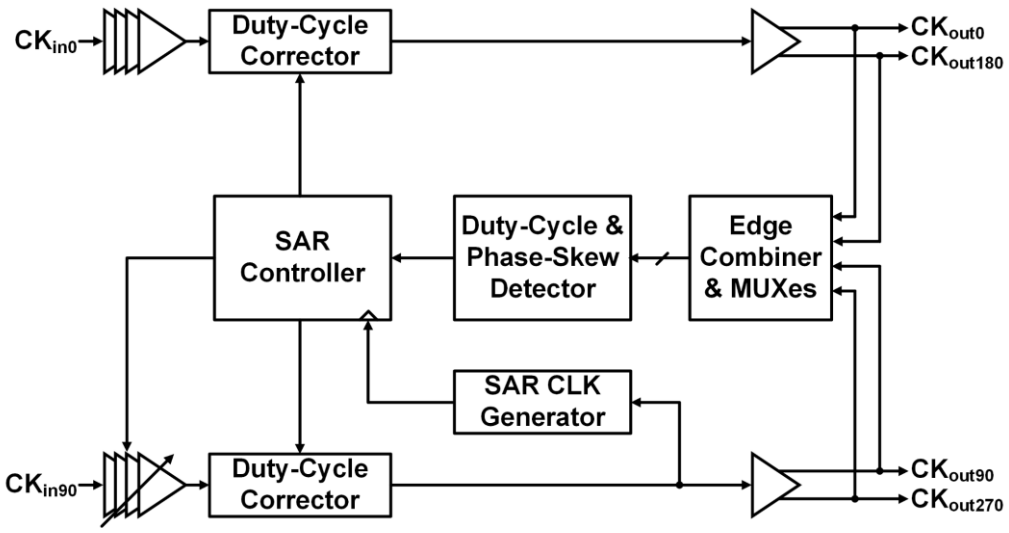


Figure 1.3.2.3. Block diagram of QSC with DCC and SAR.

the QSC change the timing of the quadrature clock sequentially, not simultaneously.

Figure 1.3.2.3. shows a QSC with a duty cycle corrector (DCC) and a successive approximation algorithm (SAR) [1.3.2.4]. The architecture can correct skew with reduced correction time by comparing the timing difference between only two clocks (CK_0, and CK_{90}) and using the SAR. CK_{180} and CK_{270} are generated by using single-to-differential amplifiers, the process for the duty correction must be performed before the skew correction. Additionally, since the QSC compares only CK_0 and CK_{90}, the skew induced into CK_{180} and CK_{270} due to mismatch of the single-to-differential amplifier cannot be corrected.

Previous works can correct skew in quarter-rate architecture. However, there are trade-off between the residual skew and the correction time. Therefore, we focus on reducing the trade-off of the skew correction.

1.4 SUMMARY

As mentioned in chapters above, two methods can be used to improve the bandwidth of DRAM by increasing data-rate per pin: first, PAM-4 signaling is used to double data-rate per pin without increasing the effect of the channel loss by using four signal levels. Second, a quarter-rate architecture can increase data-rate per pin without increasing the clock frequency which is limited in low-performance DRAM process. However, these two methods have issues. The PAM-4 DFE is used in PAM-4 receivers for equalization without amplifying noise but it has harsh timing constraint. Also, skew between the quadrature clock degrades the overall performance of the DRAM I/O and the skew must be corrected within short correction time. To alleviate the problems, we propose a single-ended PAM-4 receiver for memory interfaces, including a DFE with inverter-based summer [1.4.1]. By using inverter-based summers dedicated to each slicer, each eye can be amplified without affecting other eyes. The proposed receiver is verified by measurement of prototype chips.

Also, as mentioned in chapter 1.3, the quarter-rate architecture also can be used to improve the bandwidth DRAM without increasing clock frequency. The quarter-rate architecture has other advantages of relaxing the timing margin of the systems and lowering power consumption in clock distribution of memory interfaces. However, skew between the quadrature clocks degrades signal integrity in memory interfaces. Therefore, skew corrections must be performed. Additionally, the correction of the skew correction must be reduced since the interfaces must be in standby state until the skew correction ends. However, there is a trade-off between the residual skew and the correction time. To alleviate the trade-off, a QSC including an adaptive delay gain controller is also proposed in this

thesis. By changing the delay gains of the quadrature clocks separately, the correction time can be reduced without degrading the accuracy of the skew correction. The proposed QSC is also verified by measurement of prototype chips.

1.5 THESIS ORGANIZATION

This thesis is composed of six chapters. Chapter 1 is an introduction that explains recent trends on memory interfaces, PAM-4 signaling which is received attentions for next-generation memory interfaces and quarter-rate architecture which is used in recent memory interfaces. Chapter 2 describes the concept and the design consideration of the DFE with inverter-based summer proposed in this thesis. To explain the QSC with the adaptive delay gain controller proposed in this thesis, Overall operation on the QSC and the adaptive delay gain controller will be described in chapter 3. In chapter 4, the implementation of the proposed DFE with inverter-based summer and the QSC with the adaptive delay gain controller will be explained. Chapter 5 shows experimental setup and results of the proposed receiver with a prototype chip. The conclusion will be drawn in chapter 6.

CHAPTER 2

CONCEPTS OF DFE WITH INVERTER-BASED SUMMER

As discussed in Chapter 1.2.1, the input eye height of the slicer in PAM-4 DFE must be bigger than the sensitivity of the slicer to satisfy the timing constraint on the DFE. However, the eye height is limited by the linearity of the summer in the previous PAM-4 DFE. This limits the performance of the PAM-4 DFE even if the high-performance slicers are used. To alleviate the problem, we have proposed a DFE with inverter-based summer. By using three inverter-based summers dedicated to the three slicers, the height of each eye can be increased without considering the linearity. To increase the eye height, we utilize the gain of the inverter, which varies with the level of input signal.

2.1 CONCEPTUAL ARCHITECTURE OF DFE WITH INVERTER-BASED SUMMER

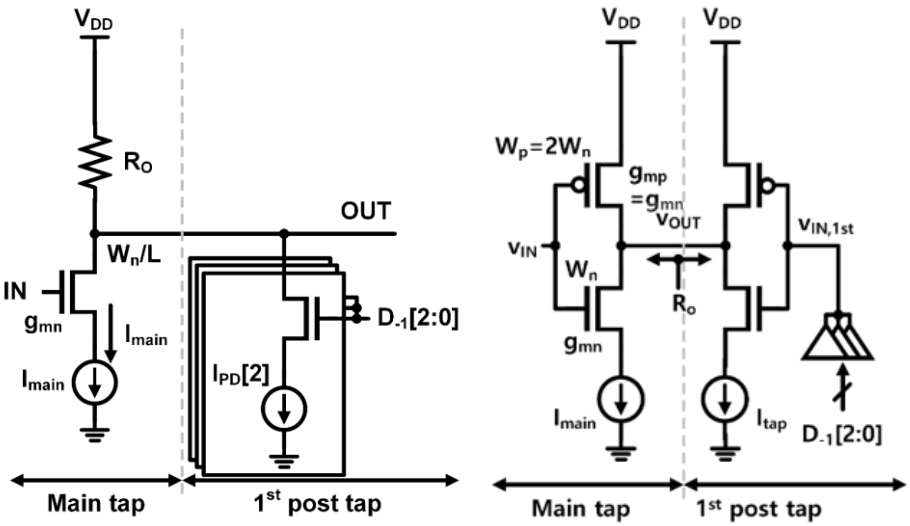


Figure 2.1.1. Simplified half circuit diagram of (a) CML summer and (b) inverter-based summer.

Table 2.1.1. Characteristics of main tap of CML summer and inverter-based summer with equal power consumption

		CML summer	Inverter-based summer
Current		I_{main}	
Equal transconductance of NMOS	Width (NMOS/PMOS)	W_n/-	$W_n/W_p(=2W_n)$
	Gain	$g_{mn}\cdot R_o$	$2g_{mn}\cdot R_o$
Equal gain	Width	$4\cdot W_n$/-	$W_n/2W_n$
	Output capacitance	$4C_d$	$3C_d$
	Input capacitance	$4C_g$	$3C_g$

* C_d : Drain capacitance of NMOS.
* C_g : Gate capacitance of NMOS.
* R_o : Output impedance of summers.

Figure 2.1.1(a) is a half circuit of a CML summer, which is frequently used in previous PAM-4 DFEs. The CML summer is composed of two parts: the amplifier with resistive load for the main tap, and the first post tap with pull-down current sources (I_{tap}[2:0]) and switches. The current sources are chosen by previous data. Figure 2.1.1(b) shows a simplified schematic of an inverter-based summer. The inverter-based summer consists of two inverter-based amplifiers: one for the main tap with the current source I_{main}, and the other one for the post tap with the current source I_{tap}. In the thesis, we designed the inverter-based summer with the width of the PMOS (W_p) in the inverter-based summer around two times larger than that of NMOS (W_n) to make the threshold voltage of the amplifier around $V_{DD}/2$.

Table 2.1.1 shows the characteristics of the main taps of the CML summer and the inverter-based summer [1.4.1]. Comparing the two summers, the inverter-based summer

		CML summer	Inverter-based summer
Current		I_{main}	
Equal transconductance	Width (NMOS/PMOS)	W_n/-	$W_n/W_p(=2W_n)$

has two-times larger transconductance, because the two MOSFET (NMOS and PMOS) share the drain current. In the case that the summers has the equal output resistance, the inverter-based summer has two-times bigger gain. In the two summers, the current and transconductance of the NMOSs are expressed as, respectively:

$$I_{main} = \frac{k}{2} \cdot \frac{W_n}{L} \cdot V_{OV}^2, \tag{2.1.1}$$

$$g_{mn} = k \cdot \frac{W_n}{L} \cdot V_{OV}, \tag{2.1.2}$$

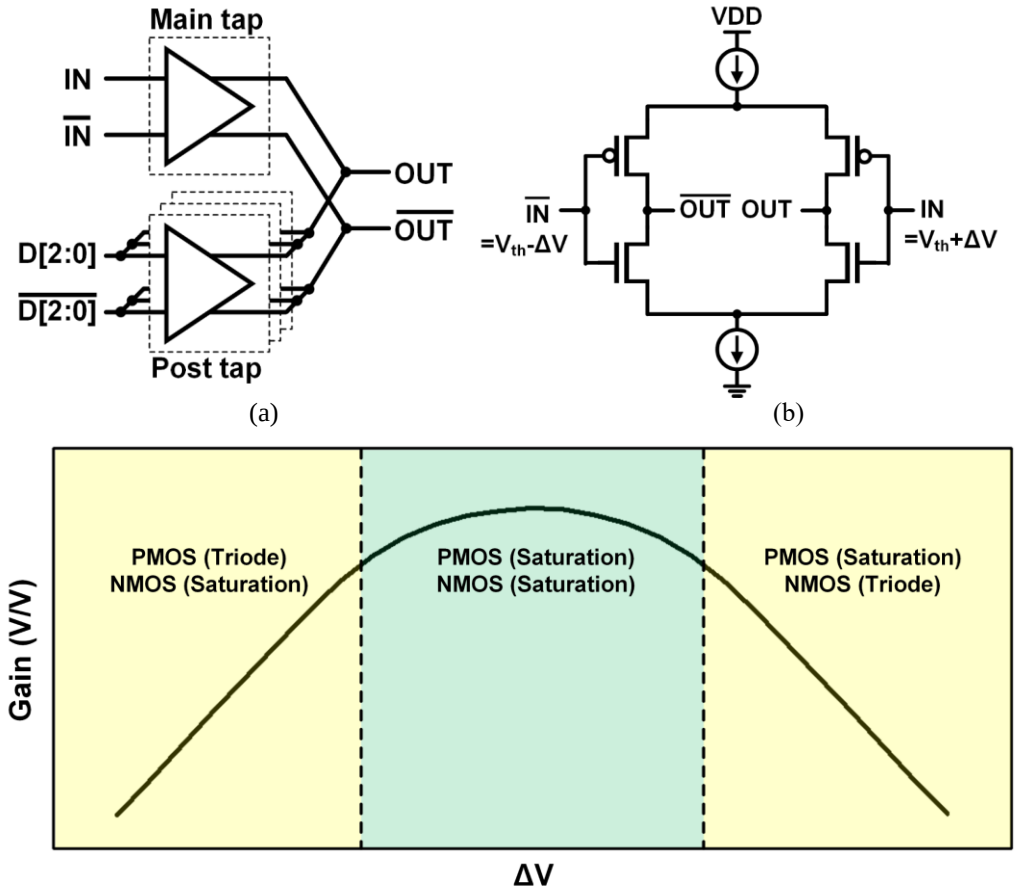


Figure 2.1.2. (a) Structure of summer, (b) inverter-based amplifier and (c) relationship between input level from threshold voltage and gain.

where k is the parameter determined by the process, V_{OV} is the overdrive voltage of the NMOS, and L is the length of the NMOS. In (2.1.1), assuming that other parameters than W_n and V_{OV} are constant, the product of V_{OV}^2 and W_n is constant. Therefore, to make the transconductance two-times bigger with I_{main} constant, the NMOS with four times larger width must be used, based on (2.1.2). Because of the four times larger W_n, the CML summer

has bigger output capacitance than the inverter-based summer. Additionally, the inverter-based summer has less input capacitance smaller than the CML summer [1.4.1].

In the CML summer, the first post tap is composed of the current sources (I_{PD}[2:0]) which is connected to the output of the summer. Based on the previous data, the current sources can vary the output common level of the CML summer. To keep the output common level constant, a common-level restoration is used in previous summer [1.2.1.1] also connected to the output, like I_{PD}[2:0]. The additional circuit makes the structure of the CML summer more complexed and increases output capacitance. However, the inverter-based summer in figure 2.1.1(b) has the main tap and the post tap that are separated, which makes the output common level of the summer not affected by the previous data.

Fig. 2.1.2(a) shows the simplified structure of the summer. The summer consists of an inverter-based amplifier for the main tap and first post tap. Fig. 2.1.2(b) shows a block diagram of inverter-based amplifier for the main tap (IN) of the summer. Inverter-based amplifiers have the advantage of wider bandwidth in a given process [2.1.1], [2.1.2]. The gain of the inverter-based amplifier can be expressed as follows:

$$A_v = g_m \cdot (r_{on} || r_{op}) \tag{2.1.1}$$

where g_m is the transconductance of the amplifier, r_{on} and r_{op} are the output resistances of the NMOS and PMOS. When the input signal is equal to the threshold voltage of the inverter (V_{th}), which is usually $V_{DD}/2$, the output of the inverter-based amplifier is also $V_{DD}/2$. At this point, all of the MOSFETs are in saturation region and the gain of the

amplifier is maximum since both NMOS and PMOS are in saturation region. As the input signal is far from the threshold, the total output resistance is decreased since r_{on} or r_{op} is reduced. As the input signal is further from the threshold, the gain of the inverter-based amplifier is decrease rapidly since the NMOS or PMOS is in triode region.

Based on the characteristics, the gain of the inverter-based can be expressed conceptually as shown in Fig. 2.1.3(c). The gain of the inverter-based amplifier reaches the maximum value when the input signal is equal to the threshold ($\Delta V = 0$).

2.2 DESIGN CONSIDERATION OF INVERTER-BASED SUMMER

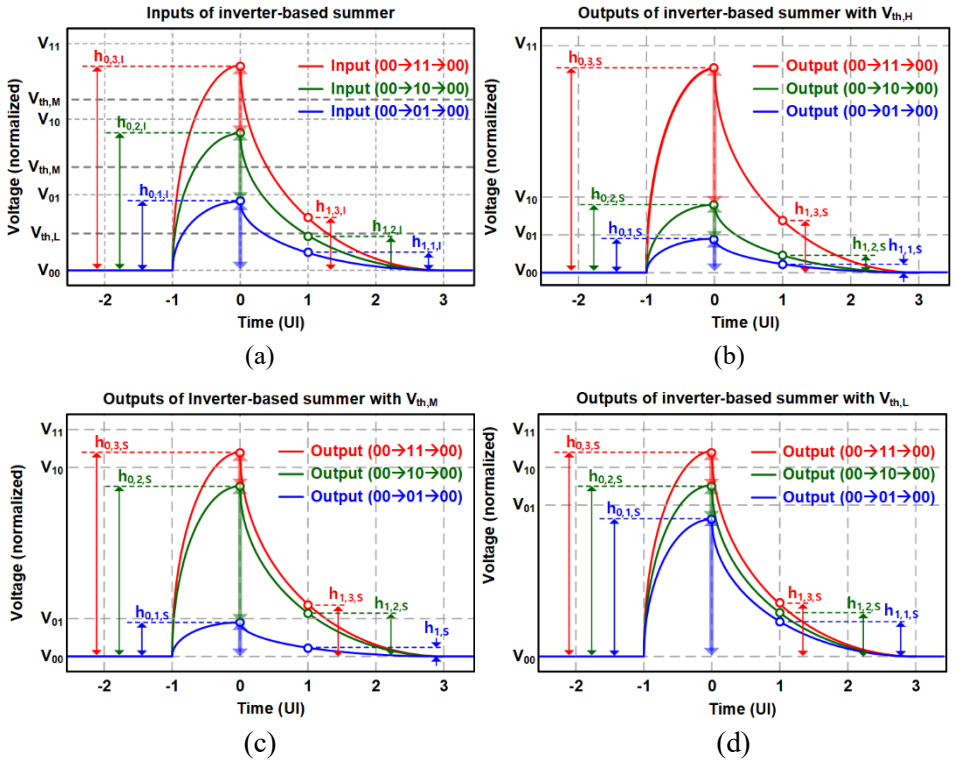


Figure 2.2.1. (a) Three data transitions for inputs, (b) output pulses of inverter-based summer dedicated to $V_{th,H}$, (c) output pulses of inverter-based summer dedicated to $V_{th,M}$ and (d) output pulses of inverter-based summer dedicated to $V_{th,L}$.

Figure 2.2.1(a) shows three data transition for input of the summer, where $h_{0,3,I}$, $h_{0,2,I}$, and $h_{0,1,I}$ are the main taps of the pulses. $V_{th,H}$, $V_{th,M}$, and $V_{th,L}$ are the three threshold voltages for distinguishing PAM-4 signal. Ideally, the differences between the main taps are equal. The spaces between the first post-cursor ISIs of the three pulses ($h_{1,3,I}$, $h_{1,2,I}$, and $h_{1,1,I}$) are also equal.

Based on the characteristic of the inverter-based amplifier shown in figure 2.1.2 (b),

figure 2.2.1(b) shows the output of the inverter-based summers dedicated to $V_{th,H}$. In figure 2.1.1(b), (c), and (d), $h_{0,3,s}$, $h_{0,2,s}$, and $h_{0,1,s}$ are the main cursors of the three output pulses. As shown in figure 2.2.1(b), the spacing between $h_{0,3,S}$ and $h_{0,2,S}$ is larger than the other spacing since $h_{0,3,I}$ and $h_{0,2,I}$ are closer to $V_{th,H}$ than other signal levels. Figure 2.2.1(c) shows the output pulses of the summer associated with $V_{th,M}$. Similar to the case of figure 2.2.1(b), the spacing between $h_{0,2,S}$ and $h_{0,1,S}$ is bigger than other spacing between the main taps. Figure 2.2.1(d) shows the output pulses of the summer associated with $V_{th,L}$. These figures show how the inverter-based summers selectively amplify the appropriate eye of PAM-4 signal to improve the clock-to-Q delay of the slicers.

Unlike figure 2.2.1(a), the first post-cursor ISIs of the output pulses ($h_{1,3,S}$, $h_{1,2,S}$ and $h_{1,1,S}$) in Figure 2.2.1(b), (c), and (d) have non-linear differences since the gain of the inverter-based summer changes depending on the input signal level. Therefore, to apply the inverter-based summer to the summer for the PAM-4 DFE, different first tap coefficients must be used based on the previous data.

Based on figure 2.2.1, each eye corresponding to the threshold voltages can be amplified. However, the height of other eyes can be decreased because of the characteristic of the gain of the inverter-based summer. To solve the problem, we use separate signal paths dedicated to each eye. Figure 2.2.2(a) shows a simplified block diagram of the DFE with the inverter-based summers and three outputs of the summers. By having summers corresponding to each slicer, the DFE can amplify the specific independent of the other eye

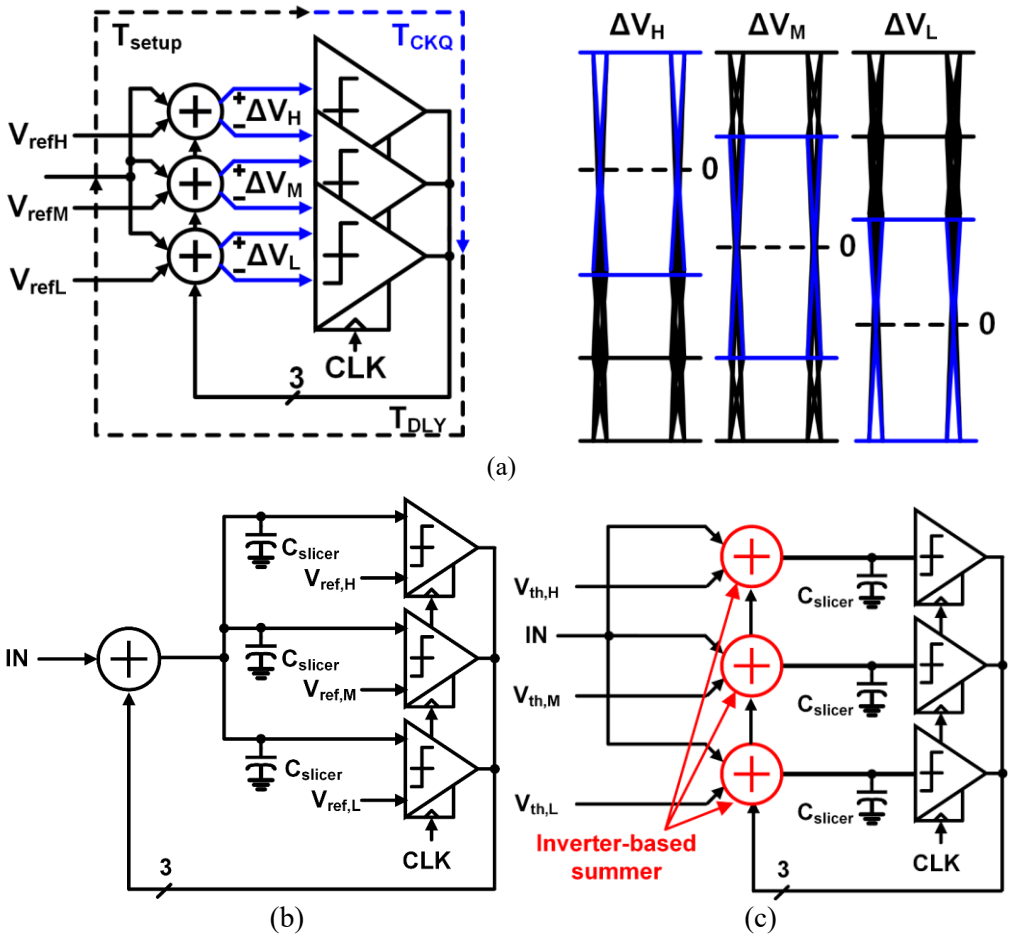


Figure 2.2.2. (a) Simplified block diagram of proposed DFE with inverter-based summer and outputs of three summers, (b) simplified block diagram of previous PAM-4 DFE with parasitic capacitance (c) PAM-4 DFE with inverter-based summers with parasitic capacitance.

heights. Figure 2.2.2 (b) and (c) show the previous PAM-4 DFE and the PAM-4 DFE with inverter-based summer with parasitic capacitance (C_{slicer}) connected to each summer. In Figure 2.2.2(c), each summer is connected to a slicer, which reduces the output capacitance of each summer. This allows the summers to maintain the bandwidth without increasing power consumption due to increasing number of the summers. In addition, the capacitance

that each summer drives is reduced, because the summer can be designed with reduced size.

CHAPTER 3

CONCEPTS OF QUADRATURE SIGNAL CORRECTOR USING ADAPTIVE DELAY GAIN CONTROLLER

To alleviate the issues about skew in the quarter-rate architectures discussed in chapter 1.3.1, a quadrature signal corrector with an adaptive delay gain controller has presented in this thesis. The QSC checks the polarity of the skew between the quadrature clocks and calculate the delays of each clock to reduce skew with optimal delay gain. By adjusting the delay gains for each clock, the QSC can correct skew quickly without scarifying the correction time.

3.1 OPERATION OF PROPOSED QUADRATURE SIGNAL CORRECTOR

Figure 3.1.1 shows the simplified block diagram of the proposed QSC. The QSC

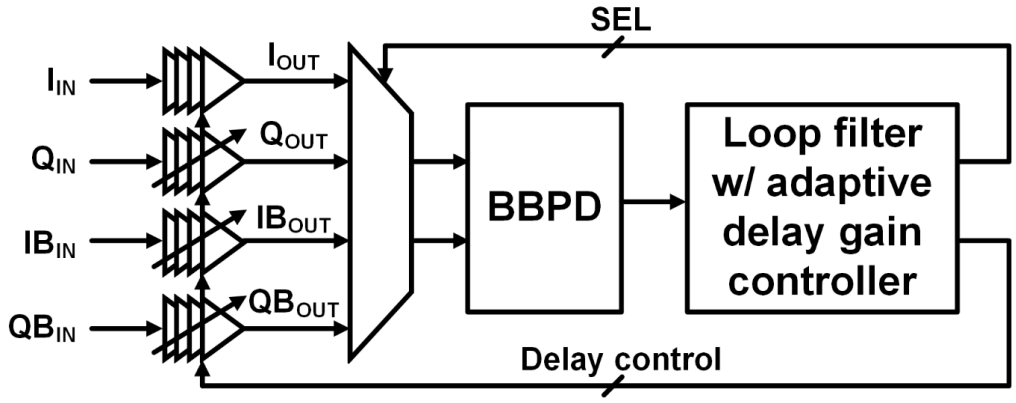
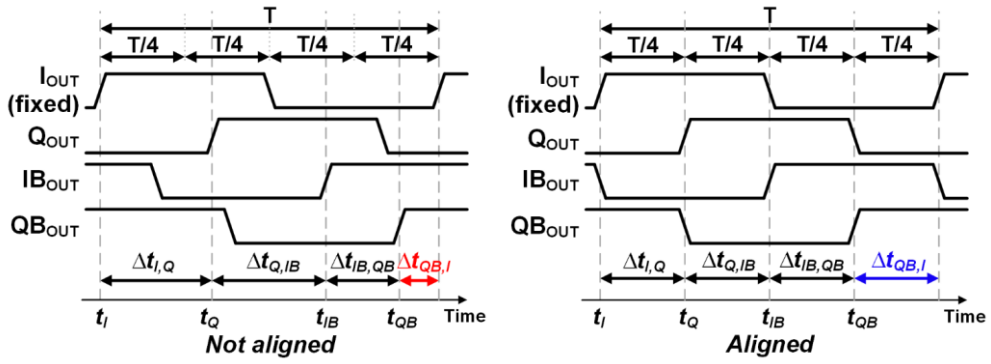


Figure 2.2.1. Simplified block diagram of proposed QSC.

consists of four DCDLs to adjust the delays of the four clocks, a MUX to choose two of the quadrature clocks for comparison based on an output of a loop filter, a bang-bang phase detector (BBPD) to compare the timing difference, and the loop filter with an adaptive delay gain controller.

Figure 3.1.2 show timing diagrams of the clocks whether there is skew or not. $\Delta t_{I,Q}$, $\Delta t_{Q,IB}$, $\Delta t_{IB,QB}$ and $\Delta t_{QB,I}$ are the timing difference between I_{OUT} and Q_{OUT}, Q_{OUT} and IB_{OUT}, IB_{OUT} and QB_{OUT}, and QB_{OUT} and I_{OUT}, respectively. As shown in figure 3.1.2(a), if there is skew between the quadrature clock, at least one of the timing differences is not equal to $\Delta t_{QB,I}$. Figure 3.1.2(b) shows the case that there the quadrature clocks are aligned without skew. In this case, all of the timing differences are equal to $\Delta t_{QB,I}$. As shown in figure 3.1.1, by comparing $\Delta t_{QB,I}$ to the other timing differences, the QSC can check if there is skew



(a) (b)

Figure 3.1.2. Example timing diagram of quadrature clocks when (a) skew exists between quadrature clocks and (b) skew does not exist.

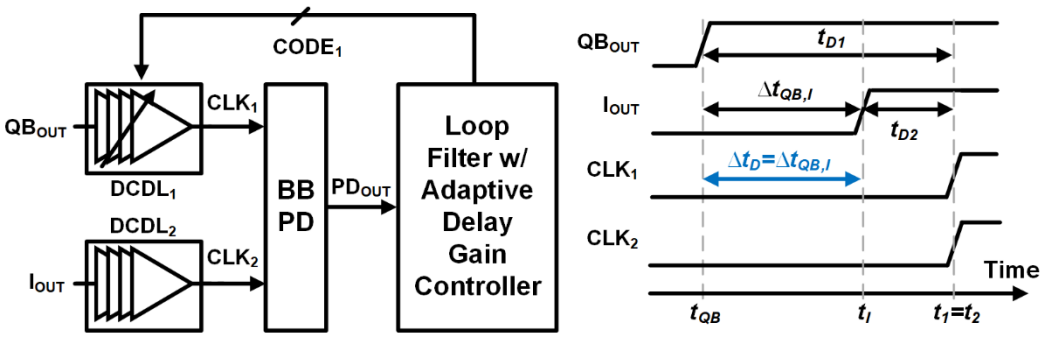


Figure 3.1.3. Method to acquire Δt_D from $\Delta t_{QB,I}$.

between the quadrature clocks.

To compare $\Delta t_{QB,I}$ to the other timing differences, the QSC need to acquire the information about $\Delta t_{QB,I}$. Figure 3.1.3 shows how the QSC compare the timing differences. t_{D1} and t_{D2} are the delays of $DCDL_1$ and $DCDL_2$, If the timing of CLK_1 and CLK_2 (i.e t_1 and t_2 in figure 3.1.3) are equal, the difference between t_{D1} and t_{D2} (i.e., Δt_D) is equal to $\Delta t_{QB,I}$. The BBPD checks if CLK_1 and CLK_2 have the same timing. Based on the output of the BBPD, the loop filter adjusts the code of $DCDL_1$ ($CODE_1$) with a unit of the product

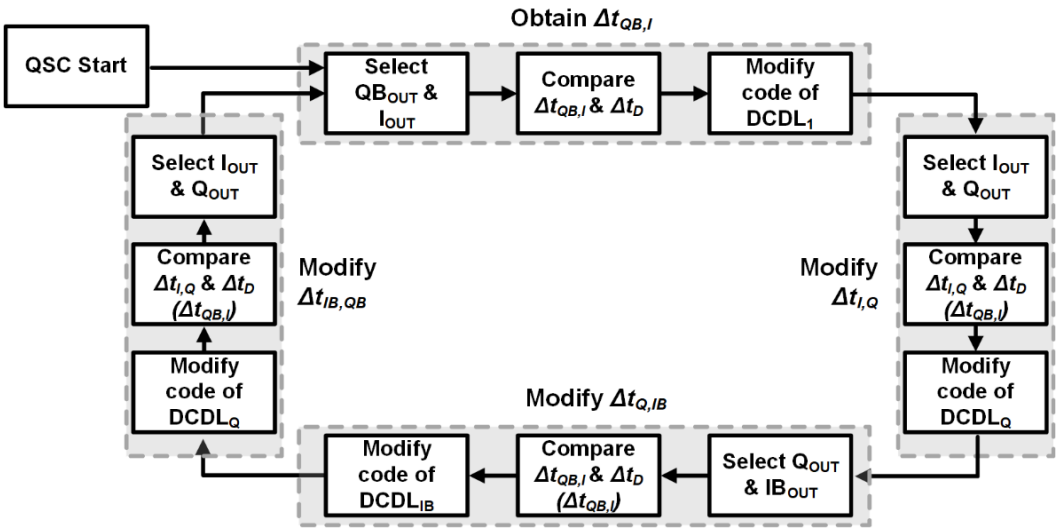


Figure 3.1.4. Procedure of skew correction.

of delay gain and the resolution of $DCDL_1$ to make Δt_D close to $\Delta t_{QB,I}$.

Figure 3.1.4 shows the processes of the operation of the QSC. When the QSC starts the skew correction, the loop filter chooses QB_{OUT} and I_{OUT} to modify Δt_D. The loop controller controls $\Delta t_{QB,I}$ to get closer to $\Delta t_{QB,I}$, as mentioned above. Next, the loop controller and the MUX select I_{OUT} and Q_{OUT} to compare $\Delta t_{QB,I}$ and Δt_D. Based on the result of the comparison, the loop controller updates the delay of the DCDL corresponding to Q_{OUT}. Afterward, the same operations are performed for the delays of DCDLs dedicated to IB_{OUT} and QB_{OUT}. Since the timing of QBOUT is changed, the current $\Delta t_{QB,I}$ is different from previous $\Delta t_{QB,I}$. Therefore, the QSC needs to update Δt_D. The QSC repeats the procedures by adjusting Δt_D. As the processes are repeated, because Δt_D follows $\Delta t_{QB,I}$, the timing differences between the clocks are getting closer to $\Delta t_{QB,I}$ gradually.

3.2 LOOP FILTER INCLUDING ADAPTIVE DELAY GAIN CONTROLLER

As described in chapter 3.1, the proposed QSC has single loop filter. The single loop filter has an advantage of reducing the effect of mismatch [1.3.2.3]. By reducing the mismatch, the QSC can correct skew more accurately than other previous QSCs. However, since all of the quadrature clocks shares the single loop filter and cannot adjust the timing of the quadrature clocks at the same time, the correction time of the QSC with the single loop filter is inevitably extended, which makes the overall system stay in standby state without any valid operation. To reduce the correction time without scarifying the accuracy of the QSC, we proposed an adaptive delay gain controller for the QSC with single loop filter.

Figure 3.2.1 shows the operation of the loop filter with an example of modifying $t_{I,Q}$. After the QSC obtains Δt_D, the MUX and the loop filter in figure 3.1.1 select I_{OUT} and Q_{OUT} to compare the timing difference of the two clocks. In the case of first iteration, the delay gains for the DCDL corresponding to Q_{OUT} (G_Q) is set to the initial delay gain. The output of the phase detector ($PD_{OUT,I,Q}$) is compared with previous output of BBPD ($PD_{PREV,I,Q}$) kept in the loop controller. If the previous and current outputs of the phase detector are different, this means that the magnitude relationship between $\Delta t_{I,Q}$ and Δt_D is reversed, and the difference is less than the product of the resolution of the DCDL and G_Q.On the other hands, the magnitude relationship is retained.

Figure 3.2.2 shows a conceptual change of difference of $\Delta t_{I,Q}$ and Δt_D.As the QSC

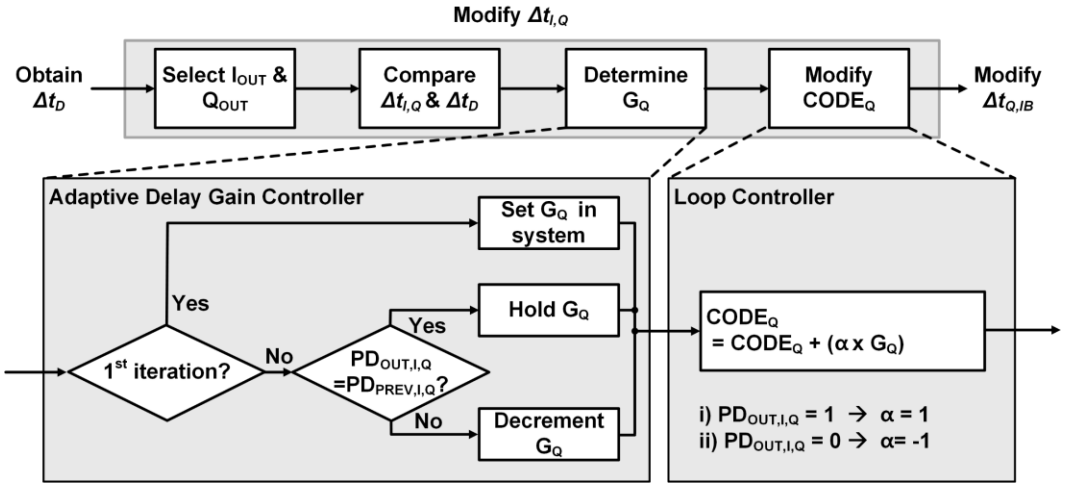


Figure 3.2.1. Example operation of loop filter.

continues to the operation, the difference is reduced with a unit of G_Q, until $\Delta t_{I,Q}$ get smaller than Δt_D.G_Q is changed if Δt_D is smaller than Δt_D, The same operation is repeated until the GQ becomes a minimum value. The process of determining G_Q can be expressed as:

$$\left|\Delta t_{I,Q} - \Delta t_D\right| - G_Q \cdot t_{res} \begin{cases} \leq 0 \rightarrow \text{Decrease } G_Q \\ \geq 0 \rightarrow \text{Hold } G_Q \end{cases} \tag{3.2.1}$$

where t_{res} is the resolution of the DCDLs. The sum of the skew between the quadrature clock is equal to zero but each skew is not equal. Therefore, the same process for the DCDLs corresponding to other quadrature clocks and Δt_D must be performed separately in the loop filter to reduce each skew with shorter correction time.

In prior work that applied SAR algorithms to reduce correction time [1.3.2.4], [3.2.1], the bits of the delay lines is not changed once it is decided. In the procedure of deciding

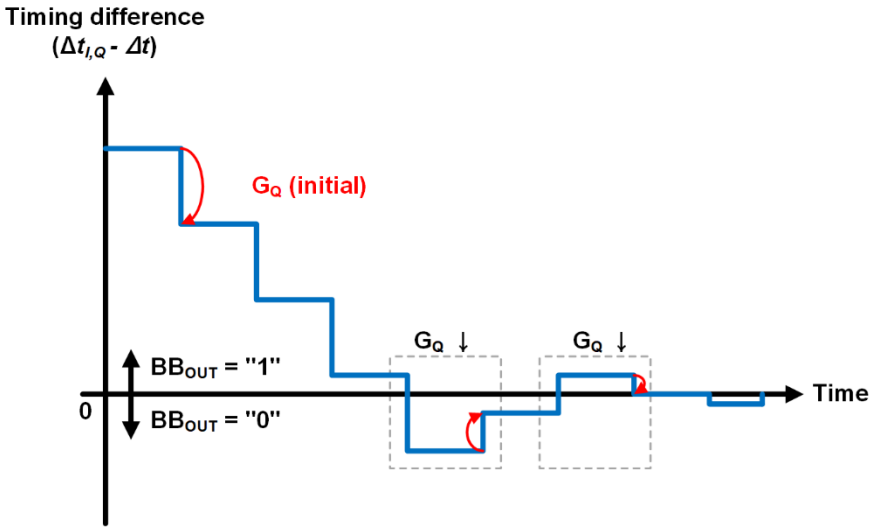


Figure 3.2.2. Conceptual change of G_Q.

each bit, if errors are caused by some factors such as noise, it is not able to be corrected during the operation. But the method of the adaptive delay gain controller can correct errors during the operation even if an error occurs in the process while reducing the correction time.

CHAPTER 4

ARCHITECTURE AND IMPLEMENTATION

In Chapter 4, we explain the overall architecture and the implementation of the proposed PAM-4 receiver including the QSC. The PAM-4 receiver is implemented with single-ended input so that the receiver can be applied to memory interfaces, which have the limited number of pin count.

4.1 OVERALL ARCHITECTURE

Figure 4.1.1 shows the block diagram of the proposed PAM-4 receiver including clock

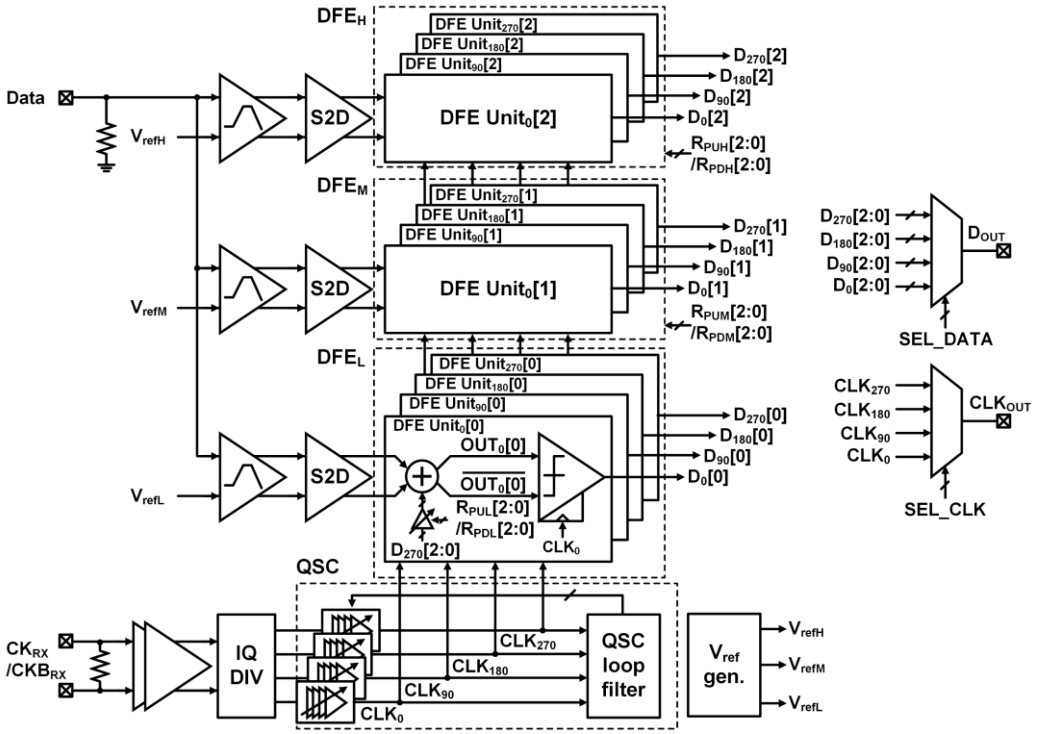


Figure 3.2.1. Overall architecture of proposed PAM-4 receiver.

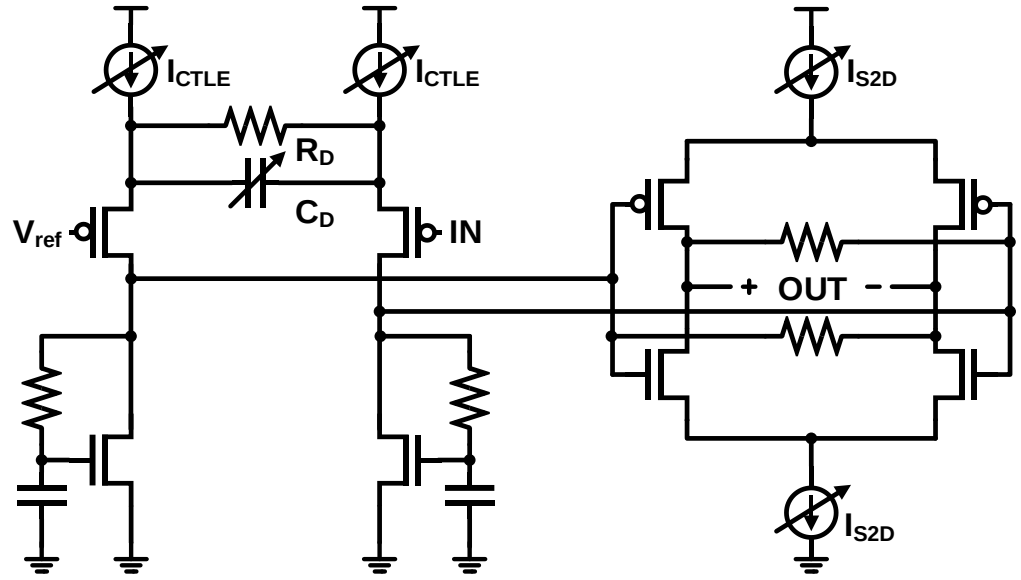
path with the QSC. The receiver is composed of continuous-time linear equalizers (CTLEs) and single-to-differential amplifiers (S2Ds) for each eye, and a DFE with inverter-based summers. The CTLEs and S2Ds are used to adjust the input common level of the summers in the DFE with inverter-based summer to threshold voltage. Also, the pairs of the CTLE and S2D can compensate for pre-cursor ISI. The 1-tap DFE with inverter-based summers is divided into three parts (DFE_H, DFE_M, and DFE_L) and each part includes inverter-based summers to amplify the corresponding eyes. The receiver uses the quadrature clocks to

secure an appropriate timing margin for the circuits in the DFE. The reference voltage generators (V_{ref} gen.) with resistor ladders are used to generate the reference voltages (V_{refH}, V_{refM}, and V_{refL}) for distinguishing data. The tap coefficients of DFE (R_{PUH}[2:0]/R_{PDH}[2:0], R_{PUH}[2:0]/R_{PDH}[2:0], and R_{PUH}[2:0]/R_{PDH}[2:0]) can be controlled separately to apply other coefficient depending on each eye based on previous data. In the PAM-4 DFE, any thermometer-to-binary converter is not used to reduce the propagation delay from the slicers to the summers, which makes the PAM-4 DFE satisfy the timing constraint with improved timing margin. Also, measuring the signal integrity of each eye can be easier by not using the thermometer-to-binary converters.

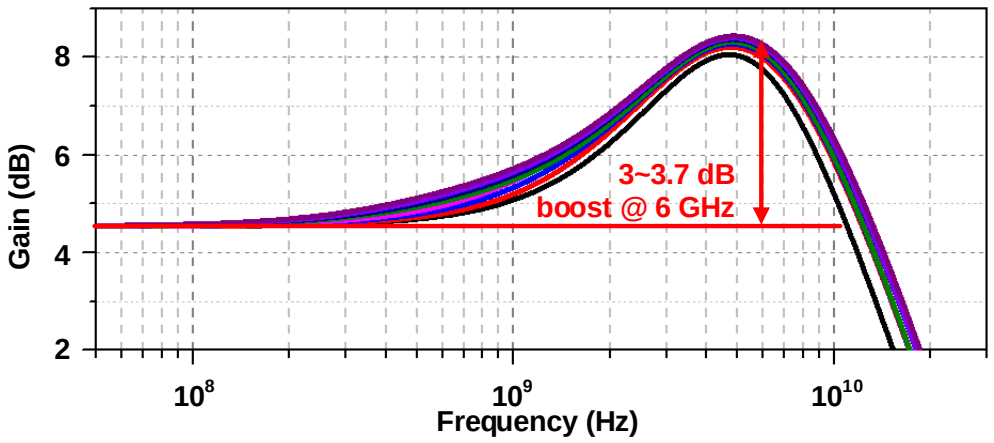
Like the clock distributions for memory interfaces [1.1.1], the quadrature clocks (CLK_0, CLK_{90}, CLK_{180}, and CLK_{270}) are made by dividing differential clocks (CK_{RX} and CKB_{RX}) by two using IQ divider (IQ DIV). The clocks pass through four delay lines in the QSC, with the skew corrected. The delays of the DCDLs are controlled by the loop filter including the adaptive delay gain controller. The quadrature clocks adjusted by the QSC is applied to the PAM-4 receiver.

To measure bit-error rates (BERs) for each eye, a MUX selects and outputs data based on an external selection signal (SEL_DATA). Thermometer codes were used for the outputs of the DFE to measure the BER for each eye intuitively. The other MUX is used to select and output clocks based on an external selection signal (SEL_CLK) for measuring skew between the four clocks without and with the operation of the QSC. The selection signals are controlled externally.

4.2 ANALOG FRONT END



(a)



(b)

Figure 4.1.1. (a) Circuit diagram of CTLE and S2D, and (b) simulated frequency response.

Figure 4.2.1(a) shows the architecture of the CTLEs and S2Ds. The pairs of CTLE and S2D are used to compensate for pre-cursor ISI and modify input common level of the

summers in the DFE. C_D in the source degeneration of the CTLE is controllable to adjust the frequency boost depending on C_D. C_D can be controlled externally. The current sources (I_{CTLE} and I_{S2D}) can be controlled to adjust the common level of the input for the DFE so that common level can be matched to the threshold voltage of the inverter-based summers. Figure 4.2.1(b) shows the frequency responses of CTLE and S2D. At the 6 GHz, the frequency boost is from 3 dB to 3.7 dB depending on the value of C_D.

4.3 DECISION FEEDBACK EQUALIZER WITH INVERTER-BASED SUMMER

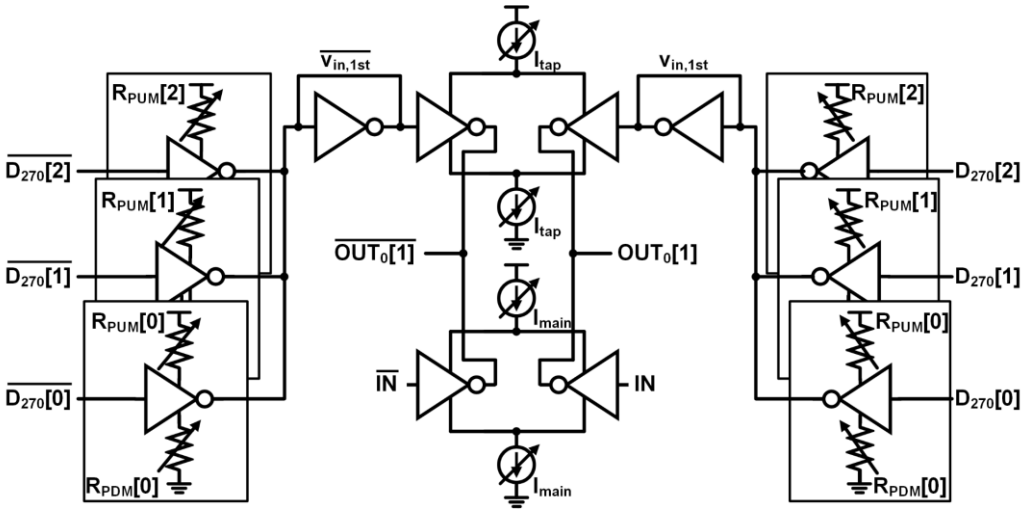


Figure 4.2.1. Block diagram of inverter-based summer.

Figure 4.3.1 is the circuit diagram of the inverter-based summer for the DFE unit$_0$[1]. The summer consists of an inverter-based amplifier for the main tap (IN) and the other part for the post first taps (D_{270}[2:0]). The inverter based amplifier corresponding to the main tap amplifies a specific eye of main tap, as explained in Chapter 2.1. The current source I_{main} and I_{tap} can be modified to compensate for the distribution of the input common levels from the CTLEs and S2Ds and the variations of the threshold of the inverter-based amplifier for the main tap. The part for post first taps consists of six inverter connected to pull-up and pull-down resistors (R_{PUM}[2:0]/R_{PDM}[2:0]), diode-connected inverters and an inverter-based amplifier associated with $v_{in,1st}$. The diode- connected inverters are used to maintain input common levels of the inverter-based amplifier associated with $v_{in,1st}$.

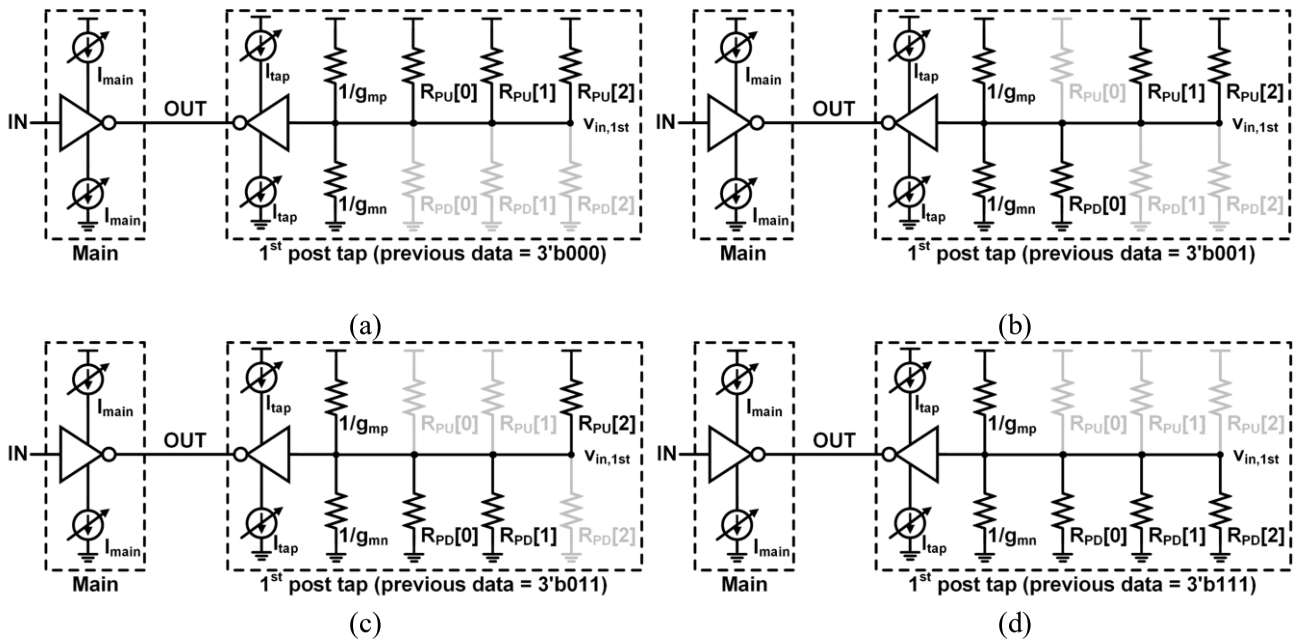


Figure 4.3.2. Equivalent circuit of inverter-based summer according to the previous data, in the cases that (a) previous data is 3'b000, (b) previous data is 3'b001, (c) previous data is '3b011 and (d) previous data is 3'b111.

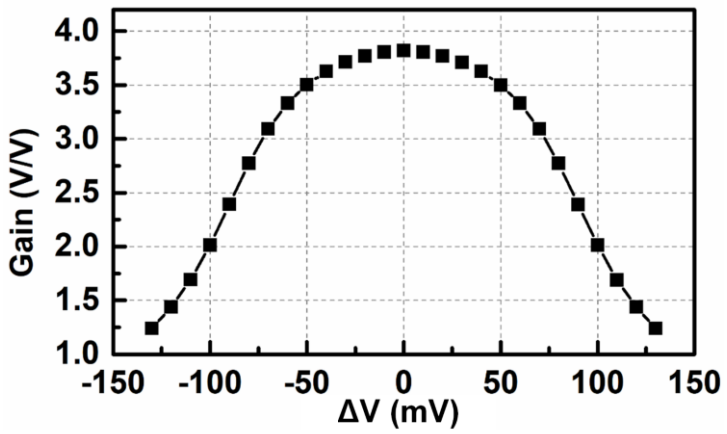
$R_{PUM}[2:0]$ and $R_{PDM}[2:0]$ act as 1st post tap coefficients for the previous data.

Figure 4.3.2 is the equivalent half circuit of the inverter-based summer based on the previous data. The inverters connected to the resistors in figure 4.3.1 act as switches. The resistors are selected based on the previous data. Since the output of the inverter-based summer is not linear, the resistors has different values controlled externally based on the ISI of the output of the summer. The sum of the coefficients (i.e., $v_{in,\,1st}$) can be expressed as follows:

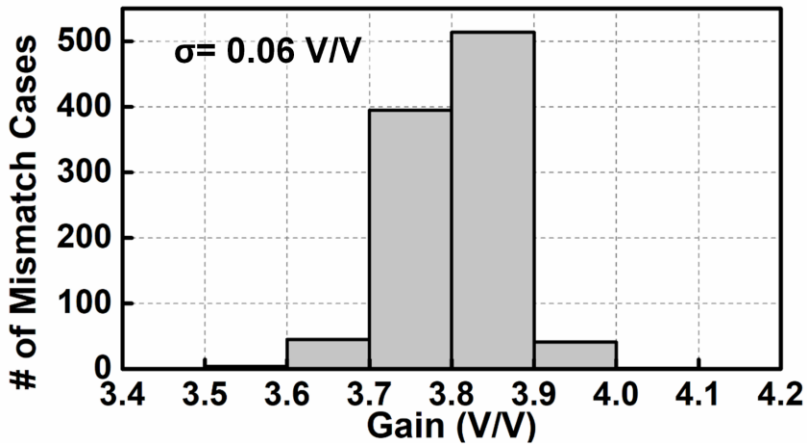
$$v_{in,1st} = \frac{(R_{PD}||\frac{1}{g_{mn}})}{(R_{PD}||\frac{1}{g_{mn}})+(R_{PU}||\frac{1}{g_{mp}})} \cdot V_{DD} \tag{4.3.1}$$

where g_{mp} and g_{mn} are the transconductances of PMOS and NMOS in the diode-connected inverter, R_{PD} and R_{PU} are the sums of the pull-down resistors and pull-up resistors respectively, and V_{DD} is the supply voltage. In the cases of figure 4.3.2 (a) and (d), inverter-based summer cannot apply the coefficients without the diode-connected inverter. In the case of the inverter-based summer without the diode-connected inverter, $v_{in,1st}$ is always V_{DD} or 0 if the previous data is 3'b111 or 3'b000 independent of the strength of the tap coefficient [2.1.1]. Therefore, the diode-connected inverter maintains the common level of the $v_{in,1st}$ and makes the inverter-based summer apply the appropriate tap coefficients. The output of the inverter-based summer can be expressed as follows:

$$v_{OUT} = A_{main} \cdot v_{IN} + A_{1tap} \cdot v_{in,1st} \tag{4.3.2}$$



(a)

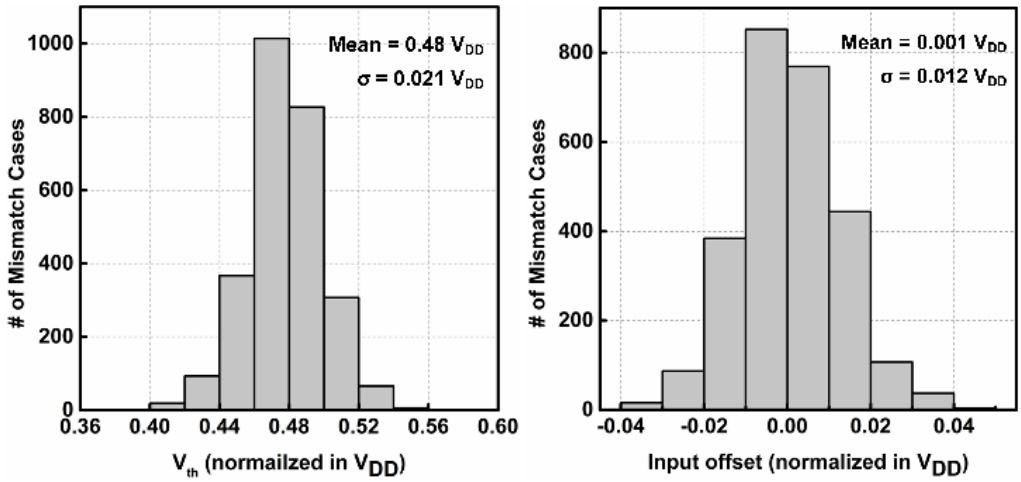


(b)

Figure 4.3.3. (a) Gain of inverter-based summer and (b) change in gain caused by mismatches in inverter-based summer based on Monte-Carlo simulation (1000 runs).

where A_{main} is the gain of the inverter-based amplifier for the main tap and A_{1tap} is the gain of the inverter-based amplifier for the first post tap. In (4.3.1), the tap coefficient is determined by not only $v_{in,1st}$, but A_{1tap}.The range of tap coefficients is widened by multiplying $v_{in,1st}$ by A_{1tap}.

Figure 4.3.3 (a) shows the gain of the inverter-based summer. As mentioned in Chapter



(a) (b)

Figure 4.3.4. Simulated variations of (a) threshold voltage of inverter-based summer and (b) input offset of blocks from AFE to inverter-based summer.

2.1, the inverter-based summer has irregular gain depending on how far the input is from the threshold voltage. The characteristic allows the inverter-based summer to amplify the eye to which the inverter-based summer is dedicated. The gain is decreased rapidly when the input swing from the threshold (ΔV) of the summer is larger than 70 mV.

Figure 4.3.3 (b) is the result of Monte-Carlo simulation of the change of the gain caused by mismatches when the input swing is 0 mV. The result is based on 1000 cases of the mismatches in the summer. In the cases of figure 4.3.3 (b), the gains of the inverter-based summer are from 3.5 to 4.0 with the standard deviation of 0.06 V/V.

Figure 4.3.4 show the variation of the threshold voltage of the inverter-based summer and input offset of the signal path including the CTLE, S2D and the summer based on Monte-Carlo simulations. The number of cases of the simulations is 2700, over the process,

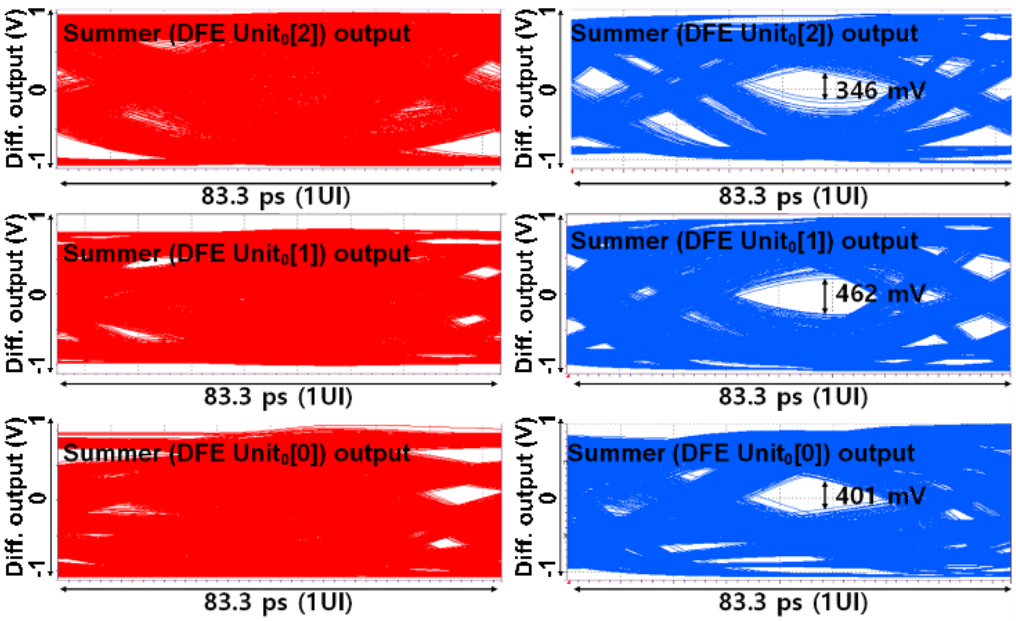
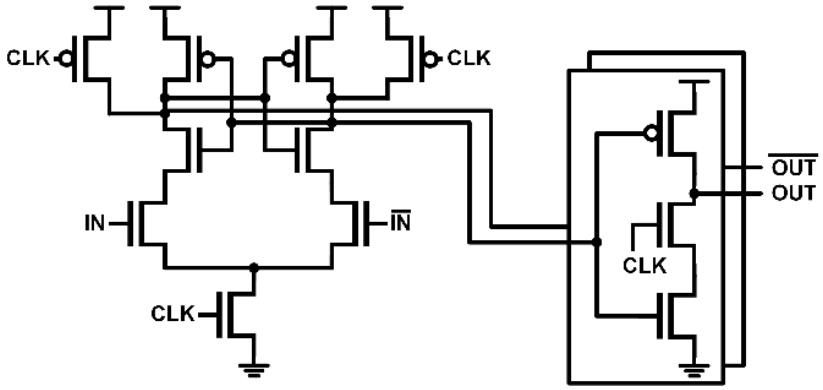


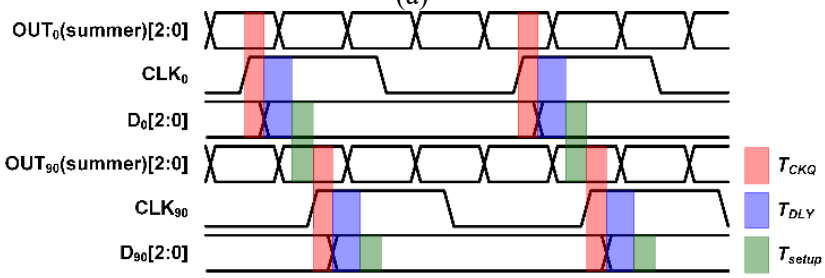
Figure 4.3.5. Simulated outputs of summers (a) without and (b) with coefficients.

voltage ($0.9 \cdot V_{DD}$ ~ $1.1 \cdot V_{DD}$), and temperature (-40 °C ~ 125 °C) variation. Memory controllers progress the calibration for the receivers during training sequence. Like the sequence the memory controller does, the operation point, such as bias and reference voltage, can be determined by the training. In addition, the blocks in the receiver is designed close together and placed symmetrically.

Figure 4.3.5 shows the simulated eye diagram of the output of inverter-based summer with a data rate of 24Gb/s and a channel loss of 9 dB at 6 GHz. Without the adequate coefficients, the eye of the inverter based summer, as shown in figure 4.3.5(a), the eye is closed. With the adequate coefficients, the summer can open the eye,. As shown in figure 4.3.5(b), the inverter-based can open each eye with the minimum eye height of 346 mV with the eye width of 23 ps. As mentioned in chapter 2.2, the summer can amplify eyes

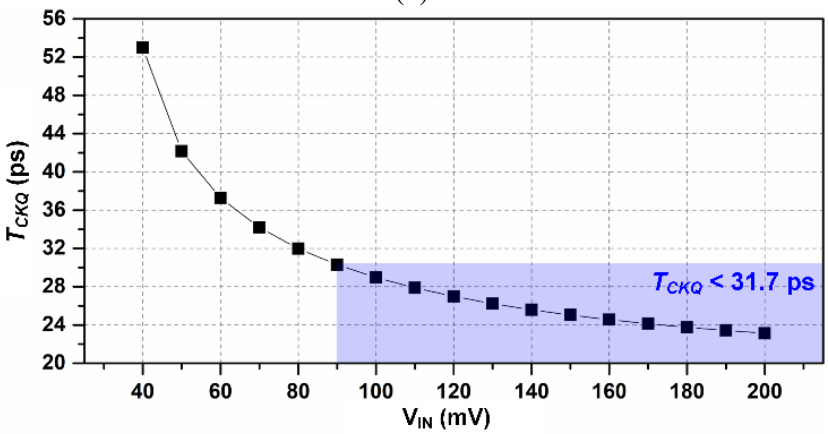


(a)



	T_{CKQ}	T_{DLY}	T_{settle}
Time (ps)	>31.7	19.3	32.3

(b)



(c)

Figure 4.3.6. (a) Structure of StrongArm slicer and buffer, (b) timing diagram of PAM-4 DFE with timing constraint, and (c) simulated clock-to-Q delay of StrongArm slicer based on input. swing.

without considering the linearity. Therefore, the inverter based summer can acquire larger

eye height, which can improve the clock-to-Q delays of the slicers in the PAM-4 DFE. Figure 4.3.6(a) is the structure diagram of the slicer and buffer in the proposed receiver. Since the StrongArm slicer is frequently utilized in memory interfaces since the slicer has low power consumption and wide output swing. However, since the clock-to-Q delay of the slicer is dependent on the input swing, the StrongArm slicer must be designed considering the sensitivity. Figure 4.3.6(b) shows the timing diagram of the PAM-4 DFE. The DFE operates with a data-rate of 24 Gb/s. Based on simulation, the propagation delay and settling time in equation 1.2.1.1 are 19.3 ps and 32.3 ps, respectively. Considering the delays, the clock-to-Q delay has to be less than 31.7 ps. Figure 4.3.6 (c) shows the simulated change of clock-to-Q delay of the slicer according to the input swing. As shown in figure 4.3.5, the inverter-based summer can reduce the clock-to-Q delay of the slicer less than 31.7 ps.

4.4 CLOCK PATH

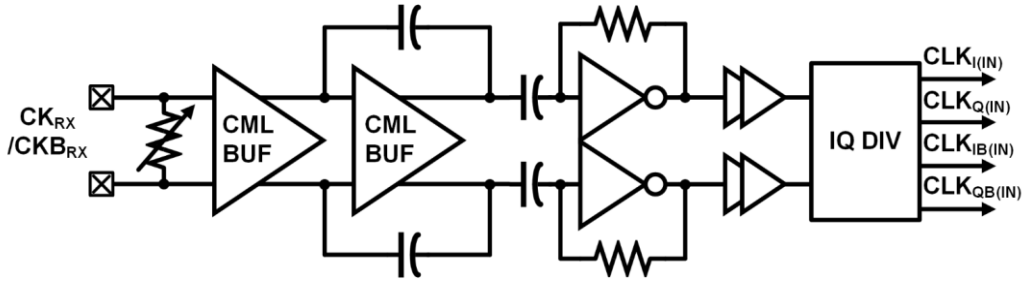


Figure 4.4.1. Block diagram of clock path before QSC.

Figure 4.4.1 shows the block diagram of the clock path which generates the quadrature clocks before the QSC. The clock path consists of a differential termination, a CML input buffer, AC coupled inverters with resistive feedback, and IQ divider (IQ DIV). The CML input buffer is composed of two-stage CML buffer, one of the two stage is with negative capacitive feedback. The input buffer amplifies the high-speed differential clocks (CK_{RX}, CKB_{RX}). The AC coupled inverters with resistive feedback are used to reduce the duty cycle distortion due to the common level of the input buffer [4.4.1]. Like the memory interfaces using quarter-rate architecture, IQ DIV generates the quadrature clocks ($CLK_{I(IN)}$, $CLK_{Q(IN)}$, $CLK_{IB(IN)}$, and $CLK_{QB(IN)}$) by dividing the high-speed clocks by two.

4.5 QUADRATURE SIGNAL CORRECTOR WITH ADAPTIVE DELAY GAIN CONTROLLER

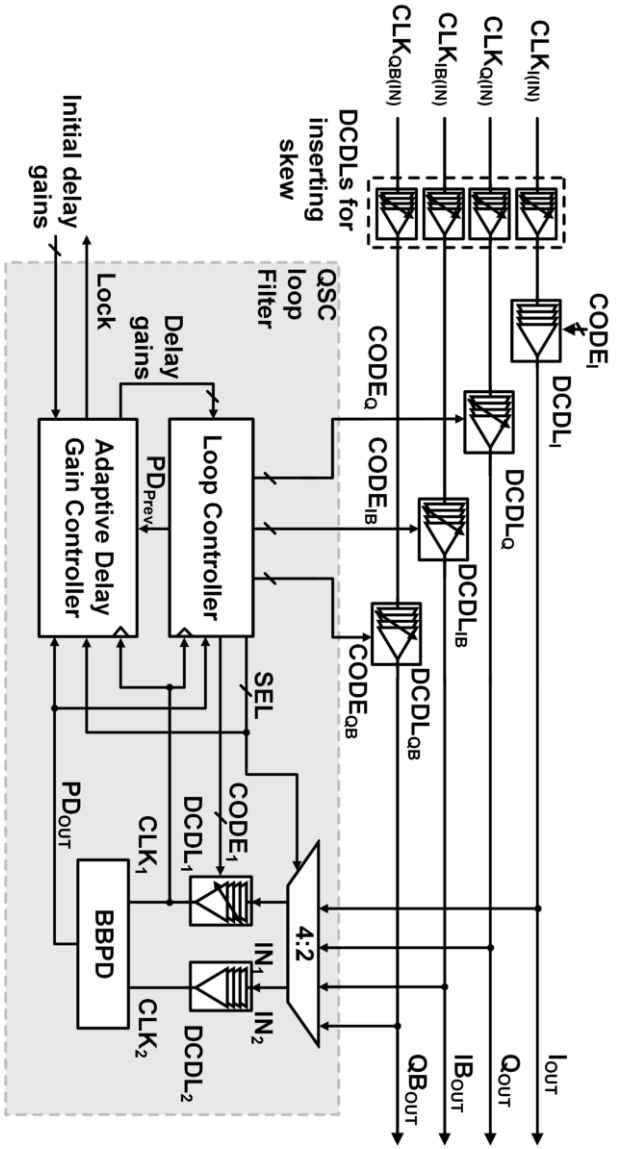


Figure 4.5.1. Block diagram of proposed QSC.

Figure 4.5.1 shows a block diagram of the proposed quadrature QSC with the adaptive

delay gain controller. The QSC can be divided into two parts: Delay controller and QSC loop filter. The delay controller consists of DCDLs ($DCDL_I$, $DCDL_Q$, $DCDL_{IB}$, and $DCDL_{QB}$), which adjusts the delay of the quadrature clocks based on the outputs of the QSC loop filter ($CODE_Q$, $CODE_{IB}$, and $CODE_{QB}$) and externally ($CODE_I$). The $DCDL_I$ is used for compensating the offset delay of the $DCDL_Q$, $DCDL_{IB}$ and $DCDL_{QB}$, and controlling the overall delay the quadrature clocks. Since the timing of the quadrature clocks are aligned based on the timing of I_{OUT}, the overall timing of the quadrature clocks can be controlled by adjusting the delay of I_{OUT}. To measure the performance of the QSC under various cases of skew, digitally controlled delay lines (DCDLs) are used before the QSC for inserting skew. The delay of the DCDLs can be controlled externally.

Figure 4.5.2 shows the circuit diagram of the DCDL. The DCDL consists of buffers

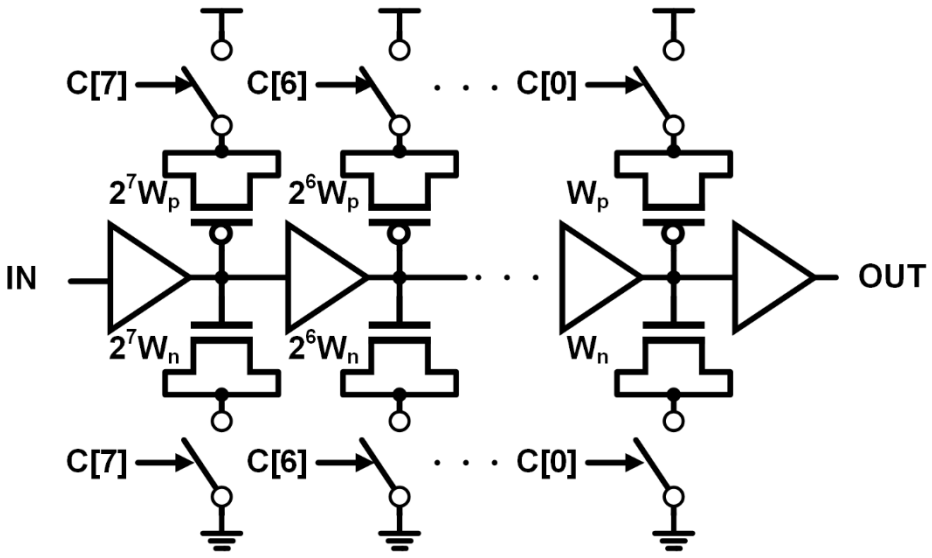


Figure 4.5.2. Block diagram of DCDL in proposed QSC.

and eight-bit digitally controlled capacitors. The overall delay can be determined by the delay code C[7:0]. The resolution of the DCDLs is 0.3 ps, with the range of 76 ps.

Figure 4.5.3 shows the block diagram of the loop filter in the QSC. The loop filter is divided into two parts: The adaptive delay gain controller and loop controller. The loop controller is composed of a timing controller (T-CON), which selects two clocks to compare, an adder to calculate new codes for DCDLs, and register set_1 and register set_2 to hold code for each DCDL and the outputs of the phase detector. The timing controller also controls the timing to update the codes of DCDLs. The adaptive delay gain controller includes shift registers to adjust the delay gains for $DCDL_Q$, $DCDL_{IB}$, $DCDL_{QB}$, and $DCDL_A$ (G_Q, G_{IB}, G_{QB}, G_A in figure 4.5.3) separately. The logic gates determine whether the shifter registers operate or not based on the relationship of the previous and current outputs of phase detectors (i.e. PD_{PREV}, and PD_{OUT}, respectively). The lock detector in the adaptive delay gain controller asserts lock signal (Lock) based on the delay gains of the DCDLs.

At the start of the operation of the QSC, the delay gains of each delay can be set externally to apply appropriate delay gains based on the magnitude of initial skew. During the operation of the QSC, the XOR gate compares the current output of the BBPD (PD_{OUT}) and previous output (PD_{PREV}). The XOR gate asserts high when PDOUT and PDPREV are different. It means that the delay gain of the corresponding DCDL need to be reduce, as explained in chapter 3.2. The AND gate pass the clock to the shift register corresponding to the delay gain of the DCDL to reduce the gain. Since the skew between the quadrature clocks are not always equal, the appropriate delay gains of each DCDL are different.

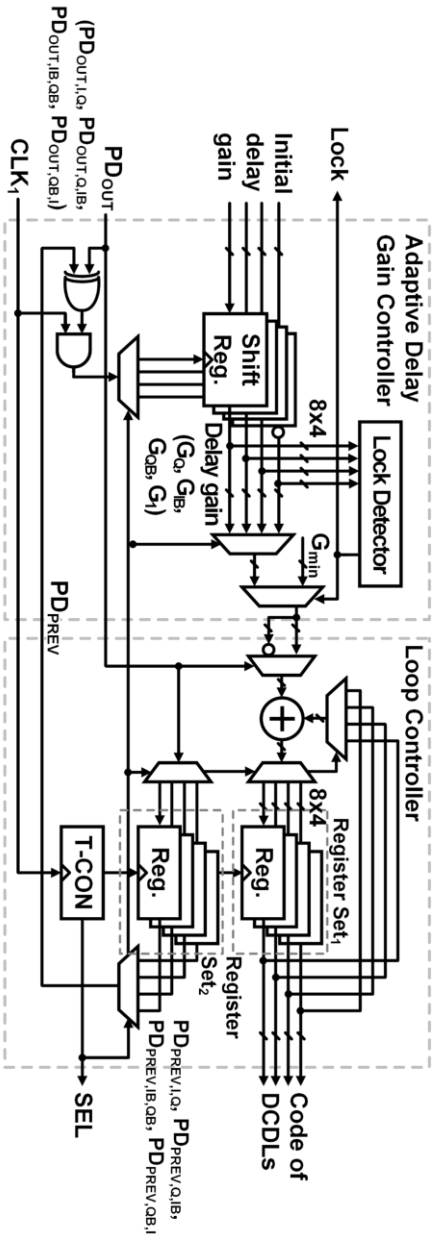


Figure 4.5.3. Block diagram of loop filter in proposed QSC.

Therefore, each DCDL need different delay gain and the four shifter registers are used. As the operation of the QSC continues, all of the delay gains reaches G_{min}. After that, since the shifter registers output G_{min} without the change, the shifter registers do not need to operate.

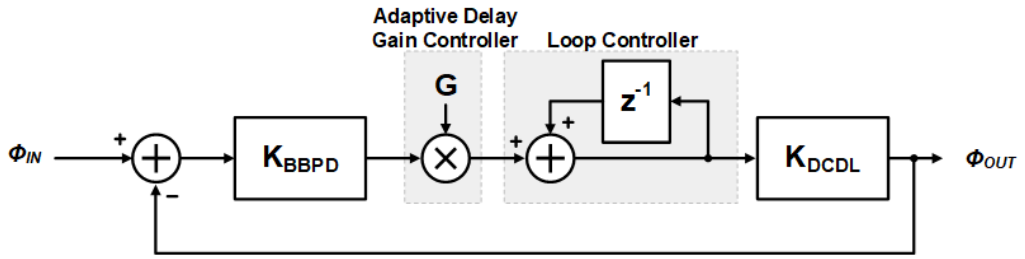


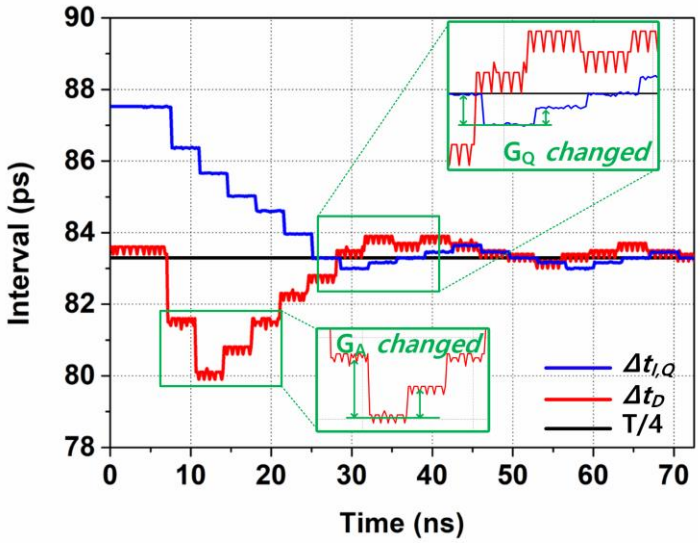
Figure 4.5.4. Block diagram of QSC in z-domain.

Therefore, the output of adaptive delay gain controller holds G_{min} after the lock detector asserts Lock, which can be reduce the power consumption of the loop filter. The QSC continues the operation with G_{min} to track small change caused by noise from clock distribution

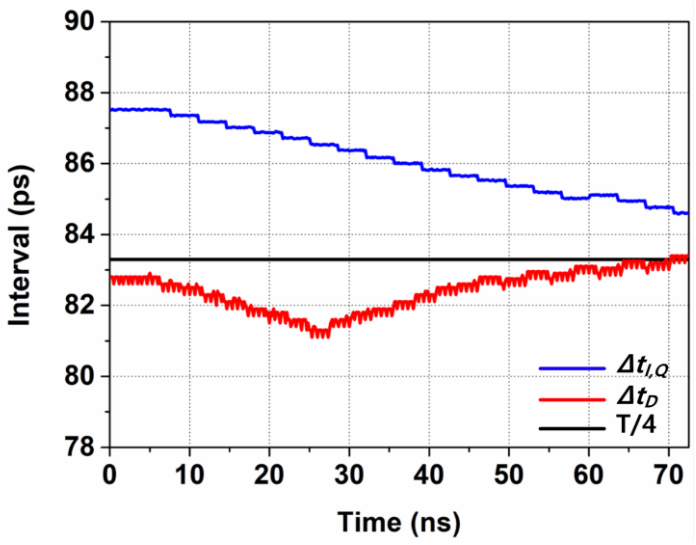
The QSC is composed of four loops for Q_{OUT}, IB_{OUT}, QB_{OUT} and Δt_D that operate sequentially. Figure 4.5.4 shows the transfer function of each loop in z domain. Figure 4.5.4 can be expressed as follows:

$$\frac{\emptyset_{OUT}}{\emptyset_{IN}} = \frac{G \cdot K_{BBPD} \cdot K_{DCDL}}{G \cdot K_{BBPD} \cdot K_{DCDL} + 1} \cdot \frac{1}{1 - \frac{1}{G \cdot K_{BBPD} \cdot K_{DCDL} + 1} \cdot z^{-1}} \tag{4.5.1}$$

where K_{BBPD} is the gain of the BBPD, K_{DCDL} is the gain of the DCDL, and G is the delay gain of each loop. The transfer function each loop, Φ_{OUT}/Φ_{IN}, is $\Delta t_D/\Delta t_{QB,I}$, $\Delta t_{I,Q}/\Delta t_D$, $\Delta t_{Q,IB}/\Delta t_D$, and $\Delta t_{IB,QB}/\Delta t_D$ in z domain. In (4.5.1), the QSC is a low pass filter whose bandwidth narrows as the delay gain decreases. Both the correction time and residual skew are determined by the loop bandwidth. A high bandwidth allows the loop to have short



(a)



(b)

Figure 4.5.5. Simulated changes in $\Delta t_{I,Q}$ and Δt_D in cases of (a) with adaptive delay gain controller and (b) without adaptive delay gain controller.

correction time with increased skew, while a low bandwidth allows the loop to have a small residual skew with increased correction time. The adaptive delay gain controller gradually

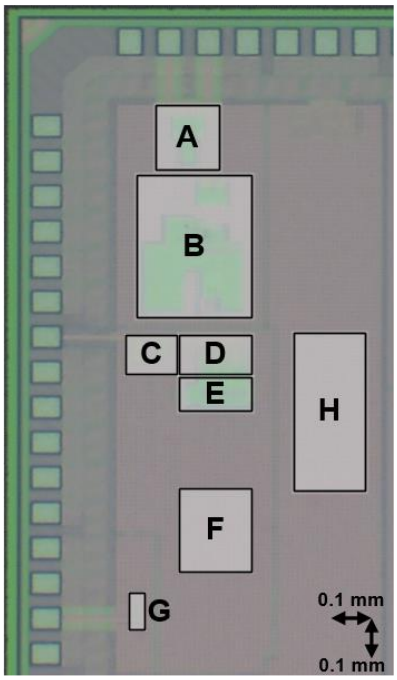
decreases the loop bandwidth from a high initial value by adjusting G. Therefore, the proposed QSC simultaneously achieves both reduced correction time and smaller skew while mitigating the trade-off between them.

Figure 4.5.5 show the simulated changes in $\Delta t_{I,Q}$ and Δt_D depending on the adaptive delay gain controller. The frequency of the quadrature clocks used in figure 4.5.5 is 3 GHz and the bandwidth of the QSC is 0.3 GHz. In figure 4.5.5(a), the adaptive delay gain controller starts the operation with the largest delay gains, which is inserted externally. Then, the adaptive delay gain controller modifies the delay gains as the QSC operates, decided by checking the change of the difference between $\Delta t_{I,Q}$ and Δt_D. The loop controller makes difference between $\Delta t_{I,Q}$ and Δt_D smaller, while Δt_D is getting closer to 83.3 ps (T/4). As shown in figure 4.5.5(a) and 4.5.5(b), the adaptive delay gain controller makes the QSC correct the skew quickly.

CHAPTER 5

EXPERIMENTAL RESULTS

5.1 EXPERIMENTAL SETUP



	Block description
A	IQ Divider & Buffer
B	DCDLs & QSC
C	On-die termination
D	CTLEs & S2Ds
E	PAM4 DFE
F	V_{ref} gen & Coeff. controller
G	Output driver
H	I2C

Figure 5.1.1. Die photograph and block description of prototype receiver.

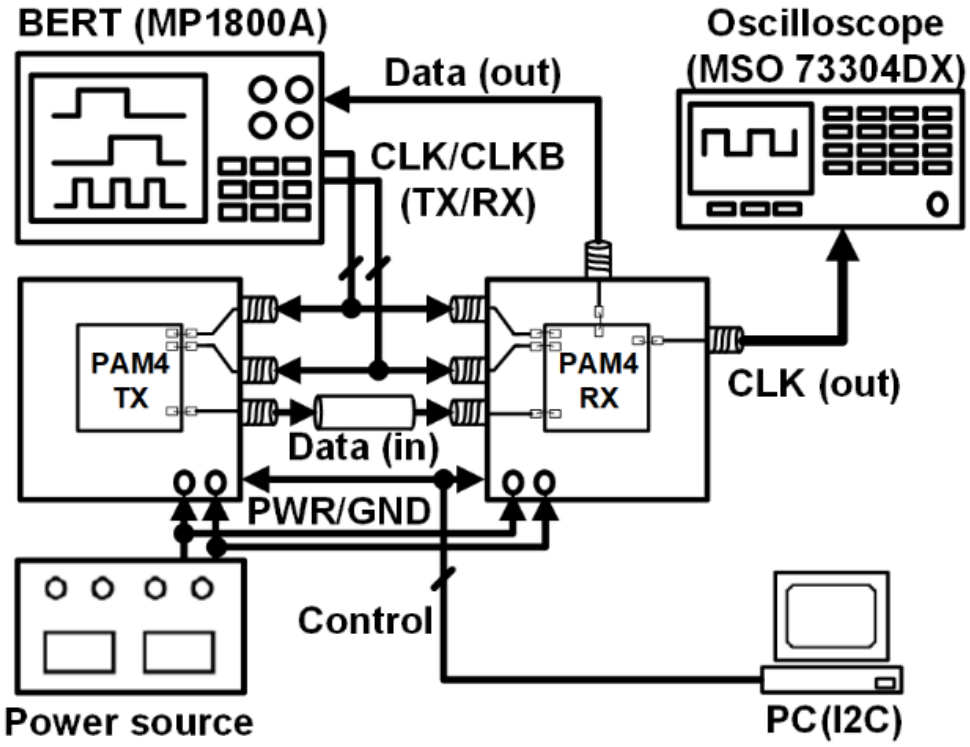


Figure 5.1.2. Measurement setup.

Figure 5.1.1 shows the die photograph and the block description of the prototype receiver for verifying the effectiveness of proposed receiver. The prototype chip is fabricated in 65 nm CMOS process with the supply voltage of 1.2 V. The total active area of the receiver is 0.071 mm^2.

Figure 5.1.2 shows the measurement setup. To measure the performance of the prototype receiver under the environment similar to memory interfaces, a single-ended PAM-4 transmitter is used [1.1.4]. Any transmitter-side equalization is not used to measure the effectiveness of receiver-side equalization only. A bit-error rate tester (BERT) applies

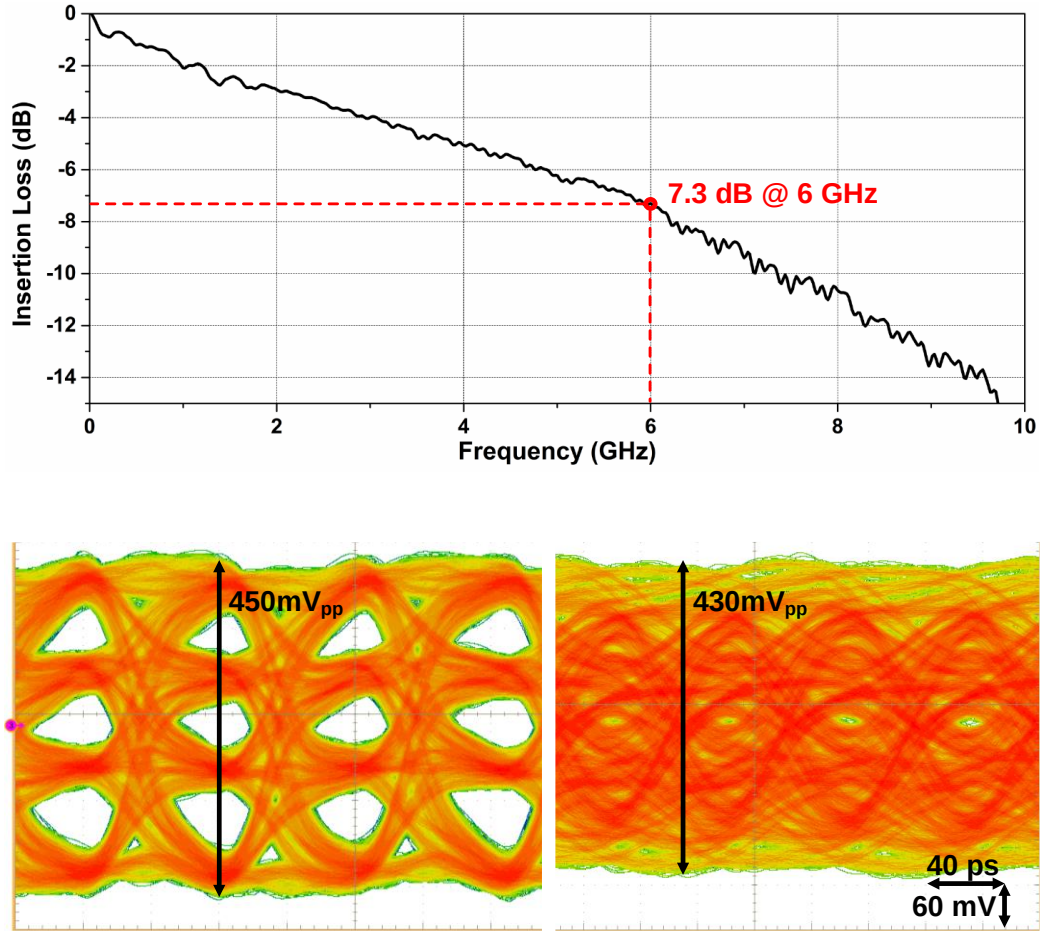


Figure 5.1.3. (a) Measured insertion loss of channel and (b) eye diagram of input signal before channel and (c) after channel.

6 GHz differential clocks to the transmitter and the receiver and measure the signal integrity of the receiver. The channel used for the measurement consists of SMA connectors, cables, and 8.5-inch FR4 PCB trace. An oscilloscope is used for measuring the skew between the outputs of the clocks (3 GHz) before and after the operation of the QSC.

Figure 5.1.3 (a) shows frequency response of the channel. As shown in figure 5.1.3(a), the channel loss is -7.3 dB at 6 GHz, which is the Nyquist frequency. Figure 5.1.3 (b) and

(c) show the eye diagram of the input of the receiver before and after channel with a data-rate of 24 Gb/s, respectively. The eyes are closed after the transmission of data through the channel. The input of the receiver can be worsened due to the parasitic components such as the test board bonding wire, and pad capacitance of the prototype chip [1.1.5].

5.2 EXPERIMENTAL RESULTS

5.2.1 MEASUREMENT RESULTS OF PAM-4 RECEIVER WITH DECISION FEEDBACK EQUALIZER USING INVERTER-BASED SUMMER

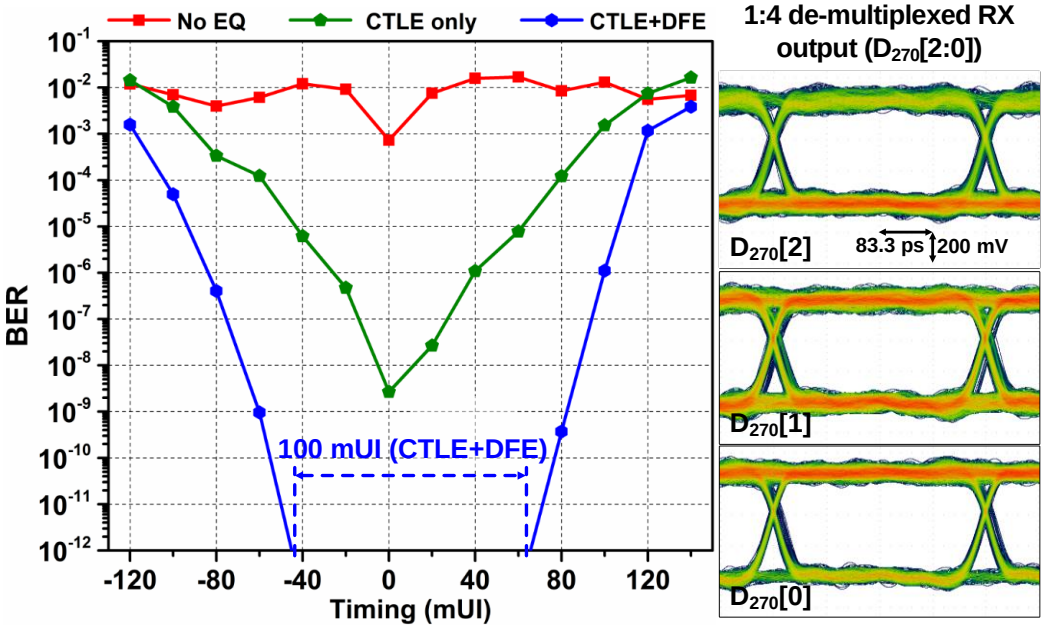


Figure 5.2.1.1. Measured BER curves according to equalization of receiver and demulplixed outputs of receiver.

We used pseudo random bit sequence seven (PRBS-7) patterns with a data-rate of 24 Gb/s. for the measurement. Figure 5.2.1.1 (a) shows the signal integrity by measuring BER curves depending on the equalizations of the receiver. Without any equalization, the eye cannot be opened, as shown in figure 5.1.3 (b). When only CTLEs are used for the equalization, the receiver can only achieve a BER of 10^{-8}. The receiver can achieve a BER of 10^{-12} with a minimum eye width of 100 mUI when the CTLEs and the proposed DFE with inverter-based summer are used. Figure 5.2.1.1 (b) shows the 1:4-demuxed output

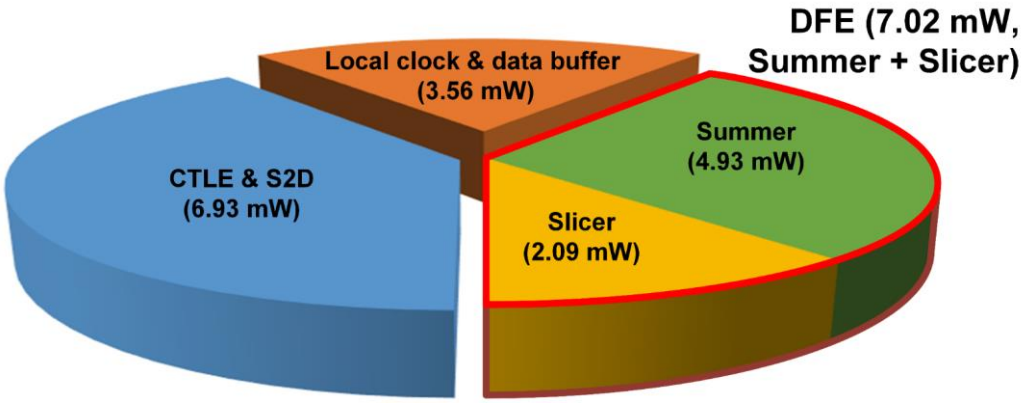


Figure 5.2.1.2. Power breakdown of proposed receiver.

(D_{270}[2:0]).

Figure 5.2.1.2 shows the power breakdown of the proposed receiver. At 24 Gb/s, the receiver consumes 17.5 mW totally. The CTLEs and S2D consume 6.93 mW, and the DFE consumes 7.02 mW. In the DFE, the inverter-based summers consume 4.93 mW and the slicers consume 2.09 mW. The receiver can achieve an energy efficiency of 0.73 pJ/b at 24 Gb/s.

Table 5.2.1.1 shows the performance comparison of our PAM-4 receiver with the previous PAM-4 receiver. In Table 5.2.1.1, our PAM-4 receiver has improved energy efficiency by using the inverter-based summers, which can reduce the power consumption of slicers. Compared to [1.2.1.2], our PAM-4 receiver has higher power consumption of the DFE, but overall power consumption is lower than [1.2.1.2] since [1.2.1.2] need the additional phase adaptation for TSSAs.

Table 5.2.1.1. Performance comparison with previous PAM-4 receivers

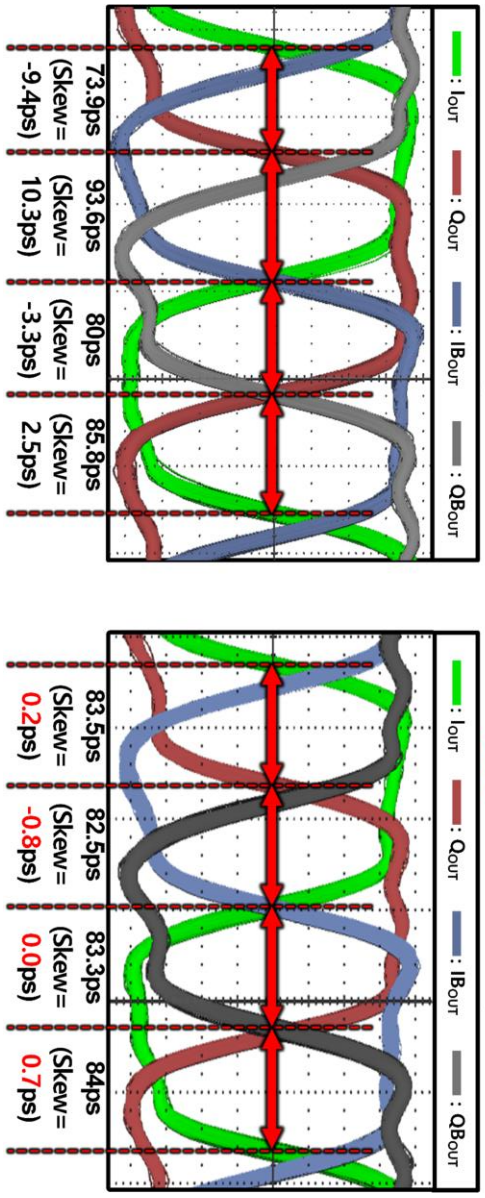
	JSSC ‘21 [1.2.1.1]	JSSC ‘19 [5.2.1.1]	ISSCC ‘18 [1.2.1.2]	ISSCL ‘18 [2.1.1]	ISSCC ‘21 [5.2.1.2]	This work
Process (nm)	28	65	65	16	1y	65
Input	Differential	Differential	Differential	Differential	Single-ended	Singled-ended
Data-rate (Gb/s/pin)	30	28	16	28	22	24
Equalization	2-stage CTLE, 2-tap DFE	CTLE, 1-tap FIR & 1-tap IIR DFE	CTLE, 1-tap DFE	Inverter-based CTLE, ADC based FFE & DFE	CTLE	CTLE, 1-tap DFE with inverter-based summer
Slicer	Track-and-regenerate slicer	CML slicer	TSSA*	N/A	Dual-tail latch	StrongArm slicer
Energy efficiency (receiver, pJ/b)	1.10	3.24	1.71**	3.32	N/A	0.73
Energy efficiency (DFE, pJ/b)	0.43	2.96	0.20	N/A	N/A	0.27
Energy efficiency (slicers, pJ/b)	0.21	2.87	N/A	N/A	N/A	0.09
Channel loss (dB)	8.2 @ 15 GHz	20.8*** @ 14 GHz	23*** @ 8 GHz	32*** @ 14 GHz	2 @ 5.5 GHz	7.3 @ 6 GHz

* Two-stage sense amplifier

** Excluding clock distribution

*** Including TX feedforward equalization

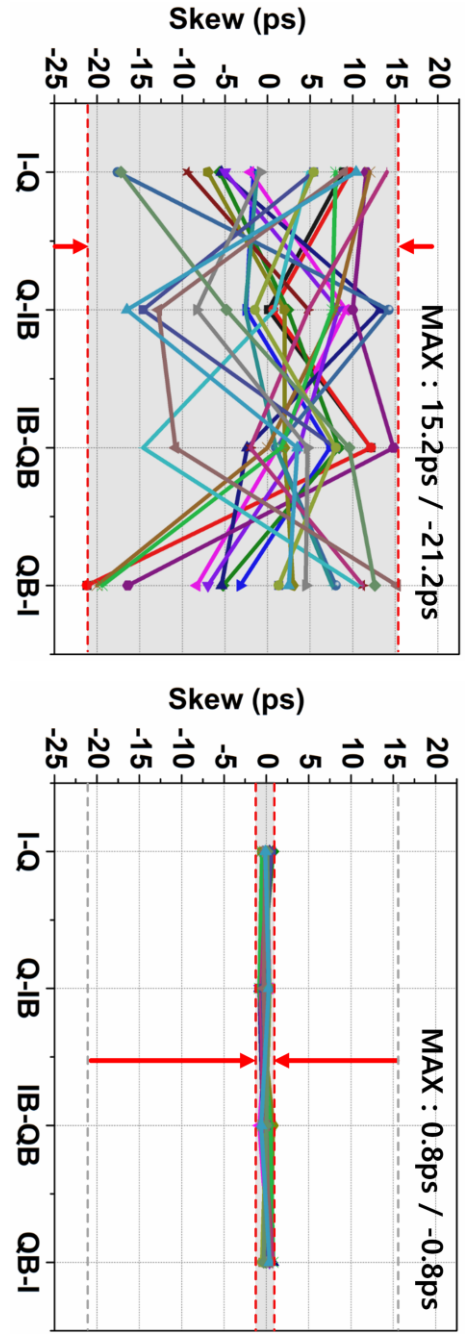
5.2.2 MEASUREMENT RESULTS OF QUADRATURE SIGNAL CORRECTOR USING ADAPTIVE DELAY GAIN CONTROLLER



(a) (b)

Figure 5.2.2.1. (a) Measured quadrature clocks (a) before QSC operation and (b) after operation of QSC.

Figure 5.2.2.1 shows measured waveforms of the quadrature clocks with a frequency



(a) (b)

Figure 5.2.2.2. (a) Measured skew between quadrature clocks (a) before and (b) after skew correction with proposed QSC.

of 3 GHz before and after the operation of the QSC. In the ideal case, the timing differences

between the quadrature clocks are equal to 83.3 ps. As shown in figure 5.2.2.1(a), the maximum skew between the clocks is -10.3 ps. In figure 5.2.2.1(b), the skew is reduced to 0.8 ps.

Figure 5.2.2.2 shows 22 cases of skew between the quadrature clocks depending on the operation of the proposed QSC. In figure 5.2.2.2(a), the range of input skew is from -21.2 ps to 15.2 ps, As shown in figure 5.2.2.2(b), the skew were reduced to 0.8 ps after the operation of the QSC.

Figure 5.2.2.3 shows the correction depending on the adaptive delay gain controller. By using the adaptive delay gain controller, the correction can be reduced by an average factor of 3.8.

Figure 5.2.2.4 shows the power breakdown of the QSC. The QSC consumes 6.45 mW totally. The DCDLs ($DCDL_I$, $DCDL_Q$, $DCDL_{IB}$, and $DCDL_{QB}$) consumes 3.39 mW, which is the largest in the QSC. The loop filter consumes 3.06 mW, of which the adaptive delay gain controller consumes 0.24 mW.

Figure 5.2.2.5 shows the BER curves of the receiver depending on the operation of the proposed QSC operation in the environments with the maximum input skew of 8 ps (#1), 9.2 ps (#2), and 12 ps (#3). As shown in figure 5.2.2.5, the BER curve with the receiver with the QSC can achieve better eye width than the cases without the QSC.

Table 5.2.2.1 shows the comparison of the previous skew correctors with the proposed QSC in this thesis. Figure of merit (FoM) is an indicator of the extent to which the trade-off between the accuracy and the correction time has been alleviated [1.3.1.2].

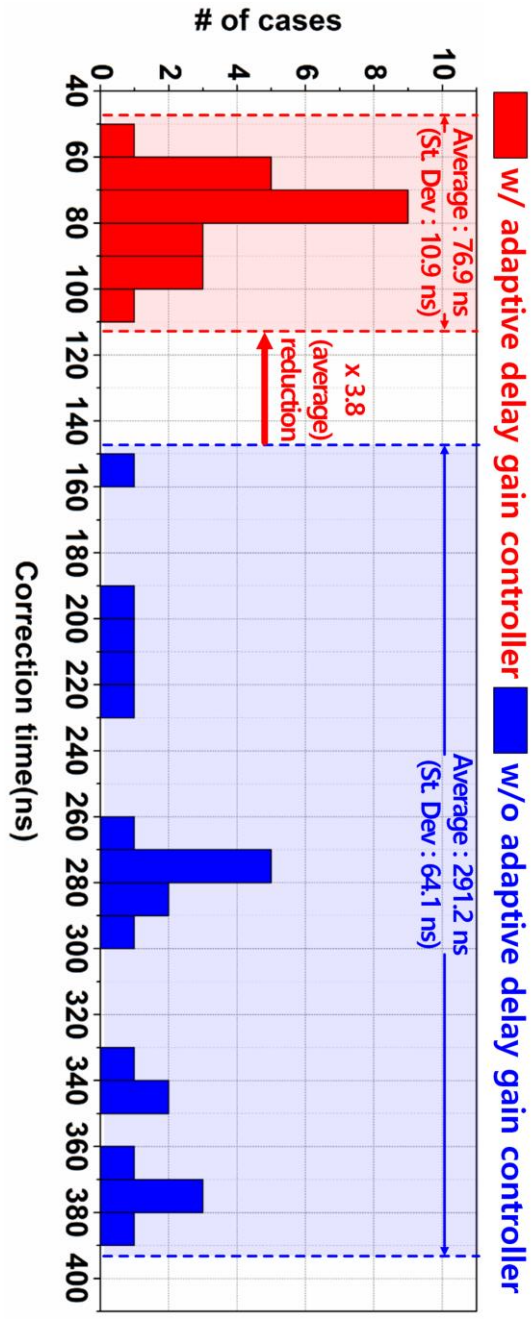


Figure 5.2.2.3. Measured correction time depending on operation of adaptive delay gain controller.

eye diagrams for a PRBS7 pattern at 6.4 Gb/s. The 12 mm length stub has a reflection

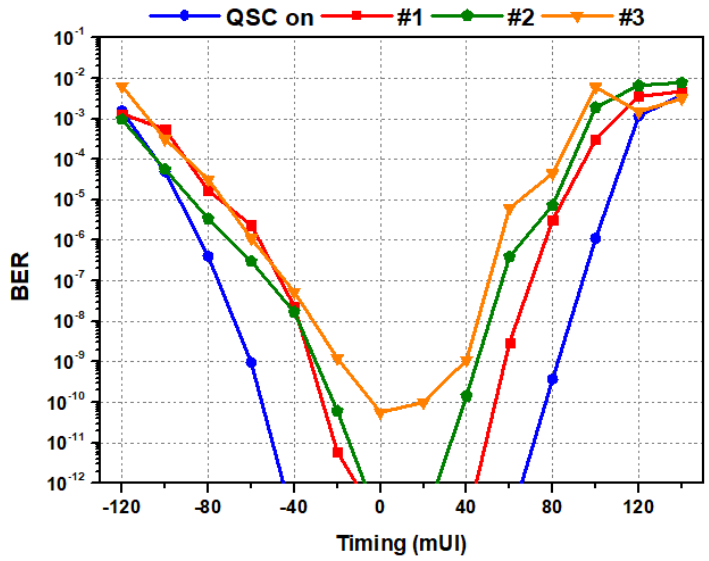


Figure 5.2.2.5. Measured BER curves depending on operation of QSC and skew.

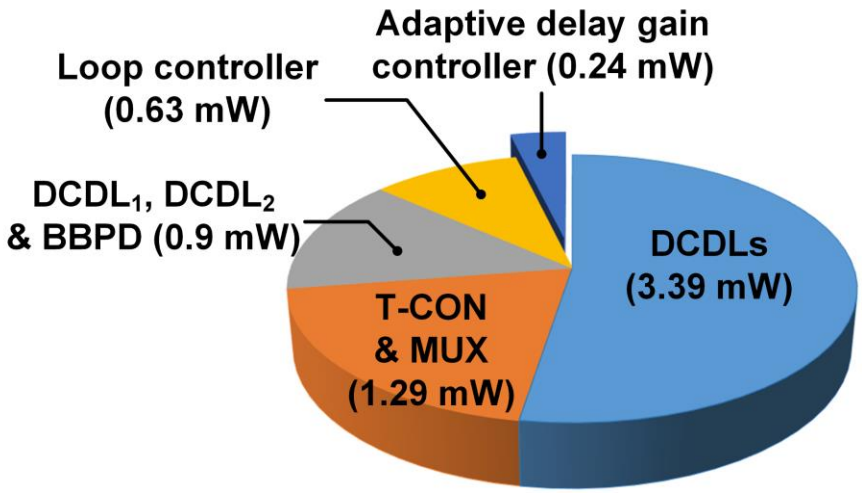


Figure 5.2.2.4. Power breakdown of QSC.

Table 5.2.1. Performance comparison with previous skew correctors.

	TCASII '17 [1.3.2.3]	TVLSI '17 [1.3.3]	TCASII '14 [1.3.2.2]	IEICE '18 [1.3.2.4]	ISSCC '20 [3.2.1]	This work
Process (nm)	65	130	130	65	40	65
Frequency (GHz)	1.25	0.1 ~ 2	0.4 ~ 0.8	0.9 ~ 1.1	0.8 ~ 2.3	3
Loop filter	Single loop filter	Analog feedback	Four 90° controller	Duty cycle corrector with SAR argorithm	Single loop filter with minimum delay tracking & SAR algorithm	Single loop filter with adaptive delay gain controller
Correction range (ps)	10.4 @ 1.25 GHz	63 @ 1 GHz	34.6 @ 0.8 GHz	40 @ 1 GHz	101.6 @ 2.3 GHz	21.2 @ 3 GHz
Resolution (ps)	0.8 @ 1.25 GHz	N/A	5.08 @ 0.8 GHz	5 @ 1 GHz	1.23 @ 2.3 GHz	0.3 @ 3 GHz
Residual skew (ps)	1.1 @ 1.25 GHz	4.1 @ 2 GHz	6.25 @ 0.8 GHz	5 @ 1 GHz	2.1 @ 2.3 GHz	0.8 @ 3 GHz
Correction time (ns)	N/A	N/A	93.75 @ 0.8 GHz	56 @ 1 GHz	500 @ 2.3 GHz	76.9 @ 3 GHz
Power efficiency (mW/GHz)	1.82	3.24	4.13	2.6	3.87	2.15
FoM[a] (ns)	N/A	N/A	0.38	0.28	0.76	0.07

[a.] FoM = resolution · (correction time / clock period)

TCASII '17 TVLSI '17 TCASII '14 IEICE '18 ISSCC '20 This work

CHAPTER 6

CONCLUSION

In this thesis, a single-ended PAM-4 receiver with the DFE using the inverter-based summers and the QSC using the adaptive delay gain controller for next-generation memory interfaces has been proposed. PAM-4 signaling has an advantage that can double data-rate without increasing clock and Nyquist frequency. However, PAM-4 signaling is more vulnerable to noise than NRZ signaling since PAM-4 signaling has 1/3 less eye height compared to NRZ signaling. The DFE is an attractive option because the DFE can equalize the signal without amplifying noise. However, the performance of PAM-4 DFE is limited by the smaller eye height, which degrade the clock-to-Q delay of the slicers in the DFE. The proposed DFE with inverter-based summer can alleviate the degradation of performance by using the inverter-based summers. Compared to previous PAM-4 DFE, the summers in the proposed PAM-4 DFE are dedicated to each slicer, the DFE can equalize and amplify the signal without considering the linearity. By amplifying each eye, the clock-to-Q delay of the slicers can be reduced without increasing the power consumption of the slicers, which can improve the performance of the PAM-4 receiver.

To verify the effectiveness of the PAM-4 receiver, a prototype receiver is fabricated

in 65 nm CMOS process. The prototype chip can achieve a BER of 10^{-12} with a minimum eye width of 160 mUI at 24 Gb/s and an channel loss of -7.3 dB. The power efficiency of the PAM-4 receiver is 0.73 pJ/b. The PAM-4 receiver is implemented with single-ended input, which is suitable for memory interface with a limited pin count.

Quarter-rate architectures have been applied to memory interfaces because the architectures have advantages of increasing the data rate without increasing the clock frequency, relaxing the timing margin of memory interfaces, and reducing power consumption in the clock distributions. However, skew between the quadrature clocks degrades overall performance of memory interfaces. Skew correction must be performed but the correction time must be considered. The proposed QSC including the adaptive delay gain controller has been proposed in this thesis. The adaptive delay gain controller checks the skew between the quadrature clocks and generates the delay gains for the DCDLs. The adaptive delay gain controller modifies delay gains based on the change of sign of skew. For shorter correction time, the delay gains for each DCDL are controlled individually.

To measure the performance of the proposed QSC, a prototype chip was fabricated in 65 nm CMOS process. The prototype QSC can reduce skew between the quadrature clocks from 21.2 ps to 0.8 ps with the resolution of 0.3 ps. The average correction time of 76.9 ps can be achieved with the adaptive delay gain controller. Compared to the operation of the QSC without the adaptive delay gain controller, the adaptive delay gain controller can reduce the correction by a factor of 3.8. The proposed QSC can alleviate the trade-off between the residual skew and the correction time. The power efficiency of the QSC is 2.15 mW/GHz.

By using the DFE with inverter-based summer and the QSC including the adaptive delay gain controller, the signal integrity of interfaces can be improved, which is verified by the measurements.

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한글초록

본 연구에서는 메모리 인터페이스를 위한 4 레벨 펄스 진폭 변조 (PAM-4) 수신기와 직교 클록을 생성하는 직교 신호 보정기를 제안된다. 데이터 센터에서 증가하는 IP 트래픽은 고속 및 저전력 메모리 인터페이스에 대한 수요를 증가시켜왔다. 이러한 요구를 만족시키기 위해 클럭 및 나이퀴스트 주파수를 높이지 않고도 데이터 전송률을 높일 수 있는 PAM-4 신호가 주목을 받고 있다.

PAM-4 신호는 제로 비 복귀 신호 (NRZ) 보다 3배 낮은 수직 마진을 가지며, 이는 결정 피드백 이퀄라이저 내 슬라이스의 클럭-큐 딜레이를 증가시키며, 이로 인해 PAM-4 결정 피드백 이퀄라이저의 성능을 제한하는 요인이다.

본 연구에서는 인버터 기반의 합산기를 이용, 선택적으로 신호를 증폭시키는 결정 피드백 이퀄라이저를 사용함으로써 슬라이서의 전력 소모를 증가시키지 않으면서 슬라이서의 클럭-큐 딜레이를 줄일 수 있다.

또한, 적응형 지연 이득 컨트롤러를 포함하는 직교 신호 보정기는 높은 정확도와 빠른 스큐 보정으로 쿼드러처 클럭 간의 스큐를 교정할 수 있다.

선택적 눈 증폭 결정 피드백 이퀄라이저와 적응형 지연 이득 컨트롤러를 포함하는 직교 신호 보정기의 성능을 검증하기 위해 프로토타입 칩을 제작하였다. 제작된 칩은 65 nm CMOS 공정으로 제작되었다. 프로토타입 칩은 24 Gb/s/pin 에서 10^{-12} 의 비트 에러율을 100 mUI 의 신호 너비로 달성하였다. 프

로토타입 칩 내 PAM-4 수신기는 0.73 pJ/b 의 에너지 효율을 갖는다.

또한 적응형 지연 이득 컨트롤러를 포함하는 직교 신호 보정기는 3 GHz 쿼드러처 클럭 간 최대 21.2 ps 의 스큐를 0.8 ps 까지 줄일 수 있으며, 이 때 76.9 ns 의 교정 시간을 갖는다. 제안하는 직교 신호 보정기는 3 GHz 에서 2.15 mW/GHz 의 전력 효율을 갖는다.

주요어 : 메모리 인터페이스, 4 레벨 펄스 진폭 변조 수신기, 인버터 기반 합산기, 직교 신호 보정기

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