Master's Thesis

Design of PAM4 Transmitter for PAM4-Binary Bridge

PAM4-바이너리 브리지 칩용 PAM4 트랜스미터 설계

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August, 2022

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Abstract

With the advancement of high-performance computing systems, large-capacity data centers, and AI technologies, the level of bandwidth demand for wired communication is increasing exponentially. However, the improvement of the bandwidth per pin in the I/O circuit compared to the required bandwidth level is difficult due to various limitations of the transmission channel. This is no exception in the next generation of DRAM. While facing limitations from the perspective of research that increases data transmission speed per pin, technologies that increase I/O bandwidth by rapidly increasing the number of pins, such as High Bandwidth Memory (HBM), have also recently developed.

One of the other approaches is a multi-level signaling method. Using a multi-level signaling method instead of a conventional Non-Return-to-Zero (NRZ) signal can increase data speed at the same Nyquist frequency, which can be a good solution for the next-generation high-bandwidth I/O interface of DRAM, and so far, a four-level Pulse Amplitude Modulation (PAM-4) has been widely adopted.

However, since PAM4 DRAM is not in the mass production stage yet, there is no memory tester dedicated to PAM4 signaling. This paper proposes a transmitter block on a 32 Gb/s PAM4 binary bridge for next-generation memory testing. The low-speed data transmitted from the NRZ tester to the bridge is converted into high-speed PAM4 data through half-rate clock control and transferred to the memory. The ground termination PAM4 driver provides a single-ended output by controlling the output current with a two-tap feed forward equalizer to achieve a Level separation Mismatch Ratio (RLM) of 0.95. Bridge transmitter manufactured with 40 nm CMOS technology occupies an active area of 0.57 mm^2 and consumes 102.1 mW of power.

Keywords : PAM-4, PAM4-Binary Bridge, Memory Tester

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Chapter 1

Introduction

1.1 Motivation

Today, data traffic is increasing and is expected to continue to increase as Internet of Things (IoT), Artificial Intelligence (AI), and Machine-To-Machine (M2M) technologies develop in addition to existing computers, mobile devices, and data centers.

According to Cisco's annual Internet report, the total number of connected devices is expected to increase to 29.3 billion by 2023, and the Internet of Things will spread to 50% of all connected devices via M2M technology [1]. As the number of devices connected to the network increases, the amount of data to be processed at the same time increases, and thus an increase in data processing speed is essential. As shown in Fig. 1.1, the International Telecommunication Union (ITU) predicted that by 2030, total mobile data traffic, including M2M data, will increase exponentially to 5 zetta bytes per month due to the increase in IoT

and Machine-Type Communication (MTC).

Since most network connection devices must be equipped with memory, the I/O transmission speed of memory must also be improved to increase the communication speed between devices. And recently, multi-level signaling methods have been widely studied to improve the transmission speed of memory. The multi-level signaling scheme may increase the I/O bandwidth at the same Nyquist frequency compared to the conventional NRZ scheme. In the case of the PAM4, which is currently the most widely adopted, the bandwidth is doubled compared to NRZ.

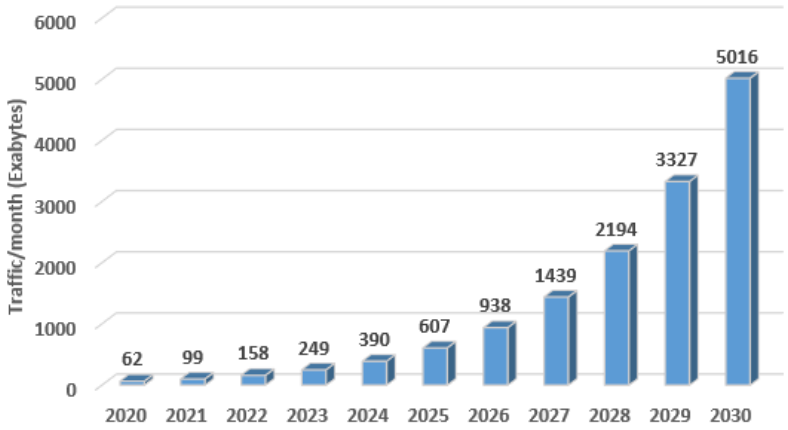


Fig. 1.1 Global mobile data traffic forecast.

However, existing test solutions of using Automatic Test Equipment/System Level Test (ATE/SLT) offer only a low-speed binary mode lacking a multi-level signaling capability, thus efficient evaluation methods for PAM4 signals must be explored. This paper introduces a

transmitter block for bridge that can test PAM4 signaling DRAM with existing test equipment for NRZ. In the PAM4-Binary bridge, the transmitter converts the NRZ signal transmitted from the test equipment into a PAM4 signal and provides VSS termination and single-ended operations considering the operation of DRAM.

1.2 Thesis Organization

This paper consists of the following. Chapter 2 briefly describes the operation of the multi-level signaling scheme, and in particular, a widely used PAM4. Then we will introduce the necessity of PAM4-Binary bridge.

Chapter 3 introduces what to consider when designing PAM4-binary transmitters to be used in DRAM, and suggests an overall circuit block completed based on this. Then, a design is proposed for each building block. In particular, the design and operation of an equalizer controlled by the amount of current and a single-ended PAM4 driver driven by current will be described.

Chapter 4 describes the performance measurement results of transmitter manufactured with 40 nm CMOS technology. The NRZ signal at 8 Gb/s speed input from the NRZ tester is converted to a PAM4 signal at 32 Gb/s speed through a bridge transmitter, showing the converted PAM4 data eye, and the RLM measurement result, the main performance of the PAM4 driver.

Chapter 5 concludes this paper by committing the proposed research.

Chapter 2

Backgrounds

2.1 Overview

Several improvement methods have been carried out to improve transmission speed in DRAM. First, from DDR1 to DDR3, the data rate was increased by increasing the number of pre-fetches, and the GDDR version used in image processing devices requiring higher speeds increased the effective clock rate per pin, and is now developed up to GDDR6. And there is a HBM, which has recently been in the spotlight since the GDDR memory.

HBM has a new method applied to the existing bandwidth increase technology. The number of existing I/Os (x8/x16/x32) has been rapidly increased to x1024, and chips have been stacked and connected using Through Silicon Via (TSV) technology to increase the number of channels. As shown in Table 2.1, the data rate per pin is lower than the GDDR memory, but the overall bandwidth is higher.

Table 2.1 Speed comparison of HBM and other DRAMs.

	DDR4	LPDDR4	GDDR6	HBM2	HBM2E	HBM3 (TBD)
Data rate	3200 Mbps	3200 Mbps	14 Gbps	2.4 Gbps	2.8 Gbps	> 3.2 Gbps
Pin count	x4/x8/x16	x16/ch	x16/x32	x1024	x1024	x1024
Bandwidth	5.4 GB/s	12.8 GB/s	56 GB/s	307 GB/s	358 GB/s	> 500 GB/s

So far, HBM is the fastest memory, but there are also disadvantages. As shown in Fig. 2.1, HBM must have TSV structure and requires a logic chip called base die, separate from a data storage chip called core die. In addition, an interposer is required to connect with the GPU and an additional process is required to assemble all of these components. Therefore, the yield decreases compared to the GDDR memory and the manufacturing cost increases.

One alternative to increasing bandwidth after HBM is the pulse amplitude modulation method. Conventional DRAMs using NRZ signaling can transmit only one data (0 or 1) per

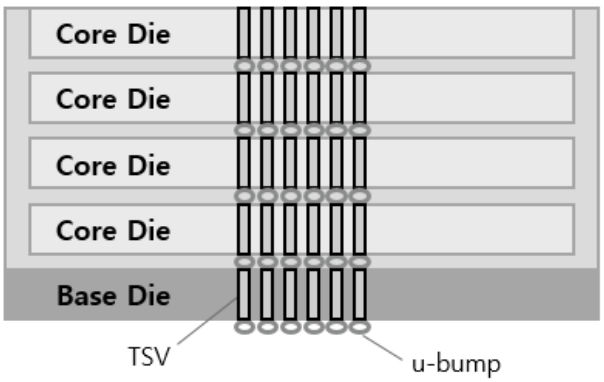


Fig. 2.1 Structure of HBM.

Unit Interval (UI) but if pulse amplitude modulation is used, multiple data can be transmitted to 1-UI. In particular, in the case of the most widely studied PAM4, two data are transmitted to 1-UI and the PAM4 method is also applied in this paper [2].

In the semiconductor industry, PAM4 methods that can be applied to memory are being studied, but there are still problems that need to be additionally considered or solved. One of them is a test problem. Until now, only the NRZ method has been applied to DRAM, so test equipment has also been developed and applied according to the NRZ method. Therefore, a solution that can test the PAM4 DRAM with the current NRZ tester should be prepared.

2.2 Basic of Multi Level Signaling

As a data transmission method, PAM4 is not a new method at the moment. It is already widely used in high-speed networking devices. However, in the memory field, many parts of the existing memory scheme must be changed to use the PAM4 method, so the application of

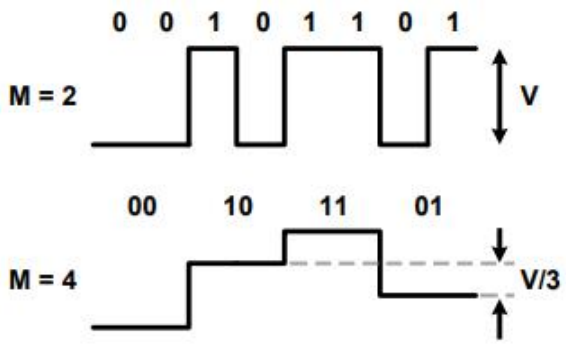


Fig. 2.2 NRZ(PAM2) and multi-level signaling(PAM4).

the PAM4 method has not been seriously reviewed.

Fig. 2.2 shows the difference between the PAM4 signal method and the NRZ signal method previously used in the memory. The NRZ signal scheme may be referred to as a kind of PAM2 scheme. The NRZ scheme can transmit one bit in one symbol, but the PAM4 scheme can transmit two consecutive bits in one symbol by adjusting the signal height. The first bit of the two consecutive bits is referred to as a Most Significant Bit (MSB) and the second bit is referred to as a Least Significant Bit (LSB). Eventually, the PAM4 method reduces the Nyquist frequency required to achieve the same bandwidth by half compared to the NRZ method [3]. For example, for the Nyquist frequency required to achieve the same 32 Gb/s data throughput, the NRZ method is 16 GHz and the PAM4 method is 8 GHz. And when the data rate is expressed as the baud rate, the NRZ method is 32 Gsymbol/s and the PAM4 method is 16 Gsymbol/s.

Then, looking at the advantages of the PAM4 method, signal attenuation occurs less compared to the NRZ method when the Nyquist frequency is reduced. And since the horizontal size of the data eye is larger than the NRZ method, it becomes less sensitive to the effect of jitter [4]. In the PAM4 method, if the same Nyquist frequency as the NRZ method is used, the baud rate is theoretically doubled.

The PAM4 method does not only have advantages over the NRZ method. The most representative disadvantage is the increase in noise effect. Since the vertical size of the PAM4 data eye is reduced to 1/3 of that of the NRZ, thus intrinsic Signal-to-Noise Ratio (SNR) loss of using PAM4 signaling compared with NRZ signaling is given by,

$$20 \cdot \log\left(\frac{1}{3}\right) \sim -9.5(dB)$$

As the pulse amplitude modulation level M increases, SNR degradation increases, and in

the case of PAM-M, the degradation of SNR is expressed as

$$20 \cdot \log(\frac{1}{M-1})(dB)$$

Based on the same bandwidth, PAM4 has half the Nyquist frequency compared to NRZ, but the horizontal size of the actual data eye is smaller than 1-UI. And as you can see in Fig. 2.3, the horizontal size of the upper and lower eyes among the three data eyes is slightly smaller [5]. For these reasons, the PAM4 method is sensitive to the effect of nonlinearity. The PAM4 method considers the degree of nonlinearity of the data eye as an important indicator because the most vulnerable eye among the three data eyes affects performance.

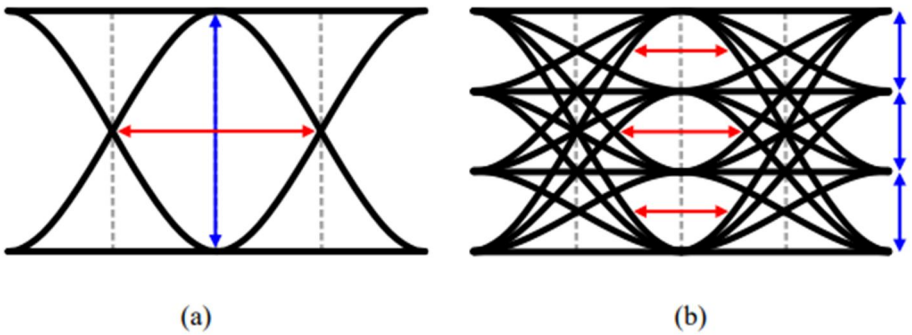


Fig. 2.3 Basic eye diagrams of (a) NRZ and (b) PAM-4 signal.

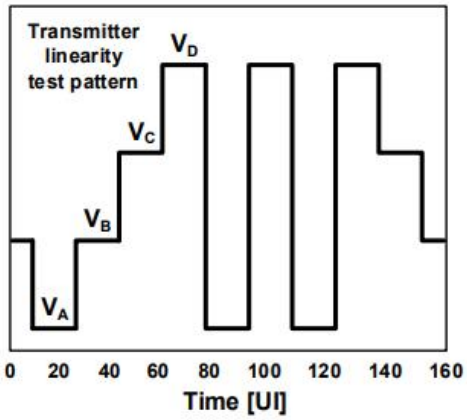


Fig. 2.4 PAM4 linearity test pattern.

The most representative method of defining the degree of nonlinearity of the PAM4 data eye is the RLM. First, one of the methods of measuring the deformation of each data eye in the PAM4 data eye diagram is to define the minimum signal level (S_{min}), and the equation is as follows [6].

$$S_{min} = \frac{1}{2}\min(V_B - V_A, V_C - V_B, V_D - V_C)$$

So, finally, RLM is defined by the following formula [6].

$$R_{LM} = \frac{6 \cdot S_{min}}{V_D - V_A}$$

In the above formula, V_A, V_B, V_C, and V_D are values measured in the PAM4 linearity test pattern shown in Fig. 2.4. In general, it is known that PAM4 transmitters must satisfy the condition RLM > 0.92 [6].

2.3 Necessity of PAM4-Binary Bridge

As mentioned earlier, the PAM4 signaling method is already widely used in the high-speed networking field, but is a completely new method in the memory field. Therefore, of course, there are many problems that follow, and one of them is the test problem.

DRAM operating in the PAM4 method cannot be tested with the currently used NRZ method memory tester. The test is an important process to verify that chips are manufactured normally and ensure reliability after shipment. This paper provides a solution that can test DRAM operating in the PAM4 method through the existing tester for NRZ.

It may be difficult to cover all test areas with only test equipment. For example, poor contact

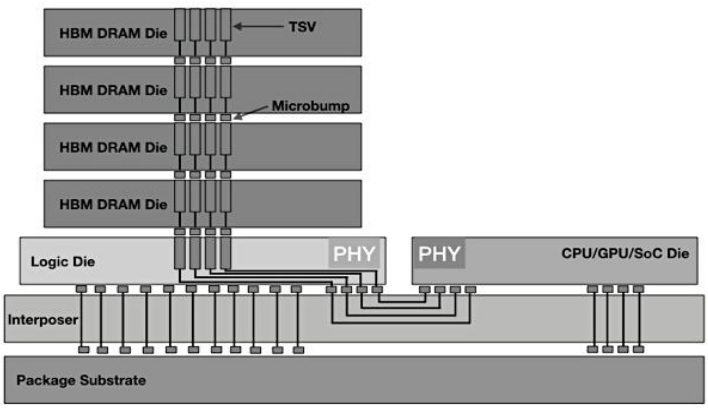


Fig. 2.5 Structure of HBM SiP (System in Package).

between the probe card of the test equipment and the pads of the DRAM, limitations of at-speed operation due to speed limitations of the test equipment, and inability to test directly when memory is mounted in a single system package as shown in Fig. 2.5.

In this case, a separate engine may be built for testing. The method in which the engine for testing is located inside the chip is called Built-In Self Test (BIST), and the method in which the engine for testing is located outside the chip is called Built-Out Self Test (BOST).

As shown in Fig. 2.6, the bridge chip proposed in this paper is located outside the memory and serves as a signal conversion between NRZ and PAM4 between the NRZ tester and PAM4 DRAM. This is a kind of Built-Out Test (BOT). In addition, the PAM4-Binary bridge transmitter to be described in this paper includes not only a function of converting NRZ signals into PAM4 signals, but also an equalizer function to compensate for signal distortion occurring in channels.

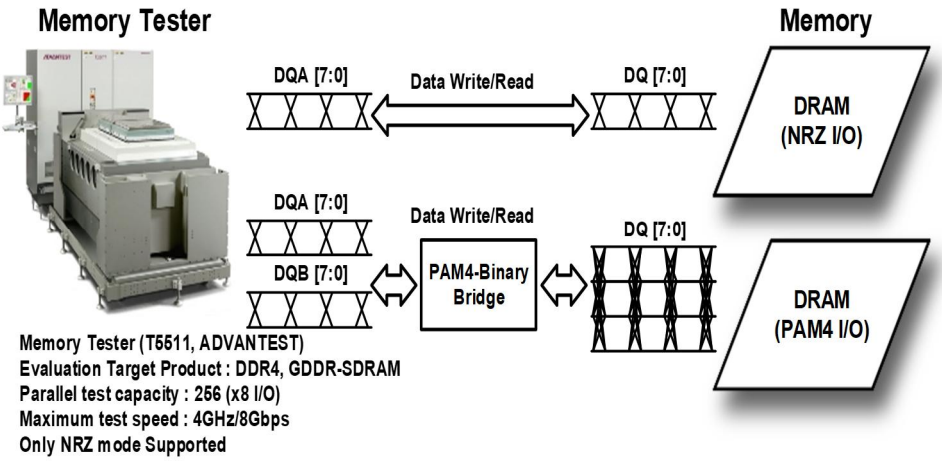


Fig. 2.6 Memory test environment with PAM4-Bianary bridge.

Chapter 3

Design of PAM4 Transmitter for PAM4-Binary Bridge

3.1 Design Consideration

When designing the PAM4 binary bridge transmitter, the circuit we consider the most is the PAM4 driver. First, it is necessary to determine whether to design the type of driver in a voltage mode or a current mode.

A voltage mode driver consumes less power than a current mode driver. On the other hand, there is a disadvantage in that the output impedance matching is difficult compared to the current mode driver [7]-[11]. If it does not match the characteristic impedance of the transmission line, distortion of the signal occurs due to the reflected wave. Impedance matching is an important factor because it is directly related to bandwidth degradation.

In the case of the current mode driver, the rise/fall time of the signal is smaller than that of the voltage mode driver, and thus the operating speed is fast. And since parallel termination resistror is used, impedance matching is also relatively easy. However, the biggest drawback is that it consumes more power than the voltage mode driver [12]-[15]. In Fig. 3.1, circuits of a typical current mode driver and a voltage mode driver are compared.

The current mode driver type was adopted in the transmitter of this paper. Although power consumption is greater than that of the voltage mode driver, it is not a circuit located inside the memory but a bridge located outside the memory, so we decided to bear the disadvantage of power consumption. Instead, it has the advantage of a relatively simple impedance matching structure and a fast operating speed.

Regardless of driver type, since the SNR characteristics of the PAM4 signal are poor compared to NRZ, a pre-emphasis circuit for a Feed Forward Equalizer (FFE) function was inserted for additional signal distortion compensation. FFE added one tab to the main tab for signal compensation, and in this paper, the post-cursor compensation method is used. This is because post-cursors have a greater effect on inter-signal interference than pre-cursors.

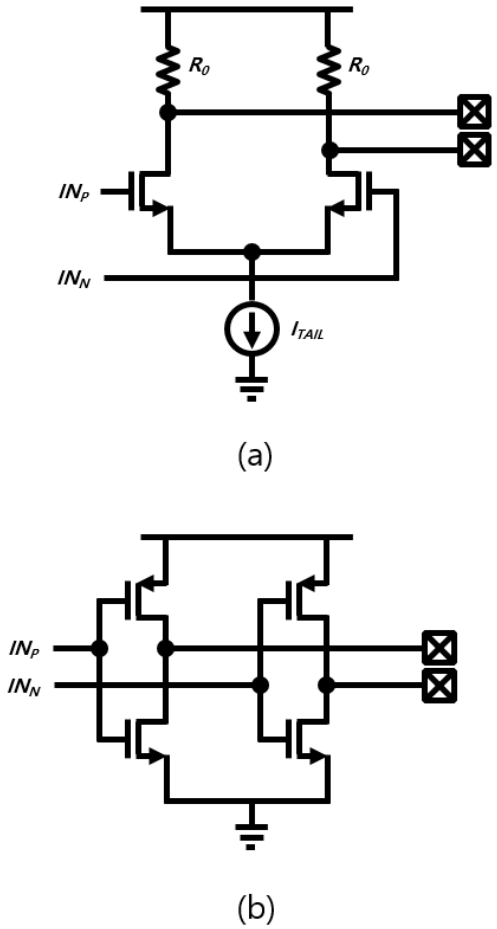


Fig. 3.1 Typical circuit diagram of conventional (a) current mode driver and (b) voltage mode driver.

When an FFE circuit is added to the current mode driver, a typical current mode driver circuit form for PAM4 may be created as shown in Fig. 3.2. Since DRAM uses a single-ended signal method, it is necessary to change the differential pair structure to a single-ended structure. In addition, in order to apply VSS termination, it is necessary to change it to the

PMOS structure rather than the NMOS structure in Fig. 3.2. When a multi-slice structure is used to adjust the coefficient of the FFE, the skew generated between the slices directly affects the characteristics of the main driver. Therefore, in this paper, a new method of adjusting the FFE coefficient by controlling the driving currents of the main tap and the post-cursor tap, respectively, was devised.

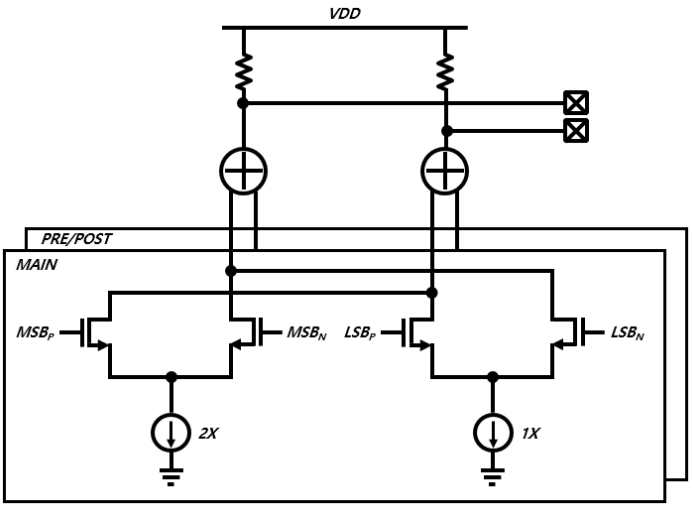


Fig. 3.2 Simplified circuit diagram of CML based PAM4 driver.

3.2 Overall Architecture

Fig. 3.3 shows the proposed PAM4-Binary bridge transmitter that allows testers that support only NRZ mode to evaluate memory with PAM4 signaling. The proposed bridge uses the WCK signaling method used in the GDDR5/6 interface. The frequency of the WCK used

in the bridge is the same as that of the WCK used in memory, so it is about twice that of the NRZ tester. The All Digital Phase Locked Loop (ADPLL) integrated into the bridge has a small area, excellent Process Voltage Temperature (PVT) tolerance, and doubles the input WCK frequency. The ADPLL output, which is an internal WCK, provides a timing criterion for data transmission after phase adjustment by a Phase Interpolator (PI) and a Duty Cycle Corrector (DCC).

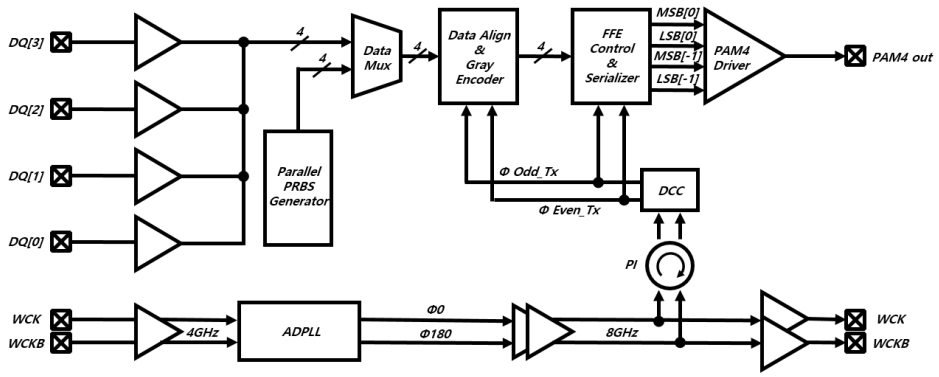


Fig. 3.3 Overall architecture of PAM4-Binary bridge transmitter.

In the case of a write operation using a PAM4 signal, the bridge first receives four NRZ data supporting VSS termination from the tester. The half-speed data is aligned in the internal WCK, and the encoder converts the NRZ into a gray-coded PAM4. The PAM4 data is then transferred to the driver by applying a 2-tap FFE function. The driver for PAM4 is a ground reference (VSS termination) and provides a single-ended output by controlling an output current with a PMOS switch.

3.3 Circuit Implementation

3.3.1 Clock Generator

The frequency of the input clock from the tester to the bridge is 4 GHz. In addition, in order for the output signal of the PAM4 transmitter to operate at 32 Gb/s, an internal clock of 8 GHz is required internally. In this paper, 4 GHz clock is increased to 8 GHz through ADPLL. The performance of the designed ADPLL is at the level of phase noise -99.2 dBc/Hz at 1 MHz offset.

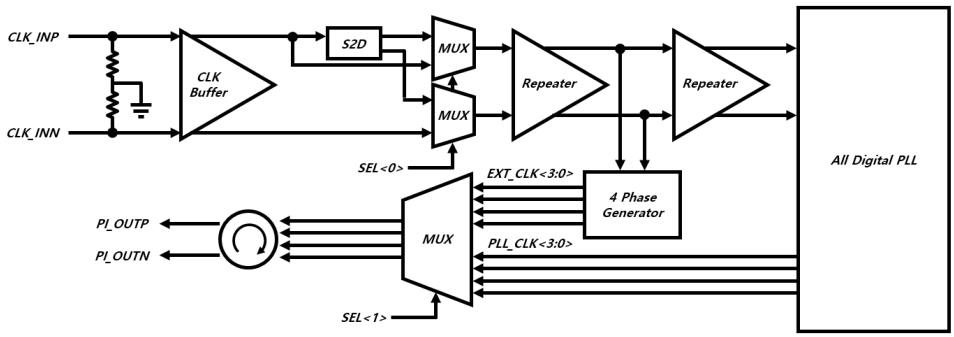


Fig. 3.4 Block diagram of internal clock generator.

As shown in Fig. 3.4, an external clock path is added for operation verification separately from the ADPLL operation. When a clock of 4 GHz is input from the outside, a clock of 8 GHz of 4-phase is output through ADPLL, which becomes an input signal of a PI. If an 8 GHz clock is input from the outside, it is transmitted as an input signal of the PI through a 4-phase generator because it does not require an ADPLL operation. If necessary, the input differential

clock can be converted to a single-ended clock. It can be operated for each case through I2C control, and the operation modes for each case are summarized in Table 3.1.

Table 3.1 Clock generator mode by SEL code.

Case	Input Source	WCK(B) Input	Single/Differential	SEL<1:0>
1	PLL Clock	4G	Differential	00
2	External Clock	8G	Differential	10
3	External Clock	8G	Single	11

The 8 GHz output clock from the ADPLL or input clock from the outside is input to the PI. PI is used to adjust the phase of the internal clock used for data align or serializer and to correct the duty cycle. The designed PI circuit is shown in Fig. 3.5. First, the CML-based PI structure was adopted because it is advantageous in terms of supply noise compared to CMOS-based PI. The CML PI adjusts the amount of current source to create a phase shift. The current amount of the current source can be adjusted up to 32 stages using the 32-bit thermometer code, and the resolution is about 1 ps. The signal output from the CML PI has a clear waveform through the AC buffer and the duty cycle is corrected.

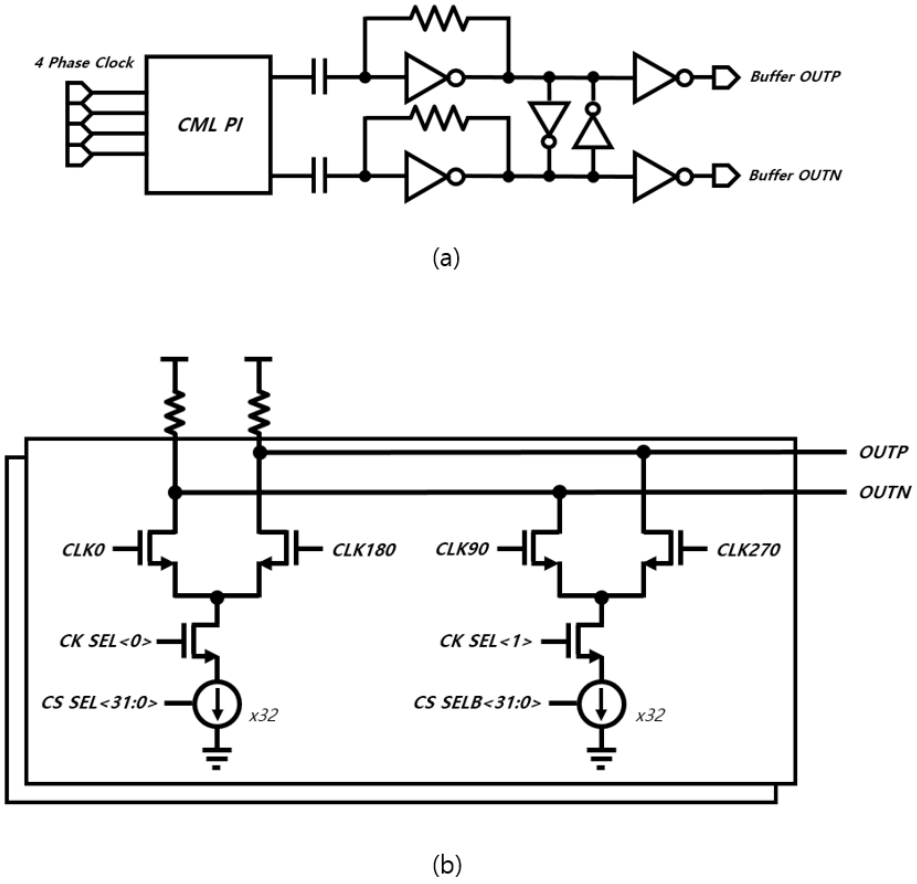


Fig. 3.5 (a) CML PI and AC buffer (b) CML based PI.

The simulation verification of the designed PI shows that, as illustrated in Fig. 3.6, when a 4-phase clock is input, a phase shift for each code is performed and output through buffer. The most important characteristic of PI circuits is linearity. And one of the most important indicators representing linearity is Differential Non-Linearity (DNL), which can be expressed as follows..

$$\mathrm{DNL} = (H_{(i)} - H_{ideal})/H_{ideal}$$

H is a difference value of each phase, and DNL is expressed as a difference value between Ideal H and current H. The DNL calculated by formula is shown in Fig. 3.7. At 8 GHz, the maximum DNL is 0.59, and if the PI code is sequentially increased, the cumulative phase delay also increases linearly.

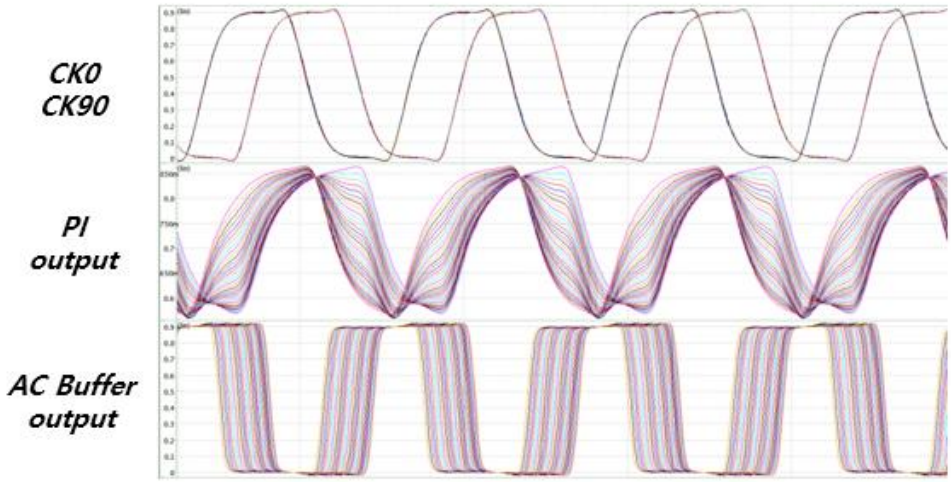


Fig. 3.6 Simulation result of PI waveform.

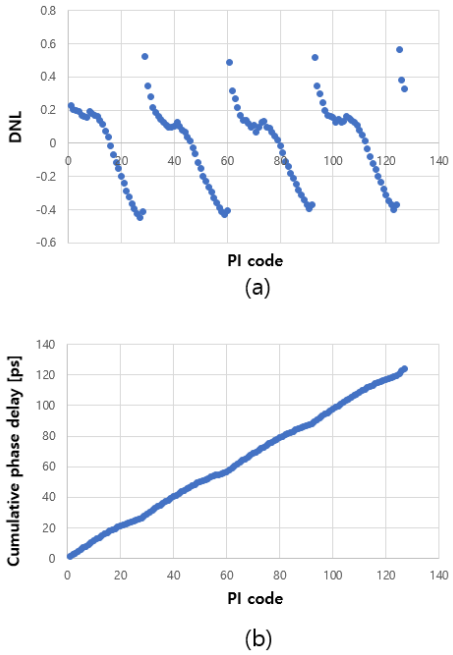


Fig. 3.7 (a) DNL and (b) Cumulative phase delay.

3.3.2 Parallel PRBS Generator

Since data can be input and output through four DQ pads connected to the outside of the bridge chip, the operation of the bridge chip can be verified through a tester. In addition, the Pseudo Random Binary Sequence (PRBS) generator circuit is designed to generate data input patterns internally without external DQ.

In this paper, the goal of the transmitter design is PAM4 signal output at a speed of 32 Gb/s (16 Gsymbol/s). In addition, since the speed of data input through an external DQ is 8 Gb/s

(maximum frequency of the tester is 4 GHz), two MSB signals and two LSB signals must be input in parallel, respectively. Therefore, in order to design a PRBS generator, four parallel PRBS sequence outputs operating at an 8 Gb/s are required. The digitally designed PRBS core circuit operates at 1 Gb/s, so clock dividers and 2:1 serializers are required to finally create an input pattern of 8 Gb/s, as shown in Fig. 3.8. And each PRBS core circuit outputs 8 bits in parallel. Seed values of each PRBS core circuit were set differently so that various transition patterns could be generated based on the PAM4 signal.

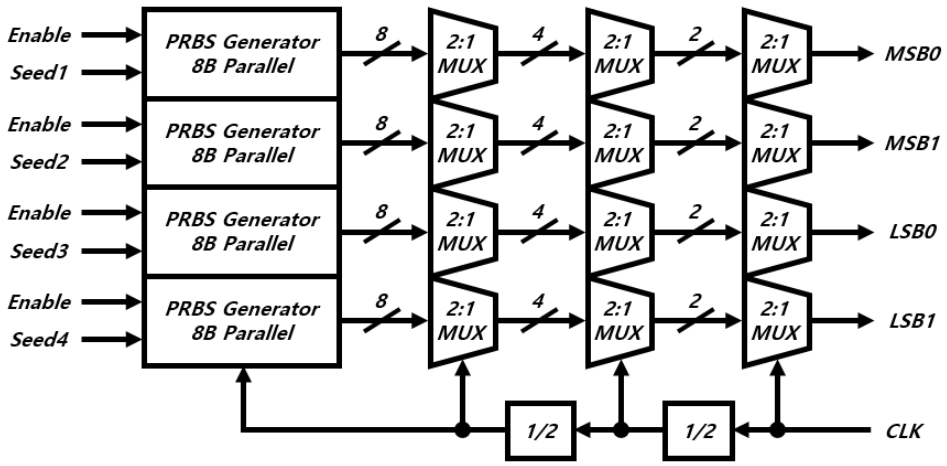


Fig. 3.8 Block diagram of PRBS generator.

The PRBS core circuit adopted the PRBS-7 sequence. The length of the PRBS sequence becomes 2^7-1, and the characteristic polynomial becomes $x^7+x^6=1$. In order to output 8 bits of signal in parallel from each PRBS core, it was designed using the 8-bit parallel transition matrix and the equation extracted therefrom in Fig. 3.9 [16],[17]. Finally, an 8-bit parallel signal with an operating speed of 1 Gb/s is output from each of the four PRBS cores with a

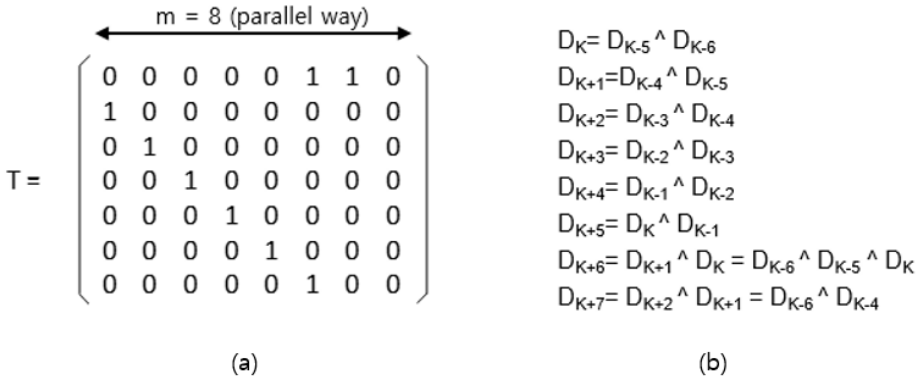


Fig. 3.9 (a) 8-bit parallel transition matrix. (b) Obtained equations from transition matrix.

length of 2^7-1. The output signal goes through three 2:1 MUXs and is converted into a serial signal with an operating speed of 8 Gb/s. In Fig. 3.10 simulation result, you can see the 8-bit parallel output of PRBS core and the final serial output through 2:1 MUXs.

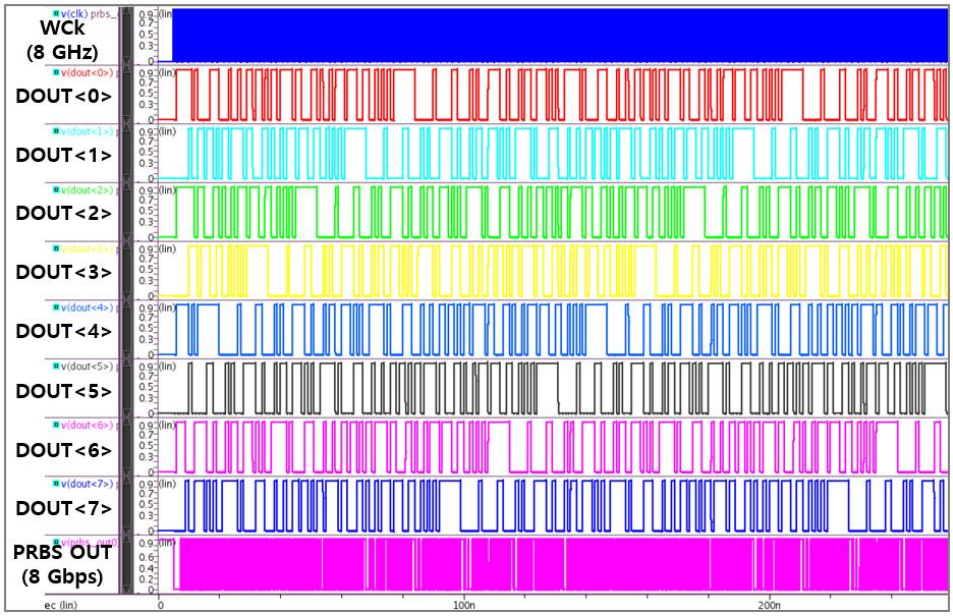


Fig. 3.10 Simulation result of 8-bit parallel PRBS generator.

Whether the transmitter receives the input signal from the external DQ pad or through the internal PRBS generator may be selected through the I2C signal control. It can also be used by mixing signals from external DQ pad and signals from PRBS generator.

3.3.3 Data Align/ Gray Code Encoder

The target of the PAM4 transmitter is a 32 Gb/s (16 Gsymbol/s) PAM4 signal output, whereas the frequency of the WCK input from the outside is 4 GHz. If so, two 8 Gb/s MSB/LSB signals must be received in parallel from the outside, and then the serializer converts the signals input in parallel into series. In order to convert the MSB/LSB signals input

in parallel in series, as shown in the timing diagram of Fig. 3.11, We need to align data so that each MSB/LSB signals with the same timing in parallel differ by 62.5 ps. The aligned MSB/LSB signals may operate at a half rate through the internal WCK 8 GHz.

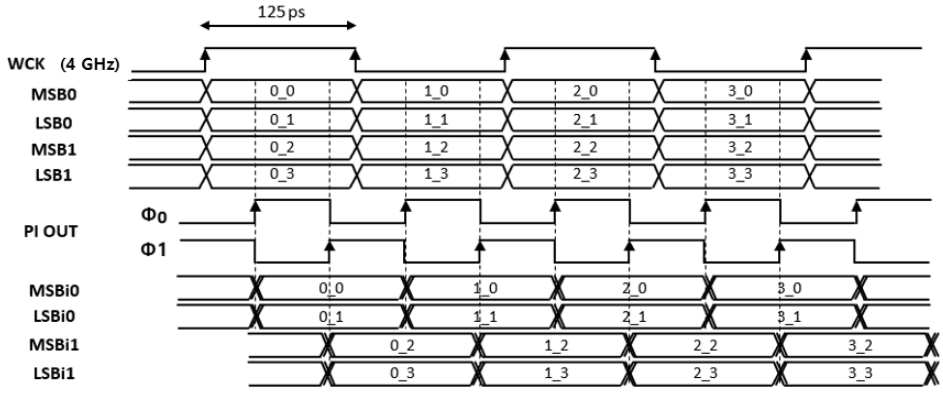


Fig. 3.11 Timing diagram after MSB/LSB data align.

And when converting from the NRZ signal to the PAM4 signal, the gray code is used. When gray coding is used, only one bit of MSB or LSB changes when the data level of PAM4 increases sequentially. In linear mapping, the data level increases sequentially to 00, 01, 10, and 11, and in gray mapping, it increases sequentially to 00, 01, 11, and 10.

The biggest advantage of using gray coding in the PAM4 method is that not only PAM4 mode but also NRZ mode can be used. As shown in the gray mapping of Fig. 3.12, with gray coding, an NRZ mode is possible up to 16 Gb/s using only MSB bits while LSB bits are fixed as 0s.

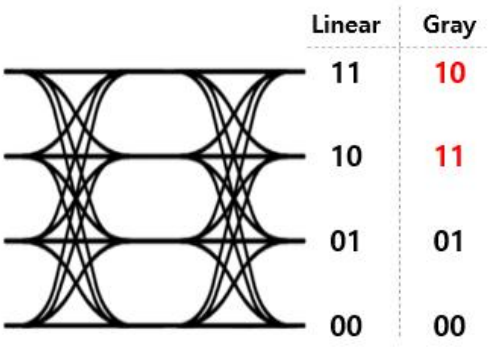


Fig. 3.12 PAM4 data level linear mapping vs. gray mapping.

Fig. 3.13(a) is a data alignment block, and Fig. 3.13(b) is a circuit for conversion to the gray code. MSB/LSB signals of the same timing were aligned to have a difference of 62.5 ps through a 2-phase clock with a phase difference of 180° by the D-flip flop/D-latch, and a circuit for gray coding was designed with 2x1 encoders.

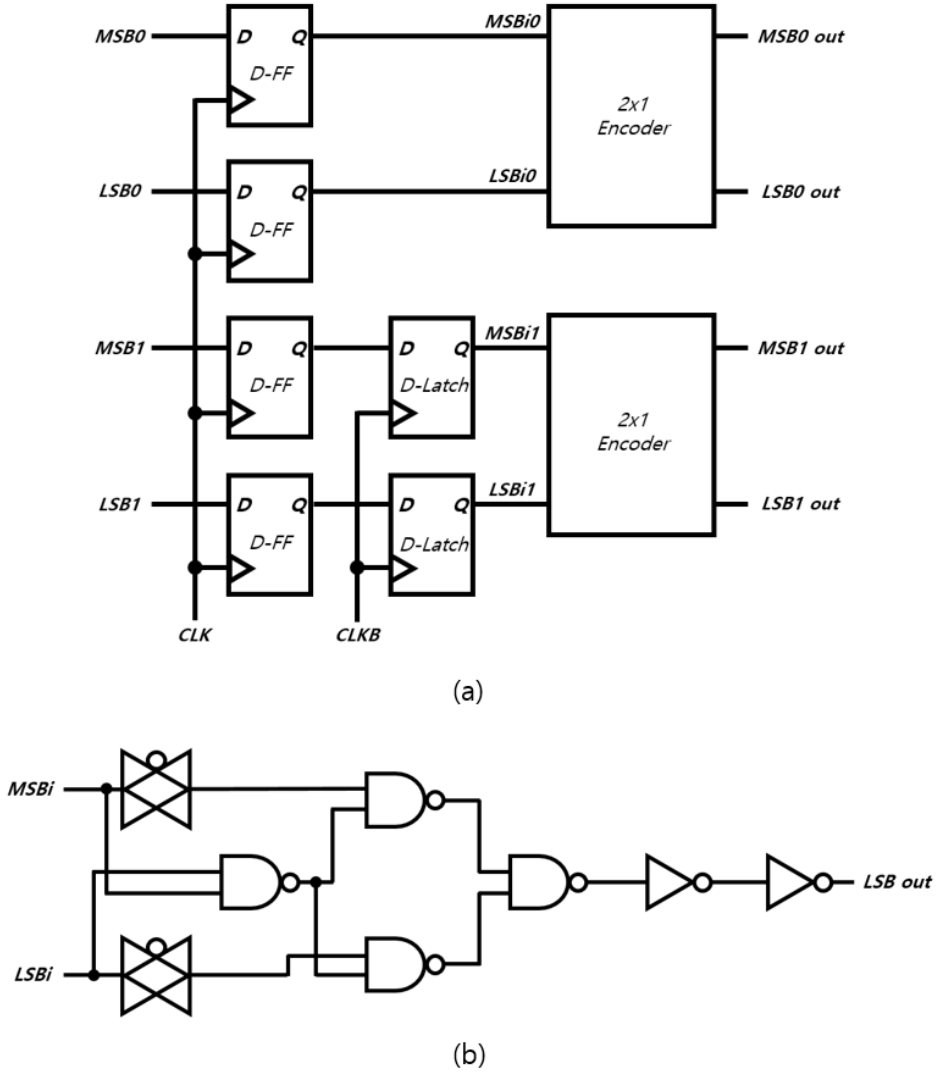


Fig. 3.13 (a) Data alignment block diagram and (b) 2x1 encoder for gray coding.

3.3.4 FFE Control/ Serializer

As shown in Fig. 3.14, when the single bit passes through the lossy channel, the amplitude is extended outside the 1-UI to the surroundings, creating a number of pre-cursors and post-cursors in addition to the main-cursor. An ideal single bit should have a fixed amplitude only in the 1-UI area, but unintentionally generated pre-cursors and post-cursors reduce bandwidth in high speed operations. Therefore, a FFE is required to solve this Inter-Symbol Interference (ISI) problem.

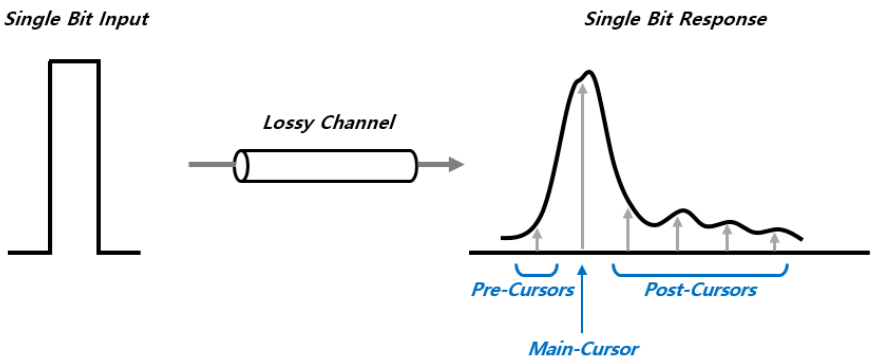


Fig. 3.14 Single bit response and pre/post cursors.

This paper used the pre-emphasis method, and Fig. 3.15 describes the principle of pre-emphasis. The number of taps depends on the number of pre-cursors and post-cursors to be compensated, including the main-cursor. In addition, a specific coefficient value can be designated for each tap to compensate as needed. However, it should be noted that since the total peak amplitude is determined, the main-cursor amplitude decreases as the tap number

increases or the compensation coefficient value increases, so all factors should be considered comprehensively in design.

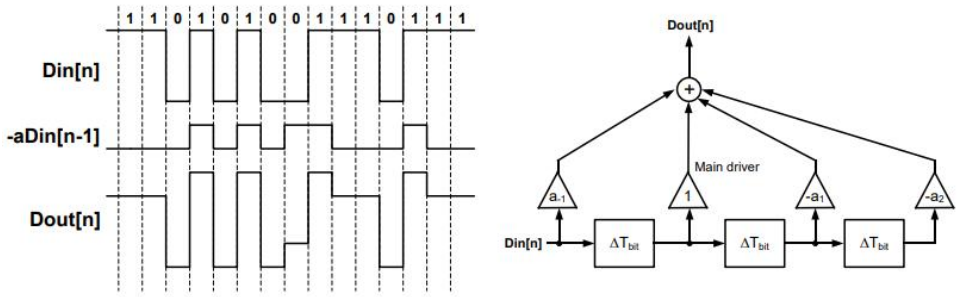


Fig. 3.15 Method of pre-emphasis equalization.

In this paper, a 2-tap FFE method that compensates for post-cursor was adopted. Except for the main-cursor tap, it is necessary to determine whether to compensate 1-tap as pre-cursor or post-cursor. As mentioned above, since the post-cursor has a greater effect, it is decided to compensate for the post-cursor with 1-tap.

First, the MSB/LSB signal of the previous data is inverted, delayed by 1-UI, and the signal aligned in parallel is converted into series through a serializer. As shown in Fig. 3.16, D-latch and 2x1 MUX were used for the circuit. In the timing diagram of Fig. 3.17, it can be confirmed that the previous data and the current data delayed by 1-UI are aligned with the same timing, and all MSB/LSB signals are converted from parallel to series. The main-cursor signal and post-cursor signal converted in series are transmitted to the final driver.

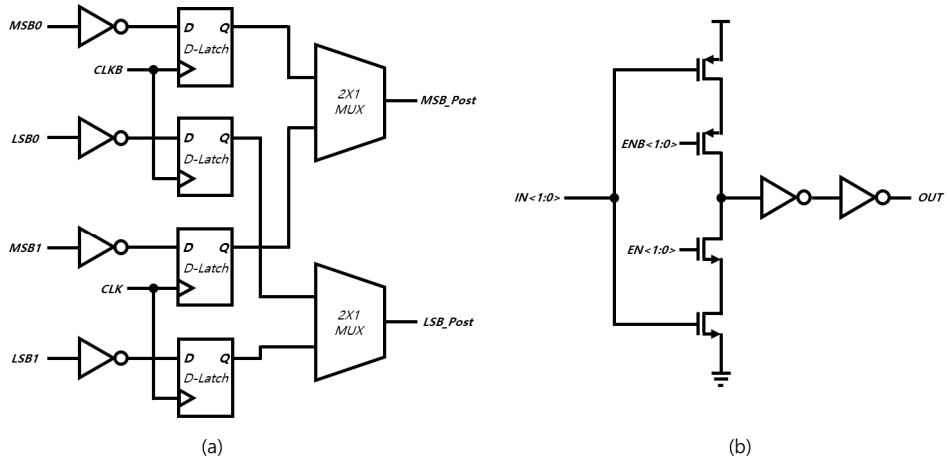


Fig. 3.16 (a) MSB/LSB generator for post-cursor tap and (b) 2x1 MUX.

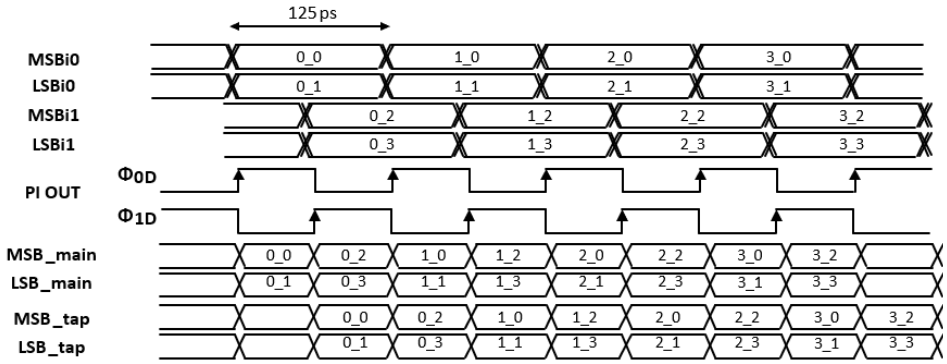


Fig. 3.17 Timing diagram of MSB/LSB for 2-tap FFE.

3.3.5 PAM4 Driver

PAM4 driver is composed of single-to-differential converter, pre-driver, and main driver as shown in Fig. 3.18. The four signals input to the driver, MSB_Main, LSB_Main, MSB_Post, and LSB_Post are single-ended types. Since the pre-driver is a differential pair type, a single-to-differential converter is needed to convert the single-ended signal to a differential type. The pre-driver uses VDD 0.9 V, and only one signal from the differential outputs is input to the main driver. The main driver uses VDDH 1.25V to make enough PAM4 output swing.

The single-to-differential converter is basically designed using inverters and a pass gate as

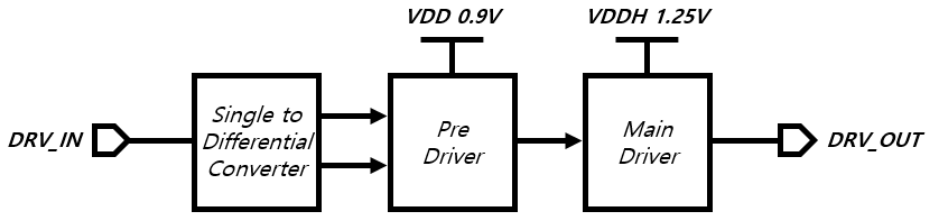


Fig. 3.18 Block diagram of driver.

shown in Fig. 3.19, and a cross coupled inverter is added to improve the duty cycle of the generated differential signal. Since the load of the MSB signal is twice that of the LSB signal, the strength of the inverter is also twice that of the LSB.

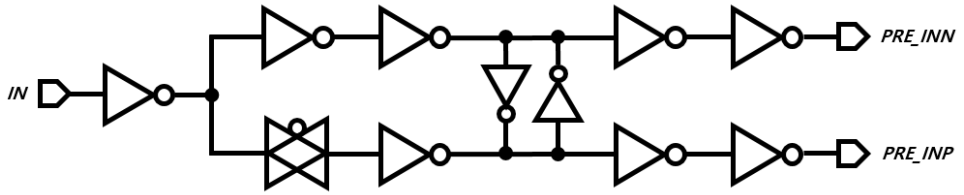


Fig. 3.19 Single-to-differential converter.

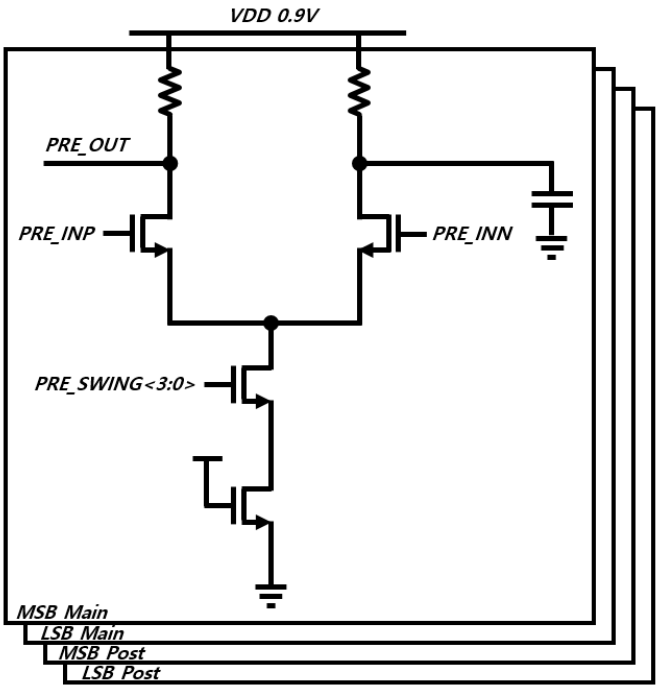
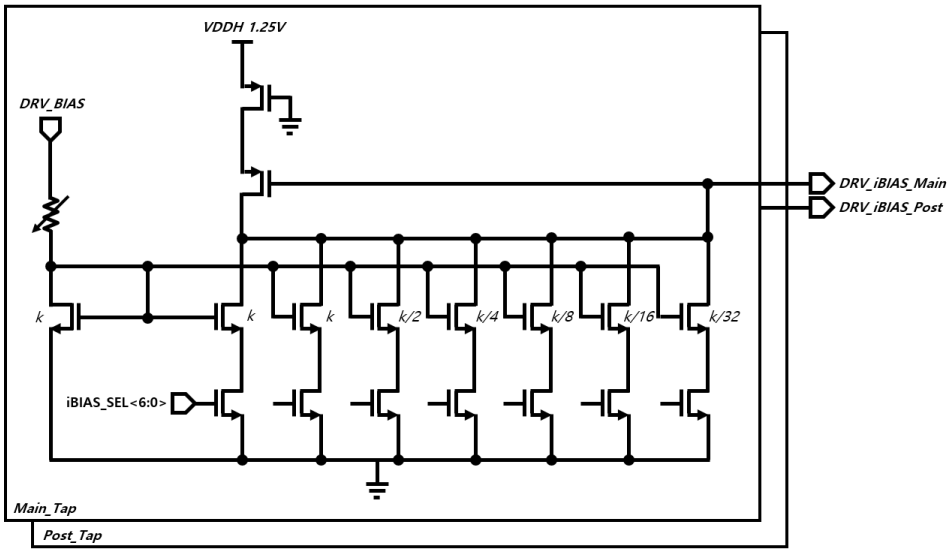


Fig. 3.20 Pre-drivers.

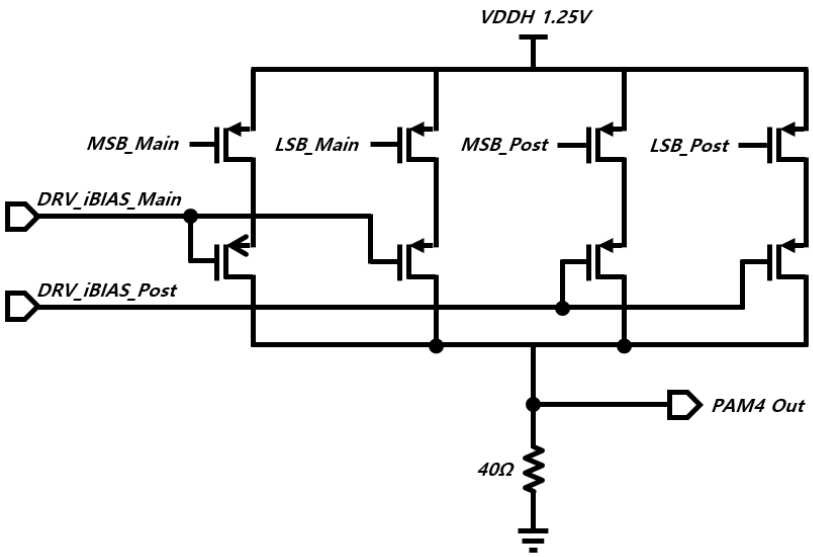
The pre-driver plays the role of making the 'low' level input to the PMOS of the main driver. The pre-drivers was designed as in Fig. 3.20. The output level can be determined by the resistance ratio of the passive resistor and the on-resistance of the NMOSs. And by adjusting

the value of on-resistance of the NMOSs through 4-bit thermometer code, the total resistance ratio can be adjusted. Like the single-to-differential converter, the driver strength of the MSB signal is designed to be twice that of the LSB signal. A capacitor is connected to the output terminal not used in the main driver to match the load to the output terminal connected to the main driver.

The main driver was designed as a current mode type that was disadvantageous in terms of power consumption but advantageous in terms of operating speed and impedance matching. The proposed main driver circuit is designed with PMOSs as shown in Fig. 3.21(b), because GDDR DRAM uses VSS termination. It consists of PMOSs that receive driver inputs, and resistors. The resistance value was designed as 40 Ω, which is slightly smaller than the commonly used 50 Ω to take advantage of high speed characteristics.



(a)



(b)

Fig. 3.21 (a) Current source circuit and (b) PAM4 main driver with 2-tap FFE.

The part of driver for the post-cursor tap is not designed in the multi-slice type that is generally used. If a multi-slice type FFE tap is used, the overall I/O characteristics may deteriorate due to the skew generated in each slice unit for adjusting the tap coefficient. In this paper, as shown in Fig. 3.21(a), the FFE coefficients of the main-cursor tap and the post-cursor tap were designed by controlling the amount of current of the current source with a 7-bit thermometer code through I2C. Fig. 3.22 shows the simulation result of the PAM4 data eye from the main driver for each FFE coefficient. As the coefficient of α_{+1} increases, it can be seen that the peak amplitude of the main-cursor decreases.

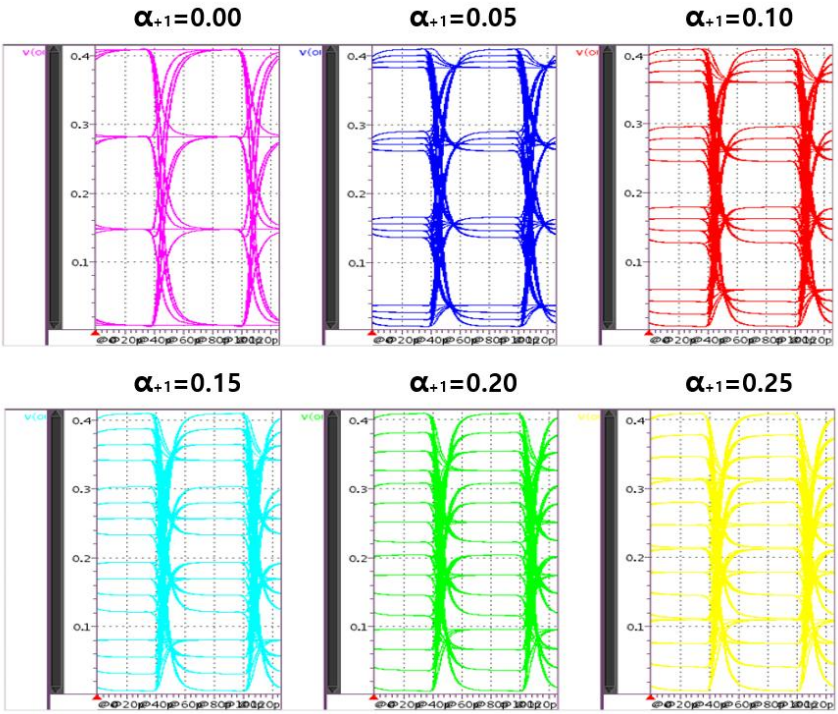


Fig. 3.22 Simulation results of PAM4 eye according to FFE coefficient values.

Chapter 4

Measurement Results

4.1 Chip Photomicrograph

Fig. 4.1 shows a micrograph of the PAM4-Binary bridge chip. The prototype chip is fabricated on the TSMC 40 nm GP CMOS process. In the case of I2C circuits, digital blocks written in verilog RTL codes were routed through synthesis, and other analog blocks except for I2C circuits were designed and routed manually. A dummy metal line and decoupling capacitor are placed in an empty space with no circuit around the block to reduce noise generated by the power supply. The total active area of the PAM4-Binary bridge transmitter block is 0.57 mm^2, and the area excluding the I2C block, WCK generator, ADPLL, PI and PRBS generator is 0.41 mm^2, occupying 71.9 % of the total transmitter block. Total transmitter power consumed is 102.1 mW.

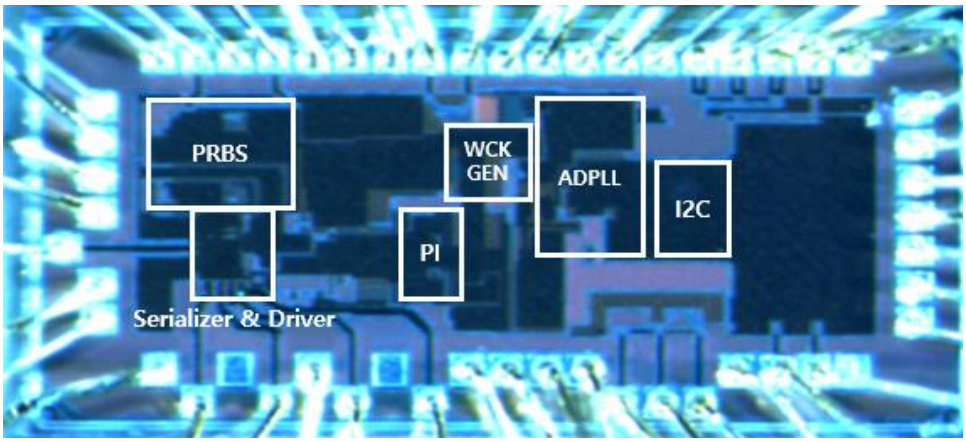


Fig. 4.1 Chip photomicrograph.

4.2 Measurement Setup

In order to measure the operation of PAM4 transmitter, as shown in Fig. 4.2, power supply, PC for I2C input to control test mode, differential clcok/NRZ data input from outside, and oscilloscope to measure output waveform are needed. The power regulation board receives 5V power and ground from the Agilent E3649A DC power supply, then generates and supplies the appropriate voltage to each power domain. Various test modes controlled by I2C block can be changed and measured through PC. In the PAM4 transmitter, you can control the drive strength of the pre-driver and the coefficient of FFE. PC and I2C block communicate through Aardvark, and the signal is written to I2C block using python tool. Anritsu MP1800A equipment provides differential clock and NRZ input data. The PAM4 transmitter of this paper requires 4-NRZ input data, but only 2-NRZ input data are provided by the device due to the

output port limit of Anritsu MP1800A device. Two additional NRZ input data required are provided through the PRBS generator inside the chip. PAM4 signal waveform output from PAM4 transmitter is measured by Tektronix MSO73304DX.

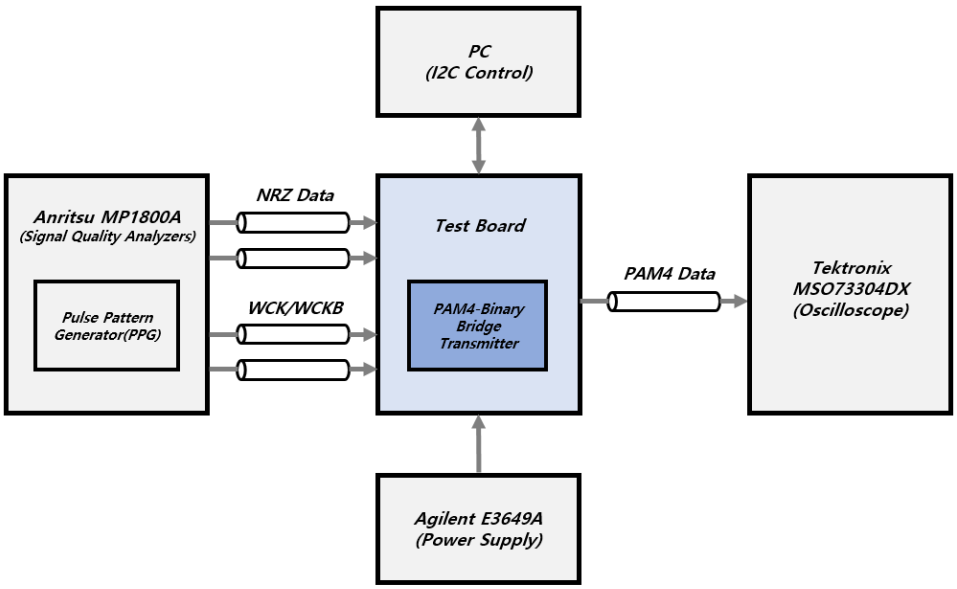


Fig. 4.2 Measurement setup.

4.3 Measurement Results

Fig. 4.3 shows the PAM4 data eye measured through the oscilloscope. When FFE is not applied, data eye opening cannot be obtained as shown in Fig. 4.3(a), but when FFE is applied, data eye opening can be obtained as shown in Fig. 4.3(b). It is presumed that this is because bandwidth attenuation occurs in the channel of the board and cable on which the chip is

mounted.

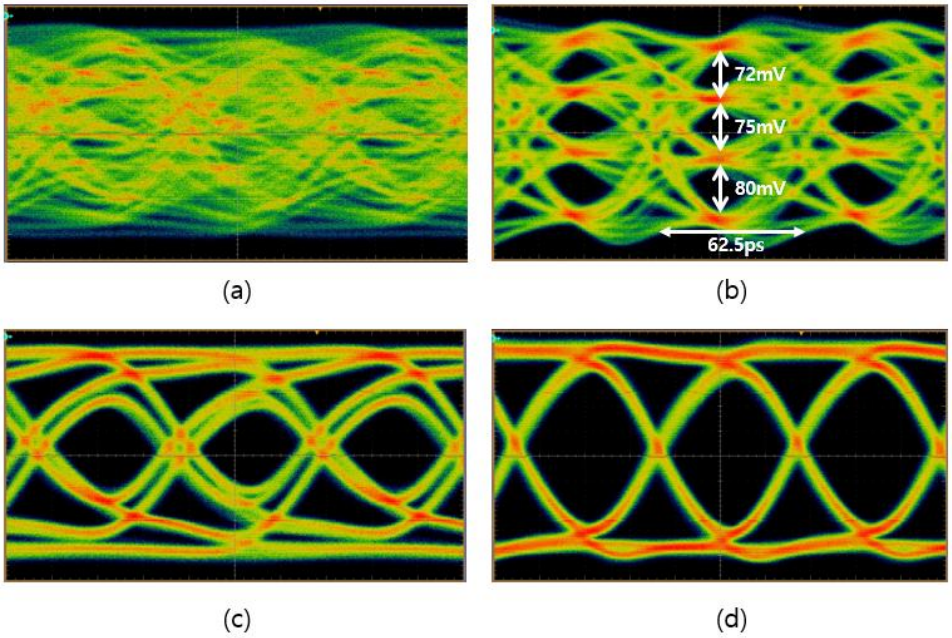


Fig. 4.3 Measured PAM4/NRZ transmitter data eye (a) PAM4 32 Gb/s without 2-tap FFE, (b) PAM4 32 Gb/s with 2-tap FFE, (c) NRZ 16 Gb/s without 2-tap FFE, and (d) NRZ 16 Gb/s with 2-tap FFE.

It was confirmed that the PAM4 transmitter operates at the speed of 32 Gb/s (16 Gsymbol/s) when 2-tap FFE is applied. The vertical opening size of each data eye is 70 mV or more, and the RLM value is 0.95. As mentioned earlier, gray coding is applied to the transmitter in this paper, so it can operate in PAM4/NRZ dual mode. Fig. 4.3 (c),(d) shows the NRZ data output when the LSB signal is fixed to ‘low’.

Fig. 4.4 shows the PAM4 data eye for each operating speed, and Table 4.1 shows the FoM for each operating speed. At the maximum operating speed of 32 Gb/s, FoM achieved 2.83

pJ/bit.

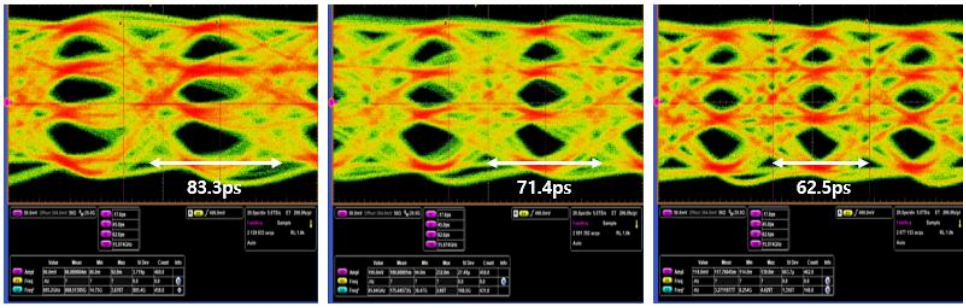


Fig. 4.4 Measured PAM4 data eye of (a) 24 Gb/s, (b) 28 Gb/s and (c) 32 Gb/s.

Table 4.1 Performance summary of Fig. 4.4.

Clock Frequency[GHz]	VDDH[V]	VDD[V]	Power[mW]	Data Rate[Gb/s]	FoM[pJ/bit]
6	1.25	0.9	65.7	24	3.17
7	1.25	0.9	70.2	28	2.95
8	1.25	0.9	90.4	32	2.83

4.4 Performance Summary

The total area of the proposed PAM4-Binary bridge transmitter is 0.57 mm^2, and the area of the ATE(Tester) to DRAM path excluding the I2C block, digital block, ADPLL, PI, and PRBS generator is 0.41 mm^2. When operating at PAM4 32 Gb/s speed, the entire transmitter

consumes a total of 102.1 mW of power and the ATE to DRAM path consumes 90.4 mW of power.

Table 4.2 and Fig. 4.5 show the power consumption of each block in the transmitter and their share of the total power consumption. Since the transmitter shares the supply voltage with the receiver and other analog blocks, the power breakdown was calculated based on the simulation results after layout. Except for the I2C block, 0.9 V supply power is used, and in the main driver, 1.25 V supply power is additionally used to secure output swing. It was confirmed that power consumption is high because the driver of the current mode type is used.

The 8 Gb/s NRZ data input from the tester is output as 32 Gb/s (16 Gsymbol/s) PAM4 data through the transmitter, and the RLM of the PAM4 data eye is 0.95.

Table 4.2 Power supply voltage and power breakdown of each block.

Block	Power Supply Voltage [V]	Power Breakdown [mW]
ATE to DRAM Path	0.9/ 1.25	90.39
ADPLL	0.9	8.43
Digital Block	0.9	2.53
PI	0.9	0.79

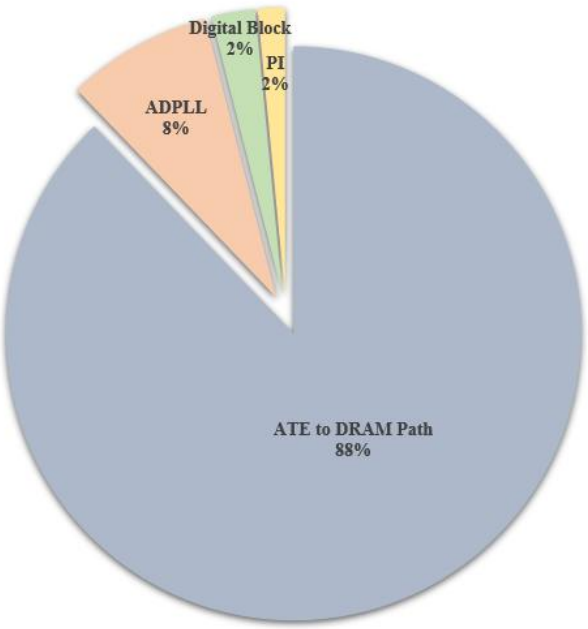


Fig. 4.5 Power breakdown.

Table 4.3 shows comparison with other PAM4 Tx chips using single-ended signaling. Unlike chips that use voltage mode PAM4 driver, this work uses current mode PAM4 driver and achieves 36 Gb/s operating speed and RLM 0.95.

Table 4.3 Comparison with other Tx chips.

	ISSCC' 21 [18]	ASSCC' 21 [19]	ISCAS' 19 [20]	JSSC' 21 [21]	This Work
Technology	1Ynm	28nm	65nm	65nm	40nm
Supply [V]	1.35	1.2/1.0	1.0	1.0/0.6	1.25/0.9
Data Rate [Gb/s/pin]	22	24	20	28	32
Signaling	Single-Ended	Single-Ended	Single-Ended	Single-Ended	Single-Ended
Tx Driver Topology	Voltage-Mode SST	Voltage-Mode	Voltage-Mode SST	Voltage-Mode	Current-Mode
Tx Equalization	Pulse-Based De-emphasis	-	2-Tap FFE	2-Tap Asymmetric FFE	2-Tap FFE
Signaling Type	PAM4/NRZ	PAM4/NRZ	PAM4/NRZ	PAM4	PAM4/NRZ
Clocking Type	No PLL	External	External	External	ADPLL
Tx Driver RLM	-	0.95 @24 Gb/s	0.98 @20 Gb/s	0.993 @28 Gb/s	0.95 @32 Gb/s
Energy Effeciency [pJ/bit]	-	-	3.07	0.64	2.83

Chapter 5

Conclusion

In this paper, we propose a PAM4 transmitter chip in PAM4-Binary bridge that can test PAM4 type DRAM with NRZ tester. The frequency of the external input clock is doubled through ADPLL, and two MSB signals and two LSB signals input in parallel are aligned through the doubled clock. To compensate for channel loss, a 2-tap FFE scheme was applied, and the driver was designed as a current mode with an emphasis on operating speed. The final PAM4 data is output as single-ended signal according to DRAM signaling.

The total area of the proposed PAM4-Binary bridge transmitter is 0.57 mm^2, and the area of the ATE to DRAM path excluding the I2C block, WCK generator, ADPLL, PI, and PRBS generator is 0.41 mm^2. The PAM4 transmitter consumes a total of 102.1 mW of power when operating at 32 Gb/s, and the ATE to DRAM path consumes 90.4 mW of power. The NRZ data of 8 Gb/s input from the tester is output as PAM4 data of 32 Gb/s (16 Gsymbol/s) through the transmitter. The maximum operating speed of output PAM4 data is 32 Gb/s, and FoM achieves 2.83 pJ/bit..

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초 록

고성능 컴퓨팅 시스템, 대용량의 데이터 센터, AI 기술의 발전으로 인해 유선 통신의 대역폭 요구 수준은 기하급수적으로 증가하고 있다. 그러나 I/O 회로의 핀당 대역폭의 향상은 통신 채널의 다양한 한계로 인해 어려움을 겪고 있다. 이는 차세대 DRAM 분야에서도 예외는 아니다. 핀당 데이터 전송 속도를 증가시키는 연구 방향에서는 어느 정도 한계에 봉착하면서 최근에는 High Bandwidth Memory (HBM)와 같이 핀의 개수를 급격히 늘려서 대역폭을 증가시키는 기술도 발전하고 있다.

다른 접근 방식 중 한가지가 다중 레벨 신호 방식이다. 기존의 Non-Return-to-Zero (NRZ) 신호 대신에 다중 레벨 신호 방식을 이용하면 동일한 Nyquist 주파수에서 데이터 속도를 높일 수 있고 이는 DRAM 의 차세대 고대역폭 I/O 인터페이스에 좋은 솔루션이 될 수 있으며 현재까지는 4 레벨 펄스 진폭 변조 방식 (PAM-4)이 널리 채택되어 있다.

하지만 현재 PAM-4 방식 DRAM 이 양산 단계가 아니기 때문에 PAM-4 전용 Memory Tester 가 없는 상황이다. 본 논문에서는 차세대 메모리 테스트를 위한 32 Gb/s PAM4 바이너리 브리지에서의 트랜스미터를 제안한다. NRZ 테스터에서 브리지로 전송된 저속 데이터는 고속 PAM4 데이터로 변환되어 메모리로 전달된다. 접지 종단 PAM4 드라이버는 2-탭 피드포워드 이퀄라이저로 출력 전류를 제어하여 0.95 의 레벨 불일치 비율 (RLM)을 달성함으로써 단일 종단 출력을 제공한다. 40 nm CMOS 기술로 제작된 브리지 트랜스미터는 0.57 mm^2 의 활성 영역을 차지하고 102.1 mW 의 전력을 소모한다.

주요어 : 4 단계 펄스 진폭 변조, 4 단계 펄스 진폭 변조-2 진법 브리지, DRAM 검사 장비.

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