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Ph.D. DISSERTATION

Gas Sensor Platform Based on Si CMOS Technology

실리콘 CMOS 공정 기술 기반 가스 센서 플랫폼

by

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August 2022

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING COLLEGE OF ENGINEERING SEOUL NATIONAL UNIVERSITY

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Gas Sensor Platform Based on Si CMOS Technology

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ABSTRACT

Nowadays, indoor and outdoor air pollution due to harmful gases emitted from various industrial fields and means of transportation has been emerged with the progress of industrialization and urbanization. To monitor the atmospheric condition in real time, the development of gas sensing technology is essential, and this technology can be widely utilized in various fields such as disease diagnosis and food freshness check. Therefore, numerous research groups have conducted research and development (R&D) on various types of gas sensors such as optical, electrochemical, and semiconductor-type. Among them, resistive gas sensors, which is a type of semiconductor-type gas sensors, have been reported the most research results thanks to the advantages of simple device structure and manufacturing process. However, the area of the sensors should be increased to obtain the output current required for their operation. On the other hand, field-effect transistor (FET)-based gas sensors are compatible with complementary metaloxide-semiconductor (CMOS) process technology, so they can be manufactured in a miniaturized size. Thus, CMOS integrated circuits (IC) such as multiplexers (MUX), analog-to-digital converters (ADC), and gain control amplifier (PGA), and flash memories capable of the read, write, and erase operations can be integrated onto a single substrate using the same manufacturing process.

In this dissertation, a gas sensor platform using the conventional silicon (Si) CMOS process technology is proposed. The proposed gas sensor platform can be manufactured with only 10 photomasks, and has a structure in which FET-type gas sensors having a horizontal floating-gate structure (HFGFET-type), thin-film transistor (TFT)-type gas sensors having a bottom gate, and resistive gas sensors are integrated together with polysilicon (poly-Si) gate FETs and flash memories. A micro-heater is formed at the bottom of the sensing layer of the HFGFET-type gas sensor to locally heat the sensing layer to the optimal operating temperature corresponding to target gas. Since the structure of the HFGFET-type gas sensor includes that of the floating-gate MOSFET, the flash memory operation is possible, and thus it can be utilized for calibration of a sensor output signal by changing an operating point. Meanwhile, the gas sensing characteristics of the TFT-type and resistive gas sensors, integrated onto the same substrate, were investigated, and the operability of each sensor was verified. Furthermore, a design optimization guideline of FET-type gas sensors including the HFGFET-type gas sensor is proposed considering of gas sensitivity, noise characteristics, power consumption, and so forth. The electrical characteristics depending on the structure, such as the size and shape of the sensing layer and transducer, were modeled using actual measurements and technology computer-aided design (TCAD) device simulation, and the optimization indicator was designed using the established model. Utilizing the optimized HFGFET-type gas sensor, gas and humidity sensing characteristics

were investigated using harmful gases such as nitrogen dioxide (NO₂) and hydrogen

sulfide (H₂S), and the sensing mechanism of the sensor was explained.

The proposed gas sensor platform is expected to be mass-produced at a low

cost because it is possible to integrate various types of gas sensors and CMOS

devices/circuits onto a substrate using the same manufacturing process. In addition,

the proposed design optimization guideline of FET-type gas sensors is expected to

be very effective and useful in improving their gas sensing characteristics and

designing a gas sensor array in the future.

Keywords: FET-type gas sensor, HFGFET-type gas sensor, gas sensor platform,

CMOS, design optimization, antenna effect

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iii

CONTENTS

Abstract	i
Contents	iv
List of Figures	viii
List of Tables	xxiii
Chapter 1	
Introduction	1
1.1 Study background	1
1.1.1 Gas sensing technology	1
1.1.2 FET-type gas sensors	6
1.2 Purpose of research	13
1.3 Dissertation outline	16

Chapter 2

Platform structure and fabrication1	8
2.1 Platform structure	18
2.2 Platform fabrication2	22
2.2.1 Fabrication process2	22
2.2.2 Simulation study for channel implantation	30
2.2.3 Formation of sensing layer	4 1
Chapter 3	
Fundamental FET characteristics4	1 5
3.1 <i>I-V</i> characteristics of poly-Si gate FET	15
3.2 Flash memory functionality	53
3.3 CMOS inverter characteristics	57
3.4 Application to HFGFET-type gas sensor	55

Chapter 4

Semiconductor-based gas sensors	69
4.1 TFT-type gas sensors	69
4.2 Resistive gas sensors	75
Chapter 5	
Horizontal floating-gate FET-type gas sensors	79
5.1 Electrical characteristics	79
5.2 Thermal characteristics of micro-heaters	90
5.3 Gas sensing characteristics	94
5.4 Design optimization	16
5.4.1 Sensing material area1	16
5.4.2 FET channel	25
5.4.3 Comprehensive optimization13	32
5.5 Examples of gas sensing	41

Chapter 6	
Conclusions	149
Appendix A	
Breakdown characteristics of FETs	152
A.1 Dielectric breakdown	152
A.2 Junction breakdown	154
Bibliography	158
Abstract in Korean	167
List of Publications	169

List of Figures

Figure 1.1. Schematic drawing of an optical gas sensing measurement [17]2
Figure 1.2. Schematic diagram of an electrochemical NO sensor [19]
Figure 1.3. Schematic diagram of a resistive gas sensor [22]5
Figure 1.4. Schematic diagram of an organic TFT-type gas sensor [34]7
Figure 1.5. Schematic diagram of a palladium (Pd)-gate FET-type gas sensor
[43]
Figure 1.6. Schematic diagram of a SGFET-type gas sensor [40]
Figure 1.7. Schematic diagram of a CCFET-type gas sensor [40]10
Figure 1.8. (a) Top scanning electron microscopy (SEM) image and (b) schematic
diagram of an HFGFET-type gas sensor [44]12

Figure 2.1. Schematic bird's eye view of the proposed gas sensor platform21
Figure 2.2. (a) Schematic diagram of the three different gas sensors in the proposed
gas sensor platform. (b) Top SEM images of the fabricated HFGFET-type gas sensor
(c) resistive gas sensor, and (d) TFT-type gas sensor
Figure 2.3. Key process flow of the Si CMOS gas sensor platform. Here, (a)-(f)
correspond to Fig. 2.4(a)-(f)
Figure 2.4. (a)-(f) Schematic diagram of the key fabrication process of the Si CMOS
gas sensor platform
Figure 2.5. SEM images of the field oxide formed by the LOCOS technique29
Figure 2.6. Simulated I_D - V_{GS} curves as a parameter of the channel implantation
energy in the <i>n</i> -channel FETs
Figure 2.7. Simulated I_D - V_{GS} curves as a parameter of the channel implantation dose
in the mahannel FETs

Figure 2.8. Simulated I_D - V_{GS} curves as a parameter of the channel implantation
energy in the <i>p</i> -channel FETs35
Figure 2.9. Simulated I_D - V_{GS} curves as a parameter of the channel implantation dose
in the <i>p</i> -channel FETs36
Figure 2.10. Simulated I_D - V_{GS} curves of the short and long, n - and p -channel FETs
without the sidewall spacers at a $ V_{\rm DS} $ of 0.1 V and 1.0 V40
Figure 2.11. Simulated I_D - V_{GS} curves of the short and long, n - and p -channel FETs
with the sidewall spacers at a $ V_{\rm DS} $ of 0.1 V and 1.0 V40
Figure 2.12. Top SEM image of a part of the sensing layer (In ₂ O ₃ film) in the
platform
Figure 2.13. EDS spectrum of the In ₂ O ₃ /SiO ₂ /Si sample after PDA44
Figure 2.14. XRD spectrum of the In ₂ O ₃ /SiO ₂ /Si sample after PDA44
Figure 3.1. Schematic diagram of the fabricated poly-Si gate <i>n</i> -channel FET47

Figure 3.2. I_D - V_{GS} characteristics of the fabricated n -channel FETs as a parameter
of the channel length and $V_{\rm DS}$ at room temperature
Figure 3.3. I_D - V_{DS} characteristics of the fabricated n -channel FETs as a parameter
of the $V_{\rm GS}$ at room temperature
Figure 3.4. Schematic diagram of the fabricated poly-Si gate <i>p</i> -channel FET50
Figure 3.5. I_D - V_{GS} characteristics of the fabricated p -channel FETs (a) with and (b)
without the sidewall spacers as a parameter of the channel length and V_{DS} at room
temperature
Figure 3.6. I_D - V_{DS} characteristics of the fabricated n -channel FETs (a) with and (b)
without the sidewall spacers as a parameter of the $V_{\rm GS}$ at room temperature52
Figure 3.7. Schematic diagram of the fabricated flash memory
Figure 3.8. P/E characteristics of the fabricated n - and p -channel flash memories
under the different V_{DGM} and V_{ERS} at room temperature.

Figure 3.9. Retention characteristics of the fabricated n - and p -channel flash
memories at room temperature
Figure 3.10. Schematic diagram of the fabricated CMOS inverter58
Figure 3.11. (a) VTCs (V_{out} versus V_{in}) of the fabricated CMOS inverter as a
parameter of the $V_{\rm DD}$ at room temperature. (b) TW and normalized TNM extracted
from the VTCs in (a)62
Figure 3.12. (a) VTCs of the fabricated CMOS inverter utilizing the HFGFET-type
gas sensors as a parameter of the $V_{\rm DD}$ at room temperature. (b) TW and normalized
TNM extracted from the VTCs in (a)63
Figure 3.13. (a) Schematic diagram of the fabricated CMOS buffer. (b) VTCs of the
fabricated CMOS buffer as a parameter of the $V_{\rm DD}$ at room temperature64
Figure 3.14. (a) I_D - V_{CG} curves of the fabricated n - and (b) p -channel HFGFET-type
gas sensors before and after the 500 ppb NO_2 injection at 160 °C for 10 min67
Figure 3.15. (a) Transient gas responses of the fabricated <i>n</i> - and (b) <i>p</i> -channel

HFGFET-type gas sensors to NO ₂ (100 ppb, 200 ppb, 500 ppb) at 160 °C68
Figure 4.1. Schematic structure of the fabricated TFT-type gas sensor71
Figure 4.2. I_D - V_{GS} curves of the fabricated TFT-type gas sensor under the various
$T_{\rm S}$ (= 60 °C, 90 °C, 120 °C, and 150 °C) at a $V_{\rm DS}$ of 1 V71
Figure 4.3. I_D - V_{GS} curves of the fabricated TFT-type gas sensor before and after the
(a) NO ₂ and (b) H ₂ S gas reaction under the various T s at a V _{DS} of 1 V72
Figure 4.4. Transient (a) NO ₂ and (b) H ₂ S responses of the fabricated TFT-type gas
sensor under the various gas concentration at 150 °C
Figure 4.5. Schematic diagram for explaining the NO ₂ and H ₂ S sensing mechanisms
of the TFT-type gas sensor
Figure 4.6. Schematic structure of the fabricated resistive gas sensor
Figure 4.7. I_R - V_R characteristics of the fabricated resistive gas sensor under the
various Ts (= 60 °C, 90 °C, 120 °C, and 150 °C)

Figure 4.8. I_R - V_R characteristics of the fabricated resistive gas sensor before and
after the (a) NO ₂ and (b) H ₂ S gas reaction under the various <i>Ts.</i>
Figure 4.9. Transient (a) NO ₂ and (b) H ₂ S responses of the fabricated resistive gas
sensor under the various gas concentration at 150 °C
Figure 5.1. Structure overview of the fabricated HFGFET-type gas sensor. This
shows the bird eye's view and top schematic view of the sensor [55]80
Figure 5.2. I_D - V_{CG} characteristics of the fabricated HFGFET-type gas sensors as a
parameter of the $N_{\rm f}$ using the DC and PIV measurements at 20 °C [55]82
Figure 5.3. $I_{\rm H}$ - $V_{\rm H}$ characteristics of the embedded micro-heaters as a parameter of
the $N_{\rm f}$ using the DC and PIV measurements at 20 °C [55]83
Figure 5.4. Simplified equivalent circuit of the fabricated HFGFET-type gas sensor
[55]
Figure 5.5. 3D structures of the HFGFET-type gas sensor created by mimicking the
device structure in the TCAD simulation tool

Figure 5.6. Simulated and measured $I_{\rm D}$ - $V_{\rm CG}$ curves of the HFGFET-type gas sensors
with four different $N_{\rm f}$ s at 20 °C.
Figure 5.7. (a) $V_{\rm FG}$ versus $V_{\rm CG}$ as a parameter of the $N_{\rm f}$ in the p -channel HFGFET-
type gas sensors. (b) γ of the sensors as a function of the $V_{\rm CG}$ extracted from (a)
[55]
Figure 5.8. Operating scheme of the fabricated embedded micro-heater92
Figure 5.9. $\Delta R_{\rm H}$ -T characteristics as a parameter of the $N_{\rm f}$ of the fabricated
HFGFET-type gas sensors
Figure 5.10. (a) Transient T as a function of the $V_{\rm H}$ at a f of 1 kHz with 50% duty
cycle. (b) T -power as a parameter of the $N_{ m f}$ of the fabricated gas sensors
[55]93
Figure 5.11. (a) ΔT versus energy consumption for an initial 5 μ s of the heating
period. (b) C of the fabricated embedded micro-heaters with different N_{f} s at 20 °C
[55]

Figure 5.12. (a) ΔV_{th} and (b) Max(ΔI_{D}) versus T as a parameter of the N_{f} of the fabricated HFGFET-type gas sensors when 500 ppb NO₂ is injected for 10 min. ...98 Figure 5.13. (a) ΔV_{th} and (b) Max(ΔI_{D}) versus T as a parameter of the N_{f} of the fabricated HFGFET-type gas sensors when 50 ppm H₂S is injected for 10 min.99 Figure 5.14. Energy band diagram of the fabricated HFGFET-type gas sensor when the atmosphere ambience is air and NO₂. $\Delta \rho$ is additionally introduced below. ...100 Figure 5.15. I_D - V_{CG} curves of the fabricated HFGFET-type gas sensors before and Figure 5.16. Simplified equivalent circuit of the fabricated HFGFET-type gas Figure 5.17. (a) Simulated I_D - V_{CG} curves of the HFGFET-type gas sensor with an $N_{\rm f}$ of 3 and an $L_{\rm f}$ of 2.5 μ m as a function of the $\rho_{\rm sheet}$ at 20 °C. (b) $\Delta V_{\rm th}$ versus $\rho_{\rm sheet}$ as a function of N_f [55].

Figure 5.18. Simulated and measured $\Delta V_{\rm th}$ versus $N_{\rm f}$. The sensors reacted to 500

ppb NO ₂ for 10 min at 160 °C, and in the simulation, the $\rho_{\rm sheet}$ was set to -1.95 ×
10 ¹² cm ⁻² [55]
Figure 5.19. (a) I_D - V_{CG} curves of the fabricated HFGFET-type gas sensors with an
$N_{\rm f}$ of 4 and an $L_{\rm f}$ of 2.5 μ m before and after the NO ₂ gas reaction at a $V_{\rm DS}$ of -0.1
V (in the linear region). (b) max(ΔI_D) versus ΔV_{th} of the sensors [55]107
Figure 5.20. (a) I_D - V_{CG} curves of the fabricated HFGFET-type gas sensors with an
$N_{\rm f}$ of 4 and an $L_{\rm f}$ of 2.5 μ m before and after the NO ₂ gas reaction at a $V_{\rm DS}$ of $-1~{ m V}$
(in the saturation region). (b) max(ΔI_D) versus ΔV_{th} of the sensors
Figure 5.21. (a) $\log(I_{\rm D})$ - $V_{\rm CG}$ curves of the fabricated HFGFET-type gas sensors with
an $N_{\rm f}$ of 4 and an $L_{\rm f}$ of 2.5 $\mu{\rm m}$ before and after the NO ₂ gas reaction (in the
subthreshold region). (b) $\max(R)$ versus ΔV_{th} of the sensors
Figure 5.22. (a) max(ΔI_D) versus NO ₂ gas concentration as a parameter of the N_f of
the HFGFET-type gas sensors. (b) max(ΔI_D)/gas concentration of the sensors111
Figure 5.23. (a) $max(R)$ versus NO_2 gas concentration as a parameter of the N_f of

the HFGFET-type gas sensors. (b) $\log(\max(R))/\log(\text{gas concentration})$ of the
sensors
Figure 5.24. (a) γ , (b) ΔV_{th} , (c) g_{m} , (d) $\max(\Delta I_{\text{D}})$, (e) SS, and (f) $\max(R)$ of the
HFGFET-type gas sensors with different combinations of the W and L at a V_{DS} of
-0.1 V. The max(R) is obtained in the subthreshold region
Figure 5.25. (a) ΔV_{th} , (b) g_{m} , and (c) $\max(\Delta I_{\text{D}})$ of the HFGFET-type gas sensors
with different combinations of the W and L at a V_{DS} of -1 V
Figure 5.26. (a) γ , (b) ΔV_{th} , (c) g_{m} , (d) SS , (e) ΔI_{D} , and (f) $\max(R)$ of the HFGFET-
type gas sensors with the different $N_{\rm f}$ s (1, 2, 3, and 4) and $L_{\rm f}$ s (2.5, 5.5, and 12 μ m)
[55]
Figure 5.27. (a) $g_{\rm m}$ versus $N_{\rm f}$ as a parameter of the $L_{\rm f}$ in the saturation region of the
HFGFET-type gas sensors. (b) $\Delta I_{ m D}$ versus $L_{ m f}$ as a parameter of the $N_{ m f}$ in the
saturation region of the sensors. (c) $\Delta I_{\rm D}$ /power versus $L_{\rm f}$ as a parameter of the $N_{\rm f}$ in
the saturation region of the sensors.

Figure 5.28. (a) Power, (b) ΔI_D /power, (c) ΔV_{th} /power, and (d) max(R)/power of the
HFGFET-type gas sensors with the different $N_{\rm f}$ s and $L_{\rm f}$ s
Figure 5.29. $\Delta I_{\rm D}$ of the fabricated HFGFET-type gas sensors having the different
N _f s with five different NO ₂ gas concentration (100-500 ppb) at 160 °C122
Figure 5.30. (a) Transient I_D of the fabricated HFGFET-type gas sensor having the
different $N_{\rm fS}$ with 100 ppb and 500 ppb NO ₂ at 160 °C. (b) Energy consumption and
t _{gd} versus NO ₂ gas concentration at 160 °C
Figure 5.31. $t_{\rm gd}$, energy consumption, and power consumption of the fabricated
HFGFET-type gas sensors having the different $N_{\rm f}$ s at 160 °C
Figure 5.32. (a) γ versus WL of the fabricated HFGFET-type gas sensors. (b) $\Delta V_{\rm tl}$
versus WL of the sensors
Figure 5.33. $\Delta I_{\rm D}$ /power versus W as a parameter of the L of the fabricated HFGFET
type gas sensors

Figure 5.34. (a) $S_{\rm ID}/I_{\rm D}^2$ of the fabricated HFGFET-type gas sensors with a W of 1.0

μ m as a parameter of the L . (b) $S_{\rm ID}/I_{\rm D}{}^2$ of the sensors sampled at a 10 Hz versus $1/L$
as a parameter of the W
Figure 5.35. (a) ΔI_D , (b) δI_D , (c) SNR, (d) max(R), and (e) max(R) × SNR of the
fabricated HFGFET-type gas sensors with the different FET channel designs
[55]
Figure 5.36. ΔI_D /power of the HFGFET-type gas sensors with the different channel
sizes as a function of the $N_{\rm f}$ at (a) $L_{\rm f}$ = 2.5 μ m, (b) $L_{\rm f}$ = 5.5 μ m, and (c) $L_{\rm f}$ = 12 μ m
while maintaining the $W/L = 1$
Figure 5.37. (a) Power consumption versus $L_{\rm f}$ of the HFGFET-type gas sensors. (b)
$\Delta V_{\rm th}$ versus $L_{\rm f}$ of the sensors. (c) $\Delta V_{\rm th}$ versus WL of the sensors
Figure 5.38. $\sqrt{WL}\Delta V_{\rm th}/{\rm power}$ of the HFGFET-type gas sensors with an $N_{\rm f}$ of 1
versus WL as a parameter of the L_f [55]
Figure 5.39. (a) Transient CO (250-2000 ppm) responses of the fabricated pristine
In ₂ O ₃ and Pt-decorated In ₂ O ₃ sensors at 200 °C. (b) Transient CO (500 ppm)

responses of the sensors as a parameter of the Pt concentration (wt%) at 200 °C
[49]
Figure 5.40. Transient O ₂ (30%) responses of the fabricated sensor at 25 °C, 140 °C,
and 200 °C [48]
Figure 5.41. Energy band diagram of the fabricated sensor before (black) and after
(red) the O ₂ injection
Figure 5.42. Transient O ₂ (30%) responses of the fabricated sensor as a parameter
of the V_{pre} at (a) 25 °C and (b) 200 °C [48]
Figure 5.43. (a) I_D - V_{CG} curves of the fabricated humidity sensor as a parameter of
the RH at 25 °C. (b) Transient humidity responses of the sensor as a parameter of
the RH at 25 °C [50]147
Figure 5.44. Schematic diagram of the humidity sensing mechanism and adsorption
model of the fabricated sensor [50]
Figure A.1. Measured gate oxide breakdown characteristics of the fabricated <i>n</i> - and

<i>p</i> -channel poly-Si gate FETs at room temperature
Figure A.2. Measured source/drain-to-body junction breakdown characteristics of
the fabricated <i>n</i> - and <i>p</i> -channel poly-Si gate FETs at room temperature156
Figure A.3. Measured drain-to-source (channel) breakdown characteristics of the
fabricated <i>n</i> - and <i>p</i> -channel poly-Si gate FETs at room temperature156
Figure A.4. Measured well-to-substrate junction breakdown characteristics of the
fabricated <i>n</i> - and <i>p</i> -channel poly-Si gate FETs (4 samples) at room
temperature 157

List of Tables

Table 2.1. Several device parameters extracted from the simulated I_D - $V_{\rm GS}$ curves as
a parameter of the channel implantation energy in the <i>n</i> -channel FETs. Here, SS
represents subthreshold swing of each device
Table 2.2. Several device parameters extracted from the simulated I_D - V_{GS} curves as
a parameter of the channel implantation dose in the <i>n</i> -channel FETs33
Table 2.3. Several device parameters extracted from the simulated I_D - V_{GS} curves as
a parameter of the channel implantation energy in the <i>p</i> -channel FETs36
Table 2.4. Several device parameters extracted from the simulated I_D - V_{GS} curves as
a parameter of the channel implantation dose in the <i>p</i> -channel FETs37
Table 5.1. Comparison of the ΔI_D /power of the HFGFET-type gas sensors with the
different W, L, L_f , and N_f .

Table 5.2. Comparison of the $(\Delta V_{\rm th} \sqrt{WL})$ /power of the sensor	ors with the different W
$L, L_{\mathrm{f}},$ and N_{f}	140

Chapter 1

Introduction

1.1 Study background

1.1.1 Gas sensor technology

Recently, due to rapid industrialization and urbanization, indoor and outdoor air pollution caused by harmful gases emitted from various industrial fields and means of transportation has been increased worldwide [1-4]. To monitor and resolve the problem, the development of a gas sensing technology is essential. Moreover, the gas sensing technology can be widely utilized in various fields such as disease diagnosis, food freshness check, industrial safety, and agriculture [5-7]. A gas sensor, responsible for gas detection, should satisfy requirements such as fast response/recovery speed, low power operation, low cost, low operation temperature, high reliability, high selectivity to target gas, and portability. Thus, numerous research groups have researched and developed diverse types of gas sensors such

as optical [8-10], electrochemical [11-13], and semiconductor-type [14-16] in accordance with these requirements.

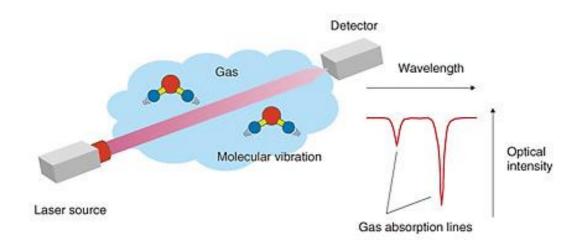


Fig. 1.1. Schematic drawing of an optical gas sensing measurement [17].

Optical gas sensors, in general, consist of three primary components: a light source, a gas chamber, and a light detector [17]. Each target gas has its own absorption characteristics at a certain wavelength of the light source. Thus, the target gas molecules will only absorb light of a certain wavelength among the light of various wavelengths coming from the light source, and the existence of the target gas may be recognized by the light detector, as shown in Fig. 1.1. They offer a high

level of selectivity and a rapid response time since the operating concept is only based on the physical property of the target gas and does not include any chemical reaction between the target gas molecules and the sensors [18]. Nonetheless, their commercialization is limited because to limitations in terms of shrinking, mobility, and cost, and they require additional research.

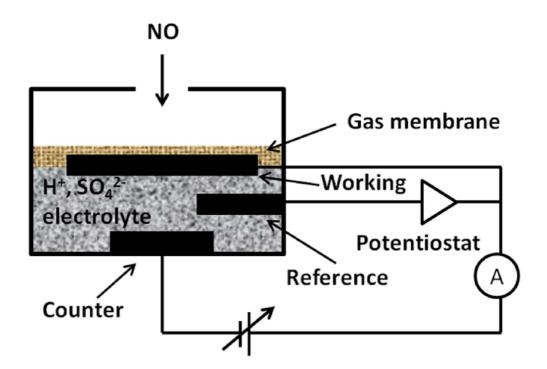


Fig. 1.2. Schematic diagram of an electrochemical NO sensor [19].

As shown in Fig. 1.2, electrochemical gas sensors are made up of a working electrode, a reference electrode, a counter electrode (optional), and an electrolyte solution in which the two or three electrodes are immersed. They detect target gas by measuring the current or potential difference between their two electrodes, which is created by a reduction-oxidation reaction on the working electrode [13,19]. They are sensitive to target gas at low concentrations and may operate with very little power. They are very affordable and resistant to environmental moisture [20]. However, because the electrolyte solution in them might dry up at high temperatures or low humidity, they have a limited operating temperature range. They have a short lifespan and necessitate electrolyte solution maintenance and calibration [21].

Gas sensors based on semiconductors, specifically resistive and field-effect transistor (FET)-type, are also available. Because of their low cost and simplicity, resistive gas sensors are the most explored kind of gas sensors. The change in resistance (*R*) of the sensors caused by target gas exposure is utilised. It is straightforward to apply various gas sensing materials such as semiconducting

metal oxides (MOX) [23-25], carbon nanomaterials [26-28], and transition metal dichalcogenides (TMDC) [29-31] to them due to a relatively simple two-terminal structure [22], as shown in Fig. 1.3. Various studies on the shape and chemical functionalization of sensing materials have also been undertaken in order to improve sensitivity to target gas. They should be larger in size to reduce output signal fluctuation and acquire enough working current. Furthermore, because to their enormous sensing surface, a big heater is required to enhance working temperature, resulting in significant power usage [32]. FET-type gas sensors, on the other hand, partially overcome the difficulties noted above with resistor-type gas sensors. The following section goes into greater depth about them (Chapter 1.1.2).

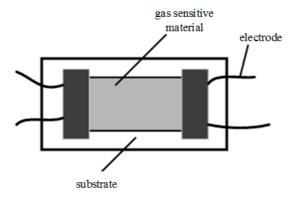


Fig. 1.3. Schematic diagram of a resistive gas sensor [22].

1.1.2 FET-type gas sensors

When exposed to target gas, FET-type gas sensors use a sensing layer as a gate or channel, and the threshold voltage (V_{th}) or drain current (I_D) change. They are compatible with complementary metal-oxide-semiconductor (CMOS) production technology, as opposed to the previous three types of gas sensors. Multiplexers (MUX), analog-to-digital converters (ADC), and gain control amplifiers (PGA), as well as flash memories capable of read, write, and erase operations, are CMOS integrated circuits (IC) designed to control variation in output signals as well as calibrate changes in ambient factors during gas sensing such as humidity, temperature, and so on [33]. As a result, FET-type gas sensors, which can be easily coupled with CMOS ICs and flash memory on a single chip, can be used to construct practical high precision gas sensing systems efficiently. Furthermore, using CMOS process technology, they may be made in a very compact form at a low cost. However, research on FET-type gas sensors is limited in comparison to other types of gas sensors.

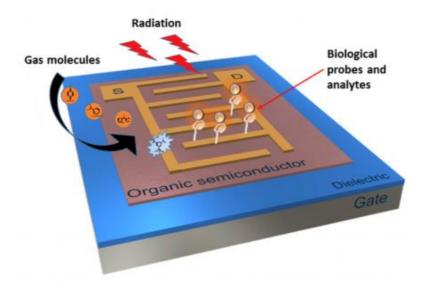


Fig. 1.4. Schematic diagram of an organic TFT-type gas sensor [34].

Thin-film transistor (TFT) [34-36], catalytic metal gate FET [37-39], suspended gate FET (SGFET) [40], capacitively coupled FET (CCFET) [41] are examples of conventional FET-type gas sensors.

As shown in Fig. 1.4, TFT-type gas sensors normally feature three terminals: a gate, a source, and a drain, and use a sensing layer as its active layer (channel). When exposed to the gas, they detect it by measuring changes in device characteristics produced by charge transfer or redistribution in the active layer. The use of CMOS ICs for signal amplification allows them to outperform resistive

sensors in terms of detection limits and sensitivity. They do, however, require a large sensing area for a consistent output and waste a lot of heating power [35]. Furthermore, when injected into the sensors, target gas can induce traps surrounding the interface between the active layer (sensing layer) and the gate insulator to degrade [42].

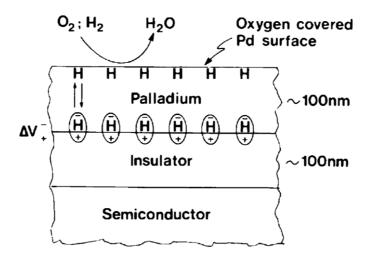


Fig. 1.5. Schematic diagram of a palladium (Pd)-gate FET-type gas sensor [43].

Catalytic metal gate FET-type gas sensors have a metal-insulatorsemiconductor (MIS) structure and detect change caused by the catalytic reaction in the metal gate, which forms a dipole layer at the interface between the metal gate and gate insulator [43] as shown in Fig. 1.5. They are easily produced using Si CMOS process technology. However, the size of gas molecules that can be detected is limited since large gas molecules are difficult to pass through the metal gate. Furthermore, metals that can be utilized as the metal gate are limited.

SGFET- and CGFET-type gas sensors have as suspended gate that is covered with a sensing layer, as well as an air gap formed between the sensing layer and transducer (FET) [40] as shown in Figs. 1.6 and 1.7. During gas sensing, the target gas molecules might pass through the air gap and react with the sensing layer, resulting in a potential difference. As such, they are capable of circumventing the restrictions of catalytic metal gate FET-type gas sensors. The air gap in these sensors allows them to detect gas molecules of any size. As the flip-chip mounting technology is applied for forming the sensing layer, the desired sensing layer can be applied. However, the presence of the air gap reduces the coupling between the control-gate (CG) and floating-gate (FG), lowering sensitivity. Because at least eight photomasks and the flip-chip mounting technology are required, the fabrication process is complicated.

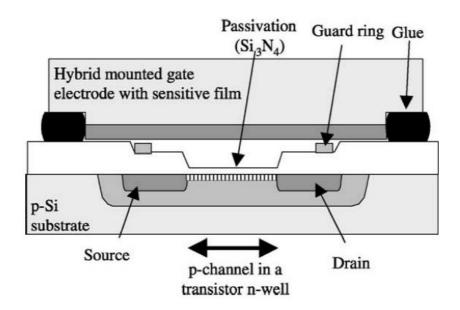


Fig. 1.6. Schematic diagram of a SGFET-type gas sensor [40].

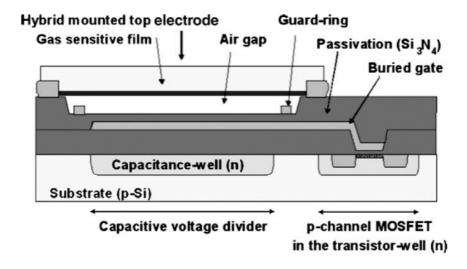


Fig. 1.7. Schematic diagram of a CCFET-type gas sensor [40].

Our research group was the first to propose a silicon (Si) horizontal floatinggate FET (HFGFET)-type gas sensor [44,45] to address the shortcomings of traditional FET-type gas sensors as shown in Fig. 1.8(a) and (b). Because the two electrodes are interdigitated and face each other, high coupling can be created in this sensor. A sensing layer is produced locally between a CG and a FG. The manufacturing process is simpler than that of SGFET- and CCFET-type gas sensors. They have a small micro-heater generated at the bottom of the sensing layer that consumes less electricity by heating the sensing layer locally [46]. Furthermore, to improve the gas detecting features of HFGFET-type gas sensors, a pre-bias pulse measurement approach was presented [47]. During the sensing characteristics measurement, the CG can be subjected to appropriate pre-bias and read-bias. The polarity and amplitude of the pre-bias will change both the response and recovery properties of the sensors, thereby boosting sensing performance without the inclusion of any bulky equipment such as a light source. Furthermore, because the sensors' read function is limited in tens of microseconds, the possibility of undesired charge trapping was greatly reduced.

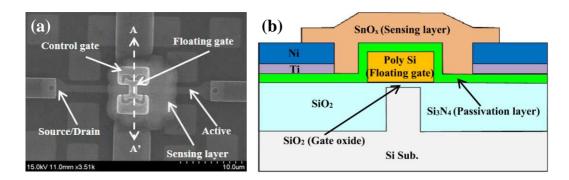


Fig. 1.8. (a) Top scanning electron microscopy (SEM) image and (b) schematic diagram of an HFGFET-type gas sensor [44].

1.2 Purpose of research

Although several FET-type gas sensors including the HFGFET-type gas sensor capable of overcoming the limitations of the resistive and conventional FET-type gas sensors have been proposed so far, there has been very little research on gas sensor platforms in which various types of gas sensors including FET-type gas sensors and CMOS ICs for processing output signals are integrated together. In our research group, the HFGFET-type gas sensors have been fabricated using only a single type of Si substrate [44-50], but the standard CMOS process technology including the well formation process should be utilized to integrate CMOS ICs onto a single substrate using the same manufacturing process. Furthermore, a gas sensor array, combined with neuromorphic computing technology, helps to detect and selectively discriminate target gas in a short time [51,52]. To manufacture a highly sensitive and energy-efficient gas sensor array using the FET-type gas sensors, their structure should be optimized.

In this dissertation, a gas sensor platform using the conventional Si CMOS process technology is proposed. The proposed gas sensor platform has a structure

in which FET-type gas sensors with a horizontal floating-gate structure (HFGFETtype), thin-film transistor (TFT)-type gas sensors with a bottom gate, and resistive gas sensors are integrated together with polysilicon (poly-Si) gate FETs and flash memories and can be manufactured with only 10 photomasks. At the bottom of the sensing layer of the HFGFET-type gas sensor, an embedded micro-heater is formed to locally heat the sensing layer to the optimal operating temperature corresponding to the target gas. Because the HFGFET-type gas sensor's structure includes that of a floating-gate MOSFET, flash memory operation is conceivable, and therefore it may be used to calibrate a sensor output signal by altering an operating point. Meanwhile, a design optimization guideline for FET-type gas sensors, including the HFGFET-type gas sensor, is proposed, taking gas sensitivity, noise characteristics, power consumption, and other factors into account. The electrical characteristics depending on the structure, such as the size and shape of the sensing layer and transducer, were modeled using actual measurements and technology computer-aided design (TCAD) device simulation, and the optimization indicator was designed using the established model. Utilizing the optimized HFGFET-type

gas sensor, gas and humidity sensing characteristics were investigated using harmful gases such as nitrogen dioxide (NO₂) and hydrogen sulfide (H₂S), and the sensing mechanism of the sensor was explained. Furthermore, the gas sensing characteristics of the TFT-type and resistive gas sensors were also investigated, and the operability of each sensor was verified.

1.3 Dissertation outline

This dissertation is organized as follows. Chapter 1 outlines the background of the study, providing an introduction of gas sensor technology by introducing various types of gas sensors. Then, the advantages of FET-type gas sensors are described compared to other types of gas sensors. Moreover, the characteristics of the several conventional FET-type gas sensors and the HFGFET-type gas sensor, proposed previously in our research group, are covered in this chapter. The purpose of research and the outline of dissertation are also introduced, respectively. In chapter 2, the structure and fabrication process of the Si CMOS gas sensor platform consisting of the HFGFET-type, TFT-type, and resistive gas sensors with the CMOS transistors and flash memories are explained in detail. Then, the sensing material in the gas sensor platform is introduced and characterized. In chapter 3, the electrical characteristics of the fabricated n- and p-channel poly-Si gate FET are described. Then, the functionality of the flash memory devices and CMOS inverters fabricated onto the same substrate and manufacturing process are introduced. Furthermore, the operability of both types of the HFGFET-type gas sensors fabricated using CMOS process technology is also covered in this chapter. Chapter 4 contains the design optimization process and guideline of the FET-type gas sensors utilizing the fabricated HFGFET-type gas sensors as an example. The examples of gas sensing of the HFGFET-type gas sensors and the thermal characteristics of the embedded micro-heaters are also covered in this chapter. Chapter 5 introduces the fundamental and gas sensing characteristics of the TFT-type and resistive gas sensors, and deals with the operability of them. Finally, the conclusion of the study is presented in Chapter 6.

Chapter 2

Platform structure and fabrication

2.1 Platform structure

Fig. 2.1 shows a schematic bird's eye view of the proposed gas sensor platform which consists of the HFGFET-type, TFT-type (having a bottom-gate structure), and resistive gas sensors. Utilizing standard 0.5 μ m Si CMOS process technology, various types of gas sensors are easily integrated onto a same substrate. No more than ten photomasks are used to fabricate the platform. Therefore, the platform is very advantageous for mass production at a low cost. In addition, CMOS ICs such as MUX, ADC, and PGA, and flash memories, which can be used to process and calibrate the output signal of the gas sensors, can be integrated with the gas sensors thanks to the process compatibility. The gas sensors in the platform can be utilized as unit devices of a gas sensor array for the purpose of improving selectivity to a target gas. For example, if each of the gas sensors uses the same sensing material, the different types of gas sensors may be bundled together to form the gas sensor array. Besides, the same type of gas sensors with different sensing materials can also be utilized as the gas sensor array. Since the sensing layer is formed at the end of the fabrication process, any sensing material can be applied to the platform.

The structure of each of the gas sensors composing the platform is depicted as a schematic diagram and top SEM images of them in Fig. 2.2(a)-(d). In the HFGFET-type gas sensors, the CG and FG are horizontally interdigitated each other, resulting in a high coupling ratio (γ) between them compared to that of the conventional FET-type gas sensors [44], and the sensing layer is formed between the two gates as shown in Fig. 2.2(a) and (b). The field oxide isolates the FET channels of each of the sensors to significantly reduce the interference of the electrical signal. The embedded micro-heater, composed of n⁺-doped poly-Si (R_{Sheet} = $\sim 80 \Omega/\text{sq.}$) and simultaneously formed with the FG, designed to heat the sensing layer for effective gas sensing. Here, the width and thickness of the micro-heater are $\sim 2 \mu m$ and ~ 300 nm, respectively. To inhibit the heat dissipation caused by the micro-heater, an air gap of $\sim 10 \ \mu m$ is created under and around the sensing layer.

Note that the air gap should be designed so that it is not created near the FET channel. The sensing layer is thought to function as a kind of a gate of the sensor because it is insulated from the FG by the SiO₂/Si₃N₄/SiO₂ (O/N/O) layer but connected to the CG. In addition, the O/N/O layer, especially N layer, acts as a passivation layer to prevent contaminants outside the sensor from penetrating into the FET channel. The resistive gas sensors fabricated in the platform has a twoterminal structure like that of the conventional sensors. Each of the electrodes is formed in an interdigitated shape as shown in Fig. 2.2(c). Here, both the field oxide and O/N/O layer isolate the sensor and Si substrate. The fabricated TFT-type gas sensors feature a bottom-gate structure as shown in Fig. 2.2(a) and (d). Here, the gate is composed of n^+ -doped poly-Si, same with the FG and micro-heater in the HFGFET-type gas sensors. The structure of the sensors is like adding a gate under the structure of the resistive gas sensors. The sensing material serves both as a sensing layer and a channel (active) for the TFT.

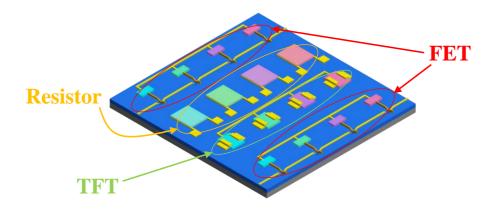


Fig. 2.1. Schematic bird's eye view of the proposed gas sensor platform.

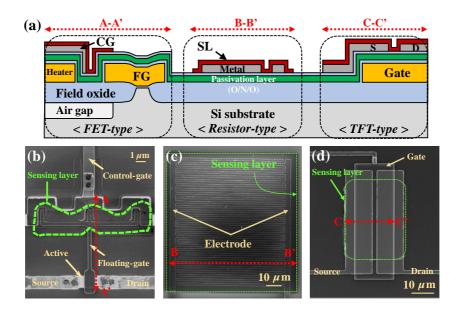


Fig. 2.2. (a) Schematic diagram of the three different gas sensors in the proposed gas sensor platform. (b) Top SEM images of the fabricated HFGFET-type gas sensor, (c) resistive gas sensor, and (d) TFT-type gas sensor.

2.2 Platform fabrication

2.2.1 Fabrication process

The Si CMOS gas sensor platform having the various gas sensors, and the CMOS devices and circuits was fabricated using no more than ten photomasks and standard Si CMOS process technology containing the well formation process. Figs. 2.3 and 2.4 show the key process flow and schematic diagram of the key process steps. Detailed fabrication process of the platform is as follows.

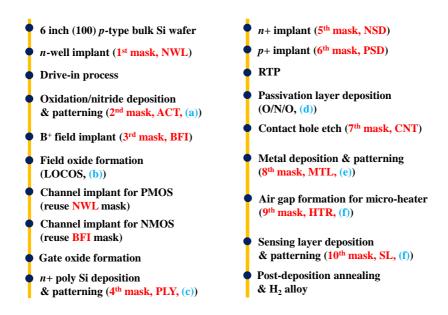


Fig. 2.3. Key process flow of the Si CMOS gas sensor platform. Here, (a)-(f) correspond to Fig. 2.4(a)-(f).

A 6-inch p-type bulk Si wafer having (100) orientation was cleaned using the following standard wafer cleaning process. First, the sulfuric peroxide mix (SPM) cleaning was performed at 120 °C for 10 min using a solution consisting of sulfuric acid (H₂SO₄) and hydrogen peroxide (H₂O₂) with a ratio of 4:1 to remove heavy organics and metallics from the wafer surface. Subsequently, the APM cleaning was performed at 80 °C for 10 min using a solution consisting of ammonium hydroxide (NH₄OH), H₂O₂, and distilled (DI) water (H₂O) with a ratio of 1:8:64 to remove organics, metallics, and particles from the wafer surface. Then, the HPM cleaning was performed at 80 °C for 10 min using a solution consisting of hydrochloric acid (HCl), H₂O₂, and H₂O with a ratio of 1:1:5 to remove remaining metallics and ions such as sodium ions (Na⁺) and potassium (K⁺) from the wafer surface. Since a thin layer of SiO₂ film is unavoidably grown on the Si wafer surface during the cleaning process, the native oxide should be completely removed by a diluted hydrofluoric acid (DHF) solution consisting of HF and H₂O with a ratio of 1:100 at room temperature for 60 sec. To align more compactly between the patterns to be formed by the subsequent photolithography processes, the reference markers can be utilized optionally. A photomask was formed onto the Si substrate by the photolithography (SS03A9), and the substrate was patterned by the inductively coupled plasma (ICP) dry etching. To form *n*-well region for the *p*-channel devices, the well formation process was performed. First, a 10-nm-thick SiO₂ layer was deposited by the low pressure chemical vapor deposition (LPCVD) to form the sacrificial oxide, which serves to protect the substrate from damage that occurs during the ion implantation process. Subsequently, a photomask was formed onto the SiO₂ layer by the photolithography (SS03A9), and the *n*-well implantation process (P^+ , 120 keV, 3 × 10¹² cm⁻²) was performed. Then, the drive-in process was carried out at 1100 °C for 11 h to form the *n*-well with a depth of \sim 2 μ m. After the sacrificial oxide removal, the local oxidation of silicon technique was performed to form the field oxide. First, a 10-nm-thick SiO₂ layer and a 150-nm-thick Si₃N₄ layer were consecutively formed onto the substrate by the thermal oxidation (@ 950 °C, 3 min 30 sec, Dry) and LPCVD (@ 785 °C, 1 h), respectively. Then, a photomask was formed onto the Si₃N₄ layer by the photolithography (SS03A9), and the layers were sequentially patterned by the reactive ion etching (RIE) process to define the active regions of the FET (Figs. 2.3(a) and 2.4(a)). To perform the B⁺ field implantation, which protects the thick-oxide field regions of *n*-channel devices by penetrating the thick oxide and increasing the doping concentration at the silicon interface, a photomask was formed by the photolithography (SS03A9) again, and the B⁺ field implantation (40 keV, 1.6×10^{13} cm⁻²) was performed. Then, a 550-nm-thick SiO₂ layer was thermally grown (@ 1000 °C, 1 h 55 min, Wet) to form the field oxide. Because the SiO₂ and Si₃N₄ layers above the active regions were no longer needed, the layers were removed by the wet etching using the DHF and phosphoric acid (H₃PO₄) solutions. As the final process of the LOCOS technique, the thermal oxidation process (@ 950 °C, 50 min, Dry) was performed to remove the white-ribbon-shaped residues created during the wet oxidation process, and the thermal oxide was etched back except for a 10-nm-thick sacrificial oxide layer for the channel implantation process using the DHF wet etching (Figs. 2.3(b) and 2.4(b)). The field oxide formed by the LOCOS technique is depicted in the SEM image as shown in Fig. 2.5. The thickness of the remaining field oxide after the LOCOS technique was ~500 nm, and the unintended oxide structures, usually called bird's beaks, grew in the direction of the channel center by $\sim 0.25 \mu m$. To manipulate the electrical characteristics of the FET devices including the $V_{\rm th}$, the channel implantation was performed after the photolithography (SS03A9) to open the region corresponding to each channel type (n or p) of the FET device. Note that the photomasks used for the B⁺ field implantation and n-well formation can be reused when the channel implantation is carried out for the *n*- and *p*-channel FET devices, respectively. Detailed channel implantation conditions are described in the next section (Chapter 2.2.2). A 10-nm-thick SiO₂ layer was thermally grown (@ 850 °C, 40 min, Dry) to be used as a gate insulator, and then a 300-nm-thick in situ n^+ -doped poly-Si was deposited by the LPCVD (@ 580 °C, 1 h 25 min) and patterned by the photolithography (SS03A9) and ICP dry etching for the FG and micro-heater of the HFGFET-type gas sensors and the bottom gate of the TFT-type gas sensors (Figs. 2.3(c) and 2.4(c)). Then, the source/drain (S/D) implantation (n-channel: As⁺, 40 keV, 2×10^{15} cm⁻², p-channel: BF₂⁺, 25 keV, 2×10^{15} cm⁻²) was performed after the photolithography (SS03A9) to open the region corresponding to each channel type (n or p) of the device. Note that the body implantation was spontaneously performed because the n- and p-channel FET devices usually require the p^+ and p^+ body contacts, respectively. After the rapid thermal process (RTP) (@ 1050 °C, 5 sec), which is usually performed to form a desired junction depth and recover crystal defects in the Si substrate that occur during the implantation process, the O/N/O layer (10 nm/20 nm/10 nm) was consecutively deposited by the thermal oxidation (@ 800 °C, 10 min, Dry) and LPCVD (N: @ 785 °C, 6 min, O: @ 800 °C, 13 min) (Figs. 2.3(d) and 2.4(d)). Then, the contact holes were defined by the photolithography (SS03A9) and RIE process. To form the CG and electrodes, the photolithography (DNR-L300-30) was performed first. Note that the negative photoresist (PR) was used to pattern the electrodes in shape of a negative slope. Following the buffered HF (BHF) wet etching to remove native oxide, a metal stack consisting of Ti/TiN/Al/TiN layer (20 nm/20 nm/50 nm/10 nm) was consecutively deposited by the sputter. Subsequently, the lift-off process was performed using the acetone (CH₃COCH₃) immersion and sonication (Figs. 2.3(e) and 2.4(e)). Note that the sputtering process should be performed at a temperature below 100 °C for the effective lift-off process. To create an air gap under the micro-heater, the field oxide along the edge of the micro-heater was patterned by the photolithography (SS03A9) and ICP dry etching with carbon tetrafluoride (CF₄) gas. Then, the air gap was finally created by the deep RIE process with sulfur hexafluoride (SF₆) gas. Note that the dry etching was carried out anisotropically by the first etching process, but isotropically by the second etching process. After the sensing layer formation process (Figs. 2.3(f) and 2.4(f)), the H₂ alloy process was finally performed in a 5% of hydrogen (H₂) ambience at 400 °C for 10 min. Detailed sensing layer formation process is described in the Chapter 2.2.3.

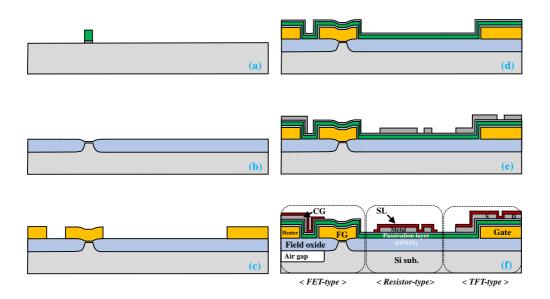


Fig. 2.4. (a)-(f) Schematic diagram of the key fabrication process of the Si CMOS gas sensor platform.

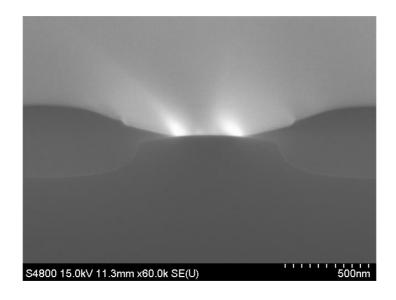


Fig. 2.5. SEM images of the field oxide formed by the LOCOS technique.

2.2.2 Simulation study for channel implantation

The channel implantation was conducted to control the electrical characteristics of the FET devices including the $V_{\rm th}$. To design the FET devices more accurately, the TCAD process simulation tool (Silvaco Inc. Athena) was utilized. Here, the simulation was carried out by realizing all fabrication process steps of poly-Si gate FETs that could be simulated in the tool. In the platform, the FET devices including the FETs in the ICs was designed so that the $V_{\rm th}$ s were greater than 0 V to operate in enhancement mode (normally-off state). Furthermore, since the n^+ -doped poly-Si was used to serve as a gate for all FETs in the platform, the $V_{\rm th}$ s of the p-channel FETs was fairly high. Therefore, the buried channel implantation, forming a buried channel by implanting with ions of a dopant type opposite to that of the substrate, through BF₂⁺ ions was performed to lower V_{th} for the p-channel FETs only. Besides, the buried channel implantation has the effect of lowering the flicker (1/f) noise, deeply linked to the low-frequency noise (LFN) characteristics [53]. In the nchannel FETs, on the other hand, the surface channel implantation, rather than the buried channel implantation, was performed.

Fig. 2.6 shows the simulated transfer characteristics $(I_D - V_{GS})$ of the *n*-channel FETs (the channel width/length (W/L) = 1.0 μ m/0.5 μ m) at a drain voltage (V_{DS}) of 0.1 V as a parameter of a B⁺ implantation energy (keV) from 20 to 35 with a fixed B⁺ implantation dose (cm⁻²) of 4.0×10^{12} . The V_{th} of the *n*-channel FET is decreased as the implantation energy increases. This is because as the implantation energy increases, the hole density in the FET channel near Si/SiO2 interface decreases, so that the FET channel can be inverted even at a lower gate voltage ($V_{\rm GS}$). Fig. 2.7 shows the simulated I_D - V_{GS} characteristics of the *n*-channel FETs at a V_{DS} of 0.1 V as a parameter of a B⁺ implantation dose (cm⁻²) from 2.0×10^{12} to 6.0×10^{12} with a fixed B^+ implantation energy (keV) of 28. The V_{th} of the *n*-channel FET is increased as the implantation dose increases due to the increase in the hole density in the FET channel near Si/SiO₂ interface. Regardless of the implantation energy and dose, the off-current, I_D extracted at a V_{GS} of 0 V, of the *n*-channel FET is found to be less than 100 fA as shown in Figs. 2.6 and 2.7. The detailed device parameters extracted from the simulated curve is displayed in Tables 2.1 and 2.2.

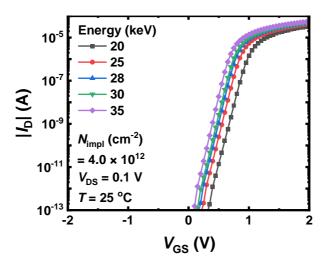


Fig. 2.6. Simulated I_D - V_{GS} curves as a parameter of the channel implantation energy in the n-channel FETs.

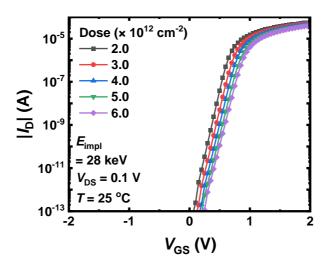


Fig. 2.7. Simulated I_D - V_{GS} curves as a parameter of the channel implantation dose in the n-channel FETs.

Energy (keV)	V _{th} (V)	SS (mV/dec)	Off-current (A)
20	0.889	92.1	1.14×10^{-15}
25	0.763	88.0	1.20×10^{-15}
28	0.700	86.4	1.81×10^{-15}
30	0.666	85.5	3.09 × 10 ⁻¹⁵
35	0.591	84.0	1.17×10^{-14}

Table 2.1. Several device parameters extracted from the simulated I_D - V_{GS} curves as a parameter of the channel implantation energy in the n-channel FETs. Here, SS represents subthreshold swing of each device.

Dose (cm ⁻²)	V _{th} (V)	SS (mV/dec)	Off-current (A)
2.0×10^{12}	0.561	80.6	1.83×10^{-14}
3.0×10^{12}	0.639	84.1	4.92 × 10 ⁻¹⁵
4.0×10^{12}	0.700	86.4	1.81×10^{-15}
5.0×10^{12}	0.752	87.0	8.41 × 10 ⁻¹⁶
6.0×10^{12}	0.798	89.1	4.50 × 10 ⁻¹⁶

Table 2.2. Several device parameters extracted from the simulated I_D - V_{GS} curves as a parameter of the channel implantation dose in the n-channel FETs.

Fig. 2.8 shows the simulated I_D - V_{GS} of the p-channel FETs ($W/L = 1.0 \mu m/0.5$ μ m) at a V_{DS} of -0.1 V as a parameter of a BF₂⁺ implantation energy (keV) from 20 to 30 with a fixed BF₂⁺ implantation dose (cm⁻²) of 2.7×10^{12} . Here, that of the pchannel FETs with the surface channel implantation (70 keV, 8×10^{11} cm⁻²), which is implanted by P⁺ ions, is also investigated as a reference. In the p-channel FETs, an additional implantation (P⁺, 110 keV, 1.1 × 10¹² cm⁻²), usually called punchthrough stop implantation, is involved to alleviate the punch-through effect, which refers to a phenomenon in which a current flows between the source and drain regardless of the V_{GS} when the source-drain depletion region directly overlaps at the bottom of the channel. Note that the punch-through stop implantation does not apply to n-channel FETs because the B⁺ channel implantation spontaneously prevents the punch-through effect. The $V_{\rm th}$ of the p-channel FET is negatively decreased as the implantation energy increases. This is because as the implantation energy increases, the point at which the acceptor (BF₂⁺) and donor (P⁺) concentrations become the same deepens in the FET channel region, resulting in being inverted even at a lower V_{GS} . Fig. 2.9 shows the simulated I_D - V_{GS} characteristics of the p-channel FETs at a $V_{\rm DS}$ of -0.1 V as a parameter of a BF₂⁺ implantation dose (cm⁻²) from 2.0×10^{12} to 3.5×10^{12} with a fixed BF₂⁺ implantation energy (keV) of 25. The $V_{\rm th}$ of the p-channel FET is negatively decreased as the implantation dose increases due to the increase in the hole density in the FET channel region. As shown in Figs. 2.8 and 2.9, the off-current is formed quite high when the BF₂⁺ implantation energy or dose is high. This is because the hole density in the channel region is sufficiently high that an intentional sourcedrain leakage current may flow even before the inversion. The detailed device parameters extracted from the simulated curve is displayed in Tables 2.3 and 2.4.

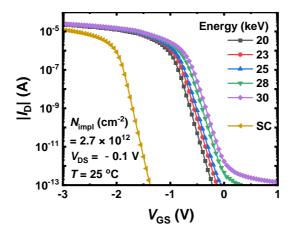


Fig. 2.8. Simulated I_D - V_{GS} curves as a parameter of the channel implantation energy in the p-channel FETs.

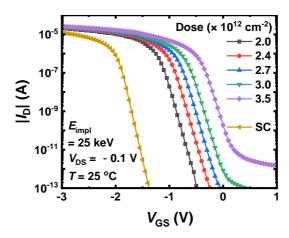


Fig. 2.9. Simulated $I_{\rm D}$ - $V_{\rm GS}$ curves as a parameter of the channel implantation dose in the p-channel FETs.

Energy (keV)	$V_{\mathrm{th}}\left(\mathrm{V}\right)$	SS (mV/dec)	Off-current (A)
20	-0.893	103.2	5.85×10^{-15}
23	-0.823	104.4	2.36×10^{-14}
25	-0.782	107.6	5.80×10^{-14}
28	-0.683	109.6	4.58×10^{-13}
30	-0.624	111.8	1.73×10^{-12}
SC	-1.906	81.6	1.44×10^{-16}

Table 2.3. Several device parameters extracted from the simulated I_D - V_{GS} curves as a parameter of the channel implantation energy in the p-channel FETs.

Dose (cm ⁻²)	$V_{\mathrm{th}}\left(\mathbf{V}\right)$	SS (mV/dec)	Off-current (A)
2.0×10^{12}	-1.121	99.4	5.33×10^{-16}
2.4×10^{12}	-0.932	104.6	5.65×10^{-15}
2.7×10^{12}	-0.782	107.6	5.80 × 10 ⁻¹⁴
3.0×10^{12}	-0.628	108.2	8.45×10^{-13}
3.5×10^{12}	-0.367	113.3	1.89×10^{-10}
SC	-1.906	81.6	1.44×10^{-16}

Table 2.4. Several device parameters extracted from the simulated I_D - V_{GS} curves as a parameter of the channel implantation dose in the p-channel FETs.

One of the short-channel effects (SCE) that occur frequently in FET devices is the drain-induced barrier lowering (DIBL), which has been actually found more prominently in p-channel FETs. Fig. 2.10 shows the simulated I_D - V_{GS} characteristics of the n- and p-channel FETs with a W/L of 1.0 μ m/0.5 μ m (short-channel) and 1.0 μ m/2.0 μ m (long-channel) at a $|V_{DS}|$ of 0.1 V and 1.0 V. Here, the n-channel implantation was performed using B⁺ ions at a implantation energy (keV) of 28 and a implantation dose (cm⁻²) of 4.0 × 10¹², and the p-channel implantation was performed using BF₂⁺ ions at a implantation energy (keV) of 25 and a

implantation dose (cm $^{-2}$) of 2.7×10^{12} . In both types of the long-channel FETs, the DIBL did not occur significantly. However, in the short-channel FETs, the DIBL of the p-channel FET (= 112.2 mV/V) is much larger than that of the n-channel FET (= 11.7 mV/V) as shown in Fig. 2.10. This is because the B $^+$ ions in the S/D regions diffuse toward the center of the FET channel in the p-channel FETs by the RTP after the S/D implantation, thereby shortening their effective gate length. Here, the DIBL value can be calculated as follows:

$$DIBL = \frac{V_{\text{th,low}} - V_{\text{th,high}}}{V_{\text{DS,high}} - V_{\text{DS,low}}}$$
(1)

where the $V_{\rm DS,high}$ and $V_{\rm DS,low}$ represent the relatively high and low $V_{\rm DS}$, and the $V_{\rm th,high}$ and $V_{\rm th,high}$ and V

simulated I_D - V_{GS} characteristics of the short and long, n- and p-channel FETs with the sidewall spacers at a $|V_{DS}|$ of 0.1 V and 1.0 V. Here, the thickness of the sidewall spacers is $\sim 0.1 \,\mu \text{m}$, and the acceptor concentration at the inner edges of the sidewall spacers is formed to be $\sim 2 \times 10^{19}$ cm⁻³ in the *p*-channel FETs. As shown in Fig. 2.11, the SCEs including the DIBL (= 43.3 mV/V) and $V_{\rm th}$ roll-off were considerably reduced in the p-channel FETs. Meanwhile, the effective channel length of the *n*-channel FETs became longer due to the formation of the sidewall spacers. To offset this, the lightly doped drain (LDD) process (P^+ , 10 keV, 5×10^{13} cm⁻²) was introduced in them. The LDD process refers to implanting at a slightly lower dose than the dose at the S/D implantation prior to forming the sidewall spacers. By implementing the LDD process, the donor concentration at the inner edges of the sidewall spacers is changed from $\sim 5 \times 10^{16}$ cm⁻³ to $\sim 2 \times 10^{19}$ cm⁻³ in the *n*-channel FETs. Besides, the LDD process also reduces the potential SCEs such as hot carrier injection (HCI) effect. However, the sidewall spacer formation and LDD processes should not be applied to the HFGFET-type gas sensors because the sidewall spacer formed on the FG inhibits the coupling between the CG and FG.

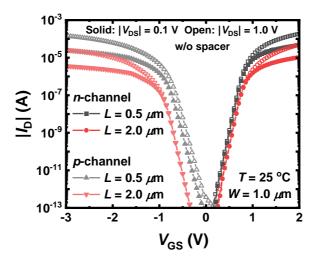


Fig. 2.10. Simulated I_D - V_{GS} curves of the short and long, n- and p-channel FETs without the sidewall spacers at a $|V_{DS}|$ of 0.1 V and 1.0 V.

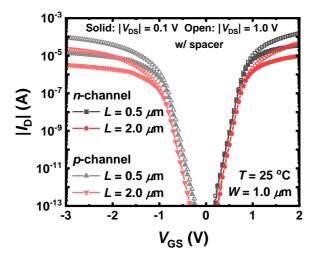


Fig. 2.11. Simulated $I_{\rm D}$ - $V_{\rm GS}$ curves of the short and long, n- and p-channel FETs with the sidewall spacers at a $|V_{\rm DS}|$ of 0.1 V and 1.0 V.

2.2.3 Formation of sensing layer

In the HFGFET-type gas sensors, the sensing layer is formed between the CG and FG so that the FET channel and sensing layer are formed apart horizontally. Nevertheless, most gas sensing material such as MOXs, carbon nanomaterials, and TMDCs are incompatible with the CMOS manufacturing process. Consequently, the sensing layer should be formed in the final step of the fabrication process to protect the sensors from contamination during the sensing layer formation.

Our research group has been utilized three typical methods for forming sensing layers onto the sensors: sputtering [44,53], atomic layer deposition (ALD) [46,47], and inkjet printing [48-50]. Among them, the inkjet printing has advantages in low cost and ease of integration with diverse sensing materials in sensor arrays without the need for patterning. However, the device-to-device variation and inadequate contact with the CG may limit the reliability of the gas sensing characteristics. On the other hand, the physical vapor deposition (PVD) including the sputtering and ALD have disadvantage of forming the same sensing material onto the sensors and necessitating additional photolithography steps, but are commonly employed due

to the homogeneous deposition and excellent contact properties between the CG and sensing layer.

In this dissertation, the indium oxide (In_2O_3) film was used as a sensing layer, formed by the radio-frequency (RF) magnetron sputter using an In_2O_3 target (99.99%). The argon/oxygen (Ar/O₂) flow rates, sputtering pressure, RF power, substrate temperature, and process time were set to 30 sccm/3 sccm, 5 mTorr, 50 W, $20\,^{\circ}$ C, and $10\,$ min, respectively. Here, the deposition rate of the In_2O_3 film was $\sim 1.2\,$ nm/min, and thus the thickness of the deposited film is $\sim 12\,$ nm. After the sputtering, the post-deposition annealing (PDA) was finally performed to crystallize the In_2O_3 film in a vacuum at $300\,^{\circ}$ C for $10\,$ min.

The SEM picture of a portion of the sensing layer (In₂O₃ film) in the platform is shown in Fig. 2.12. It is discovered that the sensing layer is porous enough to allow target gas molecules to permeate to the In₂O₃/SiO₂ interface. To determine the constituent elements of the sensing layer, energy-dispersive X-ray spectroscopy (EDS) was performed on an In₂O₃/SiO₂/Si sample (after PDA) with the identical formation conditions as the platform sensors. As illustrated in Fig. 2.13, the X-ray

peaks reveal the constituent elements of the sensing layer. Those values are the same as their equivalent inherent values in the In₂O₃ film. Furthermore, the structural investigation of the sensing layer was performed using X-ray diffraction (XRD). The In₂O₃/SiO₂/Si sample (after PDA) was also employed in this study. Figure 2.14 depicts the sample's XRD spectrum. The sample contains diffraction peaks corresponding to reflections from (211), (222), (400), (411), (332), (510), (440), (611), (541), (622), (631), and (444), indicating that the deposited In₂O₃ film has a cubic bixbyite structure [54].

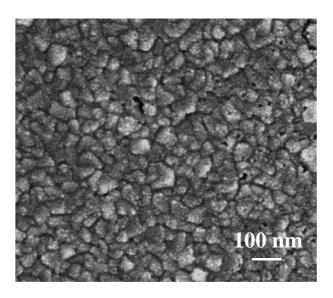


Fig. 2.12. Top SEM image of a part of the sensing layer (In₂O₃ film) in the platform.

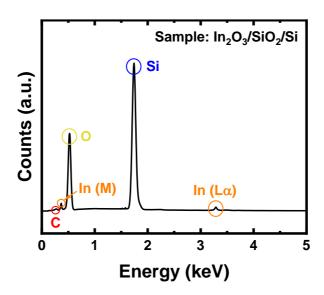


Fig. 2.13. EDS spectrum of the In₂O₃/SiO₂/Si sample after PDA.

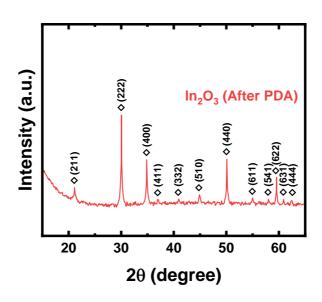


Fig. 2.14. XRD spectrum of the In₂O₃/SiO₂/Si sample after PDA.

Chapter 3

Fundamental FET characteristics

3.1 I-V characteristics of poly-Si gate FET

Transistors, including a MOSFET, a tunneling FET (TFET), and a bipolar junction transistor (BJT), which play a role in switching electrical signals from onto off-state, have been important components in any ICs, required in various fields of application. In the platform, poly-Si gate FETs can be fabricated using the same fabrication process with the gas sensors. In addition, since the CMOS process technology was utilized in the fabrication process of the platform, both types of the FET channel devices can be manufactured onto the same substrate. Here, the n^+ -doped poly-Si, O/N/O layer, and Ti/TiN/Al/TiN metal stack serve as the gate, intermetal dielectric (IMD), and electrodes/pads, respectively.

First, the I-V characteristics, such as the I_D - V_{GS} and output (I_D - V_{DS}) characteristics, of the fabricated n-channel FETs were investigated. The structure of

the *n*-channel FET is simply depicted in Fig. 3.1. The electrical measurement was conducted by a DC *I-V* method using a semiconductor parameter analyzer (B1500A, Agilent). The I_D - V_{GS} characteristics of the fabricated *n*-channel FETs were measured as a parameter of the channel length ($L = 0.5 \mu m$, 2.0 μm) and V_{DS} (= 0.1 V, 1.0 V) at room temperature as shown in Fig. 3.2. Here, the channel width was fixed to 2.0 μm . The FET channel was formed by the surface channel implantation (B⁺, 28 keV, 4.0 × 10¹² cm⁻²), mentioned in Chapter 2.2.2. The off-current flows below 1 pA. The V_{th} and SS are ~0.65 V, which is enough to operate in enhancement mode, and ~90 mV/dec, respectively. They can be extracted using following Eqs. (2) and (3).

$$V_{\text{th}} = V_{\text{GS}} \ (@ I_{\text{D}} = \frac{W}{L} \times 100 \text{ nA})$$
 (2)

$$SS = \frac{d\log(I_{\rm D})}{dV_{\rm CG}} \tag{3}$$

Here, Eq. (2) refers to the constant current (CC) method. In the fabricated FET with a channel length of 0.5 μ m, the SCEs such as DIBL and V_{th} roll-off hardly occurred,

and the on-/off-current ratio was calculated to be $\sim 10^8$ at a $V_{\rm DS}$ of 0.1 V. In addition, the $I_{\rm D}$ - $V_{\rm DS}$ characteristics of the fabricated n-channel FETs were measured as a parameter of the $V_{\rm GS}$ (= 0.75 V to 1.50 V, 0.25 V step) at room temperature as shown in Fig. 3.3. Here, the W/L of the measured FET was 2.0 μ m/0.5 μ m. Regardless of the $V_{\rm GS}$, the channel length modulation (CLM), one of the SCEs, hardly occurred in the fabricated n-channel FET.

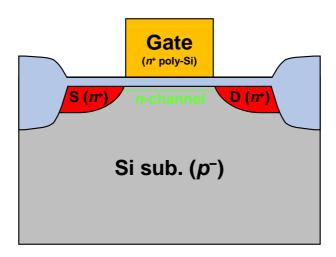


Fig. 3.1. Schematic diagram of the fabricated poly-Si gate *n*-channel FET.

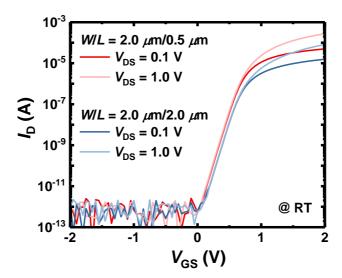


Fig. 3.2. I_D - V_{GS} characteristics of the fabricated n-channel FETs as a parameter of the channel length and V_{DS} at room temperature.

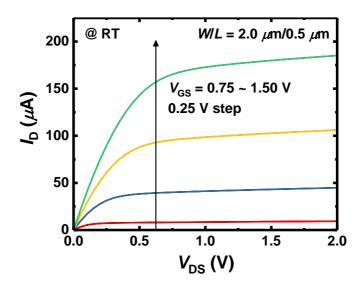


Fig. 3.3. I_D - V_{DS} characteristics of the fabricated n-channel FETs as a parameter of the V_{GS} at room temperature.

Likewise, the I-V characteristics of the fabricated p-channel FETs were investigated. The structure of the p-channel FET, which has the different dopant type of the S/D and substrate, and channel type than the *n*-channel FET (Fig. 3.1), is simply depicted in Fig. 3.4. Here, the *n*-well structure was applied to the *p*channel FET. Fig. 3.5(a) (without the sidewall spacers) and (b) (with the sidewall spacers) show the I_D - V_{GS} characteristics of the fabricated p-channel FETs as a parameter of the channel length ($L = 0.5 \mu m$, 2.0 μm) and V_{DS} (= -0.1 V, -1.0 V) at room temperature. Here, the channel width was fixed to 2.0 µm, like the nchannel FET. The FET channel was formed by the buried channel implantation $(BF_2^+, 25 \text{ keV}, 2.7 \times 10^{12} \text{ cm}^{-2})$, mentioned in Chapter 2.2.2. The off-current flows below 1 pA, like the *n*-channel FET. The $|V_{th}|$ and SS are 0.9-1.0 V, which is enough to operate in enhancement mode, and 80-90 mV/dec, respectively. In the fabricated FET with a channel length of 0.5 μm, and without the sidewall spacers, there were visible SCEs such as DIBL and $V_{\rm th}$ roll-off as shown in Fig. 3.5(a). Here, the value of DIBL is ~67 mV/V. To resolve the SCEs in the fabricated p-channel FETs, the sidewall spacers were used. Here, the thickness of the sidewall spacers is $\sim 0.06 \ \mu m$. As a result, the value of DIBL decreased to ~40 mV/V, and the $V_{\rm th}$ roll-off was reduced significantly as shown in Fig. 3.5(b). The on-/off-current ratio had a value between 10^7 and 10^9 , depending on the channel length or $V_{\rm DS}$ in the fabricated p-channel FETs. In addition, the $I_{\rm D}$ - $V_{\rm DS}$ characteristics of the fabricated p-channel FETs were measured as a parameter of the $|V_{\rm GS}|$ (= 1.25 V to 2.00 V, 0.25 V step) at room temperature as shown in Fig. 3.6(a) (without the sidewall spacers) and (b) (with the sidewall spacers). Here, the W/L of the measured FET was 2.0 μ m/0.5 μ m, like the n-channel FET. As expected, the p-channel FET without the sidewall spacers were more prone to the CLM compared to that with them.

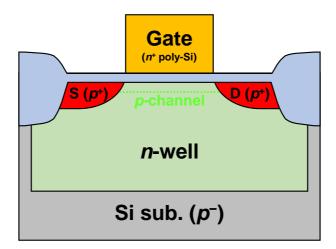


Fig. 3.4. Schematic diagram of the fabricated poly-Si gate *p*-channel FET.

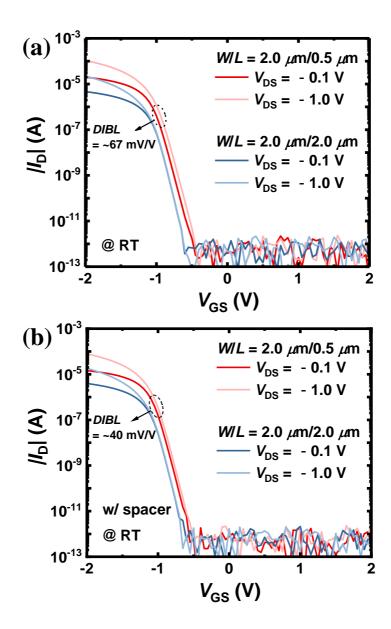


Fig. 3.5. I_{D} - V_{GS} characteristics of the fabricated p-channel FETs (a) with and (b) without the sidewall spacers as a parameter of the channel length and V_{DS} at room temperature.

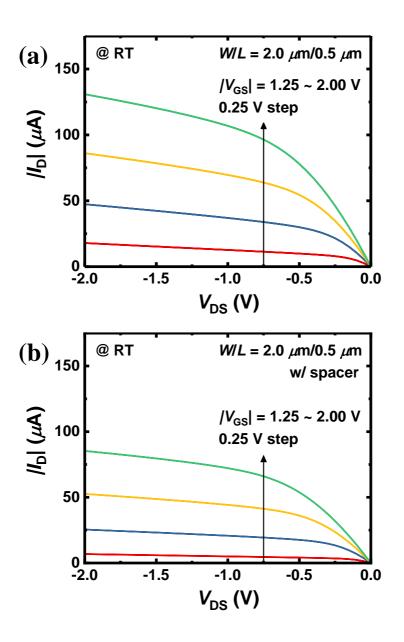


Fig. 3.6. I_D - V_{DS} characteristics of the fabricated n-channel FETs (a) with and (b) without the sidewall spacers as a parameter of the V_{GS} at room temperature.

3.2 Flash memory functionality

Unlike a dynamic random-access memory (DRAM) and a static random-access memory (SRAM), where stored information disappears when the power is turned off, a flash memory is a non-volatile memory that does not lose stored information even when the power is turned off. A flash memory is not only used in various storage devices and electronic products, but also recently used in neuromorphic computing. In the platform, a flash memory can be fabricated using the fabrication process of the HFGFET-type gas sensor thanks to its FG MOSFET structure.

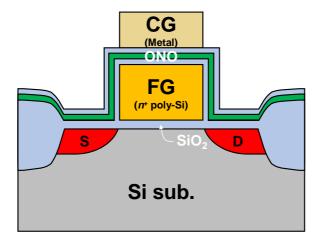


Fig. 3.7. Schematic diagram of the fabricated flash memory.

The structure of the fabricated flash memory is simply depicted in Fig. 3.7. Here, the O/N/O layer serves as a blocking oxide of conventional FG MOSFETs. The shift of the I_D - V_{GS} curves of the fabricated n- (solid symbol) and p-channel (opened symbol) flash memories ($W/L = 2.0 \mu m/0.5 \mu m$) under the different program (V_{PGM}) and erase (V_{ERS}) voltages at room temperature is shown in Fig. 3.8. Here, a $|V_{DS}|$ of 0.1 V was applied. The flash memories exhibit the program/erase (P/E) characteristics by Fowler-Nordheim (F-N) tunneling like conventional negative-AND (NAND) flash memories. The body, source, and drain of the flash memories were grounded while the V_{PGM} or V_{ERS} was applied to the CG for 5 sec simultaneously. In the *n*-channel device, the I_D - V_{GS} curve shifts to the right when the positive V_{PGM} is applied to the CG. On the other hand, the I_D - V_{GS} curve shifts to the left when the negative $V_{\rm ERS}$ is applied to the CG. The p-channel device also exhibits the P/E characteristics. Note that the bias condition for the P/E in the pchannel device is opposite to that in the *n*-channel device. In this way, the $V_{\rm th}$ of the flash memory can be tuned by adjusting the P/E times (t_{PGM} , t_{ERS}), V_{PGM} , and V_{ERS} . Fig. 3.9 shows the retention characteristics of the fabricated *n*- (solid symbol) and p-channel (opened symbol) flash memories at room temperature. In both the P/E states and both types of the devices, negligible V_{th} shifts ($\Delta V_{th} < 0.036$ V) occurred for 10^4 sec. As a result, the retention time of the fabricated flash memories can be said to be more than 10^4 sec.

The flash memory functionality can be also applied to the HFGFET-type gas sensor. Due to its interdigitated gate structure, the high γ can be achieved. Thus, the HFGFET-type gas sensor is expected to have the low V_{PGM} and V_{ERS} for the P/E operation. The tunable V_{th} is highly beneficial for calibrating the sensor's output signal as well as adjusting the operating point of the load transistors in a transimpedance amplifier (TIA), one of the read-out ICs (ROIC) required to process the sensor's output signal.

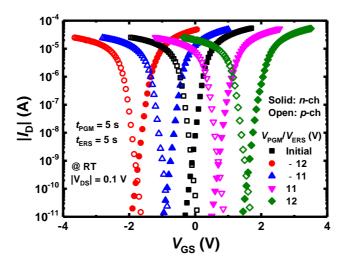


Fig. 3.8. P/E characteristics of the fabricated n- and p-channel flash memories under the different V_{PGM} and V_{ERS} at room temperature.

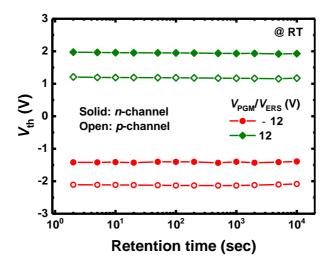


Fig. 3.9. Retention characteristics of the fabricated *n*- and *p*-channel flash memories at room temperature.

3.3 CMOS inverter characteristics

Among the CMOS ICs, logic devices/circuits such as inverter, buffer, and ring oscillator have been utilized as an important component in various signal processing circuits of gas sensors. In the platform, the most basic and simplest form of a CMOS inverter was integrated by simply connecting the aforementioned n- and p-channel poly-Si gate FETs in series. The schematic diagram of the fabricated CMOS inverter is depicted in Fig. 3.10. For convenience, a parasitic capacitance at the output stage of the inverter is omitted. The gates and drains of the n- and p-channel FETs are connected to each other. Here, the connected gate and drain are used as the input and output terminals, respectively. The source of the *n*-channel FET is grounded, while a positive voltage $(V_{\rm DD})$ is applied to that of the p-channel FET. Ideal CMOS inverter operates so that the output signal becomes the '1' state when the input signal is the '0' state, whereas the output signal becomes the '0' state when the input signal is the '1' state. Here, the '0' and '1' states refer to when the input $(V_{\rm in})$ /output voltage $(V_{\rm out})$ is 0 V and $V_{\rm DD}$, respectively. When the input signal is the '0' state, the *n*-channel FET is turned off, while the *p*-channel FET is turned on. Consequently, the output signal becomes the '1' state. In the opposite case, the output signal becomes the '0' state because only the *n*-channel FET is turned on.

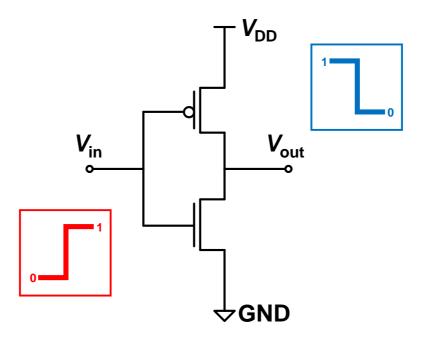


Fig. 3.10. Schematic diagram of the fabricated CMOS inverter.

Fig. 3.11(a) shows the voltage transfer curves (VTC) of the fabricated CMOS inverter as a parameter of the $V_{\rm DD}$ (= 1.0 V to 3.0 V, 0.5 V step) at room temperature. Here, the W/Ls of the n- and p-channel FETs are 2.0 μ m/1.0 μ m and 2.0 μ m/0.5 μ m, respectively. The VTCs of the inverter exhibit an excellent inverting performance

with the abrupt transition, full logic swing, and low leakage current in the static condition. In ideal CMOS inverter, the logic transition, which refers to the change of the output signal's state ('1' state \rightarrow '0' state), occurs at the point (V_{th} of the inverter) where the $V_{\rm in}$ and $V_{\rm out}$ are equal. In Fig. 3.11(a), the logic transition occurs at a $V_{\rm in}$ closer to 0 V than $V_{\rm DD}$ because the $V_{\rm th}$ of the n-channel FET is lower than that of the p-channel FET. The voltage gains of the inverter are higher than 50 except for a $V_{\rm DD}$ of 1.0 V. Fig. 3.11(b) shows the width of the transition region (TW) extracted from the VTCs of the fabricated CMOS inverter. The TW can be extracted as the width of the region where the voltage gain is larger than 1. In the fabricated inverter, the TWs are less than 0.36 V under the all measured $V_{\rm DD}$ s. Meanwhile, the noise margin (NM) is another important factor in influencing the sensitivity and tolerance to signal interference in logic devices including conventional inverters. The NM can be extracted utilizing the ideal output high voltage ($V_{\rm OH}$), ideal output low voltage $(V_{\rm OL})$, minimum input high voltage in the transition region $(V_{\rm IH})$, and maximum input low voltage in the transition region $(V_{\rm IL})$. Here, the NM for the '1' state $(NM_{\rm H})$ and '0' state $(NM_{\rm L})$ are defined as follows.

$$NM_{\rm H} = V_{\rm OH} - V_{\rm IH} \tag{4}$$

$$NM_{\rm L} = V_{\rm OL} - V_{\rm IL} \tag{5}$$

Consequently, the normalized total noise margin (TNM) can be extracted as follows.

normalized
$$TNM = \frac{NM_{\rm H} + NM_{\rm L}}{V_{\rm DD}}$$
 (6)

The normalized TNMs is extracted from the VTCs of the fabricated CMOS inverter under the all measured $V_{\rm DDS}$ as shown in Fig. 3.11(b).

The CMOS inverter can be also fabricated utilizing the HFGFET-type gas sensors. Here, the n- and p-channel sensors are connected in series like conventional CMOS inverters. Fig. 3.12(a) shows the VTCs of the fabricated CMOS inverter utilizing the sensors as a parameter of the $V_{\rm DD}$ (= 1.0 V to 3.0 V, 0.5 V step) at room temperature. Here, the W/Ls of the n- and p-channel sensors are 1.0 μ m/2.0 μ m and 2.0 μ m/1.0 μ m, respectively, same with the poly-Si gate CMOS inverter. The VTCs

of the inverter show a symmetrical and abrupt inverting performance with a slightly lower voltage gain than the poly-Si gate CMOS inverter. The voltage gain of the inverter are \sim 41 at a $V_{\rm DD}$ of 1.5 V. Fig. 3.12(b) shows the TWs and normalized TNMs extracted from the VTCs of the fabricated CMOS inverter utilizing the sensors. The TWs and normalized TNMs, related to a margin of inverters, of the inverter utilizing the sensors are slightly worse than those of the poly-Si gate inverter.

Additionally, a CMOS buffer was fabricated by connecting the output terminal of one CMOS inverter and the input terminal of the other CMOS inverter in the platform (Fig. 3.13(a)). Note that the fabricated buffer is actually different from conventional CMOS buffers in that the W/Ls of the inverters constituting the fabricated buffer are all the same. Therefore, the buffer can only play a role in digitizing the state of the output signal in two steps ('0' and '1' states). Fig. 3.13(b) shows the VTCs of the fabricated CMOS buffer as a parameter of the $V_{\rm DD}$ (= 1.0 V to 3.0 V, 0.5 V step) at room temperature. As expected, the VTCs of the buffer show an abrupt digitizing performance.

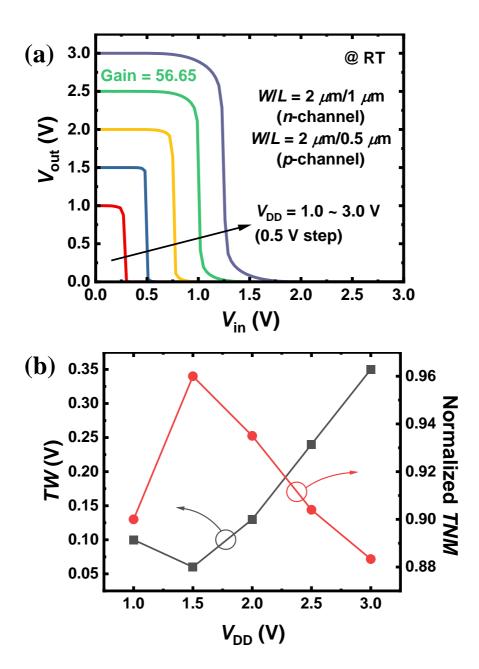


Fig. 3.11. (a) VTCs (V_{out} versus V_{in}) of the fabricated CMOS inverter as a parameter of the V_{DD} at room temperature. (b) TW and normalized TNM extracted from the VTCs in (a).

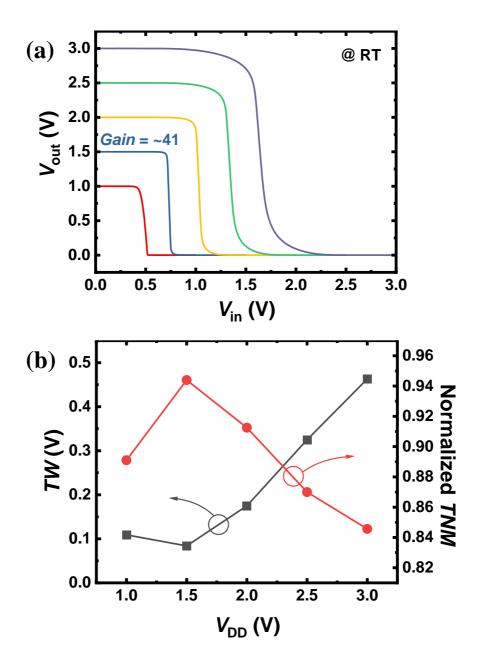


Fig. 3.12. (a) VTCs of the fabricated CMOS inverter utilizing the HFGFET-type gas sensors as a parameter of the $V_{\rm DD}$ at room temperature. (b) TW and normalized TNM extracted from the VTCs in (a).

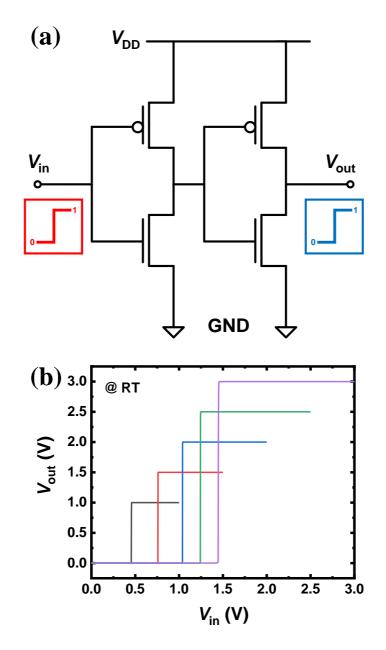


Fig. 3.13. (a) Schematic diagram of the fabricated CMOS buffer. (b) VTCs of the fabricated CMOS buffer as a parameter of the $V_{\rm DD}$ at room temperature.

3.4 Application to HFGFET-type gas sensor

The CMOS process technology can be directly applied to the HFGFET-type gas sensor. Utilizing the well formation process, both the n- and p-channel sensors were fabricated in the platform like the poly-Si gate FETs. Fig. 3.14(a) and (b) indicate the I_D - V_{CG} characteristics of the fabricated n- and p-channel HFGFET-type gas sensors at $|V_{DS}|$ s of 0.1 V (black solid line) and 1 V (red solid line). Here, the operating temperature (T) was set to 160 °C to accelerate the gas reaction using the embedded micro-heater. Both the sensors operate normally with an off-current of hundreds of fA. In addition, the NO₂ gas sensing characteristics were briefly investigated measuring the I_D-V_{CG}. Here, the gas was injected into the sensor for 10 min, and its concentration was set to 500 ppb. In both the *n*- and *p*-channel sensors, the I_D - V_{CG} curves shift to the right due to the oxidizing property of NO₂, so the fabricated sensors can be said to detect NO2 well. Furthermore, the transient measurements were carried out by alternately injecting air and various concentrations of NO₂ from 100 ppb to 500 ppb in the both types of fabricated sensors at 160 °C shown in Fig. 3.15(a) and (b). Here, the $|V_{DS}|$ and initial $|I_D|$ was

fixed to 0.1 V and \sim 1 μ A, respectively. The gas reaction occurred in a direction consistent with the direction of the gas reaction corresponding to each type of the gas sensors because the I_D - V_{CG} curves shift to the right. Detailed explanations about the gas sensing mechanism and additional gas sensing characteristics are described in the next chapter (Chapter. 4).

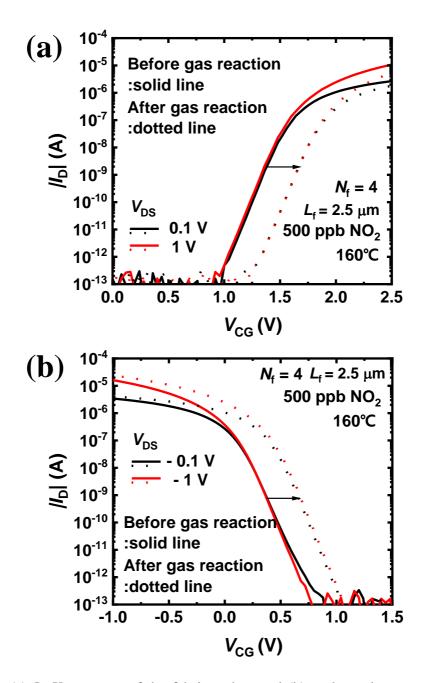


Fig. 3.14. (a) I_D - V_{CG} curves of the fabricated n- and (b) p-channel HFGFET-type gas sensors before and after the 500 ppb NO₂ injection at 160 °C for 10 min.

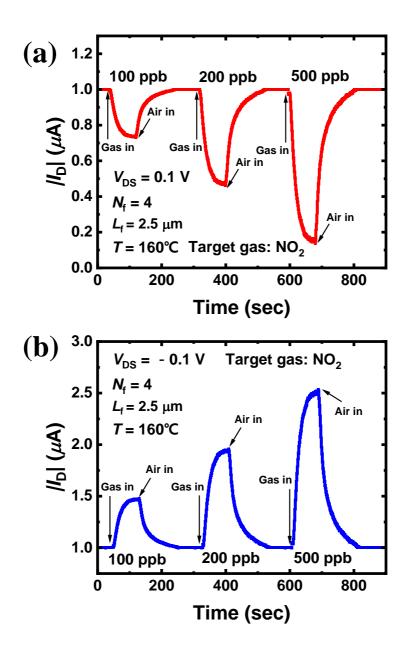


Fig. 3.15. (a) Transient gas responses of the fabricated n- and (b) p-channel HFGFET-type gas sensors to NO₂ (100 ppb, 200 ppb, 500 ppb) at 160 °C.

Chapter 4

Semiconductor-based gas sensors

4.1 TFT-type gas sensors

In the platform, a bottom-gate TFT-type gas sensor (Fig. 4.1) can be fabricated through the same fabrication process with the HFGFET-type gas sensor. n^+ -doped poly-Si was used as a gate material, and the O/N/O layer was utilized as a gate insulator. Sputtered In_2O_3 film acts as both a sensing layer and an active (channel).

Fig. 4.2 shows the I_D - V_{GS} characteristics of the fabricated TFT-type gas sensor under the various T_S (= 60 °C, 90 °C, 120 °C, and 150 °C) at a V_{DS} of 1 V. Here, the W/L of the sensor is 40 μ m/2 μ m. The I_D - V_{GS} curves indicate that the In₂O₃ film has the properties of an n-type semiconductor. Fig. 4.3(a) and (b) show the I_D - V_{GS} curves of the sensor before and after the NO₂ (500 ppb) and H₂S (50 ppm) gas reactions under the various T_S , respectively. Here, both the target gases are injected into the sensor for 1 min. The I_D is decreased and the V_{th} is increased when NO₂ is

injected into the sensor (Fig. 4.3(a)), whereas the I_D is increased and the V_{th} is decreased when H_2S is injected into the sensor (Fig. 4.3(b)). Furthermore, the gas sensing performance is most excellent at 150 °C in the measured T range. The transient NO_2 and H_2S responses of the TFT-type gas sensor as a parameter of the gas concentration also show the gas sensing characteristics of the sensor as shown in Fig. 4.4(a) and (b), respectively. Here, the concentration of NO_2 ranges from 50 ppb to 500 ppb, and that of H_2S ranges from 5 ppm to 50 ppm. Both the t_{res} and t_{rec} of the sensor are within ~100 sec at 150 °C. Note that the t_{res} and t_{rec} become shorten as the T rises. As expected, the $|\Delta I_D|$ is increased as the gas concentration increases.

As described above, when NO₂ molecules is injected into the sensor, they deprive the sensing material of electrons, and they become the negatively charged molecules (NO₂⁻). Consequently, the sensing layer become more depleted (Fig. 4.5), resulting in the I_D decrease and V_{th} increase. On the other hand, when H₂S molecules is injected into the sensor, they react with the previously adsorbed O₂⁻s and donate electrons to the sensing layer. As a result, the depletion layer of the sensing layer become narrower (Fig. 4.5), resulting in the I_D increase and V_{th} decrease.

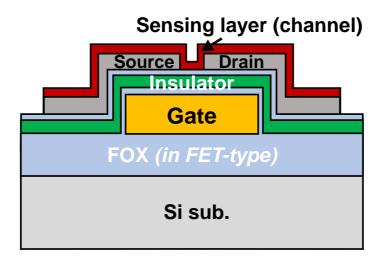


Fig. 4.1. Schematic structure of the fabricated TFT-type gas sensor.

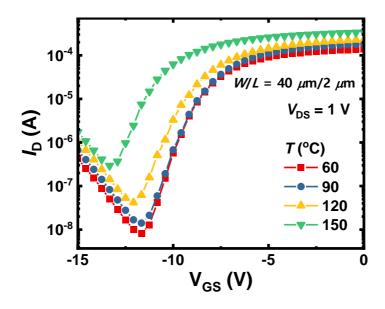


Fig. 4.2. I_D - V_{GS} curves of the fabricated TFT-type gas sensor under the various T_S (= 60 °C, 90 °C, 120 °C, and 150 °C) at a V_{DS} of 1 V.

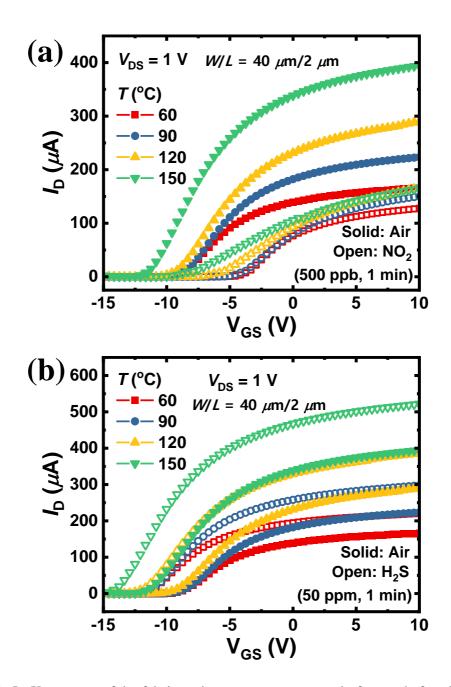


Fig. 4.3. I_D - V_{GS} curves of the fabricated TFT-type gas sensor before and after the (a)

 NO_2 and (b) H_2S gas reaction under the various Ts at a V_{DS} of 1 V.

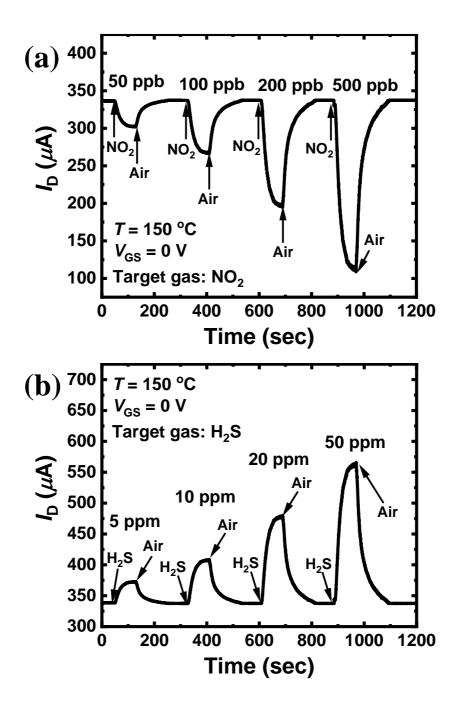


Fig. 4.4. Transient (a) NO₂ and (b) H₂S responses of the fabricated TFT-type gas sensor under the various gas concentration at 150 °C.

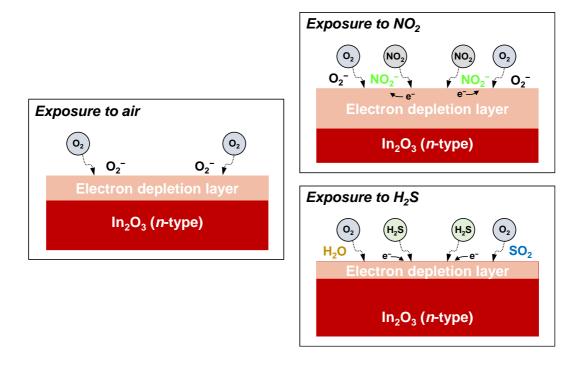


Fig. 4.5. Schematic diagram for explaining the NO_2 and H_2S sensing mechanisms of the TFT-type gas sensor.

4.2 Resistive gas sensors

Resistive gas sensor (Fig. 4.6) can be also fabricated using the same fabrication process with the HFGFET-type gas sensor in the platform. Like conventional resistive gas sensors, a sensing layer (In₂O₃) is formed between two electrodes.

Fig. 4.7 shows the ohmic (I_R-V_R) characteristics of the fabricated resistive gas sensor under the various Ts (= 60 °C, 90 °C, 120 °C, and 150 °C). It can be seen that the resistance of the sensing layer is decreased as the T increases, like the intrinsic property of semiconductor. Fig. 4.8(a) and (b) show the I_R - V_R characteristics of the sensor before and after the NO₂ (500 ppb) and H₂S (50 ppm) gas reactions under the various Ts. Here, both the target gases are injected into the sensor for 1 min. Like the TFT-type gas sensor, the I_R is decreased when NO₂ is injected into the sensor, while the I_R is increased when H_2S is injected into the sensor. Fig. 4.9(a) and (b) show the transient NO₂ and H₂S responses as a parameter of the gas concentration at 150 °C. These results are also similar to those of the TFT-type gas sensor (Fig. 4.4(a) and (b)). The NO₂ and H₂S sensing mechanisms of the resistive gas sensor is the same with those of the TFT-type gas sensor.

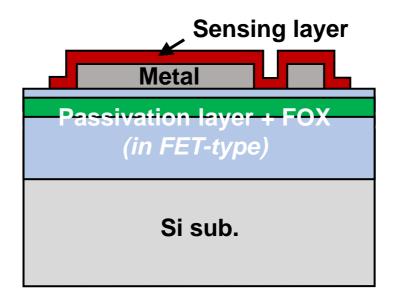


Fig. 4.6. Schematic structure of the fabricated resistive gas sensor.

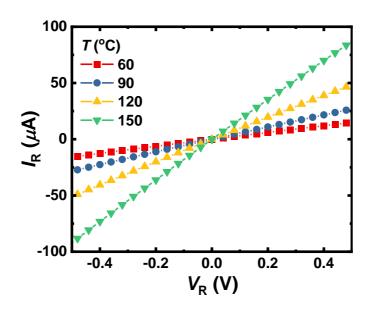


Fig. 4.7. I_R-V_R characteristics of the fabricated resistive gas sensor under the various

Ts (= 60 °C, 90 °C, 120 °C, and 150 °C).

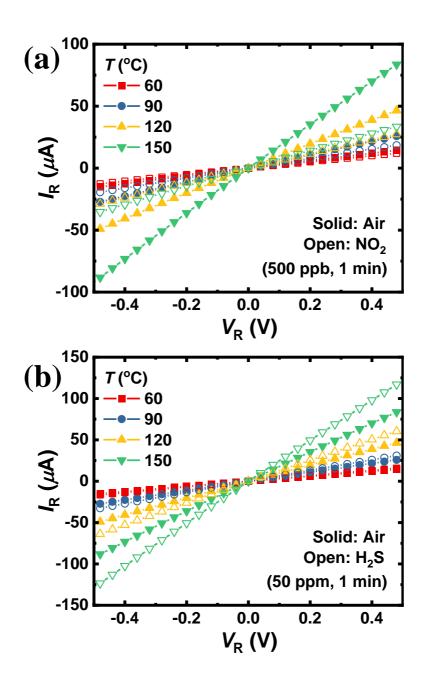


Fig. 4.8. I_R - V_R characteristics of the fabricated resistive gas sensor before and after the (a) NO₂ and (b) H₂S gas reaction under the various T_S .

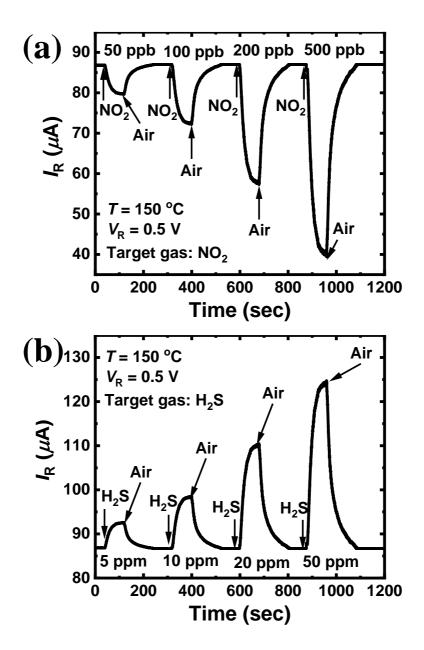


Fig. 4.9. Transient (a) NO_2 and (b) H_2S responses of the fabricated resistive gas sensor under the various gas concentration at 150 °C.

Chapter 5

Horizontal floating-gate FET-type gas sensors

5.1 Electrical characteristics

The electrical characteristics of the HFGFET-type gas sensors, briefly covered in Chapter 3.4, are investigated. Fig. 5.1 shows the structure overview of the fabricated HFGFET-type gas sensor [55]. Here, the CG and FG is interdigitated, and the distance between the two gates is fixed to 0.5 μ m. The sensor can be divided into two parts: a sensing material area and an FET channel. In terms of the sensing material area, the number (N_f) and length (L_f) of the FG digits, related to a coupling area between the CG and FG, are important parameters that determine the electrical characteristics of the sensor. Besides, the FET channel size (W and L) also affects them. Note that the electrical and thermal characteristics of the embedded microheater depend on both the $N_{\rm f}$ and $L_{\rm f}$ of the sensor because the micro-heater is formed similar to the shape of the CG at the bottom of the sensing layer.

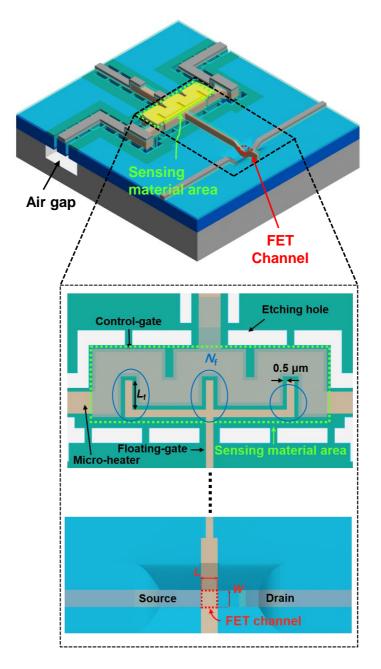


Fig. 5.1. Structure overview of the fabricated HFGFET-type gas sensor. This shows the bird eye's view and top schematic view of the sensor [55].

Fig. 5.2 shows the I_D - V_{CG} characteristics of the fabricated HFGFET-type gas sensors as a parameter of the N_f using the DC (Line) and pulsed I-V (PIV) (Symbol) measurements [55]. Here, the T, V_{DS} , and L_f are set to 20 °C, -0.1 V, and 2.5 μ m, respectively. In Chapter 5, only the p-channel gas sensors are utilized because they have less 1/f noise than the n-channel devices. The PIV measurement is conducted using waveform generator and fast measurement unit (WGFMU) measurement system based on Agilent B1500. The applied pulse waveform is depicted in Fig. 5.2. Here, the CG read voltage (V_{rCG}) and base voltage $(V_{base}, 0 \text{ V})$ is alternately applied to the CG with pulse widths of the on-time (t_{on}) of 10 μ s. Note that the drain read voltage $(V_{\rm rDS})$ is synchronized with the $V_{\rm rCG}$. As shown in Fig. 5.2, the $I_{\rm D}$ - $V_{\rm CG}$ curves measured in the PIV method are nearly same with those measured in the DC method except for the off-current regions due to the limitation of measurement resolution of the WGFMU module. As the $N_{\rm f}$ of the sensor increases, the $I_{\rm D}$ - $V_{\rm CG}$ curve shifts to the right and the SS is decreased due to the increment of the γ between the CG and FG. Note that the off-currents will not increase if the T rises due to the long distance (> 10 µm) between the micro-heater and FET channel [46]. In addition, the micro-heater's current-voltage (I_H - V_H) characteristics were also investigated as a parameter of the N_f using the DC (Line) and pulsed I-V (PIV) (Symbol) measurements as shown in Fig. 5.3 [55]. As expected, the R of the micro-heater is increased as the N_f increases. Detailed thermal characteristics of the micro-heater is introduced in Chapter 5.2.

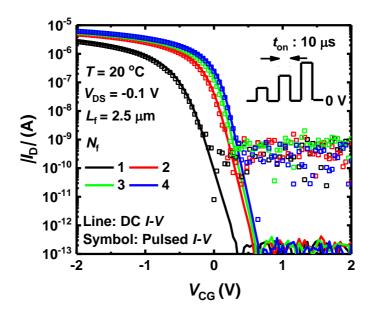


Fig. 5.2. I_D - V_{CG} characteristics of the fabricated HFGFET-type gas sensors as a parameter of the $N_{\rm f}$ using the DC and PIV measurements at 20 °C [55].

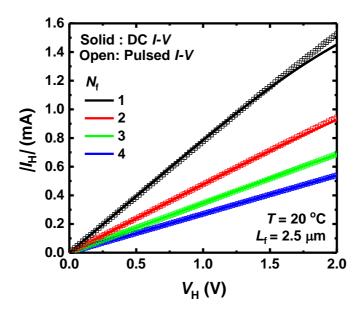


Fig. 5.3. $I_{\rm H}$ - $V_{\rm H}$ characteristics of the embedded micro-heaters as a parameter of the $N_{\rm f}$ using the DC and PIV measurements at 20 °C [55].

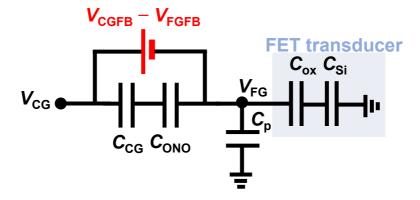


Fig. 5.4. Simplified equivalent circuit of the fabricated HFGFET-type gas sensor [55].

Fig. 5.4 shows the simplified equivalent circuit of the fabricated HFGFET-type gas sensor [55]. In the equivalent circuit, the capacitance of the O/N/O layer, gate oxide, Si substrate, and the parasitic capacitance are denoted by the C_{ONO} , C_{ox} , C_{Si} , and C_{p} , respectively. In addition, the capacitance resulting from the depletion of the sensing layer is denoted by the C_{CG} . The V_{CGFB} and V_{FGFB} are the flat band voltages (V_{FB}) of the sensor and poly-Si gate FET (transducer), respectively. The relation between the FG voltage (V_{FG}) and CG voltage (V_{CG}) can be defined using the γ as:

$$V_{\rm FG} - V_{\rm FGFB} = \gamma (V_{\rm CG} - V_{\rm CGFB}) \,(\text{accumulation}) \tag{7}$$

$$V_{\text{FG}} - V_{\text{FGth}} = \gamma (V_{\text{CG}} - V_{\text{th}}) \text{ (strong inversion)}$$
 (8)

where the $V_{\rm FGth}$ represents the $V_{\rm th}$ of the poly-Si gate FET (transducer). The γ can be expressed using the equivalent circuit as follows.

$$\gamma = \frac{(C_{\text{CG}} \parallel C_{\text{ONO}})}{[(C_{\text{CG}} \parallel C_{\text{ONO}}) + C_{\text{p}} + (C_{\text{ox}} \parallel C_{\text{Si}})]}$$
(9)

TCAD device modeling was used to determine the γ of the constructed sensors as a parameter of the $N_{\rm f}$. The sensors' 3D architectures were generated by simulating the device structure in Sentaurus Device Editor (SDE) (Synopsys Inc.), as illustrated in Fig. 5.5. The I_D - V_{CG} curves of the sensors with four different N_f s were derived using the calibrated TCAD deck, as illustrated in Fig. 5.6. The generated I_D - V_{CG} curves matched the observed curves closely. The $V_{\rm FG}$ of the sensors was then retrieved while the $V_{\rm CG}$ of them was changed in the TCAD device simulation (Fig. 5.7(a)). In this case, the γ is the gradient of the sensors' $V_{\rm FG}$ - $V_{\rm CG}$ curves and is a function of $V_{\rm CG}$. The $C_{\rm Si}$ fluctuates depending on the $V_{\rm CG}$, causing the γ to vary (Fig. 5.7(b)). When the Si substrate is depleted in a $V_{\rm CG}$, the $C_{\rm Si}$ decreases and the γ increases. If $V_{\rm CG}$ is large enough, either positively or negatively, an accumulating layer or a strong inversion layer will grow on the Si channel at the Si/SiO₂ contact. As a result, the $C_{\rm Si}$ grows much greater than the $C_{\rm ox}$ ($(C_{\rm ox}||C_{\rm Si}) \approx C_{\rm ox}$), and the γ becomes constant [55]. Because the sensor mostly functions in strong inversion, the γ may be estimated using Eq (10).

$$\gamma = \frac{(C_{\text{CG}} \parallel C_{\text{ONO}})}{[(C_{\text{CG}} \parallel C_{\text{ONO}}) + C_{\text{p}} + C_{\text{ox}}]}$$
(10)

Since the $C_{\rm CG}$ and $C_{\rm ONO}$ are increased as the $N_{\rm f}$ increases, the γ of the sensor in the strong inversion is increased as shown in Eq. (10). Note that the γ of the sensor can be altered by the change in the $C_{\rm CG}$ due to gas reaction.

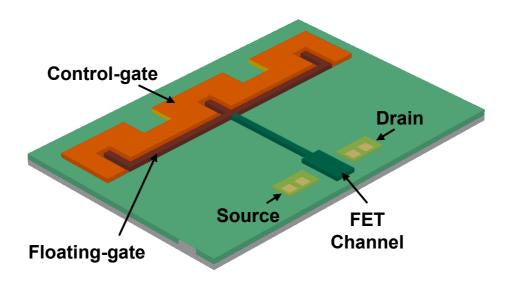


Fig. 5.5. 3D structures of the HFGFET-type gas sensor created by mimicking the device structure in the TCAD simulation tool.

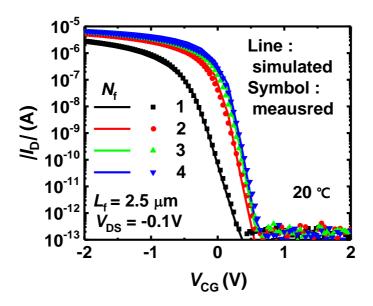


Fig. 5.6. Simulated and measured $I_{\rm D}$ - $V_{\rm CG}$ curves of the HFGFET-type gas sensors with four different $N_{\rm fS}$ at 20 °C.

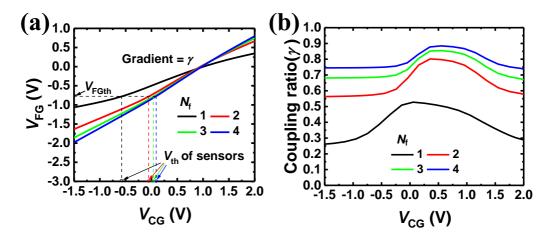


Fig. 5.7. (a) $V_{\rm FG}$ versus $V_{\rm CG}$ as a parameter of the $N_{\rm f}$ in the p-channel HFGFET-type gas sensors. (b) γ of the sensors as a function of the $V_{\rm CG}$ extracted from (a) [55].

The I_D of the fabricated HFGFET-type gas sensor in the subthreshold ($|V_{DS}| >> kT/q$), saturation, and linear regions can be expressed as:

$$|I_{\rm D}| = \mu_{\rm eff} C_{\rm ox}' \frac{W}{L} \sqrt{\frac{\varepsilon_{\rm Si} q N_{\rm D}}{4\psi_{\rm B}}} \left(\frac{kT}{q}\right)^2 e^{\frac{q\gamma(|V_{\rm CG} - V_{\rm th}|)}{mkT}}$$
(subthreshold region) (11)

$$|I_{\rm D}| = \mu_{\rm eff} C_{\rm ox}' \frac{W}{L} \gamma^2 \frac{(|V_{\rm CG} - V_{\rm th}|)^2}{2m}$$
(saturation region) (12)

$$|I_{\rm D}| = \mu_{\rm eff} C_{\rm ox}' \frac{W}{L} \left(\gamma (|V_{\rm CG} - V_{\rm th}|) - \frac{m|V_{\rm DS}|}{2} \right) |V_{\rm DS}| \text{ (linear region)}$$
 (13)

where the $\mu_{\rm eff}$, $C_{\rm ox}$, $N_{\rm D}$, $\varepsilon_{\rm Si}$, $\psi_{\rm B}$, and m stand for the effective mobility in the FET channel, oxide capacitance per unit area, n-type doping concentration in the FET channel, dielectric constant of Si, surface potential at threshold condition, and body-effect coefficient, respectively. Meanwhile, the $V_{\rm th}$ can be expressed as:

$$V_{\rm th} = \phi_{\rm ms} - \frac{Q_{\rm ox}}{C_{\rm oxe}} - 2\psi_{\rm B} - \frac{WL\sqrt{4qN_{\rm D}\varepsilon_{\rm Si}|\psi_{\rm B}|}}{C_{\rm oxe}}$$

$$\approx \phi_{\rm ms} - \frac{Q_{\rm ox}}{\gamma C_{\rm ox}} - 2\psi_{\rm B} - \frac{\sqrt{4qN_{\rm D}\varepsilon_{\rm Si}|\psi_{\rm B}|}}{\gamma C_{\rm ox}'}$$
(14)

$$C_{\text{oxe}} = (((C_{\text{CG}} \| C_{\text{ONO}}) + C_{\text{p}}) \| C_{\text{ox}}) \approx \gamma C_{\text{ox}}$$
(15)

where the ϕ_{ms} and Q_{ox} represent the work function difference between the CG and Si channel and the effective oxide charge, respectively. The transconductance (g_m) of the sensor in the saturation and linear regions can be written as following Eqs. (16) and (17), respectively.

$$g_{\rm m} = \mu_{\rm eff} C_{\rm ox}' \frac{W}{L} \gamma^2 \frac{|V_{\rm CG} - V_{\rm th}|}{m} \text{ (saturation region)}$$
 (16)

$$g_{\rm m} = \mu_{\rm eff} C_{\rm ox}' \frac{W}{L} \gamma |V_{\rm DS}| \text{ (linear region)}$$
 (17)

The theoretical SS of the sensors can be written as following Eq. (18).

$$SS = \frac{\ln(10) \, mkT}{q\gamma} \tag{18}$$

As the N_f of the sensor increases, the g_m of the sensor is increased, and the SS of the sensor is decreased as shown in Fig. 5.6.

5.2 Thermal characteristics of micro-heaters

The thermal properties of four distinct $N_{\rm f}$ s integrated micro-heaters were examined in HFGFET-type gas sensors. The $L_{\rm f}$ of the sensors utilized in the investigation is set to 2.5 μ m in this case. Heater voltage ($V_{\rm H}$) pulses are given to the micro-heater at a frequency (f) of 1 kHz and a duty cycle of 50%. (Fig. 5.8). It should be noted that the room temperature is kept at 20 °C. The resistance temperature detection (RTD) method was used to determine the T of the microheaters [46]. The change in the R ($\Delta R_{\rm H}$) of the micro-heaters with the T is shown in Fig. 5.9. As a result, the $\Delta R_{\rm H}$ -T characteristics were used to calculate the T of the micro-heater when $V_{\rm H}$ pulses were delivered to it. When the micro-heater is turned on, the T increases fast within 100 μ s and then begins to saturate, as illustrated in Fig. 5.10(a). Similarly, after turning off the micro-heater, the T of the micro-heater drops fast within 100 μ s and then begins to saturate. As predicted, as the $V_{\rm H}$ grows, so does the T of the micro-heater when the heat is entirely created. As illustrated in Fig. 5.10(b), the power consumption of the micro-heaters is compared to a parameter of the N_f . As the N_f of the sensor falls, so does the T of the micro-heater for the same power consumption. To attain a T of 300 °C, for example, a microheater with a N_f of 1 consumes 1.44 mW, whereas a micro-heater with a N_f of 4 consumes 1.94 mW, using 35% more power than a micro-heater with a N_f of 1. The T variations (ΔT) of the constructed embedded micro-heaters with energy are shown in Fig. 5.11(a) during the first 5 μ s of the heating period. The heat capacity (C) of the micro-heaters may be calculated using an equation (Fig. 5.11(a)) based on their ΔT for the first 5 μ s of the heating period, as illustrated in Fig. 5.11(b). As the N_f of the sensor grows, so does the C of the micro-heater. The C of a micro-heater with a N_f of 4 is double that of a micro-heater with a N_f of 1.

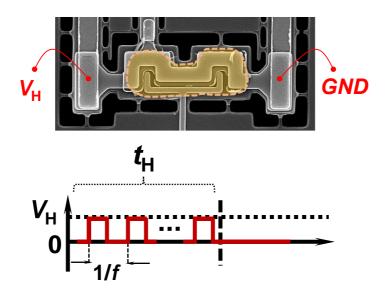


Fig. 5.8. Operating scheme of the fabricated embedded micro-heater.

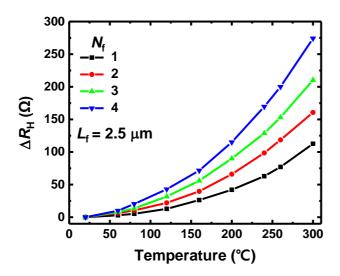


Fig. 5.9. $\Delta R_{\rm H}$ -T characteristics as a parameter of the $N_{\rm f}$ of the fabricated HFGFET-type gas sensors.

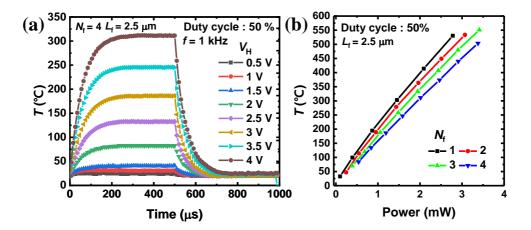


Fig. 5.10. (a) Transient T as a function of the $V_{\rm H}$ at a f of 1 kHz with 50% duty cycle.

(b) T-power as a parameter of the $N_{\rm f}$ of the fabricated sensors [55].

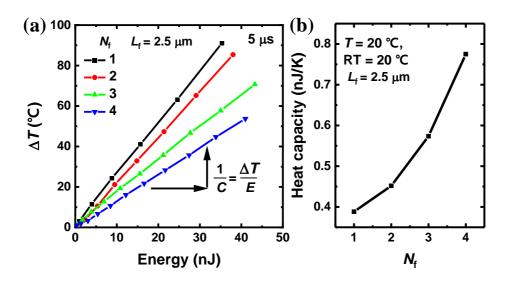


Fig. 5.11. (a) ΔT versus energy consumption for an initial 5 μ s of the heating period.

(b) C of the fabricated embedded micro-heaters with different $N_{\rm f}$ s at 20 °C [55].

5.3 Gas sensing characteristics

The gas sensing characteristics of the manufactured HFGFET-type gas sensors were studied. The sensors can detect NO₂, which has been shown to be sensitive to In_2O_3 [56-58]. The four sensors with varying N_f s were responded to NO_2 at different Ts, and all of the sensors showed the highest $\Delta V_{\rm th}$ and max($\Delta I_{\rm D}$) at 160 °C, as shown in Fig. 5.12(a) and (b). In this case, the sensors' $V_{\rm th}$ and $I_{\rm D}$ were measured five times and displayed using the mean (m) and standard deviation (σ) . As the N_f of the sensor grows, so do the V_{th} and $\max(I_{\text{D}})$. Furthermore, the sensors can detect H_2S , which is a reducing gas with the opposite qualities of an oxidizing gas and is known to be sensitive to In₂O₃ [59,60]. The same measurements as with NO₂ were carried out. As demonstrated in Fig. 5.13(a) and (b), all of the sensors had the highest $V_{\rm th}$ and $\max(I_{\rm D})$ at 215 °C. As the sensor's $N_{\rm f}$ grows, so do the $|V_{\rm th}|$ and $|\max(I_{\rm D})|$ values.

The NO₂ sensing mechanism is explained as follows. When the sensor is exposed to NO₂, the NO₂ molecules are chemically adsorbed onto the sensing layer (In₂O₃). Since NO₂ is an oxidizing gas ionized into NO₂⁻ by taking electrons from the sensing layer, the interface between the sensing layer and ONO layer gets

depleted (Fig. 5.14), resulting in reducing the C_{CG} and γ . The decrease in the C_{CG} due to the gas adsorption negatively increases the $V_{\rm th}$ of the sensor. Nevertheless, the $C_{\rm CG}$ reduction effect is negligible because the $C_{\rm CG}$ and $C_{\rm ONO}$ are much larger than the other capacitances thanks to the interdigitated gate structure. Instead, the negatively charged ions significantly impact the ΔV_{th} change [45]. Since the In₂O₃ is an *n*-type semiconductor, the positive charges are induced in the FET channel to fully satisfy the charge neutrality's law when NO2 is injected into the sensor as shown in Fig. 5.14. As a result, the I_D - V_{CG} curve of the sensor shifts to the right (Fig. 5.14). The sensing mechanisms for most oxidizing gases is similar to the explained NO₂ sensing mechanism. On the other hand, the H₂S sensing mechanism is explained as follows. When the sensor is exposed to H₂S, the H₂S molecules are chemically reacted with oxygen ions (O₂⁻) adsorbed onto the sensing layer. After the reaction, electrons are produced and returned to the sensing layer, resulting in improving the C_{CG} and γ . The increase in the C_{CG} due to the gas reaction negatively decreases the $V_{\rm th}$ of the sensor. However, the $C_{\rm CG}$ improving effect is negligible thanks to the interdigitated gate structure. Instead, as the O₂-s adsorbed onto the sensing layer are removed by the gas reaction, the positive charges generated by the aforementioned charge neutrality's law become reduced [45]. Thus, the I_D - V_{CG} curve of the sensor shifts to the left as shown in Fig. 5.15. The sensing mechanisms for most reducing gases is similar to the explained H₂S sensing mechanism.

The $\Delta V_{\rm th}$ induced by the gas reaction may be described using the simpler equivalent circuit depicted in Fig. 5.16. Here, $Q_{\rm gas}$ represents the charge created by the gas reaction, and $Q_{\rm eff}$ represents the charge that effectively impacts the $\Delta V_{\rm th}$. According to the small-signal paradigm, the two capacitors are linked in parallel. The $Q_{\rm eff}$ can be expressed as following Eq. (19).

$$Q_{\text{eff}} = Q_{\text{gas}} \times \frac{C_{\text{ONO}} \parallel (C_{\text{p}} + C_{\text{ox}})}{C_{\text{CG}} + C_{\text{ONO}} \parallel (C_{\text{p}} + C_{\text{ox}})}$$
(19)

The $\Delta V_{\rm eff}$, caused by the $Q_{\rm eff}$, is expressed as following Eq. (20).

$$|\Delta V_{\text{eff}}| = \frac{|Q_{\text{eff}}|}{C_{\text{CG}} + C_{\text{ONO}} \parallel (C_{\text{p}} + C_{\text{ox}})}$$
(20)

The $\Delta V_{\rm eff}$ changes the $V_{\rm CGFB}$ of the sensor, and the $\Delta V_{\rm th}$ (= $\Delta V_{\rm CGFB}$) can be expressed as following Eq. (21).

$$\Delta V_{\text{eff}} = \Delta V_{\text{th}} \times \frac{C_{\text{ONO}} \parallel (C_{\text{p}} + C_{\text{ox}})}{C_{\text{CG}} + C_{\text{ONO}} \parallel (C_{\text{p}} + C_{\text{ox}})}$$
(21)

From Eqs. (19)-(21), the ΔV_{th} can be extracted as following Eq. (22).

$$|\Delta V_{\rm th}| = \frac{|Q_{\rm gas}|}{C_{\rm CG} + C_{\rm ONO} \parallel (C_{\rm p} + C_{\rm ox})} \approx \frac{|Q_{\rm gas}|}{C_{\rm CG} + C_{\rm p} + C_{\rm ox}} (C_{\rm ONO} \gg (C_{\rm p} + C_{\rm ox}))$$
(22)

The $\Delta V_{\rm th}$ increases when the FET channel area shrinks (smaller $C_{\rm ox}$) and the sensing material area expands (larger $Q_{\rm gas}$ and $C_{\rm CG}$). In other words, as the antenna impact increases, the $\Delta V_{\rm th}$ increases as the action of the charged gas molecules is concentrated in the narrow FET channel region.

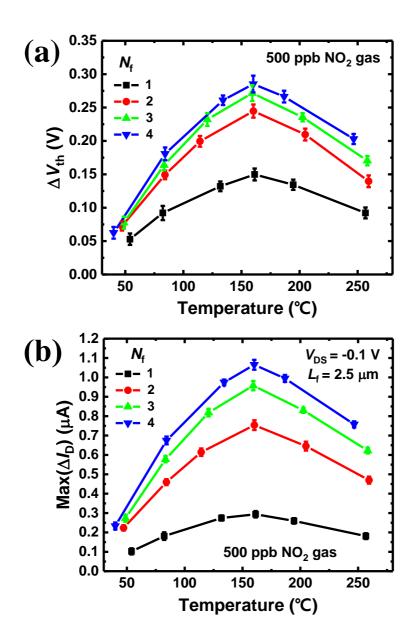


Fig. 5.12. (a) $\Delta V_{\rm th}$ and (b) Max($\Delta I_{\rm D}$) versus T as a parameter of the $N_{\rm f}$ of the fabricated HFGFET-type gas sensors when 500 ppb NO₂ is injected for 10 min.

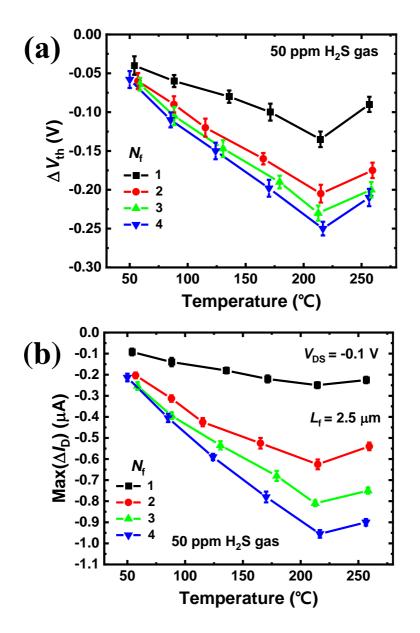


Fig. 5.13. (a) $\Delta V_{\rm th}$ and (b) Max($\Delta I_{\rm D}$) versus T as a parameter of the $N_{\rm f}$ of the fabricated HFGFET-type gas sensors when 50 ppm H₂S is injected for 10 min.

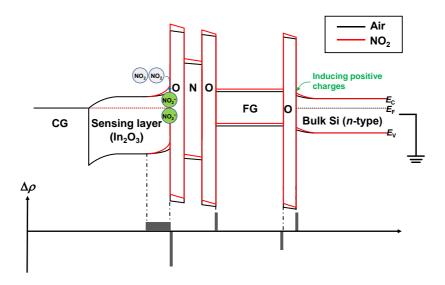


Fig. 5.14. Energy band diagram of the fabricated HFGFET-type gas sensor when the atmosphere ambience is air and NO₂. $\Delta \rho$ is additionally introduced below.

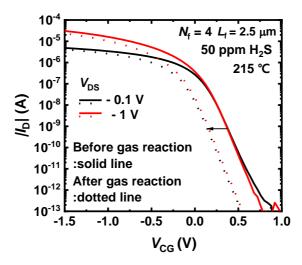


Fig. 5.15. I_D - V_{CG} curves of the fabricated HFGFET-type gas sensors before and after the 50 ppm H₂S injection at 215 °C for 10 min.

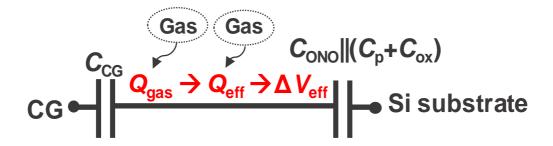


Fig. 5.16. Simplified equivalent circuit of the fabricated HFGFET-type gas sensor during the gas reaction.

Because the HFGFET-type gas sensors in the platform use the same sensing material, the response between the sensing layer and the target gas is the same. The $Q_{\rm eff}$ s of sensors with various sensing material area sizes at the same size of the FET channel are variable, even though the quantity of gas molecules adsorbed onto the sensing layer per unit area is the same. The aforementioned gas detecting techniques and the antenna effect in the sensors were validated using the TCAD device simulation. The $Q_{\rm gas}$ was modeled as a negative sheet charge ($\rho_{\rm sheet}$) produced at the interface between the sensing layer and the O/N/O layer that covered the FG. Because they are closer to the O/N/O layer, adsorbed ions have a considerable

impact on the ΔV_{th} . Ions produced in the sensing layer's bulk region that surpass the Debye length (λ_D) at the interface between the sensing layer and the O/N/O layer have no effect on the FET channel. Adsorbed ions can thus be represented as sheet charges. Fig. 5.17(a) depicts the simulated I_D - V_{CG} curves of HFGFET-type gas sensors with a $N_{\rm f}$ of 3 as a parameter of $\rho_{\rm sheet}$ (= 0 to -2 × 10¹² cm²) at 20 °C. The $L_{\rm f}$ of the sensors was set to 2.5 μ m in this case. As the sheet thickness grows, the ΔV_{th} of the sensor decreases, as do the actual NO₂ gas readings. Fig. 5.17(b) depicts the $\Delta V_{\rm th}$ versus the $\rho_{\rm sheet}$ as a parameter of the sensors' $N_{\rm f}$. At all $\rho_{\rm sheet}$ values, the $\Delta V_{\rm th}$ grows as the $N_{\rm f}$ increases. The growth in $\Delta V_{\rm th}$ looks to be saturated as the $N_{\rm f}$ increases. The calculated $\Delta V_{\rm th}$ agrees well with the measured $\Delta V_{\rm th}$ for all $N_{\rm f}$ s at a ρ_{sheet} of -1.95×10^{12} cm², as shown in Fig. 5.18.

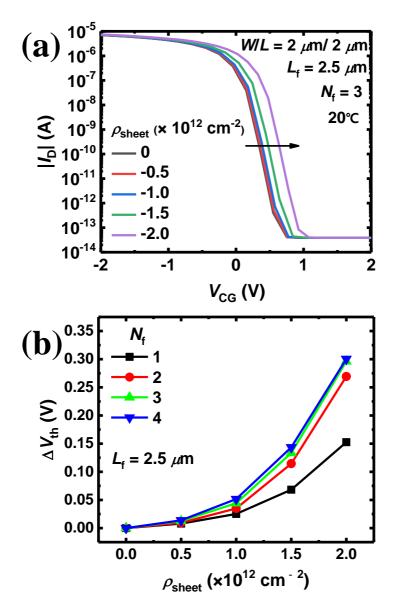


Fig. 5.17. (a) Simulated I_D - V_{CG} curves of the HFGFET-type gas sensor with an N_f of 3 and an L_f of 2.5 μ m as a function of the ρ_{sheet} at 20 °C. (b) ΔV_{th} versus ρ_{sheet} as a function of the N_f [55].

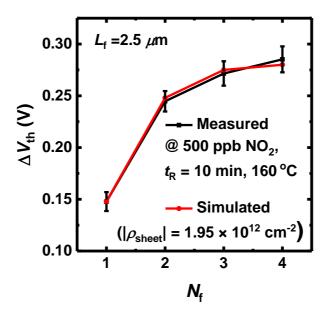


Fig. 5.18. Simulated and measured $\Delta V_{\rm th}$ versus $N_{\rm f}$. The sensors reacted to 500 ppb NO₂ for 10 min at 160 °C, and in the simulation, the $\rho_{\rm sheet}$ was set to -1.95×10^{12} cm⁻² [55].

Figs. 5.19(a) and 5.20(a) show the I_D - V_{CG} curves of the fabricated HFGFET-type gas sensor with an N_f of 4 and an L_f of 2.5 μ m before and after the NO₂ gas reaction at V_{DSS} of -0.1 V and -1 V, respectively. In the linear and saturation regions, the ΔI_D of the sensor can be approximated as following Eq. (23).

$$\Delta I_{\rm D} = \frac{\Delta I_{\rm D}}{\Delta V_{\rm CG}} \times \Delta V_{\rm CG} \approx g_{\rm m} \times \Delta V_{\rm th} \text{ (linear and saturation regions)}$$
 (23)

When the sensor is operating at a $V_{\rm CG}$ that assures a big $g_{\rm m}$, the $\Delta I_{\rm D}$ can be rather significant. The max($\Delta I_{\rm D}$) of the sensors versus the $\Delta V_{\rm th}$ at $V_{\rm DSS}$ of -0.1 V and -1 V are shown in Figs. 5.19(b) and 5.20(b), respectively. Because of the higher $\Delta V_{\rm th}$ and max($g_{\rm m}$), sensors with a high $N_{\rm f}$ have a considerably higher max($\Delta I_{\rm D}$). As shown in Fig. 5.12(b), the max($\Delta I_{\rm D}$)s of sensors with $N_{\rm fS}$ of 1 and 4 at a $V_{\rm DS}$ of -0.1 V are 0.275 μ A and 1.06 μ A, respectively.

The gas response (R) of the sensor in the linear and saturation regions can be defined as following Eqs. (24) and (25).

$$R = 1 + \frac{\Delta I_{\rm D}}{I_{\rm D}} \approx 1 + \frac{\Delta V_{\rm th}}{|V_{\rm CG} - V_{\rm th}|}$$
 (linear region) (24)

$$R = 1 + \frac{\Delta I_{\rm D}}{I_{\rm D}} \approx 1 + \frac{2\Delta V_{\rm th}}{|V_{\rm CG} - V_{\rm th}|}$$
 (saturation region) (25)

The sensor's R in the linear and saturation zones increases as the $\Delta V_{\rm th}$ increases and the $|V_{\rm CG}-V_{\rm th}|$ decreases. Because the $\Delta V_{\rm th}$ grows as the $N_{\rm f}$ of the sensor increases,

increasing $N_{\rm f}$ to have a big R is favorable. By the way, the sensor's max(R) is acquired in the subthreshold zone. The $\log(I_{\rm D})$ - $V_{\rm CG}$ curves of the HFGFET-type gas sensor with a $N_{\rm f}$ of 4 and a $L_{\rm f}$ of 2.5 μ m before and after the NO₂ gas reaction are shown in Fig. 5.21(a). The R of the sensor in the subthreshold region may be estimated using these two curves as follows:

$$\log(R) = \frac{\Delta \log(I_{\rm D})}{\Delta V_{\rm CG}} \times \Delta V_{\rm CG} \approx \frac{d \log(I_{\rm D})}{d V_{\rm CG}} \times \Delta V_{\rm th} = \frac{\Delta V_{\rm th}}{SS}$$
 (26)

$$SS = \frac{d\log(I_{\rm D})}{dV_{\rm CG}}$$
 (subthreshold region) (27)

The max(R) versus $\Delta V_{\rm th}$ of the four sensors is shown in Fig. 5.21(b). At the same $\Delta V_{\rm th}$, the max(R) grows as the $N_{\rm f}$ of the sensor increases. The slopes of the curves in Fig. 5.21(b) correspond to the sensors' 1/SS. The following Eq. (28) can be used to estimate max(R).

$$\max(R) \approx 10^{(\Delta V_{\text{th}}/SS)} \tag{28}$$

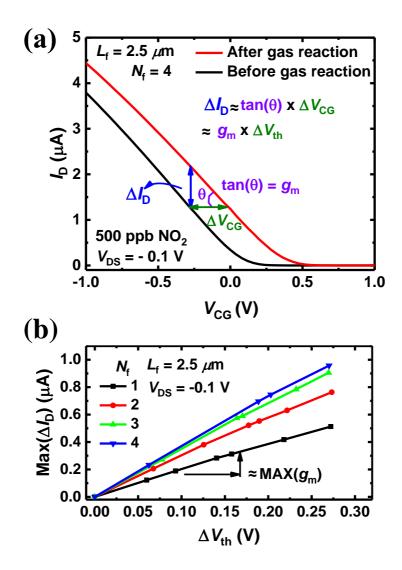


Fig. 5.19. (a) I_D - V_{CG} curves of the fabricated HFGFET-type gas sensors with an N_f of 4 and an L_f of 2.5 μ m before and after the NO₂ gas reaction at a V_{DS} of -0.1 V (in the linear region). (b) max(ΔI_D) versus ΔV_{th} of the sensors [55].

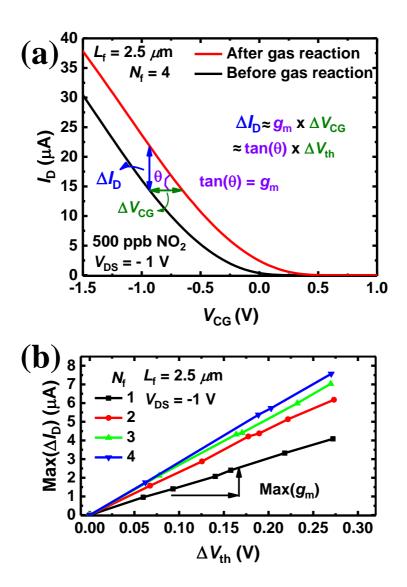


Fig. 5.20. (a) I_D - V_{CG} curves of the fabricated HFGFET-type gas sensors with an N_f of 4 and an L_f of 2.5 μ m before and after the NO₂ gas reaction at a V_{DS} of -1 V (in the saturation region). (b) max(ΔI_D) versus ΔV_{th} of the sensors.

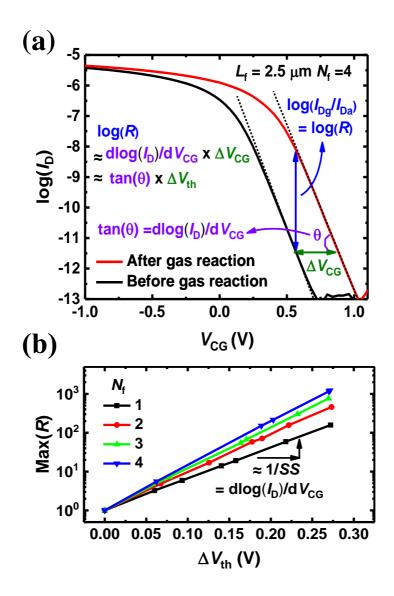


Fig. 5.21. (a) $\log(I_{\rm D})$ - $V_{\rm CG}$ curves of the fabricated HFGFET-type gas sensors with an $N_{\rm f}$ of 4 and an $L_{\rm f}$ of 2.5 $\mu{\rm m}$ before and after the NO₂ gas reaction (in the subthreshold region). (b) $\max(R)$ versus $\Delta V_{\rm th}$ of the sensors.

Sensors with a high $N_{\rm f}$ can have a substantially greater R because to their bigger $\Delta V_{\rm th}$ and lower SS. When the sensors are subjected to 500 ppb NO₂ gas for 10 minutes at 160 °C, the $\Delta V_{\rm th}$ s of a sensor with $N_{\rm f}$ s of 1 and 4 are 0.149 and 0.285, respectively, and the max(R)s of the two sensors are 14.9 and 1533.6. Although the $\Delta V_{\rm th}$ of the two sensors differs by 1.91 times, the log(max(R)) and max(R) of the two sensors differ by 2.71 times and 102.9 times, respectively, due to the difference in 1/SS.

The max(ΔI_D) of the four sensors is shown against the NO₂ gas concentration in Fig. 5.22(a). In all observed gas concentration ranges, sensors with a higher N_f have a higher max(ΔI_D). The max(ΔI_D)/gas concentration increases as the N_f of the sensor increases, as illustrated in Fig. 5.22(b). Figure 5.23(a) depicts the max(R)s of the four sensors as the NO₂ gas concentration varies. The slope of the log(max(R))-log(gas concentration) curve grows as the N_f of the sensor increases, as illustrated in Fig. 5.23(b). Sensors with a higher N_f have a steeper slope since they have a higher γ and a lower SS. The higher the sensitivity, the larger the detecting material area of the sensor.

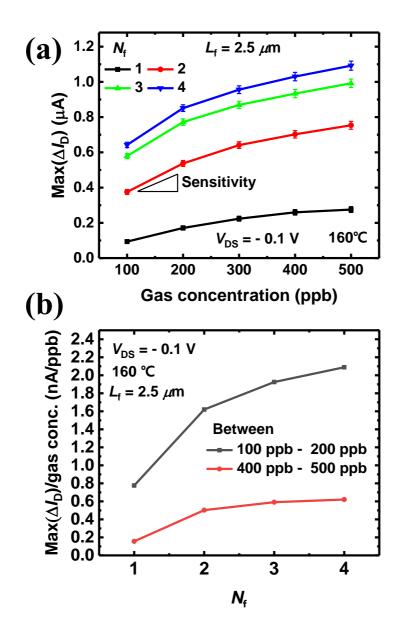


Fig. 5.22. (a) $\max(\Delta I_{\rm D})$ versus NO₂ gas concentration as a parameter of the $N_{\rm f}$ of the HFGFET-type gas sensors. (b) $\max(\Delta I_{\rm D})$ /gas concentration of the sensors.

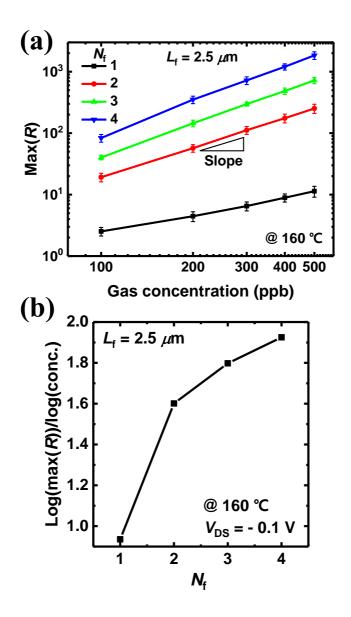


Fig. 5.23. (a) $\max(R)$ versus NO₂ gas concentration as a parameter of the $N_{\rm f}$ of the HFGFET-type gas sensors. (b) $\log(\max(R))/\log({\rm gas\ concentration})$ of the sensors.

The effect of FET channel design (W and L) on the sensitivity of the HFGFET-type gas sensor was further explored. Sensors with varying W and L were created and manufactured, with the N_f and L_f of the sensors set to 3 and 2.5 μ m, respectively. As the WL of the sensor drops, the C_{ox} decreases and the γ increases (Eq. (10) and Fig. 5.24(a)). The ΔV_{th} increases when the WL drops and the γ increases (Figs. 5.24(b) and 5.25(a)). It should be noted that the ΔV_{th} behaves similarly in the linear and saturation zones. The sensor's gm and max(ΔI_D) rise with increasing $\gamma W/L$ and $\gamma^2 W/L$, respectively (Figs. 5.24(c)-(d) and 5.25(b)-(c)). The SS reduces as the γ increases (Eq. (18)), therefore the SS lowers when the WL drops (Fig. 5.24(e)). As a result, as the WL drops, the max(R) ($\approx 10^{(\Delta V th/SS)}$) increases (Fig. 5.24(f)).

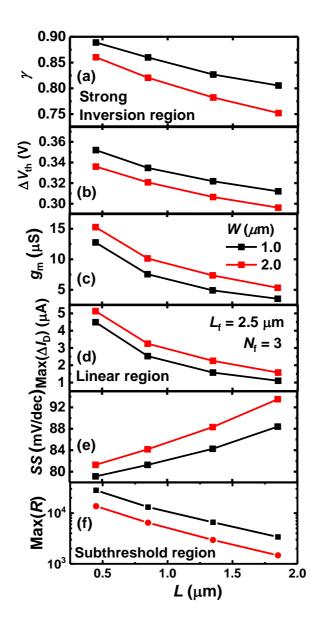


Fig. 5.24. (a) γ , (b) $\Delta V_{\rm th}$, (c) $g_{\rm m}$, (d) $\max(\Delta I_{\rm D})$, (e) SS, and (f) $\max(R)$ of the HFGFET-type gas sensors with different combinations of the W and L at a $V_{\rm DS}$ of -0.1 V. The $\max(R)$ is obtained in the subthreshold region.

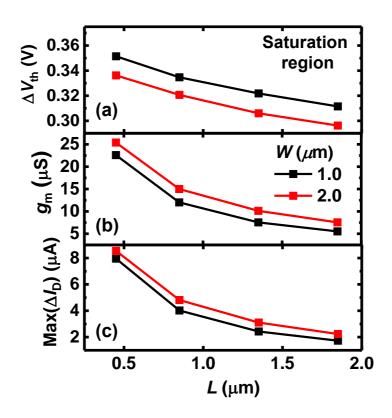


Fig. 5.25. (a) ΔV_{th} , (b) g_{m} , and (c) $\max(\Delta I_{\text{D}})$ of the HFGFET-type gas sensors with different combinations of the W and L at a V_{DS} of -1 V.

5.4 Design optimization

5.4.1 Sensing material area

The HFGFET-type gas sensors with various sensing material area designs were examined in terms of device features, sensitivity, and power consumption. Different $N_{\rm fS}$ (1, 2, 3, and 4) and $L_{\rm fS}$ (2.5, 5.5, and 12 μ m) sensors were used. The W/L of the used sensors is 2 μ m/2 μ m in this case. The $L_{\rm f}$ was not designed to be less than 2.5 μ m in order to interdigitate the CG and FG. As the $N_{\rm f}$ and $L_{\rm f}$ grow, so do the γ and ΔV_{th} (Fig. 5.26(a) and (b)). The g_{m} and SS both grow and decrease as the increases (Figs. 5.26(c)-(d) and 5.27(a)). As the sensing material area grows, so do the $\Delta V_{\rm th}$ and $g_{\rm m}$, and therefore the $\Delta I_{\rm D}$ in the linear and saturation zones (Figs. 5.26(e), 5.27(b), and Eq. (22)). As the N_f and L_f increase, the R in the linear and saturation regions increases as well (Eqs. (24) and (25)). As N_f and L_f increase, so does R in the subthreshold region (Fig. 5.26(f)). However, as N_f and L_f increase, so does power consumption (Fig. 5.28(a)). The size of the sensor material area influences the sensitivity and power consumption. As a result, the sensing material area must be designed with both of these factors in mind. It has the maximum value in the linear and saturation zones when the $N_{\rm f}$ and $L_{\rm f}$ are 3 and 2.5 μ m, respectively (Figs. 5.27(c) and 5.28(b)). The $\Delta V_{\rm th}$ /power, on the other hand, is greatest when the $N_{\rm f}$ and $L_{\rm f}$ are 1 and 12 μ m, respectively (Fig. 5.28(c)). In the subthreshold area, the max(R)/power has the greatest value when the $N_{\rm f}$ and $L_{\rm f}$ are 3 or 4 and 12 μ m, respectively (Fig. 5.28(d)).

The energy consumption was added here as a measure of sensor performance. The $\Delta I_{\rm D}$ of the manufactured HFGFET-type gas sensors with different $N_{\rm f}$ s with five different NO₂ gas concentrations (100, 200, 300, 400, and 500 ppb) at the same reference current (100 nA) is shown in Fig. 5.29. When the $\Delta I_{\rm D}$ becomes gas detectable, the gas detection time ($t_{\rm gd}$) necessary for detecting the target gas is specified ($\Delta I_{\rm gd}$). The $\Delta I_{\rm gd}$ was calculated using the signal-to-noise ratio (SNR):

$$\Delta I_{\rm gd} = \int_0^{t_{\rm gd}} \frac{dI_{\rm D}}{dt} dt \approx \frac{\Delta I_{\rm D}}{\Delta t} \times t_{\rm gd} = c \times \delta I_{\rm D}$$
 (29)

$$SNR = \frac{\Delta I_{gd}}{\delta I_{D}} = c \tag{30}$$

where the δI_D and c denote the noise of the sensor and the target SNR for detecting the target gas. The $\Delta I_{\rm gd}$ was reduced to $\Delta I_{\rm D}/\Delta t \times t_{\rm gd}$ since the $\Delta I_{\rm D}$ grows linearly with time during the first gas reaction (Fig. 5.30(a)). The Igd and c values were set to 10 nA and 100, respectively. At a $|I_D|$ of 100 nA, the sensor's normalized noise spectral density $(S_{\rm ID}/I_{\rm D}^2)$ equates to $10^{-6}/{\rm Hz}$, resulting in 100 pA of noise. As a result, when the $\Delta I_{\rm gd}$ is set to 10 nA, the SNR increases to 100, which is substantially higher than the limit of detection (LOD) of 3 [61]. The noise of the produced HFGFET-type gas sensors is determined by the FET channel size rather than the sensing material area [62]. As a result, the $\Delta I_{\rm gd}$ of the sensors with varied sensing material regions is set to the same value. The $t_{\rm gd}$ s and energy consumption of the four sensors were determined when the NO₂ gas concentration varied (Fig. 5.30(b)). By multiplying the power by the $t_{\rm gd}$, the energy used for target gas detection may be estimated.

Energy = Power
$$\times t_{\rm gd} \propto \frac{\text{Power}}{\text{SNR}}$$
 (31)

$$t_{\rm gd} = \frac{\Delta I_{\rm gd}}{\Delta I_{\rm D}/\Delta t} = \frac{c\delta I_{\rm D}}{\Delta I_{\rm D}/\Delta t} \propto \frac{c\delta I_{\rm D}}{\Delta I_{\rm D}} = \frac{c}{\rm SNR}$$
(32)

The four gas sensors' $t_{\rm gd}$, power consumption, and energy consumption were compared, as shown in Fig. 5.31. As the $N_{\rm f}$ of the sensor grows, there is a trade-off between increased power consumption and reducing $t_{\rm gd}$. The ideal $N_{\rm f}$ may be calculated by taking into account the energy consumption related with both power consumption and $t_{\rm gd}$. The energy consumption of the sensor with a $N_{\rm f}$ of 3 is smaller than that of the sensors with other $N_{\rm f}$ s for a particular NO₂ gas concentration range, a $L_{\rm f}$ of 2.5 μ m, and a W/L of 2 μ m/2 μ m, as shown in Fig. 5.31.

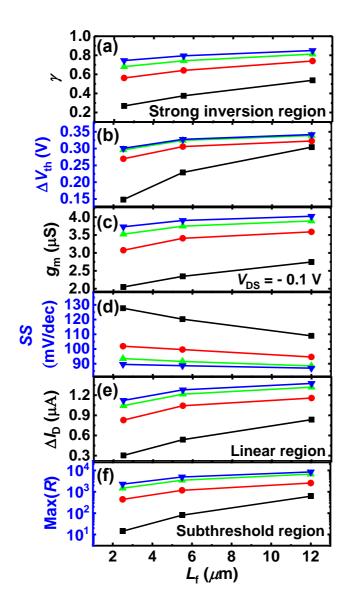


Fig. 5.26. (a) γ , (b) ΔV_{th} , (c) g_{m} , (d) SS, (e) ΔI_{D} , and (f) max(R) of the HFGFET-type gas sensors with the different N_{fS} (1, 2, 3, and 4) and L_{fS} (2.5, 5.5, and 12 μ m) [55].

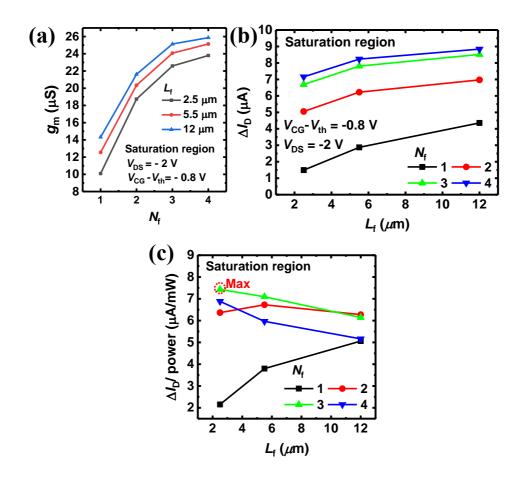


Fig. 5.27. (a) $g_{\rm m}$ versus $N_{\rm f}$ as a parameter of the $L_{\rm f}$ in the saturation region of the HFGFET-type gas sensors. (b) $\Delta I_{\rm D}$ versus $L_{\rm f}$ as a parameter of the $N_{\rm f}$ in the saturation region of the sensors. (c) $\Delta I_{\rm D}$ /power versus $L_{\rm f}$ as a parameter of the $N_{\rm f}$ in the saturation region of the sensors.

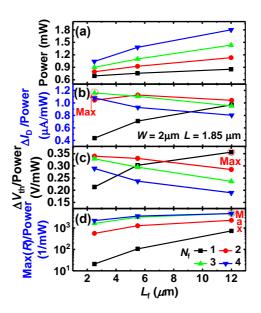


Fig. 5.28. (a) Power, (b) ΔI_D /power, (c) ΔV_{th} /power, and (d) max(R)/power of the HFGFET-type gas sensors with the different N_{fS} and L_{fS} .

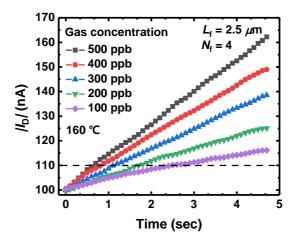


Fig. 5.29. $\Delta I_{\rm D}$ of the fabricated HFGFET-type gas sensors having the different $N_{\rm f}$ s with five different NO₂ gas concentration (100-500 ppb) at 160 °C.

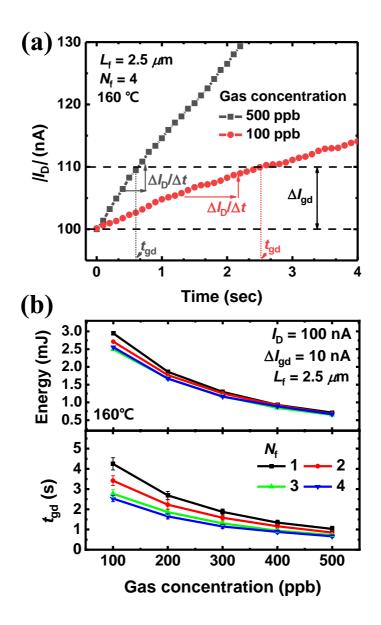


Fig. 5.30. (a) Transient I_D of the fabricated HFGFET-type gas sensor having the different $N_{\rm f}$ s with 100 ppb and 500 ppb NO₂ at 160 °C. (b) Energy consumption and $t_{\rm gd}$ versus NO₂ gas concentration at 160 °C.

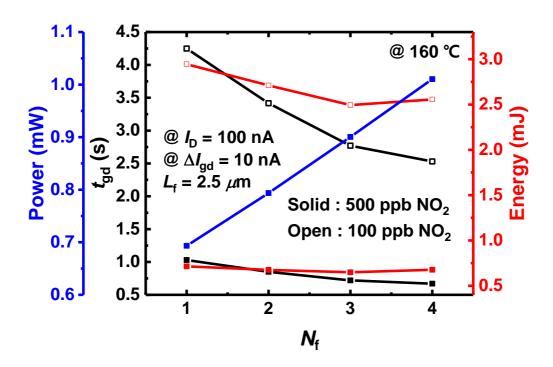


Fig. 5.31. $t_{\rm gd}$, energy consumption, and power consumption of the fabricated HFGFET-type gas sensors having the different $N_{\rm f}$ s at 160 °C.

5.4.2 FET channel

In Chapter 5.4.1, The ΔI_D /power of HFGFET-type gas sensors was studied with both the W and L fixed to 2 μ m. The sensor had the highest ΔI_D /power ratio, with a N_f of 3 and a L_f of 2.5 μ m in both the linear and saturation areas. In this part, the FET channel (W and L) condition that maximizes ΔI_D /power while keeping the N_f and L_f fixed at 3 and 2.5 μ m was explored. As the sensor's W and L decline, the C_{ox} decreases and the γ increases (Eq. (10) and Fig. 5.32(a)). Using the γ values obtained from the sensors having the different W and L, the γ of the sensor with a N_f of 3 and a L_f of 2.5 μ m in the strong inversion may be calculated using Eq. (10) as follows (33). (Fig. 5.32(a)).

$$\gamma \approx \frac{11.32}{12.78 + WL} \tag{33}$$

The ΔV_{th} can be approximated by fitting the ΔV_{th} values of the sensors to Eq. (22) as following Eq. (34) (Fig. 5.32(b)).

$$\Delta V_{\rm th} \approx \frac{5.98}{17.13 + WL} \tag{34}$$

Here, the $Q_{\rm gas}$, $C_{\rm CG}$, and $C_{\rm p}$ are constant as the size of the sensing material area is fixed. The $\Delta V_{\rm th}$ is increased as the W and L get smaller. On the other hand, the max $(g_{\rm m})$ is increased as the W/L increases (Eqs. (16) and (17)). Since the $\Delta I_{\rm D}$ can be approximated as $g_{\rm m} \times \Delta V_{\rm th}$ (Eq. (23)), the $\Delta I_{\rm D}$ has the following relation to the W and L (Eqs. (35) and (36)).

$$\Delta I_{\rm D} \propto \frac{W}{L(17.13 + WL)(12.78 + WL)}$$
 (linear region) (35)

$$\Delta I_{\rm D} \propto \frac{W}{L(17.13 + WL)(12.78 + WL)^2}$$
 (saturation region) (36)

The ΔI_D and ΔI_D /power are largest at $WL \approx 14.76~\mu\text{m}^2$ in the linear region and $WL \approx 7.02~\mu\text{m}^2$ in the saturation region as shown in Fig. 5.33. For the L, it is recommended to make it as small as possible. Most of the power consumption of the sensor comes from the embedded micro-heater, and the power consumption of the micro-heater is constant regardless of the W and L.

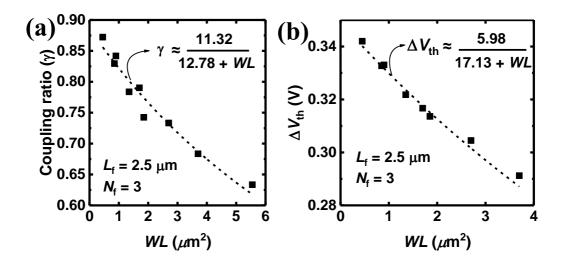


Fig. 5.32. (a) γ versus WL of the fabricated HFGFET-type gas sensors. (b) $\Delta V_{\rm th}$ versus WL of the sensors.

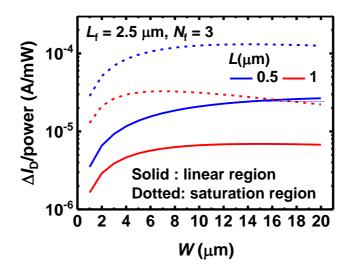


Fig. 5.33. ΔI_D /power versus W as a parameter of the L of the fabricated HFGFET-type gas sensors.

The noise of gas sensors has a substantial impact on the LOD, sensing signal resolution, and SNR. The LFN of FET-type gas sensors, including the HFGFET-type gas sensor, is affected by the FET channel state (W and L). It should be noted that the FET transducer is primarily responsible for the LFN features of the HFGFET-type gas sensor. The $S_{\rm ID}/I_{\rm D}^2$ of the HFGFET-type gas sensors at a W of 1.0 μ m is shown as a parameter of the L in Fig. 5.34(a). The Hooge's mobility fluctuation (HMF) model [63] can explain the LFN properties of p-type buried channel FETs. The HMF model is given as follows:

$$\frac{S_{\rm ID}}{I_{\rm D}^2} = \frac{\alpha_{\rm H}q}{fWLQ_{\rm i}} \tag{37}$$

where the $\alpha_{\rm H}$ and $Q_{\rm i}$ are the Hooge's parameter and inversion charge density. The $S_{\rm ID}/I_{\rm D}^2$ is decreased with increasing the WL as the current fluctuation in the FET channel is averaged by the increase in the total carrier number. Fig. 5.34(b) shows the $S_{\rm ID}/I_{\rm D}^2$ sampled at 10 Hz versus the 1/L as a parameter of the W. The $S_{\rm ID}/I_{\rm D}^2$ is proportional to the 1/WL, which offers an excellent agreement with the Eq. (37).

The SNR in the linear and saturation regions can be defined as follows:

$$SNR = \frac{\Delta I_{\rm D}}{\delta I_{\rm D}} = \frac{\Delta I_{\rm D}}{\sqrt{\int_{f_1}^{f_2} S_{\rm ID}(f) df}} \propto \frac{g_{\rm m} \Delta V_{\rm th}}{I_{\rm D}} \times \sqrt{\frac{WLQ_{\rm i}}{\alpha_{\rm H} q}} \propto \sqrt{WL} \Delta V_{\rm th}$$
(38)

where the f_1 and f_2 are the low and high cutoff f_3 , respectively. In this work, the f_1 and f_2 are 0.1 Hz and 1.6 kHz, respectively.

The $\Delta I_{\rm D}$, $\delta I_{\rm D}$, SNR, max(R), and max(R) × SNR of HFGFET-type gas sensors with different FET channel designs (W and L) were compared [55]. As L increases, both the $\Delta I_{\rm D}$ and $\delta I_{\rm D}$ drop (Fig. 5.35(a) and (b)). However, because the $S_{\rm ID}/I_{\rm D}^2$ decreases as the WL grows, the $\delta I_{\rm D}$ decreases more slowly than the $\Delta I_{\rm D}$ as the L increases. As a result, the greater the W and L, the greater the SNR in the observed range (Fig. 5.35(c)). The SNR rises as the WL rises, but the $I_{\rm D}$ rises as the W/L rises. If the W and L decrease, the γ is raised, and therefore the max(R) increases (Fig. 5.35(d)). The max(R) × SNR increases as W and L decrease (Fig. 5.35(e)). If the SNR is the key performance component, it is preferable to increase the W and L to

a particular amount ($WL \approx 17.13 \ \mu \text{m}^2$). However, if the R is taken into account, it is preferable to keep the W and L minimal.

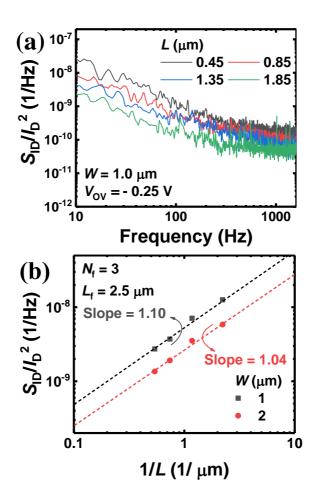


Fig. 5.34. (a) $S_{\rm ID}/I_{\rm D}^2$ of the fabricated HFGFET-type gas sensors with a W of 1.0 μ m as a parameter of the L. (b) $S_{\rm ID}/I_{\rm D}^2$ of the sensors sampled at a 10 Hz versus 1/L as a parameter of the W.

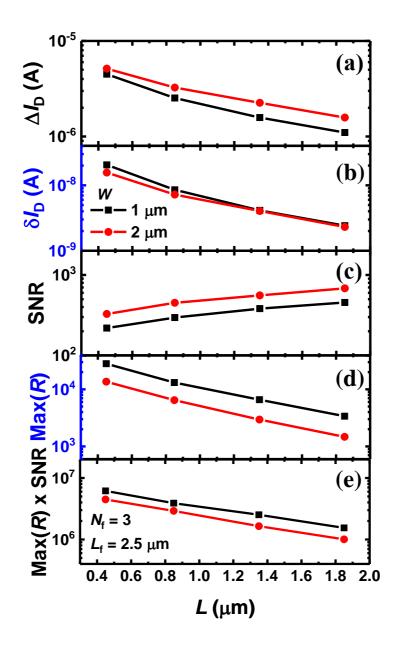


Fig. 5.35. (a) ΔI_D , (b) δI_D , (c) SNR, (d) max(R), and (e) max(R) × SNR of the fabricated HFGFET-type gas sensors with the different FET channel designs [55].

5.4.3 Comprehensive optimization

The design of the HFGFET-type gas sensor can be optimized to maximize various indicators. Design optimization guidelines of the sensor to maximize the ΔI_D /power and SNR/power are provided in this section.

In Chapter 5.4.2, the ΔI_D /power of the HFGFET-type gas sensors was compared by changing either the sensing material area or FET channel. Here, the $\Delta I_{\rm D}$ /power of the sensors with the different sensing material areas is compared by changing the FET channel (W and L) (Fig. 5.36(a)-(c) and Table 5.1). As the W and L get smaller, the area of the sensing material area at which the ΔI_D /power is the largest also gets smaller. When the W/L of the sensor is 4 μ m/3.85 μ m, the $\Delta I_{\rm D}$ /power gets maximum when the $N_{\rm f}$ and $L_{\rm f}$ of the sensor are 3 and 5.5 μ m, respectively. On the other hand, when the W/L of the sensor is 1 μ m/0.85 μ m, the $\Delta I_{\rm D}$ /power gets maximum when the $N_{\rm f}$ and $L_{\rm f}$ of the sensor are 3 and 2.5 μ m, respectively. If the FET channel size (WL) is small (= C_{ox} is small), the γ can be relatively large even if the size of the sensing material area is small (= C_{CG} and $C_{\rm ONO}$ are small) (Eq. (10)). Therefore, the size of the sensing material area that

maximizes the ΔI_D /power can be relatively small. On the other hand, if the WL is large (= $C_{\rm ox}$ is large), the size of the sensing material area needs to be large to have the efficient γ . Therefore, the sensor with a larger WL requires a relatively large sensing material area for a large ΔI_D /power. As a result, the optimal sensing material area varies depending on the FET channel. As the FET channel size increases, the optimal size of the sensing material area is also increased.

Besides, a design guidance for the SNR/power in the HFGFET-type gas sensor is also introduced. The SNR/power in the linear and saturation regions can be expressed as following Eq. (39).

SNR/power
$$\propto \frac{\sqrt{WL}\Delta V_{\rm th}}{\text{power}}$$
 (39)

The $\sqrt{WL}\Delta V_{\rm th}$ /power of the sensors with the different designs is compared in Table 5.2. If the WL is large ($WL \geq 3.7 \ \mu {\rm m}^2$), the sensor has the largest $\sqrt{WL}\Delta V_{\rm th}$ /power when the sensing material area is designed with an $N_{\rm f}$ of 1. Therefore, the design with an $N_{\rm f}$ of 1 is the most efficient structure to increase the $\sqrt{WL}\Delta V_{\rm th}$ /power. To

obtain the optimal WL and L_f for the maximum $\sqrt{WL}\Delta V_{th}$ /power, the measured and simulated ΔV_{th} and power consumption of the sensor with an N_f of 1 is fitted using following Eqs. (40) and (41) (Fig. 5.37(a)-(c)).

power
$$\approx 0.015L_f + 0.67$$
 (40)

$$\Delta V_{\rm th} \approx \frac{0.253L_{\rm f} - 0.260}{L_{\rm f} + 0.2WL - 1.373} \tag{41}$$

Using the Eqs. (40) and (41), the $\sqrt{WL}\Delta V_{th}$ /power of the sensor with an $N_{\rm f}$ of 1 can be expressed as following Eq. (42).

$$\sqrt{WL}\Delta V_{\text{th}}/\text{power} \approx \frac{\sqrt{WL}(0.253L_{\text{f}} - 0.260)}{(L_{\text{f}} + 0.2WL - 1.373)(0.015L_{\text{f}} + 0.67)}$$
 (42)

The $\sqrt{WL}\Delta V_{\rm th}/{\rm power}$ is maximum when the $L_{\rm f}$ and WL are 46 $\mu{\rm m}$ and 223 $\mu{\rm m}^2$, respectively (Fig. 5.38) [55].

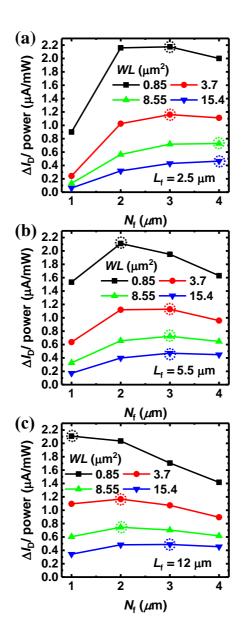


Fig. 5.36. ΔI_D /power of the HFGFET-type gas sensors with the different channel sizes as a function of the $N_{\rm f}$ at (a) $L_{\rm f}$ = 2.5 μ m, (b) $L_{\rm f}$ = 5.5 μ m, and (c) $L_{\rm f}$ = 12 μ m while maintaining the W/L = 1.

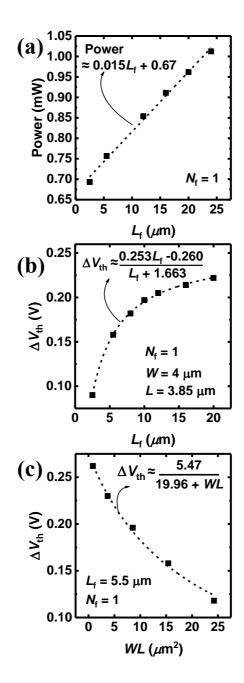


Fig. 5.37. (a) Power consumption versus $L_{\rm f}$ of the HFGFET-type gas sensors. (b)

 ΔV_{th} versus L_{f} of the sensors. (c) ΔV_{th} versus $W\!L$ of the sensors.

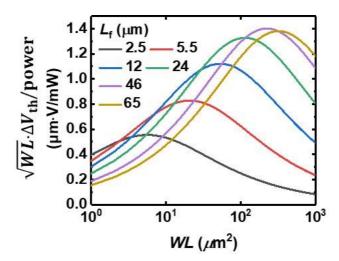


Fig. 5.38. $\sqrt{WL}\Delta V_{\text{th}}$ /power of the HFGFET-type gas sensors with an N_f of 1 versus WL as a parameter of the L_f [55].

As aforementioned, a sensor suitable for a variety of applications can be designed using the relational expression between the design factors (N_f , L_f , W, and L) and the performance factors (SNR, R, power consumption, etc.) [55]. Other performance considerations, such as the sensor size, can be taken into account. As the size of the sensor increases, so does the size of the chip, and therefore the manufacturing cost per chip is increased, so the smaller the size of the sensor is advantageous. As a result, the optimization indicator can be multiplied by, for example, $1/\sqrt[4]{N_f L_f WL}$. Considering the fundamental performance factors such as R,

SNR, power consumption, and sensor size, the generalized optimization indicator can be set as:

Optimization indicator =
$$\frac{R^a \times SNR^b}{power^c \times size^d}$$
 (43)

where a, b, c, and d are weights for R, SNR, power consumption, and sensor size, respectively. By selecting the optimization indicator for implementing the design factors that maximize it, an application-optimized sensor can be generated.

The design optimization suggestions for the HFGFET-type gas sensor described above can be applied to a variety of FET-type gas sensors. Most FET-type gas sensors that use the sensing material as part of the gate [64-66] have a trade-off relationship between the SNR and power consumption based on the size of the sensing material area, and between the sensitivity and noise depending on the size of the FET channel. As a result, even for FET-type gas sensors, it is useful to establish an optimization indication that takes into account numerous performance parameters and build a sensor that can optimize the indicator.

Channel area	$N_{ m f}$ $L_{ m f}$	1	2	3	4
$W = 1 \mu \text{m}$ $L = 0.85 \mu \text{m}$	2.5 μm	0.90	2.14	2.17 (Max)	2.00
	5.5 μm	1.53	2.11	1.95	1.63
	12 μm	1.99	1.92	1.61	1.34
$W = 2 \mu \text{m}$ $L = 0.35 \mu \text{m}$	2.5 μm	1.96	4.37	4.42 (Max)	4.04
	5.5 μm	3.25	4.21	3.91	3.23
	12 μm	4.07	3.82	3.22	2.69
$W = 4 \mu \text{m}$ $L = 0.35 \mu \text{m}$	2.5 μm	2.17	5.63	5.87 (Max)	5.39
	5.5 μm	3.86	5.66	5.33	4.44
	12 μm	5.27	5.24	4.41	3.73
HV 2	2.5 μm	0.437	1.045	1.16 (Max)	1.079
$W = 2 \mu \text{m}$ $L = 1.85 \mu \text{m}$	5.5 μm	0.71	1.127	1.105	0.927
	12 μm	0.96	1.03	0.94	0.80
$W = 4 \mu \text{m}$ $L = 0.85 \mu \text{m}$	2.5 μm	1.00	3.08	3.41 (Max)	3.22
	5.5 μm	2.00	3.32	3.26	2.78
	12 μm	3.09	3.20	2.84	2.42
$W = 3 \mu \text{m}$ $L = 2.85 \mu \text{m}$	2.5 μm	0.13	0.56	0.72	0.73 (Max)
	5.5 μm	0.33	0.66	0.72	0.65
	12 μm	0.57	0.70	0.66	0.58
$W = 4 \mu m$ $L = 3.85 \mu m$	2.5 μm	0.06	0.32	0.43	0.46
	5.5 μm	0.17	0.40	0.47 (Max)	0.45
	12 μm	0.32	0.45	0.46	0.42
$W = 5 \mu \text{m}$ $L = 4.85 \mu \text{m}$	2.5 μm	0.05	0.26	0.40	0.44
	5.5 μm	0.14	0.34	0.46 (Max)	0.45
	12 μm	0.27	0.43	0.46	0.42

Table 5.1. Comparison of the $\Delta I_{\rm D}$ /power of the HFGFET-type gas sensors with the different W, L, $L_{\rm f}$, and $N_{\rm f}$.

Channel area	$N_{ m f}$ $L_{ m f}$	1	2	3	4
$W = 1 \mu \text{m}$ $L = 0.85 \mu \text{m}$	2.5 μm	0.267	0.394	0.366	0.325
	5.5 μm	0.346	0.362	0.317	0.256
	12 μm	0.376	0.307	0.246	0.199
$W = 2 \mu \text{m}$ $L = 1.85 \mu \text{m}$	2.5 μm	0.441	0.680	0.655	0.577
	5.5 μm	0.608	0.664	0.591	0.475
	12 μm	0.714	0.571	0.472	0.381
$W = 3 \mu \text{m}$ $L = 2.85 \mu \text{m}$	2.5 μm	0.511	0.824	0.803	0.721
	5.5 μm	0.777	0.807	0.723	0.589
	12 μm	0.885	0.705	0.569	0.461
$W = 4 \mu \text{m}$ $L = 3.85 \mu \text{m}$	2.5 μm	0.519	0.867	0.853	0.773
	5.5 μm	0.835	0.878	0.807	0.667
	12 μm	0.960 (Max)	0.774	0.647	0.533
$W = 5 \mu \text{m}$ $L = 4.85 \mu \text{m}$	2.5 μm	0.469	0.806	0.833	0.760
	5.5 μm	0.780	0.827	0.809	0.667
	12 μm	0.902	0.778	0.642	0.527

Table 5.2. Comparison of the $(\Delta V_{\rm th} \sqrt{WL})$ /power of the sensors with the different W, L, $L_{\rm f}$, and $N_{\rm f}$.

5.5 Examples of gas sensing

Based on the aforementioned gas sensing characteristics of the HFGFET-type gas sensor, several examples of gas sensing utilizing the sensors that were not previously introduced are covered in this section.

First, carbon monoxide (CO) gas sensing characteristics of the sensors were investigated at 200 °C [49]. Here, the sensing material is pristine In₂O₃ and platinum (Pt)-decorated In₂O₃. Since CO is one of the reducing gases, the I_D-V_{CG} curves of the sensors shifts to the left, resulting in the decrease in the $|I_D|$ in the p-channel sensors. When CO is injected into both the sensors, the gas sensing performances including the sensitivity, and the response and recovery times (t_{res} and t_{rec}) are quite poor in the pristine sensor, but excellent in the Pt-decorated sensor as shown in Fig. 5.39(a). Decorated Pt acts as a kind of reaction catalyst, which plays a role in accelerating the oxygen reduction [67,68], so the gas sensing performance can be improved by the Pt decoration. Fig. 5.39(b) shows the transient CO responses of the sensors as a parameter of the decorated Pt concentration (wt%). The gas sensing performance are improved up to 5 wt%, but rather deteriorate thereafter.

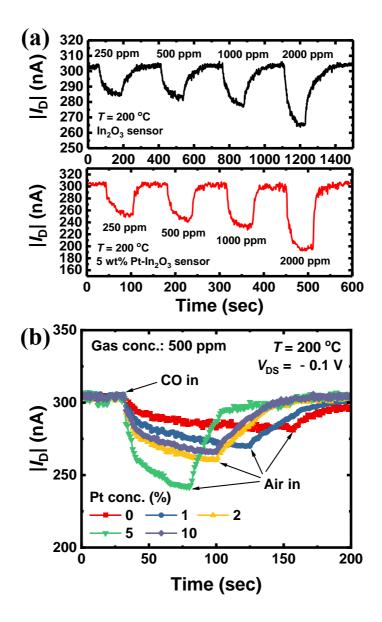


Fig. 5.39. (a) Transient CO (250-2000 ppm) responses of the fabricated pristine In_2O_3 and Pt-decorated In_2O_3 sensors at 200 °C. (b) Transient CO (500 ppm) responses of the sensors as a parameter of the Pt concentration (wt%) at 200 °C [49].

Furthermore, O₂ gas sensing characteristics of the sensors were investigated [48]. Here, the sensing material is Pt-decorated In₂O₃. Since O₂ is one of the oxidizing gases, the I_D - V_{CG} curves of the sensors should shift to the right, resulting in the increase in the $|I_D|$ in the p-channel sensors. However, the $|I_D|$ is decreased at 25 °C, and the $|I_D|$ is increased only after 140 °C when O_2 is injected into the sensor as shown in Fig. 5.40. This is because the physisorption mechanism, which refers to the adsorption of non-polar gas molecules by a kind of physical force (van der Waals force), predominates at low T, and dipoles are generated at the interface between the sensing layer and O/N/O layer as shown in Fig. 5.41. The dipoles shifts the energy band of the FET channel upward in parallel [69], resulting in the decrease in the $|I_D|$. As the T increase, the rotation of the molecules is increased, making it difficult to form the dipoles. Thus, the sensitivity is lowered to 140 °C, and the chemisorption mechanism begins to gradually emerge. The pre-bias ($V_{\rm pre}$) effect can verify the physisorption mechanism in the O₂ sensing. The sensing performance hardly changes regardless of the value of the $V_{\rm pre}$ at 25 °C, but changes as previously reported [47] at 200 °C (Fig. 5.42(a) and (b)).

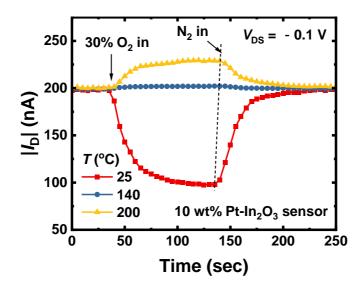


Fig. 5.40. Transient O_2 (30%) responses of the fabricated sensor at 25 °C, 140 °C, and 200 °C [48].

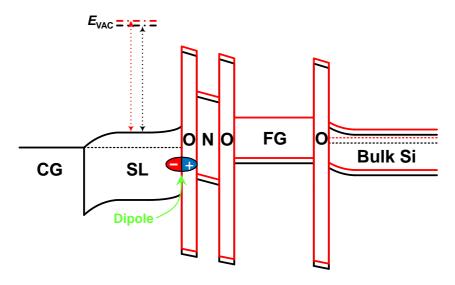


Fig. 5.41. Energy band diagram of the fabricated sensor before (black) and after (red) the O₂ injection.

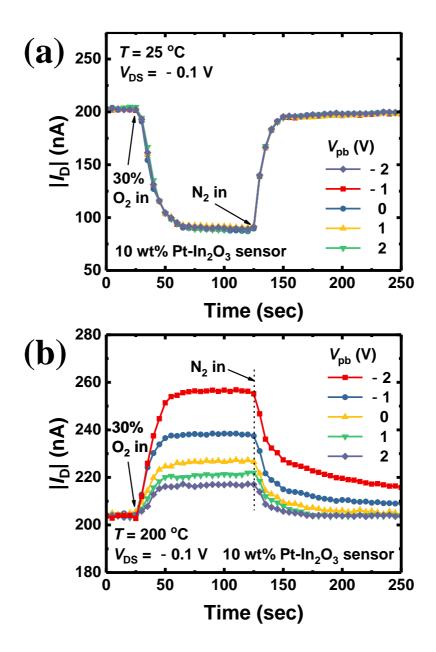


Fig. 5.42. Transient O_2 (30%) responses of the fabricated sensor as a parameter of the $V_{\rm pre}$ at (a) 25 °C and (b) 200 °C [48].

Finally, humidity sensing characteristics of the sensors were investigated [50]. Here, the sensing material is pristine In₂O₃. As expected, as the relative humidity (RH) increases from 17.5% to 68.0%, the $\Delta V_{\rm th}$ and $\Delta I_{\rm D}$ of the sensor are also increased as shown in Fig. 5.43(a) and (b). The adsorption of the H₂O molecules onto the sensing layer depends on the RH level (Fig. 5.44). At low RH, the molecules are chemisorbed onto the sensing layer. The molecules donate electrons to the sensing layer during the adsorption and are positively ionized. In particular, the ionized molecules adsorbed at the interface between the sensing layer and O/N/O layer induce negative charges in the FET channel. Thus, the humidity causes the $V_{\rm th}$ of the sensor to increase negatively as shown in Fig. 5.43(a). As the RH increases, the H₂O molecules are physisorbed onto the chemisorbed molecules through hydrogen bonds. When the RH further increases, multilayer H₂O molecules are adsorbed as shown in Fig. 5.44. The multilayer molecules gradually exhibit the liquid-like behaviors due to the Grotthus chain reaction, which refers to the proton (H₃O⁺) hopping, resulting in inducing dipoles at the interface. The induced dipole also cause the $V_{\rm th}$ of the sensor to increase negatively [69].

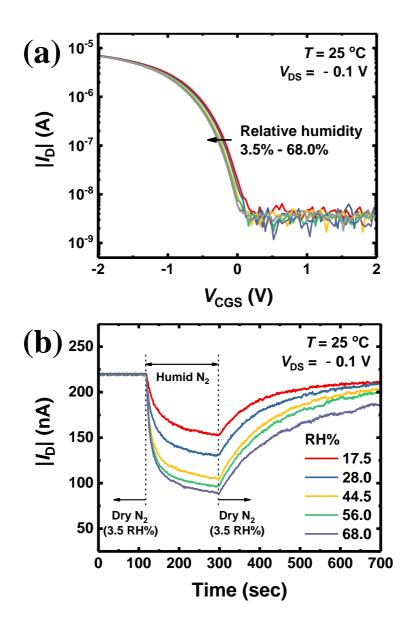


Fig. 5.43. (a) I_D - V_{CG} curves of the fabricated humidity sensor as a parameter of the RH at 25 °C. (b) Transient humidity responses of the sensor as a parameter of the RH at 25 °C [50].

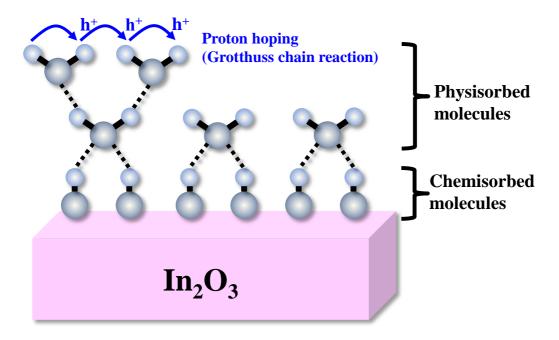


Fig. 5.44. Schematic diagram of the humidity sensing mechanism and adsorption model of the fabricated sensor [50].

Chapter 6

Conclusions

In this dissertation, a gas sensor platform using Si CMOS manufacturing process has been proposed. Various types of gas sensors (ex. HFGFET-type gas sensors, TFT-type gas sensors, and resistive gas sensors), poly-Si gate FETs, flash memories, and CMOS logic devices are integrated onto the same substrate using the same fabrication process. Using the conventional well formation process, both the *n*- and *p*-channel FETs and HFGFET-type gas sensors can be fabricated at the same time, resulting in convenience of CMOS IC process. To fine-tune the threshold voltage of the FETs, the channel implant process simulation is performed using TCAD device simulation tool.

The electrical characteristics of the fabricated CMOS devices including the FETs, flash memories, and CMOS inverters are investigated. The poly-Si gate FETs operate as designed with a high on/off-current ratio (= \sim 10 8) and an infrequent

short-channel effects. The flash memories show good memory functionality and retention characteristics ($> 10^4$ sec) like conventional floating-gate MOSFET memories. The CMOS inverters also exhibit excellent inverting performance with a high voltage gain (> 50).

The electrical and gas sensing characteristics of the fabricated TFT-type and resistive gas sensors are investigated. Both the sensors are designed similarly to the conventional sensors, and to be fabricated onto the same substrate using the same fabrication process with the HFGFET-type gas sensor. The NO₂ and H₂S sensing in the two sensors are carried out, and it is confirmed that the sensors detect the target gases well like the HFGFET-type gas sensor.

Furthermore, the electrical and gas sensing characteristics of the fabricated HFGFET-type gas sensors and the thermal characteristics of the embedded microheaters are investigated. The effect of the HFGFET-type gas sensor design on a variety of performance aspects is explored, and design guidelines for optimizing the HFGFET-type gas sensors are proposed. The device parameter of the sensors, including the threshold voltage, drain current change, gas response, power

consumption, and noise, are evaluated and compared with various designs. Depending on the application, it may be beneficial to create an indicator by combining the gas response, SNR, power consumption, and sensor size, and then optimizing the sensor to maximize the indicator. The proposed optimization guideline is applicable not only to the HFGFET-type gas sensor but also to several FET-type gas sensors. Various examples of gas and humidity sensing in the HFGFET-type gas sensors are also introduced. Thus, it is verified that the sensors detect the target gases well through the measurement results.

The proposed gas sensor platform is very advantageous for mass production because it is manufactured using the standard CMOS manufacturing process. If the sensors, FETs, flash memories, and CMOS ICs in the proposed gas sensor platform are further developed, it is expected to become an promising candidate for a low-power, high-efficiency, ultra-small gas sensor platform, which could be widely utilized in artificial intelligence (AI) technologies such as smart olfactory/taste systems in the future.

Appendix A

Breakdown characteristics of FETs

A.1 Dielectric breakdown

Breakdown characteristics of CMOS FETs are very important information for designing CMOS ICs using various electrical signals. In this section, breakdown characteristics for the gate oxide are introduced. Several junction breakdown characteristics are described in the next section (A.2).

Fig. A.1 shows the measured gate oxide breakdown characteristics of the fabricated n- (solid) and p-channel (dashed) poly-Si gate FETs at room temperature. Here, the measurement was carried out only for the FETs with W/Ls of 2.0 μ m/0.5 μ m (red) and 2.0 μ m/2.0 μ m (blue). The breakdown characteristics were measured by applying the voltage between the gate and body of the FETs ($|V_{\rm GB}| \le 42 \, {\rm V}$). The breakdown voltages (BV) can be extracted as the $|V_{\rm GB}|$ at the point where the gate current ($|I_{\rm G}|$) suddenly increases. In all measured FETs, the BVs were measured to

be between 5 V to 10 V. Note that the gate oxide BV can be modulated by changing the thickness or formation technique of the gate oxide of the FETs.

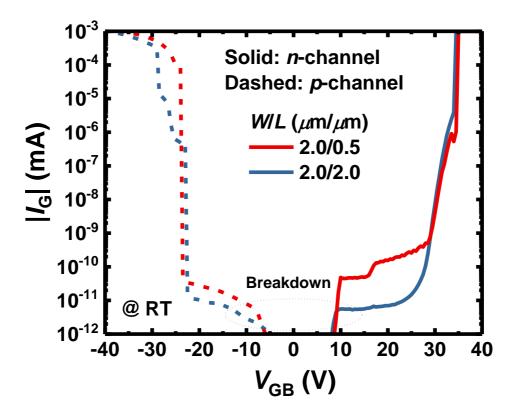


Fig. A.1. Measured gate oxide breakdown characteristics of the fabricated *n*- and *p*-channel poly-Si gate FETs at room temperature.

A.2 Junction breakdown

Several junction breakdown characteristics of the fabricated n- and p-channel poly-Si gate FETs are introduced. Here, the measurement was carried out only for the FETs with W/Ls of 2.0 μ m/0.5 μ m and 2.0 μ m/2.0 μ m.

First, the source/drain-to-body junction breakdown characteristics of the FETs are investigated at room temperature as shown in Fig. A.2. The breakdown characteristics were measured by applying a reverse bias between the body and the source or drain of the FETs ($|V_R| \le 42 \text{ V}$). The junction BVs (JBV) can be extracted as the $|V_R|$ at the point where the reversed diode current ($|I_R|$) suddenly increases. The JBVs were measured to be ~10 V for both the n- and p-channel FETs. Note that the junctions in the p-channel FETs were broken more slowly than in the n-channel FETs thanks to the buried channel implantation applied to the p-channel FETs.

Moreover, the drain-to-source (channel) breakdown characteristics of the FETs are investigated at room temperature as shown in Fig. A.3. The breakdown characteristics were measured by applying the voltage between the drain and source $(|V_{\rm DS}| \le 42~{\rm V})$ while the gate is floated. The drain-to-source breakdown voltages

(BVDSS) can be extracted as the $|V_{\rm DS}|$ at the point where the $|I_{\rm D}|$ suddenly increases. The BVDSSs were measured to be ~20 V for both the n- and p-type short channel ($W/L = 2.0~\mu \text{m}/0.5~\mu \text{m}$) FETs. Note that the long channel FETs did not show the drain-to-source breakdown.

Finally, the well-to-substrate junction breakdown characteristics of the FETs are investigated at room temperature as shown in Fig. A.4. Here, the well and substrate are doped with the n- and p-type dopants, respectively. The breakdown characteristics were measured by applying a reverse bias between the well and substrate of the FETs ($|V_R| \le 42 \text{ V}$). The junction BVs (JBV) can be extracted as the $|V_R|$ at the point where the reversed diode current ($|I_R|$) suddenly increases. The JBVs were not measured within the measurable range ($\le 42 \text{ V}$) for both the n- and p-channel FETs (4 samples).

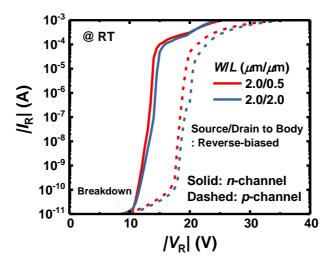


Fig. A.2. Measured source/drain-to-body junction breakdown characteristics of the fabricated *n*- and *p*-channel poly-Si gate FETs at room temperature.

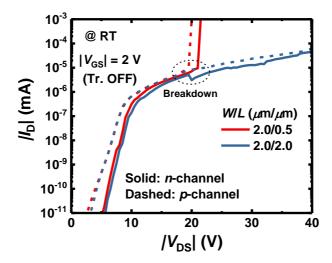


Fig. A.3. Measured drain-to-source (channel) breakdown characteristics of the fabricated *n*- and *p*-channel poly-Si gate FETs at room temperature.

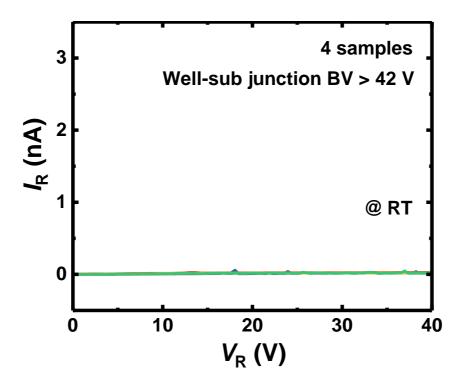


Fig. A.4. Measured well-to-substrate junction breakdown characteristics of the fabricated *n*- and *p*-channel poly-Si gate FETs (4 samples) at room temperature.

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초 록

최근 산업화와 도시화의 진행에 따라, 각종 산업 및 운송수단 등으로부터 배출되는 유해 가스에 의한 실내외 대기오염 문제가 대두되고 있다. 대기 상태를 실시간으로 관찰하기 위해서는 가스 감지 기술의 발전이 필수적이며, 본 기술은 질병 진단 및 식품 신선도 확인의 목적 등다양한 분야에도 널리 활용될 수 있다. 따라서 많은 연구 그룹에서는 광학형, 전기화학형, 반도체형 등의 다양한 종류의 가스 센서에 대해 연구개발을 진행하고 있다. 그 중 반도체형 가스 센서의 일종인 저항형가스 센서는 소자 구조와 공정 과정이 간단하다는 장점 덕분에 가장 많은 연구 결과가 보고되고 있다. 그러나 동작에 필요한 출력 전류를 얻기 위해서는 센서의 면적이 커져야만 한다. 반면, 전계 효과 트랜지스터(FET)기반 가스 센서는 상보형 금속-산화막-반도체 (CMOS) 공정 기술과 호환성이 있으므로, 보다 소형화된 크기로 제작이 가능하며, 곱셈기(MUX), 아날로그-디지털 변환기 (ADC), 이득 조절 증폭기 (PGA)와 같은 CMOS 집적회로와 읽기, 쓰기, 지우기 연산이 가능한 플래시 메모리를 기판 상에 동일 공정을 사용하여 집적할 수 있다.

본 논문에서는 종래의 실리콘 CMOS 공정 기술을 활용한 가스 센서 플랫폼을 제안한다. 제안한 가스 센서 플랫폼은 10장 이하의 포토마스 크만으로 제작이 가능하며, 수평형 플로팅 게이트 구조를 갖는 FET (HFGFET)형, 하단 게이트를 갖는 박막 트랜지스터 (TFT)형, 저항형 가스 센서와 함께 폴리실리콘 게이트 FET 및 플래시 메모리가 집적되어

있는 구조를 갖고 있다. HFGFET형 가스 센서의 감지부 하단에는 마이크로 히터가 형성되어 있어 표적 가스에 해당하는 최적 동작 온도로 감지부를 국소적으로 가열할 수 있고, 플로팅 게이트 MOSFET 구조 덕분에 플래시 메모리 동작이 가능하므로, 동작점 변경을 통한 센서 출력신호 보정 등에 활용될 수 있다. 한편, 같은 기판에 집적된 TFT형과 저항형 가스 센서의 가스 감지 특성에 대해서 조사하였고, 각 센서에 대한 동작 가능성을 검증하였다. 또한, 가스 반응성, 잡음 특성, 소비 전력등을 고려하여 HFGFET형 가스 센서를 비롯한 FET형 가스 센서의 구조를 최적화하는 방법에 대해 제안한다. 감지부 및 변환부의 크기, 모양등의 구조에 따른 전기적 특성을 실제 측정과 티캐드 (TCAD) 소자 시뮬레이션을 사용하여 모델링을 진행하였고, 이를 활용하여 최적화 지표를 설계하였다. 최적화된 HFGFET형 가스 센서의 가스 및 습도 감지 특성에 대해서 이산화질소 (NO2), 황화수소 (H2S) 등의 가스를 사용하여 조사하였고, 본 가스 센서의 감지 기작에 대해서 설명하였다.

제안한 가스 센서 플랫폼은 기판 상에 동일 공정을 사용하여 여러 종류의 가스 센서와 CMOS 소자 및 회로의 집적이 가능하므로, 저가격으로 대량 생산이 가능할 것으로 기대된다. 또한, 제안한 FET형 가스 센서의 구조 최적화 방법은 센서의 감지 특성 개선 및 추후 가스 센서 어레이 설계에 매우 효과적일 것으로 기대된다.

주요어 : FET형 가스 센서, HFGFET형 가스 센서, 가스 센서 플랫폼, CMOS, 구조 최적화, 안테나 효과

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