Ph.D. DISSERTATION

Negative Capacitance Field-Effect Transistors with Stacked Nanosheet Structure

적층 나노시트 구조의 음의 정전용량 전계 효과 트랜지스터

BY

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AUGUST 2022

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING
COLLEGE OF ENGINEERING
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이 논문을 공학박사 학위논문으로 제출함

2022 년 8 월

서울대학교 대학원

전기 · 정보공학부

김 시 현

김시현의 공학박사 학위논문을 인준함

2022 년 8 월

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Abstract

The development of integrated circuit (IC) technology has continued to improve speed and capacity through miniaturization of devices. However, power density is increasing rapidly due to the increasing leakage current as miniaturization advances. Although the remarkable advancement of process technology has allowed complementary-metal-oxide-semiconductor (CMOS) technology to consistently overcome its constraints, the physical limitations of the metal-oxide-semiconductor field-effect transistor (MOSFET) are unmanageable. Accordingly, research on logic device is being divided into a CMOS-extension and a beyond-CMOS. CMOS-extension focuses on the gate-all-around field-effect transistors (GAAFETs) which is a promising architecture for future CMOS thanks to the excellent electrostatic gate controllability. Particularly, nanosheet (NS) architecture with high current drivability required in ICs, is the most promising. However, NS GAAFET has a trade-off relation between the controllability and the drivability, which requires the necessity of a higher-level effective oxide thickness (EOT) scaling for further scaling of NS GAAFET.

On the other hand, beyond-CMOS mainly focuses on developing devices with novel mechanisms to overcome the MOSFETs' physical limits. Among several

candidates, negative capacitance field-effect transistors (NCFETs) with exceptional CMOS compatibility and current drivability are highlighted as future logic devices for low-power, high-performance operation. Although the NCFET utilizing the negative capacitance (NC) effect of a ferroelectric has been demonstrated theoretically by the Landau model, it is challenging to be implemented due to the fact that stabilized NC and sub-thermionic subthreshold swing (*SS*) are incompatible.

In this dissertation, a GAA NCFET that maintains a stable capacitance boosting by NC effect and exhibits high performance is demonstrated. A ferroelectric-antiferroelectric mixed-phase hafnium-zirconium-oxide (HZO) thin film was introduced, whose effect was confirmed by capacitors and FET experiments. Furthermore, the mixed-phase HZO was demonstrated on a stacked nanosheet gate-all-around (stacked NS GAA) structure, the advanced CMOS technology, which exhibits a superior gate controllability as well as a satisfactory drivability for ICs. The hysteresis-free stable NC operation with the superior performance was confirmed in NS GAA NCFET. The improved *SS* and on-current (I_{on}) compared to MOSFETs fabricated in the same manner were validated, and its feasibility as a low-power, high-performance logic device was proven based on a variety of figure of merits.

Keywords: Gate-all-around (GAA), Stacked nanosheet (stacked NS), Negative

capacitance field-effect transistor (NCFET), Ferroelectric, Mixed-phase, Hafnium-zirconium-oxide (HZO).

Student Number: 2014-21698

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Chapter 1

Introduction

1.1 Power and Area Scaling Challenges

In 1965, Gordan Moore reported that the number of transistors in an integrated circuit (IC) chip is doubling every year, as shown in **Figure 1.1**(a) [1]. Although the doubling interval has been extended to 2-years [**Figure 1.1**(b)] [2], the complementary metal oxide semiconductor (CMOS) device has been continuously scaled down, thus increasing the clock speed [3]. In 1974, Robert Dennard proposed a constant field scaling law, and accordingly the design parameters of metal-oxide-semiconductor field-effect transistors (MOSFETs) has been shrunk with the scaling factor [4]. Nonetheless, fundamental physical limits gradually hampered device scaling. As illustrated in **Figure 1.2**(a), the frequency growth trend due to device scaling down

broke down in the middle of the 2000s [3]. Particularly, in the conventional planar MOSFET architecture, the short channel effect (SCE), in which the source/drain junction becomes closer as the gate length increases, hence weakening the channel controllability of the gate, has severely degraded the device properties [5-7]. As depicted in **Figure 1.2**(b), the power density increased rapidly as the device density of integrated circuit (IC) chips increased rapidly, and further scaling of supply voltage (V_{DD}) became challenging as a result of increasing standby power density caused by SCE [8]. It is required to guarantee a sufficient on/off current ratio within a given V_{DD} in order to scale down V_{DD} while increasing performance, which is how CMOS devices have been developed. As indicated in **Figure 1.3** [9], strained silicon (90-nm node) was introduced utilizing SiGe source/drain to enhance the on-current (I_{on}) in planar MOSFETs [10]. The continuous reduction of gate oxide thickness in accordance with Dennard's scaling law has resulted in an increase in gate leakage current, leading to the introduction of a high-κ metal gate (HKMG) in the 45nm node [11]. Due to the low thermal budget of high-κ, the advent of HKMG brought a replacement metal gate process at the same time. Despite these attempts, continued gate length scaling required an ever-increasing degree of gate controllability. Eventually, for further length scaling at the 22-nm node, a multi-gate structure, represented by Fin field-effect transistor (FinFET), has been implemented [6, 12-14]. FinFETs, in which a narrow Fin-shaped channel is covered by a gate, can have better

electrostatic controllability, and are currently being applied to mass manufacturing at nodes as small as sub-5nm [15, 16]. However, from the same perspective, rather than a tri-gate structure, a gate-all-around (GAA) structure in which the gate wraps around the channel in all directions can enhance the gate-controllability ultimately, which is being researched extensively as a platform for the sub-3nm node [17-29].

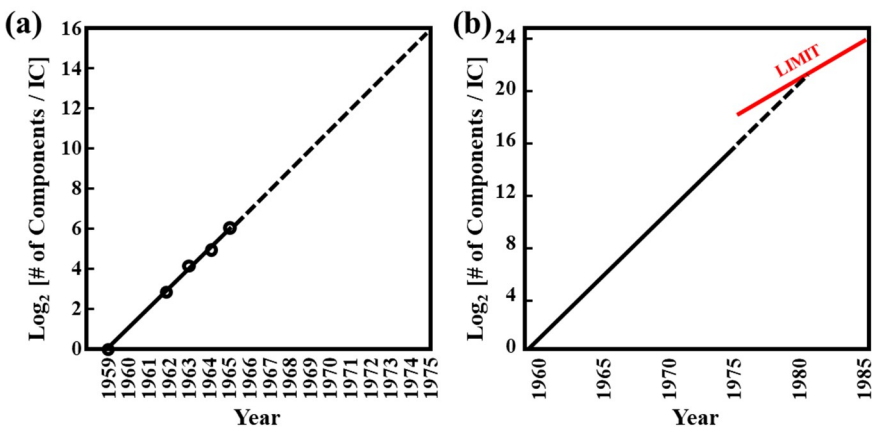


Figure 1.1. Trend lines of the number of components in integrated circuit introduced by Moore: (a) Doubling every year [1] and (b) Doubling interval increased to 2 years [2].

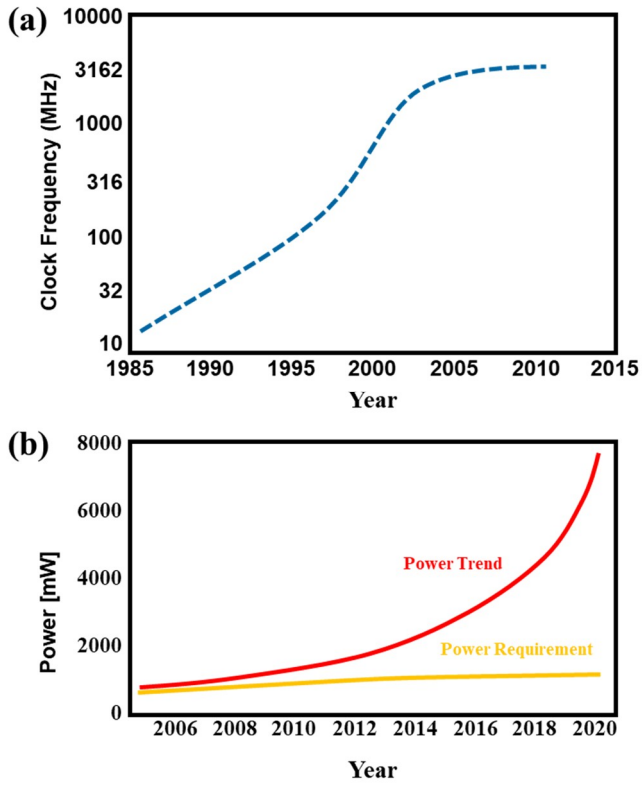


Figure 1.2. (a) Clock frequency [3] and (b) power dissipation trend [8] of logic device.

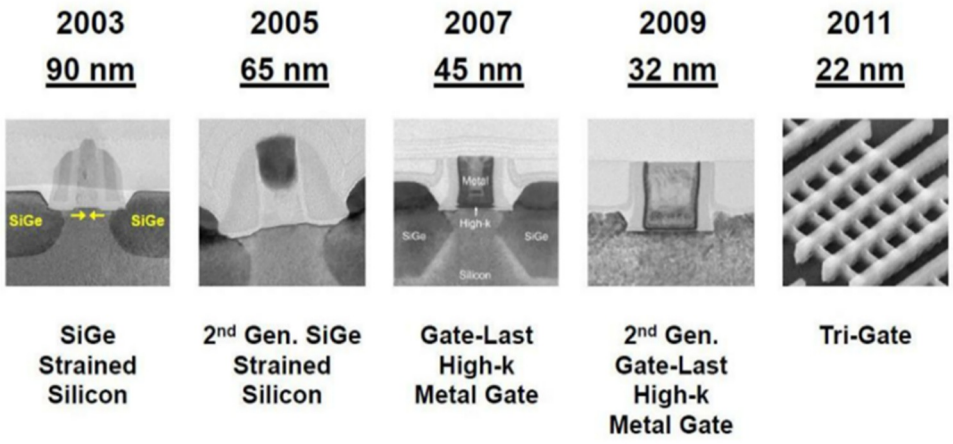


Figure 1.3. Development of CMOS device from planar to 3D Fin structure [9].

1.2 Nanosheet Gate-All-Around FETs

1.2.1 Gate-All-Around FETs

According to international roadmap for devices and systems (IRDS) 2021 (**Figure 1.4**), the trend of CMOS devices is eventually towards gate-all-around MOSFETs (GAAFET) [30]. As depicted in **Figure 1.5**(a), a cylindrical nanowire (NW) structure, where the gate electric field is concentrated to the channel, is optimal for achieving the highest electrostatic controllability [29]. Accordingly, numerous research groups have investigated NW GAAFETs [17-20, 26-28]. IRDS 2018 estimated that vertical-type NW GAAFET would be implemented in the 1.5nm node in 2028. [31]. Although the vertical NW GAA structure offers higher area scaling through pillar-structured channel patterning, due to numerous fabrication issues, notably the difficulty of the self-aligning process [27], the prediction of vertical GAA was eliminated in IRDS 2021 [30]. On the other hand, the NW GAA structure of the horizontal type is regarded desirable due to its compatibility with the existed FinFET process with the exception of the channel release process [17-20].

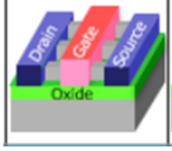
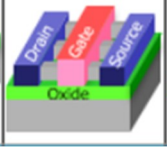
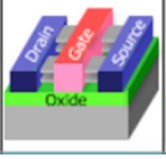
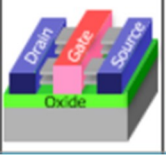
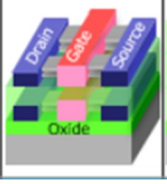
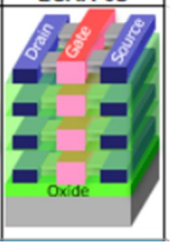
2021	2022	2025	2028	2031	2034
G51M30	G48M24	G45M20	G42M16	G40M16/T2	G38M16/T4
"5"	"3"	"2.1"	"1.5"	"1.0 eq"	"0.7 eq"
i7-f5	i5-f3	i3-f2.1	i2.1-f1.5	i1.5e-f1.0e	i1.0e-f0.7e
FinFET	finFET LGAA	LGAA	LGAA	LGAA-3D	LGAA-3D
finFET	finFET	LGAA	LGAA	LGAA-3D	LGAA-3D
					

Figure 1.4. Device architecture roadmap for future logic devices [30].

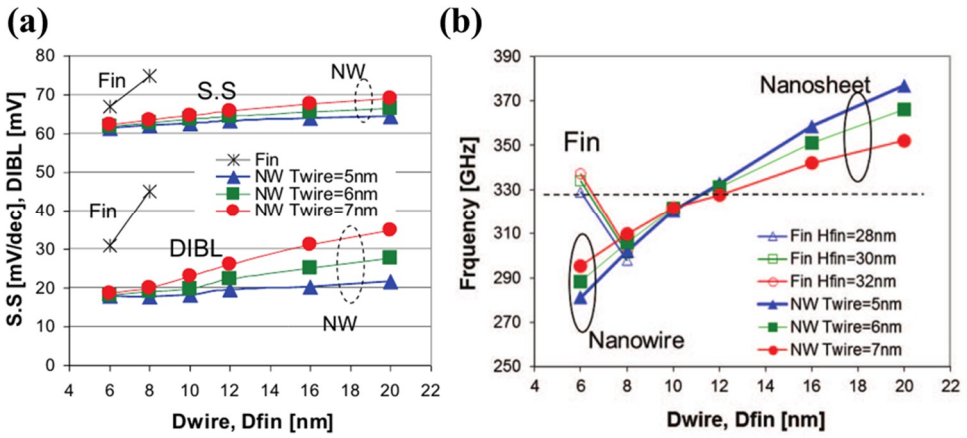


Figure 1.5. (a) Subthreshold swing (*SS*) / drain-induced-barrier-lowering (DIBL) and (b) frequency of GAAFETs according to the nanosheet width [29].

1.2.2 Nanosheet GAAFETs

As can be recognized by the development process of FinFETs evolving toward a higher Fin aspect ratio [32-34], current drivability must be adequately guaranteed in

order to improve device performance. For satisfying the current requirements, there has been a demand for vertically-stacking of horizontal NWs; unfortunately, the performance increase as stacking of NW channels is restricted by the increase in parasitic resistance and capacitance. In addition, as shown in **Figure 1.6**(a), as the aspect ratio of the device increases, the channel width between layers varies due to the etch slope; hence, the current does not increase proportionally to the number of stacked channels [**Figure 1.6**(b)]. Eventually, as a future logic device architecture alternative for FinFET, a vertically-stacked nanosheet (NS) was introduced to achieve sufficient current drivability along with greater gate-controllability [21-25, 29]. **Figure 1.7** compares the effective width (W_{eff}) of aggressively scaled FinFETs and various types of NS GAAFETs [21], which claims that a single stacked NS structure is considered to obtain the largest current drivability in a limited active width.

In CPU blocks, circuit components with various performances are required, which are co-integrated on one wafer. The requirement is satisfied by the tuning of current drivability, implemented by the number of Fin in FinFET technology. However, the multiple Fin scheme has disadvantages; firstly, it can only achieve discrete current quantity fundamentally, and secondly, the increase of cell area is unavoidable due to the constant Fin pitch. In the case of NS GAAFETs, on the other hand, continuous current drivability can be provided by patterning the NS width as required.

Although there are numerous challenges, such as parasitic resistance and capacitance issues, as well as process difficulties, in terms of electrostatic controllability and current drivability, a vertically-stacked horizontal NS GAAFET is considered to be the most optimal device for the structure of the next-generation CMOS device. However, as illustrated in **Figure 1.8** [also in **Figure 1.5**(a)], the gate controllability is fairly deteriorated as increasing W_{NS}; that is, electrostatic controllability and the current drivability is trade-off relation. Therefore, for the nanosheet technology to be applied to the future logic device moving toward further length scaling, a higher-level of EOT engineering is necessary.

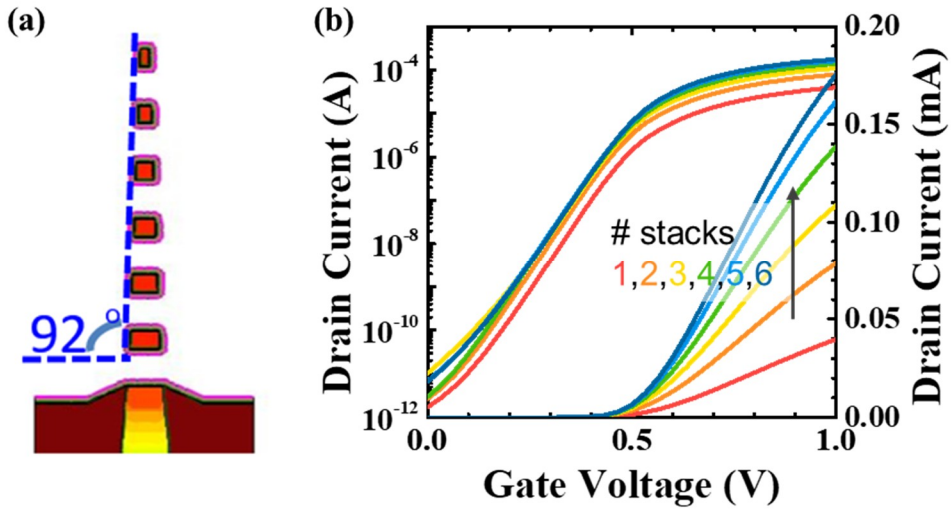


Figure 1.6. (a) Schematic image of simulated stacked-GAAFET. (b) Simulated current characteristics according to the number of stacked channels.

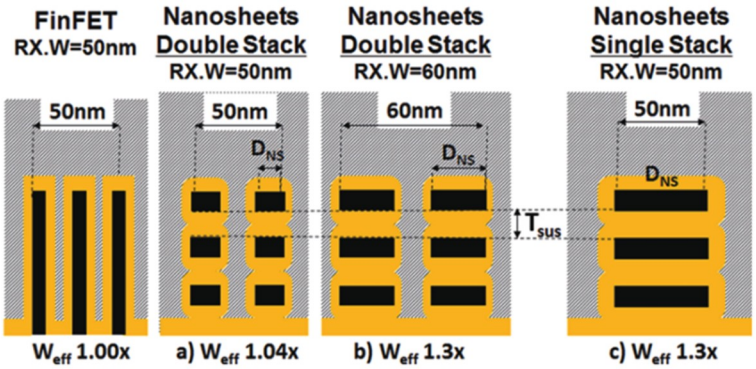


Figure 1.7. Optimum GAA structure for high current drivability (~W_{eff}) considering the active width (*RX. W*) [21].

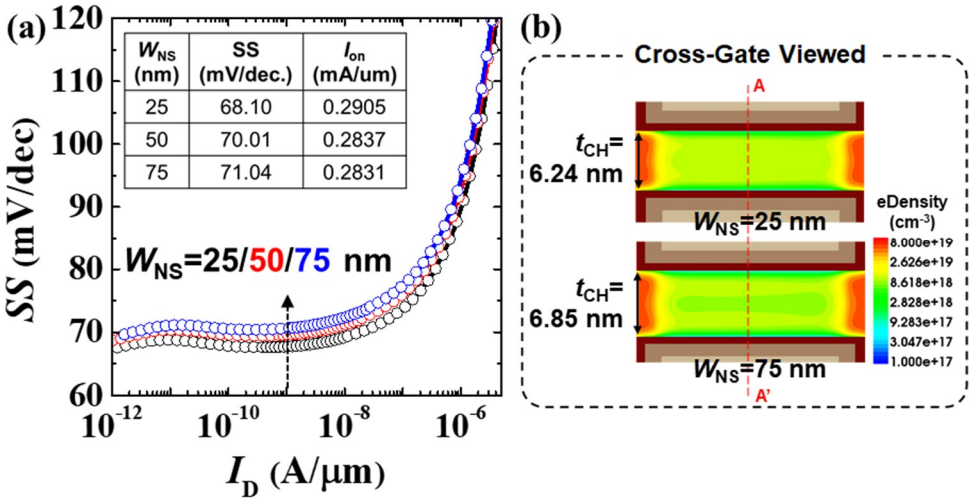


Figure 1.8. (a) *SS*-I_D of NS GAAFET with regard to nanosheet width (W_{NS}). (b) Electron density along the channel of NS GAAFET w/ W_{NS} = 25 and 75 nm.

1.3 Negative Capacitance FETs

1.3.1 Negative Capacitance in Ferroelectric Materials

In 1976, Rolf Landauer reported that the capacitance of ferroelectric materials can be negative [35]. Ferroelectric materials have spontaneous polarization due to their non-centrosymmetric crystal structure, which maintains a permanent dipole even in the absence of an electric field. His theory is based on the thermodynamic Landau model [36-38], where the ferroelectric free-energy (F) is expressed as follows.

$$F / t_{\mathrm{F}} = \alpha P^2 + \beta P^4 + \gamma P^6 - E_{\mathrm{F}} P \qquad 1.1$$

where t_{F}, E_{F} and P represent thickness, electric field and polarization of ferroelectric material. The relationship between the ferroelectric electric field and polarization can be established In Equation 1.1, by determining the point at which the value of the derivative of F with respect to P becomes zero (stable point).

$$E_{\mathrm{F}} = 2\alpha P + 4\beta P^3 + 6\gamma P^5, \text{ when } \frac{\partial F}{\partial P} = 0 \qquad 1.2$$

Figure 1.9(a) illustrates the free-energy landscape as a function of polarization for a ferroelectric material according to the Landau model (Equation 1.1) [39]. It has a double well shape, where the two stable energy states mean polarization up and down, respectively. **Figure 1.9**(b) depicts the ferroelectric *P-E* curve (Equation 1.2)

calculated by differentiating the free-energy with respect to polarization, also known as the Landau S-curve [39]. The spontaneous polarization is either positive or negative (or 0) at $E = 0$ and polarization switching occurs in an electric field above the coercive electric field (E_C), which indicates that the charge in the energy well surpasses the energy barrier shown in the **Figure 1.9**(a). Remarkably, an unstable region with a negative curvature between the two energy wells exists, which implies negative capacitance (NC) region: the region with a negative slope in the S-curve since the capacitance is proportional to dP/dE [40].

In the past, researches on ferroelectricity in perovskite-structured materials such as BaTiO [41, 42], PZT [43, 44], and polymer-based materials [45, 46] were predominantly reported. Since the discovery of ferroelectricity in CMOS-friendly and thickness-scalable HfO in 2011 [47], a significant amount of research has been undertaken on nonvolatile memory [48-52] and NC transistors [53-65] utilizing HfO-based ferroelectric material. The ferroelectricity of HfO stems from a non-centrosymmetric polycrystal phase [66, 67]. **Figure 1.10** explains the polycrystal phase transition of HfO, exhibiting ferroelectricity in the intermediate orthorhombic phase (o-phase) [68]. The crystal phase transition of HfO is induced by heat and stress and is promoted with the help of dopants such as Si, Al, and Zr. Among the different doped-HfO materials, Zr-doped HfO (HZO) has been attracting attention since its o-phase crystallize temperature is relatively (~500°C) [69] as well as the ferroelectricity

has been reported at an extremely scaled thickness of ~1 nm [70].

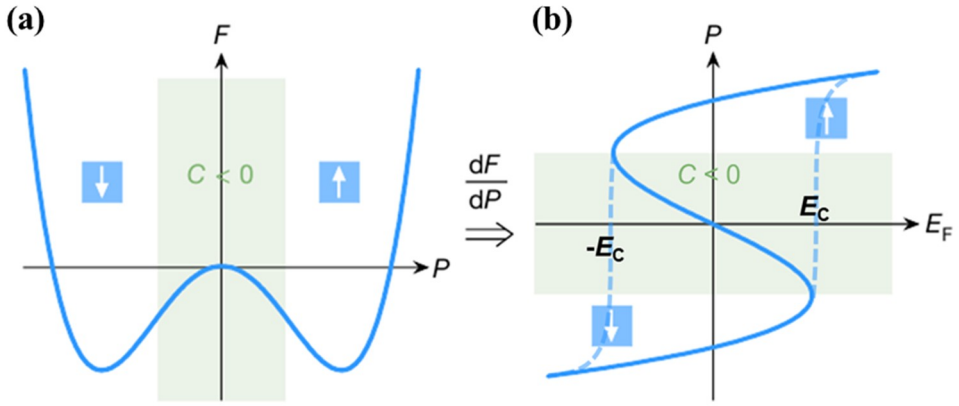


Figure 1.9. (a) Double-well free-energy landscape and (b) Polarization (*P*) - electric field (*E*) relationship of ferroelectric material [40].

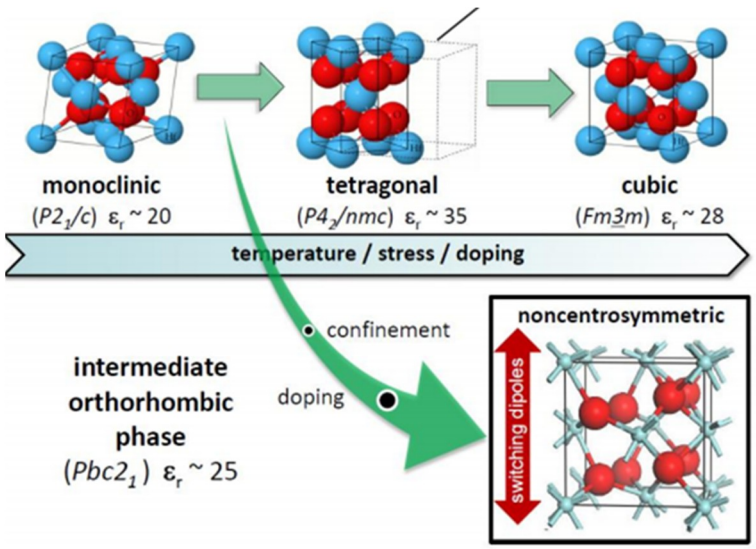


Figure 1.10. Non-centrosymmetric intermediate phase (orthorhombic phase) of polycrystalline HfO for ferroelectricity [68].

1.3.2 Negative Capacitance for Steep Switching Devices

The aforementioned NC effect of ferroelectric materials has the potential to overcome the limits of MOSFETs when used to CMOS technology. The subthreshold swing (*SS*) of a MOSFET is defined as the amount of gate voltage (V_G) required to change the drain current (I_D) 10 times in the subthreshold region: the inverse slope of $\log_{10} I_D$ - V_G curve in the subthreshold region, reflecting how abruptly on-off switching occurs.

$$SS = \left(\frac{\partial \log_{10} I_D}{\partial V_G} \right)^{-1} = \frac{\partial V_G}{\partial \psi_s} \times \frac{\partial \psi_s}{\partial \log_{10} I_D} = m \times n \qquad 1.3$$

where, ψ_s represents surface potential of silicon.

As seen in Equation 1.3, *SS* is determined by how much surface potential changes with V_G (*m*) and how much drain current varies with surface potential (*n*). By voltage dividing of oxide capacitance and semiconductor capacitance connected in series, *m* is represented as $(1+C_{ox}/C_{dm})$, which cannot be less than 1 because C_{ox} has a positive value. In the case of *n*, since the number of carriers injected from the source to the channel is governed by the Boltzmann statistics, it cannot be reduced below a certain value. By substituting the I_D of subthreshold region into *n*, one can obtain n = 2.3 kT/q, which is limited to 60 mV/dec at 300k, thus the *SS* of a MOSFET fundamentally cannot be less than 60 mV/dec at room temperature. In order to overcome the Boltzmann constraint (limitation of "*n*"), numerous devices with a novel transport

mechanism, such as tunnel-FETs utilizing band-to-band tunneling of pin diodes [71], feedback-FETs using positive feedback loops of n-p-n-p diodes [72], and i-MOS utilizing impact ionization of p-i-n diodes [73], have been extensively studied. Although TFET can exhibit superior *SS* and on/off ratio theoretically, its I_{on} is several decades below that of MOSFETs, leaving it unsuitable for use as high-performance logic devices. Feedback-FET cannot respond to high-speed operation, while i-MOS requires high V_{DD} for breakdown, as well as has reliability issues. In addition, above devices are not applicable for highly-scaled CMOS technology due to the difficulty in self-aligned junction formation.

In 2008, Sayeef Salahuddin suggested a FET utilizing the NC effect [74], which contains the concept of enabling $m < 1$ by employing a NC material in the gate oxide of MOSFET [67]. He demonstrated that the NC effect in the MOSFET causes the amplification of the surface potential by the applied voltage amplification ($\partial\psi_s / \partial V_G > 1$) through the mathematical calculations using the Landau model. As shown in **Figure 1.11**(a), negative capacitance FET (NCFET) enables V_{DD} scaling with the same performance, since it has steep *SS* and current drivability similar to that of the existing MOSFET, which is the simplest method for power scaling [67]. Since [74], numerous studies on the understanding of NCFET and demonstration of NCFETs with HfO-based ferroelectric material have been published. [53-65]. NCFET with CMOS compatible HfO-based material can be easily implemented to the existing

logic device structure such as FinFET, featuring high current drivability due to the same carrier injection mechanism as conventional MOSFET; consequently, being regarded as the most promising candidates among other emerging next generation logic devices such as TFET, feedback-FET and i-MOS. NCFET is being evaluated as a solution to extend V_{DD} and equivalent oxide thickness (EOT) scaling of CMOS devices, which has stalled since the middle of the 2000s due to the Boltzmann limit and increasing gate leakage current [**Figure 1.11**(b)].

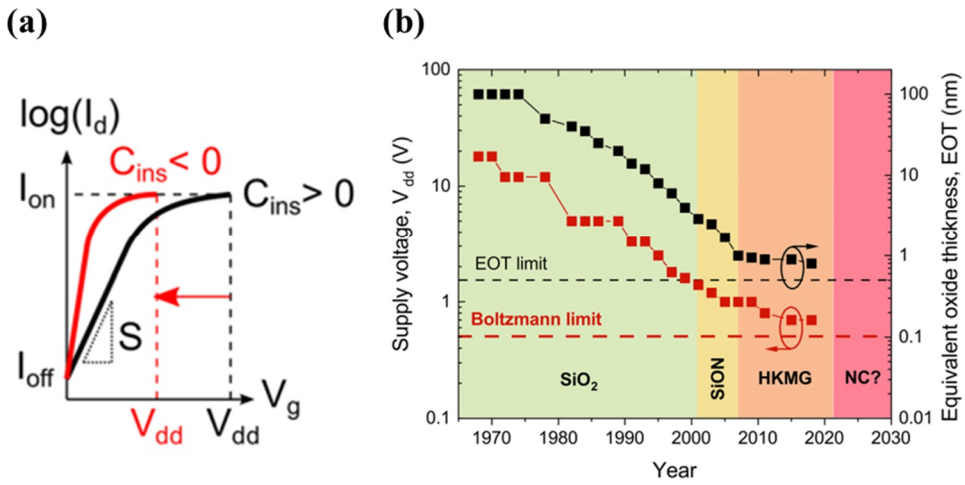


Figure 1.11. (a) Schematic transfer characteristics of MOSFETs with positive / negative capacitance. (b) V_{DD} and EOT scaling trend [67].

1.3.3 Stable NC vs. Sub-thermionic SS

However, the NC region claimed by the simple thermodynamic Landau model is thermodynamically unstable because it exists on the maximum of free-energy as shown in **Figure 1.9**(a). Charge can exist in two energy minima in a ferroelectric material; hence, only polarization switching is seen above the E_C, leading to the memory hysteresis of the ferroelectric FET's I_D. That is, NC cannot be accessed in a stand-alone ferroelectric capacitor. Therefore, it is necessary to answer the questions of whether NC exists and whether it is actually possible to be utilized. Several groups have tried to experimentally observe the NC of ferroelectric materials [39, 75-78]. Michael Hoffmann [39] has calculated a double-well free-energy landscape from the voltage and current measured in the resistor for applied transient voltage pulses using a ferroelectric capacitor including a second dielectric layer and a series-connected resistor. The second dielectric and external resistor used in this experiment delay the charge screening of the electrode for voltage pulses. The phenomenon observed when metal charge screening is slower than polarization switching in fast measurement is referred to as the transient NC effect [39, 67]. However, it is only a transient observation which eventually ends up in positive capacitance with a hysteresis loop due to the instability of the NC region. Since the transient NC involves polarization switching, it generates hysteresis in transfer characteristics [53-56, 79] and requires

a great amount of voltage or time; thus, the direct observation of NC using transient NC nature still does not answer whether NC can be applied to logic devices.

On the other side, research has been performed on the thermodynamically stabilization NC [67, 80, 81]. NC stabilization in previous studies means the introduction of a series-connected positive capacitor (dielectric). They argue that the total capacitance of dielectric + ferroelectric can be positive even in the NC region of the ferroelectric as following description. The free-energy (F_d) of a dielectric material is a quadratic function of the charge with the coefficient inversely proportional to the capacitance ($F_d = Q/2C^2$). Therefore, the total free-energy (F_t) of the system [**Figure 1.12**(a)] in which the ferroelectric material following the landau model (Equation 1.1) and the dielectric are connected can be expressed as follows.

$$F_t = F_f + F_d = \left(\alpha t_f + \frac{t_d}{2\varepsilon_0 \varepsilon_d} \right) P^2 + t_f \beta P^4 + t_f \gamma P^6 - VP \qquad 1.4$$

, where ε_0, ε_d and t_d represents vacuum permittivity, relative permittivity and thickness of dielectric. The free-energy landscape of total system along with that of ferroelectric and dielectric are illustrated in **Figure 1.12**(b) [67]. Here, the curvature of the total free-energy near $P = 0$ is determined by the second-order coefficient in Equation1.4: capacitance of the series-connected dielectric (t_d and ε_d), the landau second-order constants (α), and t_f. The total free-energy can be stabilized near $P = 0$ while the ferroelectric is in NC region only if the second-order coefficient of Equation 1.4 is

positive, which is satisfied when the dielectric capacitance is adequately small. However, in advanced CMOS technologies utilizing high-κ dielectric, interfacial layer (IL) SiO_2 is indispensable to reduce interfacial trap density (D_{it}) and it must be extremely thin (~several angstrom) for EOT scaling, which is contrary to the requirement of a series-connected dielectric for stable NC [81]. Furthermore, stabilized NC cannot be realized in the real devices due to the screening effect by trapped charges [39].

Meanwhile, the criterion for achieving a stable NC in MOS system with a ferroelectric layer can be expressed in a capacitance form as,

$$| C_{FE} | \; < \; C_{MOS} = (C_{IL}^{-1} + C_{Si}^{-1})^{-1} \tag{1.5}$$

where, C_{FE}, C_{MOS}, C_{IL} and C_{si} represents the capacitance of ferroelectric layer, MOS system, IL and Si, respectively. In addition, the capacitance condition for sub-thermionic SS (< 60 mV/dec) in NCFET can be expressed as,

$$| C_{FE} | \; > \; | C_{IL} \tag{1.6}$$

from

$$SS = 60 \text{ mV/dec} \times \left(1 + \frac{C_{Si}}{(C_{IL}^{-1} + C_{FE}^{-1})^{-1}} \right) \tag{1.7}$$

Here, since the C_{Si} of Equation 1.5 is negligible in the inversion region, the criterions of Equation 1.5 and Equation 1.6 are incompatible. Although there surely is a window

for satisfying both conditions in the depletion region, where C_{Si} is quite small, little design space exists for the entire operating voltage including the inversion region. Consequently, the sub-thermionic *SS* claimed by conventional NCFETs is difficult to be implemented in practically [82]; thus, recent researches on NCFET focuses on the performance enhancement through stable capacitance boosting using the NC effect of ferroelectric material [83]. They aim at employing a high-κ with a larger permittivity, hence enhancing SCE immunity through near-60 mV/dec *SS* and enabling performance boosting by improved I_{on}.

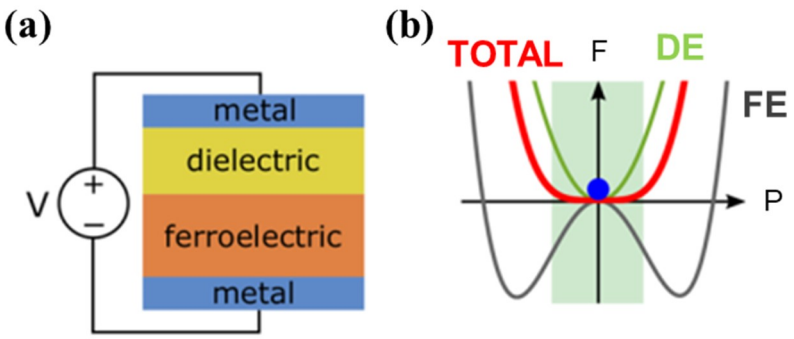


Figure 1.12. (a) Schematic of dielectric (DE)-ferroelectric (FE) series capacitor for NC stabilization. (b) Corresponding free-energy landscapes [67].

1.4 Scope and Organization of Dissertation

This thesis focuses on the design of NC material for stable capacitance boosting for low-power and high-performance logic device and the fabrication of the stacked NS GAA structure utilizing it. To overcome the constraints of previous research described in Subsection 1.3.3, optimization of a stable NC HZO and application of NC material to the ultimate advanced logic technology, stacked NS GAAFET for the first time.

In Chapter 2, the concept of stable NC material using mixed-phase HZO proposed in this research and the NS GAA NCFET with optimized HZO are described.

Chapter 3 describes the process of optimizing NC materials experimentally using ferroelectric capacitors and silicon-on-insulator (SOI) planar NCFETs.

Chapter 4 describes the fabrication process for NS GAA NCFET, which is the ultimate objective of this study, and provides a solution for issues in gate-first process.

Electrical characteristics of fabricated NS GAA NCFET are estimated in Chapter 5, which includes DC performance enhancements in fabricated NS GAA NC device. The comparison to other reported NCFETs is also presented, which verifies the superiority of demonstrated NS GAA NCFET in terms of hysteresis-free, steep-*SS* and high current drivability.

Chapter 2

Stacked NS GAA NCFET with Ferroelectric-Antiferroelectric-Mixed-Phase HZO

2.1 Mixed-Phase HZO for Capacitance Boosting

As mentioned in Subsection 1.3.3, a focus on stable capacitance boosting, not an achieving sub-60mV/dec *SS* is essential to utilize the NC effect of ferroelectric materials in logic devices, since the sub-thermionic SS with a thermodynamically stabilized NC is not applicable. This dissertation focuses on an NCFET with a ferroelectric-antiferroelectric-mixed-phase HZO, which utilizes NC effect for capacitance boosting in operating regime, and attempts to experimentally validate its

effect at the FET level.

Figure 2.1 shows the free-energy landscape of ferroelectric, antiferroelectric and ferroelectric-antiferroelectric-mixed-phase materials. Since the NC region located near $P = 0$ of the ferroelectric material is thermodynamically unstable, it is impossible to statically access it. On the other hand, the curvature of the free-energy landscape of the ferroelectric-antiferroelectric-mixed phase material has a positive value near $P = 0$ (NC region of ferroelectric) [84]. In other words, free-energy of mixed-phase preserves a thermodynamically stable state in the NC region of ferroelectric, which is similar to the result of NC stabilization by employing a series-connected dielectric explained in Subsection 1.3.3. However, it is significant compared to the capacitance matching method through the interfacial layer (IL) SiO_2 in that it enables the introduction of an EOT-scalable NC material.

As demonstrated in **Figure 2.2**, the polarization characteristic of HZO varies with the composition rate (x) of Zr, where the pure HfO exhibits paraelectric property; HZO with increased x displays ferroelectric hysteresis loop; and pure ZrO shows antiferroelectricity [85]. From the **Figure 2.2**, it is expected that the ferroelectric-antiferroelectric-mixed-phase material proposed in this research can be obtained in Zr-rich HZO.

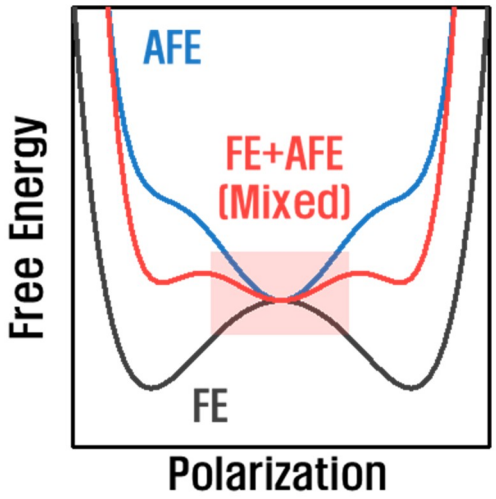


Figure 2.1. Free-energy landscape of ferroelectric (FE), antiferroelectric (AFE) and FE+AFE mixed phase material [84].

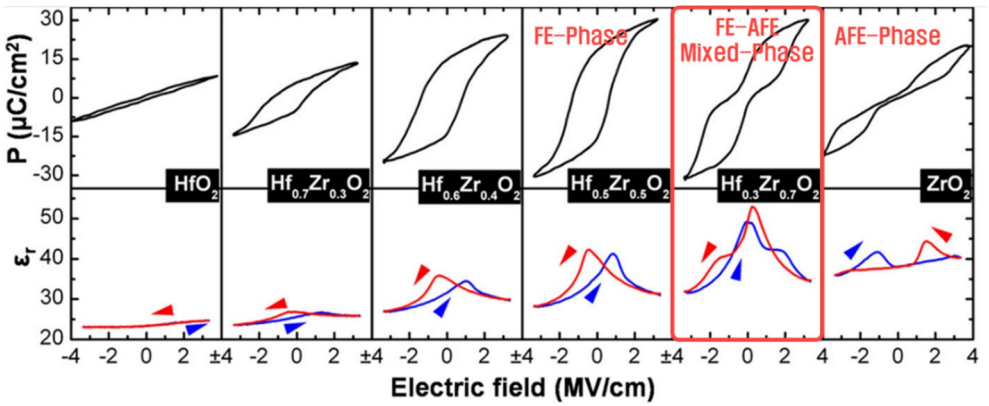


Figure 2.2. Polarization-electric field (*P*-*E*) characteristics of HZO with regard to the Hf / Zr composition [85].

2.2 NS GAA NCFET using Mixed-Phase HZO

Since the discovery of ferroelectricity in CMOS-compatible doped HfO, extensive researches on HfSiO (HSO) or HZO-based NCFETs of various topologies have been conducted [53-65]. **Figure 2.3** shows the *SS* and on-current (I_{ON}) (at V_{DD} = 0.65 V) benchmarks of reported NCFETs. Multiple reports claim to have demonstrated a *SS* of sub-60 mV/dec based on minimum point *SS* [54, 56, 57, 59, 61, 62, 64, 65] or exhibit a steep slope with ferroelectric counter-clockwise hysteresis [53-56], which implies the transient NC through polarization switching as described in Subsection 1.3.3. In addition, numerous studies merely validate the effect of NC HZO on the 2D planar structured transistor [53-55, 58, 63], demonstrating poor current drivability, and do not verify its applicability to the advanced logic structure.

This research proposes and demonstrates a stacked NS GAA NCFET utilizing a ferroelectric-antiferroelectric mixed-phase HZO material as illustrated in **Figure 2.4**. A hysteresis-free stabilized operation and high performance is to be confirmed by applying the mixed-phase HZO to the vertically-stacked nanosheet FET which requires a higher-level of EOT scaling for CMOS extension. Dissertation aims to validate that the capacitance boosting effect of HZO enhances *SS* and I_{on} compared to the reference high-κ NS GAAFET fabricated in the same manner. For the first time, crystalline Si NS GAA structured NCFET is demonstrated, evaluating the feasibility

of NCFET in the future CMOS technology.

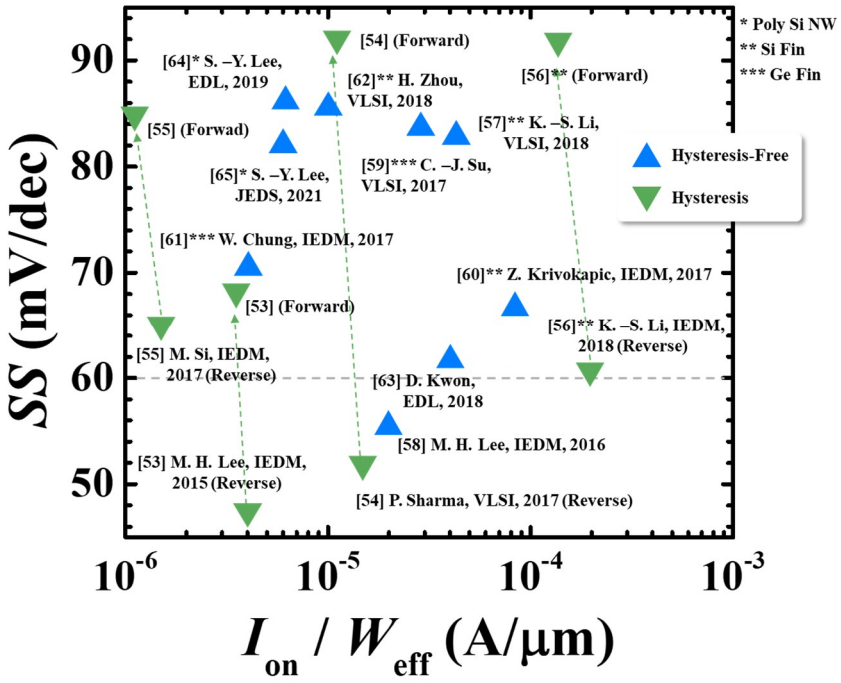


Figure 2.3. *SS*-I_{on} benchmarks of reported NCFETs [53-65].

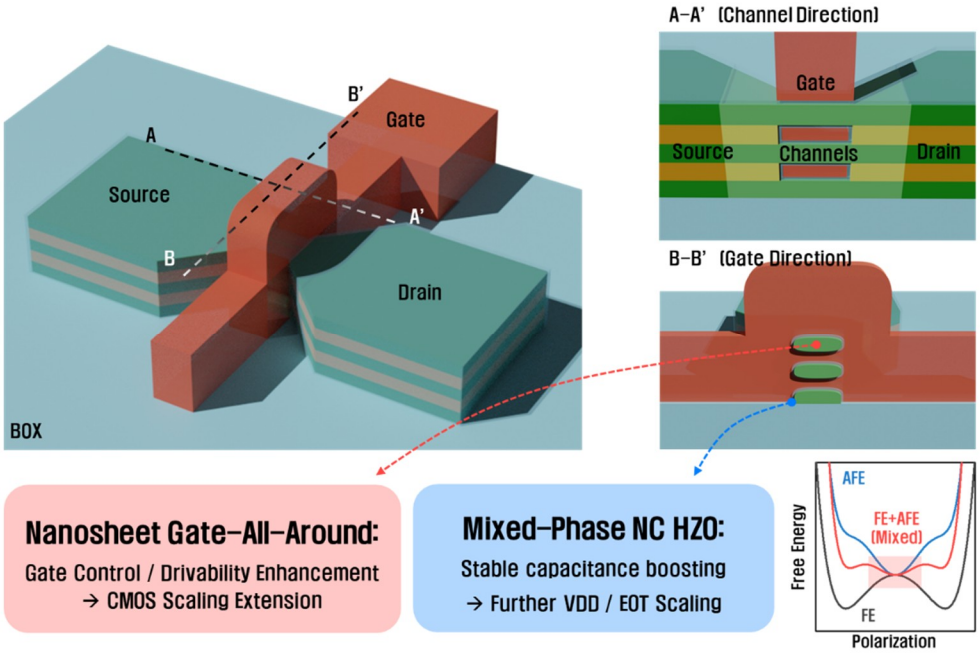


Figure 2.4. Proposed device: stacked NS GAAFETs with ferroelectric-antiferroelectric mixed-phase HZO for low-power and high-performance logic technology.

Chapter 3

HZO ALD Stack Optimization

This chapter describes the optimization process of negative capacitance thin films using ferroelectric-antiferroelectric mixed-phase HZO. In order to evaluate the capacitance boosting effect induced by the NC effect, metal-ferroelectric-interlayer-silicon (MFIS) capacitors are fabricated for multiple HZO stacks and their gate capacitance properties are evaluated.

Prior to employing the HZO thin film optimized through MFIS and metal-ferroelectric-metal (MFM) capacitor experiments to the NS GAA NCFETs, planar NCFETs using silicon-on-insulator (SOI) are fabricated to verify the improvement of current characteristics in MOSFETs. The processes were carried out mainly in the inter-university semiconductor research center (ISRC), Seoul National University, while some parts of fabrication were requested to the other fabs. By validating the

characteristics of SOI Planar NCFETs with floating body structures identical to those of NS GAA structures, it would be possible to predict the characteristics of HZO thin films when applied to actual NS GAA structures, as well as to compare the features with NS GAA NCFETs that will be processed later.

3.1 Metal-Ferroelectric-Interlayer-Silicon (MFIS) / MFM Capacitors

3.1.1 Fabrication of MFIS Capacitors

A common approach for validating the ferroelectricity of a ferroelectric thin film is to measure the displacement current for voltage pulses of metal-ferroelectric-metal (MFM) capacitor. However, as stated previously, it is impossible to observe unstable negative capacitance in a single MFM capacitor [39]. In addition, since it is necessary to examine the effect of the ferroelectric layer on the structure of the actual device to be fabricated, a metal-ferroelectric-interlayer-silicon (MFIS) capacitor was fabricated and compared with the existing HfO (high-κ dielectric) MOS.

The manufacturing sequence of MFIS capacitor is as follows [**Figure 3.1**(a)]. (1) An interfacial layer (IL) SiO_2 (15 cycles) followed by several Hf(Zr)O stacks were deposited on the p^- bare wafer through atomic layer deposition (ALD): As a high-κ control, 34 cycles of pure HfO were deposited; and two kinds of Zr-rich HZO stacks

(HZO stack 1, HZO stack 2, totaling 34 cycles) were deposited to adopt a ferroelectric-antiferroelectric mixed-phase, as illustrated in **Figure 3.1**(b). In the case of HZO stack 1, ZrO and HfO were deposited in a nanolaminate structure that was repeatedly deposited in 4 cycles and 2 cycles, respectively, and in the case of HZO stack 2, it was deposited in a superlattice form in the order of HfO 4 cycle-ZrO 26 cycle-HfO 4 cycle. (2) Subsequently, ALD TiN deposition was carried out for two reasons: i) If TiN is directly deposited on a insulator as a gate material via sputtering, the high-κ layer is damaged resulting in the increase of trap states. Therefore, the ALD TiN 300 cycle (100 A) was deposited preferentially as a sputtering damage barrier. **Figure 3.2**(a) compares the gate capacitance characteristics of MOS (TiN-HfO-SiO_2-p^- Si) capacitors with and without barrier ALD TiN deposition. Since the ISRC TiN sputtering power is quite high (5000 W), the capacitance hump in the depletion region induced by the high-κ thin film's trap is apparently exhibited without the barrier metal. On the other hand, it is confirmed that the hump in the depletion region is significantly alleviated with barrier TiN ALD of 300 cycles (100 A). ii) Since the to-be-fabricated device is a GAA structure with a suspended channel, the gate metal between the vertically stacked channels must be filled using the chemical vapor deposition (CVD), which cannot be fulfilled by physical vapor deposition (PVD). (3) TiN gate electrode material was deposited through sputtering. (4) Patterning was performed through photo lithography and inductively coupled

plasma–reactive ion etching (ICP-RIE) dry etching using Cl_2 gas. (5) To assess the inversion region characteristic of the MFIS capacitor, a self-aligned n^+ doping was conducted under the condition of As^+, 20 keV, 2×10^{15} cm^{-2} using a medium current ion implanter. (6) Post metal annealing (PMA) process (500℃, 30 seconds) was performed using rapid thermal annealing (RTA) for HZO crystallization and dopant activation. (7) Lastly, in order to minimize the interfacial trap density (D_{it}), high pressure annealing (HPA) was carried out in an H_2 atmosphere (18 Bar, 400℃, 1hour). **Figure 3.2**(b) illustrates the capacitance-voltage (*C* - *V*) characteristics of a MOS (TiN-HfO-SiO_2-p^- Si) capacitor with and without HPA process. The lowering of the C-V curve's hump in MOS capacitor with HPA confirms that the D_{it} was greatly reduced due to the elimination of the Si - SiO_2 interfacial dangling bond. Transmission electron microscopy (TEM) image confirms that the stack was deposited with IL (SiO_2) 1.0 nm / HZO 3.2 nm, while Energy-dispersive X-ray spectroscopy (EDS) analysis verifies the composition ratio (Hf 0.26 : Zr 0.74), which has been designed to produce Zr-rich mixed-phase HZO [**Figure 3.1**(c)].

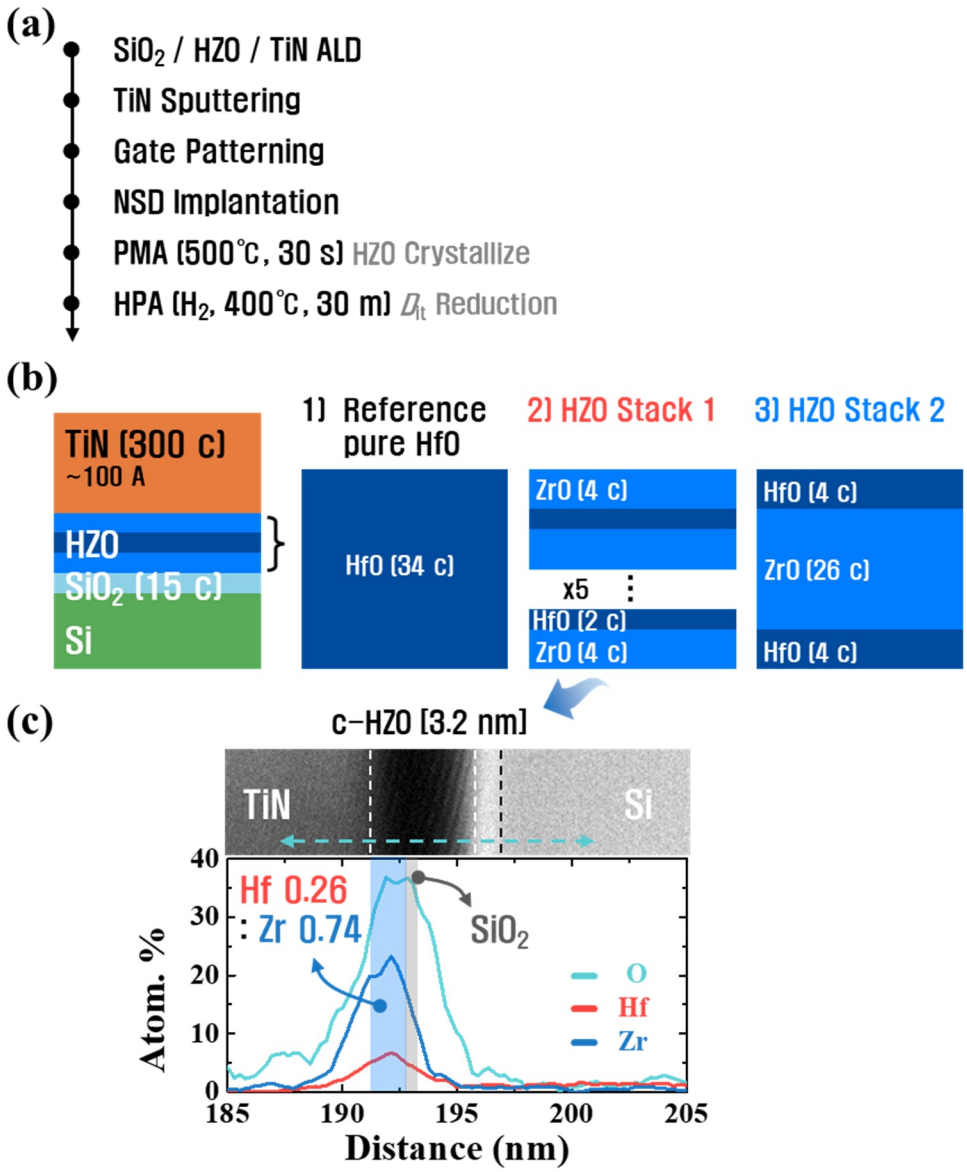


Figure 3.1. (a) Summarized process flow of MFIS capacitors. (b) Schematic image of MFIS capacitors fabricated on p- Si. Two types of HZO ALD stacks along with reference pure HfO ALD stack are depicted. (c) TEM / EDS analysis of HZO stack 1.

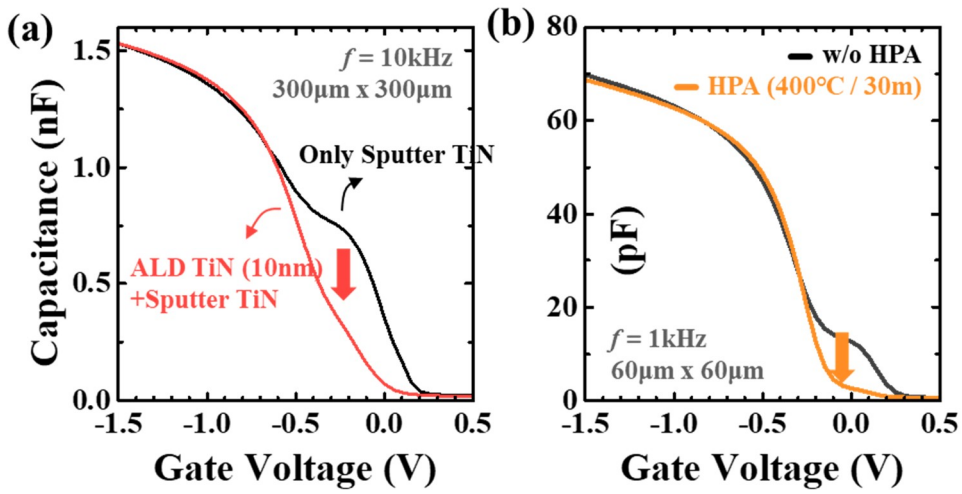


Figure 3.2. (a) Capacitance-Voltage (*C*-*V*) characteristics of MOS (TiN-HfO-SiO_2-p^-Si) capacitor with different TiN gate stack (ALD TiN + sputter TiN and only sputter TiN). (b) *C*-*V* characteristics of MFIS capacitor with and without HPA process.

3.1.2 Electrical Characteristics of MFIS / MFM Capacitors

Gate capacitance characteristics of the reference HfO and two types of ferroelectric thin films (HZO stack 1 and HZO stack 2) were electrically measured for validating the capacitance enhancement by NC effect of the fabricated MFIS capacitors. Capacitance measurements were conducted using an Agilent B1500A capacitance

measuring device (CMU). Dimension of capacitor was 60 × 60 μm^2 and the capacitance measuring frequency was 1 kHz. Both inversion capacitance and accumulation capacitance can be measured owing to n^+ doping. As can be seen in **Figure 3.3**(a), accumulation and inversion capacitance enhancements were validated in HZO stack 1 and HZO stack 2 compared to the pure HfO. The capacitive effective oxide thickness (CET) was calculated to be 1.79 nm for pure HfO, 1.64 nm for HZO stack 1 and 1.57 nm for HZO stack 2. Since TEM [**Figure 3.1**(c)] proved the thickness of IL to be 1.0 nm, the dielectric constant of ALD Hf / HZOs can be calculated. As summarized in **Table 3.1**, it was determined that the dielectric constant of pure HfO was 14.5, and that of HZO stack 1 / 2 was 20.4 / 22.5, respectively, where the dielectric constant improvement was 40% in HZO stack 1 and 55% in HZO stack 2. Here, note that the accumulation capacitance is not saturated yet at gate voltage (V_G) = -1.5 V, due to the large area of capacitor; thus, the calculated CET could be underestimated.

However, the leakage current-gate voltage (*I*-*V*) graph [**Figure 3.3**(b)] reveals that the gate leakage current of HZO stack 2 is quite large. In general, it is known that the poly crystallization temperature of ZrO is slightly lower than that of HfO [86, 87]. Since the same PMA temperature (500℃, 30 seconds) was applied to all three samples in this experiment, it can be concluded that poly-crystallization was greatest in the case of HZO stack 2 deposited in the form of superlattice, leading to the

increase of leakage. Accordingly, the capacitance was distorted in the inversion region, as indicated by the *C-V* characteristic [**Figure 3.3**(a)]. Considering the actual device area and operating voltage, the HZO stack1 with an acceptable leakage level was chosen for the NC thin film.

In order to examine the polarization characteristics of the HZO stack, MFM capacitor was fabricated to measure displacement current for triangular voltage pulses. In the case of MFM capacitor, if the thin film is too thin, leakage current becomes too large to distinguish the the displacement current due to polarization. Therefore, HZO stack 1 was deposited twice as thick as the prior MFIS experiment, in 68 cycles with the identical HfO / ZrO composition. For pulse measurement, an Agilent B1500 waveform generator/fast measurement unit (WGFMU) was utilized. In order to validate the polarization characteristic of the ferroelectric film, a triangle-shaped voltage pulse was applied to the top electrode. As depicted in **Figure 3.4**(a), a triangular V_G pulse with a rising / falling period of 1 ms was applied, and the resulting current was measured in the bottom electrode to exclude the external parasitic capacitance of pulse generator. The measured current consists of leakage current and displacement current which is separated into a paraelectric capacitive component and a polarization component induced by ferroelectric switching. In ferroelectric materials, current peaks due to polarization switching are observed when the voltage increases at a positive voltage above coercive voltage (polarization up) and when the

voltage decreases at a negative voltage (polarization down), whereas the current peak is not observed in the opposite cases (*V* decrease in positive and *V* increase in negative region) as it maintains the polarization state. However, as indicated by the red arrow in the voltage / current - time diagram [**Figure 3.4**(a)], it can be confirmed that the current peak appears in the case of *V* decrease in positive and *V* increase in negative region, indicating the antiferroelectric nature. Calculating the polarization by integrating the current over time results in the graph presented in **Figure 3.4**(b), which confirms that ferroelectricity and antiferroelectricity coexist in HZO stack 1.

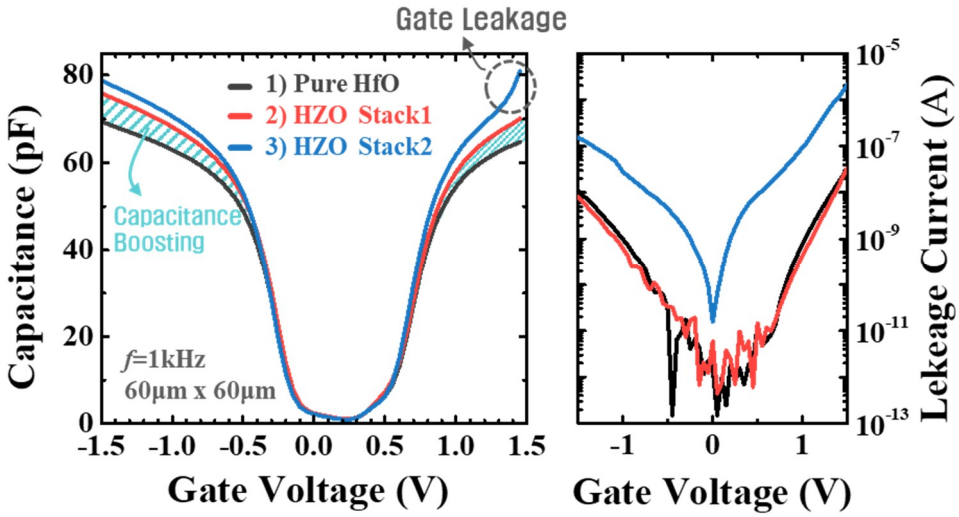


Figure 3.3. (a) Gate capacitance characteristics of various MFIS stacks: 1) Pure HfO / 2) HZO stack 1 3) HZO stack 2. Capacitance enhancements in HZO stacks are noticeable. (b) Gate leakage currents of three ALD stacks.

Table 3.1. Dielectric constants of high-κ films extracted from accumulation capacitances (V_G=-1.5 V).

	CET [nm]	t_{IL} [nm]	CET_{HK} [nm]	Dielectric Constant
1) Pure HfO	1.79		0.79	14.5
2) HZO Stack1	1.64	1.0	0.64	20.4
3) HZO Stack2	1.57		0.57	22.5

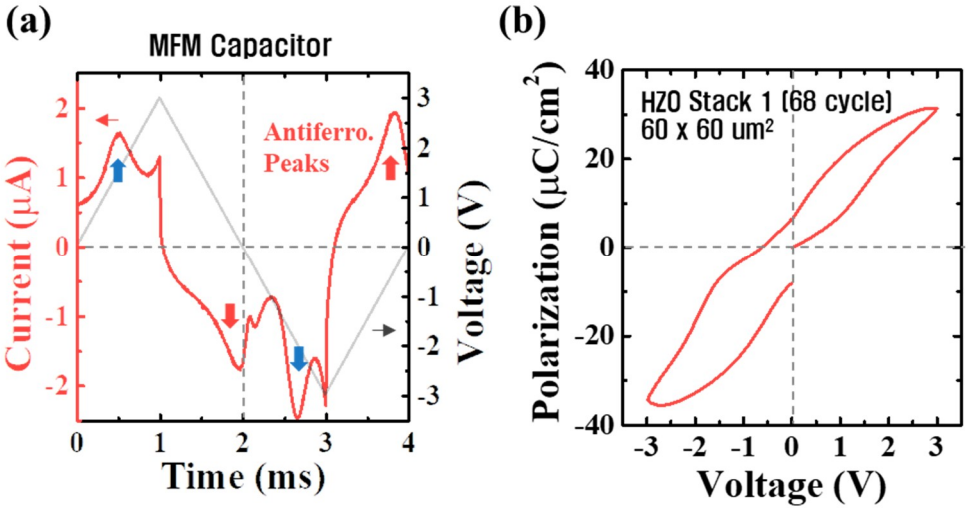


Figure 3.4. (a) Displacement current measurement of MFM capacitor (HZO stack1) for triangular voltage pulse. (b) *P-V* curve obtained from (c), showing ferroelectric-antiferroelectric-mixed characteristic.

3.2 SOI Planar NCFETs

3.2.1 DC Measurements

Prior to applying the HZO thin film which was setup through MFIS and MFM capacitor experiments to the NS GAA architecture, a planar NCFET was fabricated using a silicon-on-insulator (SOI) wafer in order to validate the current improvement in the FET. Since the NS GAAFET has a body floating structure, an SOI wafer was employed, and the device dimensions [channel width (W) and gate length (L)] were defined by photolithography for the convenience of the fabrication process. The schematic image and physical parameters of the fabricated device are shown in **Figure 3.5** and **Table 3.1**. As a control for the NCFET with HZO stack 1, a MOSFET with a pure HfO high-κ gate dielectric was fabricated in the same manner. The detailed device fabrication method including the source / drain (S/D) 1st doping and self-aligned (S-A) S/D doping shown in **Table 3.1** is similar to the NS GAA NCFET process, which will be covered in Chapter 4.

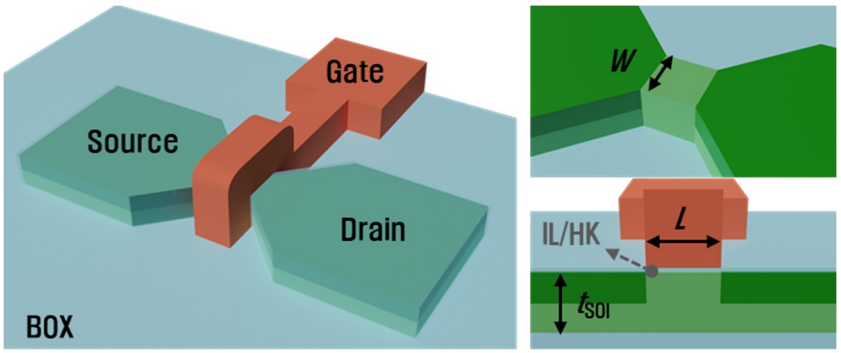


Figure 3.5. Schematic image of SOI planar NCFET.

Table 3.2. Physical parameters and process conditions of SOI planar NCFET

Physical Parameters		**Process Conditions**	
t_{SOI}	100 nm	HK	Pure HfO / HZO stack 1
W	0.5 ~ 50 μm	S/D 1st Doping	As^{+} / 2×10^{15} cm^{-2}
L	0.5 ~ 50 μm	S-A S/D Doping	P^{+} / 2×10^{15} cm^{-2}
t_{IL}	1.0 nm		
t_{HK}	3.2 nm		

Figure 3.6(a) illustrates the drain current (I_D) - V_G characteristics of the SOI planar NCFET under different drain voltages (V_{DS}). The enlarged transfer curve [**Figure 3.6** (b)] demonstrates that the majority of HZO devices exhibit stable characteristics with clockwise hysteresis of 5mV or less (nearly hysteresis-free) thanks to the mixed-phase stable NC material. However, as shown in **Figure 3.6**(c), few devices had an uncommon counterclockwise hysteresis loop, with the steeper subthreshold swing (*SS*) in the reverse-swept I_D. The memory effect (counter-

clockwise hysteresis) of ferroelectric (FE) material induced by polarization switching arises above the coercive electric field (E_C), which requires much higher V_G than the operating VG of a typical logic device [48]. Nonetheless, the counterclockwise hysteresis in the very low gate voltage sweep region of **Figure 3.6**(c) might be attributed to the extremely low energy barrier for polarization switching in the FE+AFE energy landscape [**Figure 3.6**(d)]. The steeper *SS* in the reverse sweep direction also indicate the effect of polarization switching as described in the Subsection 1.3.3.

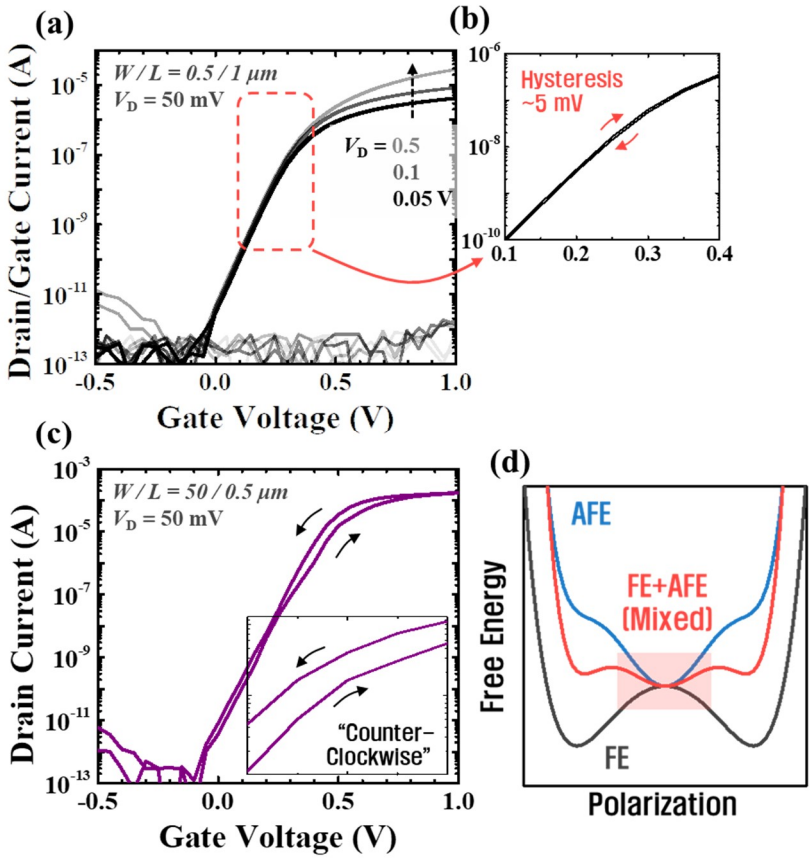


Figure 3.6. (a) Transfer characteristics of most SOI planar NCFET (b) enlarged graph of (a), showing nearly hysteresis-free feature. (c) Transfer characteristic of few devices and enlarged graph (inset), showing counter-clockwise hysteresis. (d) Free-energy landscape of ferroelectric (FE), antiferroelectric (AFE), and mixed phase (FE + AFE).

Figure 3.7(a) and (b) show the I_D / I_G - V_G characteristics (at V_D = 50 mV and 0.5 V, respectively) for pure HfO and HZO stack 1 device with W / L = 0.5 / 1 μm. It was confirmed that the gate current had a low value of 10^{12} A or less in the V_G ~1 V sweep range in both devices. When the V_G is set to identical off-current (I_{off}) in the linear V_D (50 mV) condition, it can be observed that the current in the HZO stack 1 device is enhanced from near the threshold voltage (V_{th}) compared to the pure HfO device. The gate-induced-drain-leakage (GIDL) current of saturation V_D (0.5 V) condition is different as can be seen in **Figure 3.7**(b), which is thought to be due to the misalignment occurred in the non-self-aligned S/D doping (S/D 1st doping). *SS* – I_D plot [**Figure 3.7**(c)] confirms the *SS* enhancement by capacitance boosting of HZO stack 1. A 3-decades average *SS* (W_{eff}-normalized I_D range from 10^{-10} A/μm, where I_D is sufficiently larger than I_G, to 10^{-7} A/μm) for reference and HZO device was 75.5 mV/dec and 71.4 mV/dec, respectively.

On the other hand, the transfer characteristics of devices with relatively large *W* (*W* = 10 μm) [**Figure 3.8**(a)] exhibits somewhat extraordinary behavior: the I_D of HZO device was enhanced from near the V_{th} as similar to **Figure 3.7**(a), but I_D of reference device overtakes that of HZO device as the V_G increase. The phenomenon can be explained as follows. The on-resistance (R_{ON}) component of MOSFET is shown in **Figure 3.8**(b) and Equation 2.1.

$$R_{ON} = R_{CH} + R_{External} = R_{CH} + (R_{EXT} + R_{SD} + R_{CNT}) \quad 2.1$$

, where R_{CH} and $R_{External}$ refers to the channel and external resistance, respectively, and the $R_{External}$ consists of S/D extension resistance (R_{EXT}), doped S/D resistance (R_{SD}) and contact resistance (R_{CNT}). The R_{CH} become comparable to $R_{External}$ in the high VG region, leading to the increase of $R_{External}$'s dominance. Particularly in the case of a device with a wide W the channel resistance is relatively low (since the size of the pad where the contact is placed is designed to be the same regardless of W), thus the influence of $R_{External}$ is more significant. Therefore, the behavior depicted in **Figure 3.8**(a) can be considered because the $R_{External}$ of the pure HfO device is less than that of the HZO device. This interpretation is consistent with the explanation of the GIDL difference in **Figure 3.7**(b). As described in **Figure 3.8**(c), the total resistance of the FET according to 1/overdrive voltage ($1/V_{OV}$) was calculated from the I_D-V_G characteristics of linear V_D. At the point where $1/V_{OV} = 0$ (V_{OV} goes to infinity), R_{CH} can be ignored; that is, y-intersect of the graph can be approximately regarded as the $R_{External}$. The $R_{External}$ of reference pure HfO device (0.11 kΩ) was revealed to be significantly lower than that of HZO stack1 device (0.3 kΩ). Nevertheless, given that the HZO device's current is larger in the relatively low V_G region, it can be confirmed that the current improvement due to the capacitance boosting of fabricated HZO devices is an intrinsic performance enhancement regardless of the $R_{External}$.

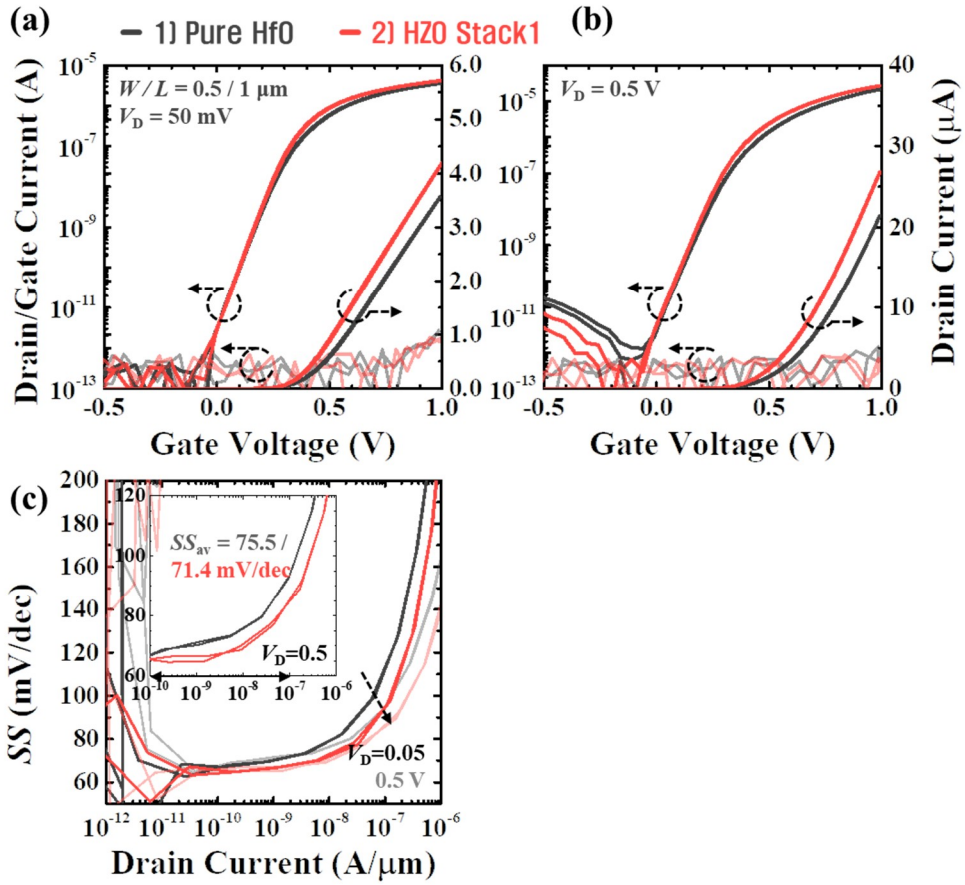


Figure 3.7. (a) and (b) Transfer characteristics of SOI planar NCFET with HZO stack1 (V_D = 50 mV and 0.5 V, respectively) compared with reference pure HfO device. (c) Subthreshold swing (SS)-I_D curve extracted from (a) and (b).

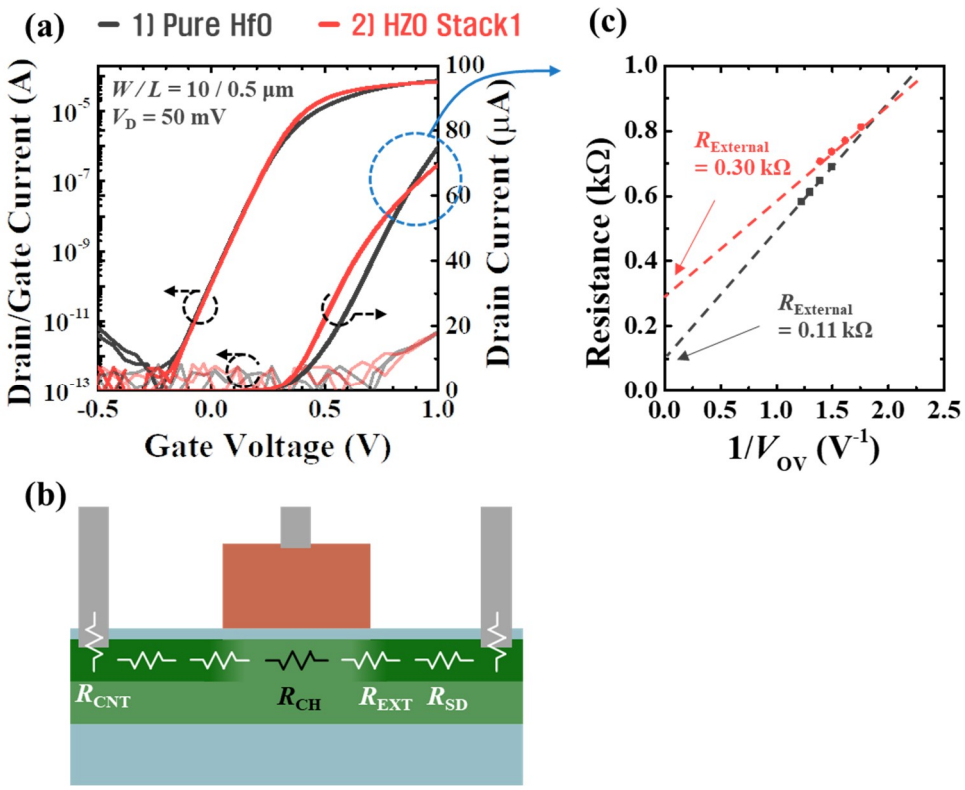


Figure 3.8. (a) Transfer characteristics of NCFET and reference MOSFET with relatively large channel width (W = 10μm). (b) Series resistance of MOSFET (c) External resistance extraction by $1/V_{OV}$ method.

Figure 3.9 demonstrates that the HZO enhances the current by 25 to 50% compared to the reference HfO device in the linear (V_D = 50 mV) and saturation (V_D = 0.5 V) regions, and under various overdrive voltage (V_{OV}) conditions ranging from 0.25 to 0.45 V. Here, V_{OV} = 0.45 V and V_{OV} = 0.35 V corresponds to the operation V_G considering the V_{th} and V_{DD} of 2.1nm-node and 0.7nm-eq-node high performance (HP)

device presented in IRDS 2021 [30], respectively. It can be noticed that the current improvement is larger as the smaller the V_{OV}; this is due to the fact that i) the V_{th} of the HZO device is slightly smaller, thus difference of I_{DS} in low V_{OV} (near the subthreshold region) is amplified, and ii) the impact of $R_{External}$ increases at the high V_{OV}. Consequently, it is possible to anticipate ever-improving current characteristics in the on state through the optimized processes including junction control and contact formation. A Schottky barrier NCFET using silicide S/D has been proposed to minimize the $R_{External}$ in the gate-first process [88]. The output characteristic [**Figure 3.10**] confirms the current gain of HZO device in the entire V_D region compared to the reference pure HfO devce.

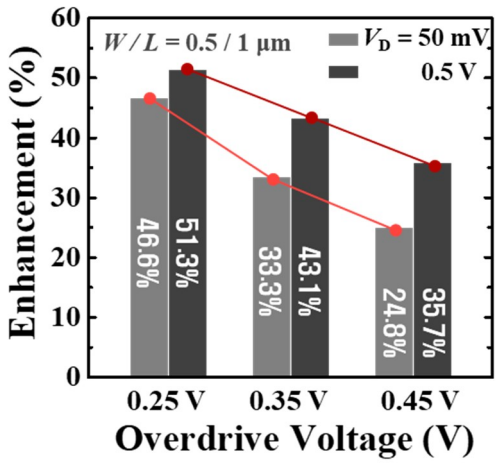


Figure 3.9. On-current enhancement in SOI planar NCFET compared to the reference HfO device at linear and saturation V_D conditions.

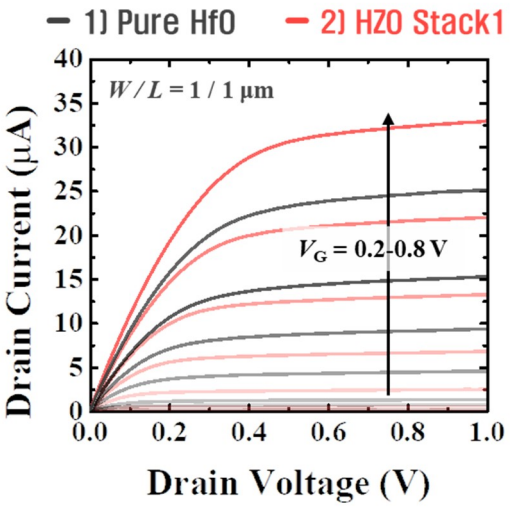


Figure 3.10. Output characteristics (I_D-V_D) of SOI planar NCFET compared to pure HfO device.

3.2.2 Direct Capacitance Measurements

The *SS* and current enhancement confirmed in the Subsection 3.2.1 result from the capacitance boosting effect of the mixed-phase HZO. In order to verify the capacitance enhancing effect of the mixed-phase HZO at the FET level, direct gate capacitance measurements in the FET were performed. For the sufficient resolution of small-signal capacitance measurement, the planar SOI FETs with relatively large width (W = 50 μm) were used. As depicted in **Figure 3.11**(a), the gate capacitance of HZO device has been enhanced compared to the pure HfO device. The capacitance enhancement of the HZO device over the HfO device is expressed as (C_{HZO} / C_{HfO}),

where the C_{HZO} and C_{HfO} represents the capacitance of HZO device and HfO device, respectively. It should be emphasized that the capacitance boosting at near / above threshold voltage is exhibited. It results from the electric field dependence of permittivity in mixed-phase HZO, as opposed to the dielectric whose permittivity is constant. **Figure 3.11**(b) exhibits the transfer characteristic of the same devices as **Figure 3.11**(a), which clearly demonstrates the current boosting at the near / above V_{th} region.

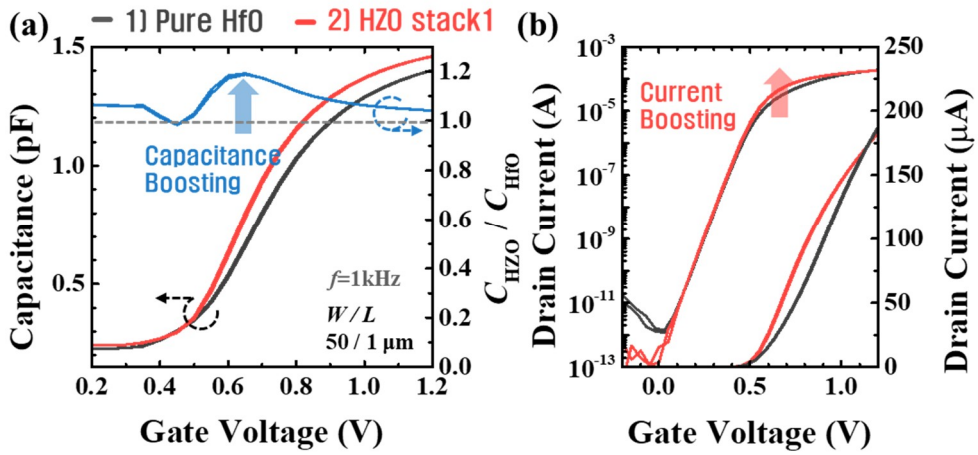


Figure 3.11. (a) Capacitance-voltage characteristics (y1) directly measured from SOI planar FETs (Pure HfO and HZO stack 1) and the capacitance ratio (y2). (b) Transfer characteristics of the same device as (a).

3.2.3 Speed Measurements

In order for NCFETs to be used in high-speed logic applications, it must be determined whether capacitance boosting by the NC effect is effective at high speed. In order to determine if the current enhancement of HZO discussed in Chapter 3.2.1 is effective at high-speed V_G, the current characteristics were evaluated by applying the step-wise V_G pulses. The step-wise V_G pulses (0 ~ 1 V) was applied and resulting I_D was measured using Agilent B1500 WGFMU as shown in **Figure 3.12** (a). Rising time (t_R) was set to 10 ns, and delay time (t_D) + measurement time (t_M) was set to the range from 20 ns which is the minimum time that the equipment can apply to 100 μs, while the t_D and the t_M were set the be identical. Note that a device with a wide W (= 50 μm) was used for achieving sufficient current level, due to the speed - resolution trade-off in fast current measurement. As depicted in **Figure 3.12**(b) and the enlarged graph [**Figure 3.12**(c)], despite the fact that V_{th} slightly shifts as the speed increases, it was confirmed that the current characteristics were comparable to those of DC-measured current. This demonstrates that the HZO layer's capacitance-boosting effect is effective even at speeds of several tens of ns. However, further speed response experiments are necessary to determine whether current enhancement by NC effect is effective for the speed required in the actual CPU block (~several ps), which can be verified using ring-oscillator or radio-frequency (RF) test element group (TEG)

[89]. Daewoong Kwon [83] has reported a delay of 8.5ps using a Fin NCFET-based 101-stage ring oscillator manufactured in the industry fab.

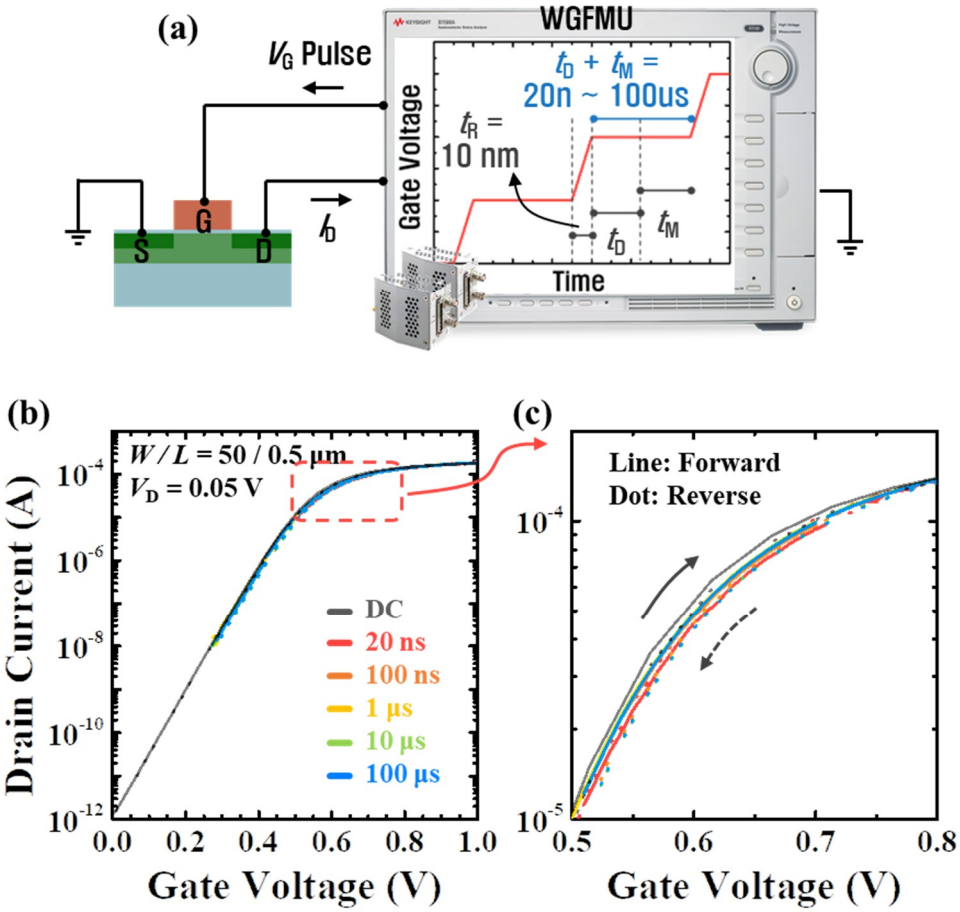


Figure 3.12. (a) Measurement setup for transient I_D-V_G using B1500 WGFMU. (b) I_Ds of SOI planar NCFET (W / L = 50 / 0.5 μm) with V_G pulse of t_D + t_M = 20 ns ~ 100 μs. (c) Enlarged I_D-V_G graph.

Chapter 4

Device Fabrication of Stacked NS GAA NCFET

This chapter describes the fabrication process to apply the HZO negative capacitance (NC) stack designed in Chapter 3 to the stacked NS GAA structure. Chapter 4.1 introduces initially-considered process flow. Since it is difficult to implement the replacement metal gate technique in the scaled device at the university fab level, the stacked NS GAA NCFET was fabricated using the gate-first process. A variety of issues resulting from the gate-first method and the solutions are addressed in Chapter 4.2. Chapter 4.2.4 describes the methodology and experiment details for channel release process via selective etching, which is the key-step of the stacked NS GAA fabrication. Chapter 4.4 concludes by introducing the revised process flow and the fabricated device structure through unit process experiments.

4.1 Initial Process Flow of NS GAA NCFET

The initially planned process flow is shown in **Figure 4.1**. In this research, a gate-first process method with a SOI substrate was used. **Figure 4.1**(a) summarizes the initial process flow, and **Figure 4.1**(c)-(h) depict the A-A' cross section of the 3D-schematic image [**Figure 4.1**(b)]. The detailed sequence is as follows. (1) SiGe / Si / SiGe / Si was epitaxially grown in sequence on a SOI substrate thinned to 35 nm [**Figure 4.2**(a)], which was carried-out by IQE Silicon Corp. in the United Kingdom. **Figure 4.2**(b) shows the atomic percent profile of the test epitaxy wafer, where the composition ratio of SiGe was confirmed to be 0.75:0.25. Here, single crystalline Si is a channel material, while SiGe is used as a sacrificial layer for channel release, which will be described later in Chapter 4.2.4. (2) Active was formed via mix-and-match lithography using photolithography and e-beam lithography, and following inductively coupled plasma–reactive ion etching (ICP-RIE) using HBr gas [**Figure 4.1**(c)]. **Figure 4.3** depicts the top-viewed scanning electron microscopy (SEM) image of the active with a width of 50 nm to 200 nm, where the relatively narrow channel was confirmed to be clearly defined. (3) In order to suspend the channel, SiGe epitaxially grown between Si is etched selectively with an etchant selective for Ge; the detailed procedure of selective etching will be addressed in Chapter 4.2.4 [**Figure 4.1**(c)]. (4) a gate-stack composed of an interfacial layer (SiO) and a high-κ

layer (HZO) is deposited using ALD, followed by the TiN gate deposition, which is combination of ALD TiN (for buffering sputter damage as well as filling the space between channels, as addressed in Subsection 3.1.1) [**Figure 4.1**(e)] and (5) sputtered TiN for gate electrode [**Figure 4.1**(f)]. (6) The gate patterning is then accomplished by means of photo / e-beam mix-and-match lithography and RIE etching with Cl_2 gas. Here, as shown in the B-B' cross-sectional image of **Figure 4.1**(f), the two layers of the released Si channel and the bottom SOI channel are wrapped around by TiN gate. (7) Afterwards, self-aligned source / drain (S/D) ion implantation is conducted using the TiN gate as a mask under the conditions of P^+, 40 keV, 2×10^{15} cm^{-2} for nSD and $BF2^+$, 40 keV, 2×10^{15} cm^{-2} for pSD. (8) Next, post metal annealing (PMA) for S/D activation and ferroelectric crystallization of HZO are carried out [**Figure 4.1**(g)]. (9) The process is completed with back-end-of-line (BEOL) process including inter-layer dielectric (ILD) deposition using tetraethyl orthosilicate (TEOS), contact hole etching, and metal [Ti (300 A) / TiN (300 A) / Al (2000 A) / TiN (300 A)] deposition / pad patterning [**Figure 4.1**(h)].

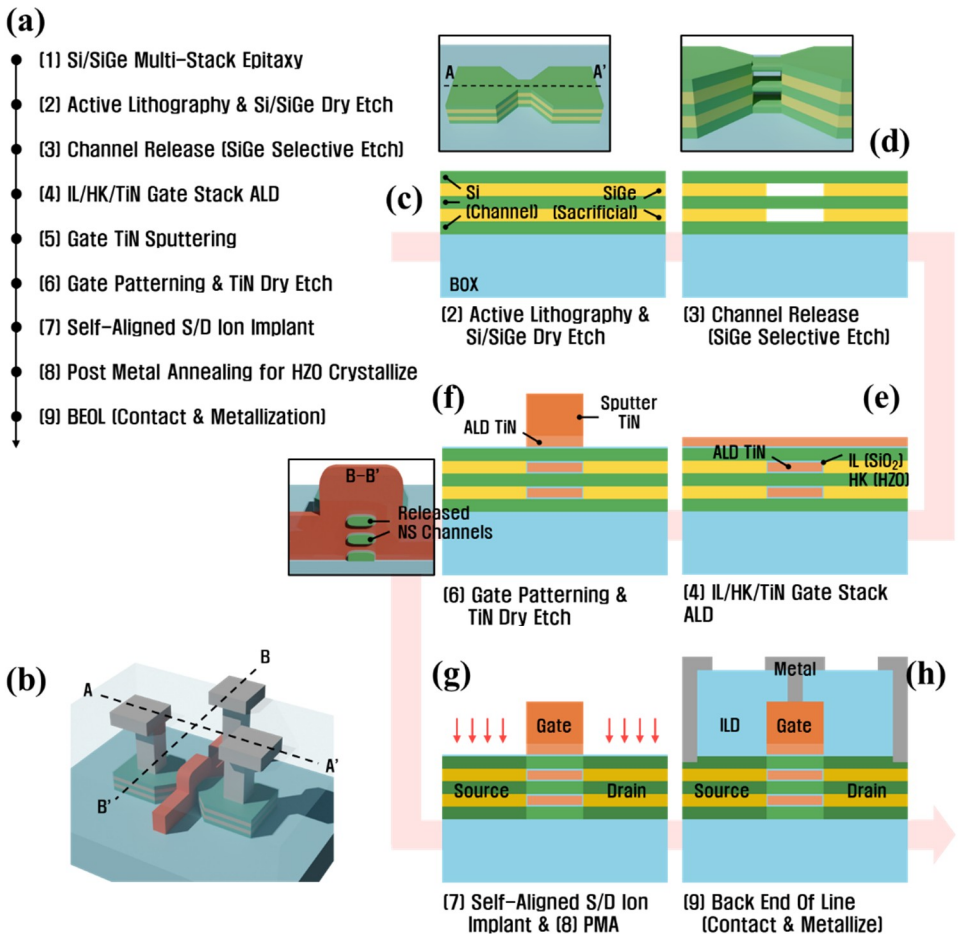


Figure 4.1. (a) Summarized process flow of initially designed NS GAA NCFET fabrication. (b) 3D schematic image of NS GAA NCFET. (c)-(h) Cross-sectional schematic images of several key fabrication steps.

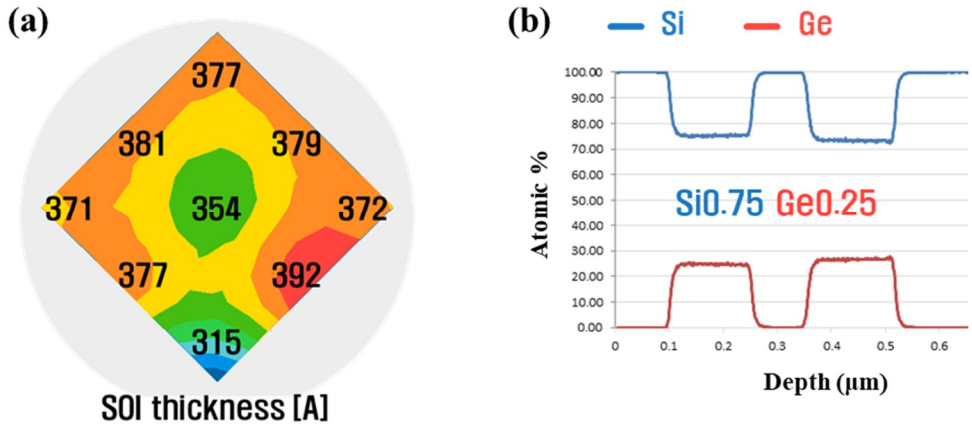


Figure 4.2. (a) Silicon-on-insulator (SOI) thickness thinned from 1000A to ~350A. (b) Atomic percent (Si and Ge) profile of SiGe/Si/SiGe/Si multi-stacked epitaxy test wafer.

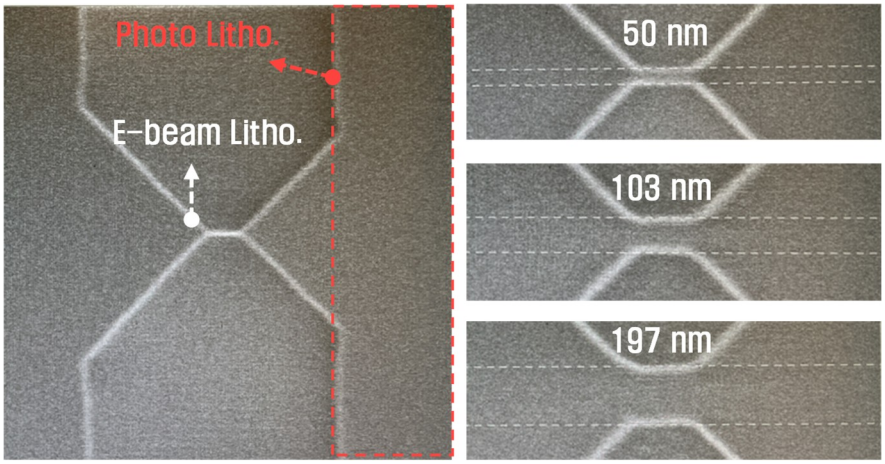


Figure 4.3. Top-viewed SEM image after active patterning (photo / e-beam lithography and Si/SiGe dry etching). Actives with width of 50 nm, 100 nm, 200 nm are clearly defined by e-beam lithography.

4.2 Process Issues and Solution

Several issues that occurred with the simple gate-first method described in the Section 4.1 were found. The first issue is the relatively large resistance caused by the low dopant activation temperature; the second is the gate-induced-drain-leakage (GIDL) issue owing to the TiN spacer remaining on the active sidewall after the TiN gate etching. In addition, GIDL issues caused by unintentional etching of SiGe exposed in the region other than the channel can be expected during the channel-release process. This chapter describes the analysis and solutions for such problems.

4.2.1 External Resistance

Figure 4.4 shows the I_D-V_G characteristics at V_D = 0.05 V and 0.5 V of the SOI planar FET fabricated with the initial process excluding the channel release process. The linear scaled current characteristic reveals that the current is quickly saturated, indicating that the external resistance is extremely large. As seen in Subsection 3.2.1, MOSFET's on-resistance (R_{ON}) consists of the components depicted in **Figure 3.8**(b). Since the PMA temperature for HZO crystallization (500℃) is insufficient to completely activate S/D, both R_{SD} and R_{CNT} are predicted to be considerable. It is required to minimize the influence of external resistance ($R_{External}$) in order to confirm the intrinsic current enhancement at operation voltage.

To solve this issue, as depicted in **Figure 4.5**(a), non-self-aligned S/D ion implantation (1st ion implantation) and high-temperature activation were performed prior to the gate stack. Here, non-self-align S/D doping was conducted somewhat further (~350 nm) than the region where the gate would be produced. Note that the self-aligned S/D ion implantation was additionally performed after the gate stack formation. **Figure 4.5**(b) compares the I_D-V_G characteristics of SOI planar FET subjected to 1st S/D doping and high temperature annealing and FET fabricated with initial process. Since the 1st S/D dopant was sufficiently activated, $R_{External}$ including R_{CNT} and R_{SD}, was reasonably lowered, leading to the current not being saturated even in the high V_G area. The R_{ON} calculated from the current characteristic is illustrated in **Figure 4.5**(c), from where the extracted $R_{External}$ was confirmed to be dramatically improved to ~1/30. It should be noted that the dopant activation annealing, which is performed after the 1st S/D ion implantation, should be performed right after the channel release process (before the gate stack), taking into account Ge intermixing [18].

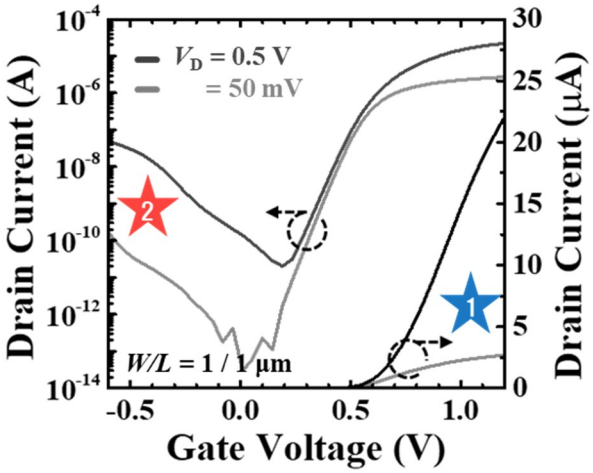


Figure 4.4. I_D-V_G characteristics of SOI planar FET fabricated with initial process excluding the channel release process: two major issues are represented. (1) Early current saturation at operation V_G due to large external resistance especially remarkable at low V_D (50mV). (2) Large GIDL current at negative V_G region.

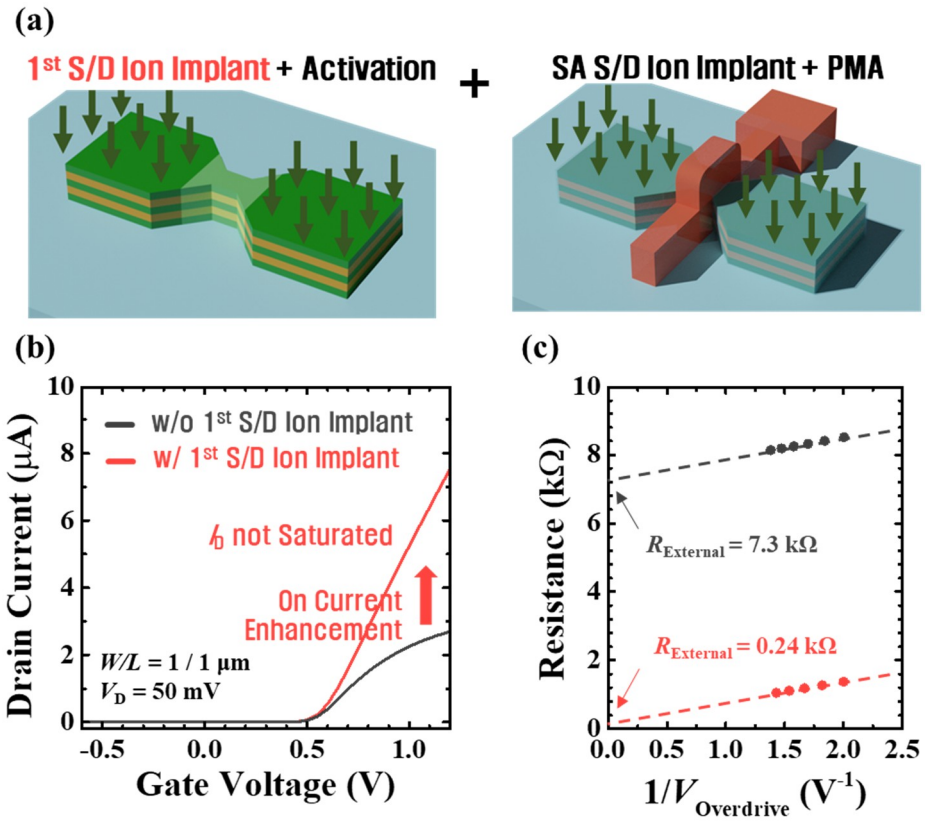


Figure 4.5. (a) Schematic images of revised process for external resistance reduction: 1st S/D ion implant and high temperature activation before the gate stack formation. (b) Transfer characteristics of SOI planar FETs with initial / revised process. (c) External resistance of two devices extracted by $1/V_{OV}$ method.

4.2.2 TiN Gate Sidewall Spacer

Figure 4.4 further demonstrates that the GIDL current is relatively high, particularly remarkable at high V_D. GIDL current is highly likely to occur in the gate-to-drain overlap region. As can be seen from the top-viewed SEM image and 3D schematic image [**Figure 4.6**(a) and (b)] after TiN gate dry etching, TiN spacer remains along the active sidewall. The remaining IL/high-κ/gate stack along the doped Si region leads to the increase of the overlap area between the gate and S/D. Considering the considerably large S/D active pad area (several hundreds of μm in length), it must be removed completely. Especially in the case of the GAA process, as the overall height of the epitaxy with multi-stack is considerably high (approximately 1800 A), TiN sidewall spacer is more difficult to be removed, of which the effect is anticipated to be more significant. To solve this issue, increasing the amount of TiN over-etching during gate dry etching can be considered as a first step. Nonetheless, given the Si as well as HfO and SiO selectivity of the existing ISRC metal etch recipe is quite poor, excessive over-etching would bring the danger of S/D region etching. **Table 4.1** compares the Al etch recipe (existing ISRC metal etch recipe) with the newly optimized TiN etch recipe for achieving adequate selectivity, where the rate of physical etching was lowered by reducing the DC power. The etch rate and the selectivity of each recipe for several types of SiO and ALD HfO are shown in **Figure**

4.7. Although the etch rate was drastically reduced as a result of the decrease of physical etching, it was determined that the selectivity was dramatically enhanced as a result of the increased dominance of chemical etching. The selectivity of SiO and HfO was confirmed to be 20 and 46, respectively; thus, it is expected that the TiN spacer remaining on the active sidewall can be partially removed by sufficient over-etching. However, the top-viewed SEM image [**Figure 4.8**(b)] indicated that a part of the TiN spacer formed on the active sidewall containing ALD-deposited TiN remained even after over-etching. For complete removal of the remained TiN spacer, additional TiN wet etching using hydrogen peroxide (H_2O_2) was conducted after the TiN dry etching as illustrated in **Figure 4.8**(a). It should be considered that since the gate length (L) defined by e-beam lithography is relatively small, the amount of additional wet etching should be minimized. The in-line top-viewed SEM monitoring was conducted during the TiN wet trimming, of which the etch rate was confirmed to be 10 nm/min in diluted H_2O_2 (1:4, 60℃) solution. After 5 minutes of wet etching, it was determined that the TiN spacer was fully removed, as illustrated in **Figure 4.8**(c). **Figure 4.8**(d) depicts the logarithmic I_D-V_G curves of SOI planar FET subjected to additional TiN wet etching and FET without additional TiN wet etching. It was found that the GIDL current was lowered by more than 2-decades. Note that the on-current increase is due to the simultaneous application of 1st S/D ion implantation and high temperature activation in this experiment.

In summary, SOI planar FET fabricated with initially planned gate-first process suffered from the external resistance issue due to the low activation temperature and the GIDL issue due to the TiN sidewall spacer, which were resolved with additional processes including 1st S/D doping and TiN over etching / wet etching.

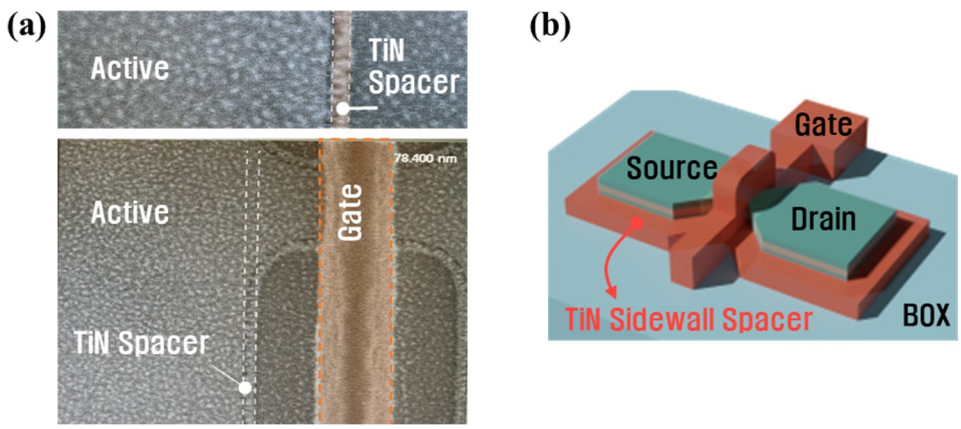


Figure 4.6. (a) Top-viewed SEM image after gate dry etching, where the TiN spacer remained along the active region is remarkable. (b) 3D schematic image after the gate dry etching.

Table 4.1. ISRC ICP metal etcher recipe (existed Al etch and new TiN etch recipe)

	Al Etch RCP	TiN Etch RCP
Cl_2 (sccm)	30	70
BCl_3 (sccm)	20	-
DC Power (W)	100	25

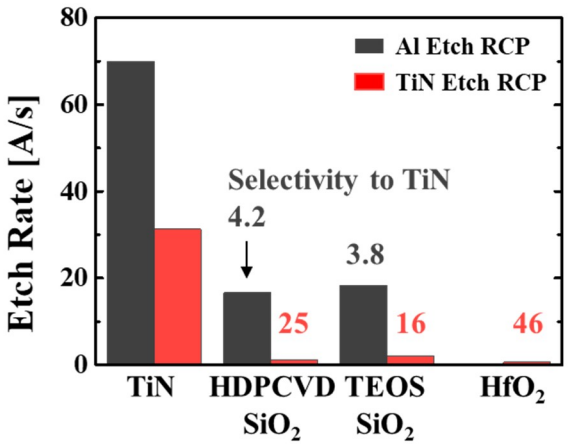


Figure 4.7. Etch rate of ISRC ICP metal etcher recipes (existed Al etch recipe and new TiN etch recipe) for TiN and several dielectrics.

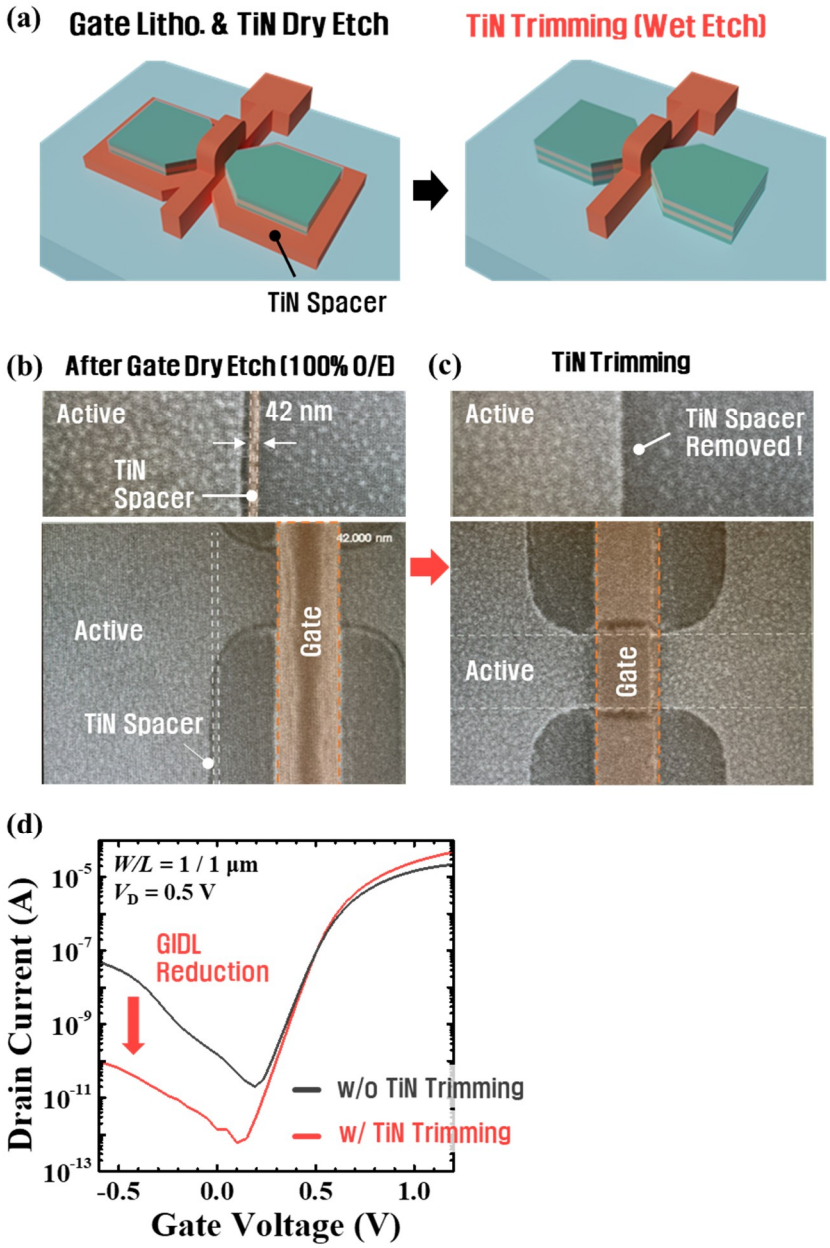


Figure 4.8. (a) 3D schematic image of TiN wet trimming after gate dry etching. Top-viewed SEM image of SOI planar FET (b) after TiN dry etch (100% over etching using new TiN etch recipe) and (c) after TiN trimming (d) Transfer characteristics of SOI planar FETs with initial / revised process.

4.2.3 Unintentionally Etched Sacrificial Layer

Another problem that can be anticipated when fabricating a GAA structure with a suspended channel through the initial process is the unintentionally etched SiGe region. The I_D-V_G characteristic of the NS GAAFET is depicted in **Figure 4.9**(a), where the considerable GIDL current is observed despite the additional TiN trimming.

Figure 4.9(b) and its enlarged image [**Figure 4.9**(c)] exhibits the tiled-viewed SEM image of the structure after the channel release process. Although the sacrificial layers between channels are completely removed, the sacrificial layer of region outside the channel [e.g., S/D extension and pad region, marked with slash lines in **Figure 4.9**(c)] was also etched unintentionally. The gate stack will be filled in these doped Si / SiGe S/D region, resulting in a huge gate-to-S/D overlap area, which is assumed to be the reason the GIDL current was increased in the NS GAA FET in **Figure 4.9**(a). This issue also only occurs in the gate-first process, since the selective etching is proceeded after the dummy gate is removed, where only the channel region is exposed in the gate-last process. In order to alleviate this issue, a lithography process covering the area outside the channel was added, similar to selective etching in the gate-last process, as described in **Figure 4.10**(a) and (b). Obviously, although the opening region is quite greater than the designed L (100 ~ 300 nm) since the i-line photolithography without self-aligning is used, it is expected that the blocking

photo resist (PR) could cover the huge S/D pad area adequately.

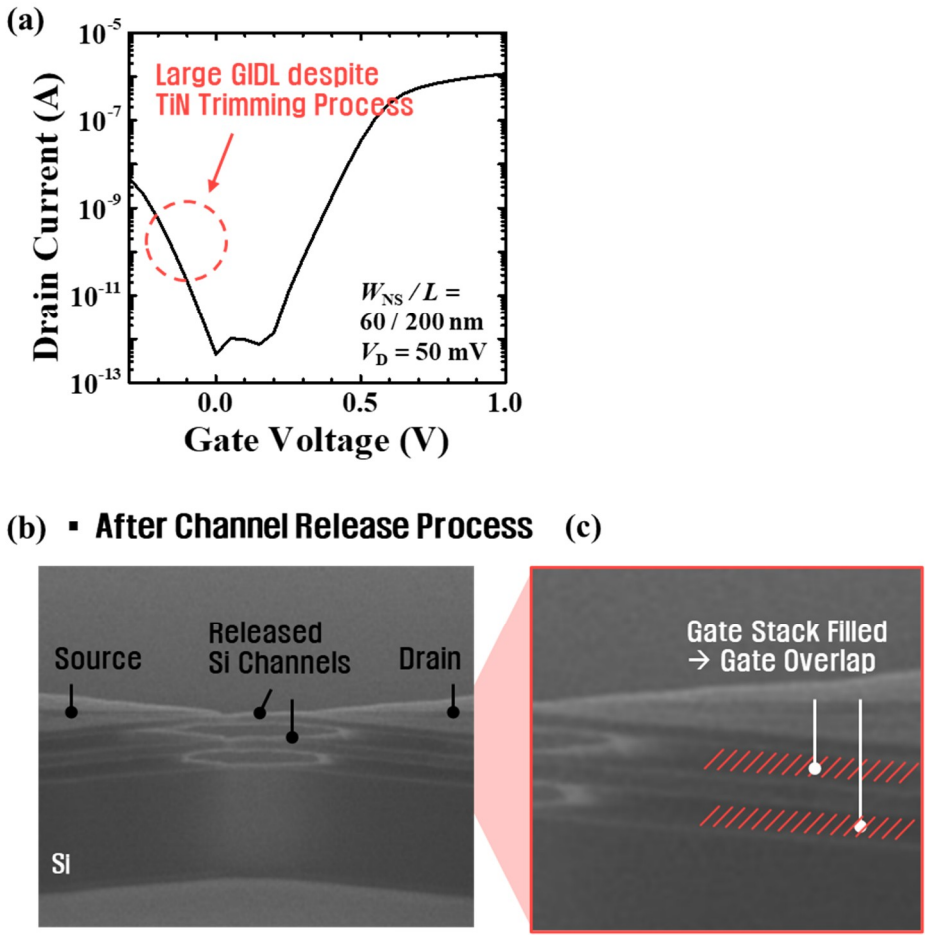


Figure 4.9. (a) I_D-V_G characteristic of fabricated NS GAA FET with initial channel release process. (b) Tilted-viewed SEM image after channel release

process and (c) its enlarged image.

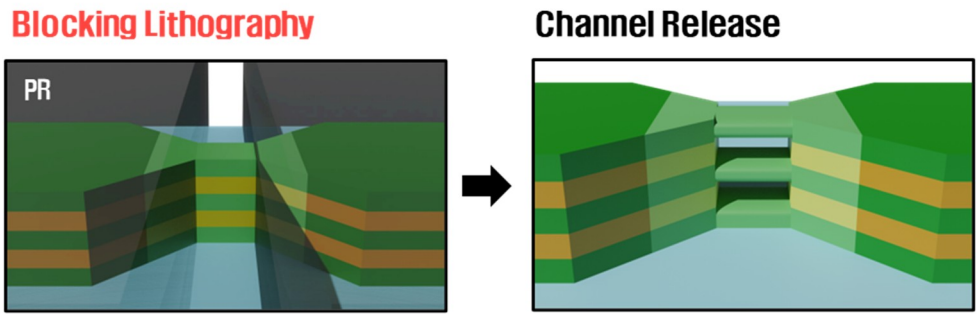


Figure 4.10. Schematic image of solution for initial channel release process: blocking lithography for channel release, which hinder the sacrificial layers located out of the channel region from being unintentionally etched.

4.2.4 Discussions

The three issues discussed in Section 4.2 are all caused by the gate-first methodology; they may not arise in replacement metal gate process being employed in advanced CMOS technologies. First, since S/D formation including ion implantation or in-situ doping epitaxy and high temperature annealing is conducted after dummy gate patterning (before HZO deposition, which has low thermal budget), the problem regarding insufficient dopant activation indicated in Subsection 4.2.1 can be eased. Second, ALD gate stack deposition is accomplished after sequential ILD deposition, chemical mechanical polishing (CMP) of ILD, and dummy gate removal; hence, there is no issue with the TiN sidewall spacer as addressed in Subsection 4.2.2. Lastly, since the channel release process is conducted with the dummy gate removed, i.e., only the channel region is exposed, the problem of exposed S/D SiGe layer discussed in Subsection 4.2.3 no longer exists.

Since it is difficult to implement the gate-last method in manufacturing a device with a relatively short channel at the university fab level, part of this dissertation tries to obtain sufficient current characteristics by solving the problems as much as feasible, while using the simple gate-first approach. Therefore, with the gate-last technique, enhanced characteristics with more stable processes in the fabricated NS GAA NCFETs would be achievable.

4.3 Channel Release Process

4.3.1 Consideration in Channel Release Process

The channel release process to make a single crystalline silicon GAA channel starts with repeatedly-stacked epitaxial growth of Si, a channel material, and silicon germanium (SiGe), a sacrificial layer, which is followed by the selective etching of sacrificial SiGe after the active patterning. In this study, a silicon-on-insulator (SOI) substrate was utilized, and epitaxial growth was conducted after thinning a wafer with a 100-nm-thick SOI layer to around 37-nm-thickness. Epitaxial growth was performed on the SOI layer, as follows: $Si_{0.75}Ge_{0.25}$ (40 nm) / Si (30 nm) / $Si_{0.75}Ge_{0.25}$ (40 nm) / Si (30 nm), as addressed in **Figure 4.2**(a) and (b).

Prior to the development of the technology for SiGe selective etching, structural stability of the released channel was considered. As illustrated in **Figure 4.10**(b), the released Si channel is suspended in the large S/D region. Here, the released channel is physically unstable and highly likely to bend or collapse if the suspended length (L_{SUS}) is too long, hence it is necessary to examine the requirement of L_{sus}. For a simple experiment, SiO_2 (sacrificial) / a-Si (channel) / SiO_2 / a-Si multi-stacks were sequentially deposited using chemical vapor deposition (CVD), and active patterning was performed with different L_{sus}s. Afterwards, a channel release process was

performed through SiO_2 wet etching using a 7:1 buffered HF solution [**Figure 4.11**(a) and (b)]. **Figure 4.11**(c) is a cross-sectional transmission electron microscopy (TEM) image of a sample exposed to SiO_2 selective etching after active patterning with L_{sus} = 1μm, which confirmed that the L_{sus} of 1 μm was too long to ensure structural stability of the suspended channel. As seen in **Figure 4.11**(e), the released channel also likely to bend if L_{sus} is too long [90]. When the L_{sus} was lowered to 250 nm, as shown in the TEM image of **Figure 4.11**(d), the two-layer Si channel was confirmed to be stably released. It was determined that supporting fixtures should be designed fairly closely (L_{sus} < 250 nm) using a e-beam lithography.

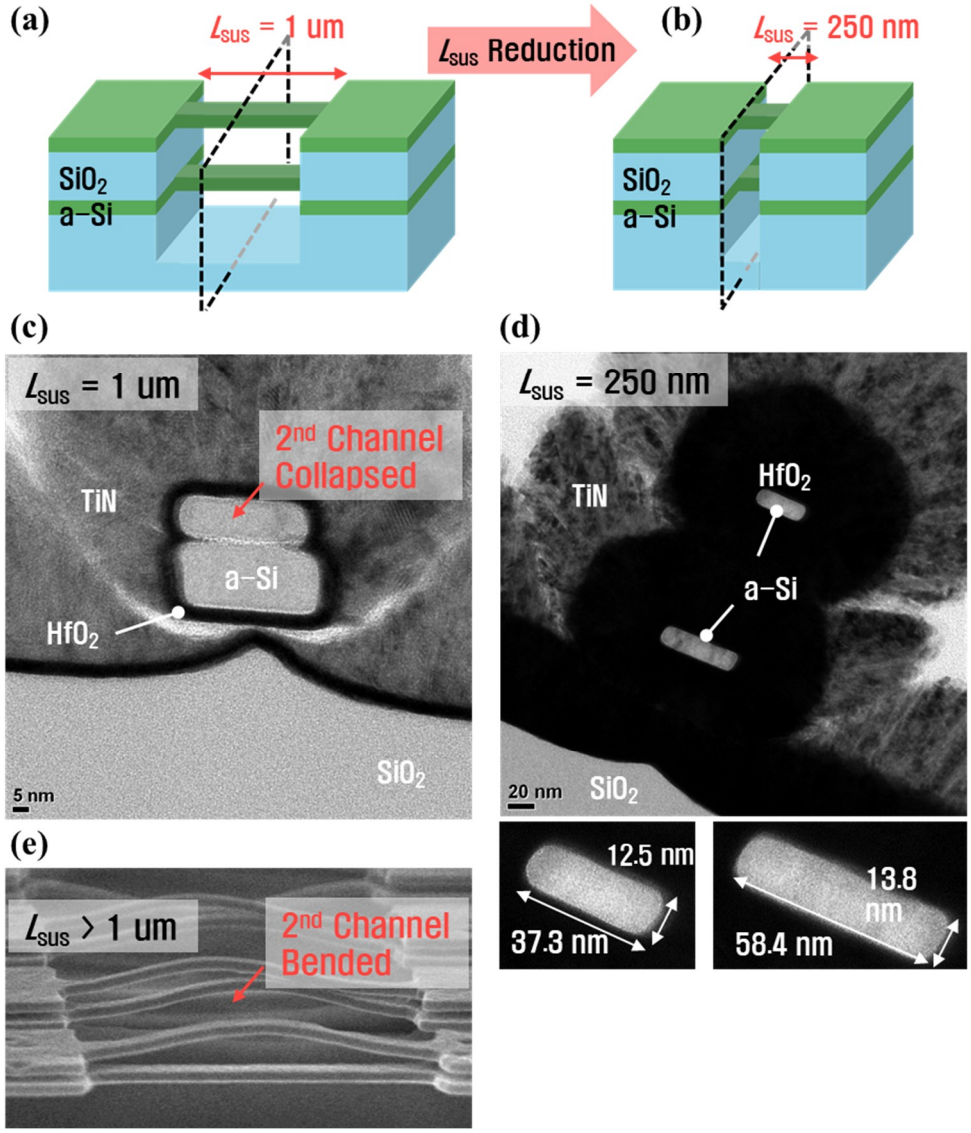


Figure 4.11. Schematic images of experiment for the structural stability of suspended channel with (a) long and (b) reduced L_{SUS} (1 μm and 250 nm). Cross-sectional TEM images of structure after the channel release process with (c) L_{SUS} = 1 μm and (d) 250 nm. (e) Tilted-viewed SEM image of released channel with L_{SUS} > 1 μm [90].

4.3.2 Methods for SiGe Selective Etching

The reported SiGe selective etching methods include chemical dry etching (CDE) using plasma [91, 92], hot HCL etching [91], and wet etching [91, 93-98]. SiGe selective etching in CDE utilizes CF_4 / O_2 / N_2 gas. The reaction of the radicals with the surface is called CDE. When SiGe and Si are exposed simultaneously to fluorine species, SiGe is preferentially etched due to the difference between Si–Si and Si–Ge binding energies (2.31 and 2.12 eV, respectively) [92]. The CDE conditions used in the research are summarized in **Table 4.2**. Note that since the designed nanosheet width (W_{NS}) ranges between 50 and 200 nm, the etch goal was set to 100 nm per side based on the maximum W_{NS}. **Figure 4.12** depicts the results (SEM image in cross-section) of selective etching using CDE on repeating epi-stacked wafers of which the Ge composition rate of SiGe was 25%. It was confirmed that with the CF_4 flow rate of 80 sccm [99], SiGe etch rate (E/R =200 A/s) was considered to be difficult to control [**Figure 4.12**(a)], while the lowered flow rate (15 sccm) exhibits the adequate E/R (38 A/s) [**Figure 4.12**(b)]. However, **Figure 4.12**(b) indicates that the selectivity with Si is insufficient, whereas **Figure 4.12**(c) shows that the Si layer is largely damaged by plasma, which concludes inadequacy of CDE for stable released Si NS channel.

Table 4.2. Process condition of CDE for SiGe selective etching.

Power (W)	Pressure (mTorr)	CF4 (sccm)	O2 (sccm)	N2 (sccm)
700	350	15	12	12

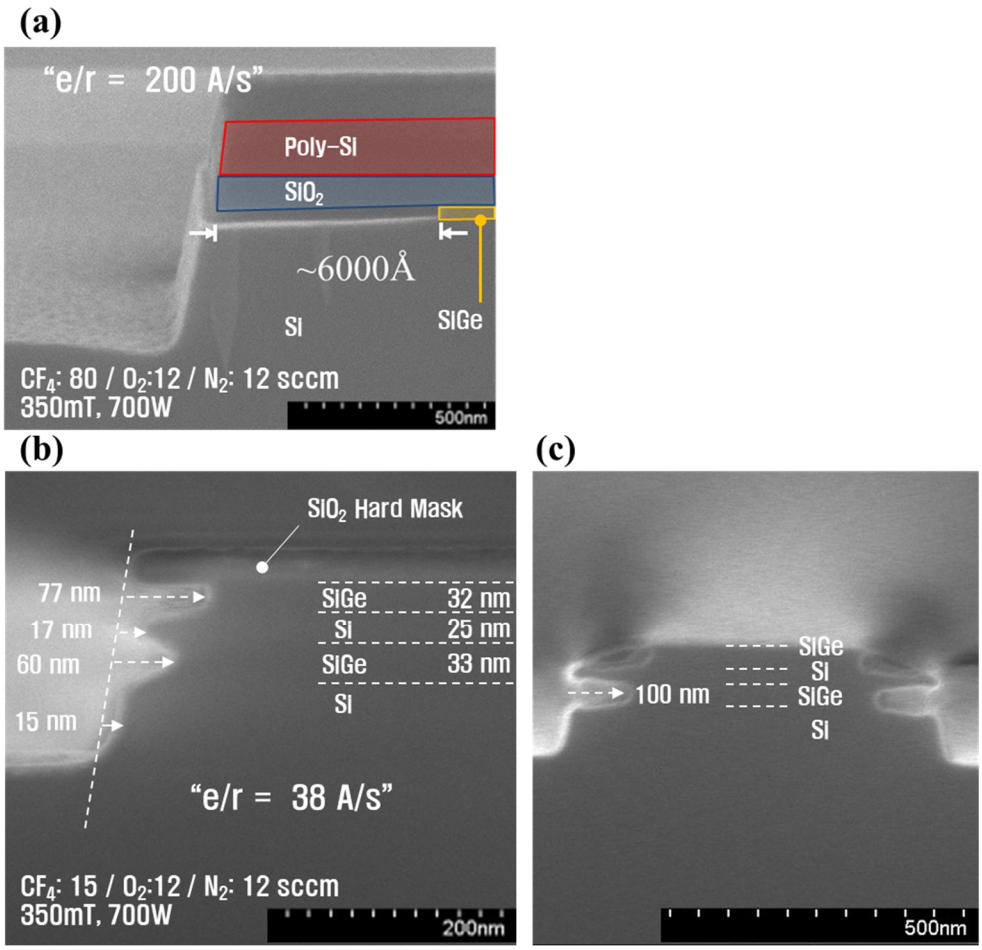


Figure 4.12. Cross-sectional SEM images after SiGe selective etching using CDE with CF_4 flow rate of (a) 80 sccm [99] and (b)/(c) 15 sccm (reduced).

Among the approaches of SiGe selective wet etching, a mixture of NH_4OH / H_2O_2 / H_2O also known as standard cleaning-1 (SC-1) solution has been reported [93], which utilizes the oxidation of Ge by H_2O_2 (faster than that of Si) and removal of GeO. **Figure 4.13** represents a cross-sectional SEM image of SiGe / Si epitaxy structure after the SiGe selective etching in the wet solution [NH_4OH : H_2O_2 : H_2O (1 : 8 : 64) at 65℃] for 30 minutes. Although the solution exhibits high selectivity to Si, the E/R of 10 A/min is too slow considering the designed W_{NS}.

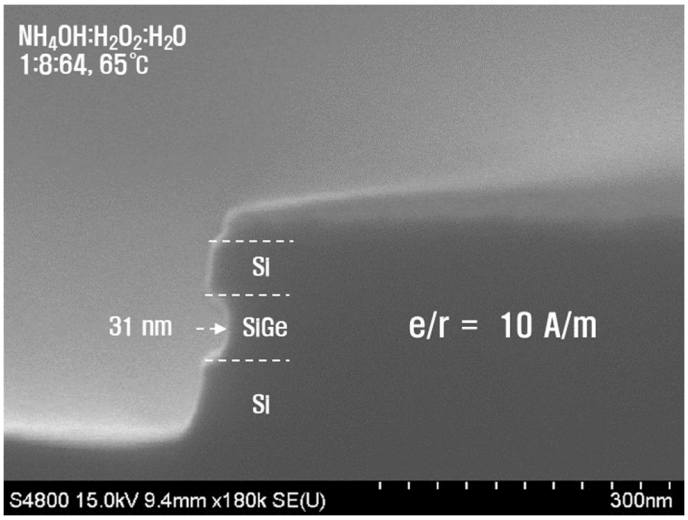


Figure 4.13. cross-sectional SEM image after SiGe selective etching with 1:8:64 SC-1 solution.

4.3.3 SiGe Selective Etching using Carboxylic Acid Solution

Another wet-etching approach for isotropic SiGe selective etching is carboxylic acid (R-COOH) wet etching [94-96, 98], which utilizing a chemical reaction between R-COOH and Ge. The reaction equation for etching SiGe using a solution composed of CH_3COOH (R-COOH) / H_2O_2 / HF is shown below [98].

$$CH_3COOH + H_2O_2 \rightarrow CH_3COOOH + H_2O_2 \quad 3.1$$

$$Ge + 2CH_3COOOH + 2e^- \rightarrow Ge^{2+} + 2CH_3COO^- + 2OH^- \quad 3.2$$

Equation 3.1 represents the reaction that produces peroxyacid (R-COOOH), which reacts with Ge as Equation 3.2. Considering the number of moles of CH_3COOH and H_2O_2, a mixture of a 49% HF : 30% H2O2 : 99% CH3COOH (weight ratio) was prepared with a volume ratio of 2:160:50. On the other hand, it is known that the reaction rate of Equation 3.1 is quite slow, which leads to the change of E/R according to the aging time [98]. It was determined through the experimentation that e/r was saturated after approximately 96 hours (4 days) [**Figure 4.14**(d)]. **Figure 4.14**(a)-(c) depicts the cross-sectional SEM images of the epitaxy structure after the R-COOH wet etching. By measuring the Si E/R of the solution via comparing the Si thicknesses of epi-grown region and the exposed region in **Figure 4.14**(c), a high etch selectivity (approximately 55:1) was verified, which is maintained regardless of the aging duration [**Figure 4.14**(a)-(c)]. The E/R of 180 ~ 380 A/min depending on the aging

time is controllable level, considering the W_{NS}. **Figure 4.15**(a) and (b) depict a tilted SEM image of a structure exposed to a channel release procedure using R-COOH wet etching after the active formation with a L_{sus} of 250 nm, which confirms the stable suspended Si NS channel.

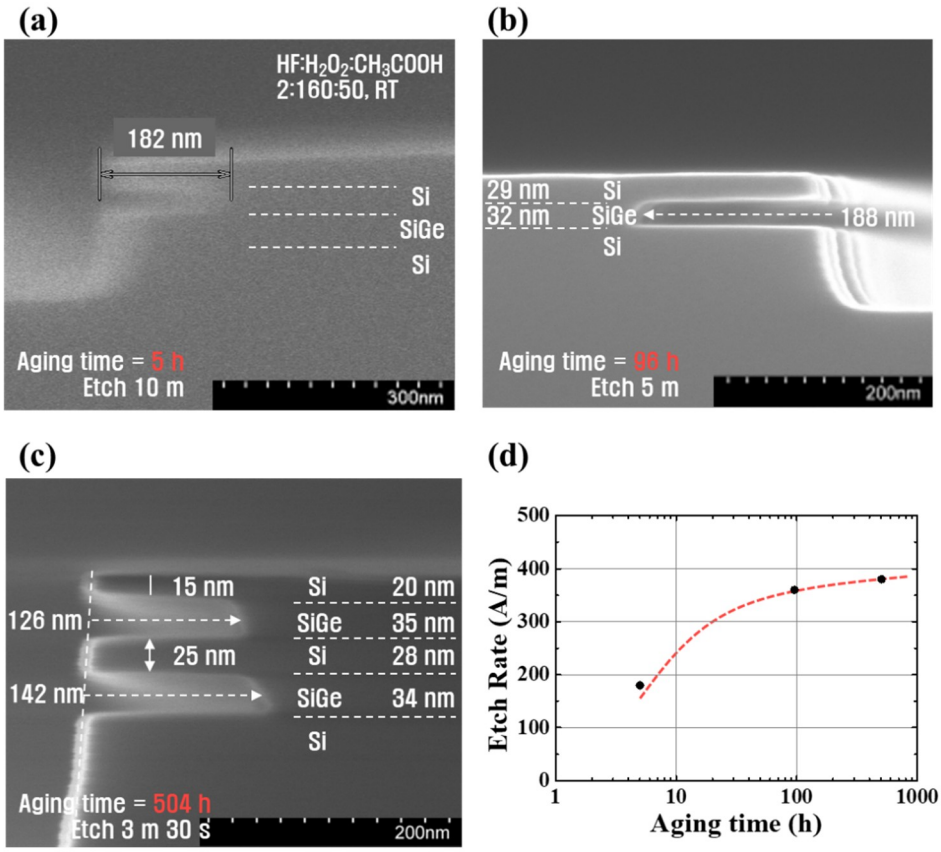


Figure 4.14. Cross sectional SEM images after SiGe selective etching using carboxylic acid solution (HF : H_2O_2 : CH_3COOH = 2 : 160 : 50 at room temperature) of which aging times are (a) 5 hours, (b) 96 hours and (c) 504 hours. (d) SiGe etch rate in the solution according to the aging time.

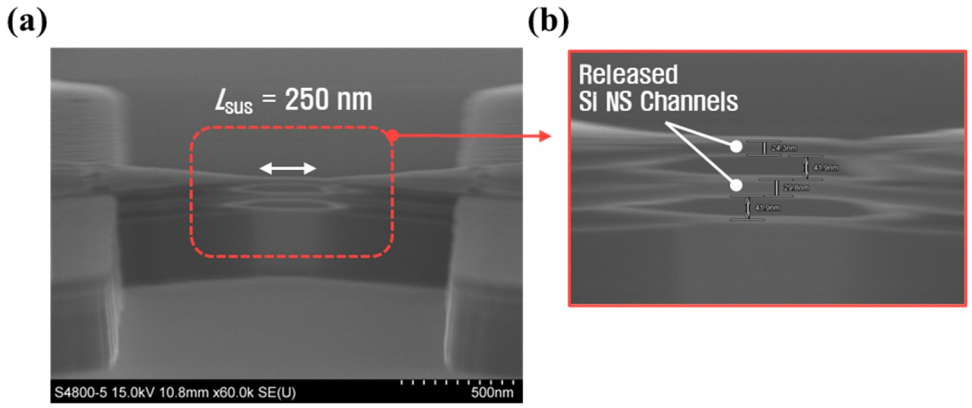


Figure 4.15. (a) tilted-viewed SEM image of released NS channels of which L_{SUS} = 250 nm after the active patterning by photo / e-beam mix-and-match lithography. (b) enlarged image of (a).

4.4 Revised Process of NS GAA NCFET

The final process flow including additional processes for the solution to the three issues discussed in Section 4.2 is described in **Figure 4.16**. Starting from a multi-stacked epitaxy wafer of SOI / SiGe / Si / SiGe / Si, 1st S/D implantation (As^+, 20keV, 2×10^{15} cm^{-2} for nSD and BF_2^+, 20keV, 2×10^{15} cm^{-2} for pSD) was introduced to lower external resistance after active formation [**Figure 4.16**(c)]. Before the channel release procedure, blocking lithography was conducted to eliminate the gate-to-S/D overlap resulting from the unintentionally etched SiGe region [**Figure 4.16**(d)]. After releasing the channel using SiGe selective etching by R-COOH solution, the 1st S/D dopant was activated by high temperature (900℃, 10s) rapid thermal annealing (RTA) [**Figure 4.16**(e)]. In order to lower the GIDL current induced by the remained TiN spacer after gate dry etching, a TiN trimming process was implemented [**Figure 4.16**(f)]. The subsequent self-aligned S/D ion implantation (P^+, 40keV, 2×10^{15} cm^{-2} for nSD and BF_2^+, 40keV, 2×10^{15} cm^{-2} for pSD) and PMA (500°C, 30s) for HZO crystallization are identical to the initial process [**Figure 4.16**(g)]. Note that using P^+ as the nSD dopant is advantageous in that the dopant activation rate of high dose at low temperature is comparably larger than As^+ [100], as well as the lattice damage caused by ion implantation is less. After the PMA process for HZO crystallization, the fabrication was finished through the BEOL process in the same manner as the initial process [**Figure 4.16**(h)].

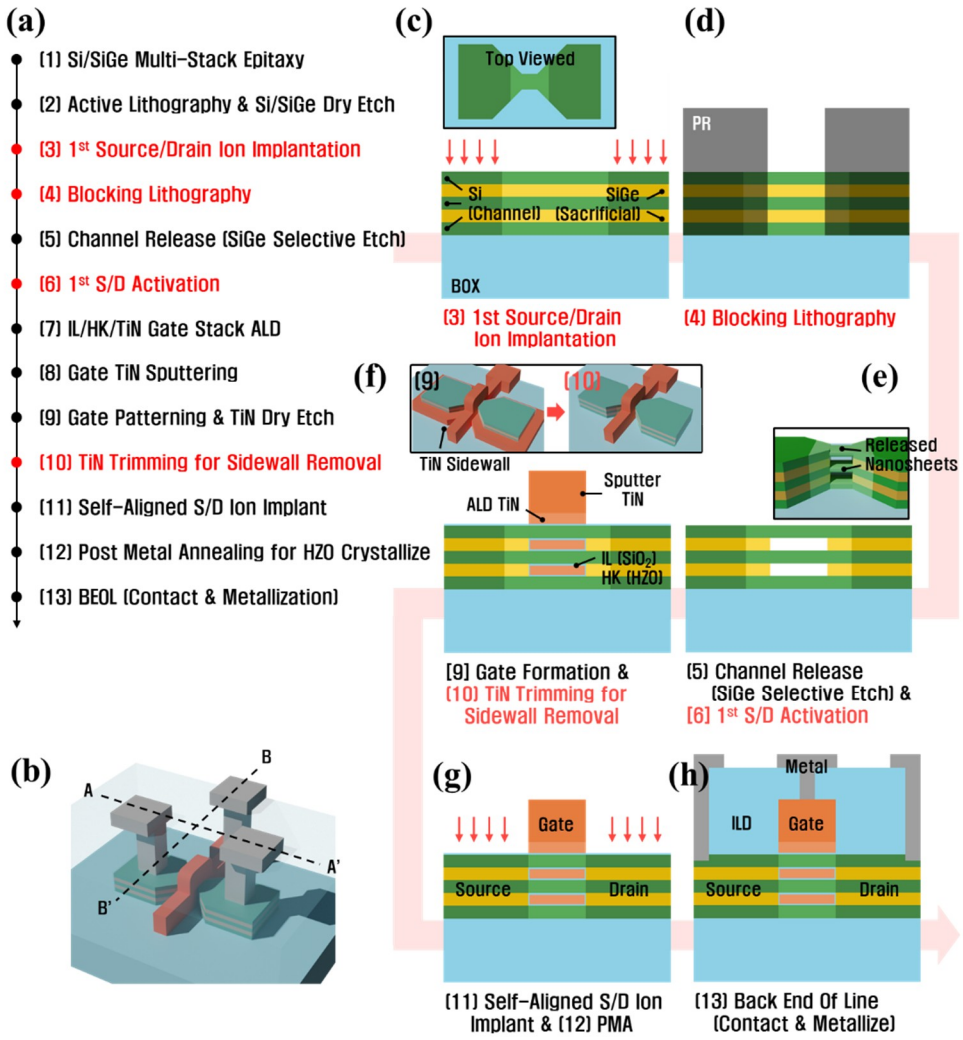


Figure 4.16. (a) Summarized process flow of revised NS GAA NCFET fabrication. (b) 3D schematic image of NS GAA NCFET. (c)-(h) Cross-sectional schematic images of several key fabrication steps.

Figure 4.17 depicts the gate direction cross-section [B-B' of **Figure 4.16**(b)]-viewed TEM image of the fabricated stacked NS GAA NCFET. The 2-layer Si NS channels were confirmed to be released above the SOI channel, while the channel thickness was measured as 25 nm for 1st Si layer and 18 nm for 2nd layer, respectively. Different from the epitaxy target (SiGe 40 nm and Si 30 nm), it was found that the actual epitaxial-grown thickness of Si layers became thinner as epitaxy progressed (as also examined in **Figure 4.14**). In addition, the 2nd Si layer would have been thinned, since it was exposed to selective etchant without any hard mask on top, which should be optimized for ensuring identical channel thickness. Furthermore, it is confirmed that the NS width of the 2nd Si channel is smaller due to the etch slope in active dry etching, which should also be solved by optimizing the etch conditions. Also, one can recognize that the space between the 1st Si channel and the 2nd Si channel is also different than expected (i.e., the thickness of the sacrificial layer), which is likely owing to the difficulty in maintaining the physical stability of the thinned Si layer in a suspended architecture. As demonstrated by the magnified TEM image [**Figure 4.17**(c)], the ALD gate stack was deposited as intended: ALD SiO_2 (15 cycles) and HZO (34 cycles) were deposited 1 nm and 3.2 nm, respectively. In addition, the poly crystallization of HZO by PMA was validated [doted rectangle in **Figure 4.17**(c)]. From the 2D material mapping data obtained by Energy-Dispersive X-Ray Spectroscopy (EDS) analysis [**Figure 4.17**(d)], it was

determined that the ALD gate stack entirely wraps the released NS channels. In addition, 1D (line) atomic percent data obtained by EDS analysis [**Figure 4.17**(e)] revealed that the SiGe layer was totally eliminated through adequate selective etching and the Hf and Zr composition rate was 24% and 76% in HZO stack. **Figure 4.18**(b) and (a) represent the channel direction cross-section [A-A' of **Figure 4.16**(b)]-viewed TEM image of the fabricated stacked NS GAA NCFET and corresponding 2D material mapping data acquired by EDS analysis. It should be noticed that the SiGe layer was over-etched to the S/D direction and correspondingly the gate stack was filled deeper, resulting in the longer gate length between the channels than intended length, i.e., top gate length. This would not have happened with the epitaxy Si S/D technique, which is used in the industrial advanced logic fabrication.

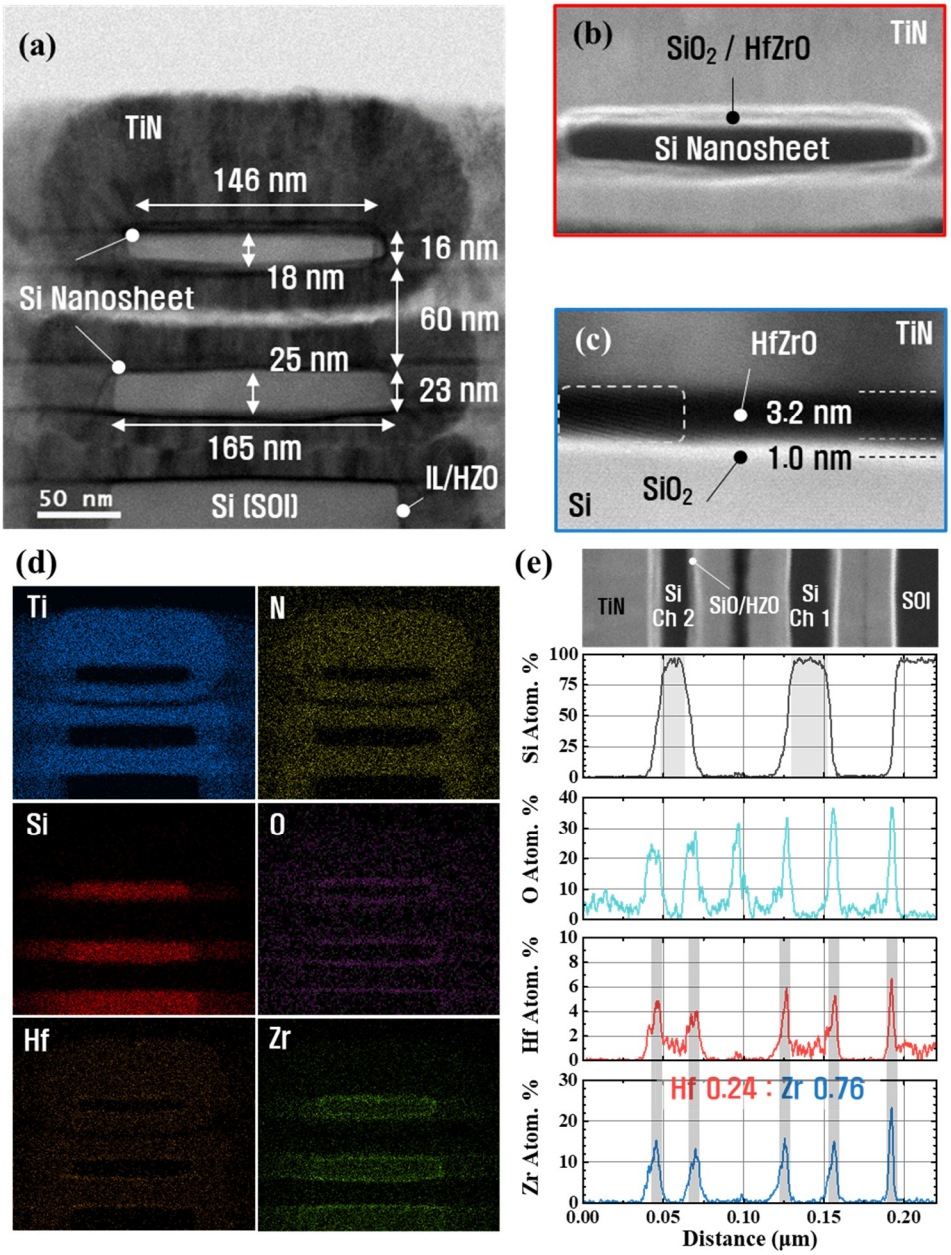


Figure 4.17. (a) Cross-sectional [B-B' direction of **Figure 4.16**(b)] TEM image of 2-stacked Si NS GAA NCFET. Enlarged TEM image of (b) 2nd (top) Si NS channel and (c) bottom Si (SOI). EDS analysis of 2-stacked Si NS GAA NCFET (d) 2D material mapping and (e) line mapping.

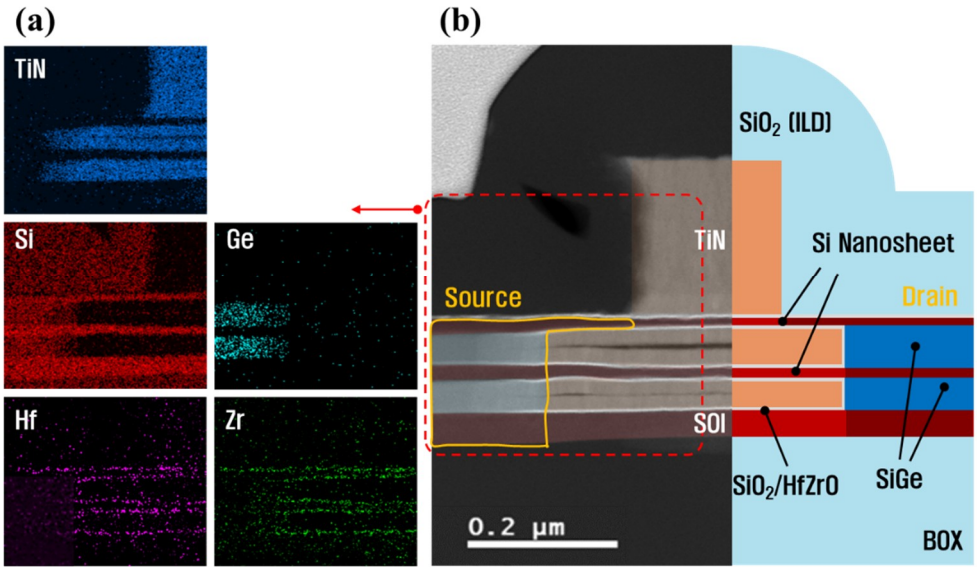


Figure 4.18. (a) EDS analysis of 2-stacked Si NS GAA NCFET [red dotted area of (b)]. (b) Cross-sectional [A-A' direction of **Figure 4.16**(b)] TEM image of 2-stacked Si NS GAA NCFET.

Chapter 5

Electrical Characteristics of Fabricated NS GAA NCFET

This chapter evaluates and analyzes the electrical properties of 2-stacked NS GAA NCFETs with mixed-phase NC HZO optimized in Chapter 3, fabricated using the processes discussed in Chapter 4. The gate electrostatic controllability of the NS GAA NCFET is assessed by comparing with the SOI planar NCFET evaluated in Section 3.2. In addition, the effect of HZO in the NS GAA structure is analyzed through the comparison with the HfO device fabricated with the same process, and various figures of merit are evaluated.

5.1 DC Characteristics

5.1.1 NS GAA NCFET vs. Planar SOI NCFET

Figure 5.1(b) shows the effective width (W_{eff})-normalized transfer characteristics of the SOI planar NCFET (W / L = 0.5 / 0.5 μm) analyzed in Section 3.2 and the fabricated NS GAA NCFET [W_{NS} = 50 / L = 240 nm, as shown in **Figure 5.1**(a)] at V_D = 50 mV (linear region) and 0.5 V (saturation region). In comparison to planar FET, the GAA structure exhibits a greater normalized drain current (I_D) thanks to the enhanced gate electrostatic controllability. However, a higher GIDL current can be observed in the GAA NCFET as a result of the structural issues stated in Subsection 4.2.3, which should be resolved by process optimization. Subthreshold swing (SS) according to the I_D [**Figure 5.1**(c)] also reveals the better gate controllability, where the 3-decades average SS (I_D/W_{eff} = 10^{-10} ~ 10^{-7} A/μm) was 70.3 and 64.5 mV/dec for planar and GAA NCFET, respectively. Note that the gate length (L) of GAA NCFET (240 nm) is much shorter than that of planar device (500 nm). **Figure 5.1**(d) compares the short channel effect (SCE) in two types of devices according to L. In this research, the drain-induced-barrier-lowering ($DIBL$) was calculated as

$$DIBL = \frac{V_{th,Lin} - V_{th,Sat}}{V_{D,Sat} - V_{D,Lin}} \quad 4.1$$

, where the V_{th} was defined as V_G at $I_D = 10^{-7}$ A × (W_{eff} / L), and the linear / saturation region represents the conditions of V_D = 50 mV and 0.5 V, respectively. Note that contrary to industrial logic technology, which uses in-situ S/D doping via epitaxy for junction formation, ion implantation was used in this study, making it difficult to verify the properties of devices with shorter Ls. The electrical characteristics of GAA devices with a L of 140 nm to 300 nm were analyzed and compared to the planar devices: a fairly low average *SS* of 60.67 mV/dec and a *DIBL* of 16.4 mV/V were observed in the device with L = 300 nm. From the **Figure 5.1**(d), greater L scalability was confirmed in GAA devices compared to the planar devices thanks to their excellent electrostatic controllability.

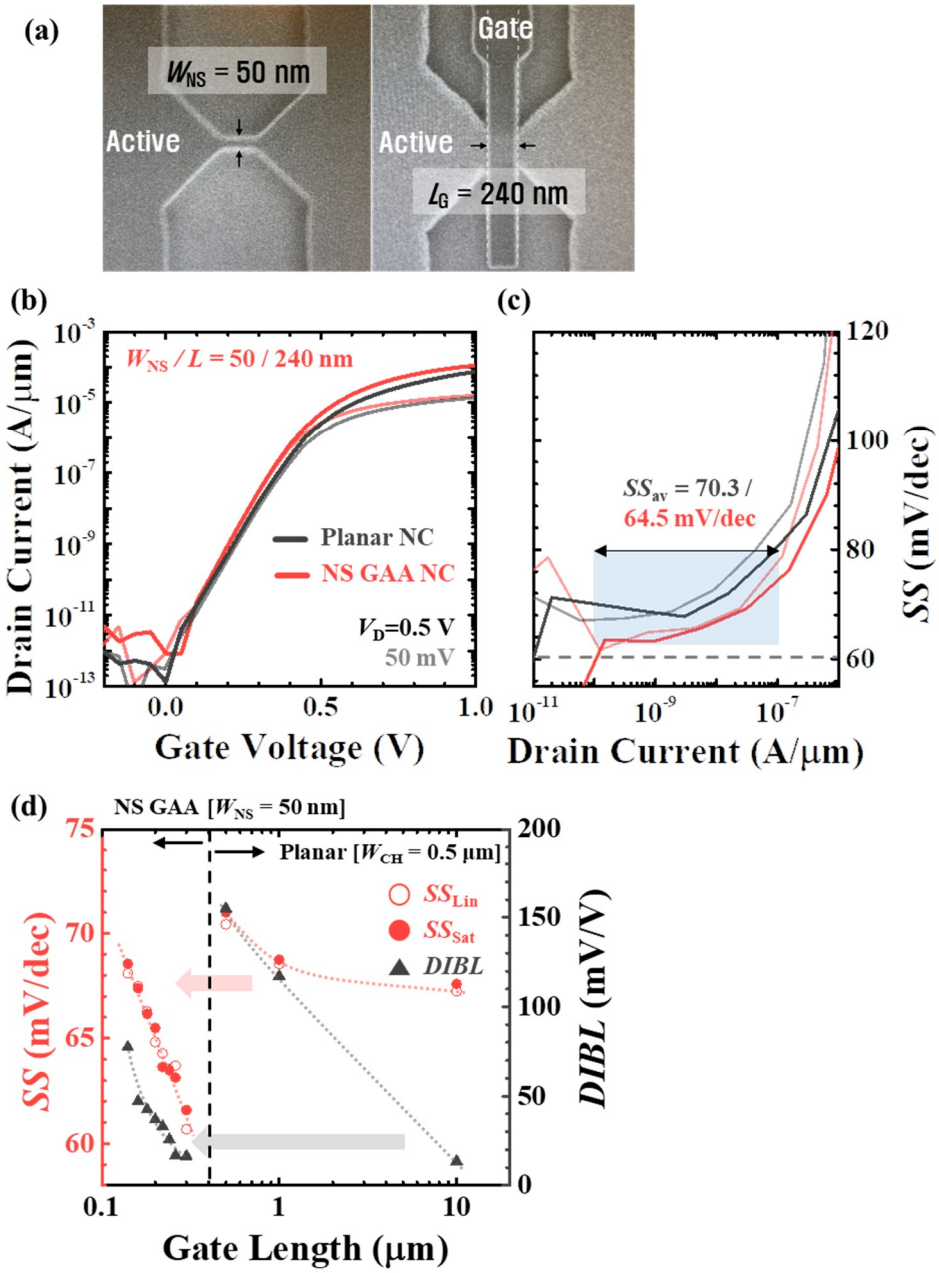


Figure 5.1. (a) Top-viewed SEM images representing e-beam defined W_{NS} and L. (b) I_D-V_G, (c) SS-I_D and (d) SS / $DIBL$ vs. L_G plots of NS GAA NCFET compared to the SOI planar NCFET (W / L = 0.5 / 0.5 μm).

5.1.2 Performance Enhancement of NS GAA NCFET

In order to investigate the capacitance boosting effect of the HZO NC thin film on the fabricated NS GAA NCFET, the current properties were compared with the reference pure HfO device fabricated in the same manner. **Figure 5.2**(a) and (b) depict the n- and p-type NS GAA NCFET transfer characteristics relative to the reference NS GAAFET at V_D = 50 mV (linear) and 0.5 V (saturation), respectively. Nearly hysteresis-free property was observed in NC devices which might stem from the NC stabilization in mixed-phase HZO, as exhibited in **Figure 5.2**(c). Here, since n- and p-type devices were fabricated without the body doping, there is a mismatch in V_{th}, with p-type devices being roughly 0.2 V smaller. Similar to the results of SOI planar FET discussed in Section 3.2, current boosting is observed at the same off-current from near V_{th}, which indicates the compatibility of mixed-phase HZO with GAA structure. In the case of p-type devices, despite the larger W_{NS} and the smaller L, the current level is much lower than that of n-type devices (×0.5 or less), which would be attributed to the lower carrier mobility of hole. In addition, external resistance ($R_{External}$) of p-type device is thought to be considerably larger than that of n-type device, which can be inferred from the linear-scaled transfer curves; calculated $R_{External}$s from $1/V_{OV}$ method of n- and p-type NS GAA NCFETs were 2.16 kΩ and 11.9 kΩ, respectively. **Figure 5.2**(d) compares SS of p- / n-type NC and reference

devices according to I_D, which confirms the *SS* enhancement in NC devices. Especially, n-type NS GAA NCFET exhibits a quite low *SS* of 61.9 mV/dec. The improvement of gate controllability by HZO NC material leads to the reduction of *DIBL*. **Figure 5.3**(a) and (b) plot *DIBL* of NC and reference devices with various *L*s (140 nm ~ 300 nm) and W_{NS}s (50 nm ~ 150 nm), where the quite enhanced *DIBL* can be observed in NC devices. **Figure 5.3** denotes the V_D dependence of V_{th} shift, where the slope of V_{th} shift with regard to V_D (namely, *DIBL*) of NC devices decrease sharply at higher V_D due to the enhanced gate capacitance.

These *SS* and I_D enhancement of NS GAA NCFETs either improves the performance at the same V_{DD} or enables V_{DD} scaling while preserving the same performance. Advanced CMOS technology struggles to develop a multi-work function scheme for various devices ranging from high-performance to ultra-low power through work function metal (WFM) modulation and/or dipole engineering [101]; particularly further lowering of WF is remarkably challenging. The *SS* and current improvement of NCFETs allows performance enhancement without burdensome WF tuning and increasing off-current (I_{off}). Furthermore, further V_{DD} scaling for reducing power consumption can be achieved by NS GAA NCFET's *SS* enhancement effect. To access the above-mentioned benefits of NS GAA NCFET, current enhancement and V_G scalability of NC devices compared to reference devices were investigated. Here, current enhancement was represented as ($I_{on,NC}$ - $I_{on,Ref}$)/

$I_{on,Ref}$, where the $I_{on,NC}$ and $I_{on,Ref}$ represent the on-current of NC and reference devices at the identical I_{off} and V_{OV}s. Also, the V_G scalability was calculated by the difference of V_{OV} in NC and reference device for achieving the same I_{on}.

In the meanwhile, one can recognize from the linear-scaled transfer curves [**Figure 5.2**(a)] that the $R_{External}$ of reference device is somewhat larger than that of NC device; the extracted $R_{External}$s are 3.35 kΩ for reference and 2.16 kΩ for NC devices as illustrated in **Figure 5.4**, might being brought from the process variation. Therefore, it is fair to estimate the performance gain with subtracting the $R_{External}$. **Table 5.1** provides a summary of I_{on} enhancement and V_G scalability of n-type devices (reference and NC) with being included and excluded the $R_{External}$. The NC GAA NCFET exhibits I_{on} gain of 23.3% at V_{OV} = 450 mV (HP device V_{DD} target in IRDS 2021 [30]) when $R_{External}$ is included, and 15.7% even when $R_{External}$ is subtracted. V_G scalability for the same performance was determined to be 109 mV with $R_{External}$ and 66.8 mV without $R_{External}$, which is significant improvement considering the WF modulation challenges.

Figure 5.5 summarizes figure of merits extracted from the DC characteristics of multiple NS GAAFETs (reference and NC). **Figure 5.5**(a) and (b) depict the 3-decades averaged *SS* and W_{eff}-normalized I_{on} at V_{OV} = 0.45 V in linear and saturation V_D, respectively. Obviously, NC devices tends to be located in the lower right corner, signifying their superior performance. **Figure 5.5**(c) displays *DIBL*-*SS* plots in $V_{D,Lin}$

for assessing the SCE immunity of NS GAAFETs, where the NC devices exhibit enhanced *DIBL* as well as *SS*. I_D-V_D characteristics of p- and n-type NS GAAFETs [**Figure 5.6** (a) and (b)] reveals the current enhancement in the entire V_D range in NC device.

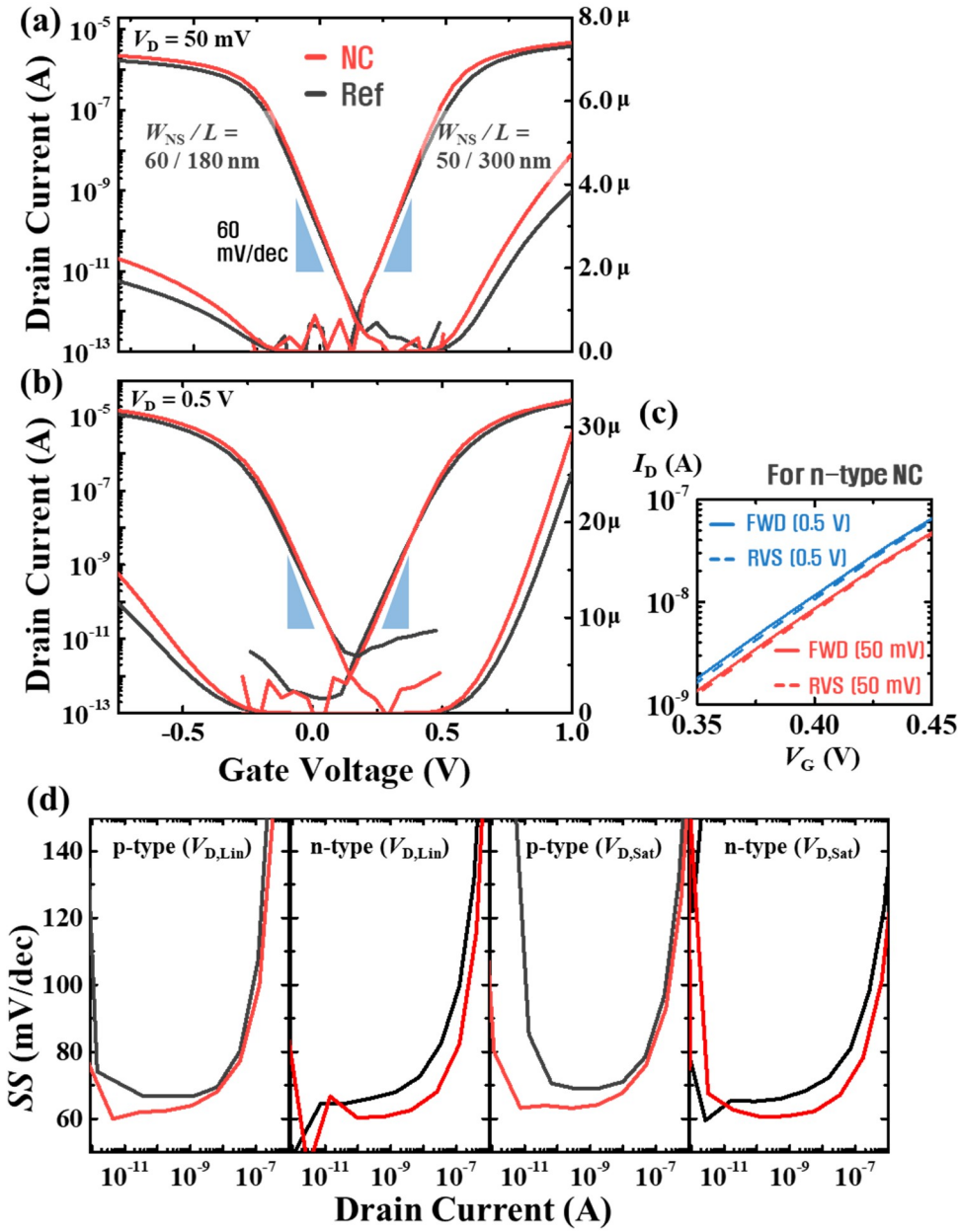


Figure 5.2. Transfer characteristics of n- and p-type stacked NS GAA NCFET at (a) linear (V_D = 50 mV) and (b) saturation region (V_D = 0.5 V). (c) Enlarged forward and reverse swept I_D-V_Gs of n-type NS GAA NCFET (d) *SS*-I_D plots of n- and p-type devices at different V_D conditions.

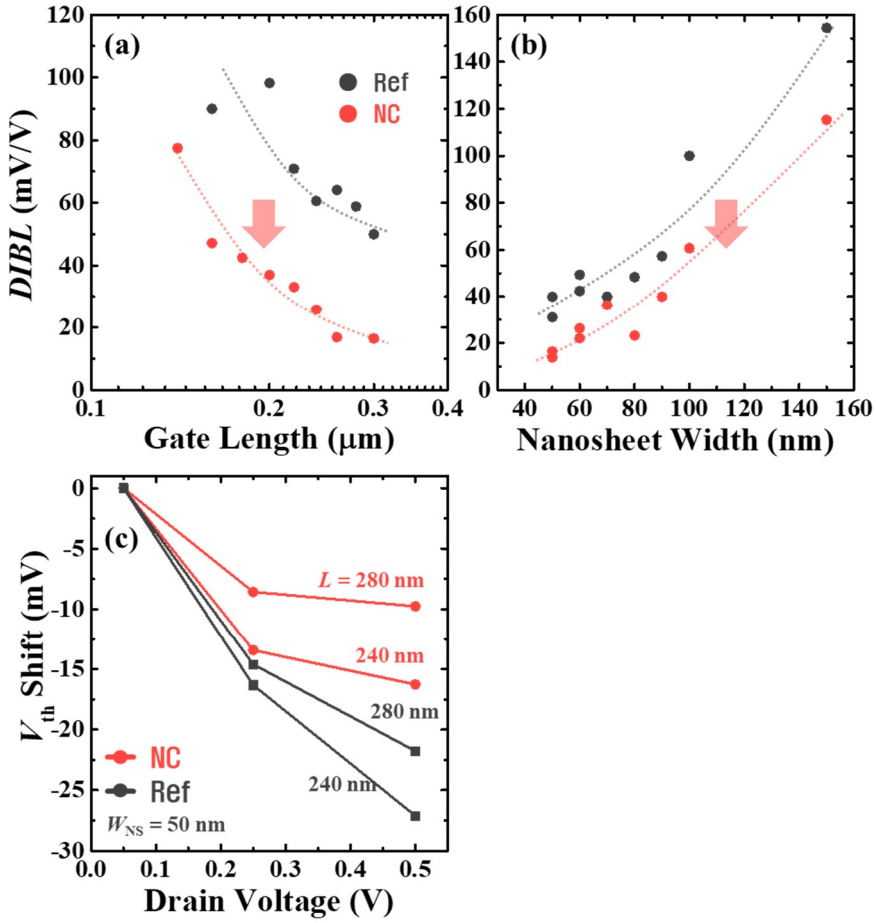


Figure 5.3. *DIBL* of n-type NS GAAFETs (w/ reference HfO and NC HZO) according to (a) the gate length and (b) the nanosheet width. (c) V_{th} shift of n-type NS GAFETs (reference and NC) with regard to V_D.

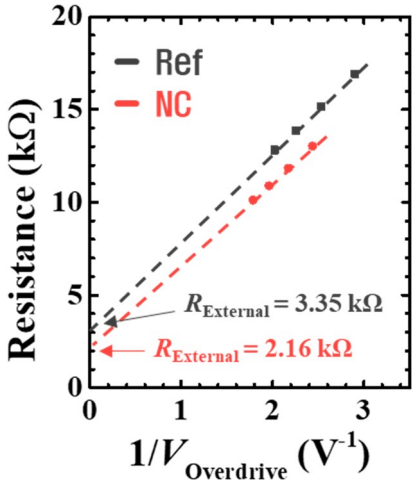


Figure 5.4. $R_{External}$ of n-type NS GAAFETs (w/ reference HfO and NC HZO) extracted by $1/V_{OV}$ method.

Table 5.1. I_{on} enhancement [($I_{on,NC}$ - $I_{on,Ref}$)/ $I_{on,Ref}$] and V_G scalability for the same I_{on} including/excluding $R_{External}$ at $V_{D,Lin}$ and various V_{OV}s.

V_{OV} (mV)	Including $R_{External}$		Excluding $R_{External}$	
	I_{on} Enhancement	V_G Scalability	I_{on} Enhancement	V_G Scalability
250	29.3%	65.1 mV	25.8%	53.6 mV
350	24.2%	82.5 mV	18.3%	57.2 mV
450	23.3 %	109 mV	15.7%	66.8 mV

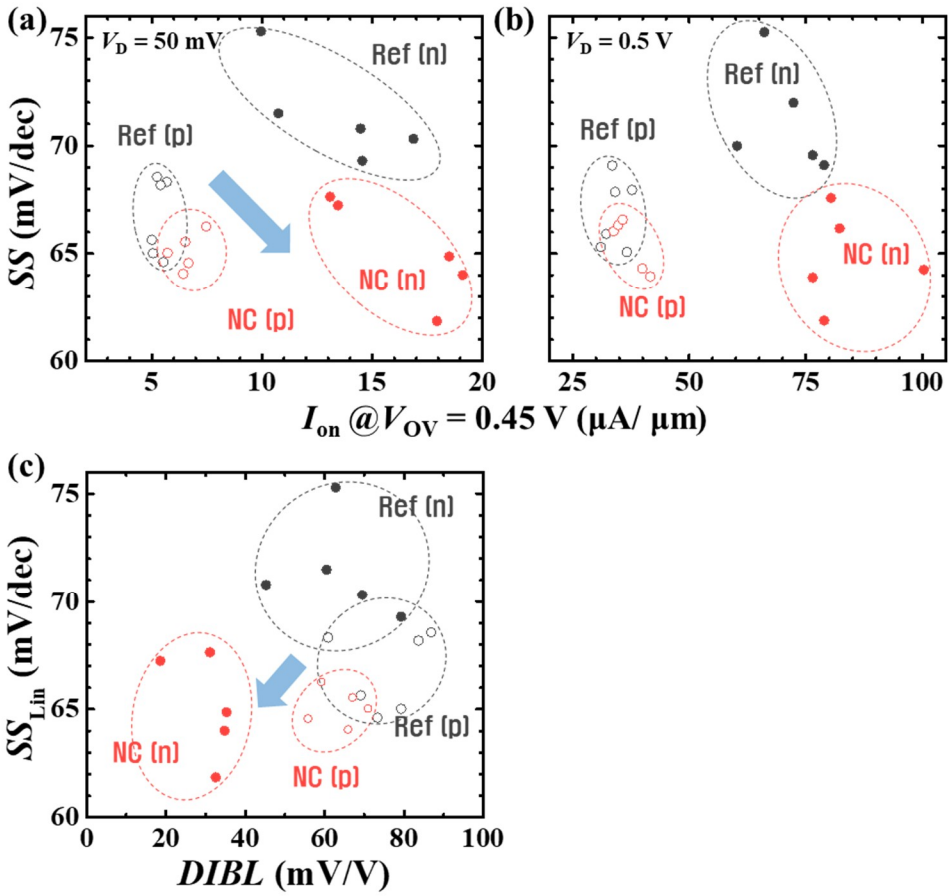


Figure 5.5. *SS*-I_{on} plots of multiple reference and NC NS GAAFETs (n- and p-type) at (a) V_D = 50 mV and (b) V_D = 0.5 V. (c) SS_{Lin} – *DIBL* plots.

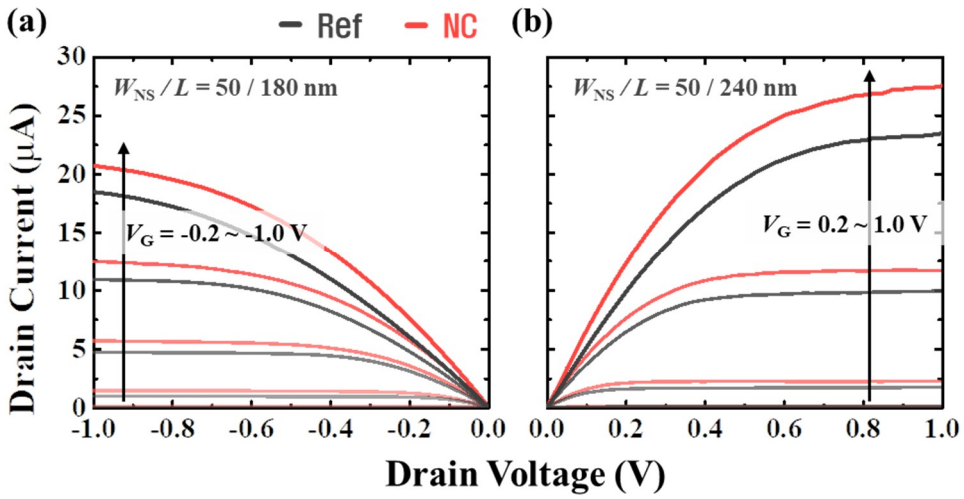


Figure 5.6. Output characteristics of (a) p- and (b) n-type NS GAA FETs (reference and NC).

5.1.3 Performance Evaluation

Figure 5.7(a) represents the *SS*-I_{on} benchmarks of reported NCFETs. *SS* refers to the average *SS* over 3-decades (I_D/W_{eff} = 10^{-10} ~ 10^{-7} A/μm), and I_{on} represents the W_{eff}-normailized I_D at V_G = 0.65 V with I_{off} = 10^{-10} A/μm. Here, the W_{eff} represents the perimeter of the 3D-structured channel such as Fin or GAA. Marked annotations indicate the device structure, while unannotated devices are planar type. The devices represented by the green inverted triangle [53-56] exhibits hysteretic transfer characteristics, which means that the ferroelectric polarization switching occurred. Here, notice that the steeper reverse-swept-*SS* implies the transient NC, not stable NC.

[56, 57] whose I_{on} is considerable, are industry-fab-fabricated Fin-type NCFETs with the gate length of 30 nm and 60 nm. **Figure 5.7**(b) illustrates the *SS*-I_{on} plots where the I_{on} is normalized by top channel width (W_{top}). W_{top}-normalized current emphasizes the current drivability of the devices at the same footprint, which has greater significance in 3D structures. It is certain that 3D structured devices, compared to the planar devices, displays superior W_{top}-normalized current drivability. NS GAA NCFETs demonstrated in this dissertation exhibit favorable electrical performance (right-lower corner of *SS*-I_{on} plot) thanks to its GAA structure and enhanced gate capacitance. For the first time, single-crystalline Si NS GAA structured NCFET were demonstrated by the application of ferroelectric-antiferroelectric mixed-phase NC HZO, which displays enhanced current characteristics with hysteresis-free and near-60 mV/dec-*SS*. The exceptional performance of NS GAA NCFETs validated in this dissertation definitely points at the directivity of future logic technology. It is firmly expected that much improved current characteristics can be achieved in the NS GAA NCFET with the help of optimized advanced CMOS fabrication techniques including contact formation (silicidation), S/D junction (epi S/D), and replacement metal gate (gate-last) processes.

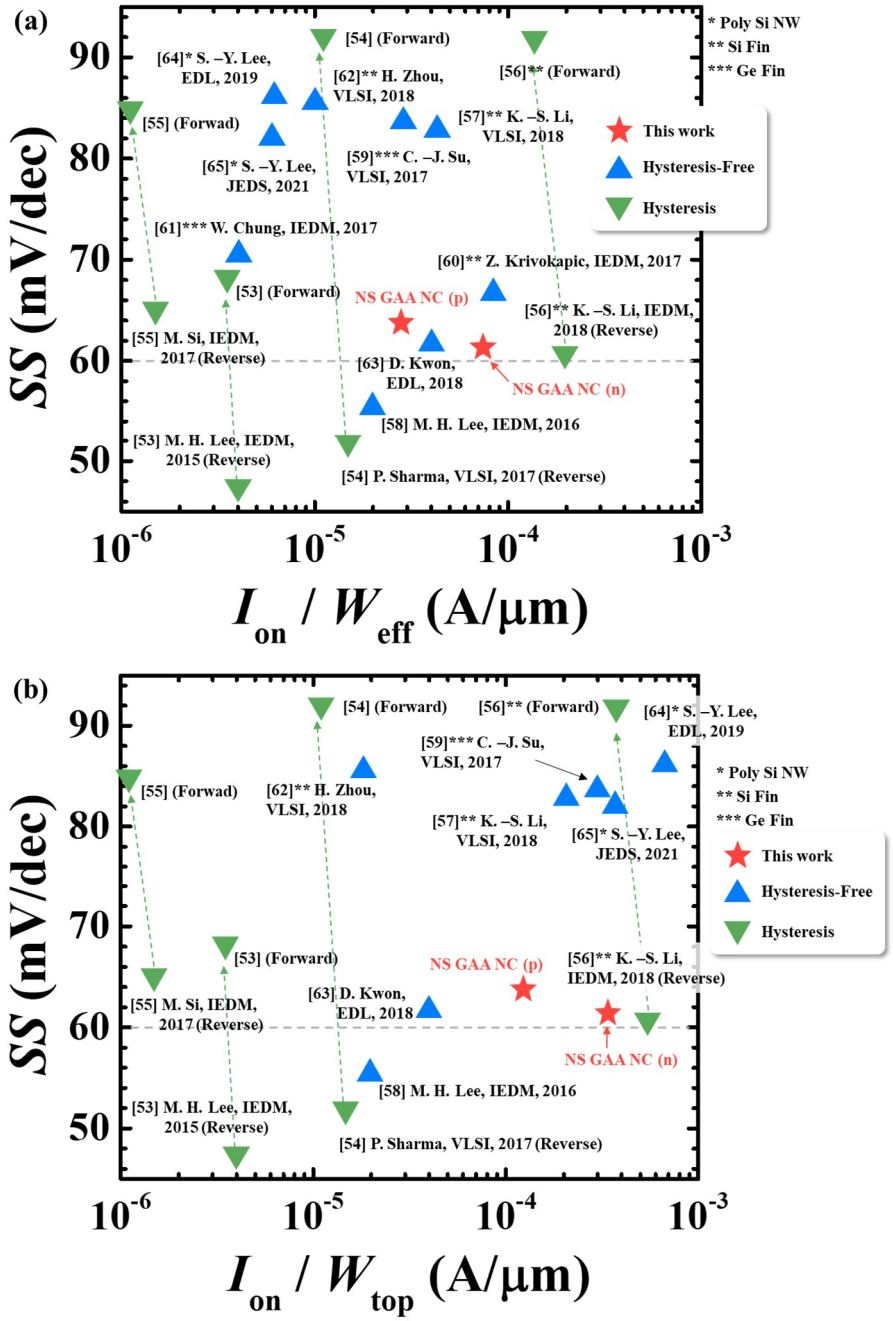


Figure 5.7. Average SS – I_{on} [normalized by (a) effective channel width and (b) by top channel width] benchmarks of NS GAA NCFET (this work) compared to other reported NCFETs.

5.2 Operating Temperature Properties

The integrated chip (IC) has an operating temperature range of up to 70℃ for commercial devices such as mobile phones, up to 85℃ for industrial devices, and up to 125℃ for devices operating in harsher environments. It is crucial to examine the temperature dependence of FET's electrical characteristic, especially for the case of emerging devices like NCFET. Not many studies on the temperature behavior of NCFET have been reported [102, 103], whose focuses are based-on the theoretical Landau S-curve. This subsection demonstrates the feasibility of mixed-phase HZO NCFET in variety range of operating temperature.

The transfer characteristics of the NS GAA NCFET at various temperatures (from 25 to 125℃) are depicted in **Figure 5.8** (a) and (b) (linear and saturation region, respectively). Log-scaled transfer curves confirms that as temperature increases, V_{th} is decreased due to the Boltzmann nature of carriers (dV_{th}/dT = -0.58 mV/℃). Furthermore, *SS* and I_{off} are deteriorated, I_{off} increase being apparent in high V_D [**Figure 5.8**(b)]. In addition, as seen in the linear-scale transfer curves, the I_{on} decreases despite the V_{th} reduction, owing to the increase of phonon scattering. In order to determine whether the degradation of electrical properties in NC device differs from that of the reference device, I_{on} and *SS* of two n-type devices as a function of operating temperature were examined [**Figure 5.8**(c) and (d)]. No significant

difference in I_{on} and *SS*-temperature trend were observed, although the degree of I_{on} degradation was slightly smaller. In other words, the temperature-dependent behavior of mixed-phase HZO material are comparable to that of HfO used in conventional CMOS devices, confirming that even in the high temperature as 125 ℃, the superiority of performance is maintained in NC device. Although [102, 103] reported that NC nature was deteriorated as temperature increases, it is estimated that the temperature behavior of ferroelectric/antiferroelectric in mixed-phase HZO is not significantly different from that of paraelectric.

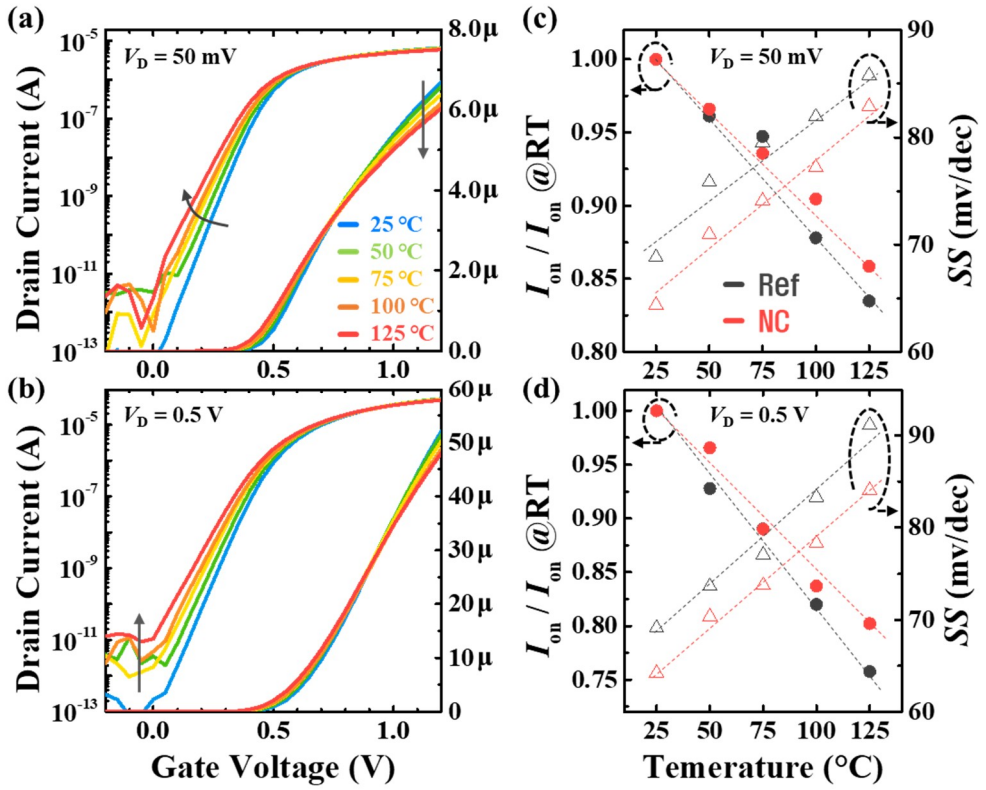


Figure 5.8. (a) and (b) Transfer curves (linear and saturation region) of NS GAA NCFET at various operating temperatures (25℃ ~ 125℃). (c) and (d) I_{on} / I_{on} at room temperature (RT) and *SS* (linear and saturation region) of NS GAAFETs (reference and NC) according to the operating temperature.

Chapter 6

Conclusion

This dissertation demonstrated a stacked-nanosheet gate-all-around negative capacitance field-effect transistor (NS GAA NCFET) with ferroelectric-antiferroelectric mixed-phase HZO. The objectives of the proposed device are i) implementation of stabilized capacitance boosting effect with CMOS-compatible HZO, and ii) application of NC material to NS GAAFET, which requires further EOT scaling for low-power and high-performance advanced logic device.

The NC effect of ferroelectric material theoretically occurs in a thermodynamically unstable region, which was constructed by Landau model; thus, stand-alone ferroelectric capacitor cannot reach NC region. Numerous studies on stabilizing NC have been reported. The main idea of those studies is that with the help of a dielectric with positive capacitance, the NC can be stabilized. However, the

requirement for stabilizing total system is incompatible with that for achieving sub-thermionic *SS*. Therefore, recent studies for the NC device focus on performance boosting effect by gate capacitance enhancement. In this dissertation, by using ferroelectric-antiferroelectric mixed-phase HZO material, which enable stable capacitance boosting with the help of NC effect, NCFET is demonstrated on the stacked NS GAA structure, the state-of-art logic architecture.

Mixed-phase HZO material was preferentially optimized through MFIS and MFM capacitance production and characteristic analysis. The Zr-rich HZO deposited in the form of nanolaminate (HZO stack 1) exhibited apparent capacitance enhancement (40% gain in permittivity) in MFIS experiment, whose MFM direct measurement confirms the ferroelectric-antiferroelectric mixed nature. Subsequently, SOI planar NCFET with the optimized HZO stack was fabricated to examine the feasibility of NC effect in FET: The capacitance boosting of HZO brought the current as well as the subthreshold swing (*SS*) improvement in planar NCFET. Transient current measurement revealed that the enhanced properties of NCFET can be sustained in the fast operation (~20 ns), although further verification for higher speeds (~ ps) is required.

For the final goal of this dissertation, which is the application of mixed-phase HZO to the stacked NS GAA structure, NS GAA FET fabrication with the gate-first process was optimized. By analyzing the DC electrical characteristics of

demonstrated 2-stacked NS GAA NCFET, it was confirmed that i) GAA structure enabled device scaling by enhanced short channel effect immunity, ii) nearly hysteresis-free stable operation with boosted gate capacitance was achievable in mixed-phase HZO, iii) *DIBL*, as well as *SS* and current enhancement compared to the reference NS GAAFET was observed. The on-current (I_{on}) gain was 15.7% in overdrive voltage (V_{OV}) of 0.45 V, while the voltage scalability was 66.8 mV compared to the reference device, which clearly addresses the feasibility of use as future low-power and high-performance logic device. It is meaningful in that the performance gain of fabricated devices increases in smaller V_{OV}s; thus, they are favorable for low-power applications. Furthermore, the temperature analysis confirmed that NS GAA NCFET's improved electrical characteristics were maintained even in higher temperatures (~125℃), without deteriorated NC nature.

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초 록

집적회로 기술의 발전은 소자의 소형화를 통한 속도 및 용량의 향상을 위해 발전을 거듭해왔다. 그러나 소형화를 거듭할수록 증가하는 누설전류의 문제로 전력 밀도가 급격하게 증가하고 있다. 상보형 금속-산화막-반도체(CMOS) 기술은 눈부신 공정기술의 성장에 힘입어 한계를 끊임없이 극복해왔으나, 기존의 금속-산화막-반도체 전계-효과-트랜지스터(MOSFET)의 물리적 한계는 극복할 수 없는 문제이다. 이에 따라 논리 반도체에 관한 연구는 CMOS를 연장하는 방향과 CMOS를 뛰어넘는 방향으로 나뉘어 진행되고 있다. CMOS를 연장하는 방향은 뛰어난 정전기적 게이트 장악력을 갖는 차세대 CMOS 구조로 유망한 게이트-올-어라운드 전계-효과-트랜지스터(GAAFET)에 관한 연구가 주를 이룬다. 특히 높은 전류 구동력을 가질 수 있는 나노시트(NS) 구조가 가장 유망한데, 게이트 장악력이 전류 구동력과 상충된다는 단점이 있다. 이에 따라 NS GAAFET 기술을 위해서는 더 높은 수준의 유효산화막두께 (EOT) 스케일링이 필수적이다. 한편, CMOS를 뛰어넘는 방향의 연구는 MOSFET의 물리적 한계를 극복하기 위해 새로운 메커니즘을 갖는 소자를 개발하는 방향으로 이루어진다. 다양한 후보군 중 CMOS 호환성과 전류 구동능력이

뛰어난 음의 정전용량 전계-효과-트랜지스터(NCFET)이 저전력, 고성능 동작을 위한 미래 CMOS 소자로 각광받고 있다. 강유전체의 음의 정전용량 (NC) 효과를 이용한 NCFET은 Landau 모델에 의해 이론적으로 증명되었으나, 열역학적으로 안정한 상태와 60 mV/dec 이하의 문턱전압-이하-기울기(*SS*)를 동시에 구현하기 불가능하다는 문제가 있다.

본 학위논문에서는 안정한 정전용량 향상 특성을 가지며 높은 성능을 갖는 NS GAA NCFET을 구현하였다. 강유전체(ferroelectric)-반강유전체 (antiferroelectric) 혼합상(mixed-phase) 하프늄-지르코늄-옥사이드(HZO) 박막의 정전용량 향상 효과를 커패시터 및 FET 제작을 통해 효과를 검증하였다. 또한 높은 게이트 장악력을 가지며 집적회로에서 요구하는 전류 구동력을 만족시킬 수 있는 적층형 나노시트 게이트-올-어라운드(stacked NS GAA) 구조에 혼합상 NC 박막을 적용한 FET을 시연하고 성능의 우수성을 확인하였다. 동일하게 제작된 MOSFET 대비 향상된 SS와 구동 전류(I_{on})를 확인하였고, 다양한 성능 지수를 토대로 저전력, 고성능 로직 소자로서의 타당성을 검증하였다.

주요어 : 게이트-올-어라운드(GAA), 적층형 나노시트(Stacked NS), 음의 정전용량 전계-효과-트랜지스터(NCFET), 강유전체(Ferroelectric), 혼합상(Mixed-phase), 하프늄-지르코늄-옥사이드(HZO).

학번 : 2014-21698