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Avalanche multiplication phenomena in ambipolar TMDC field-effect transistors

양극성 전이금속 칼코겐화합물 기반 전계효과 트랜지스터에서의 아발란치 증폭 현상 연구

2023 년 2 월

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물리·천문학부

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Abstract

Avalanche multiplication phenomena in ambipolar TMDC field-effect transistors

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Two-dimensional (2D) materials are considered as one of the most prominent candidates for next-generation semiconductor technology. Due to their high mobility, tunable band gap and structural uniformity preserved down to single atom thickness, 2D materials are under intensive research in a wide range of fields from transistors, photodetectors, sensors to neuromorphic devices. Taking advantage of their potential in the field of optoelectronics, there has recently been growing number of reports on implementing avalanche multiplication in these materials. Previous studies have mainly focused on optimizing material selection and device architecture, and as a result realized highly sensitive avalanche photodetectors and low subthreshold-swing avalanche transistors. However, most of the investigations are based on the theory for avalanche multiplication in conventional three-dimensional (3D) materials, and fundamental analysis on avalanche phenomena in 2D materials is required to further enhance device performance and establish novel architectures.

A fundamental question is the comparison between ionization rates of electrons and holes. In most of the conventional 3D semiconductors, it has been thoroughly examined that the ionization rates are different for these two charge carriers, and their ratio also varies in different materials. However, until now there has been very little research on the comparison of these quantities in 2D materials. In order to study

the ionization rates of both charge carriers in a single 2D material, it must be tunable to allow the flow of either charge carrier, *i.e.*, it must be ambipolar. Although ambipolar 2D materials have the advantage of facile carrier type tuning through electrostatic gating, simultaneously allowing both carrier types in a single channel poses an inherent difficulty in analyzing their individual contributions to avalanche multiplication. In ambipolar field-effect transistors (FETs), two different phenomena of ambipolar transport and avalanche multiplication can occur, and both exhibit secondary rise of output current at high lateral voltage. In my thesis study, I proposed the method of channel length modulation to distinguish these two phenomena, and successfully analyzed the properties of electron- and hole-initiated multiplication in ambipolar WSe_2 FETs.

First, I investigated ambipolar transport in WSe_2 FETs, which occurs in devices with longer channel lengths. Ambipolar transport is a phenomenon where electrons and holes flow through the channel simultaneously and each contribute to the total current. It is induced when the drain voltage surpasses the gate voltage, so that the electrostatic gating is locally reversed in part of the channel near the drain electrode. To confirm the occurrence of ambipolar transport in WSe_2 FETs, I conducted high voltage sweep measurements in the devices under various gate bias conditions. The critical voltage of the secondary current shifted in accordance with the modulation of gate voltage, which is direct evidence of the ambipolar transport model. I also discuss the working mechanism of the phenomenon through charge carrier distribution and band structure description of the system.

Next, I analyzed avalanche multiplication in WSe_2 FETs, which occurs in devices with shorter channel lengths. Here, the lateral electric field is much higher

than that in long-channel devices, so that impact ionization can begin before the drain voltage reaches the critical voltage for ambipolar transport. The measurements in devices with various channel lengths clearly show the correlation of breakdown voltage with channel length, which yields the intrinsic breakdown field of the material in agreement with the avalanche model. Band structure description is also utilized to discuss the contrasting results from the ambipolar transport characteristics. As the principal motive of the research, I extracted and compared the ionization rates of electrons and holes through the analysis of multiplication factors and breakdown voltages. Ionization rates of hole were found to be higher than electrons, in agreement with the result of lower breakdown voltage of holes than electrons. Finally, I suggest a method of selectively engineering the two competing phenomena of ambipolar transport and avalanche multiplication through careful choice of the channel and dielectric materials.

The essential accomplishment of my thesis study was devising a simple and robust method of channel length modulation to separate and thoroughly differentiate between two seemingly alike phenomena of ambipolar transport and avalanche multiplication. With the commercialization of 2D materials approaching and the interest in the fields of both phenomena still expanding, this research will foster the development of high-performance devices and novel architectures utilizing ambipolar transport and avalanche multiplication.

Keywords: Transition metal dichalcogenides, 2D materials, Avalanche multiplication, Ambipolar transport, Field-effect transistors.

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This work is dedicated to my beloved wife Daeun and our families.

Chapter 1. Introduction

1.1. Transition metal dichalcogenides

Two-dimensional (2D) materials are a family of materials that have emerged from the advent of graphene and have grown to be an enormous research field in materials science and electronics.[1-3] These materials form strong covalent bonds in the *xy*-plane, but weak van der Waals bonds in the out-of-place direction leading to easy separation of layers even to a single atom thickness. Since there are no dangling bonds throughout the surface, the intrinsic property of each layer is preserved when 2D materials are stacked together. Thus, various types of 2D materials such as semiconductors, insulators and semimetals can be carefully chosen and stacked to easily design and form diverse interfaces such as p-n junctions, tunnel barriers and quantum wells.[4,5]

Transition metal dichalcogenides (TMDCs) are a group within the family of 2D materials, where each repeating layer consists of a transition metal atom at the center sandwiched by two chalcogen atoms (*i.e.,* group 16 elements) on top and bottom. This bonding formation leads to a unit cell that is three atoms thick, generally having the thickness of 6 to 7 angstroms.[6] Within the TMDCs, the band gap is lowered as the chalcogen atom is changed from S, Se to Te, resulting in S and Se groups being semiconductors while Te groups are generally semimetals.[7] Out of the many combinations of transition metals and chalcogens, MoS_2 and WSe_2 are known to have the highest mobility, and show most active research in the field.

The most interesting feature of TMDC is, as is the same for other 2D materials, that the band structure changes greatly as the thickness is varied.[8] The band gap increases as the thickness is reduced due to quantum confinement effect, and in most cases only monolayers exhibit a direct gap while thicker forms have an indirect gap. For example, MoS_2 has a band gap of ~1.2 eV at bulk, but its optoelectronic band gap increases to ~1.87 eV at monolayer, while WSe_2 changes from ~1 eV at bulk to ~1.65 eV at monolayer.[9] While the naturally generated sulfur vacancies act as electron donors in MoS_2 allowing only an n-type behavior in most of the cases, the Fermi level of WSe_2 is located nearly at the center of the band gap, leading to its ambipolar behavior. The Fermi level can be easily tuned through electrostatic gating in a field-effect transistor structure, with a metal gate closely placed to the TMDC and a dielectric material in between to apply the field effect. Thus, ambipolar materials such as WSe_2 are more versatile in that a single material can be used to locally form an n-type channel and a p-type channel through designing the gating structure appropriately.[10,11]

The TMDCs are under a wide range of research for their applications as the next-generation semiconductor device materials. First of all, they are one of the most promising candidates for ultimate scaling of devices because they preserve high mobility and clean interface even to sub-nm thickness where the current silicon technology faces severe challenges.[12] Moreover, the strong light-matter interaction of these materials has led to an abundant number of studies in the field of optoelectronics, while the valley selectivity to research in spintronics.[13,14] The rich possibilities of TMDC materials has been demonstrated in a plethora of device applications from biosensors,[15] LEDs,[16] to neuromorphic devices.[17,18]

There are, however, challenges to overcome for the device application of

TMDCs to be realized. First of all, high quality wafer-scale synthesis of monolayer TMDC materials is difficult. Although growth techniques are continuously improving, the uniformity of synthesized monolayers is still hampered by wrinkles, cracks, and local domains of polycrystalline areas.[19-21] Secondly, many of the materials in the TMDC family are vulnerable to ambient conditions. Although some are quite robust under these conditions, continuous exposure to oxygen and moisture result in degradation of material quality, which requires passivation. With these challenges overcome, TMDC materials will potentially be utilized for next-generation semiconductor technology.

1.2. Avalanche multiplication

When large electric field is applied to a material, the charge carriers inside the material are accelerated, eventually to the point where they have enough kinetic energy to knock out bound electrons from the atoms upon collision. Such process of electron-hole pair creation is called impact ionization. The newly created electrons and holes can be accelerated to cause subsequent impact ionization themselves, and when the number of charge carriers grows exponentially in a chain reaction, the phenomenon is called avalanche multiplication.[22] The magnitude of electric field required to induce avalanche multiplication varies with the material in question, but is usually in the order of $10^5 \sim 10^6$ V/cm.[23]

Avalanche multiplication itself is a nondestructive and reversible process, so that the device will return to the initial state when the electric field is removed. However, generally a strong field creates a large current, and Joule heating that results from such current flow can cause permanent device failure. In this manner, a device structure that can yield an extremely high electric field while keeping the current low is required to form an avalanche, and hence reverse-biased $p-n$ (or $p-i-n$) junction have been used to study the physics of avalanche multiplication, as well as utilized for device applications.

The device structure that can best utilize the phenomenon is the photodetector. A photodetector senses light through the formation of photocarriers through the absorption of photons to the active channel. With the use of avalanche multiplication, even a small number of photocarriers can be amplified inside the channel, and hence lead to a much higher responsivity. Through this mechanism avalanche photodiodes (APDs) exhibit much higher detectivity than normal $p-i-n$ photodiodes and can even be used to detect single photons with an appropriate design of the device, known as a single photon avalanche detector (SPAD).[24] Nonetheless, APD has drawbacks of requiring a higher voltage to operate and having excess noise due to multiplication of dark current, so that APDs and $p-i-n$ photodiodes are used for different purposes in a complementary manner.

Avalanche multiplication in bulk materials such as Si, Ge, SiN and GaAs has been thoroughly investigated since mid-1950s, and successfully put into application in the form of APDs and SPADs from 1980s. Since the discovery of 2D materials, the number of research on avalanche multiplication in these materials have also been gaining much attention.[25] The fundamental phenomenon of freeing additional electron-hole pairs through high-energy collision is the same as in bulk materials, and reported experimental data are in agreement to a certain extent. However, it is expected that the correlation between relevant parameters may be contrasting from bulk materials because of the two-dimensional configuration of electric field distribution and the passage of charge carriers participating in the collision event.

There are also some discrepancies in quantitative results between various reports on 2D avalanche multiplication, presumably because the experiments have been mostly performed without fully eliminating artificial variables such as contact geometry and field distribution. Therefore, theoretical analysis on avalanche multiplication specifically in 2D materials as well as experiments conducted in controlled systems will result in a deeper understanding of 2D avalanche multiplication phenomenon and its practical utilization.

References

1. Mak, K. F.; Lee, C.; Hone, J.; Shan, J.; Heinz, T. F. Atomically Thin MoS_2: A New Direct-Gap Semiconductor. *Phys. Rev. Lett.* **2010**, *105* (13), 136805.
2. Wang, Q. H.; Kalantar-Zadeh, K.; Kis, A.; Coleman, J. N.; Strano, M. S., Electronics and Optoelectronics of Two-Dimensional Transition Metal Dichalcogenides. *Nat. Nanotechnol.* **2012,** *7* (11), 699-712.
3. Duong, D. L.; Yun, S. J.; Lee, Y. H., van der Waals Layered Materials: Opportunities and Challenges. *ACS Nano* **2017,** *11* (12), 11803-11830.
4. Geim, A. K.; Grigorieva, I. V., Van der Waals heterostructures. *Nature* **2013,** *499* (7459), 419.
5. Xia, F.; Wang, H.; Xiao, D.; Dubey, M.; Ramasubramaniam, A., Two-dimensional material nanophotonics. *Nat. Photonics* **2014,** *8* (12), 899-907.
6. Manzeli, S.; Ovchinnikov, D.; Pasquier, D.; Yazyev, O. V.; Kis, A., 2D transition metal dichalcogenides. *Nat. Rev. Mater.* **2017,** *2* (8), 17033.
7. Chhowalla, M.; Shin, H. S.; Eda, G.; Li, L.-J.; Loh, K. P.; Zhang, H., The chemistry of two-dimensional layered transition metal dichalcogenide nanosheets. *Nat. Chem.* **2013,** *5* (4), 263-275.
8. Li, S.-L.; Tsukagoshi, K.; Orgiu, E.; Samorì, P., Charge transport and mobility engineering in two-dimensional transition metal chalcogenide semiconductors. *Chem. Soc. Rev.* **2016,** *45* (1), 118-151.
9. Zhou, C.; Zhao, Y.; Raju, S.; Wang, Y.; Lin, Z.; Chan, M.; Chai, Y., Carrier Type Control of WSe_2 Field-Effect Transistors by Thickness Modulation and MoO_3 Layer Doping. *Adv. Funct. Mater.* **2016,** *26* (23), 4223-4230.
10. Baugher, B. W. H.; Churchill, H. O. H.; Yang, Y.; Jarillo-Herrero, P., Optoelectronic devices based on electrically tunable p–n diodes in a monolayer dichalcogenide. *Nat. Nanotechnol.* **2014,** *9*, 262.
11. Ross, J. S.; Klement, P.; Jones, A. M.; Ghimire, N. J.; Yan, J.; Mandrus, D.; Taniguchi, T.; Watanabe, K.; Kitamura, K.; Yao, W., Electrically tunable excitonic light-emitting diodes based on monolayer WSe_2 p–n junctions. *Nat. Nanotechnol.* **2014,** *9* (4), 268.
12. Su, S.-K.; Chuu, C.-P.; Li, M.-Y.; Cheng, C.-C.; Wong, H. S. P.; Li, L.-J., Layered Semiconducting 2D Materials for Future Transistor Applications. *Small Struct.* **2021,** *2* (5), 2000103.
13. Mak, K. F.; Shan, J., Photonics and optoelectronics of 2D semiconductor transition metal dichalcogenides. *Nat. Photonics* **2016,** *10* (4), 216-226.
14. Schaibley, J. R.; Yu, H.; Clark, G.; Rivera, P.; Ross, J. S.; Seyler, K. L.; Yao, W.; Xu, X.,

Valleytronics in 2D materials. *Nat. Rev. Mater.* **2016,** *1* (11), 16055.

15. Barua, S.; Dutta, H. S.; Gogoi, S.; Devi, R.; Khan, R., Nanostructured MoS_2-Based Advanced Biosensors: A Review. *ACS Appl. Nano Mater.* **2018**, *1* (1), 2-25.
16. Withers, F.; Del Pozo-Zamudio, O.; Mishchenko, A.; Rooney, A.; Gholinia, A.; Watanabe, K.; Taniguchi, T.; Haigh, S.; Geim, A.; Tartakovskii, A.; Novoselov, K., Light-emitting diodes by band-structure engineering in van der Waals heterostructures. *Nat. mater.* **2015**, *14* (3), 301.
17. Shi, Y.; Liang, X.; Yuan, B.; Chen, V.; Li, H.; Hui, F.; Yu, Z.; Yuan, F.; Pop, E.; Wong, H. S. P.; Lanza, M., Electronic synapses made of layered two-dimensional materials. *Nat. Electronics* **2018**, *1* (8), 458-465.
18. Liu, C.; Chen, H.; Wang, S.; Liu, Q.; Jiang, Y.-G.; Zhang, D. W.; Liu, M.; Zhou, P., Two-dimensional materials for next-generation computing technologies. *Nat. Nanotechnol.* **2020**, *15* (7), 545-557.
19. Yu, H.; Liao, M.; Zhao, W.; Liu, G.; Zhou, X. J.; Wei, Z.; Xu, X.; Liu, K.; Hu, Z.; Deng, K.; Zhou, S.; Shi, J.-A.; Gu, L.; Shen, C.; Zhang, T.; Du, L.; Xie, L.; Zhu, J.; Chen, W.; Yang, R.; Shi, D.; Zhang, G., Wafer-Scale Growth and Transfer of Highly-Oriented Monolayer MoS_2 Continuous Films. *ACS Nano* **2017**, *11* (12), 12001-12007.
20. Li, T.; Guo, W.; Ma, L.; Li, W.; Yu, Z.; Han, Z.; Gao, S.; Liu, L.; Fan, D.; Wang, Z.; Yang, Y.; Lin, W.; Luo, Z.; Chen, X.; Dai, N.; Tu, X.; Pan, D.; Yao, Y.; Wang, P.; Nie, Y.; Wang, J.; Shi, Y.; Wang, X., Epitaxial growth of wafer-scale molybdenum disulfide semiconductor single crystals on sapphire. *Nat. Nanotechnol.* **2021**, *16* (11), 1201-1207.
21. Liu, Y.; Gu, F., A wafer-scale synthesis of monolayer MoS_2 and their field-effect transistors toward practical applications. *Nanoscale Advances* **2021**, *3* (8), 2117-2138.
22. Miller, S. L., Avalanche breakdown in germanium. *Physical Review* **1955**, *99* (4), 1234-1241.
23. Levinshtein, M. E.; Kostamovaara, J.; Vainshtein, S., *Breakdown phenomena in semiconductors and semiconductor devices*. World Scientific: 2005; Vol. 36.
24. Kardynał, B. E.; Yuan, Z. L.; Shields, A. J., An avalanche-photodiode-based photon-number-resolving detector. *Nature Photonics* **2008**, *2* (7), 425-428.
25. Miao, J.; Wang, C., Avalanche photodetectors based on two-dimensional layered materials. *Nano Research* **2021**, *14* (6), 1878-1888.

Chapter 2. Ambipolar transport in WSe_2 FETs

In this chapter, I will discuss the ambipolar transport phenomenon that occurs in WSe_2 FETs. An ambipolar material is a semiconducting material that can easily transport either electrons or holes. However, in certain conditions both charge carriers can simultaneously flow through the channel, each contributing to the total current. This effect occurs when drain-source voltage exceeds the gate bias so that the minority charge carriers can be accumulated near the drain electrode. I investigated non-linear transport at high lateral voltages in WSe_2 FETs, and the shift of critical voltages in proportion with the modulation of gate voltage is given as the evidence for ambipolar transport. The resulting current flow is explained through charge carrier accumulation model in three different regimes categorized by the range of applied lateral voltage. The mechanism and the effect of gate bias is systematically discussed through band structure description.

2.1. Introduction

Transistors that are most widely used in contemporary devices made with silicon are generally unipolar, meaning that they can only accumulate either electrons or holes to transport current. This is because these transistors consist of previously *n*-doped or *p*-doped silicon through ion implantation, and junctions are made with joining the silicon components in *npn* or *pnp* formation.[1] However, emerging materials such as organic or 2D materials are different from the traditional silicon in that pristine materials can be used directly to form the channel of a transistor and contacted with metal electrodes which act as the source and drain.[2] Because the Fermi level of the channel is close to the middle of the band gap, it is theoretically possible for most of the materials to function as either electron channels or hole channels, depending on the direction of electrostatic gating.[3,4] These transistors are called ambipolar transistors, when their transfer curves have an off-state in the middle and on-state in both directions.[5] Practically, however, only some of these materials actually exhibit the ambipolar behavior, and most materials are still unipolar. The reason for unipolarity is closely related to the choice of metal electrodes and is also affected strongly by defects and interface conditions.[4] For example, MoS_2, one of the most prominently studied 2D materials, generally exhibit *n*-type behavior regardless of the metal electrode. The most important contribution generally known is from sulfur vacancies in the material, which act as electron donors, and form naturally in large amounts due to their low formation energy.[6] Efforts to engineer these vacancies by either passivation or synthesizing the material in a condition to reduce the density of sulfur vacancies have resulted in reducing the electron concentration as a whole, which is a good supporting evidence of the *n*-type behavior originating from these sulfur vacancies.[7]

Using an ambipolar material as the channel material, an unusual phenomenon can occur when the transistor is operated at high voltages.[8] Because the charge accumulation in the channel is modulated through the electrostatic gating, the carrier distribution can vary locally within the channel due to the difference of the gate and the voltage of each local point. When the voltage applied to the drain becomes greater than the gate voltage, the effect of gating can even be reversed at the channel close to the drain electrode. In this case, the originally minority charge carrier in the channel is now accumulated at one side and begins to flow to the opposite direction.[9] During the simultaneous transport of electrons and holes in the channel, the amount of recombination taking place can vary depending on the channel material properties. When the transistor is engineered to facilitate carrier recombination, it can be used to create ambipolar light-emitting devices, while the case of lower recombination can be used for ambipolar transistors of higher current transport. This phenomenon of ambipolar transport has been observed and investigated not only in two-dimensional materials but in various types of materials from organic molecules, polymers to perovskites, and holds great potential in device applications from memory and logic to light-emitting transistors.[10]

2.2. Experiments

2.2.1 Device fabrication

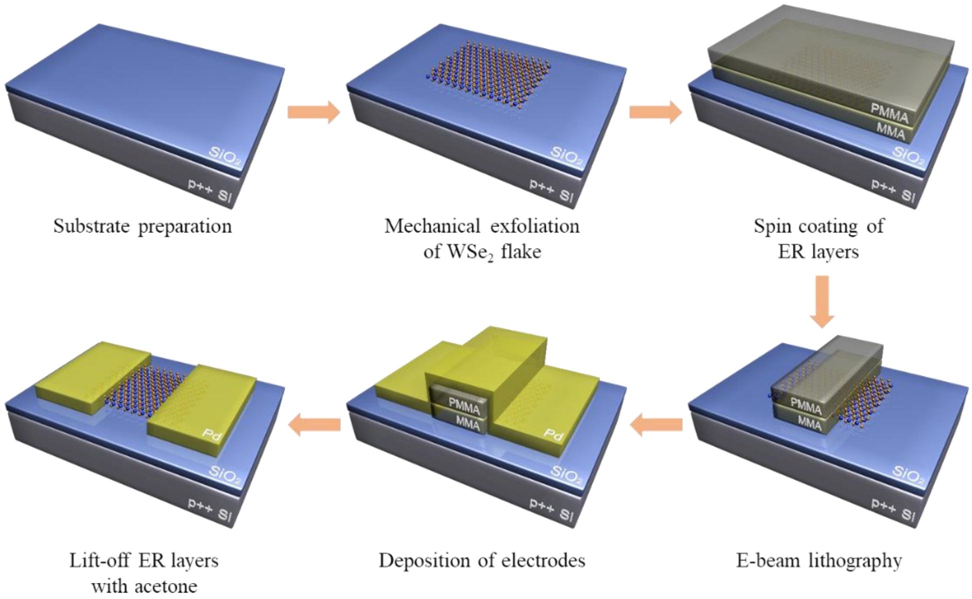

Figure 2.1 Device fabrication process of WSe_2 field-effect transistors.

The device fabrication process is illustrated in Figure 2.1. Few-layer WSe_2 flakes were first transferred onto 270 nm thick SiO_2/Si substrate from bulk crystal by mechanical exfoliation to fabricate WSe_2 FETs. Then, on top of WSe_2 flakes, a double electroresist layer of methyl methacrylate (9% concentration in ethyl lactate) and polymethyl methacrylate (950,000 molecular weight, 5% concentration in anisole) were spin-coated at 4000 rpm. Each resist layer was baked at 180°C for 90 s on a hot plate after coating. Electron-beam lithography method (JSM-6610, JEOL) was used to pattern the source and drain electrodes, and Pd (50 nm thick) was deposited with an electron-beam evaporator system (KVE-2004L, Korea Vacuum Tech.) for the formation of electrodes. The fabricated WSe_2 FETs were annealed at 150°C for 1 h for enhancement of electrical performance.

2.2.2 Optical and electrical characterization.

Raman and PL spectra of WSe_2 crystals were measured using a 532 nm laser with an intensity of 30 μW as the excitation source (XperRam 200, Nanobase Inc.). Next, the thickness of WSe_2 flakes was measured using an atomic force microscope (AFM) (NX10, Park Systems). Finally, the electrical characteristics of the devices were measured using a semiconductor parameter analyzer (Keithley 4200-SCS) in a vacuum.

2.3. Results and discussion

2.3.1 Electrical characteristics of WSe_2 FETs

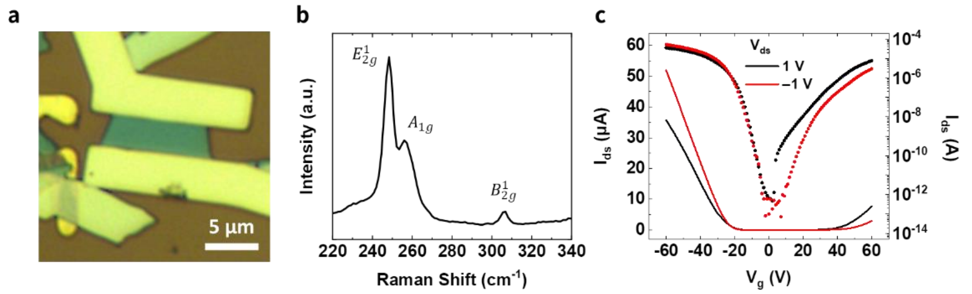

Figure 2.2 (a) Optical image, (b) Raman spectrum and (c) transfer curve

of the ambipolar WSe_2 FET device.

WSe_2 is an atomically thin semiconducting material, where each layer is separated by a van der Waals gap of ~0.65 nm (Figure 2.2a). I used a mechanical exfoliation method to transfer few-layer WSe_2 flakes onto a $SiO_2/p{+}{+}$ Si substrate with an oxide thickness of 270 nm, then used the electron-beam lithography method to pattern source and drain electrodes. Pd with a thickness of 50 nm was deposited through evaporation as the electrode to provide efficient hole injection at the contacts due to its high work function, and also because Pd is known to form covalent bonds with WSe_2 and form thinner Schottky barrier by metallization of the interface.[5] The thickness of the WSe_2 channel was measured with an atomic force microscope to be ~9.8 nm. The crystalline quality of WSe_2 was further examined using Raman spectroscopy (Figure 2.2b). The flakes used in the experiments showed the characteristic E_{2g}^{1}, A_{1g}, and B_{2g}^{1} peak at ~249, ~258, and ~307 cm^{-1}, respectively, indicating interlayer vibrational modes in multilayer flakes.[11] Figure 2.2c shows the transfer curves (drain-source current *versus* gate voltage, $I_{ds} - V_g$) of a representative WSe_2 FET device. The measurement data showed good ambipolar electronic characteristics, exhibiting a high on-off ratio of ~10^7 for electrons and ~10^8 for holes. Field-effect mobility values for electrons and holes extracted from the data shown in Figure 1c were determined to be μ_e = 13.9 $cm^2/V \cdot s$ and μ_h = 37.3 $cm^2/V \cdot s$, respectively, using the formula $\mu = \left(\frac{\partial I_{ds}}{\partial V_g}\right)\frac{L}{WC_iV_{ds}}$ with a channel length (L) = 3.2 μm, channel width (W) = 9.9 μm, and capacitance per unit area (C_i) = 1.3×10^{-8} F/cm^2.

2.3.2 Current−voltage relation at high lateral voltages

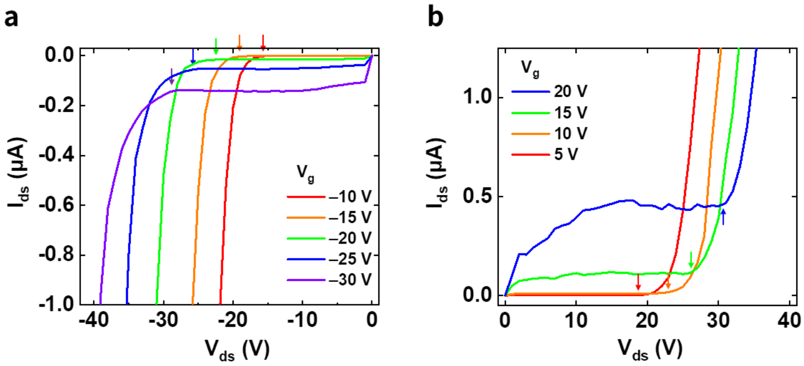

Figure 2.3 Output curves of the device at various gate bias, showing non-linear ambipolar transport from (a) hole to electron and (b) electron to hole.

When sufficiently high voltage is applied between the drain and source electrodes, metal-oxide-semiconductor FETs (MOSFETs) typically enter the saturation region due to the pinch-off near the drain electrode.[12] However, when the voltage is increased further, various physical phenomena can occur in the semiconductor channel. Figures 2.3a and b illustrate the dynamics of the device under high drain-source voltage in *p*-type and *n*-type modes, respectively. The output curves (drain-source current *versus* drain-source voltage, $I_{ds}-V_{ds}$) clearly exhibit triode and saturation regions at low drain-source voltage. As the drain-source voltage exceeds a particular value, the current rises further from its saturation level. The onset voltage of the secondary current increases proportionally to the applied gate bias in both *p*-type and *n*-type modes. This is in support of ambipolar transport and has been reported in FET systems with various channel materials,[8-10, 13,14] and its mechanism is discussed later in the paper. The device operates by majority carriers up to the saturation point, and the secondary rise of current after the saturation is due to the accumulation of opposite charge carriers (*i.e.*, minority carriers) near the drain electrode.

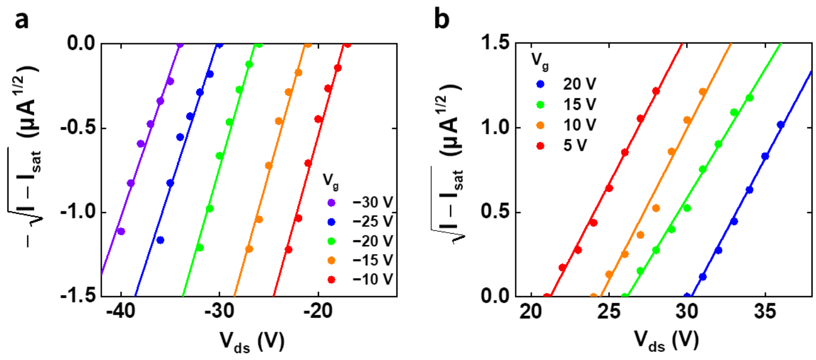

Figure 2.4 Square-root plot of the additional non-linear current after saturation in (a) negative and (b) positive gate bias.

Since accumulation occurs similarly to how depletion occurs during the pinch-off, the current-voltage relation at this region is also parabolic in shape.[9] To confirm the parabolic nature of the ambipolar current, the square root of the secondary current (defined as $I–I_{sat}$) was plotted against V_{ds} in Figure 2.4. The plot of each measurement begins from each of the critical voltages, which is shifted proportionally with the gate bias as previously mentioned. The linearity of these relations are evidence of parabolic shape of the secondary current, and support the ambipolar transport model. Moreover, the data from various gate bias have a similar slope because the same amount of minority carriers are accumulated at the same effective gate bias near the drain electrode (defined by $V_{ds} – V_{cr}$).

2.3.3 Three distinct transport regimes

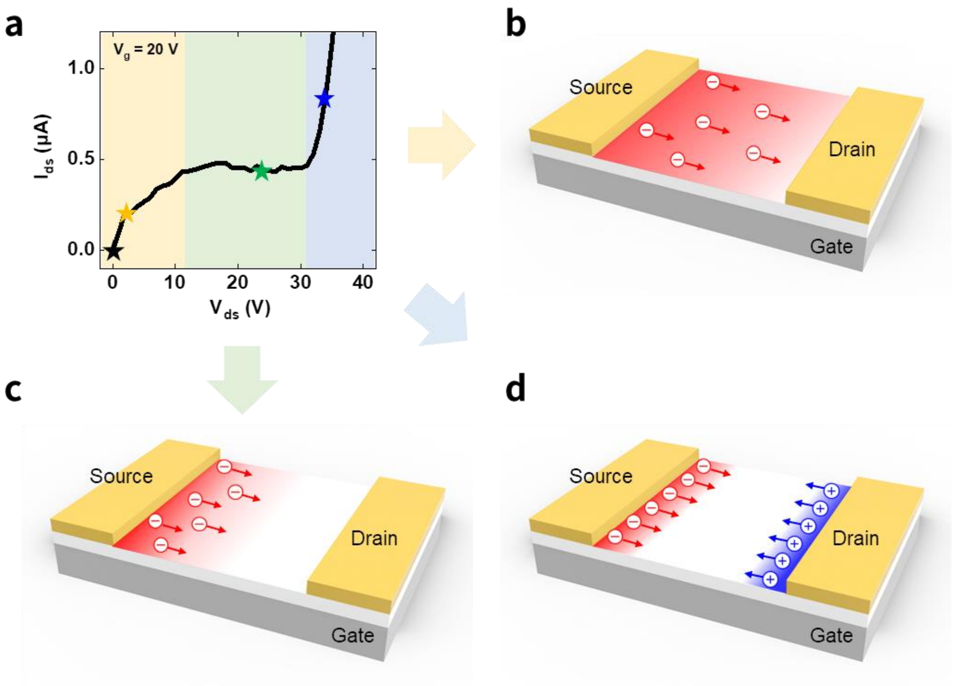

Figure 2.5 Three distinct transport regimes depending on the V_{ds} range. (a) Output curve of the device. (b-d) Illustration of charge carrier density in (b) unipolar transport at low V_{ds}, (c) pinch-off saturation at medium V_{ds}, and (d) ambipolar transport at high V_{ds}.

The electrical characteristics of these devices can be separated into three different transport regimes. Figure 2.5 describes how the output curve can be divided into different operating regions, and also illustrate the charge carrier concentration throughout the channel in each of the regions. The following analysis is described in the *n*-type mode where electrons act as primary carriers, but the opposite case of *p*-type mode is the same with electrons and holes replaced. First, at low voltages, the device behaves as an ordinary MOSFET where electrons are accumulated throughout the channel due to positive gate bias above the threshold voltage (V_{th}).

As the lateral voltage is increased, the effective gate bias at the channel near the drain electrode, described by $V_{g\_eff} = V_{ds} - V_{gs}$, is reduced, resulting in reduction of electron concentration. When the edge of the channel is fully depleted, the channel is pinched off and the device enters the saturation region, where MOSFETs are normally operated in order to provide a stationary current level.[1]

When the drain voltage exceeds the gate voltage, the effective gate voltage at the drain electrode becomes negative. Once it passes the threshold voltage for hole accumulation, holes begin to flow from the drain electrode (Figure 2.5d).

Altogether, the current-voltage response in each of the three transport regimes can be described by the following equations.

$$I_{uni} = \frac{\mu_1 C_i W}{L}\left\{\left(V_g - V_{th,1}\right) - \frac{V_{ds}}{2}\right\} V_{ds} \tag{2.1}$$

in unipolar region, where $|V_{ds}| \leq |V_g - V_{th,1}|$.

$$I_{sat} = \frac{\mu_1 C_i W}{2L}\left(V_g - V_{th,1}\right)^2 \tag{2.2}$$

in saturation region, where $|V_g - V_{th,1}| \leq |V_{ds}| \leq |V_g - V_{th,2}|$.

$$I_{ambi} = I_{sat} + \frac{\mu_2 C_i W}{L}\left\{V_{ds} - \left(V_g - V_{th,2}\right)\right\}^2 \tag{2.3}$$

in ambipolar region, where $|V_{ds}| \geq |V_g - V_{th,2}|$.

In equations (2.1), (2.2), and (2.3), I_{uni}, I_{sat}, and I_{ambi} denote the output currents in the unipolar, saturation, and ambipolar region, respectively. V_{th} is the threshold voltage, and the subscripts 1 and 2 stand for electron and hole for $V_{ds} > 0$ case, respectively, and vice versa for $V_{ds} < 0$ case.

2.3.4 Band structure discussion

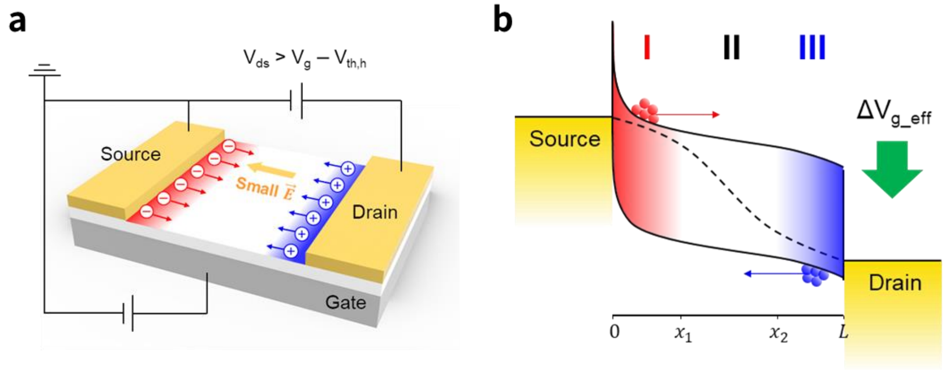

Figure 2.6 Band structure description of ambipolar transport. (a) Schematic of the device at high V_{ds} during ambipolar transport, and (b) energy bands throughout the channel. The dotted line indicates the Fermi level.

The ambipolar transport phenomenon is explained in depth through the band structure description. Figure 2.6a shows the distribution of electron and hole concentrations during ambipolar transport regime, with the level of current flow described by equation (2.3). Here, the small lateral electric field is mentioned so that the lateral field does not actively participate in the transport phenomenon, whereas it is the primary factor or avalanche multiplication discussed in the next chapter.

Assuming a uniform channel resistance without consideration of defects and interface traps, the voltage across the channel can be modeled as a linear function

$$V(x) = V_s + \frac{x}{L}(V_d - V_s) \tag{2.4}$$

where V_s and V_d are the voltages applied to the source and drain electrode, respectively, and x is the distance from the source electrode. Electron concentration at position x is then determined by

$$n(x) = C_i\{V_{g\_eff} - V_{th,e}\}/e \tag{2.5}$$

where e is the electron charge and $V_{g\_eff} = V_g - V(x)$ is effective gate voltage at each position. Electrons are accumulated near the source electrode but decrease in concentration along the channel. Near the middle of the channel where $V(x) \cong V_g - V_{th,e}$, electrons are totally depleted. However, close to the drain electrode, V_{g_eff} becomes negative and eventually reaches the condition $V_{g\_eff} < V_{th,h}$. From this position of $V_{g\_eff} < V_{th,h}$, holes start accumulating and hole concentration becomes larger toward the drain electrode.[9] In this region, the hole concentration can be determined similarly to electron-rich region as

$$p(x) = C_i\{V_{th,h} - V_{g\_eff}\}/e = C_i\{-V_g + V_{th,h} + V(x)\}/e \qquad (2.6)$$

The corresponding energy band diagram in the channel is described in Figure 2.6b, where the regions I, II, and III represent electron-rich, depletion, and hole-rich regions, respectively. The preceding analysis of charge carrier density with respect to position can be represented with varying Fermi level E_F. At each position in the channel, E_F can be expressed in terms of either n or p as

$$E_F = E_i + kT\ln\left(\frac{n}{n_i}\right) = E_i - kT\ln\left(\frac{p}{n_i}\right) \qquad (2.7)$$

where E_i is the intrinsic Fermi level, n_i is the intrinsic carrier concentration, k is the Boltzmann constant, and T is the temperature.

By substituting the previously acquired formulas for $n(x)$ and $p(x)$, E_F near each end of the channel is expressed as

Region I ($0 < x < x_1$): $E_F = E_i + kT\ln\left[\frac{C_i\{V_g - V_{th,e} - V(x)\}}{n_i e}\right]$ (2.8)

where $V(x_1) = V_g - V_{th,e}$

Region III ($x_2 < x < L$): $E_F = E_i - kT\ln\left[\frac{C_i\{-V_g + V_{th,h} + V(x)\}}{n_i e}\right]$ (2.9) where $V(x_2) = V_g - V_{th,h}$

In region II ($x_1 < x < x_2$), the effective gate voltage is between $V_{th,e}$ and $V_{th,h}$ such that both charge carriers are below the threshold. In this case, n and p are determined by the subthreshold diffusion model as

$$n = n_i \exp\left(\frac{e\{V_g - V(x)\}}{\eta kT}\right) \text{ and } p = \frac{n_i^2}{n} \tag{2.10}$$

where η is the subthreshold ideality factor, leading to $E_F = E_i + e\{V_g - V(x)\}/\eta$. The Fermi level throughout the channel is drawn as a dotted curve in Figure 2.6b. The modulation of V_{g_eff} near drain electrode also affects the band bending at the channel-electrode interface. As the Fermi level moves downward close to the valence band, the Schottky barrier is also reduced significantly, as illustrated by the green arrow.

2.3.5 Gate-bias dependence of ambipolar transport

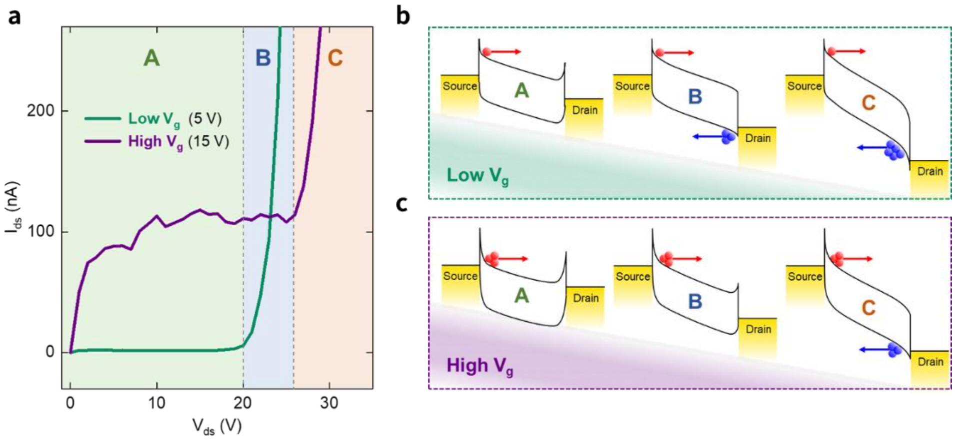

Figure 2.7 (a) Comparison of ambipolar transport in low and high gate bias. (b, c) Band structure description of the transition from unipolar to ambipolar regime in (b) low gate bias and (c) high gate bias.

The ambipolar current discussed in the previous sections, described by equations (2.3) and (2.9), contain the dependency on the gate voltage. Figure 2.7 illustrates the transition from saturation to ambipolar transport for two cases of low−V_g condition and high−V_g condition. In region A, both cases are in the saturation region, and only electrons act as majority charge carriers. More current flows in the high−V_g case because it has higher concentration of electrons. As V_{ds} is increased and enters region B, holes start to be accumulated in the drain side of the low−V_g case, due to lowering of effective gate voltage. Meanwhile in the high−V_g case, the V_g was too high for holes to be injected though the barrier at this point. Hence, ambipolar transport does not begin in the high−V_g case. In region C, hole injection occurs in both cases, but the ambipolar current is much greater in the low−V_g case because the effective gate at the drain side is more negative. In total, the ambipolar transport is manifested as a crossing and reversal between the output curves of different gate voltages.

2.4. Conclusion

In this chapter, the phenomenon of ambipolar transport in WSe_2 FETs was analyzed. Ambipolar transport is induced when the drain-source voltage exceeds the gate bias, so that the effective gate voltage near the drain electrode is reversed to the opposite polarity. When high lateral voltages were applied, the output curves of WSe_2 FETs exhibited the characteristic features of ambipolar transport referred to as three distinct transport regimes of triode, saturation and non-linear regions, in both directions from *n*-type to *p*-type and vice versa. Moreover, the critical voltages for non-linear current shifted in proportion with the modulation of gate bias, which serves as direct evidence of ambipolar transport. Charge carrier distribution and band structure description were utilized to explain the current−voltage characteristics, as well as the effect of gate bias on the critical voltage. These results show that ambipolar transport can be observed in a simple 2D FET device structure, even with a gate oxide with low dielectric constant, suggesting the versatile utilization of the phenomenon using 2D channels.

References

1. Sze, S. M.; Ng, K. K., *Physics of Semiconductor Devices*. Wiley: **2006**.
2. Radisavljevic, B.; Radenovic, A.; Brivio, J.; Giacometti, V.; Kis, A., Single-layer MoS_2 transistors. *Nat. Nanotechnol.* **2011**, *6* (3), 147-150.
3. Wang, Q. H.; Kalantar-Zadeh, K.; Kis, A.; Coleman, J. N.; Strano, M. S., Electronics and optoelectronics of two-dimensional transition metal dichalcogenides. *Nat. Nanotechnol.* **2012**, *7* (11), 699-712.
4. Kang, J.; Liu, W.; Sarkar, D.; Jena, D.; Banerjee, K., Computational Study of Metal Contacts to Monolayer Transition-Metal Dichalcogenide Semiconductors. *Phys. Rev. X* **2014**, *4* (3), 031005.
5. Braga, D.; Gutiérrez Lezama, I.; Berger, H.; Morpurgo, A. F., Quantitative Determination of the Band Gap of WS_2 with Ambipolar Ionic Liquid-Gated Transistors. *Nano Letters* **2012**, *12* (10), 5218-5223.
6. Liu, D.; Guo, Y.; Fang, L.; Robertson, J., Sulfur vacancies in monolayer MoS_2 and its electrical contacts. *Applied Physics Letters* **2013**, *103* (18), 183113.
7. Cho, K.; Pak, J.; Kim, J. K.; Kang, K.; Kim, T. Y.; Shin, J.; Choi, B. Y.; Chung, S.; Lee, T., Contact-Engineered Electrical Properties of MoS_2 Field-Effect Transistors via Selectively Deposited Thiol-Molecules. *Adv. Mater.* **2018**, 1705540.
8. Zhang, Y. J.; Ye, J. T.; Yomogida, Y.; Takenobu, T.; Iwasa, Y., Formation of a Stable *p–n* Junction in a Liquid-Gated MoS_2 Ambipolar Transistor. *Nano Letters* **2013**, *13* (7), 3023-3028.
9. Risteska, A.; Chan, K.-Y.; Anthopoulos, T. D.; Gordijn, A.; Stiebig, H.; Nakamura, M.; Knipp, D., Designing organic and inorganic ambipolar thin-film transistors and inverters: Theory and experiment. *Organic Electronics* **2012**, *13* (12), 2816-2824.
10. Ren, Y.; Yang, X.; Zhou, L.; Mao, J.-Y.; Han, S.-T.; Zhou, Y., Recent Advances in Ambipolar Transistors for Functional Applications. *Adv. Funct. Mater.* **2019**, *29* (40), 1902105.
11. Zhang, R.; Drysdale, D.; Koutsos, V.; Cheung, R., Controlled Layer Thinning and *p*-Type Doping of WSe_2 by Vapor XeF_2. *Adv. Funct. Mater.* **2017**, *27* (41), 1702455.
12. Hu, C., Modern semiconductor devices for integrated circuits. Prentice Hall Upper Saddle River, NJ: **2010**; Vol. 2.
13. Zaumseil, J.; Friend, R. H.; Sirringhaus, H., Spatial control of the recombination zone in an ambipolar light-emitting organic transistor. *Nat. Mater.* **2006**, *5* (1), 69-74.
14. Zhang, Y.; Suzuki, R.; Iwasa, Y., Potential Profile of Stabilized Field-Induced Lateral *p–n* Junction in Transition-Metal Dichalcogenides. *ACS Nano* **2017**, *11* (12), 12583-12590.

Chapter 3. Channel-length-modulated avalanche multiplication in WSe_2 FETs

In this chapter, the properties of avalanche multiplication inside the WSe_2 channel were investigated. As discussed in the last chapter, WSe_2 is a material that can easily support electrons or holes as the majority charge carrier through electrostatic gating, and this tendency allows ambipolar transport to take place with suitably large voltage applied to the drain electrode. However, to study the physics of avalanche multiplication, ambipolar transport must be suppressed in the channel. I separated the two competing phenomena by the modulation of channel length, where devices with shorter channels allowed avalanche multiplication to dominate through high lateral field throughout the channel. Other possible origins of secondary current in short-channel devices such as Joule heating or current crowding are systematically analyzed. I provide evidence of avalanche multiplication taking place in the channel by observing channel length dependency and gate bias stability, and examined the ionization rates of electrons and holes with the use of suitable approximations on basic theories of avalanche multiplication. Holes were found to have higher ionization rates in WSe_2 than electrons, which agrees with the smaller breakdown voltage observed for holes. The results were also compared to 3D semiconductors in terms of band gap analysis.

3.1. Introduction

Avalanche multiplication is a process where highly accelerated charge carriers collide with atoms and break free valence electrons to create additional electron-hole pairs in a chain reaction[1] and has been utilized in ultrasensitive optoelectronic devices such as avalanche photodiodes and even single-photon avalanche detectors.[2] Moreover, device architectures such as impact ionization transistors have been realized to overcome the fundamental thermionic limit of transistors.[3-5] Recently, avalanche photodetectors and transistors utilizing 2D materials as active channels have been reported, and some of them exhibited ultrahigh performance,[4,6-13] which signifies the need for a deeper analysis of the fundamental physics and transport mechanism of avalanche multiplication in 2D materials. Although previous studies have examined the multiplication phenomenon, the experiments mainly focused on devising high-performance photodetectors, and the carrier type was limited to unipolar transport. However, implementing avalanche multiplication in ambipolar devices may provide another way toward high-performance electronics, and a detailed analysis of avalanche multiplication in ambipolar materials is highly desired.

In three-dimensional (3D) semiconductors, the impact ionization rates of electrons and holes are generally different from each other.[1,14-16] However, while ambipolar 2D materials such as WSe_2 are well known for their simple carrier type tuning *via* electrostatic gating in a field-effect transistor (FET) structure, the coexistence of both charge carriers in the channel hinders the separate analysis of multiplication by each charge carrier. Hence, there has been very little research in determining the impact ionization rates of ambipolar 2D materials. In this study, I investigated the multiplicative characteristics of ambipolar WSe_2 FETs by suppressing ambipolar transport and only allowing avalanche multiplication to occur in the channel. This was done through the method of channel length modulation, where devices with longer channels were subject to ambipolar transport due to the large voltage applied to the drain, while devices with shorter channels went through avalanche multiplication due to the high lateral electric field in the channel. Other phenomena that may result in similar current−voltage relations such as Joule heating and current crowding effect are systematically considered. I analyzed the properties of avalanche multiplication such as multiplication factor and breakdown voltage, and successfully compared the ionization rates of electrons and holes. Finally, method of selectively engineering the two different phenomena of ambipolar transport and avalanche multiplication is proposed, utilizing the intrinsic multiplication rates of the channel material and dielectric constant of the gate dielectric material.

3.2. Experiments

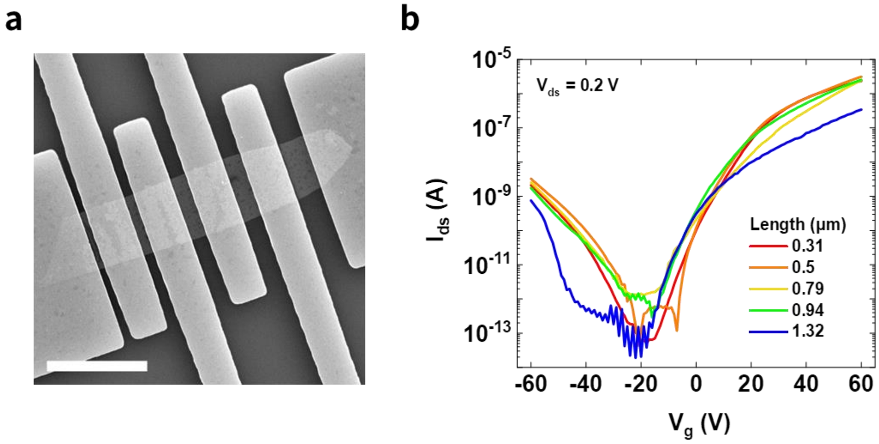

Figure 3.1 (a) Optical image and (b) transfer curves of the WSe_2 FETs of various channel lengths.

To investigate the properties of avalanche multiplication occurring in WSe_2 channel, FET devices with short channel lengths were fabricated. Figure 3.1a shows a field-emission scanning electron microscopy (FE−SEM) image of five independent devices made on a single multilayer WSe_2 flake with a thickness of 8 nm, each with a channel length of 0.31, 0.5, 0.79, 0.94, and 1.32 μm, respectively. The device fabrication process is the same as that described in Section 2.2.1. Figure 3.1b illustrates the transfer curves of the five devices, showing that the devices have similar electrical characteristics.

3.3. Results and discussion

3.3.1 Channel length dependence of I−V curves

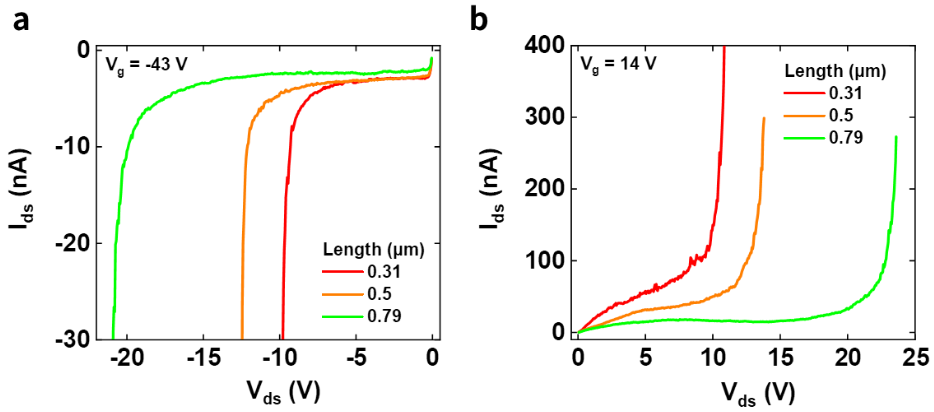

Figure 3.2 Output curves of different devices at high lateral voltages showing non-linear transport by avalanche multiplication in (a) hole transport and (b) electron transport.

Figure 3.2 shows I−V curves of three of the short channel devices under high drain-source voltages. All of them exhibited triode, saturation, and non-linear transport regions. Although this behavior is similar to the case of ambipolar transport discussed in the previous chapter, there are two significant differences that distinguish the phenomena. First, the onset point of non-linear transport is much lower than that needed to induce ambipolar transport. Considering the applied gate voltage (−43 V for holes and 14 V for electrons) and the transfer curves of these devices shown in Figure 3.1b, nearly 40 V of lateral voltage is needed to cause ambipolar transport in either charge polarities. However, the non-linear transport started at voltages lower than 25 V in all cases, and as low as 10 V for devices with shortest channel lengths. Therefore, the origin of non-linear transport for these devices must be a different phenomenon. Secondly, the onset voltages increased in proportion with channel length, which is unexpected from the analysis of ambipolar transport because ambipolar transport is only governed by the threshold voltages and unrelated to channel length of the device.

Considering these results, possible origins of secondary non-linear current include hot electron injection through Joule heating, current crowding at contacts, and avalanche multiplication inside the channel. First, Joule heating can cause an increase of current due to injection of additional electrons induced by broadening of Boltzmann distribution from the Fermi level. However, this case can be neglected in the system because the current level is not large enough to generate sufficient amount of heat required for noticeable hot electron injection. In the output curves in Figure 3.2, the onset of current mostly appeared when the current level is below 100 nA, with the lateral voltage of ~10 V. Even considering the contact and channel resistances together, the total electrical power generated in the device is expected to be at most ~3 μW. To find the total area through which the current is injected, I assume a transfer length at the contact of ~0.5 μm from known values in similar systems.[17,18] Then, the total area including contacts and the channel is ~7.9 μm^2, which yields power per unit area of ~0.38 $\mu W/\mu m^2$. In a multi-layer WSe_2 FETs similar to our devices, the temperature dependence on electrical power density was determined to be ~0.3 K per 1 $\mu W/\mu m^2$.[19] From this result, the average temperature increase (ΔT) at high V_{ds} limit in our device is estimated to be ~0.11 K. Even if we consider strong current crowding and assume current injection near the edge to be ten times the average value, the local temperature increase would be ΔT ~1 K, which is negligible in room temperature measurements.

The possible cases of current crowding and avalanche multiplication are discussed through the effects of gate voltage.

3.3.2 Gate bias dependence of $I-V$ curves

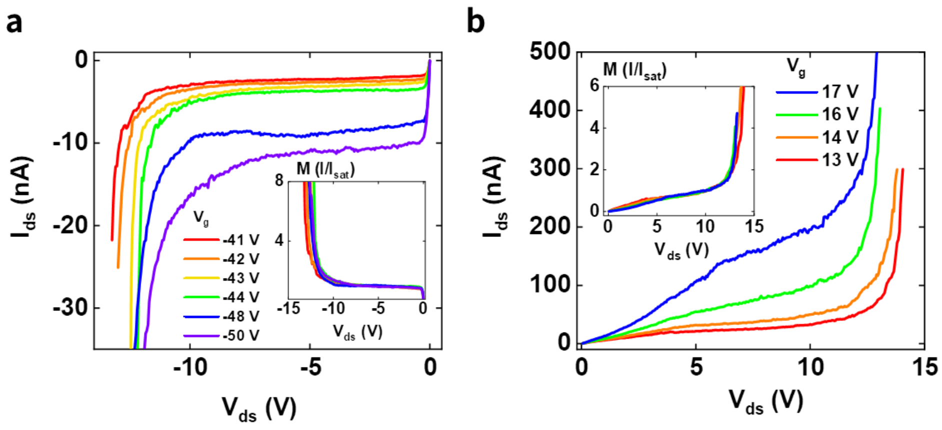

Figure 3.3 Output curves of the device of channel length 0.5 μm at various gate bias in (a) hole transport and (b) electron transport.

Figure 3.3 presents the output curves of a representative device of channel length L = 0.5 μm at various gate voltages. Secondary non-linear current after the saturation region was observed in all of the measurements. However, contrary to ambipolar transport occurring in FETs of longer devices, the secondary increase of current did not begin at different voltages. Instead, the current multiplied at a similar rate from its saturation value regardless of the gate voltage, as shown by the multiplication factor ($M = I/I_{sat}$) values in the insets of Figure 3.3a and b. This data rules out current crowding at the contacts. If considerable current crowding was taking place at the contacts, the behavior of multiplication factor would have changed with gate voltage since the transfer length varies accordingly.[18] Since the data is independent of the applied gate voltage, it is more plausible that the multiplication in the system is caused by avalanche multiplication instead of other factors such as Joule heating or current crowding at the contacts.

Since the increase of current is due to avalanche multiplication instead of ambipolar transport, the phenomenon is described through a variable different from the critical voltage used for ambipolar transport. In the case of avalanche multiplication, breakdown voltage (V_b) is defined as the voltage where the current diverges to infinity. However, because the current through the device is limited to an extent due to other practical factors, V_b is obtained through extrapolation of the relation between M and V_{ds}. The comparison between breakdown voltages in these short-channel devices and critical voltages in the long-channel devices in Chapter 2 are summarized in Figure 3.4.

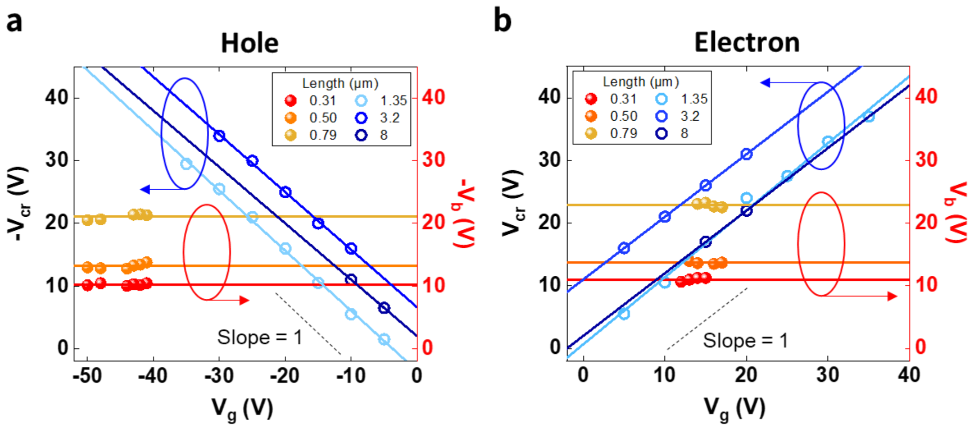

Figure 3.4 Comparison of critical voltages (V_{cr}) of long-channel devices and breakdown voltages (V_b) of short-channel devices, for (a) p-type (negative V_g) and (b) n-type (positive V_g). V_{cr} values are represented with blue open circles, while V_b values are represented with red filled circles.

Here, V_{cr} values are represented with blue open circles, while V_b values are represented with red filled circles. The fit lines for long-channel devices have slopes close to 1 (shown in dotted lines), which agrees with the ambipolar transport model described in the previous chapter. On the other hand, the breakdown voltages of short-channel devices were not strongly affected by the gate voltage but stayed nearly constant regardless of the applied V_g. In an atomically thin channel, the vertical movement of carriers is negligible, and the magnitude of applied V_g has little effect on the kinetic energy of charge carriers. Hence, modulation of V_g only changes the overall carrier concentration but not the multiplicative behavior. Instead, the V_b values increased with channel length, which is an indication that the mechanism of the observed breakdown phenomenon is related to the lateral electric field in the channel. This channel length dependency is not observed in V_{cr} values of long-channel devices, because ambipolar transport is governed only by the threshold voltages of both polarities, which in turn is affected by the dielectric constant but not the channel length of the device.

The channel dimensions and thicknesses of the devices included in Figure 3.4 are summarized in Table 3.1 below.

Device	Channel Length (μm)	Channel Width (μm)	Thickness (nm)
Long #1	1.35	1.73	0.7
Long #2	3.2	9.9	9.8
Long #3	8	7.3	16
Short #1	0.31	2.95	5.3
Short #2	0.5	3.04	5.3
Short #3	0.79	3.22	5.3

Table 3.1 Channel length, width and thickness of the long-channel and short-channel devices included in Figure 3.4

3.3.3 Band structure discussion

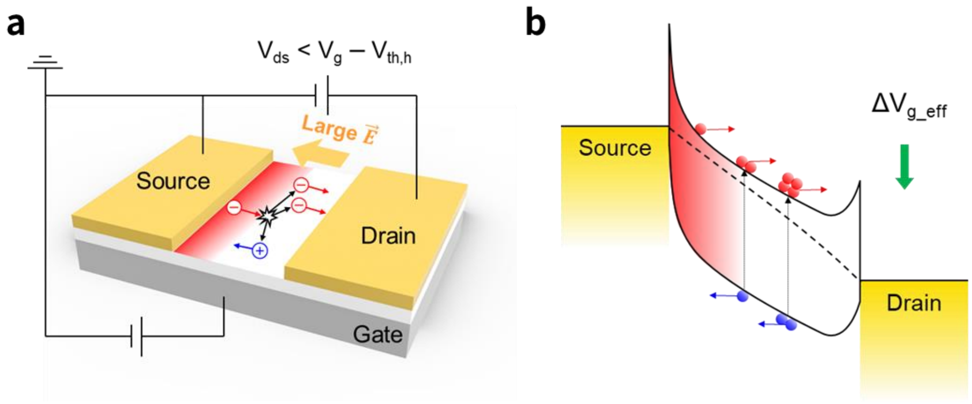

Figure 3.5 (a) Schematic diagram of the short-channel device in n-type operation mode showing electron-induced avalanche multiplication in the channel. (b) Band structure of the device during avalanche multiplication. Fermi level throughout the channel is drawn with a dotted curve.

The operation of avalanche multiplication is described through charge carrier distribution and band structure description. Figure 3.5a shows the carrier density throughout the channel while high lateral voltage (V_{ds}) is applied. Due to the short channel length, a high lateral electric field is created at relatively low V_{ds}, enough to induce avalanche multiplication before reaching the critical voltage for ambipolar transport. As the large electric field accelerates electrons, they gain enough energy to knock off bound electrons from atoms upon collision, generating electron-hole pairs. These newly created charge carriers are subsequently accelerated in opposite directions and undergo the same operation in a chain reaction, resulting in an avalanche breakdown.[20] It is notable that while avalanche multiplication had been traditionally studied in p-n junctions based on 3D semiconductors, many reports have successfully demonstrated the phenomenon and its application in photodetectors using an FET structure with 2D materials and metal electrodes.[21]

It has been previously studied in the case of bulk semiconductors that electrons and holes generally contribute to impact ionization at different rates.[14-16,22] To accurately determine the ionization rate of each carrier type, many experiments controlled the initial conditions to allow only unipolar injection in bipolar transistors or diodes.[22,23] In my experiment, the unipolar carrier injection was accomplished through electrostatic gating, which allows only one type of carrier to be injected from the source electrode. The corresponding band structure is illustrated in Figure 3.5b. The high electric field in the channel is portrayed as a steep slope the conduction and valence bands. In the n-type operation where $V_g > 0$, the Fermi level (E_F) of the channel near the source electrode is close to the conduction band minimum, allowing the injection of electrons. Toward the drain electrode, V_{g_eff} is lowered, and pinch-off occurs similarly to long-channel devices. However, before the drain voltage is increased enough to induce the accumulation of holes, avalanche multiplication occurs throughout the channel. Here, the modulation of effective gate voltage is small, so the band bending at the interface and the height of the Schottky barrier are reduced by a small amount, as illustrated by the green arrow in Figure 3.5b. Note that a sharp barrier is drawn at the interface between the channel and the source, in order to express the high work function of the Pd electrode in comparison to the energy level of the WSe_2 channel. However, the barrier is thin enough for electrons to tunnel through, which can be confirmed through the output curves of these devices indicating negligible Schottky barrier (shown in Figures 3.2 and 3.3).

3.3.4 Multiplication factors of electrons and holes

Although the discussion in the previous section has been considering the electron-initiated avalanche multiplication, the case of multiplication initiated by holes can be described in a similar manner, with the direction of V_{ds} and V_g replaced to negative values. A direct comparison between the ionization rates of electrons and holes is possible because WSe_2 is an ambipolar material and its majority charge carrier polarity can be easily tuned through electrostatic gating. This section summarizes the difference between the multiplication factors (M) of electrons and holes.

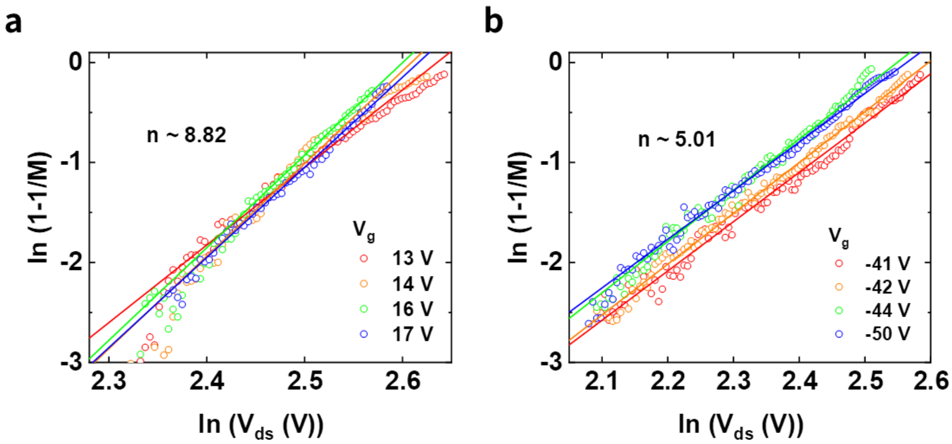

Figure 3.6 Logarithmic plot of (1-1/M) *versus* V_{ds} in (a) electron-initiated and (b) hole-initiated avalanche multiplication. n is the ionization index.

Figure 3.6 illustrates the dependence of the multiplication factor M on lateral voltage V_{ds} for electrons and holes, which is directly acquired from the $I-V$ measurements. As briefly mentioned in the Introduction, M is known to follow an empirical formula,

$$1 - \frac{1}{M} = \left(\frac{V}{V_b}\right)^n \tag{3.1}$$

where n is the ionization index, for conventional semiconductors such as Ge[1] and

Si,[14] and also 2D materials such as InSe,[6] black phosphorus[11] and Bi_2O_2Se.[24] In my experiment, the *M* values for electrons and holes was independently measured through controlling unipolar injection *via* electrostatic gating. Measurements at various gate voltages show no notable difference between the values of *M* and the slope of the graphs, which is anticipated because V_g influences only the total number of charge carriers involved in the carrier multiplication process but not the lateral field strength that drives the impact ionization in the 2D channel. The average values of the parameter *n* in electron- and hole-initiated multiplication are determined to be ~8.82 and ~5.01, respectively, for the selected device. However, these values ranged between 3 and 9 in different devices. Such variance has been previously observed in Si bipolar junction transistors (BJTs) with values from 2 to 5 and is understood to be dependent on temperature and doping profile in the case of BJT structure.[25] In 2D FET systems, this variance could be affected by interfacial defects between the channel and the dielectric, which would hinder carrier multiplication due to increased scattering. Although additional experiments with the control of interfacial defects (*i.e.*, by using top and bottom hBN encapsulation) would lead to more reliable results, the values of parameter *n* observed in WSe_2 FETs are consistent within the range of reported values for other 2D semiconductor.[6,10-11]

3.3.5 Breakdown voltage and impact ionization rates

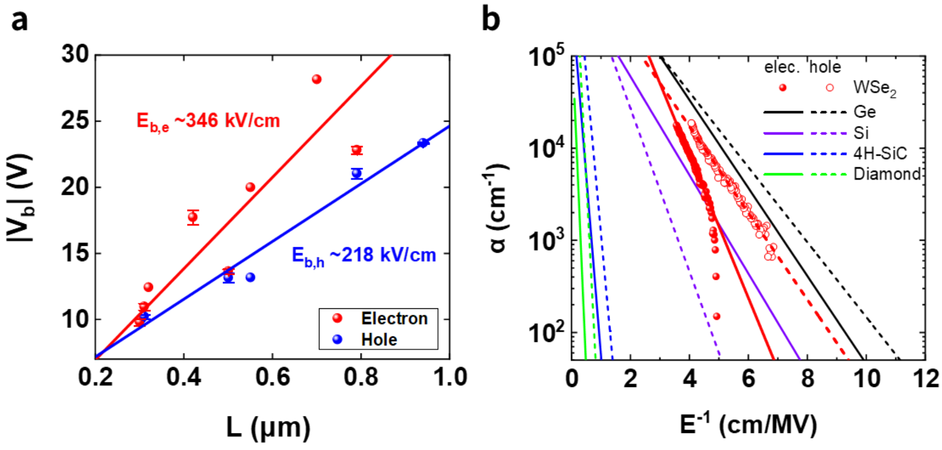

Figure 3.7 (a) Breakdown voltages as a function of channel length for *n*-type and *p*-type operation modes. The slopes are the breakdown field for electrons ($E_{b,e}$) and holes ($E_{b,h}$). (b) Ionization rates (α) of electrons and holes as a function of inverse electric field for WSe_2 in comparison with various materials.

The breakdown voltages (V_b) with respect to the channel length (L) of various devices are summarized in Figure 3.7a. The relationship clearly shows a linear dependence of V_b on L. The slopes of the graphs $(V_b/L = E_b)$ defines the breakdown field, which is an intrinsic property of the semiconductor material. The E_b values of electrons and holes deduced from my experiments are ~346 and ~218 kV/cm, respectively, which are comparable to the previously reported values for MoS_2.[9]

Another important parameter describing the avalanche multiplication phenomenon in a semiconductor material is the impact ionization rate α, which is defined as the number of generated electron-hole pairs by an initial charge carrier per unit distance travelled.[26] From the basic model describing the number of electrons in an electron-initiated multiplication,[20] the relationship between M and α

can be written in the form of

$$1 - \frac{1}{M} = \int_0^W \alpha_n \exp\left[-\int_0^x (\alpha_n - \alpha_p) dx'\right] dx \tag{3.2}$$

where α_n and α_p are ionization rates of electrons and holes, respectively, and W is the width of the junction where multiplication occurs.

Since the equation (3.2) is difficult to solve analytically, some assumptions are made to simplify the relation. Under the approximation of $\alpha_n = \alpha_p$, which can be used within a reasonable error range,[27] equation (3.2) can be turned into

$$1 - \frac{1}{M} = \int_0^W \alpha_n \, dx \tag{3.3}$$

Also, another approximation is made for uniform electric field within the WSe_2 channel, which further simplifies the above equation into

$$\alpha = \frac{1}{L}\left(1 - \frac{1}{M}\right) \tag{3.4}$$

The extracted impact ionization rates of WSe_2 using the equation (3.4) for electrons and holes are plotted in Figure 3.7b and compared with reported values of various conventional materials.[28,29] The impact ionization rate is naturally a function of electric field because the charge carriers can acquire enough kinetic energy to induce ionization at a shorter distance when the applied field is stronger. The model widely used in the literature to characterize impact ionization rates is the Shockley model,[30] given by

$$\alpha_{n,p} = \alpha_{n,p}^{\infty} \exp\left(-\frac{\beta_{n,p}}{E}\right) \tag{3.5}$$

where the subscripts n and p represent electrons and holes, respectively, and $\alpha_{n,p}^{\infty}$ and $\beta_{n,p}$ are the ionization coefficients. My data measured from the representative

WSe_2 FET are well fitted to the model, as shown by the fit lines (red lines) in Figure 3.7b, with

$$\alpha_n = 1.08 \times 10^7 \exp\left(-1.79 \times \frac{10^6}{E}\right)$$

$$\alpha_p = 1.31 \times 10^6 \exp\left(-1.08 \times \frac{10^6}{E}\right)$$

The values of α_n and α_p calculated from other devices are summarized in Table 3.2.

Device	α_n^∞	β_n	α_p^∞	β_p
A	2.76×10^7	-2.43×10^6	1.44×10^6	-1.23×10^6
B	1.08×10^7	-1.79×10^6	1.31×10^6	-1.08×10^6
C	2.10×10^6	-1.47×10^6	4.57×10^5	-9.81×10^5
D	1.75×10^6	-1.34×10^6		
E	2.90×10^6	-1.77×10^6		
F			2.05×10^5	-7.59×10^5

Table 3.2 Measured parameters of impact ionization rates in several WSe_2 FETs

The obtained ionization rates of WSe_2 can be understood through the band gap analysis of avalanche multiplication in 3D materials. From the band-to-band ionization model, materials with higher band gap requires a higher electric field to initiate impact ionization, and the data from the previously reported bulk materials follow this trend as shown in Figure 3.7b. Few-layer WSe_2 with a band gap (~1.2 eV) similar to Si (1.12 eV) has ionization rates close to Si in the evaluated range. Note that the β values (*i.e.,* the slope of the graphs in Figure 3.7b) of WSe_2 are found to be similar to those of conventional 3D materials. However, there has been little research that has explicitly evaluated the ionization rates of 2D materials to determine if there is a fundamental difference in ionization rates of 2D from those of bulk materials.

Another noticeable feature is the relative magnitude of ionization rates of electrons and holes. The ionization rate of electrons in WSe_2 is lower than that of holes, similar to most bulk materials, whereas the opposite is true for Si. This result is in agreement with the breakdown fields obtained in Figure 3.7a, because electrons would require higher electric field to initiate avalanche breakdown due to their lower ionization rates than holes. A fundamental reason behind this discrepancy is not clearly understood, but combined effects of effective mass, mean free path of carriers, and also the shape of the band near the band gap are expected to influence the ionization rates.[22,31] Further studies on impact ionization in other semiconductors are desired for understanding the precise physics that determine the ionization rates of electrons and holes.

3.3.6 Selective engineering of ambipolar transport and avalanche multiplication

Lastly, I propose a method for selectively engineering the two competing phenomena of ambipolar transport and avalanche multiplication. Based on the results of gate-dependent measurements in Figure 3.4, the transition length between the two phenomena is shown to be approximately 1 μm for the system under consideration. This value is affected by the dielectric constant, because the gate window between threshold voltages of electrons and holes will be reduced with higher dielectric constant κ. Then, ambipolar transport will begin at a smaller lateral voltage[32] while avalanche multiplication is unaffected by such modification of gate dielectric, thus shortening the transition length. In the opposite manner, using low-κ dielectric will increase the transition length, because ambipolar transport is suppressed.

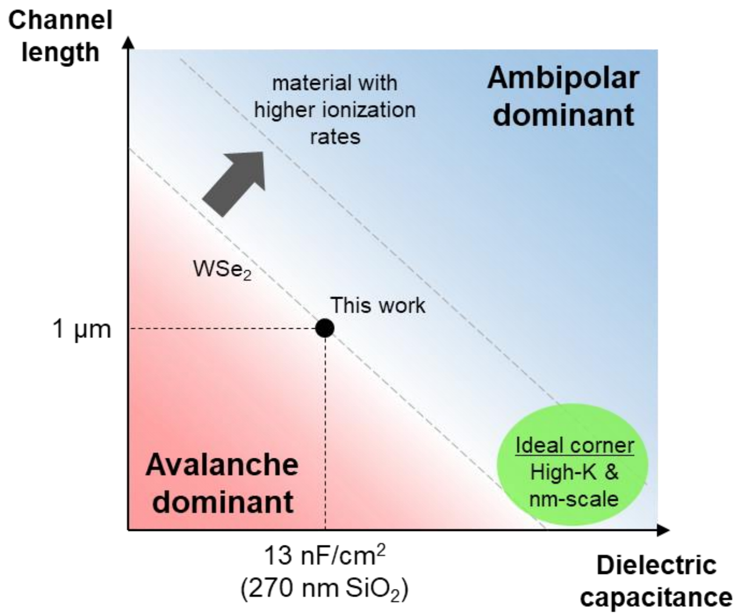

Figure 3.8 Illustration of dominant phenomenon between avalanche multiplication and ambipolar transport under varying conditions of channel length and dielectric capacitance.

This balance between the two phenomena is summarized in Figure 3.8, where both axes are drawn qualitatively in logarithmic scale. The transition point moves along the dotted line drawn for WSe_2, with the length inversely proportional to the dielectric capacitance. Meanwhile, changing the channel material will move the boundary line itself, because the breakdown voltage and gate threshold window will be different for other materials.

It may be useful to combine both phenomena together in a more complex device configuration, taking advantage of simultaneous injection and flow of both charge carriers (ambipolar transport) and intrinsic carrier multiplication inside the channel (avalanche multiplication). To utilize such balance of avalanche multiplication and ambipolar transport for engineering purposes, it is best to choose the channel length and the gate dielectric constant in the green region in Figure 3.8. In this region, the channel length is very short, and the dielectric constant is large. Requiring only small voltages to induce either phenomenon. this is the most suitable condition to realize low-power electronics.

3.4. Conclusion

In this chapter, avalanche multiplication in few-layer WSe_2 FETs is examined from the non-linear transport at high lateral voltages. Other possible origins such as hot electron injection from Joule heating and current crowding at the contacts are systematically analyzed and eliminated. There were similarities in current−voltage characteristics with respect to ambipolar transport, showing triode, saturation and non-linear regions. In order to distinguish between avalanche multiplication and ambipolar transport, the method of channel length modulation was proposed.

Devices with shorter channels exhibited avalanche multiplication because the lateral electric field was large enough to cause impact ionization, while devices with longer channels exhibited ambipolar transport because of the reversal of effective gate voltage near the drain electrode. The two competing phenomena were characterized by the dependency of critical & breakdown voltage with respect to gate bias, where ambipolar transport showed linear dependency but avalanche multiplication showed negligible correlation with the gate bias.

Following the distinction of avalanche multiplication from other phenomena, the impact ionization rates of electrons and holes in WSe_2 were separately investigated through limiting the initial conditions to unipolar carrier injection by electrostatic gating. The ionization rates of electrons were found to be smaller than holes in the studied range but had greater dependence on the applied electric field. The comparison of breakdown voltages coincided with the result, showing larger breakdown voltages of electrons than holes. The observed differences in the multiplicative properties between electrons and holes call for further studies on the fundamental mechanism of field-induced carrier multiplication process in 2D materials.

References

1. Miller, S. L., Avalanche breakdown in germanium. *Physical Review* **1955,** *99* (4), 1234-1241.
2. Kardynał, B. E.; Yuan, Z. L.; Shields, A. J., An avalanche-photodiode-based photon-number-resolving detector. *Nature Photonics* **2008,** *2* (7), 425-428.
3. Gopalakrishnan, K.; Griffin, P. B.; Plummer, J. D. In *I-MOS: a novel semiconductor device with a subthreshold slope lower than kT/q*, Digest. International Electron Devices Meeting, 8-11 Dec. 2002; 2002; pp 289-292.
4. Gao, A.; Lai, J.; Wang, Y.; Zhu, Z.; Zeng, J.; Yu, G.; Wang, N.; Chen, W.; Cao, T.; Hu, W.; Sun, D.; Chen, X.; Miao, F.; Shi, Y.; Wang, X., Observation of ballistic avalanche phenomena in nanoscale vertical InSe/BP heterostructures. *Nature Nanotechnology* **2019,** *14* (3), 217-222.
5. Liu, Y.; Guo, J.; Song, W.; Wang, P.; Gambin, V.; Huang, Y.; Duan, X., Ultra-Steep Slope Impact Ionization Transistors Based on Graphene/InAs Heterostructures. *Small Structures* **2021,** *2* (1), 2000039.
6. Lei, S.; Wen, F.; Ge, L.; Najmaei, S.; George, A.; Gong, Y.; Gao, W.; Jin, Z.; Li, B.; Lou, J.; Kono, J.; Vajtai, R.; Ajayan, P.; Halas, N. J., An Atomically Layered InSe Avalanche Photodetector. *Nano Letters* **2015,** *15* (5), 3048-3055.
7. Ahmed, F.; Kim, Y. D.; Yang, Z.; He, P.; Hwang, E.; Yang, H.; Hone, J.; Yoo, W. J., Impact ionization by hot carriers in a black phosphorus field effect transistor. *Nature Communications* **2018,** *9* (1), 3414.
8. Hattori, Y.; Taniguchi, T.; Watanabe, K.; Nagashio, K., Impact ionization and transport properties of hexagonal boron nitride in a constant-voltage measurement. *Physical Review B* **2018,** *97* (4), 045425.
9. Pak, J.; Jang, Y.; Byun, J.; Cho, K.; Kim, T.-Y.; Kim, J.-K.; Choi, B. Y.; Shin, J.; Hong, Y.; Chung, S.; Lee, T., Two-Dimensional Thickness-Dependent Avalanche Breakdown Phenomena in MoS2 Field-Effect Transistors under High Electric Fields. *ACS Nano* **2018,** *12* (7), 7109-7116.
10. Jia, J.; Jeon, J.; Park, J. H.; Lee, B. H.; Hwang, E.; Lee, S., Avalanche Carrier Multiplication in Multilayer Black Phosphorus and Avalanche Photodetector. *Small* **2019,** *15* (38), 1805352.
11. Deng, W.; Chen, X.; Li, Y.; You, C.; Chu, F.; Li, S.; An, B.; Ma, Y.; Liao, L.; Zhang, Y., Strain Effect Enhanced Ultrasensitive MoS2 Nanoscroll Avalanche Photodetector. *The Journal of Physical Chemistry Letters* **2020,** *11* (11), 4490-4497.
12. Gao, A.; Zhang, Z.; Li, L.; Zheng, B.; Wang, C.; Wang, Y.; Cao, T.; Wang, Y.; Liang, S.-

J.; Miao, F.; Shi, Y.; Wang, X., Robust Impact-Ionization Field-Effect Transistor Based on Nanoscale Vertical Graphene/Black Phosphorus/Indium Selenide Heterostructures. *ACS Nano* **2020,** *14* (1), 434-441.

13. Seo, J.; Lee, J. H.; Pak, J.; Cho, K.; Kim, J.-K.; Kim, J.; Jang, J.; Ahn, H.; Lim, S. C.; Chung, S.; Kang, K.; Lee, T., Ultrasensitive Photodetection in MoS2 Avalanche Phototransistors. *Advanced Science* **2021,** *8* (19), 2102437.
14. Lee, C.; Logan, R.; Batdorf, R.; Kleimack, J.; Wiegmann, W., Ionization rates of holes and electrons in silicon. *Physical review* **1964,** *134* (3A), A761-A773.
15. Ito, M.; Kagawa, S.; Kaneda, T.; Yamaoka, T., Ionization rates for electrons and holes in GaAs. *Journal of Applied Physics* **1978,** *49* (8), 4607-4608.
16. Niwa, H.; Suda, J.; Kimoto, T., Impact ionization coefficients in 4H-SiC toward ultrahigh-voltage power devices. *IEEE Transactions on Electron Devices* **2015,** *62* (10), 3326-3333.
17. Allain, A.; Kang, J.; Banerjee, K.; Kis, A., Electrical contacts to two-dimensional semiconductors. *Nature Materials* **2015,** *14* (12), 1195.
18. Moon, I.; Choi, M. S.; Lee, S.; Nipane, A.; Hone, J.; Yoo, W. J., Analytical measurements of contact resistivity in two-dimensional WSe2 field-effect transistors. *2D Materials* **2021,** *8* (4), 045019.
19. Majee, A. K.; Hemmat, Z.; Foss, C. J.; Salehi-Khojin, A.; Aksamija, Z., Current Rerouting Improves Heat Removal in Few-Layer WSe2 Devices. *ACS Applied Materials & Interfaces* **2020,** *12* (12), 14323-14330.
20. McKay, K. G., Avalanche Breakdown in Silicon. *Physical Review* **1954,** *94* (4), 877-884.
21. Miao, J.; Wang, C., Avalanche photodetectors based on two-dimensional layered materials. *Nano Research* **2021,** *14* (6), 1878-1888.
22. Miller, S., Ionization rates for holes and electrons in silicon. *Physical Review* **1957,** *105* (4), 1246-1249.
23. Woods, M. H.; Johnson, W. C.; Lampert, M. A., Use of a Schottky barrier to measure impact ionization coefficients in semiconductors. *Solid-State Electronics* **1973,** *16* (3), 381-394.
24. Sangwan, V. K.; Kang, J.; Lam, D.; Gish, J. T.; Wells, S. A.; Luxa, J.; Male, J. P.; Snyder, G. J.; Sofer, Z.; Hersam, M. C., Intrinsic carrier multiplication in layered Bi2O2Se avalanche photodiodes with gain bandwidth product exceeding 1 GHz. *Nano Research* **2021,** *14* (6), 1961-1966.
25. Levinshtein, M. E.; Kostamovaara, J.; Vainshtein, S., *Breakdown phenomena in semiconductors and semiconductor devices*. World Scientific: 2005; Vol. 36.

26. Maes, W.; De Meyer, K.; Van Overstraeten, R., Impact ionization in silicon: A review and update. *Solid-State Electronics* **1990,** *33* (6), 705-718.
27. Chynoweth, A. G., Ionization Rates for Electrons and Holes in Silicon. *Physical Review* **1958,** *109* (5), 1537-1540.
28. Mikawa, T.; Kagawa, S.; Kaneda, T.; Toyama, Y.; Mikami, O., Crystal orientation dependence of ionization rates in germanium. *Applied Physics Letters* **1980,** *37* (4), 387-389.
29. Rashid, S. J.; Tajani, A.; Coulbeck, L.; Brezeanu, M.; Garraway, A.; Butler, T.; Rupesinghe, N. L.; Twitchen, D. J.; Amaratunga, G. A. J.; Udrea, F.; Taylor, P.; Dixon, M.; Isberg, J., Modelling of single-crystal diamond Schottky diodes for high-voltage applications. *Diamond and Related Materials* **2006,** *15* (2), 317-323.
30. Shockley, W., Problems related to p-n junctions in silicon. *Solid-State Electronics* **1961,** *2* (1), 35-67.
31. Konstantinov, A. O.; Wahab, Q.; Nordell, N.; Lindefelt, U., Ionization rates and critical fields in 4H silicon carbide. *Applied Physics Letters* **1997,** *71* (1), 90-92.
32. Zhang, Y.; Suzuki, R.; Iwasa, Y., Potential Profile of Stabilized Field-Induced Lateral p–n Junction in Transition-Metal Dichalcogenides. *ACS Nano* **2017,** *11* (12), 12583-12590.

Chapter 4. Summary

In this thesis, I devised a simple and robust method of channel length modulation to distinguish the two contrasting phenomena of ambipolar transport and avalanche multiplication in WSe_2 FETs, both of which can take place in FETs with ambipolar 2D channel materials in general. The key insight is that ambipolar transport is governed by the voltage difference between drain and gate electrodes, while avalanche multiplication is induced by strong lateral electric field in the channel. Hence, devices with longer channels exhibited ambipolar transport characteristics, while avalanche multiplication was dominant in devices with shorter channels.

In the first part, I analyzed ambipolar transport in long-channel devices, which was characterized by the linear shift of the critical voltage in proportion with the modulation of gate bias, as well as the parabolic shape of the secondary current. The three distinct transport regimes were explained with charge carrier distribution throughout the channel at each of the ranges of drain-source voltage. The working mechanism of the phenomenon is discussed through the band alignment and the energy levels in the channel.

In the second part, I examined the avalanche multiplication phenomenon in WSe_2 FETs. In order to suppress ambipolar transport while obtaining high lateral electric field enough to induce impact ionization, very short channel lengths of less than 1 μm were required. Other than the two competing phenomena, possible origins of secondary rise of current such as Joule heating and current crowding were systematically discussed and eliminated. The linear dependence of breakdown voltage on channel length yielding a common, intrinsic breakdown field was given as the decisive criterion for avalanche multiplication. The contrasting results from ambipolar transport were discussed through the band structure description. Once avalanche multiplication was successfully distinguished from other phenomena, the impact ionization rates of electrons and holes in WSe_2 were compared. Ionization rates of holes were found to be higher than electrons, which coincided with the lower breakdown voltage of holes compared to electrons. Finally, I analyzed the relative dominance between ambipolar transport and avalanche multiplication in a WSe_2 FET system with varying channel length and dielectric capacitance. Ambipolar transport was dominant towards longer channel and higher dielectric constant, and avalanche multiplication vice versa. From this balance, I proposed a method of selectively engineering the two competing phenomena of ambipolar transport and avalanche multiplication through a careful choice of the channel and dielectric materials.

Ambipolar transport and avalanche multiplication are two completely different phenomena, and research interests in both fields are showing a steady increase in the past few years, especially using 2D materials as the active channel. The occurrence of both phenomena in an identical 2D FET system can be misleading if not examined thoroughly, but it can also turn into an opportunity of integrating both phenomena for applications with a simple device structure and low-cost fabrication process. Hence, the method of discriminating the two phenomena through channel length modulation proposed in this thesis could serve as an efficient tool for developing high-performance and novel device architectures with ambipolar 2D materials.

국문초록

양극성 전이금속 칼코겐화합물 기반 전계효과 트랜지스터에서의 아발란치 증폭 현상 연구

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이차원 물질은 차세대 반도체 기술로 각광받고 있는 물질군 중 하나이다. 높은 전하이동도와 조절가능한 밴드 갭, 그리고 단원자 두께까지 유지되는 균일한 구조 등의 장점으로 인해 이차원 물질들은 트랜지스터, 광검출기, 센서, 나아가 뉴로모픽 소자까지 다양한 분야에서 활발하게 연구되고 있다. 최근 광전자학 분야에서의 잠재력에 힘입어 아발란치 증폭을 이차원 물질에 도입하는 연구들이 보고되고 있다. 기존 연구들은 주로 재료 물질과 소자 구조를 최적화하는 데 초점을 두고 있고, 그 결과로 적외선부터 자외선 영역까지 다양한 파장대의 고감도 광검출기를 구현하는데 성공하였다. 그러나 대부분의 분석은 상용화된 삼차원 물질에 대한 이론을 바탕으로 하고 있으며, 소자 성능 향상 및 새로운 소자구조 개발을 위해서는 이차원 물질에서의 아발란치 증폭에 대한 보다 근본적인 연구가 필수적이다.

가장 핵심이 되는 문제 중 하나는 전자와 양공의 충돌 이온화율에 대한 비교이다. 상용화된 삼차원 물질 대부분에 대해서는 이 두 값이 서로 다르다는 것이 알려져 있고, 물질에 따라서도 그 비율이 다르다. 그러나 이차원 물질에서 이 물리량들을 비교하는 연구는 아직까지 거의 보고된 바 없다. 동일한 물질 내에서 두 전하 운반자의 충돌 이온화율을 탐구하려면, 해당 물질은 각 전하 운반자의 흐름을 허용할 수 있도록

조절 가능해야 하고, 다시 말해 양극성 물질이어야 한다. 양극성 이차원 물질은 정전기적 게이팅을 통해 손쉽게 다수 캐리어를 전환할 수 있다는 장점이 있지만, 한 물질 내에 동시에 두 캐리어를 허용함으로 인해 각각이 아발란치 증폭에 미치는 영향을 분석하는 데 있어 내재적인 어려움이 있다. 양극성 전계효과 트랜지스터에서는 양극성 수송과 아발란치 증폭의 두 가지 현상이 일어날 수 있는데, 두 현상 모두 고전압에서 출력 특성곡선의 전류가 재차 증가하는 모습을 보인다. 본 연구에서는 채널 길이 조절 방법을 통해 이 두 현상을 분리하였고, 양극성 물질인 WSe_2 전계효과 트랜지스터에서 전자 혹은 양공으로 개시된 아발란치 증폭의 성질을 성공적으로 비교하였다.

본 연구에서는 먼저 상대적으로 긴 채널 길이의 소자에서 나타나는 양극성 수송을 분석하였다. 양극성 수송은 전자와 양공이 채널 안에서 동시에 흐르며 총 전류에 기여하는 현상이다. 이 현상은 드레인 전압이 게이트 전압을 넘어서며, 드레인 전극 주변의 채널에서 국소적으로 게이팅 방향이 뒤바뀔 때 일어난다. WSe_2 전계효과 트랜지스터에서 위 현상이 나타남을 확인하기 위해, 다양한 게이트 전압 조건에서 고전압 측정을 수행하였다. 이차적인 전류가 시작되는 임계점은 게이트 전압 변화에 따라 함께 변하였으며, 이는 양극성 수송 모형에 대한 직접적인 증거로 볼 수 있다. 또한 전하 운반자 분포와 밴드구조 묘사를 통해 위 현상의 작동원리를 논하였다.

다음으로, 상대적으로 짧은 채널 길이의 소자에서 나타나는 아발란치 증폭을 분석하였다. 여기서는 긴 채널 소자에 비해 측면 방향의 전기장이 매우 강하고, 따라서 양극성 수송의 임계점에 도달하기 전에 높은 전기장으로 인한 아발란치 증폭이 일어날 수 있다. 여러 채널 길이의 소자를 측정한 결과에서는 항복 전압과 채널 길이 사이의 분명한 상관관계가 나타났으며, 이 관계에서 아발란치 증폭 모형으로 설명되는 내재적인 항복 전기장 값을 도출할 수 있었다. 역시 밴드구조 묘사를 활용하여 이전 장에서의 결과와의 차이를 설명하였다. 또한 증폭 계수와

항복 전압 간의 관계를 분석함으로, 연구의 핵심 목표였던 전자와 양공의 충돌 이온화율을 도출하고 비교하였다. 양공의 충돌 이온화율이 전자보다 높았으며, 이 결과는 양공의 항복 전압이 더 낮게 나타난 것과 일치한다. 마지막으로, 채널 물질과 유전체를 세심하게 선택함으로써 서로 경쟁 관계에 있는 양극성 수송과 아발란치 증폭을 선택적으로 활용할 수 있는 방법을 제시하였다.

본 연구의 핵심 의의는 서로 유사해 보이는 양극성 수송과 아발란치 증폭을 분리하고 정밀히 분석할 수 있는 간단하면서도 탄탄한 방법을 고안한 데 있다. 이차원 물질의 상용화가 가까워지고 있고, 두 현상에 대한 연구들도 점점 확장되어 가는 시점에, 본 연구는 양극성 수송과 아발란치 증폭을 활용하는 참신한 구조와 고성능의 소자 개발에 기여할 것이다.

주요어 : 전이금속 칼코겐화합물, 이차원 물질, 아발란치 증폭, 양극성 수송, 전계효과 트랜지스터

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감사의 글

6년 반이라는 대학원 생활, 더 길게는 이십 대 전부를 보낸 서울대에서의 삶이 막을 내리려 합니다. 찬찬히 돌아볼 때, 제게 있어 대학원 기간은 열정이 넘치는 도전의 장보다는, 끝이 보이지 않는 어두운 터널이자 망망대해 한가운데 홀로 표류한 것처럼 느껴졌던 시간이 훨씬 길었던 것 같습니다. 한 번의 연구실 변경과 이어진 주제 폐기, 이후로도 긴 시간 동안 계속해서 예상치 못한 방향으로 흘러가는 연구. 주변 사람들은 다들 논문 한 편은 냈던 연차가 1년 2년 지나면 지날수록 실패감과 무력감이 한없이 쌓여만 갔고, 진지하게 자퇴를 고민하기도 했습니다. 그러나 오히려 그런 시간이었기 때문에 저는 제가 뛰어나서 학위를 받는다기보다는 감사할 것밖에 없다고 느낍니다. 제게 있어 대학원이라는 장소는 인내와 겸손, 감사와 주변 이들에 대한 소중함을 가르쳐 주는 곳이었습니다. 참으로 오랫동안 저의 옆을 지켜주고, 위로해 주고, 지탱해 준 분들이 아니었더라면 이 경주를 끝내지 못했을 것입니다.

가장 먼저, 세상에 둘도 없는 최고의 부모님께 진심으로 감사드립니다. 어떤 고민을 털어놓아도 귀 기울이고 위로해 주신, 그리고 어떤 상황에서도 엄마는 네 편이라고 말해 주시던 우리 엄마. 피곤할 때면 부탁하지 않아도 왕복 두 시간이 넘는 거리를 차로 수없이 많이 태워 주신, 표현은 잘 하지 않으면서도 묵묵하게 항상 앞서 챙겨 주신 우리 아빠. 철부지 아들을 말로 다 표현할 수 없이 사랑해 주시는 두 분이 계셨기에 주말마다 올라가는 집이 마음의 안식처였고, 끝끝내 여기까지 올 수 있었습니다. 결혼해서 나온 후에는 깊은 대화를 할 수 있는 시간도 줄고, 사랑하고 감사하다는 표현도 많이 못했던 것 같은데, 앞으로 더 많이 표현할게요. 사랑해요 엄마 아빠.

영적인 부모와 같이 저를 사랑해 주시고 양육해 주신 이문선 목사님, 유승자 사모님, 보라 선교사님, 그리고 동백이 형께도 감사드립니다. 많은 사역으로 바쁘시면서도 틈틈이 제 상황들을 기억하고 물어봐 주시는, 저희 아빠와 참 닮으신 목사님. 저와 비슷한 기질이셔서 가장 좋은 롤 모델이 되시는, 한없는 사랑과 동시에 정확한 권면으로 이끌어 주시는 사모님. 진심으로 자신을 다 내어주시는, 예수님의 사랑을 떠올리게 하시는 보라 선교사님. 어떤 상황에서도 의지가 되고 위로가 되는, 온유함의 대명사 동백이 형. 그리스도의 몸인 교회 공동체를 위한 그 헌신의 사랑을, 저도 시간이 지나며 조금씩 더 알아가게 되는 것 같습니다. 특히 최근 몇 년 동안 세 분 모두에게 직접 양육 받을 수 있어서 감사했습니다. 제가 막막하고 고단한 마음을 토로할 때 깊이 들어 주시고 또 기도

해 주셔서, 저도 매주 다시금 주님을 붙잡고 소망하며 갈 수 있었습니다. 저도 목사님 가정을 위해 더욱 기도하고, 그 사랑에 보답하고 또 흘려보내기를 힘쓰겠습니다.

최고의 인품을 가지신 이탁희 교수님, 존경하고 감사드립니다. 언제나 학생들을 배려해 주시고, 경청해 주시고, 존중해 주시는 교수님은 참으로 상사가 아니라 스승이셨습니다. 교수님의 지도 덕에 지난한 대학원 기간 가운데서도 버티고 힘낼 수 있었고, 무사히 박사과정을 마칠 수 있었습니다. 오랫동안 함께하고 싶은 좋은 연구실 동료들을 만나게 된 것도 교수님 덕분이고, 항상 감사한 마음입니다. 졸업 후에도 꼭 종종 찾아뵙겠습니다.

이어서 긴 시간을 함께 동고동락한 MNE 여러분들, 두 말 할 것도 없이 함께 해서 즐겁고 고마웠다고 이야기하고 싶습니다. 한 명 한 명 세 보았는데, 제가 연구실에 있는 동안 함께 시간을 보냈던 분들이 모두 서른 여섯 명이나 되더군요. 든든하게 연구실을, 그리고 저를 이끌어 주셨던 박사님들과 선배님들부터 이제 막 대학원이라는 여정을 시작하려는 꿈나무들까지 (그리고 MNE의 기둥인 고은 누나도), 많은 분들과의 추억이 새록새록하네요. 똑부러지는 사람, 시원시원한 사람, 섬세한 사람, 유쾌한 사람, 정 많은 사람 등… 정말 다양한 분들과 함께 있어서 그만큼 다채롭고 즐거웠던 시간이었습니다. 공통점이라면 모두 좋은 사람들이라는 점이겠죠. 제가 본 다른 어떤 연구실과도 비교할 수 없는, 가장 친밀하고 끈끈하고 행복한 연구실을 만들어 준 여러분 한 분 한 분께 감사합니다. 앞으로도 자주 연락하며 지내요!

나의 절친 성현아, 친구 중에 가장 고맙고 추억이 많은 한 명을 꼽으라면 단연 너일 거야. 고1 첫날부터 너는 참 나랑 잘 맞는 편한 친구였는데, 어느덧 14년이 지나는 동안 고등학교, 대학교, 교회에서 항상 같이 오고, 마지막 1년은 다시 캠퍼스와 제자반에서도 함께 하게 되었네. 이제는 정말 사랑의 사도라는 말이 가장 먼저 떠오를 정도로, 섬세하면서도 강단이 있는 너의 모습이 든든하고 앞으로도 어디에서 어떤 모습으로 쓰임 받을지 참 기대가 된다.

짧은 글에서 다 언급하지 못했지만 제 삶에 많은 부분을 차지하고 의지가 되었던 분들께도 진심으로 감사의 말씀 전합니다. 항상 든든하게 믿고 가는 청년 3부, 그리고 정말 가족처럼 생각하는 창대교회의 형 누나 동생들. 앞으로도 한 마음 한 뜻으로 믿음이 성숙해 가길 축복합니다. 16년도에 우연히 같이 복학해서 들은 수업을 통해 지금까지 베프가 된 은우와 광준이도 항상 내 마음에 편안함을 줘서 고맙고, 대학원 기간 함께 고생했던 물천12 동지들, 졸업한 친구들 수고 많았고 남은 친구들도 고지가 눈앞이니 힘내자!

마지막으로 나의 사랑하는 아내 다은이에게.

다은아, 우리가 처음 친구로 만났던 고등학교 3학년 때의 인연이, 평생의 동반자로 이어질 줄은 우리 둘 다 상상도 못 했는데, 이후로 여러 모습의 인도하심 가운데 기다림의 훈련도 있었고 말씀을 통한 인도하심도 있었지. 둘 모두 처음 걷는 길이었지만, 그 준비되는 시간을 한 마음으로 걸어올 수 있어서 나는 정말 감사해. 우리가 드렸던 작은 순종에 주님이 몇 배로 축복해 주신다는 것을 항상 느껴. 너는 내 삶의 가장 큰 축복이고, 너와 함께하는 매일매일이 기쁨으로 충만해. 항상 나를 사랑해 주고, 세워 주고, 믿음으로 먼저 이끌어 주기도 하는 등 모든 것들로 인해 고맙고, 이 대학원 기간의 마무리를 함께할 수 있어서 감사해. 결혼과 졸업, 많은 것들이 변하는 이 시기 가운데 서로를 더욱 주님께로 이끌어 주며 한 걸음씩 사랑하며 가자.

[야고보서 1:2-4]

2 내 형제들아 너희가 여러 가지 시험을 당하거든 온전히 기쁘게 여기라
3 이는 너희 믿음의 시련이 인내를 만들어 내는 줄 너희가 앎이라
4 인내를 온전히 이루라 이는 너희로 온전하고 구비하여 조금도 부족함이 없게 하려 함이라

사랑의 주님, 참 감사합니다.

지난 6년의 시간 동안, 이 곳에서 저를 빚어 주셔서 감사합니다.

믿음도 끈기도 열심도 항상 흔들리던 불안정한 제게, 이 시간을 통해 인내를 가르쳐 주시고, 주님을 의지하는 것을 알려 주시고, 또한 그 가운데 놀라운 인도하심들을 경험할 수 있게 하심에 감사합니다.

지금까지와는 완전히 다를 앞으로의 삶에서, 어디로 저를 인도하시고 어떻게 저를 사용하실 지 기대됩니다.

오직 구하는 것은, 주님을 향한 믿음이 더욱 굳건해지도록, 그리하여 저를 보내실 곳에서 주님의 뜻이 이루어지는 삶이 되기를 간절히 구합니다.

예수님의 이름으로 기도드립니다.

아멘.