이학석사 학위논문

Indium telluride grown by molecular beam epitaxy for electronic devices

분자선 에피택시를 이용한 전자소자를 위한 인듐 텔루라이드 성장

2023년 2월

서울대학교 대학원

물리천문학부 물리학 전공

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초 록

주요어 : Group III-VI chalcogenide, Indium telluride, 2D material, Field effect transistor

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As promising two-dimensional layered semiconductor materials, many studies have been conducted about graphene, transition metal dichalcogenide materials (TMDc), black phosphorus, indium selenide, gallium selenide and hexagonal boron nitride(hBN). Among them, a study was conducted to confirm the suitability of the device by making a field effect transistor using a group III-VI chalcogenide material on a two-dimensional material using molecular beam epitaxy (MBE). It could be verified that the SEM and TEM were grown in a single crystal, and it could be verified that the manufactured device possessed the performance of a transistor.

Among the two-dimensional materials, chalcogenide related materials are in the spotlight for the use of next generation electronic and optoelectronic devices. Here, I conducted a study on the back-gated field effect transistor device of In_2Te_3 film on hBN

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1. Introduction

1.1 Motivation

Two-dimensional materials received attention, and group III-VI chalcogenide materials also began to receive attention [1,2]. Many studies have been conducted on these materials, which are used in electronic devices and optoelectronic devices as semiconductors. In the case of indium telluride studied in this paper, there are several phases, so much research as a device has not been conducted. [3-7]

Since it is important to understand the characteristics of matter that has grown epitaxially on a two-dimensional material and to make high-quality materials, research was conducted to grow materials and make devices through a molecular beam epitaxy system.

2. Literature review

2.1 Device application of group III-VI chalcogenide

Group III-VI chalcogenide studies using Ga, In, Se, Te, etc. have been conducted. There were memory devices using optoelectronic devices and ferroelectric property. [3,7] In addition, indium telluride has the performance of a photodetector, so it has been conducted as an optoelectronic device study. These compounds have a bandgap ranging from 0.24 to 2.1 eV and can also be used as a device. [3-10]

2.2 Advantages of van der Waals epitaxial growth using Molecular beam epitaxy (MBE)

Unlike other material growth methods, MBE systems have the advantage of being able to grow with high-quality, low-defect, grow, and monitor in-situ crystallinity. If van der Waals epitaxy is used, defect formation due to lattice mismatch, which is a problem in the conventional hetero epitaxy, and uniform thin film cannot be obtained can be minimized. In addition, it is advantageous to obtain a uniform thin film with an accurate thickness because of its slow growth rate. Therefore, research on using this method has an advantage. [11-13]

3. Experimental methods

3.1 MBE system for indium telluride growth

This MBE consists of two chambers, divided into a load lock and a main chamber, and is a modified version of Alpha Plus's UHV thermal evaporator.

The main chamber system consists of four fused cells containing In, Ga, Se and Te. Each cell is connected by a 4.5-inch flange. Gallium (Ga) effusion cell is manufactured by Alpha Plus (STE1400S Ga 20cc). Indium (In), Tellurium (Te) and Selenium (Se) effusion cells are manufactured by Effucel Inc. which is the company of Professor, Cho Seong-Rae of the University of Ulsan. The main chamber is pumped by TMP (Pfeiffer Vacuum Inc. TC353) and backed by Rotary oil pump (KODIVAC Inc. GHP-800K). The gauge uses a convectron gauge (Longmont Inc. 275196) to read rough vacuum, and an ion gauge (Granville Phillips) to read high vacuum. High quality elemental sources are used (99.9999% In, Ga, Se, Te purchased from Thermo Fischer Scientific Inc.). The thickness monitor (SYCON Inc. STM100.) and oscillator (SYCON Inc. OSC-100A) uses and is installed near the substrate holder. In and Te use the power of DB1000B and the PID controller, and the power of Ga and the substrate uses Alpha Plus products, and the PID controllers are Eurotherm 3206 and 3216, respectively. For Se (see product name) power is used and the PID controller is Eurotherm 3216.

In general, atmospheric temperatures are Ga(224°C), Se(100°C), Te (90°C), In(100°C), and the temperatures used for growth are approximately Ga(900°C), Se (144°C), Te (145°C), In(324°C). The substrate holders (HITC Inc.) are made by molybdenum and substrate are glued by liquid phase gallium to allow for adhesion even at high temperature.

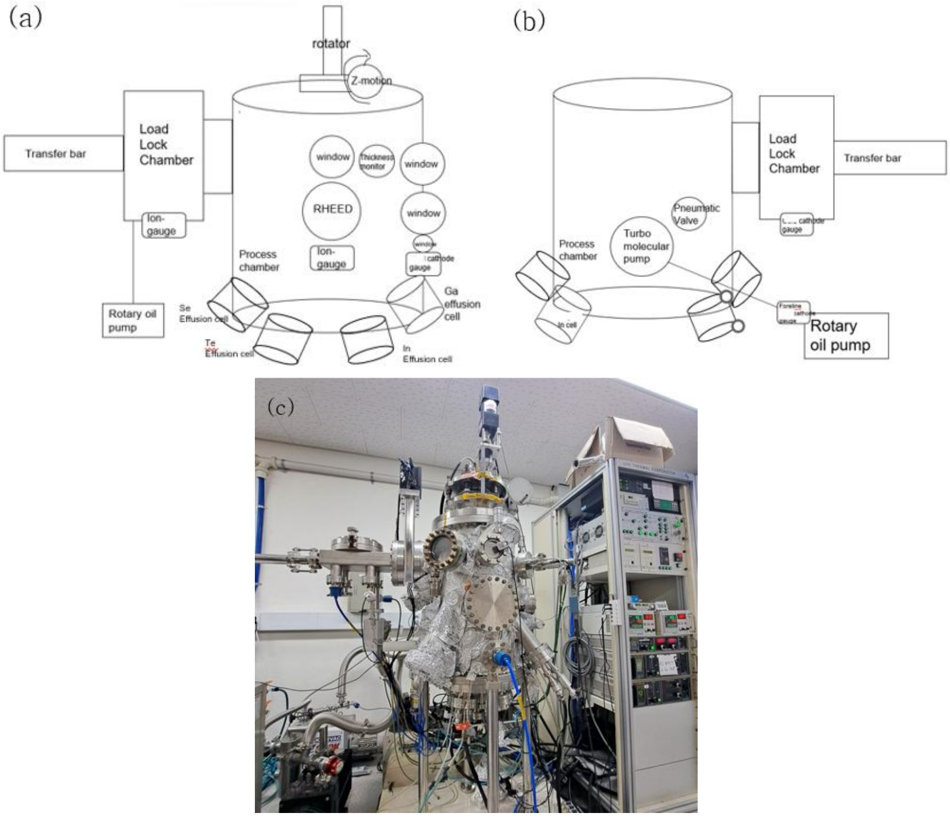

Figure 3.1 (a) Front side schematic of the MBE system for Group III-VI chalcogenide growth, (b) Back side schematic of the MBE system for group III-VI chalcogenide growth (c) Picture of MBE

3.1 Characterization tools

3.1.1 Field emission scanning electron microscopy

Field Emission Scanning Electron Microscopy (SUPRA, AURIGA, SIGMA, MERLIN COMPACT, ZEISS Inc.) was used for checking growth conditions and morphology. FESEM measurement optimized conditions was 2kV high voltage with high current and 4~6mm of working distance.

3.1.2 Raman spectroscopy

Optical properties of indium telluride was measured using Raman spectroscopy system, as descried in figure 3.2 at room temperature. Continuous Diode pumped solid state laser (DPSS) 532nm laser(Samba 50mW, Cobolt Inc.) was used. Rayleigh scattering signal was analyzed with charge couple device (CCD, 100B eXcelon, PIXIS Inc.) which is attached to spectrometer(HRS-300, Princeton Instruments Inc.).

For low frequency Raman shift range measurement, three 532nm notch filters(Opti gate Inc.) was installed in front of spectrometer. And also, pinhole was used for reducing noise. For micro-Raman spectroscopy measurement, 100x objective lens was used. For minimizing the unintentional damages of samples, the power of 532nm laser was used below 300μW.

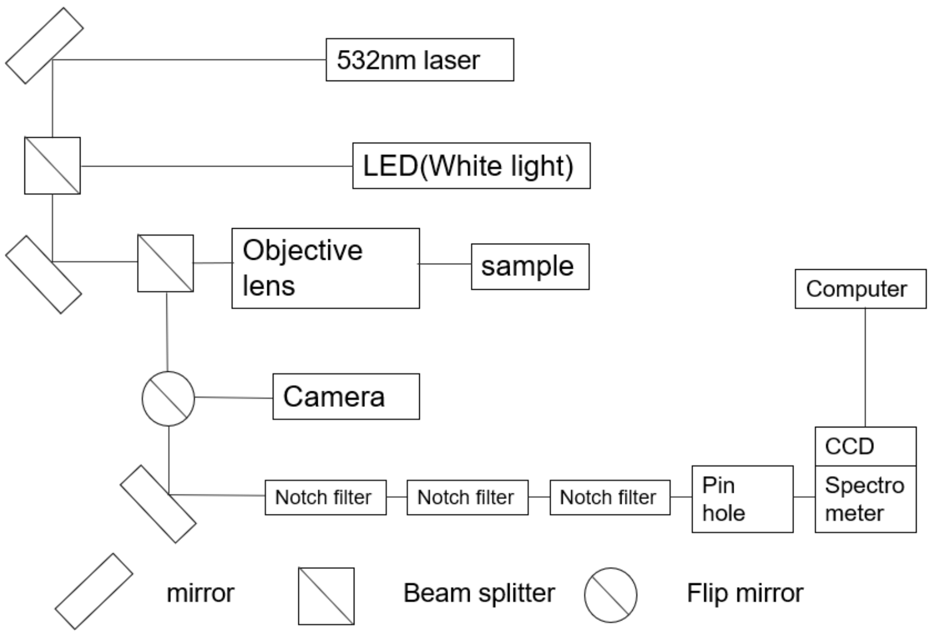

Figure 3.2 Schematic of the Raman spectroscopy

3.1.3 Device fabrication and electrical characterization

Indium telluride film was grown on hBN by mechanical exfoliation on dry Si wafer with 300nm SiO2 thickness layer. A positive photo resist (AZ5214E) was spin-coated at 1000/4000 rpm 10/60s to make an aligner marker and pad thereon. Bake out for 60s to blow off solvent on a 110°C hotplate. After that, patterning was performed at a dose of 100μJ/cm^2 using maskless photolithography (DL-1000A1, Nano System Solutions, Inc.). Photo resist was developed for 60s at room temperature with AZ 300 MIF. 10/30 nm Ti/Au was deposited using an e beam evaporator. After metal deposition, lift-off was carried out in acetone at 50°C. To make contact metal, each layer was spin-coated with PMMA/copolymer bilayer positive e beam resists (PMMA 950K A5 on MMA (8.5)MAA EL9, MicroChem) at 1000/4000 rpm 10/60s. And bake out 60s on a 90°C hotplate. After that, e beam lithography was performed using FESEM (MIRA 3 TESCAN), and the e beam resists were developed at room temperature for 60s with MIBK: IPA 1:3 developer. To deposit 50nm Au, which is a contact metal, it was deposited in an e beam evaporator. It was lifted off in acetone at 50°C. For making bottom gate, I scrapped the lower part of the Si wafer with a diamond pen to remove the SiO2 layer, which would have been unintentionally, and then attaching it to the slide glass with Cupper foil using silver paste (CANS ELCOAT). To measure the electrical characterization of the output curve and transfer curve, Keithley 2400, 2601A source meters and Keithley 4200 SCS semiconductor parameter analyzer were used.

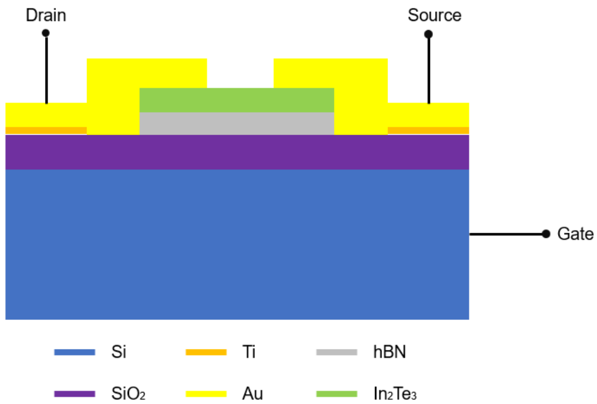

Figure 3.3 Schematic of the back-gated In_2Te_3 FET

Table 3.1 Typical process conditions for the fabrication of the back-gated In_2Te FET

Fabrication steps	Process conditions
1.1 Spin coating of photoresist	AZ 5214E Spin: 1000/4000rpm 10/60s, Baked at 110°C for 60s
1.2 Photo lithography of alignment markers and pad	Dose 100mJ/cm^2
1.3 Development	AZ MIF300 for 60~62s, at room temperature
2.1 Alignment marker Metallization	e-beam evaporator Ti/Au 10/30nm
2.2 Lift- off	in 50°C acetone bath
3.1 Spin coating of e-beam resist	Bottom layer: MMA (8.5) MAA EL9 Spin: 1000/4000rpm 10/60s, Baked at 90°C for 60s Top layer: PMMA 950K A5 Spin 1000/4000rpm 10/60s, Baked at 90°C for 60s
3.2 e-beam lithography of direct Contacts and interconnect line between Direct contacts and pads	Direct contacts: H.V 30kV, Current 20pA Magnification: x800, Step size: 3.81nm Dose: 425μC/cm^2 Interconnect line: H.V 30kV, Current 17nA Magnification: 800, Step size: 3.81nm Dose: 425μC/cm^2
3.3 Development	MIBK/IPA 1:3 for 60~62s, at room

	temperature
4,1 contact metallization	e-beam evaporator Au 50nm
4.2 Lift-off	in 50°C acetone bath

4. Indium telluride growth study

4.1 Growth method and substrate preparation

To peel off and stamp more hBN and grapheme flakes on Si wafer, O_2 plasma ashing process was treated on Si wafer for 5 minutes and then exfoliation was conducted. To withstand high temperature, a holder made of molybdenum was used as the substrate holder. To fix the sample to the molybdenum holder, using gallium that did not generate vapor and had adhesion characteristics even at high temperature.

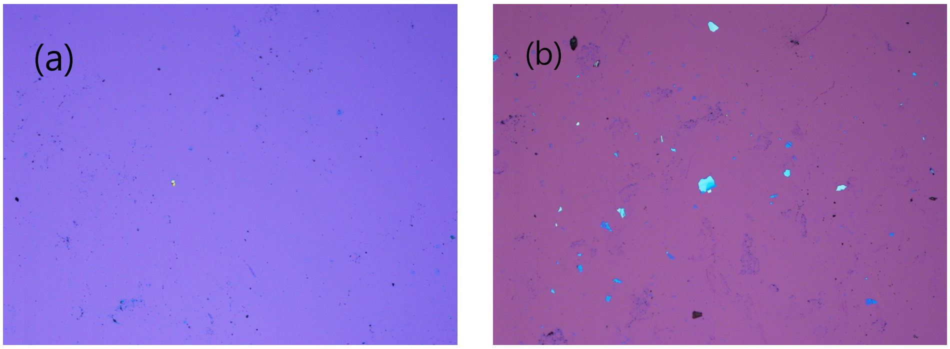

Figure 4.1 (a) PDMS stamp method without O_2 ashing (b) with O_2 ashing

4.2 Effect of growth temperature and time

4.2.1 Single-step growth on graphene layers

The growth temperature and time are the significant effects for epitaxial growth. To confirm the effects of growth temperature and time for indium telluride epitaxial growth, growth temperature and time were studied. In terms of the growth temperature, as the growth temperature increase based on the same time, the thickness of the indium telluride growing on the graphene layer tends to decrease. While the facet of the triangle is observed dominantly at low temperatures, curved nanostructures begin to be found as the temperature rose.

In terms of growth time, the thickness is observed to grow over time, especially at 520℃, when the growth time is short, a pyramid-shaped nanostructure is observed, but as time increase, a curved nanostructure is observed.

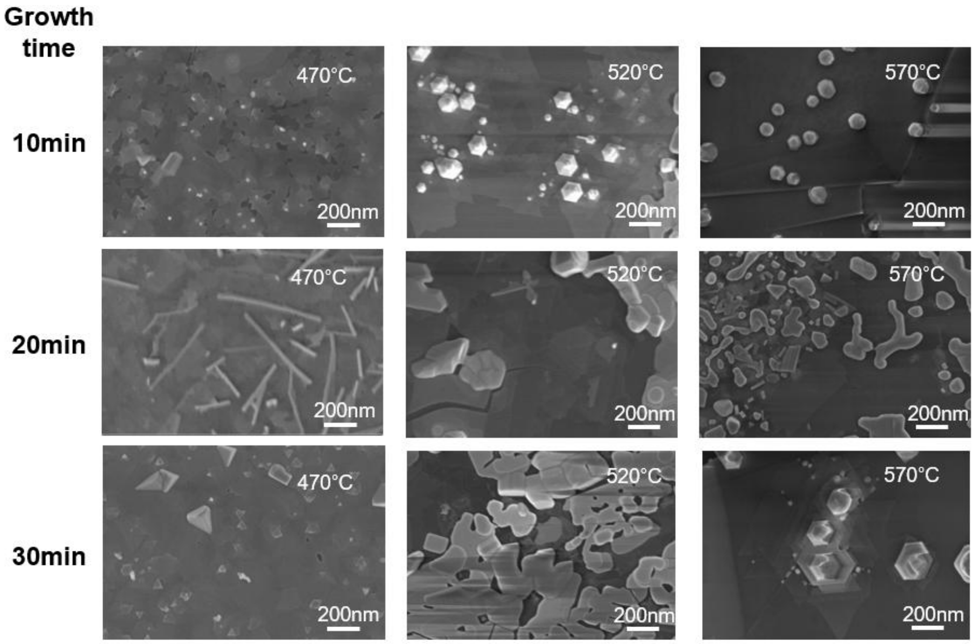

Figure 4.2 FE-SEM images of indium telluride grown on graphene layers under different growth temperatures and time

4.2.2 Single-step growth on CVD graphene

In CVD graphene, indium telluride grows on graphene when the temperature is low, and it can be observed that triangular facets and curved nanostructures are mixed, and curved nanostructures become dominated as the growth time increases. It is possible to observe nanostructure in which pyramid and circular structure are mixed on graphene when the growth temperature is high and the growth time is short, and the thickness of indium telluride deposited on graphene increases as time increases. It was confirmed that a square nanostructure occurred when grown at 570°C for 30 minutes.

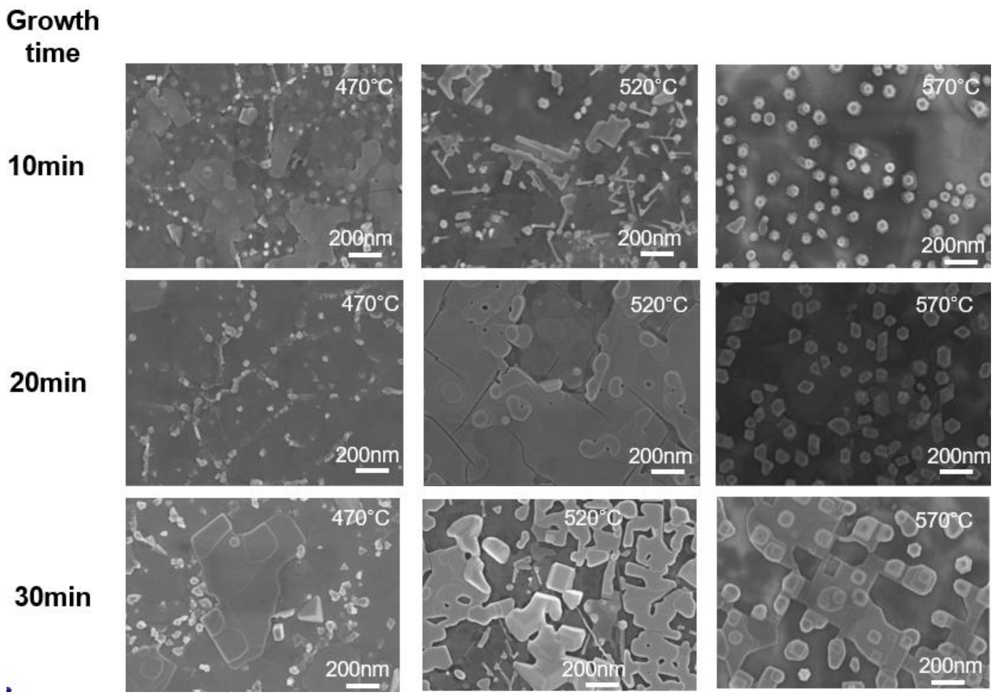

Figure 4.3 FE-SEM images of indium telluride grown on chemical vapor deposition (CVD) graphene under different growth temperatures and time

4.2.3 Single-step growth on hBN layers

When indium telluride was grown on hBN layers, indium telluride did not grow at high temperature, and indium telluride was found to grow at 470°C and 520°C. In this case, unlike when grown on the graphene layer, there was no curved or pyramid-like nanostructures, and it was confirmed that the triangular facet and needle-shaped nanostructures appeared.

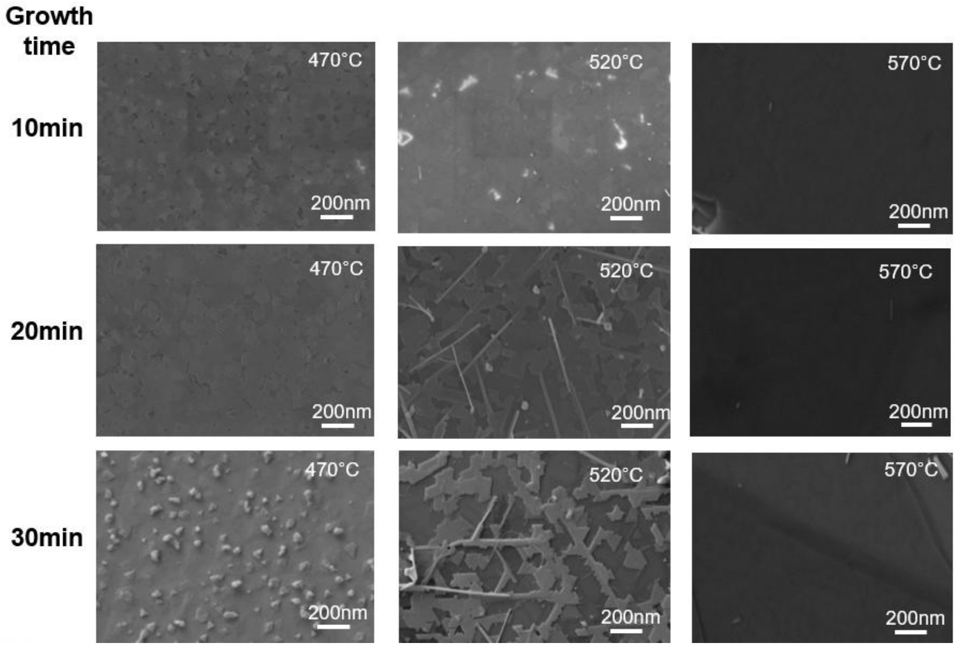

Figure 4.4 FE-SEM images of indium telluride grown on hBN layers under different growth temperatures and time

4.2.4 Single-step growth on c-Al_2O_3

When c-Al_2O_3 was used as a substrate, a ball-like nanostructure was observed at 470°C and 520°C, and a needle-shaped nanostructure was observed at 570°C. It was confirmed that the size of the ball-like nanostructure increased as time increased. It increased from a diameter of 50 nm to 100 nm.

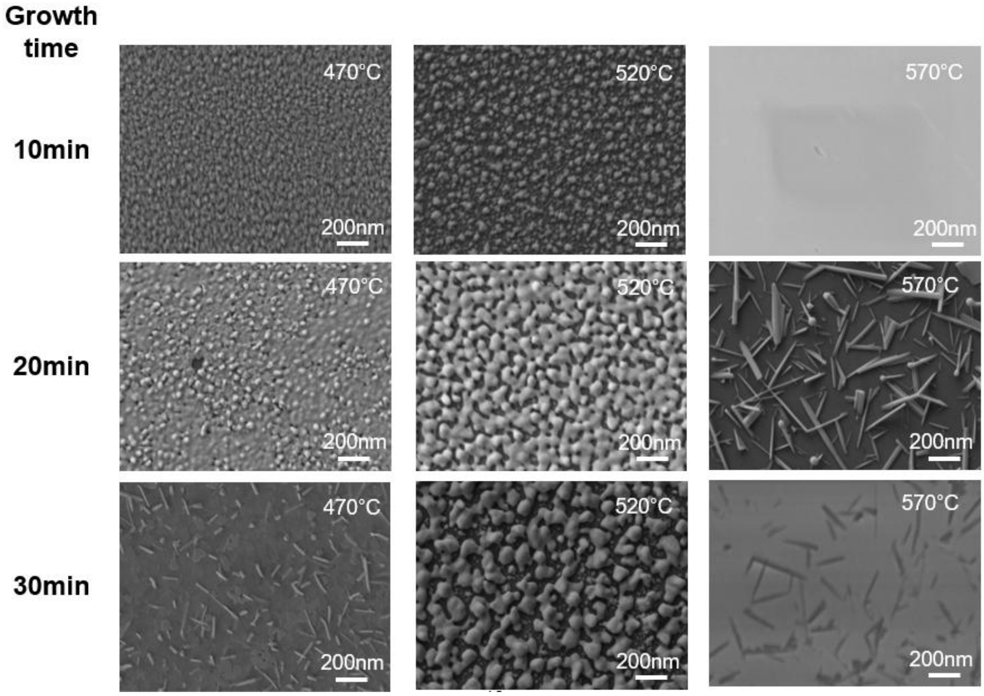

Figure 4.5 FE-SEM images of indium telluride grown on c-Al_2O_3(0001) under different growth temperatures and time

4.2.5 two-step growth on hBN layers

For avoiding valleys, voids or 3D structures on indium telluride surface, two-step growth was conducted. Nucleation is deposited at low temperature and anneal at high temperature for recrystallization. In addition, additional growth was performed at high temperature. Figure 4.7 (b) shows the atomically smooth terraces over a large area.

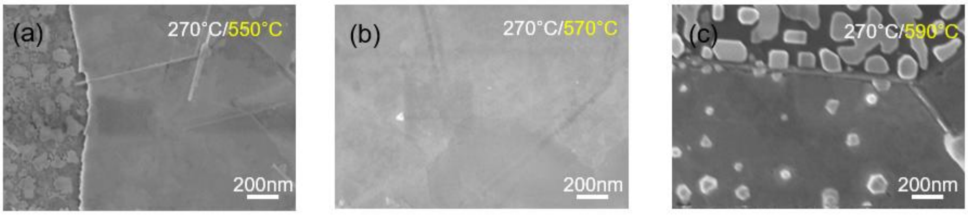

Figure 4.6 FE-SEM images of indium telluride grown on hBN layers under different second growth temperatures -

4.3 Raman spectrum· of indium telluride on hBN layers

Figure 4.7 (a) shows the Raman shift positions from indium telluride single-step grown at 470°C about 104, 125, and 141 cm^{-1} are consistent with the Raman peaks of In_2Te_3. [14] Figure 4.7 (b) shows the Raman spectrums from indium telluride single-step grown 520°C. The peaks about 46cm^{-1} and 137 cm^{-1} are related to E_g photon mode of InTe. The peak at 126cm^{-1} is from Te-Te vibrational E mode. 86cm^{-1} peak can be assigned as $B_1{}^g$ symmetry of InTe. These Raman shift positions are relative to the Raman peaks of InTe. Figure 4.7 (c) shows the Raman peaks highly relative to the Raman peaks In_2Te_3. [15-17].

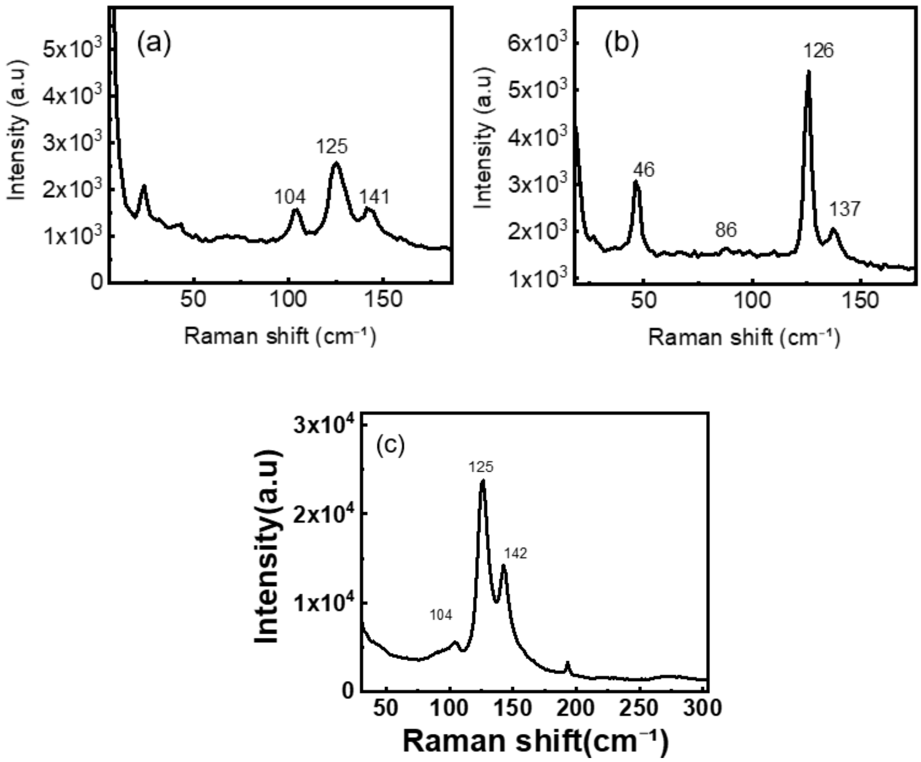

Figure 4.7 (a) Raman spectrums of single step grown In_2Te_3 at 470°C (b) Raman spectrums of single step grown InTe at 520°C (c) Raman spectrums of two-step grown In_2Te_3 at 270/570°C

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5. Electronic device application: the back-gated field effect transistor using In_2Te_3 on hexagonal boron nitride(hBN) layers

5.1 Fabrication of the back-gated In_2Te_3 FET in hBN layers

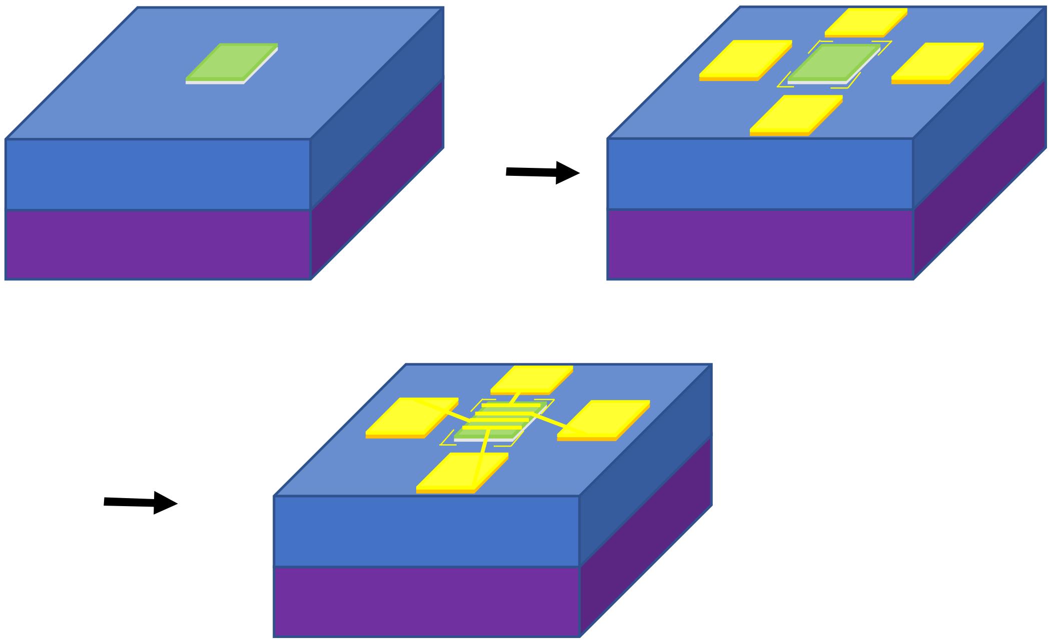

Figure 5.1 Device fabrication process of the back-gated In_2Te_3 FET

To make the alignment marker and gold pad faster, photolysis is performed after sample growth, and Ti/Au is deposited using e beam evaporator. After that, e-beam lithography is performed on indium telluride grown on hBN and gold is deposited for making contact.

5.2 Electrical characteristics of the back-gated In_2Te_3 FET

Figure 4. In_2Te_3 FET. a) Schematic illustration of the structure of the In_2Te_3 FET. Electrical characteristics of the TFT, b) output, c) transfer, d) gate leakage current curves. Figure 4a shows the schematic of the back-gated In_2Te_3 FET with bottom gate. Since hBN is an insulator, it was used as a substrate. The fabrication was performed on SiO_2 layer on a dry p-Si carrier wafer which has lower defects than wet Si wafer for reducing the possibilities of gate leakage. Si wafer was used for the bottom gate and SiO2 layers served as the bottom dielectric oxide layers. The InTe channel was grown by molecular beam epitaxy (MBE) using two step growth method at the temperature of 270 °C (1st step for making seed) and 570 °C (2nd step for epitaxial growth). The 50nm Au was used as an interface contact material to the In_2Te_3. TC/Au leads and pads were connected to the source and drain for ease of electrical access. The channel width/length were 20 μm/10 μm.

$$\mu_{FE} = \left(\frac{L}{W * C_i * V_{sd}}\right)\left(\frac{dI_{sd}}{dV_{sd}}\right) (L : Channel\ Length, W : Channel\ Width, C_i : Capacitance\ per\ unit\ area)$$

The μ_{FE} is ~ 4.7 cm /V*s. I measured the output curve and transfer curve for checking characteristics of the MOSFET with bottom gate. Figure 4b shows the output curves of the MOSFET device, measured by sweeping the drain bias from -2 to 2 V for the gate biases in the range of -50 to 0 V at steps of 10 V with respect to the source. The current increase at small drain bias and channel pinch-off at high drain bias represent typical p-type semiconductor behavior of the channel. Figure 4c shows the transfer curve measured by sweeping the gate bias from -50V to 50V at a fixed drain bias. The on/off ratio of the device is I_{max}/I_{min} ratio ~ 10^3. Figure 4d shows the gate leakage current was in the order of a 1nA or smaller.

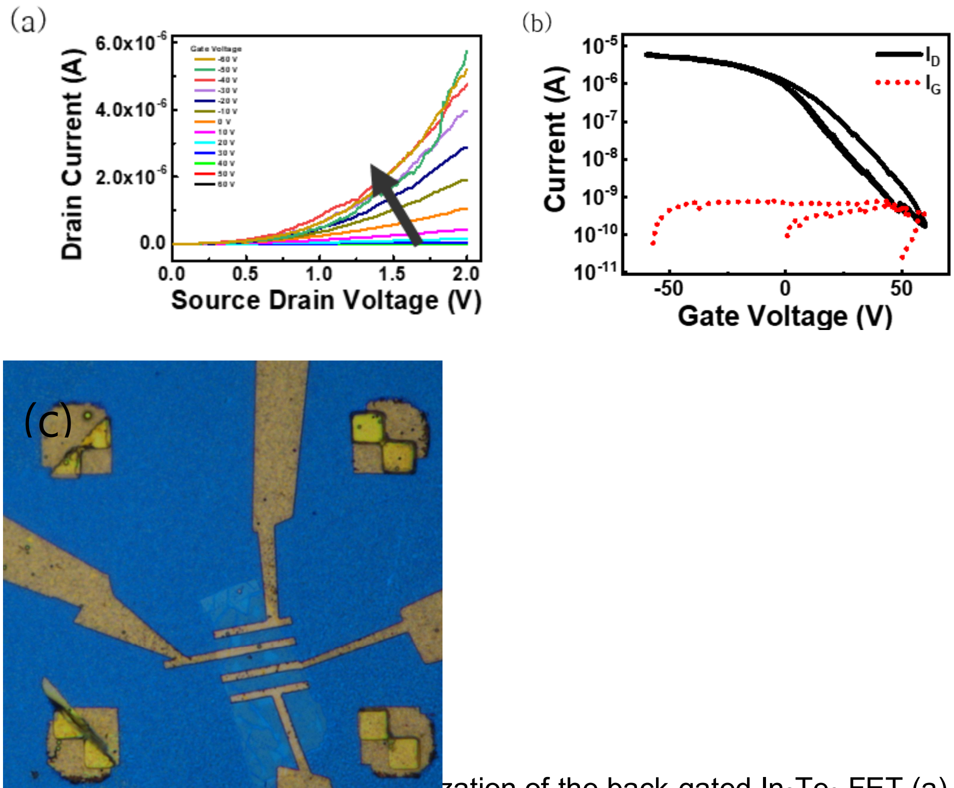

Figure 3.2 Electrical characterization of the back-gated In_2Te_3 FET (a) output curve (b) transfer curve (c) Optical microscopy image of the back-gated In_2Te_3 FET

6. Conclusion

6.1 Summary

In this paper, indium telluride was grown by changing various growth parameters using the MBE system, and particularly, optical and electrical characteristics were analyzed. The grown indium telluride was confirmed using SEM and Raman spectroscopy. It was confirmed that indium telluride of different phases grew according to temperature. InTe was grown when the temperature was high, and In_2Te_3 when the temperature was low.

In the above study, it was confirmed that the temperature growing was different depending on the substrate, and that it did not grow when it exceeded a specific temperature. It was confirmed that indium telluride of different phases grew according to the growth time even at the same temperature. Based on this, a transistor was made using In_2Te_3 grown on hBN, a two-dimensional material, and it was confirmed that it was a p-channel device, and it was observed that it could use an electrical device with transistor performance. Further research may include the strain of the 2D material electrical device designed in this paper, the change of device characteristics according to temperature change, etc.

Summary in Korean

본 논문에서는 MBE system을 활용하여 다양한 성장 파라미터를 바꿔 인듐 텔루라이드를 성장하였으며, 특히 광학적, 전기적 특성을 분석하였다. 성장된 인듐 텔루라이드는 SEM과 라만 분광을 사용하여 확인하였다. 온도에 따라 다른 상의 인듐 텔루라이드가 자라는 것을 확인하였다. 온도가 높은 경우 InTe가 성장되었으며, 온도가 낮은 경우 In_2Te_3로 성장되었다.

위 연구에서 기판에 따라 성장되는 온도가 달랐으며, 특정 온도를 넘어가면 성장되지 않는 것을 확인하였다. 같은 온도 더라도 성장시간에 따라 다른 상의 인듐 텔루라이드가 성장하는 것을 확인을 하였다. 이를 바탕으로 2차원 물질인 hBN 위에서 성장된 In_2Te_3를 이용하여 트랜지스터를 만들었으며, p 채널 소자임을 확인하였으며, 트랜지스터 성능을 가지고 있어 전기적 디바이스를 활용 가능한 것을 관측하였다. 추가적인 연구는 본 논문에서 고안된 2차원 물질 전기적 디바이스의 strain, 온도 변화에 따른 디바이스 특성 변화 등을 포함할 수 있다.

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