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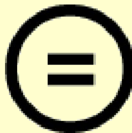

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Ph.D. Dissertation of Materials Science and Engineering

Reconfigurable and Electrostatically Controllable van der Waals Devices for Multifunctional Electronic Applications

다기능 전자 소자 응용을 위한 재구성과 정전기적 조절 가능한 반데르발스 소자

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Graduate School of Seoul National University
Department of Materials Science and Engineering

June-Chul Shin

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Prof. Gwan-Hyoung Lee

Submitting a Ph.D. Dissertation of Engineering

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Graduate School of Engineering
Seoul National University
Department of Materials Science and Engineering

June-Chul Shin

Confirming the Ph.D. Dissertation written by
June-Chul Shin
July 2023

Chair	SangBum Kim	(Seal)
Vice Chair	Chul-Ho Lee	(Seal)
Examiner	Gwan-Hyoung Lee	(Seal)
Examiner	Jihyun Kim	(Seal)
Examiner	Jangyup Son	(Seal)

Abstract

Reconfigurable and electrostatically controllable van der Waals devices for multifunctional electronic applications

June-Chul Shin
Materials Science and Engineering
The Graduate School
Seoul National University

The limitations in scaling silicon semiconductors have prompted the exploration of new channel materials, and two-dimensional (2D) materials with atomic-scale thickness have emerged as the most promising candidates. 2D material such as graphene and transition metal dichalcogenides (TMDs) has unique physical, electrical, and optical properties. Combining these materials in van der Waals heterostructures opens new possibilities in the field of electronics. 2D materials offer advantages such as ultra-flat surfaces, high charge carrier mobility, and immunity to short-channel effects. However, the research on 2D material-based electronic devices is still in the early stages and has focused on emulating conventional silicon-based device technologies. Therefore, it is necessary to leverage the inherent characteristics of 2D materials and explore innovative approaches to improve significant

performance in devices.

One interesting characteristic of 2D materials as electronic devices is the confinement of all carriers within the atomic layer thickness, allowing effective control of the Fermi energy level by external electric fields. This enables efficient modulation of carrier polarity within the channel through electrical gating, without the additional doping techniques. Therefore, research on new device concepts that utilize these unique properties of 2D materials should be prioritized.

This thesis focuses on multifunctional van der Waals electronic devices based on 2D materials, which exhibit effective electrostatic controllability and efficient polarity modulation. Before introducing the detailed research findings, Chapter 1 provides background information on 2D materials and 2D material-based electronic devices. It highlights key attributes of 2D materials, including van der Waals heterostructures, effective electrostatic controllability, and efficient polarity modulation. Moreover, the research objectives are introduced, aiming to leverage these properties of 2D materials for further investigations.

Chapter 2 introduces high-efficiency light-emitting devices based on 2D materials using effective electrostatic controllability to achieve efficient charge injection into the emission region. Due to their direct bandgap and excellent optical properties, 2D semiconductors like TMDs are promising candidates for optoelectronic devices. However, previous reports on 2D-based light-emitting devices utilizing have mainly focused on functions based on the exotic properties of 2D materials, resulting in low external quantum efficiency (EQE). To order to address this issue, a highly efficient WSe_2 light-emitting transistor (LET) based on van der Waals heterostructure is

introduced. By utilizing a van der Waals contact electrode made of graphene, which suppresses the Fermi-level pinning effect, the LET effectively confines neutral excitons in the one-dimensional (1D) intrinsic region of WSe_2. The ambipolar channel of WSe_2 allows for the efficient injection of electrons and holes into the emitting layer of WSe_2 through electrostatic modulation. Moreover, the double gate structure enables localized doping of the WSe_2 channel and efficient injection of electrons and holes into the 1D region simultaneously. By achieving a balance in the injection density of electrons and holes, the WSe_2 LET electrically localizes neutral excitons in the one-dimensional region and emits charged excitons from the doped region. As a result, the LET demonstrates strong electroluminescence with a high EQE of about 8.2%. This research highlights the significant potential of 2D light-emitting devices and proposes a method to modulate the recombination of neutral and charged excitons in excitonic devices.

Chapter 3 presents research on reconfigurable memory devices based on 2D materials for logic-in-memory applications using efficient polarity modulation. Logic-in-memory has been considered a promising electronic approach for efficient data processing, and the enhancement of processor performance through high integration is essential. 2D semiconductors have shown great potential for implementations of highly integrated logic-in-memory due to their high carrier mobility, absence of short channel effect, and effective electrostatic controllability. This article demonstrates reconfigurable and cascadable two-dimensional floating-gate field-effect transistors (FG-FET) for highly integrated logic-in-memory applications. By modulating the trapped charges in the floating gate using only a single gate, the device achieves reconfigurable transport behaviors with all types of

electrical conduction (n- and p-type, metallic, and insulating) and threshold voltage control. Logic circuits composed of WSe_2 FG-FETs can perform all 16 Boolean logic functions within a single configuration while optimizing energy consumption by selectively activating the required components for the programmed function. In addition, I integrated a reconfigurable microprocessor capable of performing 1-bit full adders, subtractors, and comparators using cascade which enables the design of complex circuits. The device can significantly enhance circuit design flexibility and device functionality through reconfiguration and cascade, offering area and energy-efficient solutions for logic synthesis. This work highlights the great potential of memory as an efficient next-generation electronic component in the processing in-memory field.

Lastly, Chapter 4 reports on research regarding contact engineering, which is a crucial issue in 2D materials. Due to the high sensitivity of 2D materials to external conditions, passivating the 2D material is essential to maintain the stability of 2D electronic devices. However, forming suitable contacts for passivated 2D devices is challenging due to the surrounding passivation layer around the 2D channel. This study proposes a new approach to forming irreversible conductive filaments (ICF) contacts in the hexagonal boron nitride (hBN)-passivated 2D channel. Oxygen plasma intentionally creates defect paths in the upper hBN layer of hBN-passivated graphene (or MoS_2). Subsequently, repetitive bias forms ICFs in the 2D channel layer along the defect paths. The ICF contacts, composed of a combination of migrated metal atoms and vacancies along the defect paths, are maintained stably during device operation and are not reversible, unlike the filaments in hBN memristors. Field-effect transistors (FETs) with ICF contacts exhibited low contact resistance

and high stability. My research demonstrates a new contact approach with significant potential for high-performance 2D electronic devices.

Keywords: polarity modulation, electrostatic controllability, multi-functional van der Waals device, two-dimensional materials

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Chapter 1. Introduction

Chapter 1 serves as an introduction to the research, offering essential background information on the topic. It presents a comprehensive overview of two-dimensional (2D) materials, with a specific focus on transition metal dichalcogenides (TMDs) that primarily exhibit semiconductor properties. Furthermore, it explores the key factors contributing to two-dimensional materials' importance in semiconductor devices. This chapter also explains the research purpose, establishing the necessary foundation for subsequent chapters.

1.1 Introduction of 2D Materials

1.1.1 Atomic Structure of 2D Materials

Since the discovery of graphene, extensive research has been conducted on 2D materials, which possess a layered structure that distinguishes them from bulk materials[1]. As shown in Figure 1a, intralayer atoms in 2D materials have strong covalent bonds between layers, while interlayers are formed by weak van der Waals interaction between layers, allowing for easy separation and precise control of atomic-level thickness[2]. 2D materials can be composed of various combinations of elements. In addition to those consisting of a single element like graphene, they can also exist in different forms such as binary and ternary compounds, exhibiting diverse atomic structures depending on the material[3,4] (See Figure 1b, c).

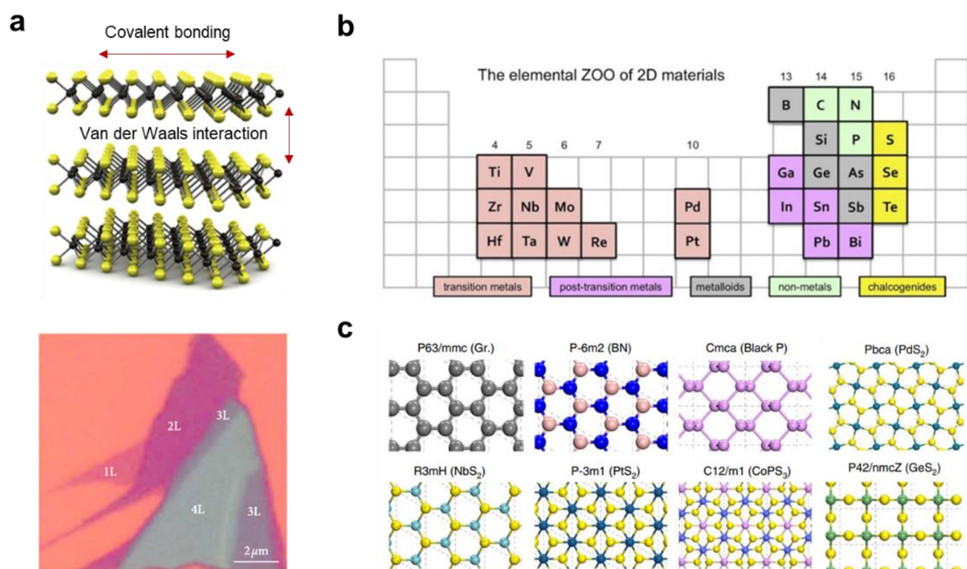


Figure 1. Structure of 2D materials. **a** Schematic of the atomic structure on MoS_2 of representative TMDs, and optical image of thickness-dependence on MoS_2. **b** Periodic table highlighting the elements, which form the most common layered and 2D materials. **c** Various space groups and typical structural configurations (top views) of the 2D materials. Figures adapted from refs [2-4].

1.1.2 Electronic Properties of 2D Materials

2D materials exhibit a variety of band structures depending on their chemical composition and crystal structure. These band structures give rise to a wide range of electrical properties such as superconductivity, metal, semiconductor, and insulator, and optical bandgaps spectrum ranges from infrared to ultraviolet, as shown in Figures 2a, b[5,6]. Recently, exotic 2D materials with magnetic, ferroelectric, piezoelectric, and other unique properties have also been reported. Furthermore, 2D materials exhibit a layer-dependent band structure when they have different thicknesses[7]. A prominent example is TMDs, which are 2D semiconductors. In Figure 2c, monolayer TMDs possess a direct band gap, while multilayer TMDs exhibit an indirect band gap[8]. Therefore, these materials demonstrate distinct electron structures and optical properties distinct from conventional bulk materials, allowing their significant potential in the field of optoelectronics.

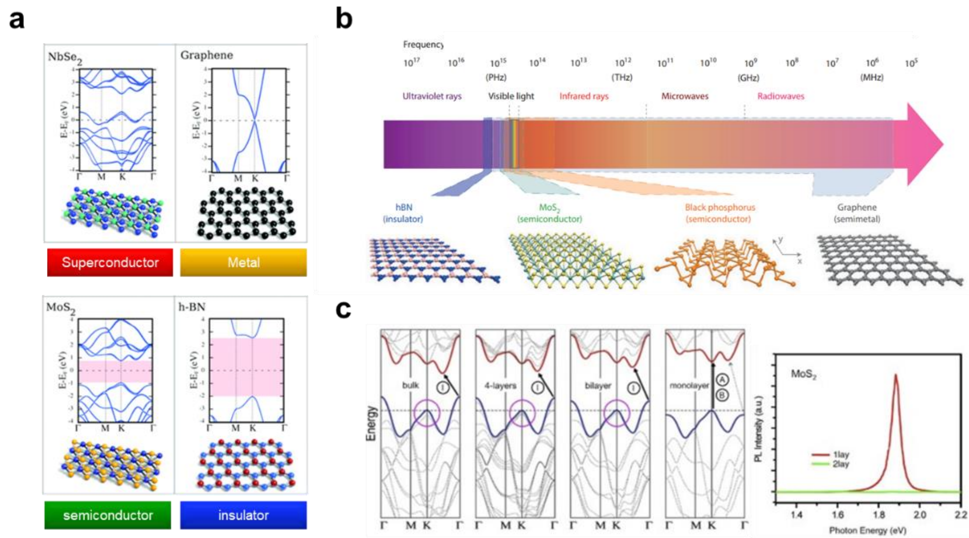


Figure 2. Electronic Properties of 2D Materials. a Crystalline lattice and band structures of different 2D materials. **b** Electromagnetic spectrum of various 2D materials. **c** Thickness-dependent bandgap properties and PL spectra for mono- and bilayer MoS_2. Figures adapted from ref [5-8].

1.2 Introduction of Transition Metal Dichalcogenides

1.2.1 Transition Metal Dichalcogenides (TMDs)

Semiconductor properties are of utmost importance in the field of electronics. In this regard, I aim to focus on and introduce a group of 2D materials known as transition metal dichalcogenides (TMDs) that exhibit semiconductor properties[9]. TMDs typically have the chemical formula MX_2, where transition metal atoms (M) are sandwiched between chalcogen atoms (X). By combining various transition metal atoms (M: Ti, Zr, Hf, V, Nb, Ta, Re, etc.) with chalcogen atoms (X: S, Se, Te), more than 30 different compounds are formed, including MoS_2 and WSe_2. While most of these compounds exhibit semiconductor properties, they can also manifest various properties such as semi-metallic, metallic, and superconducting properties depending on their crystal structure. Monolayer TMDs exhibit four different polymorphs: 1H phase (space group $P\bar{6}m2$), 1T phase (space group $P\bar{3}m2$), 1T' phase (space group $P2_1/m$), and $1T_d$ phase (space group $P1m1$). When TMDs are stacked, they can form three structural polymorphs: 2H structure (hexagonal symmetry, two layers per unit cell, triangular lattice coordination), 3R structure (hexagonal cubic symmetry, three layers per unit cell, triangular lattice coordination), and 1T structure (square symmetry, one layer per unit cell, octahedral lattice coordination). Most TMDs (e.g., WS_2, $MoTe_2$) are stable in the 2H structure and exhibit semiconductor properties, while some TMDs like WTe_2 are stable in the 1T structure and exhibit metallic properties at room temperature. These diverse crystal structures and properties make TMDs highly promising materials in the field of electronics and optics. Additionally, unlike graphene, TMDs can be synthesized on insulating substrates on a large scale, which has sparked strong research and

development interest in TMDs[10].

1.2.2 Electrical Properties of TMDs

Field-Effect Transistor (FET) is the most critical electronic component in the semiconductor market, capable of controlling the flow of electrons using an external voltage. To achieve high-performance computing processors, increasing the number of transistors within an electronic circuit is essential. Therefore, scaling down the size of transistors becomes necessary. However, the scaling of silicon-based transistors, which are widely used in the industry, has reached the sub-3-nm technology node, and further reduction is constrained by physical limitations. The thickness of silicon plays a pivotal role in reducing its size. The switching behavior of typical thin film-based single-gate FETs is described by a one-dimensional Poisson equation[11].

$$\frac{d^2\varphi(x)}{dx^2} - \frac{\varphi(x)}{\lambda} = 0 \ \ with\ \lambda = \sqrt{\frac{t_b t_{ox} \varepsilon_b}{\varepsilon_{ox}}}$$

λ represents the length at which the electric field generated at the drain penetrates the channel, and it is a parameter that determines the transistor size. When considering only the channel, decreasing the thickness of the dielectric constant can decrease the transistor size. However, reducing the silicon thickness to below 10 nm leads to performance degradation, specifically mobility, due to interface roughness scattering caused by dangling bonds and surface roughness of silicon. Therefore, further size reduction for the device is practically challenging[12].

However, 2D semiconductors such as TMDs exhibit exceptional properties that make them attractive for electronic applications. TMDs maintain high carrier mobility despite their atomic-scale thickness and exhibit a smooth surface without dangling bonds. Moreover, MoS_2, a representative material of TMDs, has a low in-plane dielectric constant of about 4[13]. This characteristic allows for further reduction in transistor size according to the Poisson equation. Additionally, 2D materials have a larger effective mass and bandgap than silicon. These attributes effectively suppress direct tunneling between the source and drain in a single-channel device, leading to a notable reduction in leakage current. Consequently, 2D materials exhibit excellent immunity to the short-channel effect Computational studies have confirmed the superior immunity of two-dimensional materials compared to silicon in terms of subthreshold swing and leakage current[14]. Recent experiments have also provided evidence of the short-channel effect immunity in FETs based on TMD channels with a channel length of 9 nm. Recently, experiments have also demonstrated the immunity to the short-channel effect in TMD channel-based FETs with a channel length of 9 nm[15]. Therefore, in recent semiconductor trends, since silicon has reached its limits for scaling below sub-2 nm, 2D can be considered one of the most suitable candidates for extending Moore's Law.

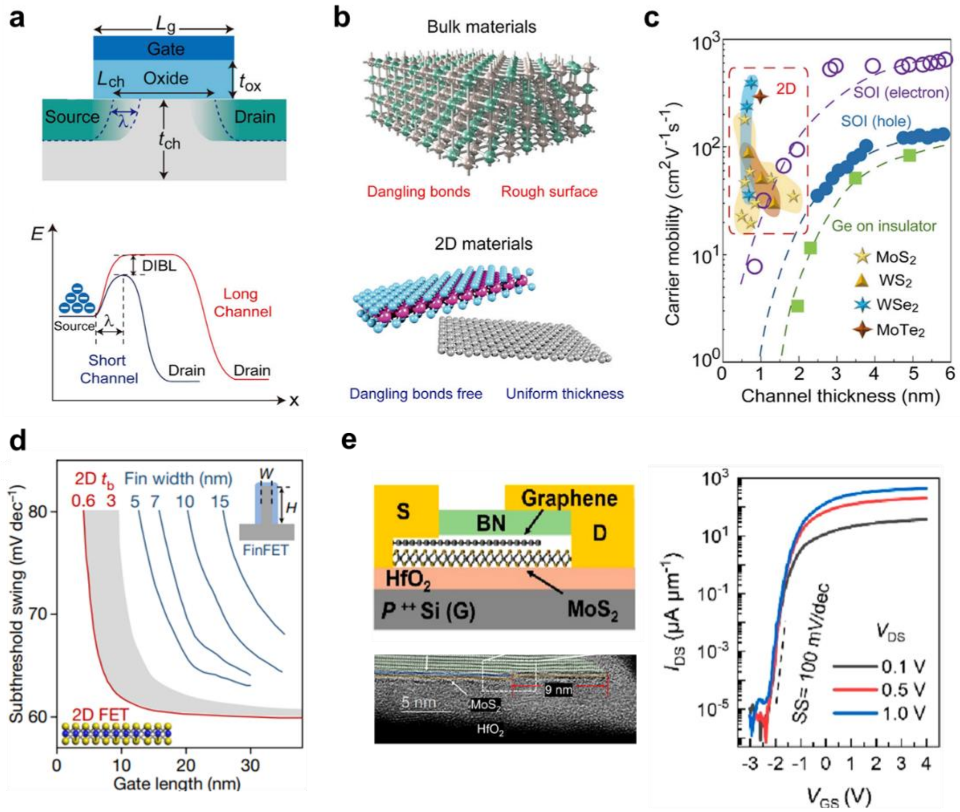


Figure 3. Electrical properties of TMDs. a Schematic of the device structure and energy band diagram of the Si transistor in long and short channel configurations at the extreme scale. **b** Crystalline structure of typical 3D bulk materials and typical 2D TMD and graphene with obvious dangling bonds on the rough surface. **c** Carrier mobility as a function of channel thickness for both 3D Si. **d** Subthreshold swing versus gate length for transistors with different fin widths (blue lines) or 2D body thickness (red line and grey shaded area) **e** Device structure, cross-section scanning transmission electron microscope image and transfer characteristic curve of sub-10 nm channel length MoS_2 FETs. Figures adapted from refs [12,14,15].

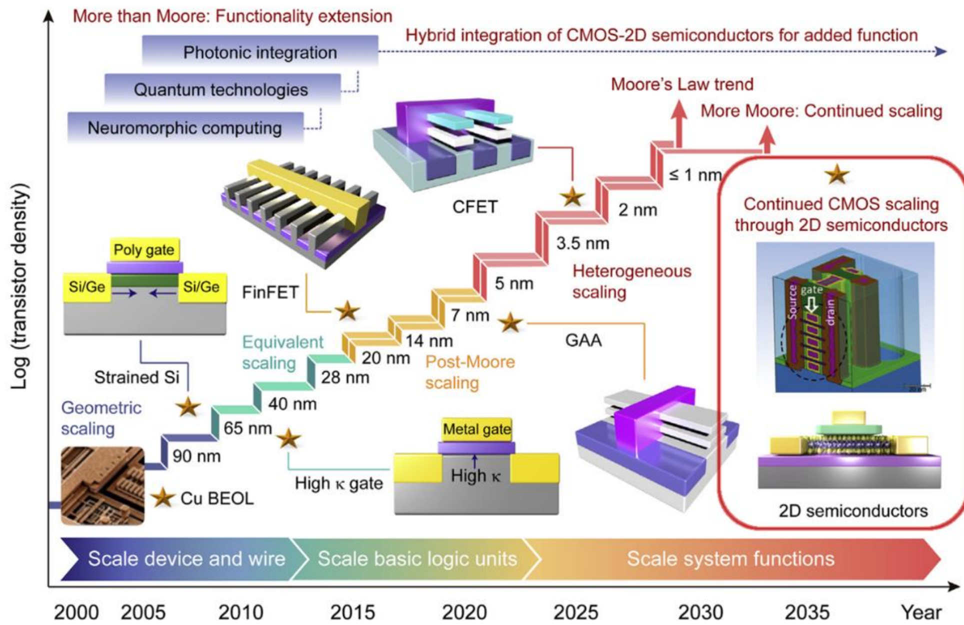


Figure 1. The evolution trend of the technology nodes for Si transistors. Figure adapted from ref [12].

1.3 Key Factors of 2D Materials for Multi-functional Electronic Applications

1.3.1 van der Waals (vdWs) Heterostructure

Heterostructures, which are structures composed of different materials in proximity, serve as the fundamental building blocks in the electronic and optoelectronic fields. The seamless integration of heterogeneous materials is essential for designing functional devices. However, when growing bulk materials using chemical epitaxy techniques such as molecular beam epitaxy (MBE) and metal-organic chemical vapor deposition (MOCVD), the chemical bonding between the two materials is formed by dangling bonds on the surface, requiring the crystal structures and lattice constants of the two heterogeneous materials to be similar. Moreover, there are limitations to achieving comparable processing conditions for both materials. Therefore, fabricating heterostructures with significantly different lattice structures or processing conditions can result in numerous defects and deformations at the interface, posing obstacles to epitaxial growth and compromising the unique properties of each material.

In contrast, van der Waals (vdWs) heterostructures offer a different approach. These heterostructures involve stacking different 2D materials together, similar to building blocks. Unlike bulk materials, 2D materials have no dangling bonds on their surfaces, and there exists a vdWs gap between the layers due to vdWs interactions. This unique characteristic means that there are no direct chemical bonds between heterogeneous materials, alleviating constraints on the similarity of lattice structures or crystal structures between the heterogeneous materials, as well as the synthesis conditions. Consequently, vdWs integration emerges as a highly valuable technique for

seamlessly integrating diverse 2D atomic crystals, even if they possess vastly different lattice structures[16].

Recently, there have been notable advancements in the research of vdW heterostructures involving combinations of 2D/2D materials and different dimensions, such as 1D/1D, 0D/2D, 1D/2D, 2D/2D, 2D/3D, and 3D/3D. These studies have explored the integration of materials with distinct properties into various structures, leveraging the freedom of combining these materials combinations. As a result, research on electronic devices based on vdWs heterostructures and various optoelectronic devices has been reported. The integration of diverse materials within vdWs heterostructures enables the fabrication of novel concepts and high-performance electronic devices. This unique and low-energy approach serves as a valuable solution to overcome the limitations of traditional methods for material integration[17].

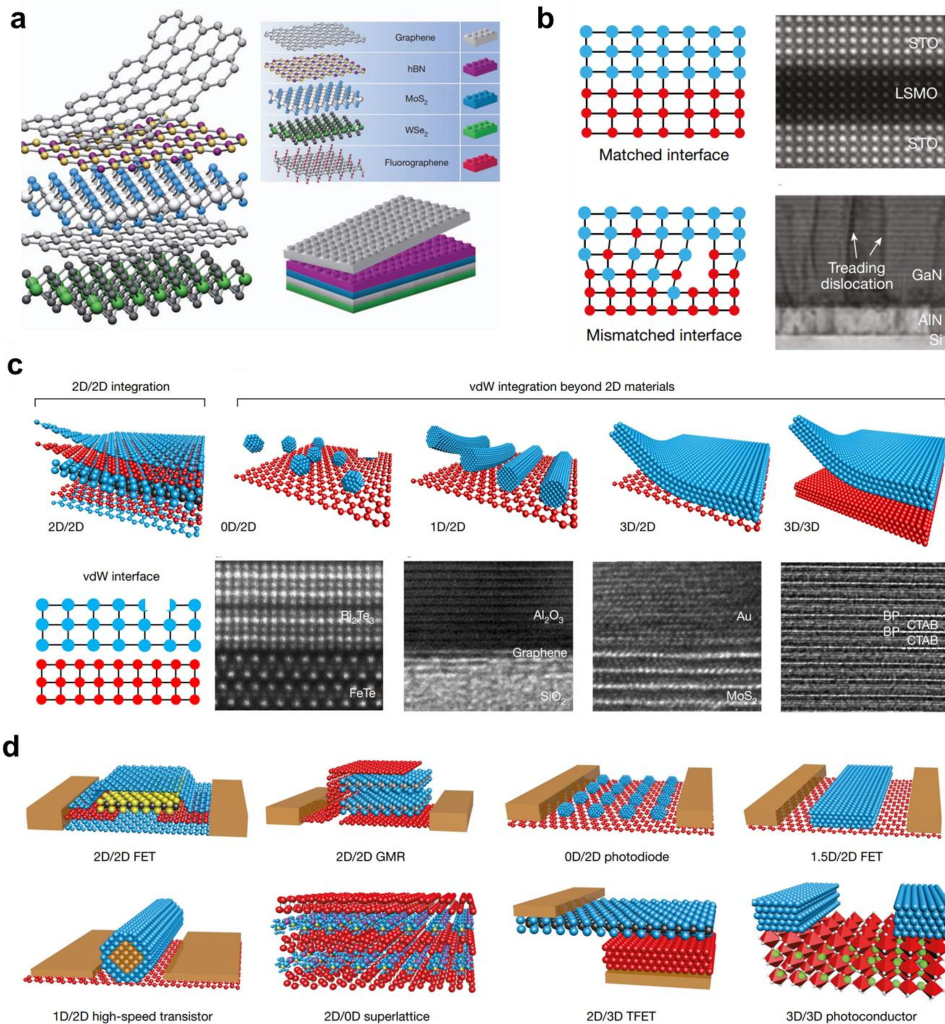


Figure 2. van der Waals heterostructures. a Building van der Waals heterostructures like Lego blocks. **b** Schematic illustrations and cross-sectional images of bonded heterostructure interfaces; a lattice-matched interface (top) and a lattice-mismatched interface (bottom). **c** Illustration and structural characteristics of vdWs integrated interfaces. **d** Schematics of state-of-the-art vdWs integrated electronic and optoelectronic devices. Figures adapted from refs [16,17].

1.3.2 Effective Electrostatic Controllability

2D materials possess excellent properties as electronic device materials, and one of their notable characteristics is effective electrostatic controllability. Specifically, when reducing the thickness of 3D bulk materials to create ultra-thin body (UTB) semiconductors below 5 nm[18], the presence of dangling bonds and surface roughness leads to significant scattering of charge carriers, leading to a detrimental impact on device performance. Consequently, these physical limitations prevent further reduction in thickness beyond 5nm. This implies that the thickness of the components cannot be decreased below a certain threshold, indicating the need for higher gate voltages to control charge in depletion or accumulation states[14].

Additionally, when the gate dielectric and source/drain electrodes are fabricated on top of a semiconductor, unintentional bonding can lead to the formation of dangling bonds. This interface trap state not only causes additional scattering for electrons but also hinders the gate electric field, weakening gate coupling. As a result, in silicon, the majority of charged carriers capable of movement in the semiconductor channel are located approximately 1.2 nm away from the insulating interface, reducing the characteristics of electrical controllability[19].

However, in FETs with a two-dimensional semiconductor channel, all electrons are confined to a thin channel composed of atomic layers, allowing all carriers to be consistently influenced by the gate voltage. Furthermore, due to the absence of dangling bonds, there are no interface trap charges, resulting in excellent gate coupling. This enables the suppression of current leakage by applying gate voltage. Consequently, transistors with a 2D channel utilizing these electrostatic

controllability characteristics exhibit an exceptionally high on/off ratio of 10^7 or higher[2].

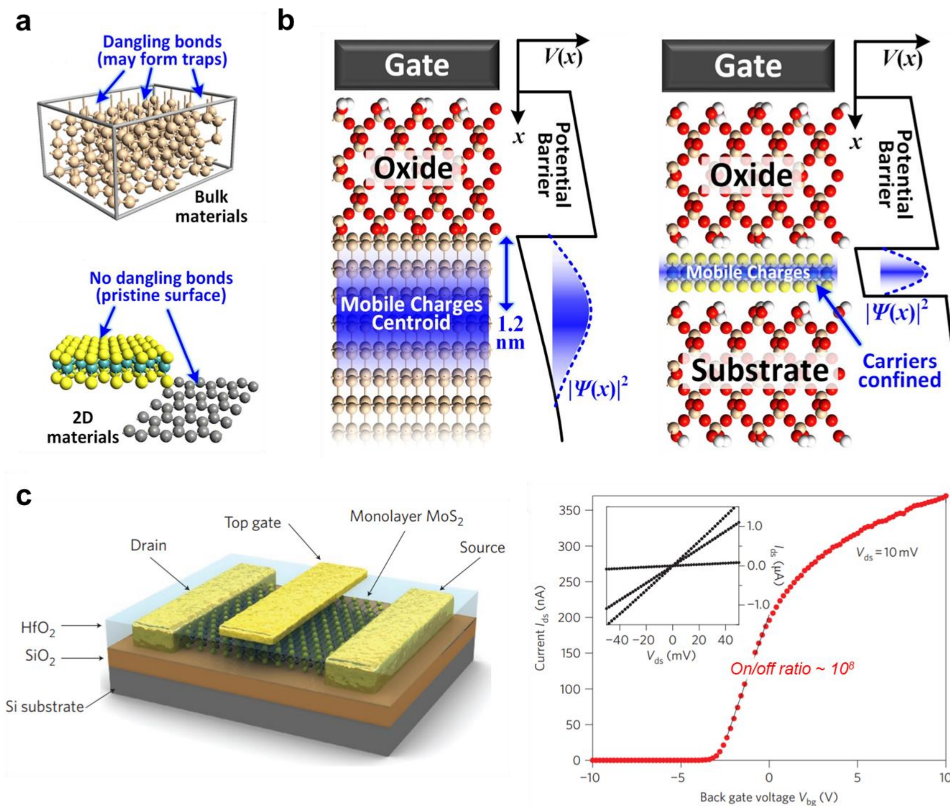


Figure 3. Effective electrostatic controllability. a Schematic illustrating advantages of 2D materials: surfaces of 3D and 2D materials. The pristine interfaces (without out-of-plane dangling bonds) of 2D materials help reduce the interface traps. **b** Mobile charge distribution in 3D and 2D crystals used as channel materials. The carrier confinement effect in 2D materials leads to excellent gate electrostatics. **c** Three-dimensional schematic view and electrical characterization of monolayer MoS_2 transistors. Figures adapted from refs [2,19].

1.3.3 Efficient Polarity Modulation

2D semiconductor-based transistors rely on the barrier of the metal-semiconductor interface between the source and drain to facilitate carrier injection and inherently exhibit ambipolar characteristics. This enables efficient modulation of electron and hole injections into the gate electric field, harnessing the effective electrical control and ambipolar properties of 2D materials. This paves the way for the development of a new concept of reconfigurable polarity-modulated transistors through careful material selection and device structure engineering.

To enhance processor performance, various technologies are being researched on new approaches due to the scaling physical limits of CMOS technology. One of these approaches focuses on expanding the functionality of individual component elements. Reconfigurable FETs are among the technologies being explored in this regard[20]. Reconfigurable FETs can perform multiple operations within a single device by adjusting the voltage input. They provide the flexibility to freely select p-type and n-type switching characteristics by controlling the electrical inputs. This technology differs from traditional CMOS techniques, where p-type and n-type transistors are implemented through fixed doping processes. By changing between different polarity modes, Reconfigurable FETs eliminate the need to separate components, thereby reducing the number of transistors. In addition to these advantages, reconfigurable FETs enable circuit designs with diverse functions and the ability to modify circuit configurations. This offers greater flexibility in circuit design compared to CMOS technology. Furthermore, the reconfigurable devices offer security benefits by making it challenging to identify the functional characteristics of the circuit based on its configuration[21]. Therefore, by leveraging

the efficient polarity modulation characteristics of 2D materials, it becomes possible to implement novel concepts of electronic components distinct from conventional approaches.

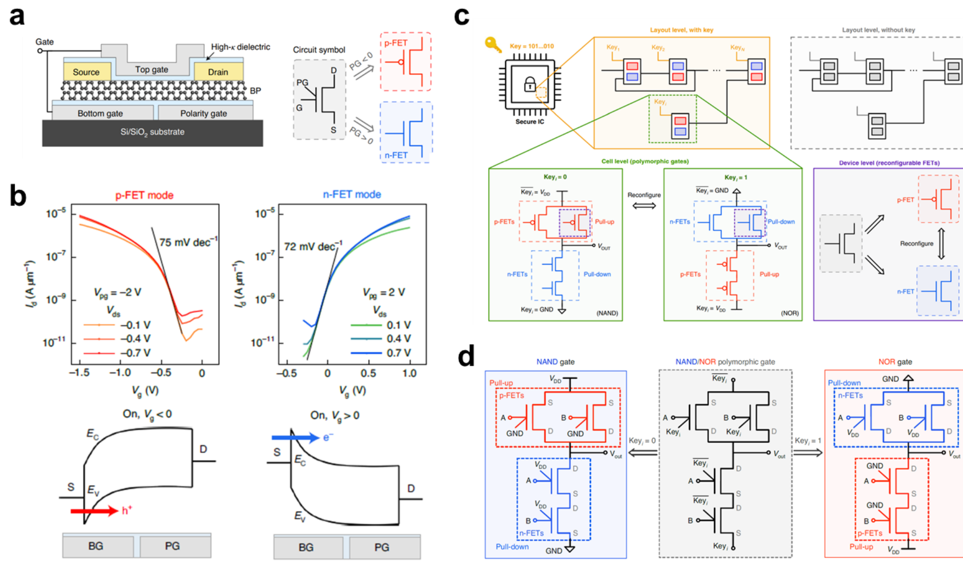


Figure 7. Efficient polarity modulation a Schematic of the reconfigurable BP transistor with polarity gate. **b** Transfer characteristics and Energy band diagrams of a reconfigurable BP transistor in the p-FET mode and n-FET mode. **c** Schematic of a secure chip-enabled by reconfigurable FETs **d** Schematic of a NAND/NOR polymorphic gate leveraging the tunable polarities of the reconfigurable BP transistors. Figures adapted from ref [21].

1.4 Purpose of Research

2D materials possess characteristics such as a flat surface, high charge mobility, and immunity to short-channel effects, allowing them potential candidates to replace silicon semiconductors. However, research on electronic devices based on 2D materials is still in its early stages and has not yet reached the performance level of optimized silicon devices. Therefore, to achieve innovative performance improvements in electronic components, it is necessary to explore approaches that leverage the unique properties and new mechanisms of 2D materials. Consequently, my research goal is to develop a new concept of electronic devices using van der Waals (vdWs) heterostructures, which combine the distinctive features of 2D materials, such as effective electrostatic controllability and efficient polarity modulation, and demonstrate their potential as next-generation materials.

Chapter 2. Highly Efficient WSe_2 Light-emitting Transistor

2.1 Introduction

Transition metal dichalcogenides (TMDs) and their heterostructure have emerged as promising platforms for next-generation optoelectronics application since TMDs in the monolayer (1L) limitation has a large exciton binding energy and strong light-matter interactions due to broken-inversion symmetry[22-26]. These unique characteristics have enabled the development of exotic optoelectronic quantum devices with functions of chiral light emission, excitonic complexes, and high-temperature exciton condensation, that have not been realized in bulk materials[27-31]. In addition, the photoluminescence (PL) quantum yield (QY) of TMDs can reach near unity by suppressing nonradiative recombination of the charged excitons[32,33]. Despite the great potential of TMD, the low external quantum efficiency (EQE) of TMD-based light-emitting devices with various device structures, such as lateral p-n junctions, vertical quantum well, and AC-driven emitter, has been the major obstacle to overcome for their practical applications[34-39].

There are two main requirements to improve the EQE of TMD-based light-emitting devices: enhancing the PL QY of the emitting material and efficient injection of charge carriers[40]. However, it is challenging to achieve both conditions simultaneously. Efficient carrier injection into the emission layer requires increasing the doping concentration of the emitting layer using electrostatic or chemical doping to reduce Schottky barrier height[41]. However, high doping in TMDs leads to the

formation of excitonic systems such as charge excitons, which have lower efficiency than neutral excitons with dominant radiative recombination paths[32]. This tradeoff limits the range of doping as a carrier injection technique and demands looking for alternative injection mechanisms that can facilitate carrier injection without creating excess charge populations. Therefore, a new structure is needed that meets both requirements.

Here, I demonstrate the electroluminescence (EL) of neutral excitons electrically confined in the one-dimensional (1D) neutral region using light-emitting transistors (LETs) based on van der Waals (vdWs) heterostructure with double gates. The WSe_2 LETs consist of a WSe_2 emission layer, graphene electrodes, or gate, and hBN dielectric layer. To achieve highly efficient light emission in gate tunable LETs structure, I chose WSe_2 as an emission layer due to its ambipolar transport properties, direct bandgap semiconductor, and high-temperature quantum yield[42-47]. The 1L graphene was used as a gate-tunable electrode with vdWs contact to suppress Fermi level pinning and achieve band alignment of ambipolar transport between graphene and WSe_2[48-50]. I confirmed that an hBN-encapsulated 1L WSe_2 FET with 1L graphene contacts exhibits ambipolar transport, while intrinsic 1L WSe_2 FET using evaporated metal reported p-type conductance regardless of metal types[51,52] By electrically modulating gate and drain bias, WSe_2 LETs device selectively injected charge carriers into WSe_2 from graphene and controlled the transport of injected charges by modulating the barrier height between WSe_2 homojunction, resulting in a reconfigurable electrical characteristic. I achieved strong electroluminescence with a high EQE of ~8.2% at room temperature by optimizing the injected density of electrons and holes. The EL exhibits dominant emission of neutral excitons by

electrically confining excitons and releasing charged excitons in the intrinsic 1D region of WSe_2.

2.2 Experiment Section

2.2.1 Device Fabrication Process

All the flakes were mechanically exfoliated from a bulk crystal onto SiO_2/Si substrate with a thickness of 285 nm of SiO_2. Stacks of flakes consisting of top hBN, graphene electrodes, WSe_2, and bottom hBN were fabricated using the pick-up transfer technique with a polydimethylsiloxane (PDMS) stamp coated with a polycarbonate (PC) film[53]. The stacked heterostructure was transferred onto graphene as a gate on a SiO_2 (285 nm)/Si substrate by releasing the PC film from the PDMS at 180 °C. The PC film was dissolved in chloroform overnight. The stacked heterostructure was annealed at 300℃ for 3h in a 10^{-4} Torr vacuum to enhance adhesion between layers 37. To form connections between the metal and embedded graphene, I patterned the sample using e-beam lithography (Raith pioneer 2) and then exposed it to XeF_2 gas of 2Torr for 200s at room temperature using XeF_2 etcher (VPE-4F, SAMCO)[54]. The metals Cr (1 nm)/Pd (40 nm)/Au (50 nm) were deposited by an e-beam evaporator (Korea Vacuum Tech.) under ultrahigh vacuum conditions of ~10^{-7} Torr, followed by a lift-off process.

2.2.2 Material Characterizations

Raman and photoluminescence spectra were measured using Raman spectroscopy (LabRAM HR Evolution) with 532nm laser excitation under ambient conditions. To

obtain Raman and photoluminescence mapping images, samples were scanned on an x-y stage with laser illumination.

2.2.3 Electrical and Optoelectrical Measurements

For electrical measurement, a semiconductor parameter analyzer (Keithley 4200A-SCS) was used at room temperature under 10^{-3} Torr. EL spectra were measured by using a customized optical measurement system with a photodetector (Si avalanche) and electrical bias and gate voltage were applied by source meters (Keithley 2400). All EL measurements were performed in a 10-2 Torr vacuum chamber, with light signals collected through X100 objective lens. The use of vacuums enabled stable measurement of the devices.

2.2.4 Electrostatic Simulation for EL of Electrically Confined Neutral Exciton in WSe_2.

To obtain quantitative information on the charge density distributions, electrical potentials, electric field, and excitonic confining potential in the device, I used commercial finite element analysis software (COMSOL Multiphysics). The simulated device geometry is depicted in Figure 13 including double gates of graphene gate and silicon back gate, 1L graphene electrodes, and hBN with 30 nm thickness. The semiconductor behavior of WSe_2 was calculated using the drift-diffusion model with the density-gradient theory[55]. The carrier density was determined based on the Fermi-Dirac distribution, considering the band structure, Fermi level, and density of states (DOS) of WSe_2. The following material parameters were used in the calculation: WSe_2 bandgap: 1.65 eV, dielectric constant: 21 mobility

= 31 cm^2/Vs election affinity= 3.7 V, effective DOS = 6×10^{24} m^{-3}. The dielectric constants for hBN were 3.76 in the out-of-plane direction and 6.93 in the in-plane direction[55-61].

The excitonic confining potential of excitons was calculated using an equation derived from the previous studies, based on electric field and charge density which were obtained from calculation and measurement constants[62]. The constants used were exciton polarizability of 10.027×10^{-5} $meVcm^2/kV^2$, trion polarizability of 411.367×10^{-5} $meVcm^2/kV^2$, trion hyperpolarizability 8.48×10^{-7} $meVcm^4/kV^4$, effective exciton-electron coupling strength of approximately 0.7 $\mu eV\mu m^2$ and trion-electron coupling strength of 1.32 $\mu eV\mu m^2$ [63-65].

2.3 Result and Discussion

2.3.1 Device Structure and Fabrication Process

Figure 9a illustrates the WSe_2 LETs structure with double gates used to demonstrate the confinement of neutral excitons in the 1D region of WSe_2. To fabricate the device, individual 2D flakes were exfoliated on SiO_2/Si substrate and then stacked layer-by-layer using a dry pick-up transfer method[53] (see Figure 8). During the transfer process, a stacked sample was aligned precisely so that the graphene gate overlapped a portion of 1L WSe_2, as shown in Figure 9b. The WSe_2 and graphene were encapsulated with hBN, as an ultra-flat and trap-free 2D dielectric that can neutralize doping levels and enhance optical and electronic properties[66-68]. By adjusting the contact barrier height, 1L graphene was used as an electrode to selectively inject electrons or holes into WSe_2. After the transfer of the stacked sample onto the graphene gate, it was annealed at 300°C to enhance interfacial adhesion between

layers[69]. Since the stacked sample of WSe_2 and graphene are embedded in hBN, I performed the graphene etch stop technique for the 2D via contact to connect with metal leads, as described in previous reported my group research[54,70]. To form the metal leads to the embedded graphene as electrodes and gate, the stacked sample patterned by e-beam lithography was exposed to XeF_2 gas to etch only the hBN, converting the exposed graphene to fluorographene, followed by metal deposition on the etched region and fluorographene. After the device fabrication processes, there were no contaminations and cracks at the interfaces between layers in the stacked sample, as shown in the dark-field optical microscopic image (see Figure 8).

The energy band diagram depicted in Figure 9c illustrates that double gates can independently control the band structure of divided two regions of WSe_2. The graphene contact can selectively inject electrons or holes into the WSe_2 by modulating the contact barrier between WSe_2 and graphene. Simultaneously, injected charge carriers of electrons and holes from each contact can be transported through potential difference by drain bias into the intrinsic region in the WSe_2 p-i-n junction, leading to emission in the 1D region due to electron-hole (e-h) recombination.

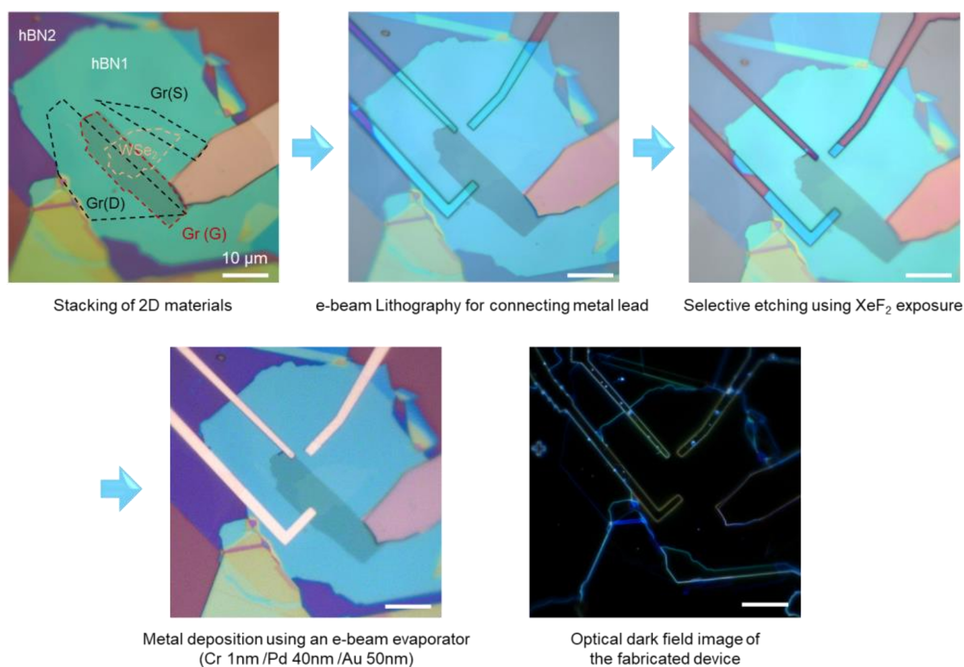


Figure 8. The fabrication process of WSe_2 LETs. First, the top hBN (hBN1), 1L WSe_2, two 1L graphene (Gr(D), Gr(S)), and bottom hBN (hBN2) flakes were stacked in sequence and transferred onto multilayer graphene exfoliated on a SiO_2/Si wafer. Next, e-beam lithography was used to pattern windows to connect metal leads to graphene. To contact the embedded graphene, I etched only the hBN using XeF_2 gas exposure, converting the exposed graphene to fluorographene. The following metal was deposited via e-beam evaporation, forming the metal leads to connect with the graphene. Finally, I checked a clean interface at the fabricated device using dark-field optical microscopy The van der Waals heterostructure was confirmed to have clean interfaces with free contamination or cracks. All scale bars are 10μm in length.

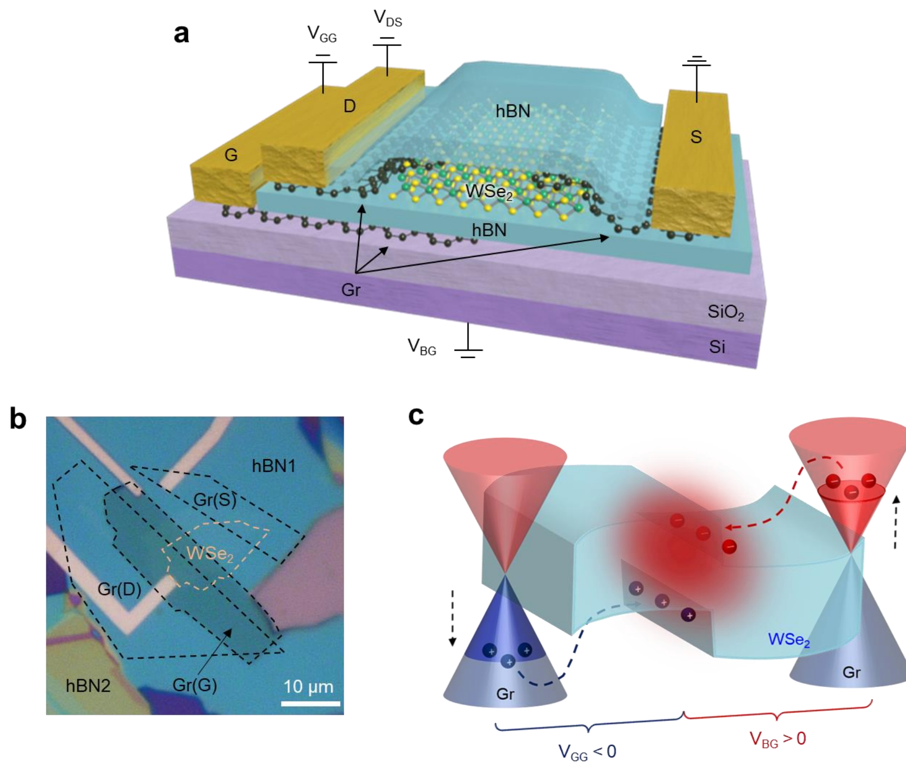


Figure 9. Device geometry and working principle of WSe_2 LET. a Schematic illustration of 1L WSe_2 LET with 1L graphene contact encapsulated by hBN. **b** Optical image of the fabricated device. A portion of 1L WSe_2 is overlapped by the graphene gate. **c** Band diagrams of the device at electroluminescence operation.

2.3.2 Reconfigurable Electrical Characteristics

To validate efficient carrier injection and control of carrier transport in WSe_2 LET, I measured the reconfigurable electrical characteristics of polarity control and operation mode by modulating electric bias, as shown in Figure 10. When a constant positive voltage was applied to the silicon back gate (V_{BG} = 60 V), the transfer curve (V_{GG} - I_{DS}) of low drain bias (V_{DS} = 0.5 V) in Figure 10a exhibited n-type transport behavior with no hysteresis, similar to reports on an hBN-encapsulated 2D transistor with n-type polarity[71]. At positive back gate bias of 60 V, the work function of graphene contact as the source (Gr (S)) shifted close to the conduction band of WSe_2, and the conduction band of WSe_2 bent down simultaneously, resulting in efficient electron injection, as illustrated in Figure 10c. By sweeping graphene gate voltage (V_{GG}), the transport of injected electrons in WSe_2 could be controlled due to the energy barrier of homojunction WSe_2, thereby enabling transistor operation with switching modes between on and off states (see Figure 10c. (i) – (ii)). Under the high drain bias (V_{DS} = 2 V, V_{BG} = 60 V), the transfer curve (V_{GG} - I_{DS}) exhibited bipolar transport behavior with higher on-current compared to the low drain bias case. When the negative voltages were applied to the graphene gate, the current increased in contrast to off-current at a low drain voltage of 0.5 V. This increase can be attributed to the injection of holes from the graphene contact used as the drain (Gr (D)) into WSe_2. Consequently, the enhanced current is caused by e-h recombination in the WSe_2 homojunction by the injected carrier from each electrode as shown in Figure 10c (iii). Under positive voltage conditions of $V_{GG,}$ injected electrons from Gr (S) are transported across the energy barrier formed in the WSe_2 homojunction, leading to electron conductive mode. Conversely, in the case of positive gate voltages of V_{GG} = -6 V for p-type operation, holes can be injected from the Gr (D) into the WSe_2

layer, leading to p-type transport. These results indicate that the device can efficiently control the other selective injection of charge carriers and the transport of injected carriers through WSe_2.

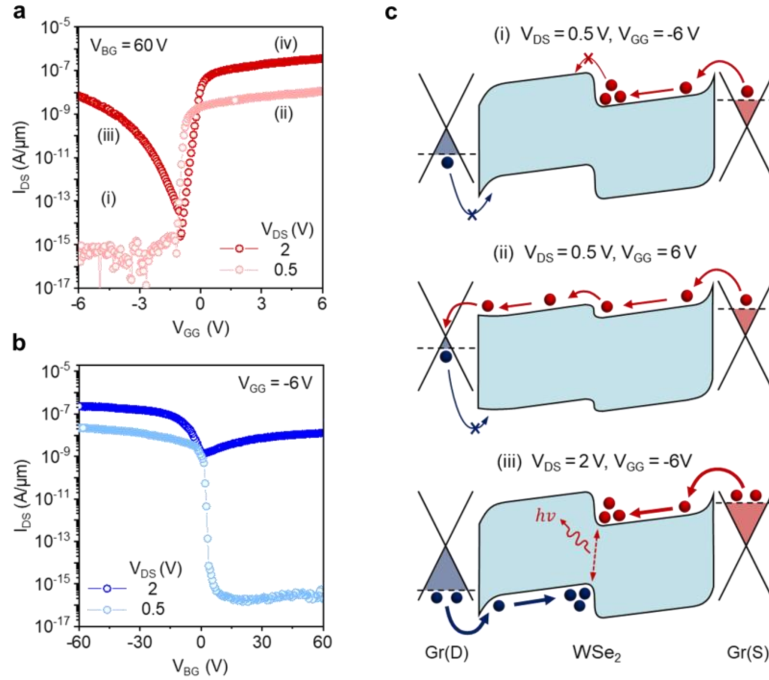


Figure 10. Reconfigurable transport properties using electrical modulation of WSe_2 LET. **a** Transfer curve (I_{DS}-V_{GG}) of the device at a fixed voltage of V_{BG} = 60 V for n-type transport operation. **b** Transfer curve (I_{DS}-V_{BG}) of the device at a fixed voltage of V_{GG} = -6 V for p-type transport operation. **c** Schematics of band diagrams of three conditions at the n-type operation of the device using electrical modulation.

2.3.3 Light Emission

Applying opposite voltage using double gates (V_{BG} = 60 V and V_{GG} = -6 V) created a p-n homojunction formed in WSe_2, resulting in strong rectifying behavior in the output curves as shown in Figure 11a. The increasing current under forward bias can be attributed to the radiative recombination of e-h pairs injected from each graphene in the intrinsic region of the 1L WSe_2 channel, leading to light emission. When a forward bias of V_{DS} = 3 V was applied, the device exhibited EL with a spectrum consistent with the PL spectrum of WSe_2 as shown in Figure 11b. This correspondence indicates that the EL at 1.65eV originated from the recombination of excitons across the direct bandgap of WSe_2. The strong EL was observable through an optical microscope in Figure 11c and was mainly emitted from the 1D regions between p-n WSe_2 homojunction. Thus, the 1D region can be considered an intrinsic region with a built-in electric field, where excitons could efficiently dissociate into free carriers or inject free carriers to recombine e-h pairs.[41,72] Based on the EL emission region, it is expected that light emission occurs within the confined 1D intrinsic region between WSe_2 p-n homojunction through the radiative recombination of electrons and holes. injected over the contact barriers.

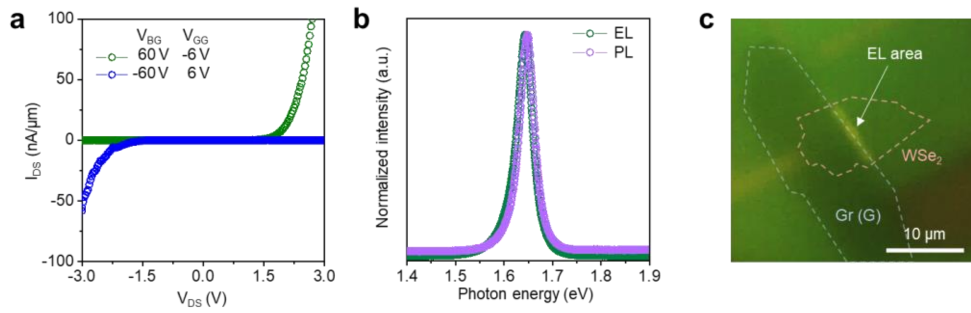


Figure 11. Light emission of WSe_2 LET. a Output curves (I_{DS}-V_{DS}) at opposite voltage using double gates. **b** Normalized PL and EL spectra of the device. **c** Optical image of light emission of the device. Strong EL is observed at the p-n junction of WSe_2.

2.3.4 Electrical Tunability of Electroluminescence

To investigate the electrical tunability of WSe_2 LET, I measured the EL intensity and EQE at varying drain bias or gate voltages in Figure 12. As V_{DS} increased, the EL intensity increased as shown in Figure 12a, along with an increasing current density of the output curve with strong rectifying behavior (Figure 11a). To improve the accuracy of EQE, I estimated the total loss of the system using a standard AlInGaP micro-LED with an emission window of a 20μm diameter, of which EQE is measured precisely in an integrated sphere.[73] As shown in Figure 12b, the EQEs of the WSe_2 LET increased as a function of the $V_{DS,}$ reaching a maximum of ~5.3% around 2.5V at room temperature. Beyond 2.5 V, EQE decreased due to the emergence of nonradiative recombination paths, such as exciton annihilation at high exciton concentration. In addition, I measured the EL intensity while varying one of the double gates, with the other fixed, to verify the gate tunability of EL in the device. The EL contour plot of Figure 12c shows n-type modulation by varying with V_{BG}. At fixed V_{GG}, holes were accumulated near the WSe_2 homojunction by being easily injected from high p-doping. By reducing the contact barrier through V_{BG} and lowering the Fermi energy level of the graphene contact, more electrons could be injected. Consequently, the EL intensity increased as V_{BG} increased, exhibiting a sharp EL peak at 1.65 eV. In the reverse case of p-type modulation with varying V_{GG} at fixed V_{BG} and V_{DS}, the EL intensity also increased due to lower the contact barrier for the hole injection (see Figures 12e, f). It is worth noting that the contour plot showed that a monochromic EL peak was consistently maintained at 1.65eV, regardless of which $V_{DS,}$ V_{BG}, and V_{GG} were modulated. This phenomenon suggests that EL occurred within the 1D intrinsic region at the WSe_2 homojunction, and the more detailed results were further investigated in Figure 13. Furthermore, I extracted

EQE while varying the V_{BG} in Figure 12. The EQE of the WSe_2 LET increased as a function of the V_{BG}, reaching a maximum of ~8.2% in the vicinity of 5V at room temperature, which is the highest value compared to 2D-based emitters. Above 5V of V_{BG}, the EQE slightly decreased. However, when varying V_{GG} for the p-type modulation, no deterioration in EQE was observed (see Figure 12f.) This indicated that achieving a high EQE is not solely dependent on increasing the carrier density but also relies on maintaining a balance of electrons and holes. Therefore, I have demonstrated that the WSe_2 LET with efficient gate tunability is an effective structure.

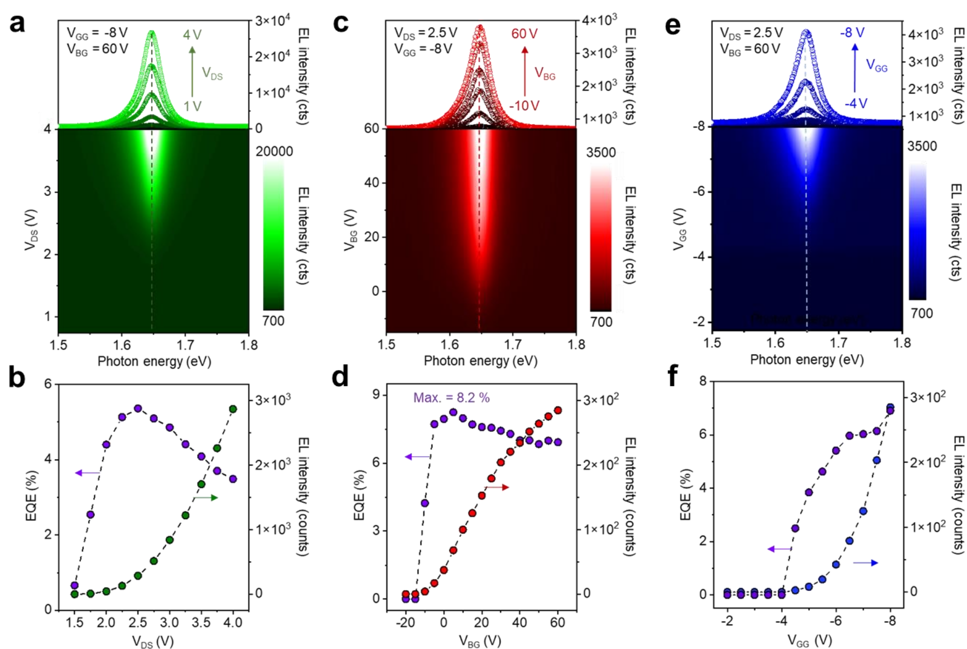


Figure 12. Electrical tunability of electroluminescence of WSe_2 LET. a EL spectrum and contour plot of the device at varying V_{DS} and fixed V_{GG} = -8 V and V_{BG} = 60 V. **b** EQE (purple) and EL intensity (green) as a function of V_{DS}. V_{GG} and V_{BG} were fixed at -8, and 60 V, respectively. **c** EL spectrum and contour plot of the device at varying V_{BG} and fixed V_{DS} = 2.5 V and V_{GG} = -8 V. **d** EQE (purple) and EL intensity (red) as a function of V_{BG}. V_{DS} and V_{GG} were fixed at 2.5, and -8 V, respectively. **e** EL spectrum and contour plot of the device at varying V_{GG} and fixed V_{DS} = 2.5 V and V_{BG} = 60 V. **f** EQE (purple) and EL intensity (red) as a function of V_{GG}. V_{DS} and V_{BG} were fixed at 2.5, and 60 V, respectively.

2.3.5 Electroluminescence of Electrically Confined Neutral Exciton

To investigate the origin of electroluminescence of neutral exciton in the confined 1D region of the WSe_2 homo-junction, I compared the gate-tunable PL spectrum and EL spectrum of WSe_2 LET in Figures 13a, b. All EL and PL spectra were normalized and deconvoluted into a neutral exciton peak (X^0) and charged exciton peak (X^*) for comparison. In Figure 13a, the PL spectrum of hole-doped and electron-doped regions in WSe_2 LET exhibited both peaks, with the X^* being stronger than X^0. As the doping density increased with applied gate bias, the charged exciton peak became dominant, resulting in a redshift of the PL peak and a decrease in the PL intensity of WSe_2 [44]. However, in the EL spectrum emitted in the WSe_2 homojunction in Figure 13b, X^0 was more dominant than X^*. As shown in Figure 13c, the ratio of the neutral exciton to charged exciton in the EL peak was about 14 times higher than that of PL peaks for both n-doped and p-doped cases. This indicates that the EL predominantly originated from the intrinsic region with low doping concentration, occurring at WSe_2 p-i-n homojunction. The energy band diagram in Figure 13d shows the formation of the int intrinsic region near the two n-doped and p-doped regions due to the alignment with the Fermi level. In the intrinsic region, neutral excitons are generated by transported charge carriers injected from each electrode. Figure 13e shows the charge density, exciton potential, charge exciton potential, and voltage near the p-i-n homojunction in the WSe_2 obtained from the device's electrostatic simulations. When WSe_2 is formed into p-type and n-type regions from both sides, electrons, and holes diffuse in both directions, leading to the generation of a strong in-plane electric field in the intrinsic region due to the density difference between the n-type and p-type regions. In addition to the built-in potential, excitons formed by the combination of injected electrons and holes experience repulsive interaction

energies proportional to the charge density, causing them to be pushed toward the intrinsic region. This repulsive interaction is a force acting on the exciton due to the charge density gradient, which pushes the exciton toward an area of lower charge density[62]. This is a unique phenomenon observed TMDs with large exciton binding energies, which allows the exciton to withstand in-plane electric fields[74]. Furthermore, charged excitons with electric charges experience repulsive potentials that push them toward the n-doped and p-doped regions, respectively. As a result of these two phenomena, only confined neutral excitons emit light in the 1D intrinsic region.

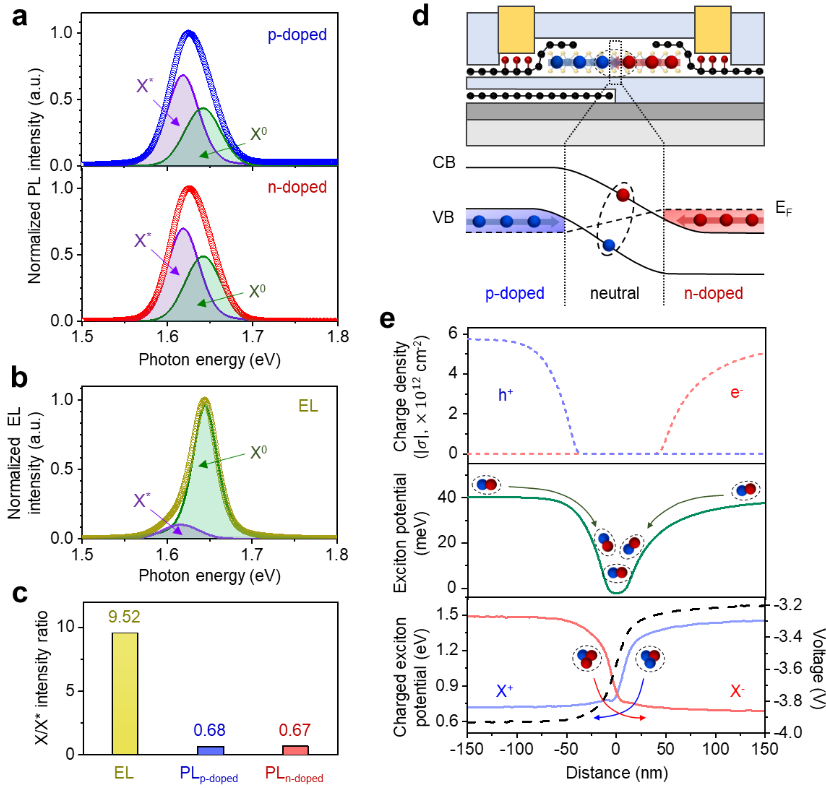


Figure 13. Electroluminescence of electrically confined neutral exciton at the intrinsic region in p-i-n homo-junction of WSe_2. a Normalized PL spectrum of hole-doped (blue) and electron-doped (red) WSe_2 in the WSe_2 LET measured at V_{GG} = -6 V and V_{BG} = 60 V, respectively. **b** Normalized EL spectrum of the device. All spectrums were deconvoluted into the two distinct peaks of the neutral exciton (X^0, green) and charged exciton (X^*, purple)**. c** X/X^* intensity ratio of comparison of PL and EL. **d** Schematic of the device structure of WSe_2 LET and energy band diagram in the p-i-n regime of WSe_2. **e** Electrostatic simulation of the spatial dependence of charge density of holes (blue dashed line) and electrons (red dashed line), exciton potential (green line), and potential of the positively charged exciton (blue line) and negatively charged exciton (red line), and voltage (black dashed line) in WSe_2.

2.3 Conclusion

In conclusion, I have demonstrated the electroluminescence of electrically confined neutral excitons using the light-emitting transistor structure with double gates. By carefully aligning the band structure of WSe_2 and graphene, my WSe_2 LETs exhibited reconfigurable electrical characteristics. Through the precise balance of electrons and hole concentrations, I achieved a high EQE of ~8.2%, which is attributed to the presence of electrically confined neutral excitons, which undergo dominant radiative recombination in the 1D intrinsic region of WSe_2. This work not only highlights the potential of 2D light-emitting devices but also provides a new avenue for modulating the recombination of neutral and charged excitons for excitonic devices.

Chapter 3. Reconfigurable 2D Memory for Logic-in-memory

3.1 Introduction

The demand for high-performance memory continues to grow as artificial intelligence applications expand and technology advances. In traditional von Neumann architectures, the separation of the processing unit (CPU) and the data storage device leads to bottlenecks in data transfer, making efficient data processing challenging[75]. To overcome these issues, the development of new approaches for high-performance processors is necessary. Recently, logic-in-memory technology has gained attention as an efficient approach to data processing[76,77]. This technology performs data storage and processing functions in a single device, offering advantages in overall performance improvement. However, to meet the demands of high-performance processors, the development of logic-in-memory devices with high integration and complex functionality is crucial.

Two-dimensional materials, with their high mobility even at the atomic thickness and immunity to short-channel effects through effective electrostatic controllability, hold great promise as candidates for scaling semiconductor devices[14,15,19]. Logic-in-memory technologies based on these unique properties of two-dimensional materials have been reported, primarily focusing on implementing complex functionalities in devices and exploring new computing array applications[78,79]. However, the crucial aspect of high integration in high-performance processors has not been discussed yet.

In this study, I demonstrated a high-integration logic-in-memory application using

van der Waals heterostructure-based reconfigurable and cascadable floating-gate field-effect transistors (FG-FETs). The device consists of a WSe_2 ambipolar channel layer, graphene floating gate, and hBN tunneling layer. I utilized WSe_2 as the channel layer due to its ambipolar transport characteristics and efficient polarity modulation[80]. By controlling the programming voltage of a single gate, I can manipulate the trapped charge density and voltage on the floating gate, allowing us to control the type and density of doping in WSe_2, resulting in reconfigurable conduction characteristics encompassing all types of electrical conduction (n- and p-type, metallic, and insulating). Moreover, I can precisely control the movement of the threshold voltage concerning the trapped charge density. In the logic circuits composed of these devices, I can implement all 16 Boolean logic functions within a single configuration. Furthermore, by utilizing electrical threshold voltage control without additional gates or structural optimizations, I can apply cascading techniques, significantly enhancing the flexibility of complex circuit designs[81]. I integrated 1-bit full adders, subtractors, and comparators using the reconfigurable microprocessor with continuous connections, demonstrating its contribution to high functionality and high integration in logic synthesis.

3.2 Experiment Section

3.2.1 Device Fabrication Process and Material Characterizations

All flakes were obtained through mechanical exfoliation from a bulk crystal onto a SiO_2/Si substrate with a 285 nm thickness of SiO_2. I performed characterization using Raman spectroscopy (JASCO) with 532nm laser excitation under ambient conditions and atomic force microscopy (AFM, NX10) to confirm the thickness of

all flakes. To achieve ambipolar transport and maintain a consistent operating voltage, specific thicknesses were selected for the WSe_2: (5 ± 1) nm, hBN: (8 ± 1) nm, and graphene (7 ± 1) nm flakes. To fabricate stacks of flakes comprising the top WSe_2 channel, hBN tunneling layer, and bottom graphene floating gate, the pick-up transfer technique was conducted A polydimethylsiloxane (PDMS) stamp coated with a polycarbonate (PC) film was used for the transfer[53]. The stacked heterostructure was transferred onto a SiO_2 (285 nm)/Si substrate by releasing the PC film from the PDMS at 180 °C. The PC film was dissolved in chloroform overnight. To form connections between the metal and channel, the sample was patterned using e-beam lithography (Raith Pioneer 2). The metals Ti (30 nm)/ Au (30 nm) were deposited using an e-beam evaporator (Korea Vacuum Tech.) under ultrahigh vacuum conditions of ~10^{-7} Torr, followed by a lift-off process. To enhance adhesion between the layers and remove polymer residues, the fabricated devices were annealed at 200 °C for 3 hours under a 10^{-4} Torr vacuum[82].

3.2.2 Electrical Measurements

A semiconductor parameter analyzer (Keithley 4200A-SCS) carried out all electrical measurements at room temperature. For the inverter, the pads of the samples were connected using a wire bonder. (K4523) to enable electrical measurements.

3.3 Result and Discussion

3.3.1 Highly Integrated Logic-in-memory Circuit based on WSe_2 FG-FETs

Figure 14a illustrates the highly integrated circuit layout of the memory device for logic-in-memory This single circuit can perform various complex operations, such as adder, reducing the number of circuits required for computations and thus demonstrating superiority in terms of high integration. To achieve high integration for logic in memory, our memory component has been designed considering three key features. First, it should offer multiple functions within a single device. The more functions a device can provide, the significantly smaller the area of the constituent components of the circuit. Secondly, the number of gates should be minimized. An increased number of gates leads to increased spatial requirements, complex circuit layouts, and higher power consumption. Thirdly, it should allow for cascading to enhance circuit design flexibility. Cascading enables simplified circuit configurations and facilitates important parallel processing capabilities in logic in-memory applications. Figure 14b, c shows an ambipolar WSe_2 floating gate memory structure and optical image that exhibits these characteristics. Our device is a van der Waals heterostructure composed of a WSe_2 ambipolar channel layer, graphene floating gate, and hBN tunneling layer. I chose WSe_2 as the channel layer due to its intrinsic ambipolar transport characteristics and efficient polarity modulation, which enable control of both p-type and n-type charge polarities[80,83,84]. Additionally, the ultra-flat 2D dielectric hBN enhances the electrical properties of the channel material and provides freedom from charge traps, thereby improving the reliability of the device. Graphene is chosen as the floating gate due to its high charge storage capacity even at atomic thickness[85]. Furthermore, the van der Waals heterostructure is transferred onto a SiO_2/Si substrate, enabling the presence of a silicon back gate that serves as the control gate. (See the Method section for a detailed fabrication process.)

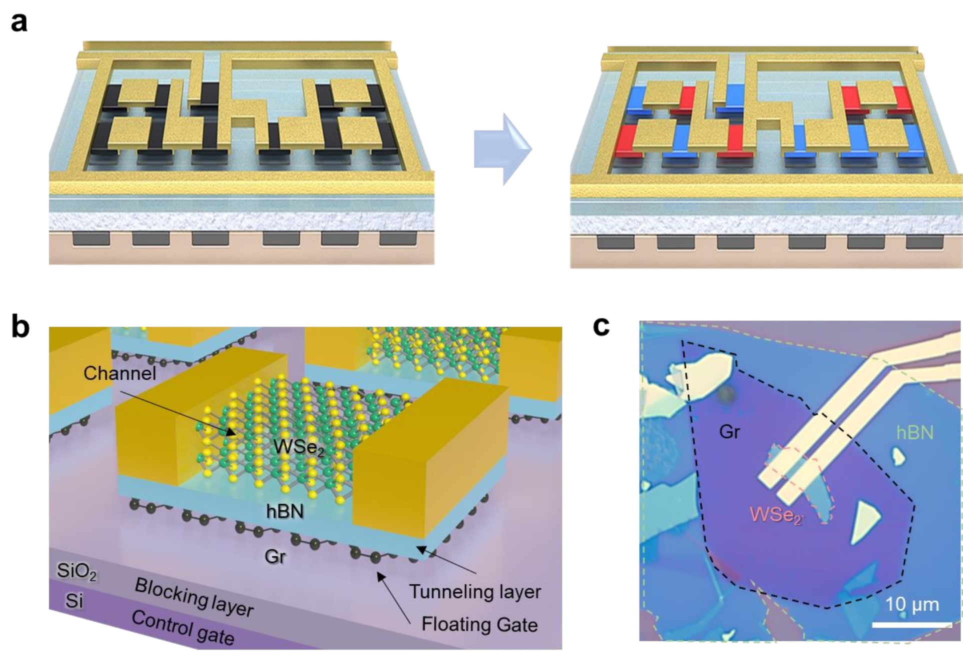


Figure 14. Highly integrated logic-in-memory circuit based on WSe_2 FG-FETs. **a** Schematic illustration of a highly integrated logic-in-memory circuit based on WSe_2 FG-FETs. **b** Schematic illustration of WSe_2 FG-FET based on van der Waals heterostructure. **c** Optical image of the fabricated device.

3.3.2 Ambipolar Memory Characteristics

Since logic-in-memory is composed of memory cells that implement logic operations, I conducted measurements on the basic memory characteristics of the WSe_2 FG-FET. In Figure 15a, the device exhibits the ambipolar memory behavior with significant hysteresis in both n-type and p-type conductance in the transfer curve (V_{BG} - I_{DS}), as the back-gate voltage is swept within the range of ±60 V under a fixed 50 mV drain bias condition. This hysteresis in the transfer curve, known as the memory window, is attributed to the storage of carriers within the graphene floating gate[86]. Figure 15b shows the changes in the memory window size with threshold voltage shift, as the sweeping range varies. The memory window shows a linear increase with back gate voltage for both n-type and p-type conductance, allowing precise control over the type and density of carriers stored in the floating gate in response to voltage (See Figure 15c). To evaluate the stability of the memory operation of our device, I measured the retention and endurance characteristics of the WSe_2 FG-FET. Unless specifically stated, all programming pulse times were 100 ms. Retention measurement in Figure 15d shows a high extinction ratio of both n-type and p-type conductance of over 10^7 even after programming pulses with no noticeable degradation in performance for up to 10,000 s. Additionally, the device performance remains unchanged even after 400 cycles, exhibiting a high extinction ratio. (see Figure 15e) Figure 15f demonstrates the switching characteristics of the memory device as a function of pulse duration with no change in the extinction ratio even at a pulse width of 1 ms. Notably, similar MoS_2 FG-FET structures have achieved fast switching speeds in the nanosecond range, indicating the potential for high-speed operation in our device as well[87,88].

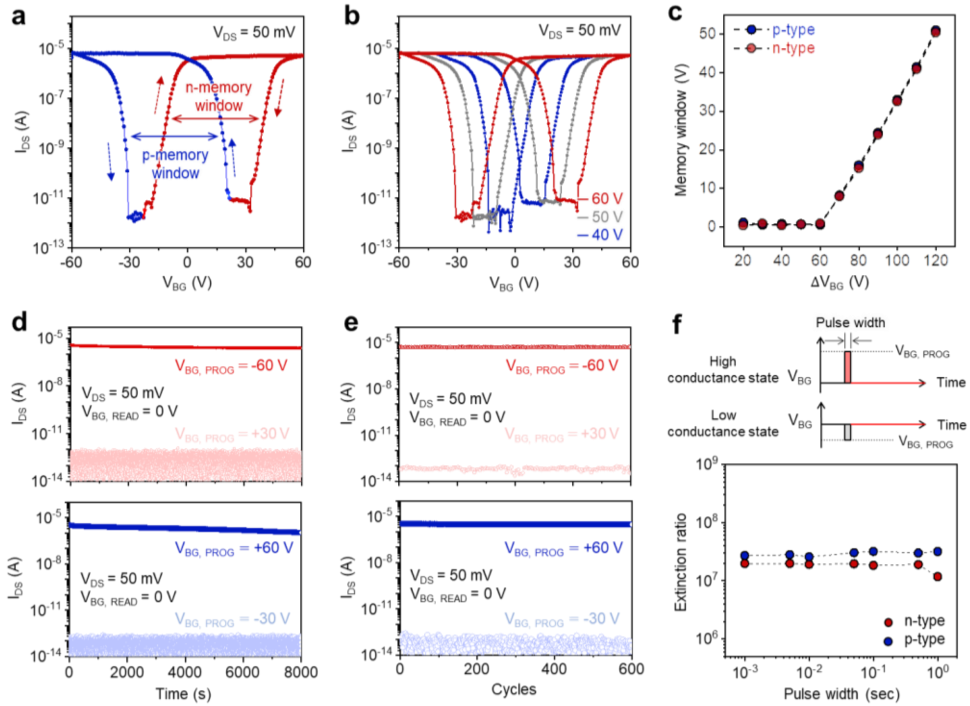


Figure 15. Ambipolar memory characteristics of WSe_2 FG-FET. a Transfer curve (I_{DS}-V_{BG}) of the WSe_2 FG-FET at a fixed voltage of V_{DS} = 50 mV. **b** Transfer curve (I_{DS}-V_{BG}) of the WSe_2 FG-FET with various sweep ranges. **c** Relationship between memory window size and sweep voltage in transfer curve. **d** Retention performance for n-type and p-type transport on the time dependence of drain current for high conductance state (dark circle) and low conductance state (light circle). **e** Endurance performance on n-type and p-type transport for cycles of the high conductance state (dark circle) and low conductance state (dark circle). **f** Extinction ratio varying with programming pulse width.

3.3.3 Reconfigurable Electrical Switching Characteristics

The WSe_2 FGFET, which is used as the basic building block of logic-in-memory instead of conventional FETs, offers reconfigurable switching operations through changes in the threshold voltage with programming pulses, providing an additional degree of freedom in the circuit. A single gate is used to set the memory state with a programming voltage, V_{PROG}, while the device can be switched using relatively low voltages during logical operations. The switching voltage range is limited to $\pm$5 V to preserve the programmed memory state. This allows our memory cell to reprogram electrical conductivity of all types, including metal, insulating, n-semiconductor, and p-semiconductor, by controlling the charge density and type using V_{BG}, as shown in Figure 16a. These states are determined by the charged carriers in the floating gate, which in turn affects the doping density of the channel. Additionally, our device takes advantage of the precise control over the material's conduction state based on V_{BG} to finely adjust the memory cell's threshold voltage (V_{th}). The output curves in each programming state exhibit linear behavior and demonstrate Ohmic-like contacts. (See Figure 16b, c) Figure 16d demonstrates the dynamic switching performance of the WSe_2 FG-FET. Our device shows clear switching characteristics according to different states such as insulating, n-type semiconductor, p-type semiconductor, and metallic state by controlling the programming voltage using a single gate, demonstrating the stability and reproducibility of various circuit configurations.

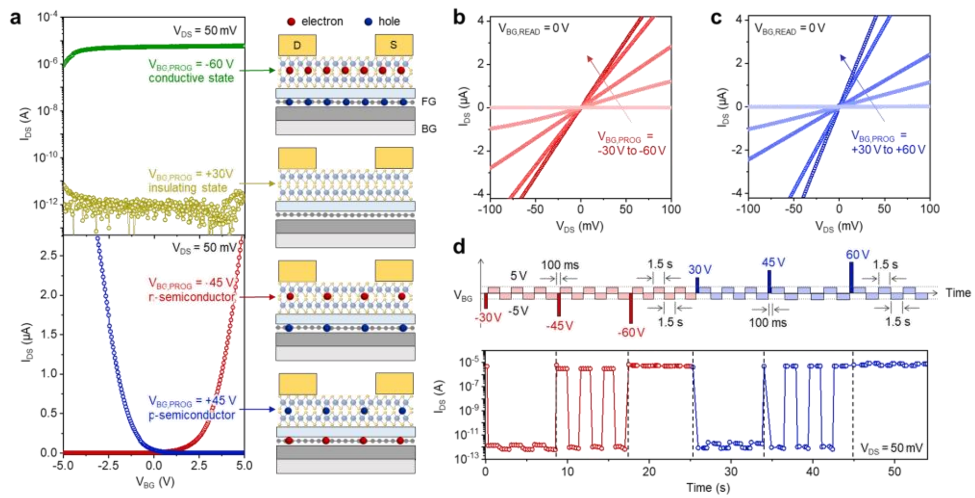


Figure 16. Reconfigurable electrical switching characteristics of WSe_2 FG-FET. **a**. Reconfigurable transfer curve (I_{DS}-V_{BG}) and the corresponding schematic diagrams of the working mechanism of the WSe_2 FG-FET under different programming conditions using $V_{BG,\ and\ PROG}$. **b, c** Output curves (I_{DS}-V_{DS}) of the WSe_2 FG-FET measured at fixed $V_{BG,\ READ}$ = 0 V, for various programming conditions using $V_{BG,\ PROG}$. **d** Dynamic switching performance of the reconfigurable operation as a function of programming pulse.

3.3.4 Programmable Inverter based on WSe_2 FG-FETs

When our reconfigurable FGFET memory is operated in an inverter circuit, it enables various logic operations. By connecting two WSe_2 FGFETs in series, as shown in Figure 17a, the inverter can perform various operations based on the programming state of each memory cell. Figure 17b exhibits the voltage transfer curves (V_{IN} - V_{OUT}) at V_{DD} = 1V after programming each unit cell, demonstrating the logic operations of FALSE, NOT A, A, and TRUE within a single inverter, depending on the programming state. Additionally, our unit memory cell, with its ambipolar characteristics based on WSe_2, allows it to function as both p-type and n-type FETs, enabling the construction of a CMOS inverter, an integral component of integrated circuits (See Figure 17c). In the designed CMOS circuit based on two WSe_2 FG-FET devices programmed to p-type and n-type FETs, the voltage transfer curve (V_{IN} - V_{OUT}) in Figure 17d, exhibits full swing output at various supply voltages while achieving higher voltage gain and lower power consumption.

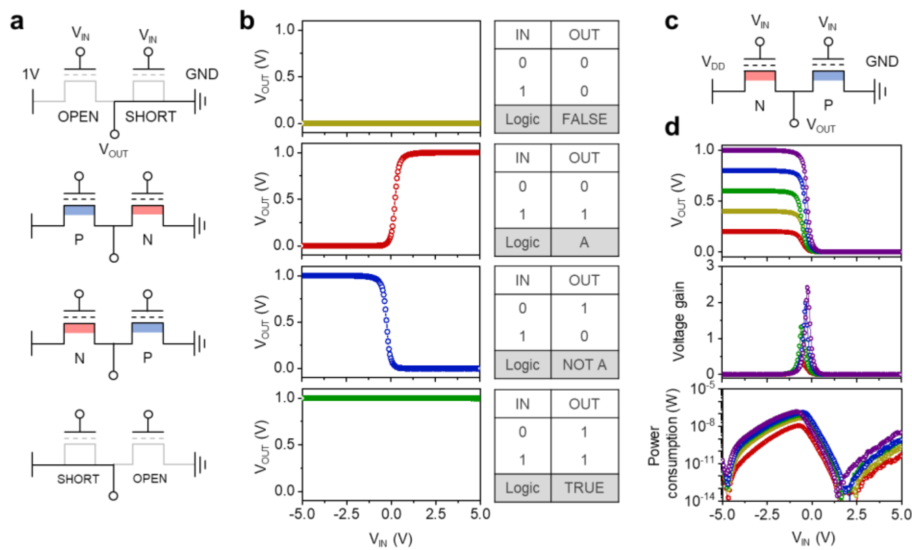
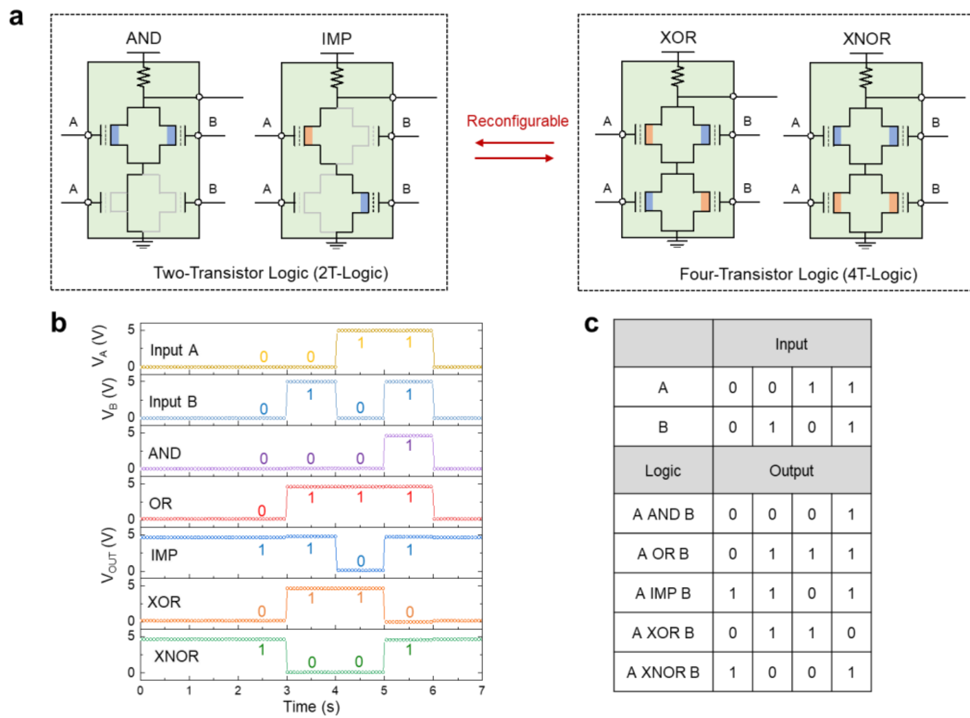


Figure 17. Programmable inverter based on WSe_2 FG-FETs. a Schematic of a circuit diagram for different programming states of the inverter. **b**. Output voltage curves for different programming states at fixed V_{DD} = 1 V, and the corresponding truth tables. **c** Schematic diagram of the CMOS inverter circuit comprising two reconfigurable WSe_2 FG-FETs. **b** Voltage transfer curve, voltage gain, power consumption of WSe_2 FG-FET based CMOS inverter at various supply voltage (V_{DD}).

3.3.5 Programmable Logic-in-memory Circuits for 16 Boolean Logic Functions

The reconfigurable logic functions based on various memory states suggest the potential to construct a collective array of diverse logic circuits within the memory array. When multiple FGFETs are combined as logic gates, the number of possible functions exponentially increases with the number of devices. To demonstrate this, I conducted simulations on the logic-in-memory circuit with 4 memory cells and 1 resistor, exhibiting that it can perform reconfigurable logic functions (see Figure 18a.) As shown in Figures 18b and c, by configuring 2 or 4 transistor logics based on programming, our memory circuit can implement basic logic gates such as AND, OR, IMP, XOR, and XNOR. Additionally, our circuit composed of WSe_2 FGFETs can perform all 16 Boolean functions, which are fundamental operations in logic circuits[89]. (See Figure 19) Our circuit based on WSe_2 FGFETs proves its ability to perform a wide range of logic functions with the least component configuration compared to previously reported 2D-based reconfigurable logic gates.



	Input			
A	0	0	1	1
B	0	1	0	1
Logic	Output			
A AND B	0	0	0	1
A OR B	0	1	1	1
A IMP B	1	1	0	1
A XOR B	0	1	1	0
A XNOR B	1	0	0	1

Figure 18. Programmable logic-in-memory circuit to operate 16 Boolean Logic functions. a Logic gate structure and reconfiguration with proposed FGFET devices. **b** Simulation results of input and output in voltage form. **c** Truth table of logic gate operations

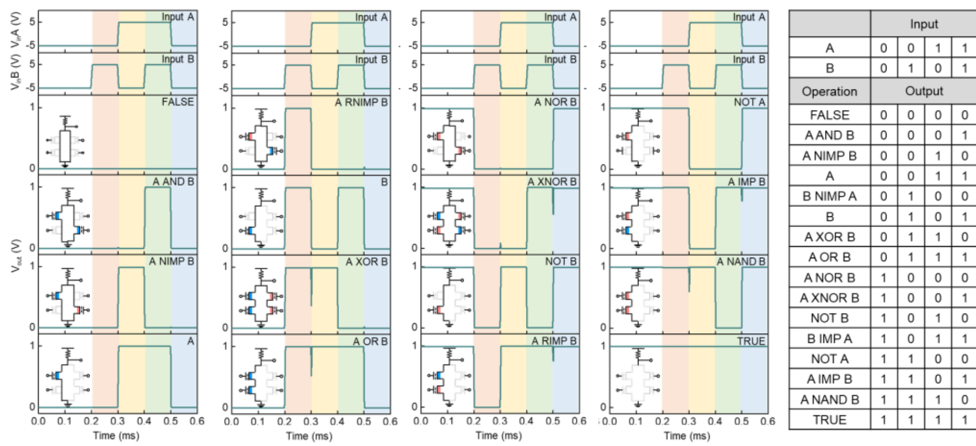


Figure 19. Simulation data of 16 Boolean logic functions

3.3.6 Reconfigurable and Cascadable Logic-in-memory Processor

I present the logic-in-memory processor based on various logic functionalities. As shown in Figures 20a-c, this processor is composed of three cascaded circuits, which can perform 16 Boolean logic operations. Cascading is a circuit configuration approach where the output of one circuit or device is used as the input for the next one, allowing for continuous operation and increasing design flexibility. Therefore, within this structure, I can perform operations such as 1-bit full adder, subtractor, and comparator (see Figures 20d-f). These operations serve as fundamental components in modern processors, demonstrating that our logic-in-memory device can be extended to more complex computation accelerators. By comparing our device with other papers that construct 1-bit full adder circuits based on 2D technology, that our device utilizes the fewest number of components among all 2D-based circuits while offering a wide range of operations.

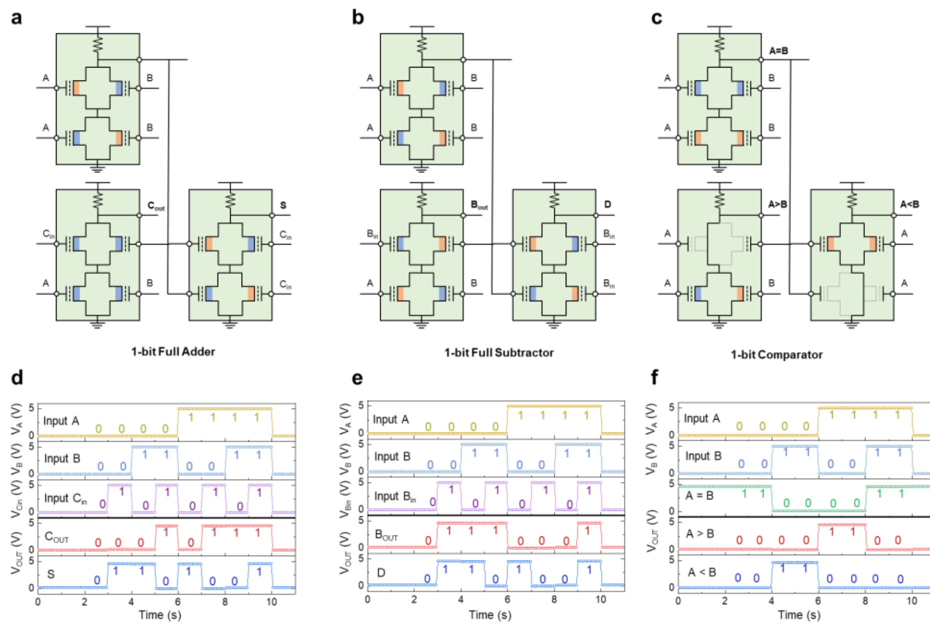


Figure 20. Reconfigurable and cascadable logic in memory processor of computing units. a-c Schematic of three combined configurations to demonstrate (a) 1-bit Full Adder, (b) 1-bit Full Subtractor, and (c) 1-bit Comparator. **d-f** Simulation results of each logic gate. (d) 1-bit Full Adder, (e) 1-bit Full Subtractor, (f) 1-bit Comparator

3.4 Conclusion

In this study, I demonstrated high-integration logic-memory applications using van der Waals heterostructure-based reconfigurable and cascadable FG-FETs. The memory devices allow for reconfigurable electrical conductance through programming, enabling the implementation of 16 Boolean logic functions in circuit configurations. Furthermore, precise control of threshold voltage through the captured charge density enabled us to achieve a reconfigurable microprocessor capable of performing 1-bit full adder, subtractor, and comparator operations through cascading. These results prove the contribution of our logic-in-memory cell in terms of high functionality and integration. Therefore, our proof of concept indicates that s that our high-integration logic in-memory device can serve as a crucial electronic component for next-generation in-memory fields, enabling efficient circuit design and logic operations in terms of area and energy.

Chapter 4. Irreversible Conductive Filament Contact for Passivated vdWs Heterostructure

4.1 Introduction

Among 2D materials, graphene and transition metal dichalcogenides (TMDs) are promising candidates for next-generation electronic devices due to their exceptional electrical properties, such as high carrier mobility at the atomic thickness and immunity to the short channel effect.[2,14,90] However, the sensitive nature of ultrathin 2D materials makes it challenging to avoid unintentional doping and degradation caused by the substrate, adsorbates, and polymer residue[91,92]. To achieve high performance and stability in 2D materials-based devices, it is crucial to form clean interfaces of the 2D channel layer by effective passivation. In this regard, hBN, an impermeable 2D insulator, has proven to be an effective passivation layer, enhancing stability and reducing charged impurity scattering.[67,93,94] Therefore, stacking techniques have been developed to construct the van der Waals (vdW) heterostructures, such as hBN-encapsulated devices with a 2D channel.[41,53,95,96]

For vdW heterostructure devices, forming the metal contacts to the embedded 2D channel layer is essential. While edge contacts have been successfully demonstrated for graphene by making contacts between deposited metal electrodes and the exposed lateral edges of the embedded layer, they are not efficient for TMDs due to edge oxidation during the fabrication process. The graphene etch stop (GES) technique has been proposed as a way to fabricate via contacts of fluorinated graphene (FG) to the embedded graphene.[54] However, this contact technique cannot be applied to TMDs. Recently, transferred via contacts, also known as vdW contacts,

have been demonstrated by transferring metal pre-deposited hBN onto a TMD channel [97] Nevertheless, the transfer of pre-fabricated contacts is challenging and not suitable for large-scale fabrication.

Here, I demonstrate a new contact method for irreversible conductive filament (ICF) contacts to the 2D channel passivated by hBN layers. First, the vdW heterostructures of hBN-encapsulated graphene and MoS_2 were fabricated by stacking 2D layers. Through repeatedly electrical forming processes, ICFs were generated within defective top hBN layers treated by oxygen plasma. These ICF contacts composed of migrated metal atoms and vacancies, functioned as irreversible low-resistance contacts to the 2D channel layer of graphene and MoS_2.

4.2 Experiment Section

4.2.1 Device Fabrication Process

All flakes were prepared by mechanically exfoliating a bulk crystal onto a 285nm SiO_2/Si substrate. The stacks of flakes were fabricated using the pick-up transfer technique with a polydimethylsiloxane (PDMS) stamp coated with polycarbonate (PC) film.[53] The stacks were transferred onto SiO_2/Si substrate by releasing the PC film from the PDMS at 180°C. After the transfer, the PC film was dissolved in chloroform overnight. Then, electrodes were patterned using e-beam lithography. To generate defects in the top hBN, the oxygen plasma treatment was conducted using our customized plasma equipment in a reactive ion etch (RIE) mode (Femto-Science, CUTE). The treatment conditions are the power of 100 W, frequency of 100 kHz, pressure of 10^{-1} Torr, O_2 flow rate of 20 sccm, and treatment time of 30 s. Metals of

Cr (1 nm) / Pd (30 nm) / Au (40 nm) or Ag (30 nm) / Au (30 nm) were deposited using e-beam evaporation under ultrahigh vacuum conditions of approximately ~10^{-7} Torr, followed by a lift-off process.

4.2.2 TEM Observation

For TEM observation, a protective layer of amorphous carbon with a thickness of 10 nm was evaporated on top of the stacks. Subsequently, a focused ion beam lift-out procedure was performed using the FEI Helios 600i Dual Beam FIB-SEM system. Cross-sectional TEM images were obtained using a Cs-corrected TEM (JEOL, JEMARM200F) operating at an acceleration voltage of 80 kV.

4.2.3 Electrical Measurements

All electrical measurements were conducted at room temperature and under a pressure of 10^{-2} Torr using a semiconductor parameter analyzer (Keithley 4200A-SCS). The heavily doped Si substrate served as the global back-gate, and the back-gate voltage (V_{BG}) was applied to modulate the electrical poten tial of the channel layer, such as graphene and MoS_2.

4.3 Result and Discussion

4.3.1 Mechanism of Irreversible Conductive Filaments (ICFs)

Conventional memristors with metal/insulator/metal (MIM) structures create conductive filaments (CFs) through the diffusion of metal ions and vacancies within the insulator at critical bias. These CFs can be reversibly retracted during the reset process by applying a reverse voltage.[98-100] The presence of reversible CFs (RCFs)

is a key characteristic of memristors as described in Figure 21a. In contrast, Figure 21b shows our approach to fabricating irreversible conductive filaments (ICFs) contact with the hBN-encapsulated 2D layer, such as graphene and MoS_2. By inducing defective paths in the hBN through oxygen plasma treatment, permanent conductive paths are formed via the migration of metal ions and vacancies[101,102] Consequently, the CFs generated along these defective paths remain irreversible even during the reset process, leading via contacts to the embedded 2D channel layer.

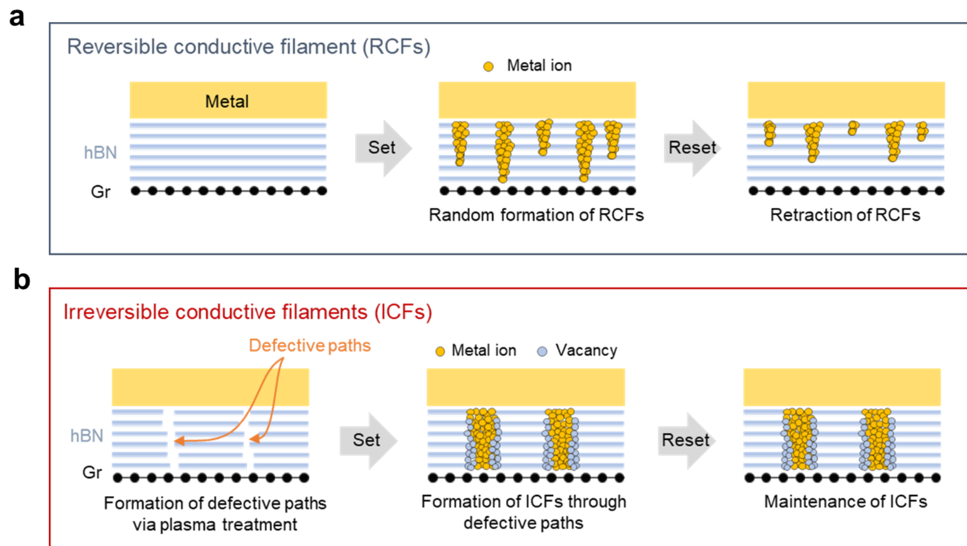


Figure 21. Mechanism of reversible and irreversible conductive filament formation in passivated vdWs heterostructure. a-b Schematics of formation processes for reversible and irreversible conductive filament by electrical switching processes. When the hBN is pristine, the conductive filament in hBN by the electrical set process is reversible. When the hBN has a defective path using plasma treatment, the conductive filament is irreversible.

4.3.2 Device Geometry and Fabrication Processes

Figures 22a and b show the schematic device structure and the optical microscopic image of a representative hBN-encapsulated graphene heterostructure FET with ICF contacts. As shown in the device fabrication process of Figure 22c, the heterostructure of hBN1 (3.2 nm)/Gr (1.1 nm)/hBN2 (5.5 nm) was stacked on a SiO_2 (285nm)/Si substrate using the dry pick-up transfer technique.[53] To fabricate two types of electrodes (ICF and G in Figure 22a), the graphene was partially covered by the top hBN (hBN1). Four electrodes of ICF contacts (ICF1 and ICF2) and conventional top contacts (G1 and G2) were patterned in two regions of hBN1/Gr/hBN2 and Gr/hBN2. For the formation of defective regions in the top hBN, hBN1/Gr/hBN2 region was patterned by e-beam lithography, followed by oxygen plasma treatment and metal deposition for ICF1 and ICF2. By e-beam lithography, metal electrodes of G1 and G2 were fabricated in the Gr/hBN2 region. The same metals of Pd(or Ag, 30 nm))/Au (40 nm) were deposited by e-beam evaporation for all four electrodes with a pre-deposited adhesion metal layer of Cr 1 nm. For the ICF contacts, I used Pd because Pd has been known as a suitable metal for graphene.[103,104]

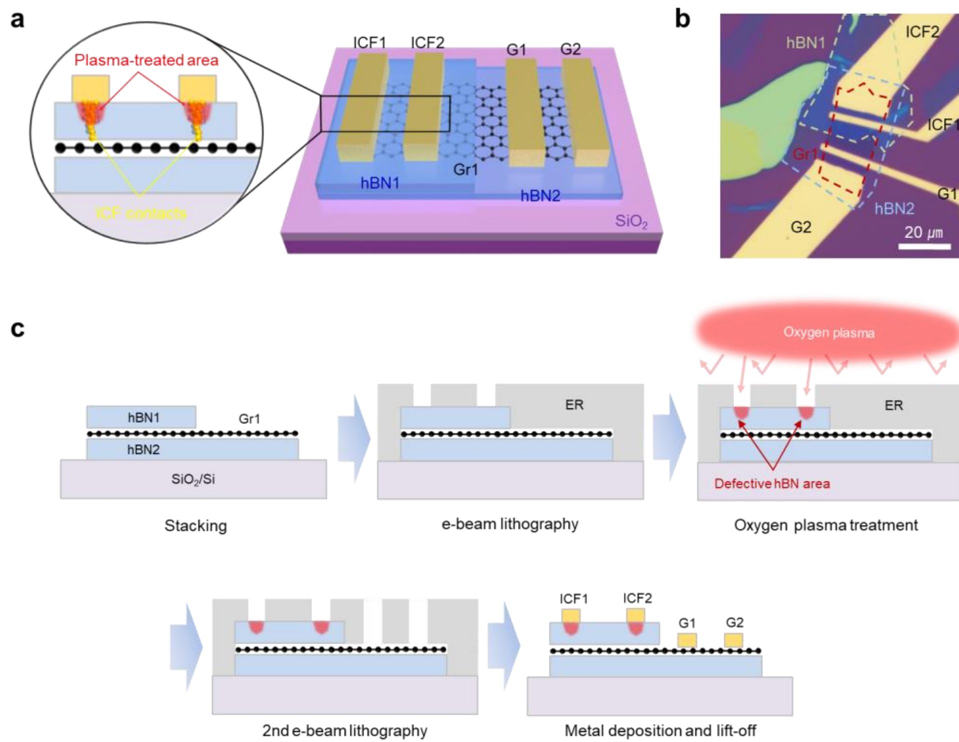


Figure 22. Device geometry and fabrication processes of hBN-encapsulated graphene FET. a Schematic of the vdWs heterostructure of embedded graphene FET with ICF contact. **b** Optical image of a corresponding heterostructure of the fabricated device. **c** Schematics of fabrication processes of the embedded graphene FET with ICF contact.

4.3.3 ICFs Formation using Electrical Processes.

To evaluate the effect of plasma treatment on the generation of ICFs, I compared two types of devices: one with RCFs and the other with ICFs. It is important to note that all measured devices consisted of the Pd for the metal contacts. To form the ICFs, a bias was applied at a fixed gate voltage through a Si back gate using the G and ICF electrodes of Figure 22a. With a positive gate voltage of 60 V, graphene was n-doped, allowing the bias to be applied to the insulating hBN between the metal electrode (ICF) and conductive graphene channel. This resulted in the formation of RCFs or ICFs. When the bias was swept from zero to a negative voltage, the device with untreated hBN exhibited only tunneling behavior in the I-V curve ($I_{G1\text{-}ICF1}$-$V_{G1\text{-}ICF1}$) of Figure 23a, even after the 40th cycle of bias. Meanwhile, the devices with plasma-treated hBN demonstrated a significant increase in current as the forming process of ICFs was repeatedly conducted, as shown in Figure 23b. Following repetitive bias sweeping, the I-V curve ($I_{G1\text{-}ICF1}$-$V_{G1\text{-}ICF1}$) of the plasma-treated device showed low resistance. Figure 23c shows a comparison of the I-V curve between the first and fifth forming processes of the plasma-treated device. It illustrates that oxygen plasma treatment enables the formation of Ohmic-like contacts comprising the CFs.

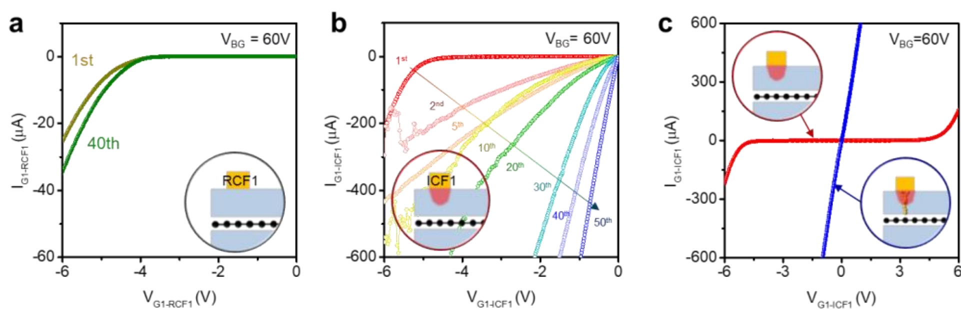


Figure 23. Irreversible conductive filament formation of hBN-encapsulated graphene FET using electrical set processes. a Output curve ($I_{G1\text{-}RCF1}$-$V_{G1\text{-}RCF1}$) of the RCF contact device at fixed V_{BG} of 60 V without plasma treatment. **b** Output curve ($I_{G1\text{-}ICF1}$-$V_{G1\text{-}ICF1}$) of the ICF contact device with multiple sweeps at fixed V_{BG} of 60V to form conductive filaments. **c** Output curve ($I_{G1\text{-}ICF1}$-$V_{G1\text{-}ICF1}$) at fixed V_{BG} of 60V before (red curve) and after (blue curve) forming conductive filament.

4.3.4 Atomic Structure of ICFs

Figure 24a shows a cross-sectional high-resolution transmission electron microscope (HR-TEM) image of the hBN1/Gr/hBN2 heterostructure with Pd ICF contacts. Following oxygen plasma treatment and forming process, the heterostructure exhibits distorted layers of hBN1 and an interface comprising a mixture of Pd and hBN1. However, the layered structure of graphene and hBN2 remains intact. This indicates that only the topmost few layers of hBN are damaged, resulting in the formation of defective paths or CFs within the hBN1, as shown in the magnified HR-TEM image in another region in the hBN1 (See Figure 24b). In contrast, the hBN2 maintains a pristine layered structure (See Figure 24c).

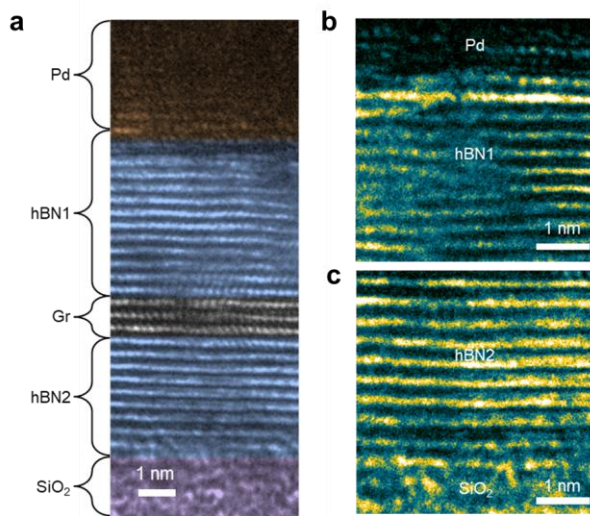


Figure 24. Atomic structure of hBN after forming ICF. a Low-magnification cross-sectional HR-TEM images of embedded graphene FET after forming ICF contact. **b, c** Magnified HR-TEM images of the device.

4.3.5 Irreversibility and Effective ICFs Contact

After the formation of the ICFs within the hBN, I conducted measurements of I-V curves fifty times, as shown in Figure 25a. The I-V curves ($I_{G1\text{-}ICF1}$-$V_{G1\text{-}ICF1}$) of the plasma-treated device with ICFs exhibited no change, indicating the stability and persistence of ICFs throughout several measurements. Figure 25b shows the electrical transport of graphene measured with the ICF contact (ICF1) and graphene contact (G1) without any hysteresis, and exhibited a shifted charge neutrality point at -17 V. These observations are consistent with previous reports on hBN-encapsulated graphene devices.[54,105] The low gate leakage current indicates that there is no leakage in the hBN even after plasma treatment. Furthermore, the output curves ($I_{G1\text{-}ICF1}$-$V_{G1\text{-}ICF1}$) of the graphene device in Figure 25c demonstrated a linear behavior, indicating the formation of effective electrical contact between the metal electrode and graphene through ICFs within the hBN layer.

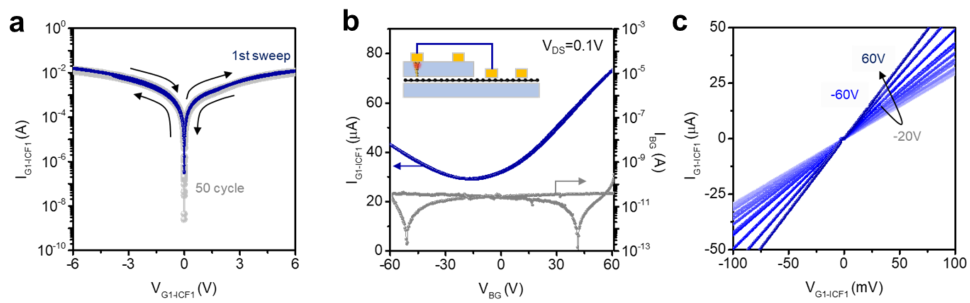


Figure 25. Irreversibility and effective electrical contact between the metal electrode and graphene through ICFs. a Output curve ($I_{G1\text{-}ICF1}$-$V_{G1\text{-}ICF1}$) of repeated 50 cycles after forming process. After forming process, the output curve during the 50 cycles is nearly uniform. **b** Transfer curve ($I_{G1\text{-}ICF1}$-V_{BG}) of the device at fixed V_{DS} of 0.1 V **c** Output curve ($I_{G1\text{-}ICF1}$-$V_{G1\text{-}ICF1}$) of the device varies with V_{BG}

4.3.6 Electrical Characteristics of the FET with ICFs Contact

The hBN-encapsulated graphene device was characterized using ICF1 and ICF2 as shown in Figures 26a and b. The transfer curve ($J_{ICF1\text{-}ICF2}$-V_{BG}) exhibited similarities to that in Figure 25b. Notably, ICF2 contact demonstrated a comparable resistance to the G1 contact, which was fabricated by conventional metal deposition directly onto graphene. Furthermore, no hysteresis was observed in the transfer curve of the hBN-encapsulated graphene device with the ICF contacts. Remarkably, even after a two-week interval, the graphene device with the ICF contacts showed minimal change when measured in Figure 26a, supporting the high stability of ICFs formed within the device. The output curves ($J_{ICF1\text{-}ICF2}$-$V_{ICF1\text{-}ICF2}$) shown in Figure 25b also showed a linear behavior over a broad range of gate voltage (V_{BG}), indicating an Ohmic-like behavior at both ICF contacts. Aside from metal ion migration, the CFs in the defective hBN can also be formed through vacancy migration. It is important to note that the Pd ICF contact has significantly lower resistance compared to the Ag and Gr contacts as shown in Figure 26c. It might be due to the strong interaction between Pd with the graphene, resulting in very low contact resistance.[104,106]

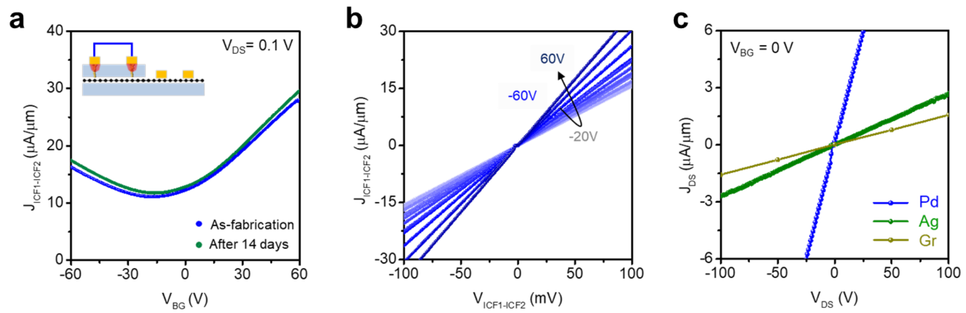


Figure 26. Electrical characteristics of the graphene FET with ICF contact after forming conductive filament. a Transfer curve ($J_{CF1-CF2}$-V_{G2}) of the device at fixed V_{DS} of 0.1V at as-fabrication (blue curve) and after 14 days (green curve). **b** Output curve ($J_{CF1-CF2}$-$V_{CF1-CF2}$) varying with $V_{BG.}$ **c** Output curve ($J_{CF1-CF2}$-$V_{CF1-CF2}$) of the device with ICF contact of Pd metal (green curve), Ag (blue curve), and graphene (red curve).

4.3.7 Universality of ICFs Contact

To examine the universality of ICF contacts for various 2D materials, I fabricated an hBN-encapsulated MoS_2 device as shown in Figure 27a. For this device, I chose Ag for ICFs, because the Ag-MoS_2 contact is known to exhibit effective contact with low contact resistance.[107] Through the same procedure used for the formation of ICFs in the hBN-encapsulated graphene device, I fabricated the ICFs in the hBN-encapsulated 4L MoS_2 device. The I-V curves ($I_{M1\text{-}ICF1}$-$V_{M1\text{-}ICF1}$) of the MoS_2 device demonstrated a gradual change as the bias sweep was repeated, as shown in Figure 27b. Furthermore, when the same MoS_2 channel of Figure 27a was measured by ICF contacts (ICF1 and ICF2) or conventional top contacts (M1 and M2), the hBN-encapsulated MoS_2 device with the ICF contacts showed a higher on/off ratio of ~10^7 and reasonable on-current of 10^{-6} A compared to the conventional MoS_2 device with top contacts, as shown in transfer curves (I_{DS}-V_{BG}) of Figure 27c.[108] The ICF-contacted MoS_2 FET shows the field-effect mobility of 1.11 cm^2/Vs, which is similar to that of the top contacted-MoS_2 FET (1.57 cm^2/Vs). It is worth noting that the top-contacted device is n-doped by adsorbates,[109,110] resulting in a smaller threshold voltage. The contact resistance (R_c) of the ICF contact, extracted by the Y-function method,[111] was 463 kΩ · μm, which is comparable to that of the top-contacted device (49Ωμm).

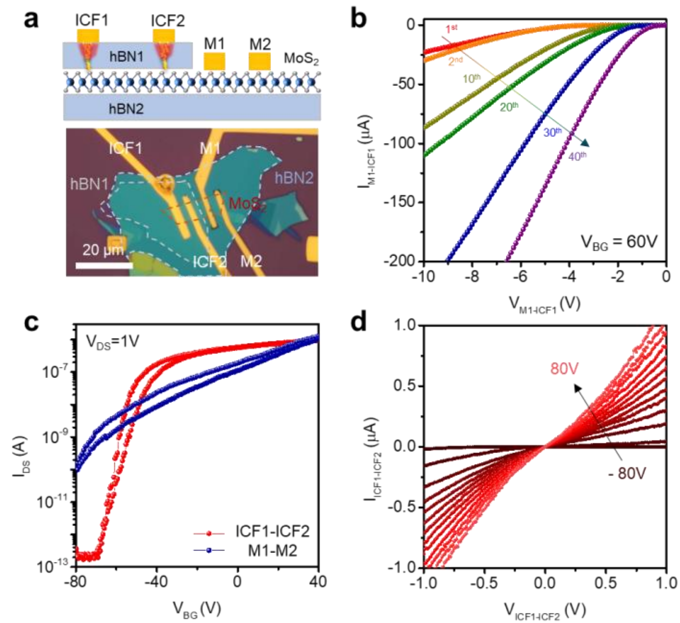


Figure 27. N-type semiconducting transported MoS_2 FET with ICF contact a Schematic of the vdW heterostructure of embedded MoS_2 FET with ICF contact and optical image of a corresponding heterostructure of the fabricated device. **b** Output curve ($I_{M1\text{-}ICF1}$-$V_{M1\text{-}ICF1}$) of the device with multiple sweeps at fixed V_{BG} of 60 V to form conductive filaments. **c** Transfer curve ($I_{M1\text{-}ICF1}$-V_{BG}) at fixed V_{DS} of 1 V. **d** Output curve ($I_{ICF1\text{-}ICF2}$-$V_{ICF1\text{-}ICF2}$) varying with V_{BG}.

4.4 Conclusion

In conclusion, I demonstrated the fabrication technique of the ICFs in passivated 2D devices, enabling the electrical connection of embedded active channels. Through oxygen plasma treatment on hBN, the formation of ICF is achieved with high stability and low resistance, by the migration of metal ions and vacancies along defective paths. Our work presents a new contact method that holds great potential for high-performance 2D electronic devices.

Chapter 5. Conclusion

In conclusion, my research highlights the key factors that contribute to the development of electronic devices based on 2D materials, including van der Waals (vdW) heterostructures, effective electrostatic controllability, and efficient polarity modulation. Van der Waals heterostructures offer a unique and low-energy approach to integrating diverse 2D atomic crystals with different lattice structures. This technique overcomes the limitations of conventional material integration methods and opens new possibilities for fabricating novel concepts and high-performance electronic devices. One notable characteristic of 2D materials is their effective electrostatic controllability. Unlike bulk materials, 2D semiconductors possess excellent gate coupling and reduced scattering of charge carriers due to their ultra-thin body and absence of dangling bonds. This property enables precise control of carrier behavior and results in high on/off ratios, enhancing the overall device performance. Efficient polarity modulation, facilitated by the ambipolar characteristics of 2D materials, enables the realization of reconfigurable field-effect transistors (FETs). These FETs allow for the selection of both p-type and n-type characteristics within a single device through voltage adjustment. This approach offers advantages such as reduced transistor count, flexible circuit design, and enhanced security, surpassing traditional CMOS techniques.

By considering these key factors, this research demonstrates the significant potential of 2D materials for the development of next-generation electronic components. The findings presented include highly efficient light-emitting devices based on 2D materials, reconfigurable memory devices for logic-in-memory

applications, and a novel contact engineering approach. These contributions highlight the innovative performance improvements achievable by leveraging the unique properties and mechanisms of 2D materials.

Chapter 1 provides background information on 2D materials and their characteristics, including van der Waals heterostructures, effective electrostatic controllability, and efficient polarity modulation. The research objectives are introduced, emphasizing the need to leverage these properties for further investigations.

Chapter 2 presents high-efficiency light-emitting devices based on 2D materials, utilizing effective electrostatic controllability to achieve efficient charge injection into the emission region. A highly efficient WSe_2 light-emitting transistor (LET) is introduced, incorporating a van der Waals heterostructure and a graphene contact electrode to confine neutral excitons and achieve strong electroluminescence with a high external quantum efficiency (EQE) of approximately 8.2%.

Chapter 3 focuses on 2D material-based reconfigurable memory devices for logic-in-memory applications, highlighting efficient polarity modulation. Reconfigurable and cascadable two-dimensional floating-gate field-effect transistors (FG-FET) are demonstrated, offering versatile transport behaviors and threshold voltage control. Integrated logic circuits composed of WSe_2 FG-FETs can perform all 16 Boolean logic functions within a single configuration, optimizing energy consumption and enhancing circuit design flexibility.

Chapter 4 addresses the crucial issue of contact engineering in 2D materials. A new approach to forming irreversible conductive filaments (ICF) contacts in passivated

2D channels is proposed, enhancing device stability, and reducing contact resistance. Field-effect transistors (FETs) with ICF contacts exhibit low resistance and high stability, demonstrating the potential of this contact approach for high-performance 2D electronic devices.

In summary, the exploration of van der Waals heterostructures, effective electrostatic controllability, and efficient polarity modulation in 2D materials opens promising possibilities for the future of electronics. Further advancements in this field hold the potential to revolutionize electronic device design, leading to enhanced functionality, energy efficiency, and integration in electronic systems.

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Abstract in Korean

다기능 전자 소자 응용을 위한 재구성과 정전기적 조절 가능한 반데르발스 소자

신준철
공과대학 재료공학부
서울대학교

현재 실리콘 반도체 소자의 스케일링 한계로 인해 새로운 반도체 물질을 찾아야 하는 필요성이 제기되고 있으며, 이에 따라 원자 단위 두께를 가진 2차원 물질이 매우 유망한 후보로 인식되고 있습니다. 그래핀과 전이 금속 칼코겐 화합물로 대표되는 2차원 물질은 새로운 물리적, 전기적, 광학적 특성을 가지며, 이러한 물질들을 결합한 반데르발스 이종구조는 전자 분야에서 새로운 가능성을 제시하고 있습니다. 2차원 물질은 평평한 표면과 높은 전하 이동도를 가지며, 단 채널 효과에도 강한 내성을 보입니다. 그러나 2차원 물질 기반 전자 소자에 대한 연구는 여전히 초기 단계에 머무르고 있으며, 실리콘 기반 소자 기술을 모방하는 수준에 그치고 있습니다. 따라서, 2차원 물질만의 특성을 활용하거나 새로운 메커니즘을 이용하여, 소자의 획기적인 성능 향상을 이루어 내야 합니다. 2차원 물질의 전자소자로서 흥미로운 특성 중 하나는 모든 캐리어가 원자층 두께 내에서 제한되므로, 외부 전기장에 의해 페르미 에너지 레벨이

효과적으로 변조될 수 있고 정전기적 도핑을 추가적인 도핑 기술 없이도 외부 전기장만을 이용하여 반도체 채널 내에 수송되는 캐리어의 극성을 효율적으로 조절할 수 있습니다. 따라서, 2차원 물질의 이러한 고유한 특성을 활용한 새로운 소자 컨셉에 대한 연구가 우선시되어야 합니다.

본 논문은 효과적인 정전기적 제어성과 효율적인 극성 변조성을 이용한 2차원 물질로 이루어진 반데르발스 이종구조 기반의 다기능 전자 소자에 대한 연구를 소개합니다. 연구 내용을 자세히 설명하기 전에, 2차원 물질과 2차원 물질 기반 전자 소자에 대한 배경 정보를 다루고 있으며, 특히 반데르발스 이종구조, 효과적인 정전기적 제어성, 효율적인 극성 변조성과 같은 2차원 물질의 중요한 특성을 강조하여 다루고 있습니다. 또한, 이러한 특성을 활용한 연구의 목표도 본 논문의 2장에서 설명하고 있습니다.

본 논문의 3장에서는 효과적인 정전기적 제어성을 활용한 2차원 물질 기반 고효율 발광 소자를 소개하고 있습니다. 전이 금속 칼코겐 화합물과 같은 2차원 반도체는 direct bandgap과 높은 광학 효율과 같은 우수한 광학 성질을 가지므로, 광전자 소자에 대한 유망한 후보로 알려져 있습니다. 그러나 이전 연구에서 보고된 발광 소자들은 2차원 물질의 특이한 현상을 이용한 기능성에 초점을 맞춰졌으며, 외부 양자 효율은 낮은 수준을 보이고 있습니다. 이러한 낮은 효율을 해결하기 위해, 본 논문에서는 반데르발스 이종구조 기반 고효율 WSe_2 발광 트랜지스터(LET)를 구현하였으며, 이를 통해 WSe_2의 1차원 공핍층 영역에서 전기적으로

구속된 중성 엑시톤이 발광하는 매커니즘을 보고하고 있습니다. WSe_2 LET 소자는 반데르발스 접촉이 가능한 그래핀을 전극으로 사용하여 페르미 레벨 고정 현상을 억제하였으며, 양극성 채널인 WSe_2을 사용하여 정전기적 도핑 제어을 통해 효율적으로 전자와 정공을 발광층 인 WSe_2로 주입시켰습니다. 또한 이중 게이트를 이용하여 채널을 국부적으로 도핑 하면서 동시에 전자와 양공을 1차원 영역에 주입할 수 있습니다. WSe_2 LET는 중성 엑시톤을 1차원 영역에 전기적으로 구속시키는 동시에 전하를 띈 엑시톤 입자인 트라이온들을 도핑 된 영역으로 밀어내어, 중성 엑시톤 입자가 주로 발광 되며, 이러한 과정에서 전자와 양공의 주입 농도가 균형을 이룰 때, 약 8.2%를 높은 발광효율을 나타냄을 확인하였습니다. 이 연구는 2차원 발광 소자의 큰 잠재력을 보여주며, 엑시톤 복합체 기반 발광소자에서 엑시톤 복합체의 재결합을 변조하는 방법을 제시하고 있습니다.

본 논문의 4장에서는 2차원 물질의 효율적인 극성 변조성을 활용하여 차세대 데이터 처리 방식인 논리-인-메모리 컴퓨팅을 위한 2차원 물질 기반 메모리 소자에 대해 보고하고 있습니다. 논리-인-메모리는 효율적인 데이터 처리를 위한 유망한 전자 접근 방식으로 간주되며, 고성능 데이터 처리를 위한 소자의 고직접화는 필수적입니다. 2차원 반도체는 높은 이동성, 짧은 채널 효과의 부재, 그리고 효과적인 정전기 제어 기능으로 인해 논리-인-메모리 컴퓨팅을 위한 고직접화 측면에서 큰 잠재력을 보여주고 있습니다. 본 연구에서는 재구성 가능하고 연속 연결 가

능한 2차원 물질 기반의 플로팅 게이트 필드-효과 트랜지스터(FG-FET)를 소개하여 고직접화된 논리-인-메모리 응용을 구현하였습니다. 단일 게이트만을 이용하여 플로팅 게이트에 갇힌 전하를 변조함으로써, 이 장치는 모든 종류의 전기 전도(n- 및 p-형, 금속, 및 절연체)를 가진 재구성 가능한 전달 특성을 제공하며, 임계전압 제어도 가능합니다. WSe_2 FG-FET로 구성된 논리 회로는 단일 구성에서 16가지 불대수 논리 기능을 모두 수행할 수 있으며, 연속 연결을 사용하여 1비트 전가산기, 감산기, 비교기를 수행할 수 있는 재구성 가능한 마이크로프로세서도 통합되었습니다. 이러한 재구성과 연속 연결 방식을 통해 장치는 회로 설계의 유연성과 기능성을 크게 향상시킬 수 있으며, 논리 합성을 위한 면적 효율적인 솔루션을 제공합니다. 우리의 연구는 처리-인-메모리 분야에서 효율적인 차세대 전자 부품으로서 우리의 메모리의 큰 잠재력을 강조하고 있습니다.

마지막으로, 본 논문의 5장에서는 2차원 물질의 가장 중요한 이슈인 컨택 엔지니어링에 대한 연구를 보고하고 있습니다. 2차원 물질은 외부 조건에 매우 민감하기 때문에, 2D 전자 기기의 안정성을 유지하기 위해서는 2D 소재의 표면을 보호하는 패시베이션 공정이 반드시 필요합니다. 그러나 패시베이션 공정 시, 패시베이션 층으로 감싸진 2D 채널에 금속 접촉을 형성하는 것은 기술적으로 어렵습니다. 본 연구에서는 2차원 절연체인 hBN으로 패시베이션된 2D 채널에 비가역적인 전도 필라멘트 접촉을 형성하는 새로운 컨택 방법을 제안하였습니다. 산소 플라즈마를 이

용하여 hBN 패시베이션된 그래핀 (또는 MoS_2)의 상부 hBN에서 의도적으로 결함 경로를 형성한 후 반복적으로 바이어스를 적용하여 비가역적 전도 필라멘트를 결함 경로를 따라 형성하여 2D 채널 층에 컨택을 형성하였습니다. 금속 원자와 결함의 이동을 통한 필라멘트 형성으로 생성된 비가역적 전도 필라멘트 접촉은 장치 작동 중 안정적으로 유지되며, 이는 멤리스터에서 보이는 가역적 필라멘트와는 달리 비가역적이므로 안정적인 컨택 형성을 보입니다. 따라서 이러한 비가역적 전도 필라멘트 접촉을 가진 전계 효과 트랜지스터 (FET)를 구현한 결과, 낮은 접촉 저항과 높은 안정성을 보였습니다. 따라서 이 연구는 고성능 2D 전자 기기에 큰 잠재력을 가지는 새로운 접촉 방법을 보여줍니다.

핵심어: 재구성성, 극성 변조, 전기적 제어성, 다기능 반데르발스 소자, 2차원 재료

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서울대학교
카피킬러캠퍼스 표절 검사
결과 확인서

확 인
성 명
서 명

아이디	semiron1@snu.ac.kr	표절률	3%
소속	재료공학부		
성명	신준철		

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비교범위	[현재첨부문서] [카피킬러 DB]
검사설정	표절기준 [6 어절], 인용/출처 표시문장 [제외], 법령/성전 포함문장 [제외], 목차/참고문헌 [제외]

검토 의견	