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Study on fabrication of metal-ferroelectric-insulator-semiconductor (MFIS) device with doped-HfO_2 film and its operation mechanism

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Abstract

Since the first discovery of ferroelectricy in doped-HfO_2 materials, extensive research has been in underway for their application in semiconductor-based memory devices. The advantageous properties of a large bandgap and excellent compatibility with Si have broadened the range of their potential uses to high-performance complementary metal-oxide-semiconductor (CMOS) devices. Meanwhile, the complex and nonlinear charge behaviors in semiconductors have hindered a comprehensive understanding of ferroelectric (FE) switching mechanism in metal-ferroelectric-insulator-semiconductor (MFIS) structures. The formation of a SiO_2 interface layer between the FE material and the Si substrate is unavoidable, resulting in charge injection and disruption of FE bound charge screening. As a result, issues such as retention failure, fatigue in FE switching and a reduced memory window (MW) may arise to seriously degrade the functionality of the memory devices.

This thesis provides an overview of the general FE switching mechanism in MFIS structures and proposes a promising solution to address the associated issues that diminish the characteristics of MW. First, the optimal thickness of doped-HfO_2 materials is evaluated, taking into account the different voltage distribution behavior in MFIS structures. The serially-connected interface and depletion layers require a thicker film to achieve optimal FE switching due to the capacitance effect. The relationship between the carrier concentration in the

semiconductor and FE switching is also investigated to gain a deeper understanding of the compensation of FE bound charges in lightly-doped and highly-doped Si structures.

Second, various MFIS structures are fabricated and utilized to induce FE switching and assess the properties of MW in lightly-doped Si structures. Despite achieving sufficient voltage distribution across the FE layer and the presence of inversion charges in the semiconductor, the interface layer disrupts the screening of FE bound charges, resulting in incomplete FE switching and a significant depolarizing field that tends to reverse the switched polarization. Nonetheless, it is observed that reducing the thickness of the interface layer leads to complete FE switching and an MW characterized by switching-induced capacitance hysteresis.

Third, based on the observed significance of the interface layer, an oxygen-scavenging process is employed to induce structural decomposition of the SiO_2 interface layer in MFIS structures. By inserting Ti, a material with high oxygen solubility, into the top electrode and subjecting it to a high post-annealing condition, the Si and O_2 components in the interface layer decompose, which allows for the scavenging and transportation of oxygen to Ti for oxidation. Consequently, the thickness and trap density of the interface layer are reduced to enhance the FE switching and retention properties. It is anticipated that these advancements will ultimately contribute to optimizing the characteristics of MW in MFIS memory devices.

Keywords: CMOS, ferroelectric switching, MFIS, memory window, carrier concentration, inversion charges

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List of Abbreviations

AC	Alternating Current
ALD	Atomic Layer Deposition
AO	Al_2O_3
APM	Ammonium Peroxide
C_{acc}	Accumulation Capacitance
C_{eq}	Equivalent Capacitance
CET	Capacitance Equivalent Thickness
C_{HAO}	Capacitance of Al-doped HfO_2
C_{HZO}	Capacitance of Zr-doped HfO_2
CMOS	Complementary Metal-Oxide-Semiconductor
C-V	Capacitance-Voltage
D_{avg}	Average Grain Size
DC	Direct Current
D_{it}	Interface Trap Density
E_c	Coercive Field
EDS	Energy-Dispersive X-ray Spectroscopy
ϵ_0	Vacuum Permittivity
ϵ_{SiO_2}	Dielectric Constant of SiO_2
FE	Ferroelectric
FeFET	Ferroelectric Field-Effect-Transistor
FeMOSCAP	Ferroelectric Metal-Oxide-Semiconductor Capacitor
GIXRD	Grazing Incidence X-ray Diffraction
HAO	Al-doped HfO_2
HF	Hydrofluoric Acid

HPM	Hydrochloric Peroxide
HRTEM	High Resolution Transmission Electron Microscopy
HZAHZ	Al_2O_3-inserted Zr-doped HfO_2
HZO	Zr-doped HfO_2
I-V	Current-Voltage
MFISFET	Metal-Ferroelectric-Insulator-Semiconductor FET
MFM	Metal-Ferroelectric-Metal
MFMIS	Metal-Ferroelectric-Metal-Insulator-Semiconductor
MFS	Metal-Ferroelectric-Semiconductor
MFSFET	Metal-Ferroelectric-Semiconductor FET
MIS	Metal-Insulator-Semiconductor
MOSCAP	Metal-Oxide-Semiconductor Capacitor
MW	Memory Window
N_a	Doping Concentration of Acceptor
P	Polarization
PDA	Post-Deposition Annealing
PMA	Post-Metallization Annealing
P_r	Remanent Polarization
PUND	Positive-Up-Negative-Down
P-V	Polarization-Voltage
RF	Radio Frequency
S/D	Source / Drain
SEM	Scanning Electron Microscopy
SPM	Sulfuric Acid Peroxide
TE	Top Electrode
TEMAH	Tetrakis-ethylmethylaminohafnium
TMA	Trimethylaluminum

V_{appl}	Applied Voltage
V_c	Coercive Voltage
V_F	Ferroelectric Voltage
V_{FB}	Flat Band Voltage
V_G	Gate Voltage
V_N	Node Voltage
V_o	Oxygen Vacancy
w	Depletion Width
XPS	X-ray Photoelectron Spectroscopy

1. Introduction

1.1. Study Background

Doped-HfO_2 ferroelectric materials, with a relatively large bandgap and superior Si-compatibility, have been widely utilized in high-performance complementary metal-oxide-semiconductor (CMOS) memory devices.[1-5] However, the intricate and nonlinear charge behaviors exhibited by semiconductors have impeded a comprehensive understanding of the ferroelectric (FE) switching mechanism in metal-ferroelectric-insulator-semiconductor (MFIS) structures.[6-7] The formation of a SiO_2 interface layer between the FE material and the Si substrate is an unavoidable consequence, resulting in charge injection and disruption of the screening of FE bound charges. Depolarizing field induced by the under-compensation of the FE bound charges tends reverse the switched polarization after an applied gate voltage is removed.[8] Consequently, significant issues such as retention failure, fatigue in FE switching, and a reduction in the memory window (MW) may arise, severely compromising the functionality of memory devices.

1.2. Purpose of Research

The objective of the present thesis is to profoundly analyze the switching mechanism in semiconductor-based capacitors with doped-HfO_2 ferroelectric materials. This leads to the comprehension of probable limitations of memory operation in semiconductor-based ferroelectric memory devices, which may contribute to optimizing the characteristics of MW.

Chapter 2 investigates the general dependence of the film thickness of doped-HfO_2 ferroelectric materials on their switching operation in MFIS structures. Compared to the typical metal-ferroelectric-metal (MFM) structure, in which the screening of ferroelectric bound charges is not hindered by an interfacial layer, the serial capacitance effect of an inevitably formed interfacial oxide layer in the MFIS structure leads to less voltage distribution at the ferroelectric film for switching. Moreover, depletion operation by semiconductor also induces voltage distribution at the depletion layer prior to ferroelectric switching, which requires a larger thickness of film for optimal ferroelectric switching. Switching mechanism based on different doping concentrations of Si substrate is also examined to understand the dependence of carrier concentration on ferroelectric switching. It has been observed that highly-doped Si substrates can be used as metallic electrodes with sufficient majority carriers and, consequently, space charges in opposite polarity for bi-polar switching. Meanwhile, lightly-doped Si substrates do not possess sufficient majority

carriers, which also leads to a large depletion layer with insufficient space charges in opposite polarity for bi-polar switching.

Chapter 3 evaluates the MW characteristics of various metal-ferroelectric-metal-insulator-semiconductor (MFMIS) and MFIS structures with lightly-doped Si substrate. As ferroelectric field-effect-transistor (FeFET) memory devices operate with the formation of a minority carrier channel from source and drain in lightly-doped Si substrate, various structures of MFMIS and MFIS capacitors are fabricated to examine the MW characteristics induced by ferroelectric switching in lightly-doped Si substrate. A configuration of serially-connected MFM and metal-insulator-semiconductor (MIS) capacitors is utilized to evaluate MW by shifts of the surface potential in the MIS capacitor with inversion operation. MFMIS structures with different area ratios of MFM and MIS stacks are fabricated to induce the larger ferroelectric voltage for switching, and only uni-polar switching is observed at the accumulation condition. This highlights the significance of inversion charges in semiconductor, which contribute more to the screening of ferroelectric bound charges for switching than the larger field induced at the ferroelectric layer. MIS capacitors with a 5 nm-Al_2O_3 insulator deposited on lightly-doped n-type Si substrate are post-annealed at various temperature conditions to form static dipoles which induce the inversion in semiconductor. MFIS capacitors with the doped-HfO_2 films presented considerable polarization switching by the dipole-induced inversion operation in semiconductor, but a significant back-switching

of the switched polarization by the depolarizing field is also observed. Accordingly, the conventional capacitance-voltage (C-V) measurement of the MFIS capacitors exhibit capacitance hysteresis in trap-induced direction and MW characteristics that are not in consistent with the coercive voltages for switching.[9] The dependence of the Al_2O_3 insulator thickness is evaluated by reducing the thickness from 5 nm to 1.5 nm, and symmetric bi-polar switching behavior is depicted and the back-switching by the depolarizing field is notably reduced to present MW by switching-induced capacitance hysteresis.

Based on the demonstrated significance of interface layer reduction for enhanced MW, Chapter 4 describes the oxygen-scavenging effect induced by adding Ti, with high oxygen solubility, in top electrode followed by high temperature post-metallization annealing for crystallization of Al-doped HfO_2 (HAO) ferroelectric film. The Ti scavenging layer triggers structural decomposition of the interface SiO_2 layer, and the oxygen vacancies which migrated from the bulk of HfO_2 layer to the interface transport the scavenged oxygen to the scavenging layer for oxidation.[10-11] The effect of interface decomposition is verified by the reduction of capacitance equivalent thickness (CET) from C-V analysis and structural images from high resolution transmission electron microscopy (HRTEM). Consequently, MFIS capacitor with the reduced interface layer by the oxygen-scavenging effect exhibits the enhanced ferroelectric switching operation along with more stable endurance characteristics without polarization degradation by fatigue phenomenon.[12]

As the reduction of the interface layer and sufficient ferroelectric bound charges have been examined to be significant parameters for MW, it is expected that the oxygen-scavenging effect can be extensively utilized to further optimize the MW characteristics of semiconductor-based ferroelectric memory devices.

Finally, the conclusion of the thesis is made in Chapter 5.

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2. Switching Mechanism in Semiconductor-based Ferroelectric Capacitor

2.1. Introduction

This chapter investigates the relationship between the film thickness of doped-HfO_2 ferroelectric materials and their switching behavior in metal-ferroelectric-insulator-semiconductor (MFIS) structures. A comparison is made with the typical metal-ferroelectric-metal (MFM) structure, where the screening of ferroelectric bound charges is not affected by an interfacial layer. In the MFIS structure, the serial capacitance effect caused by the presence of an interfacial oxide layer hampers the voltage distribution at the ferroelectric film during switching.[1-5] Additionally, the depletion operation in the semiconductor results in voltage distribution at the depletion layer before ferroelectric switching, necessitating a thicker film for optimal ferroelectric switching.[6-9]

The switching mechanism is also examined in relation to different doping concentrations of the Si substrate, aiming to understand the influence of carrier concentration on ferroelectric switching. It is observed that highly-doped Si substrates can function as metallic electrodes with sufficient majority carriers,

allowing for the presence of space charges in the opposite polarity required for bi-polar switching.[10-12] On the other hand, lightly-doped Si substrates lack sufficient majority carriers, leading to the formation of a large depletion layer with insufficient space charges in the opposite polarity necessary for bi-polar switching.[13-15]

2.2. Experimental

Figure 2-1 presents the schematic and fabrication flow of MFS capacitor with Zr-doped HfO_2 (HZO) film. To investigate the FE switching operation of doped-HfO_2 ferroelectric materials in semiconductor-based capacitors, highly-doped Si substrate is used as a metallic bottom electrode in MFS structure. P-type Si substrate with doping concentration of approximately 10^{20} cm^{-3} and resistivity less than 0.005 Ω·cm is first cleaned by HF solution to remove the native oxide. 10 nm-, 20 nm- and 30 nm-HZO films are deposited by atomic layer deposition (ALD) with HfO_2:ZrO_2 ratio of 5:5. A metal shadow mask is attached on the sample to sputter circular top electrode of TiN/Pt. Finally, post-meallization annealing (PMA) is performed at 450 °C for 30 s for crystallization of the deposited films.

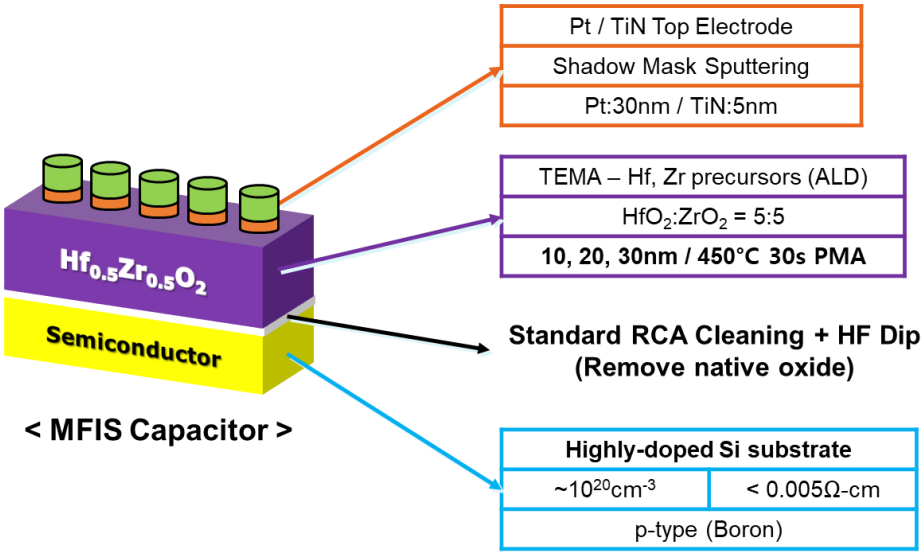

Figure 2-1. Schematic and fabrication process of HZO-based MFS capacitor.

2.3. Results and Discussions

Figure 2-2 shows the polarization hysteresis characteristic of MFS capacitors with HZO deposited at different thicknesses. Similar to the MFM structure, as the thickness increases, E_c decreases. However, in contrast to the MFM structure where the highest ferroelectricity was observed at a thickness of 10 nm, the MFIS structure exhibited a different trend. In the MFIS structure, the $2P_r$ increased further at a thickness of 20 nm and then decreased again at 30 nm. When examining the switching current characteristic at the 10 nm condition, unlike other thicknesses, there was not a peak in the switching current near E_c. Instead, it showed a switching current characteristic with significant leakage current due to a leaky dielectric. Comparing it with the MFM characteristic of the same HZO thickness of 10 nm, it can be observed that $2P_r$ of MFIS is smaller, and E_c is higher. The reason for this trend will be explained in more detail in the subsequent discussion.

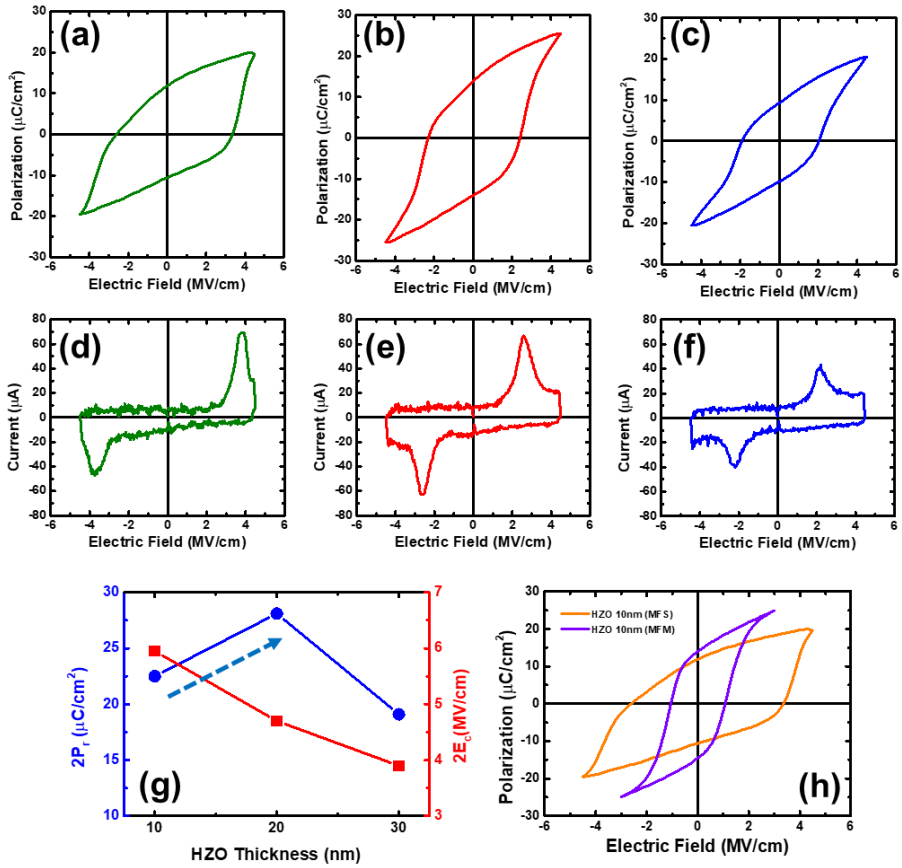

Figure 2-2. Polarization hysteresis of MFS capacitors (highly-doped p-type Si) with (a) 10 nm-, (b) 20 nm-, and (c) 30 nm-HZO films. Current-voltage (I-V) characteristics of MFS capacitors with (d) 10 nm-, (e) 20 nm-, and (f) 30 nm-HZO films. (g) Plot of 2Pr and 2Ec for different thicknesses of HZO film. (h) Polarization hysteresis of MFS and MFM capacitors with 10 nm-HZO film.

As shown in Figure 2-3, it is examined whether the observed variation in ferroelectricity depending on the thickness is influenced by the o-phase ratio due to grain size growth, as in the previous MFM case, using SEM images and XRD measurements. In the MFIS structure, the film thickness corresponding to the critical grain size was higher, around 20 nm, compared to the proximity to 10 nm in the MFM structure. However, the decrease in the o-phase ratio with increasing thickness was even more pronounced in the MFIS structure compared to the MFM case. At the thickness of 20 nm, corresponding to the critical grain size, the o-phase ratio was almost at the level of 0.5. In the MFIS structure, similar to MFM, the o-phase ratio was highest when the film thickness was 10 nm, and it decreased significantly as the thickness increased to 20 nm. However, a different interpretation was needed to explain why the $2P_r$ was highest at a thickness of 20 nm.

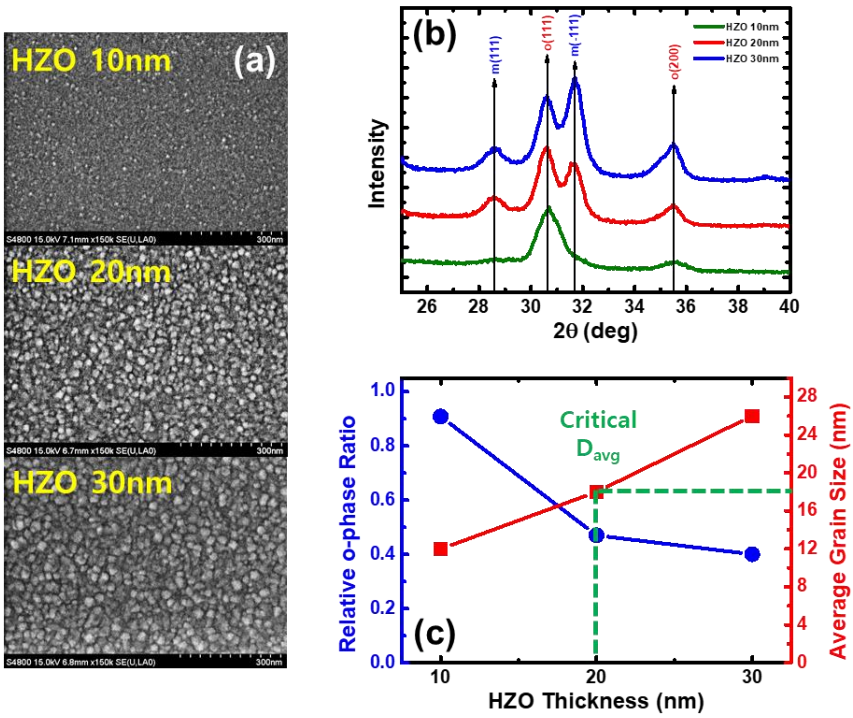

Figure 2-3. (a) SEM images of 10 nm-, 20 nm, and 30 nm-HZO films for average grain size measurement. (b) GIXRD measurements of 10 nm-, 20 nm-, and 30 nm-HZO films after PMA for polar orthorhombic phase (o-phase) ratio calculation. (c) Plot of relative o-phase ratio and average grain size for different thicknesses of HZO film.

The reason why $2P_r$ is higher at a thickness of 20 nm compared to 10 nm in the semiconductor structure can be attributed to the depletion region in the semiconductor and the capacitance component of the interface layer present at the interface. In the MFIS structure, the depletion region is encountered before the voltage reaches V_c. During this stage, the depletion region has a capacitance component based on the depletion width and area. Additionally, an interface layer of oxide film is inevitably formed between the ferroelectric film and the semiconductor due to thermal processes. As a result, a structure is formed where these capacitance components are connected in series. When the thickness of HZO is small, such as 10 nm, the background dielectric capacitance of HZO is large. Consequently, the voltage across HZO is less. However, when the thickness of HZO increases to 20 nm, the capacitance decreases, resulting in a higher voltage across HZO. In reality, assuming the Si substrate is sufficiently highly doped, resulting in a very small depletion width, and the thickness of the SiO_2 oxide film is 1 nm, the voltage applied to each thickness of HZO can be calculated as shown in Table 2-1. When applying 4.5 V to 10 nm of HZO, the voltage ratio across HZO is 0.2. This means that only 0.9 V is applied to HZO, which is lower than the V_c of 1.1 V, making it difficult to achieve full switching. On the other hand, when applying 9 V to a thickness of 20 nm, a voltage of about 3 V, which is greater than the V_c of 2.2 V, can be applied, allowing for full switching. Therefore, in the absence of the interface layer and depletion capacitance components in the MFM structure, full switching can be induced

at a thickness of 10 nm. However, in the MFIS structure, insufficient voltage is applied to HZO due to the presence of other interface layers and voltages applied to the semiconductor, resulting in a leaky switching characteristic.

	MFS			MFM
HZO Thickness (nm)	V_{appl} (V)	C_{eq} / C_{HZO}	V_{HZO} (V)	V_C (V)
10	4.5	0.2	0.9	1.1
20	9	0.33	3	2.2

Table 2-1. Coercive voltages and applied voltage distribution at 10 nm- and 20 nm-thick HZO ferrolectric layers when the thickness of interface layer is 1 nm and that of the depletion layer is 12.5 nm in highly-doped Si substrate.

The depletion behavior in the semiconductor has an influence on switching, and an important factor in forming this depletion region is the doping concentration of the semiconductor. The reason why the switching was smooth when using a highly doped p-type substrate is that the doping concentration of holes is sufficiently high, and when those holes are depleted, there are enough negatively charged spaces of the opposite type left in their place, allowing for switching in both directions. As shown by the simulation result in Figure 2-4, when the acceptor doping concentration is high enough at 10^{21} cm^{-3} and a positive voltage of 6 V is applied to induce the depletion state, the depletion width, where the holes are completely pushed toward the bulk region, is only 12.5 nm. If it is considered that the amount of negative charge left is proportional to the concentration of pushed-out holes, the polarization is around 200 $\mu C/cm^2$, which is sufficient to induce switching in the opposite direction. Therefore, by using a highly-doped substrate, it is observed that switching occurs similar to the MFM structure. The reason why the E_c of the MFIS structure becomes larger than that of the MFM structure is due to the necessary voltage for depletion behavior and the voltage drop that inevitably occurs at the interface layer.

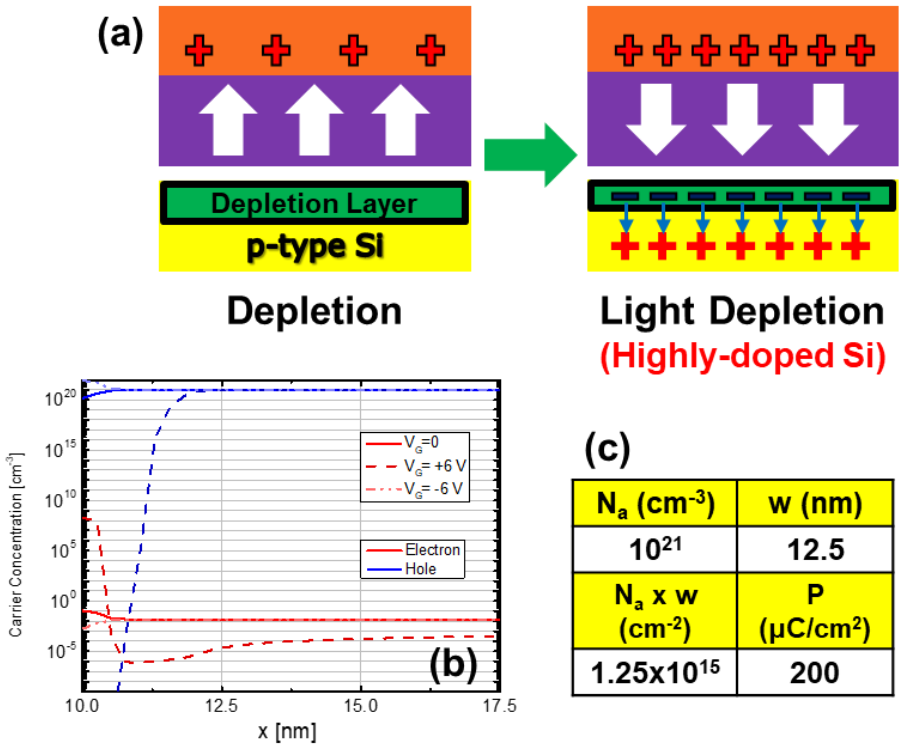

Figure 2-4. (a) Light depletion operation in MFS capacitor with highly-doped Si substrate. Sufficient negative space charges formed by depletion of accumulated holes induce ferroelectric switching. (b) Simulated carrier concentrations of electron and hole at accumulation and depletion conditions. (c) Calculated acceptor concentration, depletion width, and polarization at depletion condition.

Figure 2-5 shows the polarization hysteresis of HZO-based MFIS capacitors with different thicknesses of SiO_2 interface layer. It can be seen that both positive and negative V_c values are increased as the thicker SiO_2 interface layer is present between HZO and the substrate. This refers to the occurrence of charge injection through the interface layer. Holes accumulated by the applied negative bias are injected during negative switching, and electrons from the bulk of Si are injected through both depletion and interface layers by the applied positive bias. This leads to the changes of positive V_c, which is larger than its corresponding negative V_c for all thicknesses of the SiO_2 interface layer.

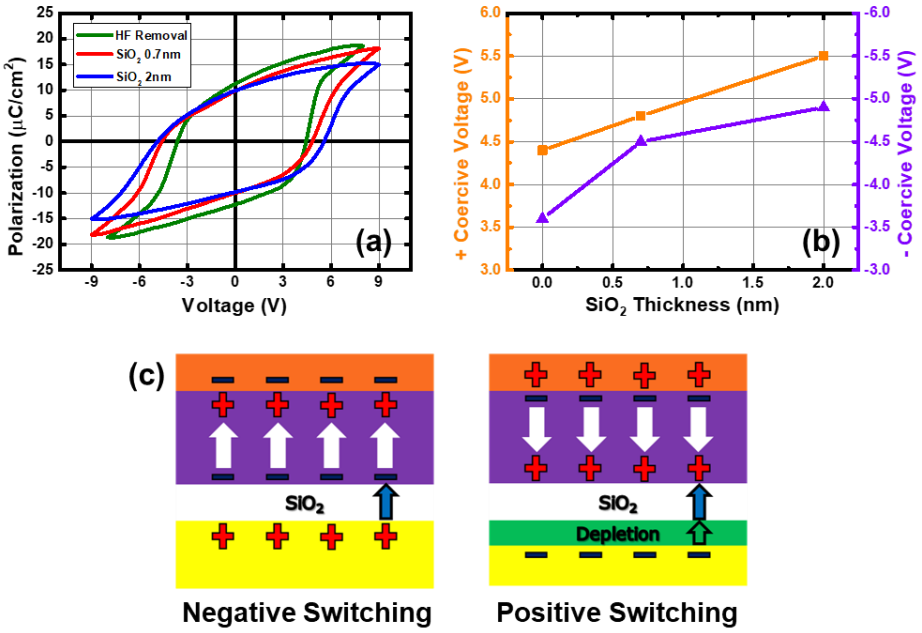

Figure 2-5. (a) Polarization hysteresis of 20 nm-HZO MFIS capacitors with interface SiO_2 layers at thickness of 2 nm, 0.7 nm, and removed by HF cleaning. (b) Plot of positive and negative coercive voltages at different interface SiO_2 layer thicknesses. (c) Schematics of hole injection through SiO_2 during negative switching and electron injection through both depletion and SiO_2 layers during positive switching.

On the other hand, when a lightly-doped substrate is used, the number of holes that can be pushed out during the depletion state is initially low, resulting in a larger depletion width. Consequently, there are very few holes left after depletion, leading to an insufficient amount of negative space charge, which prevents switching from occurring. As shown by the simulation result with an acceptor doping concentration of 10^{14} cm^{-3} in Figure 2-6, it is observed that the depletion width, where the holes are completely pushed away, is much larger at 9 μm. As a result, the amount of negative space charge is close to zero. In reality, when using a lightly-doped substrate to deposit HZO in the MFIS capacitor, a phenomenon called deep depletion occurs with a continuous increase in the depletion region. As a result, the depletion capacitance becomes extremely small leading to no saturated polarization. In the accumulation region, although the capacitance increases as the holes accumulate, there is a decrease in polarization due to the same background dielectric capacitance component rather than HZO switching. The hysteresis direction of the capacitance, resulting from these characteristics, can serve as an important indicator for understanding the ferroelectric switching or trap effects induced by charge injection.

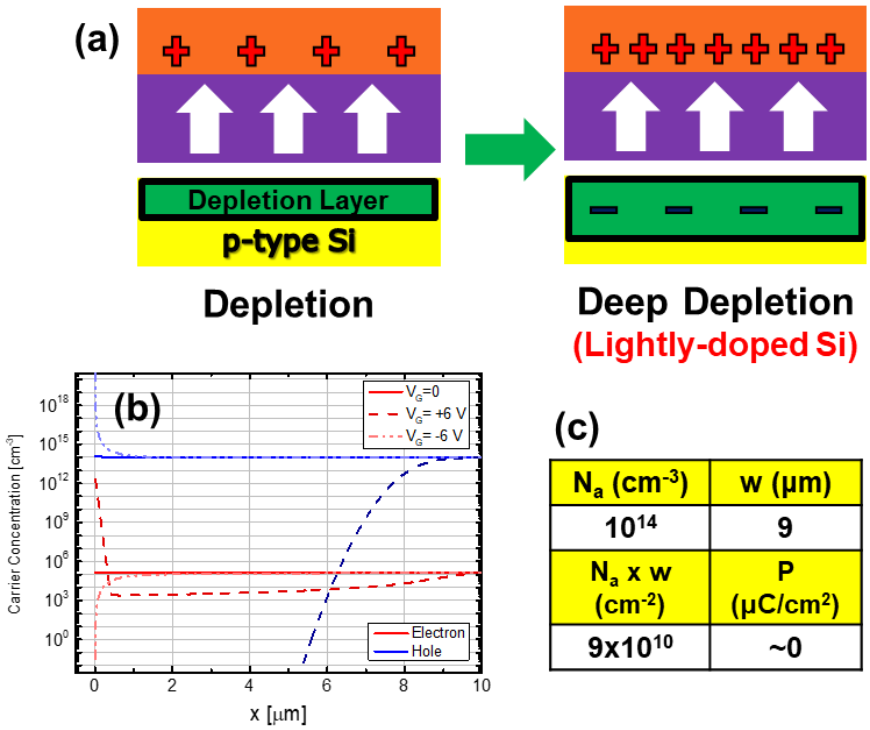

Figure 2-6. (a) Deep depletion operation in MFS capacitor with lightly-doped Si substrate. Insufficient negative space charges formed by depletion of accumulated holes induce no ferroelectric switching. (b) Simulated carrier concentrations of electron and hole at accumulation and depletion conditions. (c) Calculated acceptor concentration, depletion width, and polarization at depletion condition.

The hysteresis of the capacitance observed when sweeping the voltage in both directions is determined by the direction in which it shifts relative to the flat band voltage of an ideal MOSCAP without hysteresis. In the case where FE switching is involved, the voltage required for switching in each direction is added to the flat band voltage. This causes the flat band voltage to shift in the same direction as the sweep direction, based on the reference of the original flat band voltage. Therefore, when switching is involved, a clockwise hysteresis is observed with respect to the p-type substrate. On the other hand, the hysteresis caused by the injected charge at the interface appears in the opposite direction. This is because, under a negative voltage, the accumulation of holes in the semiconductor flows into the interface, creating favorable conditions for depletion to occur at a lower voltage. As a result, the flat band voltage shifts in the opposite direction of the sweep. Conversely, when electrons are injected into the interface under a positive voltage, the depletion where the opposite type of holes is pushed away becomes a more unfavorable condition. Therefore, the flat band voltage also shifts in the opposite direction of the sweep, resulting in an overall counterclockwise hysteresis. However, it should be noted that the remaining static negative space charge in the depletion state cannot flow into the interface. Therefore, in this case, the shift caused by hole injection is expected to be dominant.

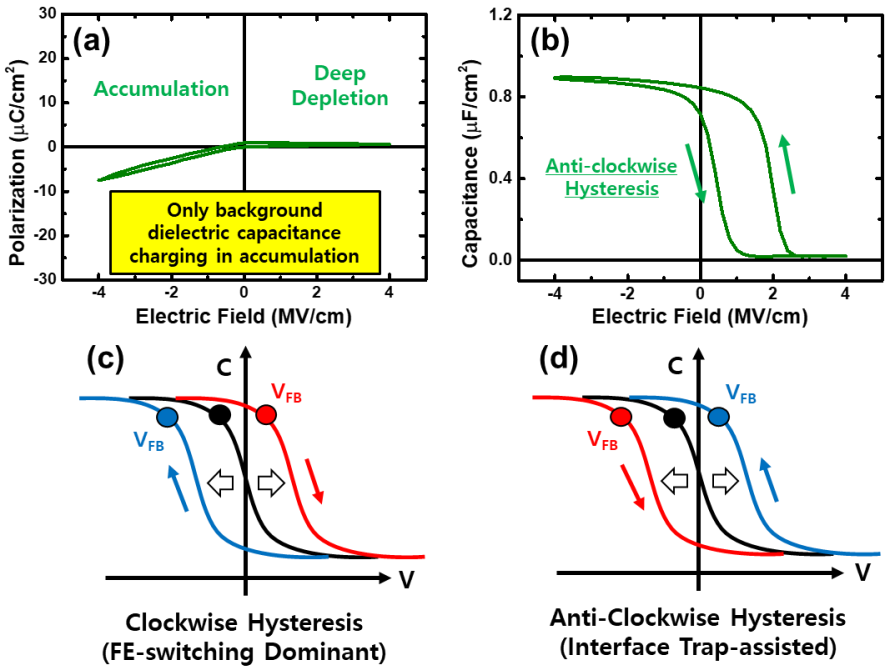

Figure 2-7. (a) Polarization characteristics of 20 nm-HZO MFS capacitor with lightly-doped Si substrate. No ferroelectric switching occurs at deep depletion condition and only background dielectric capacitance charge is observed at accumulation condition. (b) Trap-induced capacitance hysteresis of 20 nm-HZO MFS capacitor with lightly-doped Si substrate. Flat-band voltage shifts by dominance of (c) switching and (d) interface trap for opposite capacitance hysteresis directions.

2.4. Conclusion

In this chapter, it was investigated how the film thickness of doped-HfO_2 ferroelectric materials affects their switching behavior in metal-ferroelectric-insulator-semiconductor (MFIS) structures. A comparison is made with the more typical metal-ferroelectric-metal (MFM) structure, where the screening of ferroelectric bound charges is not influenced by an interfacial layer. In the MFIS structure, the presence of an interfacial oxide layer introduces a serial capacitance effect, which hinders the voltage distribution across the ferroelectric film during switching. Additionally, the depletion operation in the semiconductor causes voltage distribution at the depletion layer before the onset of ferroelectric switching. As a result, 20 nm is a more suitable thickness for optimal ferroelectric switching in the MFIS structure rather than 10 nm as in the case of the MFM structure. The switching mechanism is also examined in relation to different doping concentrations of the Si substrate, with the aim of understanding the impact of carrier concentration on ferroelectric switching. It is observed that highly-doped Si substrates can function as metallic electrodes due to the presence of sufficient majority carriers. This allows for the presence of enough space charges with the opposite polarity required for bi-polar switching. On the other hand, lightly-doped Si substrates lack a sufficient number of majority carriers, resulting in the formation of a large depletion layer. Thus, the space charges in the opposite polarity are insufficient for bi-polar switching to occur effectively.

2.5. Bibliography

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3. Analysis on Memory Window in MFMIS and MFIS Ferroelectric Capacitor

3.1. Introduction

This chapter focuses on evaluating the characteristics of memory window (MW) in different metal-ferroelectric-metal-insulator-semiconductor (MFMIS) and metal-ferroelectric-insulator-semiconductor (MFIS) structures with lightly-doped Si substrates. The study aims to examine the MW characteristics induced by ferroelectric switching in these structures, considering their relevance to ferroelectric field-effect-transistor (FeFET) memory devices, which operate by forming a minority carrier channel from the source and drain in lightly-doped Si substrates.[1-4] A serially-connected configuration of MFM and metal-insulator-semiconductor (MIS) capacitors is utilized to evaluate MW by measuring shifts in the surface potential of the MIS capacitor during inversion operation.[5-6] MFMIS structures with different area ratios of MFM and MIS stacks are fabricated to induce a larger ferroelectric voltage for switching, and only uni-polar switching is observed under accumulation conditions. This highlights the importance of inversion charges in the semiconductor, as they contribute more to the screening of ferroelectric bound charges for switching compared to the larger field induced at the ferroelectric layer. [7-9] MIS capacitors, with a 5 nm-thick Al_2O_3 insulator deposited on

lightly-doped n-type Si substrates, are subjected to post-annealing at various temperature conditions to form static dipoles that induce inversion in the semiconductor.[10] MFIS capacitors with Zr-doped HfO_2 (HZO) and Al-doped HfO_2 (HAO) films demonstrate significant polarization switching through the dipole-induced inversion operation in the semiconductor. However, a notable back-switching of the switched polarization induced by the depolarizing field is also observed.[11-13] As a result, conventional capacitance-voltage (C-V) measurements of the MFIS capacitors exhibit capacitance hysteresis in the trap-induced direction and MW characteristics that do not align with the coercive voltages for switching.[14-17] Accordingly, the thickness of the Al_2O_3 insulator is reduced to experimentally verify its dependence on the MW properties, and a difference between the quasi-static and conventional C-V analysis is also discussed.

3.2. Experimental

The first type of structure used in the experiment is a configuration of serially-connected MFM and MIS capacitors as shown in Figure 3-1. It is verified that the MIS capacitor used in the configuration operates well in both accumulation and inversion mode by its capacitance measurement. As shown in Figure 3-5, it is also experimentally observed that sufficient voltage is dropped at the MFM capacitor for ferroelectric switching when the MIS capacitor with inversion operation is connected whereas insufficient voltage drop leads to no ferroelectric switching when a MIS capacitor with no inversion (deep depletion) operation is connected. Node voltages in the serially-connected configuration are measured by an applied pulse to evaluate the voltages dropped at the MFM and MIS capacitors.

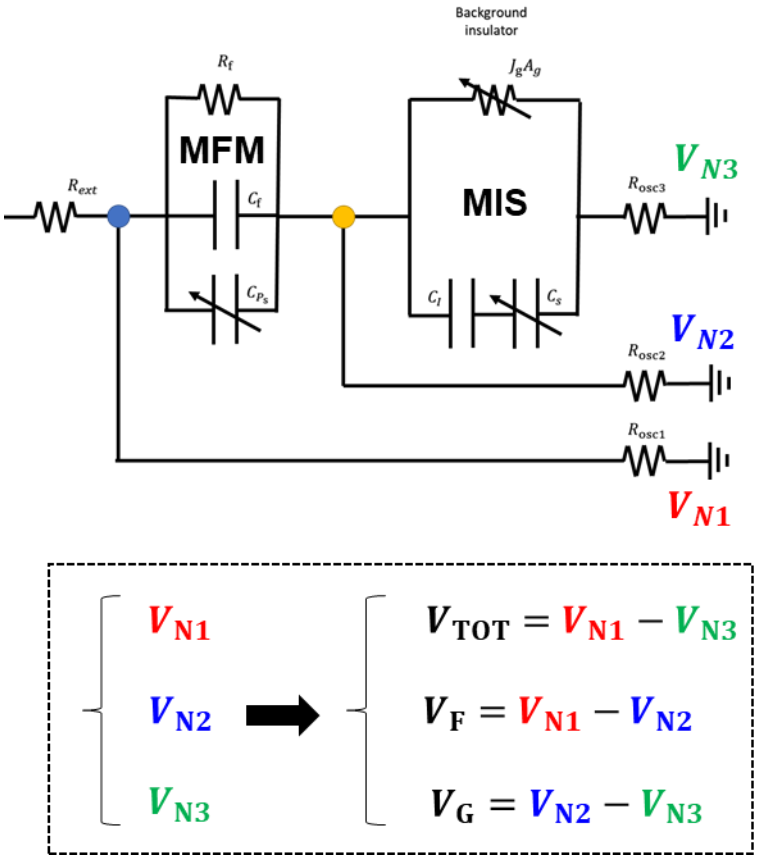

Figure 3-1. Configuration of serially-connected metal-ferroelectric-metal (MFM) and metal-insulator-semiconductor (MIS) capacitors to extract the voltage drop at each capacitor by pulse measurement.

Figure 3-2 shows the second type of MFMIS structure fabricated by increasing the area ratio between the MFM and MIS layers to induce sufficient voltage across the MFM layer for switching. 10 nm-thick HZO layer was used for the MFM stack in the MFMIS structure. For the MIS stacks, 8 nm-thick Al_2O_3 on lightly-doped n type Si substrate and 4 nm-thick SiO_2 on lightly-doped p-type Si substrate were used. By increasing the area of the MIS stacks, the area ratio between the MFM and MIS stacks increased to 4, 16 and 36. It was observed that the voltage ratio across the ferroelectric layer increased from 0.6 to 0.93. Consequently, the polarization hysteresis and memory window of the resulting capacitance-voltage (CV) hysteresis were examined.

Figure 3-3 exhibits the MIS structure with 5 nm-thick Al_2O_3 deposited on n-type Si substrate. As shown by the schematics, post-deposition annealing induces the formation of static dipoles at the interface between the Al_2O_3 layer and native oxide on the Si substrate. These dipoles lead to the accumulation of the minority carriers under the flat-band condition, which also enables the inversion operation as the inversion charges are sufficiently close to the interface.

Lastly, Figure 3-4 describes the fabrication flow of a ring-type FeMOSCAP structure. Well and channel doping were performed on a p-type substrate followed by the deposition of a gate oxide and top electrode layers. Then, an n-type source was doped around the gate region to provide minority carriers, enabling the formation of a ring-type MOSCAP device capable of inversion.

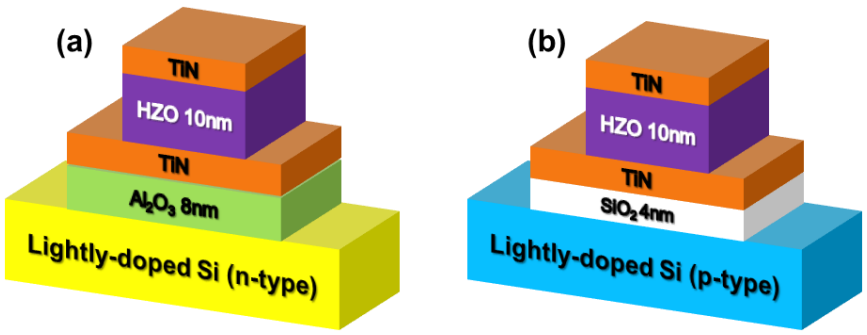

Figure 3-2. MFMIS structures with different areas of HZO-based MFM stack and MIS stacks of (a) Al_2O_3 on lightly-doped n-type Si substrate and (b) SiO_2 on lightly-doped p-type Si substrate.

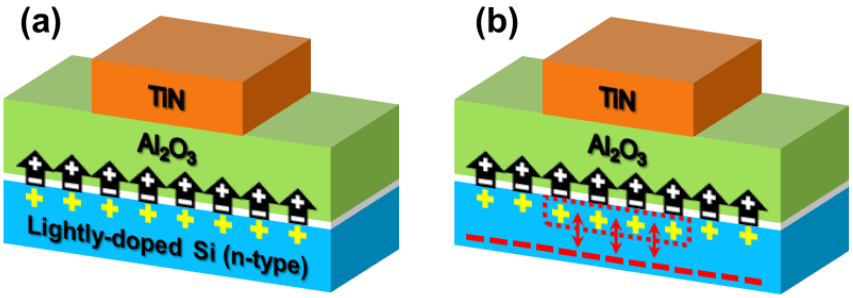

Figure 3-3. (a) Flat-band and (b) inversion / accumulation conditions of Al_2O_3-based MIS capacitor when static dipoles are formed at the interface between Al_2O_3 and lightly-doped n-type Si substrate by annealing.

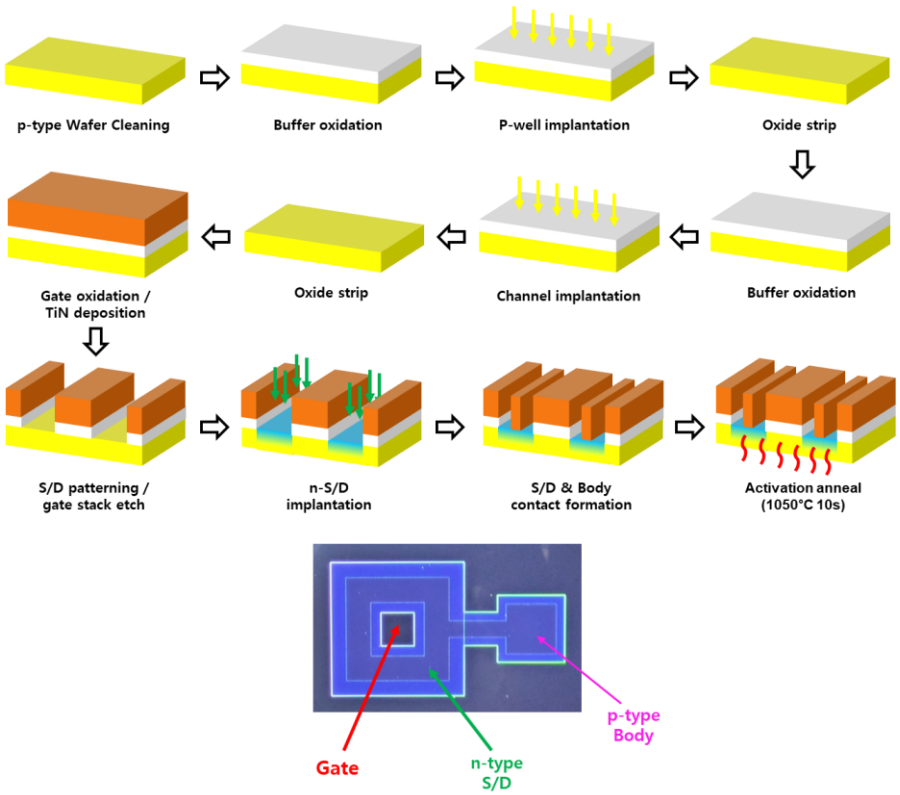

Figure 3-4. Fabrication flow and top-view of the fabricated ring-type ferroelectric metal-oxide-capacitor (FeMOSCAP)

3.3. Results and Discussions

In the serially-connected MFM and MIS configuration, MW characteristics were investigated based on the difference in surface potential when applying pulses in both directions twice as shown in Figure 3-6. By measuring the node voltage, the voltage across the entire MIS structure was extracted. Using the charge density of the MIS device, it was feasible to differentiate the voltage across the gate oxide and the surface potential. The hysteresis direction of the surface potential, as observed from these measurements, was consistently counterclockwise, which corresponds to the FE switching direction with reference to the n-type substrate. However, the MW was only about 1.1 V, which corresponds to approximately half of the coercive voltage ($2V_c$) of the actual MFM capacitor used (2.2 V). Further analysis in different structures is performed to understand why MW in the MFM structure, where sufficient switching and MIS inversion are expected, is limited to half of $2V_c$.

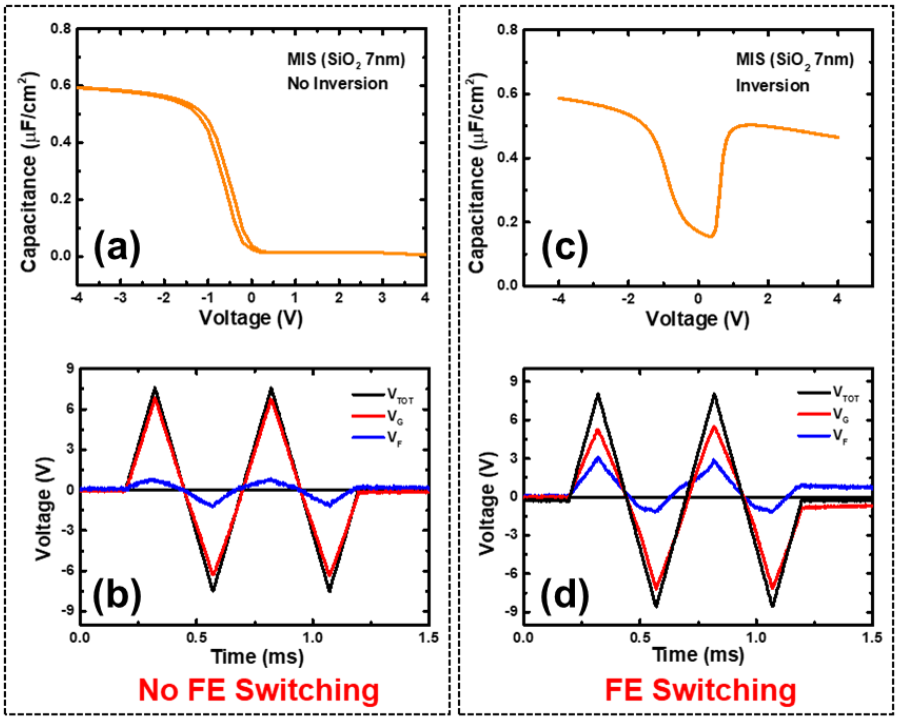

Figure 3-5. (a) Capacitance characteristics of MIS capacitor with no inversion (deep depletion) operation. (b) Voltage distribution at each capacitor showing that insufficient voltage drop at MFM leads to no ferroelectric switching. (c) Capacitance characteristics of MIS capacitor with inversion operation. (d) Voltage distribution at each capacitor showing that sufficient voltage drop at MFM leads to ferroelectric switching.

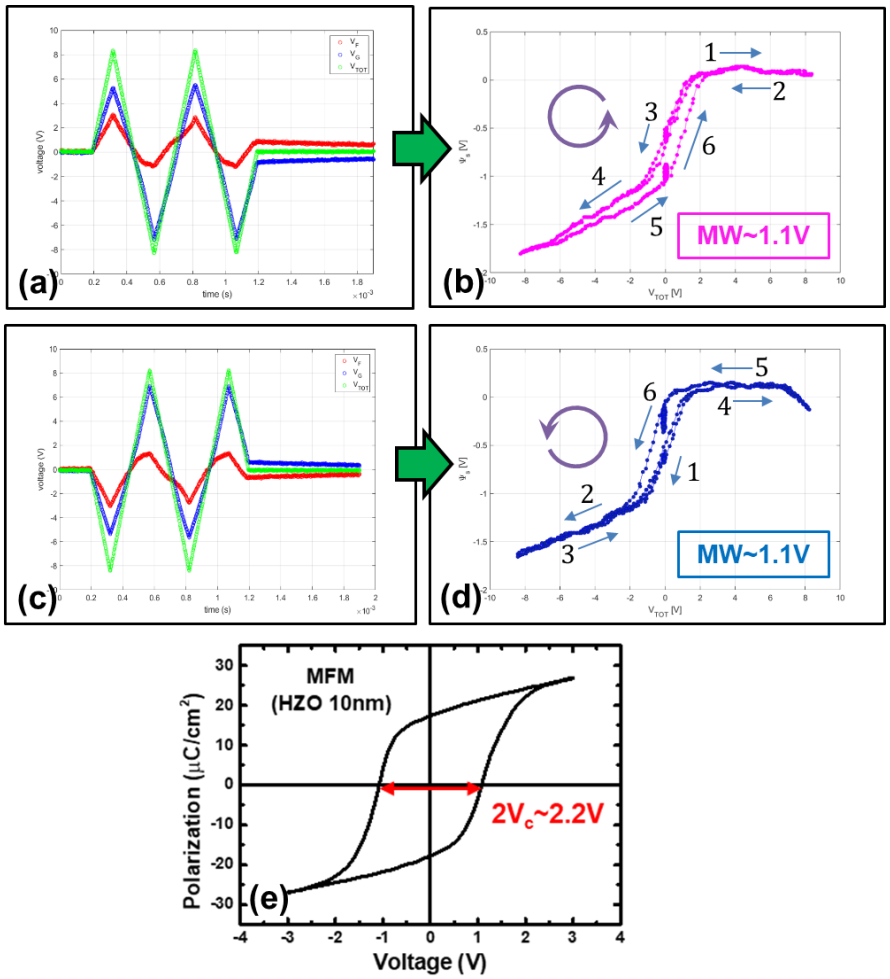

Figure 3-6. (a) Double-ramp pulse (positive first) applied to MFM+MIS configuration. (b) Ferroelectric switching-induced hysteresis of MIS surface potential with memory window of 1.1 V. (c) Double-ramp pulse (negative first) applied to MFM+MIS configuration. (d) Ferroelectric switching-induced hysteresis of MIS surface potential with memory window of 1.1 V. (e) Polarization hysteresis of serially-connected MFM capacitor with $2V_c$ of 2.2 V.

Figure 3-7 presents the polarization and capacitance hysteresis measured from MFM, MIS and MFMIS stacks with the Al_2O_3 insulator on n-type Si substrate. The saturated capacitance characteristics in the depletion region refers that no inversion is induced under all area conditions for the MIS stacks. Accordingly, only positive uni-polar switching hysteresis is observed by accumulation for the MFMIS stacks. The uni-polar switching increases as the area ratio increases, meaning that the larger voltage is distributed at HZO for FE switching.

In Figure 3-8, the orange curve represents the C-V characteristics when sweeping from negative to positive voltage, while the purple curve represents the C-V characteristics when sweeping from positive to negative voltage. When the area ratio was 4, the hysteresis was in the clockwise direction, opposite to the FE switching direction with respect to the n-type substrate. However, when the area ratio was increased to 16 and 36, the hysteresis direction was reversed, and MWs induced by FE switching were observed in the opposite direction. As the area ratio increased from 16 to 36, MW was expanded due to the larger polarization switching. However, even for the area ratio of 36 with the largest MW, it still corresponded to only about half of $2V_c$ due to the positive uni-polar switching behavior.

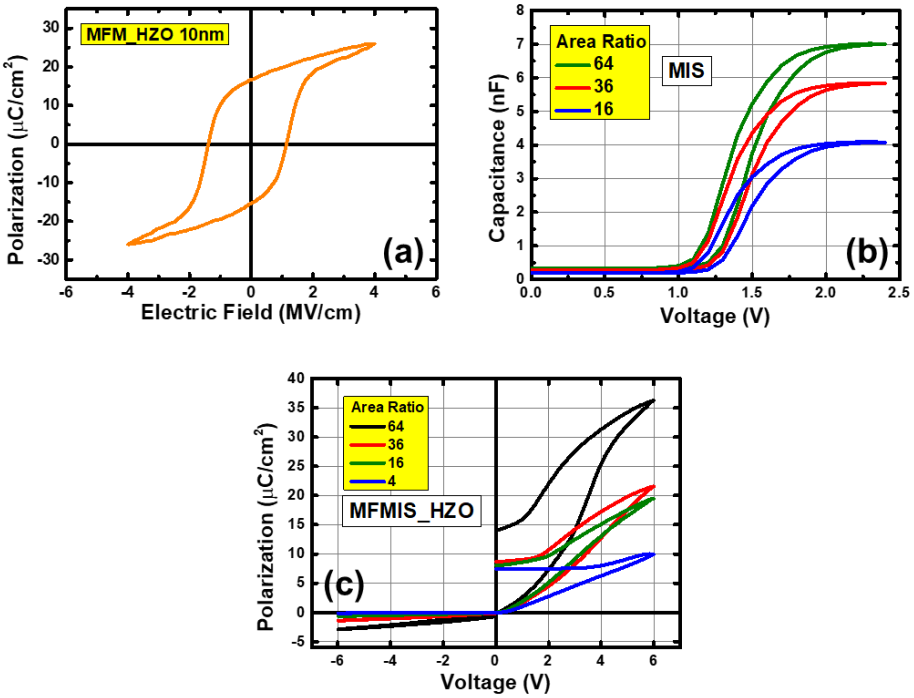

Figure 3-7. (a) Polarization hysteresis of HZO-based MFM stack in MFMIS structure. (b) Capacitance hysteresis of MIS (Al_2O_3 on n-type Si) stacks with different electrode areas in MFMIS structure. (c) Polarization hysteresis of MFMIS structure by uni-polar switching behavior only in the accumulation mode (positive bias).

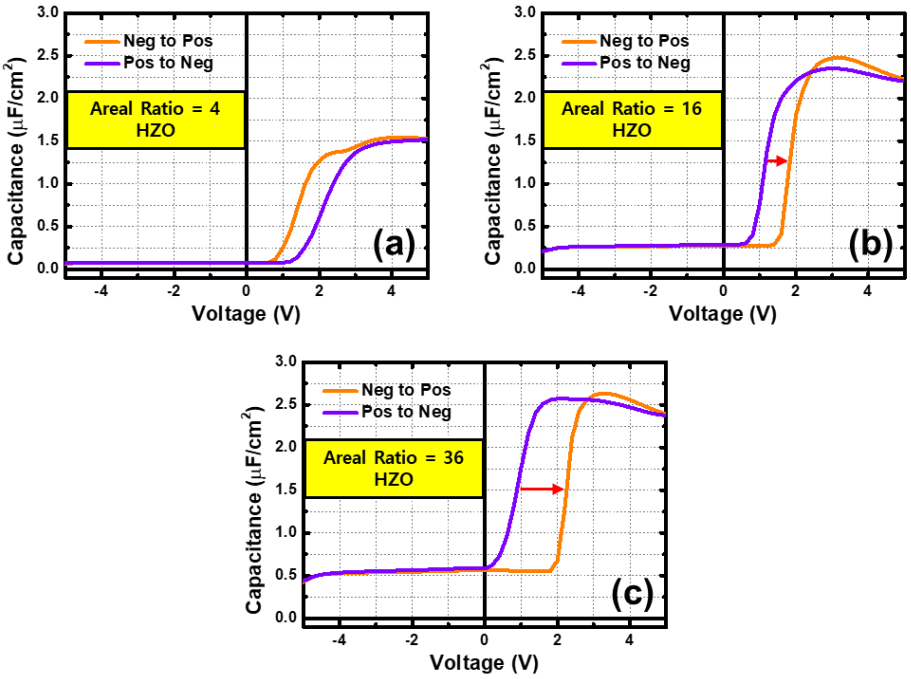

Figure 3-8. (a) Capacitance hysteresis of HZO-based MFMIS structure with MIS (Al_2O_3 on n-type Si) area ratio of (a) 4, (b) 16, and (c) 36. Trap-induced hysteresis direction is observed in the structure with MIS area ratio of 4, and the direction is inverted with expansion of memory window as the ratio increases to 16 and 36.

Figure 3-9 presents the polarization and capacitance hysteresis measured from MFM, MIS and MFMIS stacks with SiO_2 insulator on p-type Si substrate. The saturated capacitance characteristics in the depletion region refers that inversion is also not induced under all area conditions for the MIS stacks. Accordingly, only negative uni-polar switching hysteresis is observed by accumulation for the MFMIS stacks. The uni-polar switching increases as the area ratio increases, meaning that the larger voltage is distributed at HZO for FE switching.

The C-V characteristics in Figure 3-10 showed similar trends of capacitance hysteresis change as in the case of Al_2O_3-based MFMIS structure. When the area ratio was 4, the hysteresis was in the counter-clockwise direction, opposite to the FE switching direction with respect to the p-type substrate. However, when the area ratio was increased to 16 and 36, the hysteresis direction was reversed, and MWs induced by FE switching were observed in the opposite direction. As the area ratio increased from 16 to 36, MW was expanded due to the larger polarization switching. However, even for the area ratio of 36 with the largest MW, it still corresponded to much less than half of $2V_c$ due to the negative uni-polar switching behavior. Additionally, the positive-up-negative-down (PUND) measurements for the MFMIS structures in Figure 3-11 reveal that significant back-switching, possibly attributed to a depolarizing field generated by the disrupted compensation of FE bound charges due to the thick insulators, occurs in each uni-polar switching direction.

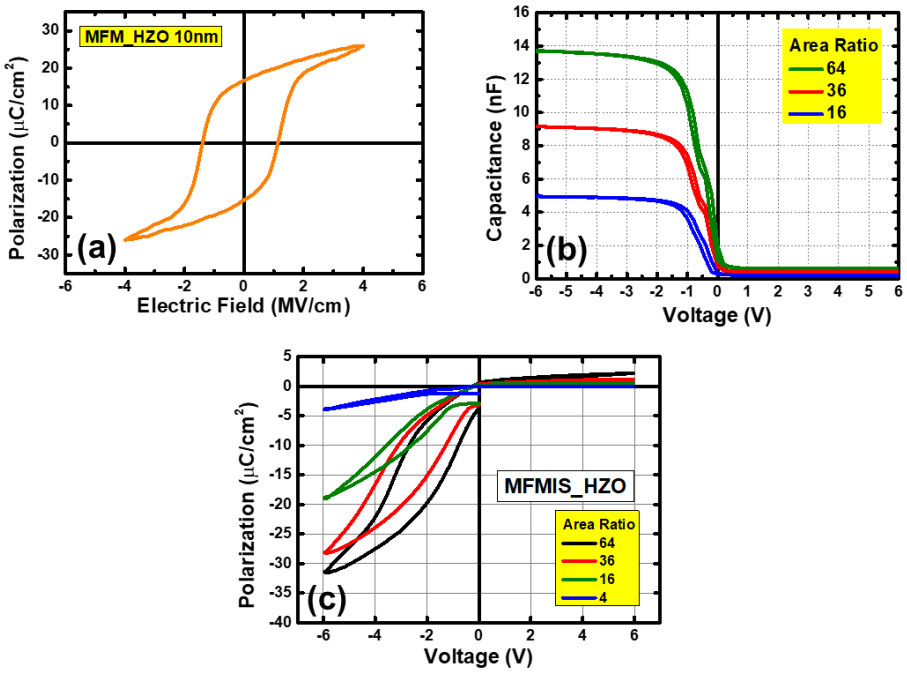

Figure 3-9. (a) Polarization hysteresis of HZO-based MFM stack in MFMIS structure. (b) Capacitance hysteresis of MIS (SiO_2 on p-type Si) stacks with different electrode areas in MFMIS structure. (c) Polarization hysteresis of MFMIS structure by uni-polar switching behavior only in the accumulation mode (negative bias).

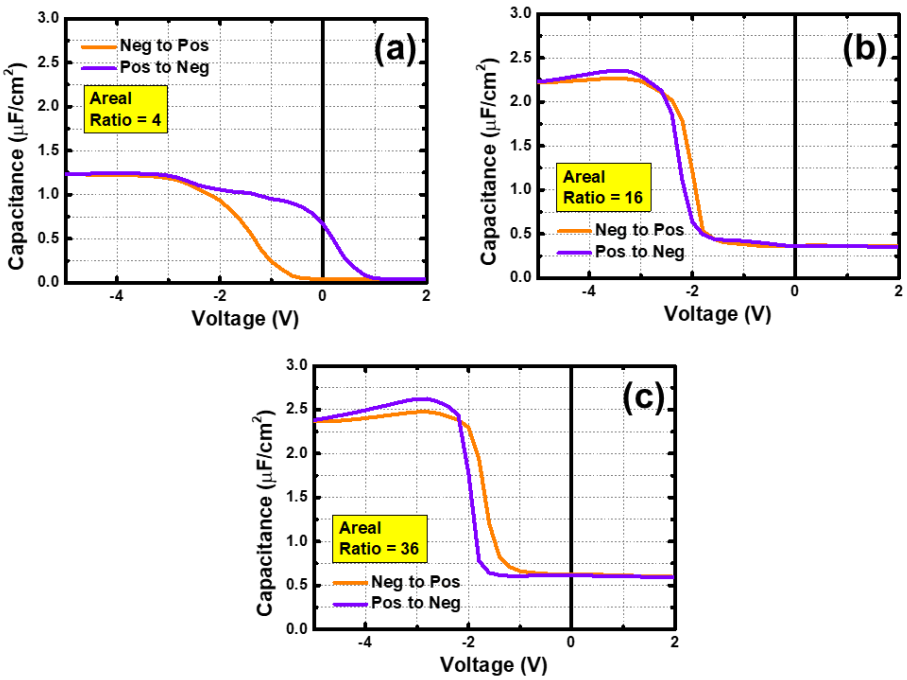

Figure 3-10. (a) Capacitance hysteresis of HZO-based MFMIS structure with MIS (SiO_2 on p-type Si) area ratio of (a) 4, (b) 16, and (c) 36. Trap-induced hysteresis direction is observed in the structure with MIS area ratio of 4, and the direction is inverted with nearly constant memory window as the ratio increases to 16 and 36.

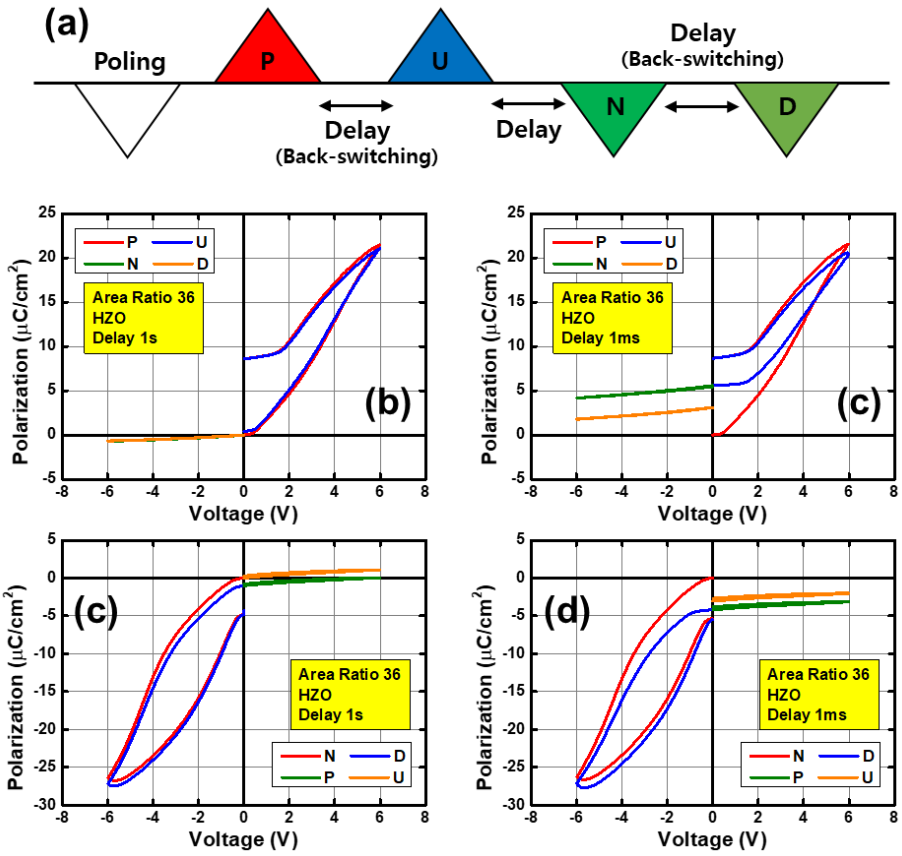

Figure 3-11. (a) Positive-up-negative-down (PUND) pulse with intermediate delays for back-switching of switched polarization. Positive uni-polar switching behavior of HZO-based MFMIS (Al_2O_3 on n-type Si) structure by PUND pulse with intermediate delays of (b) 1 s and (c) 1 ms. Negative uni-polar switching behavior of HZO-based MFMIS (SiO_2 on p-type Si) structure by NDPU pulse with intermediate delays of (d) 1 s and (e) 1 ms.

Figure 3-12 exhibits the C-V hysteresis of 4 nm- and 5.5 nm-thick Al2O3-based MIS capacitors. Inversion operation is observed for both 4 nm and 5.5 nm thickness conditions after post-deposition annealing, and, interestingly, the as-deposited condition also induced a significant inversion behavior. This is possibly due to the static dipole formation during the high thermal deposition condition of ALD.

Figure 3-13 demonstrates the schematics of MFIS capacitors with HZO and HZAHZ films deposited on 5 nm-Al_2O_3 (n-type Si substrate) and 5 nm-SiO_2 (p-type Si substrate) insulators. For the p-type Si structure, no ferroelectric switching is observed, which verifies that the inversion in the n-type Si structure is attributed to the formation of static dipoles at the Al_2O_3 and Si interface. On the other hand, the polarization hysteresis of the n-type Si structure showed considerable FE switching by inversion. However, the switching behavior is still not symmetric, feasibly due to the disrupted FE bound charge compensation (under-compensation) by the accumulated inversion charges.

The quasi-static C-V measurements of the n-type Si structures in Figure 3-14 distinctively show abrupt increases of capacitance induced by bi-polar switching behavior, but the back-switching phenomenon observed by the PUND measurements reveal that the depolarizing field is still a critical issue. The C-V characteristics measured by the conventional C-V measurement method with high-frequency small signals only exhibit the capacitance in trap-induced hysteresis direction.

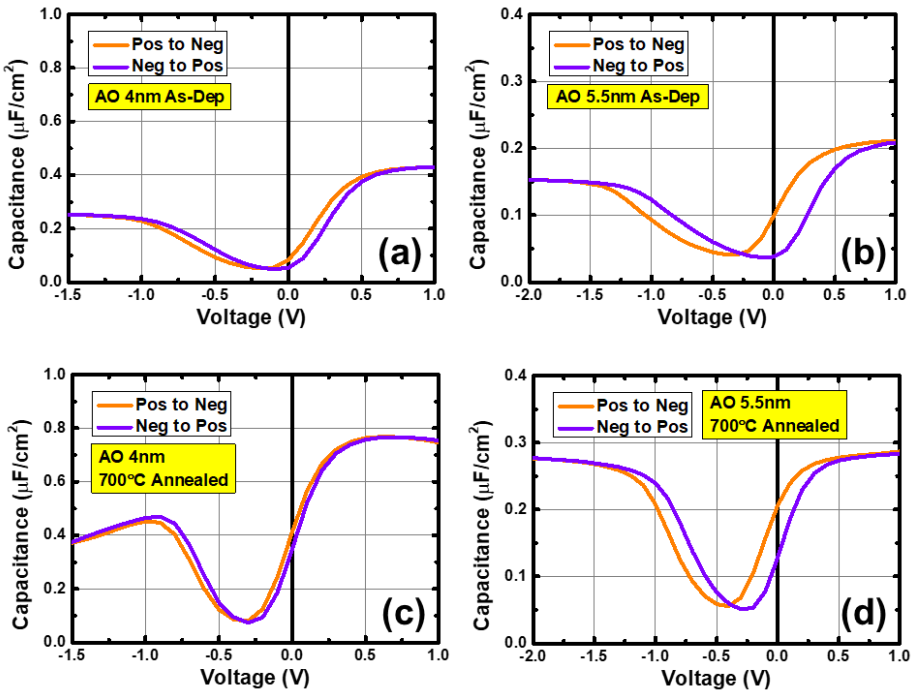

Figure 3-12. Capacitance characteristics of as-deposited MIS capacitors with (a) 4 nm- and (b) 5.5 nm-Al_2O_3 on lightly-doped n-type Si substrate. Capacitance characteristics of 700 °C-annealed MIS capacitors with (c) 4 nm- and (d) 5.5 nm-Al_2O_3 on lightly-doped n-type Si substrate.

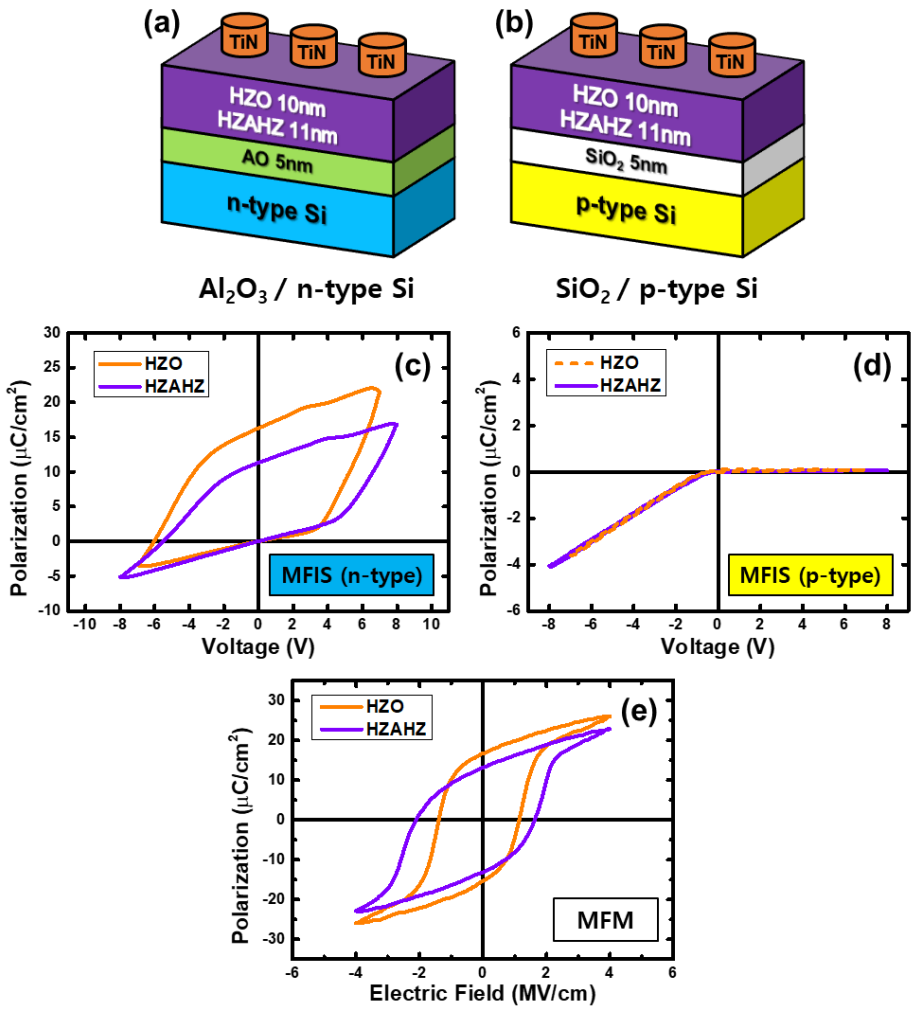

Figure 3-13. Schematics of HZO- and HZAHZ-based MFIS capacitors with (a) 5 nm-Al_2O_3 on n-type Si and (b) 5 nm-SiO_2 on p-type Si substrate. Polarization hysteresis of HZO- and HZAHZ-based MFIS capacitors on (c) n-type and (d) p-type Si substrate. (e) Polarization hysteresis of HZO- and HZAHZ-based MFM capacitors.

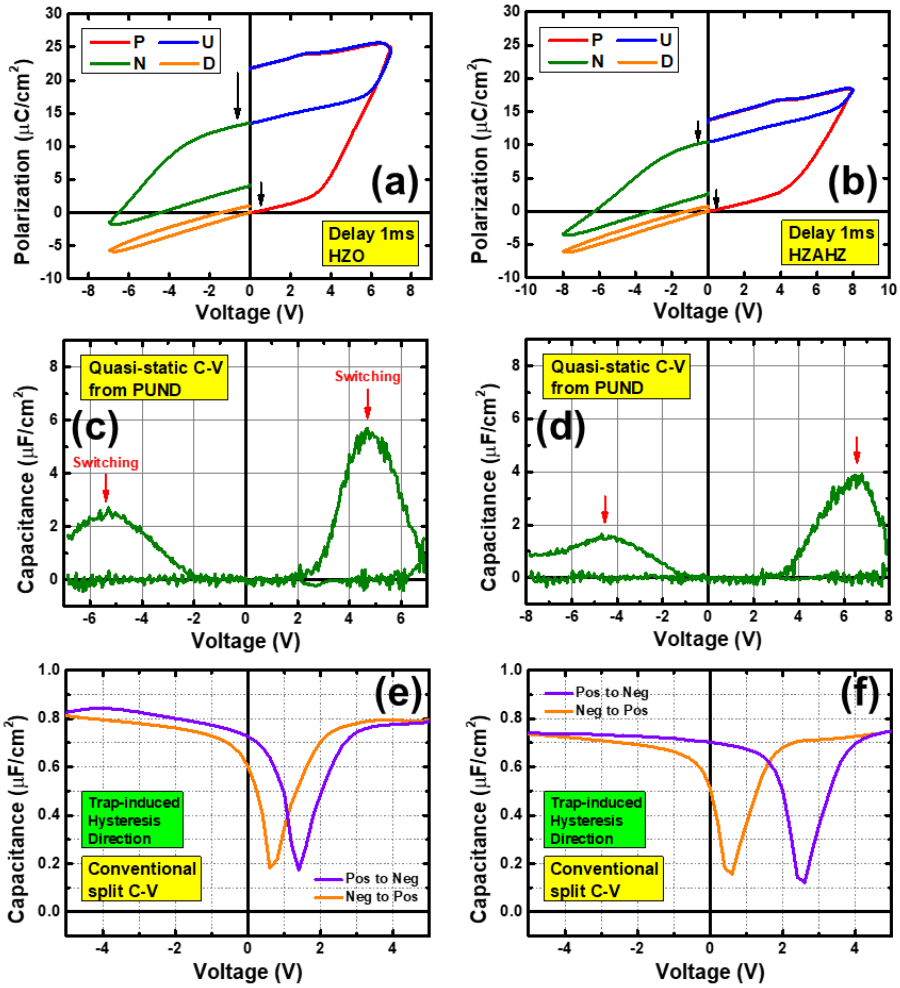

Figure 3-14. Switching and non-switching polarization behavior of (a) HZO- and (b) HZAHZ-based MFIS (n-type) capacitors measured by PUND pulses with intermediate delays of 1 ms. Quasi-static capacitance characteristics of (c) HZO- and (d) HZAHZ-based MFIS capacitors calculated from PUND measurements. Trap-induced capacitance hysteresis of (e) HZO- and (f) HZAHZ-based MFIS capacitors measured by conventional capacitance measurement method.

Figure 3-15 demonstrates the schematics of MFIS capacitors with 12 nm- and 22 nm-HAO films deposited on 5 nm-Al_2O_3 (n-type Si substrate) insulator. The polarization hysteresis of the MFIS capacitors showed considerable FE switching by inversion as in the case of HZO and HZAHZ. However, the switching behavior is still not symmetric, similarly due to the disrupted FE bound charge compensation (under-compensation) by the accumulated inversion charges.

The quasi-static C-V measurements of the MFIS capacitors in Figure 3-16 distinctively show abrupt increases of capacitance induced by bi-polar switching behavior, but the back-switching phenomenon observed by the PUND measurements reveal that the depolarizing field is still a critical issue. The C-V characteristics measured by the conventional C-V measurement method with high-frequency small signals only exhibit the capacitance in trap-induced hysteresis direction as in the case of HZO and HZAHZ.

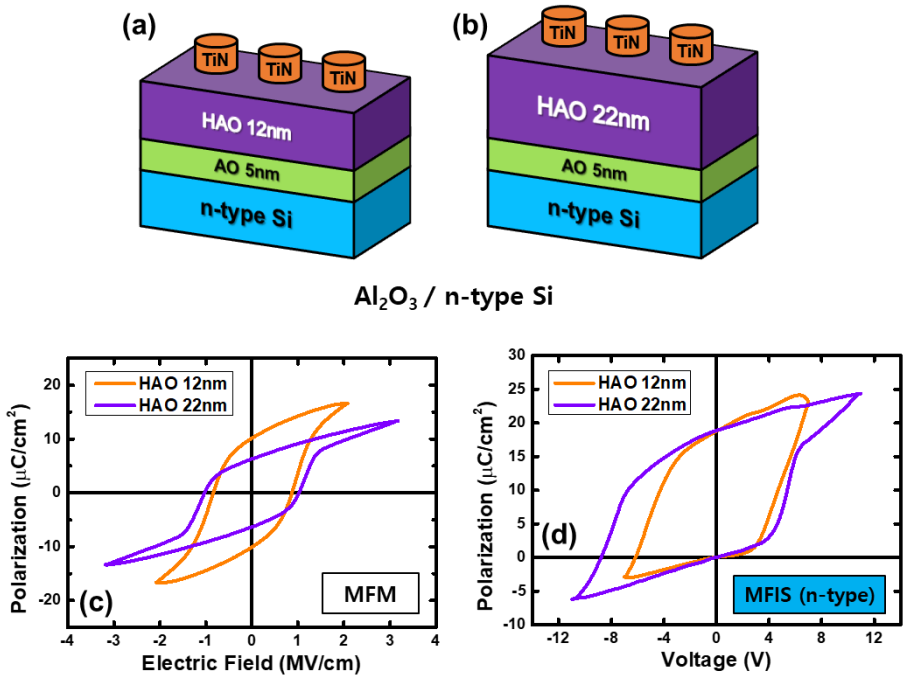

Figure 3-15. Schematics of (a) 12 nm- and (b) 22 nm-HAO MFIS capacitors with 5 nm-Al_2O_3 on n-type Si substrate. (c) Polarization hysteresis of 12 nm and 22 nm-HAO MFM capacitors. (d) Polarization hysteresis of 12 nm and 22 nm-HAO MFIS capacitors.

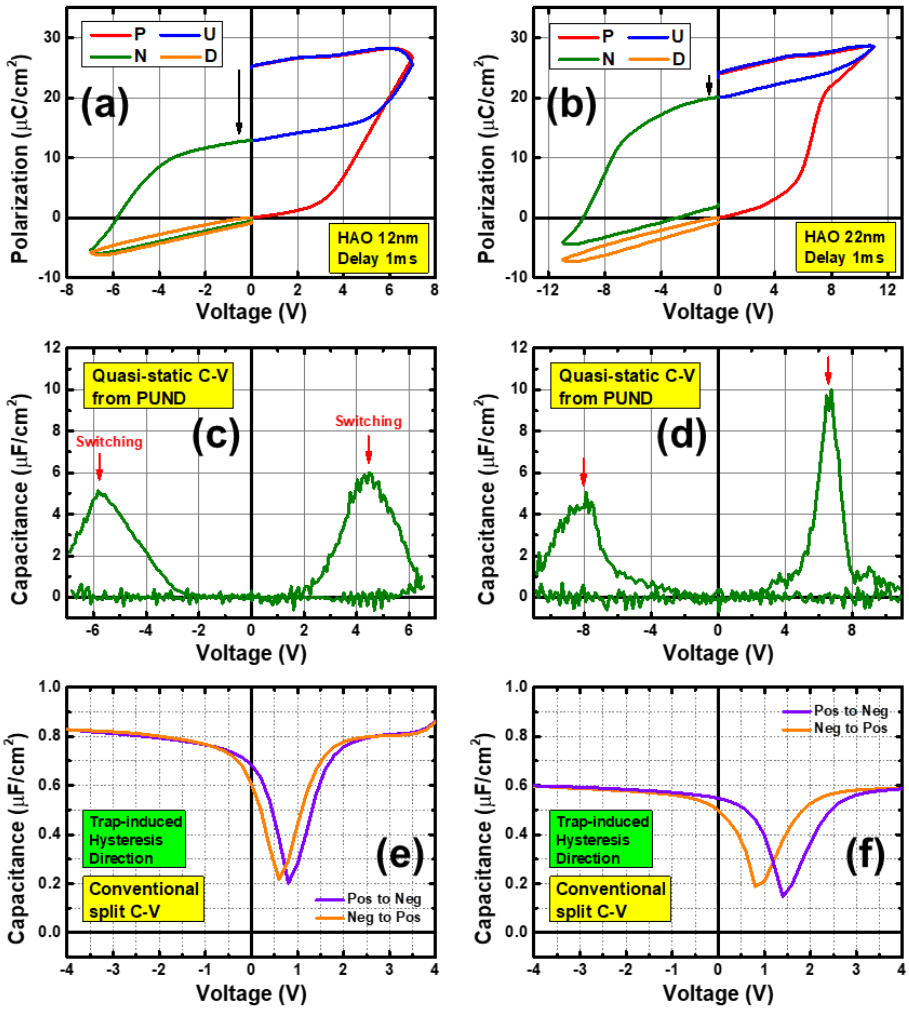

Figure 3-16. Switching and non-switching polarization behavior of (a) 12 nm- and (b) 22 nm-HAO MFIS (n-type) capacitors measured by PUND pulses with intermediate delays of 1 ms. Quasi-static capacitance characteristics of (c) 12 nm- and (d) 22 nm-HAO MFIS capacitors calculated from PUND measurements. Trap-induced capacitance hysteresis of (e) 12 nm- and (f) 22 nm-HAO MFIS capacitors measured by conventional capacitance measurement method.

Finally, the thickness of the Al_2O_3 insulator is reduced to 1.5 nm for MFIS capacitors with 17 nm and 25 nm-HAO films. The corresponding schematics are shown in Figure 3-17. The polarization hysteresis of each relevant MFM capacitor shows that $2P_r$ of the 17 nm-HAO structure is much larger than that of the 25 nm-HAO structure even though $2V_c$ is about the same. With the decreased thickness of Al2O3 insulator, the polarization hysteresis of the MFIS structures demonstrate significantly symmetric FE switching.

The PUND measurements in Figure 3-18 reveal that the previous back-switching issue induced by a depolarizing field is also reduced extensively. Nonetheless, the conventional C-V measurements of the two structures show that only the 17 nm-HAO capacitor, with large $2P_r$, exhibits a capacitance hysteresis in switching-induced direction. This refers to a feasible assumption that a large amount of FE bound charges for compensation is a more favorable condition to respond the high-frequency small signals by the C-V measurement.

Figure 3-19 describes the capacitance hysteresis of the fabricated ring-type MOSCAP and FeMOSCAP with 22 nm-HAO film. Distinct inversion operation is observed by the MOSCAP device, and FeMOSCAP also exhibits a switching-induced capacitance hysteresis with a significant MW.

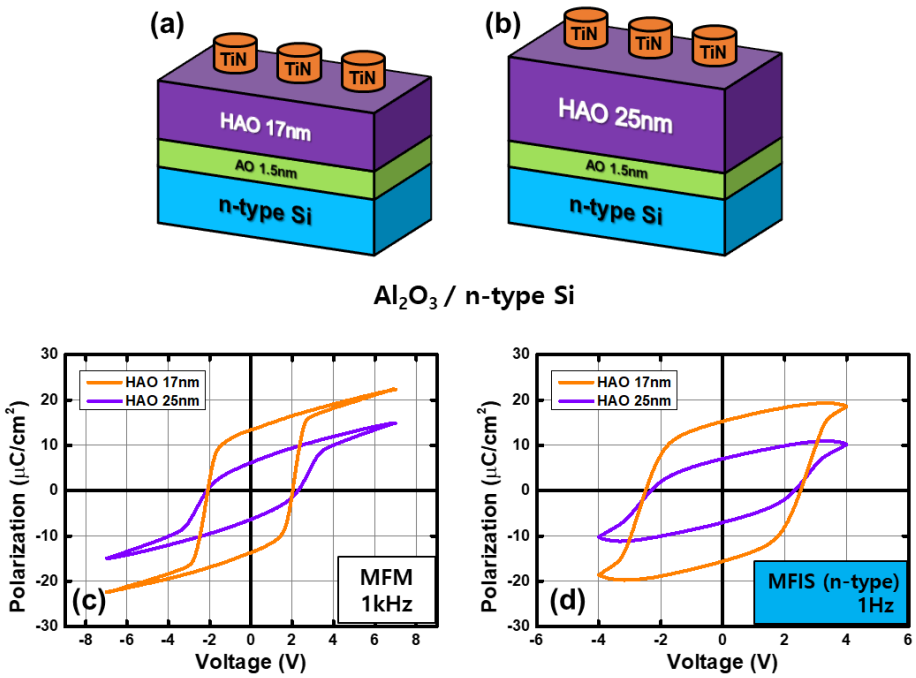

Figure 3-17. Schematics of (a) 17 nm- and (b) 25 nm-HAO MFIS capacitors with 1.5 nm-Al_2O_3 on n-type Si substrate. (c) Polarization hysteresis of 17 nm and 25 nm-HAO MFM capacitors. (d) Polarization hysteresis of 17 nm and 25 nm-HAO MFIS capacitors.

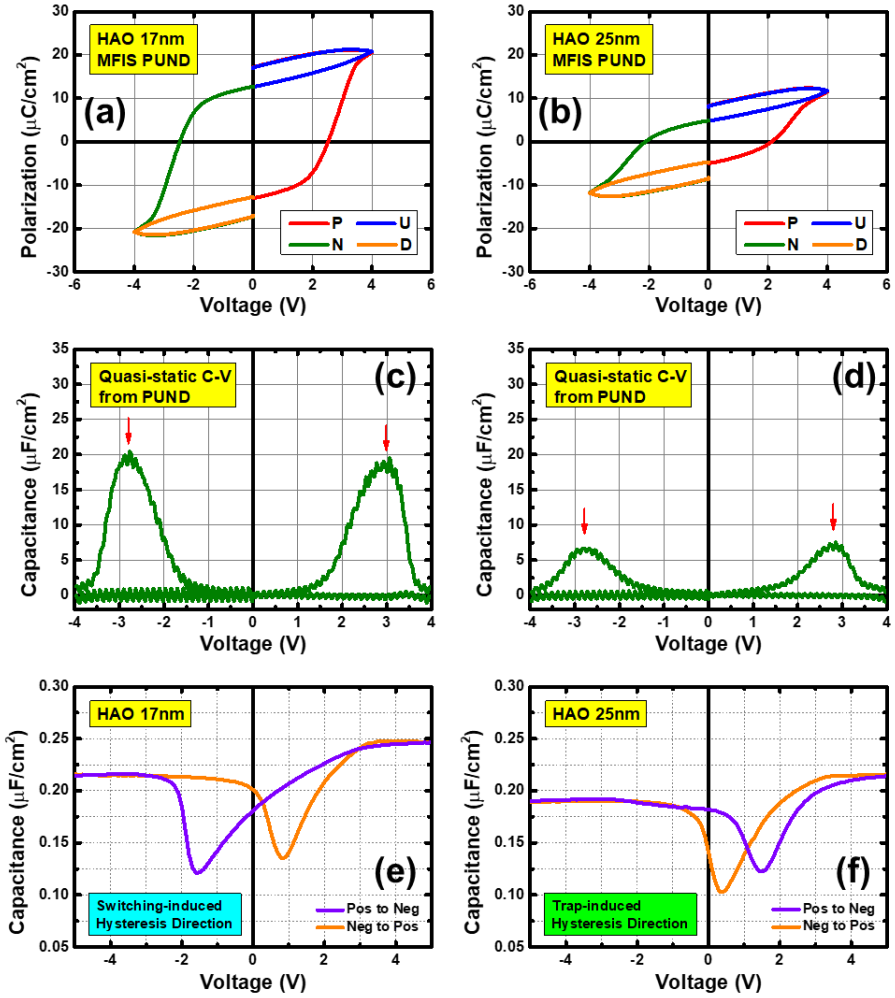

Figure 3-18. Switching and non-switching polarization behavior of (a) 17 nm- and (b) 25 nm-HAO MFIS (n-type) capacitors measured by PUND pulses with intermediate delays of 1 ms. Quasi-static capacitance characteristics of (c) 17 nm- and (d) 25 nm-HAO MFIS capacitors calculated from PUND measurements. Switching-induced capacitance hysteresis of (e) 17 nm- and trap-induced hysteresis of (f) 25 nm-HAO MFIS capacitors measured by conventional capacitance measurement method.

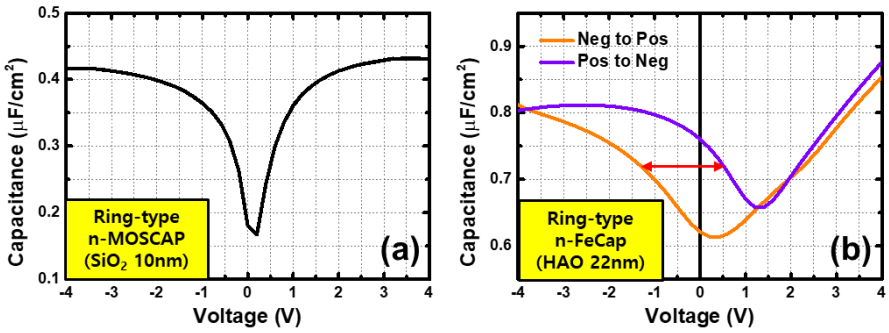

Figure 3-19. (a) Capacitance characteristics of fabricated ring-type nMOSCAP with inversion operation. (b) Switching-induced capacitance hysteresis of fabricated ring-type nFeMOSCAP with 22 nm-HAO ferroelectric film.

3.4. Conclusion

In this chapter, a variety of MFMIS and MFIS structures were fabricated to induce FE switching and evaluate the relevant MW properties in lightly-doped Si structures. For the MFMIS structure, uni-polar FE switching operation was observed although sufficient voltage distribution across the FE layer is induced by different area ratios of the MFM and MIS stacks. Additionally, it was observed from the PUND measurements that a significant depolarizing field induced back-switching of the switched polarization to degrade the expected MW characteristics. For the MFIS capacitors, in which inversion was induced by the dipole formation at the Al_2O_3 and Si interface, bi-polar switching operation was examined although the switching was still not symmetric and the depolarizing field effect was also present. Nevertheless, it was observed that reducing the thickness of the Al_2O_3 interface layer led to significantly symmetric FE switching by complete charge compensation of the FE bound charges. The capacitance hysteresis in switching-induced direction for the MFIS structure with large $2P_r$ indicates that the complete charge compensation is also a more favorable condition for the high-frequency small signal measurement. Lastly, fabricated ring-type MOSCAP and FeMOSCAP devices exhibited inversion and switching-induced capacitance hysteresis with an MW significantly close to $2V_c$ of the reference structure.

3.5. Bibliography

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4. Decomposition of Interface Layer by Oxygen-Scavenging Effect

4.1. Introduction

Stray field near the surface of the polarized ferroelectric (FE) film due to the presence of incompletely compensated FE bound charge can be used to modulate the carrier concentration of the nearby semiconductor layer. Metal-ferroelectric-semiconductor field-effect transistor (MFSFET) is a representative semiconductor device, which Moll and Tarui first suggested in 1963.[1] However, the lack of Si-compatible FE material, which does not degrade the highly interface-sensitive performance of the semiconductor, has prohibited the direct formation of the FE layer on the Si substrate.[2-4] Therefore, the conventional ferroelectric-FET (FeFET) structure has involved the insulating layer, mostly SiO_2, at the interface between the FE layer and Si substrate resulting in the metal-ferroelectric-insulator-semiconductor field-effect transistor (MFISFET). In this structure, the interface degradation, such as an increase of D_{it}, can be suppressed to guarantee the feasible operation of the FET and achieve the nonvolatile memory effect by the FE polarization switching.

Nonetheless, the involvement of the SiO_2 layer invokes several critical problems, which are mainly attributed to the interrupted FE bound charge

screening from the accumulated (or inverted) carriers in the Si-channel region during the device operation. The problems include retention failure, fatigue of the FE switching, and decayed memory window (MW) due to the incomplete FE switching. Besides, when the interfacial SiO_2 was removed, too high D_{it} and other unwanted charge-trapping-related effects deteriorated the FET performance, especially when a conventional perovskite-based FE material was adopted.[5-6] However, this problematic circumstance could be overcome if the doped-HfO_2-based FE layer is used.

As the paraelectric HfO_2-based high-k dielectrics are already in mass production for the high-performance complementary metal-oxide-semiconductor (CMOS) devices,[7-9] the integration of the doped-HfO_2-based FE layer in the MFSFET or MFISFET device must be fluent. Extensive research has been in progress to enhance the interface quality of HfO_2-based CMOS devices with various dopants and semiconductor materials.[10-13] Furthermore, it was recently elucidated that the interfacial SiO_2 could be unnecessary even in high-performance CMOS devices when the high-k layer was optimized.[14] Therefore, it is anticipated that implementing MFSFET with the doped-HfO_2 FE layer, which may not invoke the problems mentioned above of MFISFET devices, can be possible without sacrificing the FET performance, i.e., no increase in D_{it}.

There have been attempts to remove the interfacial SiO_2 layer before the HfO_2-based film growth on the Si substrate using ca. wet-etching and the

hydrogen termination of the etched Si surface.[15-16] Still, the interfacial SiO_2 layer regrew during the atomic layer deposition (ALD) of the high-k or FE films, which usually adopts highly-oxidizing species, such as O_3, to achieve the high-quality ALD oxide films.[17-18] Therefore, in the high-k gate insulator field, the oxygen-scavenging technique has been used, in which a highly oxidizing metal layer, such as Ti, was included in the gate stack.[19-20] Such a highly oxidizing layer reduces the interfacial SiO_2 layer, while the reduction of the high-k HfO_2 layer, which has the higher thermodynamic stability than SiO_2 upon reduction, was minimized.[21-23]

Inspired by these previous reports,[19-23] this work exploits the insertion of a Ti layer within the TiN gate of an MF(I)S capacitor structure, wherein 10 nm-thick HAO film is used as the FE gate insulator. As shown by the schematics in Figures 4-1(a) and (b), two different top electrode structures of TiN and Ti-inserted TiN/Ti/TiN are adopted to investigate any pertinent change of CET and its consequent effects on polarization switching through chemical decomposition of the interfacial SiO_2 and the oxidation of the inserted Ti scavenging layers. Notably, the intermediate TiN barrier layer is inserted to prevent any possible generation of leakage paths if the pure Ti metal is directly deposited and diffused into the underlying HAO film.[20,24] It is also considered that relatively rapid oxidation of a thin Ti layer by the scavenged oxygen would limit the scavenging effect as a completely-oxidized TiO_2 layer tends to trigger the scavenging cycle much less efficiently. The polarization-

voltage (P-V) characteristics in Figure 4-2 exhibits the FE performance of the TiN/Ti/TiN structures with different TiN barrier and Ti scavenging layer thicknesses. The 5 nm-TiN barrier and 5 nm-Ti scavenging layers showed the optimal performance. An annealing temperature range of 600-800 °C is applied to not only examine the phase evolutions in the HAO film but also verify the correlation between the oxygen-scavenging effects and annealing temperature as thermodynamic reactions are involved in the process. Finally, additional analysis on frequency dispersions of capacitance-voltage (C-V) characteristics and maximum D_{it} calculations by the conductance method are performed to precisely comprehend the relevant mechanism of the oxygen-scavenging process.[25-26]

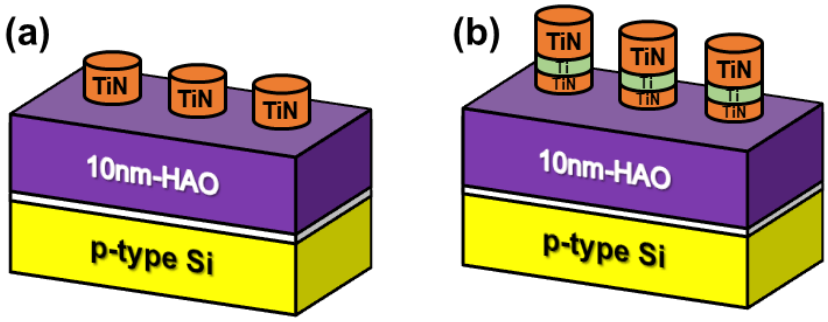

Figure 4-1. Schematics of 10 nm-Al-doped HfO_2 (HAO) MFIS capacitors with (a) 50 nm-TiN and (b) 50 nm-TiN/5 nm-Ti/5 nm-TiN top electrodes.

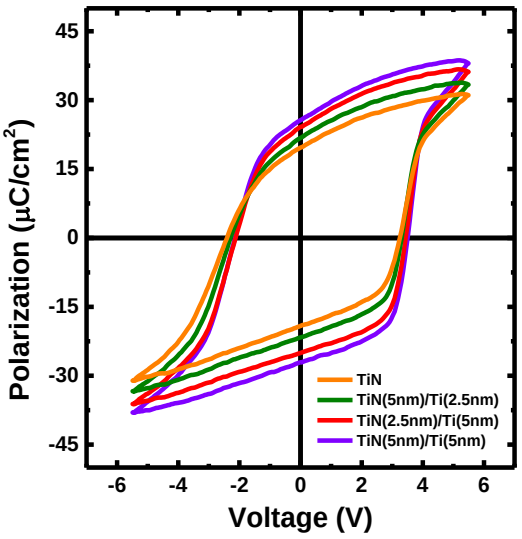

Figure 4-2. Polarization-voltage (P-V) characteristics of 800 °C-annealed HAO-based MFIS capacitors with TiN and TiN/Ti/TiN top electrodes with different thicknesses of the Ti scavenging and TiN barrier layers.

4.2. Experimental

(001) p-type lightly-doped (resistivity ≈ 10 Ω·cm) and highly-doped (resistivity < 0.005 Ω·cm) Si substrates were initially cleaned by the standard cleaning process in aqueous mixtures of sulfuric acid peroxide (SPM), ammonium peroxide (APM), and hydrochloric peroxide (HPM) followed by diluted hydrofluoric acid (HF) dip to remove the metallic contaminants and remaining native oxide. 10 nm-thick HAO films with a Hf:Al composition of 33:1 were deposited by alternating ALD (Atomic Preminum Cluster Type, CN-1) sub-cycles of HfO_2 and Al_2O_3 at a substrate temperature of 280 °C. Tetrakis-ethylmethylaminohafnium (Hf[N(CH3)(C2H5)]4, TEMAH) and trimethylaluminum (Al(CH3)3, TMA) were used as metal precursors, and O_3 was used as a reactive gas. Metal shadow masks were used to deposit the circular TiN or Ti top electrodes with a diameter of ~300 μm by radio-frequency (RF) reactive sputtering (SRN 120, Sorona) at 500 W and 400 W for TiN and Ti, respectively. The thickness of the TiN top electrode was 50 nm for both structures, and the thickness of the inserted TiN barrier and Ti oxygen-scavenging layers was 5 nm. The deposition of the TiN and Ti layers was an in-situ process to minimize any undesired oxidation before annealing. Subsequently, the fabricated samples were annealed at 600 °C, 700 °C, and 800 °C in an N_2 environment for 20 s.

The C-V and current-voltage (I-V) measurements were performed by HP4140D pA/DC voltage source and HP4194A impedance analyzer. 10 kHz

of ac oscillation frequency and 0.1 V of step voltage were used to measure the double-sweep C-V hysteresis. The cross-sectional HRTEM (JEOL Ltd., JEM-F200 (TFEG)) images were analyzed to examine the interfaces and top electrode structures of TiN and TiN/Ti/TiN, and the P-V characteristics were measured using an FE tester (TF Analyzer 2000, Aixacct Systems) with triangular pulses at a frequency of 1 kHz. XPS (Axis Supra, Kratos) analysis of the depth profile was performed to obtain the elemental signals at each layer of the sample structures, and the etch time and thickness of each profiling sequence were 75 s and ~2 nm, respectively.

4.3. Results and Discussions

As the HAO film requires a relatively high crystallization temperature for tetragonal phase (t-phase) stabilization and its transition to the desired polar orthorhombic phase (o-phase),[27] top electrode capping on the FE layer before or after annealing is a critical factor.[24,28-29] It has been reported that the grain growth in doped-HfO_2 films induced by high annealing temperatures increases the non-polar monoclinic phase (m-phase) portion, which degrades the ferroelectricity.[27,30-32] Meanwhile, the top electrode capping could mechanically confine the HAO film to suppress grain growth and shearing of the t-phase unit cell into the m-phase unit cell.[27,30-32] Thus, the relevant phase evolutions under 600-800 °C post-deposition annealing (PDA) conditions, in which no top electrode is deposited, were examined by the grazing incidence x-ray diffraction (GIXRD) measurements in Figure 4-3(a). At the elevated annealing temperatures, the ratio of the non-polar m(111) phase, denoted by the intensity peak at a 2θ angle of ~28.9°, increases whereas the polar o(111) phase ratio, denoted by the peak at 2θ ~30.8° despite being hardly distinguished from its overlapping t(101) phase peak, decreases in the absence of the top electrode.[28] For the post-metallization annealing (PMA) conditions of the TiN and TiN/Ti/TiN structures shown in Figures 4-3(b) and (c), in which the top electrodes are deposited, the non-polar m-phase formation is effectively suppressed. This coincides with the expected confinement and shear-prohibition effects of the top electrode capping. At the same time, the polar o-

phase ratio increases, and the ferroelectricity is enhanced with elevating annealing temperature in the PMA conditions, as shown by the deconvoluted m- and o-phase peaks of the TiN structure in Figure 4-4. As the annealing temperature increases, the t-phase evolution and its feasible transition to the polar o-phase are induced by the grain growth below its critical grain size. The lattice match between the FE film and the top electrode may also contribute to the transition from t- to o-phase by inducing the in-plane compressive stress in the a-b plane and the tensile strain along the c-axis of the t-phase. However, it is reasonable to assume that the TiN and TiN/Ti/TiN structures are subject to a similar lattice stress effect as the 5 nm-TiN barrier layer is deposited on the HAO film in the TiN/Ti/TiN structure. This factor leads to a negligible difference between the phase evolutions of the two structures. Regarding the dependence of phase transitions on the presence of the inserted Ti layer, it should be noted that distinct (004) anatase TiO_2 peaks, denoted as A(004), appear for all annealing conditions of the TiN/Ti/TiN structure, while a comparatively lower A(004) peak is observed only for the highest 800 °C annealing condition in the TiN structure.[33] This finding implies that the TiO_2 formation is mostly dependent on the presence of the Ti scavenging layer and the high annealing temperature condition, which are the two primary factors required for the enhanced oxygen-scavenging effects further discussed in the following sections.

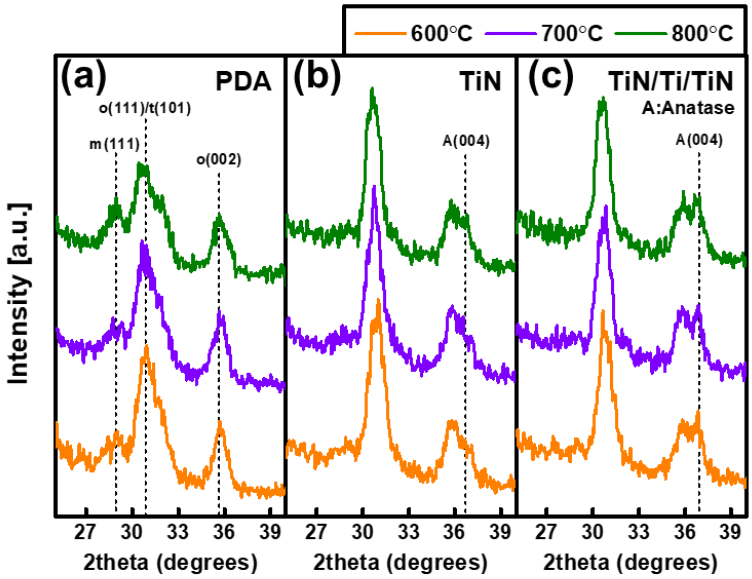

Figure 4-3. Grazing incidence x-ray diffraction (GIXRD) patterns of (a) PDA, (b) TiN PMA and (c) TiN/Ti/TiN PMA conditions at 600-800°C annealing temperatures.

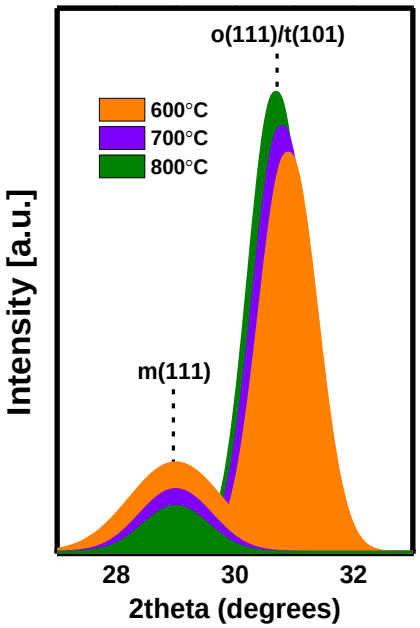

Figure 4-4. Phase transitions of non-polar monoclinic m(111) phase and polar orthorhombic o(111) phase for TiN PMA condition with the increasing annealing temperature.

One of the important parameters attainable from the C-V characteristics of lightly-doped semiconductor-based FE capacitors is the direction of a hysteresis induced by the dominance of either charge trapping or FE switching. The direction of hysteresis is determined by the shifts of two flat band voltages (V_{FB}) during the C-V sweeps in opposite voltage directions. For the p-type Si-based MFIS capacitors, a clockwise C-V hysteresis is generated if the switching of the FE bound charges plays a dominant role, while an anti-clockwise C-V hysteresis is observed if the injected holes or electrons at the interfacial trap sites dominate the V_{FB} shifts.[34] To examine such an effect, HAO-based MFIS capacitors with the TiN and TiN/Ti/TiN top electrodes were fabricated on a lightly-doped p-type Si substrate. It is interesting to note that the C-V characteristics of the MFIS capacitors in Figures 4-5(a)-(c), measured at an ac oscillation frequency of 10 kHz for 600-800 °C annealing conditions, exhibit a transition of the hysteresis direction as the annealing temperature increases from 600 °C to 700 °C. A trap-assisted anti-clockwise capacitance hysteresis is obtained for the 600 °C annealing condition regardless of the top electrode structure. In contrast, the hysteresis is inverted to a FE switching-induced clockwise direction as the annealing temperature increases to 700 °C and 800 °C. Although there is no significant difference between MWs of the TiN and TiN/Ti/TiN structures for all annealing conditions, such transition from anti-clockwise to clockwise hysteresis direction is a reasonable result considering the suppressed non-polar m-phase and increased polar o-phase as

the annealing temperature increases. Additionally, this behavior might also be related to the possible reduction of the trap sites induced by the enhanced oxygen-scavenging effects at high annealing temperature conditions.

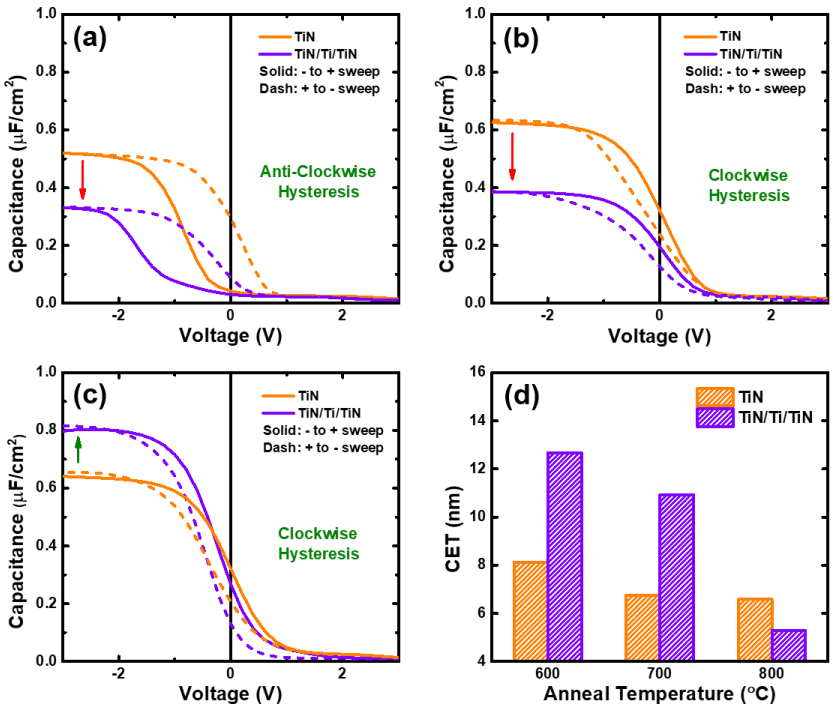

Figure 4-5. Capacitance-voltage (C-V) characteristics of (a) 600°C, (b) 700°C and (c) 800°C-annealed HAO-based MFIS (lightly-doped Si) capacitors with TiN and TiN/Ti/TiN top electrodes. (d) Capacitance equivalent thickness (CET) changes calculated with the accumulation capacitance from each condition.

Accumulation capacitance (C_{acc}) at a voltage region where the majority carriers are fully-accumulated can be efficiently utilized to evaluate CET of a capacitor.[35-36] The CET variation provides valuable information on the structural change in the overall stack of a semiconductor-based capacitor, which leads to different effective voltage distributions at the ferroelectric layer for polarization switching. The C-V characteristics in Figures 4-5(a)-(c) show that C_{acc} of the TiN/Ti/TiN structure is lower than that of the TiN structure for 600 °C and 700 °C annealing conditions. In contrast, C_{acc} of the TiN/Ti/TiN structure eventually exceeds C_{acc} of the TiN structure at the highest 800 °C temperature. The corresponding CET variations in Figure 4(d) are calculated by the equation of

$$\text{CET} = \frac{\epsilon_0 \epsilon_{SiO_2} A}{C_{acc}} \tag{4-1}$$

, where ϵ_0, ϵ_{SiO_2}, A, and C_{acc} represent the vacuum permittivity, dielectric constant of SiO_2, area of the circular top electrode, and accumulation capacitance, respectively. The CET values for both TiN and TiN/Ti/TiN structures commonly decrease as the annealing temperature increases, implying the better crystallization of the HAO films in both cases. However, such variation appears to be more crucial in the Ti-inserted structure with a larger decrease of the CET values. Therefore, it can be inferred that the larger CET values of the TiN/Ti/TiN structure at 600 °C and 700 °C annealing conditions are attributed to both the oxidized anatase TiO_2 and insufficient decomposition of the low-k SiO_2 layer at low annealing temperature conditions. Consequently,

the enhanced oxygen-scavenging process in the Ti-inserted structure at 800 °C triggers a more active decomposition of the low-k SiO_2 layer, resulting in the inversion of the CET values between the two structures.

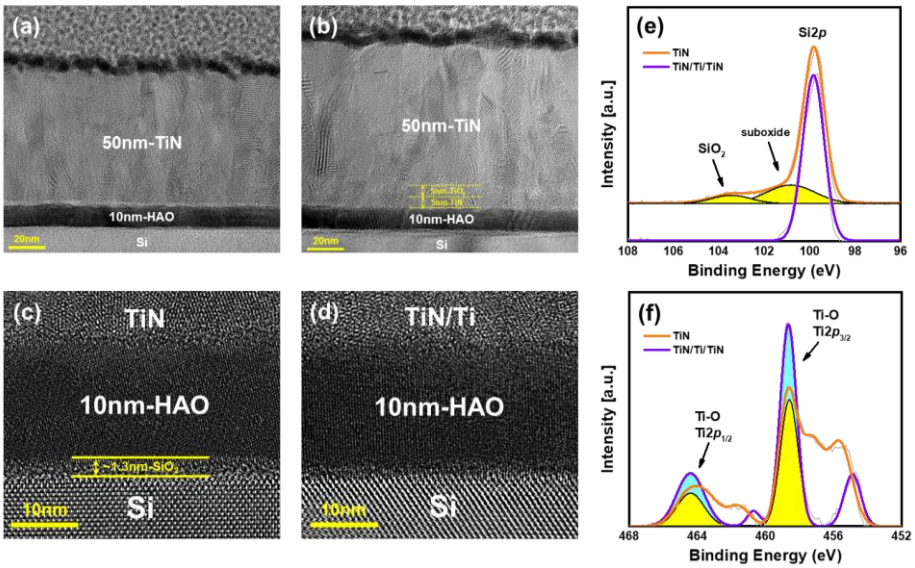

Figure 4-6. Cross-sectional high-resolution transmission electron microscope (HRTEM) images of 800 °C-annealed 10 nm-HAO-based MFIS capacitors with (a) 50 nm-TiN and (b) 50 nm-TiN/5 nm-Ti/5 nm-TiN top electrodes. HRTEM images of (c) ~1.3 nm-thick remaining SiO_2 layer in 800 °C-annealed TiN and (d) decomposed SiO_2 layer in 800 °C-annealed TiN/Ti/TiN structures. X-ray photoelectron spectroscopy (XPS) analysis on (e) Si2p and (f) Ti2p spectra of 800 °C-annealed HAO-based MFIS capacitors with TiN and TiN/Ti/TiN top electrodes.

Structural analysis of SiO_2 decomposition and Ti oxidation at 800 °C annealing condition is conducted via cross-sectional high-resolution transmission electron microscope (HRTEM) images and X-ray photoelectron spectroscopy (XPS) spectra of Si2p and Ti2p for the two different structures. The HRTEM images in Figure 4-6(a) and (b) show the different top electrode structures of TiN and TiN/Ti/TiN with a perceptible distinction of the inserted barrier-TiN and scavenging-Ti layers in the TiN/Ti/TiN structure. The interface images of the structures with the higher resolution in Figures 4-6(c) and (d) confirm that the enhanced oxygen-scavenging phenomenon effectively decomposed the interfacial SiO_2 layer in the TiN/Ti/TiN structure compared to the TiN structure with a ~1.3 nm-thick remaining interfacial SiO_2 layer. The mapping images of energy-dispersive X-ray spectroscopy (EDS) in Figure 4-7 also depict the elemental compositions and interfaces among each layer in the two different structures. The XPS peaks of SiO_2 and suboxide present only for the TiN structure in Figure 4-6(e) coincide with the TEM images. Moreover, the higher Ti-O bonding peaks for the TiN/Ti/TiN structure in Figure 4-6(f) refer to more vigorous oxidation of the inserted Ti layer.

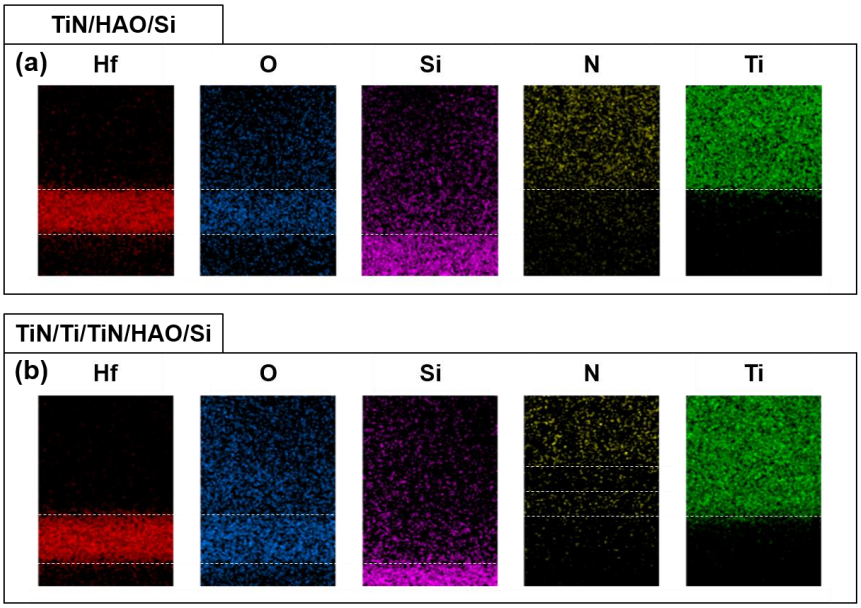

Figure 4-7. Energy-dispersive X-ray spectroscopy (EDS) mapping images of Hf, O, Si, N, and Ti elemental compositions for (a) TiN/HAO/Si and (b) TiN/Ti/TiN/HAO/Si structures.

Besides the physical decomposition of the interfacial layer reducing CET of an MFIS capacitor, it is also essential to analyze the feasible changes of defects or traps involved in the oxygen-scavenging process. A strong frequency dispersion of capacitance characteristics indicates an increase in the trap density as the increased number of traps react with the ac signals at a broad frequency range.[25-26] Furthermore, it is known that the oxygen vacancies (V_o) in the bulk of the HfO_2 layer tend to migrate toward its interface with the underlying SiO_2 layer via a thermodynamic process.[19] This process is the fundamental mean that induces the oxygen-scavenging effect by the active metal layer in the gate stack. Therefore, the frequency dispersions and the changes of D_{it} according to the different annealing temperatures and the presence of the inserted Ti layer must be examined thoroughly.

The frequency dispersions of the capacitance characteristics for the TiN and TiN/Ti/TiN structures at 600-800 °C annealing conditions are evaluated at a frequency range from 1 kHz to 100 kHz, as shown in Figures 4-8(a)-(c). The TiN structure shows more severe frequency dispersions than the TiN/Ti/TiN structure for all annealing temperatures. For further quantitative analysis, maximum D_{it} values within the range of each depletion region are calculated with the measured capacitance and conductance characteristics as plotted in Figure 4-8(d).[37] As expected by the frequency dispersions, the calculated maximum D_{it} values of the TiN/Ti/TiN structure are lower than those of the TiN structure for all annealing conditions. This finding indicates that a promising

effect of reducing the interface traps, such as transporting the decomposed oxygen to the upper Ti layer for oxidation, is achieved in the TiN/Ti/TiN structure. On the other hand, the maximum D_{it} values commonly increase for both TiN and TiN/Ti/TiN structures as the annealing temperature increases from 600 °C to 700 °C, which is a trend opposite to the CET variation. This is possibly attributed to that the thermally-induced migration of the oxygen vacancies from the HAO bulk toward the interface is more active at 700 °C than 600 °C. In contrast, the subsequent step of utilizing the accumulated vacancies for the oxygen transport is not effectively triggered before reaching the optimal 800 °C annealing temperature. As the annealing temperature reaches 800 °C, the maximum D_{it} value of the TiN structure only slightly decreases from ~5.7 × 10^{12} cm^{-2} eV^{-1} to ~5.4 × 10^{12} cm^{-2} eV^{-1}. In contrast, the maximum D_{it} of the TiN/Ti/TiN structure is substantially reduced to the lowest value of ~2 × 10^{12} $cm^{-2}eV^{-1}$ due to the optimal structural and temperature condition for the oxygen-scavenging cycle. Therefore, it is concluded that the Ti-insertion into the TiN-based gate stack is a feasible method to decrease CET and D_{it}.

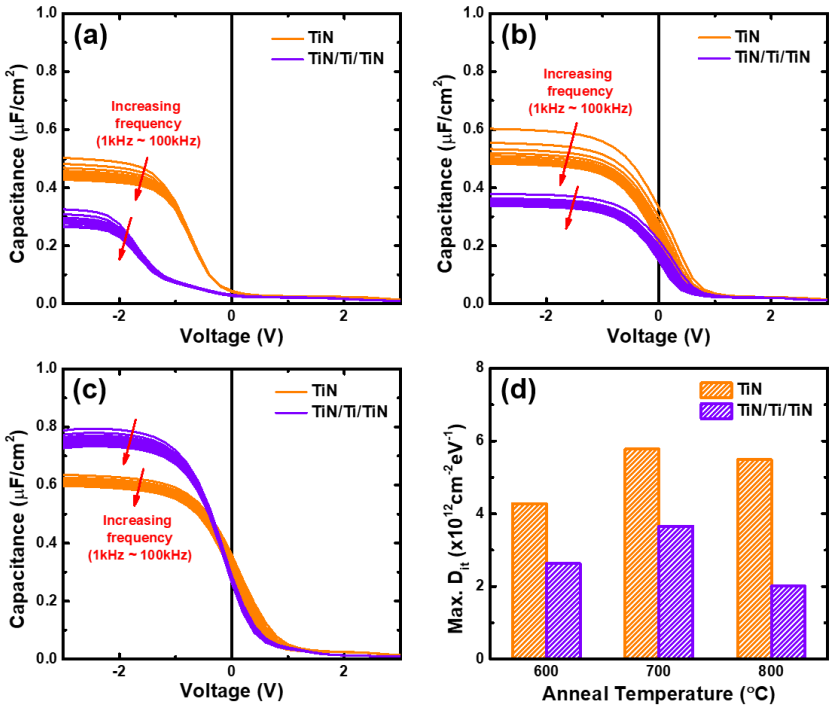

Figure 4-8. Frequency dispersions of capacitance characteristics measured at a frequency range from 1 kHz to 100 kHz for (a) 600 °C, (b) 700 °C, and (c) 800 °C-annealed HAO-based MFIS capacitors with TiN and TiN/Ti/TiN top electrodes. (d) Maximum interface trap density (D_{it}) changes calculated with the measured capacitance and conductance characteristics at the increasing frequencies.

To investigate the dependence of FE performance on the enhanced oxygen-scavenging effects with the inserted Ti layer at 800 °C annealing condition, HAO-based MFIS capacitors on heavily-doped Si substrate were fabricated. It is considered that sufficient charge carriers in the heavily-doped substrate induce sufficient FE-bound charge screening for polarization switching.[38-39] Consequently, the C-V characteristics of the TiN and TiN/Ti/TiN structures annealed at 800 °C in Figure 4-9(a) present a distinct FE switching-induced hysteresis in the clockwise direction. It is notable that the curve shape also resembles the typical butterfly-shaped C-V hysteretic curves of a metal-ferroelectric-metal (MFM) capacitor with a slope induced by the slight depletion behavior of the semiconductor. Similar to the case with lightly-doped Si substrate, C_{acc} of the TiN/Ti/TiN structure appears to be higher than that of the TiN structure. The difference in V_{FB} shifts between the two structures is negligible. Figure 4-9(b) shows the frequency dispersions of capacitance characteristics measured at a frequency range from 1 kHz to 100 kHz. The trend of reduced frequency dispersion with the inserted Ti scavenging layer also matches the lightly-doped Si case. Also, the frequency dispersion of the TiN structure on the heavily-doped Si substrate seems to be more severe than that of the TiN structure on the lightly-doped Si substrate. Accordingly, Figure 4-9(c) plots a relatively large decrease of maximum D_{it} from ~7.7×10^{12} cm^{-2} eV^{-1} to ~2.1×10^{12} cm^{-2} eV^{-1} with the inserted Ti layer on heavily-doped Si compared to that of the lightly-doped Si case, although the reduction of the CET

value is only ~0.18 nm. This result indicates a possible correlation between the oxygen-scavenging effects and the doping concentration of Si. The more easily injected charge carriers from the heavily-doped substrate to the sufficiently-decomposed SiO_2 layer may react with the interface traps, particularly oxygen vacancies, to reduce D_{it}.

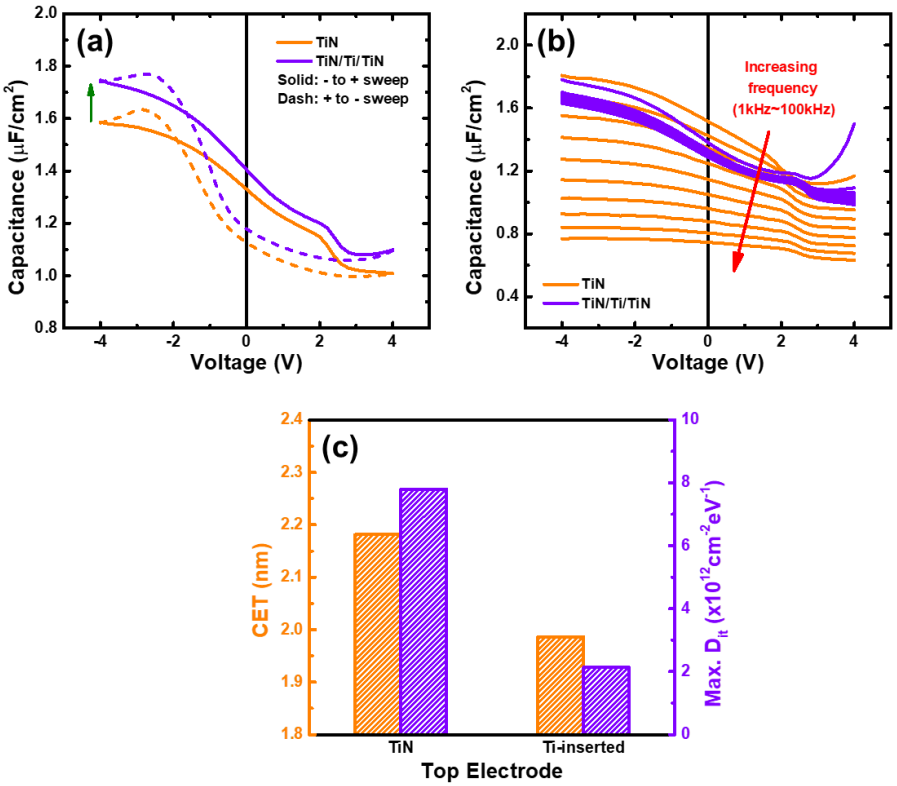

Figure 4-9. (a) Capacitance-voltage (C-V) characteristics and (b) frequency dispersions of 800 °C-annealed HAO-based MFIS (heavily-doped Si) capacitors with TiN and TiN/Ti/TiN top electrodes. (c) Calculated capacitance equivalent thickness (CET) and maximum interface trap density (D_{it}) of each structure.

Based on the above CET and D_{it} variations generated by different annealing conditions with and without the Ti scavenging layer, the general mechanism of the oxygen scavenging process is depicted by the schematic in Figure 4-10(a) and suggested as follows. The oxygen vacancies present in the HAO bulk tend to migrate toward the interface between the HAO and SiO_2 layers as HfO_2 is thermodynamically more stable than the oxidized-SiO_2 with the lower Gibbs free energy.[19,40-41] One of the two primary roles that such migrated oxygen vacancies play is to chemically decompose the oxidized-SiO_2 layer, which is particularly regarded as "oxygen-scavenging" in the overall scavenging phenomenon. The presence of Si in the substrate is also an indispensable component for the chemical decomposition of the SiO_2 layer.[22] The other key role of the migrated oxygen vacancies is that they act as mediators for the scavenged oxygen transport to the upper TiN barrier layer since Ti has a high oxygen solubility and a large positive Gibbs free energy change when forming TiO_x or TiO_2. This effect yields an energy gain compared to the conservation of the remaining SiO_2 layer,[19] and the transported oxygen permeates through the thin TiN barrier layer to complete the scavenging cycle of the high-k TiO_2 oxidation along with the low-k SiO_2 decomposition.

The reduced CET and D_{it} values of the TiN/Ti/TiN structure at 800 °C annealing condition indicate that the larger portion of an applied voltage can be effectively applied to the ferroelectric layer to enhance the polarization switching. This is because the serially-combined capacitance of the interfacial

layers is increased. Also, the reduced interface trap sites can suppress the undesired depolarization field, which degrades the reliability of the ferroelectric switching. The P-V characteristics of the TiN (PDA), TiN (800 °C PMA) and TiN/Ti/TiN (800 °C PMA) structures measured by triangular pulses with a frequency of 1 kHz and an amplitude of 5.5 V are shown in Figure 4-10(b). To avoid the adverse effect by the incomplete charge compensation layer in the lightly-doped Si substrate, the heavily-doped p-type Si substrate was used for this experiment. The PMA conditions substantially improved the FE performance compared with the PDA condition at 800 °C annealing temperature. More importantly, the $2P_r$ value of the TiN/Ti/TiN structure (~52 μC/cm^2) is larger than that of the TiN structure (~39 μC/cm^2) owing to the enhanced scavenging effects of the Ti scavenging layer. The voltage distribution at the HAO layer can be expressed as

$$V_{HAO} = \frac{C_{eq}}{C_{HAO}} V_{applied} \quad (4\text{-}2)$$

, where C_{eq}, C_{HAO}, and $V_{applied}$ represent the equivalent capacitance of the capacitor, the capacitance of the HAO layer, and the applied voltage, respectively. Due to the reduced thickness of the low-k SiO_2 layer, the increased C_{eq} value of the TiN/Ti/TiN structure with the enhanced oxygen-scavenging effects induces a larger voltage distribution at the HAO layer for FE switching than the TiN structure.

Additionally, it is noteworthy that the $2V_c$ value, particularly the negative V_c, of the TiN/Ti/TiN structure (~5.8 V) is lower than that of the TiN structure (~6.6

V). The negative voltage region is related to the negative V_{FB} region, where a transition between accumulation and depletion accompanies the polarization switching in a p-type MFIS capacitor. Therefore, the shifted negative V_{FB} indicates effectively reduced positively-charged oxygen vacancies at the HAO film and SiO_2 layer interface, which agrees with the reduced CET and D_{it} values in the TiN/Ti/TiN structure at high annealing temperature conditions.

Finally, the FE switching endurance characteristics of the TiN and TiN/Ti/TiN structures for 800 °C annealing condition are measured at 80 °C, as presented in Figure 4-10(c). $2P_r$ of the TiN/Ti/TiN is uniformly maintained over 10^9 cycles with a cycling voltage amplitude of 2.5 V, whereas a moderate $2P_r$ degradation is observed for the TiN structure. The $2V_c$ values of the TiN structure also start increasing at the same cycle where its $2P_r$ values begin to decrease, indicating that the fatigue occurs after approximately 10^6 cycles. It is commonly acknowledged that the intervention of the oxygen vacancies with ferroelectric dipoles during the polarization switching is a critical origin of a fatigue or wakeup phenomenon in ferroelectric devices.[42-44] Therefore, these endurance data corroborated the oxygen vacancy-mediated oxygen-scavenging effect in the TiN/Ti/TiN structure. Figure 4-10(d) shows the leakage characteristics of the two structures for the 800 °C annealing condition. Despite eliminating the interfacial SiO_2 layer, the TiN/Ti/TiN structure showed a slightly decreasing leakage current density compared with the TiN structure. This result is consistent with the assertion that the TiN/Ti/TiN structure involves

lower oxygen vacancy concentration in the HAO layer.

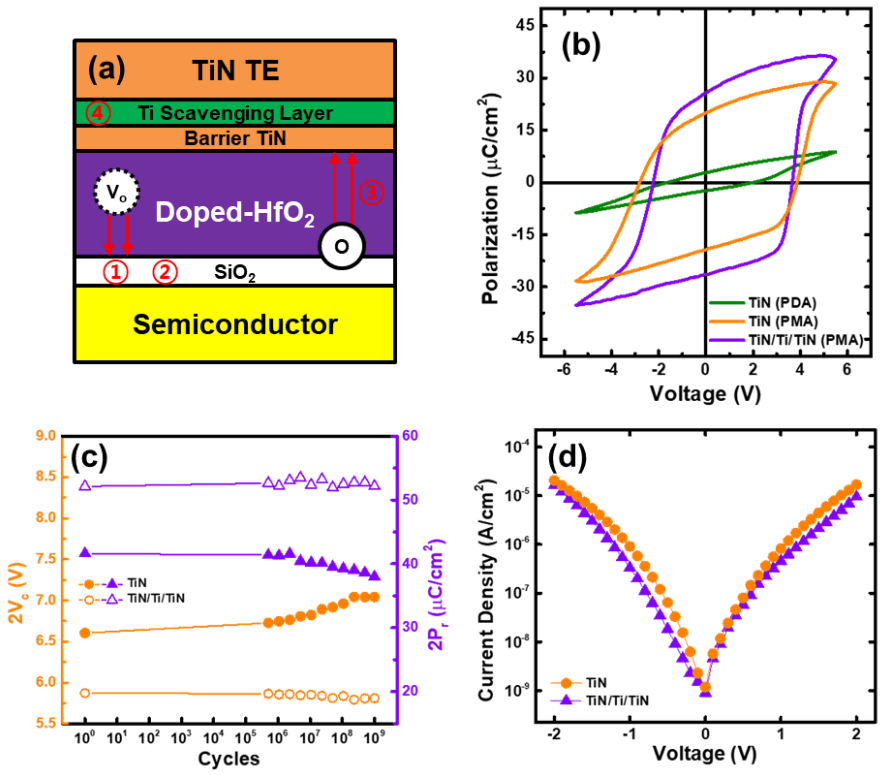

Figure 4-10. (a) Schematic of TiN/Ti/TiN MFIS structure showing the overall mechanism of the oxygen-scavenging process. (b) Polarization-voltage (P-V) characteristics of 800 °C-annealed HAO-based MFIS (heavily-doped Si) capacitors with TiN and TiN/Ti/TiN top electrodes for post-deposition annealing (PDA) and post-metallization annealing (PMA) conditions. (c) Endurance and (d) leakage current density of 800 °C-annealed TiN and TiN/Ti/TiN structures measured at an elevated stage temperature of 80 °C.

4.4. Conclusion

The dependence of the oxygen-scavenging process on the presence of a Ti scavenging layer and different annealing temperatures was investigated in HAO-based MFIS capacitors. From the C-V characteristics, the CET value of the TiN/Ti/TiN structure was steadily reduced to be lower than that of the TiN structure at 800 °C annealing condition by the actively-triggered oxygen-scavenging effects. This finding was confirmed by the HRTEM images and XPS analysis of the two structures. Consequently, the larger voltage distribution at the ferroelectric layer in the TiN/Ti/TiN structure led to the enhanced $2P_r$ (~52 μC/cm^2) and reduced $2V_c$ (~5.8 V) values compared to the TiN structure ($2P_r$ ~ 39 μC/cm2 and $2V_c$ ~ 6.6 V). Quantitative analysis on frequency dispersion and maximum D_{it} calculations verified that the Ti scavenging layer also significantly reduced the interface traps at the 800 °C annealing condition. This effect also led to the fatigue- or wakeup-free endurance and restrained leakage current characteristics as a promising optimization step for HAO-based MFIS memory devices with the requirement of high-temperature annealing conditions.

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5. Conclusion

This dissertation extensively examines the switching mechanism in semiconductor-based capacitors utilizing doped-HfO_2 ferroelectric materials. This analysis aims to gain a comprehensive understanding of the potential limitations in memory operation within semiconductor-based ferroelectric memory devices, with the ultimate goal of optimizing the characteristics of MW.

First, the focus is on investigating the general relationship between the thickness of doped-HfO_2 ferroelectric films and their switching operation in MFIS structures. The serial capacitance effect caused by the interfacial oxide layer leads to less voltage distribution across the ferroelectric film during switching. Additionally, the depletion operation in the semiconductor induces voltage distribution within the depletion layer prior to ferroelectric switching, necessitating a thicker film for optimal ferroelectric switching. It is observed that highly-doped Si substrates can be used as metallic electrodes with sufficient majority carriers, enabling the presence of space charges in opposite polarity for bi-polar switching. On the other hand, lightly-doped Si substrates lack sufficient majority carriers, resulting in a large depletion layer with insufficient space charges in opposite polarity for bi-polar switching.

Second, the characteristics of MW are evaluated in various metal-ferroelectric-metal-insulator-semiconductor MFMIS and MFIS structures using lightly-doped Si substrates. MFMIS structures with varying area ratios of

MFM and MIS stacks are fabricated to induce larger ferroelectric voltages for switching, and only uni-polar switching is observed under accumulation conditions. This emphasizes the significance of inversion charges in the semiconductor, as they contribute more to the screening of ferroelectric bound charges during switching than the larger field induced at the ferroelectric layer. MFIS capacitors, with static dipoles formed by post-deposition annealing for inversion, exhibit considerable polarization switching. However, a significant back-switching of the switched polarization caused by the depolarizing field is also observed. Nonetheless, when the thickness of the insulator is reduced from 5 nm to 1.5 nm, symmetric bi-polar switching behavior and a notable reduction in back-switching are demonstrated, leading to an MW characterized by switching-induced capacitance hysteresis.

Third, an oxygen-scavenging effect is achieved by adding Ti, which has high oxygen solubility, to the top electrode, followed by high-temperature post-metallization annealing. The Ti scavenging layer triggers a structural decomposition of the SiO_2 interface layer and a reduction in the interface trap density. The effect of interface decomposition is verified through the reduction in CET observed by C-V analysis and the structural images obtained from HRTEM. As the MFIS capacitor with the reduced interface layer exhibits enhanced ferroelectric switching operation and retention property, it is anticipated that the oxygen-scavenging effect can be a promising pathway for the optimization of MW characteristics in the future research.

Curriculum Vitae

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I. Educations

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Department of Electrical and Computer Engineering
University of Illinois at Urbana-Champaign, IL, USA

2016. 08. – 2023. 08 Integrated M. S. & Ph. D.
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II. Research Areas

1. Atomic layer deposition (ALD) of doped-HfO_2 thin film

- Analysis on ferroelectricity of doped-HfO_2 films with various dopants (Zr, Al)
- Optimization of deposition process for high endurance and low leakage property
- Application of various electrodes (TiN, W, Mo, Ru) for enhanced ferroelectricity
- Investigation on the effect of impurity on ferroelectric performance

2. Ferroelectric field-effect-transistor (FeFET) device fabrication

- Gate-last fabrication of FeFET device with Al-doped HfO_2 ferroelectric film
- Shallow trench isolation (STI) for device isolation
- Ion implantation for well and source/drain doping
- Optimization of film deposition and etch profile for gate stack formation

3. Semiconductor-based ferroelectric capacitor with doped-HfO_2 film

- Switching kinetics of doped-HfO_2 ferroelectrics on semiconductor
- Interfacial engineering for equivalent oxide thickness (EOT) reduction
- Capacitance and frequency dispersion analysis for interface trap calculation
- Fabrication of standard metal-oxide-semiconductor capacitor (MOSCAP)
- Analysis on memory window of semiconductor-based ferroelectric capacitor

III. Experimental Skills

1. Deposition and device fabrication methods

- Atomic layer deposition of oxide materials
- DC & RF reactive sputtering and E-gun evaporation of metal electrodes
- Furnace for drive-in and dry oxidation
- LPCVD for poly-Si and nitride deposition
- Maskless pattern systems for PR patterning
- RIE and ICP etcher for dry etching

- HDPCVD for oxide gap-fill
- Wet chemical etching and cleaning for surface treatment
- RTA for film crystallization
- Ion implantation for well and source/drain doping

2. Analysis methods

- X-Ray Fluorescence Analyzer (XRF, Thermo scientific, ART Quant'X EDXRF) for analysis of composition and layer density of films
- X-Ray Diffractometer (XRD, PANalytical, X'Pert PRO MPD) for measurement of X-Ray diffraction patterns of films
- X-ray photoelectron spectroscopy (XPS, UK VG, Sigma Probe) for depth profile and chemical analysis of films
- Transmission Electron Microscopy (TEM, JEOL, JEM-2100F, JEM-3000F, JEM-200CX) for microstructure analysis of thin film
- Energy Dispersive Spectroscopy (EDS, Oxford Instrument, AZtec) incorporated by Scanning Transmission Electron Microscopy (STEM, JEOL, JEM-2100F, JEM-3000F) for elemental analysis
- Scanning electron microscopy (SEM, Hitachi, S-4800) for analysis of the grain size of crystallized films
- Spectroscopic Ellipsometer (SE, J.A. Woollam, M-2000) for analysis of optical properties and thicknesses of thin films
- Four points probe for resistivity measurement of metals and conducting materials
- Pulse generator (Agilent, 81110A/81111A) and digital oscilloscope (Tektronix, TDS 684C) for pulse switching measurements

- Ferroelectric tester (TF 2000, aixACCT) for ferroelectric characterization
- Impedance analyzer (HP 4194A) for capacitance characterization
- Hall measurement (BIO-RAD, HL550PC) for carrier density measurement

IV. Academic Honors

1. Best Poster Award, 12th Japan-Korea Conference on Ferroelectrics, Nara, Japan (August 2018)

List of Publications

1. Referred Journal Articles (SCI)

1.1 Domestic

1.2 International

1. Young Hwan Lee, Han Joon Kim, Taehwan Moon, Keum Do Kim, Seung Dam Hyun, Hyeon Woo Park, **Yong Bin Lee**, Min Hyuk Park, and Cheol Seong Hwang*, "Preparation and characterization of ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ thin films grown by reactive sputtering", *Nanotechnology*, 28, 30, 305703 (2017)

2. Yu Jin Kim, Hyeon Woo Park, Seung Dam Hyun, Han Joon Kim, Keum Do Kim, Young Hwan Lee, Taehwan Moon, **Yong Bin Lee**, Min Hyuk Park, and Cheol Seong Hwang*, **"**Voltage Drop in a Ferroelectric Single Layer Capacitor by Retarded Domain Nucleation", *Nano Letters,* 17, 7796-7802 (2017)

3. Taehwan Moon, Hyun Jae Lee, Keum Do Kim, Young Hwan Lee, Seung Dam Hyun, Hyeon Woo Park, **Yong Bin Lee**, Baek Su Kim, and Cheol Seong Hwang*, "Diode Property and Positive Temperature Coefficient of Resistance of $Pt/Al_2O_3/Nb:SrTiO_3$", *Advanced Electronic Materials*, 4, 12, 1800388 (2018)

4. Seung Dam Hyun, Hyeon Woo Park, Yu Jin Kim, Min Hyuk Park, Young Hwan Lee, Han Joon Kim, Young Jae Kwon, Taehwan Moon, Keum Do Kim, **Yong Bin Lee**, Baek Su Kim, Cheol Seong Hwang*, "Dispersion in Ferroelectric Switching Performance of Polycrystalline $Hf_{0.5}Zr_{0.5}O_2$ Thin Films", *ACS Applied Materials & Interfaces,* 10 (41), 35374-35384 (2018)

5. Young Hwan Lee, Seung Dam Hyun, Hae Jin Kim, Jun Shik Kim, Chanyoung Yoo, Taehwan Moon, Keum Do Kim, Hyeon Woo Park, **Yong Bin Lee**, Baek Su Kim, Jangho Roh, Min Hyuk Park*, Cheol Seong Hwang*, "Nucleation-Limited Ferroelectric Orthorhombic Phase Formation in $Hf_{0.5}Zr_{0.5}O_2$ Thin Films", *Advanced Electronic Materials,* 1800436 (2018)

6. Keum Do Kim, Yu Jin Kim, Min Hyuk Park, Hyeon Woo Park, Young Jae Kwon, **Yong Bin Lee**, Han Joon Kim, Taehwan Moon, Young Hwan Lee, Seung Dam Hyun, Baek Su Kim, Cheol Seong Hwang*, "Transient Negative Capacitance Effect in Atomic-Layer-Deposited $Al_2O_3/Hf_{0.3}Zr_{0.7}O_2$ Bilayer Thin Film", *Advanced Functional Materials*, 1808228 (2019)

7. Hyeon Woo Park, Jangho Roh, **Yong Bin Lee**, and Cheol Seong Hwang*, "Modeling of Negative Capacitance in Ferroelectric Thin Films", *Advanced Materials*, 1805266 (2019)

8. Baek Su Kim, Seung Dam Hyun, Taehwan Moon, Keum Do Kim, Young Hwan Lee, Hyeon Woo Park, **Yong Bin Lee**, Jangho Roh, Beom Yong Kim, Ho Hyun Kim, Min Hyuk Park, and Cheol Seong Hwang*, "A comparative study on the ferroelectric performances in atomic layer deposited $Hf_{0.5}Zr_{0.5}O_2$ thin films using tetrakis (ethylmethylamino) and tetrakis (dimethylamino) precursors", *Nanoscale Research Letters,* (2020)

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Abstract in Korean

도핑된 하프늄 옥사이드 물질에서의 강유전성 연구가 처음 시작된 이후로 반도체 기반 메모리 소자에 이를 적용하기 위한 광범위한 연구가 진행되고 있다. 에너지 밴드갭이 크고 실리콘 반도체와의 호환성이 우수한 특성으로 인해 고성능 상보적 금속-산화막-반도체 (CMOS) 소자로 적용 범위가 확대되었다. 한편, 반도체 내에서 발생하는 복잡하고 비선형적인 전하의 거동으로 인해 금속-강유전체-절연체-반도체 (MFIS) 구조에서의 강유전 스위칭 매커니즘을 체계적으로 이해하기에 어려움이 있다. 강유전 물질과 실리콘 기판 사이 계면에 형성되는 산화막을 통해 전하 주입이 발생하면 강유전체의 구속 전하 스크리닝이 방해를 받게 된다. 이로 인해 스위칭된 분극이 유지되지 못하거나 메모리 윈도우 (MW) 특성이 감소하는 문제가 발생하여 메모리 장치로서의 기능이 심각하게 저하될 수 있다. 본 박사 학위 논문에서는 MFIS 구조에서의 전반적인 강유전 스위칭 매커니즘을 정리하고, MW 특성을 감소시킬 수 있는 여러 문제들에 대한 해결 방안을 제시한다.

첫번째로 MFIS 구조에서 다르게 나타나는 전압 분배 특성을 고려하여 도핑된 하프늄 옥사이드 박막의 최적 두께를 평가한다. 직렬로 연결된 산화막 계면층과 반도체 공진층의 커패시턴스 효과로 인해 최적의 강유전 스위칭을 위해서는 금속-강유전체-금속 (MFM) 구조 대비 더 두꺼운 박막을 필요로 한다. 또한, 반도체 내의 캐리어 농도와 강유전 스위칭 거동 간의 관계성을 보다 깊게 이해하기 위해 저농도와 고농도로 도핑된 실리콘 기판 구조에서 나타나는 스위칭 매커니즘에 대해 정리한다.

두번째로 다양한 MFIS 구조를 제작하여 저농도로 도핑된 실리콘 기판 구조에서 강유전 스위칭을 유도하고 이에 따른 MW 특성을 평가한다. 강유전층에 스위칭을 일으킬 수 있을 만큼 충분한 전압

분배를 유도하거나 반도체 내에 반전 전하를 형성하여도 계면 산화막으로 인해 강유전체의 구속 전하 스크리닝이 방해를 받게 되어 불균형적인 스위칭이 일어난다. 또한, 강유전체의 분극과 반대 방향의 필드를 형성하여 스위칭된 분극이 뒤집히는 문제가 발생한다. 하지만, 계면 산화막층의 두께 감소를 통해 이러한 문제점들을 개선하여 균형적인 스위칭에 의한 MW 특성을 확인한다.

세번째로는 앞선 연구 결과들을 통해 관찰한 계면층의 중요성을 고려하여 계면에 필연적으로 형성되는 산화막을 구조적으로 제거하기 위해 산소 스케빈징 효과를 이용한다. MFIS 구조에서 산화 작용이 뛰어난 Ti 물질을 상부 전극에 삽입하고 고온 열처리 조건에 노출시켜 계면 산화막이 분해되는 현상을 실험적으로 증명한다. 이러한 계면 산화막의 물리적인 두께 뿐만 아니라 계면에 존재하는 트랩 밀도의 감소로 인해 스위칭 거동 및 분극의 보존 성능이 향상되어 MFIS 구조에서의 MW 특성을 최적화 할 수 있는 효율적인 가능성을 제시한다.

주요어: CMOS, MFIS, 메모리 윈도우, 공진층, MFM, 커패시턴스 효과, 캐리어 농도, 강유전 스위칭, 계면 산화막, 반전 전하, 산소 스케빈징, 트랩 밀도

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