PH.D. DISSERTATION

A 13.2 kSPS DATA-RATE 5.1 GΩ INPUT IMPEDANCE READ-OUT SYSTEM FOR BRIDGE SENSORS

브리지 센서 감지를 위한 13.2 kSPS 데이터-레이트, 5.1-GΩ 입력 임피던스 판독 시스템

BY

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AUGUST 2023

DEPARTMENT OF ELECTRICAL AND
COMPUTER ENGINEERING
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이 논문을 공학박사 학위논문으로 제출함

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서울대학교 대학원

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박 준 영

박준영의 공학박사 학위논문을 인준함

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ABSTRACT

A 13.2 kSPS DATA-RATE 5.1 GΩ INPUT IMPEDANCE READ-OUT SYSTEM FOR BRIDGE SENSORS

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In the thesis, a read-out system for bridge sensors that can vary from hundreds of ohms to a few mega ohms is proposed. The proposed system includes a low-noise energy efficient capacitively-coupled instrumentation amplifier (CCIA), followed by an incremental delta-sigma analog-to-digital converter (I-ADC). CCIA is the high energy efficient IA topology by using a single amplifier among IA topologies, but its input impedance is low compared to other topologies. The proposed CCIA has a fine current compensation loop (FCCL), making the current seen at the CCIA input terminal small with a positive-feedback loop (PFL). The offset and 1/*f* noise of the CCIA are suppressed by correlated double sampling (CDS) techniques due to CCIA reset time. Residual low-frequency noise is reduced by the system-level chopping technique at a frequency of 13.2 kHz. Also, the sensor offset

cancellation technique is applied to cancel the sensor offset voltage from resistance mismatch of the bridge sensor. An 18-bit I-ADC operates a sampling clock of 4 MHz with a third-order cascade of integrators (CoI) filter. A prototype chip was fabricated in a 0.13 μm CMOS process with an entire area of 5.264 mm^2, drawing 1.32 mA at 5 V supply. This prototype with a gain of 128 and a data-rate of 13.2 kSPS can boost the input impedance to 5.1 GΩ, which is 1153 times the non-boosting, while consuming 2% of the additional power consumption. It has ±350 mV sensor offset voltage cancellation and 2.4 μVrms input referred noise, regardless of using FCCL within an input range of 4.8 V.

Keywords: Pressure Sensor, bridge sensor, capacitively-coupled chopper instrumentation amplifier (CCIA), input impedance, impedance boosting, 1/*f* noise, read-out system, system-level chopping, incremental delta-sigma analog-to-digital converter (ADC), sensor offset cancellation.

Student Number: 2016-20906

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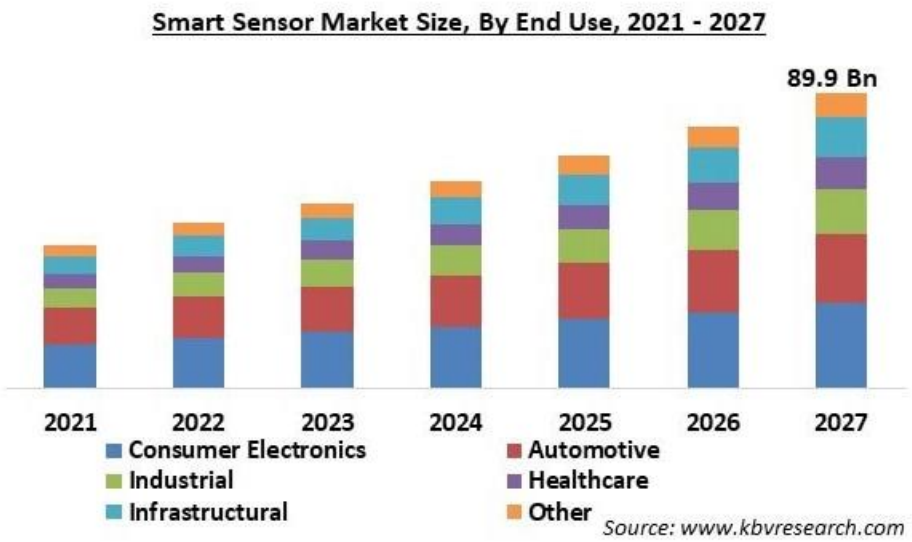
INTRODUCTION

1.1 MARKET SIZE OF PRESSURE SENSORS SYSTEM



Source: KBV Research, 2021

Fig.1.1.1. Forecast of growth in smart sensor market in 2021

As time goes by, many electronic devices around our lives have been used to make our lives more convenient, and each electronic device has several types of smart

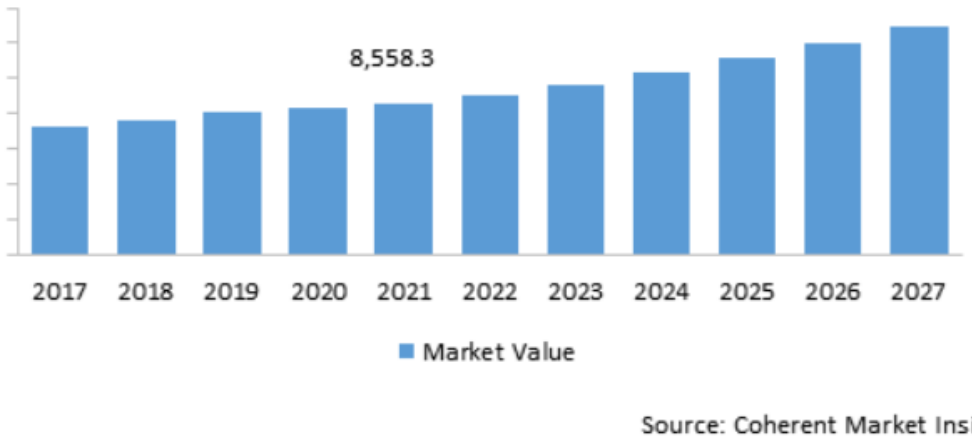


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Fig.1.1.2. Forecast of growth in pressure sensor market

sensors embedded in it.

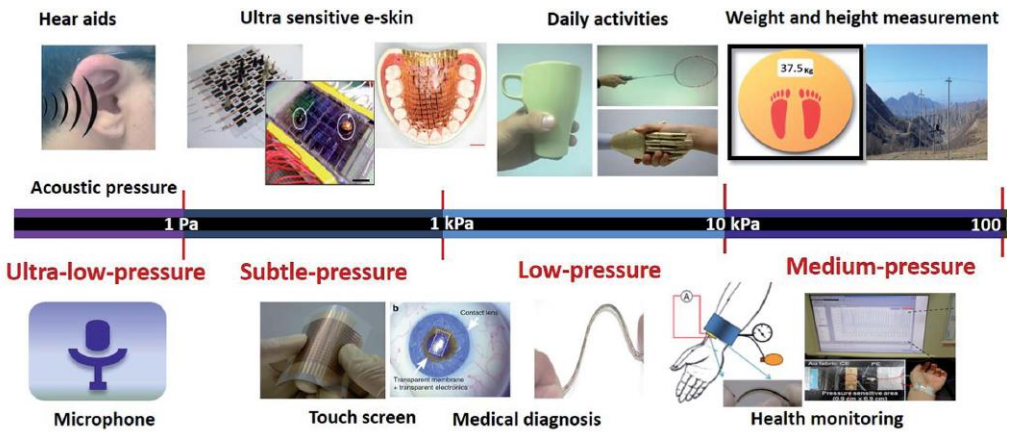
Fig.1.1.1. is a graph that forecasts the growth of the smart sensor market size from 2021 to 2027 announced by KBV research in 2021.sensors in one electronic device. The figure shows the expected market size amount for each year according to the use of smart sensors. Representative application fields of smart sensors include consumer electronics, automotive, industry, healthcare, and infrastructural applications. The field that occupies the largest market share is consumer electronics, which includes home appliances and smartphones, and touch sensors and CMOS image sensors (CIS) are used here. In the next automotive application, a pressure sensor or a force sensor is used among smart sensors, and it is also used for malfunction and danger detection functions in the field, and an ultrasonic sensor used in a parking assistance system is applicable. In other fields, it is also used for detecting defects in industrial products or detecting human heart rate

and electromyography (EMG). The cases in which smart sensors are used around us are becoming more and more diverse.

Fig.1.1.2. is a graph showing comprehensive market growth indicators for pressure sensors used in various fields mentioned above. The pressure sensor is used for measuring the amount of pressure applied to an object. The sensors are used in a wide range of products and applications such as medical devices, automobiles, electronics, and more. The main factors of the driving the market growth are growing industrial automation and the changing manufacturing environment. The increasing usage of pressure sensors in the automotive industry is predicted to drive the market's growth during the forecast period.

Due to the rising usage of force sensors in the Internet of Things (IoT), there is a predicted notable growth in the global force sensors market in the forecase period of 2020-2027, as shown in the figure. The various industries such as automotive, medical, and consumer electronics are grown rapidly by adopting the IoT technology. Users can communicate with these advanced IoT devices with the help of pressure and other physical parameters via pressure sensors.

1.2 PRESSURE SENSORS



[1.2.1]

Fig.1.2.1. The diagram of pressure regimes and the relevant applications [1.2.1].

The development of pressure sensors has enabled the successful applications in mobile devices, continuous health monitoring, intelligent robotics, and electronic skin [1.2.1] - [1.2.3]. According to Fig.1.2.1, the relevant applications of pressure regimes are described in a diagram. Depending on the pressure range, there are various applications as shown in the figure and the method of manufacturing the pressure sensors are also different depending on the usages. Piezo-resistive pressure sensors have been actively investigated because of their structure and fabrication process simplicity, a broad range of pressure detection (1 Pa – 100 kPa) as shown in Fig.1.2.1., easy signal processing, inherent

flexibility, and high sensitivity [1.2.1] - [1.2.4]. Metal particles, nanowires, polymers, and carbon nanotubes (CNTs) have been used as active materials for piezoresistive pressure sensors [1.2.1] - [1.2.7]. Theses piezo-resistive sensors have advantages in the physical properties of high conductivity and flexibility, so they are suitable for wearable and mobile applications, such as ultra-sensitive e-skin, touch screen, health monitoring devices, and so on.

1.3 BRIDGE TYPE SENSOR READ-OUT SYSTEM

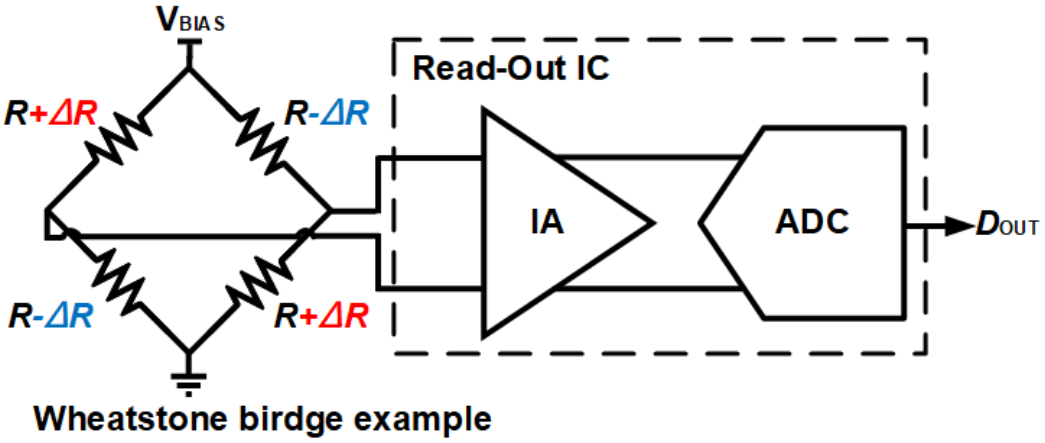


Fig.1.3.1. Bridge type read-out system.

Fig.1.3.1 is shown the bridge type read-out system. The system consists of a Wheatstone bridge composed of sensors and a read-out integrated circuit (IC). The read-out IC includes an instrumentation amplifier (IA) and an analog-to-digital converter (ADC). There are several types of the bridge type sensors, such as load cells, strain gauges, and force-sensitive resistors (FSRs).

Each type sensor has advantages and disadvantages, compared to other types of sensors. The load cell is commonly known as force transducers. The cell converts an input mechanical force as load, weight, tension, compression or pressure into an electrical output signal that can be measured. A typical load cell has a sensitivity rating in mV/V and is

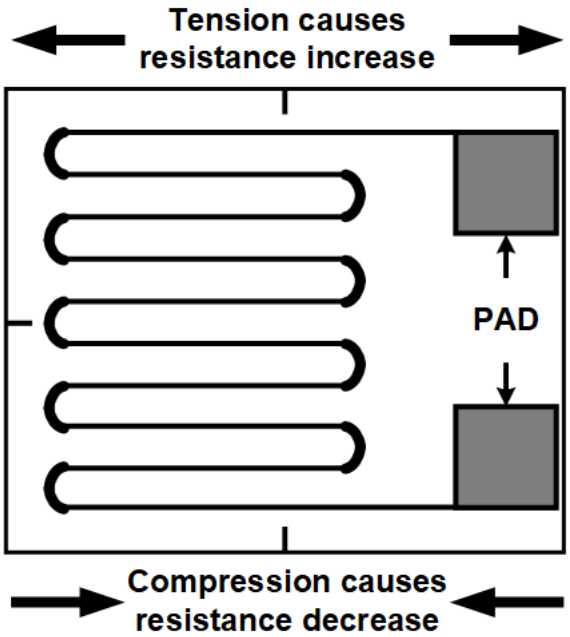


Fig.1.3.2. Working principle of a strain gauge.

usually specified in 1 mV/V – 3 mV/V range. It has better accuracy, which is <0.1 % of the full-scale, but it is bulky in size and rigid in construction.

Strain gauge sensors is shown in the Wheatstone full-bridge example of Fig.1.3.1. The gauge is a sensor that measures the change in electrical resistance, when the strain changes. Strain is a deformation or displacement of a material caused by a stress as shown in Fig.1.3.2. The stress can be defined as the amount of force exerted on a material, which is then divided by the cross sectional area of the material. The strain gauge sensors are cheap in manufacture process and small to handle easily, but theses sensors are required to be calibrated, in order to use perfectly and take reading, since each resistor in the sensors

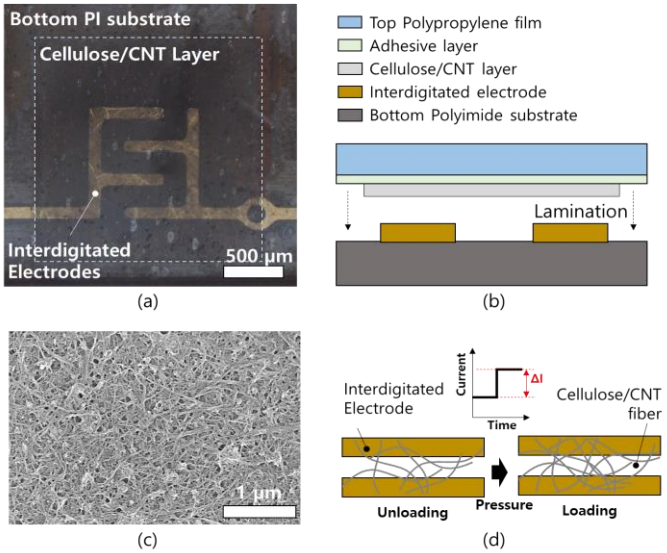


Fig.1.3.4. (a) Magnified optical image of a force sensing element (b) cross-sectional schematic illustration of the force sensor (c) SEM image of the cellulose/CNT fibers (d) operating principle of the cellulose/CNT fibers.

can have own offset that makes the signal non-linear.

FSRs are a large and growing group of embedded components, with many new sensor types having been introduced in recent years [1.2.4] - [1.2.7]. Fig.1.3.3. is ab example of the FSRs [1.2.4]. Fig.1.3.3(a) is the magnified optical image of a force-sensing element, and a cross-sectional schematic illustration of the sensor showing each component is shown in Fig. 1.3.3(b). A lower polyimide and upper polypropylene substrates are laminated to form a sensor. The lower and upper substrates include an interdigitated electrode and a cellulose/single-walled carbon nanotube (SWCNT) layer. The cellulose/SWCNT layer is deposited by spray coating a co-dispersion aqueous solution of

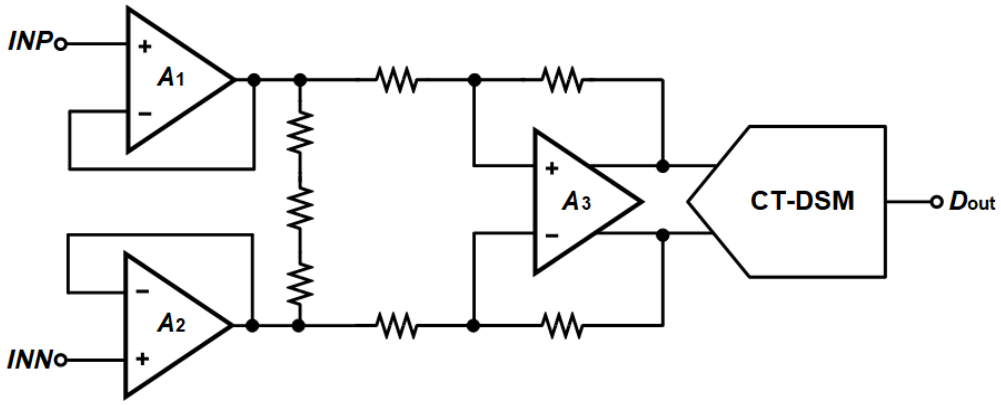


Fig.1.3.6. Block diagram of the three op-amp IA topology [1.3.1].

cellulose and SWCNT. The cellulose/CNT fibers in the dispersion become entangled and stacked, forming numerous pores during spray coating, which can be seen from the electron microscope (SEM) image shown in Fig. 1.3.3(c). Due to the porous structure, the cellulose/CNT thin film has a low Young's modulus, and structural deformation can quickly occur even with a small external force. In other words, it has a very sensitive piezo-resistive characteristic. The sensor operates on a force-dependently changing contact between the cellulose/CNT layer and the bottom interdigitated electrode. When an external force is applied, the porous cellulose/CNT film is compressed, and the number of CNT fibers connecting the interdigitated electrodes increases, forming more conductive pathways (Fig. 1.3.3(d)). When the force is removed, the cellulose/CNT layer returns to its original state, reducing the contact between the CNTs and the electrode, and the current decreases.

In Fig.1.3.1, typical topologies of instrumentation amplifiers for reading out

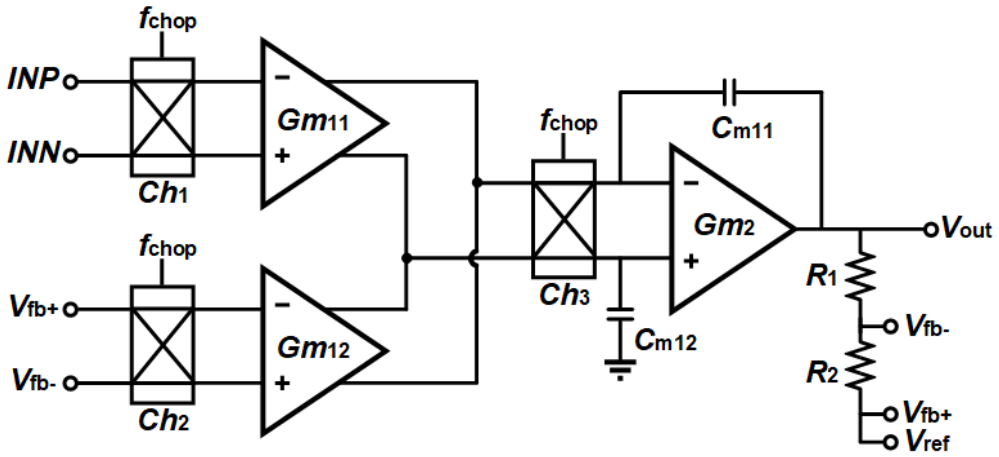


Fig.1.3.7. Block diagram of the CFIA topology [1.3.3].

resistive bridge sensors are three op-amp IA, a current feedback IA (CFIA), and a capacitively-coupled chopper instrumentation amplifier (CCIA). Fig.1.3.4 shows the block diagram of the three op-amp IA followed by a continuous delta-sigma ADC (CT-DSM) [1.3.1]. The traditional three op-amp IA applies an input to the gate of the amplifier and has the advantage of having a high input impedance. Still, it has the worst power efficiency because multiple amplifiers are required and it is hard to apply the low-noise techniques while maintain the input impedance. Also, it is greatly affected by the mismatch between each resistor, since the closed loop gain of the three op-amp IA is determined by the feedback resistor of the structure.

CFIA has better power efficiency than a three op-amp IA, but the power efficiency is still limited because of the two input and feedback trans-conductors [1.3.2]–[1.3.4]. [1.3.2] has implemented a CFIA with a high input impedance, but external resistor

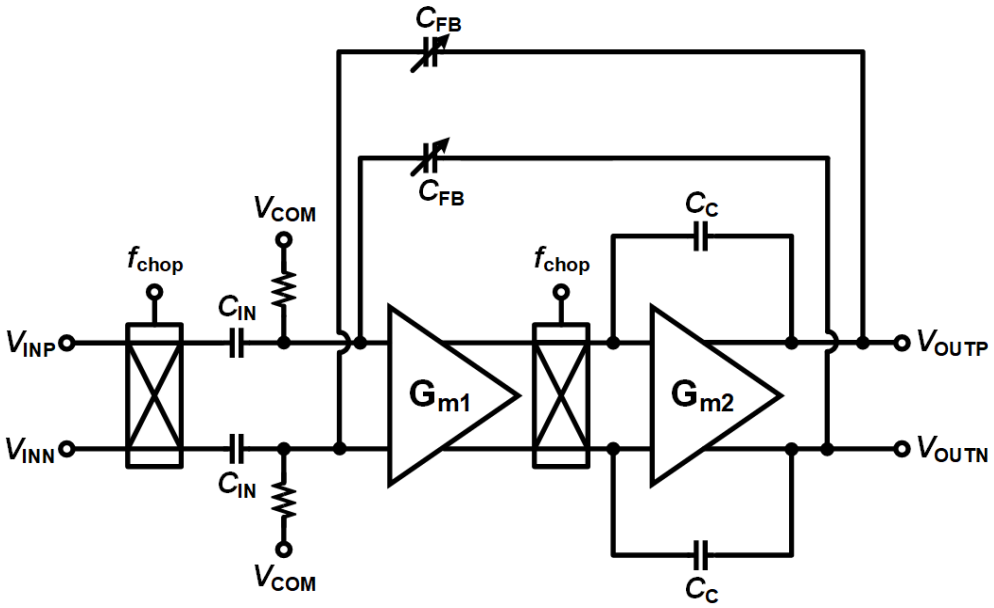


Fig.1.3.8. Block diagram of the CCIA topology [1.3.5].

trimming is required for high gain accuracy. [1.3.3] – [1.3.4] have implemented CFIAs with input choppers to reduce low-frequency noise and offset as shown in Fig.1.3.5. Input choppers (CH_1, CH_2) are placed between the input terminal (*INP*, *INN*), the feedback voltage terminal (V_{fb+}, V_{fb-}) where V_{out} is voltage-divided by R_1 and R_2, and Gm_{11}, Gm_{12} to up-modulate, and then demodulate on CH_3 to reduce *1/f* noise. By using the chopping technique, f_{chop}, parasitic capacitances of Gm_{11}, and input impedance of the CFIA are in inverse proportion, so input impedance is reduced to achieve low noise.

A CCIA is well-known for its high power efficiency and low noise characteristics [1.3.6], [1.3.7] as shown in Fig.1.3.6. It has higher noise efficiency than three op-amps or CFIA structures by designing Gm_1 and Gm_2 as a 2-stage amplifier. Since C_{IN} blocks the

input DC signal, it is easy to perform rail-to-rail sensing. Moreover, it is less affected by mismatch or process variation and has an advantage in gain accuracy because the gain of CCIA is realized by capacitive ratio. However, the input impedance of CCIA is inversely proportional to the chopping frequency (f_{chop}) and input capacitance (C_{IN}). As the input capacitance is increased to improve gain accuracy and noise performance, the input impedance decreases.

In the case of ADC following after the IA, the ADC topology is determined by the target resolution of the bridge sensor system. For high-resolution read-out of sensor signals, delta-sigma ADCs are required, and for ultra-low power systems, successive approximation (SAR) ADC is commonly used.

1.4 MOTIVATION

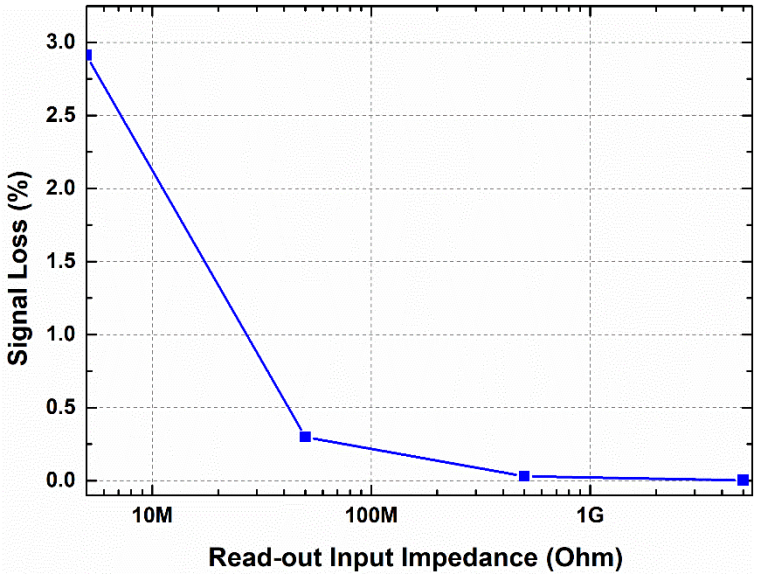


Fig.1.4.1. Signal loss against read-out input impedance @ 100 kΩ.

Bridge sensors are widely used in DC measurement systems that read out resistance values according to input such as pressure, force, or temperature. As the research of sensors continues, the differential output of the sensors can come out to a level of several mV, and to read the corresponding signal, high resolution and high gain are required for the read-out IC [1.3.1] – [1.3.5]. When pressure is applied to the sensors, the resistance of the sensors can vary from thousands of kilo-ohms to hundreds of ohms, depending on the application and the device's material [1.2.4] – [1.2.6]. To read out the signal with a gain

error of less than 0.1%, the input impedance of the read-out IC should be at least a thousand times greater than the sensor resistance as shown in Fig.1.4.1. This relationship can be expressed as:

$$\text{Gain error (\%)} = \frac{Z_{SENSOR}}{Z_{SENSOR}+Z_{IN}} \text{ X } 100 \text{ (\%)}, \tag{1.4.1}$$

where Z_{SENSOR} and Z_{IN} are the sensor impedance and the read-out IC input impedance, respectively. Additionally, power efficiency and linearity are also key design parameters.

1.5 PREVIOUS WORKS

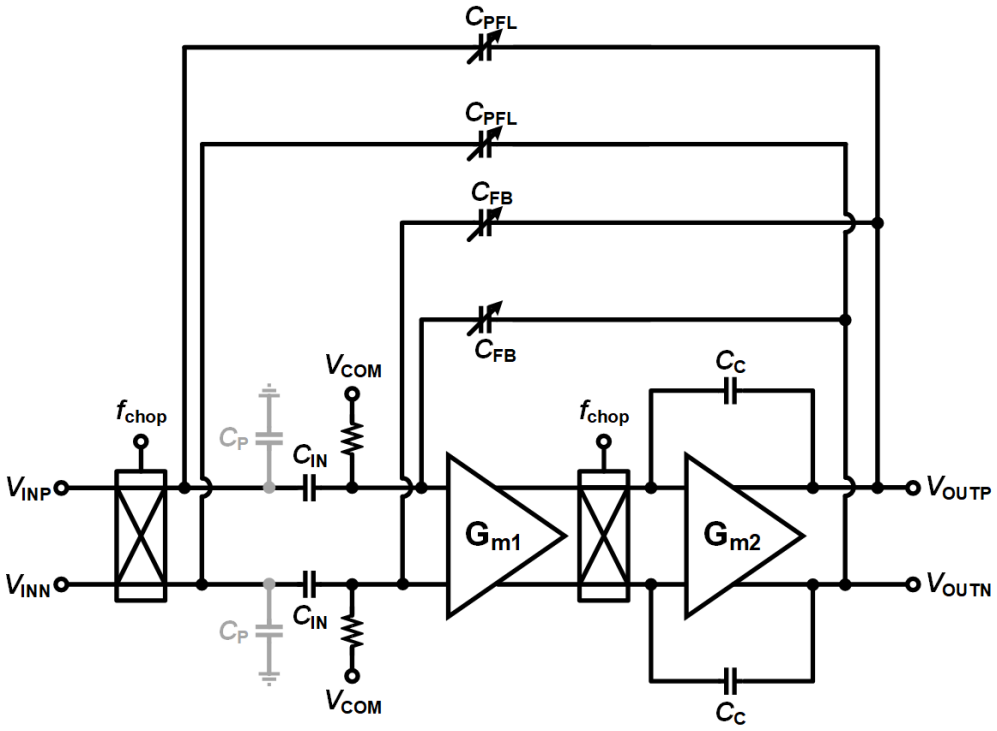


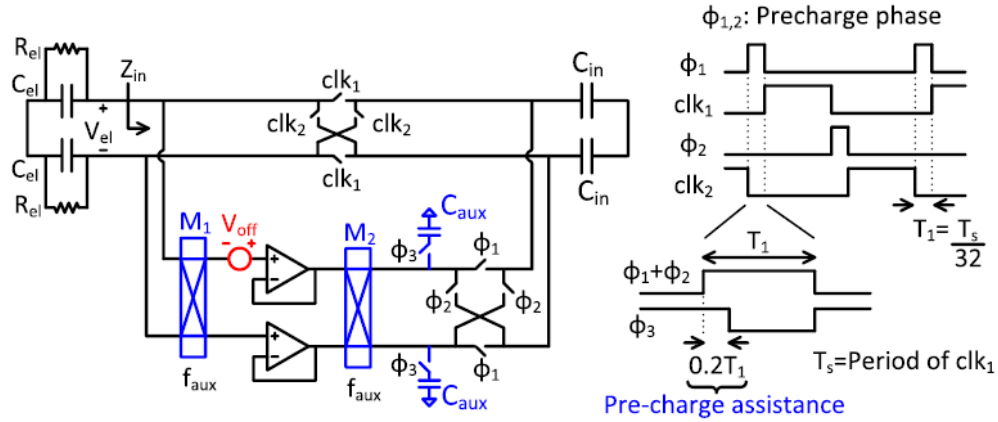
Fig.1.5.1. The block diagram of CCIA with a conventional input impedance boosting loop.

Among the IA topologies, CCIA is a suitable structure for designing an energy efficient bridge sensor read-out system except for the disadvantage of low its input impedance. Therefore, many studies have been researched to solve the problem [1.3.5], [1.5.1] – [1.5.3].

A commonly used input impedance boosting technique is using positive feedback loop (PFL), as shown in Fig.1.5.1 [1.3.5]. This technique minimizes the current flowing into the CCIA through C_{IN} by matching the current flowing through C_{FB} with the current flowing through C_{PFL}. Ideally, it is possible to increase the input impedance by the gain of CCIA. However, as shown in Fig.1.5.1, the parasitic capacitance (C_P) can be up to 40% of the input capacitance (C_{IN}) [1.3.5]. The effect of C_P on the input impedance can be expressed as

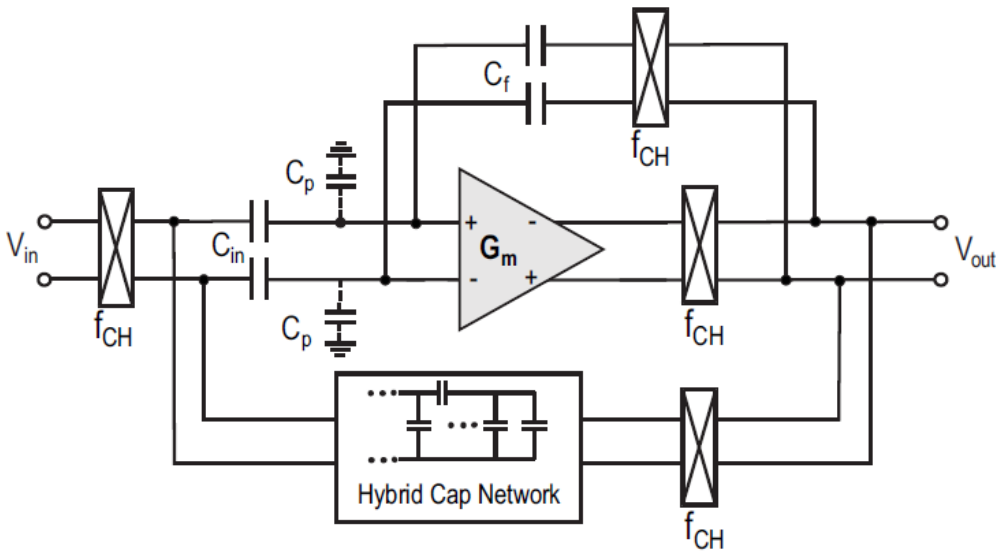
$$Z_{IN}=\frac{G}{2f_{chop}(G\cdot C_P+C_{IN})}, \tag{1.5.1}$$

where Z_{IN} is the input impedance of CCIA, C_{IN} is the input capacitor of CCIA, G is the gain of CCIA determined by the ratio C_{IN} / C_{FB}, and f_{chop} is the chopping frequency. According to the equation (1.5.1), the parasitic capacitance C_P is multiplied by the gain of CCIA, limiting the efficiency of the PFL. If C_P does not exist, it has the impedance boosting effect as G ideally.



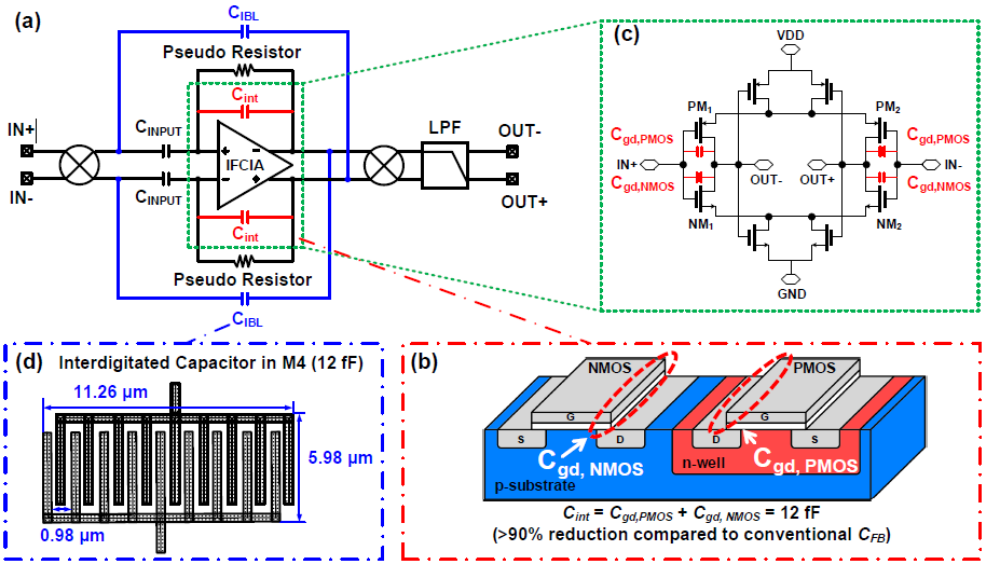
[1.5.1]

Fig.1.5.3. Auxiliary-path chopping using mixer $M_{1,2}$ to mitigate the effect of positive feedback [1.5.1].



[1.5.2]

Fig.1.5.2. Capacitively-coupled instrumentation amplifier with hybrid cap network [1.5.2].



[1.5.3]

Fig.1.5.4. (a) IFCIA closed-loop architecture (b) intrinsic feedback capacitor (C_{int}) from input pair (c) IFCIA structure (d) C_{IBL} implementation.

To mitigate the effect of the positive feedback loop, auxiliary-path chopping is proposed as shown in Fig.1.5.2 [1.5.1]. The auxiliary path has been added to pre-charge the input capacitors of CCIA. Even though the input impedance has been boosted by 76 times, it requires additional clocks and buffers, which can entail more ripples and a higher noise floor.

[1.5.2] and [1.5.3] boosted the input impedance by transforming the structure or implementation of capacitors in the capacitor array of the CCIA. [1.5.2] has boosted impedance by adding a hybrid capacitor array to increase the input impedance from 4 MΩ

to 1.2 GΩ. It does not require additional power consumption and is easy to implement, but subject to mismatches and process variations.

Fig.1.5.4 depicts intrinsic feedback capacitor instrumentation amplifier (IFCIA) [1.5.3]. Fig.1.5.4(a) shows the IFCIA closed-loop architecture, where C_{FB} is replaced by C_{int}, which is used a small gate-drain capacitance (12 fF) of the input transistor as a feedback capacitor instead of a minimum MIM capacitance (35.6 fF) provided by 0.18 μm process as show in Fig.1.5.4(b) and (c). Accordingly, input capacitance can be reduced, and the capacitance of the PFL (Fig.1.5.4(d)) is implemented to match the feedback capacitance, increasing the input impedance by more than ten times to 1.5 GΩ. However, it can be applied to a specific circuit topology that can use gate-drain capacitance, and gain accuracy can be deteriorated due to variations in MOSFET capacitances.

1.6 INTRODUCTION OF THE PROPOSED SYSTEM

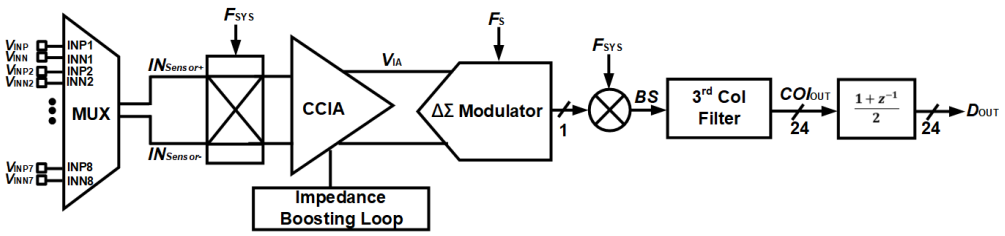


Fig.1.6.1. Proposed 13.2 kSPS bridge sensor read-out system.

As mentioned so far, there have been many studies on impedance boosting in CCIA to read-out a resistive bridge sensor without signal loss. In this paper, we propose a 13.2 kSPS, 5.1 GΩ input impedance read-out IC using the impedance boosting technique for bridge sensor system. As shown in Fig.1.6.1, the system has 8-channel differential analog inputs. To make energy-efficient, CCIA is implemented as the IA topology. And an incremental discrete delta-sigma ADC with 18-bits effective resolution, sampling frequency(F_S) of 4 MHz is designed, following after the CCIA for high precision. The system output data-rate is 13.2 kHz. The chopping frequency of the CCIA is F_{SYS}, which is system chopping frequency of 13.2 kHz and the reason using this frequency as the chopping frequency of the CCIA is explained Chapter 3.1. The impedance boosting loop

in the CCIA is consists of conventional PFL and the proposed fine current compensation loop (FCCL). The proposed read-out system boosts its input impedance without any noise degradation and malfunction and achieves 5.1 GΩ of the input impedance. Also, CCIA contains the sensor offset cancellation block for canceling the bridge type sensor offset voltage. Third order cascade-of-integrators (CoI) decimation filter is used for fast conversion. System chopping is applied to suppress system offset and 1/*f* noise by averaging two decimation filter output as shown in Fig.1.6.1.

1.7 THESIS ORGANIZATION

This paper consists of seven chapters. The first chapter introduces smart sensors and pressure sensors for various pressure range. Also, bridge sensor read-out system is introduced for the sensors and the IA topologies, respectively. Previous works are introduced to boost the input impedance of the system. Chapter 2 describes the system overview and timing of the system. Chapter 3 describes the proposed CCIA structure with FCCL and its impedance boosting effect is analyzed. Chapter 4 explains the operation and implementation of an incremental ΔΣ ADC, which includes the decimation filter. Chapter 5 describes the system-level design, which includes power peripherals and temperature sensors. Finally, chapter 6 introduces the measurement results and performance summary. Chapter 7 concludes the thesis.

CHAPTER 2

SYSTEM OVERVIEW

2.1 SYSTEM ARCHITECTURE

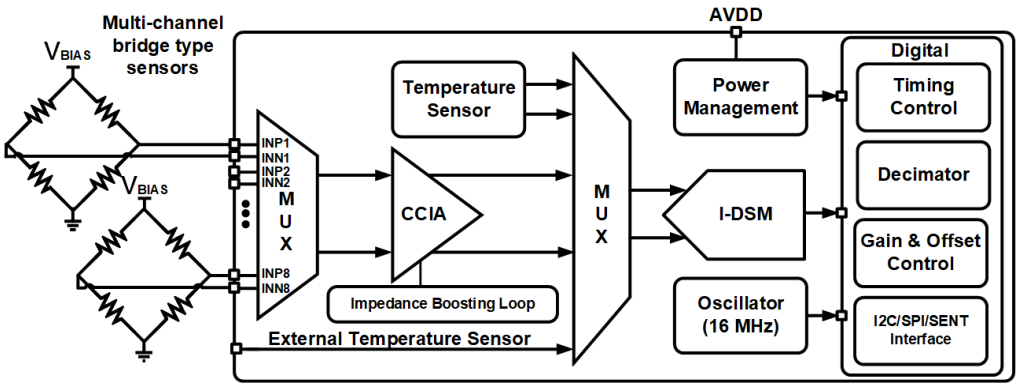


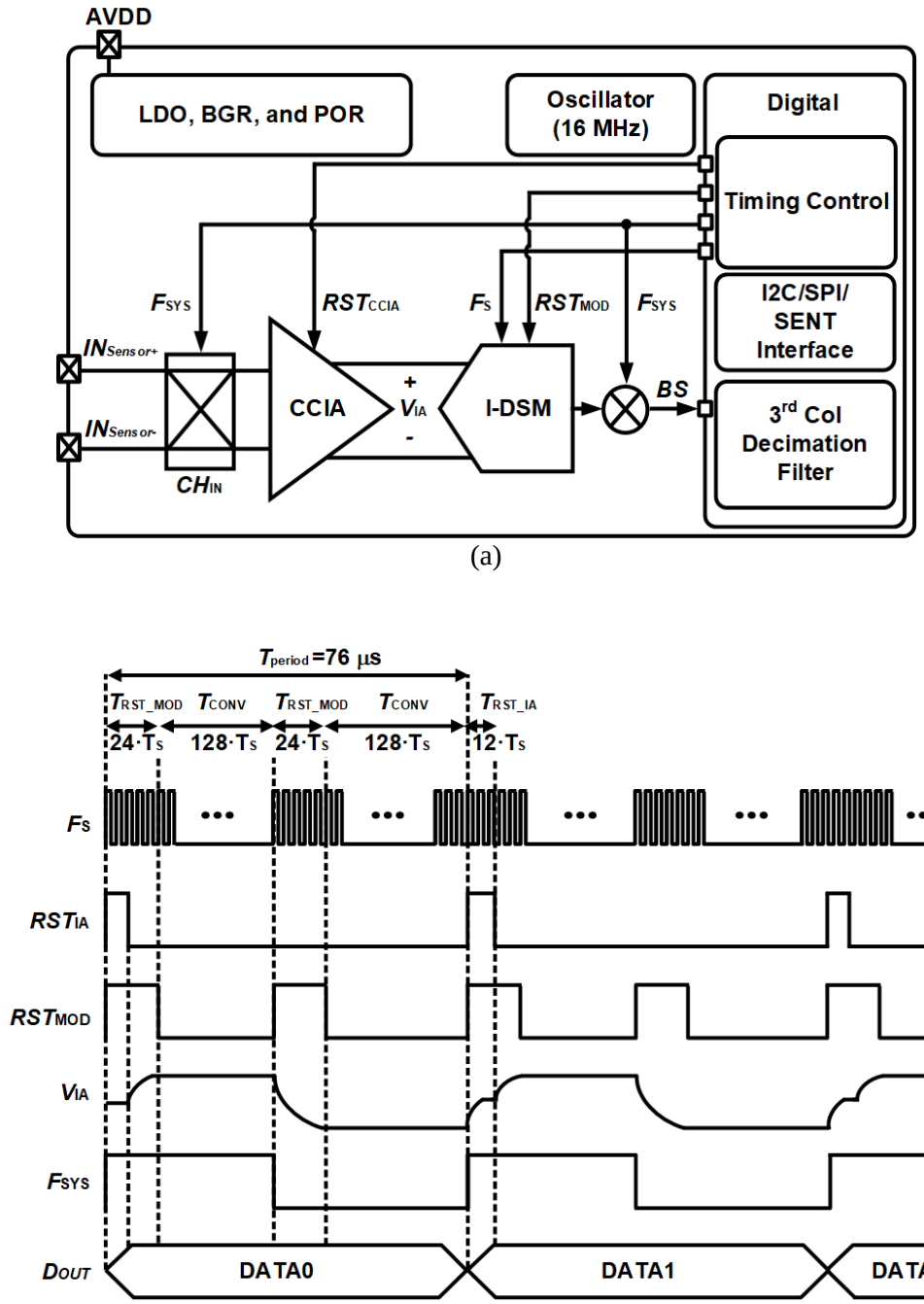
Fig.2.1.1. Simplified block diagram of the system.

This paper describes a fully integrated read-out system for resistive bridge sensors. Fig.2.1.1 shows the simplified block diagram of the system. An input multiplexer (MUX) is multiplexing the input signals from 8 different bridge sensors. There is another MUX

between the CCIA and the incremental DSM (I-DSM) with the impedance boosting loop. This MUX allows selection of I-DSM input among the internal temperature sensor output, the CCIA output, and an external temperature sensor input. The output of the DSM is applied to the input of the decimation filter. In addition to the corresponding main signal path, there is a power management block. In the corresponding block, there are a low-dropout regulator (LDO) for digital circuits that receive 5 V input and outputs 1.55 V, an under voltage lockout circuit (UVLO), power-on-reset (POR), and a 16 MHz oscillator. In addition, the system is embedded with I2C, SPI, and single edge nibble transmission (SENT) interface for automotive communication.

2.2 SYSTEM-LEVEL TIMING

The analog front end and timing diagram of the read-out system is shown in Fig. 2.2.1. The conversion time (T_{period}), which includes two sub-conversions, is 76 μs for each digital output (D_{OUT}). During each sub-conversion, the I-DSM requires 6 μs to reset (T_{RST_MOD}) and 32 μs to convert V_{IA} to a digital output (T_{CONV}). After each sub-conversion completes, the I-DSM waits for V_{IA} to settle after the input chopper (CH_{IN}) changes its polarity during RST_{MOD} for the next sub-conversation. At the beginning of each conversion, both CCIA and I-DSM are reset by RST_{IA} and $RST_{MOD,}$ respectively. After the first sub-conversion completes, F_{SYS} goes low, and the second sub-conversion begins. At the beginning of the second sub-conversion, only the modulator is reset. In the first sub-conversion, when F_{SYS} is high, the non-inverted modulator output is transferred to the decimator. In the second sub-conversion, when F_{SYS} is low, the inverted modulator output is demodulated by the output chopper to generate *BS* that is then passed to a digital decimation filter. The decimator averages the two digital values and produces D_{OUT}.



(a)

(b)

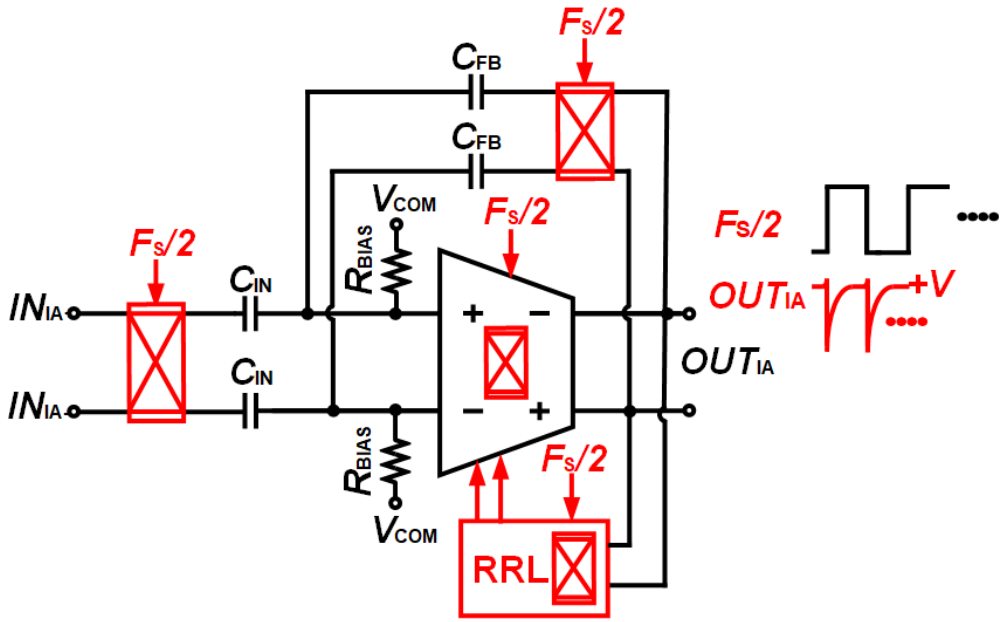
Fig.2.2.1. (a) Analog front end and (b) the timing diagram of the system.

CHAPTER 3

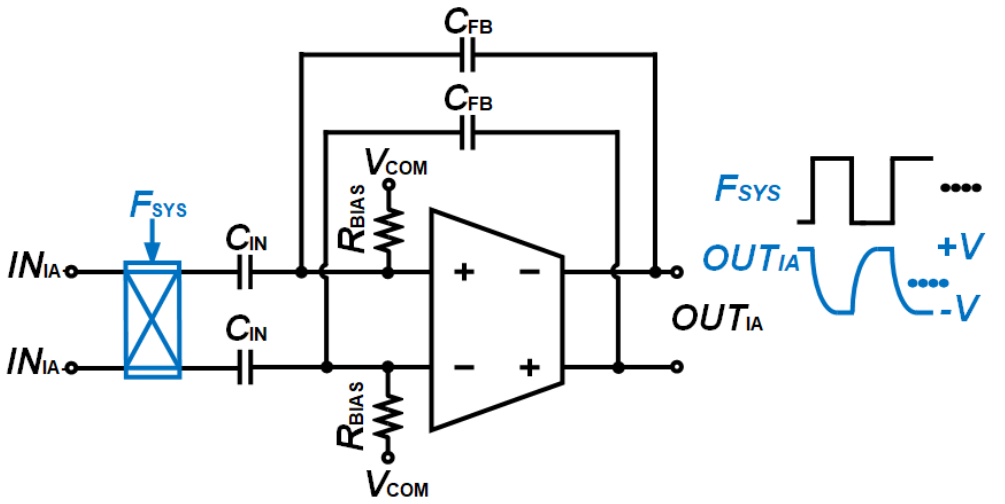
IMPLEMENTATION OF THE CCIA

3.1 CAPACITIVELY-COUPLED CHOPPER INSTRUMENTATION AMPLIFIER

The conventional chopping frequency of CCIA is half of the sampling frequency F_S of its discrete-time ΔΣ modulator [1.3.5], as shown in Fig. 3.1.1(a). To increase the speed of a read-out IC, the sampling frequency of the modulator, and the chopping frequency of the CCIA should be increased. But, this significantly reduces the input impedance of the CCIA and requires more power of it and ripple reduction loop (RRL) [1.3.5] is required to reduce chopping ripples. Fig. 3.1.1(b) shows that the proposed CCIA block diagram and the output voltage, using F_{SYS} as the chopping frequency. F_{SYS} is much higher than the 1/*f* corner frequency, but slower than $F_S/2$, which is commonly used as the chopping frequency in Fig. 3.1.1(a). The input impedance of CCIA can be increased and the power consumption of the CCIA can be reduce. Also, since RRL is not required, additional power consumption is not needed and chip area can be saved.



(a)



(b)

Fig.3.1.1. (a) Conventional CCIA with a chopping frequency of $F_S/2$, and (b) the proposed CCIA with a chopping frequency of F_{SYS}, which is $F_S/304$.

3.2 IMPEDANCE BOOSTING

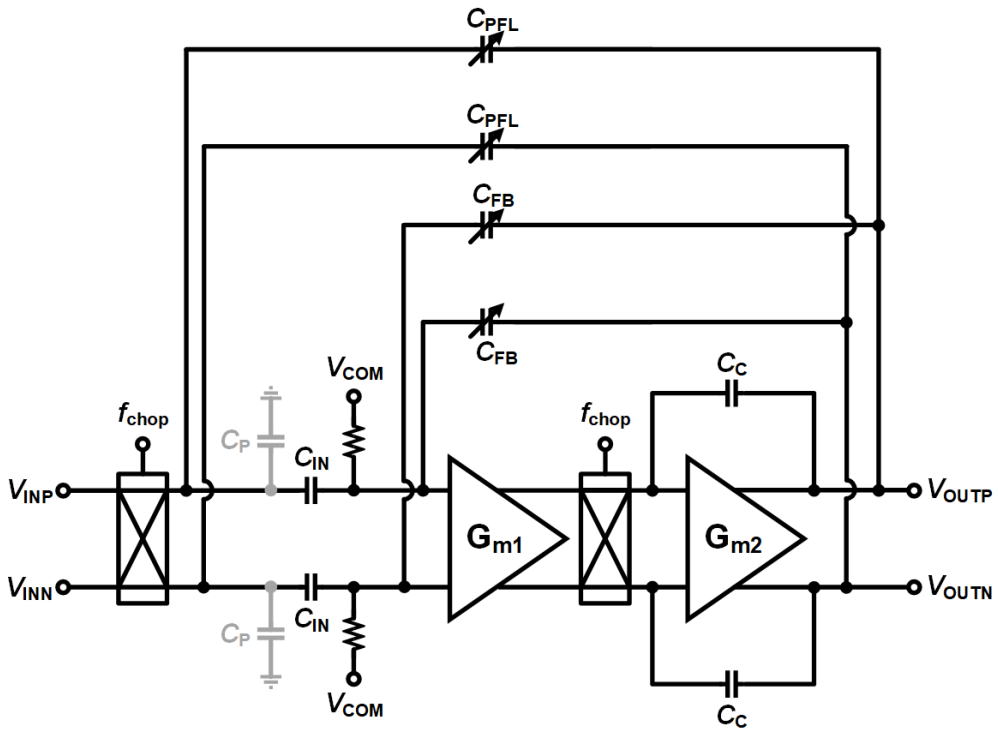


Fig.3.2.1. The block diagram of CCIA with a conventional input impedance boosting loop.

In [1.3.5], C_{IN}, C_{FB}, and C_{PFL} are implemented with multiple unit capacitors (C_{unit}s) for matching accuracy shown in Fig.3.2.1. C_{FB} and C_{PFL} have the same capacitance and they are variable for gain programmability. However, the input impedance can be further increased with the PFL when C_{FB} and C_{PFL} are different.

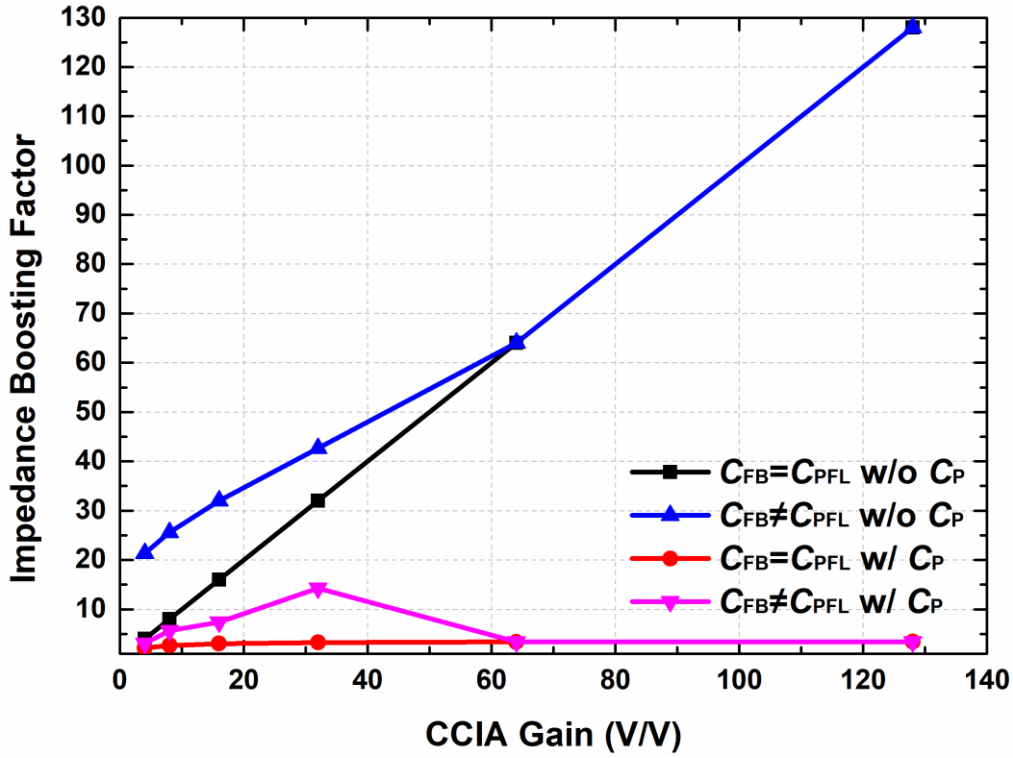


Fig.3.2.2. The impedance boosting factor against CCIA gain depending on C_{FB}, C_{PFL}, and C_{PFL}.

In that case, the input impedance Z_{IN} can be expressed with $C_{FB} = M \cdot C_{unit}$ and $C_{PFL} = N \cdot C_{unit}$ as follows:

$$Z_{IN} = \frac{1}{2 f_{chop}[C_{IN} + C_P - C_{PFL}(G-1)]} = \frac{G}{2 f_{chop}[G \cdot C_P + (G - \frac{N \cdot G}{M} + \frac{N}{M}) \cdot C_{IN}]} . \quad (3.2.1)$$

If N and M are equal, (3.2.1) can be simplified to (1.5.1).

Fig. 3.2.2 shows how the impedance boosting factor (IBF) varies with the gain of CCIA when C_P is present or not. The plot has been generated based on (2) and C_P = 40 % of C_{IN}. IBF, which describes how many times the input impedance is increased, is defined as follows:

$$\text{IBF}=\frac{\text{Input impedance w/ boosting}}{\text{Input impedance w/o boosting}}. \qquad (3.2.2)$$

For $C_P = 0$ and $C_{FB} = C_{PFL}$ (black line), IBF equals the CCIA gain. For $C_P = 0.4 \cdot C_{IN}$ and $C_{FB} = C_{PFL}$ (red line), IBF is around three at all gains. For $C_P = 0$ and $C_{FB} \neq C_{PF}$ (blue line), IBF is greater than the gain. For $C_P = 0.4 \cdot C_{IN}$ and $C_{FB} \neq C_{PFL}$ (pink line), IBF equals or exceeds the IBF when $C_P = 0$, $C_{FB} \neq C_{PFL}$ at low CCIA gain. This is because C_P, multiplied by the gain of CCIA, exceeds C_{IN}, as shown in (2). IBF can be maximized for each gain by trimming C_{PFL} and C_{FB} differently. If the gain of CCIA is from 4 to 32, manual trimming allows you to obtain a larger IBF when C_{PFL} and C_{FB} are equal, but if the gain is from 64 or 128, C_{FB} becomes too small to trim. Therefore, the desired boosting effect cannot be expected with high gains and large C_P through existing PFL techniques and manual trimming.

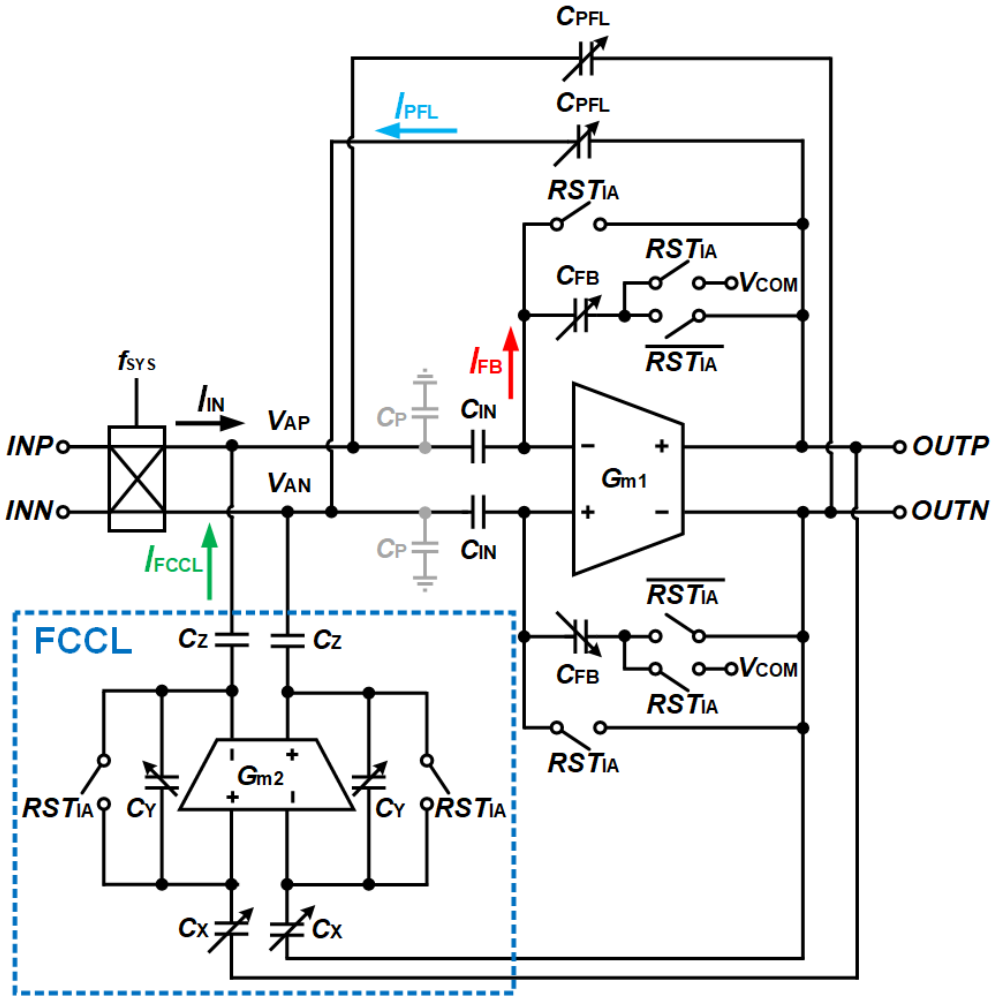


Fig.3.2.3. The block diagram of a proposed CCIA.

The schematic diagram of the CCIA with the fine current compensation loop (FCCL) and PFL is shown in Fig. 3.2.3. As explained in Section 1.5, it is ideal to have C_{PFL} equal to $C_{IN}/(G\text{-}1)$ to maximize the impedance boosting effect. However, this is challenging

in practical implementation; therefore, C_{PFL} has been chosen to be equal to C_{FB} [1.3.5]. With the proposed FCCL and PFL, the current drawn by the CCIA can be canceled further by I_{COMP}, and the total capacitor of the impedance boosting loop is closer to $C_{IN}/(G\text{-}1)$ so that the IBF greater than the CCIA gain can be achieved. C_X detects the CCIA's output voltage and converts it to current, and C_Y integrates the current and converts it back to voltage, providing a voltage gain by C_X/C_Y ratio. An operational transconductance amplifier (G_m) and C_Z convert the voltage back to current and feed it back to the V_{AP} or V_{AN}. The value of C_Z has been chosen as the minimum (unit capacitance) to have a negligible effect on the noise performance of the system. G_m in the FCCL is 1/24 times that of the CCIA's main amplifier to minimize the additional current consumption.

To analyze the effect of the input impedance boosting through the FCCL, an equation can be derived similar to (2). It can be expressed as $C_{FB}=C_{PFL}=M\cdot C_{unit}$, $C_{IN} = G_{max}\cdot C_{unit}$, where G_{max} is the maximum gain of CCIA when C_{FB} is C_{unit}. For the FCCL, C_X and C_Y are set to $N_C\cdot C_{unit}$ and $M_C\cdot C_{unit}$, respectively. C_Z is set to C_{unit} to minimize the influence on the main path. Then, the input impedance equation can be expressed as follows:

$$Z_{IN} = \frac{1}{2 f_{chop}[C_P + (\frac{1}{G} + \frac{1}{G_{max}} - \frac{N_C}{M \cdot M_C})\cdot C_{IN}]}. \qquad (3.2.3)$$

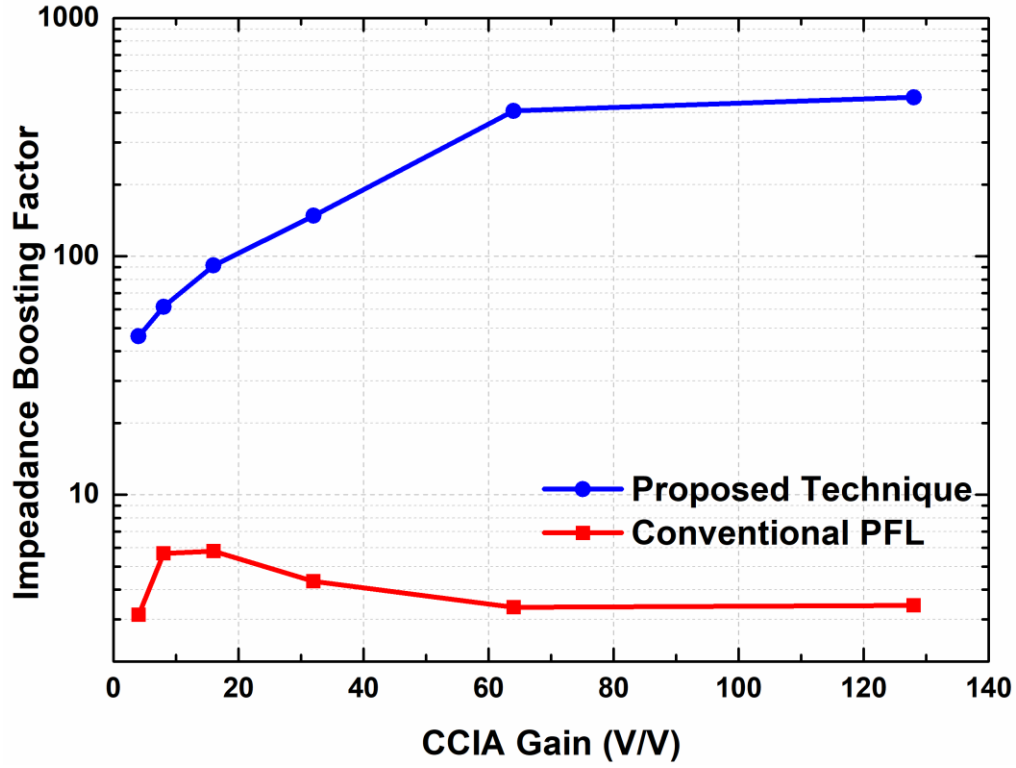


Fig.3.2.4. The graph of impedance boosting factor against CCIA gain when using conventional PFL or proposed technique together.

To compare (3.2.3) with (3.2.1), when C_P is between 10 % and 40 % of C_{IN}, the minimum IBF among the maximum IBF that can be had at each C_P according to CCIA gain using (3.2.3) is plotted in Fig. 3.2.4. Due to the capacitor array size issue, N_C is set to be less than 23, and M_C is set to be less than 47. The conventional PFL can achieve an IBF of 5.8 when C_P is present. However, the IBF increases proportionally as the CCIA gain increases when FCCL is used. When the CCIA gains are 4 and 128, the IBFs are 46 and 464, respectively, higher than the CCIA gain. Even if C_P changes, the worst IBF is larger than the conventional PFL.

3.3 SENSOR OFFSET CANCELLATION

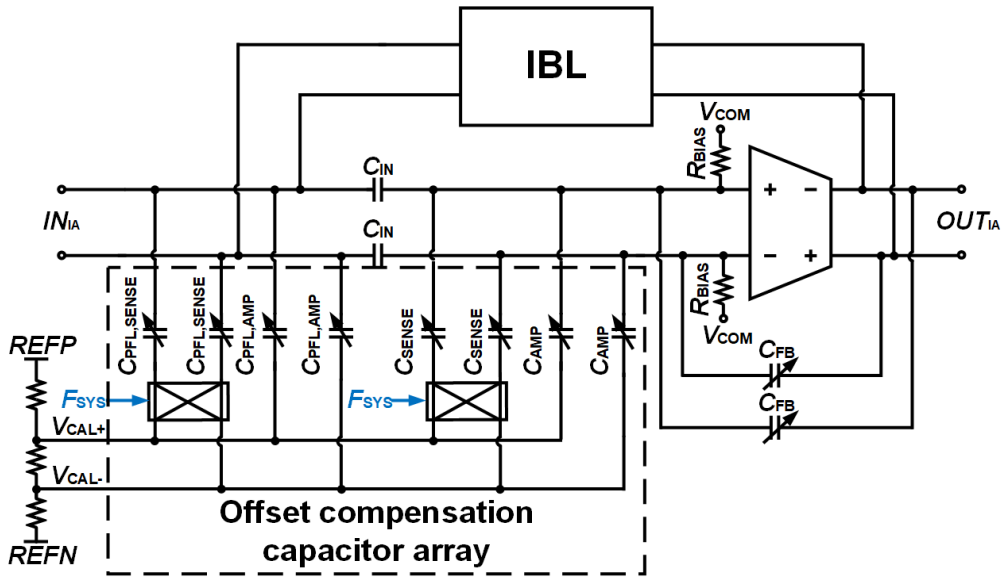


Fig.3.3.1.The offset compensation block in the CCIA.

There are two capacitive arrays as expressed in Fig.3.3.1: C_{SENSE} for compensating the sensor offset voltage, and $C_{PFLSENSE}$, has the same functions as C_{PFL}. Each of these four arrays consists of a 8-bit array with a 70 fF unit capacitors. The resistive ladder between *REFN* and *REFP* makes offset compensation voltage for C_{SENSE}. It consists of three resistors, each of 191 kΩ, to reduce the current consumption and the thermal noise to a level at which they do not affect system performance. The two choppers operate at the same clock signal F_{SYS} as the system chopper.

The voltage V_{SENSOR} from the sensor consists of an offset voltage V_{OFFSET}, and a

sensor signal V_{SIG}, which is dependent on pressure as follows:

$$V_{SENSOR} = V_{SIG} + V_{OFFSET} . \tag{3.3.1}$$

To avoid saturation, the read-out IC can be saturated if V_{OFFSET} is amplified by the gain of the CCIA, which would reduce the dynamic range. Compensation for V_{OFFSET} is applied by the chopping frequency F_{SYS} as same as the CCIA chopping frequency, the sensor offset compensation capacitors C_{SENSE}, and the voltages V_{CAL+}, and V_{CAL-}, which are generated using a resistive ladder [3.3.1], as shown in Fig.3.3.1. If F_{SYS} and the differential voltage $\Delta V_{CAL} = V_{CAL+} - V_{CAL-}$ are applied to C_{SENSE}, the output OUT_{IA} of the CCIA can be expressed as follows:

$$OUT_{IA} = \frac{C_{IN}}{C_{FB}} \times \left(V_{SIG} + V_{OFFSET} - \frac{C_{SENSE}}{C_{IN}} \nabla V_{CAL} \right), \tag{3.3.2}$$

which (3.3.2) shows that V_{OFFSET} can be canceled by ΔV_{CAL} and C_{SENSE}. There also needs to be compensation for the amplifier offset voltage V_{AMP} the amplifier in CCIA, which can be around 100 mV, must be considered.

3.4 AMPLIFIER IMPLEMENTATION

The main amplifier in the CCIA has two-stage Miller-compensated structure shown in Fig. 3.4.1, in order to meet settling and noise requirements. This main amplifier accounts for the most of the noise contribution in the entire bridge sensor read-out system. Therefore, the amplifier should be carefully designed to meet noise requirements. Its first and second stages have folded-cascode and class-AB structures respectively. To have a stable phase margin and a wide unity-gain bandwidth with using small area, a cascade Miller compensation technique is used. The amplifier is designed to have 120 dB DC gain, 11 MHz unity-gain bandwidth, and 89° phase margin. A continuous-time common-mode feedback (CT-CMFB) loop allows it to operate as a differential amplifier.

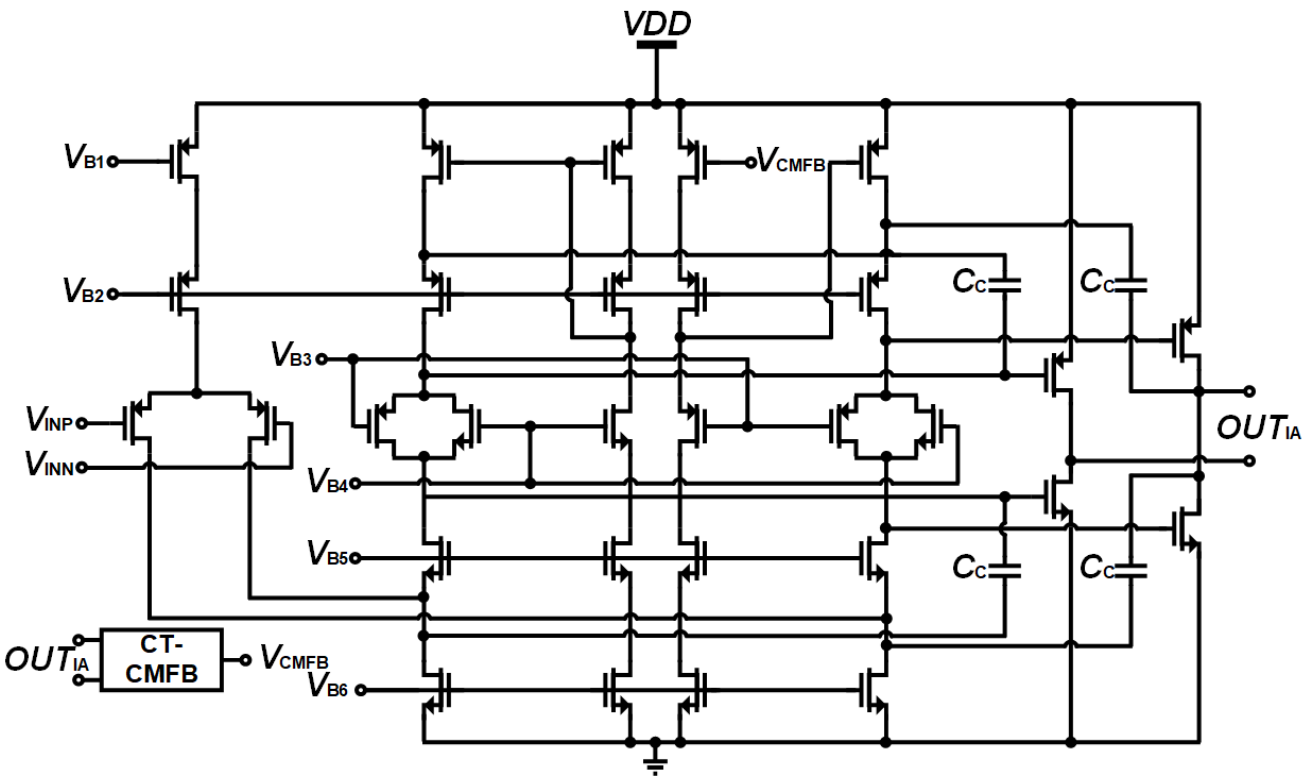


Fig.3.4.1.The two-stage amplifier in the CCIA.

3.5 IMPLEMENTATION OF THE CCIA

Fig.3.5.1 shows the block diagram of the proposed CCIA in the bridge sensor read-out system. It has both negative- and positive-feedback loops, containing capacitor arrays of negative-feedback (C_{FB}) and positive-feedback (C_{PFL}), which provide 5-bit resolution. The noise $V_{N,IA}$ of the CCIA, which is inversely proportional to C_{IN}, can be expressed as follows:

$$V_{N,IA} = \left(\frac{C_{IN} + C_{FB} + C_P}{C_{IN}} \right) \times V_{N,AMP}, \qquad (3.5.1)$$

where C_P is the parasitic capacitance at the input node of the amplifier and $V_{N,AMP}$ is the noise of the amplifier, respectively.

As shown in (3.5.1), to alleviate the effect of C_P, C_{IN} is set to 8.96 pF. This results in an input impedance of 28 kΩ when the chopping frequency is half of the sampling frequency F_S. Sensor offset voltage compensation block is located between two nodes of C_{IN}. The two input voltages are determined by the bias resistors, which are implemented as back-to-back diodes so as to achieve large resistance with low noise in a small area.

Compared to conventional CCIA structure, the proposed CCIA has the reset mode during the operation. This mode makes common-mode voltage level in the CCIA settle fast by resetting every conversion cycle. Also this mode makes the correlated double sampling (CDS) technique [3.5.1] applicable to reduce the offset voltage in the amplifier, which can

make saturate the output of the CCIA, and 1/*f* noise suppression. Conventional chopping frequency as the half of the sampling frequency in the delta-sigma modulator, offset voltage and 1/*f* noise can be suppressed using ripple-reduction loop without CDS. But, it requires the power consumption and chip are of the ripple-reduction loop. When using chopping frequency as system chopping frequency, the offset voltage of the amplifier makes saturate the output voltage of the CCIA. Adding a reset mode for the CCIA makes enable the CDS technique. While the incremental delta-sigma modulator resets to settle the CCIA output, it also resets as much as the time specified in the digital interfaces. When the CCIA reset signal is high, the floating nodes of the CCIA are initialized and an offset voltage of the amplifier in the CCIA is charged to C_{FB}. When the CCIA reset signal goes low, the CCIA output is amplified by the closed loop gain of the input signal, and the amplifier offset voltage has a residual offset which is divided by amplifier gain A_{IA}.

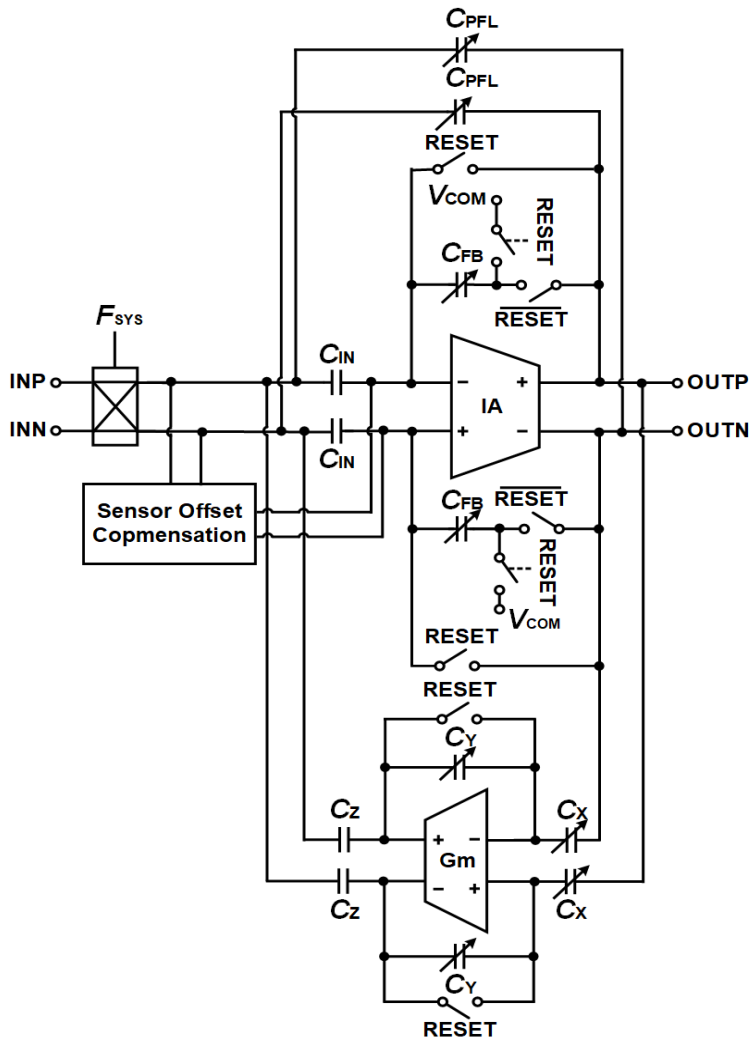


Fig.3.5.1. Block diagram of the proposed CCIA.

CHAPTER 4

INCREMENTAL ΔΣ ADC

4.1 INTRODUCTION OF INCREMENTAL ΔΣ ADC

An analog-to-digital converter (ADC) is a device that receives continuously changing analog signals and converts them into discretely coded signals, and is used throughout the industry. Currently, as the industry develops, it can be used for a long time with low power, high-speed transmission speed and high resolution are required, and the need for ADCs to improve these performances is increasing. The performance of the ADC differs depending on the bandwidth of the application to be used. Bandwidth and resolution have an inversely proportional relationship, so the ADC structure must be selectively selected according to the required application. ADCs can be largely classified into Nyquist-ADCs for high-speed, low-resolution and sigma-delta ADCs for low-speed, high-resolution.

The Nyquist-ADC is the most commonly used converter for wideband signal acquisition because it has low resolution and is advantageous for high-speed signal processing. However, it is vulnerable to variation and noise of analog devices and has limitations in implementing more than 14-bit. On the other hand, sigma-delta ADCs can

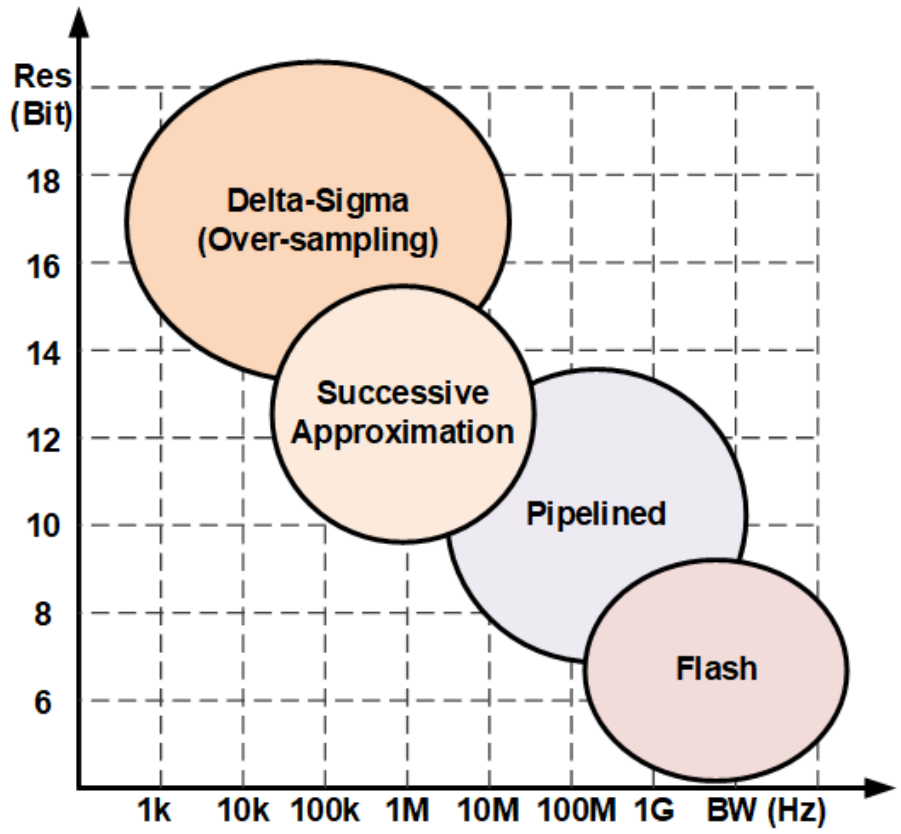


Fig.4.1.1. Resolution and bandwidth (BW) according to ADC types.

have a resolution of 16-bit or higher through oversampling and noise shaping techniques to overcome the performance limitations of devices caused by process limitations. Sigma-delta ADCs are widely used in applications that require high resolution in a narrow bandwidth, and are widely used in sensor fields such as high-resolution measurement fields, high-performance microphones, temperature/humidity sensors, and gyro sensors. As the internet-of-things (IoT) era has emerged, the demand and size of the market where sigma-delta ADCs are used are growing explosively.

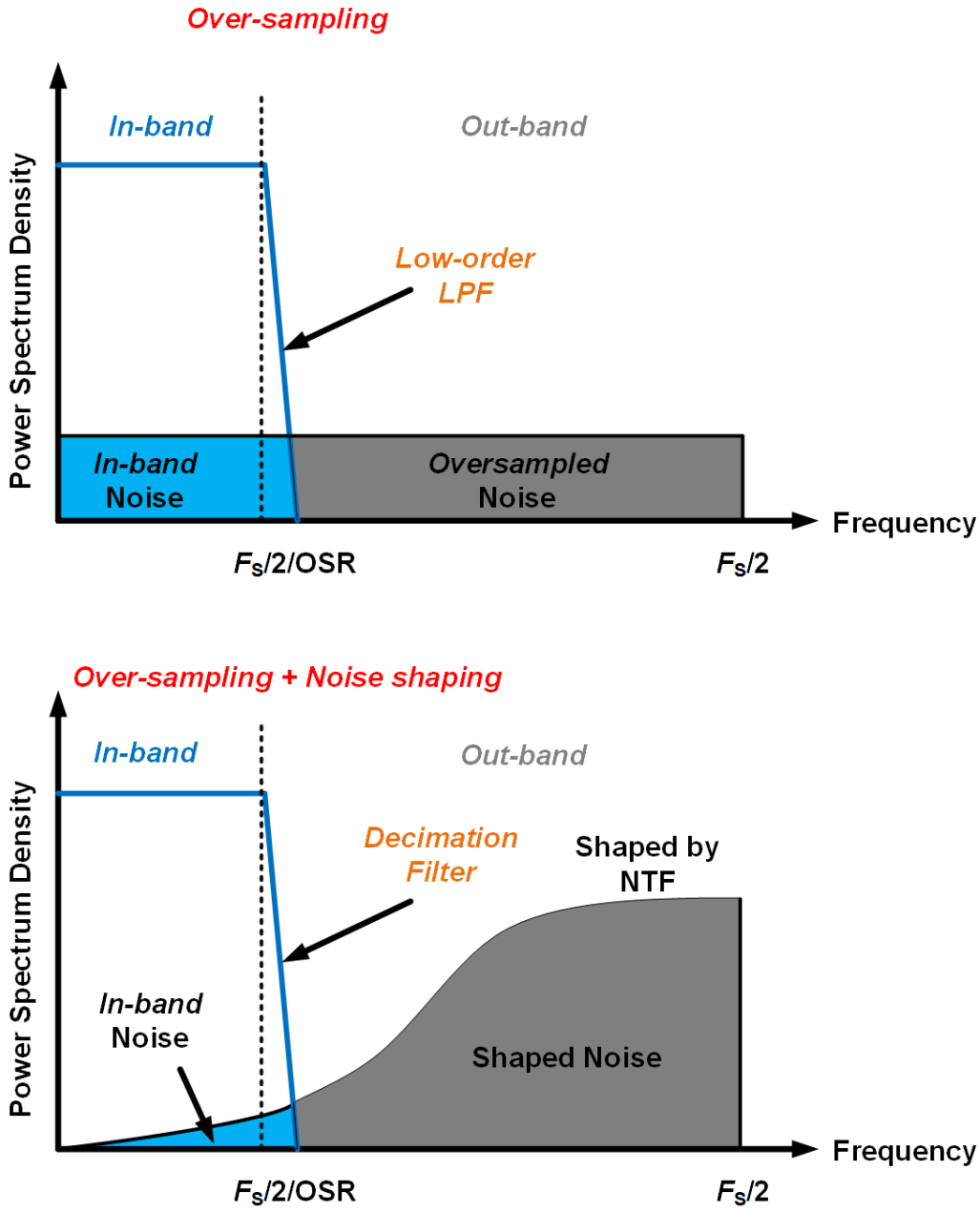


Fig.4.1.2. Conceptual diagrams of over-sampling and over-sampling with noise shaping.

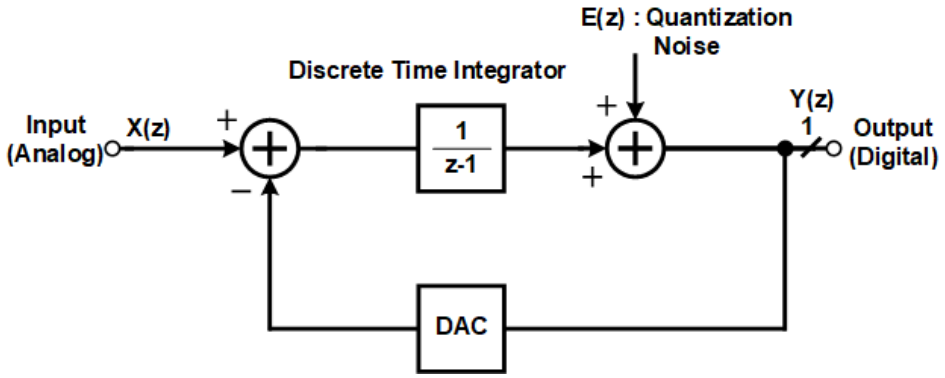


Fig.4.1.3. Block diagram of first-order delta-sigma modulator.

Delta-sigma ADCs are largely divided into delta-sigma modulators and decimation filters. The main characteristics of the delta-sigma modulator are over-sampling and noise shaping. Fig.4.1.2 shows conceptual diagrams of the over-sampling and noise-shaping. Oversampling means sampling by making the sampling frequency faster by the oversampling ratio (OSR) compared to the existing Nyquist-sampling, which can reduce the burden of the anti-aliasing filter transition period. In addition, since the base-band decreases as the OSR increases, quantization noise can be reduced. The decimation filter performs the function of a low-pass filter (LPF) and functions to down-sample the frequency that was oversampled by the modulator.

Fig.4.1.3 show a block diagram of the first-order delta-sigma modulator. In this figure, there are one discrete time integrator and a DAC, and a quantizer. In this figure, we analyze the structure of the first-order delta-sigma modulator, in terms of signal transfer

function (STF) and noise transfer function (NTF). Output signal Y(z) can be expressed as follows:

$$Y(z)=E(z)\cdot\left(1-z^{-1}\right)+X(z)\cdot z^{-1}=E(z)\cdot NTF(z)+X(z)\cdot STF(z), \quad (4.1.1)$$

which E(z) is quantization noise of the modulator and X(z) is the signal of it. Looking at the corresponding NTF in the frequency domain, $|NTF(f)|=2\left|\sin\left(\frac{\pi f}{f_S}\right)\right|$ is called a first-order noise shaping function. A feature of this function is that it attenuates quantization noise in a low frequency band and amplifies it in a high frequency band. Therefore, signal-to-noise ratio (SNR) can be increased by reducing quantization noise in the base-band frequency band.

The components of the delta-sigma modulator include an integrator, a quantizer, and a digital-to-analog converter (DAC). The integrator is a circuit for acquiring several samples for correcting errors for one obtained sample and accumulating them. That is, oversampling is performed to obtain one digital data. The structure of the integrator is a switched-capacitor, and the offset must be small to obtain a high signal-to-noise ratio (SNR). Accordingly, an amplifier is required within the integrator. The value output through the integrator outputs a high signal if it is higher than the reference value through the quantizer, and a low signal if it is lower than the reference value. The digitized value is converted back to analog through a 1-bit DAC, and subtraction operation is performed with the analog signal for error correction obtained through oversampling. In other words, it is to find the error, and the digital value obtained by repeating this process goes to the decimator, and

the decimator filters out the noise of the high frequency band through the LPF and adjusts the sampling frequency band through down-sampling.

Unlike typical sigma-delta ADCs, Incremental Delta Sigma ADC is suitable for low-power, high-sensitivity pressure sensor applications because it can adjust the resolution of the modulator according to the number of clocks in a certain conversion period, enabling easy multiplexing in multiple channels. Incremental sigma-delta ADCs differ from typical time-continuous sigma-delta ADCs in that, after resetting all internal storage elements, they operate for a predetermined number of N clock cycles within the conversion cycle of the input, and thus operate on a single input. The output for is obtained after N clock cycles.

The resolution of the modulator is determined by the number of clock cycles and the order of the modulator, and the determination process is as follows. In order to increase the SNR in the delta-sigma modulation (DSM) structure, the order of the loop filter inside the DSM should be increased or the number of bits of the quantizer must be increased. The method of increasing the order of the loop filter has a difficulty in that the maximum input value of the signal that can be accepted as input is limited to a certain size or less according to the order in order to guarantee the stability of the loop in design. The way to increase the number of bits of the quantizer is to use dynamic element matching (DEM). During multi-bit digital-to-analog conversion, the resolution is lowered due to the mismatching of the capacitor array, and it is difficult to introduce a digital filter technique to compensate for this. Since there is a trade-off between the performance and consumption area according to the selection of the order of the loop Filter and the number of quantizer bits, and the power used, the SNR performance must be obtained by adjusting the order of the loop Filter and

the number of quantizer bits according to the target performance value. Incremental delta-sigma ADC has high resolution and good linearity, so accurate conversion is possible. Since the output value is obtained every N clock cycles at the end of the conversion, it can be interpreted in the time domain.

4.2 IMPLEMENTATION OF INCREMENTAL ΔΣ MODULATOR

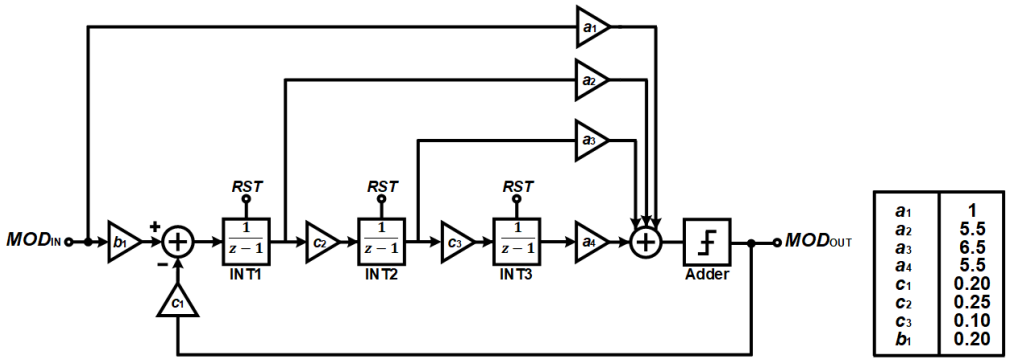


Fig.4.2.1. Block diagram of the incremental ΔΣ modulator.

Fig. 4.2.1 is a simplified block diagram of the single-bit third-order incremental ΔΣ modulator which receives the output of the CCIA. The target ER is of the ADC is 17.5 bits for detecting a 400 kPa range of the sensor, with an output data-rate (ODR) of 12.8 kSPS. A reference voltage 5.0 V is supplied to the ADC, and its input range is 4.8 V. The modulator is implemented with a cascade input feed-forward (CIFF) structure that can alleviate the slewing requirements of integrators through an input feed-forward path [4.2.1]. The integrators in the ΔΣ modulator are reset at the beginning of each conversion. The ADC can support output data-rates of 13.2 kSPS, 6.6 kSPS, and 3.4 kSPS.

Fig. 4.2.2 is a schematic diagram of the ΔΣ modulator. The input signal is sampled by the sampling capacitor C_{S1} during P_1 and integrated into the feedback capacitor C_{F1} during P_2. The bottom-plate sampling technique is used to reduce charge injection by the

switches. Since the first integrator is the critical block in terms of noise in an ADC [27], the correlate-double sampling (CDS) technique [3.5.1] has been applied in the first integrator to suppress $1/f$ noise and offset. The operation of the second and third integrators is the same as the first integrator, except that CDS is applied to the first integrator. A 1-bit quantizer, chosen to maximize linearity, follows the integrators. It determines the output when the adder has settled at the end of sampling phase P_1. The bit-stream output (BS) is down-sampled by a third-order CoI filter.

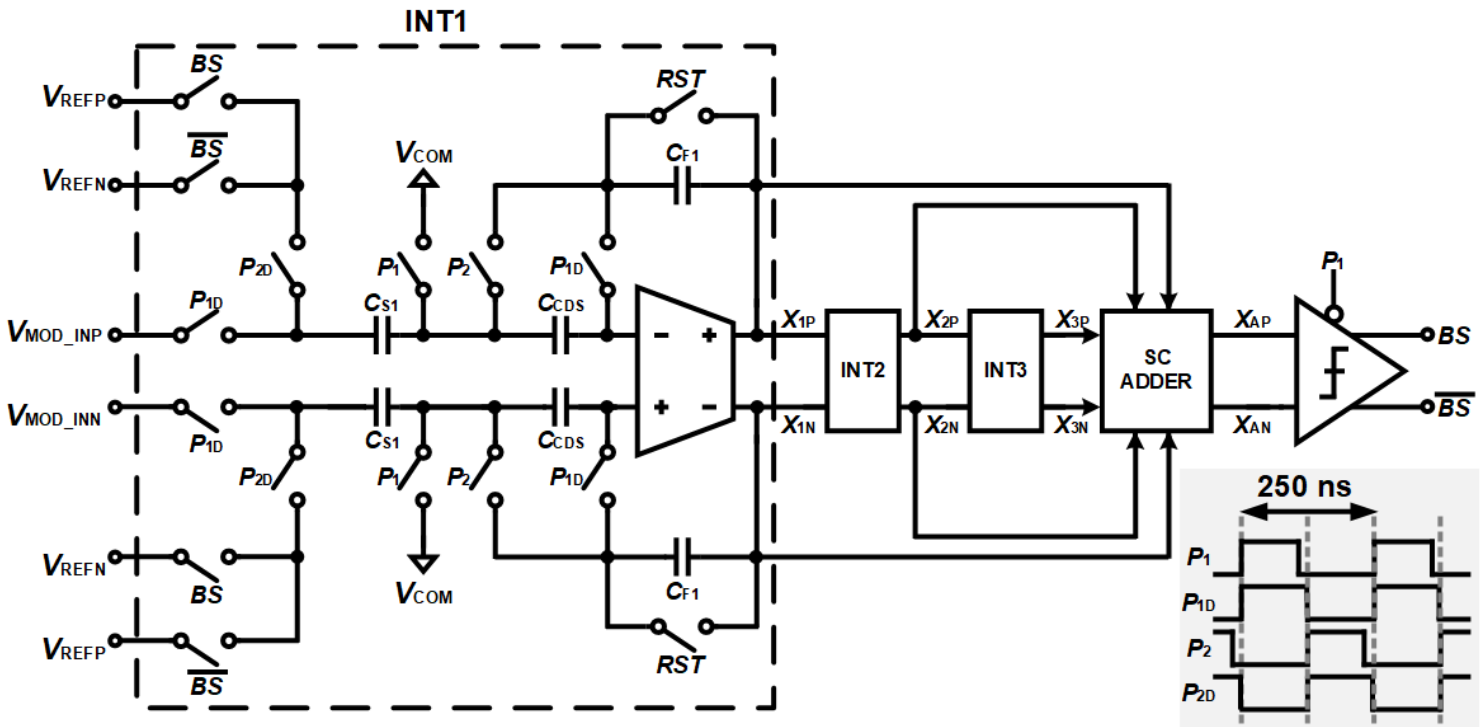


Fig.4.2.2. Schematic of the incremental ΔΣ modulator.

4.3 DECIMATION FILTER

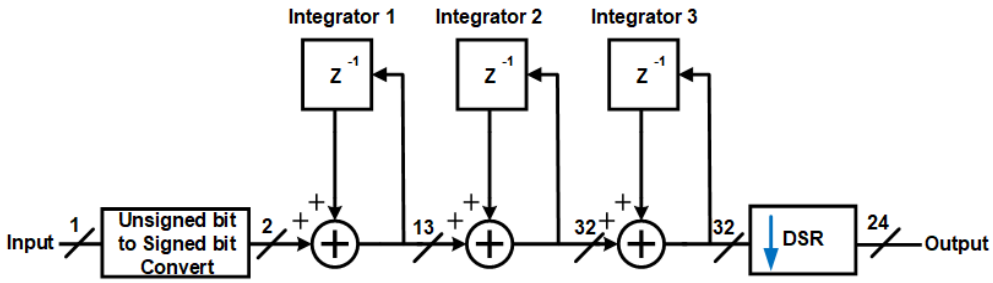


Fig.4.3.1. Third-order cascade-of-integrators.

The main function of a decimation filter is to down sample and reduce passband aliasing or error. To reduce hardware cost, a decimation filter is implemented using a cascaded-of-integrators (CoI) filter or cascaded integrator-com (CIC) filter [4.3.1] without using a multiplier. Compared to CIC filter, the CoI filter can be lower the design complexity of the decimator and has a faster conversion time than the CIC filter. If the number of stages in the CoI filter is increased, the error bound can be made smaller, but the calculation speed, hardware cost, and power consumption are additionally consumed, resulting in a trade-off relationship. Therefore, it is important to use the required number of stages.

Since the target of the filter is for DC measurement, a wide passband is not needed, a third-order CoI filter was implemented, and the logic diagram for this filter is shown in Fig.4.3.1. Looking at the logic diagram, there are 3 integrator stages and an unsigned-bit to signed-bit conversion block. The transfer function of the third-order CoI filter is expressed

as follows:

$$H[z] = H_I^3[z] = \frac{1}{(1-z^{-1})^3} = \sum_{i=0}^{DSR-1} \sum_{j=0}^{i-1} \sum_{k=0}^{j-1} z^{-k}, \quad (4.3.1)$$

which $H_I[z]$ is a transfer function of single integrator, and the down-sampling ratio of the decimation filter is referred to as DSR. In our system, the digital output is the average output of the CoI output by the system-level chopping, which suppresses the noise and offset coming from the read-out system.

CHAPTER 5

SYSTEM-LEVEL DESIGN

5.1 POWER SEQUENCE

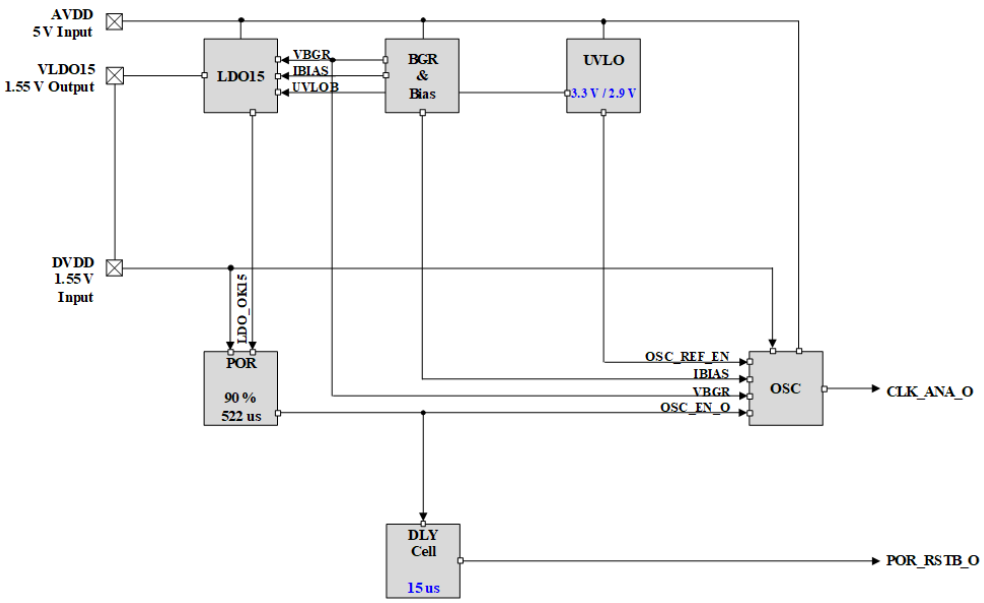


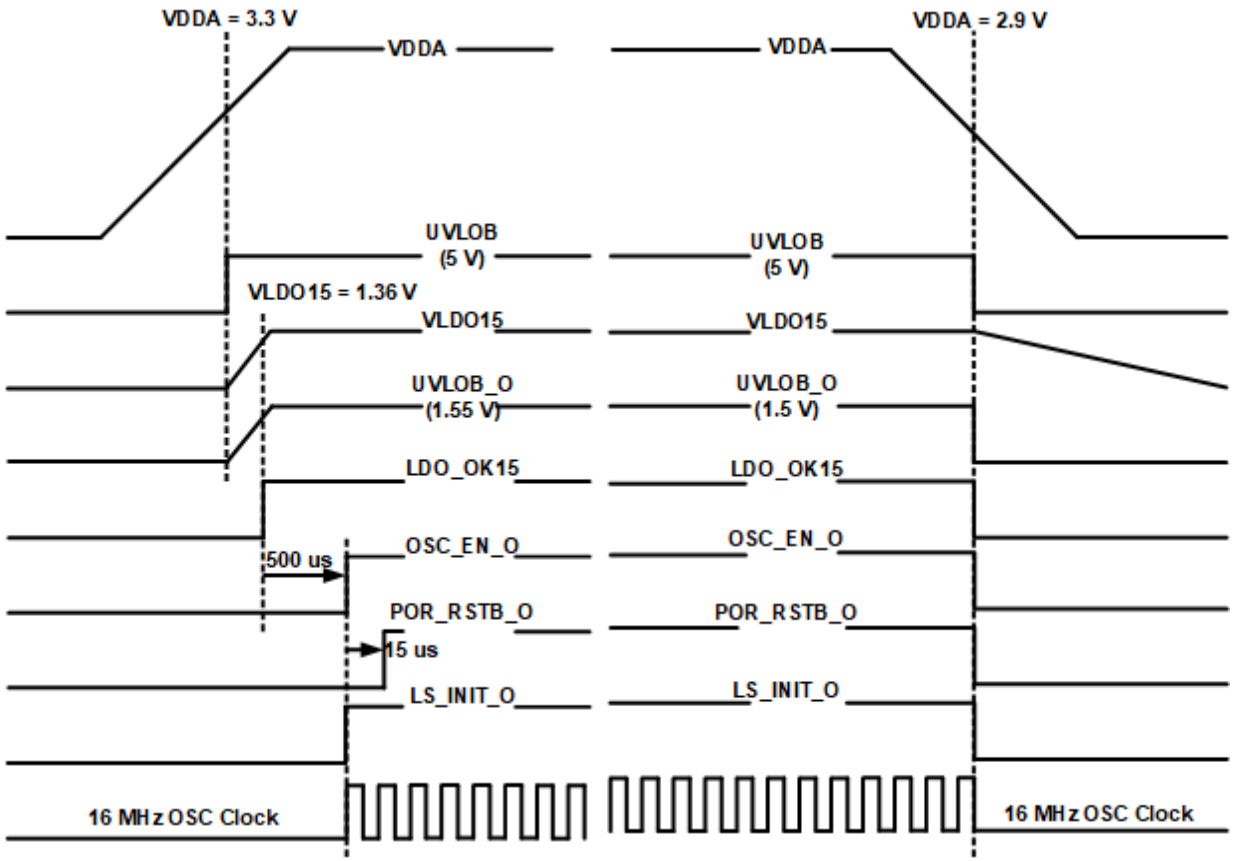
Fig.5.1.1. Block diagram of power peripherals

Fig.5.1.1 shows the block diagram of power peripherals. The power peripherals include a low-drop out (LDO) voltage regulator, bandgap reference (BGR), under-voltage lockout circuit (UVLO), power-on-reset (POR), and a 16 MHz oscillator. The LDO is for

the digital circuits in the chip, which is supplied 1.55 V. The analog supply voltage 5.0 V is supplied from the external LDO, since the automotive application provides the analog supply voltage of the chip. The LDO makes 1.55 V using the BGR voltage *VBGR* and bias current *IBIAS* coming from the BGR. When the LDO voltage is exceeded 90% of the target voltage, the reset signal in the PRO is set to low, and the oscillator enable signal *OSC_EN_O* becomes high. The *POR_RSTB_O* signal is a signal with a delay of 15 μs by inversion of the POR signal, and is used to wake up the power of the analog blocks in the chip.

Fig.5.1.2(a) shows the power up sequence of the system. When external analog supply voltage *VDDA* is rising, the BGR is always on and reset signal is occurred by *UVLOB* in the UVLO circuit. UVLOB reset is released, when *VDDA* reaches 3.3 V. After releasing the *UVLOB*, *LDO15* which wake up the LDO is enabled. After the LDO voltage rises after wake up and becomes equal to the BGR voltage of 1.21 V, *LDO_OK15* signal becomes high after 18 μs and *OSC_EN* goes high after 522 μs. As *OSC_EN* is on, the 16 MHz relaxation oscillator operates. After 15 μs, *POR_RSTB_O* becomes high, and the power up sequence ends.

Fig.5.1.2(b) show the power down sequence of the system. When the external analog supply voltage *VDDA* is falling, UVLO reset is occurred when VDDA reaches 2.9 V. Then, LDO15 signal which controls wake-up of the LDO, is disabled. Supply voltage VDDD for digital circuits starts falling, due to UVLO reset. When UVLO is reset, *LDO_OK15*, *OSEC_EN*, and *POR_RSTB_O* go low at the same time, turning off the power of the analog blocks in the chip.



(a) (b)

Fig.5.1.2. (a) Power up sequence and (b) power down sequence of the system

5.2 RELAXATION OSCILLATOR

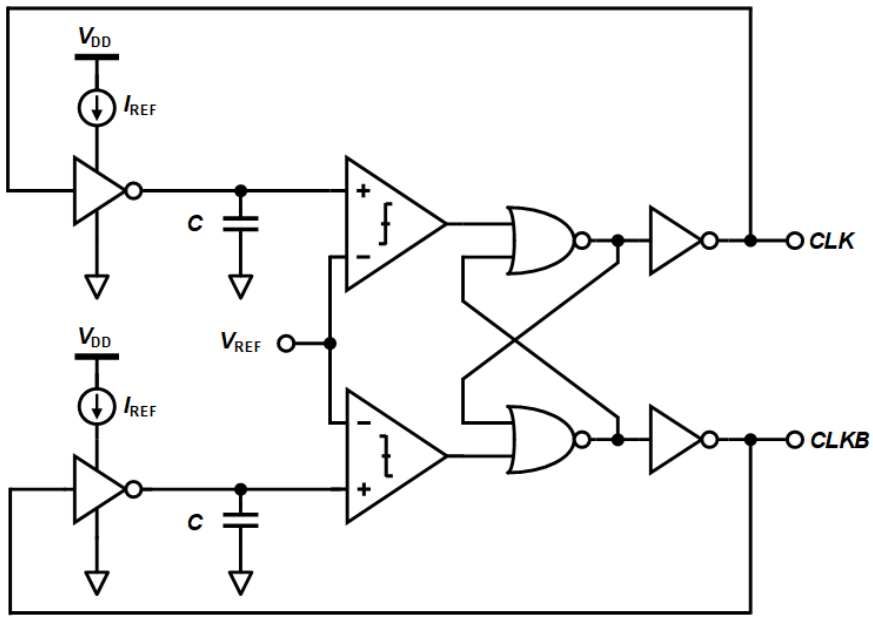


Fig.5.2.1. Block diagram of a relaxation oscillator.

Fig.5.2.1 shows the block diagram of a relaxation oscillator, which is used in the system. As shown in Fig.5.2.1, there are inverters, capacitors *C*, and comparators in pairs. Reference voltage V_{REF} and current I_{REF} is provided from LDO. When *CLK* is low, capacitor *C* is charged via I_{REF}. When the positive input of the comparator exceeds the programmable reference voltage V_{REF}, the comparator toggles its output, causing *CLK* to rise to high. Transition in *CLK* causes inverter to output low, discharging its output capacitor and thus repeating the cycle. The frequency of the relaxation oscillator is as follows:

$$f_{CLK} = \left[2\left(\frac{C \cdot V_{REF}}{I_{REF}} + \tau_{COMP} + \tau_{SR}\right)\right]^{-1}, \quad (5.2.1)$$

which τ_{COMP} represents the delay of the comparator, and τ_{RS} represents the delay of the SR latch. As shown in (5.2.1), increasing C, reference voltage V_{REF}, and delays of the blocks in the oscillator lower the frequency of the oscillator and the reference current I_{REF} lowers the frequency. In this design, we designed V_{REF} to 1.2 V and I_{REF} to 2 μA to make 16 MHz with 6-bit digital trim codes.

5.3 UNDER VOLTAGE LOCKOUT CIRCUIT (UVLO)

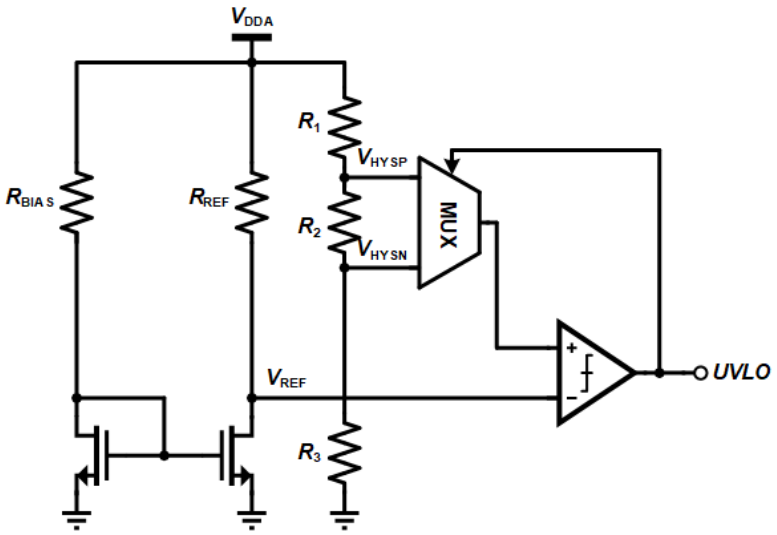


Fig.5.3.1. Block diagram of an under-voltage lockout circuit.

Fig.5.3.1 shows the block diagram of an under-voltage lockout circuit (UVLO). This block is for detection and subsequent disabling of the system at low power supply voltage. In the UVLO, there are a multiplexer (MUX), which selects hysteresis voltage depending on the output of the comparator. A working principle is comparing the reference voltage, which is from a voltage divider and current mirror, with the hysteresis voltage made from the resistive divider between analog supply voltage *VDDA* and ground. In this design, we set to a lockout voltage at 3.283 V and a release voltage at 2.892 V.

5.4 POWER-ON RESET (POR)

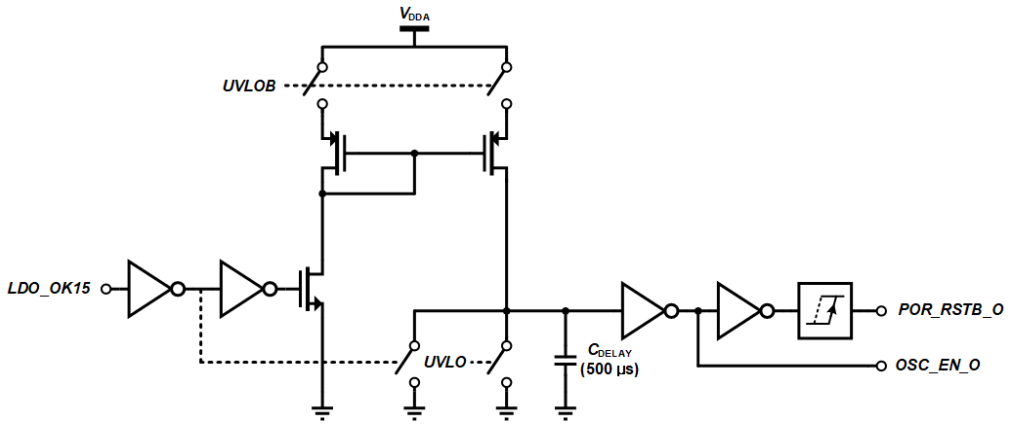


Fig.5.4.1. Block diagram of a power-on-reset.

Fig.5.4.1 shows the block diagram of a power-on-reset (POR). Its inputs are LDO_OK15, that the LDO voltage has reached 90% of the target voltage 1.55 V and UVLO, that the UVLO lockout voltage has reached 3.282 V. Its working principle is that if *UVLOB* or *LDO_OK15* is on, *OSC_EN_O* is disabled, and if one of them is on, C_{DELAY} is charged. This capacitor is composed of MOS-capacitors for the purpose of giving delay of 500 μs. This delay time is to prevent other blocks from operating as soon as the power is turned on, while having the stabilization time of the LDO output. After the delay time, *OSC_EN_O* becomes high to operate the oscillator, and additionally 15 μs later, *POR_RSTB_O* is toggled to power up the analog blocks in the chip.

5.5 LOW DROPOUT REGULATOR (LDO)

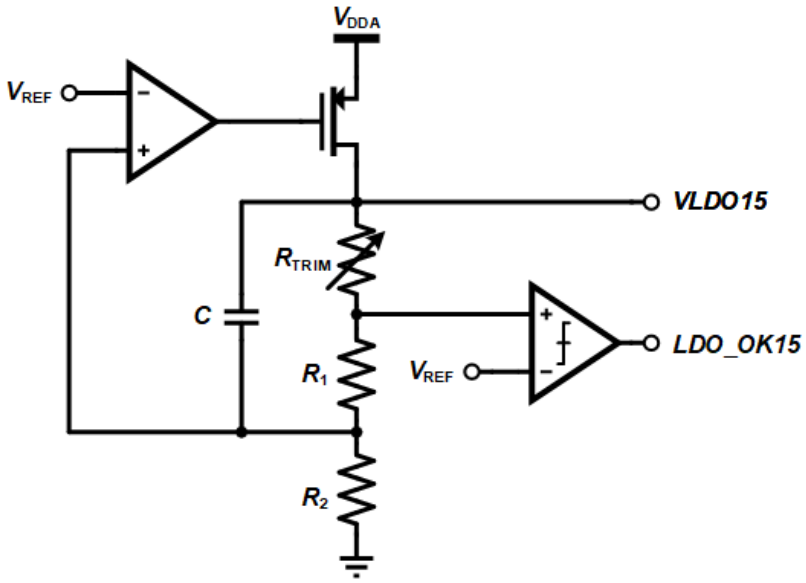


Fig.5.5.1.Block diagram of a low-dropout voltage regulator.

Fig.5.5.1 shows the block diagram of a low-dropout (LDO) voltage regulator. The function of the regulator is internal generation of 1.55 V for digital power supply voltage (VDDD). Target of the output voltage is 1.5 V, but it was set to 1.55 V, considering the voltage drop of practical issues such as the drop voltage of layout parasitic resistances and the printed circuit board (PCB) series resistance of a few mΩ. It has a 1 μF external capacitor for stability and uses 1.2 V voltage reference V_{REF} from a band-gap reference. 5-bits for digital trimming code is for controlling the output of the LDO by trimming the resistor R_{TRIM} in resistor divider. It includes an LDO_OK15 signal that is asserted once the output reaches 90% of its target value 1.55 V.

5.6 TEMPERATURE SENSOR

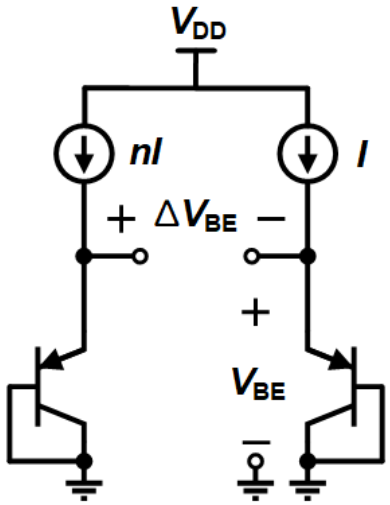


Fig.5.6.1. Block diagram of a bipolar core in temperature sensor.

Fig.5.6.1 is the block diagram of a bipolar core in temperature sensor. One diode-connected bipolar junction transistor (BJT) is fed a current I_{unit} through its emitter. Another identical diode-connected BJT is fed $n \cdot I_{unit}$ of a current through its emitter. The base-to-emitter voltage of the latter BJT is referred to as the complementary-to-absolute temperature (CTAT) voltage V_{BE}. The potential difference from the emitter of the latter BJT to the emitter of the former BJT is given by the equation as follows:

$$\Delta V_{BE} = \eta \frac{kT}{q} \ln n, \tag{5.6.1}$$

, ΔV_{BE} is the difference in base-emitter-voltages as shown in Fig.5.6.1 and is proportional to absolute temperature and is therefore referred to as the PTAT voltage. A bandgap reference can be created by first equalizing the magnitude of both the PTAT and CTAT's temperature coefficients, then adding the two voltage through analog circuitries. Since the absolute value of the PTAT voltage is smaller than that of the CTAT voltage, it is amplified by a factor of α. This results in a temperature-independent voltage V_{REF}, which is given by,

$$V_{REF}=V_{BE}+\alpha\cdot\Delta V_{BE}. \tag{5.6.2}$$

However, there is inevitable mismatch between devices during fabrication, which limit the accuracy of the bipolar core current ratio. Precise layout is not enough to reduce this mismatch. To solve this problem, dynamic-element matching (DEM) [5.6.1] is proposed in the bipolar core as shown in Fig.5.6.2. Unit elements are periodically and

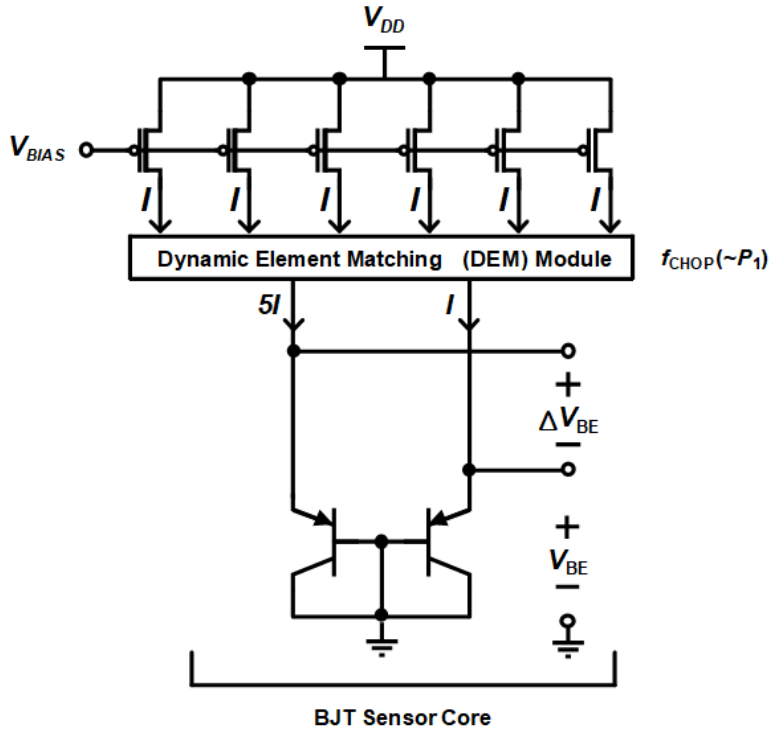


Fig.5.6.2. Block diagram of a dynamic-element matching [5.6.1].

randomly switched around, which causes mismatch errors to be averaged out. In order to dynamically match the current ratio n, one out of n+1 current sources is selected to provide I_{unit}, and the remaining n current sources combine to provide $n\cdot I_{\text{unit}}$. The unit current source providing I_{unit} is periodically alternated, thereby averaging out the ratio mismatch between the two branches. Redirection of the current is typically done with CMOS switches. Theoretically, the DEM control unit should randomly select one-unit source per delta-sigma ADC cycle; however, due to the complexity of such a circuit, it is typically implemented with a shift register instead.

An analog-to-digital converter can be used to convert the ration of $\alpha \cdot \Delta V_{BE}$ and V_{REF} into the following equation as follows:

$$\mu = \frac{\alpha \cdot \Delta V_{BE}}{V_{REF}}, \tag{5.6.3}$$

,which $\alpha \cdot \Delta V_{BE}$ is the input signal of the analog-to-digital converter and V_{REF} is used as the reference voltage of it. Lastly, the digital ratio μ can be used to obtain a digital temperature output D_{out} as follows by using (5.6.3):

$$D_{out} = A \cdot \mu - B, \tag{5.6.4}$$

where coefficients *A* and *B* are chosen to return a digital output in Celsius. Calculation of μ using V_{REF} requires a BGR circuit, which increase power consumption, and introduces an additional source of non-linearity. (5.6.3) can be modified as follows:

$$\mu = \frac{\alpha \cdot \Delta V_{BE}}{V_{REF}} = \frac{\frac{\alpha \cdot \Delta V_{BE}}{V_{BE}}}{\frac{V_{BE} + \alpha \cdot \Delta V_{BE}}{V_{BE}}} = \frac{\alpha Y}{1 + \alpha Y}, \tag{5.6.5}$$

where *Y* is defined as $\Delta V_{BE} / V_{BE}$. In (5.6.5), the variable *Y* removes the need for a dedicated BGR circuit to find μ, as V_{REF} is eliminated from the equation. Calculation of *Y* is done by using a delta-sigma ADC, with and as the ADC's input and reference voltage respectively.

Curvature of Y is straightened out through digital circuitry with the constant α.

To enhance the gain of ΔV_{BE}, we can use the chopping [5.6.2] between bipolar core and a delta-sigma modulator as shown in Fig.5.6.3 as input polarity swap. During the charge transfer or integration phase of the delta-sigma ADC, the input switches of the first integrator are typically opened. If the input switches are left closed, sampled charges stored in the input capacitors cannot move to the feedback capacitors. However, if the polarity of the input signal is reversed during the integration phase, the total charge transferred to the feedback capacitors is doubled. Also, sampling capacitors $2C_S$ [5.6.3] can be doubled to increase the total charged transferred during the integration phase. Changes in sampling capacitors do not influence the position of closed-loop poles of the delta-sigma ADC. A combination of both methods, which are input polarity swapping and adjustable sampling capacitors of the delta-sigma ADC, sets the total gain of 4, thus better utilizing the full-scale range of the delta-sigma ADC. The timing of the modular in the ADC are also shown in Fig.5.6.3. In order to use a reconfigurable delta-sigma modulator with pressure sensing, a third order cascade input feed-forward structure was used, and other integrators except for the first order integrator are the same as those for pressure sensor. However, the sampling frequency was set to 250 kHz instead of 4 MHz to reduce power consumption, unlike the case of pressure sensing.

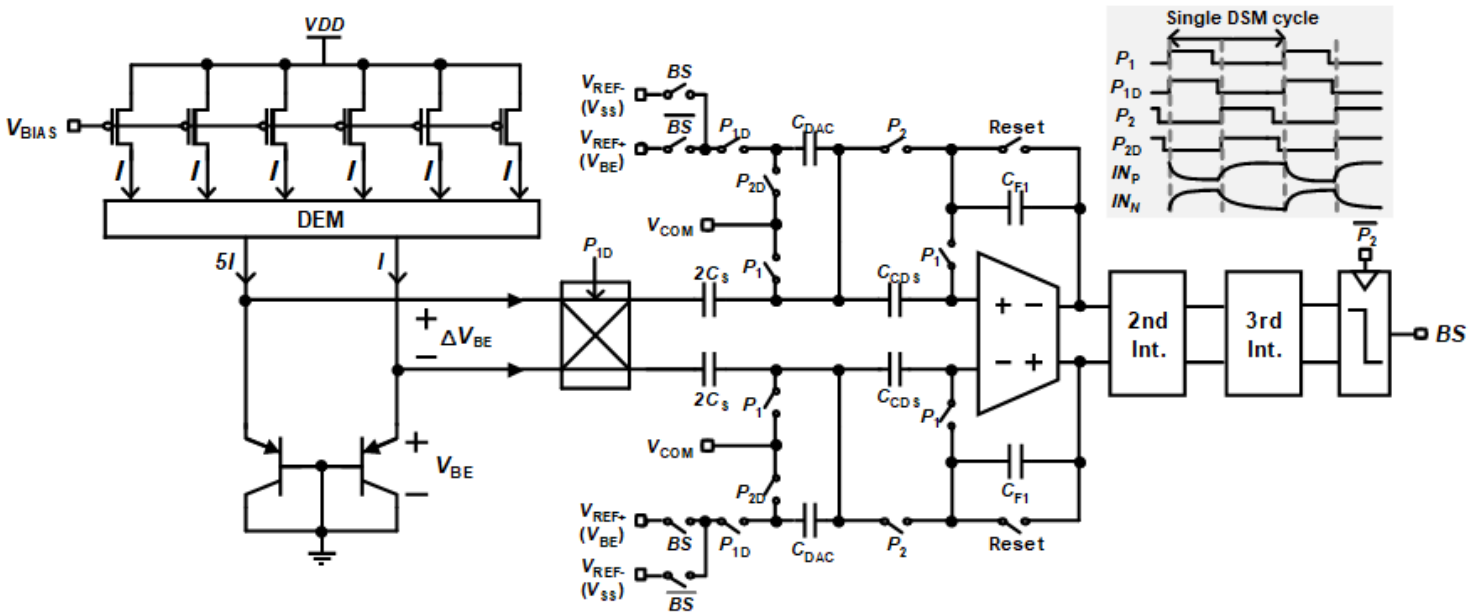


Fig.5.6.3. Schematic of the incremental ΔΣ modulator.

5.7 SENT INTERFACE

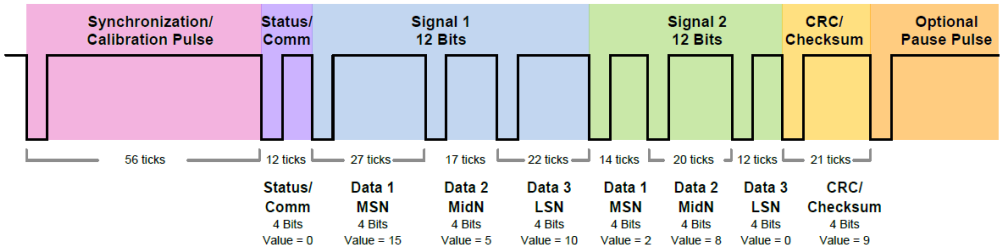


Fig.5.7.1. Typical channel message format of a SENT interface [5.7.1].

Fig.5.7.1 shows the typical single edge nibble transmission (SENT) interface protocol. It is a one-wire interface targeted for automotive applications. Users can interface with sensors used for applications such as pressure, mass airflow, and temperature. In normal operation, SENT module is waked up and the transceiver starts transmitting the SENT data. SENT is not limited to one data parameter per transmission and can use multiple usages for additional information, such as pressure, temperature, or other data. In Fig.5.7.1 [5.7.1], there are two 12-bit data, which are transmitted in each message frame. As long as the total bits of the two channels are 24-bits, it does not matter if the two channels are divided into different bits.

The basic unit of time for SENT is a tick, and the minimum data unit is a nibble for 4-bits data. When the transmission is start, the data goes from high to low and maintains this state for more than 5 ticks. In synchronization phase, this section is for checking the tick time in receiver. The time of the synchronization section is measured and divided by

56 ticks to calculate the time of 1 tick. The next section is the status section, which measures the time from a falling edge to the next falling edge, calculates how many ticks, and defines the value at this time as zero. After the section, the following data is decoded by table mapping to 4-bit data according to the number of ticks. Checksum section is used for error checking between the transmission part and the receiver. Optional pause pules is variable pause pulse, which can be used to maintain a uniform tick count or keep the number of ticks between received data constant.

CHAPTER 6

MEASUREMENT RESULTS

6.1 MEASUREMENT SUMMARY

The pressure sensor read-out system was designed and fabricated in a standard 0.13 μm CMOS process. Fig. 6.1.1 shows the measurement setup and a test board. An Agilent E3631A powers an external LDO to provide a supply voltage of 5 V and an external high-resolution digital-to-analog converter (DAC) provides a precise analog input to the read-out IC. Fig.6.1.2 show the chip microphotograph. The area of the read-out system, including CCIA, I-ADC, LDO, BGR, POR, oscillator, and digital circuits, is 5.264 mm^2. The total current consumption of the system is 1.76 mA. The CCIA and I-DSM occupy 1.54 mm^2 and consume 1.32 mA from the 5 V supply, at 13.2 kSPS output data-rate.

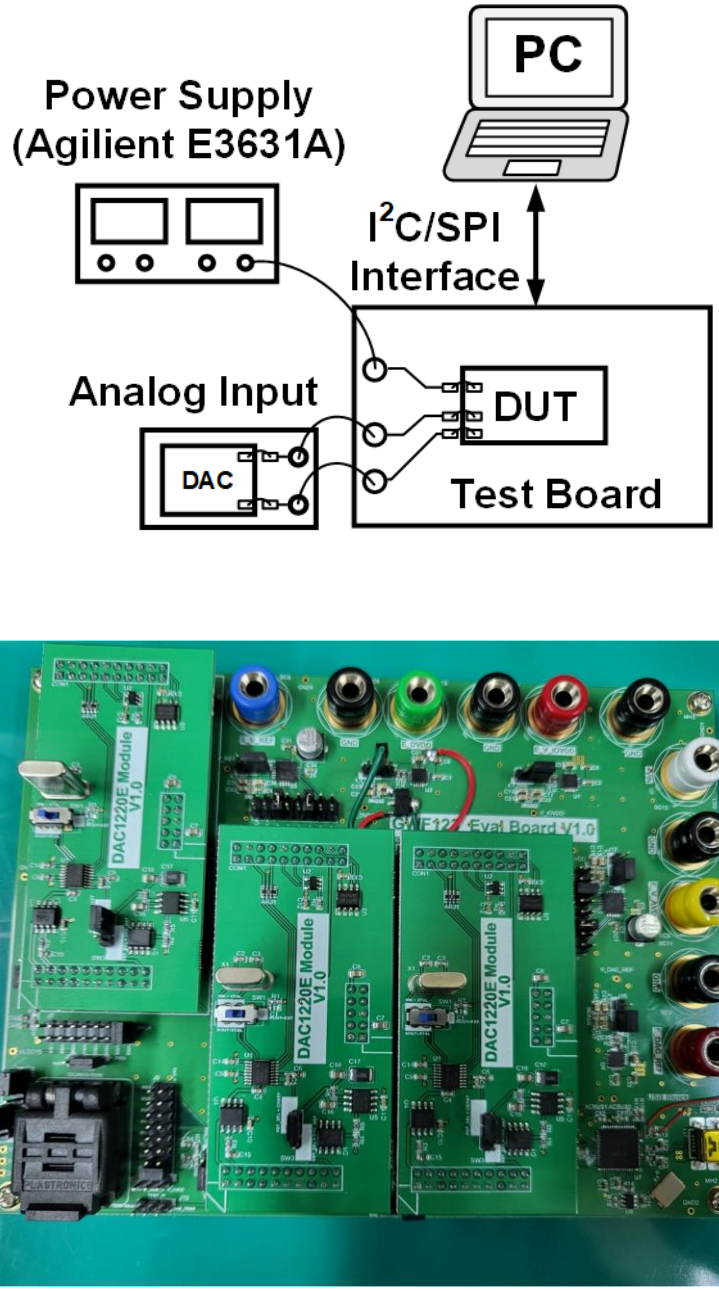


Fig.6.1.1. Measurement Setup and a test board for the read-out system.

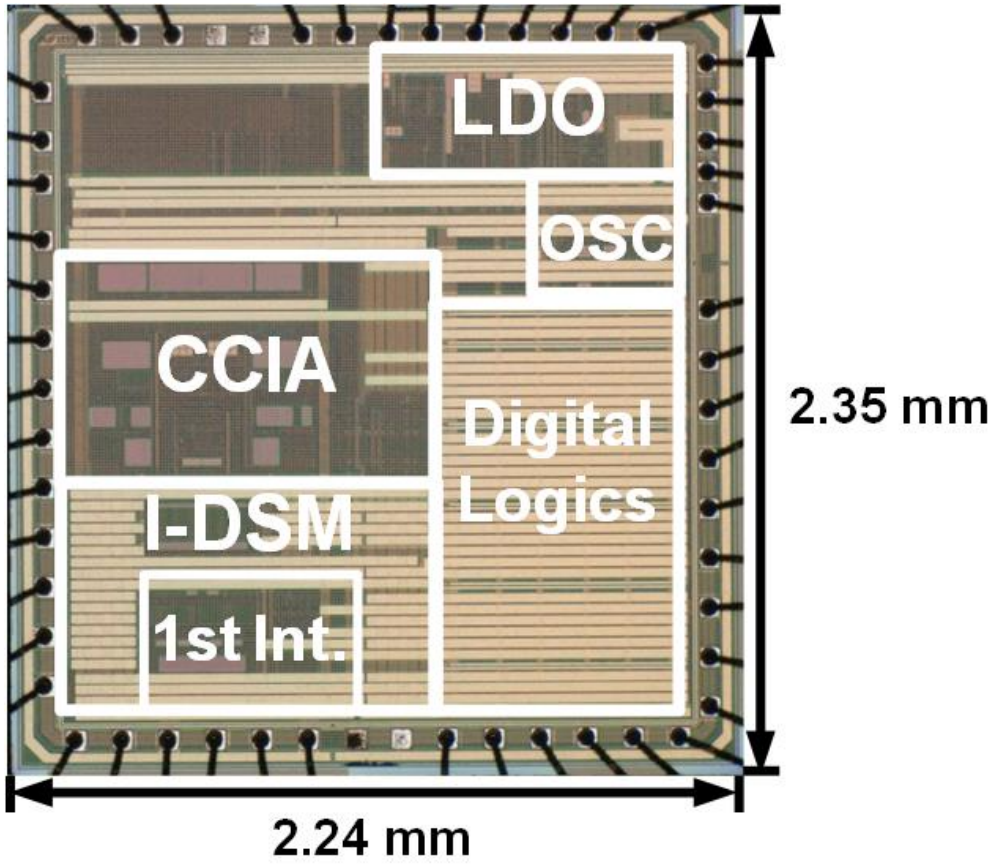


Fig.6.1.2. Chip microphotograph.

6.2 LINEARITY & NOISE MEASUREMENT

Fig. 6.2.1(a) shows that the measured output voltage of the read-out IC against the input voltage per full-scale range (FSR) applied at different CCIA gains and the FSR of the read-out IC is 4.8 V. Fig. 6.2.1(b) shows the measured output voltage against a fixed input voltage of 37.5 mV and the coefficient of determination (R^2) is 0.9999, showing the linearity of the read-out system with the FCCL depending on measured gains of 1, 8, 15.9, 63, 123. Fig. 6.2.2 shows the histograms of output voltages converted to 6000 digital output data, with a gain of 128 in CCIA and a data-rate of 13.2 kSPS and compared the input referred noise (IRN) of the read-out system with and without the proposed FCCL. Since the IRN is 2.4 μVrms for both cases, we can see that the additional FCCL circuits do not degrade the noise performance of the read-out system.

Fig.6.2.3 shows that the measured effective resolution against the gain of the CCIA with difference output data-rate. Effective resolution (ER) can be expressed as follows:

$$\mathrm{ER} = \log_2\left(\frac{\text{Full-scale output voltage range}}{\text{Standard deviation of output}}\right). \tag{6.2.1}$$

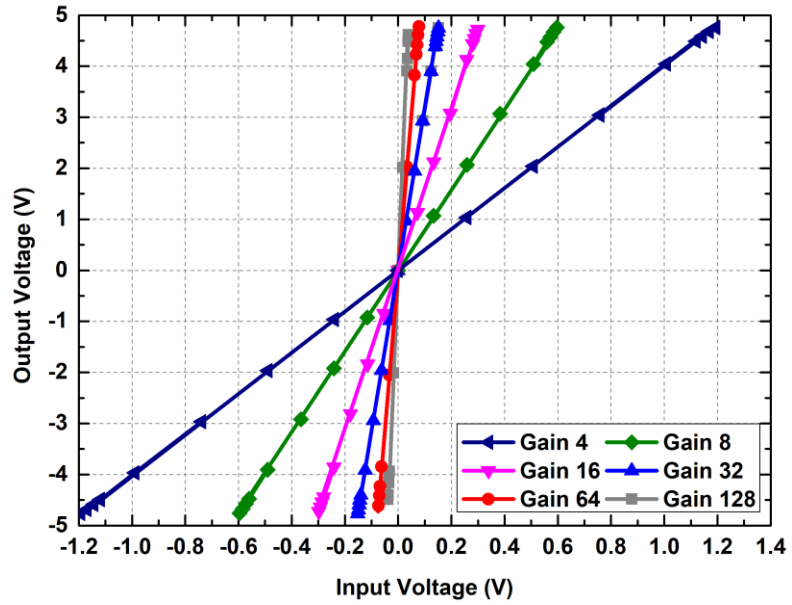
Each point in the figure was obtained by averaging 6,000 output data. When output data-

rate is 13.2 kSPS, the effective resolution is 18 bits at a gain of 1 and 15 bits at a gain of 128. As the gain of the CCIA increases, effective resolution decreases. If the output data-rate is 1/2 times, the over-sampling ratio of the I-ADC is doubled, which means 0.5-bit improvement from the ER point of view [4.2.1].

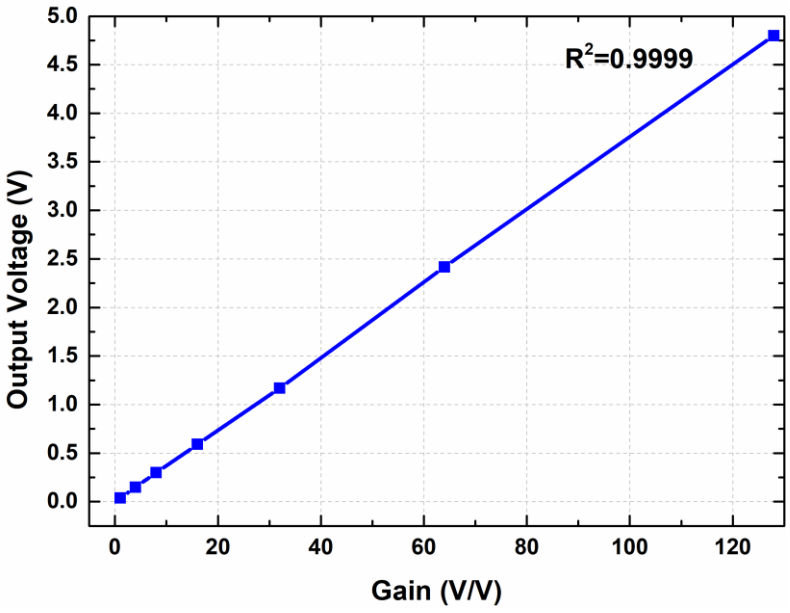
Fig.6.2.4 shows that the input referred noise against the gain of the CCIA with different output data-rate. Input referred noise can be expressed as follows:

$$\text{IRN} = \frac{\text{Full-scale output voltage range}}{\text{Standard deviation of output noise}/\text{CCIA gain}}, \qquad (6.2.2)$$

, where full-sale output voltage range is ± 4.8 V in this system. When output data-rate is 13.2 kSPS, the input referred noise is 38 μVrms at a gain of 1 and 2.4 μVrms at a gain of 128. As the gain of the CCIA increases, input referred noise decreases according to (6.2.2).

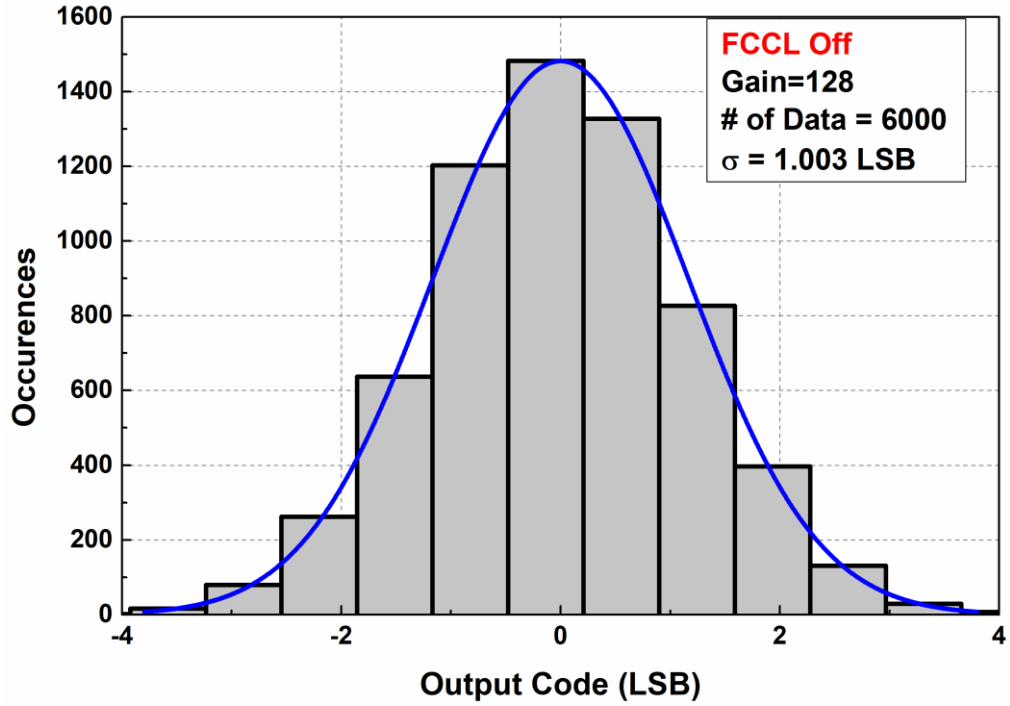


(a)

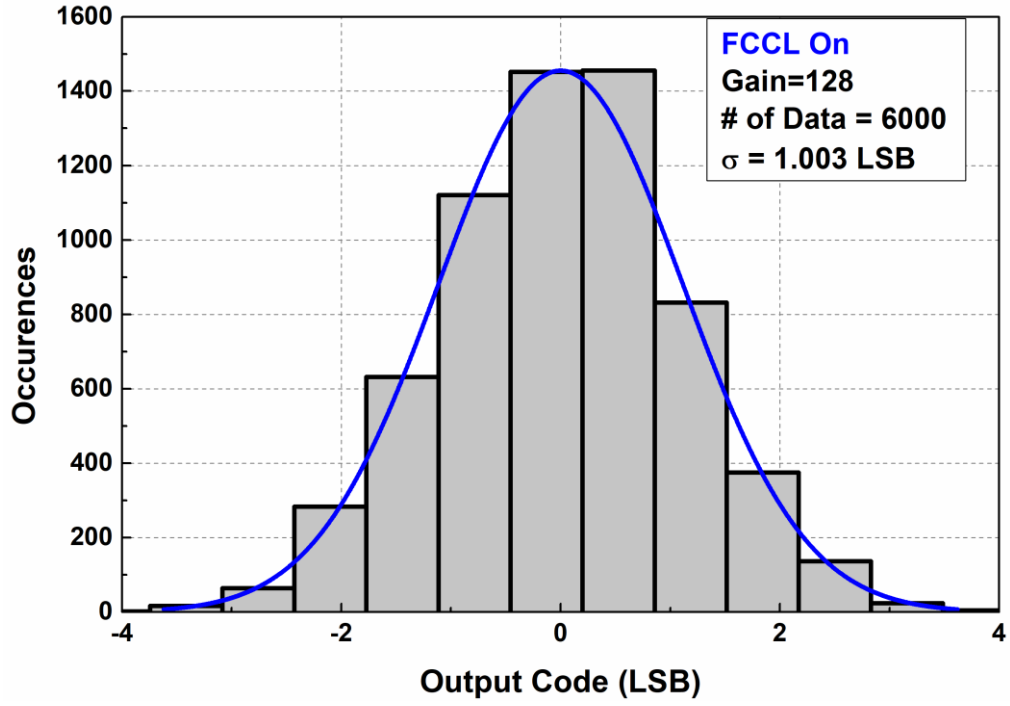


(b)

Fig.6.2.1. Measured output voltage of the read-out IC against (a) input voltage/FSR at different gains and (b) gain with a fixed input voltage of 37.5 mV.



(a)



(b)

Fig.6.2.2. Measured noise histograms of the read-out IC (a) without FIBL and (b) with FIBL at 13.2 kSPS.

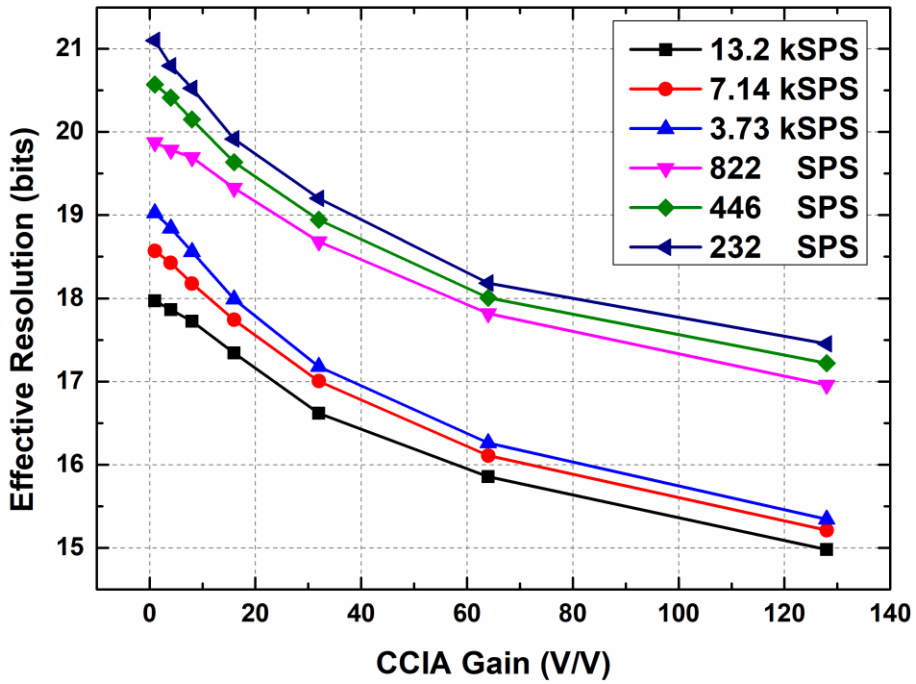


Fig.6.2.3. Measured effective resolution against the gain of CCIA.

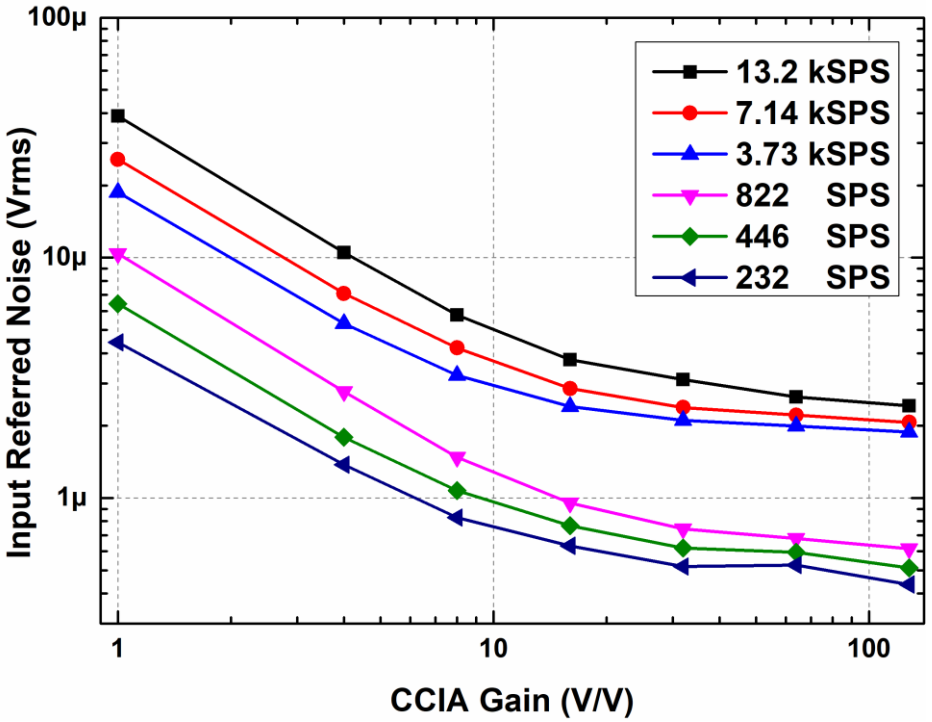


Fig.6.2.4. Measured input referred noise against the gain of CCIA.

6.3 SENSOR OFFSET CANCELLATION MEASUREMENT

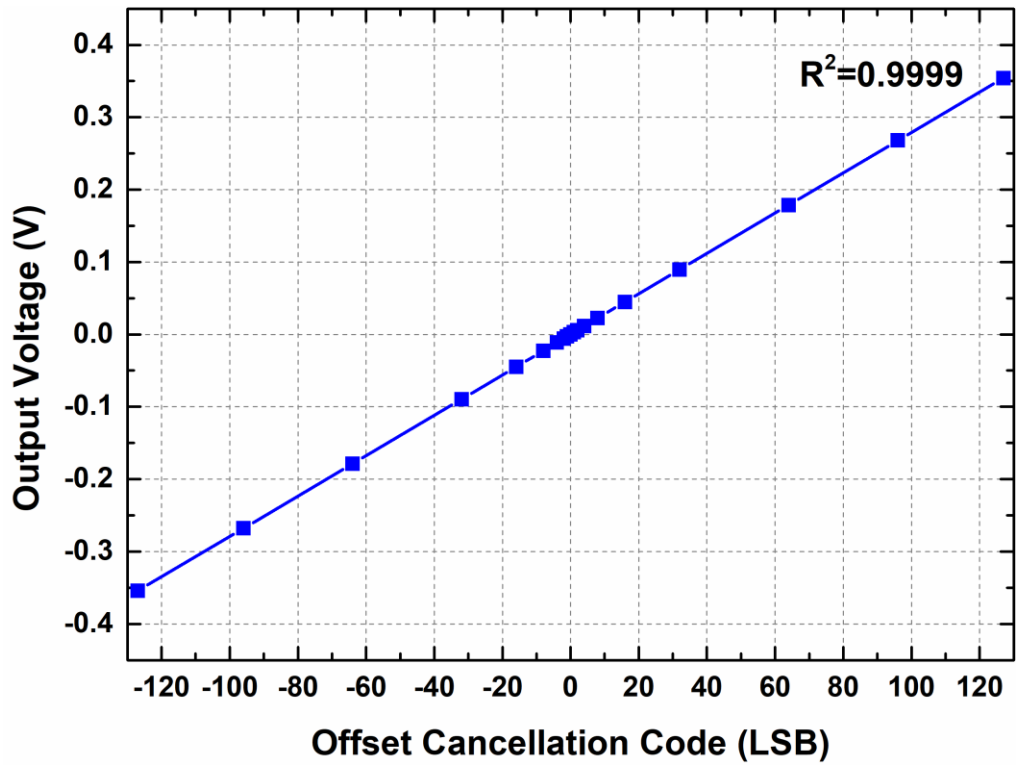


Fig.6.3.1. Measured output voltage of the read-out IC against offset cancellation codes.

Fig. 6.3.1 shows the measured output voltage of the read-out IC against the sensor offset cancellation codes that can be set to produce zero output voltage to maximize the read-out IC's dynamic range. The read-out IC can provide a sensor offset compensation range of ±350 mV with an 8-bit digital control.

6.4 INPUT IMPEDANCE MEASUREMENT

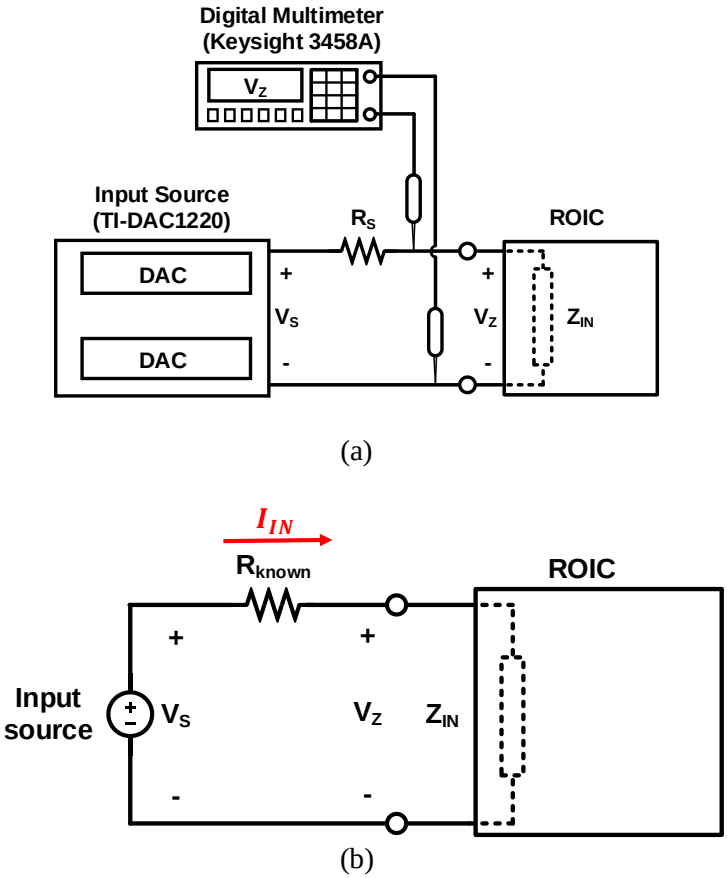
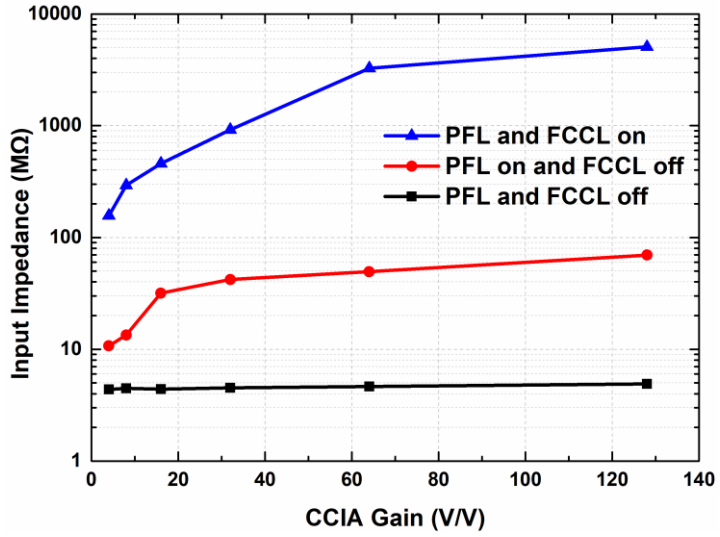


Fig.6.4.1. (a) Input impedance measurement setup and (b) measurement method.

Fig.6.4.1 shows the input impedance measurement setup and its measurement method. To measure the input impedance, 20-bit digital-to-analog coverers of TI 1220 are used and the input voltage V_S was set to 200 mV. To measure the input voltage V_Z of the chip,



(a)

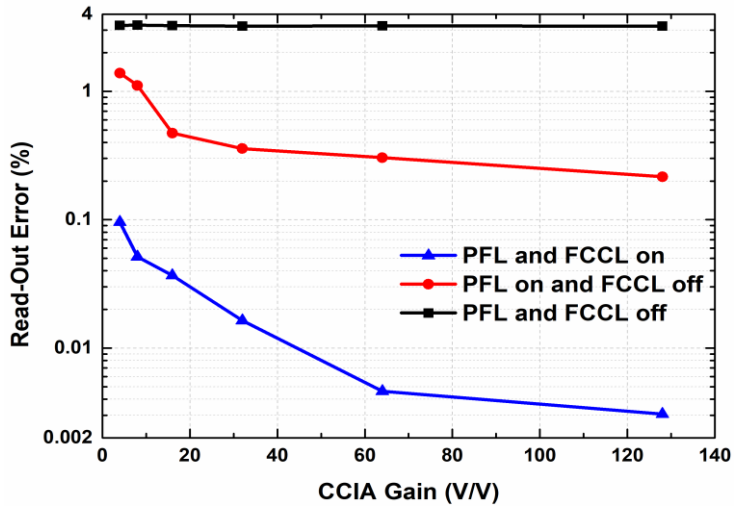


Fig.6.4.2. Measured (a) input impedance against CCIA gain and (b) read-out error against CCIA gain at a data-rate of 13.2 kSPS.

Keysight 3458A was used. The measurement was performed assuming that the DAC output and ROIC input leakage current were negligible. By using V_S, a known resistor of 150 kΩ R_S, and V_Z, Z_{IN} can be expressed as follows:

$$I_{IN}=\frac{V_S - V_Z}{R_S}, \tag{6.4.1}$$

$$Z_{IN}=\frac{V_Z}{I_{IN}}=\frac{V_Z}{\frac{V_S - V_Z}{R_S}}=\frac{V_Z}{V_S - V_Z} \times R_S. \tag{6.4.2}$$

Since the Keysight 3458A is 20-bit high precision digital multi-meter, we can calculate DC input impedance of the read-out system using (6.4.1) and (6.4.2). Fig. 6.4.2(a) shows the measured input impedance of the read-out IC by the CCIA gain according to the use of PFL and FCCL. When none of the boosting techniques is used, the measured input impedance is 4.4 MΩ in all gains. If the conventional PFL is only used, the maximum measured input impedance is 69 MΩ, and its IBF is 15.8. This shows that as the CCIA gain increases, the impedance boosting is limited by the parasitic capacitance C_P and does not increase with the CCIA gain. If the proposed FCCL is applied along with the PFL, the input impedance is 35 MΩ when the gain is four, and its IBF is 35. When the CCIA gain is 128, the input impedance is 5.1 GΩ, and its IBF is 1153. We can see that the proposed impedance boosting technique achieves a much higher IBF than the single PFL, regardless of the CCIA gain. Fig. 6.4.2(b) shows the measured read-out error against CCIA gain at a data-rate of 13.2 kSPS. When PFL and FCCL are off, the read-out error is constant at 3%, regardless of the CCIA gain. When only the PFL is on, the read-out error decreases according to the gain, but it does not reach 0.1%. However, when PFL and FCCL are on, it has a read-out error of 0.1% even at a low gain at 4, and when it is 128, it has a read-out error of 0.003%.

6.5 PERFORMANCE SUMMARY

Table 6.6.1 summarizes the performance of the proposed read-out system and compares it with that of other designs that use impedance boosting techniques. We compare these designs using an impedance boosting factor with input impedance, and a figure of merit (FoM) which is taking into account conversion time, power consumption, and signal-to-noise ratio (SNR). In the case of other works, the maximum input impedance Z_{IN} with impedance boosting is up to 1.6 GΩ [1.5.1], and the highest measured impedance boosting factor is 370 [6.5.1], but our work has a maximum input impedance of 5.1 GΩ and the measured impedance boosting factor is also 1153, which is higher than other works. This impedance boosting effect shows that our proposed FCCL is very effective in input impedance boosting, compared to other works given that our work has the shortest conversion time. Our read-out system achieves the highest IBF and input impedance in the shortest conversion time.

Table 6.6.1. Performance summary.

	[6.5.1]	[6.5.2]	[1.5.1]	[6.5.3]	**This Work**
Process (μm)	0.18	0.18	0.04	0.18	**0.13**
Supply (V)	1.8	1.8	1.2	1.8	**5.0 (A)** **1.55 (D)**
Conversion Time (ms)	3.3	5.0	5.0	1	**0.078**
Energy/Conversion (nJ/Conv)	23.3	16.2	12.0	418.1	**496**
IRN_{MIN} (μVrms)	0.225	0.65	1.8	0.61	**2.4**
Gain (V/V)	100	100	20	50	**1-128**
$Z_{IN,\,MAX}$ (Ω)	1.5 G	440 M	1.6 G	2.5 M	**5.1 G**
Measured IBF	370	88	76	6.25	**1153**
SNR_{MAX} (dB)	—	83.7	86.9	90.8	**106**
$FoM_{S,\,MAX}$ (dB)	—**	159.3	—**	151.6	**166.1**

* $FoM_{S,MAX} = SNR_{MAX}$ (dB) + 10log(1/(2 × Conversion time × Power)).
** Analog-to-digital converter is excluded.

CHAPTER 7

CONCLUSION

An energy-efficient high input impedance read-out system has been implemented in a standard 0.13 μm CMOS process. A combination of the FCCL and PFL boosts the inherently low input impedance of CCIA. The FCCL detects the output voltage of the CCIA and provides a fine feedback current that compensates for the input current, thereby successfully boosting the input impedance even at high CCIA gains. The current consumption of the FCCL circuit is only 1/24 of CCIA, which accounts for 2% of total power consumption and does not affect the overall system noise. An 18-bit I-DSM and a digital CoI filter provide high precision and fast conversion. System-level chopping and CDS techniques suppress low-frequency noise and offset. In the read-out system, power peripherals and internal temperature sensor are implemented. The prototype read-out system achieves an input impedance of 5.1 GΩ, an impedance boosting factor of 1153, and an IRN of 2.4 μVrms at a data- rate of 13.2 kSPS.

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한글초록

본 논문에서는 수백 옴에서 수 메가 옴까지 변할 수 있는 브리지 센서용 판독 시스템을 제안합니다. 제안된 시스템은 저잡음 에너지 효율적인 capacitively-coupled amplifier (CCIA)와 incremental delta-sigma 아날로그-디지털 변환기 (I-ADC)를 포함합니다. CCIA는 IA 토폴로지 중 하나의 증폭기를 사용하여 에너지 효율이 높은 IA 토폴로지이지만 다른 토폴로지에 비해 입력 임피던스가 낮습니다. 제안된 CCIA는 fine current compensation loop (FCCL)을 가지고 있어 positive-feedback loop (PFL)로 CCIA 입력 단자에서 보이는 전류를 작게 만듭니다. CCIA의 오프셋 및 1/*f* 잡음은 CCIA reset time으로 인해 correlated double sampling (CDS) 기술에 의해 억제됩니다. 잔류 저주파 잡음은 13.2kHz의 주파수로 시스템 레벨 차핑 기법에 의해 감소됩니다. 또한 브리지 센서의 저항 mismatch로 인한 센서 오프셋 전압을 상쇄하기 위해 센서 오프셋 제거 기법을 적용하였습니다. 18비트 I-ADC는 3차 cascaode-of-integrators (CoI) 필터로 4 MHz의 샘플링 클락으로 작동합니다. 프로토타입 칩은 전체 면적이 5.264 mm^2인 0.13 μm CMOS 프로세스로 제작되어 5V 전원에서 1.32 mA로 동작합니다. CCIA gain이 128이고 데이터 속도가 13.2 kSPS인 이 프로토타입은 전력 소비의 2%를 추가적으로 소비하면서 입력 임피던스를 부스팅 안했을 때에 비해 1153배인 5.1 GΩ으로 높일 수 있습니다. 4.8 V의 입력 범위 내에서 FCCL을 사용하는

것과 관계없이 ±350mV 센서 오프셋 전압 제거 및 2.4 μVrms 입력 참조 잡음을 제공합니다.

주요어 : 압력 센서, 브리지 센서, capacitively-coupled chopper instrumentation amplifier (CCIA), 입력 임피던스, 임피던스 부스팅, 1/*f* 잡음, 판독 시스템, system-level chopping, incremental delta-sigma analog-to-digital converter (ADC), 센서 오프셋 보상회로.

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